Manho Lee · Jun So Pak
Joungho Kim *Editors*

Electrical Design of Through Silicon Via

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To my beloved wife, Jeangeun Byun,
and my lovely daughter, Justine Kim,
who are the center of my universe,
for their never-ending love, support,
and understanding

—Joungho Kim

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Chapter 1
Introduction

Jun So Pak and Joungho Kim

Abstract TSV (Through Silicon Via) is now a key-technology in the mobile era because it can enable high-performance, hybrid, light-weight, small mobile devices with longer battery lifetimes and low manufacturing costs by reusing IP (intellectual property) and selecting optimized and high-yield, functional chips. This chapter discusses why TSV-based 3D ICs (3 dimensional integrated circuits) are a possible solution for future mobile devices from the perspective of exploiting advantages in their electrical designs. This chapter also provides a brief introduction to the electrical analysis of TSVs based on MIS (Metal-Insulator-Semiconductor) analyses.

Keywords Differential signal TSV · Equivalent circuit model · Single-ended signal TSV · Scalable model · TSV channel · 3D IC

1.1 TSV-Based 3D ICs

Employing high-performance, hybrid systems with small form factors and short design cycles has become the most important IC design approach for worldwide mobile devices. There are two approaches to satisfy the requirements of this approach. The first includes shrinking the transistor size (device scaling to continue to meet Moore's law), developing IC shrinkage technologies, and assembling

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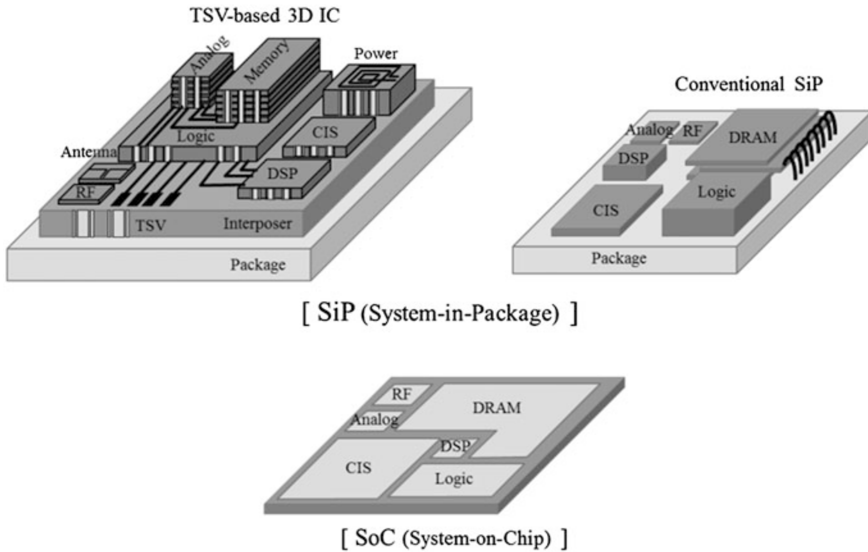

Fig. 1.1 System-in-package versus system-on-chip

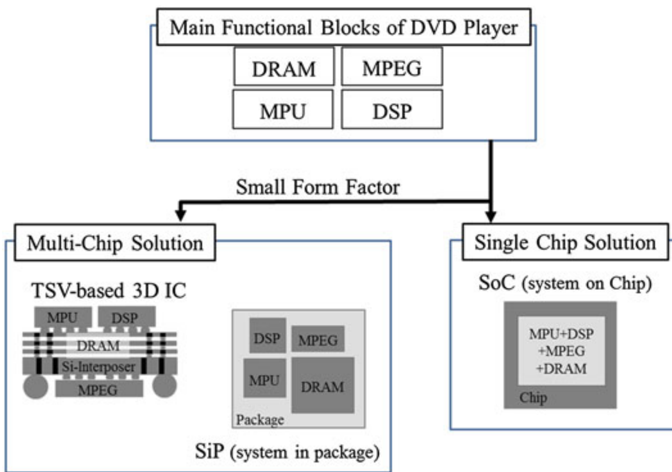

Fig. 1.2 A DVD player as an example of a high-performance system in a small form factor

ICs on a shrunken single chip, namely, the One Chip Solution (SoC, system-on-chip). The second approach includes securing KGDs (known good dies) to meet system functions and developing high-performance technologies for the interconnections between chips, namely, the Multi-Chip Solution (SiP, system-in-package), as shown in Fig. 1.1. For example, in Fig. 1.2, a conventional DVD player has four main functional blocks or chips, such as a DRAM, an MPEG, an

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MPU, and a DSP. To make the DVD player smaller, lighter, and portable, it should have a smaller case and a smaller main board embedded in the case. Of course, the main board must work better than the previous design. This requirement can be accomplished mainly by reducing the interconnection lengths between the blocks or chips with physical dimension matching, a capability that is easily understood by those who have seen any main board of any electric system and noted that the area occupied by the interconnections is much larger than that of the main functional blocks or chips and that the best way to reduce the physical size of the system is to control the area of the interconnections. However, because the interconnections are necessary for the operation of the DVD player, the number of interconnections on the main board cannot be reduced. Therefore, the SoC and SiP technologies, including the TSV-based 3D IC technology, were introduced to dramatically reduce the interconnection area. As shown in Fig. 1.2, the SoC and SiP approaches can achieve very short and narrow interconnections in a very small area. They also enable systems with high performance by inducing only small electrical parasitic losses at the interconnections. The parasitic electrical elements of interconnections are well known cause large signal distortion, long waiting times, and large interference.

In fact, during the past decade, SoC and SiP approaches have been competing with each other, and their advantages have been addressed [1–3]. SoC has several merits, such as high-speed and wide-bandwidth interconnections between functional blocks on a single chip and a small package size. Meanwhile, SiP achieves a low development cost by adopting KGDs and passive components, high flexibility regarding combined system functions, easy power management, small digital-to-analog coupling, and a short time to market. Of course, those two advantage groups have become weak points to each other. In Table 1.1, the pros and cons of SiP and SoC are listed and compared in detail. At first glance, SiP is more attractive than SoC because the pros of SiP are more numerous. However, the conventional SiP approach based on bond-wire technology has several critical weak points arising out of the inherent long length of the bond wires and bond-pad locations within the very limited area of the chip periphery. The long length and consequent large inductance of the wires and the limited number of bond-pads cause a narrow signal bandwidth and result in a low system speed. Additionally, the hook shape of the bond wires and the relatively large area required for chip-to-chip interconnections increase the package size in the vertical and horizontal directions.

To overcome the cons of conventional SiP technology, TSV-based 3D IC has been adopted by SiP technology as shown in Figs. 1.2 and 1.3. TSV is an abbreviation for "through silicon via," which is a metal pillar inside the silicon (Si) wafer with a silicon oxide coating ('liner') to block the DC leakage current between the metal pillar and the silicon wafer. The detailed structure of TSVs will be addressed in Fig. 1.12 of the Sect. 1.2. As mentioned in Fig. 1.3, TSV-based 3D IC technology has many interesting motivations. First, it increases the functional density in a limited area, for example, by allowing for a very small package and a very small system for current mobile applications without performance

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Table 1.1 Pros and Cons of the SiP and SoC approaches

	SiP		SoC	
Pros	Short time to market	Low development Cost	Highspeed interconnection	Wide bandwidth interconnection
	Small noise coupling	Easy optimized design (KGD)	High density functional blocks	Small size package
	High flexible functional block combination	Embed high Q passive component		
	Easy power Management			
Cons	Low speed interconnection	Narrow bandwidth interconnection	Long time to market	High development cost
	Large size package		High noise coupling	Difficult optimized design

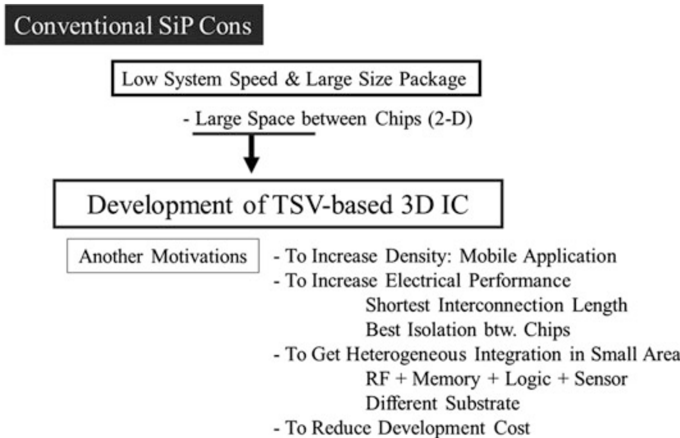

Fig. 1.3 The cons of conventional SiP overcome with TSV-based 3D IC

degradation or with enhanced performance. This great advantage is a consequence of the small TSV feature size and environment.

As shown in Fig. 1.4, the TSV length can be extremely short because it is the same as the silicon wafer thickness, and TSV enables multiple chips to be stacked vertically without off-chip supports such as bond wires. Consequently, TSV has a very small RC delay for signaling, a low impedance path for providing power through the power distribution network, and a consequent low power consumption. Additionally, heterogeneous integration is possible in a single very small SiP with the best isolation between chips or functional blocks. Of course, the performance of each block can be optimized by including optimal wafers, manufacturing technologies, and IPs. However, it is difficult to optimize SoC. Not all functional blocks need to be designed at the same time because it is not necessary for the

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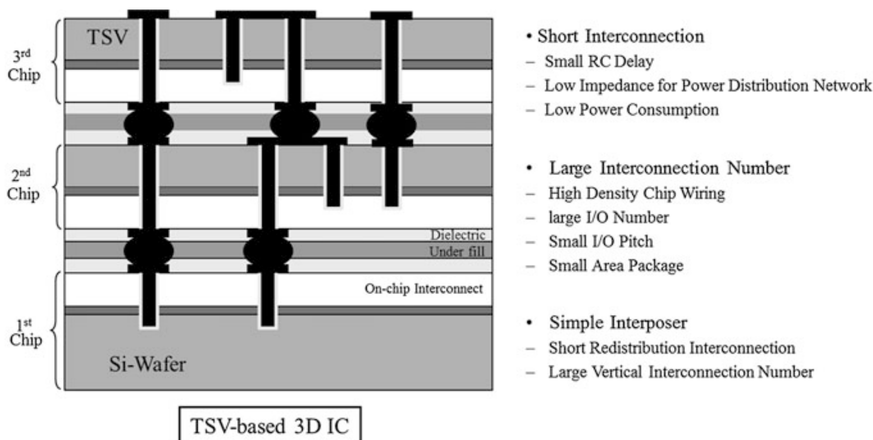

Fig. 1.4 The pros of TSV-based 3D IC

TSVs to be located in a designated area; specifically, there is flexibility to locate large number of chip-to-chip interconnections. This positional independency of TSV enables a small SiP to have high-density wiring with a large number of I/Os with a small pitch. Independently optimized functional blocks and chips can be easily stacked with a simple interposer. Finally, compared to SoC, TSV-based 3D IC can achieve lower a development cost by reusing IP, adopting well optimized KGDs, and especially by reducing time to market.

As shown in Fig. 1.5, three dimensional (3D) approaches continue to reduce manufacturing cost and follow Moore's law, even with the stacking of only two dies and without further development of shrinkage technologies. Figure 1.5 also implies that TSV-based 3D IC embedding of more than two dies can give further reduction of the manufacturing and development costs, which is of great benefit to current worldwide mobile devices.

It can be estimated that the previously mentioned advantages of TSV-based 3D IC in SiP technology will be of great benefit to industry and cause many system developers to dive into the growing the TSV-based 3D IC market, as shown in Fig. 1.6. Although the figure includes all 3D stacked chip package markets, the TSV-based 3D IC market will also grow exponentially for several decades in the future.

The TSV-based 3D IC industry began with homogeneous chip stacking to increase the chip density. (The first and second stages of Fig. 1.7) A good example is an application to memory chips [3]. As is well known, most systems have a data processing chip (i.e., logic) and memory chips (i.e., DRAM) for containing and processing data. When a system has a small memory density, it is difficult to enhance the system performance without increasing the channel signaling speed between the data processing chip and the memory chips. Increasing the channel signaling speed without adopting a new physical design induces several electrical

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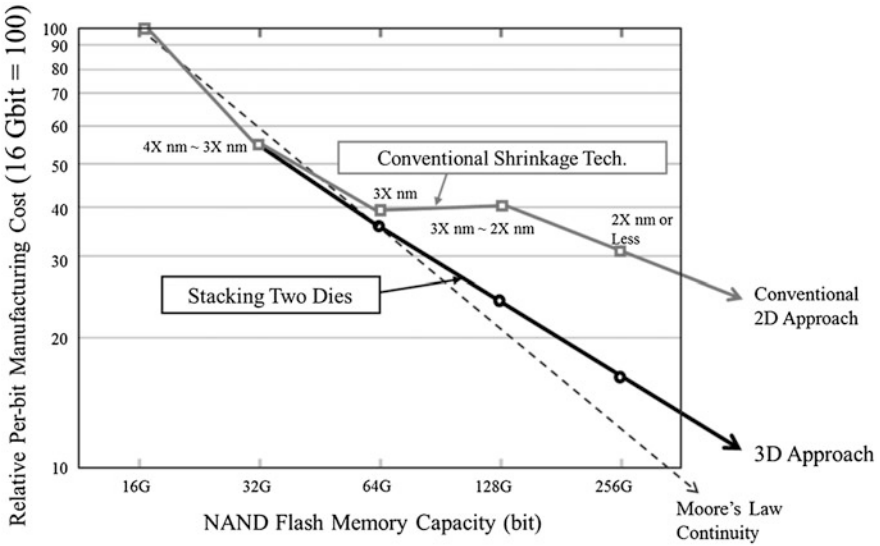

Fig. 1.5 3D stacked chip versus shrinkage technologies for cost reduction through chip density increment [1]

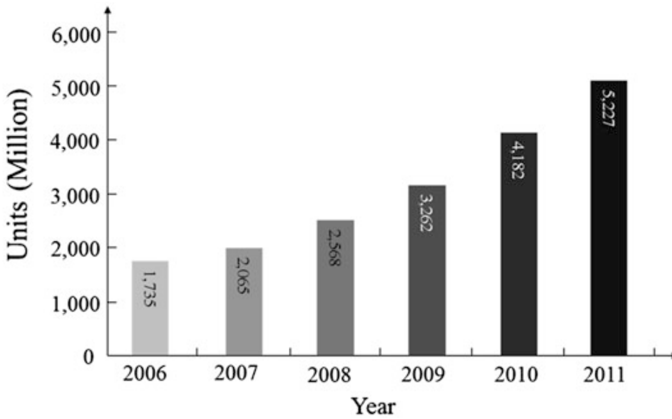

Fig. 1.6 The 3D stacked Chip SiP annual growth estimation [2]

problems, such as signal degradation and channel interference, as well as power consumption problems, such as a lack of power budget and a short battery lifetime. Therefore, to achieve a system with high performance, low interference, and low power consumption, the system should be designed to maintain a low channel signaling speed, to increase the number of channels, and to decrease the distance between the data processing chip and the memory chips. Of course, these design criteria are very helpful for the design of systems with a small physical size, such

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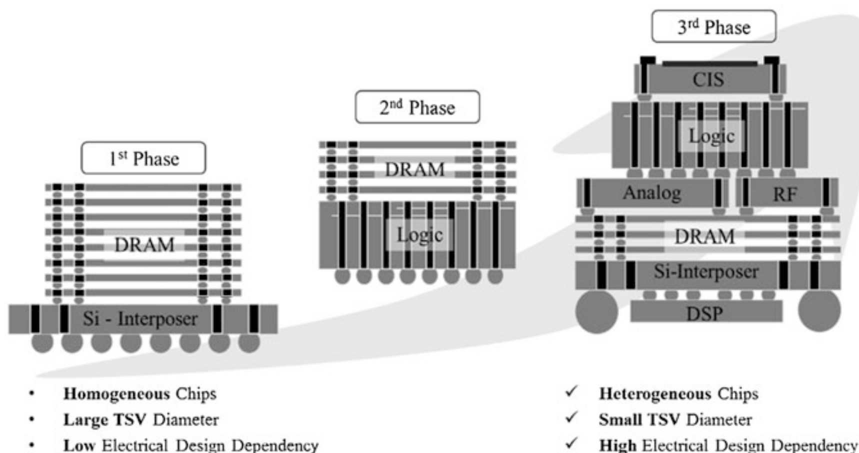

Fig. 1.7 The future roadmap of TSV-based 3D IC

as mobile devices. As shown above, it is very clear that TSV-based 3D IC will be the most important technology for future mobile devices. The final application of TSV-based 3D ICs is a real SiP, as shown in the third stage of Fig. 1.7. All functional blocks and chips are connected by TSVs and embedded in a single package. Because all the signals are transmitted through very short and small TSVs, low interference and low power consumption can be achieved while maintaining high system performance.

1.2 Core Technologies and Electrical Reliability Design for TSV-Based 3D IC

There are many core technologies for the realization of TSV-based 3D IC, as shown in Fig. 1.8. The first design technology is that of reliability analysis of electrical and thermal/mechanical fields. Because TSV is a relatively larger on-chip structure than those of transistor and on-chip wirings, thermal/mechanical reliability analysis has been conducted at the beginning stage of TSV research. However, the state of the art TSV technology will exhibit sub-micrometer-diameter TSVs, and the thermal/mechanical reliability of TSVs is no longer a critical design issue. However, thermal/mechanical reliability analysis should be completed in the case of chip stacking and chip bonding. Therefore, the recent reliability analysis of TSV itself is focused tightly on electrical reliability because, as mentioned above, TSV-based 3D IC technology is moving towards the goal of mixed-mode systems including analog and RF chips and very noisy digital chips. It is very well known that analog and RF chips suffer greatly from digital noise. Therefore, electrical reliability issues for TSV-based 3D IC of Fig. 1.9 are very

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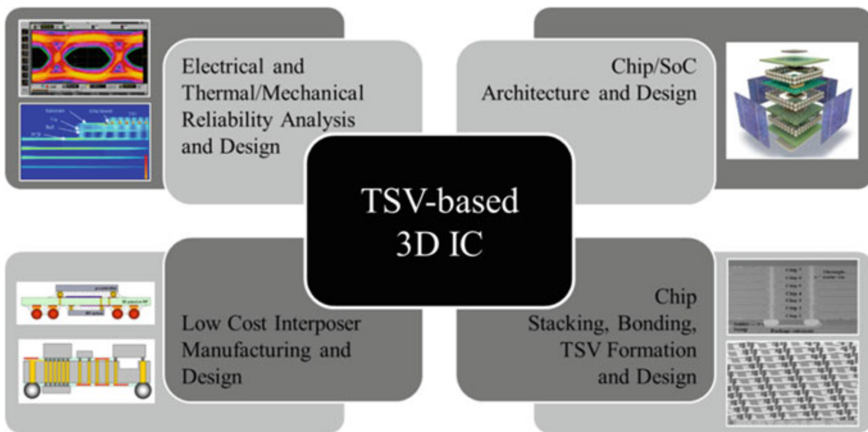

Fig. 1.8 The core technologies for TSV-based 3D IC

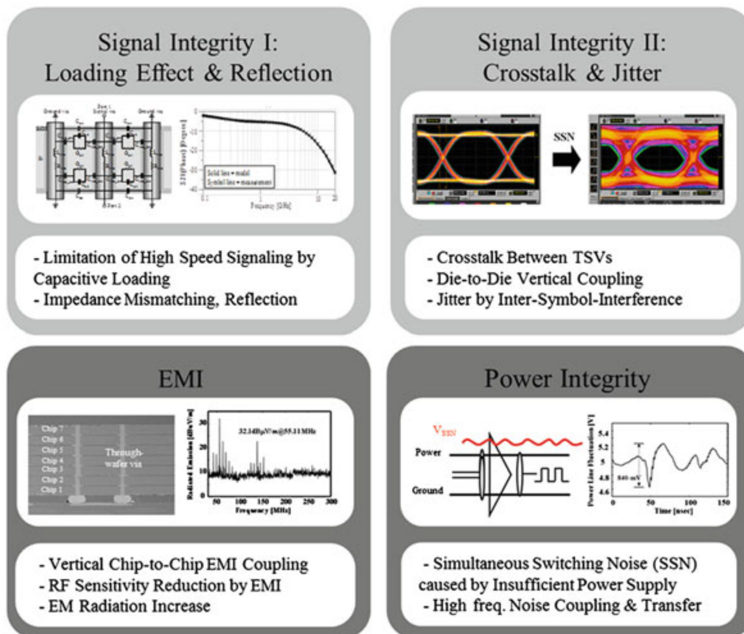

Fig. 1.9 Electrical reliability design issues for TSV-based 3D IC

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important. These issues can be classified as signal integrity (SI) design issues, such as the loading effect and reflection from large capacitive TSVs and crosstalk and jitter that result from the conductive silicon substrate, EMI (electromagnetic interference) issues that cause malfunctions of analog and RF chips, and power integrity (PI) design issues that arise from high chip densities and the consequent high current density in the TSVs. These electrical reliability design issues are covered in later chapters of this book.

Other core technologies are the chip/SoC architecture, chip stacking, bonding, TSV formation, and low-cost interposer manufacturing. Those are also very critical technologies; however, because they are beyond the scope of this book, the details are not covered.

1.3 Electrical Analysis of TSVs Based on MIS Analysis

1.3.1 Introduction of MIS Analysis for TSV Electrical Behavior

MIS (Metal-Insulator-Semiconductor) analysis may be an unusual way to analyze signal channels in the digital device world. However, MIS analysis is a conventional method for the analysis of the electrical behavior of signal lines on semiconductor wafers [4]. Therefore, to analyze TSV electrical behavior, MIS analysis should be applied because TSV is formed inside silicon, which is a typical semiconductor.

First, MIS analysis will be addressed. When a metal line is formed on a semiconductor or silicon (Si) wafer for signaling between two nodes, an insulator or silicon dioxide (SiO_2) layer should be inserted between the metal line and the semiconductor layer for blocking DC leakage current, as shown in Fig. 1.10. It is assumed that the back (or bottom) surface of the semiconductor wafer is metallized to serve as the reference for the metal line. In this situation, the surface between the Si and SiO_2 should be considered. Because Si has a finite resistance or conductance and SiO_2 is very close to a pure dielectric material, there is an impedance mismatch when the electrical field and the magnetic field pass through the surface. Additionally, because the SiO2 is usually very thin, the surface is very close to the metal line. Consequently, the electric and magnetic fields induced by a current and a voltage on the metal line have near-field characteristics. In the near-field range, the electric field has very high wave impedance of a few kiloohms while magnetic field has very low wave impedance of a few tens of ohms [5].

Therefore, the electric field feels a large impedance mismatch at the bottom surface of the SiO_2, and most of the field is reflected back. An additional reflection occurs at the top surface of the SiO_2, as shown in Fig. 1.11. Consequently, the electric field is trapped inside the SiO_2 and induces a very large capacitance. In contrast, the magnetic field does not have an impedance mismatch at the same

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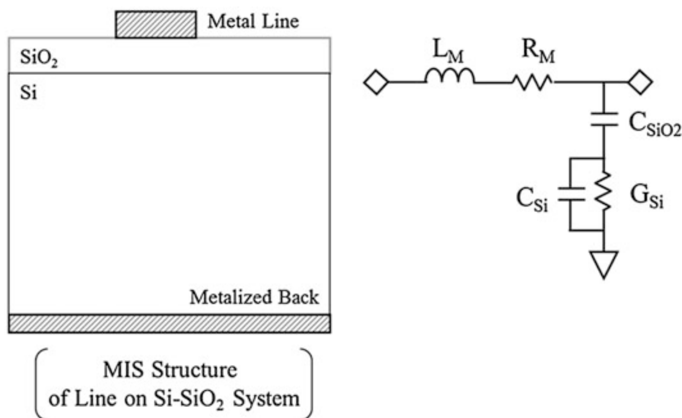

Fig. 1.10 An MIS (metal-insulator-semiconductor) structure and lumped circuit model [4, 6] © 1990, 2011 IEEE

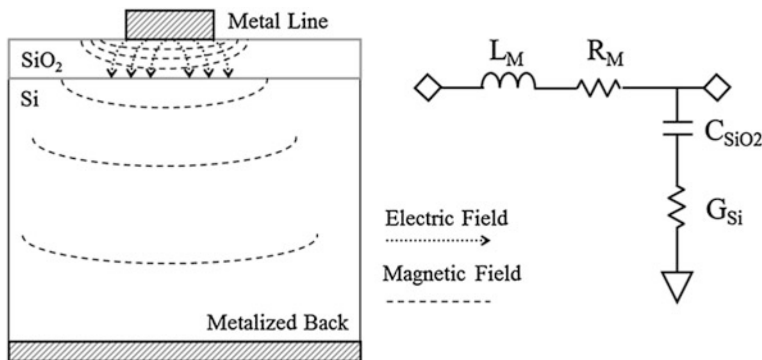

Fig. 1.11 The electromagnetic field distribution and the lumped circuit model of a slow-wave mode in an MIS structure

surface and can reach the metalized back. Finally, a signal on an MIS structure feels a very large capacitance and becomes slower than in a pure dielectric material. This signal condition is called a 'Slow Wave Mode' in this aspect of MIS analysis. Of course, the slow wave mode is very strongly dependent on the semiconductor resistivity and the signal frequency, as shown in Fig. 1.12. As the resistivity reaches a high value or the electrical characteristics of the semiconductor move toward those of a pure dielectric material, the phenomenon of the slow wave mode disappears in the low frequency range. The end of this range is called the 'dielectric relaxation frequency, f_e', which refers to the boundary of the 'slow wave mode' and the 'dielectric quasi-TEM mode' [4, 6]. Here, there is another type of a dielectric quasi-TEM mode. A dielectric quasi-TEM mode usually appears in a higher frequency range than a slow wave mode does because the dopant in the semiconductor cannot react in the higher frequency range, and

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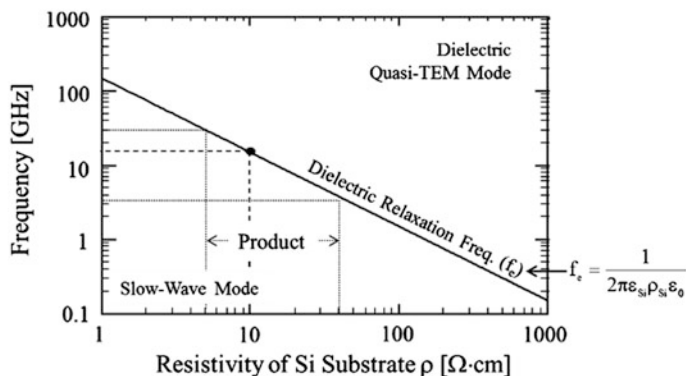

Fig. 1.12 Resistivity-frequency domain chart and dielectric relaxation Freq (f_e) [4] © 1990 IEEE

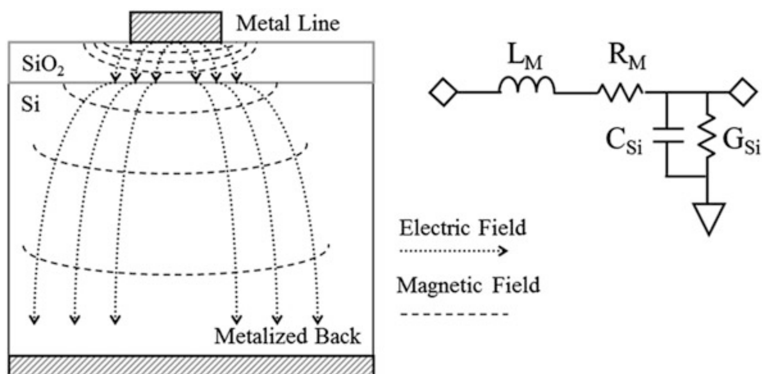

Fig. 1.13 Electromagnetic field distribution and lumped circuit model of dielectric quasi-TEM mode in MIS structure

the semiconductor acts as a pure dielectric material. Consequently there is no more impedance mismatch at the interface between the insulator and the semiconductor, as shown in Fig. 1.13. In the current semiconductor industry, the resistivity of semiconductors or silicon wafers generally used for products is in range from 5 to 40 Ω cm, and the slow wave mode and the large capacitive characteristics of a metal line begin at 30 and 3.5 GHz, respectively. Considering the 10 Ω cm resistivity of the most widely used silicon wafers, a signal on a metal line can suffer from a slow wave mode at frequencies up to 15 GHz by experiencing an increased delay, inter-symbol interference, and coupling to other metal lines. Considering the third harmonic frequency of a signal, 15 GHz can include the spectrum up to a 10 Gbps signal, and thus most signals on silicon wafers in current products are affected by a slow wave mode.

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These slow wave and dielectric quasi-TEM modes can be easily modeled by lumped circuit components such as R (resistance), L (inductance), C (capacitance), and G (conductance), as shown in Figs. 1.11 and 1.13 [4, 6]. A metal line and its reference, consisting of the metalized back, can be modeled with series R_M and L_M. The only difference is the addition of a shunt C and G. In the slow wave mode, as mentioned above, the electric field captured inside the SiO_2 can be modeled by C_{SiO_2} connected in series to G_{Si}, which is induced by the magnetic field and the resistivity inside the silicon. Because there is a very small effect of the electric field in the silicon, the capacitance C_{Si} can be negligible. For the dielectric quasi-TEM mode, because the frequency range is relatively high, the impedance of C_{SiO_2} is very small, and the electric field strongly penetrates the silicon; thus, the shunt-connected C_{Si} and G_{Si} appear.

Here, it should be additionally considered that most current products with chips use a digital signaling scheme, and the digital signal has a very wide bandwidth, i.e., from DC to greater than 10 GHz. Therefore, any channel analysis of chips based on MIS-structured metal lines cannot be separated into two modes because the signal on a channel is affected by two modes at the same time. Therefore, two modes are modeled with a single lumped circuit model for channel analysis of chips. Then, the remaining problem is how to combine the models of the two modes; however, this is not a significant problem when the capacitance is on the order of C_{SiO2} and C_{Si}. Usually, the capacitance of C_{SiO2} is 100–1000 times larger than that of C_{Si}, i.e., the capacitances of C_{SiO2} and C_{Si} are in the range of pF and fF, respectively. The exact value will be addressed in the next section of TSV analysis. Now, we must revisit the lumped circuit model of Fig. 1.10. There are three elements, C_{SiO2}, C_{Si}, and G_{Si}, in the shunt part of the metal line. In the low frequency range and the slow wave mode, the impedance of C_{Si} is so large that C_{Si} is regarded as an open circuit. In this case, the model of Fig. 1.10 is the same as that of Fig. 1.11. In the high frequency range and the dielectric quasi-TEM mode, the impedance of C_{Si} becomes so small that C_{Si} is regarded as a short circuit. Then, the model of Fig. 1.10 becomes the same as that of Fig. 1.12. Therefore, the model of Fig. 1.10 for the MIS structured metal line represents both the slow wave mode and the dielectric quasi-TEM mode at the same time. Additionally, the model can show the transition between the two modes in the middle frequency range. This is a very important result because the two modes cannot be separated discretely at the dielectric relaxation frequency. A continuous change between the two modes occurs naturally in the real world.

Based on the MIS analysis of the previous paragraphs, TSV electrical behavior can be explained because a TSV has the shape in Fig. 1.14, which shows a metal pillar for the signal path, a thin SiO_2 insulator surrounding the metal pillar to block DC leakage from the metal pillar to the silicon wafer. The figure also shows a silicon wafer embedding metal pillars and SiO_2 insulators and two TSVs, i.e., an S/G TSV pair. The S/G TSV pair has a double-sided MIS structure: M (metal pillar for signal TSV)—I (SiO_2 insulator for signal TSV)—S (silicon between two TSVs)—I (SiO_2 insulator for ground TSV)—M (metal pillar for ground TSV). In the next section, the electrical analysis of TSVs based on MIS analysis is addressed [6].

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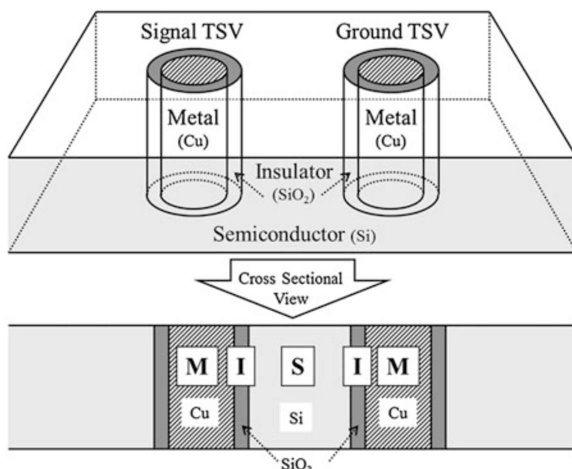

Fig. 1.14 Double sided MIS structure of signal and ground TSV pair [6, 7] © 2010, 2011 IEEE

1.3.2 *Model Extraction of S/G TSV Pair Based on MIS Analysis and Model*

Now, we know what phenomena occur in a MIS structure. Additionally, we can guess what electric behavior will occur in an S/G TSV pair, and the behavior will be very similar to that of an MIS structure, with the existence of a slow wave mode and a dielectric quasi-TEM mode [6]. Additionally, the model of an S/G TSV pair looks like that of an MIS structure because, as mentioned in the last paragraph of Sect. 1.3.1, the structure of an S/G TSV pair is regarded as a double-sided MIS structure (an MISIM structure).

In this section, we address a model of an S/G TSV pair. Before beginning the extraction of the model, the dimensional parameters of the S/G TSV pair structure should be defined, as shown in Fig. 1.15. The diameter and length of the TSV pillar are denoted by TD and TL, respectively. The pitch of the two TSV pillars is TP. The thickness of the SiO_2 insulator is TT. The model of the S/G TSV pair can be constructed as shown in Fig. 1.16 by following the model of the MIS structure in Fig. 1.10. The lumped circuit components in Fig. 1.16 are defined as the resistance (R_T), the partial inductance (L_T), the partial self inductance (L_{ST}), and the partial mutual inductance (L_{MT}) of the TSV pillars, the resistance (R_{Si}) and the capacitance (C_{Si}) from the silicon conductivity, and the capacitance (C_{SiO2}) from the SiO_2 insulator and the slow wave mode. If you fold this model along a vertical virtual line at the middle, the constructed model of an S/G TSV pair is exactly the same as the model of Fig. 1.10 [7].

The next step in the model extraction is to determine how to calculate or obtain the values of the lumped circuit components. For this approach, it is necessary to examine the shape of the S/G TSV pair to find the closest shapes whose electrical analyses and analytic equations have been well defined. First, the structure of two

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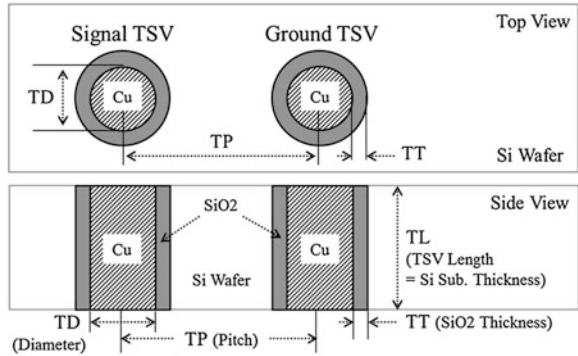

Fig. 1.15 Dimensional parameters of an S/G TSV pair for Eqs. (1.1)–(1.5) [6, 7] © 2010, 2011 IEEE

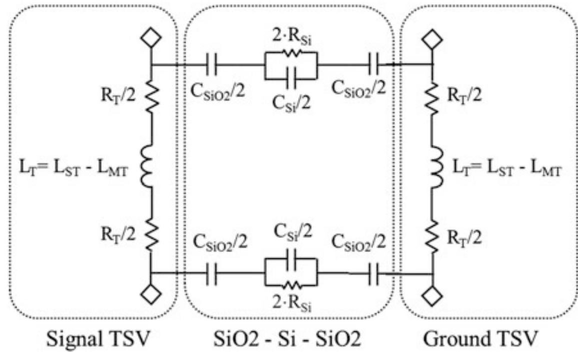

Fig. 1.16 Lumped circuit model of S/G TSV pair [6, 7] © 2010, 2011 IEEE

TSV pillars is very similar to a two-wire transmission line, and R_T, R_{Si}, and C_{Si} can be easily obtained by using Eqs. (1.1) (1.2), and (1.3) [8]. To obtain the partial inductances of the finite length of the TSV pillars, Eq. (1.4) can be used [9]. Finally, a single TSV pillar surrounded by a thin SiO_2 insulator and silicon can be regarded as a coaxial transmission line when the silicon wafer is in the slow wave mode and acts as metal. Then, C_{SiO2} can be calculated from Eq. (1.5) [8].

$$\mathrm{R}_T = \frac{TL}{\sigma_{Cu} \cdot \pi \cdot (TD/2)^2} \cdot \sqrt{1 + Cor. \cdot freq}\ [\Omega/\mathrm{TSV}] \tag{1.1}$$

$$R_{Si} = \frac{\varepsilon_{r_Si} \cdot \varepsilon_0 \cdot \rho_{Si}}{100 \cdot C_{Si}} = \frac{1}{G_{Si}}\ [\Omega/(\mathrm{S/G\ TSV\ Pair})] \tag{1.2}$$

$$C_{Si} = \frac{\varepsilon_{r_Si} \cdot \varepsilon_0 \cdot \pi \cdot TL}{ln\left(\frac{TP}{TD} + \sqrt{\left(\frac{TP}{TD}\right)^2 - 1}\right)}\ [\mathrm{F/(S/G\ TSV\ Pair)}] \tag{1.3}$$

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Table 1.2 Typical values of S/G TSV pair model parameters of Fig. 1.16 [7] © 2011 IEEE

RRS/GTSV model parameters		Rr (mΩ) @ 1 GHz	L_{ST} (pH)	L_{MT} (pH)	C_{SiO2} (pF)	C_{Si} (fF)	R_{Si} (Ω) = 1/G_{Si}
TD/TL/TI (μm)	TP (μm)						
30/100/0.5	100	12.44	32	9.4	0.65	19.1	552
	150			6.5		15	701

Copper TSV (Cu; $\sigma_{cu} = 5.8 \times 10^8$ S/m) formed in Si Wafer ($\rho_{Si} = 10$ Ω·cm)

$$L_T = L_{ST} - L_{MT} \ [\mathrm{H/TSV}] \ L_{ST} = \frac{\mu_0 \cdot TL}{2\pi} \cdot \left[\ln\left(\frac{2 \cdot TL}{TD/2}\right) - \frac{3}{4}\right]$$

$$L_{MT} = \frac{\mu_0 \cdot TL}{2\pi} \cdot \left[\ln\left(\frac{TL}{TP} + \sqrt{1 + \left(\frac{TL}{TP}\right)^2}\right) - \sqrt{1 + \left(\frac{TP}{TL}\right)^2} + \frac{TP}{TL}\right] \tag{1.4}$$

$$C_{SiO2} = \frac{2\pi \cdot \varepsilon_{r_SiO2} \cdot \varepsilon_0 \cdot TL}{ln\left(\frac{TD/2+TT}{TD/2}\right)} \ [\mathrm{F/TSV}]. \tag{1.5}$$

Cu is the conductivity of copper (5.8×10^8 S/m), Cor. (Eq. 1.1) is the correction factor for the skin depth effect, 'freq' is the frequency in Hz, μ_0 and ε_0 are the permeability and the permittivity of free space ($4\pi \times 10^{-7}$ H/m, 8.854×10^{-12} F/m), respectively, ε_{r_SiO2} and ε_{r_Si} are the relative dielectric constants of silicon dioxide ($\varepsilon_{r_SiO2} = 3.9$) and silicon ($\varepsilon_{r_Si} = 11.9$), respectively, and ρ_{Si} is the resistivity of silicon in Ω cm. Cor. is the TD dependent value. When TD is 30 μm, Cor. is $2.5 \times 10_{-8}$. If TD is reduced to 10 μm, Cor. has a new value of 1.5×10^{-8}. Two values of Cor. have been determined by a fitting method to match both the proposed model and several measured and 3D full wave simulated results [7].

By using Eqs. (1.1)–(1.5), the typical values of the lumped circuit components of a S/G TSV pair with a 30 μm pillar diameter, a 100 μm pillar length, a 0.5 μm SiO_2 insulator thickness, and pitches of 100 and 150 μm can be obtained, as in Table 1.2. Because the resistances (R_Ts) at 1 GHz are very small (12.44 mΩ), it is very difficult for them to degrade the signal transmitted through the S/G TSV pair; thus, they are not a critical design factor for TSV-based 3D ICs. The partial inductances (L_{ST}, L_{MT}) are also very small because the TSV pillars are very short and close to each other, and they have approximately 40 pH of loop inductance (2 L_T). Therefore, the partial inductances are also not a critical design factor. However, C_{SiO2} and R_{Si} are serious because they mainly determine the insertion loss occurring at an S/G TSV pair, as shown in Fig. 1.17. As the capacitance of C_{SiO2} increases and the resistance of R_{Si} decreases, the insertion loss increases. C_{SiO2} and R_{Si} can be controlled by changing the dimensions of the S/G TSV pair and the resistivity of the silicon wafer. As TD and TL increase and TT decreases,

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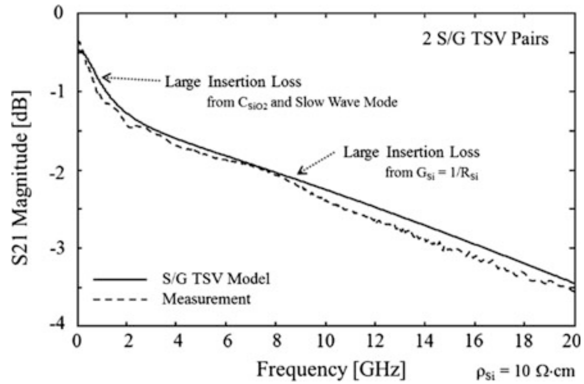

Fig. 1.17 Measured and calculated S_{21} magnitude of two S/G TSV pairs connected by metal lines [7] © 2011 IEEE

the value of C_{SiO2} increases. As TP and the resistivity decrease, R_{Si} decreases. Therefore, to achieve a small insertion loss in an S/G TSV pair, the TSV pillar diameter and length should be small and short, but the pitch of the TSV pillars, the SiO_2 insulator thickness, and the resistivity of silicon wafer should all be large.

1.3.3 TSV Electrical Behavior Based on the Model of an Extracted S/G TSV Pair

In this section, TSV electrical behavior will be examined through the use of the extracted S/G TSV pair model and by substituting various dimension values and resistivity values into Eqs. (1.1)–(1.5). Because an S/G TSV pair plays a role in signal transmission and it is one of the transmission lines, the electric behavior will be presented by the S_{21} magnitude, which is usually called the insertion loss, characteristic impedance (Z_0), attenuation constant (α), and slow wave factor (β/β_0). This electrical behavior can be calculated by using S-parameters and Eqs. (1.6)–(1.9) [4]. To determine how this electric behavior changes, we gave a ±50 % variation to the values of the dimensions (reference values: TD/TL/TP/TT (μm) = 30/100/150/0.5) used in Table 1.2 and selected several resistivity values of silicon wafers to be 5, 10, 15, 30, 60 Ω ·cm, and infinity (∞, pure dielectric material) (Table 1.3).

First, Eqs. (1.6)–(1.9) are introduced to facilitate understanding of the method for calculating the behavior with the measured and calculated S-parameters, which can be obtained through VNA (vector network analyzer) measurement and commercial Spice simulation with the extracted S/G TSV pair model.

The S-parameters form a matrix in which all of the elements are complex. Equation (1.6) shows a fundamental 2-port S-parameter and the four elements with a frequency dependency ($\omega = \pi f$, ω; angular frequency, f; frequency). In this display, all of the elements are based on Z_{SYS} (Ω) for port termination.

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Table 1.3 Dimension and material parameter variations of the S/G TSV pair for the discussions of TSV electrical behavior

S/G TSV pair dimension and material parameters	TD (μm)	TL (μm)	TT (μm)	TP (μm)	ρ_{Si} (Ω·μm)
Max.	45	150	0.75	225	∞
Ref.	30	100	0.50	50	10
Min.	15	50	0.25	75	5
Step #	3	3	3	3	6

$$2PortS - Parameter = \begin{pmatrix} S_{11}(\omega) & S_{12}(\omega) \\ S_{21}(\omega) & S_{22}(\omega) \end{pmatrix}. \tag{1.6}$$

By using the four elements, ABCD parameters (Eq. 1.7) can be obtained for calculating Z_0, α, and β of Eqs. (1.8)–(1.9).

$$ABCD\ Parameter = \begin{pmatrix} A(\omega) & B(\omega) \\ C(\omega) & D(\omega) \end{pmatrix} = \left[\begin{array}{l} A(\omega) = \frac{(1-S_{22}(\omega))(1+S_{11}(\omega))+S_{21}(\omega)S_{12}(\omega)}{2S_{21}(\omega)} \\ B(\omega) = \frac{(1+S_{22}(\omega))(1+(\omega))-S_{21}(\omega)S_{12}(\omega)}{2S_{21}(\omega)} \times Z_{SYS} \\ C(\omega) = \frac{(1-S_{22}(\omega))(1-S_{11}(\omega))-S_{21}(\omega)S_{12}(\omega)}{2S_{21}(\omega)} \times \frac{1}{Z_{SYS}} \\ D(\omega) = \frac{(1+S_{22}(\omega))(1-S_{11}(\omega))+S_{21}(\omega)S_{12}(\omega)}{2S_{21}(\omega)} \end{array} \right. \tag{1.7}$$

$$Characteristic\ Impedance(Z_0) = Real(Z_0) + j \cdot Imaginary(Z_0) = \frac{B(\omega)}{sinh(\gamma(\omega) \cdot TL)} \tag{1.8}$$

$$Complex\ Propagation\ Constant = \gamma(\omega) = \alpha(\omega) + j \cdot \beta(\omega) = \frac{arccosh(A(\omega))}{TL} = (Attenuation\ Constant) + j \cdot (Propagation\ Constant). \tag{1.9}$$

TL is the length of the transmission line or the TSV length, sinh( ) and arccosh( ) are the hyperbolic sine function and arc-cosine function, respectively. Of course, the slow wave factor defined by $\beta/\beta_0 = \sqrt{\varepsilon_{eff}}$ and Eq. (1.9) can be obtained, where β_0 is the propagation constant when the silicon wafer and SiO_2 insulator are replaced with air ($\varepsilon_r = 1$), and ε_{eff} is the effective dielectric constant determining the wavelength and speed at a typical frequency. As the slow wave factor increases, a signal with typical frequencies runs more slowly on the transmission line.

<Calculated versus Measured TSV Electrical Behavior>

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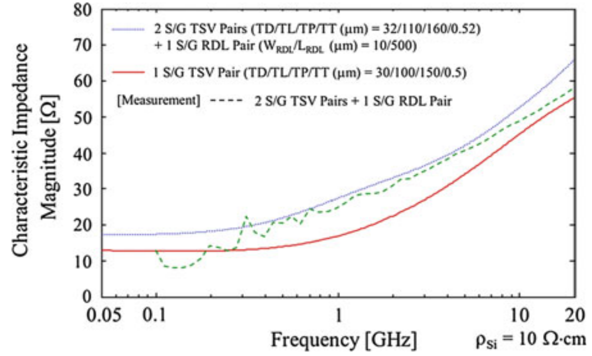

Fig. 1.18 Measured and calculated characteristic impedances of Fig. 1.17 and Single S/G TSV Pair

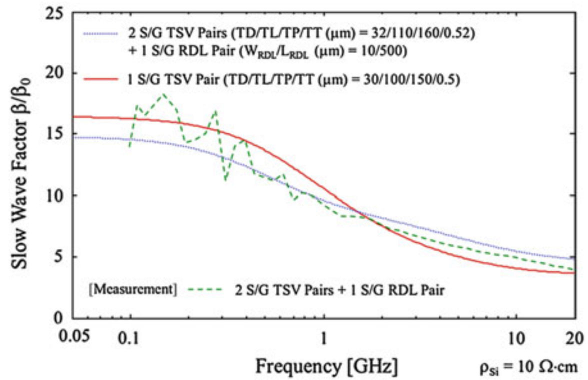

Fig. 1.19 Measured and calculated slow wave factors (β/β_0) of Fig. 1.17 and Single S/G TSV pair

Figure 1.17 compares the measured and the calculated S_{21} magnitudes (insertion loss) of two S/G TSV pairs connected in series in the chip located on top by two metal lines on the chip located on the bottom when the two chips are vertically stacked [7]. By using the measured (dashed line) and calculated (dotted line) S-parameters and Eqs. (1.6)–(1.9), two calculated and measured TSV electrical behaviors are compared in Figs. 1.19, 1.20 and 1.21. The dimension parameters for the calculations follow those of the TSV and the metal lines in the DUT (device under test). Additionally, to easily obtain intuition regarding the TSV electrical behavior, the calculations of a single S/G TSV pair with the reference values of Table 1.3 are plotted in all of the figures.

Figure 1.18 compares three characteristic impedance magnitudes, which is the absolute value of the complex characteristic impedance Z_0. Although there is a small discrepancy, the extracted S/G TSV pair model follows the measurement well and gives us high confidence. Usually, the characteristic impedance of a transmission line is defined as $Z_0 = \sqrt{(R + j\omega L)/(G + j\omega C)}$ [10]. If the characteristic impedance is small or less than 50 Ω, the transmission line is capacitive. Therefore, the low level characteristic impedance of Fig. 1.18 implies that the S/G TSV pair induces a large capacitance, especially in the low frequency range and slow wave mode. The characteristic impedance of a single S/G TSV pair is lower

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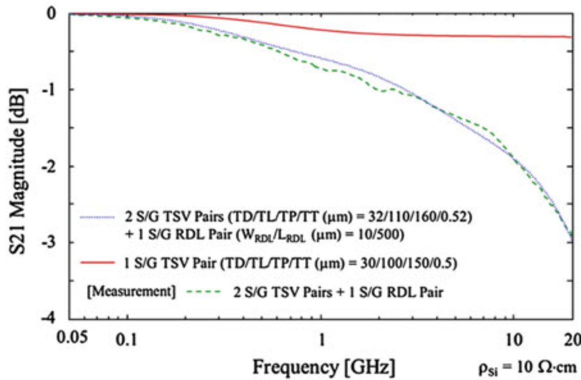

Fig. 1.20 Measured and calculated S_{21} magnitudes (Insertion losses) of Fig. 1.17 and single S/G TSV pair

than that of two S/G TSV pairs. This result shows that metal lines for connecting two S/G TSV pairs contribute to increasing the inductance of a transmission line with TSVs. The increased characteristic impedance with increasing frequency also means that because the slow wave mode converts to a dielectric quasi-TEM mode and, consequently, the TSV capacitance (C_{eff}) is reduced, the TSV inductance contribution to the characteristic impedance becomes stronger. As mentioned previously, the TSV capacitance effect due to the slow wave mode can be found in the slow wave factor, as shown in Fig. 1.19, in which two slow wave factors cross and the slow wave mode effect abruptly decreases by approximately 2 GHz, as shown in Fig. 1.17. Considering that the dielectric constant of silicon is 11.9 and the effective dielectric constant ($(\beta/\beta_0)^2 = \varepsilon_{eff}$) at 0.05 GHz is 290, the slow wave mode effect can seriously retard a signal, give a very large capacitance to a signal, and consequently degrade the signal quality.

Figure 1.20 plots three insertion losses. Because the DUT has two S/G TSV pairs and metal lines, the capacitance and the inductance are larger and, consequently, the insertion losses in all frequency ranges are larger than those of a single TSV pair.

Previously, we mentioned that the resistance and conductance are not critical design factors. This assumption can be confirmed by examining Fig. 1.21, in which the attenuation factors are very small and have very little effect on the characteristic impedance.

Through the measurements and calculations based on the extracted S/G TSV pair model, the most important design factor for TSV-based 3D ICs is the SiO2 insulator capacitance caused by the MIS-structured TSV. Therefore, to design a TSV-based 3D IC with high speed, wide bandwidth, and low power consumption, the SiO2 capacitance should be minimized by designing a TSV with a small diameter (TD), a short length (TL), and a low SiO_2 thickness (TT), referencing Eq. (1.5).

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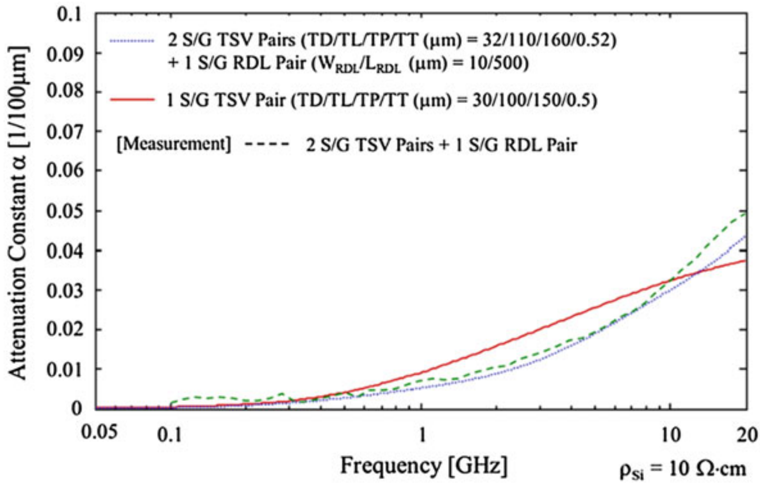

Fig. 1.21 Measured and calculated attenuation constant α of Fig. 1.17 and single S/G TSV Pair

In Sect. 1.3, the electrical analysis of a TSV based on an MIS analysis has been discussed by explaining why an MIS analysis should first be considered for the electrical analysis of a TSV, how the electrical analysis of a TSV can be achieved by showing the model of a S/G TSV pair based on a double sided MIS structure, and what TSV electrical behavior can be defined and how the behavior can vary depending on the TSV dimensions and the silicon resistivity by using the S/G TSV pair model. We would like to recommend that you completely understand this section to more easily follow the next chapters.

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Chapter 2
Electrical Modeling of a Through Silicon Via

Joohee Kim, Jun So Pak and Joungho Kim

Abstract 3D IC is emerging as a powerful solution for the next-generation system packaging and integration technology to achieve low power consumption, high channel bandwidth and high density integration capability simultaneously. As for the vertical interconnect for a 3D IC, through-silicon via (TSV) is a key component which can provide a significant performance improvement with greatly reduced physical length of channels among vertically integrated chips. In this chapter, the scalable and analytic electrical model of a TSV is proposed and the high-frequency electrical behavior and signaling performance of a TSV is analyzed in frequency and time domains.

Keywords Differential signal TSV · Equivalent circuit model · Single-ended signal TSV · Scalable model · TSV channel · 3D IC

2.1 Introduction

As technology advances in the nanometer era, the packaging density and system performance of individual chips improve. However, the scaling of the minimum feature size of the transistor slows due to the limitations from leakage power

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consumption, process variation, and cost issues [1–3]. In addition, many electronic devices, such as tablets, laptops, and smart phones, have become more compact, and, they must achieve multi-function and high-throughput computing performance simultaneously. As a new powerful paradigm for next-generation system integration and packaging technology, 3-dimensional integration emerges as a promising solution. With 3D integration, many chips can be integrated in a vertical axis, thus improving the system bandwidth by reducing the physical lengths of the channels among the integrated chips. The conceptual scheme of 3-dimensional integrated circuits (3D ICs) is shown in Fig. 2.1. As shown in Fig. 2.1, various functional dies, such as memory, RF, and processor dies, are vertically and horizontally integrated on a silicon-based interposer to be integrated in one package. A through-silicon via (TSV) forms the vertical interconnect between stacked dies, which enables a pure 3D IC to be realized and satisfies the small form factor, low power consumption and high bandwidth system requirements simultaneously. As shown in Fig. 2.1, a TSV is a via hole passing through the silicon substrate, which is filled with a conductor such as copper (Cu), tungsten (W) or polycrystalline silicon (poly-Si) for the electrical connection between dies [4]. An insulation layer surrounding the via is used to electrically isolate the conductive silicon substrate and TSV. Figure 2.2 shows SEM image of one test vehicle which includes TSV, RDL, and insulation layer. Even then, the low fabrication yield from TSV and 3D IC fabrication processes such as high-aspect-ratio via drilling/filling, thin silicon-dioxide sidewall deposition, and die stacking with micro-bumps is an issue [5]. However, a TSV-based 3D IC is the way to go because it overcomes the critical bottlenecks of 2-dimensional ICs in many ways, providing higher system bandwidth and lower power consumption from the reduced chip-to-chip channel parasitics, higher design flexibility and design freedom for multi-functional systems, and highly dense packaging to achieve a smaller form factor. In addition, a TSV, which has a diameter of several μm, can widen the bus width for the higher system bandwidth without consuming more die area than wire bonding or flip-chip bonding integrations. As a result, wide I/O design could be achieved more efficiently by using TSVs and the number of I/Os of a TSV-based 3D IC will keep increasing. Thus, understanding the electrical behavior of a TSV, which can greatly impact on the overall 3D IC system performance is very important.

To design high-speed I/O channels with TSVs and perform signal integrity analysis for the advanced 3D IC design, the TSVs must be electrically modeled using design parameters such as geometric and material information up to the GHz range. Then, the electrical model can be combined with other circuitry so that the overall electrical performances of the system can be easily computed. Therefore, the modeling and analysis of a TSV have been extensively researched as detailed in [6–15]. With various targets or applications of 3D IC designs, the model has to estimate the electrical behavior of a TSV, even if given different physical dimensions and material properties. Thus, a scalable model of the TSV incorporating analytic equations must be proposed. Then, if the physical structure or the material changes, the model can be scaled to estimate the electrical behavior of the TSV channel based on the changes in the design parameters. Furthermore, a model

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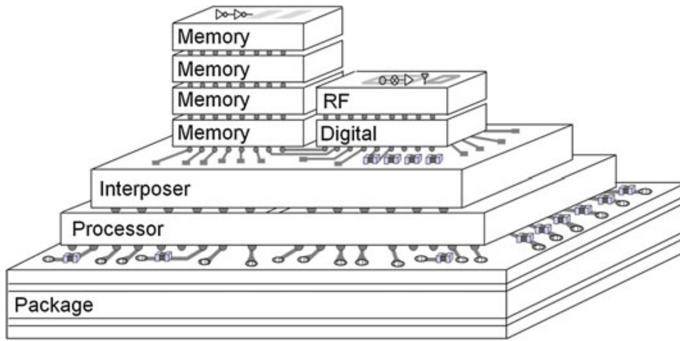

Fig. 2.1 A 3-dimensional integrated circuit (3D IC); a vertical integration of homogenous and heterogeneous dies, such as memory, RF, digital, processor die, and interposer, for realizing highly dense packaging for high-speed integrated circuit systems [15] © 2011 IEEE

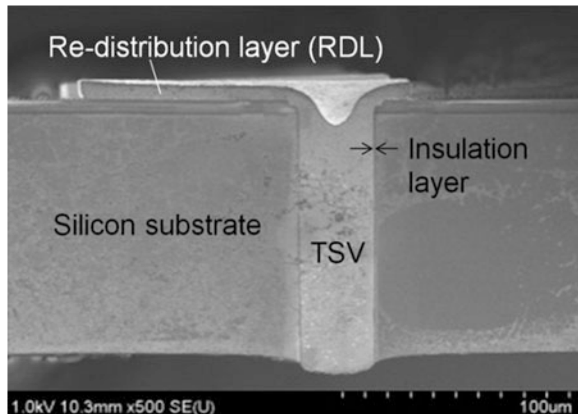

Fig. 2.2 A scanning electron microscopy (SEM) picture of a through silicon via (TSV), which is a via hole through the silicon substrate, filled with metal, and surrounded by an insulation layer between the substrate and via [15] © 2011 IEEE

with analytic closed-form equations can be expanded to evaluate electrical performances such as power consumption, delay, and skew along the TSV-based interconnect. In addition, the model provides insight into a TSV by including the physical meaning of each parasitic component. Therefore, modeling with analytic closed-from equations is very powerful.

In this chapter, the high-frequency scalable electrical model of a TSV with analytic *RLGC* equations is proposed. The electrical behaviors of a TSV are analyzed with the proposed model. The analytic equations of the scalable model are proposed in terms of design parameters, such as physical dimensions and material properties. Thus, each analytic equation fully represents the physical meaning of a parasitic component of a TSV. The scalability of the proposed model for a TSV is verified by simulation with parametric variations from the 3D field solver. As a result, a high-frequency scalable electrical model of the TSV channel is proposed. To experimentally verify the proposed model, a series of test vehicles of a TSV

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channel are fabricated. The proposed model is experimentally verified with S-parameter measurements up to 20 GHz. Therefore, the electrical characteristics of a TSV channel are analyzed in the frequency domain with the verified scalable model and with variations in design parameters. From this analysis, the capacitive and resistive electrical behaviors of a TSV channel are characterized. In addition, the design parameters that dominantly affect the TSV channel characteristic are analyzed in various frequency ranges. Furthermore, the overall electrical behavior of the TSV channel is analyzed with fabricated test vehicles in the time domain. The time-domain analysis of the TSV channel is performed using eye diagram measurements for up to 10 Gbps input signals of pseudo-random bit data patterns.

2.2 Equivalent Circuit Model of a TSV

In this section, the electrical circuit model of a TSV, which is a physics-based equivalent circuit model, is presented. This electrical model is proposed with analytic *RLGC* equations based on the lumped model. Because the model is derived from the physical structure, it fully expresses the physical meaning of each parasitic component with the proposed closed-form equations. For the scalability of the model, the model is proposed with structural parameters and material properties as variables of the analytic *RLGC* equations. The structure and parameters of a TSV are shown in Fig. 2.3.

Figure 2.3 shows the structure and parameters of a signal TSV, a ground TSV and bumps in a single-ended signaling configuration with the via-last process. A via-last TSV is a type of TSV that is formed after metallization. Thus, a via-last TSV passes through not only the substrate but also the inter-metal dielectric (IMD) layer. Because a TSV has to connect between top and bottom dies, it passes through the silicon substrate vertically and the via is filled with metal for the electrical conduction. Copper (Cu), tungsten (W), and polycrystalline silicon (poly-Si) are used as conductive fill materials. Among them, copper fill becomes the mainstream approach today. For the substrate material, silicon is generally used to support semiconductor devices; however, glass or other organic substrates are also considered as the substrate material to improve insulating performance [16].

For the current technology, the diameter of a TSV is several μm (<10 μm) and the height of a TSV is less than 50 μm. With the help of the greatly reduced length of the interconnect between chips, TSV-based 3D IC has a significant advantage over to 2D or 2.5D integration with wire bonding or flip chip packaging. In addition, TSV-based 3D IC enables wide I/O application, because TSV consumes much smaller die area per I/O. For the TSV-to-TSV pitch, the diameter to pitch ratio is approximately 1:2.5 to 1:4 and depends on the fabrication technology and the keep-out zone around a TSV. The thickness of the thin insulating layer surrounding via is in the 0.1 to 0.5 μm range. There is another insulation layer that forms on the bottom side of the silicon substrate, and this layer is referred to as the bottom oxide layer. This insulation layer is necessary to provide insulation

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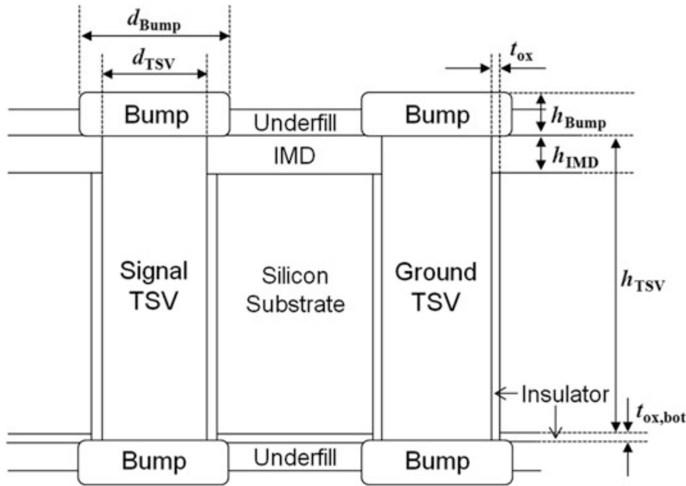

Fig. 2.3 A single-ended signal TSV structure and design parameters for the scalable modeling [15] © 2011 IEEE

between the conductive silicon substrate and the metallic bump and also has a thickness in the 0.1 to 0.5 μm range.

With this structure, a high-frequency scalable electrical model of TSVs with bumps is proposed in Fig. 2.4. Each of the *RLGC* components corresponds to a structure of a TSV. The analytic *RLGC* equations are derived from the physical configuration with the design parameters. Therefore, each *RLGC* equation is a function of the variables from the design parameters. As shown in Fig. 2.4, the scalable electrical model is proposed by lumped components. The total lengths of the TSV interconnect including the TSV and bump decrease to tens of μm as the process technology advances. Because this length is sufficiently short compared to the wavelength of the several or tens of GHz operating frequency, the lumped approximation is valid and a single lumped stage is sufficient for the TSV model.

In the case of the via-first or middle process, the parasitic capacitances such as the capacitance of IMD layer (C_{IMD}) should be neglected or other parasitic capacitances has to be additionally considered to accurately estimate the electrical behaviors of a TSV. In addition, if there are active circuits between TSVs, the assumed field distribution can be changed. However, the main electrical characteristics and the loss mechanism of a TSV channel are valid with the proposed model.

In a practical design, many TSVs, such as array-type TSVs, are designed, instead of a single GS pair of TSVs. However, the equivalent circuit model of a TSV among TSV array is equivalent to the proposed model shown in Fig. 2.4, differing in that different weights have to be applied for each *RLGC* component. Thus, we can perform array-type TSV modeling by extracting or modeling the weights of the *RLGC* components.

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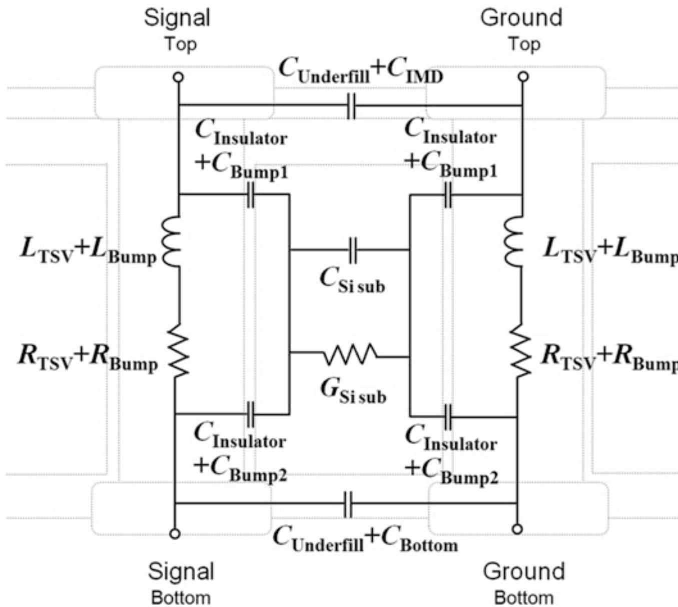

Fig. 2.4 An equivalent circuit model of a pair of signal and ground TSVs with bumps with *RLGC* lumped elements assuming that the silicon substrate is floated [15] © 2011 IEEE

2.2.1 Electrical Modeling of a TSV with the Analytic Equations

In this chapter, analytic *RLGC* components of the proposed equivalent circuit model of a TSV are proposed and electrically modeled with analytic equations which are functions of material properties, structural parameters, frequency, and etc. The proposed equivalent circuit model is derived based on the physical structure of a TSV. Among various TSV parasitics, the capacitance of a TSV is the most important factor which determines the overall electrical behavior of a TSV. To electrically isolate the TSV from the conductive silicon substrate, an insulation layer surrounding the TSV is necessary. Due to this insulation layer, there is an insulator capacitance, $C_{Insulator}$, as shown in Fig. 2.5. In this work, the substrate is assumed to be floated. If the substrate is fully biased to the ground, then the depletion capacitance has to be added to $C_{Insulator}$ in series [13]. Since the TSV is filled with metal and the silicon substrate is conductive, the insulator capacitance can be derived from the coaxial-cable capacitance model [17, 18]. This equation is originally obtained by solving Poisson's equation in a cylindrical coordinate system. Thus, $C_{Insulator}$ is a function of d_{TSV}, h_{TSV}, and t_{ox}, as shown in (2.1). Since the insulator capacitance of a TSV is separated into two parallel parts, as shown in Fig. 2.5, the equation of $C_{Insulator}$ is expressed as half of the insulator capacitance

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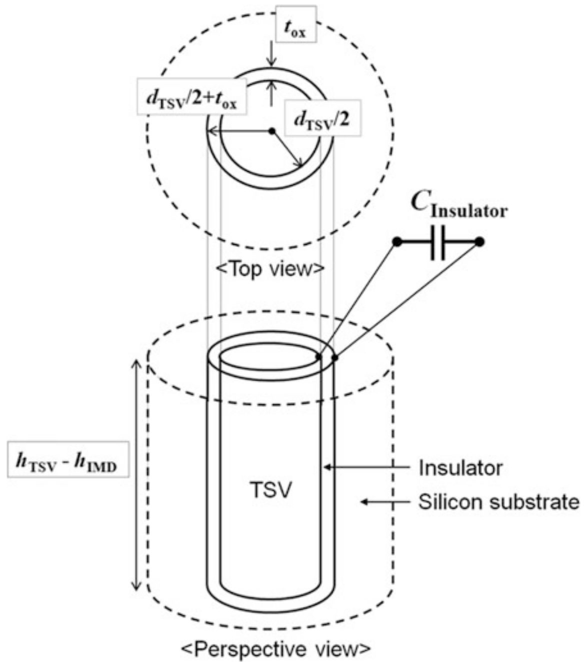

Fig. 2.5 A top view and a perspective view of a TSV which passes through the silicon substrate vertically. The TSV is surrounded by an insulator to be isolated from the conductive silicon substrate. Thus, $C_{Insulator}$ is derived from the coaxial-cable capacitance model which is determined by d_{TSV}, t_{ox}, h_{TSV}, and h_{IMD} [15] © 2011 IEEE

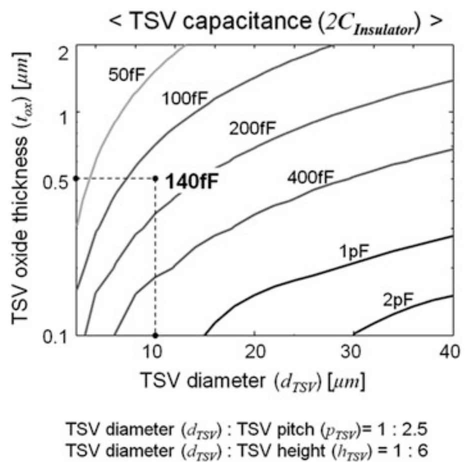

Fig. 2.6 TSV capacitance values from the proposed analytic equations of $C_{Insulator}$ depending on variations of TSV diameter (d_{TSV}) with the fixed ratio of d_{TSV} to TSV pitch (p_{TSV}) as 1:2.5 and d_{TSV} to TSV height (h_{TSV}) as 1:6

of a TSV. The calculated $C_{Insulator}$ is plotted in Fig. 2.6. Since the absolute value of the TSV capacitance is not even 1 pF with the default dimension presented in Fig. 2.6, this capacitance is the most dominant parasitic capacitance which determines the overall electrical behavior of a TSV.

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$$C_{Insulator} = \frac{1}{2}\left\{2\pi \times \varepsilon_0 \varepsilon_{r,Insulator} \times \frac{h_{TSV} - h_{IMD}}{ln\left(\frac{\frac{d_{TSV}}{2}+t_{ox}}{\frac{d_{TSV}}{2}}\right)}\right\} [\text{F}] \tag{2.1}$$

Because TSV has 3-dimensional structure in the lossy silicon substrate, there is a leakage through the substrate when there is a ground TSV near a signal TSV. The amount of leakage current through the substrate is determined by the impedance of the leakage path between signal and ground TSVs, thus, the impedance of the $C_{Insulator}$ significantly affect to the insertion loss of a TSV due to the leakage through the silicon substrate. As a result, as $C_{Insulator}$ increases, the insertion loss of a TSV increases. If we decrease TSV diameter and increase TSV oxide thickness, we can reduce TSV capacitance as shown in Fig. 2.6.

In addition, the conductance due to the loss tangent of the oxide insulator is ignored in the proposed model since it does not affect the insertion loss of a TSV considering the silicon substrate with the conductivity of 10 S/m. If the conductivity of the silicon substrate becomes very small like as high-resistivity silicon substrate, the loss of a TSV is not dominantly dependent on the silicon substrate conductance any more. Then, TSV resistance or the dielectric loss due to the loss tangent of the oxide insulator become dominant which affect the insertion loss of a TSV, and thus, we cannot ignore dielectric loss terms. For example, when the material of the substrate is glass, the dielectric loss of the insulation layer has to be considered for the accurate high-frequency modeling of a through-glass via (TGV). Furthermore, if the temperature increases, the relative permittivity of the dielectric material decreases which results in the smaller parasitic capacitance. The temperature effect on electrical behavior of a TSV is analyzed with analytical temperature-dependent modeling a TSV in Chap. 5.

One of the bump-to-silicon substrate capacitances of the upper side of the silicon substrate, C_{Bump1}, has to be added to $C_{Insulator}$ of the proposed equivalent circuit model, as shown in Fig. 2.7. This capacitance can be modeled as a parallel-plate capacitor [19]. As shown in Fig. 2.7, the area, where the electric fields are formed, corresponds to where the bump overlies the silicon substrate through the inter-metal dielectric (IMD) layer. Thus, C_{Bump1} is proportional to this area and inversely proportional to the IMD height, h_{IMD}. As a result, C_{Bump1} can be calculated with (2.2), which depends on d_{TSV}, d_{Bump}, and h_{IMD}.

$$C_{Bump1} = \varepsilon_0 \varepsilon_{r,IMD} \times \frac{\pi\left\{\left(\frac{d_{Bump}}{2}\right)^2 - \left(\frac{d_{TSV}}{2} + t_{ox}\right)^2\right\}}{h_{IMD}} [\text{F}] \tag{2.2}$$

In a similar manner, another bump-to-silicon substrate capacitance due to the bottom oxide layer on the bottom side of the silicon substrate, C_{Bump2}, has to be added to $C_{Insulator}$. This bottom oxide layer is formed by the oxidation after back-grinding of the silicon substrate. This process is necessary to expose the TSV and

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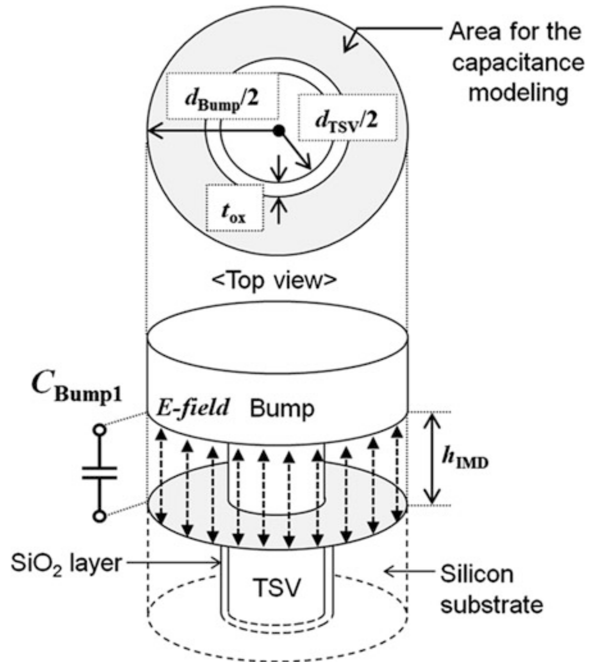

Fig. 2.7 A top view and a perspective view of the upper part of a TSV with a bump to calculate the area where the electric fields are formed between the bump and the silicon substrate to model C_{Bump1} which has parallel-plate capacitor configurations [15] © 2011 IEEE

connect it with another die. In general, the bottom oxide thickness is very thin under 0.5 μm so that the value of C_{Bump2} is considerable to the overall parasitic capacitance of a TSV. C_{Bump2} is also derived from the parallel-plate capacitor model, as shown in Fig. 2.8. Therefore, d_{TSV}, d_{Bump}, h_{Bump}, and the bottom oxide thickness, $t_{ox,bot}$, determines C_{Bump2}, as shown in (2.3). From (2.3), if the bump diameter increases, C_{Bump2} increases. Since the oxide thickness of the back-side of the silicon is in 0.1 to 0.5 μm range, if the bump diameter is much bigger than the TSV diameter, the impact of C_{Bump2} on the capacitive characteristic of a TSV becomes very significant as much as that of $C_{Insulator}$. As the TSV technology advances, fine-pitch TSVs are preferred since it can reduce capacitive parasitic as well as die area consumption even with large number of I/Os. However, if the micro-bump directly contacted to a TSV does not shrink as much as TSVs, there will be still a significant amount of parasitic capacitance due to the C_{Bump2} even with the reduced parasitic capacitance from the reduced TSV diameter effect. Therefore, not only TSV diameter but also bump diameter has to be decreased in order to effectively reduce the parasitic capacitance of a TSV. If both sides of the silicon substrate are used for metal layers for signal routing or power distribution network, then this capacitance can be removed from the equivalent circuit model of a TSV.

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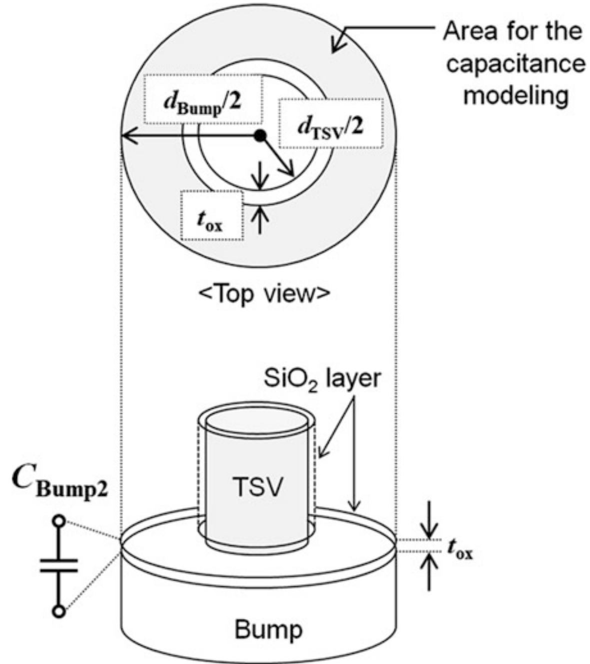

Fig. 2.8 A top view and a perspective view of the bottom part of a TSV with a bump to calculate the area where the electric fields are formed between the bump and the silicon substrate to model C_{Bump2} which has parallel-plate capacitor configurations [15] © 2011 IEEE

$$C_{Bump2} = \varepsilon_0 \varepsilon_{r,ox} \times \frac{\pi \left\{ \left(\frac{d_{Bump}}{2} \right)^2 - \left(\frac{d_{TSV}}{2} + t_{ox,bot} \right)^2 \right\}}{t_{ox,bot}} \text{ [F]} \tag{2.3}$$

With the via-last process, the capacitance between the signal and ground bumps from the underfill, $C_{Underfill}$, the capacitances between the signal and ground TSVs from the IMD layer, C_{IMD}, and the bottom oxide layer, C_{Bottom}, have to be modeled. As shown in Fig. 2.9, the cross-sectional areas of the TSV and bump are circular. Hence, $C_{Underfill}$, C_{IMD}, and C_{Bottom} are derived from the model of the parallel-wires capacitance [19]. The capacitances are determined by the distance between the signal and ground TSVs or bumps, p_{TSV}, the diameter of the TSV and bump, d_{TSV} and d_{Bump}, and the height of the underfill, IMD layer and bottom oxide, h_{Bump}, h_{IMD}, and $t_{ox,bot}$. If d_{TSV} and d_{Bump} are very small in comparison with the distance of separation, $\frac{p_{TSV}}{d_{TSV}}$ (or $\frac{p_{TSV}}{d_{Bump}}$) >> 1, the natural logarithm replaces the inverse hyper cosine to simplify the calculation. However, since the TSV in 3D IC is for denser integration with fine pitch, we assume that the ratio of p_{TSV} and d_{TSV} or d_{Bump}, $\frac{p_{TSV}}{d_{TSV}}$ (or $\frac{p_{TSV}}{d_{Bump}}$), is less than 10. Therefore, $C_{Underfill}$, C_{IMD}, and C_{Bottom} are modeled as shown in (2.4–2.6) (Fig. 2.10).

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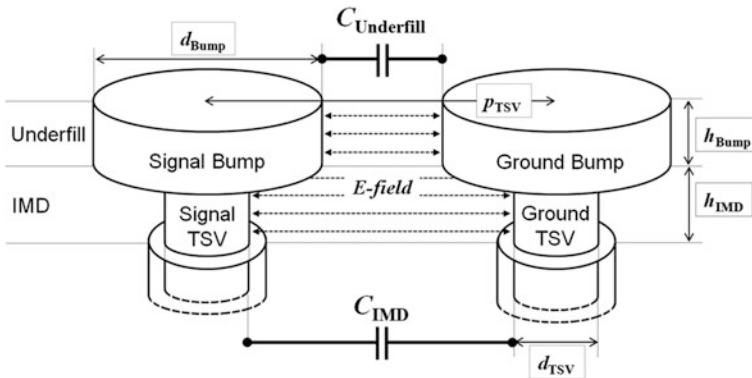

Fig. 2.9 The upper part of a TSV and a bump with electric fields formed between the signal and ground TSVs and bumps to model $C_{Underfill}$ and C_{IMD}. The TSV/Bump signal and ground pairs are in a parallel-wire capacitor configuration. $C_{Underfill}$ is formed due to the underfill between bumps, and C_{IMD} is formed due to the IMD between TSVs [15] © 2011 IEEE

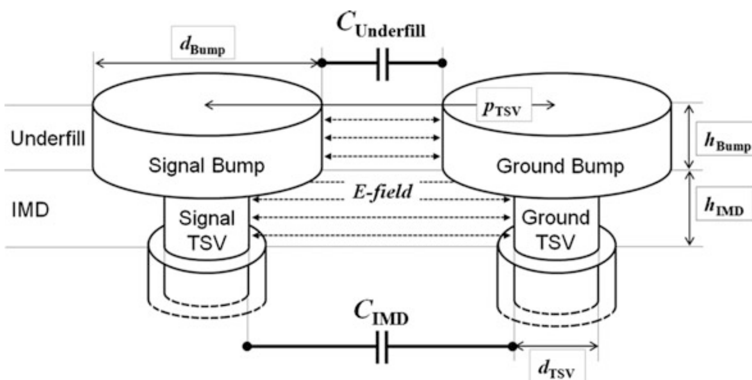

Fig. 2.10 The bottom part of a TSV and a bump with the electric fields formed between signal and ground TSVs to model C_{Bottom}, which are in the parallel-wire capacitor configuration. C_{Bottom} is formed due to the bottom oxide layer between TSVs [15] © 2011 IEEE

$$C_{Underfill} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,Underfill}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{Bump}}\right)} \times h_{Bump}\ [\mathrm{F}] \tag{2.4}$$

$$C_{Underfill} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,Underfill}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{Bump}}\right)} \times h_{Bump}\ [\mathrm{F}] \tag{2.5}$$

$$C_{IMD} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,IMD}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \times h_{IMD}\ [\mathrm{F}] \tag{2.6}$$

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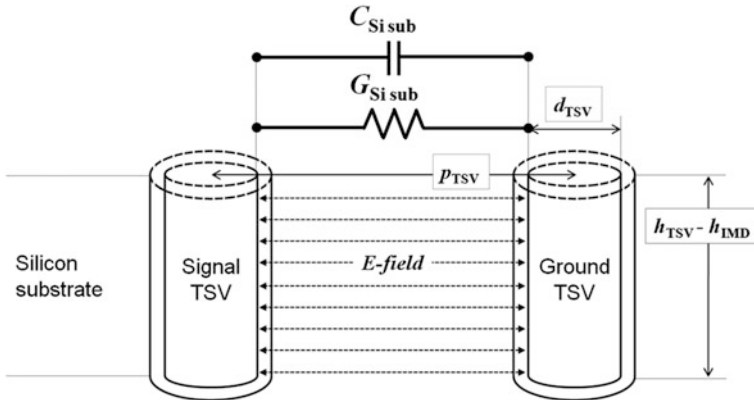

Fig. 2.11 A TSV passing through the silicon substrate with the electric fields formed between signal and ground TSVs to model $C_{Si\,sub}$ and $G_{Si\,sub}$. The parallel-wire capacitor configuration is implemented [15] © 2011 IEEE

There is another parasitic capacitance contributed to the lateral side of the bump. This capacitance is formed between the lateral side of the bump and the conductive silicon substrate. It has to be added to $C_{Insulator}$ of the proposed model. It can be calculated from the conformal mapping method of the vertical plate. This method transforms a 3-dimensional interconnect into a parallel plate configuration [20]. With d_{TSV} of 30 µm, d_{Bump} of 70 µm, h_{Bump} of 10 µm and h_{IMD} of 6 µm, this capacitance is about 10 fF. This parasitic capacitance is not included as in parallel with $C_{Insulator}$ in this proposed model, but, this fringe capacitance cannot be ignored if the value of this capacitance becomes tens of fF.

Since the silicon is a semiconductor, there are capacitance and conductance between the signal and ground TSVs, as shown in Fig. 2.11. In a similar manner as modeling $C_{Underfill}$, C_{IMD}, and C_{Bottom}, the capacitance of the silicon substrate, $C_{Si\,sub}$, is modeled by applying the parallel-wires capacitance model in (2.7). Thus, $C_{Si\,sub}$ is expressed as a function of d_{TSV}, p_{TSV}, h_{TSV}, and h_{IMD}. The $h_{TSV} - h_{IMD}$ term expresses the valid height where the electric fields are formed between the signal and ground TSVs in the silicon substrate. In addition, a material property, the relative permittivity of the silicon substrate, $\varepsilon_{r,Si}$, is also a variable of $C_{Si\,sub}$. Depending on dimension variations, the calculated $C_{Si\,sub}$ is plotted in Fig. 2.12.

$$C_{Si\,sub} = \frac{\pi \times \varepsilon_0 \varepsilon_{r,Si}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \times (h_{TSV} - h_{IMD})[\mathrm{F}] \quad (2.7)$$

In most circuit designs, the dielectric losses can be ignored since the conductor losses are dominant. However, as frequencies increase, it is important to consider the dielectric losses which vary with frequency. When dielectric losses are accounted for, the dielectric constant of the material becomes complex: $\varepsilon = \varepsilon' - j\varepsilon''$. Since the imaginary portion represents the losses, $\frac{1}{\rho} = 2\pi f \varepsilon''$ becomes the equivalent loss

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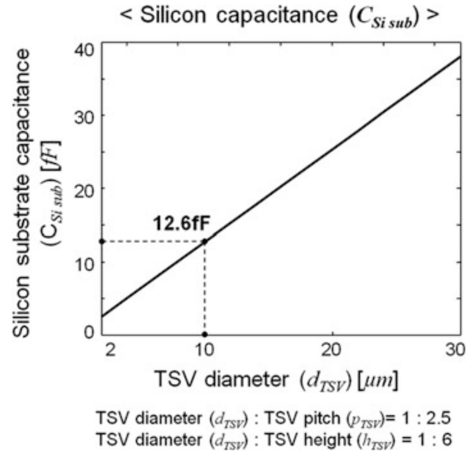

Fig. 2.12 Silicon substrate capacitance values from the proposed analytic equations of $C_{Si\,sub}$ depending on variations of TSV diameter (d_{TSV}) with the fixed ratio of d_{TSV} to TSV pitch (p_{TSV}) as 1:2.5 and d_{TSV} to h_{TSV} as 1:6

mechanism, where ρ is the effective resistivity of the dielectric material and f is the frequency. Thus, the loss tangent can characterize the loss in dielectrics with $tan|\delta d| = \frac{1}{2\rho\pi f\varepsilon} = \frac{\varepsilon''}{\varepsilon'}$ and then the relationship between capacitance and conductance can be established as $G = \frac{\varepsilon'}{\varepsilon'}(2\pi fC)$, resulting in the relationship in (2.8) [21]. Thus, the conductance of the silicon substrate, $G_{Si\,sub}$, is proposed in (2.9).

$$\frac{C_{Si\,sub}}{G_{Si\,sub}} = \frac{\varepsilon_{Si}}{\sigma_{Si}} \tag{2.8}$$

$$G_{Si\,sub} = \frac{\pi \times \sigma_{Si}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{TSV}}\right)} \times (h_{TSV} - h_{IMD})[\mathrm{S}] \tag{2.9}$$

The physical origin of $G_{Si\,sub}$ is the silicon conductivity, σ_{Si}, which is predominantly determined by the majority carrier concentration. Therefore, it is another significant design parameter, which dominantly affects the insertion loss of a TSV. As shown in Fig. 2.13, silicon conductance increases as silicon conductivity increases. Thus, high-resistivity substrate may decrease silicon conductance which reduces the insertion loss. In addition, increasing TSV-to-TSV pitch can be another way to reduce the leakage through the lossy silicon substrate to the ground by decreasing $G_{Si\,sub}$.

The resistances of the TSV and bump, R_{TSV} and R_{Bump}, are also modeled with structural parameters, as shown in (2.10) and (2.11). High-frequency current flows close to the surface of the conductor due to the formation of the eddy current, which is called the “skin effect”. To model R_{TSV} and R_{Bump} with a non-uniform current distribution at high frequencies, the depth of penetration, which is the skin depth, has to be determined to calculate the resistance of the TSV and bump. The skin depth is defined by material properties, such as the permeability in H/m and

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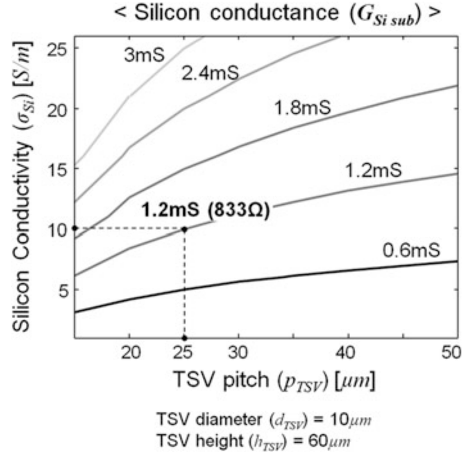

Fig. 2.13 Silicon substrate conductance values from the proposed analytic equations of $G_{Si\,sub}$ depending on variations of silicon conductivity (σ_{Si}) and TSV diameter (d_{TSV}) with d_{TSV} of 10 μm and h_{TSV} of 60 μm

the conductivity in S/m, and also the frequency in Hz [21]. Therefore, the analytic equations of R_{TSV} and R_{Bump} are presented in (2.10) and (2.11).

$$R_{TSV} = \sqrt{R_{dc,TSV}^2 + R_{ac,TSV}^2}[\Omega] \tag{2.10}$$

where
$$R_{dc,TSV} = \rho_{TSV} \times \frac{h_{TSV}}{\pi \times \left(\frac{d_{TSV}}{2}\right)^2}[\Omega]$$

$$\delta_{skin\,depth,TSV} = \frac{1}{\sqrt{\pi f \mu_{TSV} \sigma_{TSV}}}\,[\mathrm{m}]$$

$$R_{ac,TSV} = k_p\left(\rho_{TSV} \times \frac{h_{TSV}}{2\pi \times \frac{d_{TSV}}{2} \times \delta_{skin\,depth,TSV} - \pi\delta_{skin\,depth,TSV}^2}\right)[\Omega]$$

In addition, there is another effect that induces current flow on the surface of the conductor, but is non-uniformly distributed around the perimeter by attracting currents to the inside-facing surfaces of the conductors, so called "proximity effect" [22]. This effect begins to appear after the skin effect on-set frequency. The proximity factor, k_p, increases as round conducting wires such as TSVs are brought closely together. For TSVs and bumps, the magnitude of the proximity factor, k_p, is determined by the ratio $\frac{p_{TSV}}{d_{TSV}}$ or $\frac{p_{Bump}}{d_{Bump}}$ [22]. If other TSVs are located near the single-ended signal TSV, then this proximity effect between two TSVs or bumps does not have to be considered. Then, k_p is removed from the proposed equations.

And the calculated R_{TSV} are shown in Fig. 2.14. As shown in Fig. 2.14, the skin effect starts at around several hundred MHz and TSV resistance increases as frequency increases. And TSV resistance is tens of mΩ and this parasitic is less significant than other parasitics of a TSV such as TSV oxide capacitance, silicon substrate capacitance and silicon substrate conductance.

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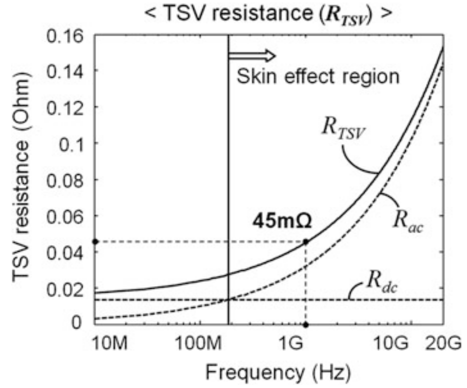

Fig. 2.14 TSV resistance values from the proposed analytic equations of R_{TSV} depending on frequencies up to 20 GHz with the TSV diameter (d_{TSV}) of 10 μm and TSV height (h_{TSV}) of 60 μm

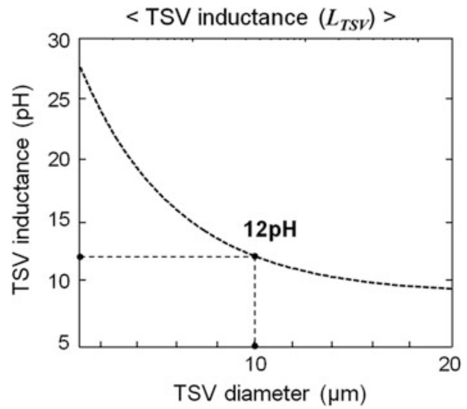

Fig. 2.15 TSV inductance values from the proposed analytic equations of L_{TSV} depending on frequencies up to 20 GHz with the TSV diameter (d_{TSV}) of 10 μm and TSV height (h_{TSV}) of 60 μm

As the operating frequency increases, the impedance of the inductance becomes more dominant than that of the resistance. And, the inductances of the TSV and bump, L_{TSV} and L_{Bump}, are modeled in (2.11) and (2.12) [17, 18].

$$L_{TSV} = \frac{1}{2}\left(\frac{\mu_0 \mu_{r,TSV}}{2\pi} \times h_{TSV} \times ln\left(\frac{p_{TSV}}{\frac{d_{TSV}}{2}}\right)\right)[\text{H}] \tag{2.11}$$

$$L_{Bump} = \frac{1}{2}\left(\frac{\mu_0 \mu_{r,Bump}}{2\pi} \times h_{Bump} \times ln\left(\frac{p_{TSV}}{\frac{d_{Bump}}{2}}\right)\right)[\text{H}] \tag{2.12}$$

They are derived from the loop inductance model between two parallel conducting wires. The L_{TSV} and L_{Bump} terms are equivalently separated into the signal and ground TSV/bumps. L_{TSV} and L_{Bump} are also calculated using structural parameters, such as d_{TSV}, p_{TSV}, h_{TSV}, d_{Bump}, and h_{Bump} and material properties, such as the permeability of the TSV, $\mu_{r,TSV}$. L_{TSV} values depending on dimension variations are plotted in Fig. 2.15 based on the proposed equations. As shown in

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Fig. 2.15, TSV inductance is 12 pH when diameter of 10 μm and the height of 60 μm which has much lower inductance than the inductance of a bond wire which has nH order.

2.2.2 Simulation and Measurement-Based Verification of the Proposed Equivalent Circuit Model

To verify the proposed scalable model of a TSV channel, S-parameters from the proposed model and a 3D field solver are compared in this section. From the comparison with variations of d_{TSV}, h_{TSV}, and p_{TSV}, the scalability of the proposed model is successfully validated up to 20 GHz. The proposed model is also experimentally validated by fabricating a series of fabricated test vehicles, which include TSVs, bumps, and RDLs.

2.2.2.1 Simulation-Based Verification of the Proposed Scalable Model of a TSV with Bumps

The scalability of the proposed TSV channel model is verified by simulation with the 3D field solver, HFSS^{TM} of Ansoft. Among many design parameters, d_{TSV}, h_{TSV}, and p_{TSV} are swept to validate the scalability of the proposed model up to 20 GHz. As shown in Fig. 2.16, the scalability of the proposed model is successfully verified.

As shown in Fig. 2.16a, the proposed scalable model is verified with d_{TSV} variations. As d_{TSV} varies from 10 to 30 μm, the S_{21} magnitude increases over the entire frequency range. The proposed scalable model estimates the change of the S_{21} magnitude and S_{21} phase well as compared to those computed from the 3D field solver with d_{TSV} variation. Even TSV diameter keeps shrinking as technology advances, TSVs on silicon interposer, which redistribute signals from the chip to the package do not have to be very small whose diameter is under 10 μm. Thus, the variation range of the TSV diameter in this simulation covers the dimension of not only on-chip TSV but also on-interposer TSV.

The proposed model with h_{TSV} variation is also validated, as shown in Fig. 2.16b. As h_{TSV} increases, the insertion loss, as shown by the S_{21} magnitude, increases. These results are due to the increased capacitance and conductance of the silicon substrate, resulting in the decreased impedance between signal and ground TSVs. It makes the insertion loss of the channel increase. The proposed scalable model estimates the S_{21} magnitude and S_{21} phase well as compared to the 3D field solver when h_{TSV} is varied from 30 to 70 μm.

As shown in Fig. 2.16c, the proposed scalable model with p_{TSV} variation is also validated. As p_{TSV} varies from 100 to 140 μm, there is a good agreement between the proposed scalable model and the 3D field solver up to 20 GHz.

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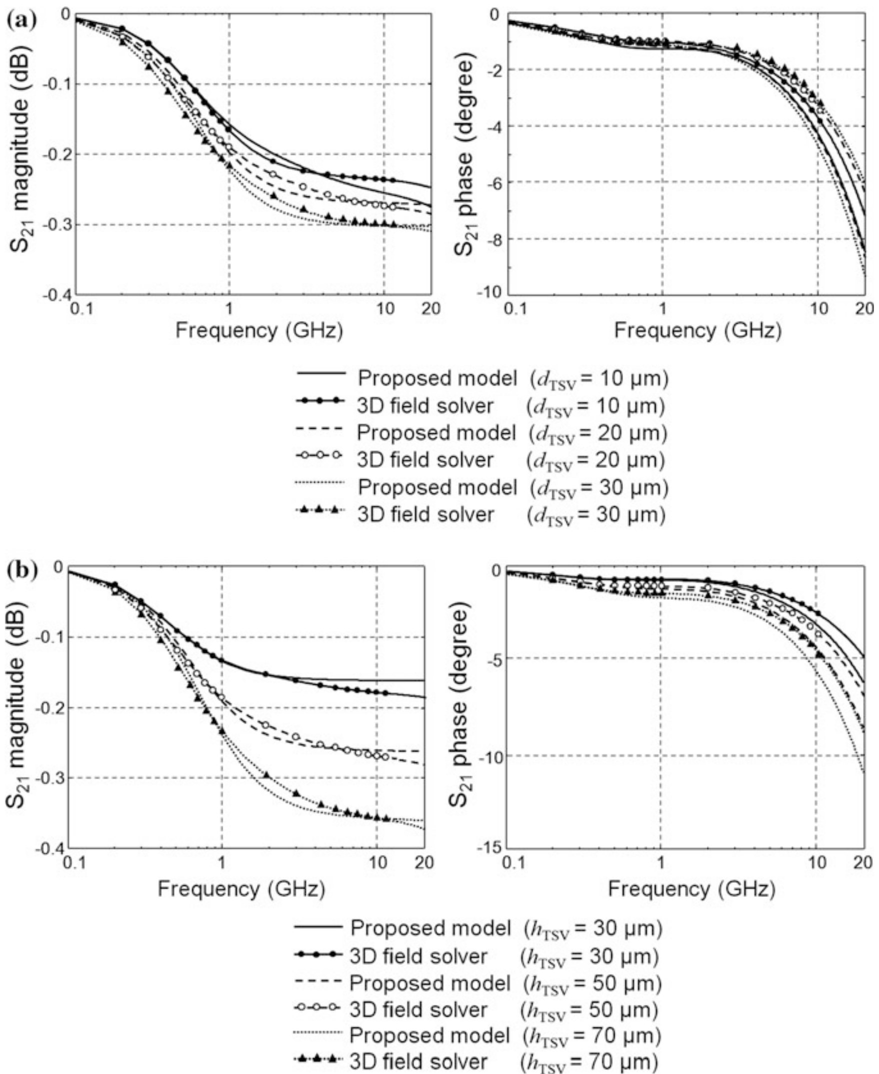

Fig. 2.16 S_{21} magnitudes and phases for the verification of the proposed scalable model of TSVs with bumps by comparing the proposed model to the simulation with a 3D field solver: **a** TSV diameter (d_{TSV}) **b** TSV height (h_{TSV}), and **c** TSV-to-TSV pitch (p_{TSV}). The other TSV and bump dimensions are fixed as d_{TSV} of 30 μm, h_{TSV} of 50 μm, p_{TSV} of 100 μm, t_{ox} of 0.5 μm, d_{Bump} of 50 μm, h_{Bump} of 10 μm, and h_{IMD} of 10 μm [15] © 2011 IEEE

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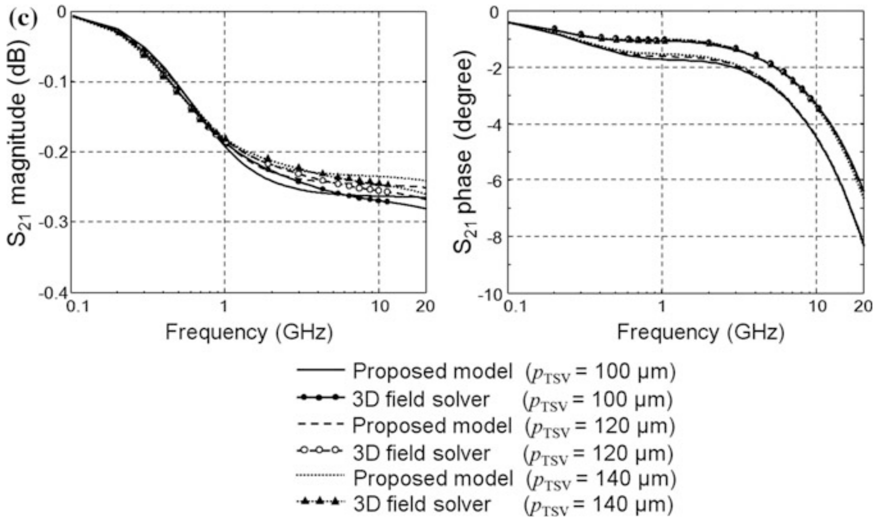

Fig. 2.16 continued

It should be observed, however, that there is an additional inductive effect from the inductance of the lumped ports when simulating with the 3D field solver, which causes increments of the slope of the S_{21} magnitudes over 10 GHz. Thus, there are some discrepancies between the calculated results from the proposed model and the simulation results from the 3D field solver over 10 GHz, as shown in Fig. 2.16a–c.

2.2.2.2 Experimental Verification of the Proposed Model of a TSV with Bumps and RDLs

To experimentally verify the proposed model, TSV channels are fabricated as for the test vehicles. The top view and the cross-sectional view of the fabricated TSV channel are shown in Fig. 2.17a, b, respectively. In order to measure the insertion loss through the TSV channel, TSVs are connected by stacking two dies. And the detailed dimensions are shown in Fig. 2.17c. There are two pairs of signal and ground TSVs on each side and each pair are connected each other by RDLs which are fabricated on the of the bottom die.

For the S-parameter measurements, on-chip cascade probes and a vector network analyzer (VNA), the Agilent N2530A, are used. Measurement results are compared to those from the proposed equivalent circuit model of the fabricated test vehicle.

The comparisons of the magnitudes and phases of both the S_{21} and S_{11} from the proposed model and measurement are shown in Fig. 2.18. The proposed model and the measurement are well correlated up to 20 GHz. As a result, we

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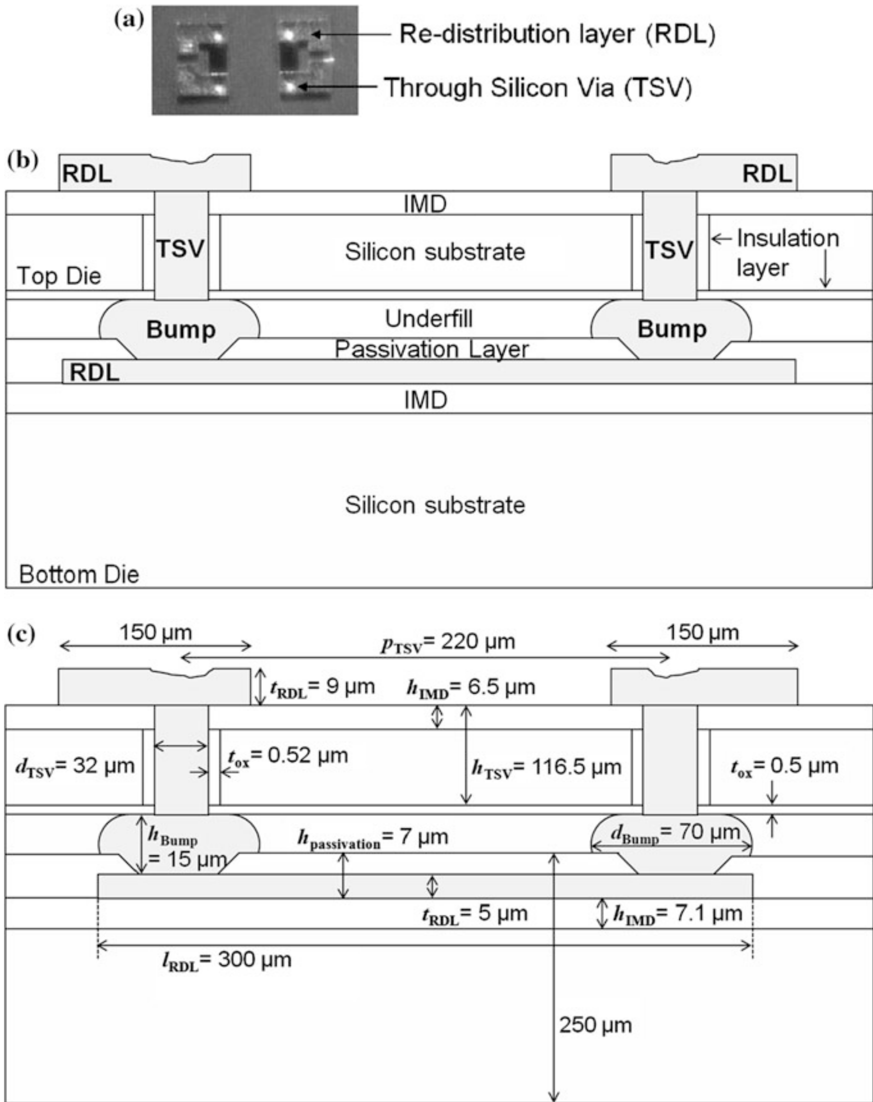

Fig. 2.17 **a** A top-view photograph of the test chip **b** the cross-sectional view and **c** the detail dimensions of the fabricated test vehicle, which is the TSV channel including the TSVs, bumps, and RDLs. The RDL on the bottom die provides horizontal connection between TSVs on the top die [15] © 2011 IEEE

experimentally verified the proposed electrical model of the TSV channel. It should be noted that the model for the verification includes the mutual effect between two TSV pairs on the top die.

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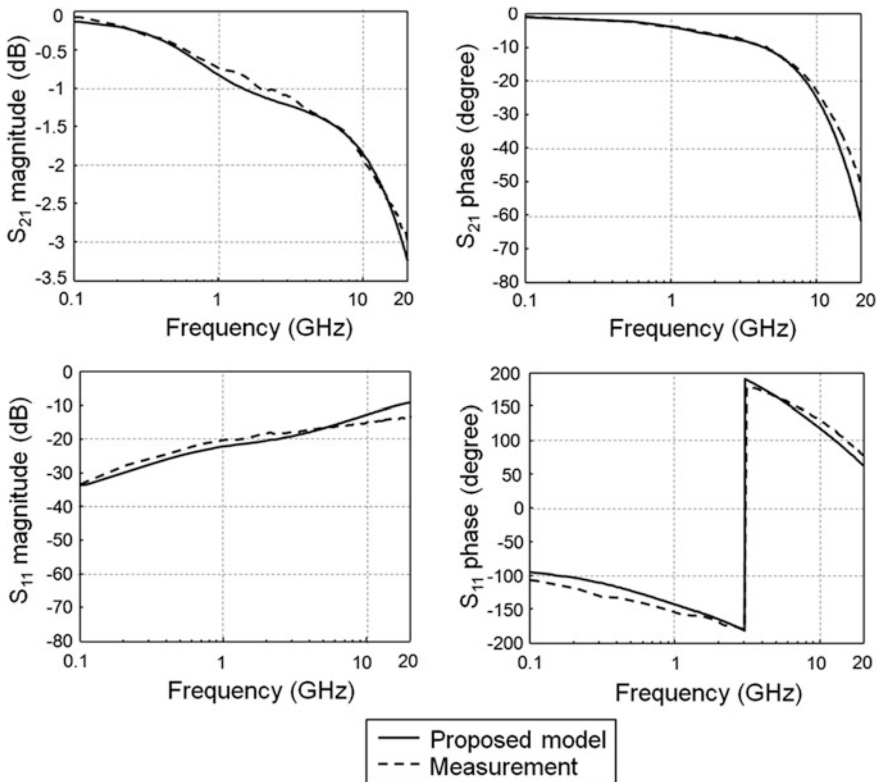

Fig. 2.18 Verification of the proposed model by comparing the measured S parameters with the calculated S parameters from the model [15] © 2011 IEEE

With the verified model, the electrical behavior of a TSV channel can be analyzed; the proposed analytic and closed-form equations can be used to estimate the power consumption, propagation delay, and timing skew of a TSV channel. The equations can also be combined with other circuits to evaluate the signal performance in 3D IC design. Since the model is scalable, it can estimate the electrical behavior depending on design parameters.

In Sect. 2.3, the electrical characteristics of the TSV channel are analyzed with the experimentally verified scalable model. Since the proposed model has scalability, the impact of each design parameter on the electrical behavior of the TSV channel can be easily analyzed. Then, the dominant *RLGC* components are analyzed which dominantly determine the insertion losses of the TSV channel in different frequency ranges.

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2.3 Electrical Characterization and Analysis of a TSV Channel

In this section, the electrical characteristics of a TSV channel are analyzed with the proposed scalable equivalent circuit model, which is experimentally verified in Sect. 2.2.2.2. The configuration of the TSV channel, which is used for the analysis in this section, is the same as that of the fabricated test vehicle. The TSV channels are analyzed as varying t_{ox}, d_{TSV}, p_{TSV}, h_{TSV}, RDL length (l_{RDL}), and σ_{Si}. In the frequency-domain analysis, the dominant design parameters are determined in specific frequency ranges by analyzing the insertion losses with S_{21} magnitudes. In addition, the frequency-dependent loss of the TSV channel is analyzed by categorizing the measured frequency range into three parts: region [A] for 0–2 GHz, region [B] for 2–10 GHz and region [C] for 10–20 GHz. In addition, eye diagram measurements with data rates up to 10 Gbps are conducted for the time-domain analysis of the TSV channel.

2.3.1 Frequency-Domain Analysis for Electrical Characterization of a TSV Channel

For the TSV structure, an insulation layer has to be formed to isolate the TSV from the conductive silicon substrate. The capacitance, $C_{Insulator}$ is directly affected by variation in t_{ox} which is explained in the proposed equation in Sect. 2.2.1. Thus, $C_{Insulator}$ increases as t_{ox} decreases. As t_{ox} decreases from 0.5 to 0.1 μm, $C_{Insulator}$ increases from 0.8 pF to 3.9 pF. The insertion loss through the TSV is dominated by the leakage through the conductive silicon substrate after passing through the insulator. As a result, an increase of $C_{Insulator}$ results in increased insertion loss due to the lowered impedance along the leakage path to the silicon substrate given by the equation, $Z = 1/j\omega C$. Therefore, the insertion loss through a TSV can be reduced by increasing the thickness of the insulator.

However, with current technology to form an insulation layer around a TSV, the thickness of the insulator, which is generally SiO_2, is limited to under 0.5 μm. This is due to process limitations in oxidizing a via with a high aspect ratio, which is also related to cost. In addition, the value of $C_{Insulator}$ is relatively big as compared to that of other parasitic capacitances of a few fF such as the $C_{Underfill}$, C_{IMD}, and C_{Bottom}. In a similar manner, if the thickness of the bottom oxide, $t_{ox,bot}$, decreases, the impedance of C_{Bump2} rapidly decreases as frequency increases. With $t_{ox,bot}$ of 0.5 μm, C_{Bump2} is 0.2 pF. Thus, if $t_{ox,bot}$ decreases and d_{Bump} increases, C_{Bump2} can bring more significant impact than $C_{Insulator}$ in region [A].

Therefore, the capacitive effect due to the insulation layer dominates the capacitive characteristic in the low frequency range, region [A], as shown in Fig. 2.19a. In this region, the insertion loss rapidly increases as frequency increases due to the decreasing impedance of $C_{Insulator}$.

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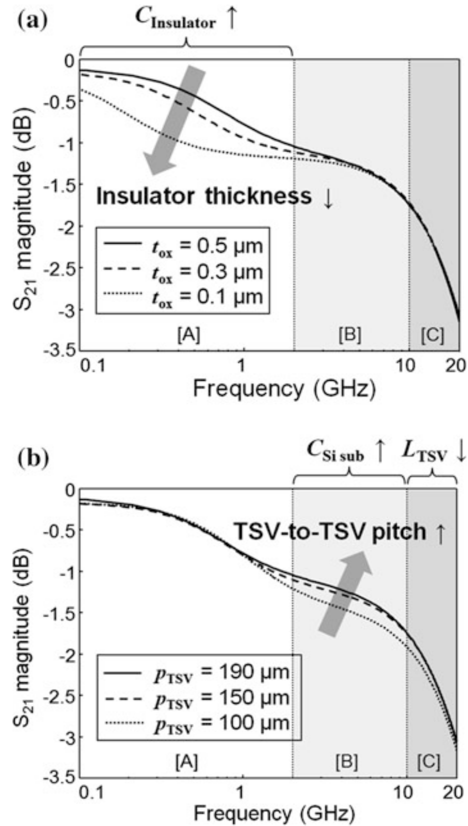

Fig. 2.19 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (**a**) TSV Insulator thickness variation and (**b**) TSV-to-TSV pitch variation [15] © 2011 IEEE

In addition, there is another loss term from the silicon substrate under the RDL, G_{sub} [15]. It also contributes to the insertion loss through the TSV channel. If the height between the RDL and the silicon substrate becomes smaller and the length of the RDL increases, the effect from G_{sub} increases [23, 24]. Thus, the resistive losses from the RDL itself and the silicon substrate under the RDLs become significant as the length of the RDL increases beyond a mm, and the width and thickness of the RDL decreases in 3D IC design. The significant factor that determines the amount of resistive loss through a TSV is the silicon substrate because it is conductive and TSVs are formed passing through it vertically.

There is one another resistive loss factor from the TSV itself, R_{TSV}. The resistive loss from R_{TSV}, in the case that it is made from copper, is negligible due to the comparatively small value of resistance, which is a few mΩ. If the metal filling the TSV is tungsten or poly silicon, which has a higher resistivity than copper, the resistive loss due to R_{TSV} will contribute more to the overall resistive loss through the TSV interconnect. There is no significant change in the insertion loss for region [C], even with the decrease of p_{TSV} resulting in an increase of $C_{Si\,sub}$ and $G_{Si\,sub}$, which dominantly affect the loss term. This is due to the decrease in inductances

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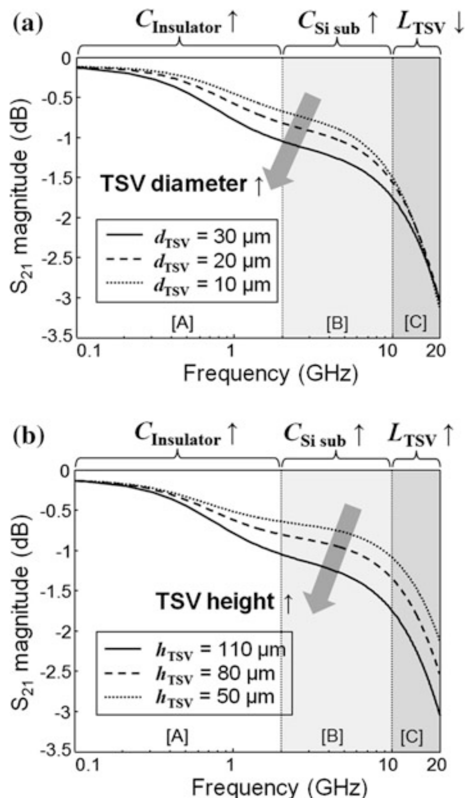


Fig. 2.20 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (**a**) TSV diameter variation and (**b**) TSV height variation [15] © 2011 IEEE

such as L_{TSV}, L_{Bump}, and L_{RDL}, as p_{TSV} decreases. A decrease in the inductance of the TSV channel reduces the insertion loss in region [C]. Thus, the effects on the insertion loss from the decreased inductance and increased $C_{Si\,sub}$ and $G_{Si\,sub}$ compensate each other in region [C] and make the loss steady even with the p_{TSV} varying. As a result, pitch variation dominantly affects the electrical characteristic of a TSV channel in region [B]. In addition, this effect is gradually reduced as frequency increases over 10 GHz due to the increased inductance effect from the TSVs, bumps, and RDLs.

Variation in d_{TSV} changes almost all the *RLGC* components of the proposed equivalent circuit model of a TSV channel. With increasing d_{TSV}, the effective distance between the signal and ground TSV decreases, when p_{TSV} is fixed. Therefore,

$C_{Si\,sub}$ and $G_{Si\,sub}$ increase, which increases the insertion loss. In addition, $C_{Insulator}$ increases due to an increase of the effective area where the TSV faces the silicon substrate through the insulation layer. Therefore, overall insertion loss in region [A] and [B] increases as d_{TSV} increases, as shown in Fig. 2.20a.

In a similar manner with the previous analysis for p_{TSV} variation, the decreased inductance effect from L_{TSV}, which makes the insertion loss constant even with the

increase of $C_{Si\,sub}$ and $G_{Si\,sub}$, is shown in region [C], Fig. 2.20a. As d_{TSV} increases from 10 to 30 μm, L_{TSV} decreases from 20.8 pH to 14.7 pH. Thus, there are no big insertion loss changes even with d_{TSV} variation in region [C]. In addition, R_{TSV} also decreases as d_{TSV} increases. However, this resistance is too small to be considered as discussed in the previous analysis for p_{TSV} variation.

Thus, the overall characteristic of the TSV channel with d_{TSV} increasing results in the increased insertion loss, which is dominantly determined by $C_{Si\,sub}$ and $G_{Si\,sub}$. In summary, d_{TSV} affects the frequency dependent loss of the TSV channel in almost all frequency ranges, but is dominant in regions [A] and [B].

As shown in Fig. 2.20b, the insertion loss of the TSV channel increases in all frequency ranges as h_{TSV} increases from 50 to 110 μm, because it not only increases $C_{Insulator}$ and $C_{Si\,sub}$, but also increases L_{TSV}. Therefore, the increasing h_{TSV} increases the insertion loss in all frequency ranges, regions [A], [B], and [C].

In a similar manner to the analysis of t_{ox} variation, $C_{Insulator}$ dominantly affects the insertion loss in region [A]. In region [B], $C_{Si\,sub}$ and $G_{Si\,sub}$ are the dominant factors that determine the insertion loss as analyzed for both p_{TSV} and d_{TSV}. In region [C], the inductances of the TSV channel start to affect the insertion loss.

As shown in Fig. 2.21a, as length of the RDL, l_{RDL}, increases from 220 to 660 μm, the insertion losses in regions [B] and [C] increase due to an increase in the inductance and the resistance of the RDL, L_{RDL} and R_{RDL}. From this analysis, it is apparent that regions [B] and [C] are dominantly affected by the inductive characteristic of the RDL. As l_{RDL} increases from 220 to 660 μm, L_{TSV} increases from 150 pH to 452 pH. As the operating frequency increases over a few Gbps, the RDL routing becomes a critical design issue for high-speed 3D IC channel design to guarantee the signal quality of the channel.

Silicon conductivity, σ_{Si}, is a material property that has a considerable influence on the electrical characteristics of the TSV channel. Because it changes $G_{Si\,sub}$ and G_{sub}, which determines overall insertion loss of a TSV channel. As σ_{Si} increases from 10 S/m to 50 S/m, $G_{Si\,sub}$ increases from 1.4 mS to 6.98 mS. As a result, the insertion loss of the TSV channel increases. The σ_{Si} change does not dominantly affect the insertion loss in region [A], however, in regions [B] and [C], it does. Therefore, the important design parameters of the TSV channel in 3D IC are not only the physical parameters but also the material properties.

In summary, the electrical characteristics of the TSV channel are analyzed with insertion loss data up to 20 GHz. The TSV channel has capacitive and resistive characteristics, and is also frequency dependent. The overall loss of the TSV channel is determined to be dominated by the conductance of the silicon substrate. If the RDL length increases to the mm range, the RDL contributes significantly to the loss of the TSV channel. The overall electrical behavior has a capacitive characteristic from the parasitic capacitances whose impedances change as frequency varies. However, the frequency dependence is determined to be dominated by the parasitic inductances of the TSV channel over 10 GHz. As a result, the capacitive TSV effect is dominant in the lower frequency range, and the inductive RDL effect becomes dominant in the higher frequency range.

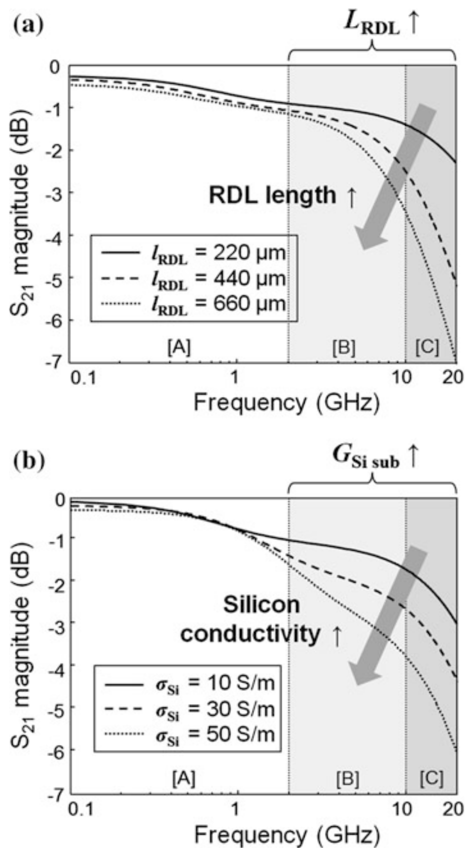


Fig. 2.21 S_{21} magnitudes from the proposed equivalent circuit model of a TSV channel with (**a**) RDL length variation and (**b**) conductivity of the silicon substrate [15] © 2011 IEEE

With these analyses, we summarize the design parameters and *RLGC* components which have a major impact on the frequency dependent loss of the TSV channel. As shown in Fig. 2.22, there are design parameters which dominantly determine the frequency dependent loss of the TSV channel; t_{ox}, $t_{ox,bot}$ and d_{TSV} in region [A], p_{TSV} and h_{TSV} in region [B], h_{TSV} and l_{RDL} in region [C]. Additionally, the dominant *RLGC* components of the proposed model of the TSV channel are summarized; $C_{Insulator}$ in region [A], $C_{Si\,sub}$ in region [B], L_{TSV} and L_{RDL} in region [C]. Other *RLGC* components which have a minor impact in each frequency range are summarized; C_{Bump2} have a minor impact in region [A], $C_{Underfill}$, C_{IMD}, C_{Bottom}, C_{RDL}, $C_{RDL_to_sub}$ and C_{sub}, have a minor impact in region [B] and [C] [15].

2.3.2 Time-Domain Analysis of a TSV Channel

For the time-domain analysis, eye diagram measurements are conducted on the fabricated TSV channel, which includes the TSVs, bumps, and RDLs. The input

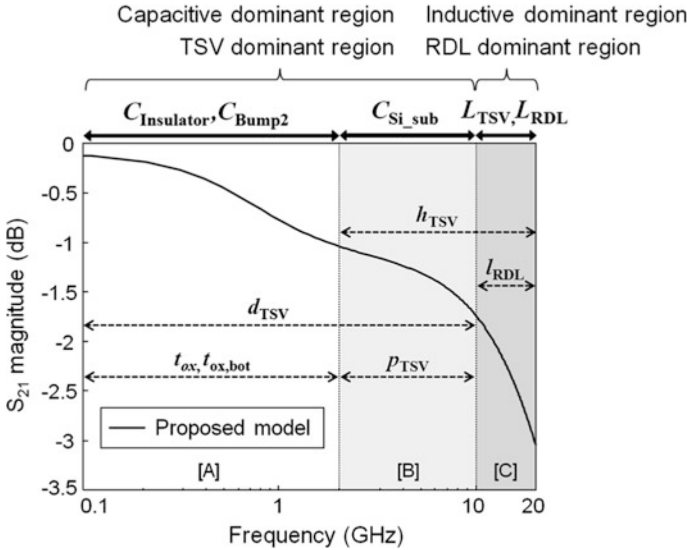


Fig. 2.22 S_{21} magnitude from the proposed model showing dominant design parameters and *RLGC* components, which determine the insertion loss for the different frequency ranges: in the lower frequency range, the capacitive TSV effect dominates; in the higher frequency ranges, the RDL effect, which is inductive, becomes dominant [15] © 2011 IEEE

signal is a $2^{31} - 1$ pseudo-random bit sequence with an amplitude of 500 $mV_{p\text{-}p}$. The output waveforms are monitored using a digital sampling oscilloscope, Tektronix/TDS8000B, equipped with a 20 GHz sampling module.

The eye diagrams from the measurement and the proposed model with data rates of 1 Gbps, 5 Gbps, and 10 Gbps with random data of $2^{31} - 1$ bits transmitting through the fabricated TSV channel are shown in Fig. 2.23. The shapes of the eye diagrams from the measurement and the proposed model are matched well. However, there are some differences in the eye opening and the pk-pk jitter between the measurement and the proposed model. Those differences are due to the cables used for the measurement that bring additional 1.4 dB, 3.6 dB, and 4.3 dB losses at 500 MHz, 2.5 GHz, and 5 GHz, respectively. Therefore, the eye openings with 1 Gbps, 5 Gbps and 10 Gbps random data are smaller than that from the proposed model by several tens of mV.

In addition, the measured pk-pk jitter is larger than that from the proposed model by 6–7 ps, because there is random jitter produced from the measurement equipment, the pulse pattern generator (PPG), and jitter additionally caused by the two cables used for the measurements.

From the measured eye diagrams in Fig. 2.23, as the data rate increases, the voltage and timing margins decrease, which are presented with the normalized eye-opening and pk-pk jitter. The normalized eye-opening and pk-pk jitter are 83.4 % and 0.8 %, respectively, for data rates of 1 Gbps. As the data rate is increased to 5 Gbps and 10 Gbps, the normalized eye-opening decreases to 70.6 %

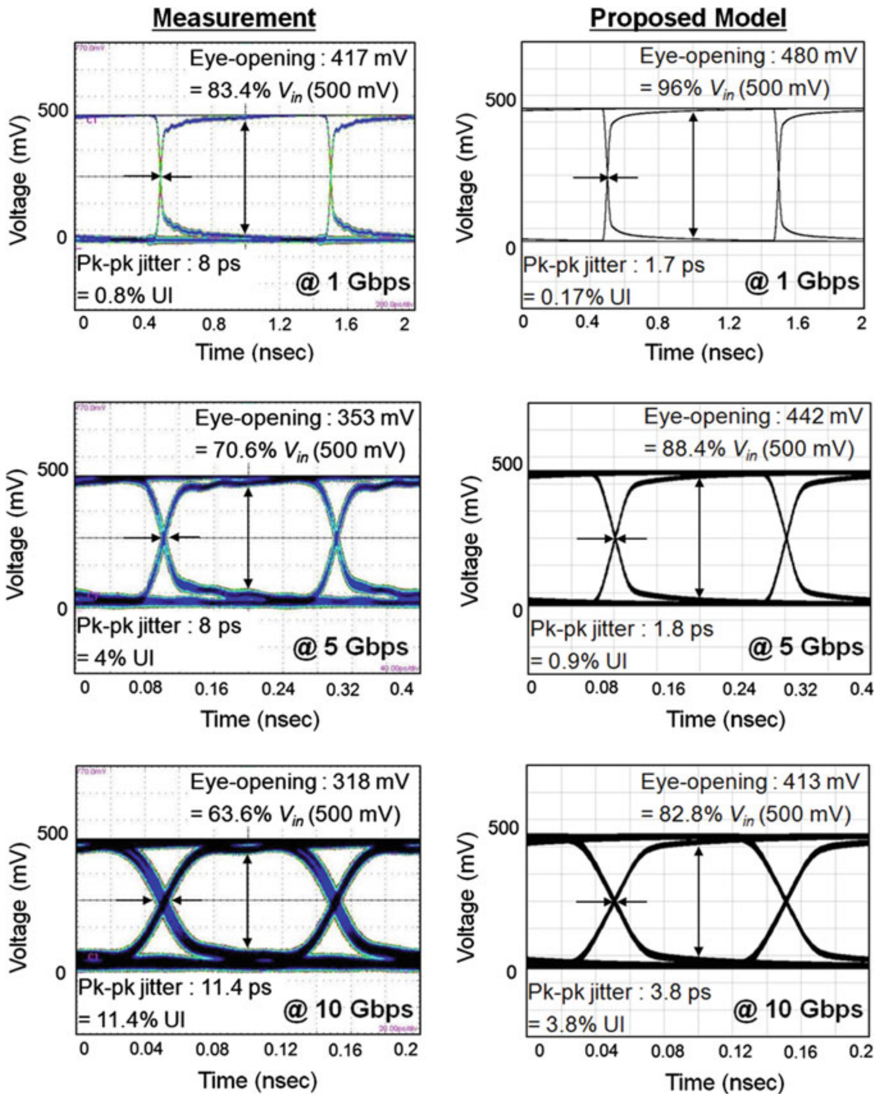


Fig. 2.23 Eye diagrams from the measurement and the proposed model with 1, 5, and 10 Gbps random data of $2^{31} - 1$ bits traveling through the fabricated TSV channel. As the data rate increases, the normalized eye opening decreases and the normalized pk-pk jitter increases due to the frequency dependent loss of the TSV channel, which are capacitive and resistive [15] © 2011 IEEE

and 63.6 % and the normalized pk-pk jitter increases to 4 % and 11.4 %. Signals through the TSV channel, however, have open eyes because of the short interconnection length of the TSV and RDL, even with a data rate of 10 Gbps.

Since the TSV channel has capacitive and resistive characteristics as analyzed in Sect. 2.3.1 on the frequency-domain analysis, it has a frequency dependent loss. In addition, because the energy of the signal is predominantly concentrated at the Nyquist frequency, the insertion loss is not constant in frequency domain, however, increases as the data rate increases. Thus, the amount of signal degradation through the TSV channel increases as the frequency increases. For example, the energy of the signal with a data rate of 1 Gbps is mostly concentrated at 0.5 GHz. From the measurement results, the insertion loss at 0.5 GHz for the TSV channel is −0.5 dB. However, with a data rate of 10 Gbps, the TSV channel has insertion loss at the Nyquist frequency, 5 GHz, of −1.5 dB. Thus, the frequency dependent loss in the frequency domain directly results in the increase of the rise time of the signal in the time domain as operating frequency increases. Furthermore, if the frequency dependent loss of the TSV channel becomes severe, it can cause intersymbol interference (ISI), which is the signal degradation of the timing and signal integrity margins.

However, as 3D integration density increases, the number of dies, which have to be vertically integrated in one system, increases. Thus, high-speed I/O signals pass through many TSVs. This can cause an additional capacitive load due to the increasing parasitic capacitances of the TSVs. It results in an increased timing delay, lowered slew rate and increased timing jitter of the signal. Based on the model and analysis of the TSV channel in the previous sections, as d_{TSV} and h_{TSV} becomes smaller or t_{ox} becomes thicker, the capacitive load due to the TSV can be reduced. Therefore, we can sharpen the rising edge of the signal for better system performance and increases the bandwidth of the TSV interconnect by optimizing d_{TSV}, h_{TSV}, and t_{ox}. In a similar manner, if there are more than two RDL layers and are densely routed, the capacitive load from the RDLs also increases and it will significantly affect to the overall signaling performance of the channel. In order to optimize the RDL design, it is necessary to minimize the capacitance due to RDLs by reducing w_{RDL}, increasing S_{RDL}, and minimizing the routed length of RDLs.

Since 3D IC design has still challenging issues in terms of yield and cost, many of industries currently focus on 2.5D integration using a silicon interposer which is a marginal silicon die enabling 2-dimensional multi-chip integration on a silicon die and provides RDLs as for the chip-to-chip interconnect on die and TSVs in order to redistribute the pins from the integrated chips to the package and the printed circuit board. In this case, the portion of RDLs along the 3D IC channel is very significant, and the length of RDLs has several mm order which may result in a severe signal degradation due to the increased RC delay, insertion loss and crosstalk effect. Therefore, the impact on high-speed signaling, I/O power consumption and routability issues from the RDL design have to be also carefully concerned for the advanced 3D IC channel design.

Eye diagrams which are computed with the proposed model are shown in Fig. 2.24, for signals passing through a different number of TSV pairs and RDLs. As the number of TSVs that the signal is traveling increases from two to eight, and the length of RDL increases from 500 to 2 mm, the eye-opening decreases 10 % and the pk-pk jitter increases 0.2 %. We can confirm the effect from the increased

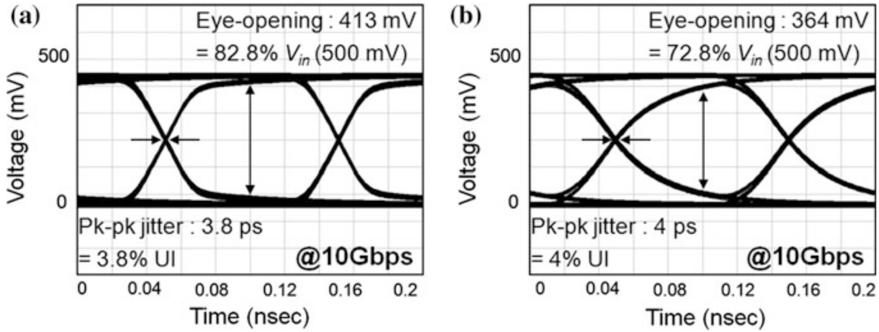


Fig. 2.24 Eye diagrams of the proposed model with 10 Gbps pseudo-random data traveling through (**a**) two TSV pairs and RDLs; and (**b**) eight TSV pairs and RDLs [15] © 2011 IEEE

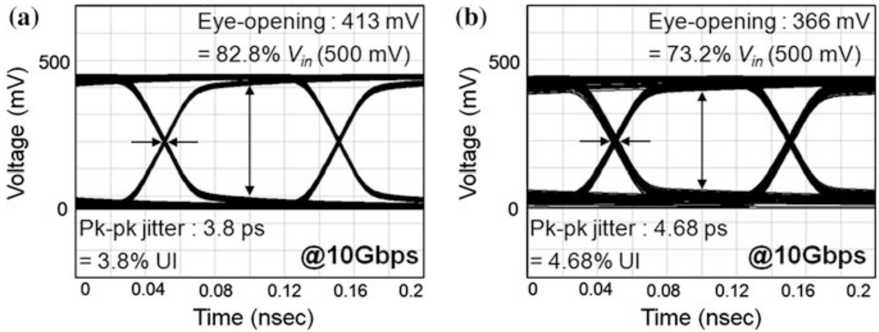


Fig. 2.25 Eye diagrams of the proposed model with 10 Gbps random data traveling through two TSV pairs and RDLs with (**a**) t_{ox} of 0.5 µm; and (**b**) t_{ox} of 0.1 µm [15] © 2011 IEEE

capacitance of the TSV channel with these computed eye diagrams from the proposed model. Even though the eye is still clearly open, if the coupling ratio among the TSVs increases significantly or the RDL coupling increases from the long and dense routing, the eye can become more degraded.

In addition, as analyzed in the frequency-domain analysis, if the thickness of the insulator, t_{ox}, becomes thinner, the insertion loss of the low frequency components, especially under 2 GHz, increases, even though the high frequency components almost does not change. Hence, as shown in Fig. 2.25, the slope of the rising edge, where the high frequency components are concentrated, does not change, when the t_{ox} is decreased from 0.5 to 0.1 µm.

Therefore, we analyzed and confirmed the frequency-dependent loss of a TSV channel in the time domain, which was characterized in the frequency domain in Sect. 2.3.2 (Fig. 2.26).

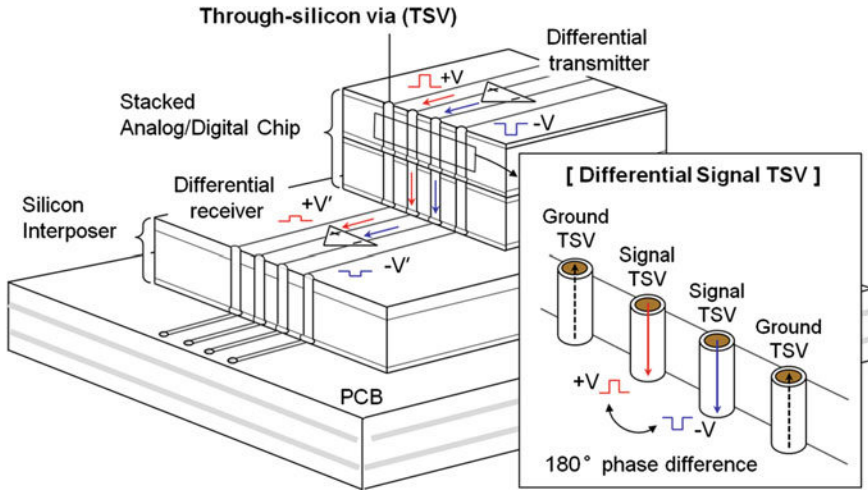


Fig. 2.26 A conceptual 3-dimensional integrated circuit (3D IC), which includes vertical integration of dies with differential signal through-silicon vias (TSVs). For differential signaling, there are two signal TSVs, which transfer the signals with the same amplitude but are out-of-phase [25]

2.4 Electrical Analysis of a Single-Ended and Differential Signal TSV Channel

For reliable high-speed signaling with high noise immunity, a differential signaling scheme is generally preferred for higher system performance than a single-ended signaling scheme. However, based on the simulation results from Sect. 2.3.2, differential signal TSVs also have frequency-dependent loss and capacitive-dominant characteristics, which can degrade the high-speed signal transmission. Thus, a differential signaling scheme (GSSG-type) is compared to a single-ended signaling scheme (GSG-type) by analyzing the insertion loss, characteristic impedance, TDR waveform, and eye diagram in this section. Then, the pros and cons of using differential signaling rather than single-ended signaling with TSVs are analyzed.

For the differential signaling scheme, a GSSG-type differential signal TSV is modeled and analyzed in this paper. The electrical behavior is compared with a single-ended signaling scheme by selecting a GSG-type configuration. The dimensions and material properties of the TSVs, bumps, and metal lines are described in Tables 2.1 and 2.2. The top views of the fabricated test vehicles of the GSSG-type and GSG-type are illustrated in Fig. 2.27. The performance analysis and comparison are conducted with frequency domain measurements including insertion loss and characteristic impedance, and time domain measurements such as a TDR waveform and eye diagram of the two signaling schemes.

Table 2.1 Design parameters and the corresponding dimensions of the fabricated differential signal TSV [25]

Design parameter	Dimension (μm)
TSV diameter (d_{TSV})	45
TSV height (h_{TSV})	60
TSV oxide thickness (t_{ox})	0.25
TSV-to-TSV pitch (p_{TSV})	250
Bump diameter (d_{bump})	120
Bottom metal line length (I_{RDL})	360
Bottom metal line width (w_{RDL})	100
Metal line thickness (t_{RDL})	2
Metal via diameter	30
Metal via height	4
Metal pad diameter	40
Metal pad thickness	2

Table 2.2 Material parameters with symbols and values for the fabricated differential signal TSV [25]

Material parameter	Value
Conductivity of Silicon substrate (σ_{Si})	10 (S/m)
Resistivity of TSV (p_{TSV})	1.68×10^{-8} (Ω·m)
Resistivity of bump (p_{Bump})	1.09×10^{-7} (Ω·m)
Resistivity of RDL (p_{RDL})	1.68×10^{-8} (Ω·m)
Relative permittivity of Silicon substrate ($\varepsilon_{r,\ si}$)	11.9
Relative permittivity of insulator ($\varepsilon_{r,\ Insulatori}$)	4
Relative permittivity of IMD ($\varepsilon_{r,\ IMD}$)	2.6
Relative permittivity of underfill ($\varepsilon_{r,\ Underfill}$)	1
Relative permeability of TSV ($\mu_{r,\ TSV}$)	1
Relative permeability of bump ($\mu_{r,\ Bump}$)	1
Relative permeability of RDL ($\mu_{r,\ RDL}$)	1

2.4.1 Frequency-Domain Measurement and Analysis of Single-Ended and Differential Signal TSV Channel

Figure 2.28 shows the measured insertion losses, which are differential mode S_{21} magnitude for a differential signal TSV and S_{21} magnitude for a single-ended signal TSV up to 20 GHz. From comparing the results, we noticed that the GSSG-type has larger insertion loss than that of the GSG-type over almost all of the frequency range up to 20 GHz. This difference is due to the equivalent capacitance and conductance difference that a signal encounters. Because a silicon substrate has losses, if the capacitance and conductance of the silicon substrate increase, the insertion loss increases. For the GSG-type, a signal TSV has two ground TSVs near a signal TSV with a pitch of p_{TSV}. However, for the GSSG-type, the mutual capacitance and conductance between the signal TSVs is effectively double the value of the GSG-

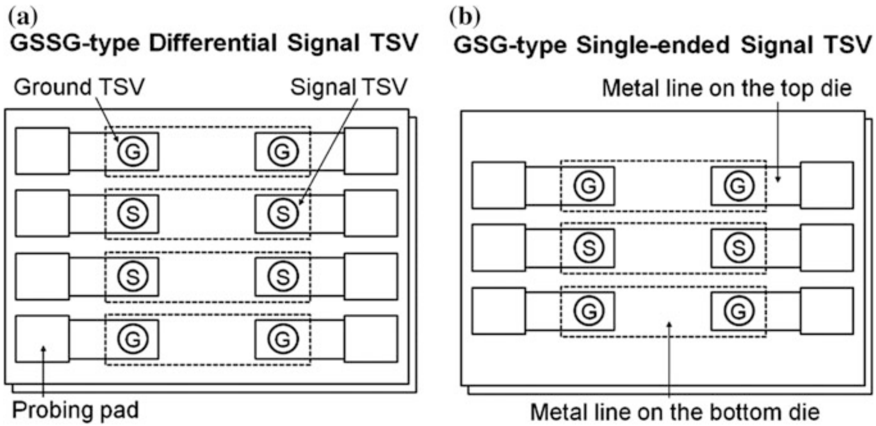


Fig. 2.27 Top view of the fabricated test vehicles of a (**a**) GSSG-type differential signal TSV and (**b**) GSG-type single-ended signal TSV for performance comparison and analysis. Two dies are stacked to connect the TSVs on the *top* die with *metal lines* on the *bottom* die [25]

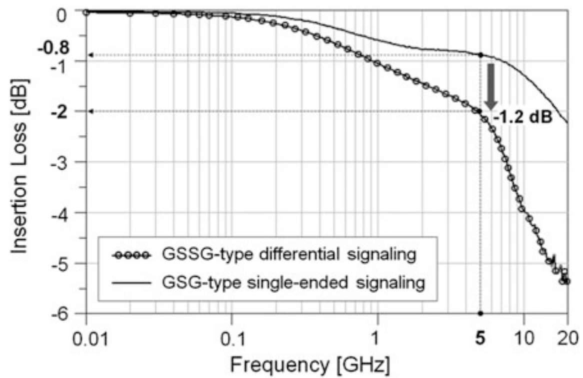


Fig. 2.28 Insertion losses from measured differential-mode S_{21} magnitude of the GSSG-type differential signal TSV and S_{21} magnitude of the GSG-type single-ended signal TSV up to 20 GHz. At 5 GHz, insertion loss of the GSSG-type is 1.2 dB larger than that of the GSG-type [25]

type due to the virtual ground effect. Thus, the GSSG-type has a larger capacitance and conductance than GSG-type. Thus, the GSSG-type has 1.2 dB larger insertion loss than the GSG-type at 5 GHz.

Next, we analyze the characteristic impedances from both signaling schemes. The characteristic impedance is computed from the measured S-parameters in Fig. 2.29.

From the Fig. 2.29, the odd-mode impedance of the GSSG-type has lower characteristic impedance than the GSG-type for all frequencies. This phenomenon is because the GSSG-type has a larger equivalent capacitance and conductance than the GSG-type. Since there is a virtual ground between two signal TSVs in case of differential signaling, the effective parasitic capacitance to the ground which affects to the loading capacitance for the signal is larger than the

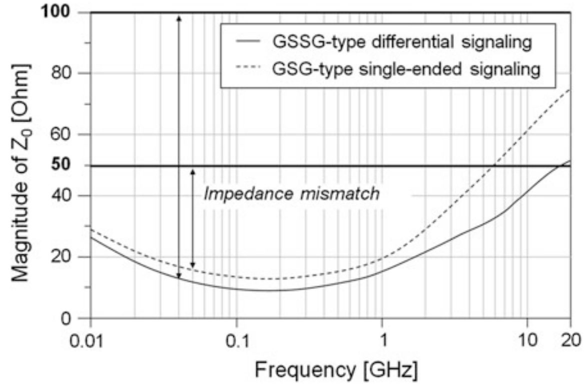


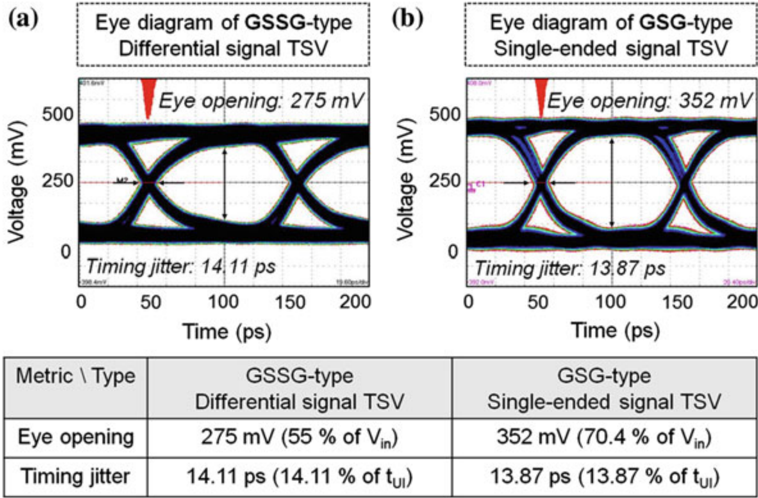
Fig. 2.29 The characteristic impedances of a GSSG-type differential signal TSV and a GSG-type single-ended signal TSV and the amount of the impedance mismatches from 100 Ohm for the differential signaling and 50 Ohm for the single-ended signaling [25]

single-ended signaling case. Additionally, the characteristic impedances of the GSSG-type and the GSG-type are less than 100 Ohm and 50 Ohm, respectively. Because a TSV has a thin insulation layer surrounding a via and has a short height, the capacitive characteristic of a TSV is more dominant than the inductive factor on the overall electrical behavior of a TSV. In terms of the characteristic impedance of TSV channels, even there's a large impedance mismatch due to TSVs along the channel, it does not result in serious signal degradation since the electrical length of a TSV is short enough.

However, if the operating frequency increases to hundreds of GHz and the number of stacked dies increases, the impact of the impedance mismatch cannot be ignored any more since the TSV channel becomes electrically long enough which has to be considered as a transmission line. The impedance of a differential signal TSV and a single-ended signal TSV can be controlled by optimizing the design parameters of a TSV. For example, a TSV with smaller via diameter, thinner oxide thickness, longer TSV-to-TSV pitch and shorter via height has the higher characteristic impedance. These design guidelines are the way to decrease the parasitic capacitance and also to increase the parasitic inductance of a TSV. Since the characteristic impedance varies as frequency increases, it is necessary to consider the Nyquist frequency of the target data when determining the target characteristic impedance of the TSV channel in order to minimize the impact of the impedance mismatch.

2.4.2 Time-Domain Measurement and Analysis of Single-Ended and Differential Signal TSV Channel

In this section, time-domain measurement and analysis of single-ended and differential signal TSV channel are presented with eye diagram and TDR measurements. In real design phases, the maximum timing and voltage margins of the channel are specified and have to be evaluated in order to guarantee the system



Metric \ Type	GSSG-type Differential signal TSV	GSG-type Single-ended signal TSV
Eye opening	275 mV (55 % of V_{in})	352 mV (70.4 % of V_{in})
Timing jitter	14.11 ps (14.11 % of t_{UI})	13.87 ps (13.87 % of t_{UI})

Fig. 2.30 Eye diagrams from measurements with a 10 Gbps pseudo-random bit sequence (PRBS) of data with $2^{31}-1$ bits traveling through (**a**) the GSSG-type single-ended signal TSV and (**b**) the GSG-type differential signal TSV of the fabricated test vehicles. The measured eye diagram includes the cable effect [25]

operation. Thus, it is necessary to analyze and evaluate the impact of the channel performance in time domain to meet the system requirements.

Based on the previous discussions on the frequency-domain analysis, it can be expected that the eye-diagrams of the signal passing through the GSSG-type differential signal TSV is worse than that of GSG-type single-ended signal TSV as shown in Fig. 2.30. The eye diagram is measured with 10 Gbps pseudo-random bit sequence (PRBS) of data with $2^{31}-1$ bits with a PPG and TDS 8000B. For the GSG-type, eye opening and timing jitter are 352 mV and 13.87 ps, respectively. For the GSSG-type, eye opening and timing jitter are 275 mV and 14.11 ps, respectively, which is a tighter voltage and timing margin than the GSG-type.

From the TDR waveforms, we can compare the capacitive or inductive characteristics of the channel. Figure 2.31 includes the measured TDR waveforms from the GSSG-type and the GSG-type. For the TDR measurements with GSSG-type, differential step pulses are injected, which have the same amplitudes but are out-of-phase, to obtain the differential reflected voltages. The straight line in Fig. 2.31 shows the TDR waveform from the GSSG-type and the dotted line shows that from the GSG-type. The capacitive peak from the GSSG-type is lower than that from the GSG-type. Thus, we confirm that the equivalent capacitance of the differential signal TSV (GSSG-type) is greater than that of the single-ended signal TSV (GSG-type), which was previously discussed in the modeling section.

Next, the coupled noise voltages with the GSSG-type and the GSG-type are measured. Figure 2.32 illustrates the top view of the fabricated samples for the measurements. The thinned dies with two pairs of GSSG-type and two pairs of

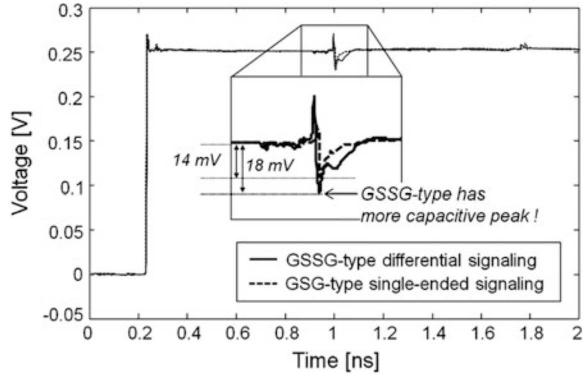


Fig. 2.31 TDR waveforms from the time-domain measurements with a 500 mV p-p step pulse with the GSSG-type differential signal TSV (*straight line*) and the GSG-type single-ended signal TSV (*dashed line*) [25]

GSG-type signal TSVs are fabricated. The dimensions of the structure are the same as those from the previous samples. However, the die is not stacked but is instead thinned to make TSVs open-ended.

For the measurement of a GSSG-type, differential clock signals with 250 mV peak-to-peak amplitude that are out-of-phase are used for the noise source at the aggressor, which is a pair of GSSG-type. The coupled noise voltages are measured at the opposite side of a GSSG-type signal TSV pair. Then, we subtract output voltages from the two signal TSVs of a GSSG-type signal TSV pair to obtain the differential output voltage. For the noise coupling measurement with the GSG-type, the measurement environment is similar. The input source is the clock signal with a 500 mV peak-to-peak amplitude and the coupled noise voltage is measured at the opposite side of a GSG-type signal TSV pair with an oscilloscope. The clock frequency is 1 GHz.

The measured coupled noise voltage waveforms are shown in Fig. 2.33. For the GSSG-type, the peak-to-peak noise voltage is 16 mV. For the GSG-type, the peak-to-peak noise voltage is 34 mV. From the measurements, a differential signal TSV (GSSG-type) is better in noise immunity than a single-ended signal TSV (GSG-type). Although differential signaling with TSVs results in a greater insertion loss and tighter voltage and timing margins, it still has the advantage of higher noise immunity for sensitive and high-speed systems.

Table 2.3 includes a comparison between a differential signal TSV (GSSG-type) and a single-ended signal TSV (GSG-type) based on the performance metrics, such as the number of TSVs, insertion loss, characteristic impedance, eye opening, timing jitter, and coupled noise voltage. Even with the advantage of a higher noise immunity for differential signaling, differential signaling with TSVs results in a more degraded signal transmission than single-ended signaling. Because a TSV is a capacitive interconnect due to the thin oxide layer and has leakage through the silicon substrate, the electrical behavior of differential signaling with TSVs is worse than that of a single-ended signaling with TSVs. To use differential signaling with TSVs in 3D ICs, we must consider these electrical behaviors.

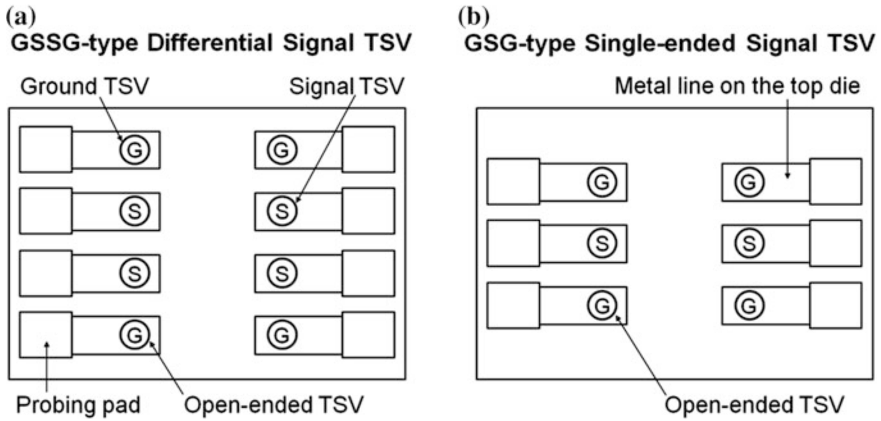


Fig. 2.32 Top view of the fabricated test vehicles of (**a**) a GSSG-type differential signal TSV and (**b**) a GSG-type single-ended signal TSV for performance comparison and analysis. The TSVs in the test vehicles are open-ended for the noise coupling measurements [25]

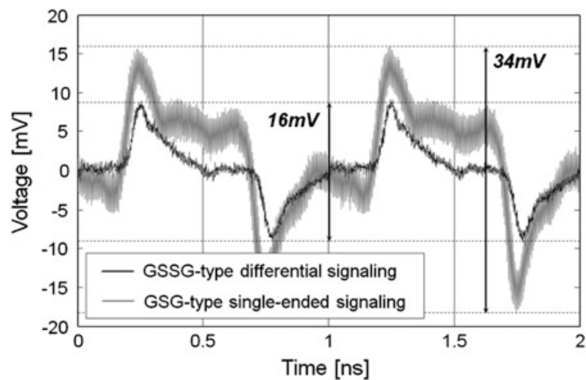


Fig. 2.33 The measured coupled noise voltage waveforms of the GSSG-type and GSG-type signal TSVs, which have peak-to-peak voltages of 34 mV and 16 mV, respectively [25]

Table 2.3 A comparison of various electrical characteristics for differential and single-ended signaling schemes [25]

Performance metrics	GSSG-type differential signaling	GSG-type single-ended signaling
Number of TSVs	4ea (GSSG)	3ea (GSG)
Insertion loss @ 5 GHz	−2 dB	−0.8 dB
Characteristic impedance (0.01–5 GHz)	27–52 Ω	28–78 Ω
Eye opening (V_{in} = 500 mV)	275 mV	352 mV
Timing jitter (t_{UI} = 80 ps)	14.11 ps	13.87 ps
Coupled noise voltage	16 mV	34 mV

2.5 Summary

In this chapter, the analytic scalable model of a TSV is proposed with closed-form equations which are functions of the design parameters, material properties and frequency. Based on the proposed model, the electrical characteristics of a TSV depending on design parameter variations are analyzed up to 20 GHz. The TSV channels are fabricated and measured for the model verification. The model is successfully verified by experimental results in frequency- and time-domain. In order to evaluate the signaling performance of single-ended and differential TSVs, the test vehicles are fabricated and measured for the analysis.

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Chapter 3
High-Speed TSV-Based Channel Modeling and Design

Heegon Kim, Jun So Pak and Joungho Kim

Abstract In this chapter, the modeling and analysis of a high-speed TSV-based channel are investigated. At the beginning of this chapter, the equivalent circuit models of TSV and silicon interposer interconnect are introduced. Based on the introduced equivalent circuit models, the electrical properties of the coaxial TSV and the silicon interposer interconnect are analyzed. In the case of the coaxial TSV analysis, the unique characteristic of the coaxial TSV comparing to that of the normal TSV is investigated. In the case of the silicon interposer interconnect analysis, the impact of the interconnect structure to the performance is intensively analyzed. The dominant impact of the silicon interposer interconnect to the performance of the total high-speed TSV channel is also analyzed. In addition, the measured S_{21} and eye-diagram of the high-speed TSV channel and the comparison of electrical properties between the high-speed TSV channel and the MCM channel are, respectively, demonstrated as examples. At the end of this chapter, a fast and precise worst-case eye-diagram estimation algorithm for high-speed TSV channel is introduced and experimentally verified.

Keywords High-speed TSV-based channel · Coaxial TSV · Silicon interposer · Channel loss (S_{21}) · Eye-diagram · Reflection · Worst-case eye-diagram estimation

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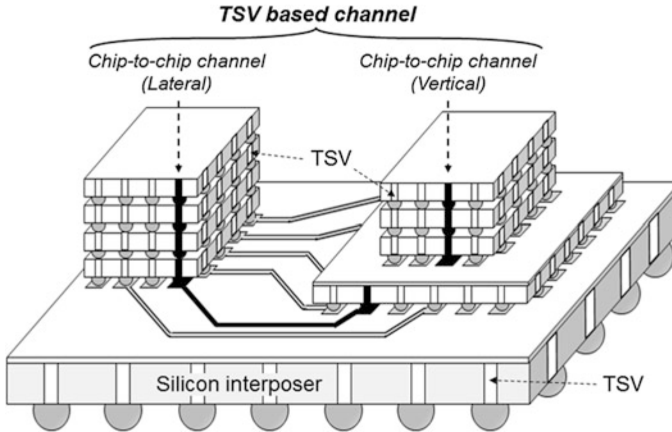


Fig. 3.1 Overview of high-speed TSV-based channel

3.1 Introduction

Spurred by industrial demand for integrated-circuit systems with improved channel bandwidths and compact sizes, TSV-based three-dimensional integrated circuits (3D ICs) technology is seen as a potential solution. As shown in Fig. 3.1, a TSV-based channel, which consists of TSVs and a silicon interposer interconnect, realizes lateral and vertical chip-to-chip interconnections with impressively short channel paths, resulting in improved channel bandwidth. Moreover, TSVs and silicon interposers provide a large number of I/Os—an essential requirement in the mobile memory shown in Fig. 3.2. This system enables not only higher memory bandwidth but also lower power consumption [1]. However, the number of I/Os cannot be increased infinitely due to routability issues. This means that a wider bandwidth per channel is required in a TSV-based system to satisfy the industrial demands of very wide system bandwidth. Though a TSV-based channel can enhance the bandwidth per channel by reducing the interconnect length, the signal integrity (SI) cannot be assured as the data rate increases due to the non-ideal properties of the channel such as channel loss and reflection [2]. Therefore, a SI analysis of a high-speed TSV-based channel is indispensable.

In this chapter, we investigate the modeling and analysis of a high-speed TSV-based channel. Because a high-speed TSV-based channel consists of TSVs and silicon interposer interconnects, both components should be analyzed at the same time. In Sect. 3.2, an equivalent-circuit model of TSVs and silicon interposer interconnects is introduced for an efficient analysis of the electrical properties of a high-speed TSV based channel. Though we already cover the analysis of TSV in the previous chapter, an additional analysis relating to the coaxial TSV is briefly covered in Sect. 3.3.1. In Sect. 3.3.2, the electrical properties of the silicon interposer interconnects are analyzed at various channel types, structures and

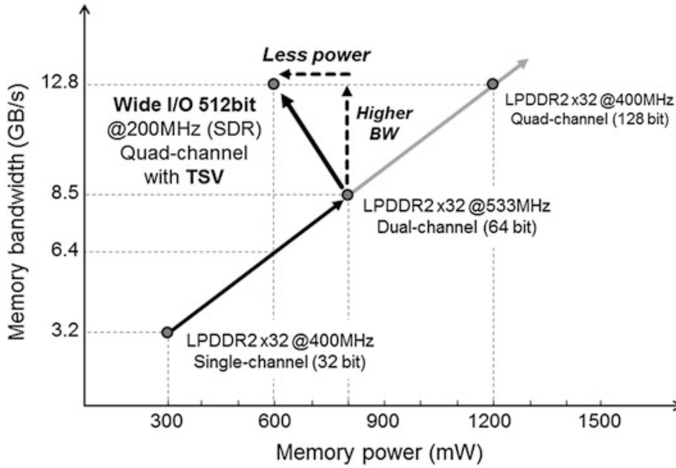


Fig. 3.2 Technical trend of mobile memory [1]

materials. In a realistic TSV-based channel design, the silicon interposer interconnect is the primary bottleneck for increasing the system bandwidth due to its long interconnect length. To analyze the dominance of the silicon interposer interconnect on the high-speed TSV-based channel, the portion of impacts of the TSV and the silicon interposer interconnect to the electrical properties of the TSV-based channel is analyzed at the end of Sect. 3.3.2. In Sects. 3.3.3 and 3.3.4, the measurement results of the high-speed TSV-based channel and the comparison results of the TSV-based channel, respectively, are compared to the channel in the MCM package that is typically employed for first-level packaging interconnections, and both are respectively demonstrated as examples. In addition, a fast and precise worst-case eye-diagram estimation algorithm (that enables efficient SI analysis for the high-speed TSV-based channel) is introduced and experimentally verified in Sect. 3.4.

3.2 Model of High-Speed TSV-Based Channel

In this section, the equivalent-circuit models for a high-speed TSV-based channel are introduced. The models for the high-speed TSV-based channel are classified as models of a TSV in a stacked die, a silicon interposer interconnect and as a TSV in a silicon interposer, as shown in Fig. 3.3. Because the TSV models in the stacked die and the silicon interposer should be similar, we concentrate on the equivalent-circuit models of the TSV and silicon interposer interconnect. These models enable the efficient analysis for the electrical properties of a high-speed TSV-based channel.

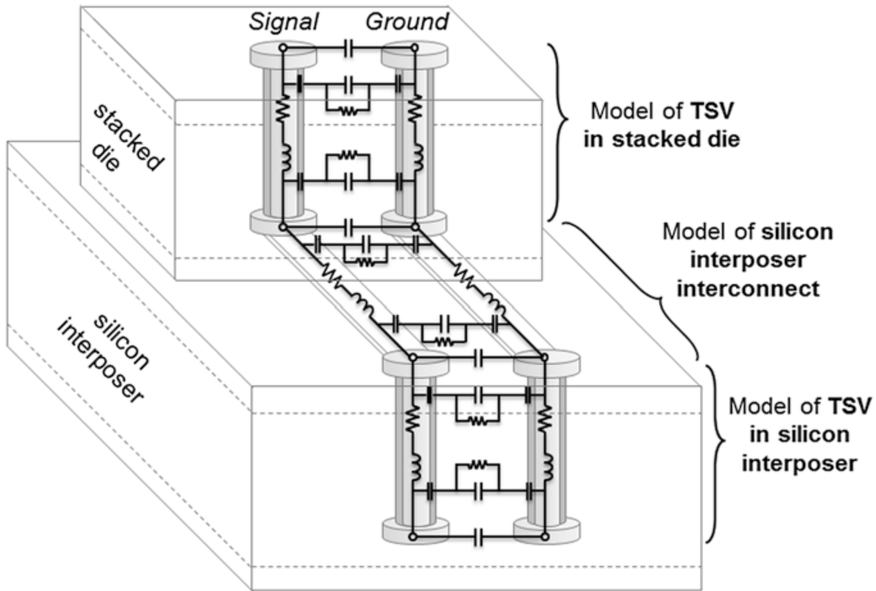


Fig. 3.3 Overall model of a high-speed TSV-based channel

3.2.1 Equivalent-Circuit Model of the TSV

The equivalent-circuit model of a GSG-type single-ended TSV is depicted in Fig. 3.4. The modeling of each lumped component is based on the GS-type TSV model discussed in the previous chapter. However, the capacitance and conductance models require additional consideration. The capacitance of the oxide layer in the signal TSV (C_{ox_TSV}) is the same as the ground TSV in the case of a GS-type TSV, but it is different in the case of a GSG-type TSV. This difference in capacitance behavior is due to the signal TSV being surrounded by two ground TSVs, thus changing the field distribution. The capacitance of the oxide layer in the ground TSV (C_{ox_TSV}') is determined by using a full-wave simulation and is approximately 1.5C_{ox_TSV}. Because the silicon substrate has a non-zero conductivity, the model of the silicon substrate includes not only the capacitance model (C_{Si_TSV}) but also the conductance model (G_{Si_TSV}). The capacitance and conductance of the silicon substrate in the GSG-type TSV are also altered relative to those in the GS-type TSV because of the additional ground TSV; they are reduced by approximately 25 %.

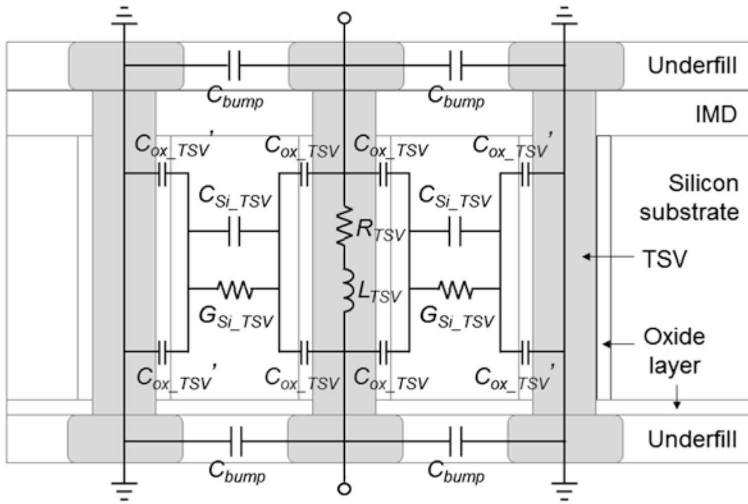


Fig. 3.4 Equivalent-circuit model of TSV [2] © 2012 IEEE

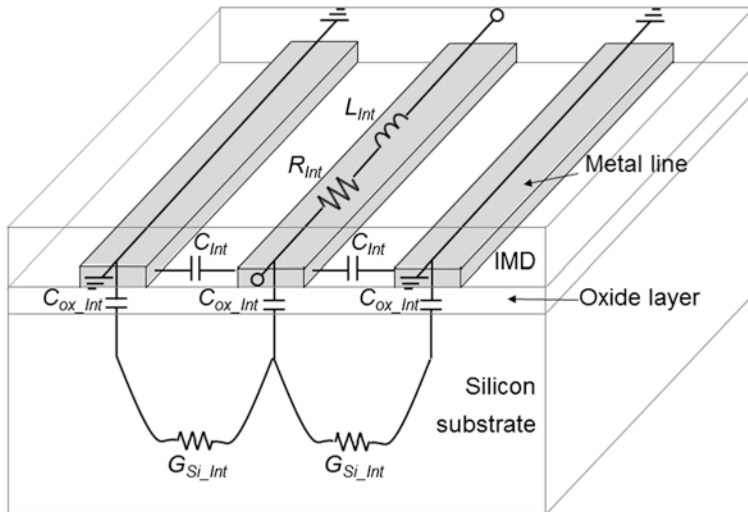


Fig. 3.5 Equivalent-circuit model of the silicon interposer interconnect [2] © 2012 IEEE

3.2.2 Equivalent-Circuit Model of the Silicon Interposer Interconnect

The equivalent-circuit model of the GSG-type single-ended silicon interposer interconnect is depicted in Fig. 3.5. The modeling of each lumped component in

the silicon interposer interconnect is based on models in previous studies [3–6]. The capacitance model (C_{Int}) of the silicon interposer interconnect is complex, as the electric fields present between the metal lines have elliptical forms in the GSG signal pattern. To determine the capacitance model, the conformal mapping method is employed, which uses the complete elliptical integral of the first kind; the details are shown in reference paper [5]. The equivalent-circuit model of the silicon interposer interconnect also contains the conductance model (G_{Si_Int}) that considers the non-zero conductivity of the silicon substrate. The capacitance model of the silicon substrate is equivalently included in C_{Int}.

3.3 Analysis of High-Speed TSV-Based Channel

In this section, the electrical properties of the high-speed TSV-based channel are analyzed based on the simulated channel loss and the single-bit response; the channel loss (S_{21}) and the single-bit response of the channel indicate the frequency- and time-domain properties, respectively. The TSV and the silicon interposer interconnect that comprise the TSV-based channel are separately analyzed in Sects. 3.3.1 and 3.3.2. In Sect. 3.3.2.3, the impacts of the TSV and the silicon interposer interconnect to the electrical properties of the total TSV-based channel are analyzed in accordance with the length of the silicon interposer interconnect.

Additionally, the measurement results of the high-speed TSV-based channel are demonstrated in Sect. 3.3.3 as an example. The unique electrical properties of the high-speed TSV-based channel are compared to the MCM channel in Sect. 3.3.4.

3.3.1 Electrical Properties of Coaxial TSV

The channel loss of a TSV is determined by the channel type. Because the electrical properties of a normal TSV are discussed in the previous chapter, those of the coaxial TSV are analyzed in this chapter. The coaxial organic lining via (COLV) that is fabricated by adjusting UV laser drilling is the coaxial TSV used for analysis in this section [7]. For comparison, the electrical properties of the through silicon lining via (TSLV), the through organic lining via (TOLV) and the normal TSV are also analyzed at the same time. The different structure of each channel type leads to different properties.

The TSV channel types are shown in Fig. 3.6. A single-ended channel is chosen as the baseline signaling type. The structures in Fig. 3.6a–d are the TSLV, TOLV, COLV and the normal TSV, respectively. The through via of TSLV is in contact with the silicon substrate, whereas the through vias of the TOLV and the COLV are isolated from the silicon substrate by the polymer. To clarify the impact of the

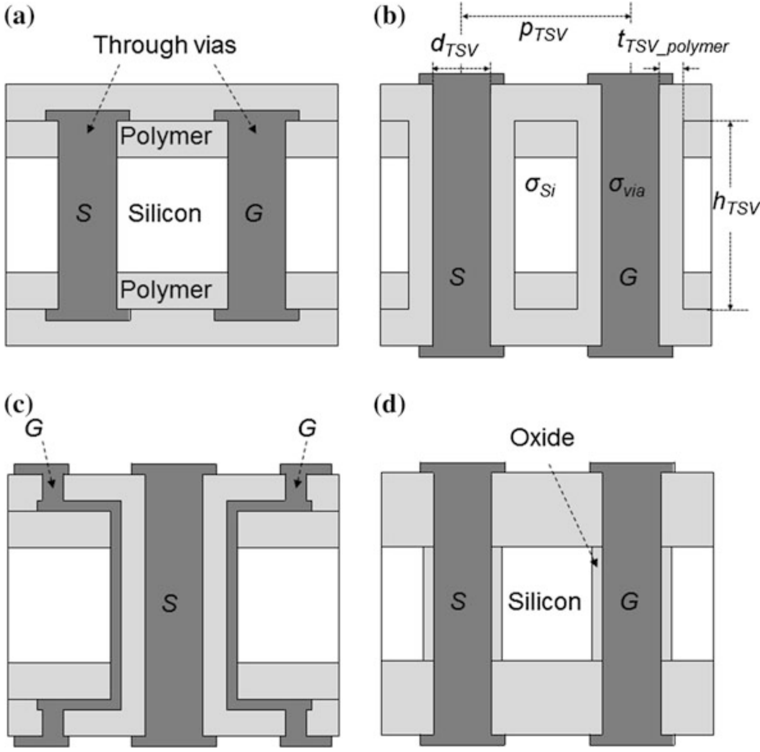


Fig. 3.6 TSV channel types. **a** TSLV **b** TOLV **c** COLV **d** Normal TSV

Table 3.1 Baseline dimensions and materials of the TSV

Parameter	d_{TSV} (μm)	p_{TSV} (μm)	h_{TSV} (μm)	$t_{TSV_polymer}$ (μm)	σ_{via} (S/m)	σ_{Si} (S/m)
Value (Case 1)	80	200	200	30	5.8×10^7	10
Value (Case 2)	10	40	120	3.75		

channel type variation to the channel loss, all of the TSVs in Fig. 3.6a–c share the same materials.

The baseline dimensions and materials for the TSV simulation are shown in Table 3.1. Case 1 and Case 2 indicate the realistic dimensions of the coaxial TSV and the size-reduced version of the normal TSV, respectively. The simulation based on the dimension of Case 1 is performed for a comparison of electrical properties between the TSLV, TOLV, and COLV. Additionally, the simulation based on Case 2 is also performed for a comparison of electrical properties between the TSLV, COLV, and normal TSV under the same physical dimensions, but the thickness of the oxide layer in the normal TSV is 0.5 μm.

The simulated channel loss of the TSV, in accordance with the channel types, is shown in Fig. 3.7. The channel losses in Fig. 3.7a, b are simulated based on the

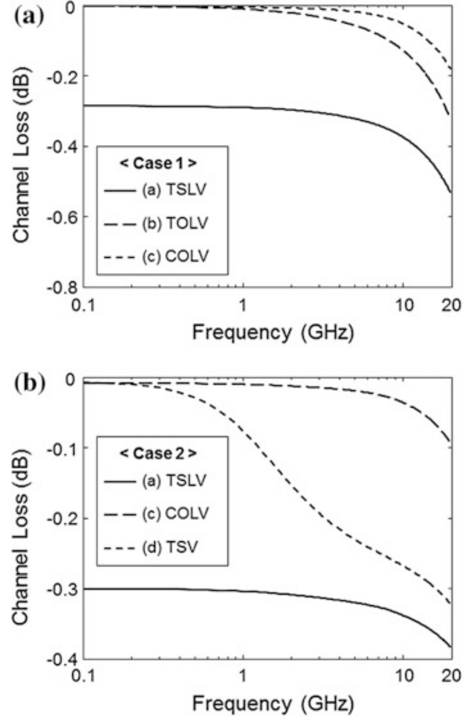


Fig. 3.7 Channel loss of the TSV. **a** Case 1 **b** Case 2

physical dimensions of Case 1 and Case 2, respectively. The stacking number of TSVs is assumed to be four in this simulation.

The channel losses of TSLV, TOLV and COLV for the dimensions of Case 1 are shown in Fig. 3.7a. In the case of TSLV, the DC level is considerably attenuated because the through via is in contact with the silicon substrate. This contact creates a direct path of leakage current from the signal via to the ground via as shown in Fig. 3.8a, resulting in the DC attenuation. In contrast, the through vias of TOLV and COLV are completely isolated from the lossy silicon substrate by the polymer, as shown in Fig. 3.8b, resulting in considerably less DC attenuation. Due to these DC level differences, the overall channel loss of the TSLV becomes higher than those of the TOLV and COLV.

$$L_{TOLV} = \frac{\mu}{2\pi} \times \ln\left(\frac{2p_{TSV}}{d_{TSV}}\right) \tag{3.1}$$

$$L_{COLV} = \frac{\mu}{2\pi} \times \ln\left(\frac{d_{TSV} + t_{TSV_polymer}}{d_{TSV}}\right) \tag{3.2}$$

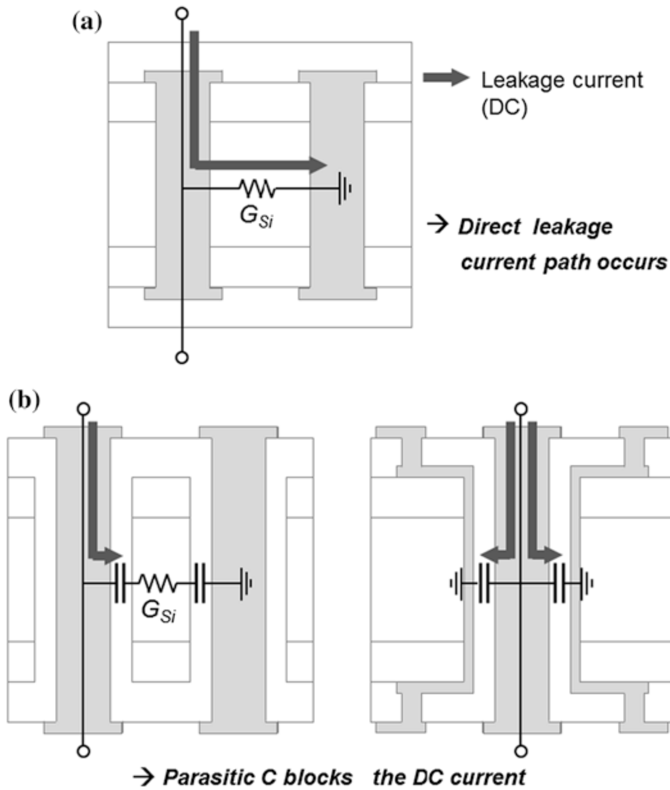


Fig. 3.8 DC leakage current paths. **a** TSLV **b** TOLV and COLV

In the comparison of TOLV to COLV, the channel loss of the TOLV is slightly higher than that of the COLV, as shown in Fig. 3.7a, due to the higher inductance. The inductances of the TOLV and the COLV can be calculated by using (3.1) and (3.2) [8, 9]. Under the same diameters of the through vias of the TOLV and COLV (d_{TSV}), the inductance of the TOLV is higher than that of the COLV due to the wide pitch between signal and ground vias. If the thickness of the polymer ($t_{TSV_polymer}$) is sufficiently thin, the channel loss of the COLV can be higher than that of the TOLV due to the impact of the large capacitance.

The channel losses of the TSLV, COLV and the normal TSV for the dimensions of Case 2 are shown in Fig. 3.7b. The channel loss in this case also presents the similar tendency of the previous case. Due to the DC attenuation resulting from the contact to the lossy silicon substrate, the overall channel loss of the TSLV is higher than those of the COLV and the normal TSV. In the case of the normal TSV, the oxide layer acts as an insulator, preventing DC attenuation through the silicon substrate [10]. In comparing the COLV to the normal TSV, the channel loss of the TSV is higher than that of the COLV, as shown in Fig. 3.7b, due to the impact of

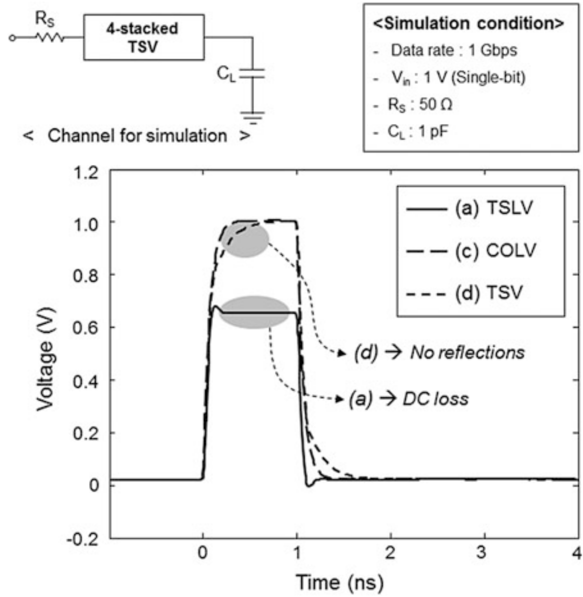


Fig. 3.9 Single-bit response of the TSV channel (@ Case 2)

the lossy silicon substrate. Because the COLV channel is isolated from the silicon substrate, the channel loss of the TSV should be higher than that of the COLV.

The simulated single-bit responses of the TSVs, in accordance with the channel types and the simulation setup, are shown in Fig. 3.9. The baseline dimension of the TSV is Case 2. The channel without the on-die termination is assumed for the full-swing of the output signal.

As shown in Fig. 3.9, the amplitude of the single-bit response is reduced in the case of the TSLV, whereas those of the COLV and the normal TSV are not reduced. The crucial point is that these DC level differences are not caused by the different DC levels of the channel loss curves in Fig. 3.7 because the channel does not include the on-die termination. In general, even if the DC loss is observed in the channel loss curve, the single-bit response of the channel without the on-die termination should be the full-swing signal akin to those of the COLV and the TSV in Fig. 3.9. However, the single-bit response of the TSLV channel is attenuated as shown in Fig. 3.9 because the DC loss of the TSLV channel is induced by the direct leakage current path to the silicon substrate. The DC loss of the normal

$$V_{out_TSV} = V_{in} \times \frac{\infty}{R_S + R_{TSV} + \infty} \approx V_{in} \tag{3.3}$$

$$V_{out_TSLV} = V_{in} \times \frac{\frac{1}{1+R_{TSLV}G_{TSLV}}}{R_S + \left(\frac{1}{G_{TSLV}} // \left(\frac{1}{G_{TSLV}} + R_{TSLV}\right)\right)} < V_{in} \tag{3.4}$$

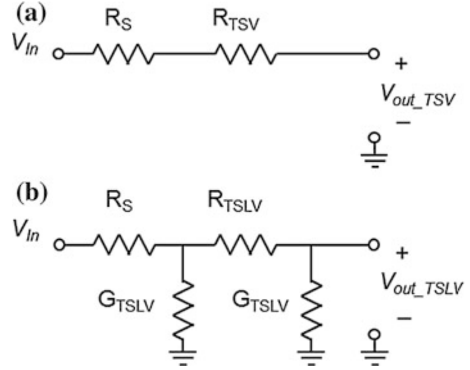


Fig. 3.10 Resistance models of the **a** TSV channel and **b** TSLV channel

TSV channel can usually be modeled to the series resistance (R_{TSV}), but the DC loss of the TSLV channel that is created by the direct leakage current path to the silicon substrate can be modeled to the shunt conductance (G_{TSLV}), as shown in Fig. 3.10. The DC levels of the output voltages (V_{out_TSV} and V_{out_TSLV}) can then be calculated by using the resistance models derived in (3.3) and (3.4). As shown in (3.3), the DC level of the normal TSV channel is independent from R_{TSV} and V_{out} has no DC attenuation. In contrast, the DC level of the TSLV channel is dependent on G_{TSLV} as shown in (3.4), resulting in the DC attenuation of V_{out}. Therefore, even though the DC levels of the TSV and TSLV channels become the same in the channel loss curves, the single-bit response of the channel with the series resistance achieves a full-swing, while that of the channel with the shunt conductance exhibits DC attenuation.

$$\text{Risetime} \approx \left.\frac{0.35}{Bandwidth}\right|_{V_{out}=10\%\sim 90\%} \tag{3.5}$$

Though the overall channel loss of the TSLV is higher than those of the COLV and TSV due to the considerably high DC attenuation, the channel loss curve of the TSLV is flatter than those of the COLV and TSV as shown in Fig. 3.7b. This means that the effective bandwidth of the TSLV is wider than that of the TSV, even though there is some DC attenuation. According to (3.5), the single-bit response of the TSLV has shorter rise and fall times than those of the COLV and TSV [11]. However, the peak occurs in the single-bit response of the TSLV channel because of the de-emphasis effect.

The negligible impact of the reflection in the TSV channel is also observed in the simulated single-bit response in Fig. 3.9. The impact of reflection should be negligible in the TSV channel due to its short interconnect length, causing the single-bit response of the TSV channel to increase or decrease monotonically. Even though the height or the stacking number of the TSV is considerably increased, the impact of the reflection will still be negligible because the reflected wave in the TSV should be considerably attenuated by the lossy silicon substrate.

Although the COLV has the lowest channel loss and no DC attenuation, the single-bit response of the COLV has no reflection because the COLV is designed to be well-matched in this simulation. Therefore, the single-bit response of the COLV becomes the almost ideal response, as shown in Fig. 3.9. Due to the inherent low loss of the COLV, the reflection can considerably affect the single-bit response of the COLV when the COLV is designed to be mismatched.

3.3.2 Electrical Properties of Silicon Interposer Interconnect

In this subsection, the electrical properties of the silicon interposer interconnect are analyzed based on the simulated channel loss and the single-bit response. The simulations are performed and analyzed with various channel types, oxide thicknesses under the metal line, silicon conductivity, width and length of the metal line.

3.3.2.1 Channel Type Variation

Depending on the design of the signal and ground lines, the channel type of the silicon interposer interconnect, which profoundly affects the electrical properties, is varied. In this chapter, the co-planar waveguide (CPW), the microstrip line, and the co-planar waveguide with ground-plane (CPWGP) are investigated as the channel types of the silicon interposer interconnect.

The channel types of the silicon interposer interconnect are shown in Fig. 3.11. A single-ended channel is chosen as the signaling type. The structures in Fig. 3.11a, b are the co-planar waveguides (CPW), those of Fig. 3.11c, d are the microstrip lines, and those of Fig. 3.11e, f are the co-planar waveguide with ground plane (CPWGP). The signal lines of the structures in Fig. 3.11a, c and e are on the metal layer of M1, and those of Fig. 3.11b, d and f are on the metal layer of M2. The baseline dimensions and materials of the silicon interposer interconnect for the simulations are shown in Table 3.2. The length of the silicon interposer interconnect is 1 mm. In the cases of CPW and CPWGP, the widths of the ground lines on either side of the signal line are the same as that of the signal line.

The simulated channel losses of the silicon interposer interconnects, in accordance with the channel types, are shown in Fig. 3.12. The signal lines of the channels in Fig. 3.12a are on the metal layers of M1, and those of Fig. 3.12b are on the metal layer of M2.

In the case of Fig. 3.12a, the channel loss of the CPW is higher than that of the microstrip line. In the case of the CPW, the some portion of the electric field from the signal line to the ground lines passes through the lossy silicon substrate. In contrast, that of the microstrip line is concentrated on the space between the signal line and the ground plane. Due to these different field distributions, the channel loss of the CPW is higher than that of microstrip line through the lossy silicon substrate. However, the channel loss of the CPW is lower than that of the CPWGP.

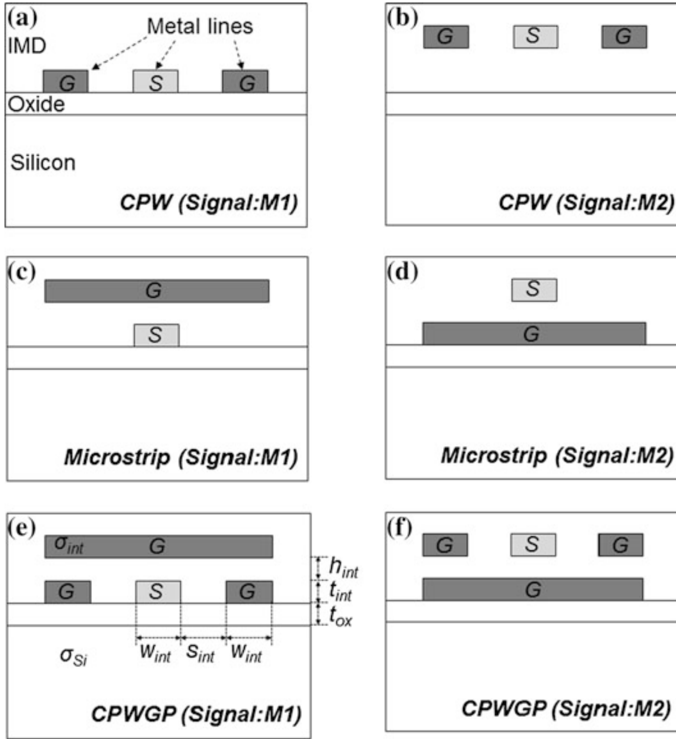


Fig. 3.11 Channel types of the silicon interposer interconnect

Table 3.2 Baseline dimensions and materials of the silicon interposer interconnect

Parameter	w_{int} (μm)	s_{int} (μm)	t_{int} (μm)	h_{int} (μm)	t_{ox} (μm)	σ_{int} (S/m)	σ_{Si} (S/m)
Value	10	10	5	5	1	5.8×10^7	10

The distance from the signal line to the ground plane in the CPWGP is so short that a larger capacitance (compared to that of the CPW) is induced. Moreover, the impact of the lossy silicon substrate is also included in the channel loss of the CPWGP due to the ground lines on either side of the signal line. Therefore, the overall channel loss of the CPWGP becomes higher than that of the CPW.

The simulated channel loss of the silicon interposer interconnects with the signal lines on the metal layer of M2 are shown in Fig. 3.12b. The channel losses in these cases are lower overall than those of the previous cases with signal lines on the metal layer of M1 due to the reduced impact of the lossy silicon substrate.

In the case of the signal line on M1, all of the channel losses at 20 GHz are higher than −0.5 dB, whereas those in the case of the M2 signal line are lower than −0.3 dB. In the case of the signal line on M2, the CPW also has a higher

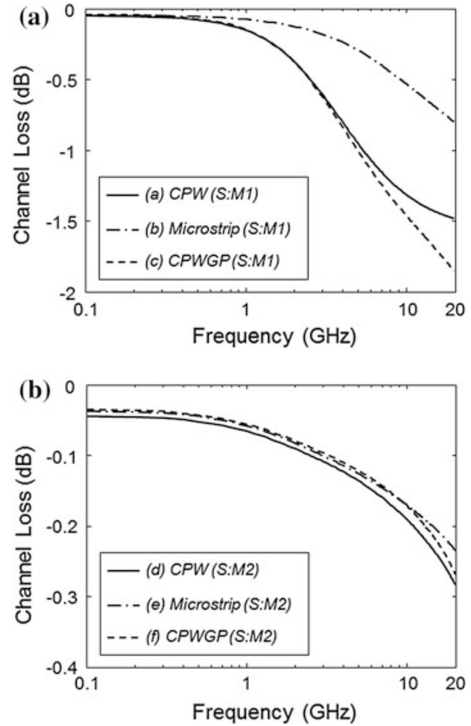


Fig. 3.12 Channel loss of the silicon interposer interconnect **a** S : M1 **b** S : M2

channel loss than the microstrip line. Compared to the channel losses in Fig. 3.12a, the channel losses of the CPW and microstrip line are much closer due to the relatively lower impact of the lossy silicon substrate. Because the distance from the signal line to the silicon substrate is increased, the amount of the field that passes through the lossy silicon substrate is decreased, lowering the channel loss of the CPW with the M2 signal line. However, as shown in Fig. 3.12b, the channel loss of the microstrip line is still lower than that of the CPW because the ground plane of the microstrip line on the M1 metal layer completely blocks the impact of the silicon substrate. In contrast to the case of the M1 signal line, the channel loss of the CPWGP is lower than that of the CPW in the case of the M2 signal line, as shown in Fig. 3.12b. This is also due to the impact of the ground plane on M1. Though the impact of the lossy silicon substrate is reduced by the larger distance from the signal line to the silicon substrate, it should still remain in the case of the CPW. However, the ground plane on M1 completely blocks the impact of the lossy silicon substrate in the case of the CPWGP, leading to lower channel loss than that for the CPW.

$$R_{CPW} = \frac{1}{\sigma_{int} t_{int}} \times \left(\frac{1}{w_{int}} + \frac{1}{w_{int}} // \frac{1}{w_{int}} \right) = \frac{1.5}{\sigma_{int} t_{int} w_{int}} \tag{3.6}$$

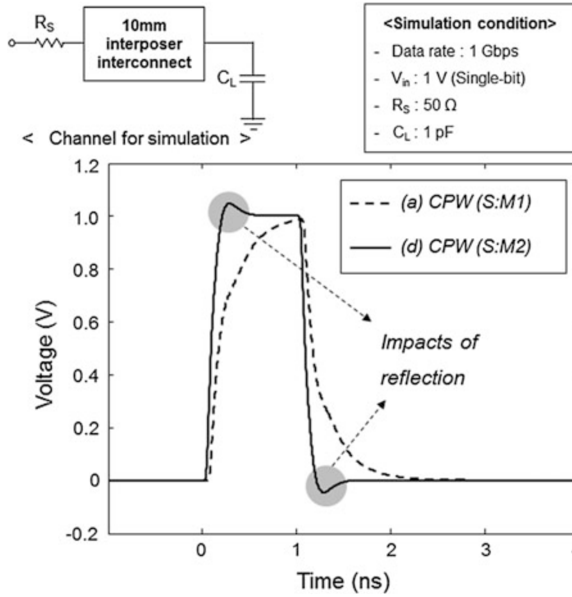


Fig. 3.13 Single-bit response of the silicon interposer interconnect (Metal layer of signal line variation @ CPW)

$$R_{uStrip} = \frac{1}{\sigma_{int} t_{int}} \times \left(\frac{1}{w_{int}} + \frac{1}{w_{Plane}} \right) \approx \left. \frac{1}{\sigma_{int} t_{int} w_{int}} \right|_{w_{Plane} \approx \infty} \tag{3.7}$$

$$\begin{aligned} R_{CPWGP} &= \frac{1}{\sigma_{int} t_{int}} \times \left(\frac{1}{w_{int}} + \frac{1}{w_{Plane}} // \frac{1}{w_{int}} // \frac{1}{w_{int}} \right) \\ &\approx \left. \frac{1}{\sigma_{int} t_{int} w_{int}} \right|_{w_{Plane} \approx \infty} \end{aligned} \tag{3.8}$$

There is a negligible resistance of the ground plane that affects the channel loss of the interposer interconnect at the DC level. The equations for the resistances of the CPW, the microstrip line and the CPWGP are shown in (3.6)–(3.8). In the cases of the microstrip line and the CPWGP, the resistances of the return current paths can be neglected because they include the ground plane [12]. In contrast, the return current path of the CPW should have considerable resistance. Therefore, the DC levels of the microstrip line and the CPWGP are lower than that of the CPW as shown in Fig. 3.12b. If the signal and ground metal lines were designed to have higher resistance by means of a narrow width (w_{int}) and thin thickness (t_{int}), then the DC level differences of the CPW, the microstrip line and the CPWGP would be considerably increased.

The simulated single-bit responses of the silicon interposer interconnects, in accordance with the metal layer of the signal line, are shown in Fig. 3.13. The channel type is the CPW.

As shown in Fig. 3.13, the impact of the reflection depends on the metal layer of the signal line. In the case of the signal line on M1, the single-bit response is

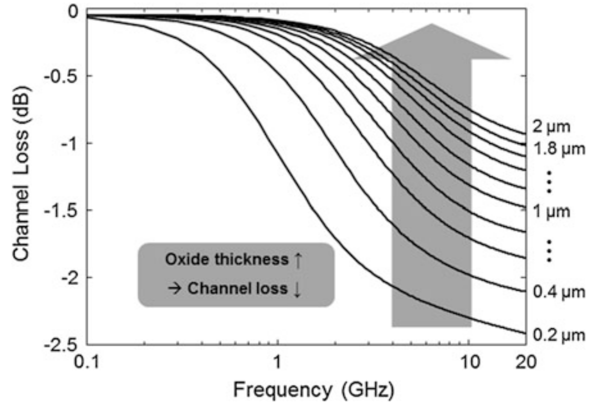


Fig. 3.14 Channel loss of the silicon interposer interconnect (Oxide thickness variation)

considerably attenuated by the silicon substrate. Therefore, the single-bit response of this case monotonically changes depending on the loss from the silicon substrate. In contrast, the loss from the silicon substrate is relatively small in the case of the signal line on M2. It leads to a reduced channel loss, resulting in reduced rise and fall times and an improved single-bit response as shown in Fig. 3.13. However, the impact of the reflection is considerable in the single-bit response of this case due to the low attenuation that is caused by the small impact of the silicon substrate. Though the reflected wave is so attenuated that it becomes negligible in the previous case of the signal line on M1, it becomes considerable in the case of the signal line on M2. Therefore, unexpected peaks occur in the single-bit response of the M2 signal case, as shown in Fig. 3.13.

3.3.2.2 Structure and Material Variation

The simulated channel loss of the silicon interposer interconnects, in accordance with the oxide thickness under the metal line, is shown in Fig. 3.14. The oxide thickness varies from 0.2 to 2 μm at intervals of 0.2 μm. The channel loss change of the silicon interposer interconnect with the oxide thickness variation has an obvious tendency; the channel loss decreases as the oxide thickness increases (as shown in Fig. 3.14) due to the decreased impact of the lossy silicon substrate and the decreased capacitance of the oxide layer. The impact of the lossy silicon substrate can be modeled as the silicon conductance that contributes to the attenuation of the transmitted signal. As the oxide thickness increases, the distance from the lossy silicon substrate to the metal line definitely increases, resulting in the lower silicon conductance. Therefore, as shown in Fig. 3.14, the channel loss of the silicon interposer interconnect is decreased as the oxide thickness increases.

The capacitance of the oxide layer determines the frequency at which the loss of the channel is enhanced by the lossy silicon substrate. The shunt impedance of the silicon interposer interconnect can be approximately modeled as shown in (3.9)

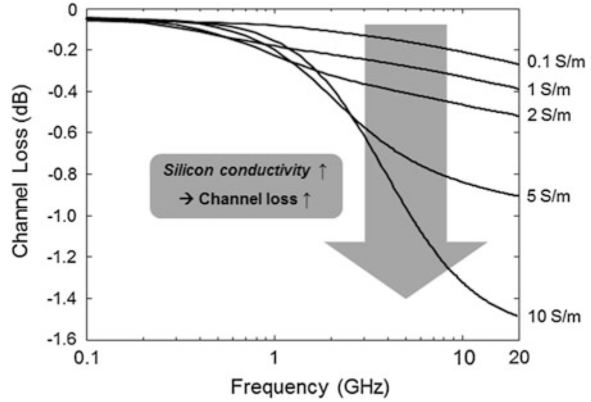


Fig. 3.15 Channel loss of the silicon interposer interconnect (silicon conductivity variation)

and (3.10). The dominant factors are the silicon conductance (G_{Si_Int}) and the oxide capacitance (C_{ox_Int}). As shown in (3.9) and (3.10), the dominant factor to the shunt impedance of the silicon interposer interconnect is changed depending on the frequency.

At the low frequency range, the oxide capacitance becomes dominant because G_{Si_Int} is greater than wC_{ox_Int}. At the high frequency range, wC_{ox_Int} is greater than G_{Si_Int}, resulting in the dominance of the silicon conductance. According to (3.11), as the oxide capacitance is increased by the thinner oxide layer, the frequency at which the loss rapidly increases due to the silicon conductance should be decreased.

$$\begin{aligned} \left|Z_{shunt_Interposer}\right| &\approx \frac{1}{G_{Si_int}} + \frac{1}{wC_{ox_int}} = \frac{G_{Si_int} + wC_{ox_int}}{wG_{Si_int}C_{ox_int}} \\ &\approx \frac{G_{Si_int}}{wG_{Si_int}C_{ox_int}} = \frac{1}{wC_{ox_int}} \quad (@\,\text{low frequency range}) \end{aligned} \tag{3.9}$$

$$\approx \frac{wC_{ox_int}}{wG_{Si_int}C_{ox_int}} = \frac{1}{G_{Si_int}} (@\,\text{high frequency range}) \tag{3.10}$$

$$f\big|_{G_{Si_int}=wC_{ox_int}} = \frac{1}{2\pi} \times \frac{G_{Si_int}}{C_{ox_int}} \tag{3.11}$$

The simulated channel loss of the silicon interposer interconnects, in accordance with the conductivity of the silicon substrate, is shown in Fig. 3.15. The silicon conductivities for the simulation are 0.1, 1, 2, 5, and 10 S/m. As shown in Fig. 3.15, the channel loss of the silicon interposer interconnect increases as the silicon conductivity increases due to the enhanced silicon conductance. The frequency at which the loss increases rapidly due to the silicon conductance also increases as the silicon conductivity increases. This tendency can also be analyzed by using (3.11). If the G_{Si_Int} increases under the constant C_{ox_Int}, the frequency at which the loss increases due to the silicon conductance should also increase.

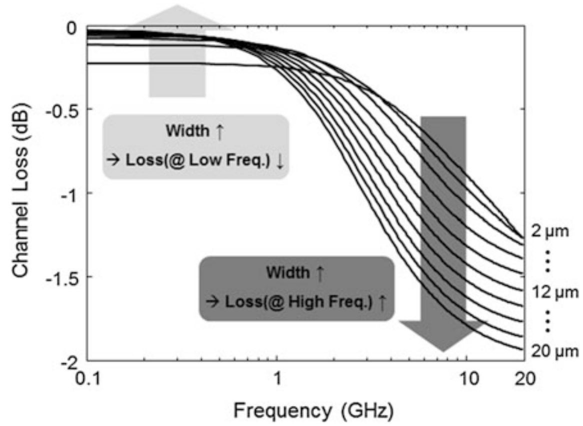


Fig. 3.16 Channel loss of the silicon interposer interconnect (Metal width variation)

The simulated channel loss of the silicon interposer interconnects, in accordance with the metal width, is shown in Fig. 3.16. The metal width varies from 2 to 20 µm at an interval of 2 µm. At the low frequency range, the channel loss of the silicon interposer interconnect decreases, as the metal width increases due to the decreased resistance of the interposer interconnect that determines the DC level. Though the wider metal width leads to the higher oxide capacitance and silicon conductance of the silicon interposer interconnect, the impacts due to the oxide capacitance and silicon conductance on the channel loss are lower than those of the resistance at the low frequency, resulting in lower channel loss. However, the impacts of the oxide capacitance and silicon conductance on the channel loss become higher than that of the resistance as the frequency increases. Therefore, the channel loss of the silicon interposer interconnect increases as the metal width increases at the high frequency range, as shown in Fig. 3.16.

The amounts of the resistance and capacitance of the silicon interposer interconnect depend on the width of the interconnect, as shown in the upper side of Fig. 3.17. As analyzed previously, the width of the interconnect is a dominant factor in the channel bandwidth because the channel bandwidth is predominantly determined by the amount of the total resistance and capacitance of the channel. If the width of the silicon interposer interconnect is sufficiently narrow, the resistance of the interposer interconnect becomes considerably high, whereas the capacitance becomes negligible. In this case, the channel bandwidth should be increased, as the metal width increases due to the dominance of the interconnect resistance. In contrast, the channel bandwidth is increased upon the decrease in the metal width when the width of the silicon interposer interconnect is sufficiently wide because the capacitance of the interposer interconnect becomes considerably high and the resistance becomes negligible in this case. As a result, there should be an optimal width of the silicon interposer interconnect that corresponds to the maximum channel bandwidth, as shown in the lower side of Fig. 3.17.

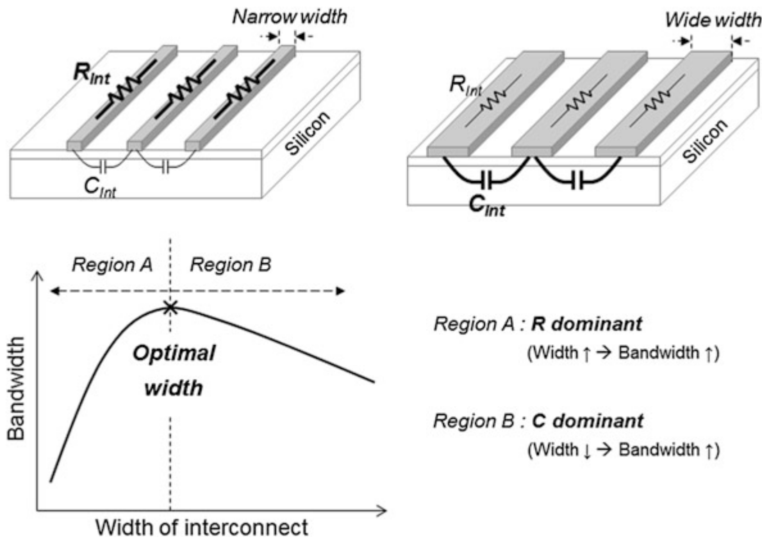
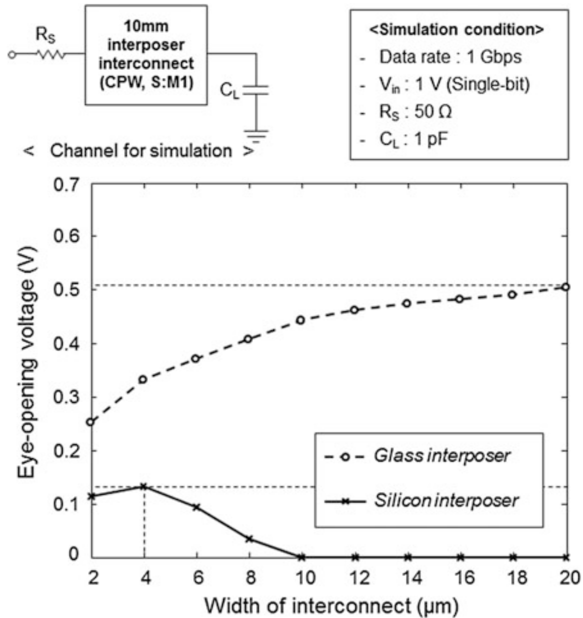


Fig. 3.17 Optimal width for the maximum channel bandwidth

Fig. 3.18 Eye-opening voltages of the silicon and glass interposer interconnects (Metal width variation)



The simulated eye-opening voltage that determines the channel bandwidth, in accordance with the width of the silicon interposer interconnect, is shown in Fig. 3.18. The data rate of the input signal is 10 Gbps. As shown in Fig. 3.18, the

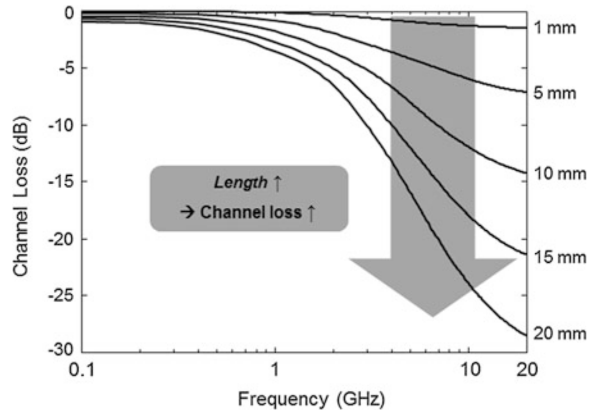


Fig. 3.19 Channel loss of silicon interposer interconnects (Interconnect length variation)

width of the silicon interposer interconnect that corresponds to the maximum eye-opening voltage is 4 μm. Narrower and wider widths (compared to 4 μm) create lower eye-opening voltages due to either the increased resistance or capacitance of the silicon interposer interconnect, respectively.

The optimal width of the silicon interposer interconnect can be changed by various factors such as the channel type, length of the interconnect, materials, and termination conditions, among others. In this chapter, the material of the interposer is covered as an example. The eye-opening voltage, in accordance with the widths of the glass interposer interconnect, is also shown in Fig. 3.18. Due to the lower permittivity and loss of the glass compared to the silicon [13], the overall eye-opening voltages of the glass interposer channels are higher than those of the silicon interposer channels. Compared to the optimal width of the silicon interposer interconnect, the glass interposer interconnect optimal width is wider (20 μm) because the capacitance of the glass interposer interconnect is lower than that of the silicon interposer interconnect for the same structure. If the metal materials used in the glass and silicon interposer interconnects are the same, their resistances should be the same at the same structure. Therefore, the impact of the resistance to the channel loss is relatively increased in the case of the glass interposer interconnect compared to the silicon interposer interconnect, resulting in a wider optimal width.

The simulated channel loss of the silicon interposer interconnects, in accordance with the length of the interconnect, is shown in Fig. 3.19. The lengths used for the simulation are 1, 5, 10, 15, and 20 mm. As shown in Fig. 3.19, the overall channel loss of the silicon interposer interconnect is proportionally increased as the length increases. The DC attenuation level is increased by the increased interconnect length due to the proportionally increased resistance. Moreover, the channel loss at mid- and high-frequency ranges is also increased by the increased interconnect length due to the proportionally increased silicon conductance. In the case of the silicon interposer interconnect at a 20 mm length, the channel loss increases severely up to −28 dB at 20 GHz. However, as shown in Fig. 3.19, the

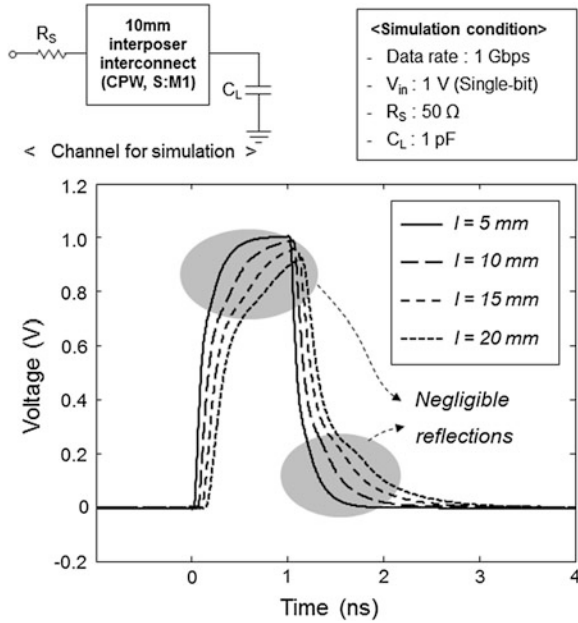


Fig. 3.20 Single-bit response of the silicon interposer interconnect (Interconnect length variation @ CPW with signal on M1)

frequency at which the channel loss rapidly increases due to the silicon conductance is almost constant because the longer interposer interconnect has not only a proportionally increased silicon conductance but also a proportionally increased oxide capacitance. The constant ratio between the silicon conductance and the oxide capacitance leads to the constant frequency at which the silicon conductance begins to impact the channel loss.

The simulated single-bit responses of the silicon interposer interconnects, in accordance with the length of the interconnect, are shown in Fig. 3.20. As shown in Fig. 3.20, the rise and fall times of the single-bit response of the silicon interposer interconnect increase as the interconnect length increases due to the enhanced channel loss, resulting in a worse single-bit response.

The impact of the reflection is negligible, even though the interconnect length increases (as shown in Fig. 3.20). The impact of the reflection is usually observed in the transition region of the single-bit response because the propagation delay of the silicon interposer interconnect is typically less than the duty of the transmitted signal. In this simulation, the propagation delay of the silicon interposer interconnect at a 20 mm length is only 132 ps, whereas the duty of the single-bit pulse is 1 ns. Because the time that the reflected wave begins to have an impact to the single-bit response should be proportional to the length of the interconnect (usually several tens of millimeters), the reflection in the silicon interposer interconnect should affect the transition region. Therefore, there are several distortions caused by the impact of the reflection in the transition region of the simulated single-bit responses in Fig. 3.20. However, the distortion level is so small that the single-bit responses of the silicon interposer interconnect monotonically increase and

decrease with the negligible changes. This is because the reflected wave in the silicon interposer interconnect is attenuated by the lossy silicon substrate.

3.3.2.3 Impacts of the TSV and Silicon Interposer Interconnect on the Total TSV-Based Channel

In the previous subsections, we separately cover the electrical properties of the TSV and silicon interposer interconnect. In practice, the high-speed TSV-based channel simultaneously consists of TSVs and a silicon interposer interconnect, as shown in Fig. 3.1. This means that the TSVs and silicon interposer simultaneously impact the electrical properties of the high-speed TSV-based channel. In this sub-subsection, we cover the impact portions of the TSV and silicon interposer interconnect on the electrical properties of the total TSV-based channel.

The simulated loss of the high-speed TSV-based channel, in accordance with the stacking number of the TSV and the length of the silicon interposer interconnect, is shown in Fig. 3.21. The stacking number of the TSV and the length of the interposer interconnect are varied by 50, 100, and 200 % of their normal values.

In the case of Fig. 3.21a, the length of the silicon interposer interconnect is 1 mm. Compared to the length variation of the silicon interposer interconnect, the loss of the high-speed TSV-based channel varies more by the stacking number variation of the TSV. Though the total height of the stacked TSV is shorter than the total length of the silicon interposer interconnect, the impact of the TSV variation is higher than that of the silicon interposer; the total height of the four-stacked TSV (=472 μm) is almost half of the silicon interposer interconnect. Under the same interconnect length, the TSV has a relatively higher oxide capacitance and silicon conductance compared to those of the silicon interposer interconnect due to the thinner oxide layer and its inherent via structure, resulting in a higher channel loss. In practice, the length of the silicon interposer interconnect can be longer than 1 mm [14]. The simulated losses of the high-speed TSV-based channel in the case of the longer interposer interconnects are shown in Fig. 3.21b, c. The lengths of the silicon interposer interconnects in these cases are 4 and 10 mm, respectively. For the length of 4 mm, the impact of the silicon interposer interconnect on the total channel becomes higher than that of the TSV. Though the channel loss per unit length of TSV is higher than that of the silicon interposer interconnect, the channel loss of the silicon interposer interconnect becomes higher in this case due to the much longer interconnect length. In the case of the silicon interposer interconnect of 10 mm, the impact of the TSV becomes negligible, as shown in Fig. 3.21c.

The simulated single-bit response of the high-speed TSV-based channel, in accordance with the stacking number of the TSV and the length of the silicon interposer interconnect, is shown in Fig. 3.22.

In the case of the silicon interposer interconnect length of 1 mm, the single-bit responses of the high-speed TSV-based channels with the aforementioned variations are almost the same as shown in Fig. 3.22a. The TSV is the capacitive

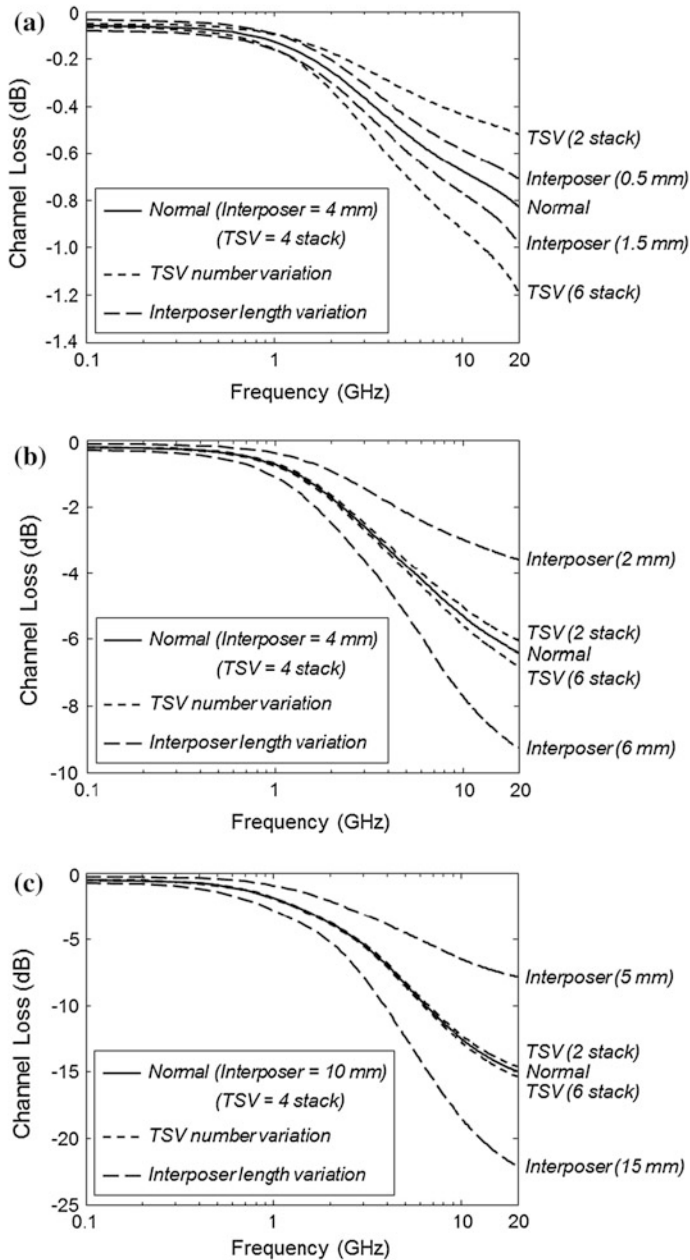


Fig. 3.21 Channel loss of the TSV-based channel (stacking number of TSV and interconnect lengths of silicon interposer variations). Baseline lengths of silicon interposer interconnects are **a** 1 mm **b** 4 mm **c** 10 mm

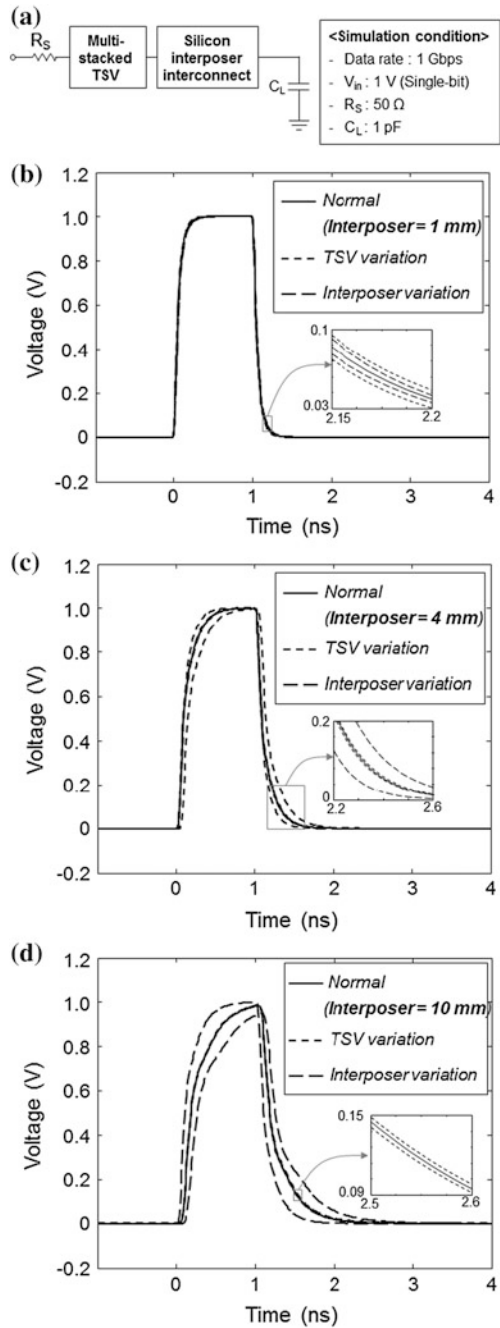


Fig. 3.22 Single-bit response of the TSV-based channel. (Stacking number of TSV and interconnect length of silicon interposer variations). **a** Simulation setup and baseline length of interposer interconnect are **b** 1 mm **c** 4 mm **d** 10 mm

channel, and the equivalent capacitance of the four-stacked TSV is much lower than the load capacitance of 1 pF. The silicon interposer interconnect of 1 mm also has a much lower impact on the channel loss than those of terminations (source resistance of 50 ohm and load capacitance of 1 pF) due to its short length. Therefore, the single-bit responses in this case are insensitive to the TSV and the silicon interposer interconnect variations. As the length of the silicon interposer interconnect increases, the single-bit response of the high-speed TSV-based channel becomes sensitive to the silicon interposer interconnect. As shown in Fig. 3.22b, c, the single-bit responses are changed by the silicon interposer interconnect variation, whereas they are still insensitive to the TSV variation. The impact of the TSV becomes more negligible as the length of the silicon interposer interconnect increases because the total capacitance of the entire TSV-based channel is increased.

The simulated eye-diagrams of the high-speed TSV-based channels with the TSV and the silicon interposer interconnect variations are shown in Fig. 3.23. As expected, the simulated eye-diagrams at the silicon interposer interconnect of 1 mm are almost the same due to the negligible impact of the TSV and silicon interposer. In the case of the silicon interposer interconnect lengths of 4 and 10 mm, the eye-diagrams are evidently sensitive to the silicon interposer interconnect variation, whereas they are still insensitive to the TSV variation.

3.3.3 Example: Measurement of the High-Speed TSV-Based Channel

In this subsection, the measurement and analysis of a high-speed TSV-based channel are demonstrated with an example. Two types of test vehicles, which are classified by the impact of the TSV to the channel loss, are fabricated and measured. Based on the analyzed electrical properties of the high-speed TSV-based channel in the previous subsection, the measurement results are additionally analyzed.

3.3.3.1 Fabricated Test Vehicle for Measurement

There are two types of test vehicles, which are classified by the number of TSVs and the length of the silicon interposer interconnect. Interconnects in the fabricated test vehicles are designed to be single-ended GSGs. Figure 3.24a, b depict the top and side views, respectively, of test vehicle A, which consists of two TSVs and a short silicon interposer interconnect. In test vehicle A, the impact of the TSVs on the channel loss is considerable because the number of TSVs is two and the length of the silicon interposer interconnect is sufficiently short. Figure 3.25a, b depict the top and side views, respectively, of test vehicle B, which consists of one TSV and

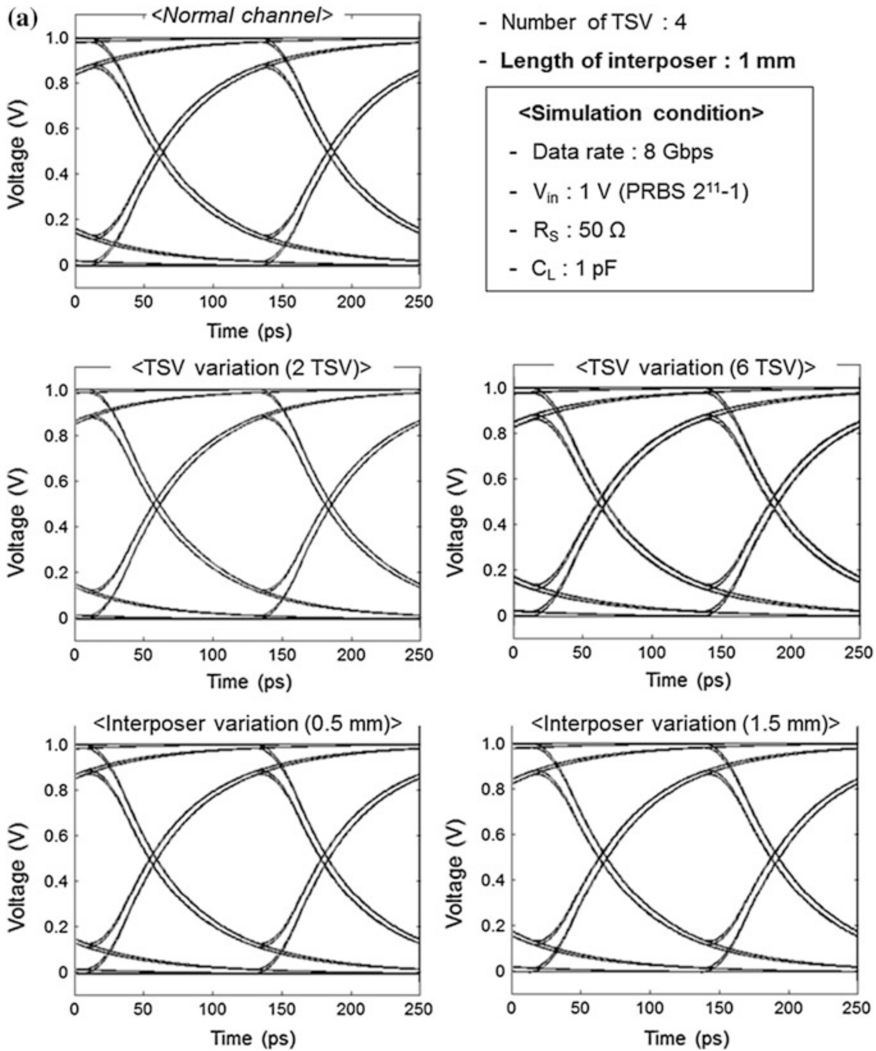


Fig. 3.23 Eye-diagram of the TSV-based channel at data rates of 8 Gbps (Stacking number of TSV and interconnect length of silicon interposer variations). Baseline lengths of silicon interposer interconnects are **a** 1 mm **b** 4 mm **c** 10 mm

a long interposer interconnect. In contrast to test vehicle A, the loss of the silicon interposer interconnect is dominant in test vehicle B due to its long length and the reduced number of TSVs. The physical dimensions of test vehicles A and B are summarized in Table 3.3.

Scanning electron microscope (SEM) images of the cross-sectional views of a fabricated test vehicle are shown in Fig. 3.26. Figure 3.26a shows the overview of the fabricated test vehicle. Figure 3.26b–d show the magnified images of the TSV,

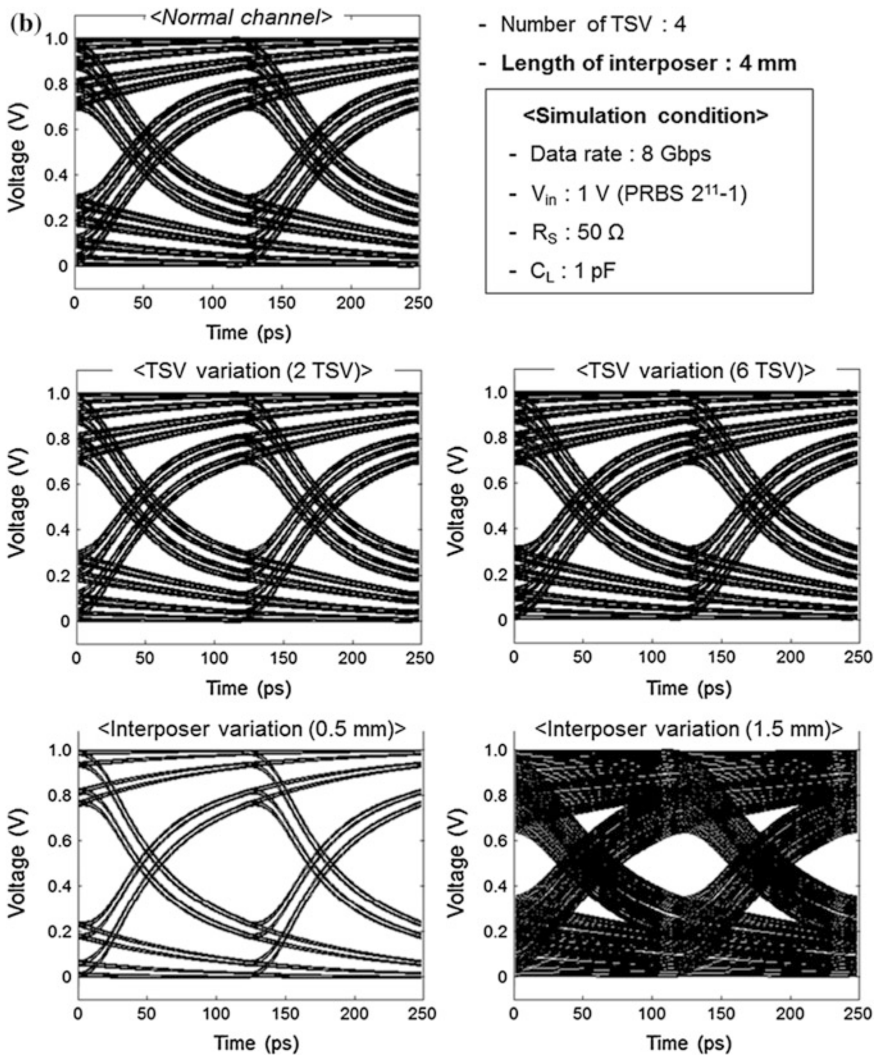


Fig. 3.23 continued

the silicon interposer interconnect and their oxide layers. The thickness of the interposer interconnect, the oxide layer on the TSV and the oxide-layer under the interposer interconnect are 3, 0.5, and 0.2 μm, respectively. Copper is used for the TSV and the interposer interconnect, and the silicon conductivities of the top and the bottom chips are 12 and 14 S/m, respectively.

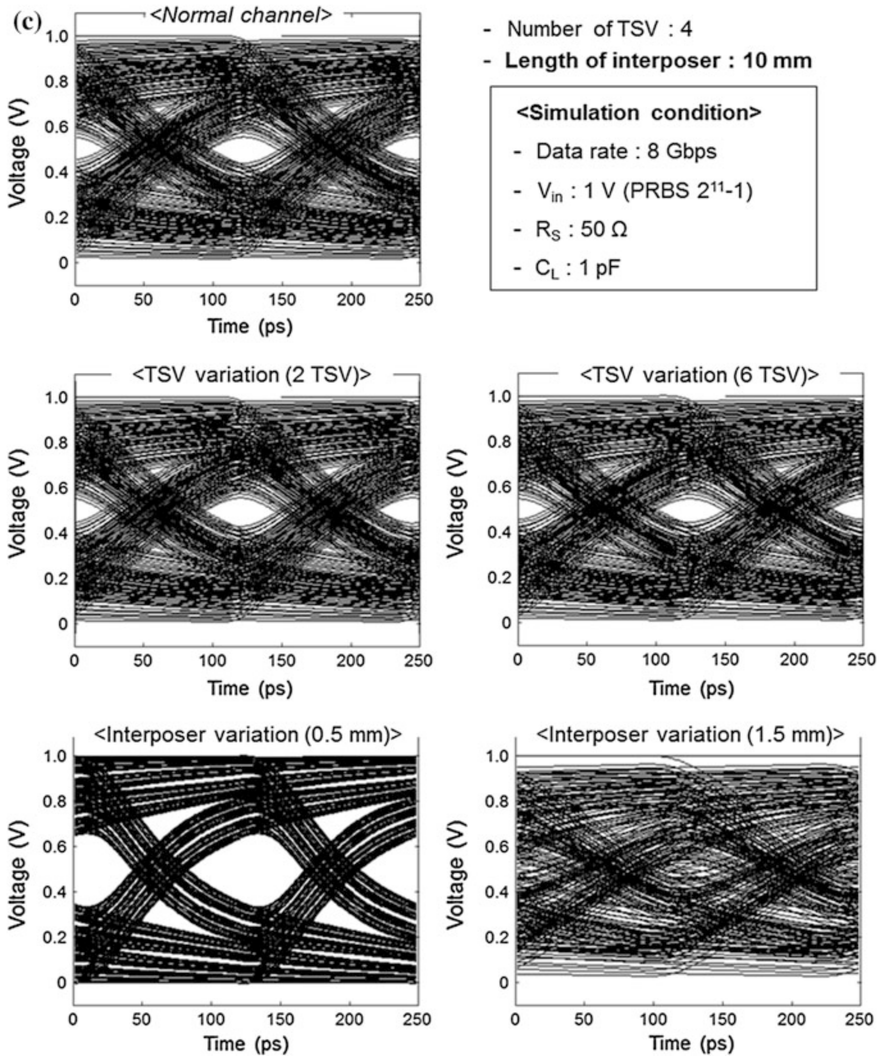


Fig. 3.23 continued

3.3.3.2 Measurement Results

The measurement setups for the frequency-domain and the time-domain are shown in Fig. 3.27a, b, respectively. In the frequency-domain measurements, a Vector Network Analyzer (VNA) was used to measure the S_{21}. The VNA, model *N2530A* from *Agilent Technologies*, has a bandwidth covering a frequency range from 300 kHz to 20 GHz. In the time-domain measurements, a pulse-pattern generator (PPG) and a digital sampling oscilloscope were used to measure the eye-diagram. The PPG, model *MP-1763C* from *Anritz*, has a sampling rate of 12.5 Gbps. The

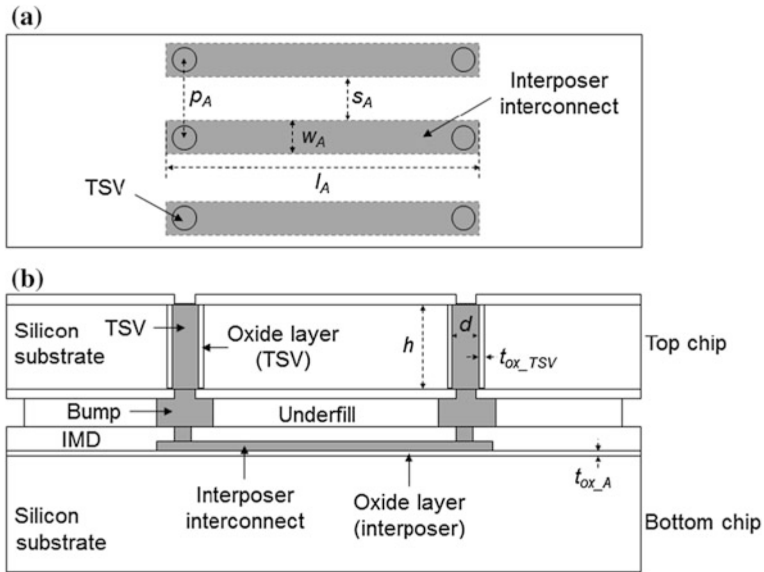


Fig. 3.24 Structure of test vehicle A **a** *Top view* **b** *Side view* [2] © 2012 IEEE

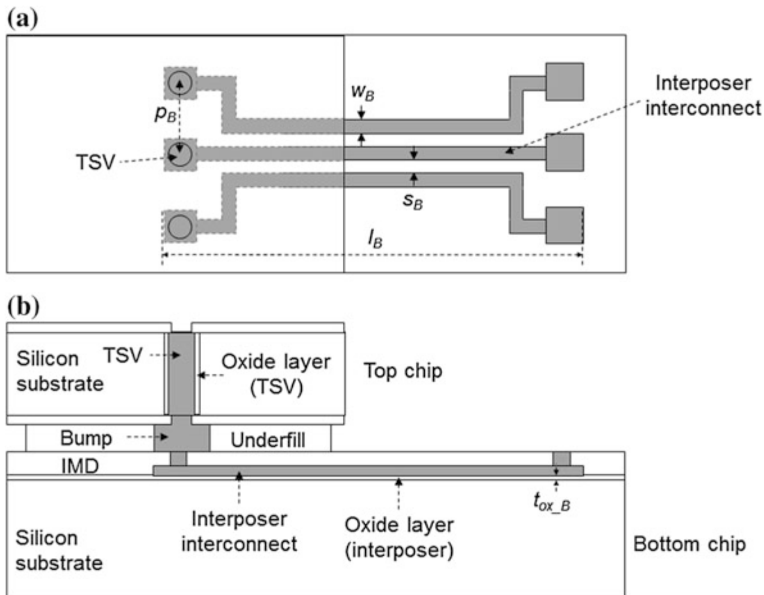


Fig. 3.25 Structure of test vehicle B **a** *Top view* **b** *Side view* [2] © 2012 IEEE

Table 3.3 Physical dimensions of test vehicles A and B [2] © 2012 IEEE

	Symbol	Value	
		Test vehicle A (μm)	Test vehicle B (μm)
TSV	D	44	
	H	50	
	t_{ox_TSV}	0.5	
Silicon interposer interconnect	l_A, l_B	150 /250 /500	2,000 /3,000 /4,000
	w_A, w_B	60	20
	s_A, s_B	90	20
	p_A, p_B	150	
	t_{ox_A}, t_{ox_B}	0.2	

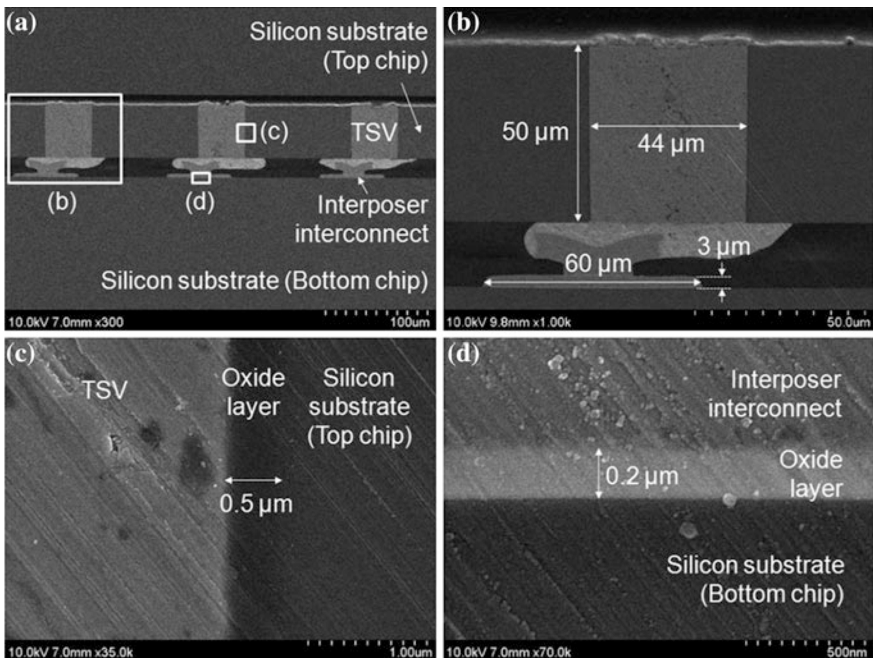


Fig. 3.26 SEM image of the fabricated test vehicle [15] © 2012 IMAPS

generated data pattern from the PPG was a pseudo-random-bit-sequence (PRBS) of 2^{11}-1, with a rise and fall time of 30 ps. The input voltage from the PPG was 1 V. The digital sampling oscilloscope, model *TDS8000B* from *Tektronix*, has a bandwidth of 20 GHz. For accurate frequency-domain measurements, a high-frequency cable with a bandwidth of 40 GHz was used. Impacts of the cable and the microprobe to the frequency-domain measurement were de-embedded by a 2-port SOLT calibration method, while their loss was included in the time-domain

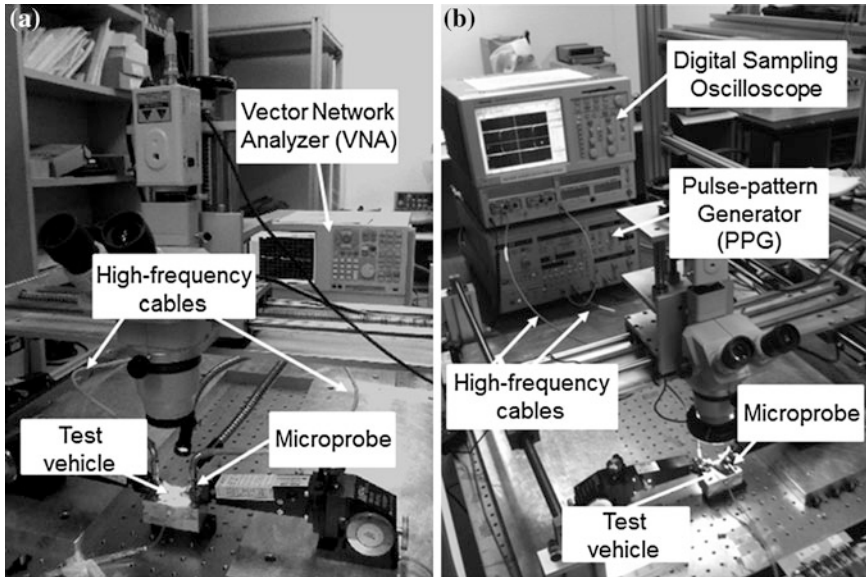


Fig. 3.27 Measurement setups for **a** frequency-domain **b** time-domain [2] © 2012 IEEE

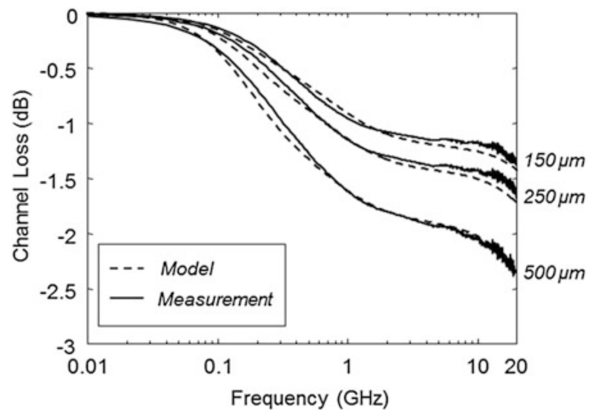


Fig. 3.28 The measured channel loss of test vehicle A [2] © 2012 IEEE

measurement. Because the loss of the high-frequency cable is only 1.7 dB at 20 GHz, the impact of the cable on the measured eye-diagram is minimal. A microprobe was used instead of a connector-based interconnect for more accurate measurements.

The measured channel losses of test vehicles A and B, respectively, are shown in Figs. 3.28 and 3.29. The measured channel loss curves have good correlation with the model and the analysis in the previous subsections. Though the structures of the TSV-based channel in the test vehicles are different from those in the

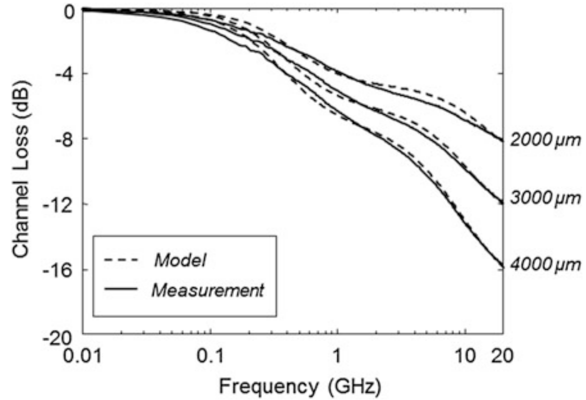


Fig. 3.29 The measured channel loss of test vehicle B [2] © 2012 IEEE

previous subsection, the overall shapes of the measured channel loss curves of the test vehicles are very similar to that of the silicon interposer interconnect (CPW on M1) in Fig. 3.12a. Due to the thin oxide-layer of the silicon interposer interconnect in test vehicle A, the frequency at which the loss of the channel is enhanced by the lossy silicon substrate is decreased to approximately 100 MHz. Though the silicon interposer interconnect in test vehicle A is shorter than that of Fig. 3.12a, the measured channel loss is slightly higher due to the increased silicon conductivity and the considerable loss of TSVs. Compared to the channel loss curves in Fig. 3.19, those of test vehicle B are much higher due to the thin oxide-layer of the silicon interposer interconnect and the increased silicon conductivity. Because the width of the interposer interconnect in test vehicle B is narrower than that of test vehicle A, the frequency at which the loss of the channel is enhanced by the lossy silicon substrate in test vehicle B is higher than that for test vehicle A. However, the narrower width of test vehicle B has no considerable impact on the channel loss at the mid- and high-frequency ranges because the space is reduced at the same time; the silicon conductances of the silicon interposer interconnect per unit length in test vehicle A and B are almost the same, as shown in Table 3.4.

The measured eye-diagrams of test vehicle A ($l_A = 500$ μm) at data rates of 1 and 10 Gbps, respectively, are shown in Fig. 3.30a, b; those of test vehicle B ($l_B = 4{,}000$ μm) are shown in Fig. 3.31a, b. As analyzed in the previous subsection, the impact of the reflection is negligible in the measured eye-diagrams of the high-speed TSV-based channel because the reflected wave is considerably attenuated by the lossy silicon substrate; the small ringing in the measured eye-diagram is not from channel reflection, but is inherent in the input signal. Because test vehicle B has a higher channel loss compared to test vehicle A, the inherent ringing of the input signal is not observed in the measured eye-diagram.

Table 3.4 Lumped components of the (a) TSV (b) silicon interposer interconnect [2] © 2012 IEEE

(a)	R_{TSV}	L_{TSV}	$G_{Si_TSV_tot}$	$C_{Si_TSV_tot}$	$C_{ox_TSV_tot}$
TSV	$10^{-7} \times \sqrt{f}$	0.084 nH	0.0018 S	0.0138 pF	0.3 pF

(b)	R_{Int} (Ω/mm)	L_{Int} (nH/mm)	$G_{Si_Int_tot}$ (S/mm)	C_{Int_tot} (pF/mm)	$C_{ox_Int_tot}$ (pF/mm)
Interposer (TV A)	0.144	0.48	0.013	0.104	11.2
Interposer (TV B)	0.36	0.55	0.014	0.106	3.9

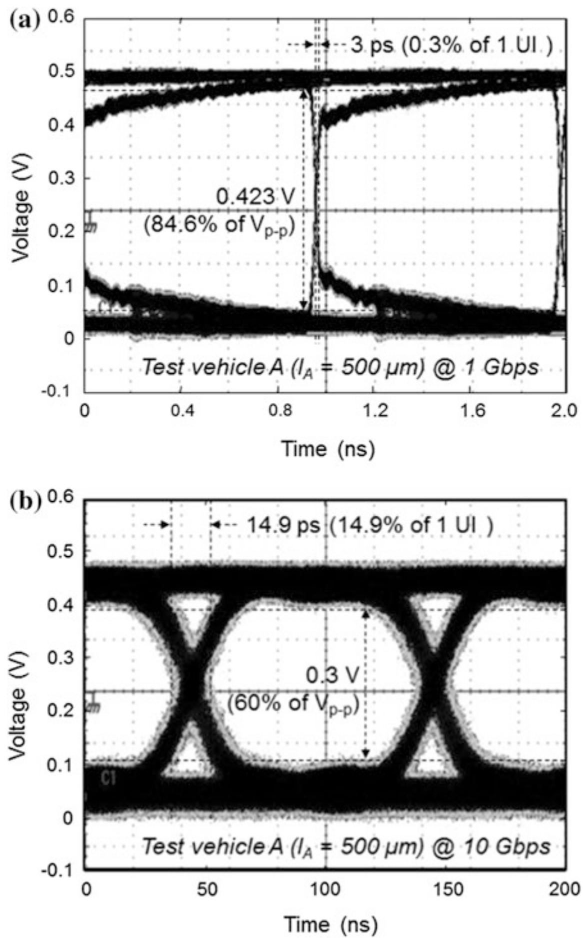


Fig. 3.30 The measured eye-diagram of test vehicle A at **a** 1 Gbps **b** 10 Gbps [2] © 2012 IEEE

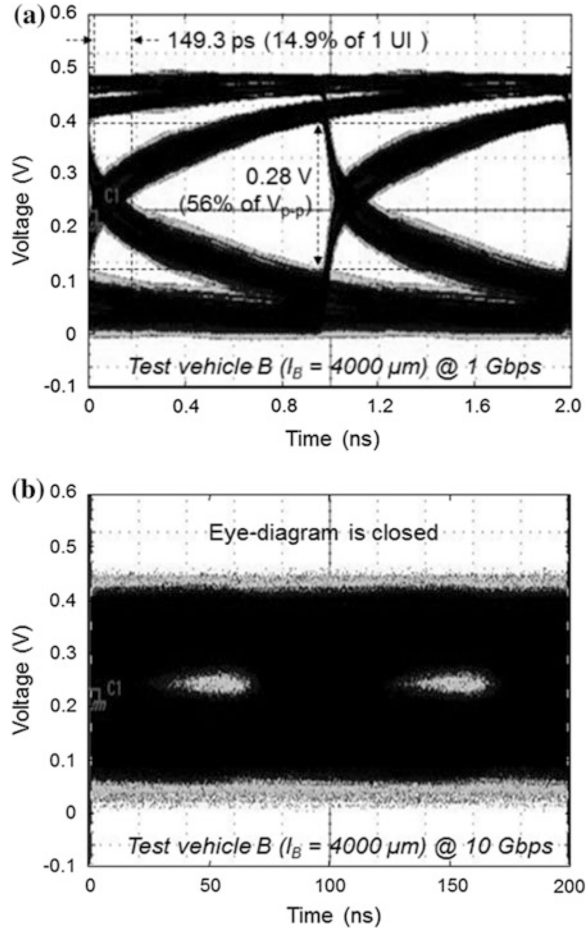


Fig. 3.31 The measured eye-diagram of test vehicle B at **a** 1 Gbps **b** 10 Gbps [2] © 2012 IEEE

3.3.3.3 Analyses of the Impacts of Silicon Conductance and Oxide Capacitance on the Loss of the TSV-Based Channel

In this sub-subsection, the channel loss of the high-speed TSV-based channel is additionally analyzed in accordance with the silicon conductance and the oxide capacitance of the TSV and the silicon interposer interconnect. In the previous subsections, the impacts of the TSV and the silicon interposer interconnect to the channel loss are separately analyzed. As analyzed in Sect. 3.3.2.3, the impact of the TSV to the total TSV-based channel can be considerable when the length of the silicon interposer interconnect is sufficiently short; test vehicle A is corresponds to this case. Therefore, the co-analysis of the TSV and the silicon interposer interconnect for the channel of test vehicle A is quite meaningful.

To analyze the loss of the high-speed TSV-based channel, values for the lumped components of a TSV and a silicon interposer interconnect are determined

and listed in Table 3.4. The lumped components of the TSV-based channel in Table 3.4 are those of the equivalent-circuit models; the models in reference papers [8, 16–18] are used for the TSV. $G_{Si_TSV_tot}$, $C_{Si_TSV_tot}$, $C_{ox_TSV_tot}$, $G_{Si_Int_tot}$, C_{Int_tot}, and $C_{ox_Int_tot}$ indicate the total conductances and capacitances. As listed in Tables 3.4a, b, all of the lumped components of the high-speed TSV-based channel except the TSV resistance are frequency independent because the skin effect can be neglected in the silicon interposer interconnect due to the thin metal, and the inductance, capacitance, and conductance are only determined by the structure; the TSV resistance is frequency dependent due to the large diameter.

As listed in Table 3.4, the considerable loss of the high-speed TSV-based channel is caused by the high silicon conductances ($G_{Si_TSV_tot}$ and $G_{Si_Int_tot}$) and oxide capacitances ($C_{ox_TSV_tot}$ and $C_{ox_Int_tot}$) from the losses due to the silicon substrate and the thin oxide layer, respectively. The considerable silicon conductance of the TSV and silicon interposer interconnect ($G_{Si_TSV_tot}$, $G_{Si_Int_tot}$) lead to the considerable channel loss. The large oxide capacitances also contribute to the loss of the high-speed TSV-based channel. If the oxide capacitances are sufficiently small, the silicon conductance can be negligible up to the high-frequency range. Unfortunately, the oxide capacitances are very high due to the thin thickness of the oxide-layers (0.5 μm in TSV and 0.2 μm in interposer), leading to a channel loss due to the silicon conductance, beginning at a frequency of approximately 100 MHz.

Table 3.4 enables a more strict analysis for the measured channel losses in Figs. 3.28 and 3.29. As listed in Table 3.4b, $G_{Si_Int_tot}$ of test vehicle A is almost the same as that of test vehicle B. Because the silicon interposer interconnect of test vehicle B is longer than that of test vehicle A, the overall channel loss of test vehicle B is higher than that of test vehicle A. Although the number of TSVs is reduced in test vehicle B, the impact of the silicon interposer interconnect is higher than that of the TSV due to the relatively long length. However, the wide width of the silicon interposer interconnect in test vehicle A makes $C_{ox_Int_tot}$ of test vehicle A three times larger than that of test vehicle B, as shown in Table 3.4b. This means that $G_{Si_Int_tot}$ of test vehicle A dominantly affects the channel loss at the lower frequency than that of test vehicle B. Therefore, the channel loss of test vehicle A increases rapidly at approximately 100 MHz, whereas the loss of test vehicle B increases rapidly at higher frequencies.

To analyze the impacts of the interposer silicon conductance (G_{Si_Int}), the TSV silicon conductance (G_{Si_TSV}), the interposer oxide capacitance (C_{ox_Int}), and the TSV oxide capacitances (C_{ox_TSV}) on the loss of the high-speed TSV-based channel, the channel losses are simulated in accordance with them. The test vehicle A that has the considerable impact of TSV to the channel loss of the total TSV based channel is employed as the target channel for simulation, and the simulation results are shown in Fig. 3.32.

The TSV and the silicon interposer interconnect have an effect on the channel loss over completely different frequency ranges. As shown in Table 3.4, $G_{Si_Int_tot}$ and $C_{ox_Int_tot}$ are much larger than $G_{Si_TSV_tot}$ and $C_{ox_TSV_tot}$ due to the wide width and relatively long length of the silicon interposer interconnect. As a result, G_{Si_Int}

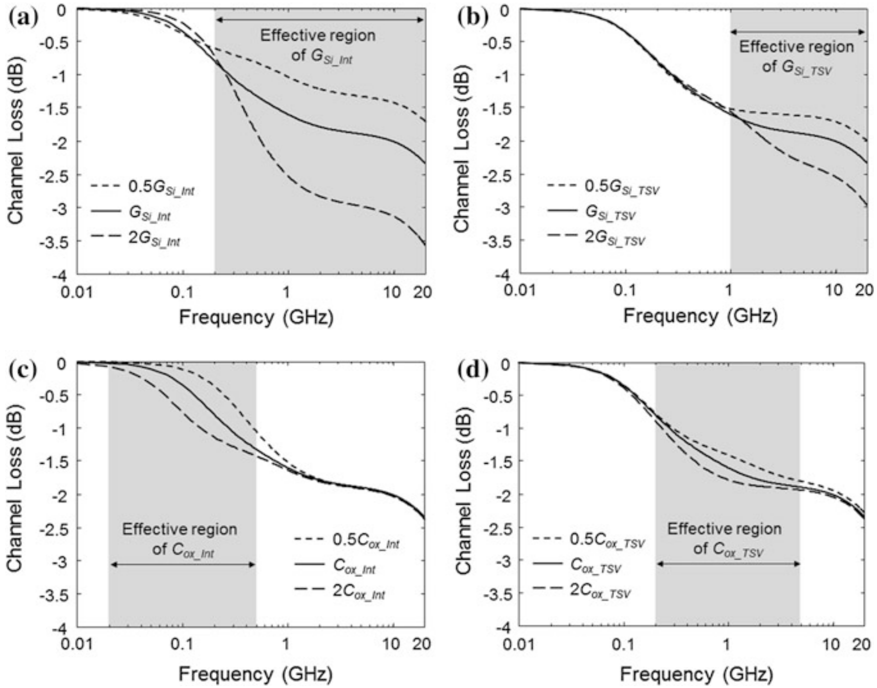


Fig. 3.32 Loss of the TSV-based channel with the variations of **a** interposer silicon conductance (G_{Si_Int}) **b** TSV silicon conductance (G_{Si_TSV}) **c** interposer oxide capacitance (C_{ox_Int}) **d** TSV oxide capacitance (C_{ox_TSV}) [2] © 2012 IEEE

and C_{ox_Int} affect the loss of the TSV channel at a lower frequency than G_{Si_TSV} and C_{ox_TSV}. Therefore, G_{Si_Int} determines the amount of the channel loss from approximately 100 MHz and G_{Si_TSV} determines the amount of the channel loss from approximately 1 GHz, as shown in Fig. 3.32a, b. In the same manner, C_{ox_Int} determines the frequency at which the channel loss increases rapidly due to the silicon conductance beginning at approximately 10 MHz, and C_{ox_TSV} determines the loss with increasing frequency beginning at approximately 100 MHz, as shown in Fig. 3.32c, d.

3.3.4 Example: Comparison to MCM Channel

In this subsection, the electrical properties of the high-speed TSV-based channel are compared to those of the MCM channel that is employed for the first-level packaging interconnection. Due to the different dimensions and materials, the unique electrical properties of the high-speed TSV-based channel can be distinguished from those of the MCM channel through comparison. The TSV-based

Table 3.5 Specifications of MCM channel for comparison [2] © 2012 IEEE

Type	Length (mm)	Width (μm)	Metal thickness (μm)	Substrate thickness (μm)	Permittivity	Loss tangent
Microstrip	100	250	25	150	4.4	0.01

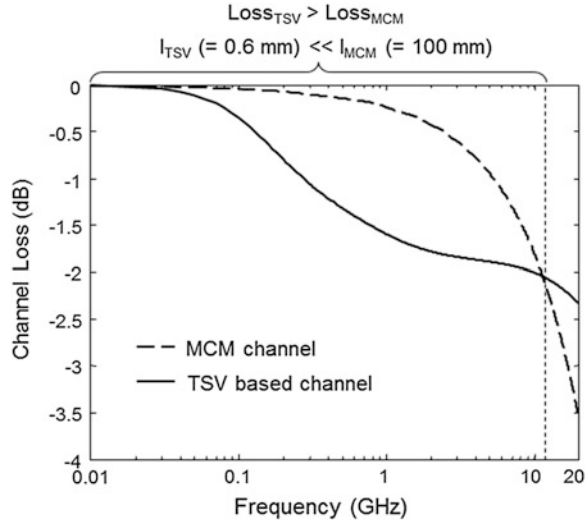


Fig. 3.33 Channel losses of TSV-based channel and MCM channel [2] © 2012 IEEE

channel used for comparison is test vehicle A (l_A = 500 μm), and the specifications of the MCM channel used for comparison are shown in Table 3.5. Similar to the measured TSV-based channel, the compared MCM channel is also single ended.

As shown in Figs. 3.28 and 3.29, the channel loss of the TSV-based channel is very high. Although the channel only consists of two TSVs of 50 μm in height and a silicon interposer interconnect of 500 μm in length, the channel loss is 2.4 dB at 20 GHz. Moreover, the loss of the TSV-based channel consisting of one TSV and the silicon interposer interconnect of 4000 μm in length is 15.8 dB at 20 GHz. The enormous loss of the TSV-based channel is illustrated when we compared to the loss of the relatively long MCM channel. The comparison between the channel losses of the TSV based channel and the MCM channel is shown in Fig. 3.33. Although the length of the MCM channel is 170 times longer than the TSV based channel, the loss of the TSV based channel is higher than that of the MCM channel for frequencies up to approximately 10 GHz.

To compare the considerable loss of the TSV-based channel to the MCM channel, the value for the lumped components of a MCM channel is determined, as listed in Table 3.6. The lumped components of the TSV and the silicon interposer interconnect are those of the values in Table 3.5. In contrast to the constant resistance and conductance of the TSV-based channel, those of the MCM channel

Table 3.6 Lumped components of a MCM channel [2] © 2012 IEEE

	R_{MCM} (Ω/mm)	L_{MCM} (nH/mm)	G_{MCM} (S/mm)	C_{MCM} (pF/mm)
MCM channel	$1.04 \times 10^{-6} \times \sqrt{f}$	0.32	$6 \times 10^{-15} \times f$	0.12

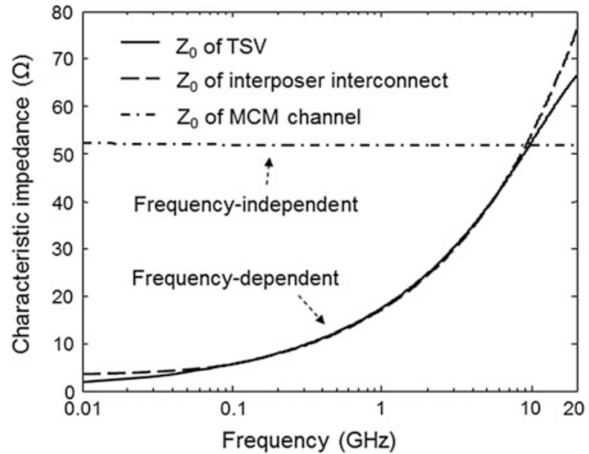


Fig. 3.34 Characteristic impedances of TSV, silicon interposer interconnect and MCM channel [2] © 2012 IEEE

are frequency dependent due to the skin effect and the frequency-dependent dielectric loss. The conductance of the MCM channel (G_{MCM}) is only 0.0005 S at 1 GHz, and it is much less than that of the TSV-based channel. However, the conductance of the MCM channel exceeds 0.005 S for frequencies over 10 GHz. Therefore, the loss of the TSV-based channel is higher than that of the MCM channel up to frequencies of approximately 10 GHz, as shown in Fig. 3.33.

The characteristic impedances of the TSV, the silicon interposer interconnect and the MCM channel are shown in Fig. 3.34. In contrast to the frequency-independent characteristic impedance of the MCM channel, the characteristic impedances of the

$$Z_0 = \sqrt{\frac{R + jwL}{G + jwC}} \quad \rightarrow \quad Z_{0_MCM} \approx \sqrt{\frac{L}{C}}\Bigg|_{R \ll jwL, G \ll jwC} \tag{3.12}$$

TSV and the silicon interposer interconnect vary with frequency. Thus, the characteristic impedance of the high-speed TSV-based channel is difficult to match perfectly due to its frequency dependence. In general, the characteristic impedance of the MCM channel is solely determined by the inductance and capacitance due to the negligible resistance and conductance, making it frequency independent as shown in (3.12). However, the significant silicon conductance of the TSV and the silicon interposer interconnect causes the frequency-dependent characteristic impedances in the TSV and the silicon interposer interconnect. The resistance can

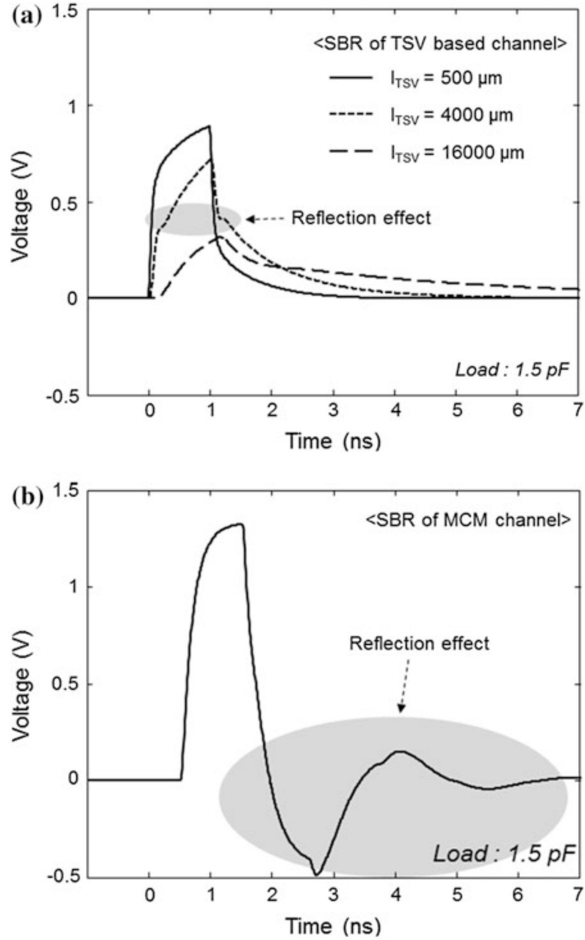


Fig. 3.35 Single-bit responses of **a** TSV-based channel **b** MCM channel [2] © 2012 IEEE

also cause the characteristic impedance of the TSV channel to become frequency dependent in a practical design.

The impact of the reflection in the high-speed TSV-based channel is also different from that of the MCM channel. The single-bit responses of the TSV-based channel and the MCM channel are simulated for comparison. A load capacitance of 1.5 pF is used for the simplified model of the I/O driver in this example. The simulation results are shown in Fig. 3.35a, b. The MCM channel with the reduced width of 50 μm is simulated to observe the reflection effect in the MCM channel.

As shown in Fig. 3.35, the impact of reflection is negligible in the single-bit response of the TSV-based channel, whereas a considerable reflection is observed in the MCM channel; the single-bit response of the MCM channel is delayed by 0.7 ns due to its long length. The TSV-based channel is too short to be affected by reflection. Moreover, the reflected wave of the TSV-based channel is severely

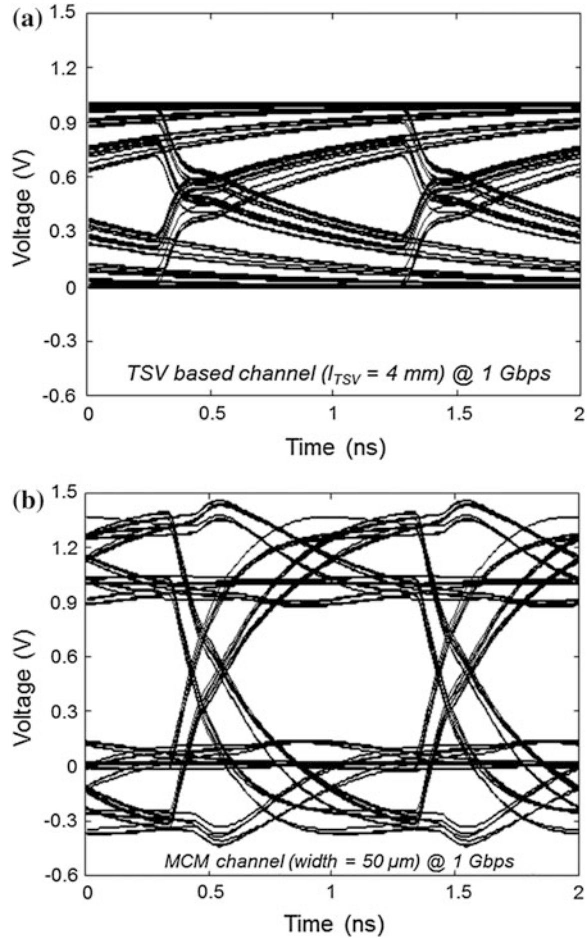


Fig. 3.36 Eye-diagrams of a **a** TSV-based channel **b** MCM channel at data rate of 1 Gbps [2] © 2012 IEEE

attenuated by the high silicon conductance. Even as the length of the TSV-based channel is increased to 4,000 and 16,000 μm, the impact of reflection is still negligible because the silicon conductance is also proportionally increased; the increased silicon conductance severely attenuates the reflected wave. The impact of reflection is considerable in the MCM channel because the length is sufficiently long and the channel loss is relatively small.

The simulated eye-diagrams of the TSV-based channel and the MCM channel at a data rate of 1 Gbps are shown in Fig. 3.36a, b, respectively. Though the eye-diagram of the TSV channel is somewhat distorted by the reflected wave, the amount of distortion is not overwhelming. Compared to the TSV-based channel, the eye-diagram of the MCM channel is remarkably distorted by the reflected wave.

3.4 Worst-Case Eye-Diagram Estimation Algorithm

The eye-diagram, which is a convenient graphical method for analyzing a received digital signal, is widely used for analyzing signal integrity. However, obtaining an eye-diagram of a TSV-based channel is embarrassed due to the complexity of the channel. Full-wave simulations and measurements of an eye-diagram in a TSV-based channel are limited by time consumption and fabrication of the test vehicles. Several studies aimed at efficiently estimating eye-diagrams [19–23], including the worst-case eye-diagram estimation, have been conducted. The worst-case eye-diagram estimation can be a good solution for overcoming these limitations because it only estimates the inner contour of the eye-diagram (that determines the eye-opening voltage and timing jitter) within a remarkably short time.

In this section, a fast and precise worst-case eye-diagram estimation algorithm for a high-speed TSV-based channel is introduced. In Sects. 3.4.1 and 3.4.2, the definition of the worst-case eye-diagram and the detail of the estimation algorithm are explained. To demonstrate the efficiency of the introduced worst-case eye-diagram algorithm for a high-speed TSV-based channel, the estimated worst-case eye-diagram is compared to the simulation and verified by the measurement in Sect. 3.4.3.

3.4.1 Worst-Case Eye-Diagram

The eye-diagram is a convenient graphical method for analyzing the degraded received digital signal with a random bit sequence. It is obtained by repetitively sampling the received digital signal with the unit-interval (UI) of a specific data rate. The eye-diagram is generally employed to analyze the signal integrity of the high-speed channel because it intuitively indicates the timing and voltage margins.

The worst-case eye-diagram is a type of simplified eye-diagram that indicates the timing and voltage margins. The eye-diagram and corresponded worst-case eye-diagram are shown in Fig. 3.37. As shown in Fig. 3.37a, the eye-width and eye-opening voltage that correspond to the timing and voltage margins are determined by the inner contour of the eye-diagram; the timing jitter can be obtained by subtracting the eye-width from 1 unit-interval. Because the inner contour of the eye-diagram is the combination of the worst output responses of Logic 0 and Logic 1, the worst-case eye-diagram is the same as the inner contour of the eye-diagram.

The advantage of the worst-case eye-diagram is the remarkably short estimation time. In the case of a general eye-diagram, a considerably long bit sequence should be employed as the input for an accurate transient simulation. However, the worst-case eye-diagram requires a much shorter bit sequence that corresponds to the worst-case bit pattern, resulting in a much shorter estimation time.

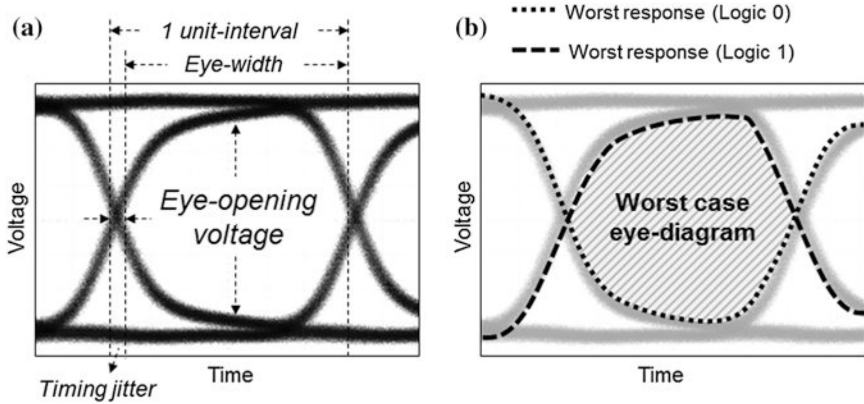


Fig. 3.37 **a** Eye-diagram and **b** Worst-case eye-diagram

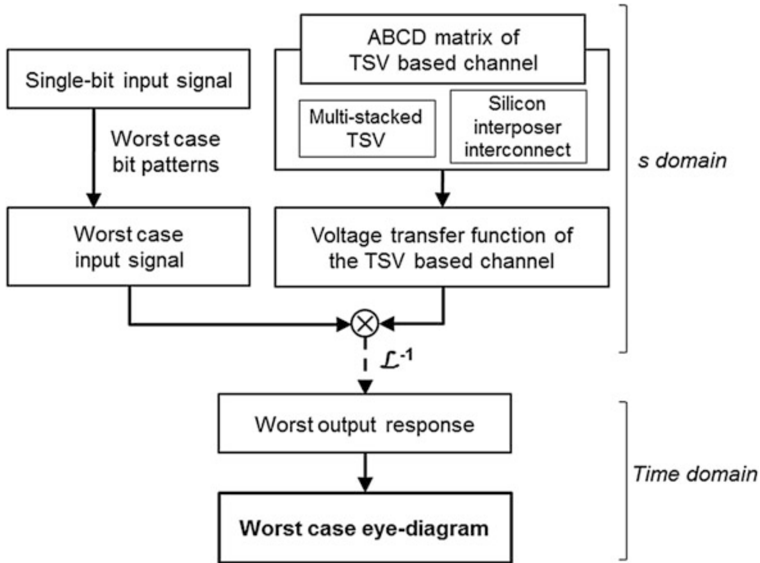


Fig. 3.38 Overview of the worst-case eye-diagram estimation algorithm for high-speed TSV-based channel [15] © 2012 IMAPS

3.4.2 Worst-Case Eye-Diagram Estimation Algorithm

The overview of worst-case eye-diagram estimation algorithm for a high-speed TSV-based channel is shown in Fig. 3.38. The inner contours of the eye-diagram that determine the eye-opening voltage and timing jitter are composed of the worst output responses. Thus, we assume that the worst-case input signals correspond to

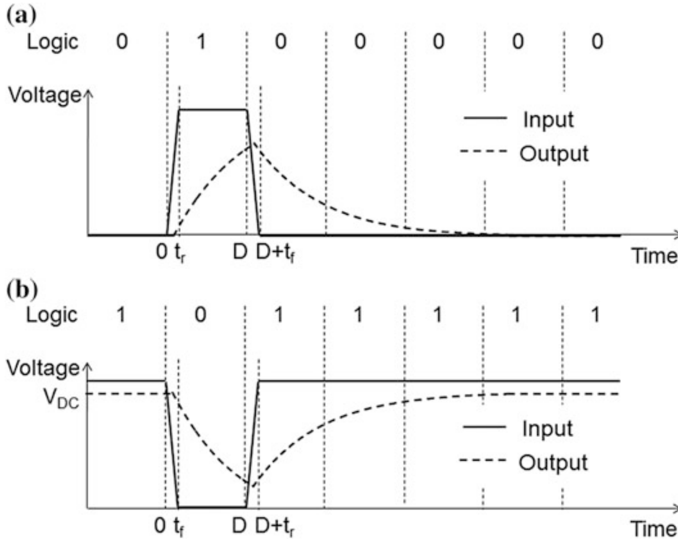


Fig. 3.39 Worst-case input signals of **a** logic ‘1’ **b** logic ‘0’

the worst output responses of the channel and use them instead of the PRBS input. The worst output responses of the TSV-based channel can be obtained by combining the assumed worst-case input signals and the voltage transfer function of the TSV-based channel. Then, the worst-case eye-diagram of the TSV-based channel can be estimated by using the obtained worst-case output responses.

In order to significantly reduce the estimation time, the worst-case input signal is employed instead of the PRBS signal. If we know the worst-case bit patterns, the worst-case input signal can be obtained by combining it with the single-bit input signal. In general, the worst-case bit pattern of the channel can be obtained by using the peak distortion analysis (PDA) method; it determines the worst-case bit pattern by considering the inter-symbol interference (ISI) voltages at all of the sampling times [19]. In this book, the algorithm employs the PDA method to find the worst-case bit pattern of the high-speed TSV-based channel. Due to the considerably high loss of the TSV-based channel resulting from the lossy silicon substrate and the high resistance of the silicon interposer interconnect, it is quite reasonable to assume that the impact of reflection is negligible in the TSV-based channel. This implies that the output response has monotonic rising and falling properties and that the single-bit pulse results in the least amount of transition of output response in the TSV-based channel. Therefore, if we employ the PDA method to determine the worst-case bit patterns, the single-bit pulse should always be the worst-case input signals of logic ‘1’, which corresponds to the worst output response of logic ‘1’ in the TSV-based channel, as shown in Fig. 3.39a. In the case of logic ‘0’, the inverse single-bit pulse becomes the worst-case input signal of logic ‘0’ and it considers the DC voltage drop, resulting in V_{DC} as shown in

Fig. 3.39b. To consider the realistic signal, the rise time (t_r) and fall time (t_f) are included in the assumed worst case input signals. The *s*-domain equations of the worst-case input signals of logic '1' and logic '0' are shown in (3.13) and (3.14). D implies the 1 UI.

$$X_{Logic1}(s) = \left\{ \frac{1}{t_r}(1 - e^{-t_r s}) + \frac{1}{t_f}\left(-e^{-Ds} + e^{-\left(D+t_f\right)s} \right) \right\} \frac{1}{s^2} \tag{3.13}$$

$$X_{Logic0}(s) = \delta(s) - \left\{ \frac{1}{t_r}(1 - e^{-t_r s}) + \frac{1}{t_f}\left(-e^{-Ds} + e^{-\left(D+t_f\right)s} \right) \right\} \frac{1}{s^2} \tag{3.14}$$

Due to the complicated structure of the TSV-based channel, the voltage transfer function of the TSV-based channel is also complicated. The voltage transfer function of the TSV-based channel is hard to define because the TSV and silicon interposer interconnect are severely entangled in a practical TSV-based channel. In order to derive the *s*-domain equation of the voltage transfer function of the TSV-based channel, the worst-case eye-diagram estimation algorithm employs ABCD matrices of the sub-sections that make up the TSV-based channel. The ABCD matrices of the multi-stacked TSV and the silicon interposer interconnect can be easily obtained from the equivalent-circuit models, and the voltage transfer function of the TSV-based channel can be derived by using them.

$$\begin{bmatrix} A_{TSV} & B_{TSV} \\ C_{TSV} & D_{TSV} \end{bmatrix} \approx \begin{bmatrix} 1 + N^2(R_{TSV} + sL_{TSV}) \times \left(\frac{2.4 \times sC_{ox__TSV}(G_{Si__TSV} + sC_{Si__TSV})}{G_{Si__TSV} + s(1.2C_{ox__TSV} + C_{Si__TSV})} \right) & N(R_{TSV} + sL_{TSV}) \\ N\left(\frac{2.4 \times sC_{ox__TSV}(G_{Si__TSV} + sC_{Si__TSV})}{G_{Si__TSV} + s(1.2C_{ox__TSV} + C_{Si__TSV})} \right) & 1 \end{bmatrix} \tag{3.15}$$

The equivalent-circuit model of the multi-stacked TSV should be the distributed model in which several models of single TSVs are cascaded in series. Though many TSVs are stacked vertically, the height of the entire TSV channel is still too short because the height of a single TSV follows thin thickness of the silicon substrate. Therefore, the distributed model of the multi-stacked TSV can be simplified to a single RLGC model when the entire height of the multi-stacked TSV channel is below 500 μm at the operating data rates of 20 Gbps. Then, the ABCD matrix of the multi-stacked TSV is derived as (3.15). *N* implies the stacking number of TSVs.

$$\begin{bmatrix} A_{Int} & B_{Int} \\ C_{Int} & D_{Int} \end{bmatrix} \approx \begin{bmatrix} 1 + (R_{Int} + sL_{Int}) \times \left(sC_{Int} + \frac{\frac{2}{3} \times sC_{ox_Int}(G_{Si_Int} + sC_{Si_Int})}{G_{Si_Int} + s\left(\frac{2}{3}C_{ox_Int} + C_{Si_Int}\right)} \right) & R_{Int} + sL_{Int} \\ sC_{Int} + \frac{\frac{2}{3} \times sC_{ox_Int}(G_{Si_Int} + sC_{Si_Int})}{G_{Si_Int} + s\left(\frac{2}{3}C_{ox_Int} + C_{Si_Int}\right)} & 1 \end{bmatrix}^M \tag{3.16}$$

Because the silicon interposer interconnect is several millimeters in length (unlike the multi-stacked TSV channel), the interposer interconnect relies on the distributed model for accurate modeling. Therefore, the ABCD matrix of the silicon interposer interconnect is derived as (3.16), which includes the exponent parameter M. M implies the number of single RLGC models shown in Fig. 3.5, and it changes depending on the length of the silicon interposer interconnect.

$$\begin{bmatrix} A_{Total} & B_{Total} \\ C_{Total} & D_{Total} \end{bmatrix} = \begin{bmatrix} 1 & Z_{Tx} \\ 0 & 1 \end{bmatrix} \times \left(\prod_{i,j} \begin{bmatrix} A_{TSV} & B_{TSV} \\ C_{TSV} & D_{TSV} \end{bmatrix}^i \begin{bmatrix} A_{Int} & B_{Int} \\ C_{Int} & D_{Int} \end{bmatrix}^j \right) \times \begin{bmatrix} 1 & 0 \\ Y_{Rx} & 1 \end{bmatrix} \tag{3.17}$$

If we know the ABCD matrices of the transmitter (Tx) and receiver (Rx), we can derive the voltage transfer function of the entire TSV-based channel. In this chapter, we employ the simplified models of I/O, and Tx and Rx are assumed to be a series and a shunt impedance (Z_{TX} and Y_{RX}), respectively. Then, the ABCD matrix of the entire TSV-based channel is derived as (3.17). Because the voltage ratio between the input and output is $\frac{1}{A}$ of the ABCD matrix, $\frac{1}{A_{Total}}$ becomes the s-domain equation of the voltage transfer function of the TSV-based channel [24].

$$g_{Logic1}(t) = L^{-1}\{G_{Logic1}(s)\} = L^{-1}\left\{X_{Logic1}(s) \times \frac{1}{A_{Total}}\right\}$$

$$= L^{-1}\left\{\left[\frac{1}{t_r}(1 - e^{-t_r s}) + \frac{1}{t_f}\left(-e^{-Ds} + e^{-(D+t_f)s}\right)\right] \times \frac{1}{s^2} \times \frac{N_m s^m + N_{m-1}s^{m-1} + \cdots + N_1 s + N_0}{D_n s^n + D_{n-1}s^{n-1} + \cdots + D_1 s + D_0}\right\} \tag{3.18}$$

$$= \sum_i L^{-1}\left\{\left[\frac{1}{t_r}(1 - e^{-t_r s}) + \frac{1}{t_f}\left(-e^{-Ds} + e^{-(D+t_f)s}\right)\right] \times \frac{1}{s^2} \times \left[\frac{K_i}{s + p_i}\right]\right\} \tag{3.19}$$

$$+\sum_j L^{-1}\left\{\left[\frac{1}{t_r}(1-e^{-t_r s})+\frac{1}{t_f}\left(-e^{-Ds}+e^{-(D+t_f)s}\right)\right]\times\frac{1}{s^2}\times\left[\frac{K_{j1}(s+a_j)}{(s+a_j)^2+b_j^2}+\frac{K_{j2}b_j}{(s+a_j)^2+b_j^2}\right]\right\} \tag{3.20}$$

Useful equations for *Inverse Laplace Transform*

$$L^{-1}\left\{\left[\frac{1}{t_r}(1-e^{-t_r s})\right]\times\frac{1}{s^2}\right\}=\frac{1}{t_r}[t\cdot u(t)-(t-t_r)\cdot u(t-t_r)]$$

$$L^{-1}\left\{\left[\frac{1}{t_r}(1-e^{-t_r s})\right]\times\frac{1}{s+p}\right\}=\frac{e^{-pt}}{t_r}[u(t)-u(t-t_r)]$$

$$L^{-1}\left\{\left[\frac{1}{t_r}(1-e^{-t_r s})\right]\times\frac{s+a}{(s+a)^2+b^2}\right\}=\frac{e^{-at}}{t_r}\left[\cos(bt)\cdot u(t)-e^{at_r}\cos(b(t-t_r))\cdot u(t-t_r)\right]$$

$$L^{-1}\left\{\left[\frac{1}{t_r}(1-e^{-t_r s})\right]\times\frac{b}{(s+a)^2+b^2}\right\}=\frac{e^{-at}}{t_r}\left[\sin(bt)\cdot u(t)-e^{at_r}\sin(b(t-t_r))\cdot u(t-t_r)\right]$$

In order to estimate the worst-case eye-diagram of the TSV-based channel, we rely on the worst output responses of logic ‘1’ and ‘0’ in the time-domain. The worst output responses in the *s*-domain can be obtained by multiplying the worst-case input signals to the derived voltage transfer function as shown in the above equations; $g_{Logic1}(t)$ and $G_{Logic1}(s)$ imply the worst output responses of logic ‘1’ in the time- and *s*-domains, respectively. In general, the voltage transfer function of the TSV-based channel should be complex because the channel contains many poles and zeros. Fortunately, the complex *s*-domain equation of the voltage transfer function can be simplified by using the partial fraction expansion method as described in (3.18). Then, the voltage transfer function can be simply classified by the real poles and the complex poles as described in (3.19) and (3.20).

By using (3.19), (3.20) and the above useful equation set for the *inverse Laplace transform*, the worst output responses of the TSV-based channel in the time-domain can be obtained.

The examples of the worst output responses of logic ‘1’ and ‘0’ that can be obtained by using the worst-case input signals and the voltage transfer function of the TSV-based channel are shown in Fig. 3.40a. The worst-case eye-diagram of the TSV-based channel can be estimated by employing these worst output responses, and Fig. 3.40b explains how to estimate it. The eye-diagram is generally estimated by folding the output responses into several time intervals, requiring multi-bits.

Because the worst output responses in Fig. 3.40a only consider single-bits, we shift the worst output responses by several UIs. Then, the worst-case eye-diagram of the TSV-based channel is successfully estimated by focusing on the overlapped

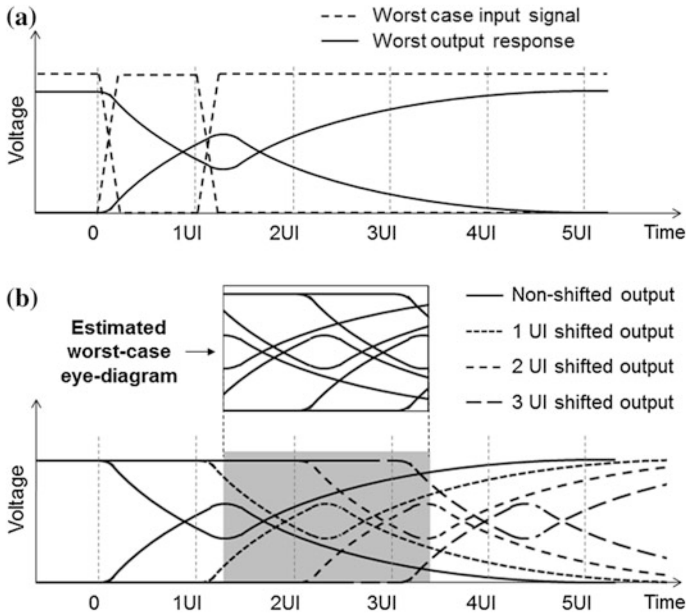


Fig. 3.40 **a** Worst output responses and **b** estimated worst-case eye-diagram

shifted-waveforms as shown in Fig. 3.40b. It is remarkable that shifting the worst output responses by 3 UI is enough to estimate the worst case eye-diagram and the estimation time becomes impressively short.

3.4.3 Verifications by Simulation and Measurement

Figure 3.41 shows the estimated eye-diagrams of test vehicle A (l_A = 500 µm) at a data rate of 10 Gbps. The eye-diagram in Fig. 3.41a is estimated by using the full-wave and circuit-level simulator; the eye-diagram of Fig. 3.41b is estimated by using the worst-case eye-diagram estimation algorithm. The shape of the estimated eye-diagram using the worst-case eye-diagram estimation algorithm is almost the same as that of the simulation; the detailed comparison results are summarized in Table 3.7. Despite the similarly estimated eye-diagrams, the estimation time is significantly reduced by the worst-case eye-diagram estimation algorithm.

In the case of Fig. 3.42, the target TSV-based channel is changed to test vehicle B (l_B = 4,000 µm). The data rate for the eye-diagram simulation is changed to a data rate of 1 Gbps. As shown in Fig. 3.42, the eye-diagrams are successfully estimated by using the full-wave, circuit-level simulators and the worst-case eye-diagram estimation algorithm. As summarized in Table 3.8, the estimated worst-

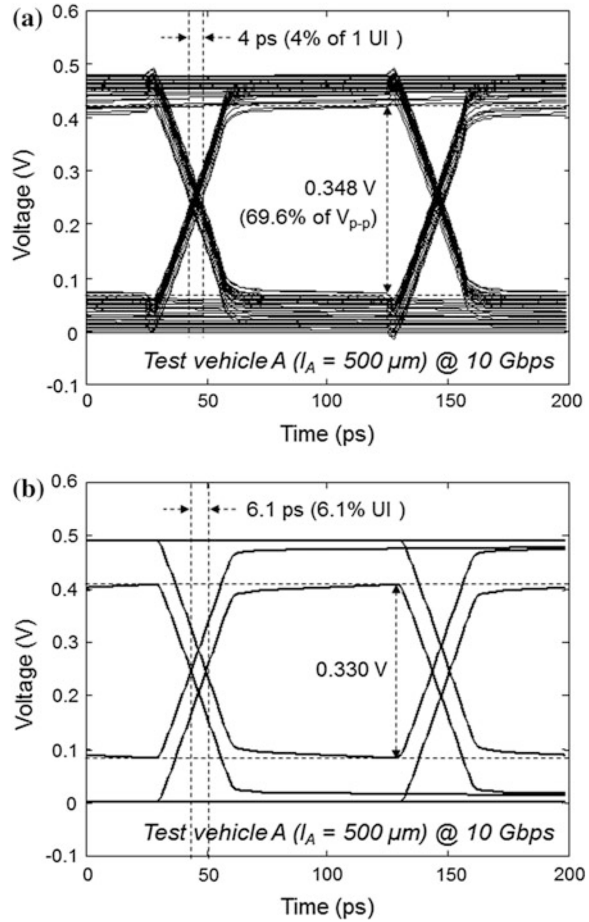


Fig. 3.41 **a** Simulated eye-diagram and **b** estimated worst-case eye-diagram of test vehicle A ($l_A = 500$ μm) at the data rate of 10 Gbps

Table 3.7 Comparison results for test vehicle A

	Full-wave and circuit-level simulators	Worst eye estimation algorithm	Comparison
Eye-opening voltage	0.354 V	0.330 V	4.8 % $V_{p\text{–}p}$ (Error rate)
Timing jitter	4.5 ps	6.1 ps	1.6 % UI (Error rate)
Estimation time	1580 s	2 s	99.9 % (Improvement)

case eye-diagram and the simulated eye-diagram show good correlation, and the estimation time is remarkably reduced.

The measured eye-diagrams and the estimated worst-case eye-diagrams of test vehicles A and B at data rates of 1, 2, 5 and 10 Gbps are shown in Figs. 3.43 and

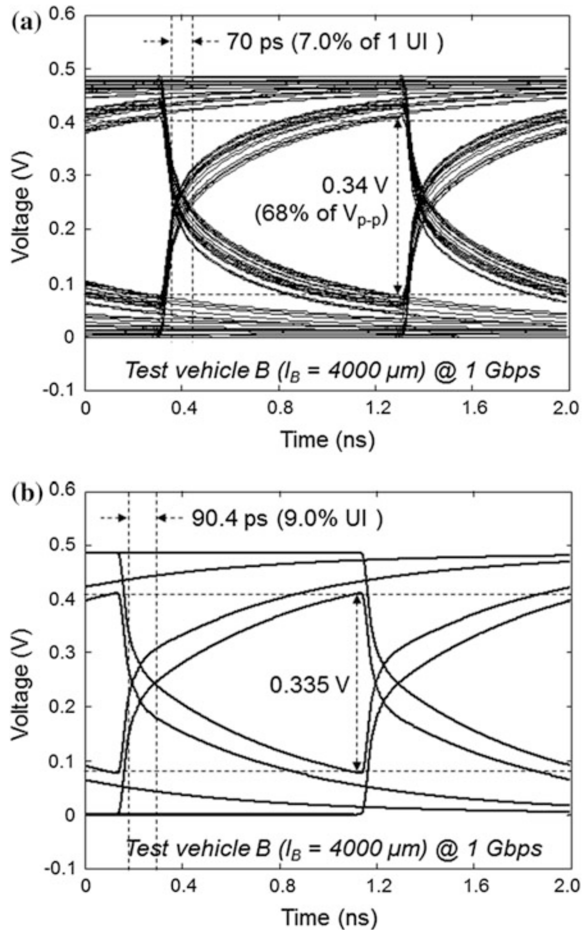


Fig. 3.42 **a** Simulated eye-diagram and **b** estimated worst-case eye-diagram of test vehicle B ($l_B = 4{,}000$ μm) at the data rate of 1 Gbps

Table 3.8 Comparison results for test vehicle B

	Full-wave and circuit-level simulators	Worst eye estimation algorithm	Comparison
Eye-opening voltage	0.317 V	0.335 V	3.6 % of V_{p-p} (Error rate)
Timing jitter	116 ps	90.4 ps	2.6 % of 1UI (Error rate)
Estimation time	9417 s	13 s	99.9 % (Improvement)

3.44, respectively. The estimated worst-case eye-diagrams show good correlation with the measured eye-diagrams. Because the loss of the cable and non-ideal properties such as random jitter are not included, the estimated worst-case eye-diagrams are of higher quality than the measured eye-diagrams.

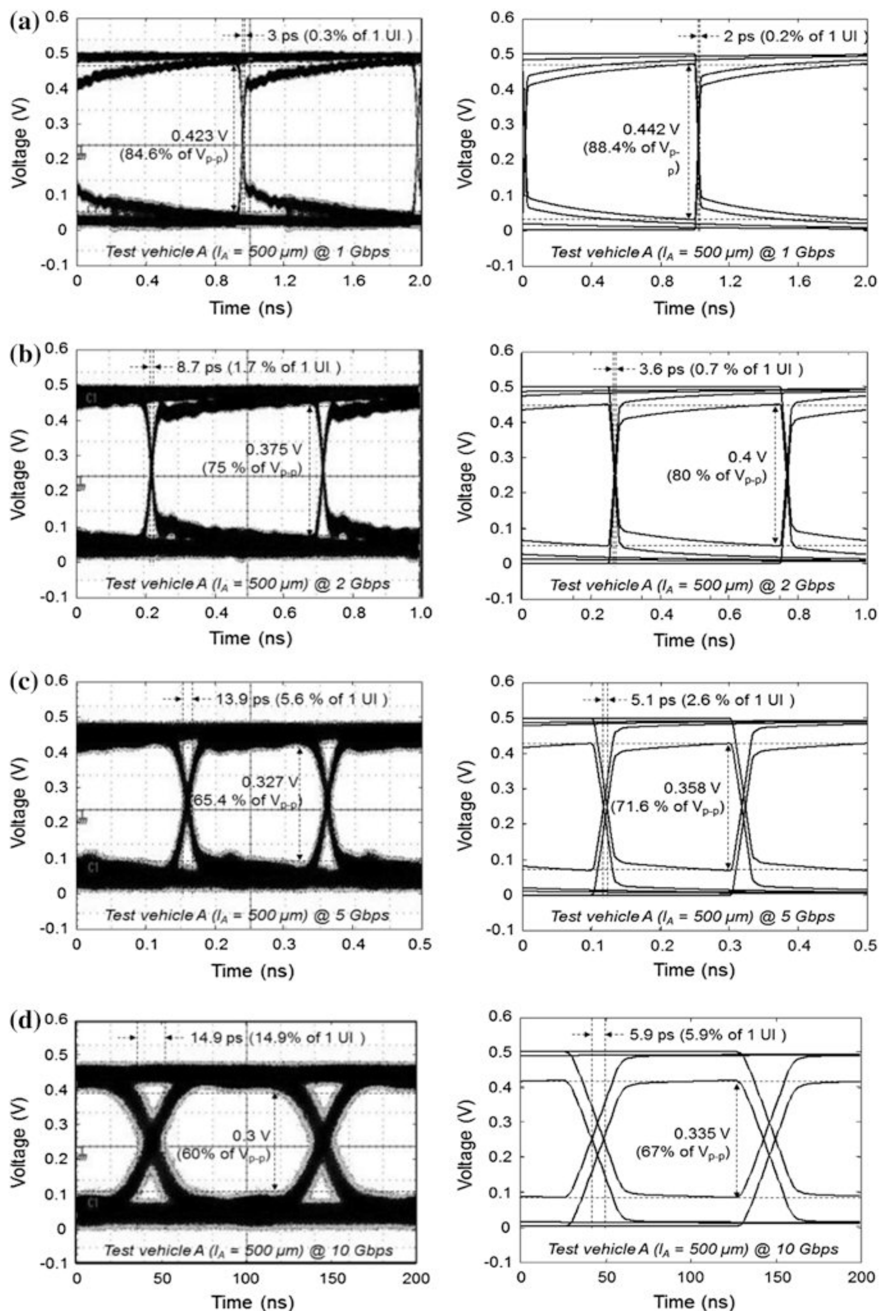


Fig. 3.43 The measured eye-diagram and estimated worst-case eye-diagram of test vehicle A at data rates of **a** 1 Gbps **b** 2 Gbps **c** 5 Gpbs and **d** 10 Gbps [15] © 2012 IMAPS

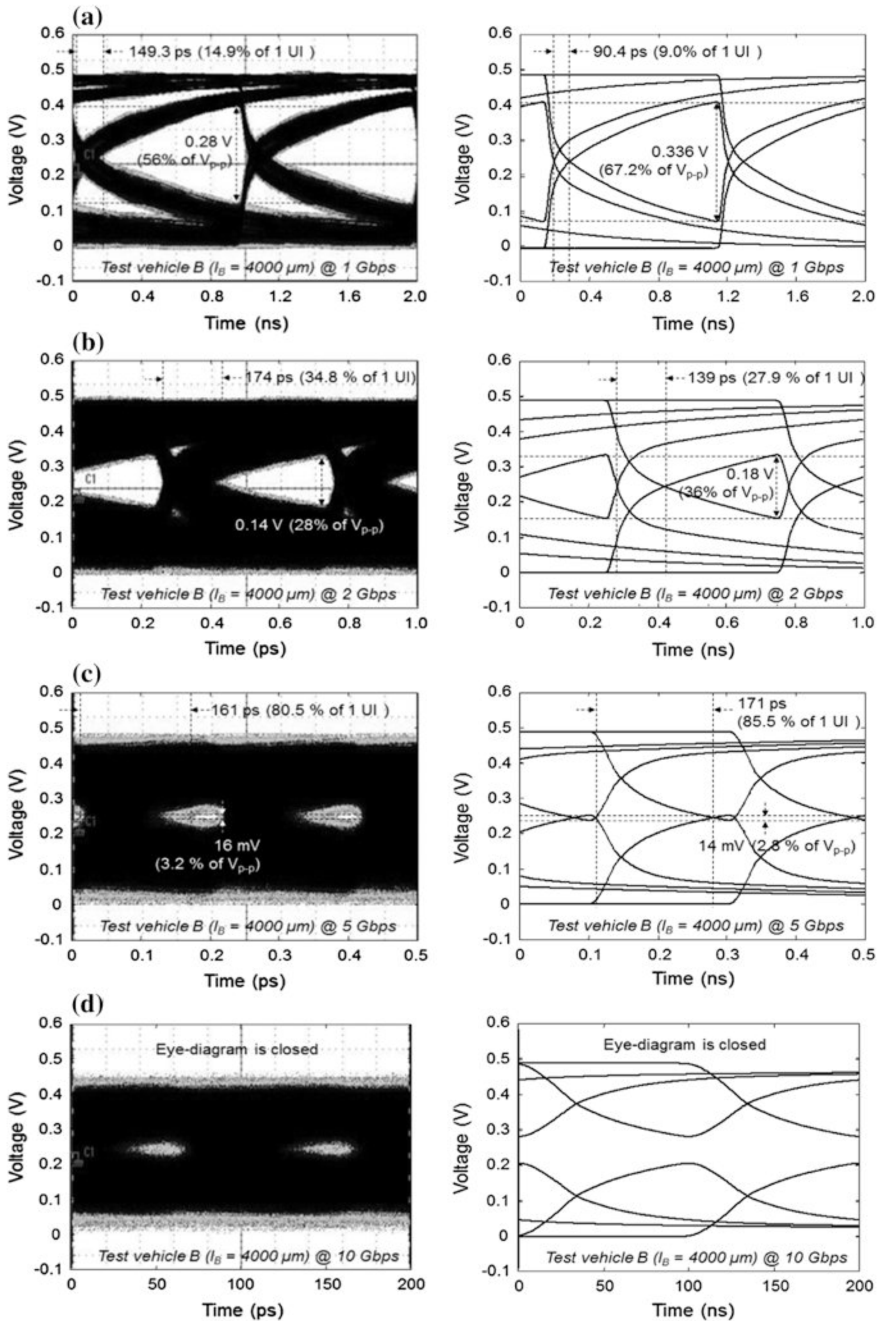


Fig. 3.44 The measured eye-diagram and estimated worst-case eye-diagram of test vehicle B at data rates of **a** 1 Gbps **b** 2 Gbps **c** 5 Gpbs and **d** 10 Gbps [15] © 2012 IMAPS

3.5 Summary

This chapter covers the modeling and analysis of the high-speed TSV-based channel that consists of TSVs and a silicon interposer interconnect. The electrical properties of the high-speed TSV channel are considerably varied depending on the channel type, structure and material of the TSV and silicon interposer interconnect. The analyses are summarized below.

- TSV
  - Channel loss of TSV is higher than that of COLV due to the impact of the lossy silicon substrate.
  - TSLV has considerable DC loss due to the direct leakage current path to the silicon substrate. The effective bandwidth of TSLV is increased by the DC attenuation, resulting in reduced rise and fall times.
  - Channel loss of TOLV is higher than that of COLV due to the higher via inductance. If the pitch between the signal and ground vias is sufficiently reduced, the channel loss of COLV can be higher than that of TSLV due to the increased capacitance.
- Silicon interposer interconnect
  - The silicon interposer interconnect with CPW type has a higher channel loss than that of a microstrip line due to the higher impact of the lossy silicon substrate.
  - The channel type with a signal on M1 has a higher channel loss than that on M2 due to the lossy silicon substrate, but it has negligible reflection.
  - The conductance of the lossy silicon substrate and the capacitance of the thin oxide layer (insulation layer) predominantly determine the loss of the high-speed TSV-based channel.
  - The silicon conductance determines the overall channel loss at mid- and high-frequency ranges.
  - The oxide capacitance determines the frequency at which the channel loss increases due to the silicon conductance.
  - The thicker thickness of the oxide layer and lower silicon conductivity lead to lower channel loss.
  - There is an optimal width of the silicon interposer interconnect that corresponds to the maximum channel bandwidth. The optimal width becomes wider in the substrate with a lower loss, such as a glass interposer.
  - Though the length of the silicon interposer interconnect is sufficiently long, the impact of the reflection is negligible because the reflected wave is considerably attenuated by the lossy silicon substrate.
- Impacts of TSV and silicon interposer interconnect on total TSV-based channel

  - In general, the impact portion of the TSV on the total TSV-based channel is negligible due to the much longer length of the silicon interposer interconnect.
  - Because the loss of the TSV is lower than that of the silicon interposer interconnect, the impact of the TSV on the loss of the TSV-based channel appears at a higher frequency than that for the silicon interposer interconnect.

- Comparison of TSV-based channel to MCM channel

  - Despite the much shorter length of the TSV-based channel, the loss of the TSV-based channel is higher than that of MCM channel up to several GHz due to the impact of the lossy silicon substrate.
  - The characteristic impedance of the TSV-based channel is frequency dependent, whereas that of the MCM channel is frequency independent.
  - The impact of the reflection is negligible in the TSV-based channel, whereas that of the MCM channel is considerable due to the lower channel loss.

In addition, the worst-case eye-diagram estimation algorithm for the high-speed TSV-based channel is introduced for efficient SI analysis. By using the algorithm, the precise worst-case eye-diagram (inner contour of the eye-diagram) of the high-speed TSV channel can be estimated within a remarkably short time.

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Chapter 4
Noise Coupling and Shielding in 3D ICs

Jonghyun Cho, Jun So Pak and Joungho Kim

Abstract This chapter explains TSV noise coupling, which is one of the significant problems in TSV-based 3DIC. TSV shows frequency-dependent noise coupling characteristics, which can be analyzed based on the TSV and silicon substrate models. The noise coupling from TSV to TSVs and transistors is severe and coupling reduction methods are essential to satisfy very tight noise tolerance budget of current high performance 3DIC; control TSV design parameters and TSV array formation, optimize TSV termination scheme, as well as design shielding structures inside TSV array using high doped guard rings, shielding TSV, shielding bump. These methods are compared by showing shielding effectiveness, design restriction, consuming area, and manufacturing process compatibility and the several design guides are provided for choosing the adequate and best way among TSV noise coupling reduction methods considering real products.

Keywords Noise coupling · TSV-TSV coupling · TSV-active circuit coupling · TSV termination · Guard-ring · Shielding TSV · Shielding bump

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4.1 Overview

Noise coupling is a significant problem in TSV-based 3D ICs. The noise coupling itself is the classical problem at high-speed electrical system and the coupling among PCB or package signal traces is well studied [1]. A noise coupling through silicon substrate is also well analyzed in previous paper [2]. However, TSV noise coupling is a new problem in 3D ICs, and the TSV I/O density is significantly increased compared with the conventional I/O density. Because the TSV noise coupling becomes much more severe, it should be analyzed, and noise coupling reduction methods should be provided.

TSV is usually formed inside doped silicon. In most cases, the TSV has an isolation layer, and it blocks direct contact between the TSV metal via and the silicon substrate. Although this isolation layer prevents noise coupling from/to TSVs at low frequency, it cannot block high-frequency noise coupling. Because of the high capacitance between the TSV metal via and the silicon substrate through the isolation layer, the TSV signal is easily coupled to the silicon substrate and vice versa at high frequency. This frequency-dependent noise coupling characteristic can be analyzed based on the TSV and silicon substrate models. The noise coupling can significantly degrade the 3D ICs performance, and coupling reduction methods are therefore essential to satisfy the very tight noise tolerance budget of a current high-performance 3D ICs.

In this chapter, we cover the modeling and the analysis of the TSV noise coupling and shielding methods. TSV noise coupling can be divided into TSV-TSV noise coupling and TSV-active noise coupling, which are covered in Sect. 4.2.1. We show the modeling and measurement results of TSV-TSV and TSV-active noise coupling. We control the TSV design parameters, and their effects are analyzed based on the TSV coupling model. In Sect. 4.2.2, the noise coupling is analyzed for the actual 3D ICs. The analysis covers the TSV termination effects and the effects of an active circuit around TSV. In Sect. 4.3., several shielding structures such as p+/DNW guard rings, shielding TSV, and shielding bumps are shown. These shielding structures are compared using the shielding effectiveness, the design restriction, the consuming area, and the manufacturing process compatibility. Several design guides are provided to choose both the adequate and best methods among all TSV noise coupling reduction methods considering the real products. Finally, we summarize and conclude this chapter in Sect. 4.4.

4.2 Analysis of Noise Coupling in 3D ICs

4.2.1 TSV Noise Coupling

In 3D ICs, noise can be coupled via several paths: TSV to TSV, TSV to substrate, or substrate to TSV. These noise coupling paths are electrically analyzed in the

frequency domain and the time domain in this chapter. In Sect. 4.2.1, TSV-to-TSV and TSV-to-substrate noise coupling are analyzed, whereas the actual noise coupling analysis is shown in Sect. 4.2.2. The actual 3D ICs with I/O termination shows very different coupling results compared with the 50 Ω termination. The importance of the noise coupling analysis is also shown in the actual 3D ICs.

TSV noise coupling can be classified as TSV-TSV coupling and TSV-active-circuit coupling. In this subsection, these 2 types of TSV noise coupling are modeled and analyzed based on the simulations and measurements. The simulations are performed with several physical parameters: the TSV insulation layer thickness, the TSV height, and the distance between the victim and the aggressor. These effects are analyzed based on the equivalent TSV noise coupling circuit model.

4.2.1.1 TSV-TSV Noise Coupling

There are many TSVs in 3D ICs, and TSV-TSV noise coupling is a very significant problem. The conceptual view for TSV-TSV noise coupling is depicted in Fig. 4.1. In the figure, the TSV signal rises and falls through the metal via, and it is electrically affected by the nearby aggressor TSV signal. To analyze the TSV-TSV noise coupling, the most basic structure with two signal TSVs and two ground TSVs are assumed. In the structure, two ground TSVs are connected by a ground line, i.e., they have common ground. The structure and the notations of the physical dimensions are depicted in Fig. 4.2.

We previously modeled the TSV channel as an RLGC equivalent circuit model in Chap. 2. TSV-TSV noise coupling can also be modeled as an RLGC equivalent circuit based on the same physical meaning that was shown in Chap. 2. The single-TSV capacitance and resistance values are obtained using the following equations.

$$C_{TSV} = \varepsilon_{ox_{TSV}} \times \frac{2\pi h_{TSV}}{\ln\left(\frac{r_{TSV}+t_{ox_{TSV}}}{r_{TSV}}\right)}\ [\mathrm{F}] \tag{4.1}$$

$$R_{TSV} = \frac{1}{\sigma_{TSV}} \times \sqrt{\left(\frac{h_{sub}}{\pi r_{TSV^2}}\right)^2 + \left(\frac{h_{sub}}{\pi\left(r_{TSV^2} - \left(r_{TSV} - \delta_{skin_{depth}}\right)^2\right)}\right)^2}\ [\Omega] \tag{4.2}$$

$$R_{TSV} = \frac{1}{\sigma_{TSV}} \times \sqrt{\left(\frac{h_{sub}}{\pi r_{TSV^2}}\right)^2 + \left(\frac{h_{sub}}{\pi\left(r_{TSV^2} - \left(r_{TSV} - \delta_{skin_{depth}}\right)^2\right)}\right)^2}$$

$$\delta_{skin_{depth}} = \frac{1}{\sqrt{\pi f \mu \sigma_{TSV}}}\ [\mathrm{m}] \tag{4.3}$$

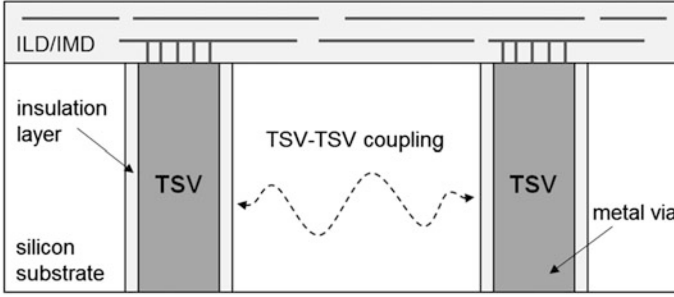


Fig. 4.1 The conceptual figure of TSV-to-TSV noise coupling

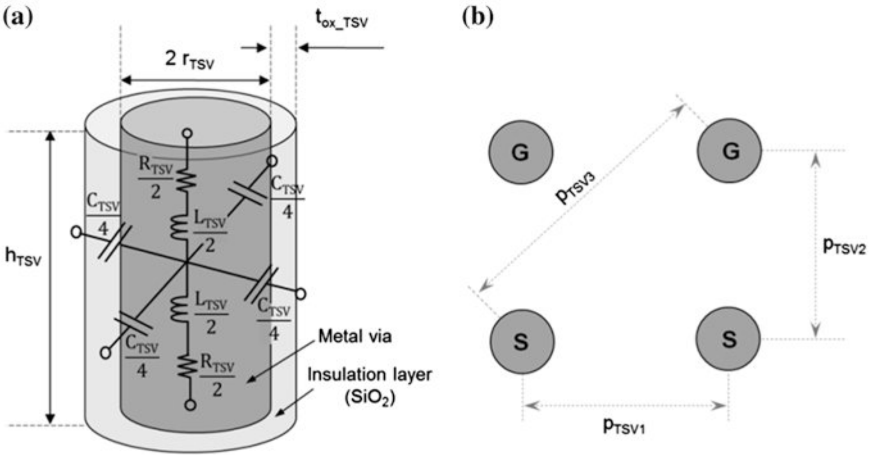


Fig. 4.2 The basic TSV-TSV coupling structure and notations for each physical dimension for **a** Single TSV and **b** TSV-TSV coupling structure with 2 signal and 2 ground TSVs

For the TSV inductance, we should consider both the self-inductance and the mutual inductance. The TSV inductance can be calculated as the sum of these inductances. Because there are four TSVs, the mutual inductance should be considered among one signal TSV and the other three TSVs. The self-inductance and the mutual inductance are calculated using the following equations [3, 4].

$$\mathrm{L}_{TSV_self} = \frac{\mu h_{TSV}}{4\pi} \times \left[\ln\left(\left(\frac{h_{TSV}}{r_{TSV}}\right) + \sqrt{\left(\frac{h_{TSV}}{r_{TSV}}\right)^2 + 1} \right) + \frac{r_{TSV}}{h_{TSV}} - \sqrt{\left(\frac{r_{TSV}}{h_{TSV}}\right)^2 + 1} \right] \ [\mathrm{H}] \tag{4.4}$$

$$\mathrm{L}_{TSV_mutual} = \frac{\mu h_{TSV}}{4\pi} \times \left[\ln\left(\left(\frac{h_{TSV}}{p_{TSV}} \right) + \sqrt{\left(\frac{h_{TSV}}{p_{TSV}} \right)^2 + 1} \right) + \frac{p_{TSV}}{h_{TSV}} - \sqrt{\left(\frac{p_{TSV}}{h_{TSV}} \right)^2 + 1} \right] \text{ [H]} \tag{4.5}$$

For the resistance and the capacitance among the TSVs, the following equations can be used. Unlike the TSV channel, these resistance and capacitance should be considered among one TSV and the other TSVs, except that between two ground TSVs. Two ground TSVs are connected via a metal line, and the resistance or the capacitance among these ground TSVs can be neglected. Hence, five resistance values and five capacitance values should be included in the TSV-TSV equivalent circuit model for the structure with 2 signal TSVs and 2 ground TSVs as shown in Fig. 4.2.

$$\mathrm{R}_{si_sub} = \frac{1}{\pi \sigma_{Si} h_{TSV}} \times \cosh^{-1}\left(\frac{p_{TSV}}{2 \cdot r_{TSV}} \right) \ [\Omega] \tag{4.6}$$

$$\mathrm{C}_{si_sub} = \frac{\pi \times \varepsilon_{Si}}{\cosh^{-1}\left(\frac{p_{TSV}}{2 \cdot r_{TSV}} \right)} \times h_{TSV} \ [\mathrm{F}] \tag{4.7}$$

To verify the TSV-TSV noise coupling model, the test vehicles in Fig. 4.3 were fabricated using the Hynix via-last TSV process [5]. Figure 4.3a shows a top view of the TSV-TSV coupling test vehicle, and Fig. 4.3b shows a cross-sectional view of the test vehicle scanning electron microscope (SEM) image. During the TSV manufacturing process, the top of the TSV is caved in, as illustrated in Fig. 4.3a, which prevents direct probing on the TSV, and the Re-distribution layer (RDL) line is used for the probing pad. The TSV has no interconnection on the bottom side, and the test vehicle is placed on an insulator to isolate the conductive silicon substrate from the environment. For the insulator, styrofoam with a dielectric constant of 1.02 is used, and its effects can be neglected because of its low dielectric constant. For the frequency domain, a vector network analyzer (VNA) is used to measure the two-port s-parameter from 10 MHz to 20 GHz. The TSV radius, r_{TSV}, is 16.5 μm, TSV oxide thickness, t_{ox_TSV}, is 0.5 μm, TSV height, h_{sub}, is 100 μm, and silicon substrate doping conductivity, σ_{sub}, is 10 S/m. The detailed physical dimensions and the material properties of the test vehicle are listed in Table 4.1.

The equivalent circuit model for the TSV-TSV coupling structure in Fig. 4.3 is illustrated in Fig. 4.4a. Because the bottom side of the TSV is open, the inductive coupling due to the mutual inductance among the TSVs is small and negligible in Fig. 4.4a. The TSV resistance has a very limited role in TSV-TSV noise coupling and is also neglected in the equivalent circuit model.

Furthermore, the test vehicle is manufactured using a via-last process; the RDL effects are significant and cannot be neglected. Thus, the RDL capacitance is

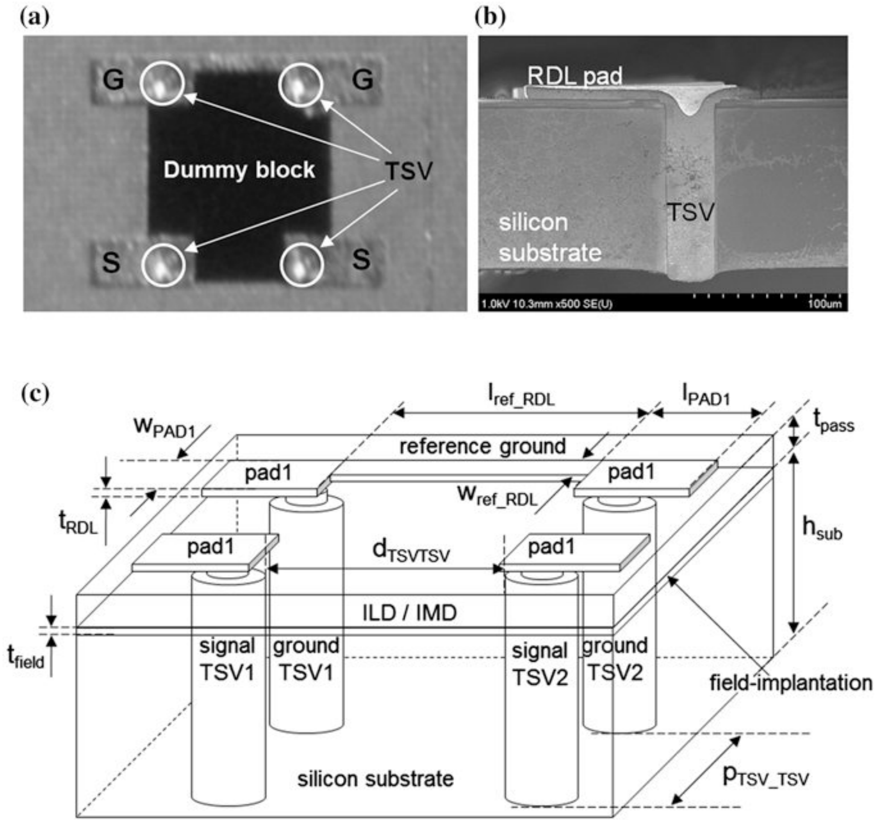


Fig. 4.3 The TSV-TSV noise coupling test structure: **a** top view of the structure optical image, **b** side view of the structure of SEM image, and **c** conceptual view and test structure physical parameters [5] © 2011 IEEE

Table 4.1 The physical dimension and material property of the test vehicle

Component	Value (μm)	Component	Value	Component	Value
r_{TSV}	16.5	l_{ref_RDL}	95 μm	l_{PAD1}	140 μm
t_{ox_TSV}	0.52	w_{ref_RDL}	20 μm	w_{PAD1}	65 μm
h_{sub}	100	t_{RDL}	9 μm	p_{TSV_TSV}	250 μm
t_{field}	0.25			d_{TSV_TSV}	130 μm
t_{pass}	5.7	σ_{sub}	10 S/m		
–	–	σ_{field}	1500 S/m	$\varepsilon_{r,sub}$	11.9
–	–	σ_{copper}	5.8×10^7 S/m	$\varepsilon_{r,ILD/IMD} = \varepsilon_{r,passivation}$	4.1

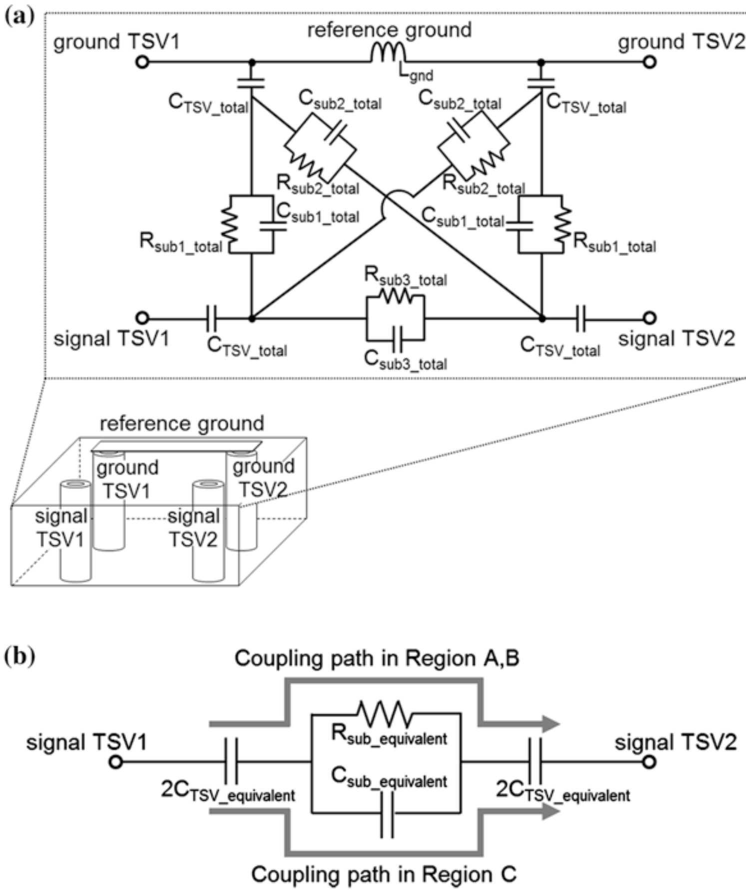


Fig. 4.4 The equivalent circuit model for TSV-TSV noise coupling with two signal TSVs and two ground TSVs. **a** The TSV-TSV structure and its equivalent circuit model with a physical meaning for each lumped parameter; **b** a more simplified model of the circuit in (**a**) [5] © 2011 IEEE

added to the TSV capacitance, and the total capacitance is labeled as C_{TSV_total} in Fig. 4.4a. The lumped circuit model in Fig. 4.4a can be further simplified into the total equivalent circuit model in Fig. 4.4b, which contains only three elements: the total equivalent TSV capacitance, substrate resistance, and substrate capacitance. The measured and modeled s-parameters for the TSV-TSV coupling structure are illustrated in Fig. 4.5. We conclude that the TSV model verification based on the measurement is valid. The TSV-TSV coupling displays a frequency-dependent noise transfer function and is divided into three frequency behavior regions A, B, and C, as illustrated in Fig. 4.5. To analyze the measurements, the total equivalent circuit model in Fig. 4.4b is used with the model values in Fig. 4.5.

In Region A, the impedance of the total equivalent TSV capacitance, $Z(C_{TSV_equivalent})$, is much larger than both the impedance of the total equivalent

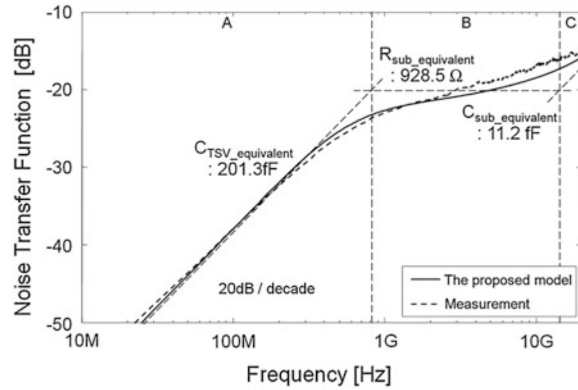


Fig. 4.5 The measured and modeled noise transfer functions for the TSV-TSV noise coupling structure with the dimensions in Table 4.1 [5] © 2011 IEEE

substrate capacitance, $Z\ (C_{sub_equivalent})$, and the impedance of the total equivalent substrate resistance, $Z\ (R_{sub_equivalent})$, whereas $Z\ (R_{sub_equivalent})$ is smaller than $Z\ (C_{sub_equivalent})$. If we consider only the major contributing elements, $C_{TSV_equivalent}$ determines the noise transfer function in Region A. Thus, as the frequency increases, $Z\ (C_{TSV_equivalent})$ decreases, and the noise transfer function increases. In Region B, $Z\ (R_{sub_equivalent})$ becomes larger than $Z\ (C_{TSV_equivalent})$ but is smaller than $Z\ (C_{sub_equivalent})$, and the noise transfer function is determined by $R_{sub_equivalent}$. Although the frequency increases, $Z\ (R_{sub_equivalent})$ remains constant, which results in a constant noise transfer function that is independent of the frequency, as illustrated in Fig. 4.4. In Region C, $Z\ (R_{sub_equivalent})$ remains larger than $Z\ (C_{TSV_equivalent})$, which is similar to Region B, but it also becomes larger than $Z\ (C_{sub_equivalent})$. Therefore, the noise transfer function is determined by $C_{sub_equivalent}$, which increases the noise transfer function when the frequency increases.

When the TSV-TSV coupling structure is terminated at both the top and the bottom sides, a similar analysis can be applied, but the inductance effects can no longer be neglected. For the analysis, the TSV-TSV noise coupling is simulated using a 3D-EM solver. In this simulation, the simulation values are chosen to have the recently used TSV dimensions instead of the previous dimension used for the test sample: the TSV radius is 5 μm the oxide thickness is 0.5 μm, the height is 100 μm, and the TSV pitch is 40 μm. The simulation is performed by terminating both the top and the bottom of the TSVs with 50-ohm resistance: the 4-port simulation is performed. The near-end crosstalk (NEXT) and far-end crosstalk (FEXT) results are compared with the 2-port simulation result with the same physical dimensions (the TSV bottom is opened as in the previous measurement case).

The noise transfer functions are compared in Fig. 4.6. Because of the open-termination at the bottom of the TSVs, the noise coupling increases by approximately 10 dB at all frequency ranges compared to the TSV bottom-termination case (4-port simulation). For the NEXT and FEXT, there are some differences both at low and high frequencies. At low frequency, NEXT shows a slightly higher noise transfer function than FEXT because of TSV resistance. At high frequency,

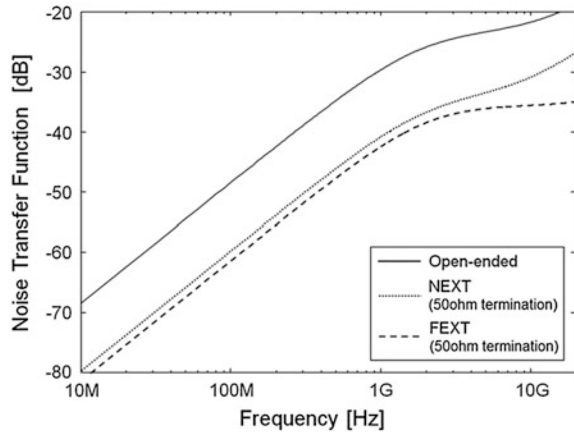


Fig. 4.6 The noise transfer function comparison for the TSV-TSV coupling structure with variation in the observing point and termination

NEXT increases as frequency increase while FEXT is almost constant as frequency increases because mutual inductance greatly affects at FEXT at high frequency.

The TSV noise coupling analysis can be performed using the total equivalent circuit model in Fig. 4.4b. There are several NEXT graphs for the TSV-TSV coupling structure in Fig. 4.7, which are obtained from the 3D-EM simulation with several parameter variations.

If t_{ox_TSV} increases, $C_{TSV_equivalent}$ decreases and $R_{sub_equivalent}$ and $C_{sub_equivalent}$ remain constant; hence, the overall noise transfer function decreases in Region A, whereas it remains nearly constant in Regions B and C, as shown in Fig. 4.7a. Thus, t_{ox_TSV} determines only the low-frequency noise-coupling behavior; it has little effect on the noise coupling suppression at high frequencies above several GHz. Moreover, increasing t_{ox_TSV} requires a significant amount of time and cost for TSV manufacturing. If d_{TSV_TSV} increases, $R_{sub_equivalent}$ increases and $C_{sub_equivalent}$ decreases. Thus, the noise transfer function decreases in Regions B and C, whereas the noise transfer function remains constant in Region A, as shown in Fig. 4.7b. Increasing the coupling distance yields a good noise coupling suppression effect from several hundred MHz to 20 GHz, which is the frequency range of interest for coupling. Although this is a good solution to suppress noise coupling, it consumes a large area and cannot be applied for dense TSV routing. If h_{sub} increases, $C_{TSV_equivalent}$ increases, $R_{sub_equivalent}$ decreases, and $C_{sub_equivalent}$ increases, which increase the noise transfer function in all regions A, B, and C, as shown in Fig. 4.7c. Decreasing the substrate height provides a good noise coupling suppression effect for the TSV-TSV coupling, but it is very difficult to decrease the substrate height under several tens of μm because of wafer-handling issues [6].

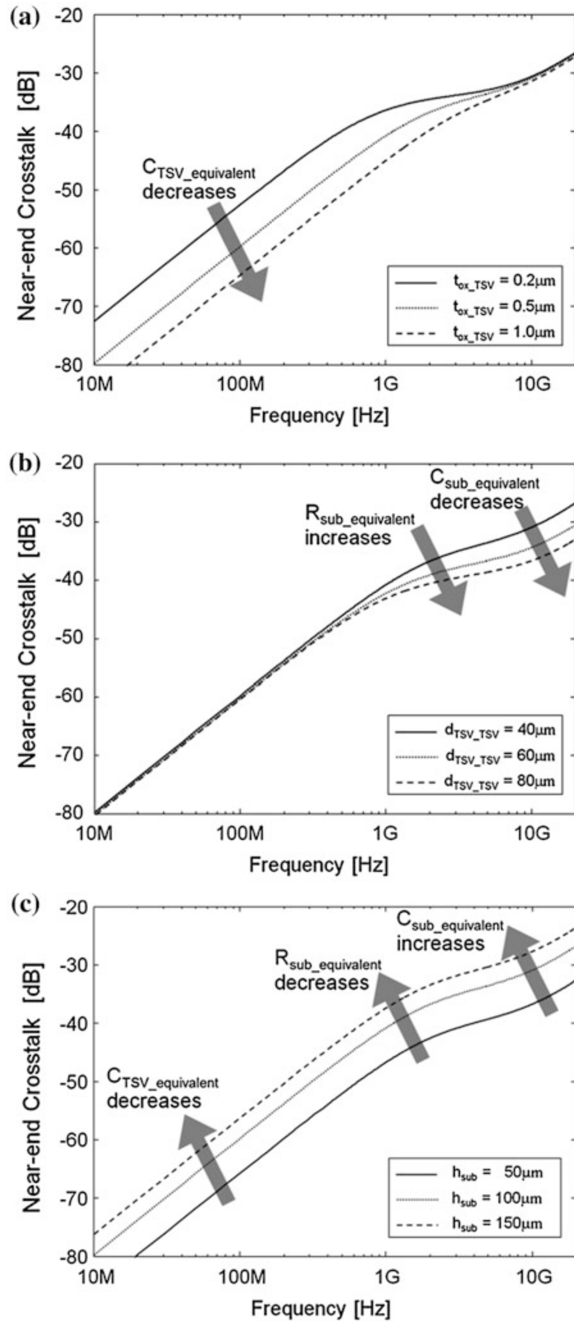


Fig. 4.7 The noise transfer function (S_{21}) for the TSV-TSV coupling structure with several parameter variations: **a** TSV insulation layer thickness variation, **b** TSV-TSV distance variation, and **c** TSV height variation. The default structure has a TSV radius of 5 μm, a height of 100 μm, a TSV oxide thickness of 0.5 μm, and a pitch of 40 μm among the TSVs

4.2.1.2 TSV-Substrate (Active Circuit) Noise Coupling

For 3D ICs, several silicon chips are stacked by TSVs, and there are many MOSs in each silicon chip. Thus, the noise coupling between the signal TSV and the active circuit can be a great problem and must be analyzed. The conceptual view of the TSV-active circuit noise coupling is illustrated in Fig. 4.8. In an actual 3D ICs, there are many active circuits, the TSV-active circuit noise coupling is almost impossible to analyze because of its great complexity, and a substrate contact is used instead of an active circuit. The P+ contact in a p-type silicon substrate can be represented as an active circuit, and the noise coupling between the TSV and the contact can be represented as the coupling between the TSV and the active circuit.

The TSV-contact noise coupling test samples are designed as illustrated in Fig. 4.9. The test sample was fabricated using the Hynix via-last TSV process like the TSV-TSV noise coupling test sample in Fig. 4.3. Figure 4.9a shows a top view of the TSV-contact coupling test vehicle, and Fig. 4.9b shows a cross-sectional view of the test vehicle SEM image. Similar to the TSV-TSV test sample, the RDL line is used for the probing pad. There is no ground TSV, and only a ground RDL line is used as the reference. The sample is placed on an insulator, and a 2-port probing measurement was performed. The material property and the physical dimensions are identical to that in Table 4.1, and some missing physical dimensions in Table 4.1 are listed in Table 4.2.

The equivalent circuit model for the TSV-contact coupling structure is illustrated in Fig. 4.10a. Here, the TSV inductance and its resistance are neglected (similar to the TSV-TSV coupling test sample), and the RDL capacitance is included in C_{TSV_total} (similar to the TSV-TSV case). For TSV-TSV coupling, we proposed several equations to calculate each value in the model. However, it is not easy to obtain substrate resistance and capacitance values using equations and 3-dimensional transmission line matrix method (3D-TLM) is used [7]. By the help of 3D-TLM, we obtain each lumped circuit value in Fig. 4.10a. The lumped circuit model in Fig. 4.10a can be further simplified into the total equivalent circuit model in Fig. 4.10b, which contains only three elements: the total equivalent TSV capacitance, the substrate resistance, and the substrate capacitance.

The measured and the modeled s-parameters for the TSV-contact coupling structure are illustrated in Fig. 4.11. We conclude that the TSV model verification based on the measurement is valid. The TSV-TSV coupling displays a frequency-dependent noise transfer function and is divided into three frequency behavior regions, A, B, and C, as illustrated in Fig. 4.11. To analyze the measurements, the total equivalent circuit model in Fig. 4.10b is used with the R and C values in Fig. 4.11.

The TSV-contract noise coupling mechanism is almost identical to the mechanism in the TSV-TSV case. In Region A, the total equivalent TSV capacitance, $C_{TSV_equivalent}$, determines the entire noise coupling, and the noise transfer function increases as the frequency increases. In this region, much more noise is coupled than in the TSV-TSV case because there is only one TSV at the TSV-contact test structure and $C_{TSV_equivalent}$ is almost four times larger than that of the TSV-TSV

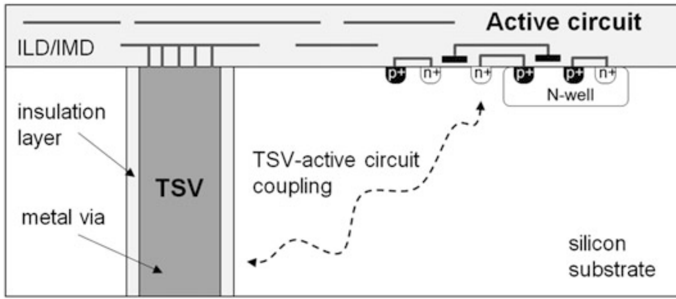


Fig. 4.8 The conceptual figure of the TSV-Substrate (active circuit) noise coupling

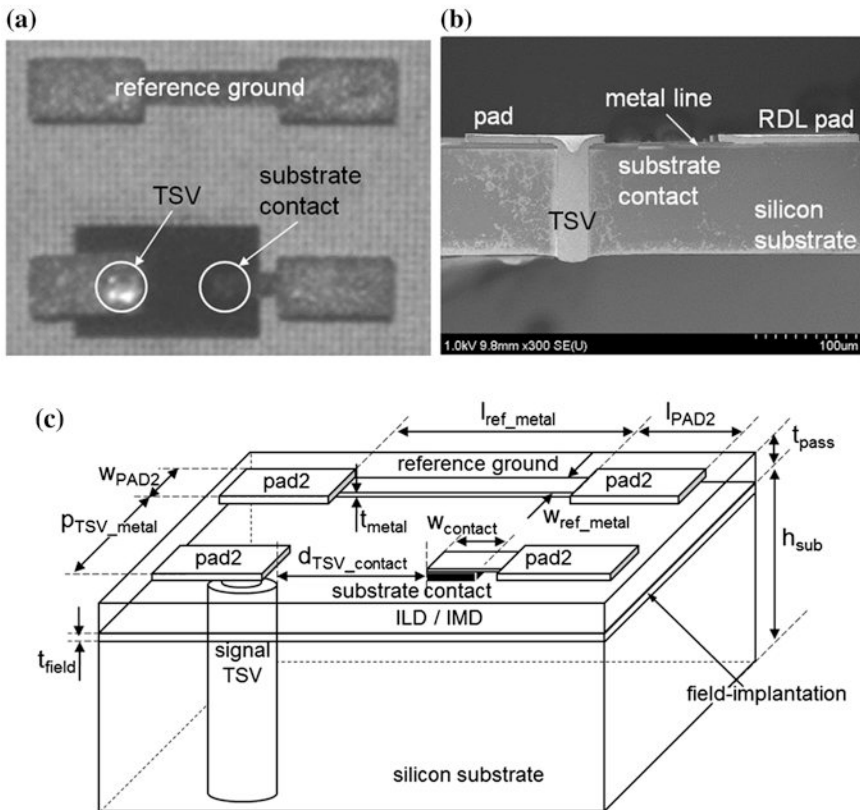


Fig. 4.9 The TSV-contact noise coupling test structure. **a** *Top view* of the structure optical image, **b** *side view* of the structure of the SEM image, and **c** *conceptual view* and the test structure physical parameters [5] © 2011 IEEE

Table 4.2 The physical dimensions of the TSV-contact coupling test vehicle

Component	Value (μm)	Component	Value (μm)	Component	Value
$t_{contact}$	0.25	l_{ref_metal}	160	p_{TSV_metal}	250 μm
l_{PAD2}	140	w_{ref_metal}	40	$d_{TSV_contact}$	100 μm
w_{PAD2}	80	t_{metal}	0.8	$\sigma_{contact}$	10^5 S/m
$w_{contact}$	30	–	–	–	–

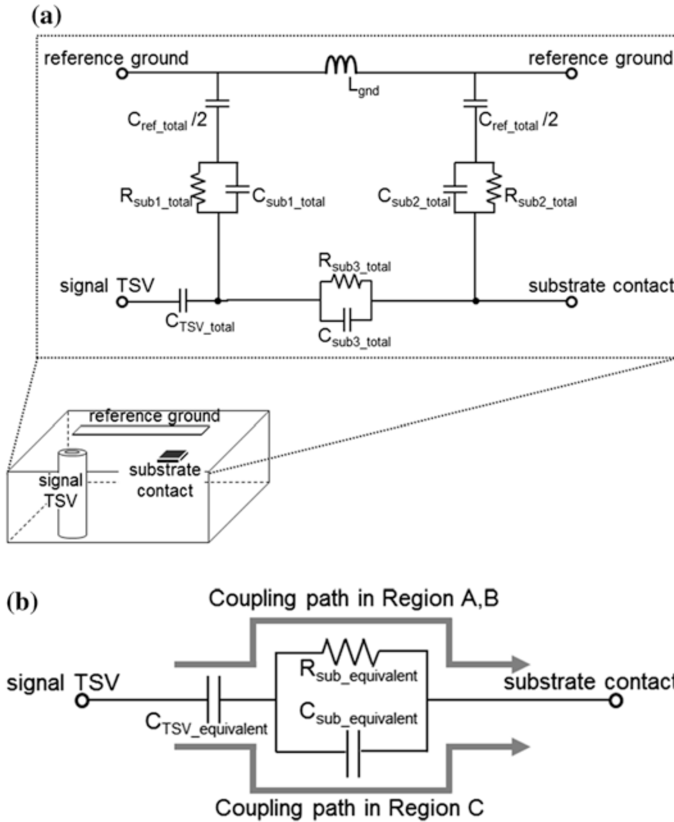


Fig. 4.10 The equivalent circuit model for the TSV-contact noise coupling with two signal TSVs and two ground TSVs. **a** TSV-TSV structure and its equivalent circuit model with physical meaning for each lumped parameter; **b** a more simplified model of the circuit in (**a**) [5] © 2011 IEEE

coupling structure. In Region B, $R_{sub_equivalent}$ is the dominant factor, whereas $C_{sub_equivalent}$ is the dominant factor in Region C. The noise transfer function remains almost constant in Region B and increases again as the frequency increases in Region C.

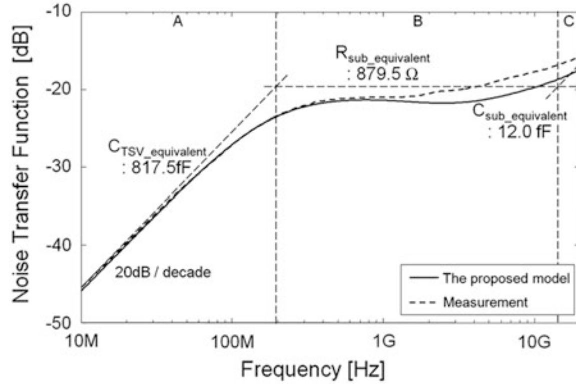


Fig. 4.11 The measured and the modeled noise transfer functions of the TSV-TSV noise coupling structure with the dimensions in Tables 4.1 and 4.2 [5] © 2011 IEEE

The TSV-contact noise coupling analysis is performed using the total equivalent circuit model in Fig. 4.10b. There are several NEXT graphs for the TSV-contact coupling structure in Fig. 4.12, which are obtained using the 3D-EM simulation with several parameter variations. The TSV-contact noise coupling analysis is performed using the total equivalent circuit model in Fig. 4.10b. There are several

NEXT graphs for the TSV-contact coupling structure in Fig. 4.12, which are obtained using the 3D-EM simulation with several parameter variations. The simulation structure is identical to the test sample structure in Fig. 4.9, and the physical dimensions are identical to the previous TSV-TSV simulation: the TSV radius is 5 μm, the TSV height is 100 μm, the contact size is 10 μm × 10 μm, and the TSV oxide thickness is 0.5 μm. When the TSV oxide thickness changes, only the low-frequency noise coupling changes as shown in Fig. 4.12a. When the TSV-contact distance changes, the mid- and high- frequency noise couplings change as shown in Fig. 4.12b. When the TSV height changes, the behavior is different from the TSV-TSV coupling case. In Fig. 4.12c, when the substrate height increases, low-frequency noise coupling increases, but it saturates at some value at mid and high frequencies. Because the TSV is a vertical structure, whereas the contact is a planar structure, the effects of the lower side of the TSV on the contact are limited, and noise coupling no longer increases when the TSV height increases above some value. When the TSV height increases, $C_{TSV_equivalent}$ increases, but $R_{sub_equivalent}$ and $C_{sub_equivalent}$ saturate at some values.

4.2.2 Noise Coupling Analysis in an Actual 3D ICs

In this subsection, TSV noise coupling is analyzed for the actual 3D ICs. In the previous sections, the TSV noise coupling is analyzed based on the assumption that all TSVs are terminated with 50 Ω and there is no other structure except the TSV coupling structure. However, TSVs are usually terminated with I/O drivers,

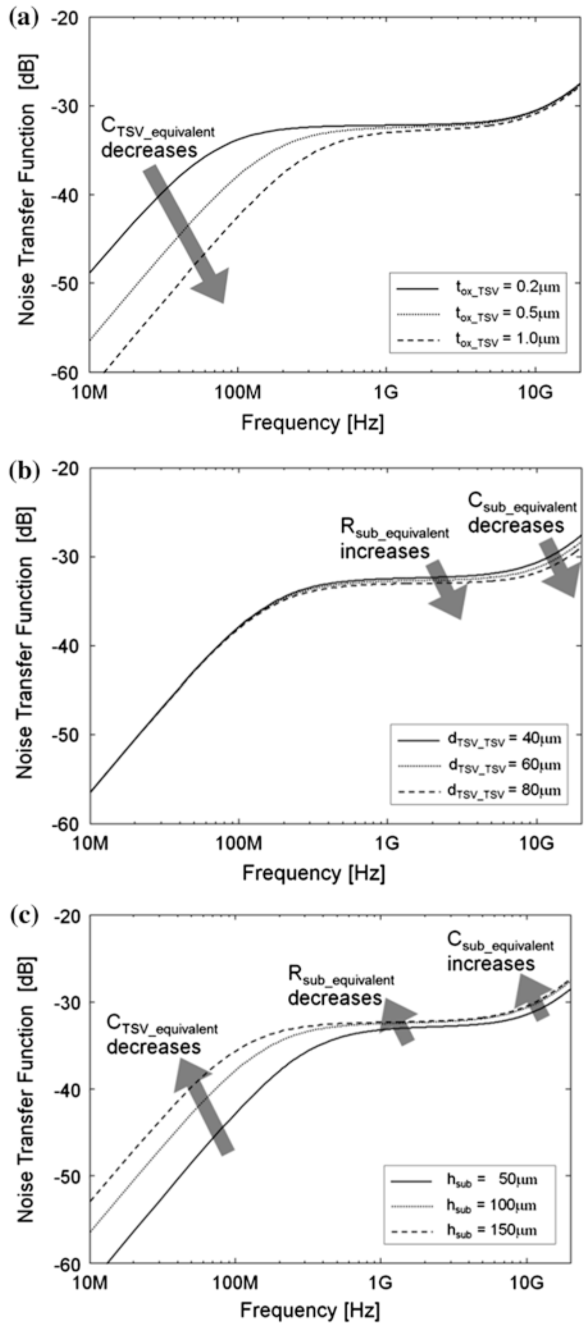


Fig. 4.12 The noise transfer function (S_{21}) for the TSV-contact coupling structure with several parameter variations: **a** TSV insulation layer thickness variation, **b** TSV-contact distance variation, and **c** TSV height variation

and there are several active circuits around the signal and ground TSVs in an actual 3D ICs. These differences significantly affect the TSV noise coupling and will be analyzed in the following subsections.

4.2.2.1 TSV Termination Effects

In an actual 3D ICs, TSVs are usually terminated by the I/O drivers, and the TSV I/O terminations should be considered because they significantly affect the TSV coupled noise voltage [8]. A typical coupled TSV channel with I/O drivers is illustrated in Fig. 4.13a. For the analysis, this conceptual figure can be modeled with some impedances (Z1 to Z5) as illustrated in Fig. 4.13b.

In Fig. 4.13b, Z1, Z2, Z3, and Z4 are the I/O termination impedances of the TSV channel, and Z5 is the impedance between the coupled TSV channels. The TSV resistance and inductance are neglected here because these effects are negligible as shown in the previous section. So, ports 1 and 2 and ports 3 and 4 are shorted in Fig. 4.13b. Based on the basic circuit theory, we can derive the coupled voltage at V_2 when V_{in} is injected. For convenience in the following equation, we define Z_{victim} as the victim I/O impedance observed at the aggressor as written in 4.8, and V_1 and V_2 are calculated using the following equations.

$$Z_{victim} = Z_3//Z_4 = \frac{Z_3 \times Z_4}{Z_3 + Z_4}\ [\Omega] \tag{4.8}$$

$$V_1 = V_{in} \times \frac{\left(Z_2//(Z_5 + Z_{victim})\right)}{Z_1 + \left(Z_2//(Z_5 + Z_{victim})\right)}\ [\mathrm{V}] \tag{4.9}$$

$$V_2 = V_1 \times \frac{Z_{victim}}{Z_5 + Z_{victim}}\ [\mathrm{V}] \tag{4.10}$$

The I/O drivers can be simply modeled as a resistor for the input driver and a capacitor for the output driver. The input driver resistor represents the MOS channel resistance while the output driver capacitor represents the MOS gate capacitance. If we use an inverter as the I/O termination instead of 50-ohm resistor, Z2 and Z4 (the impedance of output driver capacitance) has much larger value than Z1 or Z3 (the impedance of input driver resistance) up to several GHz. In addition, Z5 is usually much larger than Z1 or Z3 because Z5 is several hundred ohms to several kiloohms depending on the TSV dimensions and the interested frequency while Z1 or Z3 has scores of ohms to a few hundred ohms. Because both Z2 and Z5 are larger than Z1, V_1 is almost equal to V_{in} at the most interested frequency regarding to 4.9, and the coupled voltage, V_2, is determined by the value of Z5 and Z_{victim} as written in 4.10: the coupling noise increases when Z_{victim} increases.

Figure 4.14 shows the coupling noise voltage depending on the TSV I/O termination impedance. For the simple TSV coupling structure with two signal TSVs and two ground TSVs, the TSV coupling noise is estimated with the variation of

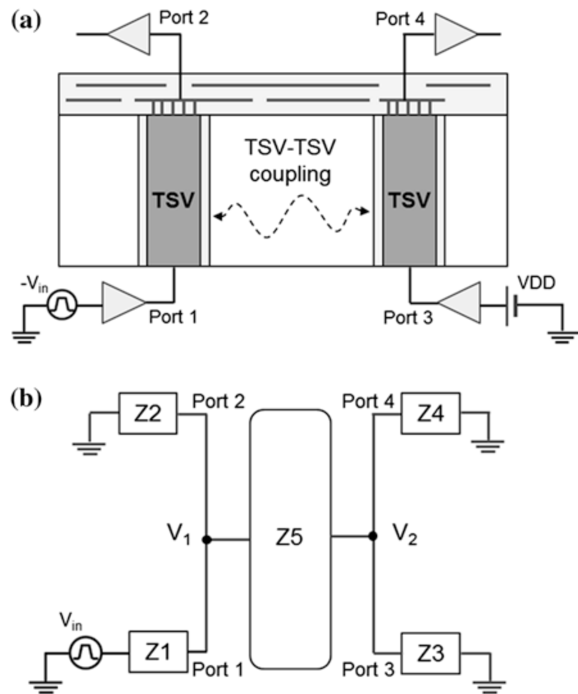


Fig. 4.13 TSV-TSV coupling structure with I/O terminations **a** The conceptual view and **b** simple schematic view with impedance from Z1 to Z5, where TSV resistance and inductance are neglected

the input resistance from 50 to 1,000 Ω. The TSV output is assumed to be terminated with a 10 fF buffer, when the TSV diameter is 10 μm, the TSV pitch is 40 μm, the TSV dioxide thickness is 0.5 μm, and the TSV height is 50 μm. A rectangular wave switching between 0 and 1.8 V with 1 GHz frequency is used as the voltage source, V_{in}. The results show that the coupling noise increases when the TSV input resistance increases. The peak-to-peak coupling noise increases from 26.1 to 158.1 mV when the source resistance changes from 50 to 1,000 Ω. This result implies that the coupling noise increases when the input driver size decreases because the buffer input resistance increases when the input driver size decreases. When the input driver size increases, input resistance decreases (Z1 and Z3 decrease), whereas output capacitance increases (Z2 and Z4 decrease) when the output driver size increases. Hence, the increase of the driver size decreases Z_{victim}, which makes the coupling noise, V_2, also decrease. The TSV I/O buffer size significantly affects the TSV noise coupling and should be increased to decrease the TSV noise coupling voltage. However, increasing buffer size requires increased chip area and cannot be applied to all TSV I/O drivers, but it should be considered and can be applied to some cases.

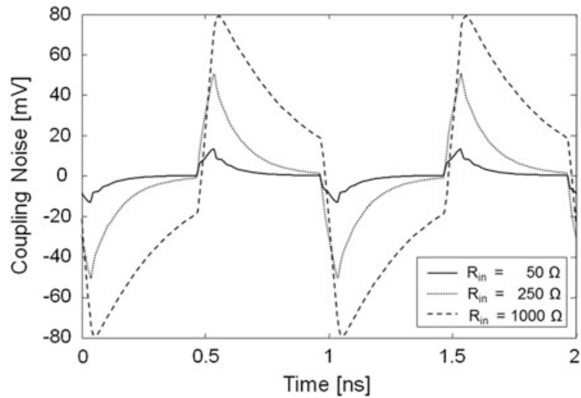


Fig. 4.14 The time-domain noise waveform for several resistance values

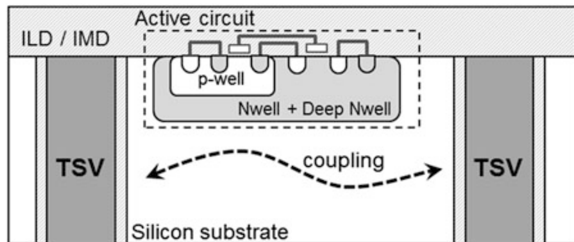


Fig. 4.15 The conceptual view of the TSV-TSV noise coupling with active circuits near the TSVs. [11] © 2011 IEEE

4.2.2.2 The Effects of an Active Circuit Around the TSVs

Noise coupling among TSVs can be divided into 2 types regarding the existence of nearby active circuits. Some silicon interposer does not contain active circuits (passive interposer); it uses only TSV and metal interconnections, which significantly reduces the cost [9]. However, for the on-chip TSV cases, the silicon substrate contains not only TSV and metal interconnections but also active circuits. The noise coupling among TSVs strongly depends on the existence of the nearby active circuits. For the current technology node, a double- or triple-well structure is widely used for active circuit to isolate the analog/RF circuits from the digital circuits [10], as illustrated in Fig. 4.15 [11].

For the reliable performance of the active circuit around the TSV, a keep-out zone from the TSV is necessary [12]. And for the active circuit, it can be simplified to deep n-well (DNW) because it is usually used for an active circuit. For the analysis of active circuit effects on TSV noise coupling, we place the DNWs surrounding the TSVs with a keep-out zone included. The test structure is illustrated in Fig. 4.16, where 2 signal TSVs, 2 ground TSVs, and DNW are used. Furthermore, we considered the depletion region, which is generated at the boundary between the DNW and the p-type silicon substrate.

The DNW should be biased with power to prevent a latch-up, and the impedance between the power and the ground is usually very small for well-

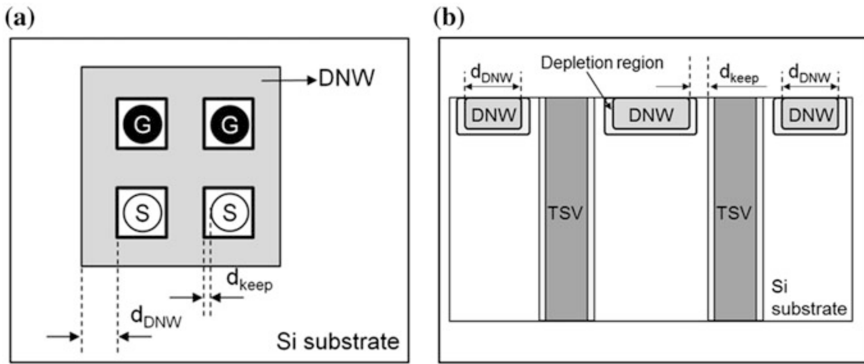


Fig. 4.16 The *top view* of the TSV-TSV noise coupling structure with deep n-wells around the TSVs. **a** *Top view* of the structure and **b** *side view* of the structure

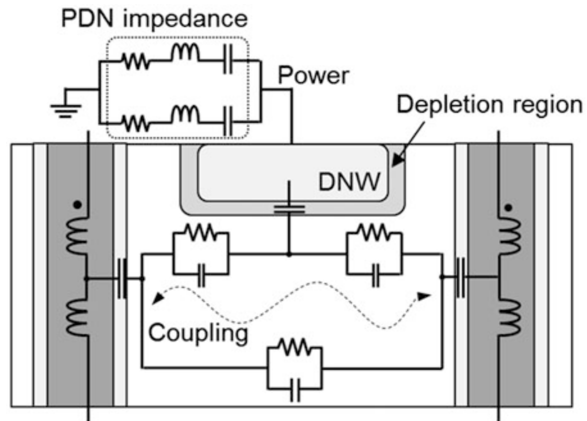


Fig. 4.17 The simplified circuit model for the TSV-TSV noise coupling with nearby active circuits. The active circuits are represented by a deep n-well [11] © 2011 IEEE

designed system [13]. The simplified circuit model of TSV-TSV noise coupling with nearby DNW is illustrated in Fig. 4.17. The circuit model contains the TSV capacitance, the DNW depletion capacitance, the substrate resistance, the substrate capacitance, and the PDN impedance. Because the DNW has relatively high conductivity compared with p-type silicon substrate, DNW doping is 500 S/m in this case, DNW resistance is neglected in the model. In addition, power distribution network (PDN) impedance also can be neglected due to its small value at the interested frequency; it indicates that the TSV reference ground and the DNW are directly connected.

Because the silicon substrate is connected to the ground through a depletion capacitance, the TSV-TSV coupling is expected to decrease compared with the case without nearby active circuits. To confirm the expected results, a 3D-EM simulation is performed for the structure in Fig. 4.16. For the simulation, the

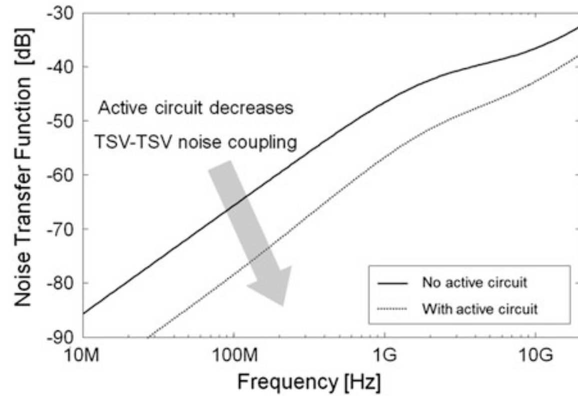


Fig. 4.18 The noise transfer function for the TSV-TSV coupling structure with and without a nearby active circuit [11] © 2011 IEEE

following default values are selected: the TSV radius is 5 μm, the height is 50 μm, the TSV oxide thickness is 0.5 μm, TSV keep-out zone is 5 μm, the PDN impedance is 0 Ω, the DNW size is 500 μm × 500 μm, DNW depletion region thickness is 1.6 μm, and the DNW thickness is 5 μm. Because active circuits are located in all silicon substrates, the default d_{DNW} is chosen to be very large. Figure 4.18 shows the noise transfer function (S_{21}) between 2 signal TSVs with and without a nearby DNW. It indicates that a DNW near TSVs significantly decreases the TSV-TSV noise coupling. Because DNW area is very large, total DNW depletion capacitance has very large value and the DNW around TSV shows good noise isolation at low frequency. The noise isolation decreases as frequency increases because DNW cannot block the inductive coupling and DNW resistance and inductance decreases the noise isolation.

4.3 Analysis of Shielding Structures in 3D-IC

In the previous section, the TSV noise coupling is analyzed considering an actual 3D ICs. However, if the TSV noise coupling exceeds the noise tolerance budget of the 3D ICs, then we need some methods to reduce the coupling.

4.3.1 Guard-Rings (p+/DNW)

In the first and second TSV noise reduction methods, p+ and DNW guard-rings are used, respectively. Guard-rings have been used to isolate the noise through the silicon substrate in conventional 2D-IC systems. In particular, for the mixed-mode system, the analog or RF circuitry is protected from the digital circuit substrate noise using a guard-ring. For 2D-IC, the entire circuitry is on the surface of the

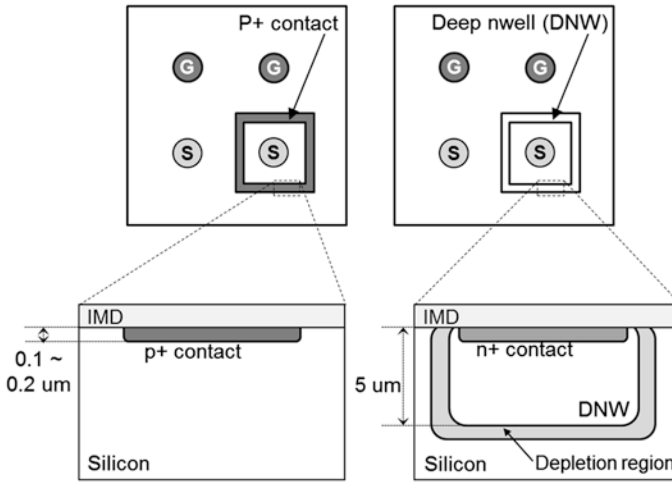


Fig. 4.19 The *top* and cross-sectional views of p+ and DNW guard-rings

silicon substrate, and the guard-ring has a significant noise isolation effect [14]. However, for 3D ICs, the TSV is a vertical structure, and the noise isolation effects of the guard-ring should be validated.

In Fig. 4.19, there are 2 types of guard-ring to reduce the TSV noise: p+ guard-ring and DNW guard-ring. The p+ guard-ring is constructed using a p+ contact connected to ground, whereas the DNW guard-ring is made by a DNW and an n+ contact connected to the DNW. The differences between these 2 guard-rings are illustrated in Fig. 4.19. The p+ contact has a very shallow depth, whereas the DNW is much thicker, and the depletion region generated for the DNW guard-ring is the critical difference between p+ and DNW guard-ring. The depletion region can be regarded as silicon without conductivity and modeled as a capacitor. The depletion capacitance significantly affects the noise coupling reduction and can be calculated using the following equations [15], (Fig. 4.20).

$$C_{dep} = \sqrt{\frac{q\varepsilon_{Si}N_aN_d}{2(N_a + N_d) \times (V_{bi} + V_{well})}}\ [\mathrm{F/m}] \tag{4.11}$$

$$V_{bi} = \frac{kT}{q} \times \ln\left(\frac{N_aN_d}{N_i^2}\right)\ [V] \tag{4.12}$$

where C_{dep} is the DNW capacitance per unit area, V_{well} is the DNW bias voltage, N_a is the doping concentration of the acceptor ions in the silicon substrate, and N_d is the doping concentration of the donor ions in the DNW. The DNW depletion capacitance has high impedance at low frequency and blocks the signal or noise transfer between the silicon substrate and the DNW guard-ring while the p+ guard-ring is directly connected to silicon substrate.

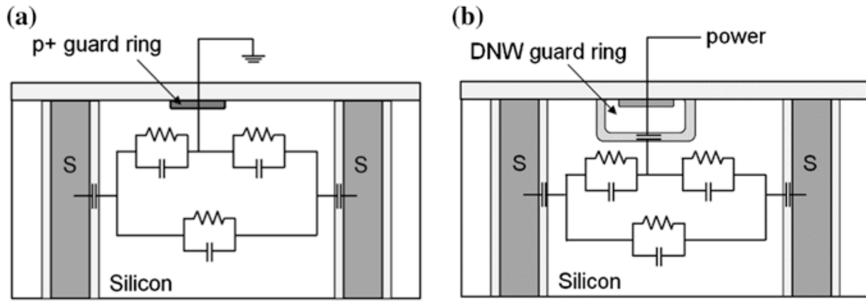
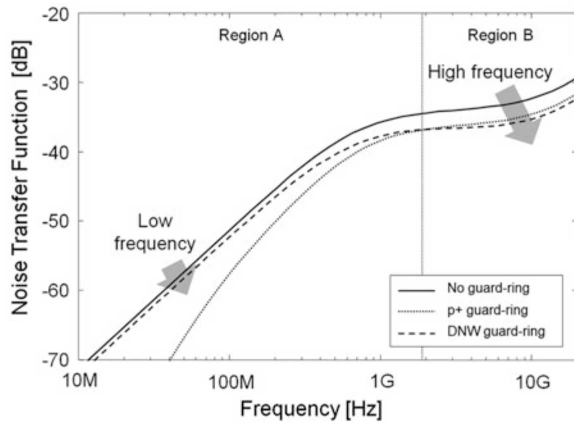


Fig. 4.20 The simplified schematic for guard-rings applied to TSV-TSV coupling structure [16] **a** the schematic of p+ guard-ring and **b** the schematic of DNW guard-ring

Fig. 4.21 The noise transfer function for the TSV-TSV noise coupling structure with and without p+ and DNW guard-rings. [17] © 2010 IEEE



Using the 3D-EM simulation, the TSV-to-TSV noise transfer function is estimated for three cases: without any guard-ring, with a p+ guard-ring, and with a DNW guard-ring. In this case, we assumed that the TSV radius is 15 μm, the height is 100 μm, the width of both the p+ and the width of DNW guard-rings is 10 μm, and the distance between the signal TSV and the guard-ring is 10 μm. To determine the DNW depletion thickness, the following values are assumed in reasonable ranges: $N_a = 10^{15}$ cm^{-3}, $N_d = 10^{18}$ cm^{-3}, $T = 300$ K, $V_{well} = 1.8$ V. Also the conductance of DNW is assumed as 500 S/m, which is 50 times larger than p-type silicon substrate. Using 4.11 and 4.12, the DNW depletion capacitance, C_{dep}, is calculated to 5.74 nF/cm^2. The simulation assumes that both the top and the bottom of the TSVs are terminated with a 50 Ω, and the simulated NEXT graphs are plotted in Fig. 4.21.

In Fig. 4.21, both the p+ guard-ring and the DNW guard-ring have noise isolation effects. At low frequency, the p+ guard-ring shows much higher noise isolation effects, whereas it has small effects at high frequency. However, the DNW guard-ring has only a small noise isolation effect at low frequency and better

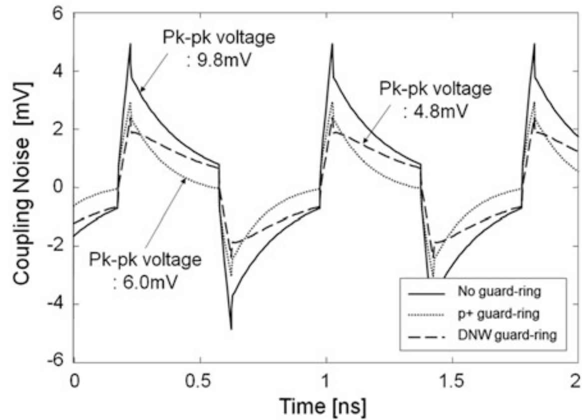


Fig. 4.22 The time-domain coupling noise waveform with and without guard-ring: p+ guard-ring and DNW guard-ring effects are compared with the case of no guard-ring. [17] © 2010 IEEE

noise isolation than the p+ guard-ring at high frequency. For the DNW guard-ring, the depletion capacitance blocks the guard-ring from the silicon substrate at low frequency, and the guard-ring has almost no noise isolation effect at low frequency. However, when the frequency increases, the impedance of the depletion capacitance decreases, and the advantages of the larger thickness appear in the noise isolation characteristics. At region B in Fig. 4.21, the DNW guard-ring has better noise isolation than the p+ guard-ring because the depletion capacitance effects are minimized and the large thickness enhances the noise isolation. This result is easy to understand using the simplified circuit model in Fig. 4.20.

The time-domain coupling noise graphs are plotted in Fig. 4.22. A 2.5 Gbps, 1-V peak-to-peak clock signal with a rise/fall time of 50 ps is inserted at the lower side of the aggressor TSV with a source impedance of 50 Ω. The upper and lower sides of the TSV are terminated with 50 Ω. Because the DNW guard-ring has better noise isolation than the p+ guard-ring at high frequency, the peak-to-peak noise voltage is smaller for the DNW guard-ring. The peak-to-peak noise voltage is 4.8 mV for the DNW guard-ring case, whereas it is 6.0 mV for the p+ guard-ring. However, at low frequency, the p+ guard-ring is better than the DNW guard-ring; at the steady state of the input signal, the coupling noise voltage is smaller for the p+ guard-ring. Therefore, depending on the system noise tolerance target, the guard-ring must be carefully selected.

4.3.2 Shielding TSVs

Before the analysis of shielding TSV, we will first focus on the TSV pitch increase, which is the preliminary step of shielding TSVs because we need at least 2 times of the minimum TSV pitch between 2 signal TSVs. Increasing the signal TSV pitch is the most basic coupling reduction methods. However, it decreases the TSV routing density, which is the opposite result of the original 3D ICs purpose, which

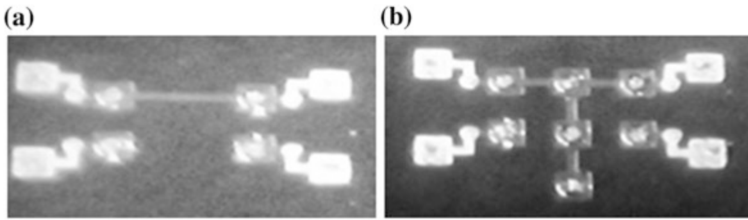
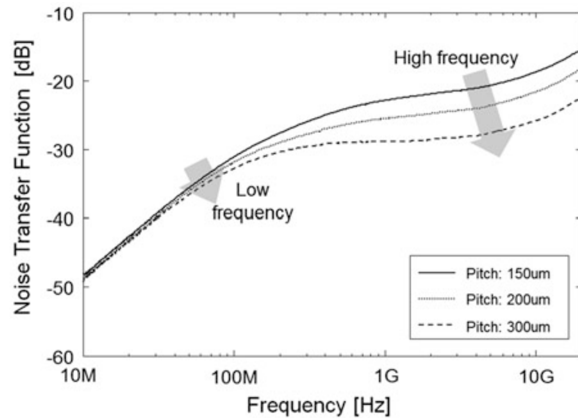


Fig. 4.23 The *top view* of the TSV-TSV noise coupling structures. **a** TSV-TSV noise coupling structure without any shielding TSV and **b** with 3 shielding TSVs

Fig. 4.24 The noise transfer function for the TSV-TSV noise coupling structure with TSV-TSV pitch variations



is to increase the number of I/Os. Nevertheless, this method is a very powerful coupling reduction method that can be used in some applications with small TSV I/Os. The effects of increasing the signal TSV pitch is previously modeled using the equations in Sect. 4.2.1. It increases substrate resistance and decreases substrate capacitance and has a noise isolation effects at mid- and high- frequency ranges. However, for the measurement-based validation of the TSV-TSV noise coupling reduction effects of increasing the signal TSV pitch, the test vehicles are manufactured by Electronics and Telecommunications Research Institute (ETRI) as shown in Fig. 4.23a. It has a radius of 30 µm, an oxide thickness of 0.1 µm, and a height of 100 µm. The TSV noise coupling was measured in both the frequency domain and the time domain. When the signal TSV pitch increases, the measured noise transfer functions are illustrated in Fig. 4.24. Because the low-frequency noise transfer function is dominated by the TSV oxide capacitance, increasing the signal TSV pitch does not give noise isolation effects at low frequency. However, it has good noise isolation effects at frequencies over several MHz.

Inserting shielding TSVs is also a good noise isolation method, and the shielding TSVs are conceptually depicted in Fig. 4.25. Although this method is expected to provide good noise isolation effects, the shielding TSVs require some area, and the TSV I/O density decreases. In addition, the signal TSV pitch should

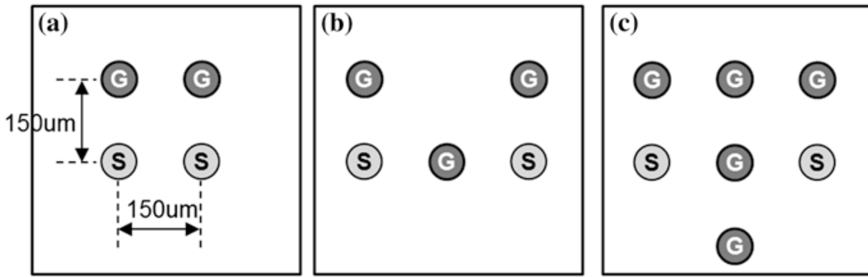


Fig. 4.25 The conceptual view of three TSV-TSV noise coupling structures. **a** Reference structure with no shielding TSV, **b** structure with 1 shielding TSV, and **c** structure with 3 shielding TSVs

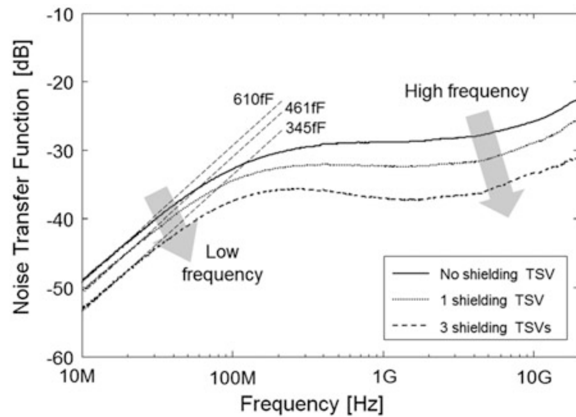


Fig. 4.26 The noise transfer function for the TSV-TSV noise coupling structure with various numbers of shielding TSVs

be increased before the shielding TSVs are inserted, because there is a minimum TSV pitch. To insert the shielding TSVs, the signal TSV pitch is increased as shown in Fig. 4.25.

To validate the noise isolation effects of the shielding TSVs, the test vehicles are manufactured by ETRI, and the dimensions are exactly identical to the previous dimensions. The frequency-domain noise transfer functions are plotted in Fig. 4.26. As we expected, the shielding TSV has good noise isolation at both low and high frequencies. When the shielding TSVs are inserted, the total equivalent TSV capacitance decreases, and the noise transfer function at low frequency decreases. It also decreases the total substrate capacitance and increases the total substrate resistance, and the noise transfer function decreases at high frequency. The total equivalent TSV capacitance is calculated as follows.

$$C_{TSV_equivalent} = \frac{C_{TSV}}{(\#\ of\ TSV)}\ [\mathrm{F}] \tag{4.13}$$

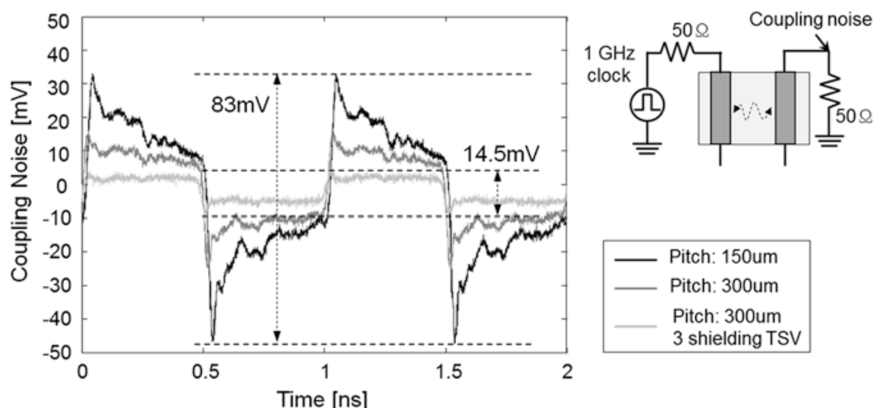


Fig. 4.27 The time-domain waveform of the TSV coupled noise when a 1 GHz clock is inserted into the signal TSV, and the TSV termination is 50 Ω

Because the total equivalent TSV capacitance is only determined by the number of TSVs, it can be calculated using Eq. 4.13. The total equivalent capacitance for the structure with no shielding TSV is $C_{TSV}/4$ and for the case of 3 shielding TSVs is $C_{TSV}/7$. In the measurement results in Fig. 4.26, the total equivalent TSV capacitance is extracted and consistent with Eq. 4.13. In this case, the TSV capacitance of the single TSV is approximately 2400 fF. The TSV coupling noise is also measured in the time domain. The 1-V peak-to-peak clock with 100 MHz and 1 GHz is injected into one TSV, and the coupling noise is measured at the other TSV. The results are illustrated in Fig. 4.27. The reference pattern has the signal TSV pitch of 150 μm, which is increased to 300 μm for the 2nd one. For the 3rd one, 3 shielding TSVs are inserted among the signal TSVs. Because the peak-to-peak noise voltage is determined using the high-frequency noise transfer function, increasing the signal TSV pitch reduces the peak-to-peak noise. For the case with 3 shielding TSVs, the noise reduction effects are maximized, and the noise decreases from 90 to 18 mV and from 83 to 14.5 mV for 100 MHz and 1 GHz, respectively. Increasing the signal TSV distance from 150 to 300 μm and inserting 3 shielding TSVs reduce the peak-to-peak noise voltage by approximately 80 %.

4.3.3 Shielding Bumps

The final TSV noise coupling reduction method is grounding the bottom side of the silicon substrate using shielding bumps. For p+/DNW guard-ring, we used top-side of silicon substrate but we can also use the back-side. At the backside of silicon substrate, oxide layer is essential to prevent direct contact of bumps to the

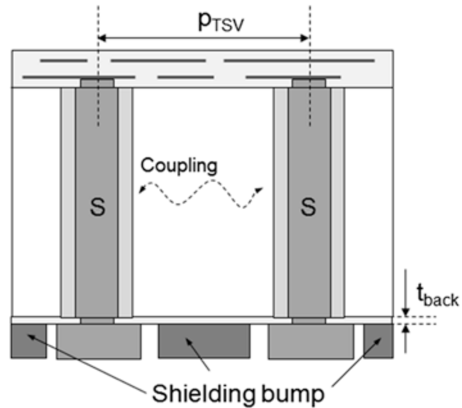


Fig. 4.28 The conceptual view of shielding bumps. The bumps at the bottom of the silicon substrate are connected to the ground to have the effects of shielding bumps [11] © 2010 IEEE

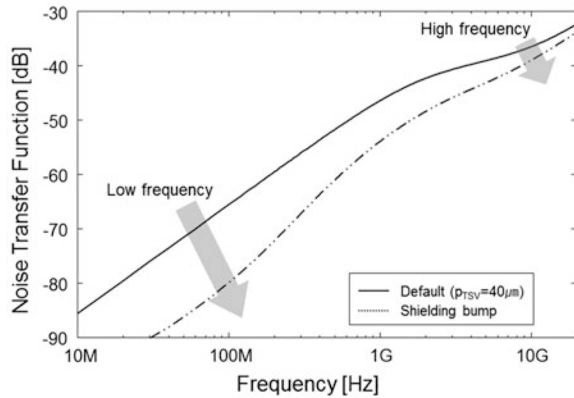


Fig. 4.29 The noise transfer function for the TSV-TSV coupling structure with and without shielding bumps

silicon substrate. If the oxide layer can be removed, the direct connection of a metal line to the silicon substrate generates Schottky contact and substrate does not be grounded. We need substrate contact to make the Ohmic contact [15], but it is impossible at the back-side of substrate.

Instead, grounding the silicon substrate using back-side bumps is a possible method as illustrated in Fig. 4.28. Because there is a capacitance between the shielding bump and the silicon substrate, the low-frequency noise isolation mechanism is exactly identical to a DNW (active circuit) near the TSVs in the previous chapter. The low-frequency shielding effects depend on the thickness of the back-side insulation layer, which is necessary to prevent direct connection between the signal bump and the silicon substrate. If this insulation layer thickness decreases, the low-frequency noise isolation effects increase because of the increased capacitance between the shielding bumps and the silicon substrate. The noise reduction effects of the shielding bumps are illustrated in Fig. 4.29. As we expected, the noise transfer function has similar shapes to that in Fig. 4.18. The

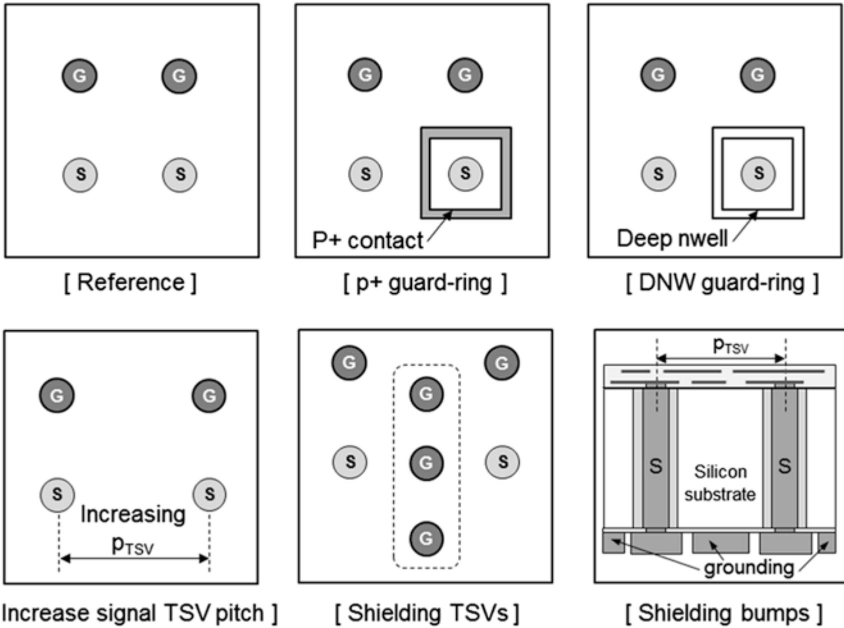


Fig. 4.30 The several TSV-TSV noise coupling reduction structures

back-side insulation layer has a large capacitance because of the thin insulation layer and the large area of the shielding bumps; it has good noise isolation effects at low frequency. At high frequency, the noise isolation effects significantly decrease because only the bottom surface of the silicon substrate is connected to the ground through a capacitor. This result is identical to the p+ guard-ring case in Fig. 4.21. For the frequency under several GHz, shielding bumps have good noise isolation effects. However, it consumes large back-side metal routing area to ground the back-side bump.

4.3.4 Comparison of TSV Shielding Structures

We proposed several TSV shielding structures such as the p+/DNW guard-ring, the shielding TSVs, and the shielding bumps. The conceptual figure of the TSV-TSV noise coupling basic structure and several shielding structures are shown in Fig. 4.30.

The noise transfer functions for these structures are shown in Fig. 4.31. Each structure has its own advantages and disadvantages. At low frequency, the p+ guard-ring and the shielding bump exhibit good noise isolation, whereas the DNW guard-ring, the increased signal TSV pitch, and the shielding TSVs provide

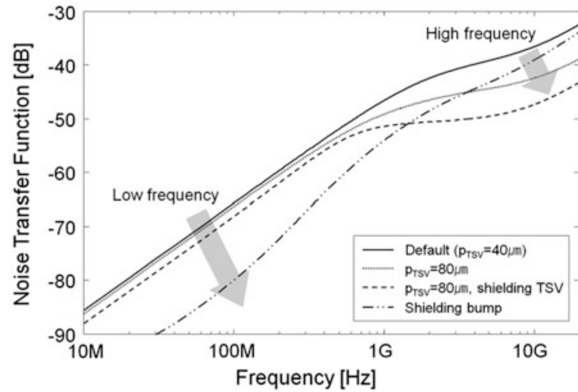


Fig. 4.31 The noise transfer function comparison for several noise coupling reduction structures [11] © 2011 IEEE

Table 4.3 Comparison of several noise coupling reduction methods

	P+ guard-ring	DNW guard-ring	Increasing signal TSV pitch	Shielding TSVs	Shielding Bumps
Needs of active process	Yes	Yes	No	No	No
Shielding at low frequency	Good	Bad	Bad	Middle	Good
Shielding at high frequency	Middle	Middle	Good	Good	Bad
Disadvantage	Active-circuit area decreased	Active-circuit area decreased	Decreased TSV density	Decreased TSV I/O density	Decreased routing area

good noise isolation at high frequency. The mechanisms of these shielding structures are explained in the previous subsections. Except the noise isolation effects at low or high frequency, we should consider several aspects, which is very important to use these noise isolation techniques in practice. To use the p+ or DNW guard-ring, we require that an active process and active circuit areas are consumed. To increase the signal TSV pitch, the TSV density decreases. For the shielding TSVs, the signal TSV I/O density decreases. For the shielding bump, we suffer from the routing area decrease at back-side. These advantages and disadvantages are summarized in Table 4.3.

4.4 Summary

This chapter models and analyzes the TSV noise coupling and proposes several TSV noise coupling reduction methods. From the analysis, which is based on the equivalent circuit model, the frequency-dependent coupling mechanisms of the TSV were analyzed in three frequency-behavior regions. When the TSV technology develops, the TSV density increases, and the TSV noise coupling is seriously considered for the noise-reliable circuit design. Therefore, an accurate estimate of the TSV noise-transfer function is necessary to efficiently manage the noise-tolerance budgets. In addition, the proposed shielding technique, which uses a guard ring, shielding TSVs, or shielding bumps, can be applied to an actual 3D ICs. The analyses are summarized as follows.

- TSV noise coupling
  - TSV is formed inside the conductive silicon substrate, and large amounts of noise are coupled through the conductive silicon substrate.
  - TSV noise coupling can be divided into TSV-TSV coupling and TSV-active circuit coupling.
  - For both TSV coupling cases, the TSV noise coupling can be analyzed in three frequency regions: At low frequency, the TSV capacitance dominates the coupling, whereas the silicon substrate resistance and capacitance dominate the coupling at mid and high frequencies.
  - For TSV-TSV coupling, mutual inductance affects the coupling at high-frequency, but the coupling through the conductive substrate is the main mechanism of the coupling.
- TSV termination effects
  - TSV termination significantly affects the time-domain TSV noise and TSV I/O driver should be considered for the actual 3D ICs.
  - If we increase the I/O driver size, input driver resistance decreases and output driver capacitance increases. By the simple calculation using the circuit theory, it was shown that TSV noise decreases when TSV I/O driver size increases.
  - For the signal propagation through TSV, large input driver and small output driver are preferable. We can reduce the TSV noise coupling by increasing the input driver size with the fixed size small output driver.
- The effects of active circuit around TSV
  - In actual 3D ICs, lots of active circuits are placed at the surface of silicon die and greatly affects TSV noise coupling.
  - The active circuit can be assumed as DNW with power connection for the simplicity and TSV noise voltage is captured by DNW.

  - By the noise capturing mechanism of DNW, TSV noise coupling decreases if active circuits are placed near the signal TSVs and it should be considered for the analysis of TSV noise coupling at actual 3D ICs.

- Several TSV noise coupling reduction methods
  - If TSV noise coupling exceeds the noise tolerance budget of 3D ICs, several noise coupling reduction methods are necessary.
  - We proposed p+/DNW guard-ring, shielding TSV, and shielding bump as the TSV noise coupling reduction methods.
  - p+ guard-ring has good noise isolation effects at low frequency while DNW guard-ring has better noise isolation at high frequency. Both guard-ring consumes active circuit area and should be carefully used considering the cost issues.
  - Shielding TSV shows good noise isolation at all frequency whereas increasing signal TSV pitch has noise isolation effects only at mid- and high-frequency. It decreases TSV I/O density and can be used in some cases.
  - Shielding bump has similar mechanism of guard-rings and it has good noise isolation. It does not consume the active circuit area while it consumes the back-side routing area.

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Chapter 5
Thermal Effects on TSV Signal Integrity

Manho Lee, Jun So Pak and Joungho Kim

Abstract In this chapter, we propose temperature dependent TSV isolation model and the result is applied to the channel model. The thermal effect on through-silicon via (TSV) noise coupling and S_{21} of TSV channel were measured in both frequency and time domain from corresponding TSV based test vehicle. These measurement results are analyzed using the temperature-dependent TSV lumped model to TSV channel and shows good correlation with measurement. Under the hundreds-of-MHz frequency range, increasing temperature decreases the S_{21} of TSV channel, but over that frequency range, increasing temperature increases the S_{21}. These phenomena are explained from the model which thermal dependence of the materials is applied.

Keywords Through-silicon via · Temperature-dependent TSV lumped model · Thermal effects · Noise coupling · TSV signal integrity

5.1 Overview

With the rapid development of IC technologies, through silicon via (TSV) based three-dimensional integrated circuits (3D ICs) have become an important technology in semiconductor industries as a new paradigm. In 3D ICs, the TSV provides a vertical interconnection with the remarkably reduced interconnect length

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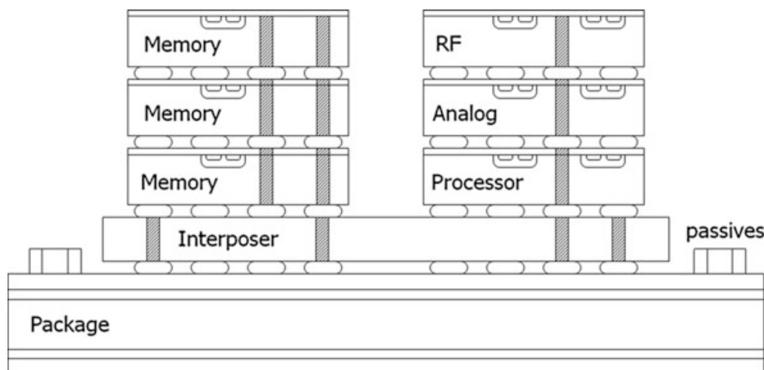


Fig. 5.1 A conceptual figure of interposer-based 3D ICs; vertical integration of both homogeneous and heterogeneous are possible. In this figure, same memories are stacked vertically and connected with processor through interposer at the *bottom*

among the stacked dies. The conceptual figure of representative 3D ICs structure using vertical interconnections is described in Fig. 5.1. As the necessity of high-speed channel between a transmitter and receiver became higher, signal integrity (SI) and power integrity (PI) analyses have become more important to ensure stable performance. One issue that is carried on through this chapter is thermal effects on TSV signal integrity. Because TSV-based 3D ICs may save area and power due to the structure itself generally, it also may isolate heat dissipation path from various switching elements and cores inside. In mechanical perspective, rising the temperature of the chip may cause bit error because it may changes not only physical feature but also material properties. Therefore, some researches tried to improve thermal issues that can be taken place in 3D ICs. Effective TSV floor planning, redundant thermal TSVs, and even micro fluidic channel inside in the silicon die [1, 2] are representative researches. As emphasized in previous chapters and preceding researches, the noise coupling result from the silicon substrate between TSVs [3] and high speed channel performance are our most interesting signal integrity issues.

For instance, noise coupling between signal TSVs may increase jitter, phase noise of the clock signal, and power ground noise [4] so that the entire performance of the system can be degraded. Also, the noise from active circuit itself can pass through the substrate and can be coupled to TSV. As a result, TSV channel transmission characteristic is changed. Figure 5.2 shows typical TSV channel and noise coupling path in 3D ICs as an example.

To resolve these signal integrity issues, researchers have proposed various ways of suppressing noise coupling between TSVs, and shielding TSVs and guard rings [5] are one of typical methods. Most of those signal integrity investigations in 3D ICs, however, assume room temperature situation.

There are two examples of thermal specifications of mass-produced state-of-art 2D ICs-based semiconductors in Figs. 5.3 and 5.4 [6, 7]. For these extreme

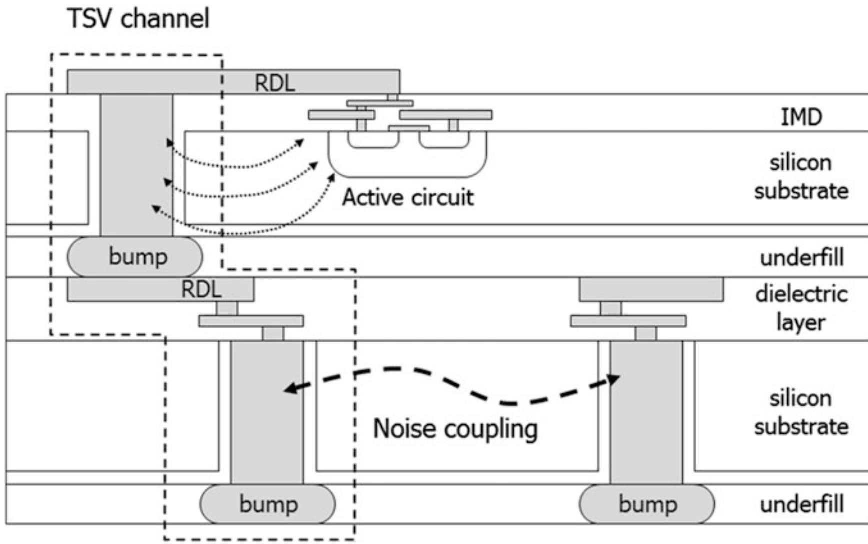
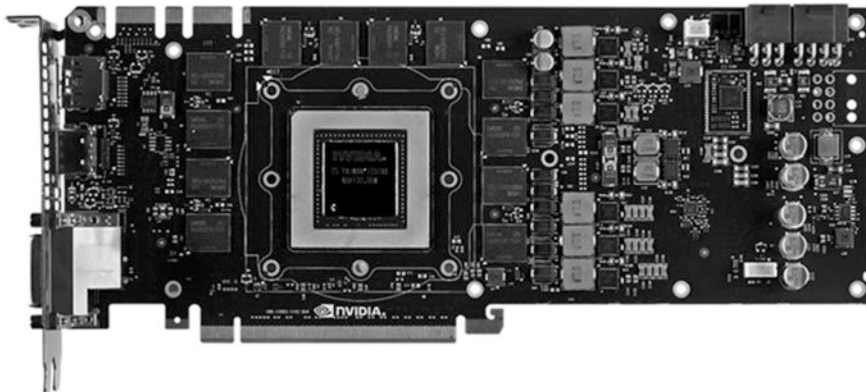


Fig. 5.2 Typical TSV channel and noise coupling path in stacked dies are shown. In 3D ICs, the coupled signal from active circuit or the other signal TSVs finally may cause a signal failure



Thermal and Power Specs:	
Maximum GPU Tempurature (in C)	95 C
Graphics Card Power (W)	250 W
Minimum System Power Requirement (W)	600 W
Supplementary Power Connectors	One 8-pin and one 6-pin

Fig. 5.3 Nvidia GeForce GTX TITAN's appearance and its thermal specifications

Package Specifications	
Max CPU Configuration	1
$T_{JUNCTION}$	100°C
Package Size	37.5mm x 37.5mm x 4.7mm
Sockets Supported	FCPGA946
Low Halogen Options Available	See MDDS

Fig. 5.4 Intel® Core™ i7-4930MX processor extreme edition's thermal specifications

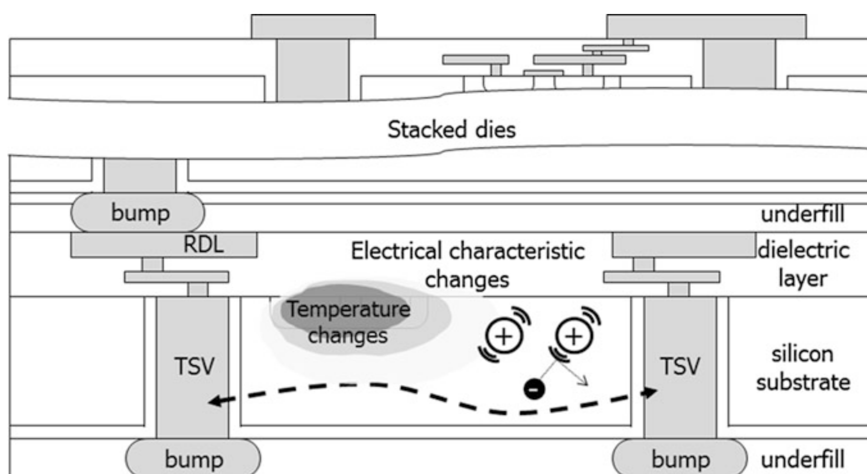


Fig. 5.5 Temperature effect on the noise coupling between signal TSVs in 3D ICs. Because the material properties of silicon are dominantly temperature-dependent, the noise coupling through the silicon substrate can be changed

processors, the max temperature is restricted to about 100 °C. As far as temperature is concerned, it means that thermal issues will become even more serious in 3D ICs and have to be considered in a view point of signal integrity.

In an actual operating case, the temperature increases as cores switch. In the higher bandwidth application, this switching speed should also increase accordingly. We are very interested in observing signal integrity issues in 3D ICs, and more realistic situations are made when temperature dependence to the signal integrity is considered. Figure 5.5 represents a conceptual figure of temperature effect on noise coupling between two TSVs. In a general manner, active circuits are fabricated in the silicon substrate which has a proper conductivity. These may cause the increase of silicon substrate's temperature. One very simple fact is, the conductivity of silicon substrate is varied in terms of temperature of it. The conductivity is not only depending on the type of doping, but also depending on the temperature. In this chapter, we utilize widely-used p-type silicon substrate with 10 Ω·cm.

5.2 Temperature-Dependent TSV Isolation Characteristics and Model

In this chapter, temperature-dependent TSV's isolation characteristic is investigated by measuring the noise coupling between signal TSVs and re-modeling the TSV's isolation characteristic with lumped elements which is proposed in the early chapter. First of all, the noise coupling is measured in frequency domain and time domain both. After, temperature-dependent TSV's isolation characteristic is modeled by applying temperature dependence of material properties. This modeling is proposed as a form of an equivalent SPICE circuit by applying some related equations. Material characteristics are properly applied to this model by referencing the former researches.

5.2.1 Measurement of Temperature-Dependent TSV and Noise Coupling

To know the effect of temperature to the signal integrity in 3D ICs, a test vehicle was fabricated with the help of SK Hynix Semiconductor Inc. This test vehicle for measuring temperature-dependent noise coupling shown in Figs. 5.6 and 5.7 has coupled-TSVs structure (Two pairs of GS TSVs). TSV radius (r_{TSV}) and height (h_{TSV}) are approximately 16.5 and 100 μm, respectively. The pitch between signal TSVs (p_{TSV}) is 160 μm and the distance between signal TSV and ground TSV is 250 μm. The oxide thickness (t_{ox}) is approximately 0.5–0.6 μm. Ground TSVs are connected through RDL between ground pads.

Basically, noise coupling frequency response between signal TSVs is obtained by taking S-parameter. To measure, the bottom ends of coupled TSVs are open-terminated and 2-port measurement is performed using VNA (Vector Network Analyzer) and 250 μm pitch micro probes. Figure 5.8 shows the measurement setup for temperature-dependent frequency domain data. To prevent electrical leakage from the contact between the open-ended TSV and the metal jig, insulation is necessary. In addition, that insulation should endure from heat. Therefore, heat resisting material (Polyurethane material Ureol®) and heat resisting double-sided tape (Kapton®; a polymide film developed by DuPont that remains stable across a wide range of temperature from −269 to 400 °C) is attached under test vehicle. In this measurement setup, we utilize hit convection and measured using IR thermal imager from fluke®.

Figure 5.9 shows the result of the temperature-dependent noise coupling coefficient in frequency domain. The noise coupling was measured from 10 MHz to 20 GHz and 25 to 100 °C. The result shows different aspects in low frequency region and high frequency region. At high frequency region above hundreds of MHz (approximately 300 MHz in this experiment), noise coupling decreases as temperature increases, however at low frequency region under it, noise coupling

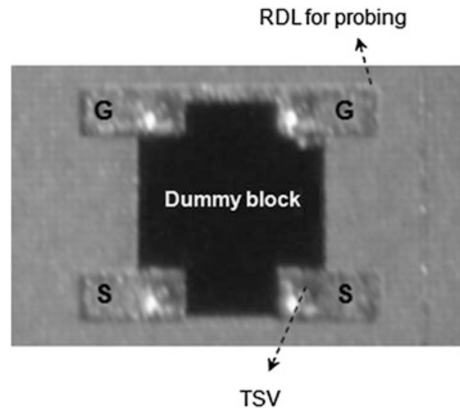


Fig. 5.6 *Top view* of SEM image of fabricated coupled TSV test vehicle. There exists RDL for probing at the *top*, and GND are connected through metal line

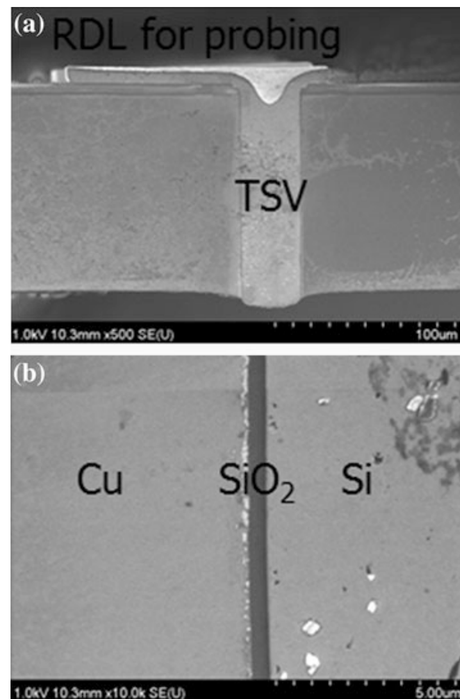


Fig. 5.7 **a** Cross section SEM image of test vehicle. **b** Zoom of SEM image at the interface between Cu, SiO_2, and Si. The role of SiO_2 is to prevent direct contact between signal (Cu) and substrate (Si)

slightly increases as temperature increases. Over 10 GHz range, the trend of noise coupling becomes same as frequency increases. At 1 GHz, noise coupling decreases about 3 dB, and at 10 MHz, noise coupling increases about 1.5 dB. Figure 5.10 shows this result in temperature domain. About 300 MHz range, the trend is reversed as explained. In next chapter, we will analyze and discuss about this phenomenon.

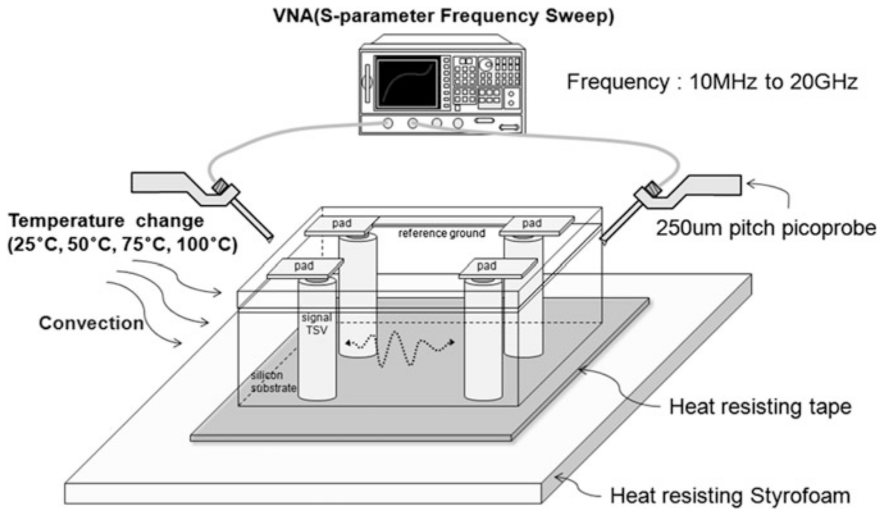


Fig. 5.8 Measurement setup for temperature-dependent TSV noise coupling in frequency domain [8] © 2012 IEEE

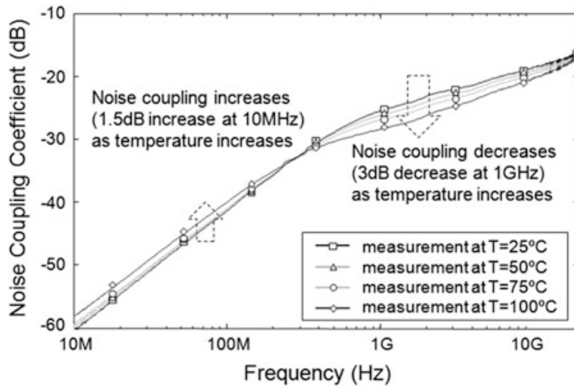


Fig. 5.9 Noise coupling measurement result with temperature variation in frequency domain. As temperature increases, noise coupling, coupling between signal TSV's near-end ports, increases at high frequency region over hundreds of MHz range but shows opposite results at the low frequency region below that range. At very high frequency over 10 GHz, the graphs are gathered as same [8] © 2012 IEEE

To confirm and correlate the frequency domain response of noise coupling, time domain measurement was also performed. Instead of VNA for frequency domain measurement, PPG (Pulse Patter Generator from Anritsu) as a source and oscilloscope for measurement are connected separately as shown in Fig. 5.11. Injected voltage in TSV is 1.0 volt peak-to-peak rectangular clock with 1 GHz frequency.

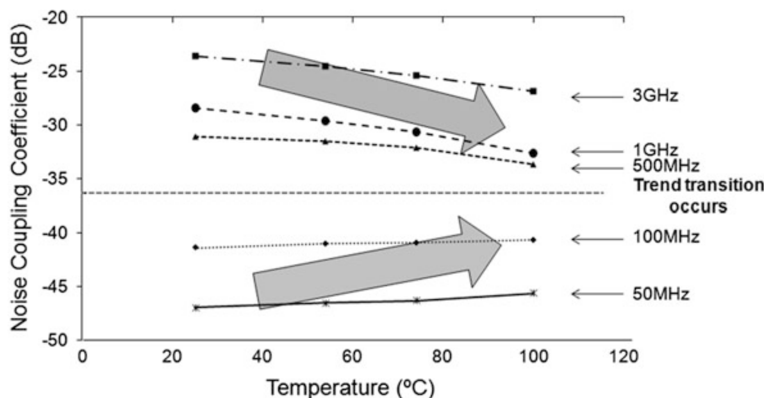


Fig. 5.10 Temperature domain measurement (which is basically as same as Fig. 5.9) is shown. About 300 MHz frequency, noise coupling trend in terms of temperature is reversed [8] © 2012 IEEE

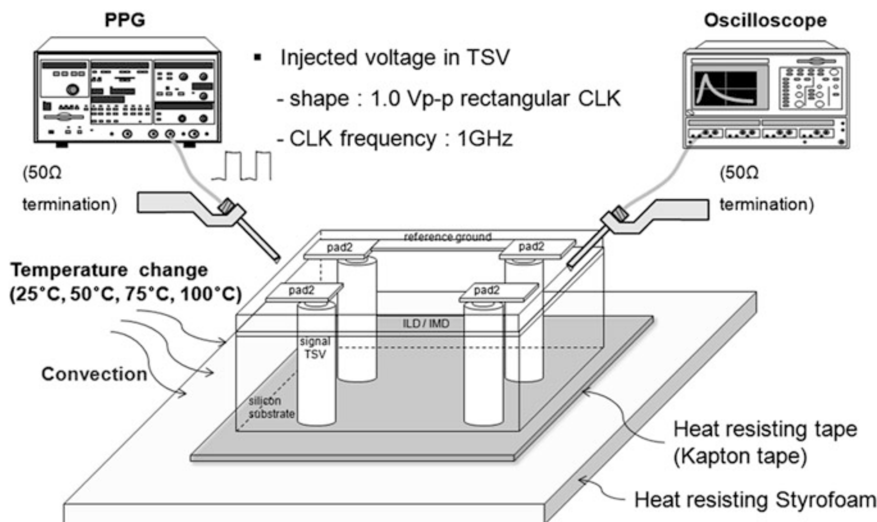


Fig. 5.11 Measurement setup for temperature-dependent TSV noise coupling in time domain. Same configuration is made except connecting PPG at one signal TSV and oscilloscope at the other. Rectangular 1Vp-p of 1 GHz signal is injected as a source

Because the rising time of PPG is about tens-of-pico seconds, the results may include some high frequency components.

Figure 5.12 shows time domain measurement results with varying temperatures from 25 to 100 °C. As the temperature rises until 100 °C, the peak-to-peak value decreased from 89 to 70 mV. A peak value of coupled signal can be varied by signal's rising time or falling time, and it is the device's property. Although the

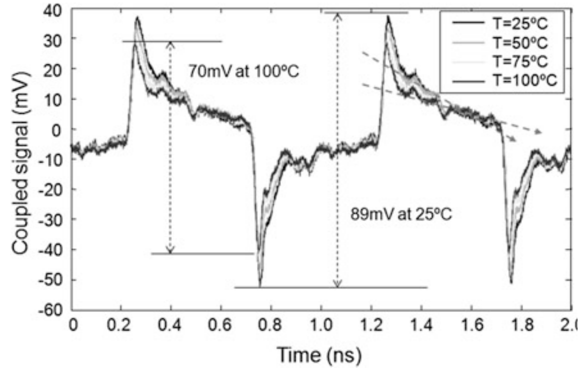


Fig. 5.12 Noise coupling measurement result with temperature variation in time domain. As shown in frequency domain measurement, high frequency component near rising and falling period and low frequency component during maintaining the DC signal show reversed characteristics when the temperature is increased [8] © 2012 IEEE

peak values are determined by the device's property, the temperature dependence of coupled signal is clearly demonstrated in the result figure. Noise coupling decreases as frequency decreases and the trend of it depends on the temperature variation. The rectangular clock signal used as an input signal basically has three frequency components; 1 GHz as an operating frequency (mid frequency range), about tens of GHz from both rising and falling (very high frequency range), and DC component (low frequency range) during maintaining rectangular clock. After the signal is rising, the signal suddenly goes to DC components to maintain voltage until falling starts. This means, the trend reversion from temperature variation shown in frequency domain should be presented in time domain measurement. In Fig. 5.12, all of these phenomena are exactly presented. As same as the frequency result, time domain result will be analyzed and discussed in next chapter by revising conventional TSV model.

5.2.2 Temperature-Dependent Modeling of TSV

To analyze the temperature dependence phenomenon of noise coupling, coupled TSV structure is temperature-dependently modeled using SPICE based components. Before establishing temperature-dependent model, temperature dependence of three main materials composing TSV (Si, Cu, and SiO_2) ICs are investigated.

5.2.2.1 Temperature Dependence of Substrate's Conductivity

Conductivity of semiconductor is mainly determined by two factors. The first is free carrier concentration, and the second is their mobility. Both are independently temperature-dependent [9]. For the case of metal like copper, only lattice scattering should be considered. However, for the semiconductors like silicon and germanium, conductivity depends not only free carriers concentration (n, p in (5.1)), but also their mobility (μ_n, μ_p in (1)). It can be expressed like this form.

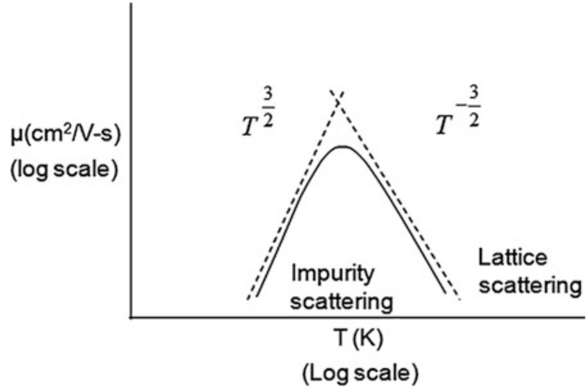


Fig. 5.13 Temperature versus semiconductor mobility. The mobility is dependent to the temperature and divided to two regions where impurity scattering dominant region and lattice scattering dominant region [9]

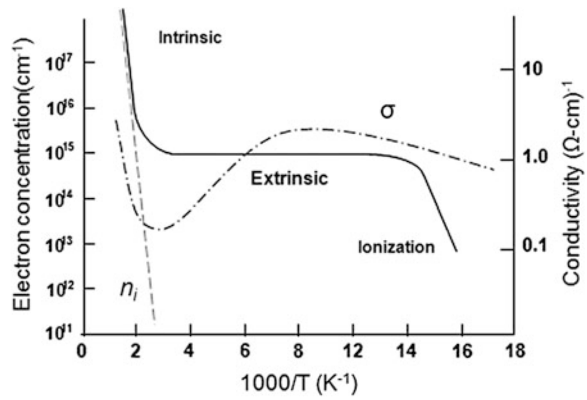


Fig. 5.14 Carrier concentrations versus temperature with 10^{15} donors/cm^3 and corresponding conductivity [9]

$$\sigma = q\left(\mu_n(T)n(T) + \mu_p(T)p(T)\right) \tag{5.1}$$

Figure 5.13 roughly represents temperature dependence of semiconductor mobility. For the low temperature region under room temperature, normally impurity scattering dominates and the carrier mobility depends on $T^{3/2}$. However, for the high temperature region, normally lattice scattering dominates and the carrier mobility depends on $T^{-3/2}$ [9].

Figure 5.14 shows the relation between carrier concentration and temperature when silicon is doped as 10^{15}/cm^3 as an example [9]. This varies with doping concentration. From this phenomenon, we can recognize that there exist some possible variations due to the temperature dependencies for the conductivity.

Figure 5.15 shows another temperature dependence of doped silicon resistivity as a function of concentration [9, 10]. As shown, the silicon resistivity is very sensitive to the doping type and concentration. The test vehicle's silicon is a p-type and the known resistivity in room temperature is about 10 Ω·cm. Based on this information, silicon concentration can be roughly obtained. If somewhat different resistivity is used, concentration will be changed.

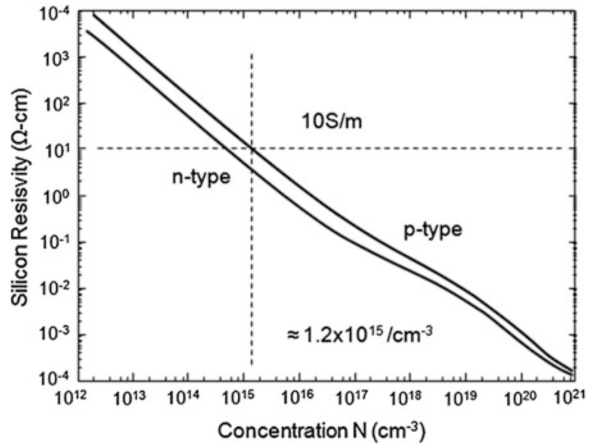


Fig. 5.15 The relationship between resistivity and dopant density for P and Br doped Silicon [9, 10]

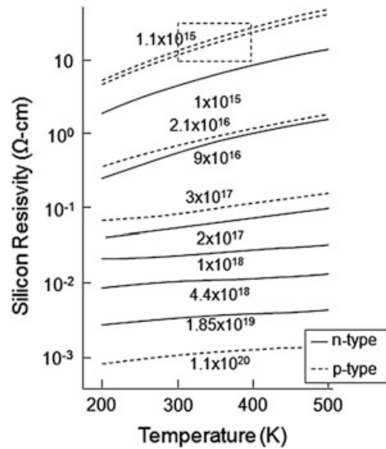


Fig. 5.16 Temperature dependence of doped silicon resistivity as a function of concentration [11]

Figure 5.16 shows the temperature dependence of doped silicon resistivity as a function of concentration [11]. As shown, silicon resistivity is not only very sensitive to the doping type and concentration, but also to the temperature. This data was obtained by using experimentally fitted equations within 250–500 K (−27 to 227 °C). Based on the reference of Figs. 5.15 and 5.16, silicon's resistivity correspond to the test vehicle's known material property can be obtained within 25–100 °C where we are looking at.

5.2.2.2 Temperature Dependence of Copper's Conductivity

We used copper as a conductor material in TSV as usual. Copper is a general metal which resistivity is dominated by lattice scattering when the temperature is

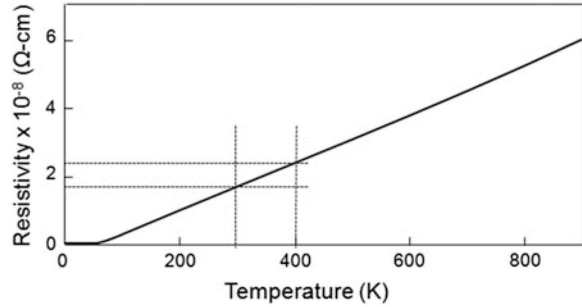


Fig. 5.17 Temperature dependence of copper resistivity. The region we need to utilize is where the resistivity is linearly proportional to the temperature [12]

increased. Thus, it is easy to know the resistivity value between room temperature to 100 °C. The dependence shows almost linear characteristics as shown in Fig. 5.17 [12].

5.2.2.3 Temperature Dependence of SiO_2

SiO_2 is a dielectric material which dielectric constant is affected by environ-mental factors not only from temperature. Therefore, specific material data for this experiment is not known. After the measurement, this temperature dependence of SiO_2's dielectric constant is simply fitted with linear equations.

5.2.3 Modeling of Temperature-Dependent Isolation Characteristic of TSV

In this section, we will model temperature-dependent isolation model of TSV by establishing some equations. Figure 5.18 shows a basic model between two TSVs, and some equivalent parameters are marked on the figure.

From the references related to the materials [9–11], resistivity (ρ, dimension: Ω·cm) and conductivity ($\sigma = 1/\rho$, dimension: S/m) values corresponding to the test vehicle depending on the temperature range were approximately obtained and arranged in Table 5.1. Silicon and Copper are conductive materials and show the same increasing trend as temperature increases within 25–100 °C.

A capacitance of silicon dioxide as an insulator is determined by dielectric constant, thickness of silicon dioxide, height of substrate, and TSV's radius.

$$C_{ox} = \varepsilon_{ox} \times \frac{2\pi h_{si}}{\ln \frac{r_{TSV}+t_{ox}}{r_{TSV}}} \, [\mathrm{F}]. \tag{5.2}$$

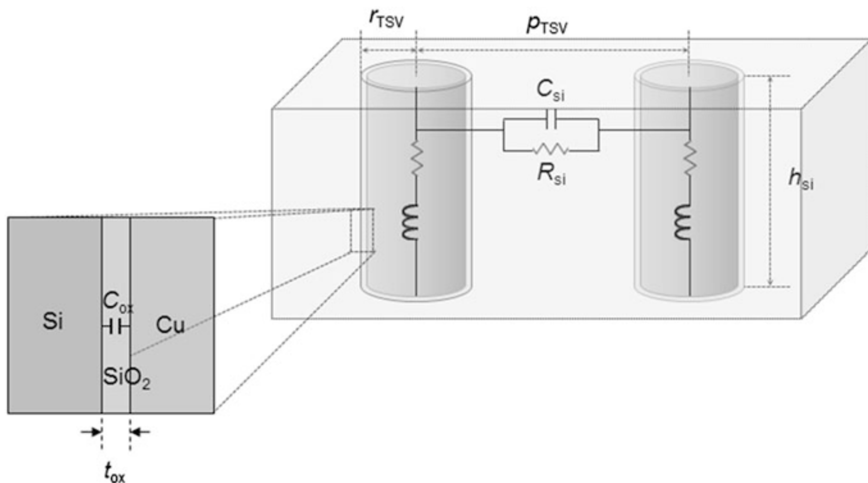


Fig. 5.18 The equivalent model of a TSV pair is shown. There exists very thin insulation layer between silicon substrate and copper via and it is modeled as oxide capacitance (C_{ox})

Table 5.1 Temperature-dependent resistivity and conductivity of silicon and copper

Temperature (°C)	Resistivity (Ohm·cm)		Conductivity (S/m)	
	Silicon	Copper	Silicon	Copper
25	10	1.725×10^{-8}	10	58000,000
50	11.5	1.893×10^{-8}	8.695	52380,000
75	14	2.060×10^{-8}	7.143	48540,000
100	19	2.231×10^{-8}	5.263	44820,000
125	21	2.402×10^{-8}	4.76	41630,000

The capacitance of silicon substrate can be modeled by the height of silicon substrate, pitch, radius of TSVs, and dielectric constant of silicon. The equations are shown below.

$$C_{si} = \varepsilon_{si}(T) \times \frac{\pi h_{si}}{\cosh^{-1}\left(\frac{p_{TSV}}{2r_{TSV}}\right)} \text{ [F]}. \tag{5.3}$$

The resistance of silicon is determined by the capacitance with the relationship as shown in equation below.

$$R_{si}C_{si} = \frac{\varepsilon_{si}}{\sigma_{si}} \tag{5.4}$$

$$R_{si} = \rho_{si}(T) \times \frac{\cosh^{-1}\left(\frac{p_{TSV}}{2r_{TSV}}\right)}{\pi r_{TSV}} \, [\Omega]. \tag{5.5}$$

The resistance of TSV is determined by the equation below. It is the combination of DC part and AC part of resistance. AC part of the resistance depends on the skin depth of TSV.

$$R_{TSV} = R_{TSV}(T) \times \sqrt{\left(\frac{h_{TSV}}{\pi r_{TSV^2}}\right)^2 + \left(\frac{h_{TSV}}{\pi\left(r_{TSV^2} - \left(r_{TSV} - \delta_{skin_depth}\right)^2\right)}\right)^2} \, [\Omega/\mathrm{m}] \tag{5.6}$$

$$\delta_{skin_depth} = \frac{1}{\sqrt{\pi f \mu_{TSV} \sigma_{TSV}}} \, [\mathrm{m}]. \tag{5.7}$$

Finally, the inductance of TSV is determined as below. The value of TSV inductance is determined by pitch, radius, height of TSV, and permeability of TSV.

$$L_{TSV} = \frac{1}{2}\left\{\frac{\mu_0 \mu_{r,TSV}}{2\pi} \times h_{TSV} \times \ln\left(\frac{p_{TSV}}{r_{TSV}}\right)\right\} [\mathrm{H/m}]. \tag{5.8}$$

Between the parameters above, parameters which have potential of sensitive to the temperature are silicon resistance R_{si}, silicon capacitance C_{si}, oxide capacitance C_{ox}, and TSV resistance R_{TSV}. Dielectric constant generally does not have large variation within this temperature range, but for the case of silicon oxide, mechanical effect due to very thin thickness will not be ignored. So, the temperature-dependent modeling of TSV is focused on R_{si}, C_{ox}, and R_{TSV}. As shown above, all components have dimension parameters like TSV radius, TSV height, or TSV pitch, and material parameters like dielectric constant and permeability. If mechanical stresses were ignored, the dimension parameters would not be changed and only material properties would be changed. This assumption will be applied to the following temperature-dependent model (Fig. 5.19).

Based on the analytical equations above, temperature-dependent values are applied to this model. In this model, ground and signal open-ended as test vehicle is fabricated, and are 50 Ω-terminated as same as VNA is connected. Some of values are optimized using the measurement result. Room temperature values are shown in Table 5.2.

From the Table 5.1, we can make experimental equations of silicon resistivity as a quadratic form

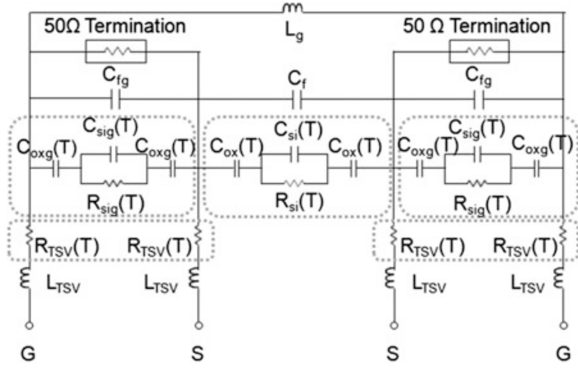


Fig. 5.19 Temperature-dependent TSV–TSV model of test vehicle. The component inside the *dotted circle* are mainly temperature dependent. In this figure substrate model between farther G-S pairs and small parasitic components are omitted [13] © 2011 IEEE

Table 5.2 Estimated parameters at room temperature model [13] © 2011 IEEE

Component	Value	Component	Value
R_{si}	1055 mΩ	R_{TSV}	0.85 mΩ
C_{ox}	239.5 fF	L_{TSV}	8.9 pH
C_{si}	11.86 fF	C_f	2.3 fF
R_{sig}	671 Ω	C_{fg}	3.9 fF
C_{oxg}	479 fF	L_g	46.6 pH
C_{sig}	18.82 fF		

$$\rho_{si}(T) = 0.0012T^2 - 0.0352T + 10. \tag{5.9}$$

For SiO_2, a temperature dependence is simply assumed as a linear form by comparing with experiment results.

$$\varepsilon_{si}(T) = 0.016T + 3.6. \tag{5.10}$$

For the silicon dielectric constant, a temperature-dependent equation is not determined here because the noise coupling difference due to temperature variation over higher frequency range over 10 GHz is negligible. This will be explained little bit more.

As shown in Fig. 5.20, when we apply temperature dependence of silicon resistivity, model and measurement shows similar trend in frequency domain. As mentioned earlier, SiO_2 variance is obtained from the experiment result. From this result, we need to know the dominant parameters in each frequency range.

Silicon capacitance, silicon resistance, and oxide capacitance can be modeled as equivalent parallel of capacitance and resistance as Fig. 5.21.

$$C_{eq} = \frac{C_{ox}\left(\left(\frac{1}{R_{si}}\right)^2 + C_{si}\omega^2(C_{si} + C_{ox})\right)}{\left(\frac{1}{R_{si}}\right)^2 + \omega^2(C_{si} + C_{ox})^2}\ [\mathrm{F}]. \tag{5.11}$$

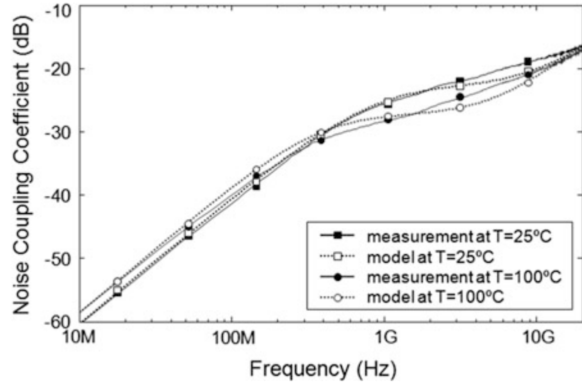


Fig. 5.20 The comparison of temperature-dependent noise coupling from the lumped model and measurement. 25 and 100 °C are compared

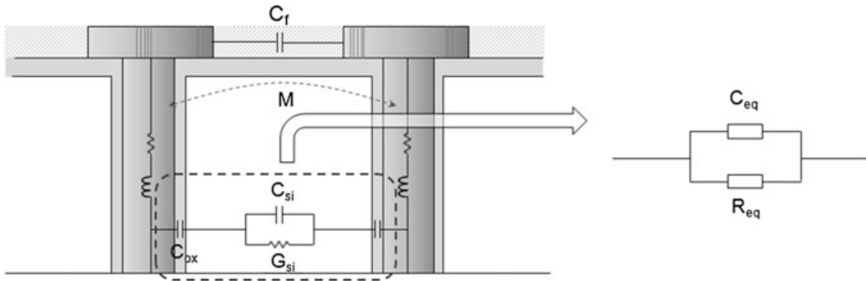


Fig. 5.21 Comparison of measurement and model in frequency domain at 25 and 100 °C

For equivalent capacitance C_{eq}, it converges to C_{ox} as frequency decreases, and goes $C_{ox}//C_{si}$ as frequency increases. Because C_{ox} is generally and comparatively larger than C_{si}, $C_{ox}//C_{si} \approx C_{si}$ and C_{eq} converges to C_{si} as frequency increases.

$$R_{eq} = \frac{\left(\frac{1}{R_{si}}\right)^2 + \omega^2 (C_{si} + C_{ox})}{\left(\frac{1}{R_{si}}\right)^2 \omega^2 C_{ox}^2} \, [\Omega]. \tag{5.12}$$

For equivalent resistance R_{eq}, it diverges to infinity as frequency decreases, and goes R_{si} as frequency increases.

From these simplifications (R_{eq} and C_{eq}), the frequency domain noise coupling response can be analyzed as shown in Fig. 5.22. At a low frequency region, the noise coupling is dominantly affected by oxide capacitance. As frequency increases, the resistance of silicon substrate effects dominantly to noise coupling. Over the 10 GHz range, silicon capacitance and fringing capacitance between metal pads becomes dominant parameter.

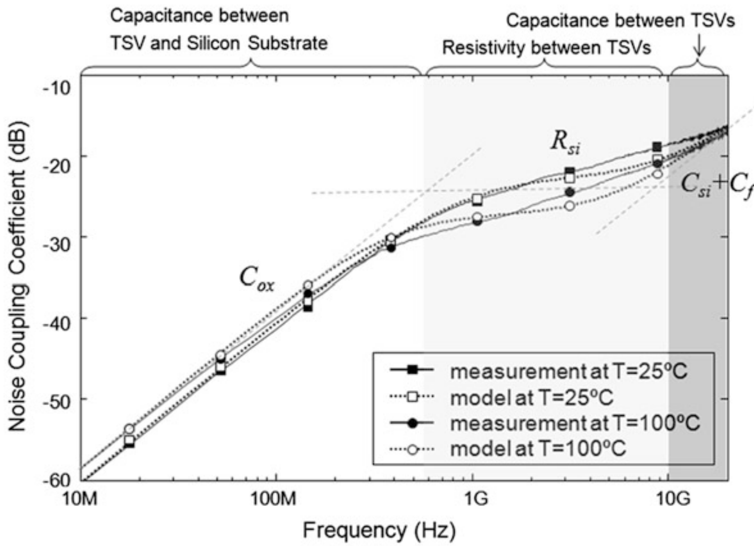


Fig. 5.22 Analysis of dominant parameters in frequency range. It can be divided into three main regions and the model and measurements are compared as Fig. 5.20

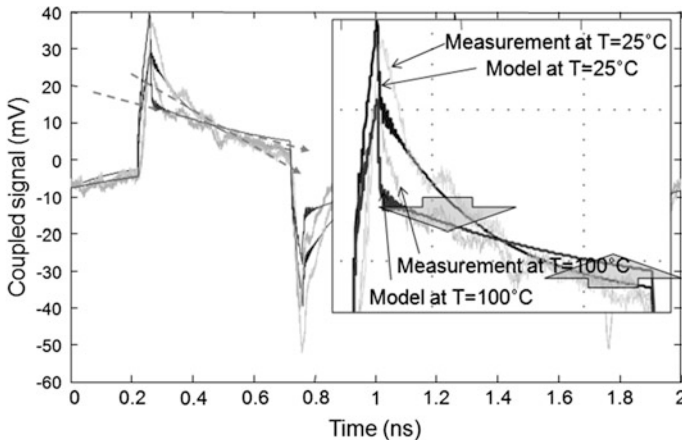


Fig. 5.23 Comparison of model and measurement in time domain at 25 and 100 °C

Figure 5.23 shows the comparison of measurement and model at T = 25 and 100 °C. As measured before, the slope of the output from temperature-dependent model changes. When signal rises, the peak value at 25 °C is much bigger than that of at 100 °C. However, as signal is maintaining DC voltage, noise coupling decreases faster. This temperature-dependent model shows good correlation with measurement result.

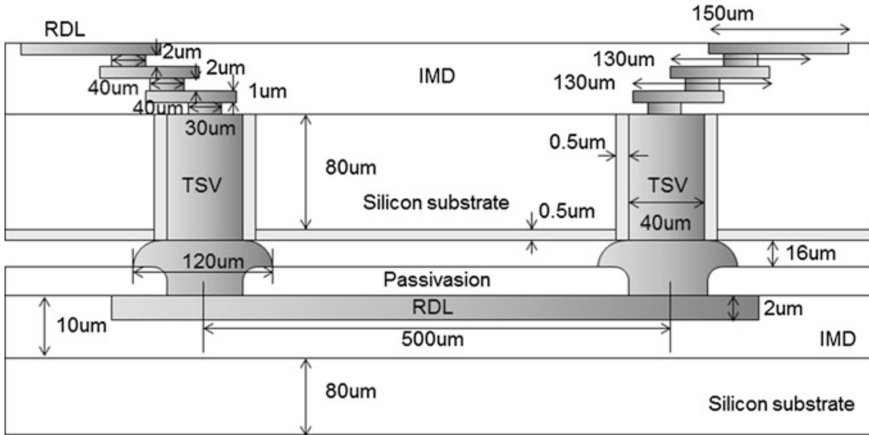


Fig. 5.24 The dimension parameters of test vehicle for measuring TSV channel. To see the channel effect, two dies are vertically stacked using bumps between the dies [8] © 2012 IEEE

5.3 Temperature-Dependent TSV Channel

In this chapter, temperature-dependent TSV channel is measured and investigated by modeling TSV and RDL.

5.3.1 Measurement of Temperature-Dependent TSV Channel

To investigate the temperature effect on TSV channel, another test vehicle fabricated from KETI was used.

Figure 5.24 represents cross section of stacked die with RDL channel between TSVs. For RDL channel, length is 500 μm, width is 100 μm, thickness is 2 μm, and the pitch is 250 μm. For TSV, radius is 20 μm, height is 80 μm, and oxide thickness is about 0.5 μm. For the bumps between TSV and RDL, radius is 120 μm, height is about 34.6 μm. The whole length of metal RDL on the TSV is about 200 μm, and the thickness is between 1 to 2 μm (1st stack: 1 μm, 2nd and 3rd stack:2 μm).

Figure 5.25 shows SEM image of test vehicle. Although it was designed using the values above, there exist manufacturing issues when dies are stacked. (Mismatch voids…). As shown in Fig. 5.25, there were some design variation and voids. These variations can slightly affect to the measurement result, but not bring dramatic changes.

The TSV channel shows basically the same structure as the test vehicle for the noise coupling except the RDL metal below the TSV. Therefore, it can be

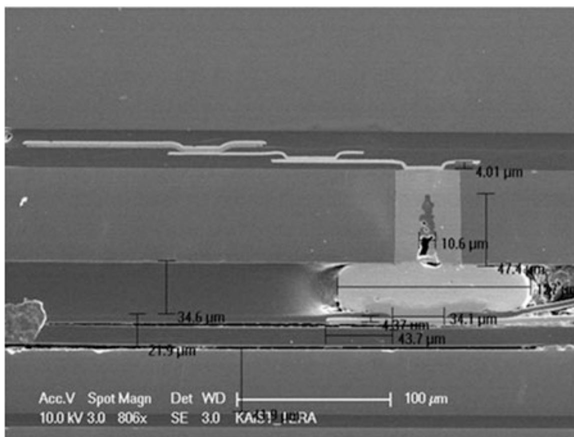


Fig. 5.25 The *side view* of the test vehicle for TSV channel SEM image [8] © 2012 IEEE

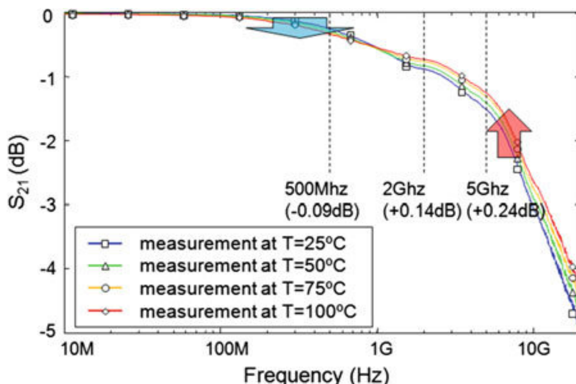


Fig. 5.26 S_{21} of TSV channel measurement result with temperature variation in frequency domain [8] © 2012 IEEE

anticipated the S_{21} characteristic will be explained with TSV noise coupling analysis. Figure 5.26 shows S_{21} measurement in frequency domain with temperature variation from 25 to 100 °C. Under GHz range, S_{21} decreases as temperature increases, but over GHz range, S_{21} increases as temperature increases. It reveals that in low frequency under GHz range, the loss increases as temperature rises, and in high frequency over GHz range, the loss decreases as temperature rises. This is correspondence with noise coupling result. At a high frequency region, the noise coupling was decreased due to the increase of silicon substrate's resistivity as temperature increase, and at a low frequency region, the noise coupling was slightly increased due to the change of oxide capacitance (in increasing way) as temperature increases. We can get insight here that substrate's temperature dependence is important as we saw in previous chapter.

To confirm the result in frequency domain, eye diagram measurement at 1, 4 and 10 GB/s with 100 °C was done with similar device setup of noise coupling. Eye height and jitter were compared between 25 and 100 °C at each bit rate. Eye

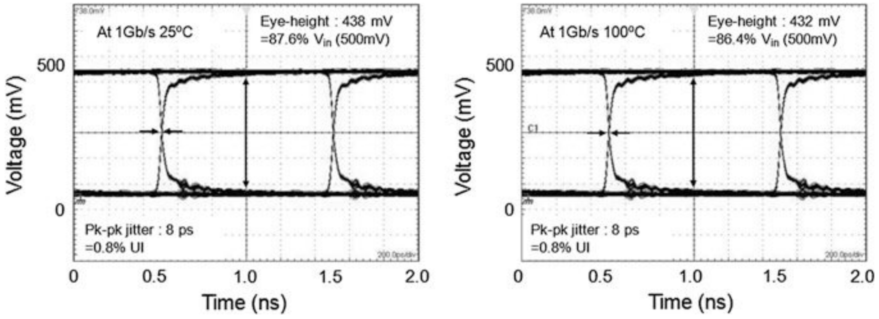


Fig. 5.27 TSV channel eye measurement of 1 Gb/s at 25 and 100 °C [8] © 2012 IEEE

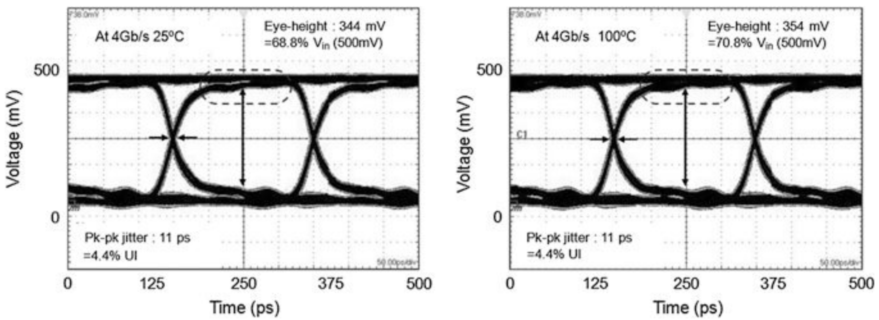


Fig. 5.28 TSV channel eye measurement of 4 Gb/s at 25 and 100 °C [8] © 2012 IEEE

height is defined as the distance between and the end point of 3σ (standard deviation) of high and low within 20 % of UI at the center, and each eye was obtained after 5,000 cycles.

For 1 Gb/s, eye height decreases about 1 % and jitter is almost same. As shown in Fig. 5.27, there exists little signal loss when temperature increases.

For 4 Gb/s, eye height increases about 2 % and jitter is almost same. As show in Fig. 5.28, signal loss is decreased when temperature increases. This comes from the increases of silicon substrate's resistivity when temperature increases.

For 8 Gb/s, eye height increases about 2.5 % and jitter is decreased about 0.4 %. As shown in Fig. 5.29, signal loss is also decreased as shown at 4 Gb/s when temperature increases.

Eye measurement showed correspondence with frequency domain measurement results that the temperature variation affects on the S_{21} of TSV channel and the magnitude of difference varies depending on the input signal's frequency.

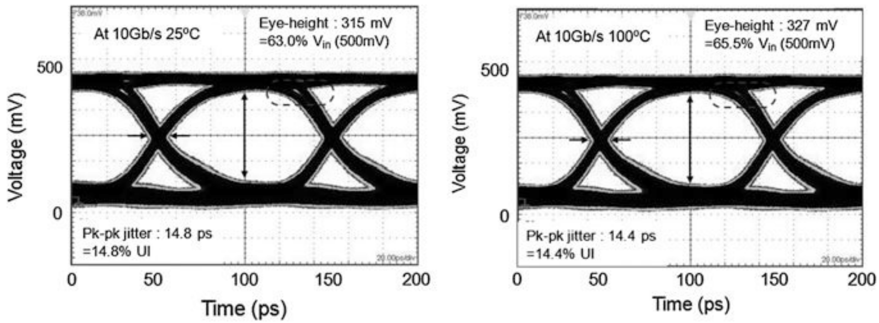


Fig. 5.29 TSV channel eye measurement of 8 Gb/s at 25 and 100 °C [8] © 2012 IEEE

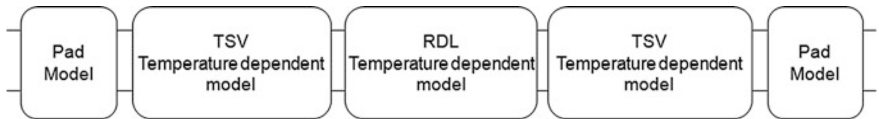


Fig. 5.30 The simplification of temperature-dependent TSV channel for modeling [8] © 2012 IEEE

5.3.2 *Temperature-Dependent Modeling of TSV Channel*

To investigate temperature-dependent TSV channel, same approach with noise coupling was done here. For TSV channel model, we need some more parts to be modeled. RDLs have significant larger length than TSV height and it should be considered. They can affect not only to the increase of resistance itself but also to the increase of substrate resistance due to the length of it.

All the dimension and material parameters are based on the actual test vehicle's SEM images and know material information. To establish the whole channel model, each section in Fig. 5.30 was modeled separately and connected. Parameters related to temperature were shared. Figure 5.31 shows perspective view of TSV channel which is fabricated through KETI. To improve the accuracy of the model, all of the parameters related to the temperature should be considered and inter-relation between the objects should be calculated.

Because the silicon substrate's resistivity variation from temperature effect is dominant, it should consider temperature's effect.

The RDL is a metal interconnect which provides horizontal interconnections between differently-sized stacked dies. Like TSVs, analytic RLGC equations for the equivalent circuit model of single-ended RDL can be modeled as Fig. 5.32 [14].

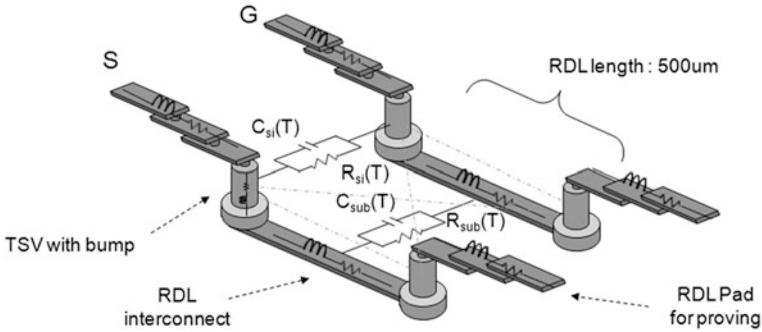


Fig. 5.31 Perspective view of TSV channel [8] © 2012 IEEE

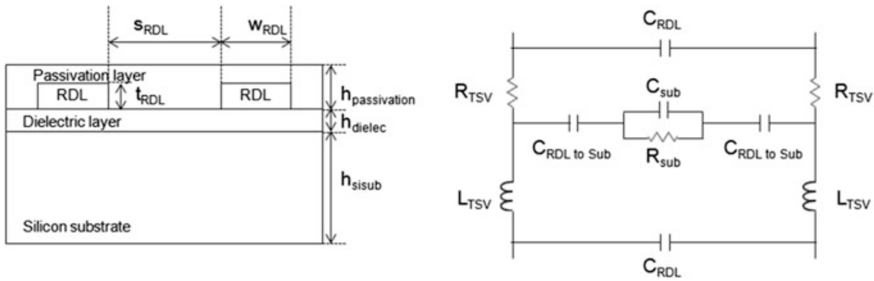


Fig. 5.32 Structure of single-ended signal RDL and its equivalent circuit [8] © 2012 IEEE

$$R_{RDL} = \rho_{TSV}(T)\sqrt{\left(\frac{1}{w_{RDL} \times \delta_{skindepth}}\right)^2 + \left(\frac{1}{w_{RDL} \times t_{RDL}}\right)^2}\ [\Omega/\text{m}] \tag{5.13}$$

$$\delta_{skindepth} = \frac{1}{\sqrt{\pi\mu\sigma \times freq}}\ [\text{m}]. \tag{5.14}$$

The inductance of RDL is modeled with the loop inductance model through approximating the two wire transmission line models.

$$\begin{aligned} L_{RDL} &= \frac{1}{2}\left(L_{signal} + L_{ground} - 2M\right) \\ &= \frac{1}{2}\left\{\frac{\mu_0\mu_r}{2\pi}\left(2\ln\frac{s_{RDL}}{t_{RDL}} + \frac{1}{2}\right)\right\}\ [\text{H/m}]. \end{aligned} \tag{5.15}$$

The parasitic capacitances of RDL, fringe capacitances between the RDLs of the air, passivation layer, and dielectric layer have to be considered as shown in Fig. 5.33.

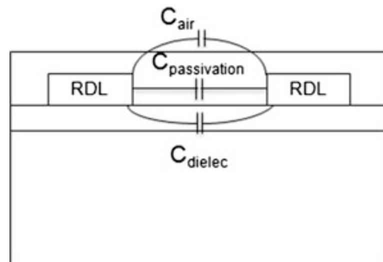


Fig. 5.33 Capacitances between RDLs

The inductance of RDL is modeled with the loop inductance model by approximation to the wire transmission line model.

$$C_{RDL} = C_{air} + C_{dielec}\ [\mathrm{F/m}] \tag{5.16}$$

$$C_{air} = \varepsilon_0 \varepsilon_{r,air} \frac{K(k_0)}{K'(k_0)}\ [\mathrm{F/m}] \tag{5.17}$$

$$C_{passivation} = \varepsilon_0 \left(\varepsilon_{r,passivation} - \varepsilon_{r,air}\right) \frac{K(k_1)}{K'(k_1)}\ [\mathrm{F/m}] \tag{5.18}$$

$$C_{dielec} = \varepsilon_0 \left(\varepsilon_{r,dielec} - \varepsilon_{r,passivation}\right) \frac{K(k_1)}{K'(k_1)}\ [\mathrm{F/m}] \tag{5.19}$$

$$k_0 - \sqrt{1 - \left(\frac{w_{RDL}}{s_{RDL}}\right)^2} \tag{5.20}$$

$$k_1 = \sqrt{1 - \frac{\sinh^2\left(\frac{\pi w_{RDL}}{2h_{passivation}}\right)}{\sinh^2\left(\frac{\pi s_{RDL}}{2h_{passivation}}\right)}} \tag{5.21}$$

$$K_1 = \sqrt{1 - \frac{\sinh^2\left(\frac{\pi w_{RDL}}{2h_{dielec}}\right)}{\sinh^2\left(\frac{\pi s_{RDL}}{2h_{dielec}}\right)}} \tag{5.22}$$

where K is complete elliptical integral of the first kind (Fig. 5.34).

As mentions earlier, RDL is put on a conductive silicon substrate, and it gives an effective electrical path between RDLs. First, electrical field penetrates through the dielectric layer and then go through the silicon substrate. The capacitance between RDL and silicon substrate is

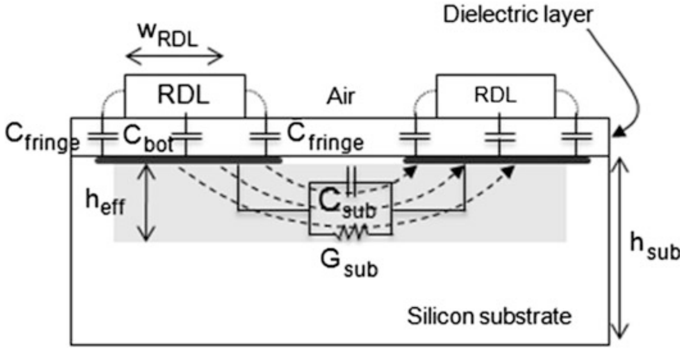


Fig. 5.34 Effective electrical field path through silicon substrate

$$\begin{aligned} C_{RDL_{to\,sub}} &= C_{bot} + 2C_{fringe} \\ &= \varepsilon_0 \varepsilon_{r,SiO_2} \times \frac{w_{RDL}}{h_{IMD}} + \varepsilon_{r,SiO_2} \frac{K\left(k_{[vp]}\right)}{K'\left(k_{[vp]}\right)} \text{ [F/m]} \end{aligned} \tag{5.23}$$

where

$$k_{[vp]} = \sqrt{1 - \left(\frac{h_{dielec}}{h_{dielec} + t_{RDL}}\right)^2}. \tag{5.24}$$

Finally, capacitance and resistance of substrate can be modeled as below. The capacitance is modeled with the effective penetration depth of the electric field into silicon substrate, h_{eff}

$$G_{sub} = \frac{\sigma_{eff} w_{RDL}}{h_{eff}} \text{ [F/m]} \tag{5.25}$$

$$C_{sub} = \varepsilon_0 \varepsilon_{r,Si} \times \frac{w_{RDL}}{h_{eff}} \text{ [F/m]} \tag{5.26}$$

where

$$\varepsilon_{r,eff} = \frac{\varepsilon_{r,si} + 1}{2} + \frac{\varepsilon_{r,si} - 1}{2\sqrt{1 + 10\frac{h_{dielec} + h_{sisub}}{w_{RDL}}}} \tag{5.27}$$

$$\sigma_{eff} = \frac{\sigma_{si}}{2\sqrt{1 + 10\frac{h_{dielec} + h_{sisub}}{w_{RDL}}}} \tag{5.28}$$

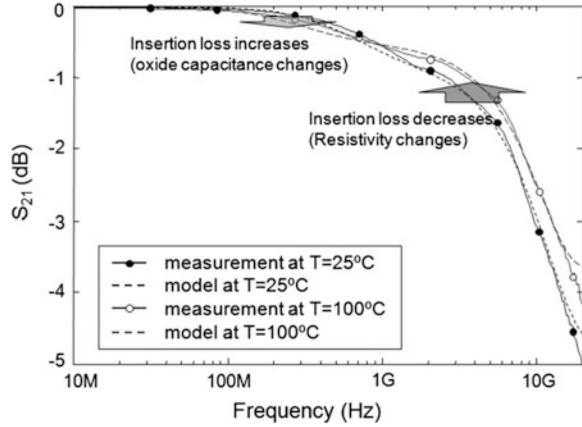


Fig. 5.35 The comparison of temperature-dependent TSV channel model and measurement at 25 and 100 °C [8]

$$h_{eff} = \frac{w_{RDL}}{2\pi} + \ln\left(\frac{8h}{w_{RDL}} + \frac{w_{RDL}}{2h}\right). \tag{5.29}$$

By using all the parameters and temperature dependence, S_{21} can be obtained by SPICE model (Fig. 5.35).

There exist some differences between the model and the measurement, and it normally comes from oxide thickness and RDL length.

5.4 Summary

This chapter discusses the effect of temperature on 3D ICs; in particular the temperature-dependent TSV model and noise coupling are presented. TSV noise coupling was measured from 25 to 100 °C and analyzed using the corresponding temperature-dependent TSV model. In the p-type 10 Ω·cm silicon substrate, the noise suppression level increases over 300 MHz as the temperature increases, whereas suppression decreases at frequency less than 300 MHz as temperature increases. The trend reversion frequency can be changed because the equivalent capacitance and resistances changes as dimension parameters changes. For the case of temperature-dependent TSV channel, the results shows similar trends with noise coupling and phenomena can be explained in same manner. Therefore, when we try to design TSV based 3D ICs, thermal effects on signal integrity should be carefully considered. A temperature increasing varies silicon substrate's property and it can even effect 3D ICs channel.

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Chapter 6
Power Distribution Network Modeling and Analysis for TSV and Interposer-Based 3D ICs in the Frequency Domain

Kiyeong Kim, Jun So Pak and Joungho Kim

Abstract In this chapter, we treat the power distribution networks (PDNs) in TSV and interposer-based 3D ICs. First, we introduce the composition of the PDNs and the conventional design methodology of the PDNs in the frequency domain. For the design of the PDNs, we propose the modeling method for the PDNs in TSV and interposer-based 3D ICs based on a segmentation method. By using the models of the PDNs, we estimate and analyze the PDN impedance in TSV and interposer-based 3D ICs in the frequency domain with respect to the variations in the main design issues for the PDNs such as the size of grid-type PDNs, the number of power/ground (P/G) TSVs, and the capacitance of the on-chip decoupling capacitors (on-chip decaps).

Keywords Power distribution network (PDN) · Grid-type PDN · Power/ground through silicon via (P/G TSV) · TSV-based stacked grid-type PDN · Segmentation method · Conformal mapping method · Phenomenological loss equivalence method (PEM)

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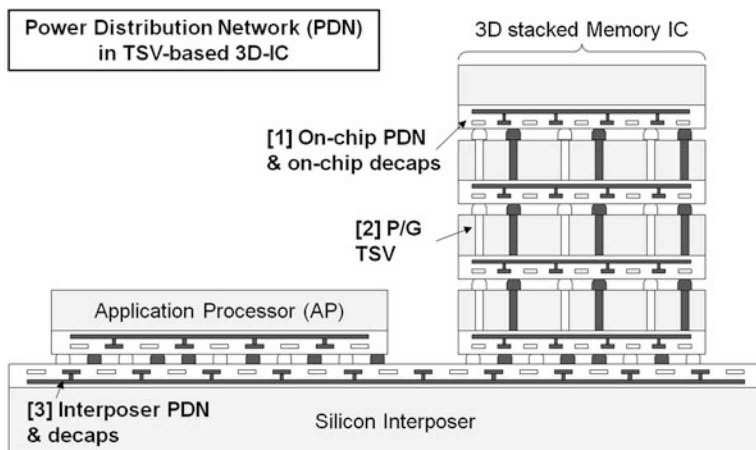


Fig. 6.1 The cross-sectional view of the power distribution network (PDN) in a TSV-based 3D-IC

6.1 Introduction

Recently, the realization of high-speed integrated-circuit systems with wider bandwidths, smaller form factors, and better electrical performance has been a continual challenge. TSV and interposer-based 3D ICs have attracted considerable attention as an ultimate solution to realize these high-speed integrated circuit systems [1–4]. The demand for high memory capacity caused by the increase in video content has fueled the use of TSVs [5] as the vertical interconnection between memory components to realize 3D stacked memory ICs. TSVs result in good electrical performance, smaller form factors, and wider bandwidths, having a much shorter interconnection length and a higher interconnection density compared to the wire bonds used in 2D-SiPs. Therefore, many of the memory ICs that have been fabricated are TSV-based 3D ICs.

Additionally, with the increase in the number of I/O drivers in 3D ICs, the number of interconnections between ICs has also dramatically increased. To make the I/O signals transferable to other ICs, interposers are most commonly used [6].

In this chapter, we focus on the power distribution network in 3D ICs, as shown in Fig. 6.1. We focus especially on the modeling and analysis of the power distribution network in the frequency domain by estimating and analyzing the PDN impedance.

6.1.1 Power Distribution Network in TSV and Interposer-Based 3D ICs

Power delivery has been a major concern in high-speed integrated systems. In particular, with the appearance of TSV and interposer-based 3D ICs, PDNs for the

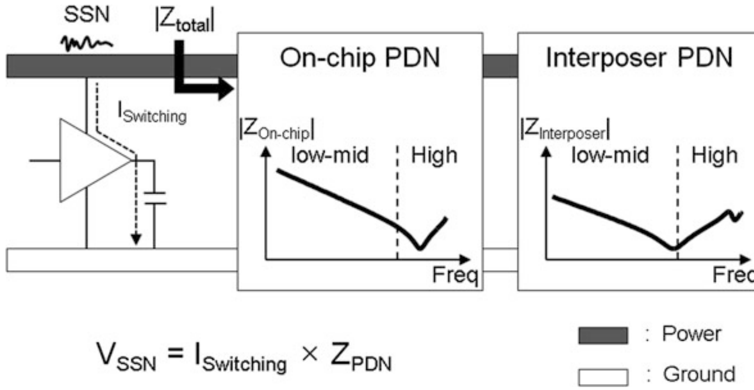


Fig. 6.2 Simultaneous switching noise (SSN) generation on the TSV and interposer-based 3D IC

power delivery are critically entangled and complicated. Additionally, with the increase in the number of I/O circuits for wider bandwidths, the current required for circuit operation is also critically increased. The increase in the switching current that occurs during the switching of the transistors together with the complexity of PDNs have caused significant noise on PDNs, which is called simultaneous switching noise (SSN) [7–10]. This noise can cause problems such as instability of the power supply and timing jitter. Therefore, the design and validation of PDNs in 3D ICs to supply clean power to circuits have become increasingly challenging.

In the 3D-IC shown in Fig. 6.1, the PDN plays a role in the power delivery to circuits in 3D ICs. The PDN consists of different types of PDNs, such as on-chip PDNs and an interposer PDN. These PDNs are hierarchically connected to each other by the power/ground (P/G) TSVs and P/G bumps. Compared to PDNs in 2D-SiPs in the previous package generation, new characteristics are observed because of the stacking of several on-chip PDNs and an interposer PDN.

In the next section, we study the structure and role of the different types of PDNs and decoupling capacitors. The reason we focus on these PDNs is related to their PDN impedance. The switching current flows through the PDNs during the circuit operation. At this time, the SSN is generated on the PDNs because the current is multiplied by the impedance of the PDNs ($V_{SSN} = I_{Switching} \times Z_{PDN}$), as shown in Fig. 6.2. Therefore, to reduce SSN, the design of the PDNs in 3D ICs is very important. For the design, we focus on the estimation and analysis of the PDN impedance based on the PDN model in the frequency domain. The modeling and analysis of the PDNs in TSV and interposer-based 3D ICs are studied in Sects. 6.2 and 6.3, respectively.

6.1.2 *Different Types of PDNs and Decoupling Capacitors in TSV and Interposer-Based 3D ICs*

6.1.2.1 On-Chip PDN

For the 3D ICs shown in Fig. 6.1, including an application processor and a 3D stacked memory IC, the PDN mainly consists of several on-chip PDNs. Due to the metal-density rule of chip fabrication, the on-chip PDNs are grid-type on-chip PDNs, as shown in Fig. 6.3a. In the grid-type PDN, several power and ground lines are quite entangled.

As shown in Fig. 6.3b, a CMOS integrated circuit is embedded in the silicon substrate. The power for the circuit is supplied from the on-chip PDNs. The impedance of the on-chip PDN is mainly determined by its capacitance, inductance, and resistance, as shown in Fig. 6.3c.

6.1.2.2 Interposer PDN in a Silicon Interposer

The demand for wider bandwidths and multi-functionality has fueled the considerable increase in the number of I/O drivers in ICs. To support these I/O signals, TSVs and RDL lines in the interposer are most commonly used. Another important function of the interposer is to supply power to the ICs in the 3D ICs through the interposer PDN and P/G TSVs in the interposer. In many cases, the interposer is fabricated by the chip fabrication process. Due to the metal density rule of the chip fabrication process, the interposer PDN in the interposer is formed as a grid-type PDN like an on-chip PDN.

The biggest difference between the on-chip PDN and the interposer PDN is their PDN size, as shown in Fig. 6.4b. Due to the larger-size of the interposer PDN, the interposer PDN has different impedance characteristics compared to the on-chip PDN, as shown in Fig. 6.5. The capacitance and inductance of the interposer PDN are higher than those of the on-chip PDN due to the larger size of the interposer PDN. Additionally, a mode resonance occurs on the interposer PDN because of its size. The mode resonance occurs due to the standing wave phenomenon in the interposer PDN. The boundary condition of the PDN is an open state. As the frequency increases, a standing wave will be formed in the interposer PDN. Due to the standing wave, an impedance peak is generated on the interposer PDN. As shown in Fig. 6.5, the mode-resonance peak appears in the PDN impedance that is observed at the port where the high impedance is generated on the standing wave.

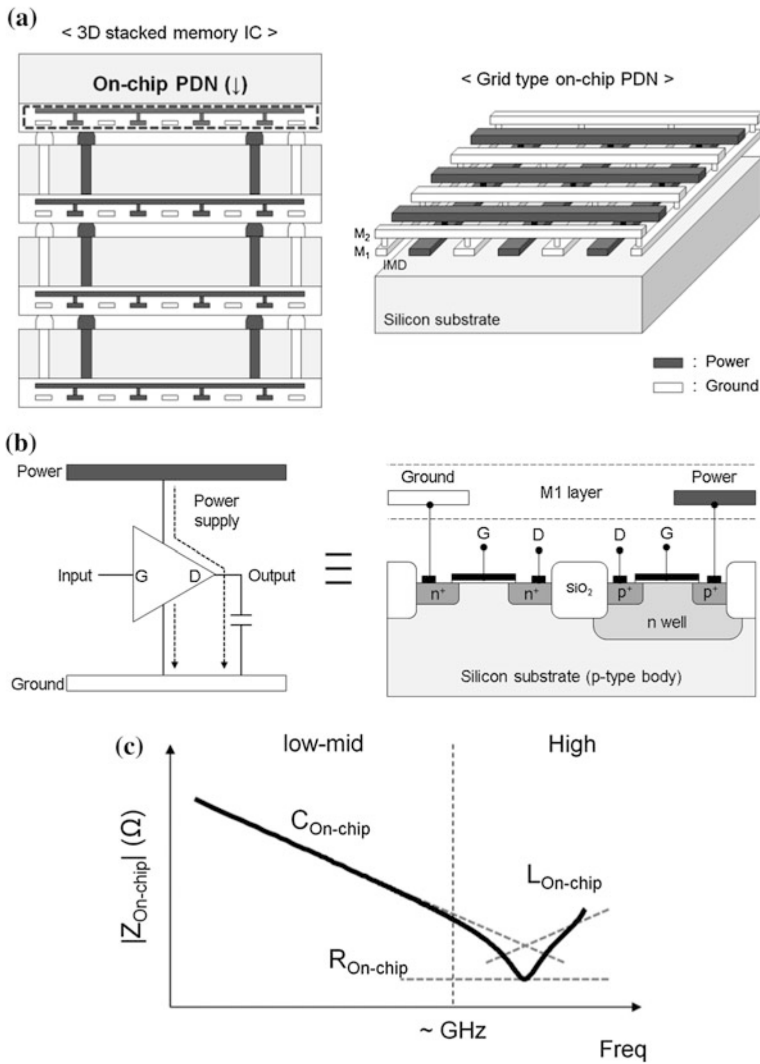


Fig. 6.3 **a** The cross-sectional view of the stacked on-chip PDNs in a 3D stacked memory IC. The on-chip PDNs are the grid-type on-chip PDNs. **b** A cross-sectional diagram of a CMOS integrated circuit. During the circuit operation, the power for the circuit is supplied from the on-chip PDNs. **c** The typical impedance of the on-chip PDN is determined by its capacitance, inductance, and resistance

6.1.2.3 Power/Ground (P/G) TSV and P/G Bump

A TSV is the structure used to form the vertical interconnection between ICs stacked vertically. Through TSV technology, the length of the interconnection between ICs is remarkably reduced. The use of TSV technology results in better

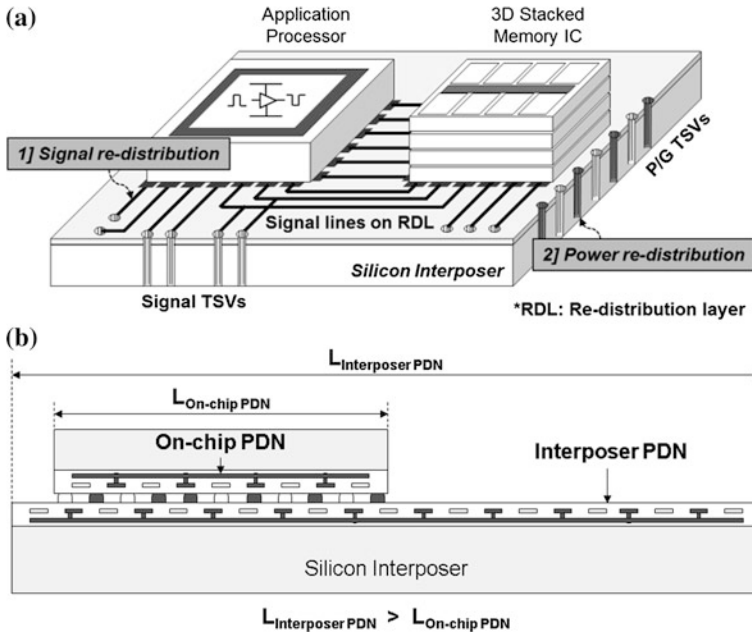


Fig. 6.4 **a** An interposer for a 3D IC with TSVs. The interposers play important roles in the distribution of signals and power to the circuits within the 3D ICs. **b** The size of the interposer PDN ($L_{\text{Interposer PDN}}$) is larger than that of the on-chip PDN ($L_{\text{On-chip PDN}}$) ($L_{\text{Interposer PDN}} > L_{\text{On-chip PDN}}$)

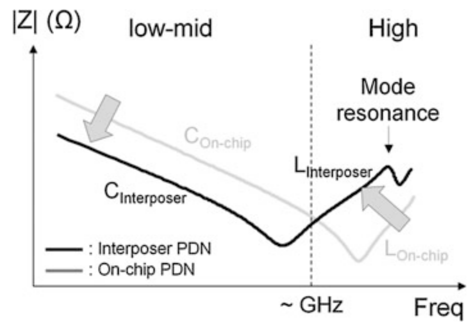


Fig. 6.5 The difference in the impedance curves between the interposer PDN and the on-chip PDN. The capacitance and inductance of the interposer PDN are higher than those of the on-chip PDN due to the larger size of the interposer PDN. Additionally, a mode resonance is generated on the interposer PDN

electrical performance and smaller form factors. As shown in Fig. 6.6, the metal vias penetrate through the silicon substrate. Due to the leakage current caused by the conductivity of the silicon substrate, a power/ground short can happen if there is no insulator material such as SiO_2. To prevent the power/ground short, the

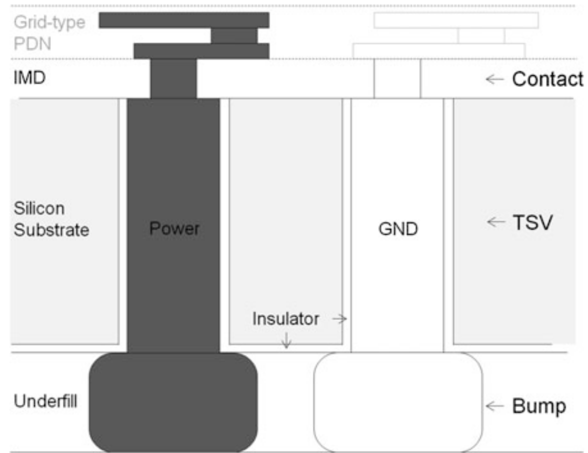


Fig. 6.6 The cross-sectional view of a P/G TSV pair. The P/G TSVs play a role in the connection between the *upper* on-chip PDN and *lower* on-chip PDN in 3D stacked on-chip PDNs

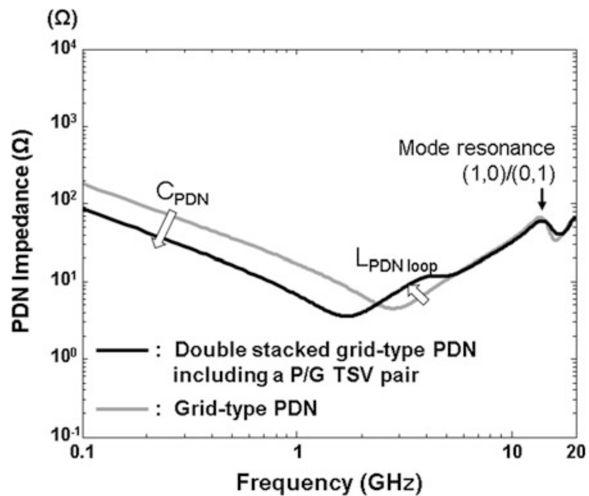


Fig. 6.7 The impedance curves of the double stacked grid-type PDN including a P/G TSV pair and grid-type PDN

power and ground TSVs are shielded by the insulator material such as SiO_2. The on-chip PDN is connected to the P/G TSVs by the contacts in the inter-metal dielectric (IMD). The bumps in the underfill material have a role in connecting the P/G TSVs with a lower-level PDN.

When P/G TSVs connect grid-type PDNs such as on-chip PDNs and interposer PDNs placed vertically, different impedance characteristics are revealed compared to those of a grid-type PDN by itself, as shown in Fig. 6.7. Compared to the impedance of a grid-type PDN, the capacitance and inductance of the stacked-grid-type PDN are increased because of the increased sizes of the PDN and of the PDN loop.

6.1.2.4 On-Chip Decoupling Capacitor (On-Chip Decap)

When we design the on-chip PDN, on-chip decoupling capacitors (on-chip decaps) cannot be omitted because of their significant role in supplying charge. Chip-technology development has caused an increase in the circuit densities and the switching speeds. These increases translate to an increase in the required current. To supply the required charges to circuits nearby, many on-chip decaps are embedded in on-chip PDNs, as shown in Fig. 6.8a.

From the frequency domain perspective, when on-chip decaps are embedded in on-chip PDNs, the PDN impedances are critically reduced by the increased capacitance caused by the on-chip decaps. This means the current required for the circuit operation can easily flow to the circuits. Therefore, it is necessary to include on-chip decaps in the on-chip PDN.

6.1.3 Simultaneous Switching Noise

During operation of core circuits, noises are generated on the PDNs. We call these noises simultaneous switching noises (SSNs). For the circuit operation, charges are supplied to circuits in the form of current. While the current flows to circuits through PDNs, the current sees the PDN impedance. Because of the current and PDN impedance, SSNs are generated on the PDNs, as shown in Fig. 6.9. The generated SSNs can critically degrade the stability of the power supply and cause timing jitter and EMI. Therefore, it is important to reduce the SSNs. Because the SSN is closely related to the PDN impedance, it is necessary to estimate and analyze the PDN impedance for the reduction of the SSN.

6.1.4 Design of PDNs in TSV-Based 3D ICs in the Frequency Domain

6.1.4.1 Impedance Analysis

The pre-estimation of the SSN is an important consideration in designing PDNs because of the negative effect of SSN on the system performance. For the estimation of SSN, the impedance of the PDN should first be estimated, because the PDN impedance is necessary to determine the SSN. Frequency analysis during the impedance estimation of the PDN enables engineers to estimate and understand all the resonance peaks in the PDN impedance that result in the critical SSNs. The estimation of the anti-resonance peaks which have high impedances is especially important. In the frequency domain, when the current spectrum coincides with the anti-resonance peaks, the critical SSNs are generated at the specific frequencies

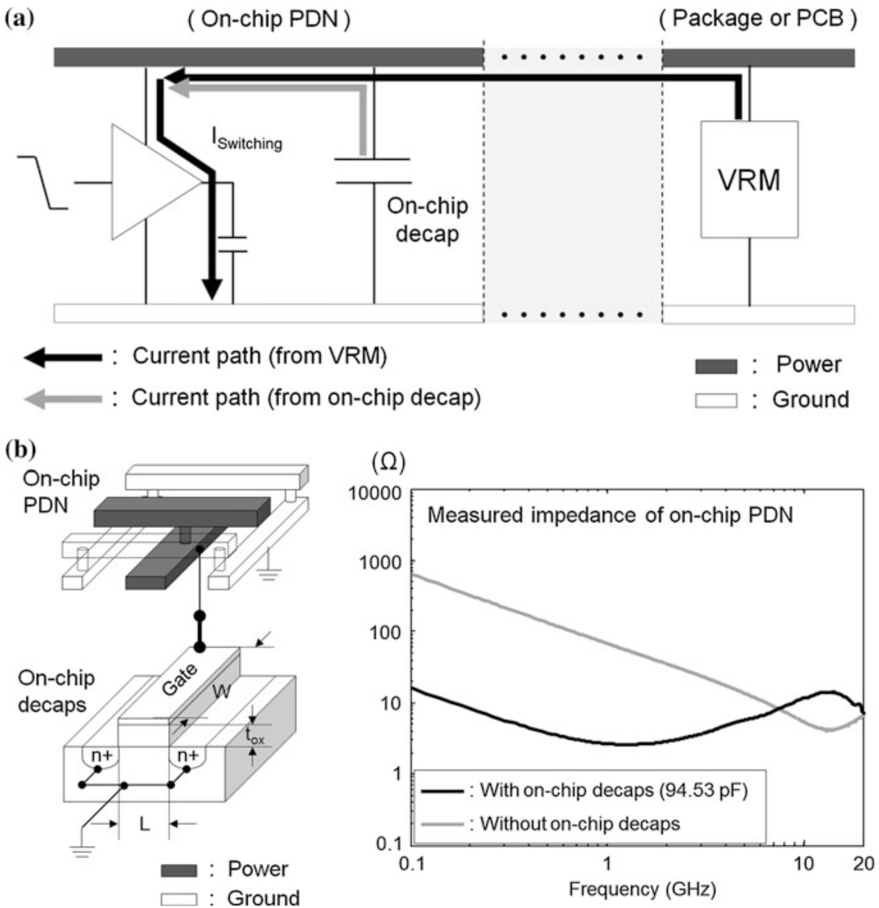


Fig. 6.8 **a** By embedding the on-chip decaps into the on-chip PDN, the required charge for the circuit operation is quickly transferred from the on-chip decaps. **b** The structure of the on-chip decaps. The on-chip decap uses the capacitance between the gate and the induced channel. When the on-chip decaps are embedded in the on-chip PDN, the PDN impedance is dramatically reduced, especially in the low frequency range

corresponding to the peaks. Therefore, PDN designers try to design PDNs by avoiding coincidence of the anti-resonance peaks and the critical current spectrum with high amplitude.

6.1.4.2 Determination of the Target Impedance

During the PDN design in the frequency domain, the target impedance is used. The target impedance is the impedance that satisfies the allowed noise level of the

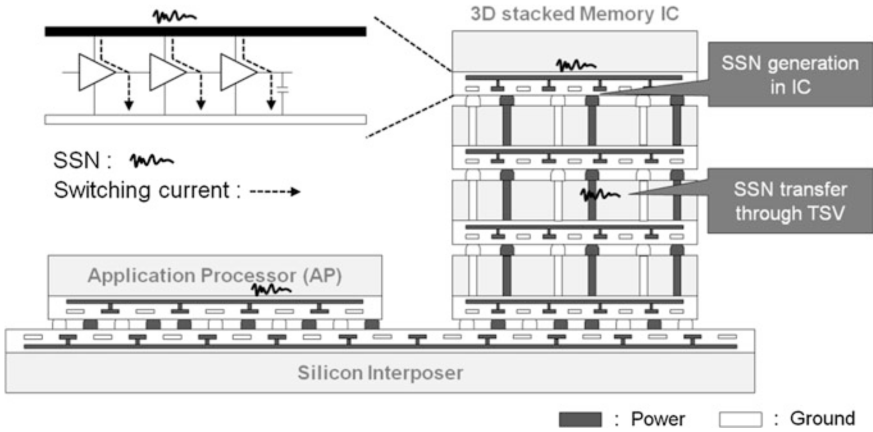


Fig. 6.9 SSN generation in 3D ICs. When the circuits in 3D ICs are operating, the switching currents flow through the PDNs in 3D ICs. At the same time, SSNs are generated on the PDNs

PDNs. The target impedance is usually used in determining the structures and sizes of the PDNs and the required capacitances obtained from decaps. The target impedance concept we usually use is based on Ohm's law. The target impedance (Z_T) is calculated by using the supply voltage, the allowed ripple (%), the activity factor (0–1), and the maximum current in Eq. (6.1) [11].

$$Z_T = \frac{Vdd \times allowed\ ripple}{activity\ factor \times I_{max}} \tag{6.1}$$

6.1.4.3 Design of PDNs in the Frequency Domain

The PDN design is usually preceded by the estimation and analysis of PDN impedance in the frequency domain. As shown in Fig. 6.10, the target impedance is a reference for the PDN design. The main purpose of the PDN design in the frequency domain is to reduce the PDN impedance to a value less than the target impedance. Additionally, the key guiding design principle of the PDN is to move the anti-resonance peak of the PDN away from the frequency at which the current spectrum has high amplitude. Based on these conventional PDN design-guides, we can design the PDN in the frequency domain. In Fig. 6.10, the PDN impedance is represented for a conventional 2D SiP that connects on on-chip PDN to a package PDN through wire-bonding. To reduce the PDN impedance of the 2D SiP, a SMD-type decap on a package PDN and an on-chip decap are used to reduce the PDN impedance and move the anti-resonance peak to the frequency at which the current spectrum has a low amplitude. In the following sections, through the estimation and analysis of the PDN impedance in the TSV and interposer-based 3D IC, we will understand the characteristics of the PDN impedance.

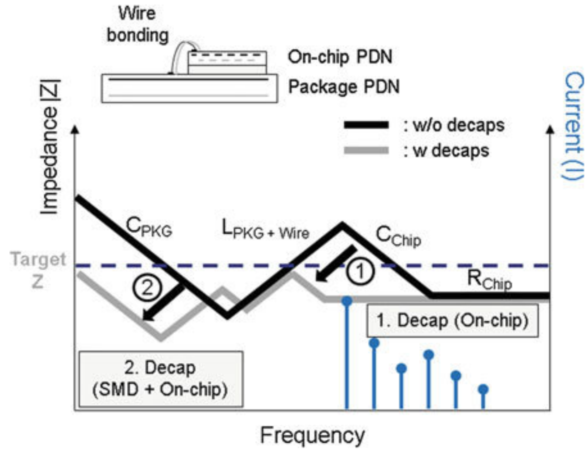


Fig. 6.10 The PDN impedance of a conventional 2D SiP. To reduce the PDN impedance in the 2D SiP, the SMD-type decap on a package PDN and an on-chip decap are used to reduce the PDN impedance and to avoid the high amplitude current spectrum

6.2 Modeling of PDNs in TSV-Based 3D ICs

6.2.1 Introduction

In general, to estimate the impedance of PDNs, 2.5D and 3D EM simulators such as SIwave (Ansoft), HFSS (Ansoft), and CST MWS are mainly used. However, it is difficult for these EM simulators to estimate the impedance of the PDNs in TSV-based 3D ICs because of their high aspect ratio and embedded MOS capacitors [12]. For the fast and effective estimation of the PDN impedance, PDN models have been used. In the modeling of PDNs, the RLGC-lumped model and an equation-based model are conventionally used. For the RLGC-lumped model, the lumped elements are extracted from the physics-based scalable equations or from an EM simulator such as Q3D extractor (Ansoft). The advantage of the RLGC-lumped model is that it provides us physical insight into the characteristics of the PDN impedance. However, a more complicated PDN structure requires a more complicated RLGC-lumped model such as the distributed RLGC-lumped model. Additionally, as the target frequency increases, the lumped elements have to include frequency-dependent characteristics to express the PDN's high frequency characteristics. For simple and ideal PDN structures, the PDN impedances can be estimated from an equation-based model based on the electromagnetic theory. This equation-based model, such as the cavity model [13], is highly accurate. However, it is difficult for this model to provide physical insight into the PDN impedances. Additionally, because the equation-based model can only be applied to simple and ideal PDNs, the model is rarely applied to overall PDN cases.

The PDNs in conventional TSV-based 3D ICs consist of the on-chip PDN, the interposer PDN, and the P/G TSVs and bumps. Additionally, to immediately supply the additional charges to the PDNs, decoupling capacitors such as on-chip

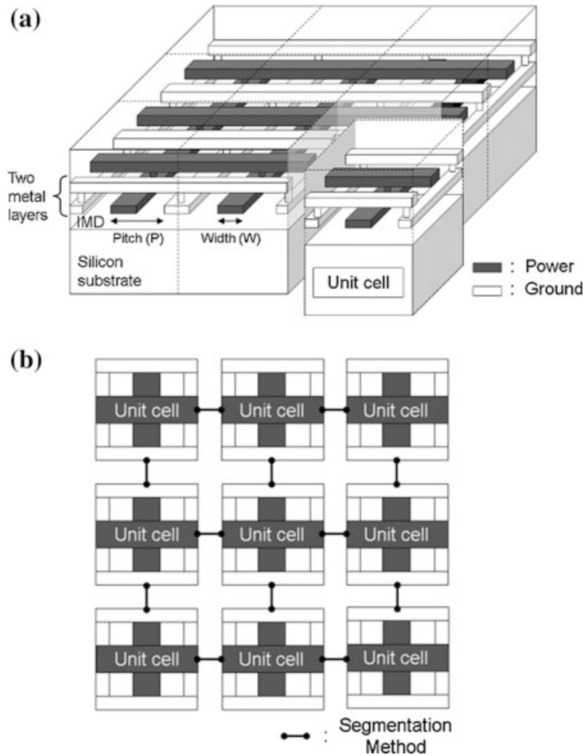


Fig. 6.11 **a** The on-chip and interposer PDNs on the silicon substrates are fabricated as grid-type PDNs because of the metal density rule of chip fabrication. In the on-chip and interposer PDNs, certain repetitive structures exist. We call this structure the unit cell of the on-chip and interposer PDNs [12]. **b** By incorporating these unit cells using a segmentation method, we can model the on-chip and interposer PDNs [12] © 2012 IEEE

decaps are commonly used. In this chapter, we introduce the modeling method for the grid-type PDNs such as the on-chip and interposer PDNs. The grid-type PDNs are modeled with distributed RLGC-lumped models based on the scalable equations with physical design parameters. After modeling these grid-type PDNs, the PDNs in TSV-based 3D ICs are modeled by connecting the models of the grid-type PDN and the P/G TSVs and bumps in a hierarchical order using a segmentation method.

In the next section, we introduce the modeling of grid-type PDNs for the on-chip and interposer PDNs.

6.2.2 Modeling of Grid-Type PDNs for On-Chip and Interposer PDNs

A grid-type PDN, shown in Fig. 6.11a, is commonly used in a digital IC and in a silicon interposer because of the metal density rule of the chip fabrication process. The only difference between the on-chip and interposer PDNs is their PDN size. Because the interposer plays a role in the stanchion of the ICs stacked on the

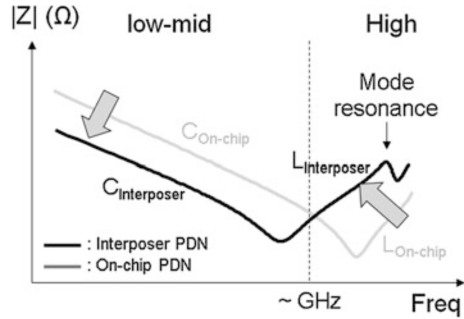


Fig. 6.12 The difference in the impedance curves between the on-chip and interposer PDNs

interposer, the size of the interposer is much larger than that of an IC. Additionally, to supply the power currents to the ICs, the size of the interposer PDN should also be larger than that of the on-chip PDN. Because of the difference in the PDN sizes, the impedance characteristics of the interposer PDN differ from those of the on-chip PDN, as shown in Fig. 6.12.

The capacitance and inductance of the interposer PDN are higher than those of the on-chip PDN because of the larger size of the interposer PDN. Additionally, a mode resonance occurs on the interposer PDN because of its size. The mode resonance results from the standing wave phenomenon in the interposer PDN. As the frequency increases, the standing wave will be formed in the interposer PDN. Because of the standing wave, the impedance peak is generated on the interposer PDN.

To accurately estimate the impedance of the grid-type PDN for the interposer PDN and for the on-chip PDN based on the PDN model, we propose the distributed RLGC-lumped model for a grid-type PDN. For the PDN modeling, we use a conformal mapping method and a phenomenological loss equivalence method (PEM).

Additionally, for rapid estimation, we use a segmentation method to connect the distributed RLGC-lumped model to form the whole grid-type PDN.

Prior to modeling the grid-type PDN, we assume that the grid-type PDN is composed of two metal layers over a silicon substrate. It is also assumed that the metal width and the pitch between a power line and the adjacent ground lines are fixed. Under these assumptions, the grid-type PDN can be decomposed into certain repetitive PDN structures, named unit cells in Fig. 6.11a [12].

Once we have a model for the unit cell, the whole grid-type PDN can be modeled through the connection of the face-to-face ports of the adjacent unit cell models based on a segmentation method [14], as shown in Fig. 6.11b. The segmentation method is a well-known method for estimating the impedance of a complete PDN from decomposed PDNs, as shown in Fig. 6.13.

The impedance matrices of the PDN structures 1 and 2 are presented in Eqs. (6.2) and (6.3).

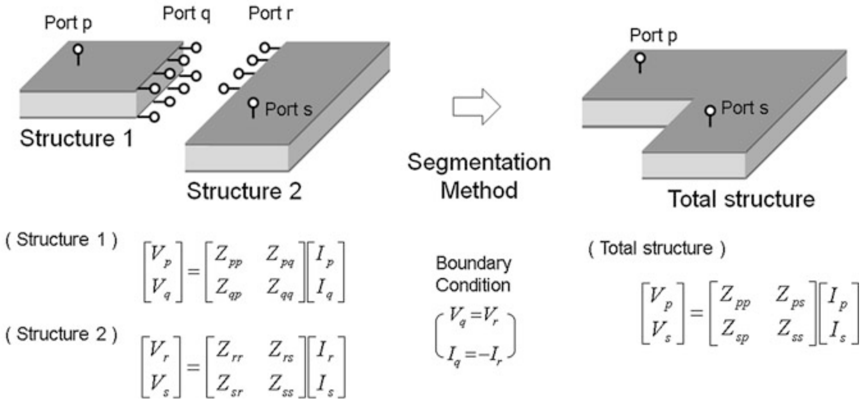


Fig. 6.13 The incorporation of decomposed structures based on a segmentation method. The segmentation method is a matrix calculation to calculate the impedance matrices of the total structure based on those of the decomposed structures

$$\begin{bmatrix} V_p \\ V_q \end{bmatrix} = \begin{bmatrix} Z_{pp} & Z_{pq} \\ Z_{qp} & Z_{qq} \end{bmatrix} \begin{bmatrix} I_p \\ I_q \end{bmatrix} \tag{6.2}$$

$$\begin{bmatrix} V_r \\ V_s \end{bmatrix} = \begin{bmatrix} Z_{rr} & Z_{rs} \\ Z_{sr} & Z_{ss} \end{bmatrix} \begin{bmatrix} I_r \\ I_s \end{bmatrix} \tag{6.3}$$

To compose the total PDN structure from PDN structures 1 and 2, we connect port q of PDN structure 1 to port r of PDN structure 2. The boundary conditions expressed in Eq. (6.4a and b) are used for the connection.

$$V_q = V_r \tag{6.4a}$$

$$I_q = -I_r \tag{6.4b}$$

Using these boundary conditions, the impedance properties of PDN structures 1 and 2 are integrated into the impedance properties of the total PDN structure as presented in Eq. (6.5) [14].

Consequently, the impedance matrix of the total structure can be derived by using the impedance matrices of the decomposed structures and the segmentation method.

$$\begin{bmatrix} \mathrm{V_p} \\ \mathrm{V_s} \end{bmatrix} = \begin{bmatrix} \mathrm{Z_{pp}} - \mathrm{Z_{pq}}(\mathrm{Z_{qq}} + \mathrm{Z_{ss}})^{-1}\mathrm{Z_{pp}} & \mathrm{Z_{pq}}(\mathrm{Z_{qq}} + \mathrm{Z_{ss}})^{-1}\mathrm{Z_{sr}} \\ \mathrm{Z_{rs}}(\mathrm{Z_{qq}} + \mathrm{Z_{ss}})^{-1}\mathrm{Z_{qp}} & \mathrm{Z_{rr}} - \mathrm{Z_{rs}}(\mathrm{Z_{qq}} + \mathrm{Z_{ss}})^{-1}\mathrm{Z_{sr}} \end{bmatrix} \begin{bmatrix} \mathrm{I_p} \\ \mathrm{I_s} \end{bmatrix} \tag{6.5}$$

Prior to the connection of unit cells based on a segmentation method, we must model the unit cell. To model the unit cell, we split the unit cell into several transmission line (TL) sections in the x and y directions, as shown in Fig. 6.14.

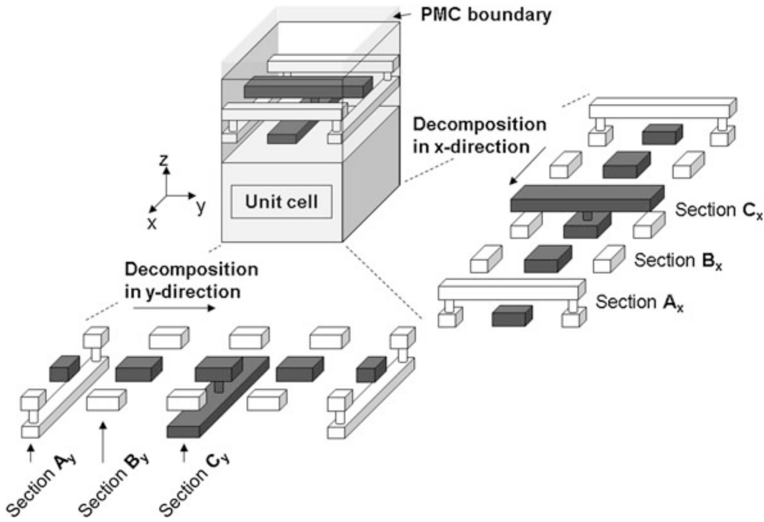


Fig. 6.14 The decomposition of a unit cell in the x and y-directions into the decomposed TL sections [23]. (*x-direction* 1. Section A_x, 2. Section B_x, and 3. Section C_x, *y-direction* 1. Section A_y, 2. Section B_y, and 3. Section C_y) © 2013 IEEE

In the next step, the procedures for modeling sections A_x, B_x, and C_x in Fig. 6.14 are introduced. In this step, the effect of the silicon substrate is included in the model of the unit cell. We do not address the procedures for modeling sections A_y, B_y, and C_y because of their similarity to sections A_x, B_x, and C_x.

In the next step, the TL sections are modeled as RLGC-lumped models. It is important to accurately model these sections because the PDN impedance is directly determined by the connections between these section models. This modeling method, which is based on structural decomposition, has the advantage that we can model the PDN seen by the wave as it moves in the PDN. As a result, the bandwidth and accuracy of the distributed RLGC-model is greater than those of other simple lumped models. Additionally, the mode resonance of the grid-type PDN can be estimated by this model. However, to model the grid-type PDN, thousands of TL sections should be connected to one another. As a result, when each TL section model contains a small modeling error, the modeling of the whole grid-type PDN can contain substantial errors. Therefore, accurate modeling of TL sections is extremely important. Thus, a conformal mapping method and a PEM are used mainly to accurately extract the capacitance and conductance (C and G) and resistance and inductance (R and L) of the TL sections, respectively.

A conformal mapping method is an angle-preserving method. For the capacitance estimation, the Schwarz-Christoffel transformation, which is a conformal transformation to transform the upper half-plane onto the interior of a simple polygon [15], is used. Through the Schwarz-Christoffel transformation, we can estimate the capacitance of the TL sections given their PMC boundary condition by transforming the partitions of the TL sections into a parallel plate [15]. Then,

we can easily estimate their capacitances by the capacitance equation for two parallel plates separated by a dielectric material.

Electromagnetic fields penetrate into the imperfect conductors as the fields move along the TL sections. The field penetrations result in resistance (R) and internal inductance (L_{int}). Because of the shallow penetration caused by the skin effect, the resistance and inductance are increased and decreased, respectively, as the frequency increases [16]. The internal impedance variation, which is represented as the variation of the resistance and internal inductance, changes the transmission characteristics, such as the characteristic impedance and complex propagation constant. The impedance of a grid-type PDN is intrinsically determined by these transmission characteristics of the TL sections that form the grid-type PDN. The mode resonance of the grid-type PDN is directly associated with the propagation constants of the TL sections because the wavelength that determines the mode generation is determined by the propagation constants [17]. Therefore, it is important to include the frequency-dependent variation in the resistance and inductance in the section models. Accordingly, a PEM is used to model the frequency dependent resistance and inductance of the TL sections.

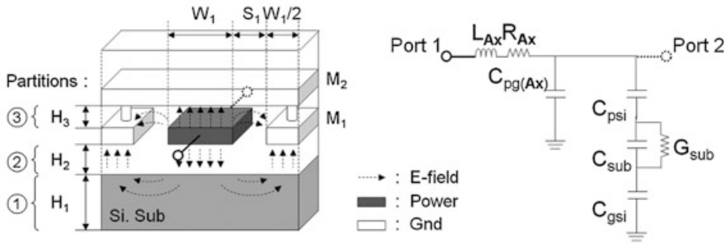
To calculate the internal impedance of the TL sections, the current distribution must be known throughout the entire conductor. The purpose of the PEM is to phenomenologically transform the TL sections into single equivalent strips and to then analyze the equivalent strips using the surface impedance for a finite conductor thickness [16]. The internal impedance can be calculated using the equivalent strip width ($W_e = 1/G$), the equivalent thickness ($t_e = AG$), and the surface impedance of a flat plane conductor with a finite thickness, as represented in Eq. (6.6).

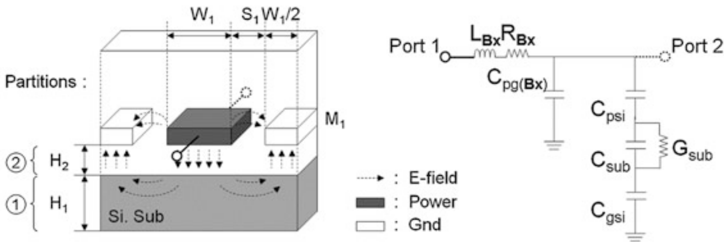
$$Z_i = R + j\omega L_i = \frac{Z_s}{W_e}\coth\left(\frac{1+j}{\delta}t_e\right) = Z_s\, G coth\left(\frac{1+j}{\delta}AG\right) \tag{6.6}$$

In this equation, Z_s is the surface impedance of the conductor medium. G and A are the geometric factor and cross-sectional area of a TL section, respectively. The usefulness of a PEM is due to its simple calculation of Z_s, G, and A. Based on the internal impedance (Z_i) obtained from a PEM, we can calculate the frequency-dependent resistance (R) and the internal inductance (L_i) caused by the current distribution in the metal of the TL sections.

By applying a conformal mapping method and a PEM to extract the RLGC components of the TL sections, all the TL sections shown in Fig. 6.15 can be modeled as RLGC-lumped models. In this paper, because of the similarity in the modeling method for the TL sections, we only focus on the modeling of sections such as A_x, B_x, and C_x, as shown in Fig. 6.15.

The structure of section A_x shown in Fig. 6.15a is a supported coplanar waveguide. All RLGC values obtained from the following equations are given as values per unit length. To model section A_x, we first calculate the air-filled capacitance ($C_{Ax}^{air-filled}$) of section A_x. For the condition that the space (S_1) is wide





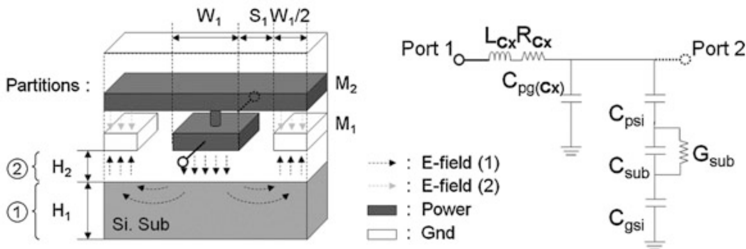


Fig. 6.15 **a** The structure and RLGC-lumped model of section A_x [23]. **b** The structure and RLGC-lumped model of section B_x [23]. **c** The structure and RLGC-lumped model of section C_x [23] © 2013 IEEE

and $W_1 \gg H_{ILD}$, the supported coplanar waveguide can be considered to be a micro-strip line [15]. Therefore, the air-filled capacitance ($C_{Ax}^{air-filled}$) of section A_x is calculated from Eq. (6.7) [15], which is the equation for the capacitance caused by all faces (top face, bottom face, and two side faces) of the micro-strip line obtained from the conformal mapping-based empirical approach (Table 6.1).

$$C_{Ax}^{air-filled} = \varepsilon_0 \left(\frac{W_1}{H_{IMD}} + 0.77 + 1.06 \left(\frac{W_1}{H_{IMD}} \right)^{0.25} + 1.06 \left(\frac{T_1}{H_{IMD}} \right)^{0.5} \right) \tag{6.7}$$

Table 6.1 Model parameters with their symbols for a proposed scalable electrical model of an interposer PDN, which includes structural and material parameters

	Parameter	Description
Grid-type PDN	W_1	Metal width of M_1 metal
	W_2	Metal width of M_2 metal
	S_1	Space between the power line and the ground line on the M_1 metal
	S_2	Space between the power line and the ground line on the M_2 metal
	P_1	Pitch between the power line and the ground line on the M_1 metal
	P_2	Pitch between the power line and the ground line on the M_2 metal
	H_{ILD}	Height of the ILD layer between the M_1 metal and the silicon substrate
	H_{IMD}	Height of partition 3 between the M_2 metal and the M_1 metal
	T_1	Thickness of the M_1 metal
	T_2	Thickness of the M_2 metal
	ε_{Sub}	Relative permittivity of the substrate
	ε_{ILD}	Relative permittivity of the ILD
	ε_{IMD}	Relative permittivity of the IMD
	σ_{Sub}	Conductivity of the substrate

The next step is the extraction of the external inductance (L_{ext}). $L_{ext(Ax)}$ is calculated by Eq. (6.8) [18]. (c: speed of light ($c = 3 \times 10^8$ m/s))

$$L_{ext(Ax)} = \frac{1}{c^2 C_{Ax}^{air-filled}} \tag{6.8}$$

The third step is the extraction of the internal impedance (Z_i) based on a PEM. First, the geometric factor (G_{Ax}) of section A_x should be calculated. The geometric factor of section A_x can be obtained when we know the external inductance ($L_{ext(Ax)}$ (W_1, h_{IMD}, T_1)) of section A_x. The geometric factor represents the surface current distribution of section A_x. Because the external magnetic flux is proportional to the surface current density, the increment of the external inductance is associated with the distribution of the current density on section A_x. The geometric factor is obtained from the derivative of the external inductance and some algebraic manipulations [16] based on the recession of the conducting walls shown in Fig. 6.16b, as presented in Eq. (6.9).

$$\begin{aligned} G_{Ax} &= \frac{1}{\mu}\sum_m \left(\frac{\partial L_{ext(Ax)}(W_1, H_{IMD}, T_1)}{\partial n_m}\right) \\ &= \frac{1}{\mu}\left[\left(\frac{\partial L_{ext(Ax)}}{\partial H_{IMD}}\right)_{(1)} + \left(-\frac{\partial L_{ext(Ax)}}{\partial T_1}\right)_{(2)} + \left(\frac{\partial L_{ext(Ax)}}{\partial H_{IMD}} - \frac{\partial L_{ext(Ax)}}{\partial T_1}\right)_{(3)} + \left(-2\frac{\partial L_{ext(Ax)}}{\partial W_1}\right)_{(4)}\right] \end{aligned} \tag{6.9}$$

In Eq. (6.9), the number 'm' is the number of metal faces ((1) (2) (3), and (4) in Fig. 6.16b) in which we consider the shallow penetration.

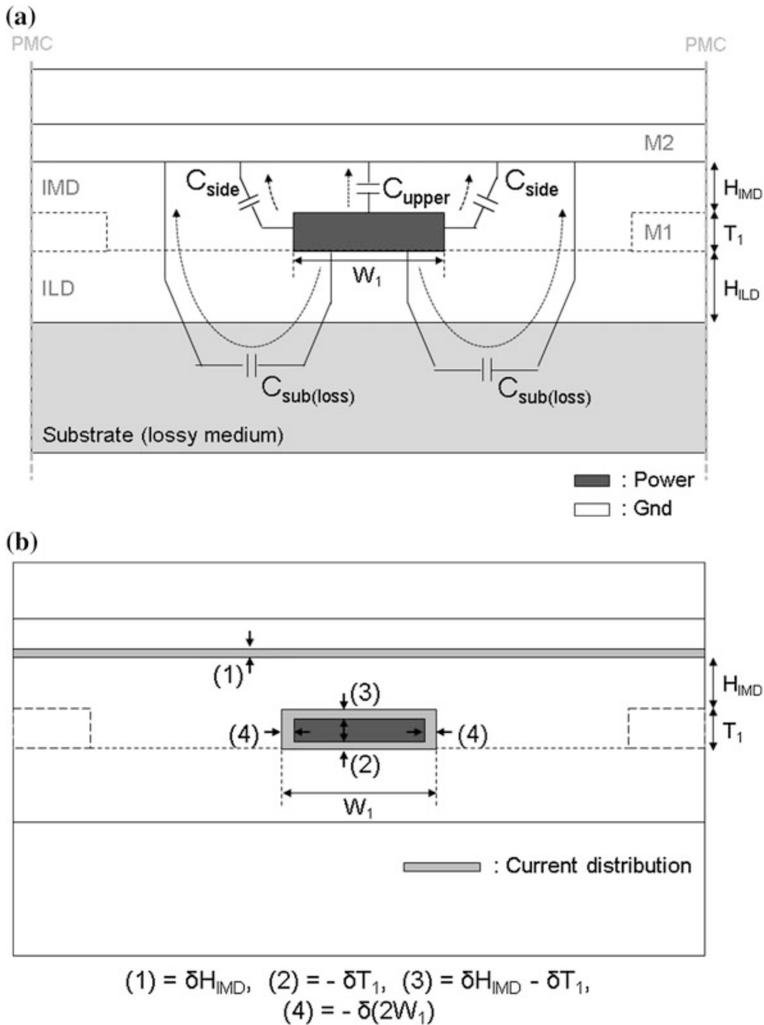


Fig. 6.16 **a** All capacitances (C_{upper}, C_{side}, and C_{sub}) are shown according to the position of the electric field generated in section A_x [23]. **b** The current distribution caused by the field penetration and physical parameter variations according to the current distribution [23] © 2013 IEEE

By using this geometric factor, we can calculate the internal impedance ($Z_{i,pwr}$ and $Z_{i,gnd}$) of the power and ground lines of section A_x by using Eq. (6.10) [18].

$$Z_{i,pwr} = Z_s G_{Ax} coth\left(\frac{1+j}{\delta} A_{pwr} G_{Ax}\right)$$
$$Z_{i,gnd} = Z_s G_{Ax} coth\left(\frac{1+j}{\delta} A_{gnd} G_{Ax}\right)$$

where,

$$
\begin{array}{c}
Z_s = (1+j)\frac{1}{\sigma\delta} \\
A_{pwr} = W_1 T_1, \qquad A_{gnd} = 10 H_{IMD} T_2
\end{array}
\tag{6.10}
$$

In $Z_{i,gnd}$ of Eq. (6.10), we use 10 H_{IMD} as the width of the return-current density because the return-current predominantly flows in the area A_{gnd} (= 10 $H_{IMD}T_2$). From these internal impedances, we can calculate the resistance (R) and internal inductance (L_i) of section A_x, as presented in Eq. (6.11) [18].

$$
R = Re\left(Z_{i,pwr} + Z_{i,gnd}\right), \qquad L_i = \frac{1}{\omega} Im\left(Z_{i,pwr} + Z_{i,gnd}\right) \tag{6.11}
$$

Finally, to calculate the capacitance of section A_x, we split the capacitance into sub-capacitances, such as C_{upper}, C_{side}, and $C_{sub\ (loss)}$, as shown in Fig. 6.16a, because this separation is necessary to extract the substrate effect, such as $C_{sub\ (loss)}$. All sub-capacitances are calculated based on a conformal mapping method. C_{upper} is the capacitance caused by the electric field between the top of the M_1 metal and the bottom of the M_2 metal, as presented in Eq. (6.12) [19].

$$
C_{upper} = \varepsilon_0 \varepsilon_{IMD} \left(\frac{W_1}{H_{IMD}} + \frac{4ln(2)}{\pi} \right) \tag{6.12}
$$

C_{side} is the capacitance caused by the electric field between the side of the M_1 metal and the bottom of the M_2 metal, as presented in Eq. (6.13) [19].

$$
C_{side} = \frac{\varepsilon_0 \varepsilon_{IMD}}{2} M(k(T_1, H_{IMD})) \tag{6.13}
$$

In this equation, k is a parameter related to the geometrical dimensions T_1 and H_{IMD}. M is a function of k. The equations for calculating these parameters have already been introduced in [19].

As shown in Fig. 6.16a, the electric field between the bottoms of the M_1 metal and the M_2 metal penetrates the substrate. When the substrate is a loss-inducing medium, such as a silicon substrate, it is necessary to model the dielectric loss of the substrate. To model the dielectric loss of the substrate, we must model the capacitance generated within the substrate itself. The capacitance is calculated by using the effective dielectric constant, which includes the conductivity of the substrate.

The micro-strip line is a symmetrical structure. When we calculate the capacitance of the line, we assume that there is a PMC boundary on the center of the line. As shown in Fig. 6.17, the half structure of the micro-strip line can be transformed into parallel plates by Wheeler's transformation [20]. Through this transformation, we can easily calculate the capacitance of the micro-strip line by using the equation for calculating the capacitance between parallel plates. The capacitance caused by the electric field penetrating the IMD (shaded area in the

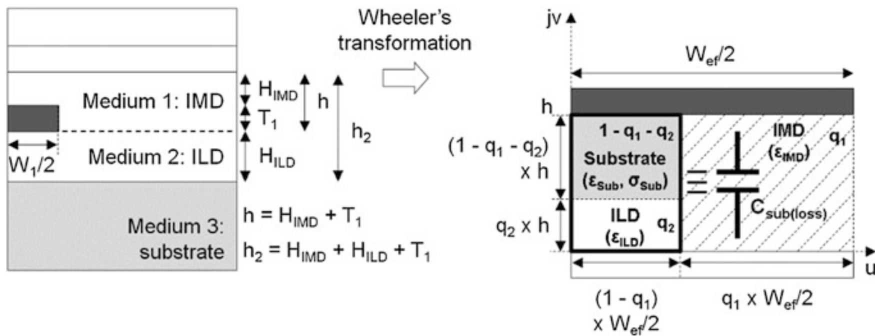


Fig. 6.17 Half of the micro-strip line is transformed into a parallel plate by Wheeler's transformation to calculate the capacitance $C_{sub\ (loss)}$ caused by the electric field penetrating the substrate [23] © 2013 IEEE

right figure of Fig. 6.17) is predominantly calculated as C_{upper} and C_{side}. To calculate $C_{sub\ (loss)}$, we focus on the capacitance in the bold box in the right figure of Fig. 6.17.

In the bold box, there are the two dielectric materials, the ILD and the substrate. The substrate material, such as the silicon, can have a high conductivity. In the case that one substrate is loss-free (ε_{ILD}) and the other is loss-including ($\varepsilon_{Sub} + \frac{\sigma_{Sub}}{j\varepsilon_0 \omega}$), the effective dielectric constant is calculated according to Eq. (6.14a–e) [21].

$$\tilde{\varepsilon}_{eff} = \varepsilon_{eff} + \frac{\Delta\varepsilon}{1 + j\omega\tau} \tag{6.14a}$$

$$q_{lossy} = \frac{(1 - q_1 - q_2)h}{q_2 h + (1 - q_1 - q_2)h} \tag{6.14b}$$

$$\varepsilon_{eff} = \frac{\varepsilon_{ILD}\varepsilon_{Sub}(1 + 2q_{lossy})}{q_{lossy}(\varepsilon_{ILD} + \varepsilon_{Sub}) + \varepsilon_{Sub}} \tag{6.14c}$$

$$\Delta\varepsilon = \frac{q_{lossy}\varepsilon_{ILD}\varepsilon_{eff}}{(1 + q_{lossy})\varepsilon_{Sub}} \tag{6.14d}$$

$$\tau = \frac{q_{lossy}(\varepsilon_{ILD} + \varepsilon_{Sub}) + \varepsilon_{Sub}}{(1 + q_{lossy})\sigma_{Sub}} \tag{6.14e}$$

In this equation, $\tilde{\varepsilon}_{eff}$ is the complex dielectric constant of the mixture and ε_{eff} is the effective dielectric constant at high frequencies. $\Delta\varepsilon$ and τ are the dielectric strength of the interfacial polarization and the relaxation time of the polarization, respectively. q_{lossy} is the filling factor of the substrate and is calculated as the ratio of the area of the substrate to the total area of the mixture. In Eq. (6.14b), there are

two filling factors q_1 and q_2, which are the filling factors of the IMD and the ILD, respectively. q_1 and q_2 are functions of W_1, h, and h_2.

Using the complex dielectric constant ($\tilde{\varepsilon}_{eff}$) of the mixture, we can calculate the capacitance ($C_{sub\,(loss)}$) using Eq. (6.15).

$$C_{sub\,(loss)} = \tilde{\varepsilon}_{eff} \frac{\frac{W_{eff}}{2}(1-q_1)}{h} \tag{6.15}$$

Finally, $C_{pg'}$ shown in the RLGC-lumped model of Fig. 6.15a is calculated from Eq. (6.16).

$$C'_{pg} = C_{upper} + 2C_{side} + 2C_{sub\,(loss)} \tag{6.16}$$

The structure of section B_x shown in Fig. 6.15b is a coplanar waveguide. We also follow the modeling steps of section A_x to model section B_x. First, we calculate the air-filled capacitance ($C_{Bx}^{air-filled}$) of section B_x. Because of the symmetry of section B_x along the horizontal and vertical directions, we can extract $C_{upper}^{air-filled}$ and $C_{side}^{air-filled}$ to calculate the air-filled capacitance ($C_{Bx}^{air-filled}$) of section B_x.

$C_{upper}^{air-filled}$ is the air-filled capacitance caused by the electric fields between the tops of the power and ground lines bounded by PMC in section B_x. The capacitance is calculated from Eq. (6.17a and b) [15].

$$k = cos(\frac{(P_1 - S_1)\pi}{2P_1}) \tag{6.17a}$$

$$C_{upper}^{air-filled} = \frac{\varepsilon_0}{2}\left(\frac{K(k')}{K(k)}\right) \tag{6.17b}$$

In these equations, $K(k)$ and $K(k')$ are the complete elliptic integral of the first type and its complement, respectively. k and k' are the elliptic modulus and complementary elliptic modulus, respectively. The relationship between k and k' is $k' = \sqrt{1 - k^2}$.

$C_{side}^{air-filled}$ is the air-filled capacitance caused by the electric fields between the sides of the power and ground lines in section B_x. The capacitance is calculated from Eq. (6.18).

$$C_{side}^{air-filled} = \varepsilon_0\left(\frac{T_1}{S_1}\right) \tag{6.18}$$

By using $C_{upper}^{air-filled}$ and $C_{side}^{air-filled}$, we can calculate the air-filled capacitance ($C_{Bx}^{air-filled}$) of section B_x according to Eq. (6.19).

$$C_{Bx}^{air-filled} = \frac{1}{\varepsilon_{IMD}} \left(4C_{upper}^{air-filled} + 2C_{side}^{air-filled}\right) \tag{6.19}$$

The external inductance ($L_{ext(Bx)}$) of section B_x is extracted in the same way using Eqs. (6.8) and (6.19).

The geometric factor of section B_x is obtained from the derivative of the external inductance ($L_{ext(Bx)}$), as presented in Eq. (6.20).

$$\begin{aligned} G_{Bx} &= \frac{1}{\mu} \sum_m \left(\frac{\partial L_{ext(Bx)}(T_1, S_1)}{\partial n_m} \right) \\ &= \frac{1}{\mu} \left[\left(-\frac{\partial L_{ext(Bx)}}{\partial T_1} \right)_{(1)} + \left(-\frac{\partial L_{ext(Bx)}}{\partial T_1} \right)_{(2)} + \left(\frac{\partial L_{ext(Bx)}}{\partial S_1} \right)_{(3)} + \left(\frac{\partial L_{ext(Bx)}}{\partial S_1} \right)_{(4)} \right] \end{aligned} \tag{6.20}$$

By using this geometric factor, we can calculate the internal impedance ($Z_{i,pwr}$ and $Z_{i,gnd}$) of the power and ground lines by using Eq. (6.21).

$$\begin{aligned} Z_{i,pwr} &= Z_s\left(= (1+j)\frac{1}{\sigma\delta} \right) G_{Bx} coth\left(\frac{1+j}{\delta} A_{pwr}(= W_1 T_1) G_{Bx} \right) \\ Z_{i,gnd} &= Z_s\left(= (1+j)\frac{1}{\sigma\delta} \right) G_{Bx} coth\left(\frac{1+j}{\delta} A_{gnd}\left(= \frac{W_1}{2} T_1\right) G_{Bx} \right) \end{aligned} \tag{6.21}$$

From these internal impedances, we can calculate the resistance (R) and internal inductance (L_i) of section B_x, as presented in Eq. (6.22).

$$R = Re\left(Z_{i,pwr} + Z_{i,gnd}\right), L_i = \frac{1}{\omega} Im\left(Z_{i,pwr} + Z_{i,gnd}\right) \tag{6.22}$$

Finally, to calculate the capacitance of section Bx, we split the capacitance into the sub-capacitances Cupper, Cside, Cpsi, Cgsi, and Csub (loss) shown in Fig. 6.18a.

To calculate Cupper, we calculate the capacitance ($C_{upper\,(IMD)}$) of the height HIMD2 according to Eq. (6.23a–c) [15].

$$\varsigma = \left(\frac{\frac{exp\left(\frac{P_2\pi}{2H_{IMD2}}\right)}{2} - 1}{\frac{exp\left(\frac{P_2\pi}{2H_{IMD2}}\right)}{2} + 1} \right)^2 \tag{6.23a}$$

$$k_1 = sn\left(\frac{S_2}{P_2} K(\varsigma), \varsigma \right) \tag{6.23b}$$

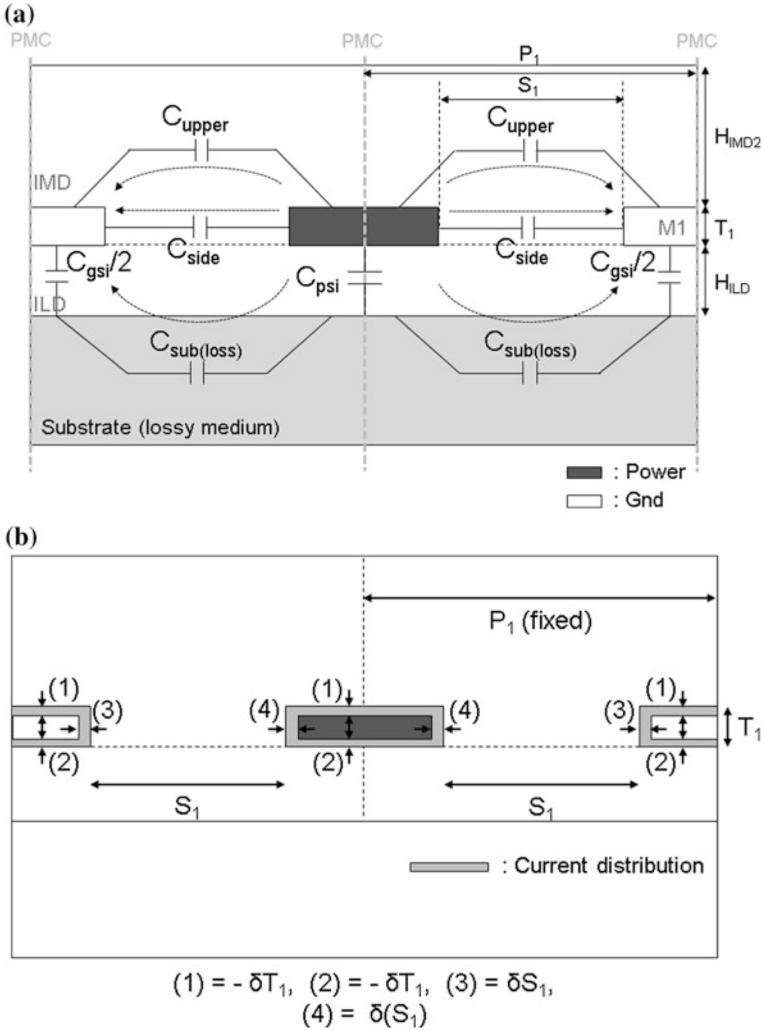


Fig. 6.18 **a** All capacitances (C_{upper}, C_{side}, C_{psi}, C_{gsi}, and C_{sub}) are shown according to the position of the electric-field generated in section B_x [23]. **b** The current distribution caused by the field penetration and physical parameter variations according to the current distribution [23] © 2013 IEEE

$$C_{upper(IMD)} = \varepsilon_{IMD} \frac{\varepsilon_0}{2} \left(\frac{K(k_1^{'})}{K(k_1)} \right) \quad (6.23c)$$

Next, by summing $C_{upper\,(IMD)}$ and $C_{upper}^{air-filled}$, we can calculate C_{upper} according to Eq. (6.24).

$$C_{upper} = C_{upper}^{air-filled} + (\varepsilon_{IMD} - 1)\frac{\varepsilon_0}{2}\left(\frac{K(k_1')}{K(k_1)}\right) \quad (6.24)$$

By using Eq. (6.18), we can calculate the capacitance C_{side}, as represented in Eq. (6.25).

$$C_{side} = \varepsilon_{IMD} C_{upper}^{air-filled} \quad (6.25)$$

To model the electric fields penetrating the substrate, we use the capacitances C_{psi}, C_{gsi}, and $C_{sub\ (loss)}$. For the conventional case in which H_{ILD} is on the order of several μm and S_1 is on the order of tens of μm, there are no electric fields in the ILD itself. We verified this by using a conformal mapping method. The verification indicates that all electric fields between the bottoms of the power and ground lines penetrate the substrate. Conventionally, the substrate is a loss-inducing medium. To include the dielectric loss in the substrate, we split the electric fields into the electric fields between the power line and the substrate, the electric fields between the ground line and the substrate, and the electric fields in the substrate. We model the classified electric fields using the capacitances C_{psi}, C_{gsi}, and $C_{sub\ (loss)}$, as represented in Eq. (6.26a and b).

$$C_{psi\&gsi} = \varepsilon_0 \varepsilon_{ILD}\left(\frac{W_1}{H_{ILD}} + \frac{4\ln(2)}{\pi}\right) \quad (6.26a)$$

$$C_{sub(loss)} = 2\varepsilon_{Sub}\left(1 + \frac{\sigma_{Sub}}{j\varepsilon_{Sub}\omega}\right)C_{upper}^{air-filled} \quad (6.26b)$$

As shown in Fig. 6.18b, the capacitances in the model are composed of C_{pg}, $C_{psi\ \&\ gsi}$, and C_{sub}. The capacitance C_{pg} is calculated from Eq. (6.27).

$$C_{pg} = 2C_{upper} + 2C_{side} \quad (6.27)$$

Although the electric fields in section C_x are separated into two current paths, all electric fields in section C_x are the same as those in section A_x. Because the area of a current path in section C_x is reduced to half of that in section A_x and because the capacitance is split in two, the resistance and inductance of each current path are twice the values of section A_x. However, because these two current paths are connected in parallel, section C_x has the same lumped model as section A_x, as shown in Fig. 6.15. These considerations mean that section C_x has the same characteristic impedance as section A_x. We confirmed the similarity in the impedance between section A_x and section C_x through 3D EM simulation by CST MWS using the waveguide port.

The unit cell of the grid-type PDN is finally modeled by connecting the RLGC-lumped models of all the TL sections based on a segmentation method, as shown in Fig. 6.19a. A segmentation method, which is a matrix calculation method, is

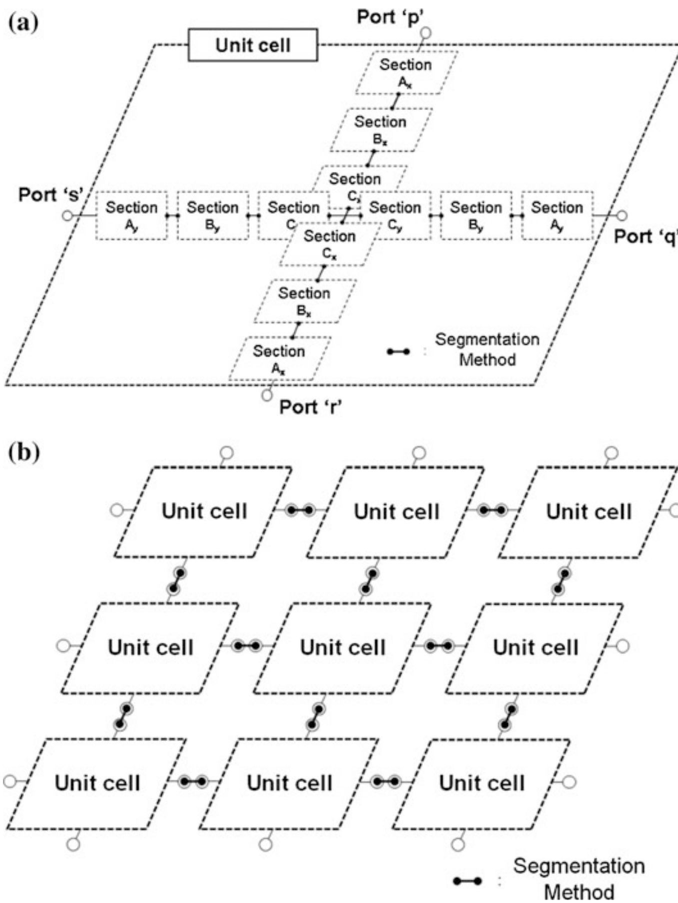


Fig. 6.19 **a** The unit cell is modeled by connecting the RLGC-lumped models of all TL sections based on a segmentation method [23]. **b** To model the grid-type PDN, all the ports of each unit cell are connected with the face-to-face ports of each adjacent unit cell with a segmentation method [23] © 2013 IEEE

used to incorporate decomposed structures into a whole structure. Then, by connecting all the ports of each unit cell with the face-to-face ports of each adjacent unit cell based on a segmentation method, we can model the whole grid-type PDN, as shown in Fig. 6.19b.

To verify the proposed models for grid-type PDNs, the PDN impedance curve of the model is compared with that of the 3D EM simulation and with that of a measurement in the frequency range from 0.1 to 20 GHz. First, an on-chip PDN was fabricated, as shown in Fig. 6.20a.

We measured the PDN impedance of the on-chip PDN shown in Fig. 6.20a, with a vector network analyzer (Agilent N5230A, bandwidth of instrument: 300 kHz to 26.5 GHz) over the frequency range of 0.1–20 GHz. To minimize the

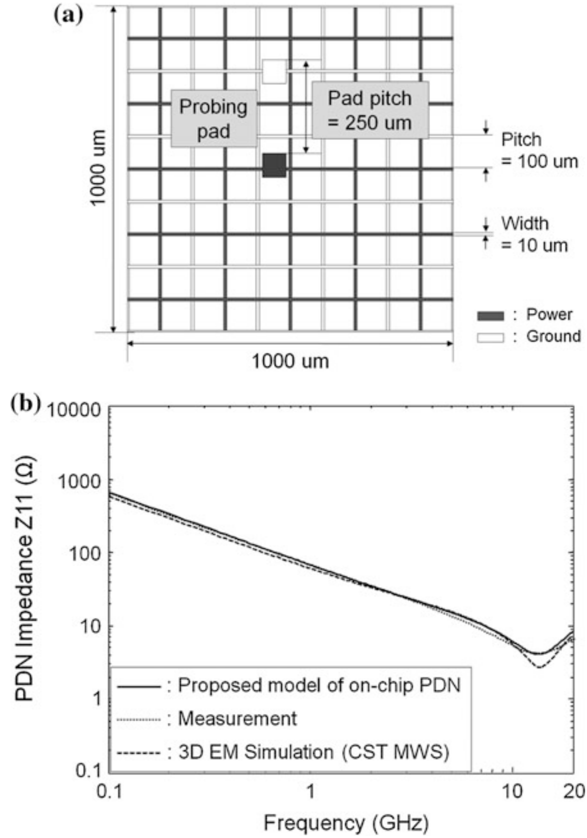


Fig. 6.20 **a** The *top view* of the fabricated on-chip PDN [12]. **b** The measured, simulated, and model-based estimated PDN impedance *curves* of the on-chip PDN in (**a**) [12] © 2012 IEEE

parasitic effects from the SMA connectors and coaxial cables, a microprobe (FPC-series GS type with a 250 μm pitch from Cascade Microtech) and its calibration kit (106-683A for wide-pitch microprobes (250–1250 μm)) were used for measurement. The PDN impedance curve obtained from the proposed model of the on-chip PDN aligns well with the measurement in the frequency range from 0.1 to 20 GHz, as shown in Fig. 6.20b.

A key feature of our approach is the substantial reduction in computation time. The 3D EM simulator (CST MWS) takes a long time (18 h 53 min) to simulate the on-chip PDN shown in Fig. 6.20a, when we use a computer with a Core 2 Duo CPU @ 3.00 GHz and 4 GB RAM memory for the simulation. On the contrary, the proposed model of the on-chip PDN takes only 8.86 s to estimate the impedance of the on-chip PDN.

Second, for verification of the proposed model for the interposer PDN, we simulated the interposer PDN shown in Fig. 6.21a. The size of the PDN pattern is 2 × 2 mm. The metal width and metal pitch between the power and ground lines are 10 and 100 μm, respectively. The pattern includes two ports: port 1 and port 2.

As shown in Figs. 6.21b and c, the simulated PDN impedance curves (a self-Z curve and a transfer-Z curve) of the interposer PDNs on the silicon substrate are well matched with those estimated from the proposed model when considering the log-log scale.

From these observations, we successfully verified the proposed model for the interposer PDN in the frequency range of 0.1–20 GHz. The self and mutual inductances (L_{PDN} and M_{PDN}), shown in Figs. 6.21b and c, respectively, are accurately estimated. Additionally, the mode resonance (1,0)/(0,1) peak generated at 14.6 GHz on the interposer PDN is successfully estimated by using the proposed model. This result confirms the ability of the proposed model to estimate the PDN inductance and mode resonance of the interposer PDNs. We can save time in impedance estimation by using the proposed model. The 3D EM simulator (CST MWS) takes a long time (approximately 25 h) to simulate the interposer PDN (# of the mesh cells: 1,219,212 ea.) shown in Fig. 6.21a when we use a computer with an Intel(R) Core i7-2600 processor @ 3.4 GHz and 16 GB RAM memory. On the contrary, the proposed model for the interposer PDN takes only 17.68 s (unit cell modeling (0.93 s) + grid-type PDN modeling (16.75 s)) to estimate the PDN impedance. Therefore, we conclude that the proposed model is an accurate and efficient method to estimate the impedance of interposer PDNs on a silicon substrate.

6.2.3 Modeling of the Power/Ground (P/G) TSVs and the P/G Bumps

The structure and parameters of a P/G TSV pair including bumps and contacts are shown in Fig. 6.22a. A high-frequency scalable electrical model of an S/G TSV pair with top and bottom bumps has already been introduced in [22]. The analytic RLGC equations are derived from the physical configuration along with the design parameters. However, in the model, the contacts for the interconnection between the grid-type PDN and the TSVs are not included. To include the contacts shown in Fig. 6.22a, the scalable electrical model of a P/G TSV pair is changed slightly from the lumped model of the S/G TSV pair by adding the resistance, inductance, and capacitance of the contacts based on their structural parameters. Because the physical length of the P/G TSV pair is considerably smaller than the wavelength corresponding to an operating frequency of several or tens of gigahertz, the lumped approximation is valid, and a single lumped stage is sufficient for the TSV model.

Because most electrical components of the TSVs and bumps of a P/G TSV pair have already been introduced in [22], only the electrical components attributed to the contacts are considered in this chapter.

The capacitance C_{Cont} between the power and the ground of the contact is considered as shown in Fig. 6.22b. This is expressed in Eq. (6.28).

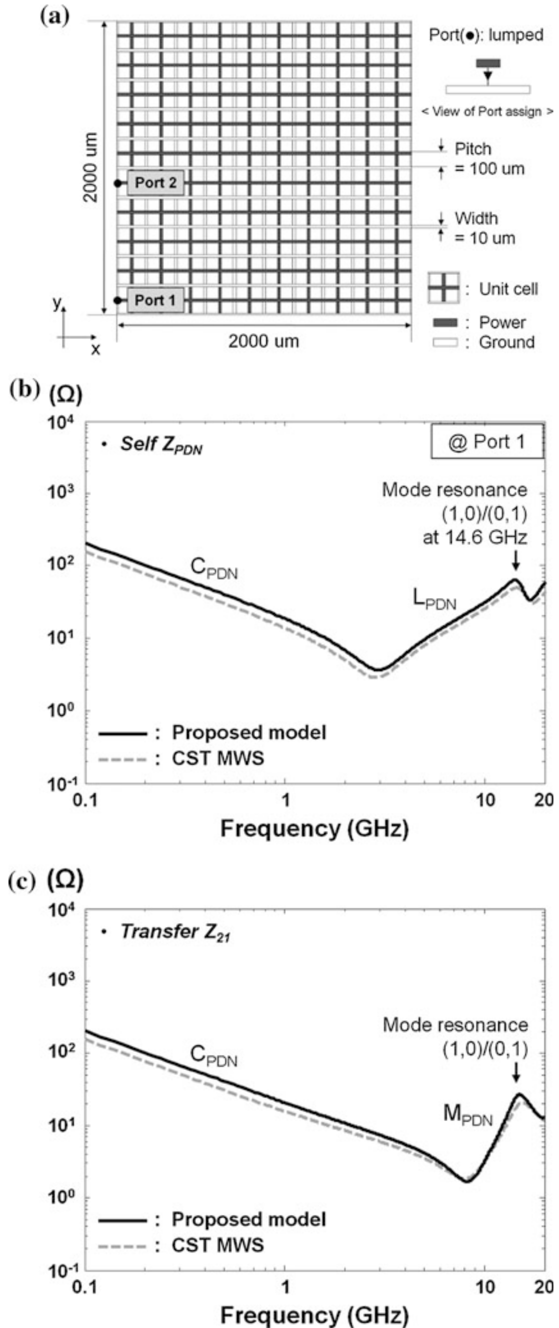


Fig. 6.21 **a** The *top view* of the simulated interposer PDN on the silicon substrate with a size of 2 mm × 2 mm and its assigned port. The metal width and the metal pitch between the power and ground lines are 10 and 100 μm, respectively [23]. **b** The self-impedance curve of the interposer PDN on the silicon substrate shown in (**a**) obtained from the proposed model and EM simulation by CST MWS [23]. **c** The transfer-impedance curve of the interposer PDN on the silicon substrate shown in (**a**) obtained from the proposed model and EM simulation by CST MWS [23] © 2013 IEEE

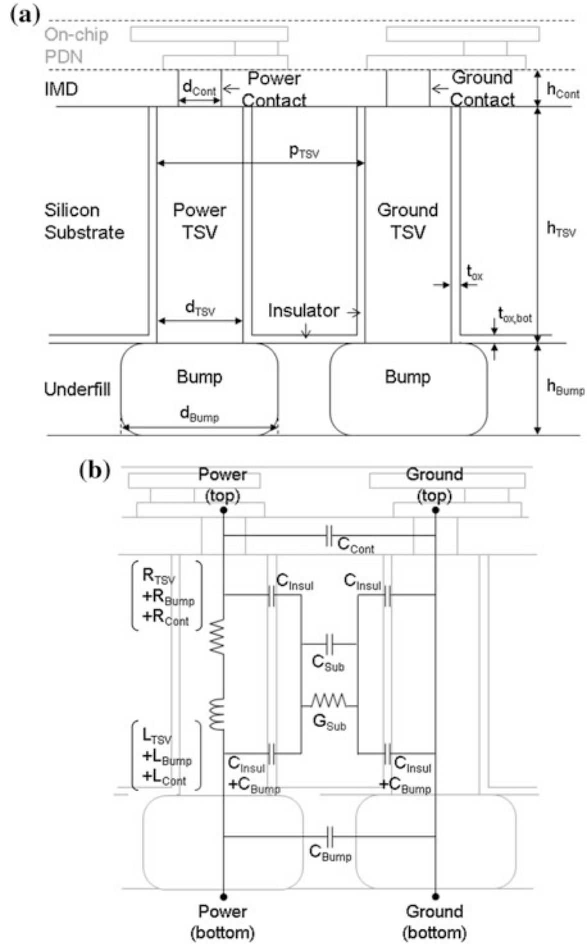


Fig. 6.22 **a** The structure of a P/G TSV pair including bumps and contacts and their structural parameters [23]. **b** The scalable RLGC-lumped model of a P/G TSV pair [23] © 2013 IEEE

$$C_{cont} = \frac{\pi \times \varepsilon_0 \varepsilon_{IMD}}{cosh^{-1}\left(\frac{p_{TSV}}{d_{Cont}}\right)} \times h_{Cont}[F] \tag{6.28}$$

The resistance of the contact R_{Cont} is expressed in Eq. (6.29). In the equation, there is a proximity factor, k_p. The magnitude of the proximity factor, k_p, is determined by the ratio p_{TSV}/d_{Cont}.

$$R_{Cont} = \sqrt{(R_{DC,Cont})^2 + (R_{AC,Cont})^2} \tag{6.29}$$

where,

$$R_{DC,Cont} = \rho_{Cont} \times \frac{h_{Cont}}{\pi \times \left(\frac{d_{Cont}}{2}\right)^2} \; [\Omega]$$

$$R_{AC,Cont} = k_p \left(\rho_{Cont} \times \frac{h_{Cont}}{2\pi \times \frac{d_{Cont}}{2} \times \delta_{skin,Cont} - \pi\delta^2_{skin,Cont}} \right) \; [\Omega]$$

$$\delta_{skin,Cont} = \frac{1}{\sqrt{\pi f \sigma_{Cont}}} \; [\mathrm{m}]$$

As the operating frequency increases, the impedance of the inductance becomes dominant. Therefore, the inductance of the contact L_{Cont} should be modeled. This is derived from Eq. (6.30).

$$L_{Cont} = \left\{ \frac{\mu_0}{2\pi} \times h_{Cont} \times ln\left(\frac{p_{TSV}}{\frac{d_{Cont}}{2}} \right) \right\} \; [\mathrm{H}] \tag{6.30}$$

6.2.4 Modeling of a TSV-Based Stacked Grid-Type PDN

As shown in Fig. 6.23a, the on-chip and interposer PDNs are hierarchically connected by power/ground (P/G) TSVs and become a "TSV-based stacked grid-type PDN." In reality, the impedance estimation of the TSV-based stacked grid-type PDN is more important than that of the interposer PDN itself in 3D ICs. The TSV-based stacked grid-type PDN can be modeled based on a segmentation method by using grid-type PDN models for the on-chip and interposer PDNs and P/G TSV models, as shown in Fig. 6.23b [23]. As shown in Fig. 6.23b, by using a segmentation method, the models of the on-chip and interposer PDNs are connected to the P/G TSV models in a hierarchical order. We can apply this modeling method to the modeling of the TSV-based stacked grid-type PDN, including the on-chip and interposer PDNs.

For experimental verification of the modeling method for the TSV-based stacked grid-type PDN, we fabricated the double-stacked grid-type PDN shown in Fig. 6.24a. The horizontal size of both the upper- and lower-level grid-type PDNs is 960 μm × 960 μm. They have the same PDN structure. The physical dimensions of the double-stacked grid-type PDN are represented in Table 6.2.

The upper- and lower-level grid-type PDNs are connected to each other by 5 pairs of P/G TSVs, as shown in Fig. 6.24a. The P/G TSVs play an important role in determining the impedance of the TSV-based stacked grid-type PDN because the total loop inductance of the PDN is critically determined by the number of the P/G TSVs. Therefore, it is important to confirm the TSV connection of the fabricated PDN. To confirm this connection, we took SEM micrographs, which are

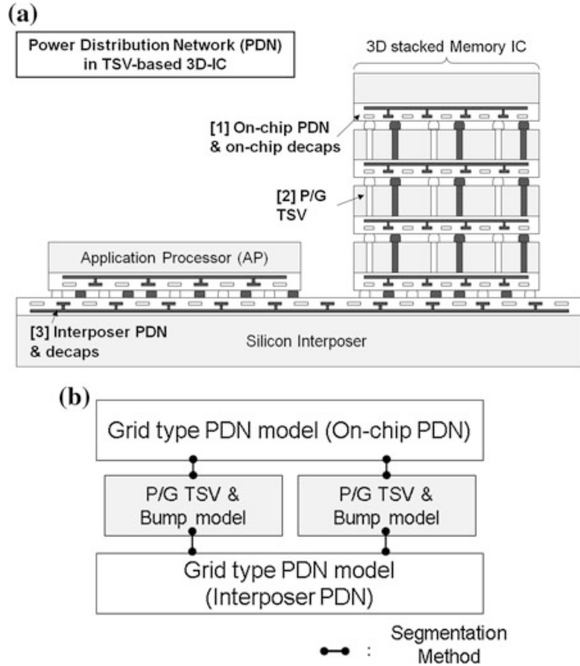


Fig. 6.23 **a** The cross-sectional view of the power distribution network (PDN) in a TSV-based 3D-IC. **b** A TSV-based stacked grid-type PDN is modeled by the sequential connections between two grid-type PDN models and the P/G TSV models in a hierarchical order with a segmentation method [23] © 2013 IEEE

shown in Fig. 6.24b. To take the SEM micrographs, we cut the fabricated sample at the dashed lines with the numbers (1) (2) (3), and (4). As a result, we obtained five SEM photos that include all TSVs. From these results, we confirmed the TSV connections and physical dimensions of the fabricated PDN represented in Table 6.2.

Based on the physical dimensions and the results of the TSV connection test, we model the fabricated double-stacked grid-type PDN by using the proposed grid-type PDN models, P/G TSV models, and an LC-lumped pad model extracted from CST MWS based on the modeling method shown in Fig. 6.23b.

The PDN impedance curves observed at the probing pad are shown in Fig. 6.25. The solid line represents the PDN impedance that is estimated from the proposed model for the TSV-based stacked grid-type PDN. The dashed line represents the PDN impedance obtained from the measurement. For this measurement, we use a vector network analyzer (Agilent N5230A, bandwidth of instrument: 300 kHz to 26.5 GHz) and a microprobe (FPC-series GS type with a 250 μm pitch from Cascade Microtech and its calibration kit (106–683 A) for wide-pitch microprobes). Using these instruments, we measured the impedance of the fabricated PDN in the frequency range of 0.1–20 GHz. The dotted line represents the PDN impedance estimated from the 3D EM simulation by CST MWS.

As shown in Fig. 6.25, these three impedance curves are well-matched with each other. From this result, we conclude that the modeling method for the TSV-based stacked grid-type PDN is experimentally verified in the frequency range of

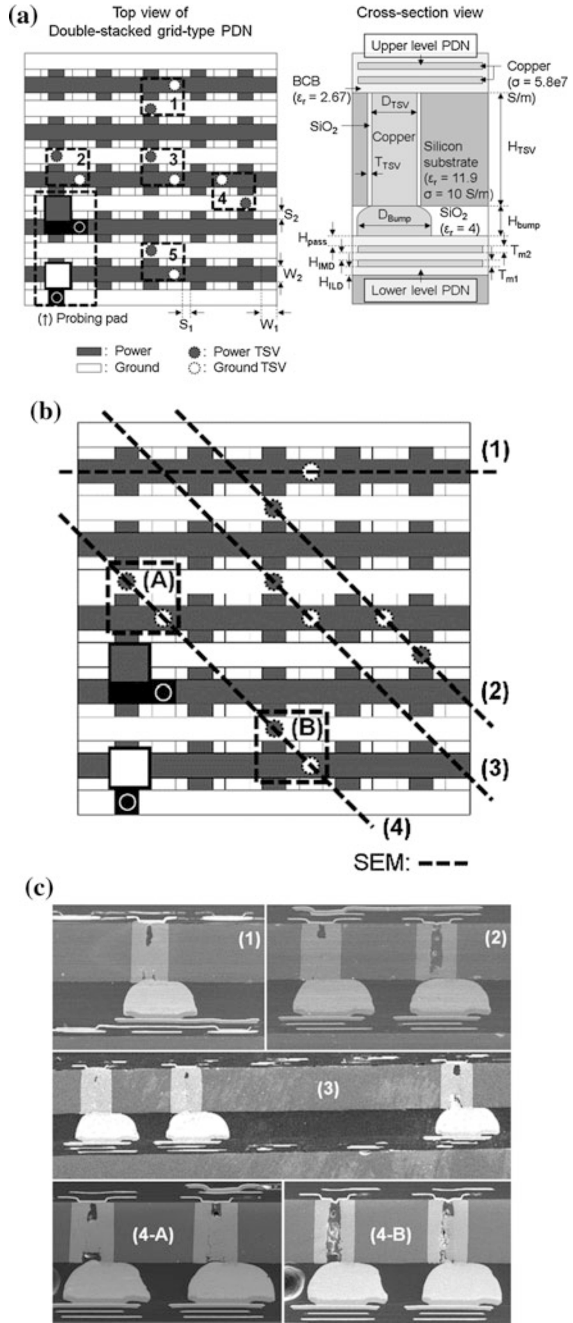


Fig. 6.24 **a** The *top* and *cross-sectional views* of the fabricated double-stacked grid-type PDN. The *upper-level* PDN is connected with the *lower-level* PDN by 5 pairs of P/G TSVs [23]. **b** To confirm the TSV connection and physical dimensions of the structure, we took SEM micrographs. We obtained five SEM micrographs that include all the TSVs. Using the SEM micrographs, we confirmed that all the TSVs are connected with the *upper-* and *lower-level* PDNs [23] © 2013 IEEE

Table 6.2 Physical parameters and their values in a fabricated double-stacked grid-type PDN

Parameter	Description	Value (μm)
W_1	Metal width of the M_1 metal	60
W_2	Metal width of the M_2 metal	60
S_1	Space between the power line and the ground line on the M1 metal	30
S_2	Space between the power line and the ground line on the M2 metal	30
H_{ILD}	Height of the ILD layer	3.88
H_{IMD}	Height of the IMD layer	3.82
H_{pass}	Height of the passivation	3.10
T_{m1}	Thickness of the M1 metal	1.94
T_{m2}	Thickness of the M2 metal	1.94
H_{TSV}	Height of the TSV	63
H_{Bump}	Height of the bump	39
D_{TSV}	Diameter of the TSV	40
D_{Bump}	Diameter of the bump	88
T_{SiO2}	Thickness of the SiO_2	0.5

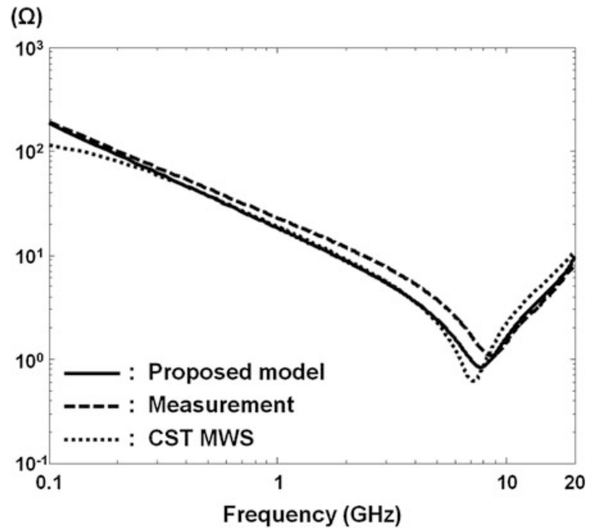


Fig. 6.25 The PDN impedance curves obtained from the proposed model, the measurement, and the 3D EM simulation observed at the probing pad shown in Fig. 6.24a [23] © 2013 IEEE

0.1–20 GHz. More importantly, we greatly decreased the simulation time. The 3D EM simulator (CST MWS) takes a long time (25.5 h) to simulate the double-stacked grid-type PDN shown in Fig. 6.24a (# of the mesh cells: 259,346 ea.), when we use a computer with an Intel(R) Core i7-2600 CPU and 16 GB of RAM operating at 3.4 GHz. In contrast, the proposed model for the stacked grid-type PDN takes only 5.79 s (unit cell modeling (1.73 s) + grid-type PDN and TSV-based grid-type PDN modeling (4.06 s)) to estimate the impedance of the double-stacked grid-type PDN. Therefore, we conclude that the proposed model is an accurate and efficient method to estimate the PDN impedance of TSV-based stacked grid-type PDNs.

6.2.5 Modeling of the On-Chip Decoupling Capacitor (On-Chip Decap)

The on-chip decaps play an important role in determining the electrical characteristics of on-chip PDNs. Therefore, we must model the on-chip PDNs and on-chip decaps together. Because the impedances of on-chip PDNs vary strongly according to the capacitances and the positions of the on-chip decaps, the effects of the capacitances and positions of the embedded on-chip decaps on the on-chip PDN should be considered. First, by connecting the RC-lumped models of the on-chip decaps with the newly generated port 'N' of the unit cell based on a segmentation method [12], as described in Fig. 6.26, the decap-embedded unit cell is generated. Port 'N' is located in the center of the unit cell, which is arranged for connection with the RC-lumped models of the on-chip decaps.

In on-chip PDNs, there are many on-chip decaps in different positions. By partitioning the on-chip PDN into several unit cells and connecting the unit cells with the on-chip decaps embedded on the unit cells, several types of decap-embedded unit cells are generated according to the number of the embedded on-chip decaps. Using the decap-embedded unit cells, the decap-embedded on-chip PDN is modeled in the same manner as the on-chip PDN, as described in Fig. 6.19b.

To verify the proposed models for a decap-embedded on-chip PDN, a decap-embedded on-chip PDN was fabricated, as shown in Fig. 6.27. The proposed model of the decap-embedded on-chip PDN has been validated by comparing the PDN impedance curve of the model with that of the experimental result in the frequency range from 0.1 to 20 GHz.

We measured the PDN impedance of the decap-embedded on-chip PDN shown in Fig. 6.27 with a vector network analyzer (Agilent N5230A, bandwidth of instrument: 300 kHz to 26.5 GHz) over the frequency range of 0.1–20 GHz. To minimize the parasitic effects from the SMA connectors and coaxial cables, a microprobe (FPC-series GS type with a 250 μm pitch from Cascade Microtech) and its calibration kit (106–683 A for wide-pitch microprobes (250–1250 μm)) were used for measurements. To measure the decap-embedded on-chip PDN, it was necessary to supply a DC bias voltage to the PDN by connecting a bias tee (GigaLane GLB265B with a broad bandwidth (16 kHz to 26.5 GHz)) to the microprobe. The PDN impedance curve obtained from the proposed model of the decap-embedded on-chip PDN aligns well with the measurement in the frequency range from 0.1 to 20 GHz, as shown in Fig. 6.28. In this respect, the usefulness of the proposed model is experimentally verified across the frequency range.

A key feature of our approach is the substantial reduction in computation time. In the case of the decap-embedded on-chip PDN, it is impossible for the 3D EM simulator to estimate its PDN impedance due to the embedded MOS capacitors. However, when we use the proposed model of the decap-embedded on-chip PDN, only 9.24 s are required to estimate the impedance of the decap-embedded on-chip PDN, which includes the generation time of the decap-embedded unit cell.

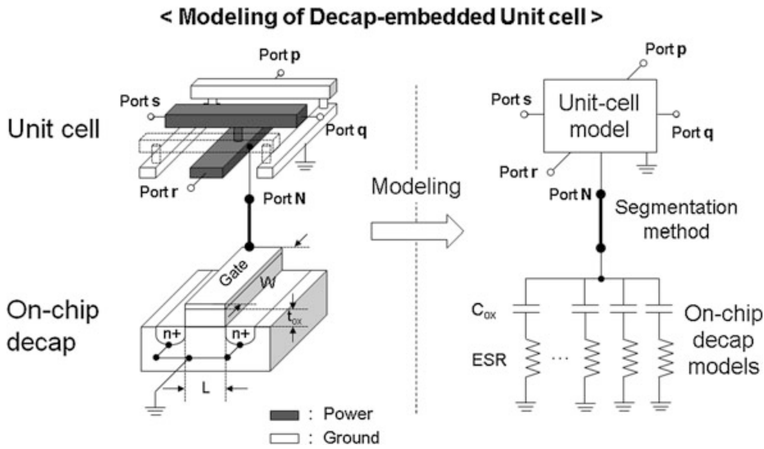


Fig. 6.26 For the modeling of the embedded on-chip decaps, the models of the on-chip decaps embedded on a certain unit cell are connected to the unit cell model based on a segmentation method [12] © 2012 IEEE

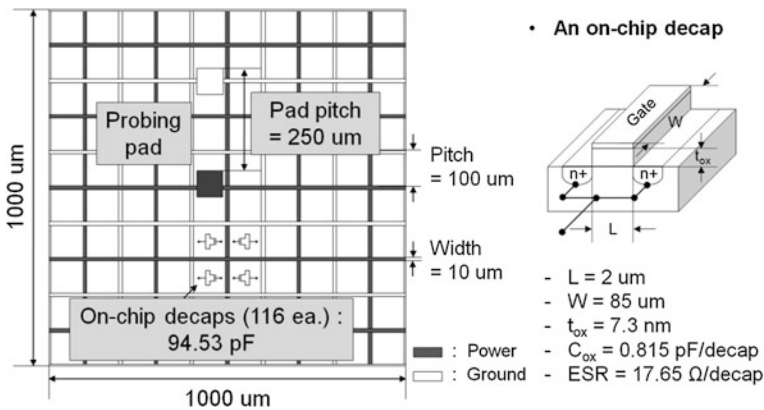


Fig. 6.27 The *top view* of the fabricated decap-embedded on-chip PDN [12] © 2012 IEEE

6.3 Analysis of the PDN Impedance in TSV-Based 3D ICs in the Frequency Domain

6.3.1 Introduction

In this Sect. 6.3, we analyze the impedance curves of the PDNs in TSV-based 3D ICs in the frequency domain based on the PDN model. The analysis items are as follows:

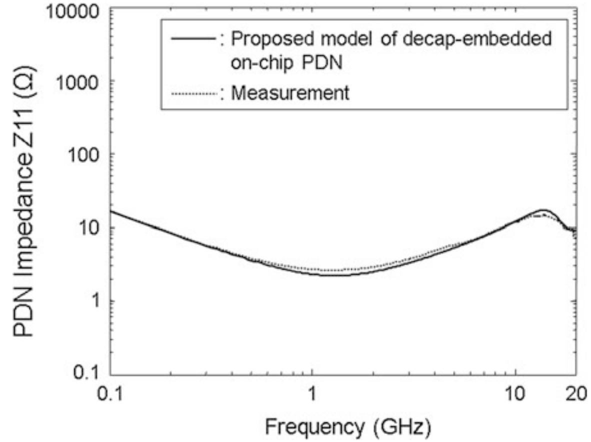


Fig. 6.28 The measured and model-based estimated PDN impedance curves of the decap-embedded on-chip PDN in Fig. 6.27 [12] © 2012 IEEE

1. Analysis with a variation in grid-type PDN size [23].
2. Analysis with a variation in the number of P/G TSVs in TSV-based stacked grid-type PDNs [12, 24, 25].
3. Analysis with a variation in the capacitance of on-chip decaps in TSV-based stacked grid-type PDNs [24, 26].

These analyses can help PDN engineers design the grid-type PDNs for the on-chip and interposer PDNs and TSV-based stacked grid-type PDNs in TSV-based 3D ICs.

6.3.2 Analysis with a Variation in the Size of a Grid Type PDN

In this section, we analyze the impedance curves of a grid-type PDN for a variation in the horizontal size of the PDN. Determination of the horizontal size of the PDN is especially important in the design of an interposer PDN.

We estimate the impedance curves of the grid-type PDNs in the frequency range from 0.1 to 20 GHz for a variation in the horizontal size of the grid-type PDN.

As shown in Fig. 6.29a, the analysis includes three types of interposer PDNs with different horizontal sizes; however, they are composed of the same unit cells. The horizontal sizes of PDN (A), PDN (B), and PDN (C) are 2 mm × 2 mm, 4 mm × 4 mm, and 6 mm × 6 mm, respectively. These PDNs have the same port position (0 mm, 0.1 mm) along the x- and y-axes. This position was selected because all mode resonances occur at the boundary of the grid-type PDN, which results from the voltage and current of all modes at the boundary always being high and low, respectively.

As shown in Fig. 6.29b, the capacitance (C_{PDN}) and inductance (L_{PDN}) of the grid-type PDN increase as the PDN size increases. Because of these increases, the PDN impedance determined by the capacitance is lowered in the low-frequency range, and the impedance determined by the inductance is increased in the mid-frequency range. The capacitance (C_{PDN}) increases linearly with the PDN area. We can represent this capacitance increase according to the size variation using Eq. (6.31).

$$C_{Target} = \frac{A_{Target}}{A_{Ref}} C_{Ref} \tag{6.31}$$

In this equation, C_{REF} and C_{TARGET} are the capacitances of the reference and target PDN, respectively, with the condition that these PDNs are composed of the same unit cells. A_{REF} and A_{TARGET} are the horizontal sizes of the reference and target PDNs, respectively.

The inductance (L_{PDN}) increases linearly with the length of the PDN in both the x- and y-axes when the PDNs are square. We can represent this inductance increase according to the size variation using Eq. (6.32). This equation is experimentally derived by comparing the inductances obtained when the PDN size is varied. The inductances are calculated using the capacitance values of the PDNs and the series resonance frequency (f_A, f_B, and f_C in Fig. 6.29b) using

$$L_{(A,B,C)} = \frac{1}{\left(2\pi f_{(A,B,C)}\right)^2 C_{(A,B,C)}}, L_{Target} = \sqrt{\frac{l_{Target}}{l_{Ref}}} L_{Ref} \tag{6.32}$$

In this equation, L_{REF} and L_{TARGET} are the inductances of the reference and target PDNs, respectively with the condition that these PDNs are composed of the same unit cells. l_{REF} and l_{TARGET} are the lengths of the reference and target PDNs, respectively. From Eq. (6.31), the capacitances of PDN (C) and PDN (B) are nine times and four times the capacitance of PDN (A), respectively. The inductances of PDN (C) and PDN (B) are $\sqrt{\frac{6\,\text{mm}}{2\,\text{mm}}} = \sqrt{3}$ times and $\sqrt{\frac{4\,\text{mm}}{2\,\text{mm}}} = \sqrt{2}$ times the inductance of PDN (A), respectively, as determined by Eq. (6.32).

As a distinct feature of the large-sized grid-type PDNs, the mode resonances of PDN (A), PDN (B), and PDN (C) occur at the resonance frequencies 'a' (4.36 GHz), 'b' (6.58 GHz), 'c' (9.64 GHz), and 'd' (14.0 GHz), respectively, in the high-frequency range. The mode numbers of these mode resonances are represented in Table 6.3. For mode resonances (i, j), i and j are the mode numbers for the x- and y- axes, respectively. The mode resonance is generated by the standing wave formed on the interposer PDN when the length of the PDN in the x- or y-direction is $\frac{N}{2}, (N = 1, 2, 3\ldots)$ times the wavelength. The number N is then the mode number of the mode resonance. The mode resonance (2,1) means that a standing wave with one wavelength is formed on the x-axis and a standing wave with half of the wavelength is formed on the y-axis. Additionally, the mode

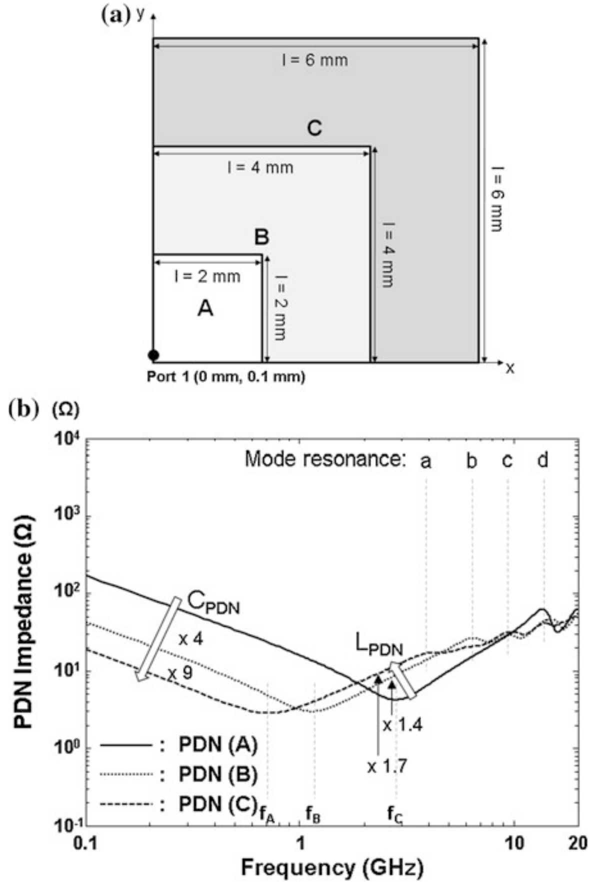


Fig. 6.29 **a** The sizes and port assigned to grid-type PDNs (A) (B), and (C) [23]. **b** The PDN impedance curves of PDN (A), PDN (B), and PDN (C). As the size of the grid-type PDN increases, the capacitance and inductance of the PDN increase. Additionally, the mode resonance occurs at a lower frequency with an increase in the PDN size [23] © 2013 IEEE

resonance (1,0)/(0,1) means that a standing wave with half of the wavelength is formed on the x- or y-axis, because the length of the PDN along the x-axis is equal to that along the y-axis in the square-shaped PDN.

As shown in Fig. 6.29b, the mode resonance occurs at a lower frequency and more resonances occur as the PDN size increases. Fortunately, the Q-factors of the resonances are reduced because of the increase in the resistance of the electrical components caused by the increase in the PDN size. These reductions flatten the parallel resonance peaks. However, because the mode resonances of a larger PDN occur at its higher inductance, the impedance gap between the larger PDN and the smaller PDN is significant. For example, the impedance level of PDN (C) is 17.09 Ω at resonance frequency ‘a’. In contrast, the impedance level of PDN (A) is 7.162 Ω at this frequency. The impedance of PDN (C) is more than two times that of PDN (A). Therefore, the SSN generated on PDN (C) at this frequency is more critical than that on PDN (A) in 3D ICs.

Table 6.3 Mode numbers of mode resonances of PDN (A), PDN (B) and PDN (C)

Mode resonance and resonance frequency (in GHz)	Mode number
a (at 4.36)	(1,0)/(0,1) in PDN (C)
b (at 6.58)	(1,0)/(0,1) in PDN (B)
	(1,1) in PDN (C)
c (at 9.64)	(1, 1) in PDN (B)
	(2,0)/(0,2) in PDN (C)
d (at 14.0)	(1,0)/(0,1) in PDN (A)
	(2,0)/(0,2) in PDN (B)
	(2,1)/(1,2) in PDN (C)

From the analysis of the change in the PDN impedance with a variation in the horizontal size of the grid-type PDN, we conclude that a larger PDN brings a significant increase in the impedance level in the mid- and high-frequency range because of the increased inductance and number of mode resonances. Of course, the increase in the PDN size helps to reduce the PDN impedance in the low-frequency range. Nevertheless, because there is a powerful method to increase the capacitance using decoupling capacitors, it is necessary to reduce the PDN size when we design the interposer PDN to ultimately reduce the SSN on the interposer PDN. In spite of the difficulty in designing the size of the interposer PDN, an interposer PDN is used because a grid-type interposer PDN can dramatically reduce the inductances of power-supply paths compared with P/G transmission lines. Therefore, the optimum size of the interposer PDN is the minimum size that can supply power to all the other PDNs stacked on the interposer PDN that serves as the grid-type PDN.

6.3.3 Analysis with a Variation in the Number of P/G TSVs in TSV-Based Stacked Grid-Type PDNs

6.3.3.1 GPU-DRAM System (Heterogeneous IC Stacking)

Figure 6.30.

6.3.3.2 Homogeneous IC Stacking

To analyze the effects of the number of P/G TSV pairs on the impedance of 3D stacked on-chip PDNs in homogenous IC stacking, we analyze the impedances of the double-stacked on-chip PDNs with respect to a variation in the number of P/G TSV pairs, as shown in Fig. 6.31a. In 3D stacked on-chip PDNs, several on-chip PDNs are connected through P/G TSV pairs. Due to the structural characteristics of the 3D stacked on-chip PDNs, PDN loops are formed through not only the on-

chip PDNs but also the P/G TSV pairs. Additionally, these loops are quite entangled. Because minimizing the complexity of the PDN loops helps when analyzing the effect of the number of P/G TSV pairs on the PDN impedance, we chose to use double stacked on-chip PDNs. In the four cases shown in Fig. 6.31a, a P/G TSV pair is separated from the other P/G TSV pairs by 800 μm. Because this length is much longer than the height of the P/G TSV pair, we can ignore the coupling between P/G TSV pairs. As shown in Fig. 6.31b, the impedances of the double-stacked on-chip PDNs are determined by the capacitances, inductances, and resistances of the PDNs.

Figure 6.31b shows the PDN impedance curves observed at the uppermost on-chip PDN for a variation in the number of P/G TSV pairs. The position of the P/G TSV pairs is described in Fig. 6.31a. The solid line represents the impedance curve of the PDN including one P/G TSV pair. The dotted line represents the impedance curve of the PDN including three P/G TSV pairs. The dashed line represents the impedance curve of the PDN including nine P/G TSV pairs, and the dash-dot line represents the impedance curve of the PDN including fifteen P/G TSV pairs. In this figure, when the number of P/G TSV pairs increases, the inductance of the PDN loop and of the on-chip PDN itself are reduced.

To analyze the change in inductance, we look at the change in the PDN loop according to the variation in the number of P/G TSV pairs. As we mentioned earlier, in 3D stacked on-chip PDNs, the PDN loops are generated through not only the on-chip PDNs but also the P/G TSV pairs. The PDN loops generated through the P/G TSV pairs are larger than those generated through the on-chip PDNs. Therefore, the inductance of the total PDN loop ($L_{PDN\ loop}$) is higher than that of the on-chip PDN ($L_{on\text{-}chip\ PDN}$). Because the PDN loops generated through the P/G TSV pairs are connected in parallel, the inductance ($L_{PDN\ loop}$) decreases as the number of the P/G TSV pairs increases in Fig. 6.31b. However, the inductance ($L_{PDN\ loop}$) cannot be reduced below the inductance of the on-chip PDN ($L_{on\text{-}chip\ PDN}$) because the PDN loop is not separated from the on-chip PDN, but the loop is larger. The inductance of the on-chip PDN ($L_{on\text{-}chip\ PDN}$) itself also decreases with an increase in the number of P/G TSV pairs because additional PDN loops are also observed from the on-chip PDN. Similar to the decrease of the inductance, as the number of P/G TSV pairs increases, the resistance of the PDN loop decreases because of the increasing number of additional PDN loops, as shown in Fig. 6.31b.

6.3.3.3 Interposer-Based 2.5D Stacked GPU-DRAM System

The structure and the PDN composition of the interposer-based 2.5D GPU system are shown in Fig. 6.32a. Here, a GPU and four DRAMs are vertically stacked on top of the silicon interposer. The silicon interposer is also stacked on an organic package. In the interposer-based 2.5D GPU system, the 3D VDDQ PDN consists of on-chip PDNs of a GPU and stacked DRAMs, the P/G TSV and bump pairs, and a package PDN. The sizes of a GPU PDN, a DRAM PDN and a package PDN are

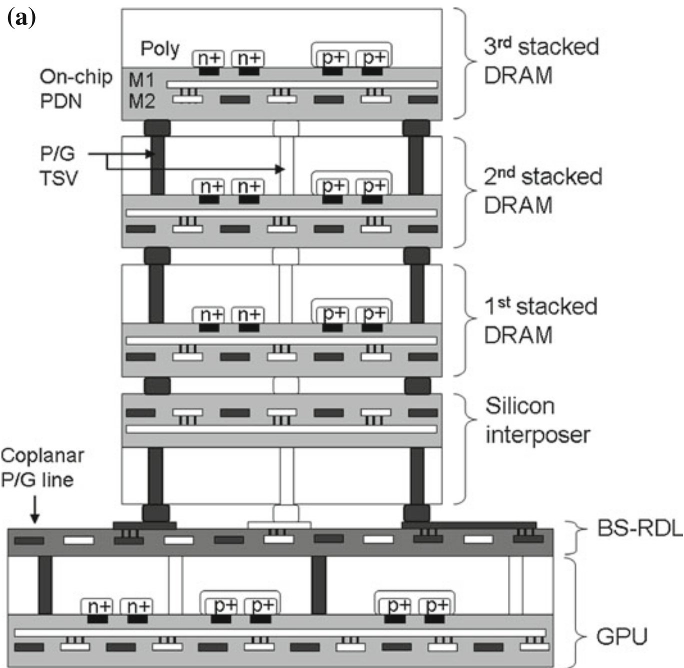


Fig. 6.30 **a** The cross-sectional view of the TSV-based GPU system consisting of three vertically stacked DRAMs with TSVs. The stacked DRAMs are connected to the GPU by TSVs, a silicon interposer, and a BS-RDL. The on-chip PDNs in the DRAM, GPU, and silicon interposer are also stacked and connected by P/G TSVs and coplanar P/G lines in the BS-RDL [25]. **b** The PDN impedance curves observed at the PDN in the third stacked DRAM when the numbers of P/G TSVs and P/G lines in the BS-RDL were changed [25]. **c** The PDN impedance curves observed at the PDN in the GPU when the numbers of P/G TSVs and P/G lines in the BS-RDL were changed [25]. © 2010 IEEE

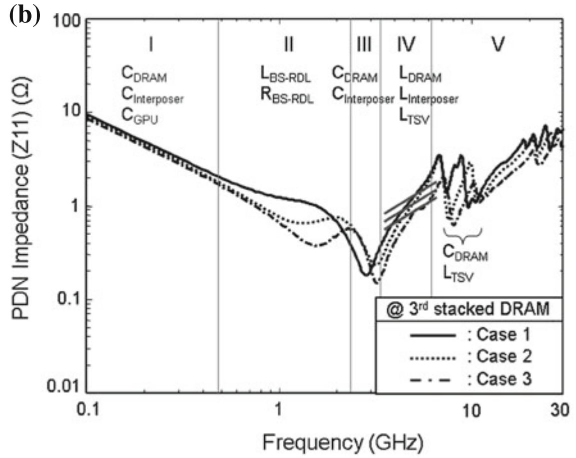
8.25 mm × 1.125 mm, 4 mm × 1.12 mm, and 15 mm × 20 mm, respectively. The length of the signal line between the GPU and the stacked DRAMs is 3 mm. The command and data signals of the GPU and the stacked DRAMs are delivered by the signal and the reference ground line (S/G line) in a silicon interposer, as described in Fig. 6.32. In the 3D VDDQ PDN shown in Fig. 6.32, the powers for the GPU and the stacked DRAMs are shared in the package level. On the contrary, the reference grounds of the GPU and the stacked DRAMs are shared in the silicon interposer because of the supply of the electrical reference toward the signal line between the GPU and the stacked DRAMs.

To estimate the PDN impedance and the pull-up impedance of the 3D VDDQ PDN, an impedance estimation method based on a segmentation method and a balanced–transmission line method (Balanced-TLM) was used. The method connects the internal ports of the models of on-chip PDNs, S/G lines, P/G TSV pairs, and a package PDN. The Balanced-TLM is a lumped modeling method that considers the electrical components of the reference ground [25].

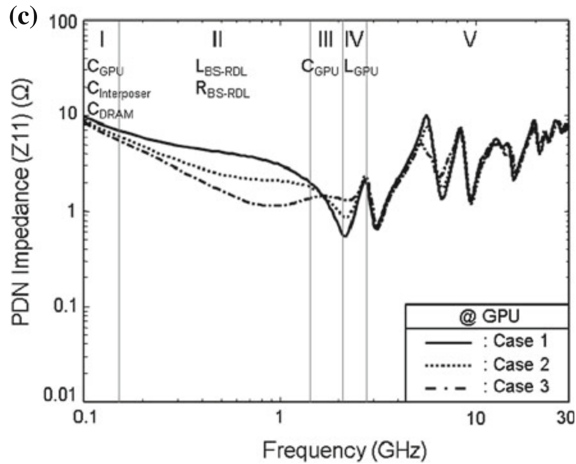
Fig. 6.30 continued

Case 1: Power TSV (12ea.) and Ground (14ea.)
Power line (12ea.) and Ground line (14ea.) in the BS-RDL.
Case 2: Power TSV (24ea.) and Ground TSV (26ea.)
Power line (24ea.) and Ground line (26ea.) in the BS-RDL.
Case 3: Power TSV (48ea.) and Ground TSV (50ea.)
Power line (48ea.) and Ground line (50ea.) in the BS-RDL.
* All cases apply the number variation to a region of the same size.

(b)



(c)



We observed the PDN impedance and the pull-up impedance at the GPU side as shown in Fig. 6.33 for a variation in the number of P/G TSV pairs.

In these estimations, the PDN impedances in region I and II in Fig. 6.33a decrease as the number of the P/G TSV pairs increases because of reduced PDN loop inductance and resistance. On the other hand, there is no variation in the pull-

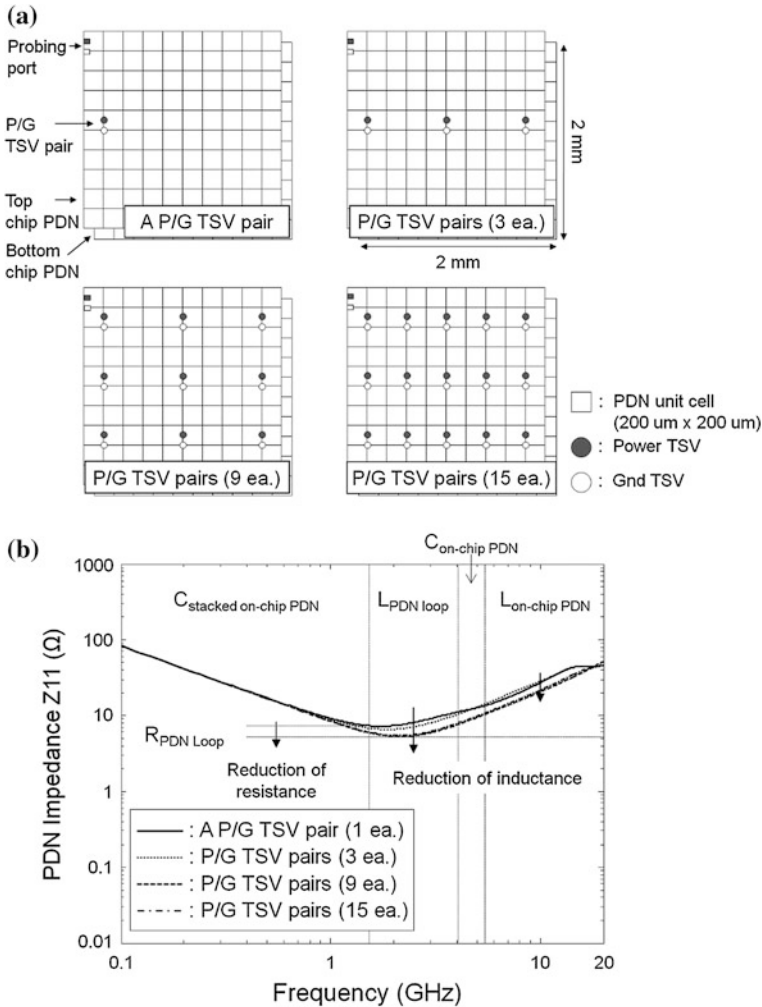


Fig. 6.31 **a** Four cases of double-stacked on-chip PDNs. In these cases, we vary the number of P/G TSV pairs. In the 3D stacked on-chip PDNs, all the on-chip PDNs have the same PDN structure. The P/G TSV pairs are attached to the same position of each on-chip PDN [23]. **b** The PDN impedance curves for a variation in the number of P/G TSV pairs. When the number of P/G TSV pairs increases, the PDN impedance decreases, which reflects the inductance and resistance of the 3D stacked on-chip PDN [23] © 2013 IEEE

up impedance for the same condition because the pull-up impedance is determined mainly by the inductance and the resistance of the signal line in the silicon interposer and the signal TSV in the stacked DRAMs. Therefore, to reduce the pull-up impedance, a structural variation such as minimizing the lengths and widening the cross-sectional areas of the signal line and the signal TSV is required.

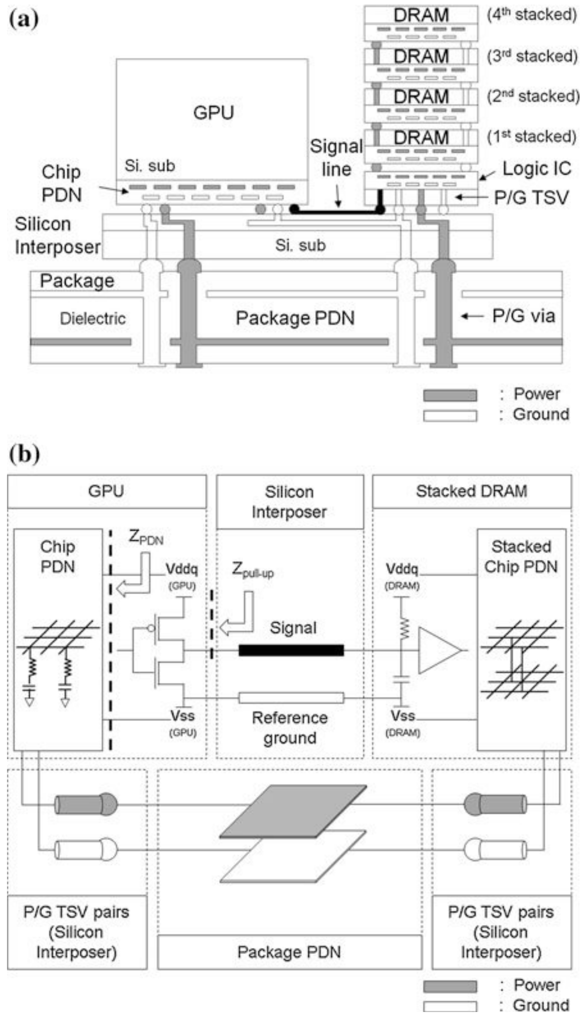


Fig. 6.32 **a** A cross-sectional view of the interposer-based 2.5D GPU system with the stacked DRAMs, a GPU, a silicon interposer, and an organic package. The stacked on-chip PDNs in the stacked DRAMs and the on-chip PDN in the GPU are connected in the package PDN level through a series of P/G interconnections such as P/G TSV pairs and P/G via pairs. The command and data signals of the GPU and the stacked DRAMs are delivered by the signal and the reference ground line in a silicon interposer [25]. **b** A Schematic of a 3D VDDQ PDN in an interposer-based 2.5D GPU system with the PDN impedance (Z_{PDN}) and the pull up impedance ($Z_{pull\text{-}up}$). The PDN impedance reflects the impedance properties of the on-chip PDNs, the P/G TSV pairs, and the package PDN forming the 3D VDDQ PDN. On the contrary, the pull-up impedance reflects the impedance properties of the on-chip PDNs, the P/G TSV pairs, the package PDN in the 3D VDDQ PDN, the signal lines in the silicon interposer, and the signal TSVs in the stacked DRAMs [25] © 2011 IEEE

6.3.4 Analysis with a Variation in the Capacitance of the On-Chip Decaps in a TSV-Based Stacked Grid-Type PDN

6.3.4.1 GPU-DRAM System (Heterogeneous IC Stacking)

The target structure for the analysis with a variation in the number of P/G TSVs in TSV-based stacked 3D ICs is shown in Fig. 6.34a. Here, three DRAMs are vertically stacked on top of the GPU employing TSV connectors, and a silicon interposer and a BS-RDL are used to interconnect the stacked DRAMs and the GPU. In the TSV-based GPU system, the PDN is hierarchically organized into the on-chip PDN, the P/G TSVs, and the coplanar P/G lines in the BS-RDL. The sizes of the on-chip PDNs supporting the I/O driver circuits in the DRAM, the GPU, and the silicon interposer are 4 mm × 1 mm, 10 mm × 1 mm, and 4 mm × 2 mm, respectively. Additionally, these on-chip PDNs are vertically stacked and connected by P/G TSVs and coplanar P/G lines in the BS-RDL.

The impedance curves observed for the on-chip PDN in the third stacked DRAM and the on-chip PDN in the GPU are shown in Fig. 6.34b and c, respectively for a variation in the ratio of the PDN area in which the on-chip decoupling capacitors are embedded to the area of the whole PDN. The on-chip decoupling capacitor can be modeled by the series connection of C_{decap} and the ESR. In this study, we varied the fraction of the PDN area in which on-chip decoupling capacitors are embedded to be 5, 10, and 15 % of the whole PDN area, with total capacitances of the on-chip decoupling capacitor used in the GPU system of 15.3, 30.6, and 45.9 nF, respectively.

As this fraction was increased, the impedance representing the capacitance of the on-chip PDN and the on-chip decoupling capacitor was reduced in regions I and III because of the increase in capacitance in Fig. 6.34. Additionally, as the fraction was increased, the PDN loop inductance was reduced in region IV because of the increase in the capacitance of the on-chip decoupling capacitor in Fig. 6.34. In addition, in region IV, the PDN mode resonance peaks and the anti-resonance peaks caused by the inductance of the TSV almost disappear because of the variation of the Q factor caused by the ESR of the on-chip decoupling capacitor. Therefore, increasing the total capacitance of the on-chip decoupling capacitor helps to lower the PDN impedance in all regions in Fig. 6.34.

6.3.4.2 Homogeneous IC Stacking

To investigate the effects of the on-chip decaps on the impedances of 3D stacked on-chip PDNs in homogeneous IC stacking, we analyze the impedances of the triple-stacked on-chip PDNs with respect to a variation in the capacitance of the on-chip decaps embedded in the PDNs shown in Fig. 6.35a.

Figure 6.35b shows the PDN impedance curves observed at the uppermost on-chip PDN for a variation in the capacitance of the on-chip decaps resulting from a

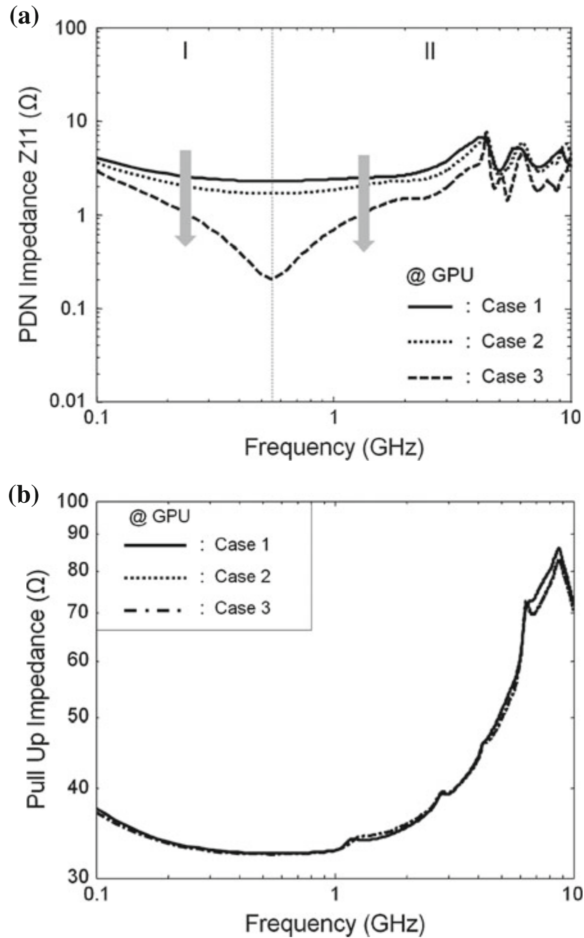


Fig. 6.33 **a** The PDN impedance curve of the 3D VDDQ PDN observed at the GPU side [25]. **b** The pull-up impedance of the 3D VDDQ PDN observed at the GPU side for a variation in the number of P/G TSV pairs. As the number of the P/G TSV pairs increase, the impedance levels in region I and II in (**a**) decrease because of reduced PDN loop inductance and resistance [25]. On the contrary, there is no change in the impedance levels in (**b**) because the pull-up impedance is affected mainly by the resistance and the inductance of the signal line in the silicon interposer and the signal TSVs in the stacked DRAMs © 2011 IEEE

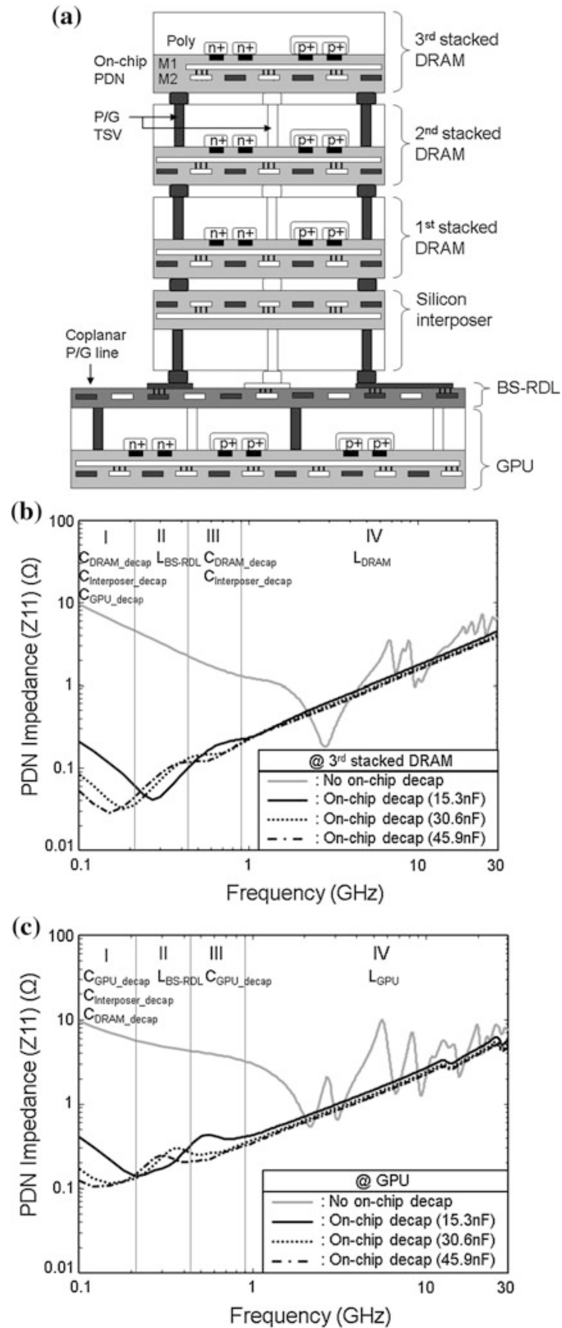


Fig. 6.34 **a** The cross-sectional view of the TSV-based GPU system consisting of three vertically stacked DRAMs with TSVs. The stacked DRAMs are connected to the GPU by TSVs, a silicon interposer, and a BS-RDL. The on-chip PDNs in the DRAM, the GPU, and the silicon interposer are also stacked and connected by P/G TSVs and coplanar P/G lines in the BS-RDL [24]. **b** The PDN impedance curves observed at the PDN in the third stacked DRAM for a variation in the ratio of the PDN area in which on-chip decoupling capacitors were embedded to the whole PDN area [24]. **c** The PDN impedance curves observed at the PDN of the GPU in the TSV-based GPU system for a variation in the ratio of the PDN area in which the on-chip decoupling capacitors were embedded to the whole PDN area [24] © 2010 IEEE

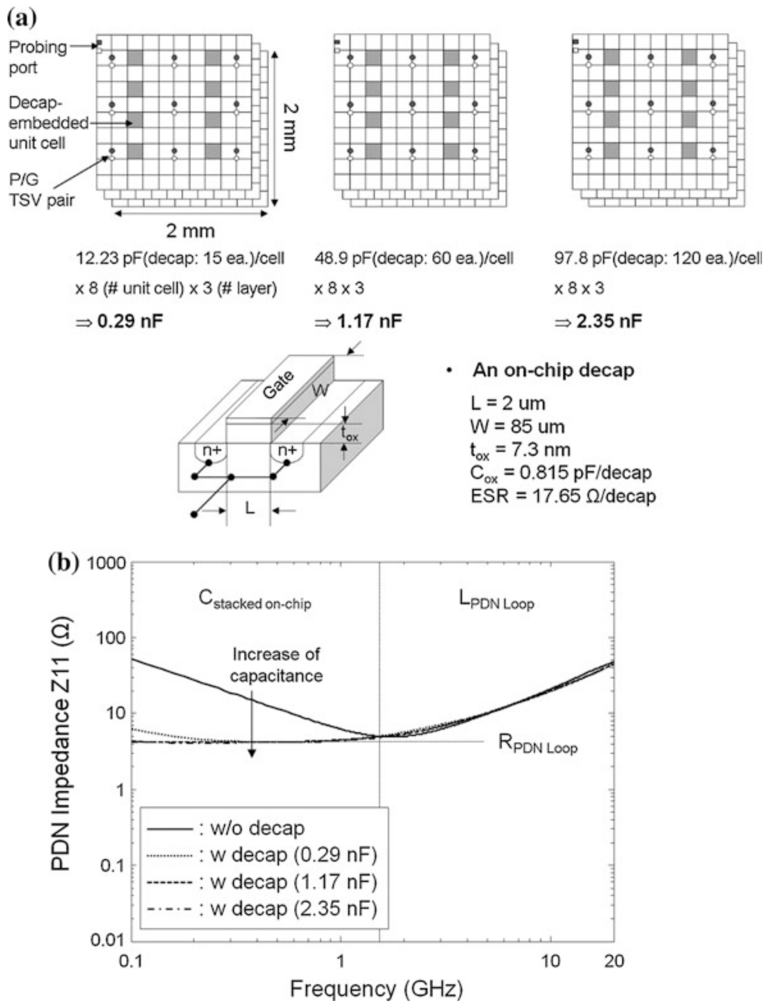


Fig. 6.35 **a** A triple stacked on-chip PDN including the on-chip decaps. To analyze the effect of varying the capacitance of the on-chip decaps, we vary the number of on-chip decaps embedded in the 3D stacked on-chip PDN [12]. **b** The PDN impedance curves for a variation in the capacitance of the on-chip decaps. As the capacitance of the on-chip decaps increases, the PDN impedance is greatly reduced in the low frequency range below 2 GHz. However, the reduction is bounded by the loop resistance of the PDN [12] © 2012 IEEE

change in the number of the on-chip decaps. The solid line represents the impedance curve of the triple-stacked on-chip PDN including no on-chip decap, the dotted line represents the impedance curve of the PDN including on-chip decaps with capacitance of 0.29 nF, the dashed line represents the impedance curve of the PDN including on-chip decaps with capacitance of 1.17 nF, and the dash-dot line represents the impedance curve of the PDN including on-chip decaps

with capacitance of 2.35 nF. When the total capacitance caused by the on-chip decaps increases, the PDN impedance decreases, as shown in Fig. 6.35b.

However, the reduction in the PDN impedance is bounded by the loop resistance $R_{PDN\ Loop}$ of the PDNs. Thus, increasing the total capacitance to more than a certain level does not help to further reduce the PDN impedance according to Eq. (6.33).

$$C_{on-chip\ decap} = \frac{1}{2\pi \times f_{min} \times R_{PDN\ loop}} - C_{stacked\ on-chip\ PDN\ (w/o\ decap)} \tag{6.33}$$

In this equation, $C_{on\text{-}chip\ decap}$ represents the capacitance required from the on-chip decaps to achieve the impedance reduction. $C_{stacked\ on\text{-}chip\ PDN\ (w/o\ decap)}$ represents the capacitance of the metal structure without on-chip decaps. $R_{PDN\ Loop}$ represents the loop resistance of the PDN. f_{min} represents the lowest frequency in the target frequency range.

We can estimate the loop resistances of 3D stacked on-chip PDNs using the impedance estimation based on the proposed model. With the estimated resistance and Eq. (6.33), we can determine how much capacitance of the on-chip decaps is required to reduce the PDN impedance in the target frequency range. Therefore, this approach can be used to efficiently design the on-chip decaps embedded in 3D stacked on-chip PDNs.

For the PDNs shown in Fig. 6.35a, $C_{stacked\ on\text{-}chip\ PDN\ (w/o\ decap)}$ is 31.83 pF, $R_{PDN\ Loop}$ is approximately 5 Ω, and f_{min} is 0.1 GHz. Using these values and Eq. (6.33), $C_{on\text{-}chip\ decap}$ is calculated to be 0.286 nF. As shown in Fig. 6.35b, the impedance of the PDN including the on-chip decaps with capacitance of 0.29 nF is almost identical to the impedances of the PDNs including the on-chip decaps with capacitances of 1.17 and 2.35 nF. These values are four times and eight times the calculated on-chip decap value, respectively. From this result, we conclude that the design approach is realistic and effective.

6.4 Summary

In this chapter, we introduced the PDNs in TSV and interposer-based 3D ICs. The PDNs in TSV and interposer-based 3D ICs are conventionally composed of several on-chip PDNs, an interposer PDN, many P/G TSV and bumps, and on-chip decaps. Because these PDNs are quite entangled in the 3D ICs, it is more difficult to design the PDNs in the 3D ICs. Therefore, we introduced a modeling method for the PDNs a grid-type PDN for the on-chip and interposer PDNs, P/G TSVs and bumps, and on-chip decaps and analyzed the effects of variations in the common design parameters.

First, we introduced the model of the grid-type PDN for the on-chip and interposer PDNs. Because the grid-type PDN plays a significant role in the power distribution in 3D ICs, the accurate and efficient modeling of grid-type PDNs is

necessary. Therefore, we introduced the model. Additionally, with the introduction of the model for the P/G TSV and bumps, we introduced the modeling method for TSV-based stacked grid-type PDNs. In 3D ICs, with IC stacking, the grid-type PDNs such as the on-chip PDNs and interposer PDN are vertically stacked. It is necessary to model the TSV-based grid-type PDN. These modeling methods we introduced are based on a structural decomposition into certain lower-level PDNs. After modeling the decomposed sections, we connect all the decomposed PDNs based on a segmentation method to model the whole PDN. The matrix-based calculation using a segmentation method accelerates the calculation speed for the PDN impedance estimation. By comparing the PDN impedance curves and simulation time obtained from the proposed models, simulations, and measurements, we successfully verified the accuracy and efficiency of the proposed models. Through these verifications, we conclude that the proposed models can be powerful and target-flexible models.

By using these verified models, we estimated and analyzed the PDN impedance curves with respect to the main design issues, namely, variations in the horizontal size of the grid-type PDNs, the number of P/G TSVs in TSV-based stacked grid-type PDNs, and the capacitance of the on-chip decaps embedded in TSV-based stacked grid-type PDNs. From these analyses, we can understand the characteristics of the PDNs in TSV-based stacked grid-type PDNs and use the characteristics for the practical design of the PDNs in TSV and interposer-based 3D ICs.

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Chapter 7
TSV Decoupling Schemes

Eunseok Song, Jun So Pak and Joungho Kim

Abstract Three-dimensional (3D) through silicon via (TSV) technologies promise increased system integration at lower cost and reduced footprint, as well as increased system bandwidth. Three-dimensional TSV may be implemented by simply adapting current silicon fabrication and package technologies. There is a strong demand for 3D, high-density and the heterogeneous integration of silicon and passive components because 3D integrated circuit (3D ICs) increase layout complexity due to the needs for additional solution space, as well as increased power density and power noise issues. To overcome the I/O speed limitation related to the above power problems in 3D ICs, on-chip decoupling capacitors and passive components used in the packaging have been implemented using TSV technologies. In this chapter, TSV decoupling schemes are introduced, showing that they have prominent advantages relative to reducing the inductive power distribution network (PDN) impedance and suppressing power noise such as the simultaneously switching noise (SSN) in the 3D ICs.

Keywords 3D integrated circuit · Decoupling capacitor · Decoupling capacitor stacked chip · Deep trench (DT) capacitor · Low equivalent series inductance · Off-chip discrete decoupling capacitor · On-chip NMOS capacitor · Power distribution network · Power/ground noise · Power integrity · Self-impedance (Z_{11}) · Stacking · Simultaneous switching noise · Through-silicon-via

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7.1 Introduction

7.1.1 Power Delivery Networks and Power Integrity Issues

In general, an ideal PDN must have a constant voltage potential. However, a real PDN exhibits supply voltage fluctuations and differences in the scale of supply voltage ripple depending on the PDN design. The supply voltage fluctuations occurring in PDNs are called SSN, and these variations are proportional to the inductance of the PDN. Thus, it is important to minimize the inductance of PDN and its associated impedance. It is understood that the characteristics of PDN can be analyzed using these impedances. For a given switching current, the reduction in the impedance of the PDN will also decrease the supply voltage fluctuations. The advantage of TSV is that this technology minimizes the inductance of PDNs because of the minimal lengths of the interconnections in the 3D IC chips. Thus, it is expected that TSV technology in 3D ICs will yield excellent electrical performances, improving signal integrity and enhancing power stability. The characteristics of a PDN determine power noise margins when switching circuits in 3D ICs are being operated. Therefore, the high-speed ICs require a more robust PDN design. The power integrity issues are generated due to various noise sources, such as SSN, IR drops and noise coupling from other power supplies. Those power supply noise sources result in signal degradations, such as slow slew rate, increased timing jitter and decreased voltage margin, due to the degraded clock performance. To minimize power supply noise and to guarantee the power integrity of a system, it is important to apply smart PDN impedance design methodologies that incorporate decoupling capacitors with TSV technology.

7.1.2 Need for Decoupling in 3D Integration

A decoupling capacitor scheme is the most prevalent solution for maintaining a robust PDN design. Decoupling capacitors have been used both on- and off-chip for over 30 years. The decoupling capacitor solution provides a low impedance path by shunting (i.e., bypassing) high-frequency noise on the supply to the ground potential and vice versa. When deployed as part of an isolation circuit between a noise-generating circuit and a noise-sensitive circuit, the decoupling capacitor serves to “decouple” or isolate the noise from the sensitive circuits; thus, the terms bypass and decoupling are used interchangeably for these capacitors. The decoupling capacitor scheme is classified into different types according to frequency ranges. With respect to a frequency band within several tens of MHz, a decoupling scheme will likely use discrete capacitors mounted on a system-board, while on-package decoupling capacitors are typically used to decrease PDN impedances when the frequency band is on the order of hundreds of MHz. On-chip MOS capacitors are generally used for decoupling purposes for the GHz high-

frequency band. Each decoupling capacitor scheme has their own set of advantages and disadvantages. In particular, these schemes exhibit limitations in a system-board, which has large inductances in high-speed digital circuits, and an on-package decoupling capacitor solution. In the case of the on-chip MOS decoupling capacitors, a large chip area is required to increase the capacitance of the PDN. Additionally, the conventional system-board and on-package decoupling capacitor schemes are not easily adapted to the 3D ICs case. Although the on-chip MOS capacitors can be incorporated into DDR3 memory and application processor (AP) chips through a standard CMOS process, the capacitance of the on-chip MOS capacitor is not sufficient. Therefore, a specific decoupling capacitor scheme suitable for the structure of a 3D integration system is required.

7.1.3 Advantages of the Decoupling Capacitor Solution

The best way to reduce power noise is to redesign the entire PDN (which consists of chips, packages, and system-boards) such that it incorporates a low impedance power distribution characteristic. Relative to the impedance of a PDN, the lower the inductance and the larger the capacitance of the PDN are, the lower the impedance for the PDN. Theoretically, the target impedance is determined by the allowable supply voltage ripple and operating frequency. These items become the criteria for judging whether power noise margins are exceeded. It is important to obtain a PDN design with a low impedance level to satisfy the target impedance. However, there exist limitations to reducing the inductance of a PDN in real products due to constraints related to the electrical performance of the entire system. As the optimization of the PDN impedance of a 3D integration system is performed, it is important that the PDN impedance is minimized in the frequency band of interest by using an appropriate decoupling capacitor scheme. An advantage of the decoupling capacitor scheme is that it is easier to control PDN capacitances than PDN inductances. A decoupling capacitor scheme enables the placement of capacitors in desired locations. In this work, capacitance values and various decoupling capacitor types were parameters is our studies that have been conducted. Although it is possible to install many capacitors on system-boards and in packages and chips, they can increase the cost of the entire system. The TSV technology-based 3D ICs structure is a promising 3D packaging technology that can largely mitigate PDN inductance issues. As TSV is applied instead of other technologies (such as bond-wire and C4 bumps for 3D packaging), it is expected that the electrical performance in a system that has many I/Os, high-bandwidth requirements with terabyte throughputs and a high-speed system is largely improved. A decoupling capacitor scheme that is suitable for the 3D ICs structure is not easy to implement due to the large size of the requisite on-chip MOS capacitor that conflicts with the budget of chip areas. Thus, a compatible decoupling capacitor scheme for the 3D ICs is required to maximize the electrical performance of the TSV-based, 3D ICs structure.

7.2 Decoupling Capacitor Schemes

The conventional decoupling capacitor schemes are classified into three different capacitor-deployment topologies, such as system-board decoupling capacitors, on-package decoupling capacitors, and on-chip decoupling capacitors. The system-board decoupling capacitors usually consist of various discrete capacitors. For the case of the low equivalent series inductance (ESL) type capacitor, it can be used up to a frequency band with several tens of MHz. The on-package decoupling capacitors are divided into two different types; one is installed on a package PCB, and the other is embedded inside of a package PCB core. The embedded decoupling capacitors exhibit a slightly lower ESL and can usually be used up to a frequency band spanning hundreds of MHz. Finally, the on-chip decoupling capacitors are implemented using standard CMOS fabrication processes and are limited by available chip area. The capacitance values range from several pF to several tens of pF. However, it is possible to use these capacitors in a frequency band up to several GHz because the ESL of the on-chip decoupling capacitors is very small.

It is imperative to use on-chip decoupling capacitors because they can significantly reduce interconnection ESL. This will ensure the chip performance of devices such as a mobile application processor, which has a system bandwidth of hundreds of gigabytes. Previous studies have demonstrated the effect of on-chip decoupling capacitance for switching circuits. A critical shortcoming of this approach is the relatively low capacitance value associated with the on-chip capacitance. The amount of on-die capacitance can be increased, but this option would compromise the amount of real estate available for other circuitry. To provide effective decoupling above several hundreds of MHz, the total capacitance of the on-chip capacitors must be increased without increasing the chip area. Capacitors suitable for implementing such a decoupling solution on chips are metal oxide semiconductor (MOS) capacitors, metal-insulator-metal (MIM) capacitors, and deep trench (DT) capacitors [1–3]. MOS capacitors have been the most popular choice for the decoupling solution. To realize tens of nF capacitance values within chips, several mm^2 chip areas are needed. Additionally, in terms of chip area consumption when using MOS capacitors compared to the chip area needed when using MOS capacitors in 3D ICs, increased chip size may be warranted due to the additional die area required for TSV.

As DRAM technology continues to be scaled, the leakage current in MOS capacitors is increasing exponentially. Thus, an increase in the power loss of the whole chips is observed due to the relatively large leakage current compared to that of MIM and DT capacitors. However, MIM capacitors exhibit very small leakage currents for the same capacitance density. When implementing capacitors possessing tens of nF capacitance values on a BEOL layer, several mm^2 chip areas are required, as is the case for MOS capacitors. There is however a serious routing issue because the on-chip metal routing cannot be applied to an MIM capacitor realized on a BEOL layer. To increase MIM capacitances within the same chip

area, it is necessary to use a material with a high dielectric permittivity, and an additional process step will be necessary.

For CMOS technology beyond 32 nm, it has been shown that DT capacitors provide relatively high capacitances, exhibit low leakage currents, and have chip area requirements compatible with our decoupling solution [4]. Approximately 10 % of the chip area needed for MOS or MIM capacitors is required to implement tens of nF capacitances within chips (approximately 200 nF/mm^2). Another advantage of DT capacitors is that they reduce power loss in the chips because the leakage current is significantly lower relative to MOS capacitors. Although DT capacitors exhibit several advantages pertaining to leakage currents, capacitances, and chip areas, they represent a significant physical barrier in TSV arrangements. Thousands of TSVs will be needed for high performance processor applications with system bandwidths of hundreds of gigabytes and DRAM chips. It is difficult to ensure that a sufficient chip area will be available for implementing DT capacitors having tens of nF capacitances within a chip that includes thousands of TSVs. Thus, it is necessary to design new decoupling capacitors that provide excellent performance with respect to leakage currents, capacitances, low ESL, chip areas, and routability such that they are compatible with a 3D IC structure.

7.2.1 Issues with SMD Capacitors

Surface-mount device (SMD) capacitors are usually installed on system-boards as shown in Fig. 7.1, and the capacitance of discrete capacitors can range up to several tens of μF. However, a disadvantage of these capacitors is that they exhibit very large ESL with increasing capacitances compared to other decoupling capacitors. The ESL in these capacitors is typically several nH, and these capacitors are suitable provided that frequencies are within the range of several MHz to several tens of MHz. Additionally, these capacitors are usually mounted on a PCB and are difficult to install in 3D IC structures. In addition, due to the frequency band limitations, it is difficult to apply these components as decoupling capacitors for high-speed chips.

7.2.2 Embedded Decoupling Capacitor

Embedded decoupling capacitors are usually embedded into the core material of a PCB. It is a structure that is used to reduce the ESL of system-boards or on-package decoupling capacitors. This can result in a complex PCB process that requires thin discrete capacitors. Although the frequency bands of these capacitors are similar to those of SMD capacitors, i.e., several tens of MHz to several hundreds of MHz, it is difficult to apply them to practical products because of the complex process and high-cost associated with PCB fabrication. In addition,

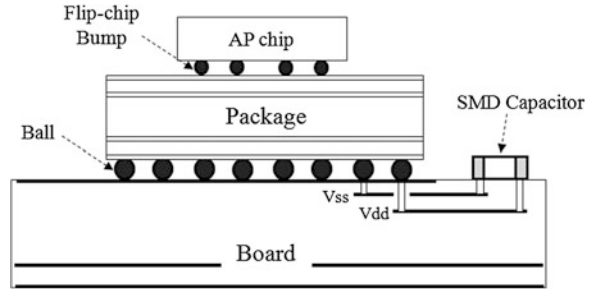

Fig. 7.1 SMD decoupling scheme in today's system

because embedded decoupling capacitors cannot be embedded in silicon, it is not an applicable structure for 3D IC topologies.

The advantages of using thin dielectrics in high performance systems are low power distribution network impedance, reduced power system noise and decreased electromagnetic interference (EMI). They also provide the opportunity to have additional power or signal layers within an available board thickness, along with the potential to reduce the number of discrete capacitors. While system clock rates have increased, logic voltages have decreased and switching currents have increased. Lower noise levels and improved power system integrity became essential, resulting in even thinner dielectrics (i.e., as small as 5–10 μm in thickness). Higher dielectric constant materials have also become available for lower impedance applications. Acting as parallel plate capacitors, the thinner layers and increased dielectric constant provide a significant increase in capacitance, and the planes used in power distribution networks reduce inductance and resistance [5]. An effective, embedded passive solution that directly embeds discrete surface-mount capacitors into the package substrate is presented Fig. 7.2. Compared with an embedded planar capacitor, the embedded discrete capacitor technology in the package substrate offers more design flexibility and lower PDN impedance to facilitate decoupling. The discrete capacitors can be placed under the chip to reduce the loop inductance. Cheng et al. [6] have presented a characterization of embedded discrete capacitors in a multi-chip package (MCP). The chip, package and print circuit board (PCB) co-simulation to obtain a well-designed, embedded discrete substrate is demonstrated. The performance of a PDN is studied in both the frequency and time domains. The peak-to-peak noise in the PDN has been reduced substantially through this design and characterization methodology [6]. Thick-core dielectric layers in the PCB package or system-board can be used for decoupling purposes, as shown in Fig. 7.2. It is noted that embedded discrete capacitors can be realized in these layers. These capacitors have different capacitances and resonate at frequencies ranging from 100 MHz to 2 GHz.

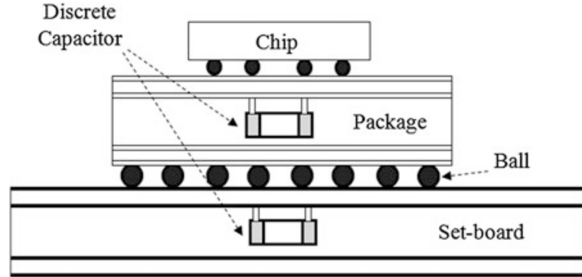

Fig. 7.2 A typical cross-section of a package PCB and board with embedded capacitors

7.2.3 *On-Chip Decoupling Capacitors*

7.2.3.1 MOS Capacitor

Because on-chip MOS decoupling capacitors exhibit very low ESL values of only a few pH, compared to the decoupling capacitors installed on PCBs, they are better suited for the high-speed chips having a frequency band of several GHz. In addition, they possess another advantage in that an extra fabrication process step is not required because MOS capacitors can be implemented using the standard CMOS process. However, area on the IC must be reserved for the MOS decoupling capacitors because these capacitors are to be implemented on the chips. To achieve large capacitances, it is necessary to ensure that a large chip area in proportion to capacitances is available. For instance, to obtain a 10 nF capacitance using the on-chip MOS decoupling, a chip area of several mm^2 is required. On-chip MOS decoupling capacitors different from the decoupling capacitors implemented on PCBs represent a decoupling scheme that can be used in 3D IC structures and that makes it possible to apply them to each chip packaged on the 3D ICs. However, because the capacitance of the MOS decoupling capacitors used in each chip is relatively low, additional decoupling capacitors are required for the 3D IC packaged with the chips, which have numerous I/Os and terabyte bandwidths. In addition, in the case of on-chip decoupling capacitors, equivalent series resistance (ESR) should be considered because silicon conductor materials exhibit large losses. MOS-based decoupling capacitors can be implemented as NMOS decoupling capacitors, pMOS decoupling capacitors, or a combination of these as CMOS decoupling capacitors, as described in Fig. 7.3. CMOS decoupling capacitors are commonly used within standard cells because a portion of the area within these cells is typically reserved for pMOS transistors, and a separate region is reserved for NMOS transistors [7].

Today, in a standard CMOS 32 nm technology, the gate oxide layer provides the thinnest dielectric layer. Therefore, the MOS-based decoupling capacitors are the most area-efficient and most commonly implemented structures. One drawback of these decoupling capacitors is the resulting leakage current that increases exponentially with decreasing oxide thickness. For designs in which leakage

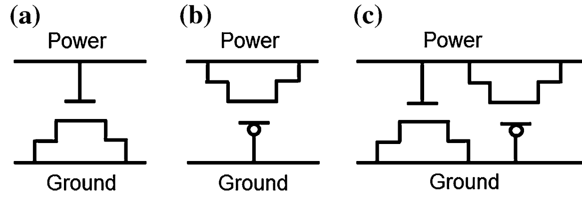

Fig. 7.3 Configurations for an **a** NMOS capacitor **b** pMOS capacitor, and **c** CMOS capacitor

currents are an important consideration, thick oxide MOS devices can be used to minimize the leakage across the gate oxide layer. The oxide thickness in these devices is typically three times that of their standard counterparts. An expected drawback of this implementation is associated with the reduction in capacitance per unit area.

7.2.3.2 MIM Capacitor

One solution to effectively reduce chip supply voltage fluctuations is to use on-chip metal-insulator-metal (MIM) decoupling capacitors to supplement the existing system package and board level capacitors. Operating frequency and instantaneous power demands are rapidly reducing the effectiveness of these off-chip capacitors at the 90 nm node and beyond. MIM capacitors based on laminate metal-oxide dielectrics have recently achieved high capacitance density and low leakage current density (Fig. 7.4).

However, their application as bypass capacitors to limit voltage transients globally over the chip power distribution grid can be challenging due to defects that occur during their integration into the copper/low-k backend. Roberts et al. [8] have reported the first successful implementation of large area MIM capacitors in the power grid of a 90-nm silicon-on-insulator (SOI) microprocessor. The results show that the inclusion of the on-chip MIM decoupling capacitor can boost system performance by approximately 10 % at the 90 nm technology node.

The need for improved on-die power supply integrity increases with technology advances due to large demand on the power supply network to instantaneously provide large currents. The problem is due to the L*di/dt voltage droops induced by the effective inductance of the package power pins. Packaging technology can only provide partial relief to solve the inherent problem associated with the instantaneous delivery of current. Active circuitry can alleviate the problem, but this solution may result in a high-cost circuit design and increased development costs. This problem is further exacerbated in SOI for small, fast die due to the inherent junction capacitance and well-capacitance loss relative to the bulk silicon. Sanchez et al. [9] have reported results of the implementation of a massively pervasive on-die metal high-k insulator-metal decoupling capacitor (high-k MIM capacitor) for improved processor core maximum frequency.

An MIM capacitor's density can be increased by using a multi-layer structure. However, this multi-layer MIM structure is not easily attainable in the monolithic

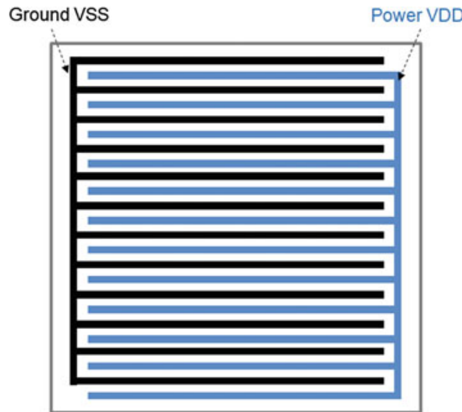

Fig. 7.4 Implementation of the single MIM capacitor in a chip produced up to an approximately 250 nF capacitance. Capacitances of SiO_2-based substrate capacitors, which are in parallel with the MIM, are approximately 25 nF in a 90 nm chip

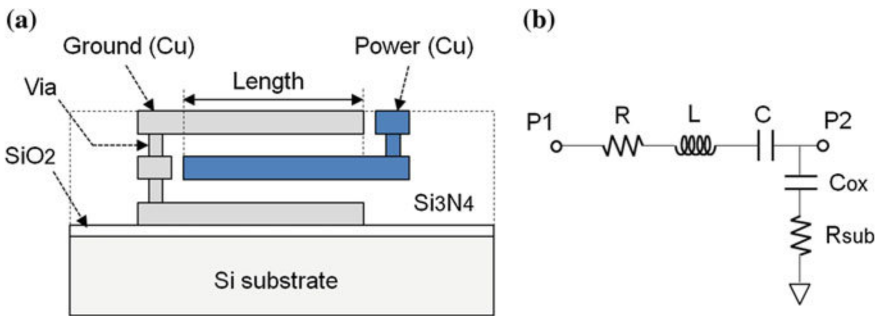

Fig. 7.5 **a** Cross-sectional view of an MIMIM capacitor on a Si substrate and **b** electrical model of the MIMIM capacitor

form because the multi-layer MIM capacitors in the complex CMOS IC process are not available. A two-layer capacitor using metal-insulator-metal-insulator-metal (MIMIM) in the Cu/SiO_2 interconnect structure has been implemented using CMOS IC technology. Figure 7.5 shows the cross-sectional view of an MIMIM capacitor on a Si substrate and a simplified electrical model of the MIMIM capacitor. The dielectric material of the MIMIM capacitor is Si_3N_4 [10].

In general, MIM capacitors have a 0.1–0.3 μm thick layer of SiN_4, which provides a capacitance density of several hundreds of pF/mm^2 and a breakdown voltage in the range of 50–100 V. The capacitance per unit area can be increased by either using ultra-thin films or by employing high dielectric constant materials. Therefore, to maximize the capacitance per unit area of a decoupling capacitor, a thin dielectric (and/or large permittivity material) is desired. A shortcoming of

using a thin dielectric is the resulting tunneling leakage current. The leakage power consumption by the decoupling capacitors typically contributes 10–20 % of the overall power budget of a chip. Not only does leakage affect the chip's power consumption, but it also reduces the effectiveness of the decoupling capacitor due to the loss of charge. The dielectric leakage effect is modeled by a resistor (R_leakage) between the supply and ground terminals.

7.2.3.3 Deep Trench Capacitor

In the last 10 years, the advances in deep Si etching technology have led to vertical DT capacitors in silicon, which provide much larger capacitance density for an available chip area, as shown in Fig. 7.6. Recently, Si-based integrated capacitors are easily available in silicon processes, which have also been used for on-chip decoupling solutions for the high-performance ICs. As silicon technology continues to scale, the deep-trench capacitors with high capacitance densities can be developed. For example, 65 nm CMOS technology can provide up to 200 nF/mm^2. DT capacitors that are realized on silicon chips as MOS decoupling capacitors offer better capacitance density, while the leakage current is much lower compared to MOS decoupling capacitors. However, a DT capacitor typically has a thicker dielectric and occupies a much lower footprint on the silicon [1, 4].

Another advantage of DT capacitors pertains to reducing the entire power loss on the chips because the leakage current is significantly lower compared with MOS decoupling capacitors. Although DT capacitors have several advantages with respect to leakage currents, capacitances, and chip areas, they represent a physical blockage for TSV arrangements. Thousands of TSVs in a 3D IC structure supporting high-performance, high-bandwidth application processors are inevitable. However, it is difficult to ensure that the chip area is available for realizing DT capacitors that have tens of nF capacitances within a chip that includes thousands of TSVs.

7.2.4 Optimal Design for Power Delivery Networks in an Interposer

To obtain desirable characteristics for a PDN in an interposer, on-chip power/ground (P/G) metal lines, TSV allocation, and decap designs should be optimized. The interposer characteristics can be largely varied according to on-chip PDN designs. In general, the design of on-chip P/G metal lines can be classified into three different types: The on-chip PDN design architecture includes meshed, ring, and finger types. Figure 7.7 depicts the on-chip PDN architecture designed using a meshed type architecture. It is a design that applies P/G TSVs at a point where P/G metal lines between the top and the bottom layers are joined. The PDN design

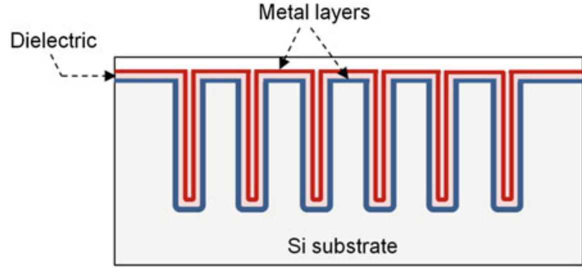

Fig. 7.6 Cross-sectional view of a Si-based deep trench (DT) capacitor

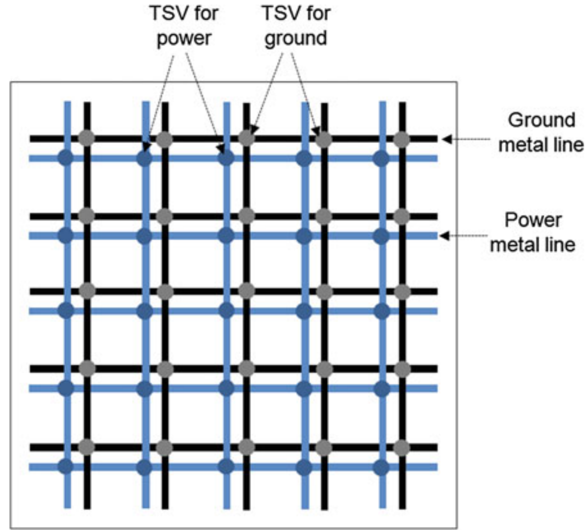

Fig. 7.7 On-chip power and ground metal lines designed to have a meshed type, which can provide easy connections from active circuits to PDNs by TSVs

using this meshed type represents an advantage relative to connecting active circuits in a chip. It also increases the capacitance of the PDN while decreasing the loop inductance between the power and ground metal lines by minimizing the distance between the power and ground conductors.

Regarding on-chip PDN design architectures, such as meshed, ring, and finger types, the power distribution technique is important because this dictates how the power is finally provided to active circuits. Because the power noise (including SSN) is proportional to PDN impedances, the PDN design may be evaluated based on whether the PDN impedances are designed to a sufficiently low level. Design architectures used in practical chips apply the meshed type architecture and produce excellent characteristics, including easy connections to decaps and active circuits. Figure 7.8 shows an example design of on-chip metal power and ground lines using the meshed type. As shown in Fig. 7.8, metal power and ground lines can be implemented as pairs and allocated using a uniform pitch. Additionally, the meshed type power and ground distribution provides easy connection in a multi-layered PDN vertically.

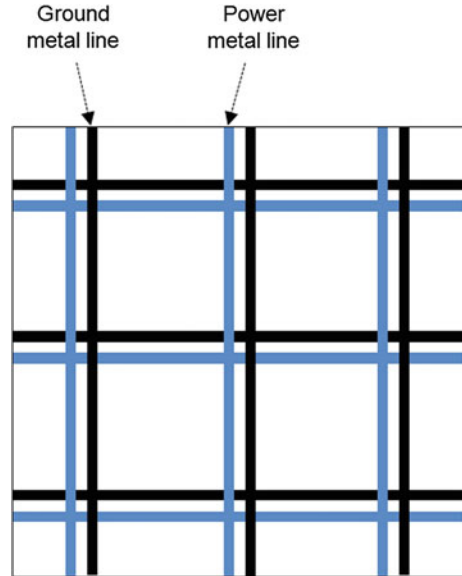

Fig. 7.8 On-chip power and ground metal lines based on a meshed type

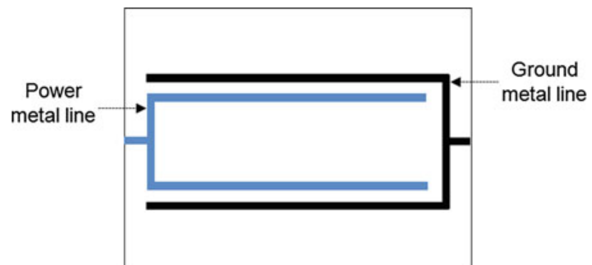

Fig. 7.9 Finger type based on-chip P/G metal lines

Another on-chip PDN design method is a finger type. As shown in Fig. 7.9, it is a method that connects power and ground lines on the same layer. On-chip P/G metal lines used in this finger type design are not appropriate for multi-layered PDNs and exhibit limitations related to the positioning of active circuits or decaps at preferred locations. In addition, they may provide a lower characteristic impedance for the PDN than the meshed type (Fig. 7.10).

Finally, a ring type is used to design on-chip metal line architectures. This method places on-chip power and ground lines in a single ring. The ring type, on-chip PDN design allocates one P/G ring on a single layer in which active circuits and decaps are usually connected through metal lines and vias. As in the case for the finger type, the PDN impedance characteristics are not excellent. Thus, an additional allocation of on-chip decaps is required to improve those characteristics. The ring type, on-chip P/G metal design is not usually applied to practical products.

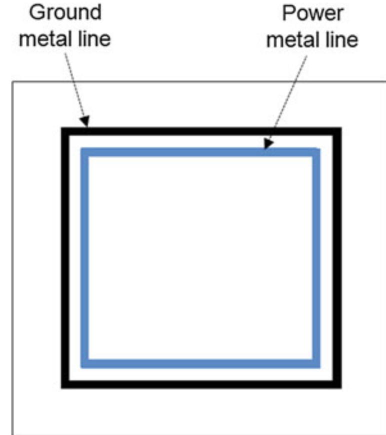

Fig. 7.10 Ring type on-chip power and ground metal lines

There are five different types of on-chip capacitors that can be implemented in interposers. Discrete capacitors, MIM capacitors, oxide capacitors (or MOS capacitors), trench capacitors, and P/G TSV decaps are used as the on-chip decaps represented in Fig. 7.11. Although these five types of on-chip capacitors utilize different manufacturing processes and exhibit a range of capacitance values and positioning constraints, any of these components may be used as decoupling capacitors. As shown in Fig. 7.11, discrete capacitors are mounted on an interposer and connected by metal lines and bumps on the interposer. Mounting these discrete capacitors on a silicon interposer has an advantage of presenting high capacitances and decreased power losses due to leakage currents. However, a process problem arises related to the mounting of a relatively thick discrete capacitor on a thin silicon interposer. MIM capacitors exhibit an architecture that can be implemented on IMD or RDL layers in a chip. In general, they can be properly used in a multi-layered metal architecture, and a dielectric material with a high dielectric constant can be applied to an insulating layer to increase the capacitance of the MIM capacitors. However, this may increase production costs because of the additional processes that are needed to implement such a high value of *k*. In the case of oxide capacitors, additional manufacturing processes may not be required because they can be implemented using a standard CMOS process. The capacitance of these oxide capacitors can be determined by the gate-oxide capacitance of MOS transistors. However, a disadvantage is that these capacitors may produce large power losses because oxide capacitors have higher channel resistances and leakage currents compared to other decaps.

Regarding the characteristics of the MIM capacitors, they show small ESR values and relatively low capacitance densities compared to oxide capacitors and discrete capacitors. Additional metal layers may be required to implement MIM capacitors in silicon interposers. Regarding the advantage of MIM capacitors, they can be implemented using low cost production techniques because there is no need for additional active processes. Additionally, MIM capacitors exhibit low power

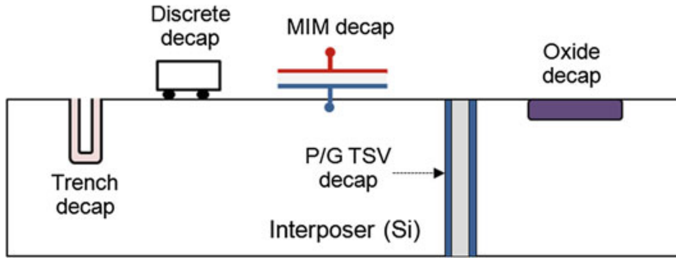

Fig. 7.11 Various types of on-chip decoupling capacitor structures

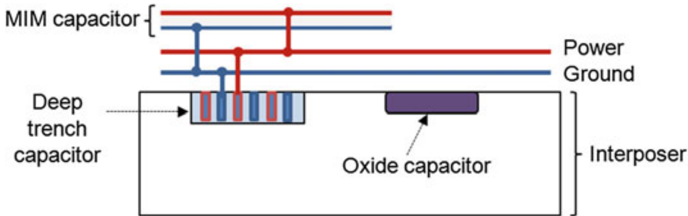

Fig. 7.12 Various decaps in interposer PDNs

loss because of their very small leakage currents. Deep trench (DT) capacitors apply a method that creates numerous holes in the silicon and generates a structure using a sequence containing a metal layer and a dielectric layer followed by another metal layer. DT capacitors increase capacitance densities by scaling the standard CMOS process down to a micro process. In this regard, DT capacitors provide an ideal tradeoff. They are realized on silicon (as are MOS decoupling capacitors), but they require a significantly smaller silicon footprint and typically have a thicker dielectric compared to MOS capacitors. Therefore, they offer better capacitance density at much lower leakage current levels. The ESR depends on the doping level in the buried plate and the resistance offered by the silicon path from the bottom plate to the actual contact.

Finally, TSV decaps represent an architecture of decoupling capacitors using P/G TSVs formed in silicon interposers. In general, for these components, the capacitance of SiO_2 surrounding TSV is dominant. Thus, capacitances are varied according to the thickness of SiO_2. Additionally, it is necessary to form thin SiO_2 or to alternatively increase the number of P/G TSV pairs to increase the capacitances in the TSV decaps. However, TSV decaps are not suitable for the ICs that require high capacitances because of their relatively low capacitance densities. Figure 7.12 shows an example of implementing various decaps in a silicon interposer.

In 3D IC systems, the architecture that laminates components incorporated into high speed digital ICs with several layers is used. The characteristics of I/Os used for digital signaling exhibit a broadband frequency component. Thus, in general, it

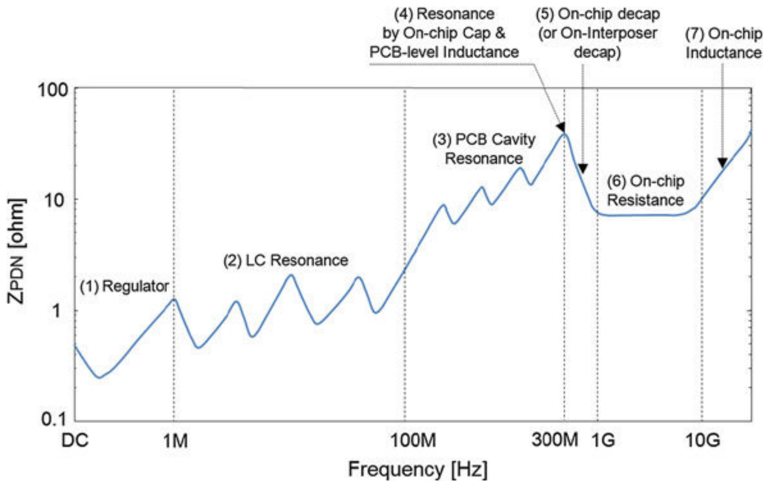

Fig. 7.13 Resonance analysis of PDN impedance and parameters according to frequency range

is necessary to decrease PDN impedance over a broadband frequency region for digital systems. Figure 7.13 shows the analysis of resonances in each frequency region and parameters causing the resonances. As shown in Fig. 7.13, the frequency region can be divided into seven different ranges, and the resonance parameters for each frequency range are as follows.

1. Regulator RC
2. LC resonance of the PCB (via, trace, ball / bump)
3. PCB cavity resonance
4. Resonance by package PCB inductance and on-chip capacitance
5. On-chip decap or on-interposer decap
6. On-chip resistance
7. On-chip inductance.

The frequency range from DC to 1 MHz corresponds to a regulator RC range, and the frequency range from 10 to 100 MHz is the dominant range for L and C resonances. Parallel resonances are generated over a band of several hundreds of MHz due to package and PCB inductances, as well as on-chip capacitances. To reduce the influences of parallel resonances, the package inductance should be minimized. Therefore, in the case of TSV-based 3D ICs, the package inductance is largely decreased down to several hundreds of pH, and the noise in the frequency range can be reduced by several hundreds of MHz. In the case where the frequency range exceeds 1 GHz, on-chip resistances dominate and result in large losses. Additionally, the impedance characteristics in the frequency range of approximately 10 GHz are dictated by on-chip inductances.

Figure 7.14 illustrates an example of designing on-chip decaps and on-chip metal lines. To minimize the impedance of the on-chip PDN, it is necessary to

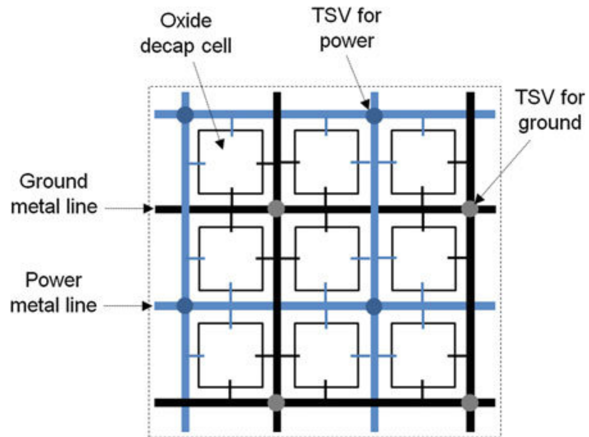

Fig. 7.14 Cell approach of oxide decaps

implement a decap cell approach and an on-chip metal design that decreases ESR and ESL. P/G metal lines are designed using the meshed type, and decap cells are allocated in each grid. Decap cells allocated in each grid are connected to adjacent power and ground lines. By utilizing smaller loop sizes in the grids, it is possible to minimize ESL values in the on-chip PDN. Additionally, metal power or ground lines form TSV at a cross point between the top and bottom layers, which creates a vertical connection. In addition, regarding the method that reduces the impedance of the PDN, the total ESR and ESL are to be reduced by allocating as many P/G TSVs as possible.

7.3 Application and Design of TSV-Based Decoupling Schemes

7.3.1 Introduction

The main drivers for the development of three-dimensional (3D) stacking technologies are the need to reduce form-factors, solve narrow-band chip-to-chip interconnect issues, and enable heterogeneous integrations over limited areas. A primary objective of 3D stacking is to increase the number of active layers by using different technologies and functions. Thus, a 3D system with high-density vertical interconnects is indispensable. TSV, a state-of-the-art, vertical interconnect technology, provides numerous benefits. These benefits include high density, low power, a low-skew 3D clock delivery network (CDN), and the wide-bandwidth interconnects inherent to 3D systems. Several challenges arise, such as the design issues associated with a low-cost 3D TSV, mechanical issues, thermal integrity issues, ESD, and power noise coupling concerns [11–16]. In addition,

TSVs should exhibit the lowest PDN impedances, ensuring sufficient margins of SSN in 3D ICs. Therefore, TSV has emerged as a promising solution for achieving 3D systems in future electronics markets, such as mobile processors, high-end computers, flat-panel high-definition TVs (HDTVs) and health care [17].

Because TSV-based 3D ICs include high-speed and high-current integrated circuits (ICs), the distribution of stable power supply voltages and the suppression of SSN pose critical design challenges. A clean power supply can be maintained in a 3D IC by designing a PDN with the lowest possible impedance [18, 19].

If only one of the 3D chips is switching, the noise is smaller than that of a single-IC because the switching chip can use the decoupling capacitors (decaps) of the other non-switching chips. Normally, the activities of several blocks having equivalent footprints are highly correlated because one of the main purposes of a 3D IC is to position the blocks that communicate with each other as closely as possible to one another. However, we must consider the worst-case scenario in which all of the chips are switching because the power noise produced in a 3D IC must not be greater than that of a single-IC. This consideration is especially true for the topmost chip that contains very power-hungry blocks, which may cause the noise level to change dramatically. A robust PDN design can even be obtained for the bottommost chip by adding more decoupling capacitors in an on-chip PDN or by adding more P/G pads [20]. In 3D nano-electronic systems, a power-integrity problem arises from the third dimension: thus, we can also push the search for solutions into the third dimension. Three-dimensional ICs make floor-planning much more difficult because the multi-tier structures dramatically enlarge the solution space and the increased power density accentuates the power noise issue. Therefore, moving to 3D IC designs greatly increases the complexity involved in developing a solution to the power integrity problem. To reduce power noise levels, particularly SSN, decoupling capacitors are strategically placed in 3D IC PDNs.

The effect of off-chip surface-mount discrete decoupling capacitors appears at frequencies less than several hundred megahertz (MHz) due to the increased effect of the loop inductance associated with the current flow between the capacitors and the switching circuits. A methodology that places the decoupling capacitors as close to the switching circuits as possible should reduce the loop inductance.

One possible solution to the power integrity problem is to provide on-chip decoupling capacitors for use above 100 MHz. Previous work has demonstrated the effect of on-chip decoupling capacitance for switching circuits [21]. A critical shortcoming of this approach is the low capacitance value associated with the on-chip capacitance. The amount of on-die capacitance can be increased, but this option would compromise the amount of real estate available for the logic circuits. To provide effective decoupling above 100 MHz, the total capacitance of the on-chip capacitors must be increased without increasing the chip area. Another approach is to include embedded capacitors within a PCB package or thin-film circuit [22]. This decoupling solution employs discrete thick- or thin-film capacitors arranged in a capacitive array that can be used within a package to provide decoupling for high-performance circuits within the frequency range spanning

100 MHz to 2 GHz [23]. Although the thin-film embedded capacitor can significantly reduce the loop inductance between the switching circuits and decoupling capacitors, it is difficult to implement this architecture in 3D integration systems.

Conventional bond wire interconnections for the power and ground delivery networks in 3D stacked packages, including system in package (SiP) and package on package (PoP) designs, can generate significant SSN above a frequency of a few hundred MHz due to a large loop inductance (on the order of nH). Although 3D stacked packages have on-package decoupling capacitors to enhance the SSN margin by providing a low-impedance power supply and return current paths, the suppression effect of the discrete decoupling capacitors is not sufficient above a few hundred megahertz due to the large equivalent series inductance (ESL) [24].

In this chapter, we introduce a new TSV-based decoupling capacitor stacked chip (DCSC) that overcomes the disadvantages of the conventional decoupling capacitor solutions [25]. A new DCSC based on extra decoupling capacitors and TSVs is introduced to overcome the narrow-bandwidth limitation of the conventional decoupling capacitor solutions in 3D ICs, exhibited by the low capacitance of the on-chip MOS decoupling capacitors and the high inductance of the off-chip discrete decoupling capacitors. The TSV-based DCSC can be realized by mounting decoupling capacitors, such as silicon-based MOS capacitors and discrete capacitors, on the backside of a chip and then connecting them to the on-chip PDN through TSVs.

The TSV-based DCSC achieves a lower PDN loop inductance than the conventional decoupling capacitor solutions by using TSV technologies between the on-chip P/G metal layers and decoupling capacitors stacked on the backside of the chip. The TSV-based DCSC also achieves the largest capacitance by using extra decoupling capacitors, such as silicon-based MOS capacitors and discrete capacitors. Thus, the TSV-based DCSC has the advantages of low on-chip level ESL (under several tens of pH) and high off-chip level capacitance (up to several μF). Consequently, the TSV-based DCSC in 3D ICs can provide a lower PDN impedance level than the conventional decoupling capacitor solutions over a wide range of frequencies. While the TSV-based DCSC exhibits certain advantages over on-chip MOS capacitors, such as an ESL of less than 50 pH, it also exhibits some disadvantages of on-package decoupling capacitors, such as a high inductance of several nH. Furthermore, it exhibits the advantages of on-package decoupling capacitors, such as a high capacitance (several μF). This feature is a weakness of on-chip MOS capacitors, which have a low capacitance of less than 0.2 μF. Although there are currently some challenges with regard to manufacturing and cost, this approach represents an adaptable, competitive technology compared to the other decoupling solution methods. The most important attribute of the DCSC structure is its use as a 3D PDN enhancing technology for 3D IC systems.

The core concept of the TSV-based DCSC is to propose a new decoupling capacitor structure that has the advantages of both on-chip MOS capacitors and off-chip decoupling capacitors. The DCSC structure is also a new decoupling capacitor solution that is easy to apply to 3D IC systems and provides enhanced 3D PDN characteristics using TSV technology. The TSV-based DCSC is more

effective than the conventional decoupling capacitor solutions because the on-chip PDN has a lower inductive impedance level. Furthermore, it has the advantage of being able to select both the capacitance value of the decoupling capacitors layered on the backside of the chip and the capacitor type according to the operational characteristics of the chip. The TSV-based DCSC introduced in this study decreases not only the high capacitive impedance, which is the disadvantage of on-chip MOS capacitors, but also the high inductive impedance, which is the disadvantage of off-chip decoupling capacitors. In other words, this structure represents the advantages of on-chip MOS capacitors and off-chip decoupling capacitors and is a new and appropriate decoupling solution that overcomes their disadvantages.

7.3.2 Design of Decoupling Technologies Using TSV (Decoupling Capacitor Stacked Chip)

As on-chip decoupling capacitors generally have a low inductance, they are effective in improving power noise such as SSN. However, they have the disadvantage of increasing the capacitance value for a specific level due to the limitation of chip area that contains the MOS transistors. In contrast, off-chip decoupling capacitors provide a very high capacitance using extra discrete capacitors. However, the relatively large loop inductance of the PDN makes these capacitors vulnerable to high frequency noise. In this chapter, we introduce the TSV-based DCSC that provides the advantages of a low on-chip ESL level and a high off-chip capacitance level. While the TSV-based DCSC exhibits certain advantages of on-chip MOS capacitors, such as an ESL of less than 50 pH, it also exhibits some disadvantages of on-package decoupling capacitors, such as a high inductance of several nH. Furthermore, it exhibits the strength of on-package decoupling capacitors, such as high capacitance values approaching several μF. It is noted that this feature is a weakness of on-chip MOS capacitors, which have relatively low capacitance values of less than 0.2 μF.

In this section, the basic ideas of the TSV-based DCSC are presented. Figure 7.15 shows the basic conceptual structure of the face-down TSV-based DCSC. As depicted in Fig. 7.15, the TSV-based DCSC uses decoupling capacitors such as silicon-based MOS capacitors or discrete capacitors mounted on the backside of a chip, and they are connected to the on-chip PDN through TSV technology. Thus, the TSV-based DCSC can provide a lower equivalent series inductance (ESL) than the conventional decoupling capacitor solutions by using TSVs between the on-chip PDN and decoupling capacitors. Furthermore, it achieves a larger capacitance by using additional decoupling capacitors in 3D IC systems. To guarantee the routability of signal I/Os in the 3D integration system, TSV-based DCSC should be stacked in a face-down manner (flip-chip).

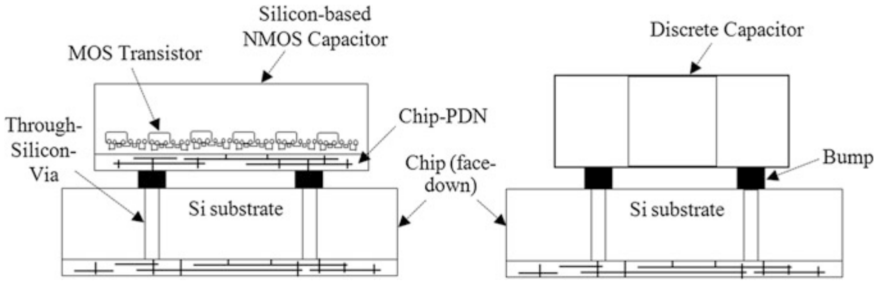

Fig. 7.15 Basic conceptual structure of the face-down TSV-based DCSC [25] © 2013 IEEE

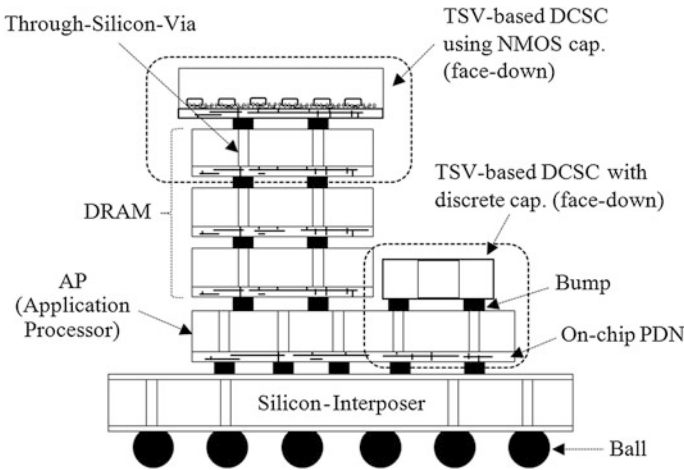

Fig. 7.16 Application and implementation of the face-down TSV-based DCSC in the 3D integration system [25] © 2013 IEEE

Figure 7.16 provides a schematic of the TSV-based DCSC's structure and its implementation in 3D ICs. As shown in Fig. 7.16, TSV-based DCSCs can be used in various 3D stacked structures, and the decoupling capacitors, which can be either silicon-based MOS capacitors or discrete decoupling capacitors, are positioned in a face-down manner. This DCSC solution needs an additional chip backside area for the stacking additional decoupling capacitors. However, in the case of stacking APs, memories, RF chips, and other various chips in a 3D IC structure, residual areas are unavoidable. Using the residual areas for stacking decoupling capacitors would largely reduce the chip area burden of the DCSC. The size of additional silicon-based MOS capacitors in the DCSC that uses a CMOS process can be flexibly controlled to satisfy its capacitances. Additionally, as thin discrete capacitors, which represent a small size (below 1 mm), large capacitance, and low ESL (several tens of pH), have been developed, the chip area burden of the DCSC using decoupling capacitors can be minimized.

In one aspect of 3D IC design, the DCSC solution requires almost no extra chip areas for on-chip metal routability and TSV positioning, implying that this is a proper decoupling scheme for TSV-based 3D ICs. In contrast, decoupling capacitors such as MOS capacitors, MIM, and DT capacitors require a chip area of approximately a few mm^2 to ensure capacitances of more than several tens of nF. Moreover, because TSVs cannot be placed on chip areas occupied by MOS capacitors, MIM capacitors, and DT capacitors, additional chip area is required.

This study suggests using a new TSV-based DCSC mounted on the backside of a chip to overcome the well-known limitations of the traditional decoupling capacitor solutions for SSN noise mitigation in PDNs. The DCSC structure obtains a large capacitance by stacking an additional decoupling capacitor, such as a silicon-based MOS capacitor chip, and a discrete decoupling capacitor exhibiting a low ESL of 90 pH. Furthermore, due to its use of TSV technology, the suggested DCSC provides a significantly reduced PDN loop inductance relative to the package-level decoupling capacitor solution. The TSV-based DCSC is a promising technology that can be used to reduce the power and ground noise in 3D ICs by placing a MOS capacitor chip between the mobile application processor (AP) and the memory chip, as shown in Fig. 7.16.

Figure 7.17 shows the well-known traditional decoupling capacitor technologies in 3D IC development. The basic decoupling capacitor technologies utilized in -D stacked chip packages can be differentiated into two categories: on-chip decoupling capacitors and off-chip MOS decoupling capacitors. Off-chip decoupling capacitors have the disadvantage of having higher PDN loop inductances (up to several nH) compared to on-chip MOS decoupling capacitors, while on-chip MOS decoupling capacitors have a limited capacitance ($\leq$0.1 μF) that results from the reduced areas of the chips.

The inductance and capacitance of each decoupling capacitor solution are compared schematically in Fig. 7.18. As shown in Fig. 7.18, this approach satisfies the target impedance requirements for a wide range of frequencies because the DCSC has a lower inductance and higher capacitance compared to the other decoupling capacitor solutions. The TSV-based DCSC is superior to on-chip MOS capacitors in terms of both effective inductive PDN impedance and its use of high-capacitance on-package decoupling capacitors in the capacitive PDN impedance region.

As described in Fig. 7.19, the DCSC uses on-chip metal power and ground conductors with multi-layers, TSVs, and discrete decoupling capacitors stacked on the backside of the chip. The DCSC structure can directly supply power to stacked decoupling capacitors during the operation of the chip by connecting the chip-PDN and decoupling capacitors with the TSVs. By ensuring low PDN impedance via the TSV and decoupling capacitors stacked on the backside of the chip, a stable SSN noise margin can be ensured.

In general, this feature restricts the number of P/G TSVs that can be used in the 3D PDN to avoid exceeding the area budget of the chip and to prevent routing congestion. This complex optimization typically results in a large area requirement, more power consumption and lower performance, thereby diminishing the benefit of TSV-based 3D ICs technology. Thus, one suggestion is to use various

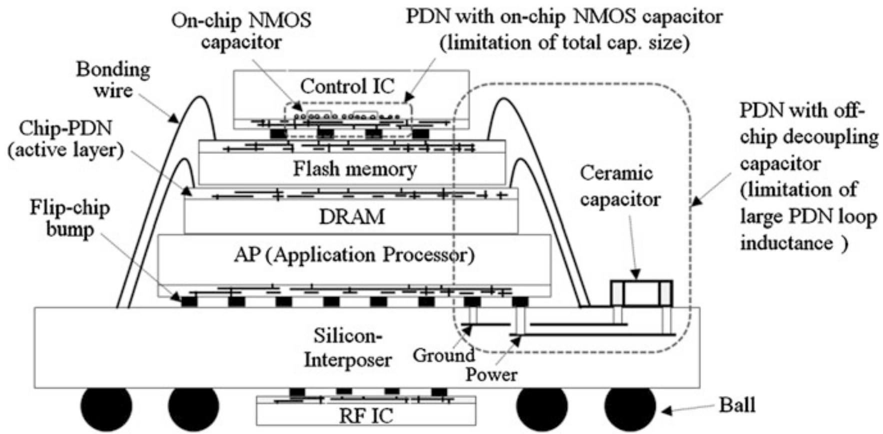

Fig. 7.17 Decoupling capacitor technologies in 3D ICs: the chip-PDN with the off-chip decoupling capacitor exhibits a large impedance due to its large inductance compared to on-chip decoupling capacitor methods. The chip-PDN with the on-chip decoupling capacitor is limited by its capacitance, which results from an insufficient chip area

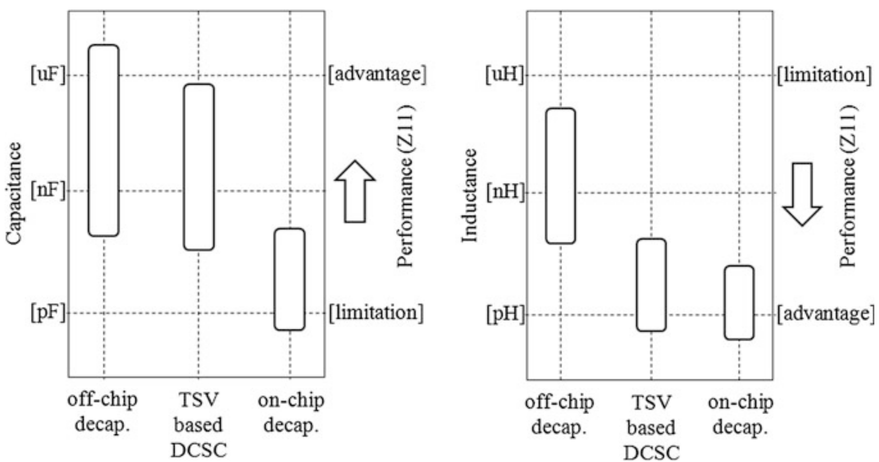

Fig. 7.18 Schematic performance comparison of the chip-level decoupling capacitor, off-chip decoupling capacitor, and TSV-based DCSC

types of chips stacked in a face-down configuration to ensure the routability of signal I/Os through the 3D stacked structure [26]. Consequently, the TSV-based DCSC in this study presumes a face-down structure that stacks decoupling capacitors on the backside of the chip, thereby presenting numerous potential applications for 3D IC systems. To overcome the limitations of the conventional decoupling capacitor solutions that exhibit a large inductance and low capacitance

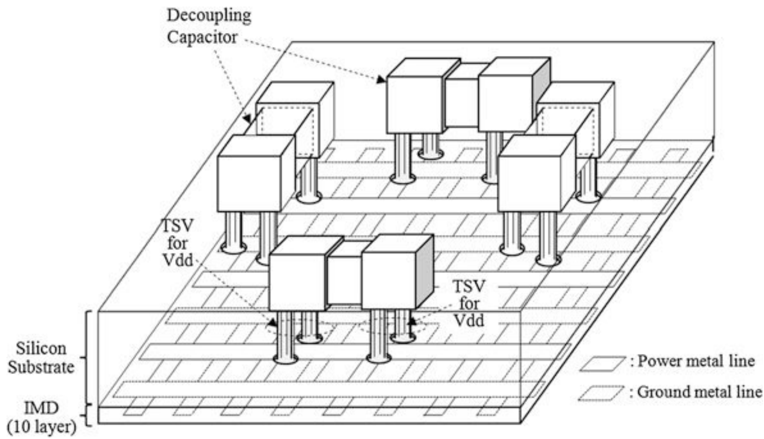

Fig. 7.19 Configuration of the face-down TSV-based DCSC; perspective view [25] © 2013 IEEE

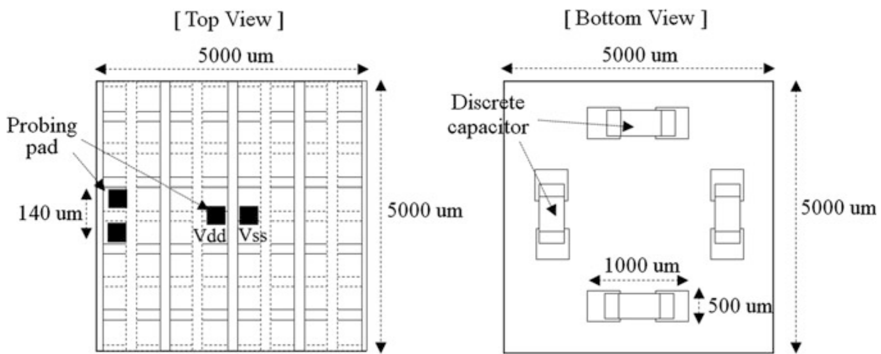

Fig. 7.20 *Top* and *bottom views* of the face-down TSV-based DCSC. Discrete decoupling capacitors with low ESLs are stacked on a chip that has 10 power and ground metal layers with a 5.0 × 5.0 mm area and a 50 μm chip thickness

power distribution network (PDN), a new TSV-based DCSC is introduced for use in 3D integration systems. This DCSC approach can enhance the PDN properties by using TSV technology (Fig. 7.20).

7.3.3 *Modeling of the Chip-PDN, TSV and Decoupling Capacitors in the TSV-Based DCSC*

In this section, the modeling of the TSV-based DCSC structure is discussed. Figure 7.21 and Table 7.1 represent the face-down TSV-based DCSC structure

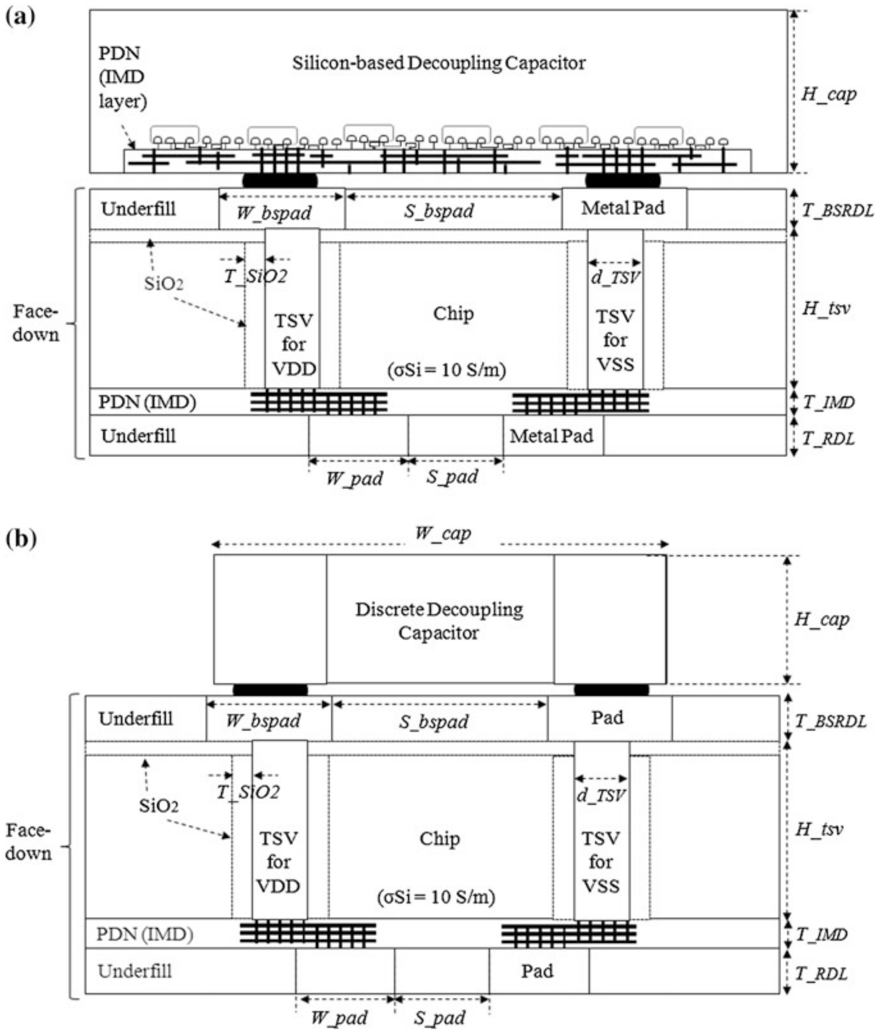

Fig. 7.21 Detailed structures, dimension variables, and materials of the face-down TSV-based DCSC: **a** silicon-based MOS capacitor **b** discrete decoupling capacitor

and its detailed parameters, respectively. The on-chip PDN metal consisted of 10 layers (mesh type) and is located entirely in the inter-metal dielectric (IMD) layer of a 5.0 × 5.0 mm chip.

The TSV used a via-middle process in which the diameter and height of the TSV were 6 and 50 μm, respectively. A metal pad was formed to stack the decoupling capacitors (chip-level MOS capacitors and package-level discrete decoupling capacitors) on the backside of the DCSC chip, facilitated by an RDL (redistribution layer) process. The experiment utilized a structure that included

Table 7.1 Design parameters for the DCSC structure utilizing TSVs

T_RDL	5 μm	*W_pad*	80 μm	*H_tsv*	50 μm
T_IMD	4 μm	*S_pad*	60 μm	*H_cap*	250 μm
T_SiO_2	0.5 μm	*D_tsv*	6 μm	*W_cap*	1,000 μm
S_bspad	850 μm	*T_BSRDL*	10 μm	*W_bspad*	80 μm

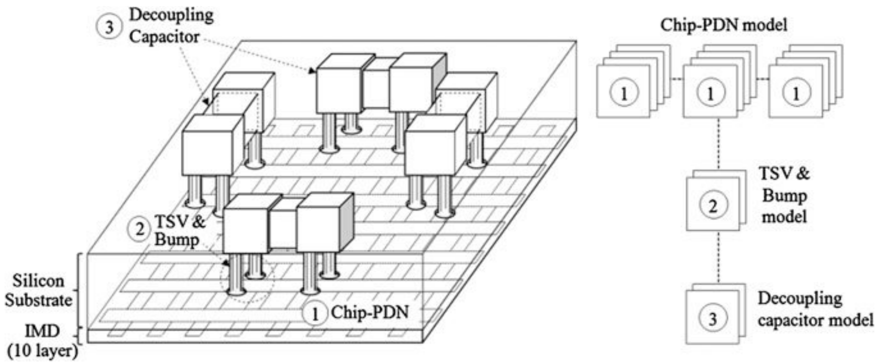

Fig. 7.22 Modeling network of the chip-PDN, TSVs, and decoupling capacitors for the face-down TSV-based DCSC

stacked discrete decoupling capacitors, and the performance of the structure stacked with chip-level MOS capacitors was evaluated via a simulation. Although MOS capacitor chips can be used with 3D ICs in the real world, the actual structure was fabricated by stacking four low-ESL discrete decoupling capacitors, each of which had a capacitance of 0.47 μF, due to limitations associated with increasing the capacitance to hundreds of nF.

Figure 7.22 depicts the TSV-based DCSC modeling network consisting of three parts: an on-chip PDN, TSVs, and decoupling capacitors. Each structure was analyzed and modeled, and the results were integrated into the overall structure using a segmentation method [27]. To analyze the 5.0 × 5.0 mm on-chip PDN of up to 20 GHz, it was divided into unit cells that were then modeled using a 3D field solver. These cells were subsequently incorporated into the overall PDN network. The size of the unit cell structures can be determined by the maximum frequency of interest, and their physical dimensions should be smaller than 5 % of the wavelength used to cover the distributed effects using lumped elements. To ensure the modeling accuracy of the mesh-type chip-PDN, only unit cells smaller than 5 % of the wavelength were used. The unit cells of the PDN consisted of edge, center, and corner cells and represent an impedance matrix as indicated in Fig. 7.23b.

Usually, an on-chip PDN is designed to have a meshed type topology, which can provide easy connections from active circuits to PDNs in the limited metal layers available on-chip. Due to the effects of P/G TSV pairs, on-chip decaps, and

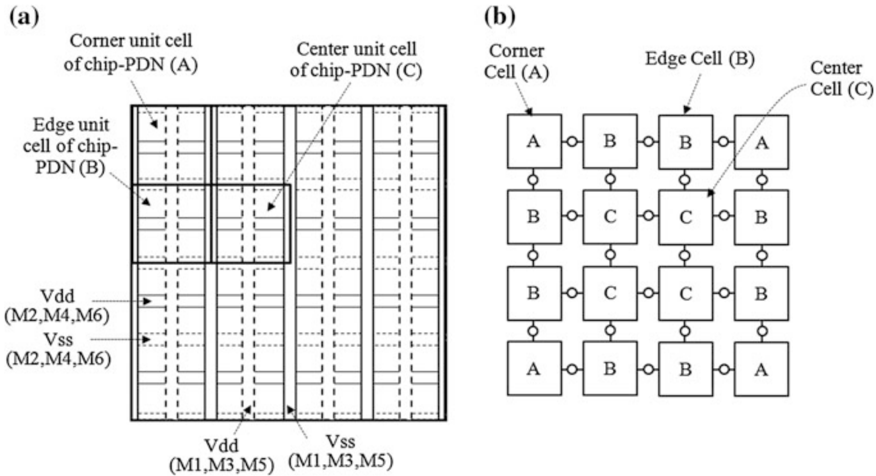

Fig. 7.23 **a** *Top view* of a mesh-type chip-PDN, and **b** the impedance matrix of the chip-PDN structure using unit-cell models. To simulate the impedance properties of the chip level PDN, the total structure was separated into the various independent unit cells. After calculating the impedance matrices of unit cells, the impedance matrix of the total DCSC structure was estimated

the silicon substrate, it is necessary to estimate the impedance of the 3D stacked on-chip PDN that included these effects. In general, to estimate the impedance of PDNs, EM simulators are used.

However, it is difficult for EM simulations using 3D field solvers to estimate the impedance of 3D stacked on-chip PDNs due to the high aspect ratio and embedded MOS capacitors. In this case, the impedance of the PDNs can be efficiently analyzed with PDN models. Therefore, for the impedance estimation, a model for 3D stacked on-chip PDNs is required that includes the effects of the P/G TSVs, on-chip decaps, and silicon substrate.

The unit cells of the mesh-type PDN are described in Fig. 7.24. Regarding the low loop inductance of the chip-PDN, metal power and ground lines were arranged in a coplanar-type transmission line, and each metal layer was a mesh-type with crossing metal lines. In Fig. 7.24, the metal width/space (w: 0.13 μm, s: 0.9 μm) of metal 1 (M1) were designed using a small scale (by a factor of five) compared to those for M2–M10, which were designed using nano-scale CMOS technology. The model for each PDN unit cell was analyzed using a Z-parameter model. The metal width/space of the chip-PDN were less than 1 μm, and each PDN layer was vertically connected using vias. Because the loop inductance of the entire PDN of the TSV-based DCSC was on the order of several nH, the PDN exhibited a relatively high inductive impedance (several ohms) in the 1 GHz band.

Figure 7.25 shows the parameters and electrical circuit model for the power and ground TSV pairs in the DCSC structure [28]. The TSV is generally formed using copper (Cu) or tungsten (W) and has a SiO_2 membrane to provide insulation around the Si substrate and TSV. The capacitance generated between the power

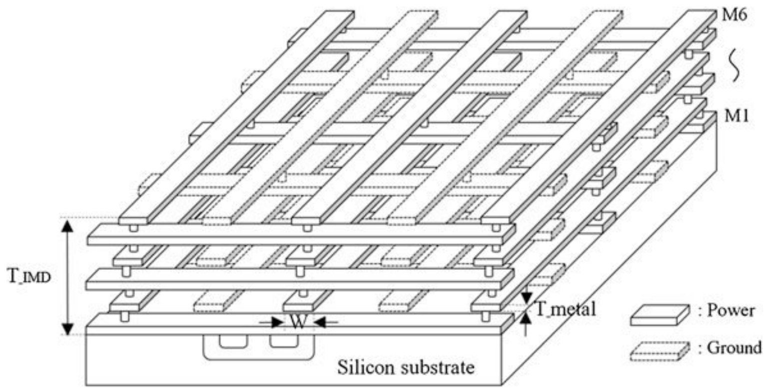

Fig. 7.24 Constitutive center-unit-cell model of the mesh-type chip-PDN. The suggested mesh-type chip-PDN is composed of 10 layers, and the on-chip P/G metal is designed in a co-planar configuration to reduce the PDN loop inductance

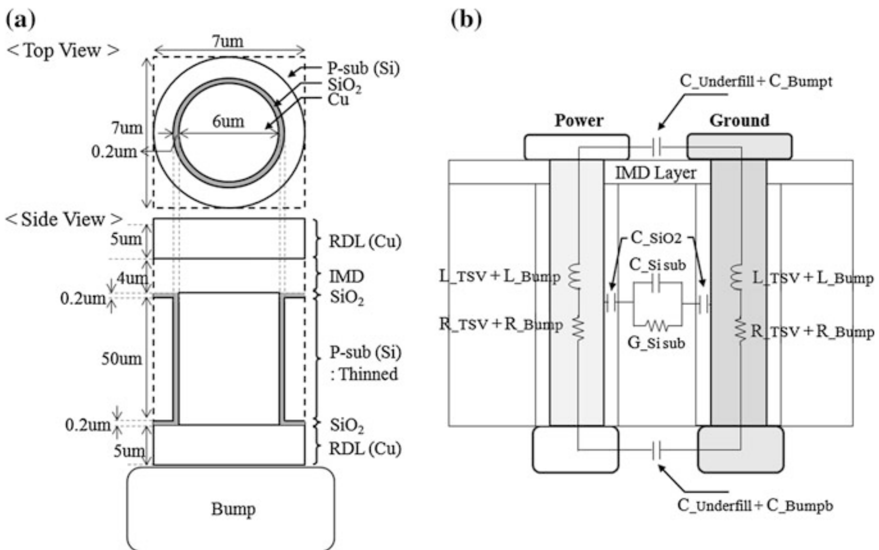

Fig. 7.25 **a** Structures of power and ground TSVs with bumps fabricated by the via-middle process and their structural parameters, and **b** the scalable electrical model with labeled RLGC components

and ground TSVs can be divided into two types: the capacitance (C_Si substrate) attributable to the Si substrate and the capacitance (C_SiO_2) associated with the SiO_2 layers. The capacitance (C_underfill + C_IMD or C_underfill + C_oxide) existing between the power and ground bumps is presented in Fig. 7.25. The inductance caused by the TSV and bumps is determined to be on the order of tens

Table 7.2 Model parameters for power and ground TSVs

Model parameter	Value	Model parameter	Value
*C*_SiO_2	172.4 fF	*R*_Bump (@ 1 GHz)	0.0011 Ω
*C*_Bumpt	6.74 fF	*L*_Bump (@ 1 GHz)	13 pH
*C*_Bumpb	136.6 fF	*C*_Si sub	2.15 fF
*R*_TSV (@ 1 GHz)	0.13 Ω	*G*_Si sub	0.6 mS
*L*_TSV (@ 1 GHz)	32.3 pH	*C*_Underfill	1.06 fF

of pH, indicating that the inductance resulting from the PDN loop inductance or the RLD in 3D ICs is dominant. Because several chips are stacked, the TSVs involved in vertical interconnection can provide low PDN impedances through the uniform arrangement of as many TSVs as possible. Table 7.2 shows the model parameters for the power and ground TSV pair with a TSV height of 50 μm, a TSV diameter of 6 μm, a SiO_2 thickness of 0.2 μm, and a RDL thickness of 5 μm. Each power and ground TSV pair has a capacitance of approximately 300 fF and an inductance of 50 pH. A frequency independent model is used to model the resistance and inductance of the TSV pair. Regarding the overall DCSC structure, it is seen that the inductance and capacitance values of a given TSV pair are very small.

The TSV-based DCSC is a structure that stacks silicon-based MOS decoupling capacitors or discrete decoupling capacitors on the backside of a chip. In this study, a MOS capacitor fabricated on 5.0 × 5.0 mm silicon and a structure stacked with four discrete (0.47 μF) decoupling capacitors was analyzed to confirm the merits of TSV-based DCSCs. The PDN impedance performance was also validated through measurements of the discrete decoupling capacitor-stacked structure. Figure 7.26 depicts the distributed RC model of the MOS transistor and the equivalent circuit model of the discrete decoupling capacitors with an ESL of 90 pH, a capacitance of 0.47 μF, and dimensions of 1.0 × 0.5 × 0.25 mm. The on-chip MOS decoupling capacitor can be modeled by including the series connection of a frequency-dependent C_decap (*C*n) and ESR (*R*n) in the unit-cell model of the on-chip PDN [29]. The gate length and channel width of the NMOS capacitor used for analyzing the PDN impedance were 30 and 315 nm, respectively. The NMOS capacitors were designed to have a capacitance of 0.067 pF (*C*n) and an ESR of 2.27 Ω (*R*n) per unit cell.

To maximize the performance of the discrete decoupling capacitors stacked on the DCSC, capacitors with a thickness of less than 0.3 mm, a high capacitance, and a low ESL (less than 90 pH) were selected. Capacitors exhibiting as low an ESL as possible should be used. If extra silicon-based MOS decoupling capacitors are used to increase the capacitance of the 3D IC systems, the ESL of the 3D PDN will be minimized.

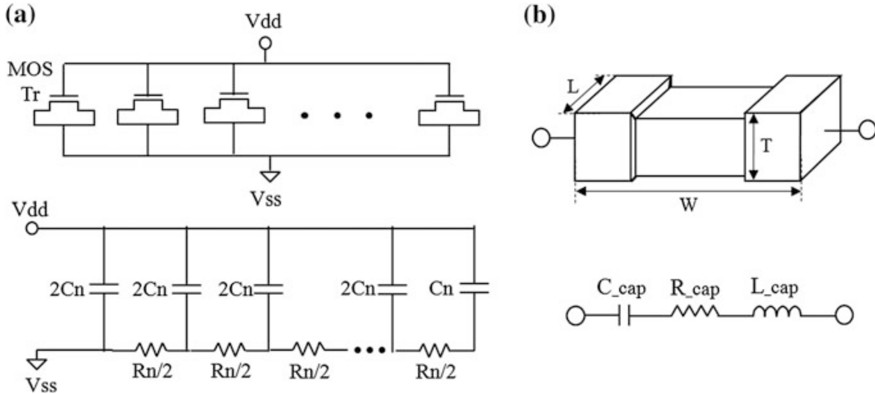

Fig. 7.26 **a** Distributed RC model of the MOS transistor channel to an open-ended line. **b** Discrete decoupling capacitors stacked on the backside of the chip and equivalent circuit model of a capacitor with a low ESL of 90 [pH], an equivalent series resistance (ESR) of 0.02 Ω and a capacitance of 0.47 μF

7.3.4 Simulation, Measurement, and PDN Analysis for Decoupling Schemes

In this section, we carefully demonstrate the advantages of a TSV-based DCSC interconnection scheme relative to decreasing the inductive and capacitive impedance of a PDN and suppressing the SSN in a 3D stacked chip. Figure 7.27 shows the micrograph and SEM image of the fabricated DCSC [30]. The chip size is 5 × 5 mm. The dimensions of the discrete decoupling capacitors with low ESLs stacked on a chip that has ten power/ground metal layers are 0.5 mm (L) × 1.0 mm (W) × 0.25 mm (T).

To demonstrate the ability of the TSV-based DCSC to enhance the PDN impedance in 3D ICs, an experimental system was constructed as shown in Fig. 7.28. The test chip was configured as an on-chip device with 10 layers and dimensions of 5.0 × 5.0 mm. Probe pads (S-G type) were located at the center and edges of the top side (the active layer). The PDN impedance of the DCSC was measured using a VNA system (Agilent, E5071B). The frequency range of the VNA equipment (E5071B) was from 1 MHZ to 8 GHz. Four discrete decoupling capacitors with an ESL of 90 pH and a combined capacitance of 0.47 μF were stacked on the backside of the fabricated test chip. The probing pad pitch along the edge is 200 μm. To minimize the current path between the probing pad on the front side of the DCSC and the decoupling capacitor on the backside of the DCSC, the position of the probing pad at the edge point is designed to be vertically aligned with the decoupling capacitor layered on the backside of the chips. The width/space of the M1 and M2–M10 metal layers are designed as 0.13–0.9 μm and 1.0–5.0 μm, respectively.

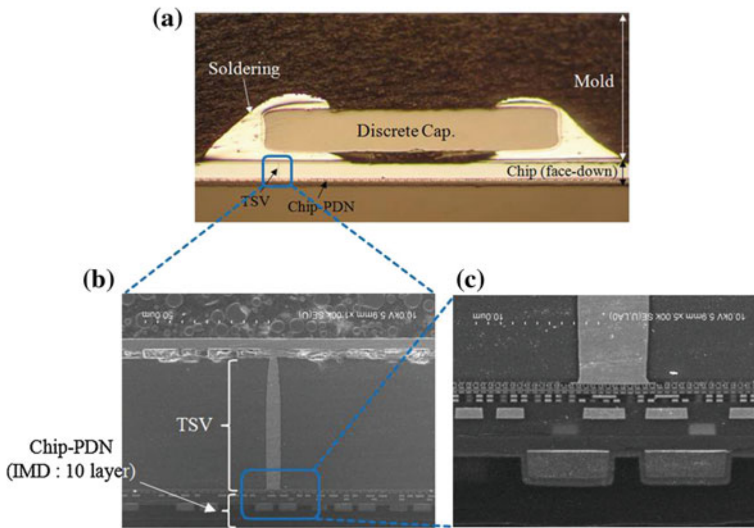

Fig. 7.27 SEM image of the face-down TSV-based DCSC with a discrete decoupling capacitor connected to the TSV in the IMD layer. The TSV was fabricated by a via-middle process, filled with copper (Cu) and surrounded by SiO_2. The IMD and insulation layers were formed with silicon dioxide (SiO_2): **a** DCSC micrograph **b** and **c** SEM images [25]

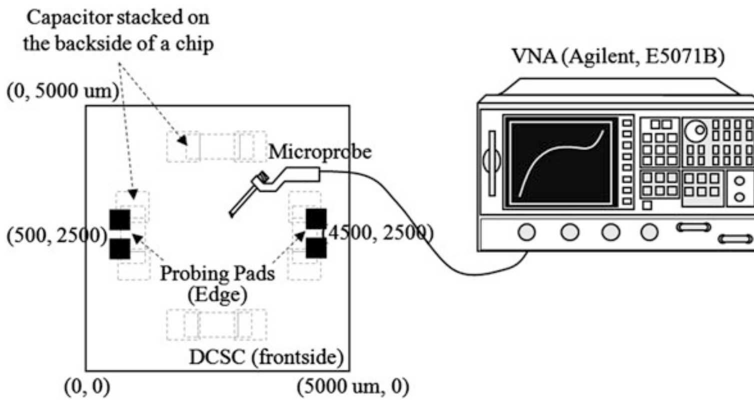

Fig. 7.28 Experimental setup for the TSV-based DCSC

As shown in Fig. 7.27b, the test vehicle is a structure that connects the chip-PDN and the decoupling capacitor using a TSV with a diameter of 6 μm. Although the test vehicle is designed and fabricated using a discrete capacitor layered structure, a silicon-based MOS capacitor layered structure using an interposer can also be used to demonstrate the DCSC concept. In addition, relative to the case of a DCSC using silicon-based MOS capacitors, it is possible to layer it to the backside of the chips even if the chip size is small.

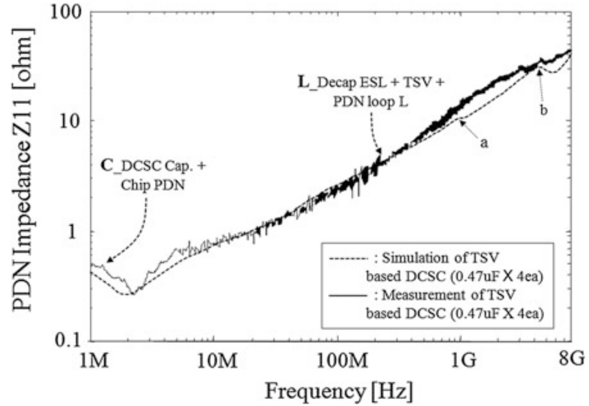

Fig. 7.29 Comparison between the measured (*solid line*) and simulated (*dotted line*) self-impedances (Z_{11}) for the 3D PDN of the TSV-based DCSC

Figure 7.29 compares the simulated and measured PDN impedances for the fabricated TSV-based DCSC. The PDN impedance simulation results obtained using a segmentation method correspond well with the VNA measurements. Figure 7.29 specifically analyzes the PDN impedance curve. The large capacitance of the discrete decoupling capacitors results in an impedance whose series resonance exists in a frequency band of approximately 2 MHz. The ESL associated with the PDN loop inductance, TSV inductance, and decoupling capacitors is dominant in the frequency band from 2 MHz to 1 GHz. The parallel resonance generated at 1 GHz ("a") is due to the interaction between the capacitances caused by the inductance of the TSV and the on-chip PDN. The resonant peak at "b" is due to the mode resonances in the chip PDN, and the mode numbers are (1, 0) and (0, 1). Because the inductance and capacitance values in the on-chip PDN, TSV, and decoupling capacitors of the DCSC are accurately modeled, the peaks of the series resonance, parallel resonance, and mode resonance between the simulated and measured impedances are clearly matched. The series resonance frequency peak at 2 MHz represents an excellent correlation between the measured and simulated values. However, the resonance peaks at the points "a" (parallel resonance) and "b" (mode resonance) are not clear because the resistance of the on-chip PDN is not large. As shown in Fig. 7.29, the Z_{11} resonance peaks at "a" and "b" are clearly matched between the measured and simulated results, and the tendency of the overall Z_{11} empirical and analytical inductive curves is well matched.

To verify the enhanced performance of the TSV-based DCSC, conventional decoupling capacitor solutions (such as wirebond SiP with decoupling capacitors and on-chip MOS decoupling capacitors) were compared. In Fig. 7.30, a wirebond SiP that has four 0.47 μF off-chip capacitors is presented. For the wirebond SiP, the impedance of the wirebond in the PDN path from the on-chip metal to the decoupling capacitor is large. This produces an increase in the inductive impedance curve at frequency bands occurring in the range of several tens of MHz. In the simulation, the PDN inductance of the wirebond SiP was determined to be 3.0 nH, and the ESL for each discrete decoupling capacitor was taken as 90 pH.

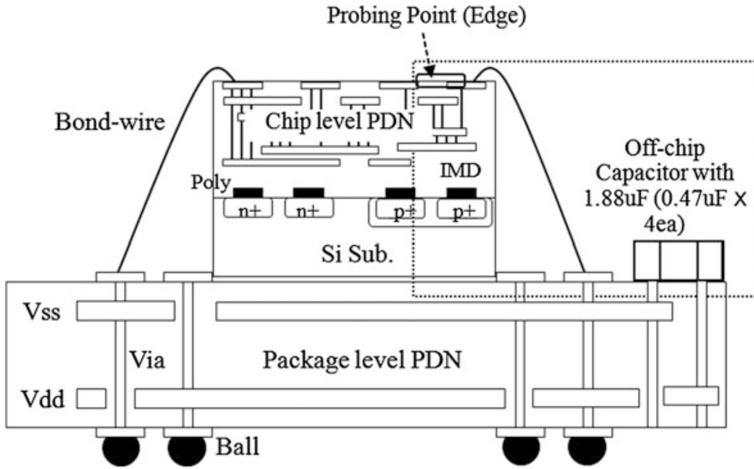

Fig. 7.30 Wirebond SiP utilizing the off-chip decoupling capacitor solution

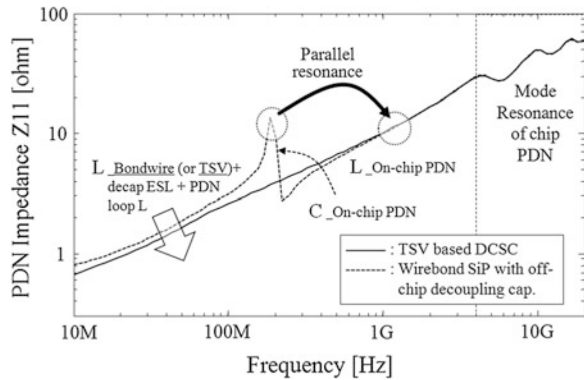

Fig. 7.31 Comparison of the simulated PDN self-impedance (Z_{11}) between the wirebond SiP (*dotted line*) with off-chip decoupling capacitors (0.47 μF × 4 ea) and the TSV-based DCSC (*solid line*). The PDN inductance of the wirebond SiP was assumed to be 3.0 nH

As indicated in Fig. 7.31 for the case of the wirebond SiP, the inductive impedance curve is relatively high. This produces a parallel resonance that occurs at a frequency of 180 MHz due to the interaction between the wirebond inductance and the on-chip PDN.

In addition, the inductance of the wirebond SiP is further increased, and the parallel resonance peak generated by the interaction between the inductance of the wirebond and the capacitance of the chip-PDN increases as well. Due to the increase in the anti-resonance impedance, the power noise margin (e.g., SSN) decreases, causing operational failures to occur in a 3D IC system. Eventually, if off-chip decoupling capacitors are used in a high-speed 3D integration system, an anti-parallel resonance peak will occur due to an exceedingly large ESL in the range of a few nH, notwithstanding a potentially large increase in the capacitance.

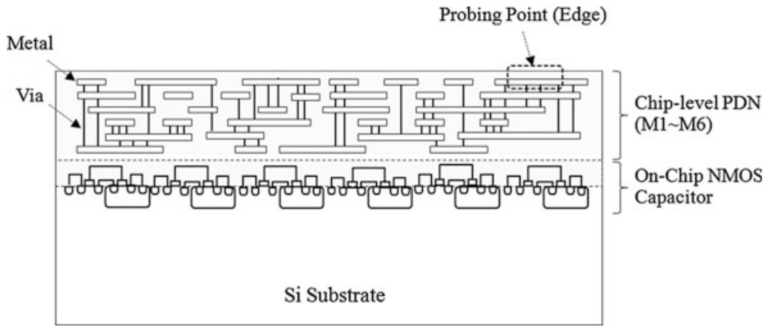

Fig. 7.32 The conventional on-chip NMOS decoupling capacitor solution fully embedded within a 5.0 × 5.0 mm chip area. The total capacitance of the NMOS capacitors was approximately 0.2 μF

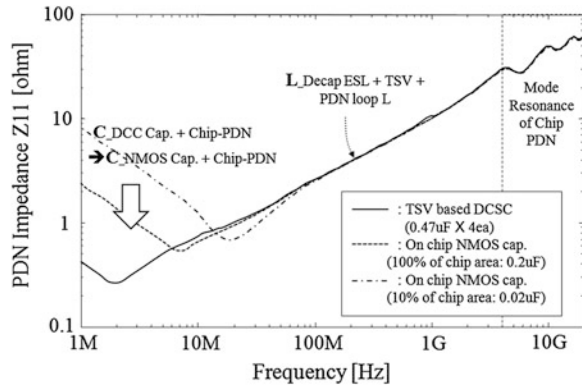

Fig. 7.33 Comparison of the simulated PDN self-impedances (Z_{11}) between the on-chip decoupling capacitors shown in Fig. 7.32 and the TSV-based DCSC

To demonstrate the performance of the DCSC structure, the TSV-based DCSC was also compared to the conventional on-chip NMOS decoupling capacitor solution. For the chip-level NMOS capacitor, the PDN simulation was performed using two different configurations: one with the NMOS capacitors embedded in only 10 % of the entire chip area, and the other with the NMOS capacitors arranged over the entire chip (100 %) using a chip size of 5.0 × 5.0 mm. In Fig. 7.32, the on-chip metal PDN was integrated into 10 layers with the same design used in the DCSC structure. In addition, this structure contained an arrangement of on-chip NMOS capacitors.

As described in Fig. 7.33, when the NMOS capacitors utilized only 10 % of the chip area (10 % area is occupied by NMOS decaps), the resulting series resonance (C_NMOS cap + C_chip PDN) // (L_PDN loop L + L_TSV + L_decap ESL) was shifted to a high frequency range due to the decrease in the NMOS capacitance. When the on-chip NMOS capacitor was used, a parallel resonance at a frequency band of 1 GHz was not observed because of the small ESL of the NMOS capacitor,

Table 7.3 Summary of the advantages and disadvantages of the wirebond-types with on-package decoupling capacitors, on-chip decoupling capacitors embedded in the chip, and the DCSC using TSV technology

	On-chip MOS decoupling capacitor	TSV-based DCSC	On-package decoupling capacitor
Capacitance	Limited (below 0.1 μF)	Good (up to several tens of μF)	Good (up to several tens of μF)
ESL	Very good (several pH)	Good (20–50 pH)	Poor (several nH)
Manufacturing	Difficult	Medium	Easy
Cost	High	Medium	Low

and the interaction between the TSV inductance and PDN loop inductance was observed in the TSV-based DCSC structure. However, because the inductance of the TSV was small compared to that of the loop inductance of the PDN (in the range of several tens of pH), the parallel resonant peak was very small.

The first series resonances for the three cases were 2.1 MHz (TSV-based DCSC), 7.0 MHz (100 % of chip area), and 20 MHz (10 % of chip area). When an on-chip NMOS capacitor was used, a parallel resonance was not observed at the frequency of 1 GHz due to the small ESL of the NMOS capacitor. In contrast, the inductive impedance curve of the TSV-based DCSC was similar to that of the on-chip NMOS capacitor because the inductance level of the TSV (under 30 pH) was much smaller than that of the loop inductance of the chip-PDN (approximately 2–3 nH). If the TSV-based DCSC is properly used in a 3D IC system, a chip NMOS capacitor level of inductance and a discrete capacitor level of capacitance could be presented simultaneously. In a 3D IC system, due to the decrease in the capacitance of the on-chip NMOS capacitors, the impedance below several tens of MHz will increase. In addition, the overall chip cost increases as the area of the chip capacitor is increased to achieve higher capacitance values for the on-chip decoupling capacitors.

The PDN impedance performance of the TSV-based DCSC was comparable to that obtained when the MOS capacitors were arranged over the entire chip area. Thus, the DCSC structure can provide a low-inductive PDN and suppress power and ground noises in 3D IC systems. In addition, it is important to consider the arrangement of the TSV, and a chip-PDN design exhibiting a low inductive level to achieve a low impedance is essential.

Table 7.3 compares the capacitances, ESLs, manufacturing challenges, and costs of the TSV-based DCSC and two conventional solutions. While the TSV-based DCSC exhibits certain advantages of on-chip MOS capacitors, such as an ESL of less than 50 pH, it also exhibits some disadvantages common to on-package decoupling capacitors, such as a high inductance (i.e., several nH). Furthermore, it exhibits the strength of on-package decoupling capacitors, including a high capacitance of up to several μF. This feature is a weak point of the on-chip MOS capacitors, which have a low capacitance of less than 0.1 μF.

Although there are currently some challenges with regard to manufacturing and cost, this design represents an adaptable competitive alternative compared to other decoupling solution methods. The most important attribute of the DCSC structure is that it may be used as a 3D PDN technology for 3D IC systems.

7.3.5 Analysis of PDN Impedance with Parameter Variations in the TSV-Based DCSC

The PDN impedance was carefully investigated using the segmentation method by varying some of the parameters, such as the number of TSVs (50-μm height), chip-level PDN size, and the capacitance of the decoupling capacitors used in the TSV-based DCSC. Additionally, the PDN impedance was analyzed by varying the number of P/G TSVs connecting to the on-chip PDN and the number of capacitors stacked on the backside of the chip. As shown in Fig. 7.34, the number of P/G TSVs can be divided into 1 pair (case I), 2 pairs (case II), and 4 pairs (case III).

As described in Fig. 7.35, the parallel resonance resulting from the PDN capacitance and TSV inductance modifications due to the decrease in the number of P/G TSV pairs shifts the frequency bands from 900 to 420 MHz. However, the PDN impedance of the overall DCSC structure can be ignored because the parallel resonant peak is too small.

For the inductive impedance curve of the chip-PDN, the PDN loop inductance was calculated as 2.55 nH. However, the loop inductance of the P/G TSV pair, which connects the decoupling capacitor of the DCSC to the metal PDN, was 20–30 pH. This is approximately 100 times greater than the PDN loop inductance. Because the portion of the TSV inductance in the entire DCSC structure is small, the parallel resonance peak in the inductive impedance curve is also small. Due to the decrease in the number of P/G TSV pairs, the TSV inductance increases, causing the resonance to move to lower frequencies [900 MHz (case I) → 620 MHz (case II) → 420 MHz (case III)]. However, there were no significant effects on the PDN impedance of the overall DCSC structure related to the TSV inductance, which was below 30 pH. This value is very low compared to the loop inductance of the chip-PDN, which was 2.55 nH.

However, TSV topology is an important consideration in 3D IC designs. The performance, power consumption, thermal integrity, and routability are all significantly affected by decisions relating to placement. Thus, a 3D placement must minimize the total number of interconnects and control the number of TSVs to ensure thermal integrity.

The PDN impedance for the TSV-based DCSC has been analyzed according to the positions of the probing pads. The simulation conditions for the results presented in Fig. 7.36 are as follows: Four 0.47 μF decoupling capacitors were stacked on the backside of the DCSC, and the size of the on-chip PDN was 5.0 × 5.0 mm. The on-chip PDN and decoupling capacitors were a structure

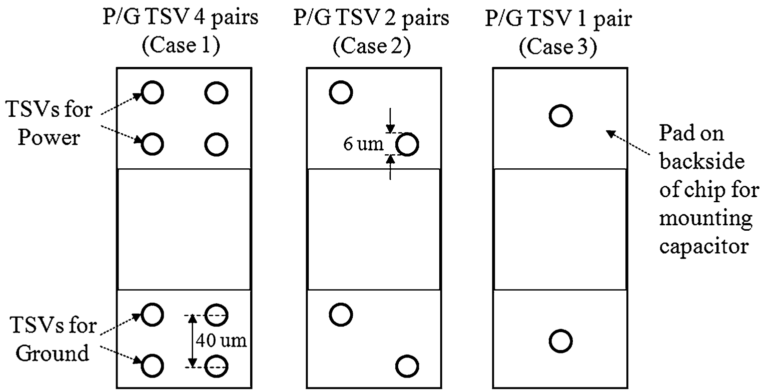

Fig. 7.34 Variation in the number of P/G TSVs in the TSV-based DCSC with four 0.47 μF discrete capacitors; Case I: four pairs of P/G TSVs in the DCSC, case II: two pairs of P/G TSVs in the DCSC, case III: one pair of P/G TSVs in the DCSC (TSV pitch: 40 μm)

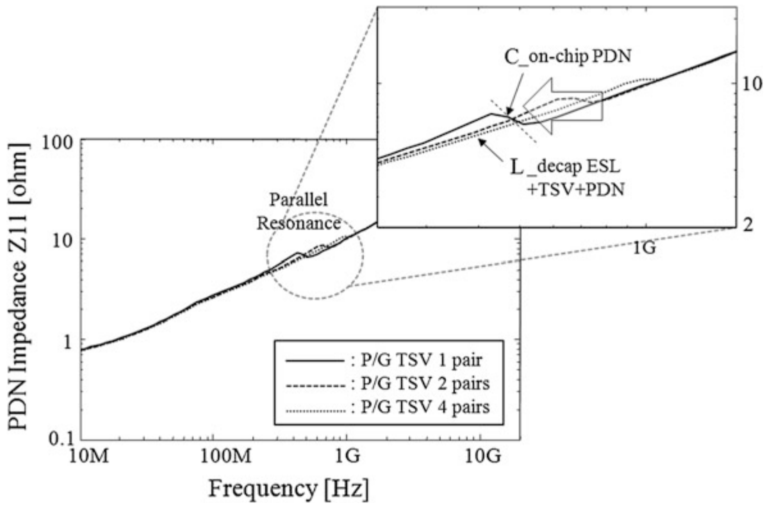

Fig. 7.35 PDN self-impedances (Z_{11}) at the edge point of a chip when the number of P/G TSVs connected to the discrete decoupling capacitors (0.47 μF) is altered. The inductance values for case I (four pairs of P/G TSVs), case II (two pairs of P/G TSVs) and case III (one pair of P/G TSVs) are 12.9 pH, 17.2 pH, and 25.7 pH, respectively

connected by TSV with a height of 50 μm. Four P/G pairs were used for each TSV. The diameter of the TSV was designed to be 6 μm using a via-middle process. In addition, because the analyzed PDN consisted of 10 layers and the PDN metal had a very small line width and space (as small as 1 μm), the loop impedance of the PDN fabricated by the 32 nm node was very large (2.5 nH).

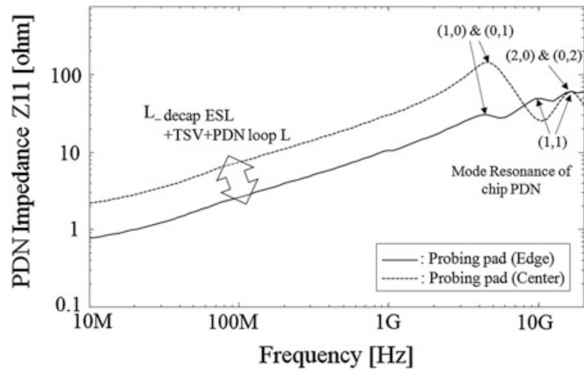

Fig. 7.36 Simulated impedance of the TSV-based DCSC obtained via the segmentation modeling method at the center (*dotted line*) and edge (*solid line*) of a chip-PDN. The impedance peaks were generated by interactions between the chip P/G metal-TSV-capacitor 3D PDN and the mode resonances of the chip-PDN

Figure 7.36 depicts the self-impedance (Z_{11}) observed in the top metal layer of the chip-PDN. As indicated in Fig. 7.36, the PDN impedance varied significantly depending on the probing pad locations. In Fig. 7.36, it is clear that the first series resonance due to the stacked decoupling capacitor had a large capacitance (1.88 μF, 4 capacitors at 0.47 μF) because it excited a resonance below 10 MHz. In addition, when calculating the loop inductance according to each position, the inductance at the center and edge points were 7.29 and 3.02 nH, respectively, indicating a 140 % increase in the loop inductance. For the DCSC analyzed, it is observed that because the decoupling capacitors were stacked at the edge of the backside of the chip, the impedance at the center was larger than that at the edge due to the increase in the PDN loop inductance.

The effectiveness of the PDN impedance (Z_{11}) based on variations in the size of the chip-PDN was also demonstrated. The PDN sizes were 5.0 × 5.0 mm (case I), 4.0 × 4.0 mm (case II), 3.0 × 3.0 mm (case III), and 2.0 × 2.0 mm (case IV). In the TSV-based DCSC structure, the simulations were performed maintaining certain conditions (e.g., the number of TSVs, capacitance of the decoupling capacitors, and location) while varying the PDN size, as shown in Fig. 7.37. As the PDN size decreased, the capacitance and inductance of the PDN also decreased.

In Fig. 7.38, the probing pads are located at the center and edge of the top metal layer. The capacitors in the DCSC are stacked along an edge of the chip's bottom surface and are connected to the on-chip PDN through TSVs. Thus, the Z_{11} impedance measured at the edge represents a vertical current path and displays the stacked capacitors on the chip backside. The Z_{11} measured at the center represents an additional PDN current path from the center to the edge and is larger than the impedance measured at the edge. Therefore, the Z_{11} impedance at the center position varied significantly with changes to the chip-PDN size. As presented in Table 7.4, the PDN loop inductance observed at the edge remained relatively stable, and the PDN loop inductance at the center varied by a few nH. To minimize the change in impedance due to the change in positions, the capacitors should be uniformly allocated on the chip backside. Furthermore, because the mode resonance depends on the size of the PDN, mode resonances of the chip-PDN vary

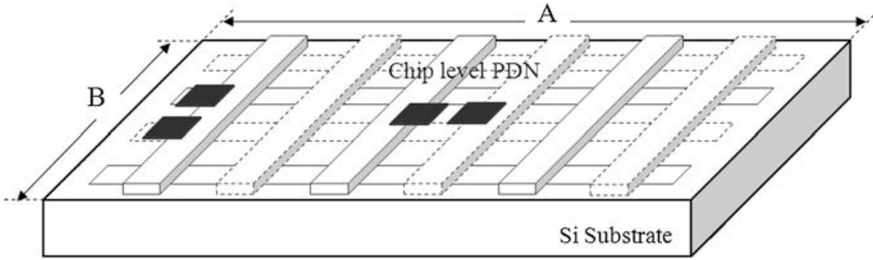

Fig. 7.37 Variation in the size (A × B) of the chip-PDN in the TSV-based DCSC: case I (5.0 × 5.0 mm), case II (4.0 × 4.0 mm), case III (3.0 × 3.0 mm) and case IV (2.0 × 2.0 mm)

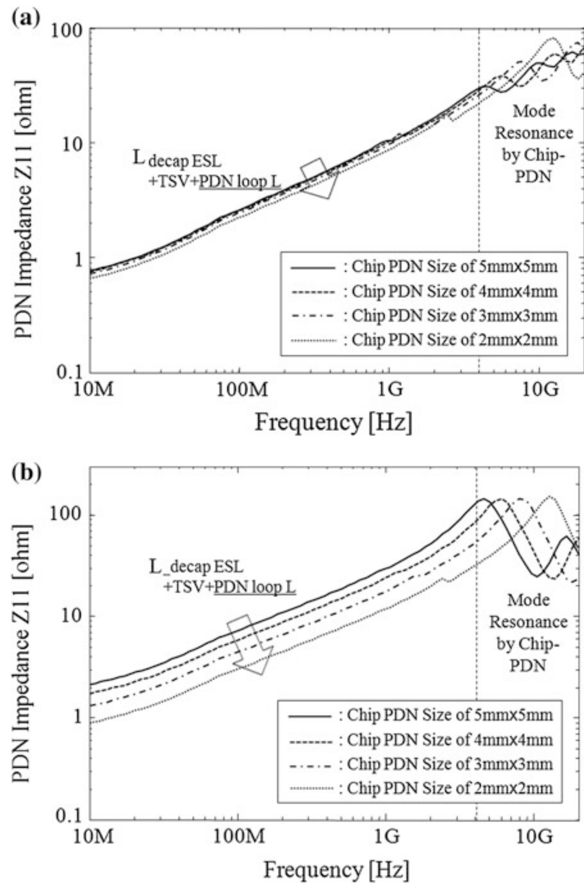

Fig. 7.38 PDN self-impedance (Z_{11}) at the edge **a** and center **b** of a chip when the size of the chip-PDN in the TSV-based DCSC is altered. As the size of the chip-PDN in the TSV-based DCSC decreased, the capacitive impedance curve decreased, and the inductive impedance curve increased through the decrease of the inductance and capacitance of the chip-PDN

with the size of the chip-PDN. In Fig. 7.38, the resonance occurring at a frequency below 10 MHz was nearly constant due to the large capacitance of the decoupling capacitors stacked on the backside of the chip (four capacitors, with a total

Table 7.4 Inductance variation in the size of chip-PDN and probing pad position

PDN size (mm)	Z_{11} (Ω) at the edge	PDN inductance (nH)	Z_{11} (Ω) at the center	PDN inductance (nH)
5.0 × 5.0	4.84	2.60	13.56	7.29
4.0 × 4.0	4.70	2.53	10.89	5.86
3.0 × 3.0	4.49	2.41	8.25	4.43
2.0 × 2.0	4.08	2.19	5.62	3.02

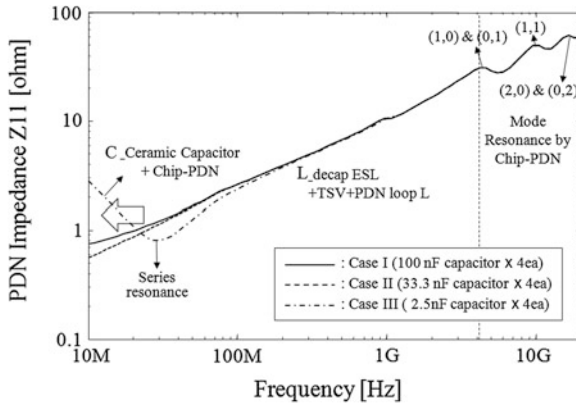

Fig. 7.39 PDN self-impedance (Z_{11}) for variations in the capacitance of the discrete decoupling capacitors stacked on the backside of the chip. The *solid line* represents the impedance of the TSV-based DCSC with a capacitance of 400 nF (four capacitors at 100 nF each), the *dotted line* shows the impedance of the TSV-based DCSC with a capacitance of 133.2 nF (four capacitors at 33.3 nF each), and the *dashed line* describes the impedance of the TSV-based DCSC with the capacitance of 10 nF (four capacitors at 2.5 nF each)

capacitance of 0.47 μF). The inductive impedance curve in the frequency band from 10 MHz to several GHz only decreased. Compared to the PDN impedance at the edge (a), the PDN impedance at the center (b) of the chip drastically changed depending on the size of the chip-PDN because the current path of the decoupling capacitor from the metal pad on the top side was comparatively much longer. To obtain a low level of PDN loop inductance, it is more effective to optimize the PDN metal width and space than to reduce the PDN size.

Next, the PDN impedance (Z_{11}) for varying capacitance values of the decoupling capacitors stacked on the backside of the TSV-based DCSC was investigated (see Fig. 7.39). The capacitance of the stacked capacitors was divided into 400 nF (4 capacitors at 100 nF each), 133.2 nF (4 capacitors at 33.3 nF each), and 10 nF (4 capacitors at 2.5 nF each) groups.

As shown in Fig. 7.39, the inductance and capacitance of the chip PDN were 2.55 nH and 1.3 nF, respectively. For case III, the series resonance in the 30 MHz frequency band was caused by the discrete capacitor (2.5 nF × 4 ea + 1.3 nF) stacked at the PDN loop inductance. In the DCSC, the first resonance was due to

Table 7.5 Series resonance variation in the capacitance of the decoupling capacitors stacked on the backside of a chip

	1st series resonance frequency (MHz)	Inductance (PDN loop L + TSV + decap ESL) (nH)	Capacitance (chip-PDN cap. + discrete cap.) (nF)
Case I (four 100 nF capacitor)	4.98	2.55	401.3
Case II (four 33.3 nF capacitors)	8.60	2.55	134.5
Case III (four 2.5 nF capacitors)	29.67	2.55	11.3

the TSV inductance and PDN loop inductance that occurred at the 1 GHz frequency. These results indicate that the TSV inductance was very small compared to that of the PDN inductance, and there was a collapse due to the large on-chip PDN resistance. In contrast to the PDN structure used in this study, the size of the on-chip PDN and the number of metal layers were small, representing a decrease in the loop impedance (Z_{11}). Thus, the ESL effects of the TSV and discrete capacitor appear large. As the inductance of the TSV increased by a few nH, the parallel resonance decreased to within the frequency band in the hundreds of MHz, and the parallel resonance peak increased to several tens of ohms. Table 7.5 shows the results of the calculations for the first series resonance for cases I, II, and III. As noted in Table 7.5, the capacitor that has associated resonances exceeding hundreds of MHz when stacked to the DCSC should be used to decrease the impedance in a low-frequency band below several tens of MHz. To ensure a low impedance at a broad frequency band, the DCSC sample used in this study was a discrete capacitor with a capacitance of 0.47 μF and an ESL of 90 pH.

As the capacitance of the DCSC capacitor increased, the first series resonant peak moved to a low-frequency range. The series resonant peak caused by (C_decoupling cap + C_chip PDN) // (L_PDN loop L + L_TSV + L_decap ESL) moved to a higher-frequency range due to the decrease in the capacitance of the capacitors stacked to the DCSC. A stable PDN impedance level can be ensured at a low-frequency range because the capacitance of the decoupling capacitors in the DCSC was determined to be as much as 100 nF.

7.3.6 PDN Analysis of the TSV-Based DCSC in Multiple Stacked 3D ICs

In a 3D IC structure where 3 chips are stacked, the performance of the TSV-based DCSC was demonstrated. Figure 7.40 shows the 3D ICs configuration that contains the DCSC structure in which each chip has a dimension of 3 × 3 mm and incorporates a 6-layered chip-PDN. The thickness for each of the 3 chips is 50 μm.

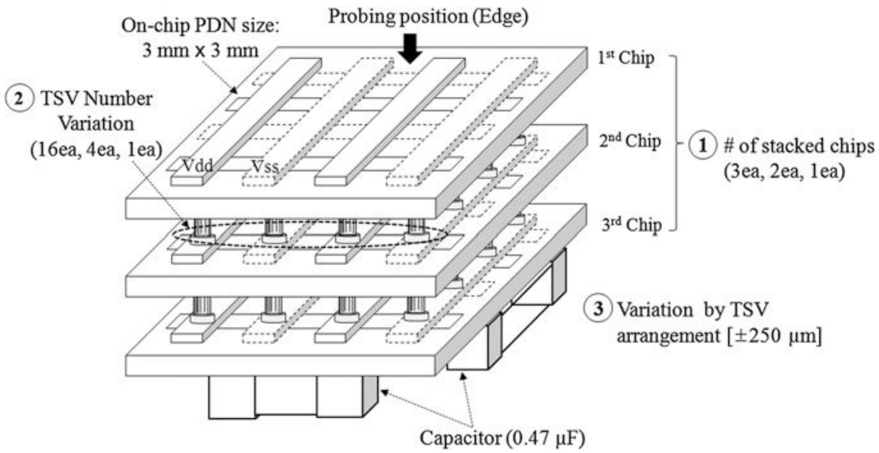

Fig. 7.40 Configuration of a multiple stacked 3D IC including three chips and the TSV-based DCSC. Each chip has six power/ground metal layers with a 3.0 × 3.0 mm area and a thickness of 50 μm

Four discrete capacitors, each having a capacitance of 0.47 μF, are stacked on the back surface of the bottom chip.

The vertical interconnection between chips is performed by using TSV technology. Figure 7.41 shows the analysis results to assess impedance variations as a function of the number of stacked chips while emphasizing that DCSC capacitors are not used for this case. As the number of stacked chips increases, the capacitance and inductance of the chip-PDN structure increase as well. The 6-layered chip-PDN was implemented using a micro process in which its metal width/space are determined as a small fine-pitch that is smaller than 1 μm. Thus, the capacitance and inductance of chip-PDN were determined as 0.5 and 2 nH, respectively. In Fig. 7.41, the first series resonance is observed at a frequency of 170 MHz when a single chip is used. To confirm the TSV effect in a 3-chip stacked 3D IC with the DCSC structure shown in Fig. 7.40, the number of TSVs used in the vertical interconnection between chips and the PDN impedance according to the position of TSV were analyzed. Figure 7.42 shows the PDN impedance variations resulting from changes to the number of vertical TSVs in each chip. Simulations results for each case were dependent on the number of TSVs (e.g., 1 TSV, 4 TSVs, and 16 TSVs) modeled, and it is noted that the impedance is analyzed at an edge point of the top chip.

In the results presented in Fig. 7.42, as the number of TSVs increases, the impedance of the entire PDN of the 3D IC decreases. For the design of the multi-stacked 3D ICs, the PDN impedance decreases associated with increases in the number of TSVs, which play a role in the vertical interconnection, are due to the increase in power current paths.

In addition, the PDN impedance variations were analyzed according to the arrangement of TSVs for a case in which the same number of TSVs is arranged in a 3-chip stacked 3D IC structure.

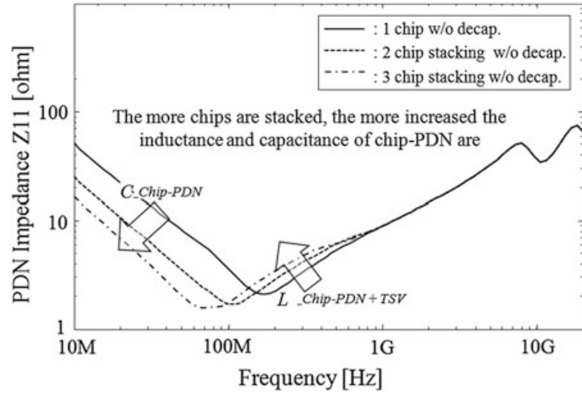

Fig. 7.41 PDN impedance variation of different numbers of stacked chips in a multiple stacked 3D IC without decoupling capacitors

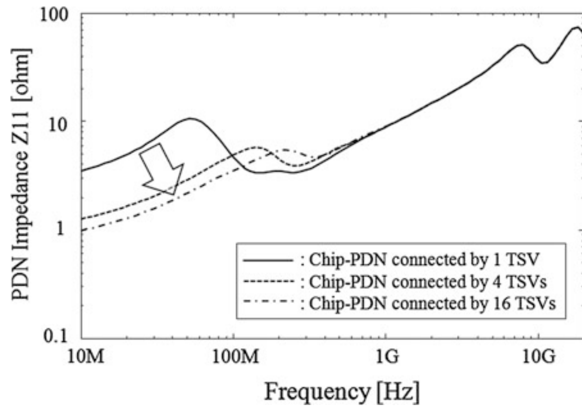

Fig. 7.42 Variation of the number of TSVs on PDN impedance. PDN (3.0 × 3.0 mm) with the capacitance of 1.88 μF (4 capacitors, 0.47 μF, stacked on the backside of the chip)

As shown in Fig. 7.43, the uniform arrangement of TSVs for the entire chip yields smaller PDN impedances than that of the randomly arranged TSVs. However, because there are no large differences in the PDN impedances of the 3D ICs when all of the TSVs are moved 250 μm, it is possible to obtain a stable 3D PDN when the power/ground TSVs are uniformly arranged among the entire chip area in a practical 3D ICs design process. The number of TSVs allocated in the available area should be maximized under this scenario. Figures 7.44 and 7.45 exhibit examples of applying the DCSC structure to a 3D ICs. DRAM chips are stacked on a package substrate in a face-down manner, and these chips are connected using TSVs. The additional capacitors stacked on the backside of the top chip play a role in supplying power to DRAM chips directly. Thus, it provides a robust 3D PDN that will facilitate stable operation of the high-speed chips in the 3D ICs.

Figure 7.46 shows a structure that allocates package decoupling capacitors in the 3D ICs. In this case, power can be supplied by decoupling capacitors, which play a role in supplying local power as DRAM and AP chips are operated. However, if the current path from the chip to the decoupling capacitors is

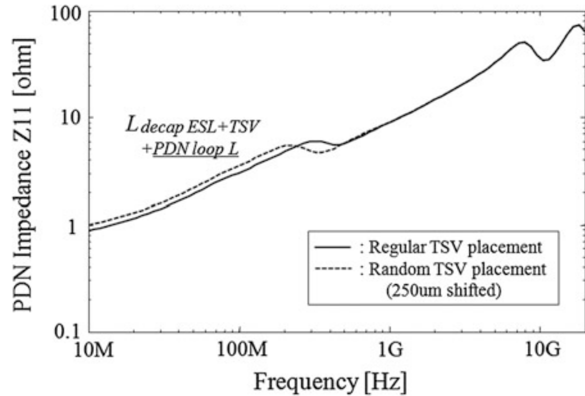

Fig. 7.43 PDN impedance variation for TSV arrangement. The difference in PDN impedance is caused by the increase of PDN loop inductance for arranging TSVs

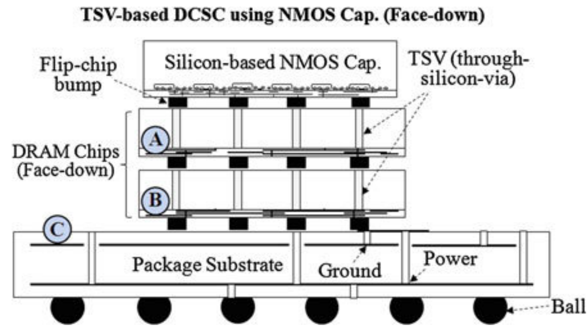

Fig. 7.44 DCSC with silicon-based NMOS capacitors in a DRAM chip stacked 3D ICs

increased, it will cause an increase in the PDN's loop inductance. As a result, it becomes a weak link with respect to power noise issues such as SSN in a 3D IC system. To assess the performance of decoupling capacitor schemes for various 3D IC systems, the impedances of the PDN topologies illustrated in Figs. 7.44, 7.45, and 7.46 were simulated. They consist of 3D structures containing two DRAM chips with a 3.0 × 3.0 mm area stacked on a 20 × 20 mm package PCB, and the DRAM chips are connected through TSVs. The TSV-based DCSC can be classified into two types: the discrete capacitor and silicon-based MOS capacitor type. The conventional decoupling solution includes on-chip MOS capacitors and on-package decoupling capacitors. The PDN impedances of the decoupling capacitor schemes in 3D ICs were compared using the segmentation method. To analyze the PDN impedance of the DCSC, simulations were performed on the 3D IC schemes presented in Figs. 7.44, 7.45, and 7.46 [30]. In the 3D ICs system, variations in the PDN impedance were analyzed using discrete capacitor and silicon-based MOS capacitor stacked DCSCs, on-chip MOS capacitors, and on-package decoupling capacitors. Figures 7.47, 7.48, and 7.49 shows impedance variations pertaining to the position of a PDN in the 3D ICs with four different decoupling solutions. The capacitance values utilized in these four types of decoupling capacitor schemes

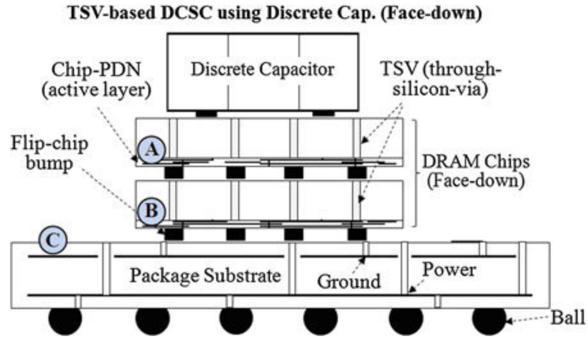

Fig. 7.45 DCSC with discrete capacitors in a DRAM chip stacked 3D ICs

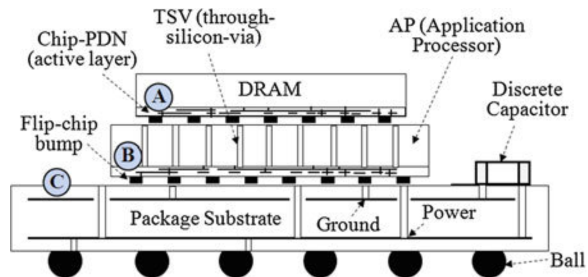

Fig. 7.46 Three-dimensional IC package with on-package capacitors

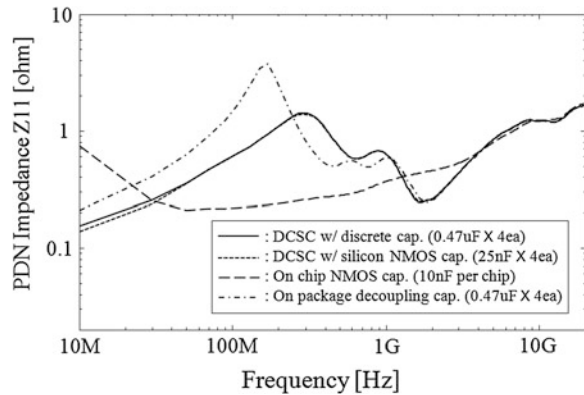

Fig. 7.47 PDN impedances at the edge (point A) of the top chip in decoupling capacitors for the 3D IC schemes presented in Figs. 7.44, 7.45 and, 7.46 [30] © 2012 IEEE

(DCSC with discrete cap., DCSC with silicon-based NMOS cap., on-chip NMOS cap., and on-package decap.) were 1.88 μF (0.47 μF × 4 ea), 100 nF (25 nF × 4 ea), 10 nF per chip, and 1.88 μF (0.47 μF × 4 ea), respectively.

Regarding the characteristics of the PDN impedance (self-impedance, Z_{11}) indicated in Figs. 7.47, 7.48, and 7.49, the TSV-based DCSC scheme displayed the best results, and the on-package decoupling capacitors yielded the worst performance. In addition, as illustrated in Fig. 7.50, the on-package decoupling

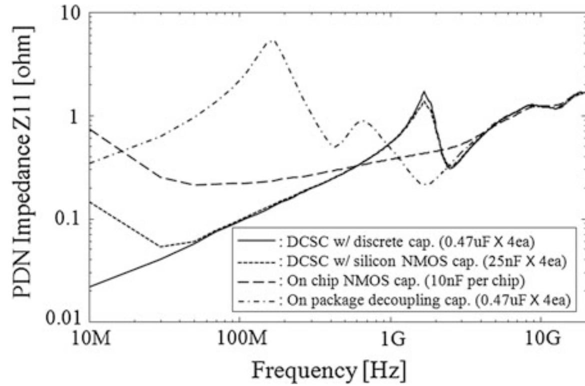

Fig. 7.48 PDN self-impedances at the edge (point B) of the bottom chip in decoupling capacitors for the 3D IC schemes shown in Figs. 7.44, 7.45, and 7.46 [30] © 2012 IEEE

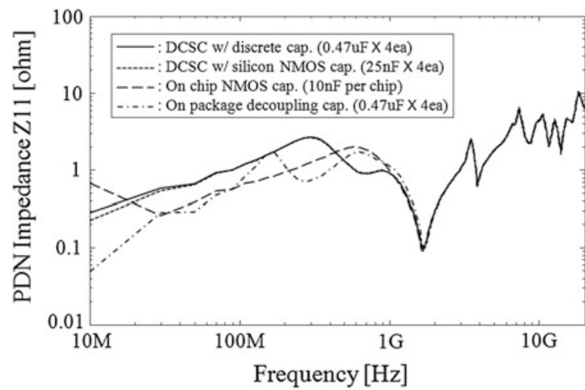

Fig. 7.49 PDN self-impedances at the edge (point C) in the package with decoupling capacitors as shown in Figs. 7.44, 7.45, and 7.46 [30] © 2012 IEEE

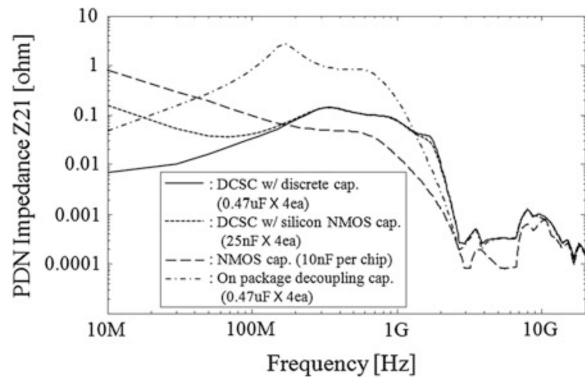

Fig. 7.50 PDN transfer-impedances (Z_{21}) from the top chip to the package (point A–point C) in decoupling capacitors for the 3D IC schemes presented in Figs. 7.44, 7.45, and 7.46 [30] © 2012 IEEE

capacitors (see Fig. 7.46) exhibited the worst PDN impedance (transfer-impedance, Z_{21}). Because the impedance of the PDN is large, a 3D ICs system has a weakness associated with coupled noise.

7.4 Summary

In 3D IC systems, the on-chip decoupling capacitor solutions implemented with silicon interposers include discrete capacitors, MIM, MOS, DT, and power/ground TSV capacitors. The decap solution based on discrete capacitors, MIM, MOS, and DT capacitors displays its advantages or disadvantages depending on capacitance density, chip area, manufacturing cost, leakage current, and resistance. For instance, MIM capacitors may lead to increases in manufacturing costs due to low capacitance densities and the additional metal layers that are required. However, it exhibits advantages associated with low power losses and small resistances because these capacitors exhibit small leakage currents. In the case of MOS capacitors, no additional manufacturing processes are required because standard CMOS processes may be utilized in this case. Another advantage is the relatively high capacitance densities available with these components. However, active circuits or TSVs cannot be allocated in chip areas that contain these MOS capacitors. Additionally, increases in power loss are incurred because MOS capacitors have large channel resistances and leakage currents. According to the development of the CMOS technology to a micro process (45 nm > 32 nm > 22 nm), DT capacitors are an attractive and promising decap solution. DT capacitors, however, utilize a process that forms a DT profile using an etching technique to yield a silicon interposer. Additionally, DT capacitors represent a higher capacitance density level and a lower leakage current density level than MOS capacitors by a factor of approximately 100 and 10 times, respectively. In addition, the DCSC architecture that laminates discrete capacitors at the backside of chips may produce relatively large capacitances and very low leakage current densities.

As a result, the TSV-based DCSC exhibits the advantages of both on-chip decoupling capacitors, which have a low ESL, and off-chip decoupling capacitors, which have a high capacitance. Finally, the TSV-based DCSC is expected to be a promising power-integrity (PI) solution for 3D IC systems in which heterogeneous chips are stacked using 3D TSV technology. However, there exist some difficulties in processes for implementing the DCSC architecture in silicon interposers. In addition, in the case of the DCSC architecture, increases in small loop inductances (<1 nH) may occur due to the soldering process for mounting DCSC decaps compared to other on-chip decaps. Thus, it is important to select a proper decoupling capacitor solution for 3D IC systems by considering 3D stacking configurations and operational frequency bands.

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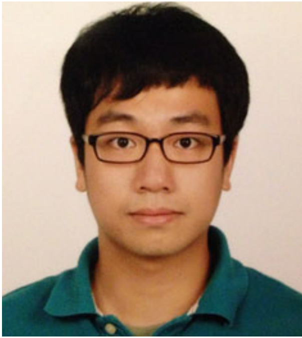

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