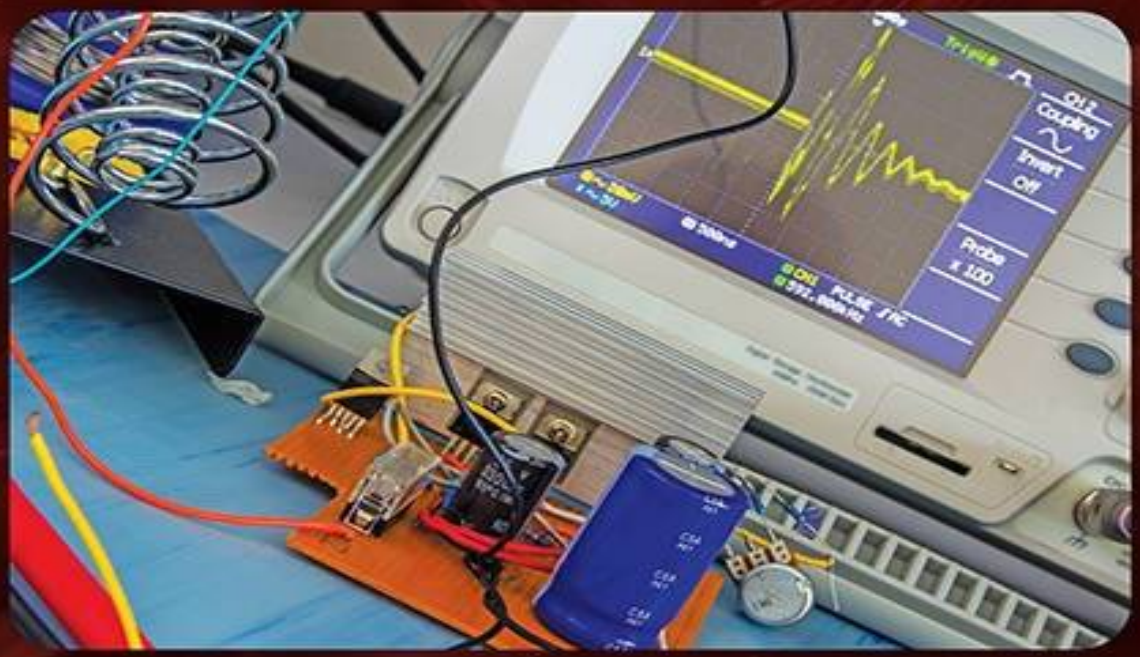
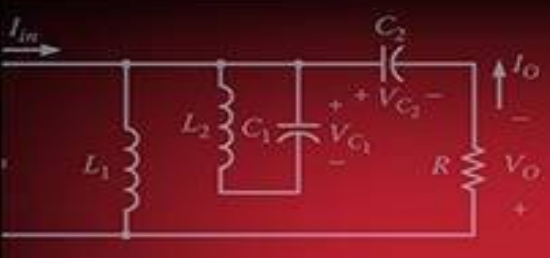
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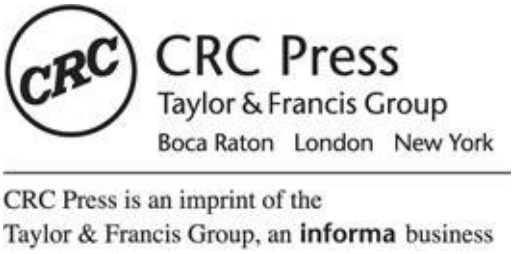
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Contents

Preface to the Second Edition
Preface to the First Edition
Acknowledgments
Authors

1. Introduction
- 1.1 Historical Review
- 1.2 Multiple-Quadrant Choppers
  - 1.2.1 Multiple-Quadrant Operation
  - 1.2.2 First-Quadrant Chopper
  - 1.2.3 Second-Quadrant Chopper
  - 1.2.4 Third-Quadrant Chopper
  - 1.2.5 Fourth-Quadrant Chopper
  - 1.2.6 First- and Second-Quadrant Chopper
  - 1.2.7 Third-Fourth-Quadrant Chopper
  - 1.2.8 Four-Quadrant Chopper
- 1.3 Pump Circuits
  - 1.3.1 Fundamental Pumps
    - 1.3.1.1 Buck Pump
    - 1.3.1.2 Boost Pump
    - 1.3.1.3 Buck-Boost Pump
  - 1.3.2 Developed Pumps
    - 1.3.2.1 Positive Luo-Pump
    - 1.3.2.2 Negative Luo-Pump
    - 1.3.2.3 Cúk Pump
  - 1.3.3 Transformer-Type Pumps
    - 1.3.3.1 Forward Pump
    - 1.3.3.2 Flyback Pump
    - 1.3.3.3 ZETA Pump
  - 1.3.4 SL Pumps
    - 1.3.4.1 Positive Super Luo-Pump
    - 1.3.4.2 Negative Super Luo-Pump
    - 1.3.4.3 Positive Push-Pull Pump
    - 1.3.4.4 Negative Push-Pull Pump
    - 1.3.4.5 DEC
- 1.4 Development of DC/DC Conversion Technique
  - 1.4.1 First-Generation Converters
    - 1.4.1.1 Fundamental Converters
    - 1.4.1.2 Transformer-Type Converters

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1.4.1.3 Developed Converters
1.4.1.4 VL Converters
1.4.1.5 SL Converters
1.4.2 Second-Generation Converters
1.4.3 Third-Generation Converters
1.4.3.1 Switched-Capacitor Converters
1.4.3.2 Multiple-Quadrant Switched-Capacitor Luo-Converters
1.4.3.3 Multiple-Lift Push-Pull Switched-Capacitor Converters
1.4.3.4 Switched-Inductor Converters
1.4.4 Fourth-Generation Converters
1.4.4.1 ZCS-QRCs
1.4.4.2 ZVS-QRCs
1.4.4.3 ZT Converters
1.4.5 Fifth-Generation Converters
1.4.6 Sixth-Generation Converters
1.5 Categorizing Prototypes and DC/DC Converter Family Tree
Bibliography

2. Voltage-Lift Converters

2.1 Introduction
2.2 Seven Self-Lift Converters
2.2.1 Self-Lift Cúk Converter
2.2.1.1 Continuous Conduction Mode
2.2.1.2 Discontinuous Conduction Mode
2.2.2 Self-Lift P/O Luo-Converter
2.2.2.1 Continuous Conduction Mode
2.2.2.2 Discontinuous Conduction Mode
2.2.3 Reverse Self-Lift P/O Luo-Converter
2.2.3.1 Continuous Conduction Mode
2.2.3.2 Discontinuous Conduction Mode
2.2.4 Self-Lift N/O Luo-Converter
2.2.4.1 Continuous Conduction Mode
2.2.4.2 Discontinuous Conduction Mode
2.2.5 Reverse Self-Lift N/O Luo-Converter
2.2.5.1 Continuous Conduction Mode
2.2.5.2 Discontinuous Conduction Mode
2.2.6 Self-Lift SEPIC
2.2.6.1 Continuous Conduction Mode
2.2.6.2 Discontinuous Conduction Mode
2.2.7 Enhanced Self-Lift P/O Luo-Converters
2.3 P/O Luo-Converters
2.3.1 Elementary Circuit
2.3.1.1 Circuit Description
2.3.1.2 Variations of Currents and Voltages

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2.3.1.3 Instantaneous Values of Currents and Voltages
2.3.1.4 Discontinuous Conduction Mode
2.3.1.5 Stability Analysis
2.3.2 Self-Lift Circuit
2.3.2.1 Circuit Description
2.3.2.2 Average Current I_{C1} and Source Current I_S
2.3.2.3 Variations of Currents and Voltages
2.3.2.4 Instantaneous Value of the Currents and Voltages
2.3.2.5 Discontinuous Conduction Mode
2.3.2.6 Stability Analysis
2.3.3 Re-Lift Circuit
2.3.3.1 Circuit Description
2.3.3.2 Other Average Currents
2.3.3.3 Variations of Currents and Voltages
2.3.3.4 Instantaneous Value of the Currents and Voltages
2.3.3.5 Discontinuous Conduction Mode
2.3.3.6 Stability Analysis
2.3.4 Multiple-Lift Circuits
2.3.4.1 Triple-Lift Circuit
2.3.4.2 Quadruple-Lift Circuit
2.3.5 Summary
2.3.6 Discussions
2.3.6.1 Discontinuous Conduction Mode
2.3.6.2 Output Voltage V_o versus Conduction Duty Cycle k
2.3.6.3 Switching Frequency f
2.4 N/O Luo-Converters
2.4.1 Elementary Circuit
2.4.1.1 Circuit Description
2.4.1.2 Average Voltages and Currents
2.4.1.3 Variations of Currents and Voltages
2.4.1.4 Instantaneous Values of Currents and Voltages
2.4.1.5 Discontinuous Mode
2.4.2 Self-Lift Circuit
2.4.2.1 Circuit Description
2.4.2.2 Average Voltages and Currents
2.4.2.3 Variations of Currents and Voltages
2.4.2.4 Instantaneous Value of the Currents and Voltages
2.4.2.5 Discontinuous Mode
2.4.3 Re-Lift Circuit
2.4.3.1 Circuit Description
2.4.3.2 Average Voltages and Currents
2.4.3.3 Variations of Currents and Voltages
2.4.3.4 Instantaneous Values of the Currents and Voltages
2.4.3.5 Discontinuous Mode

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2.4.4 Multiple-Lift Circuits
2.4.4.1 Triple-Lift Circuit
2.4.4.2 Quadruple-Lift Circuit
2.4.5 Summary
2.5 Modified P/O Luo-Converters
2.5.1 Elementary Circuit
2.5.2 Self-Lift Circuit
2.5.3 Re-Lift Circuit
2.5.4 Multiple-Lift Circuit
2.5.5 Application
2.6 Double-Output Luo-Converters
2.6.1 Elementary Circuit
2.6.1.1 Positive Conversion Path
2.6.1.2 Negative Conversion Path
2.6.1.3 Discontinuous Mode
2.6.2 Self-Lift Circuit
2.6.2.1 Positive Conversion Path
2.6.2.2 Negative Conversion Path
2.6.2.3 Discontinuous Conduction Mode
2.6.3 Re-Lift Circuit
2.6.3.1 Positive Conversion Path
2.6.3.2 Negative Conversion Path
2.6.3.3 Discontinuous Conduction Mode
2.6.4 Multiple-Lift Circuit
2.6.4.1 Triple-Lift Circuit
2.6.4.2 Quadruple-Lift Circuit
2.6.5 Summary
2.6.5.1 Positive Conversion Path
2.6.5.2 Negative Conversion Path
2.6.5.3 Common Parameters
Bibliography

3. Positive-Output Super-Lift Luo-Converters
3.1 Introduction
3.2 Main Series
3.2.1 Elementary Circuit
3.2.2 Re-Lift Circuit
3.2.3 Triple-Lift Circuit
3.2.4 Higher-Order Lift Circuit
3.3 Additional Series
3.3.1 Elementary Additional Circuit
3.3.2 Re-Lift Additional Circuit
3.3.3 Triple-Lift Additional Circuit
3.3.4 Higher-Order Lift Additional Circuit

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3.4 Enhanced Series
3.4.1 Elementary Enhanced Circuit
3.4.2 Re-Lift Enhanced Circuit
3.4.3 Triple-Lift Enhanced Circuit
3.4.4 Higher-Order Lift Enhanced Circuit
3.5 Re-Enhanced Series
3.5.1 Elementary Re-Enhanced Circuit
3.5.2 Re-Lift Re-Enhanced Circuit
3.5.3 Triple-Lift Re-Enhanced Circuit
3.5.4 Higher-Order Lift Re-Enhanced Circuit
3.6 Multiple-Enhanced Series
3.6.1 Elementary Multiple-Enhanced Circuit
3.6.2 Re-Lift Multiple-Enhanced Circuit
3.6.3 Triple-Lift Multiple-Enhanced Circuit
3.6.4 Higher-Order Lift Multiple-Enhanced Circuit
3.7 Summary of Positive-Output Super-Lift Luo-Converters
3.8 Simulation Results
3.8.1 Simulation Results of a Triple-Lift Circuit
3.8.2 Simulation Results of a Triple-Lift Additional Circuit
3.9 Experimental Results
3.9.1 Experimental Results of a Triple-Lift Circuit
3.9.2 Experimental Results of a Triple-Lift Additional Circuit
3.9.3 Efficiency Comparison of Simulation and Experimental Results
References

4. Negative-Output Super-Lift Luo-Converters

4.1 Introduction
4.2 Main Series
4.2.1 Elementary Circuit
4.2.2 N/O Re-Lift Circuit
4.2.3 N/O Triple-Lift Circuit
4.2.4 N/O Higher-Order Lift Circuit
4.3 Additional Series
4.3.1 N/O Elementary Additional Circuit
4.3.2 N/O Re-Lift Additional Circuit
4.3.3 N/O Triple-Lift Additional Circuit
4.3.4 N/O Higher-Order Lift Additional Circuit
4.4 Enhanced Series
4.4.1 N/O Elementary Enhanced Circuit
4.4.2 N/O Re-Lift Enhanced Circuit
4.4.3 N/O Triple-Lift Enhanced Circuit
4.4.4 N/O Higher-Order Lift Enhanced Circuit
4.5 Re-Enhanced Series
4.5.1 N/O Elementary Re-Enhanced Circuit

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4.5.2 N/O Re-Lift Re-Enhanced Circuit
4.5.3 N/O Triple-Lift Re-Enhanced Circuit
4.5.4 N/O Higher-Order Lift Re-Enhanced Circuit
4.6 Multiple-Enhanced Series
4.6.1 N/O Elementary Multiple-Enhanced Circuit
4.6.2 N/O Re-Lift Multiple-Enhanced Circuit
4.6.3 N/O Triple-Lift Multiple-Enhanced Circuit
4.6.4 N/O Higher-Order Lift Multiple-Enhanced Circuit
4.7 Summary of Negative-Output Super-Lift Luo-Converters
4.8 Simulation Results
4.8.1 Simulation Results of an N/O Triple-Lift Circuit
4.8.2 Simulation Results of an N/O Triple-Lift Additional Circuit
4.9 Experimental Results
4.9.1 Experimental Results of an N/O Triple-Lift Circuit
4.9.2 Experimental Results of an N/O Triple-Lift Additional Circuit
4.9.3 Efficiency Comparison of Simulation and Experimental Results
4.9.4 Transient Process and Stability Analysis
Bibliography

5. Positive-Output Cascaded Boost Converters

5.1 Introduction
5.2 Main Series
5.2.1 Elementary Boost Circuit
5.2.2 Two-Stage Boost Circuit
5.2.3 Three-Stage Boost Circuit
5.2.4 Higher-Stage Boost Circuit
5.3 Additional Series
5.3.1 Elementary Boost Additional (Double) Circuit
5.3.2 Two-Stage Boost Additional Circuit
5.3.3 Three-Stage Boost Additional Circuit
5.3.4 Higher-Stage Boost Additional Circuit
5.4 Double Series
5.4.1 Elementary Double Boost Circuit
5.4.2 Two-Stage Double Boost Circuit
5.4.3 Three-Stage Double Boost Circuit
5.4.4 Higher-Stage Double Boost Circuit
5.5 Triple Series
5.5.1 Elementary Triple Boost Circuit
5.5.2 Two-Stage Triple Boost Circuit
5.5.3 Three-Stage Triple Boost Circuit
5.5.4 Higher-Stage Triple Boost Circuit
5.6 Multiple Series
5.6.1 Elementary Multiple Boost Circuit
5.6.2 Two-Stage Multiple Boost Circuit

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5.6.3 Three-Stage Multiple Boost Circuit
5.6.4 Higher-Stage Multiple Boost Circuit
5.7 Summary of Positive-Output Cascaded Boost Converters
5.8 Simulation and Experimental Results
5.8.1 Simulation Results of a Three-Stage Boost Circuit
5.8.2 Experimental Results of a Three-Stage Boost Circuit
5.8.3 Efficiency Comparison of Simulation and Experimental Results
5.8.4 Transient Process
Bibliography

6. Negative-Output Cascaded Boost Converters

6.1 Introduction
6.2 Main Series
6.2.1 N/O Elementary Boost Circuit
6.2.2 N/O Two-Stage Boost Circuit
6.2.3 N/O Three-Stage Boost Circuit
6.2.4 N/O Higher-Stage Boost Circuit
6.3 Additional Series
6.3.1 N/O Elementary Additional Boost Circuit
6.3.2 N/O Two-Stage Additional Boost Circuit
6.3.3 N/O Three-Stage Additional Boost Circuit
6.3.4 N/O Higher-Stage Additional Boost Circuit
6.4 Double Series
6.4.1 N/O Elementary Double Boost Circuit
6.4.2 N/O Two-Stage Double Boost Circuit
6.4.3 N/O Three-Stage Double Boost Circuit
6.4.4 N/O Higher-Stage Double Boost Circuit
6.5 Triple Series
6.5.1 N/O Elementary Triple Boost Circuit
6.5.2 N/O Two-Stage Triple Boost Circuit
6.5.3 N/O Three-Stage Triple Boost Circuit
6.5.4 N/O Higher-Stage Triple Boost Circuit
6.6 Multiple Series
6.6.1 N/O Elementary Multiple Boost Circuit
6.6.2 N/O Two-Stage Multiple Boost Circuit
6.6.3 N/O Three-Stage Multiple Boost Circuit
6.6.4 N/O Higher-Stage Multiple Boost Circuit
6.7 Summary of N/O Cascaded Boost Converters
6.8 Simulation and Experimental Results
6.8.1 Simulation Results of a Three-Stage Boost Circuit
6.8.2 Experimental Results of a Three-Stage Boost Circuit
6.8.3 Efficiency Comparison of Simulation and Experimental Results
6.8.4 Transient Process
Bibliography

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7. Ultra-Lift Luo-Converter

7.1 Introduction
7.2 Operation of Ultra-Lift Luo-Converter
7.2.1 Continuous Conduction Mode
7.2.2 Discontinuous Conduction Mode
7.3 Instantaneous Values
7.3.1 Continuous Conduction Mode
7.3.2 Discontinuous Conduction Mode
7.4 Comparison of the Gain to Other Converters' Gains
7.5 Simulation Results
7.6 Experimental Results
7.7 Summary
Bibliography

8. Hybrid Split Capacitors and Split Inductors Applied in Positive-Output Super-Lift Luo-Converters

8.1 Introduction
8.2 Split Capacitors and Split Inductors
8.2.1 Split Capacitors
8.2.2 Split Inductors
8.3 Split Capacitors and Split Inductors Applied in the P/O Elementary Super-Lift Luo-Converter
8.3.1 Two Split Capacitors ($\alpha = 2$) Applied in the P/O Elementary SL Circuit
8.3.2 Two Split Inductors ($\beta = 2$) Applied in the Elementary P/O SL Circuit
8.3.3 α Split Capacitors and β Split Inductors Applied in the Elementary P/O SL Circuit
8.4 Main Series
8.5 MEC, Split Capacitors Used in DEC
8.6 Additional Series
8.6.1 Elementary Additional Circuit
8.6.2 Re-Lift Additional Circuit
8.6.3 Triple-Lift Additional Circuit
8.6.4 Higher-Order Lift Additional Circuits
8.7 Synthesis of Main Series and Additional Series P/O SL Luo-Converters
8.8 Simulation Results
8.8.1 Simulation Results of a Re-Lift Circuit
8.8.2 Simulation Results of a Triple-Lift Circuit
8.8.3 Simulation Results of a Re-Lift Additional Circuit
8.8.4 Simulation Results of a Triple-Lift Additional Circuit
8.9 Experimental Result
8.9.1 Experimental Results of a Re-Lift Circuit
8.9.2 Experimental Results of a Triple-Lift Circuit
8.9.3 Experimental Results of a Re-Lift Additional Circuit
8.9.4 Experimental Results of a Triple-Lift Additional Circuit
8.10 Transient Process Waveforms

www.EngineeringEBooksPdf.com

8.11 Summary
Bibliography

9. Mathematical Modeling of Power DC/DC Converters

9.1 Introduction
9.2 Energy Factor and Relevant Parameters
9.3 Applications of Parameters
9.3.1 Power Efficiency η
9.3.2 System Stability
9.3.3 Time Constant τ of a Power DC/DC Converter
9.3.4 Damping Time Constant τ_d of a Power DC/DC Converter
9.4 Transfer Function of Power DC/DC Converters
9.4.1 Very Small Variation of Storage Energy
9.4.2 Small Variation of Storage Energy
9.4.3 Critical Variation of Storage Energy
9.4.4 Large Variation of Storage Energy
9.4.5 Explanation of This Mathematical Modeling
9.5 Design Examples of This Theory
9.5.1 Buck Converter
9.5.2 Super-Lift Luo-Converter
9.6 Summary
Bibliography

10. Multiple-Quadrant Operating Luo-Converters

10.1 Introduction
10.2 Circuit Explanation
10.2.1 Mode A
10.2.2 Mode B
10.2.3 Mode C
10.2.4 Mode D
10.2.5 Summary
10.3 Mode A (Quadrant I Operation)
10.3.1 Circuit Description
10.3.2 Variations of Currents and Voltages
10.3.3 Discontinuous Region
10.4 Mode B (Quadrant II Operation)
10.4.1 Circuit Description
10.4.2 Variations of Currents and Voltages
10.4.3 Discontinuous Region
10.5 Mode C (Quadrant III Operation)
10.5.1 Circuit Description
10.5.2 Variations of Currents and Voltages
10.5.3 Discontinuous Region
10.6 Mode D (Quadrant IV Operation)

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10.6.1 Circuit Description
10.6.2 Variations of Currents and Voltages
10.6.3 Discontinuous Region
10.7 Simulation Results
10.8 Experimental Results
10.9 Discussion
10.9.1 Discontinuous Conduction Mode
10.9.2 Comparison with the Double-Output Luo-Converter
10.9.3 Conduction Duty *k*
10.9.4 Switching Frequency *f*
Bibliography

11. Switched-Component Converters
11.1 Introduction
11.2 Two-Quadrant SC DC/DC Converter
11.2.1 Circuit Description
11.2.1.1 Mode A
11.2.1.2 Mode B
11.2.2 Mode A (Quadrant I Operation)
11.2.3 Mode B (Quadrant II Operation)
11.2.4 Experimental Results
11.2.5 Discussion
11.2.5.1 Efficiency
11.2.5.2 Conduction Duty *k*
11.2.5.3 Switching Frequency *f*
11.3 Four-Quadrant Switched-Capacitor DC/DC Luo-Converter
11.3.1 Mode A (Q_I: Forward Motoring)
11.3.1.1 Mode A1: Condition $V_1 > V_2$
11.3.1.2 Mode A2: Condition $V_1 < V_2$
11.3.1.3 Experimental Results
11.3.2 Mode B (Q_{II}: Forward Regenerative Braking)
11.3.2.1 Mode B1: Condition $V_1 > V_2$
11.3.2.2 Mode B2: Condition $V_1 < V_2$
11.3.3 Mode C (Q_{III}: Reverse Motoring)
11.3.4 Mode D (Q_{IV}: Reverse Regenerative Braking)
11.4 Switched-Inductor Four-Quadrant DC/DC Luo-Converter
11.4.1 Mode A (Q_I: Forward Motoring)
11.4.1.1 Continuous Mode
11.4.1.2 Discontinuous Mode
11.4.2 Mode B (Q_{II}: Forward Regenerative Braking)
11.4.2.1 Continuous Mode
11.4.2.2 Discontinuous Mode

www.EngineeringEBooksPdf.com

11.4.3 Mode C (Q_{III}: Reverse Motoring)
11.4.3.1 Continuous Mode
11.4.3.2 Discontinuous Mode
11.4.4 Mode D (Q_{IV}: Reverse Regenerative Braking)
11.4.4.1 Continuous Mode
11.4.4.2 Discontinuous Mode
11.4.5 Experimental Results
Bibliography

12. Positive-Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters
12.1 Introduction
12.2 Main Series
12.2.1 Elementary Circuit
12.2.2 Re-Lift Circuit
12.2.3 Triple-Lift Circuit
12.2.4 Higher-Order Lift Circuit
12.3 Additional Series
12.3.1 Elementary Additional Circuit
12.3.2 Re-Lift Additional Circuit
12.3.3 Triple-Lift Additional Circuit
12.3.4 Higher-Order Lift Additional Circuit
12.4 Enhanced Series
12.4.1 Elementary Enhanced Circuit
12.4.2 Re-Lift Enhanced Circuit
12.4.3 Triple-Lift Enhanced Circuit
12.4.4 Higher-Order Enhanced Lift Circuit
12.5 Re-Enhanced Series
12.5.1 Elementary Re-Enhanced Circuit
12.5.2 Re-Lift Re-Enhanced Circuit
12.5.3 Triple-Lift Re-Enhanced Circuit
12.5.4 Higher-Order Lift Re-Enhanced Circuit
12.6 Multiple-Enhanced Series
12.6.1 Elementary Multiple-Enhanced Circuit
12.6.2 Re-Lift Multiple-Enhanced Circuit
12.6.3 Triple-Lift Multiple-Enhanced Circuit
12.6.4 Higher-Order Lift Multiple-Enhanced Circuit
12.7 Theoretical Analysis
12.8 Summary of This Technique
12.9 Simulation Results
12.9.1 Triple-Lift Circuit
12.9.2 Triple-Lift Additional Circuit
12.10 Experimental Result
12.10.1 Triple-Lift Circuit
12.10.2 Triple-Lift Additional Circuit

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Bibliography

13. Negative-Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

13.1 Introduction
13.2 Main Series
13.2.1 N/O Elementary Circuit
13.2.2 N/O Re-Lift Circuit
13.2.3 N/O Triple-Lift Circuit
13.2.4 N/O Higher-Order Lift Circuit
13.3 Additional Series
13.3.1 N/O Elementary Additional Circuit
13.3.2 N/O Re-Lift Additional Circuit
13.3.3 N/O Triple-Lift Additional Circuit
13.3.4 N/O Higher-Order Lift Additional Circuit
13.4 Enhanced Series
13.4.1 N/O Elementary Enhanced Circuit
13.4.2 N/O Re-Lift Enhanced Circuit
13.4.3 N/O Triple-Lift Enhanced Circuit
13.4.4 N/O Higher-Order Lift Enhanced Circuit
13.5 Re-Enhanced Series
13.5.1 N/O Elementary Re-Enhanced Circuit
13.5.2 N/O Re-Lift Re-Enhanced Circuit
13.5.3 N/O Triple-Lift Re-Enhanced Circuit
13.5.4 N/O Higher-Order Lift Re-Enhanced Circuit
13.6 Multiple-Enhanced Series
13.6.1 N/O Elementary Multiple-Enhanced Circuit
13.6.2 N/O Re-Lift Multiple-Enhanced Circuit
13.6.3 N/O Triple-Lift Multiple-Enhanced Circuit
13.6.4 N/O Higher-Order Lift Multiple-Enhanced Circuit
13.7 Summary of This Technique
13.8 Simulation and Experimental Results
13.8.1 Simulation Results
13.8.2 Experimental Results
Bibliography

14. Multiple-Quadrant Soft-Switching Converters

14.1 Introduction
14.2 Multiple-Quadrant DC/DC ZCS Quasi-Resonant Luo-Converters
14.2.1 Mode A
14.2.1.1 Interval $t = 0-t_1$
14.2.1.2 Interval $t = t_1-t_2$
14.2.1.3 Interval $t = t_2-f_3$
14.2.1.4 Interval $t = t_3-t_4$

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14.2.2 Mode B
14.2.2.1 Interval $t = 0-t_1$
14.2.2.2 Interval $t = t_1-t_2$
14.2.2.3 Interval $t = t_2-t_3$
14.2.2.4 Interval $t = t_3-t_4$
14.2.3 Mode C
14.2.3.1 Interval $t = 0-t_1$
14.2.3.2 Interval $t = t_1-t_2$
14.2.3.3 Interval $t = t_2-t_3$
14.2.3.4 Interval $t = t_3-t_4$
14.2.4 Mode D
14.2.4.1 Interval $t = 0-t_1$
14.2.4.2 Interval $t = t_1-t_2$
14.2.4.3 Interval $t = t_2-t_3$
14.2.4.4 Interval $t = t_3-t_4$
14.2.5 Experimental Results
14.3 Multiple-Quadrant DC/DC ZVS Quasi-Resonant Luo-Converters
14.3.1 Mode A
14.3.1.1 Interval $t = 0-t_1$
14.3.1.2 Interval $t = t_1-t_2$
14.3.1.3 Interval $t = t_2-t_3$
14.3.1.4 Interval $t = t_3-t_4$
14.3.2 Mode B
14.3.2.1 Interval $t = 0-t_1$
14.3.2.2 Interval $t = t_1-t_2$
14.3.2.3 Interval $t = t_2-t_3$
14.3.2.4 Interval $t = t_3-t_4$
14.3.3 Mode C
14.3.3.1 Interval $t = 0-t_1$
14.3.3.2 Interval $t = t_1-t_2$
14.3.3.3 Interval $t = t_2-t_3$
14.3.3.4 Interval $t = t_3-t_4$
14.3.4 Mode D
14.3.4.1 Interval $t = 0-t_1$
14.3.4.2 Interval $t = t_1-t_2$
14.3.4.3 Interval $t = t_2-t_3$
14.3.4.4 Interval $t = t_3-t_4$
14.3.5 Experimental Results
14.4 Multiple-Quadrant ZT DC/DC Luo-Converters

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14.4.1 Mode A (Quadrant I Operation)
14.4.2 Mode B (Quadrant II Operation)
14.4.3 Mode C (Quadrant III Operation)
14.4.4 Mode D (Quadrant IV Operation)
14.4.5 Simulation Results
14.4.6 Experimental Results
14.4.7 Design Considerations
Bibliography

15. Synchronous Rectifier DC/DC Converters

15.1 Introduction
15.2 Flat Transformer Synchronous Rectifier Luo-Converter
15.2.1 Transformer Is in Magnetizing Process
15.2.2 Switching-On
15.2.3 Transformer Is in Demagnetizing Process
15.2.4 Switching-Off
15.2.5 Summary
15.3 Active-Clamped Synchronous Rectifier Luo-Converter
15.3.1 Transformer Is in Magnetizing Process
15.3.2 Switching-On
15.3.3 Transformer Is in Demagnetizing Process
15.3.4 Switching-Off
15.3.5 Summary
15.4 Double-Current Synchronous Rectifier Luo-Converter
15.4.1 Transformer Is in Magnetizing Process
15.4.2 Switching-On
15.4.3 Transformer Is in Demagnetizing Process
15.4.4 Switching-Off
15.4.5 Summary
15.5 Zero-Current-Switching Synchronous Rectifier Luo-Converter
15.5.1 Transformer Is in Magnetizing Process
15.5.2 Resonant Period
15.5.3 Transformer Is in Demagnetizing Process
15.5.4 Switching-Off
15.5.5 Summary
15.6 Zero-Voltage-Switching Synchronous Rectifier Luo-Converter
15.6.1 Transformer Is in Magnetizing Process
15.6.2 Resonant Period
15.6.3 Transformer Is in Demagnetizing Process
15.6.4 Switching-Off
15.6.5 Summary
Bibliography

16. Multiple-Energy-Storage-Element Resonant Power Converters

www.EngineeringEBooksPdf.com

16.1 Introduction
16.1.1 Two-Element RPC
16.1.2 Three-Element RPC
16.1.3 Four-Element RPC
16.2 Bipolar Current and Voltage Sources
16.2.1 Bipolar Voltage Source
16.2.1.1 Two-Voltage Source Circuit
16.2.1.2 One-Voltage Source Circuit
16.2.2 Bipolar Current Source
16.2.2.1 Two-Voltage Source Circuit
16.2.2.2 One-Voltage Source Circuit
16.3 Two-Element RPC Analysis
16.3.1 Input Impedance
16.3.2 Current Transfer Gain
16.3.3 Operation Analysis
16.3.4 Simulation Results
16.3.5 Experimental Results
Bibliography

17. Π-CLL Current Source Resonant Inverter
17.1 Introduction
17.1.1 Pump Circuits
17.1.2 Current Source
17.1.3 Resonant Circuit
17.1.4 Load
17.1.5 Summary
17.2 Mathematical Analysis
17.2.1 Input Impedance
17.2.2 Components' Voltages and Currents
17.2.3 Simplified Impedance and Current Gain
17.2.4 Power Transfer Efficiency
17.3 Simulation Results
17.4 Discussion
17.4.1 Function of the Π-CLL Circuit
17.4.2 Applying Frequency to This Π-CLL CSRI
17.4.3 Explanation of $g > 1$
17.4.4 DC Current Component Remaining
17.4.5 Efficiency
Bibliography

18. Cascade Double Γ-CL Current Source Resonant Inverter
18.1 Introduction
18.2 Mathematical Analysis
18.2.1 Input Impedance

www.EngineeringEBooksPdf.com

18.2.2 Components' Voltages and Currents
18.2.3 Simplified Impedance and Current Gain
18.2.4 Power Transfer Efficiency
18.3 Simulation Result
18.3.1 β = 1, f = 33.9 kHz, and T = 29.5 μs
18.3.2 β = 1.4142, f = 48.0 kHz, and T = 20.83 μs
18.3.3 β = 1.59, f = 54 kHz, and T = 18.52 μs
18.4 Experimental Result
18.5 Discussion
18.5.1 Function of the Double Γ-CL Circuit
18.5.2 Applying Frequency to This Double Γ-CL CSRI
18.5.3 Explanation of $g > 1$
Bibliography

19. Cascade Reverse Double Γ-LC Resonant Power Converter
19.1 Introduction
19.2 Steady-State Analysis of Cascade Reverse Double Γ-LC RPC
19.2.1 Topology and Circuit Description
19.2.2 Classical Analysis on AC Side
19.2.2.1 Basic Operating Principles
19.2.2.2 Equivalent Load Resistance
19.2.2.3 Equivalent AC Circuit and Transfer Functions
19.2.2.4 Analysis of Voltage Transfer Gain and the Input Impedance
19.2.3 Simulation and Experiment Results
19.2.3.1 Simulation Studies
19.2.3.2 Experimental Results
19.3 Resonance Operation and Modeling
19.3.1 Operating Principle, Operating Modes, and Equivalent Circuits
19.3.2 State-Space Analysis
19.4 Small-Signal Modeling of Cascade Reverse Double Γ-LC RPC
19.4.1 Small-Signal Modeling Analysis
19.4.1.1 Model Diagram
19.4.1.2 Nonlinear State Equation
19.4.1.3 Harmonic Approximation
19.4.1.4 Extended Describing Function
19.4.1.5 Harmonic Balance
19.4.1.6 Perturbation and Linearization
19.4.1.7 Equivalent Circuit Model
19.4.2 Closed-Loop Control System Design
19.5 Discussion
19.5.1 Characteristics of Variable-Parameter Resonant Converter
19.5.2 DCM
Appendix: Parameters Used in Small-Signal Modeling
Bibliography

www.EngineeringEBooksPdf.com

20. DC Energy Sources for DC/DC Converters
20.1 Introduction
20.2 Single-Phase Half-Wave Diode Rectifier
20.2.1 Resistive Load
20.2.2 Single-Phase Half-Wave Rectifier with a Capacitive Filter
20.2.3 Inductive Load
20.2.4 Pure Inductive Load
20.2.5 Back EMF plus Resistor Load
20.2.6 Back EMF plus Inductor Load
20.3 Single-Phase Bridge Diode Rectifier
20.3.1 Resistive Load
20.3.2 Back EMF Load
20.3.3 *R-C* Load
20.4 Three-Phase Half-Bridge Diode Rectifier
20.4.1 Resistive Load
20.4.2 Back EMF Load ($0.5\sqrt{2}V_{in} < E \sqrt{2}V_{in}$)
20.4.3 Back EMF Load ($E < 0.5\sqrt{2}V_{in}$)
20.5 Three-Phase Full-Bridge Diode Rectifier with Resistive Load
20.6 Thyristor Rectifiers
20.6.1 Single-Phase Half-Wave Rectifier with Resistive Load
20.6.2 Single-Phase Half-Wave Thyristor Rectifier with Inductive Load
20.6.3 Single-Phase Half-Wave Thyristor Rectifier with Pure Inductive Load
20.6.4 Single-Phase Half-Wave Rectifier with Back EMF plus Resistive Load
20.6.5 Single-Phase Half-Wave Rectifier with Back EMF plus Inductive Load
20.6.6 Single-Phase Half-Wave Rectifier with Back EMF Plus Pure Inductor
20.6.7 Single-Phase Full-Wave Semicontrolled Rectifier with Inductive Load
20.6.8 Single-Phase Full-Controlled Rectifier with Inductive Load
20.6.9 Three-Phase Half-Wave Rectifier with Resistive Load
20.6.10 Three-Phase Half-Wave Thyristor Rectifier with Inductive Load
20.6.11 Three-Phase Full-Wave Thyristor Rectifier with Resistive Load
20.6.12 Three-Phase Full-Wave Thyristor Rectifier with Inductive Load
Bibliography

21. Control Circuit: EMI and Application Examples of DC/DC Converters
21.1 Introduction
21.2 Luo-Resonator
21.2.1 Circuit Explanation
21.2.2 Calculation Formulae
21.2.3 Design Example
21.2.4 Discussion
21.3 EMI, EMS, and EMC
21.3.1 EMI/EMC Analysis
21.3.2 Comparison with Hard Switching and Soft Switching

www.EngineeringEBooksPdf.com

21.3.3 Measuring Method and Results
21.3.4 Designing Rule to Minimize EMI/EMC
21.4 Some DC/DC Converter Applications
21.4.1 5000 V Insulation Test Bench
21.4.2 MIT 42/14 V 3 kW DC/DC Converter
21.4.3 IBM 1.8 V/200 A Power Supply
Bibliography
Index

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Preface to the Second Edition

The first edition of this book was published in 2004. Since then, we have received a great deal of feedback from readers around the world. In this second edition, we would like to retrench and update the contents to include new techniques developed over the past 12 years, improve the book based on readers' suggestions, and correct some typographical errors.

Super-lift technique is an outstanding achievement in DC/DC conversion technology. As new developments, the ultra-lift technique and hybrid split capacitor/split inductor applied in super-lift Luo-converters are introduced in Chapters 7 and 8 in this edition. They are superior to the super-lift technique in achieving higher-voltage transfer gain. Some industrial applications demonstrate their versatile and powerful characteristics.

Mathematical modeling for power DC/DC converters is a historical problem accompanying DC/DC conversion technology since the 1940s. Traditional mathematical modeling is not available for complex structure converters because the differential equation order of these converters is very high. We have theoretically defined a new concept—the energy factor (EF)—and demonstrated the relations between EF and the mathematical modeling for power DC/DC converters and applied the modeling method in two converters in Chapter 9. This investigation is very helpful for the system design and the prediction of DC/DC converter characteristics.

Organization of This Book

This book is organized into 21 chapters. The knowledge on DC/DC conversion is introduced in Chapter 1 and that on voltage-lift converters in Chapter 2. Chapters 3, 4, 5 and 6 present the four-series super-lift converters. Chapters 7 and 8 are added to introduce the new developments in DC/DC converters: the ultra-lift Luo-converter and the split capacitor/split inductor techniques in positive-output super-lift Luo-converters. Chapter 9 discusses the novel mathematical modeling concept and method for DC/DC converters. Chapter 10 introduces second-generation converters and Chapter 11 the third-generation converters. Chapters 12 and 13 focus on two-series multiple-lift push-pull switched-capacitor converters. Chapters 14, 15, 16, 17, 18 and 19 cover fourth-, fifth-, and sixth-generation converters. Chapter 20 introduces various DC voltage sources, and Chapter 21 includes the gating-signal generator and electromagnetic interference (EMI)/electromagnetic compatibility (EMC) with some applications.

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Preface to the First Edition

The purpose of this book is to provide up-to-date information on advanced DC/DC converters that is both concise and useful for engineering students and practicing professionals. It is well organized in 748 pages with 320 diagrams to introduce more than 100 topologies of the advanced DC/DC converters originally developed by the authors. EMI/EMC reduction and various DC voltage sources are also illustrated in this book. All prototypes represent novel approaches and great contributions to modern power engineering.

Power engineering is the method used to supply electrical energy from a source to its users. It is of vital importance to the industry. It is likely that the air we breathe and the water we drink are taken for granted until they are not there. Energy conversion technique is the main focus of power engineering. The corresponding equipment can be divided into four groups:

1. AC/AC transformers
2. AC/DC rectifiers
3. DC/DC converters
4. DC/AC inverters

From recent reports, the production of DC/DC converters occupies the largest percentage of the total turnover of all conversion equipment production. DC/DC conversion technology is progressing rapidly. According to incomplete statistics, there are more than 500 topologies of DC/DC converters existing, with new topologies created every year. It is a lofty undertaking to treat the large number of DC/DC converters. The authors have sorted these converters into six generations since 2001. This systematical work is very helpful for DC/DC converter's evolution and development. The converters are listed as follows:

1. First-generation (classical/traditional) converters
2. Second-generation (multiple-quadrant) converters
3. Third-generation (switched-component) converters
4. Fourth-generation (soft-switching) converters
5. Fifth-generation (synchronous rectifier) converters
6. Sixth-generation (multiple-element resonant power) converters

A review of the DC/DC conversion technique development reveals that the idea was induced from other equipment. Transformers successfully convert an AC source voltage to other AC output voltage(s) with very high efficiency. Rectifier devices such as diode, transistor, and thyristor effectively rectify an AC source voltage to DC output voltage. Nearly eight decades ago people sought to invent equipment to convert a DC source voltage to another DC output voltage(s) with high efficiency. Unfortunately, no such simple apparatus, such as a transformer and/or rectifier, was found for DC/DC conversion purpose.

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High-frequency switch-on and switch-off semiconductor devices paved the way for chopper circuits. This invention inspired the idea for DC/DC conversion. Therefore, the fundamental DC/DC converters were derived from the corresponding choppers. At present, the fundamental converters—buck converter, boost converter, and buck-boost converter—are still the basic circuits for DC/DC conversion technique in research and development.

The voltage-lift technique is a popular method that is widely applied in electronic circuit design. Applying this technique effectively overcomes the effects of parasitic elements and greatly increases the output voltage. Therefore, these DC/DC converters can convert the source voltage into a higher output voltage with high power efficiency, high power density, and simple structure. It is applied in the periodical switching circuit. Usually, a capacitor is charged during switch-on by a certain voltage. This charged capacitor voltage can be arranged on top-up to output voltage during switch-off. Therefore, the output voltage can be lifted. A typical example is the sawtooth-wave generator with a voltage-lift circuit.

The voltage-lift technique has been successfully employed in the design of DC/DC converters. However, its output voltage increases in arithmetic progression, stage by stage. The super-lift technique is a great achievement in DC/DC conversion technology. It is more powerful than the voltage-lift technique; the output voltage transfer gain of super-lift converters can be very high, which increases in geometric progression, stage by stage. It effectively enhances the voltage transfer gain in power series. Four-series super-lift converters created by the authors are introduced in this book. Some industrial applications verified their versatile and powerful characteristics.

Multiple-quadrant operation is often required in industrial applications. Most publications in the literature concentrate on the single-quadrant operation. This fact is reasonable since most novel approaches were derived from its simple structure. To compensate for these losses, the authors have spent much time and spirit to develop multiple-quadrant converters and positive-negative converters in various generations.

This book is organized into 18 chapters. The DC/DC conversion technique is introduced in Chapter 1 and the voltage-lift converters in Chapter 2. Chapters 3, 4, 5 and 6 introduce the four-series super-lift converters. Chapter 7 introduces the second-generation converters and Chapter 8 the third-generation converters. Chapters 9 and 10 introduce the two-series multiple-lift push-pull switched-capacitor converters. Chapter 11 introduces the fourth-generation converters and Chapter 12 the fifth-generation converters. Chapters 13, 14, 15 and 16 introduce the sixth-generation converters. Chapter 17 introduces various DC voltage sources, and Chapter 18 introduces the gating-signal generator, EMI/EMC, and some applications.

The authors are pioneers in DC/DC conversion technology. They have devoted many years to this research area and created a large number of outstanding converters, including world-renowned series DC/DC converters, namely, Luo-converters, which cover all six-generation converters. Super-lift converters are our favorite achievement in our 20-year research fruits. Our biographies and information are provided on the following page.

We acknowledge the executive editor for this book.

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Introduction

Conversion technique is a major research area in the field of power electronics and has applications in industry, research and development, government organizations, and daily life. It can be divided into four technologies:

1. AC/AC converters
2. AC/DC rectifiers
3. DC/DC converters
4. DC/AC inverters

According to an incomplete statistics, there have been more than 800 prototypes of DC/DC converters developed in the past seven decades. All existing DC/DC converters were designed to meet the requirements of certain applications. They are usually named by their function, for example, buck converter, boost converter, and buck-boost converter, and zero-current-switching (ZCS) and zero-voltage-switching (ZVS) converters. The large number of DC/DC converters had not been evolutionarily classified until 2001, by the authors of this book. The authors have systematically classified DC/DC converters into six generations according to their characteristics and sequence of development, to be introduced in this chapter. This categorizes all existing DC/DC converters and new prototypes. Since the DC/DC converter family tree was built in 2001, this classification has been recognized worldwide. Following this categorization, it is now easy to sort and allocate DC/DC converters and assess their specific technical features.

1.1 Historical Review

DC/DC conversion technology is a major subject area in the field of power engineering and drives and is widely used in industrial applications and computer hardware circuits. DC/DC converters have been under rapid development for seven decades since the 1940s. In addition to its high growth rate, the DC/DC converter market is undergoing dramatic changes as a result of two major trends in the electronics industry: high voltage and high power density. The production of DC/DC converters in the world market is much higher than that of AC/DC converters.

The DC/DC conversion technique was established in the 1920s. A simple voltage conversion, the simplest DC/DC converter is a voltage divider (e.g., rheostat and potential meter), but it only transfers output voltage lower than input voltage with poor efficiency. The multiple-quadrant chopper is the second step in DC/DC conversion. Much time has been spent

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trying to find equipment to convert the DC energy source of one voltage to another DC actuator with another voltage, as does a transformer employed in AC/AC conversion.

Some preliminary types of DC/DC converters were used in industrial applications before the Second World War. Research was hindered during the war, but applications of DC/DC converters were recognized. After the war, communication technology developed very rapidly and required low-voltage DC power supplies. This resulted in the rapid development of DC/DC conversion techniques. Preliminary prototypes can be derived from choppers.

In the 1940s, the buck converter was derived from the "A"-type chopper. The boost converter was derived later from the "B"-type chopper. The buck-boost converter was invented after buck converter and boost converter, and its output voltage is negative. In the 1990s, two types of positive-output (P/O) voltage converters called "P/O buck-boost converter" and "P/O buck and boost converters" were invented.

The 1980s and 1990s are the decades called the "DC/DC conversion prosperous decades." Hundreds of DC/DC converters were invented during this period, such as Cúk converter, single-ended primary inductance converter (SEPIC), Luo-converters, and soft-switching converters. Extending the developing impetus, many new types of DC/DC converters followed, such as super-lift (SL) Luo-converters, cascaded boost converters, switched-capacitor converters, and synchronous rectifier (SR) converters.

SL conversion technique, invented by the authors of this book, is the summit in the DC/DC conversion development till now. The voltage transfer gain can be hundreds to thousands of times. Its great impact inspired emergence of high-output-voltage converters using this technique, such as SL Luo-converters and split capacitor/inductor SL Luo-converters. IEEE Magazine admired the authors of this book as the pioneers in the advanced conversion technology.

DC/DC converter's mathematical modeling is a historic problem accompanying DC/DC conversion development since the 1940s. The traditional mathematical modeling is not available for complex structure converters because of the very high-order differential equations involved. Many experts have devoted in this subject area. Unfortunately, their modelings did not provide any clear concept to describe the relationship between the stored energy and the characteristics of power DC/DC converters. We proposed a mathematical modeling in Chapter 9 that is generally applicable for all power DC/DC converters and is well recognized over the world.

1.2 Multiple-Quadrant Choppers

Choppers are the circuits that convert fixed DC voltage to variable DC voltage or pulse-width-modulated AC voltage. In this book, we concentrate on its first function.

1.2.1 Multiple-Quadrant Operation

A DC motor can run in forward running or reverse running. During the forward starting process, its armature voltage and armature current are both positive. We usually call this

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forward motoring operation or *quadrant I* operation. During the forward braking process, its armature voltage is still positive and its armature current is negative. This state is called the forward regenerating operation or *quadrant II* operation. Analogously, during the reverse starting process, the DC motor armature voltage and current are both negative. This reverse motoring operation is called the *quadrant III* operation.

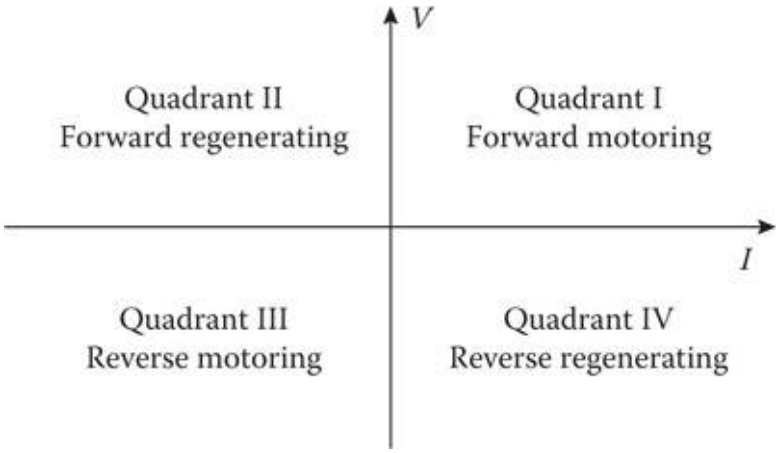


FIGURE 1.1
Four-quadrant operation.

During the reverse braking process, its armature voltage is still negative and its armature current is positive. This state is called the reverse regenerating operation or *quadrant IV* operation.

Referring to the DC motor operation states, we can define the multiple-quadrant operation as follows:

Quadrant I operation: Forward motoring, voltage is positive and current is positive.
Quadrant II operation: Forward regenerating, voltage is positive and current is negative.
Quadrant III operation: Reverse motoring, voltage is negative and current is negative.
Quadrant IV operation: Reverse regenerating, voltage is negative and current is positive.

The operation status is shown in Figure 1.1. Choppers can convert a fixed DC voltage into various other voltages. The corresponding chopper is usually named according to its quadrant operation chopper, for example, the first-quadrant chopper or "A"-type chopper. In the following description, we use the symbols V_{in} as the fixed voltage, V_p the chopped voltage, and V_o the output voltage.

1.2.2 First-Quadrant Chopper

The first-quadrant chopper is also called "A"-type chopper, and its circuit diagram is shown in Figure 1.2a and corresponding waveforms are shown in Figure 1.2b. The switch *S* can be some semiconductor devices such as BJT, IGBT, and MOSFET. Assuming all parts are ideal components, the output voltage is calculated by the formula

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$$V_o = \frac{t_{on}}{T} V_{in} = kV_{in} \tag{1.1}$$

where

T is the repeating period, $T = 1/f$ (where f is the chopping frequency)

t_{on} is the switch-on time

k is the conduction duty cycle, $k = t_{on}/T$

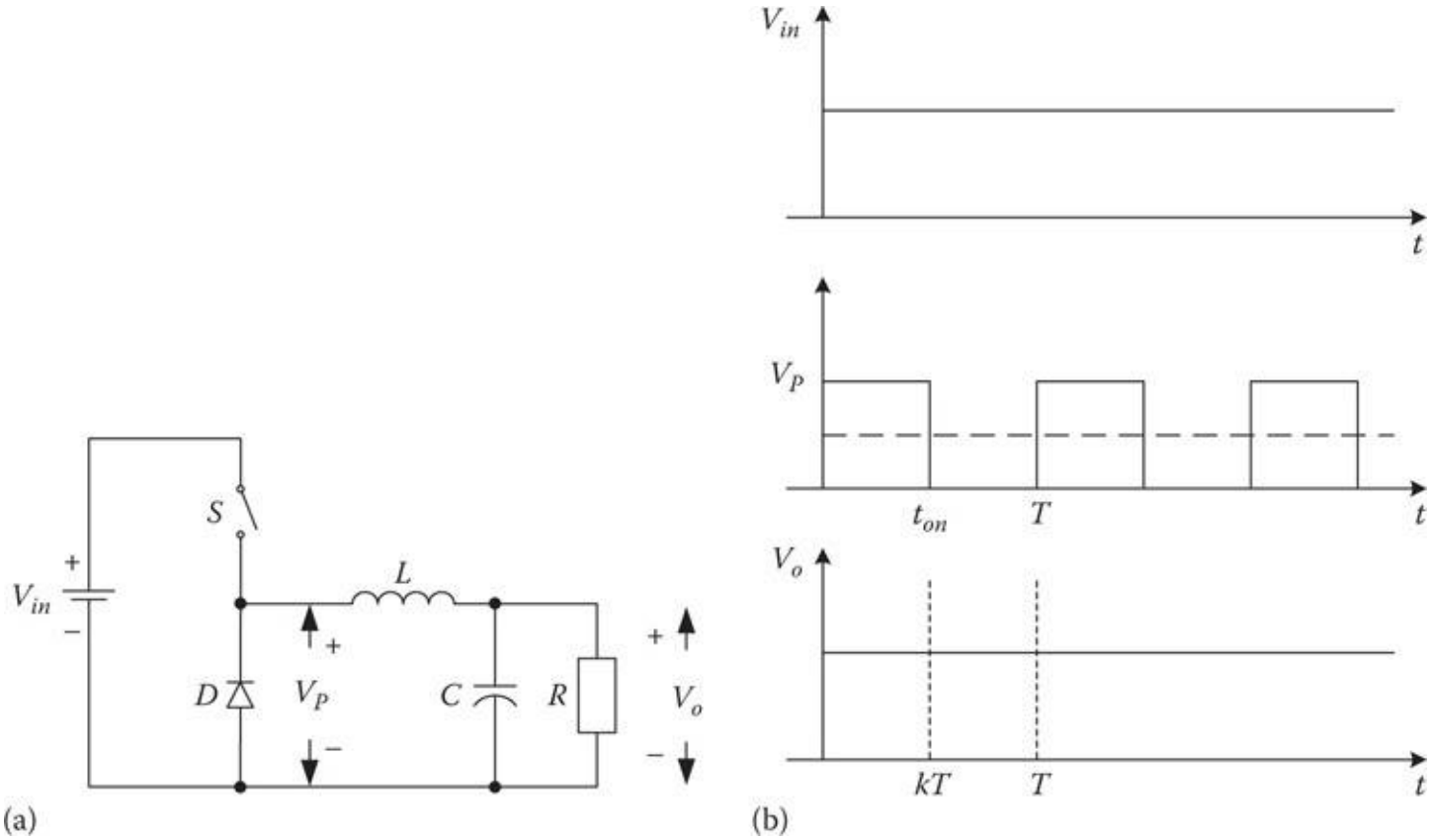


FIGURE 1.2
First-quadrant chopper: (a) circuit diagram and (b) voltage waveforms.

1.2.3 Second-Quadrant Chopper

The second-quadrant chopper is also called "B"-type chopper. The circuit diagram and corresponding waveforms are shown in Figure 1.3a and b. The output voltage can be calculated by the formula

$$V_o = \frac{t_{off}}{T} V_{in} = (1-k)V_{in} \tag{1.2}$$

1.2.4 Third-Quadrant Chopper

The third-quadrant chopper and corresponding waveforms are shown in Figure 1.4a and b. All voltage polarities are defined in the figure. The output voltage (absolute value) can be calculated by the formula

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$$V_o = \frac{t_{on}}{T} V_{in} = kV_{in} \tag{1.3}$$

1.2.5 Fourth-Quadrant Chopper

The fourth-quadrant chopper and corresponding waveforms are shown in Figure 1.5a and b. All voltage polarities are defined in the figure. The output voltage (absolute value) can be calculated by the formula

$$V_o = \frac{t_{off}}{T} V_{in} = (1-k)V_{in} \tag{1.4}$$

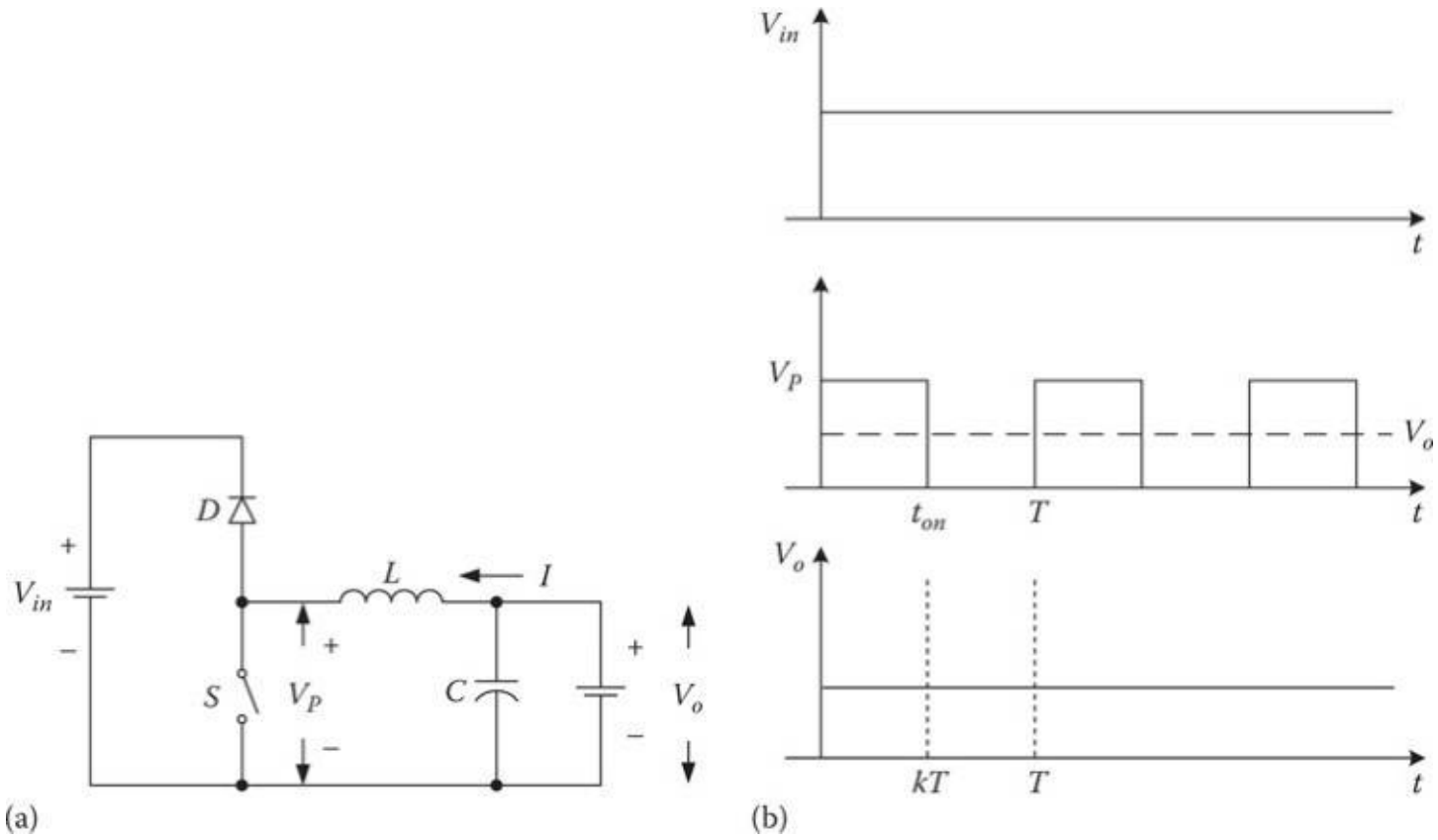


FIGURE 1.3
Second-quadrant chopper: (a) circuit diagram and (b) voltage waveforms.

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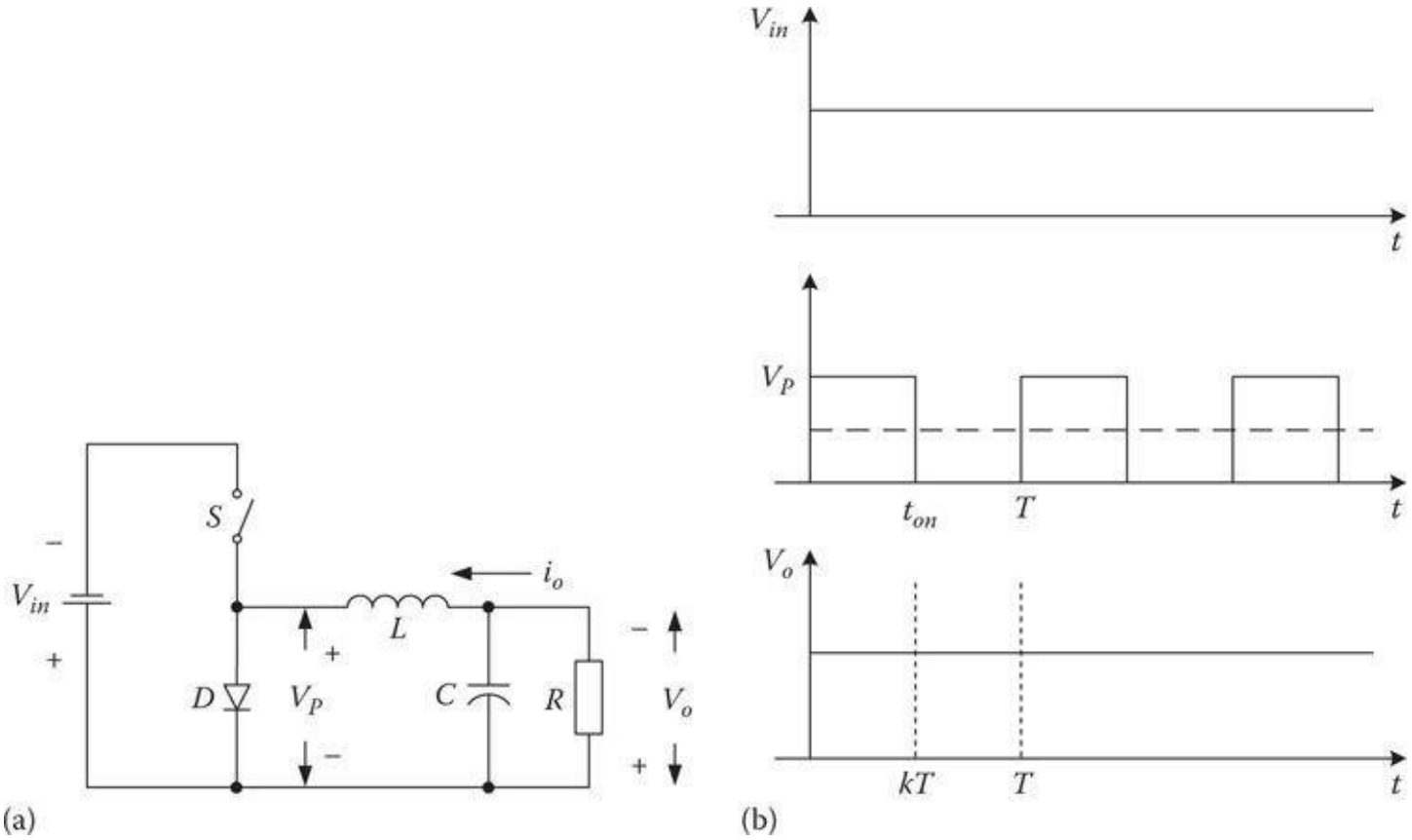


FIGURE 1.4
Third-quadrant chopper: (a) circuit diagram and (b) voltage waveforms.

1.2.6 First- and Second-Quadrant Chopper

The first-second-quadrant chopper is shown in Figure 1.6a. Dual-quadrant operation is usually requested in the system with two voltage sources V_1 and V_2. Assume that the condition $V_1 > V_2$ and the inductor L is an ideal component. During quadrant I operation, S_1 and D_2 work and S_2 and D_1 are idle. Vice versa, during quadrant II operation, S_2 and D_1 work and S_1 and D_2 are idle. The relation between the two voltage sources can be calculated by the formula

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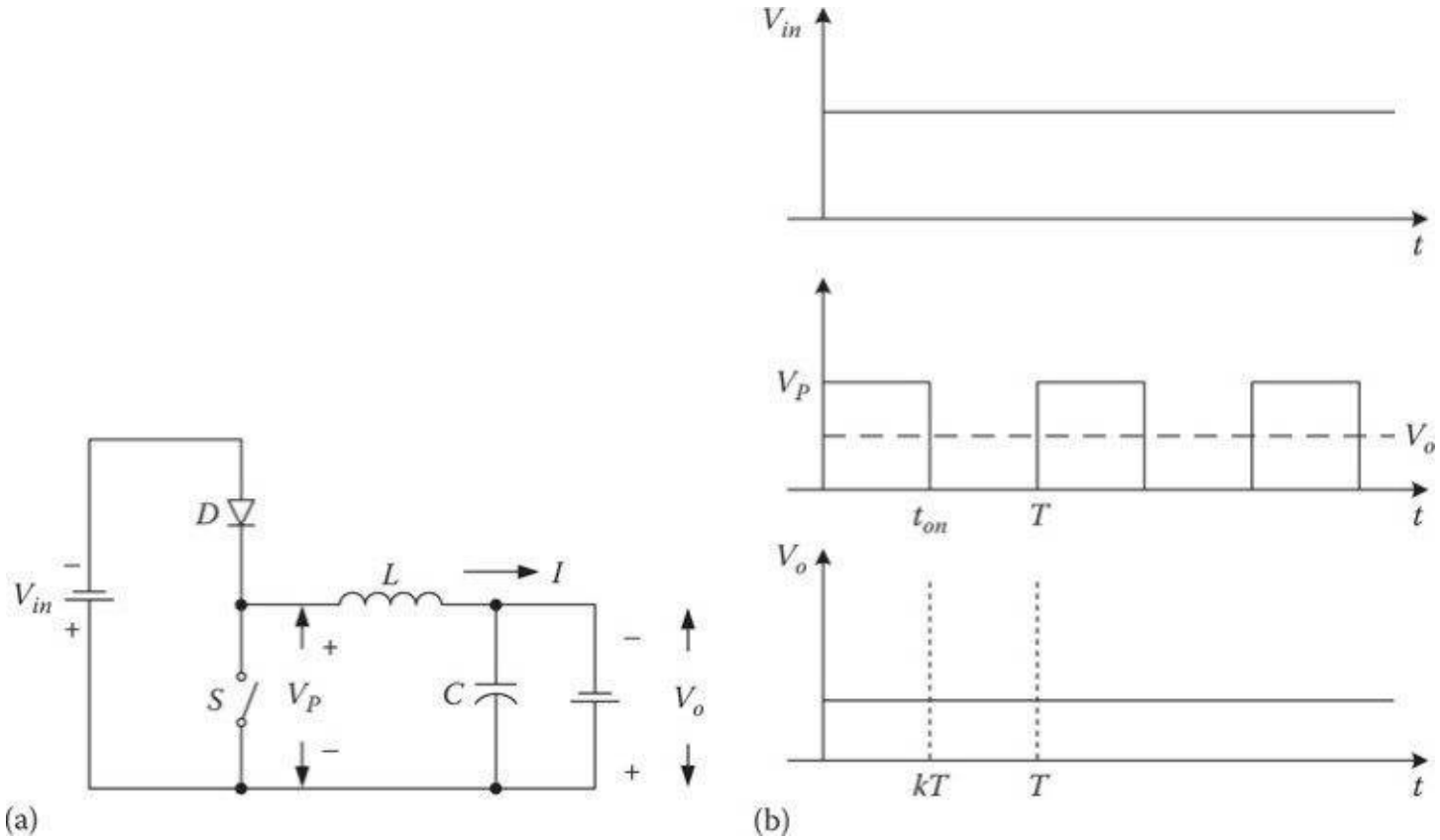


FIGURE 1.5
Fourth-quadrant chopper: (a) circuit diagram and (b) voltage waveforms.

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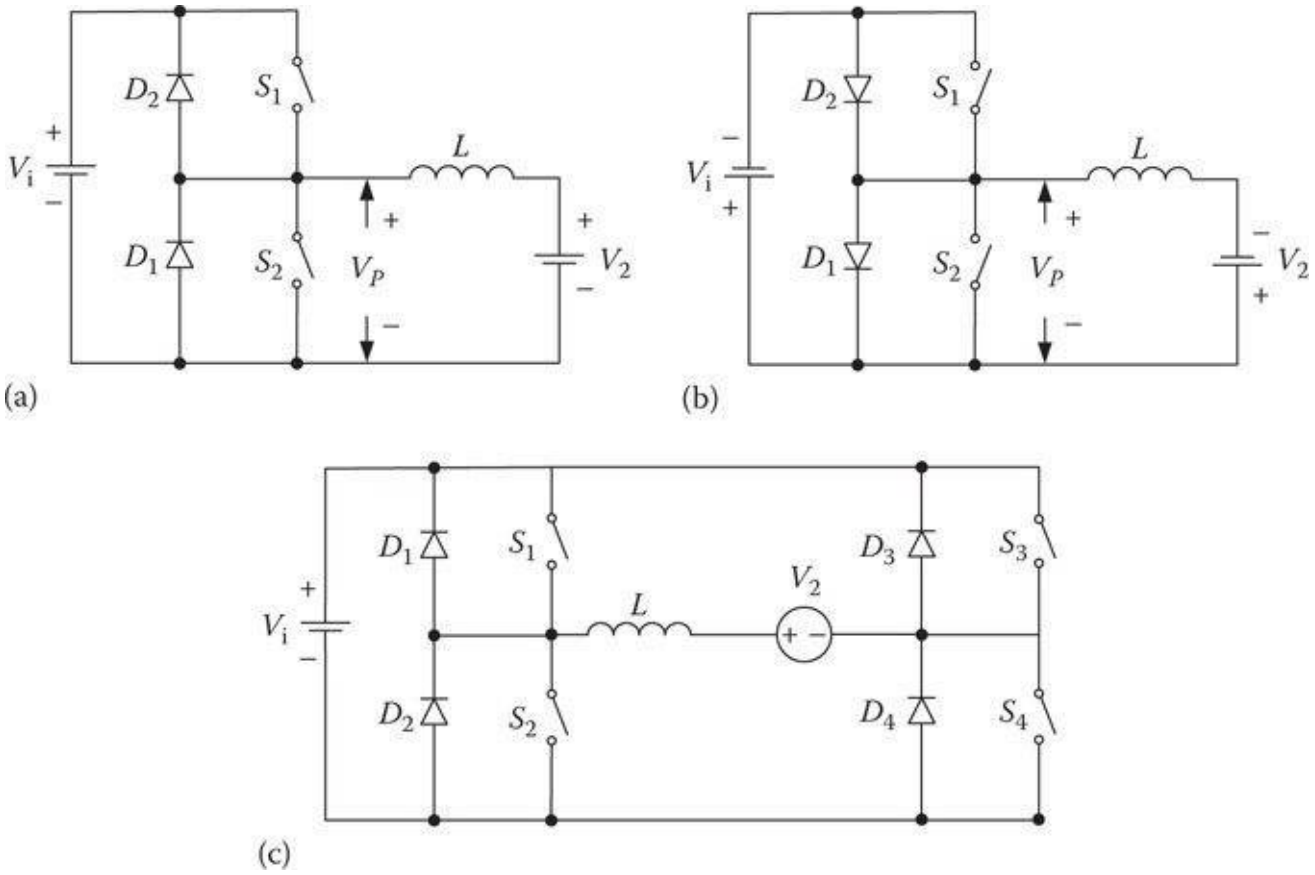


FIGURE 1.6
Multiquadrant choppers: (a) first-second-quadrant chopper; (b) third-fourth-quadrant chopper; and (c) fourth-quadrant chopper.

$$V_2 = \begin{cases} kV_1 & QI_operation \\ (1-k)V_1 & QII_operation \end{cases} \tag{1.5}$$

1.2.7 Third-Fourth-Quadrant Chopper

The third-fourth-quadrant chopper is shown in Figure 1.6b. Dual-quadrant operation is usually requested in the system with two voltage sources V_1 and V_2. Both voltage polarities are defined in the figure; we just concentrate their absolute values in analysis and calculation. Assume that the condition is $V_1 > V_2$; the inductor L is an ideal component. During quadrant I operation, S_1 and D_2 work and S_2 and D_1 are idle. Vice versa, during quadrant II operation, S_2 and D_1 work and S_1 and D_2 are idle. The relation between the two voltage sources can be calculated by the formula

$$V_2 = \begin{cases} kV_1 & QIII_operation \\ (1-k)V_1 & QIV_operation \end{cases} \tag{1.6}$$

1.2.8 Four-Quadrant Chopper

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The four-quadrant chopper is shown in Figure 1.6c. The input voltage is positive, and the output voltage can be either positive or negative. The switches and diode status for the operation are shown in Table 1.1. The output voltage can be calculated by the formula

$$V_2 = \begin{cases} kV_1 & QI_operation \\ (1-k)V_1 & QII_operation \\ -kV_1 & QIII_operation \\ -(1-k)V_1 & QIV_operation \end{cases} \tag{1.7}$$

TABLE 1.1
Switches and Diodes' Status for Four-Quadrant Operation

Switch or Diode	Quadrant I	Quadrant II	Quadrant III	Quadrant IV
S_1	Works	Idle	Idle	Works
D_1	Idle	Works	Works	Idle
S_2	Idle	Works	Works	Idle
D_2	Works	Idle	Idle	Works
S_3	Idle	Idle	On	Idle
D_3	Idle	Idle	Idle	On
S_4	On	Idle	Idle	Idle
D_4	Idle	On	Idle	Idle
Output	V_{2+}, I_{2+}	V_{2+}, I_{2-}	V_{2-}, I_{2-}	V_{2-}, I_{2+}

1.3 Pump Circuits

The electronic pump is a major component of all DC/DC converters. Historically, they can be sorted into four groups:

1. Fundamental pumps
2. Developed pumps
3. Transformer-type pumps
4. SL pumps

1.3.1 Fundamental Pumps

Fundamental pumps are developed from corresponding fundamental DC/DC converters:

- Buck pump
- Boost pump
- Buck-boost pump

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All fundamental pumps consist of three components: a switch *S*, a diode *D*, and an inductor *L*.

1.3.1.1 Buck Pump

The circuit diagram of the buck pump and some current waveforms are shown in Figure 1.7. Switch *S* and diode *D* are alternatively on and off. Usually, the buck pump works in continuous operation mode; inductor current is continuous in this case.

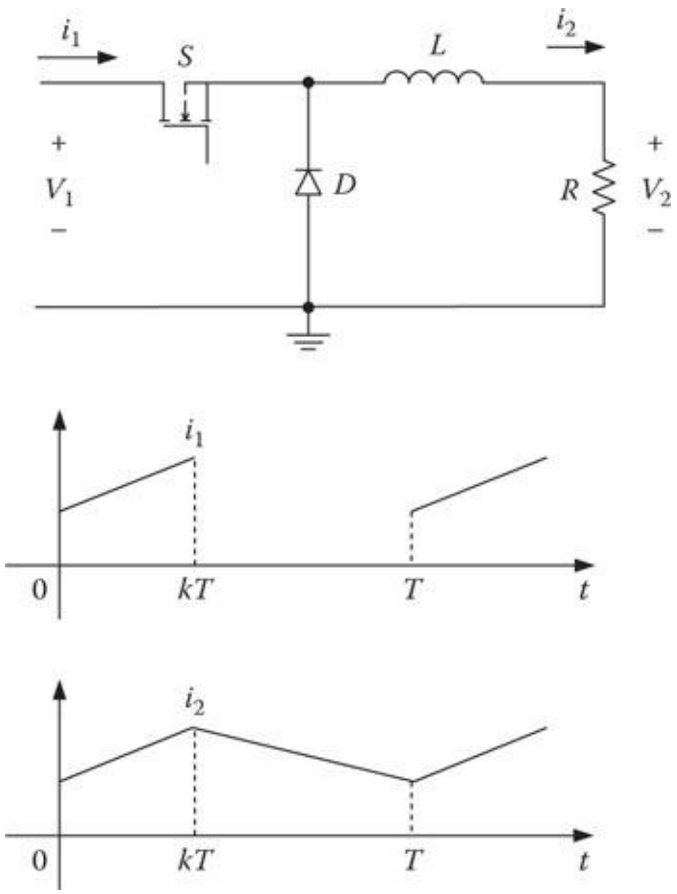


FIGURE 1.7
Buck pump.

1.3.1.2 Boost Pump

The circuit diagram of the boost pump and some current waveforms are shown in Figure 1.8. Switch S and diode *D* are alternatively on and off. The inductor current is constantly continuous, no matter continuous, or discontinuous of the diode current.

1.3.1.3 Buck-Boost Pump

The circuit diagram of the buck-boost pump and some current waveforms are shown in Figure 1.9. Switch *S* and diode *D* are alternatively on and off. Usually, the buck-boost pump works in continuous operation mode, and the inductor current is continuous in this case.

1.3.2 Developed Pumps

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Developed pumps are created from the corresponding developed DC/DC converters:

- Positive Luo-pump
- Negative Luo-pump
- Cúk pump

All developed pumps consist of four components: a switch *S*, a diode *D*, a capacitor *C*, and an inductor *L*.

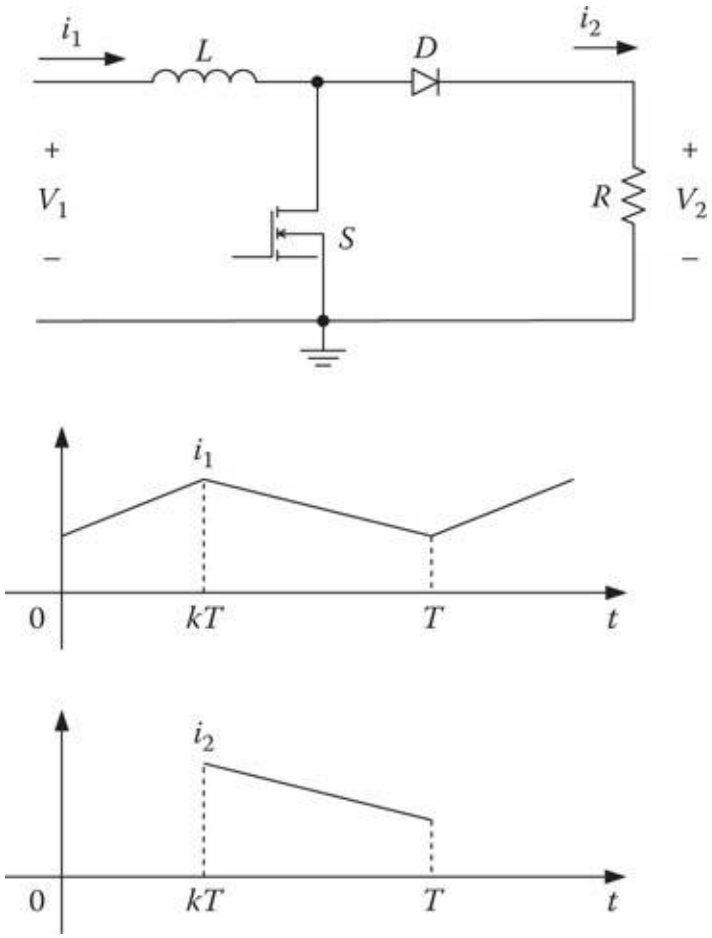


FIGURE 1.8
Boost pump.

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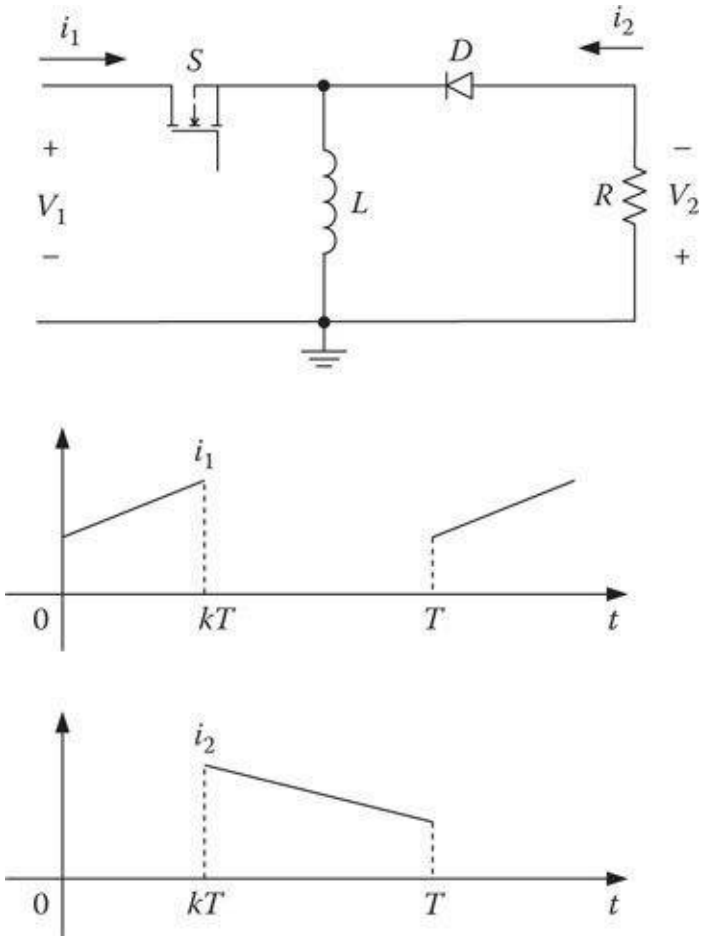


FIGURE 1.9
Buck-boost pump.

1.3.2.1 Positive Luo-Pump

The circuit diagram of the positive Luo-pump and some current and voltage waveforms are shown in Figure 1.10. Switch *S* and diode *D* are alternatively on and off. Usually, this pump works in continuous operation mode; inductor current is continuous in this case. The output terminal voltage and current are usually positive.

1.3.2.2 Negative Luo-Pump

The circuit diagram of the negative Luo-pump and some current and voltage waveforms are shown in Figure 1.11. Switch *S* and diode *D* are alternatively on and off. Usually, this pump works in continuous operation mode; inductor current is continuous in this case. The output terminal voltage and current are usually negative.

1.3.2.3 Cúk Pump

The circuit diagram of the Cúk pump and some current and voltage waveforms are shown in Figure 1.12. Switch *S* and diode *D* are alternatively on and off. Usually, the Cúk pump works in continuous operation mode; inductor current is continuous in this case. The output terminal voltage and current are usually negative.

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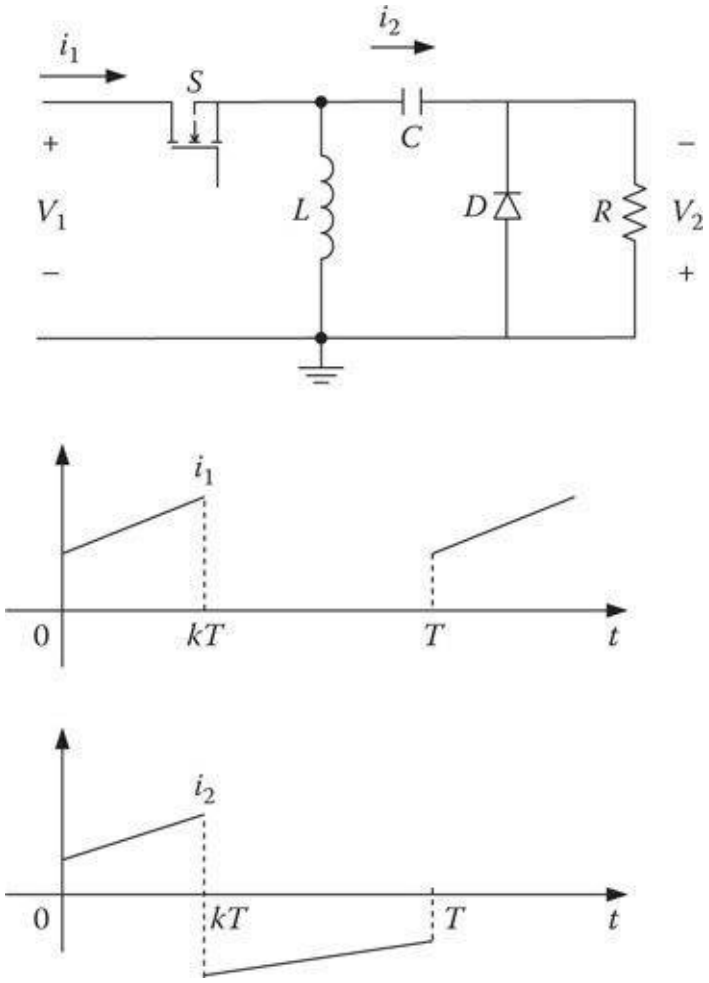


FIGURE 1.10
Positive Luo-pump.

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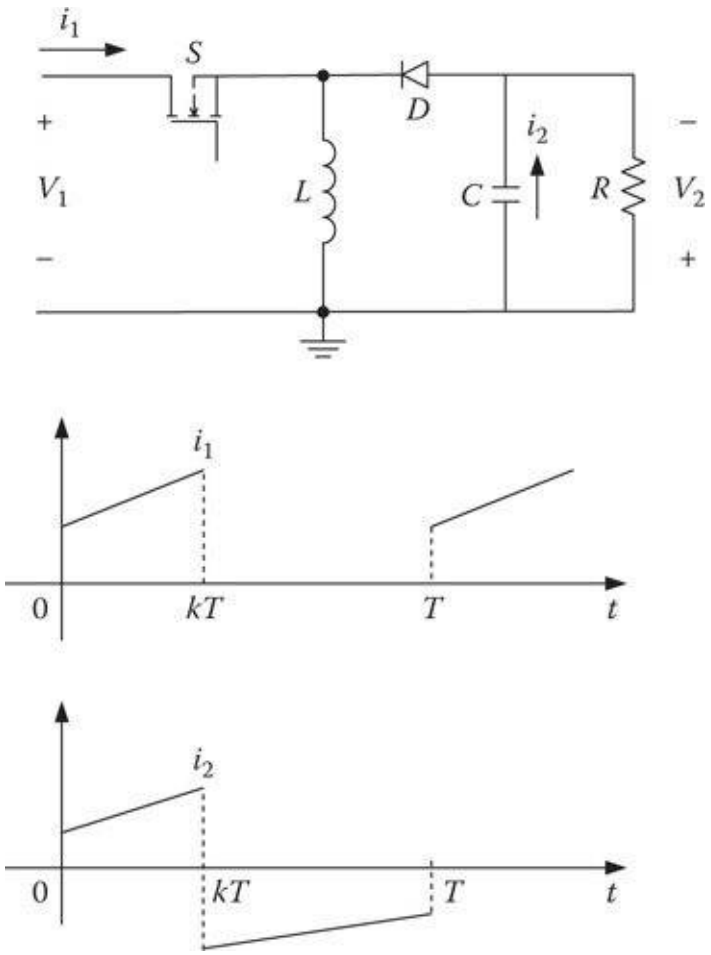


FIGURE 1.11
Negative Luo-pump.

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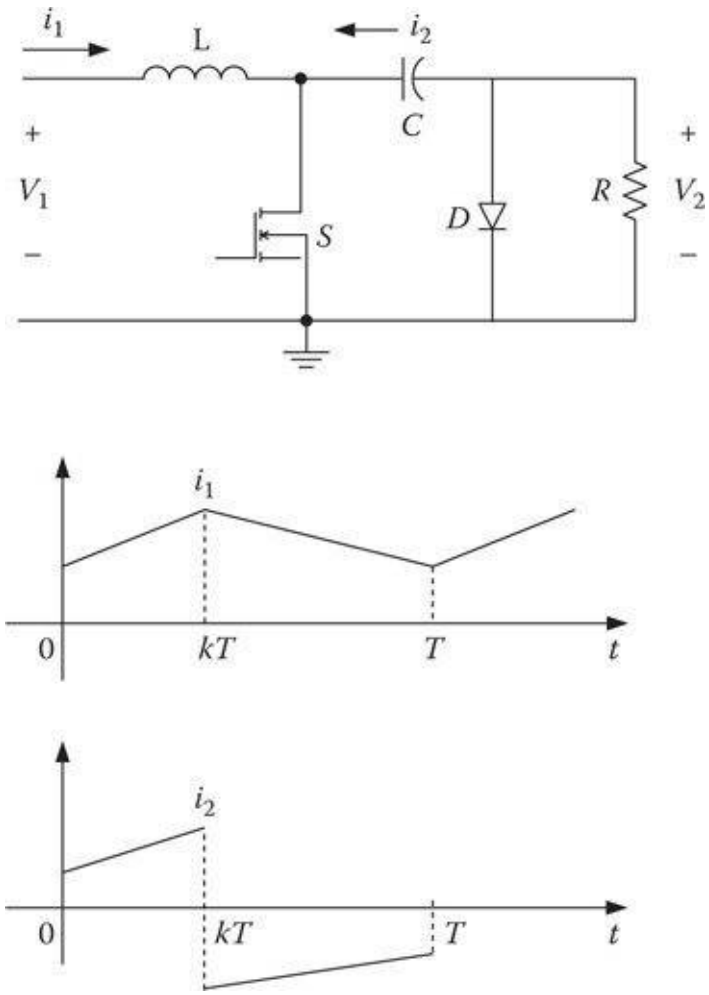


FIGURE 1.12
Cúk pump.

1.3.3 Transformer-Type Pumps

Transformer-type pumps are developed from corresponding transformer-type DC/DC converters:

- Forward pump
- Flyback pump
- ZETA pump

All transformer-type pumps consist of a switch *S*, a transformer with the turns ratio *N*, and other components such as diode *D* (one or more) and capacitor *C*.

1.3.3.1 Forward Pump

The circuit diagram of the forward pump and some current waveforms are shown in Figure 1.13. Switch *S* and diode D_1 are synchronously on and off, and diode D_2 is alternatively off and on. Usually, the forward pump works in discontinuous operation mode; input current is discontinuous in this case.

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1.3.3.2 Flyback Pump

The circuit diagram of the flyback pump and some current waveforms are shown in Figure 1.14. Since the primary and secondary windings of the transformer are purposely arranged in inverse polarities, switch *S* and diode *D* are alternatively on and off. Usually, the flyback pump works in discontinuous operation mode; input current is discontinuous in this case.

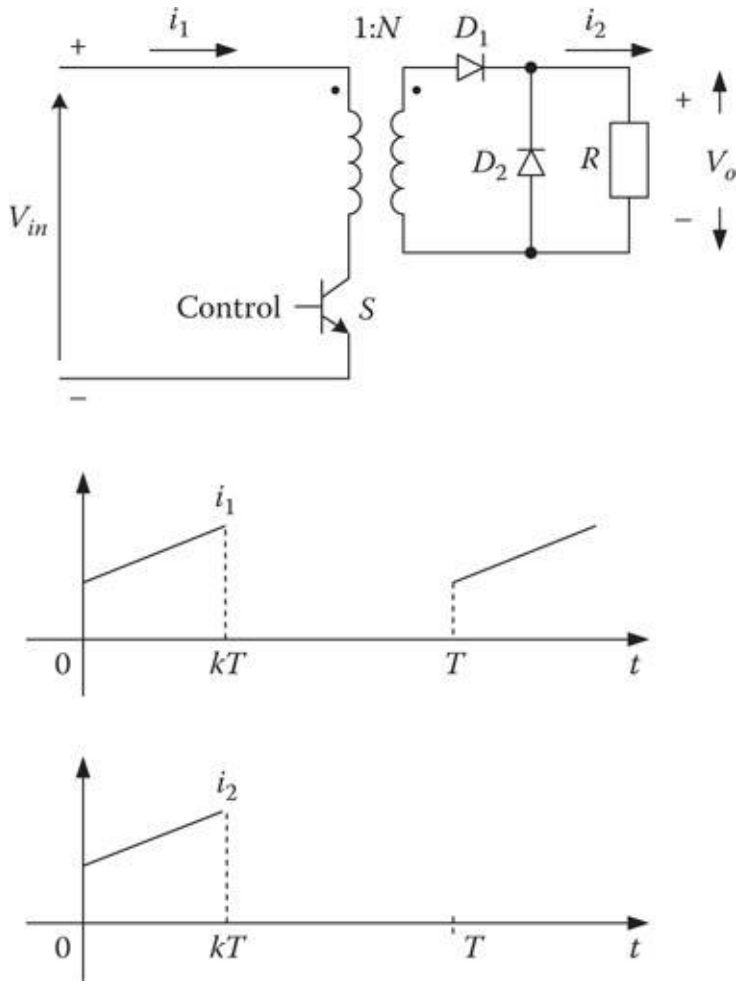


FIGURE 1.13
Forward pump.

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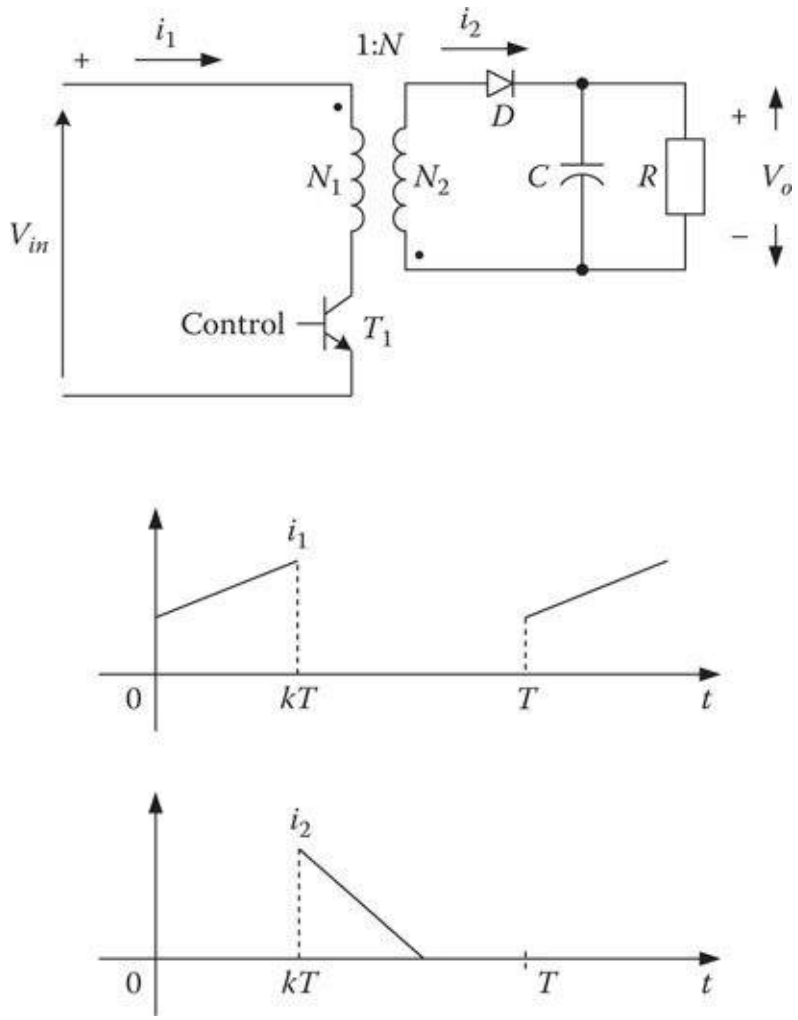


FIGURE 1.14
Flyback pump.

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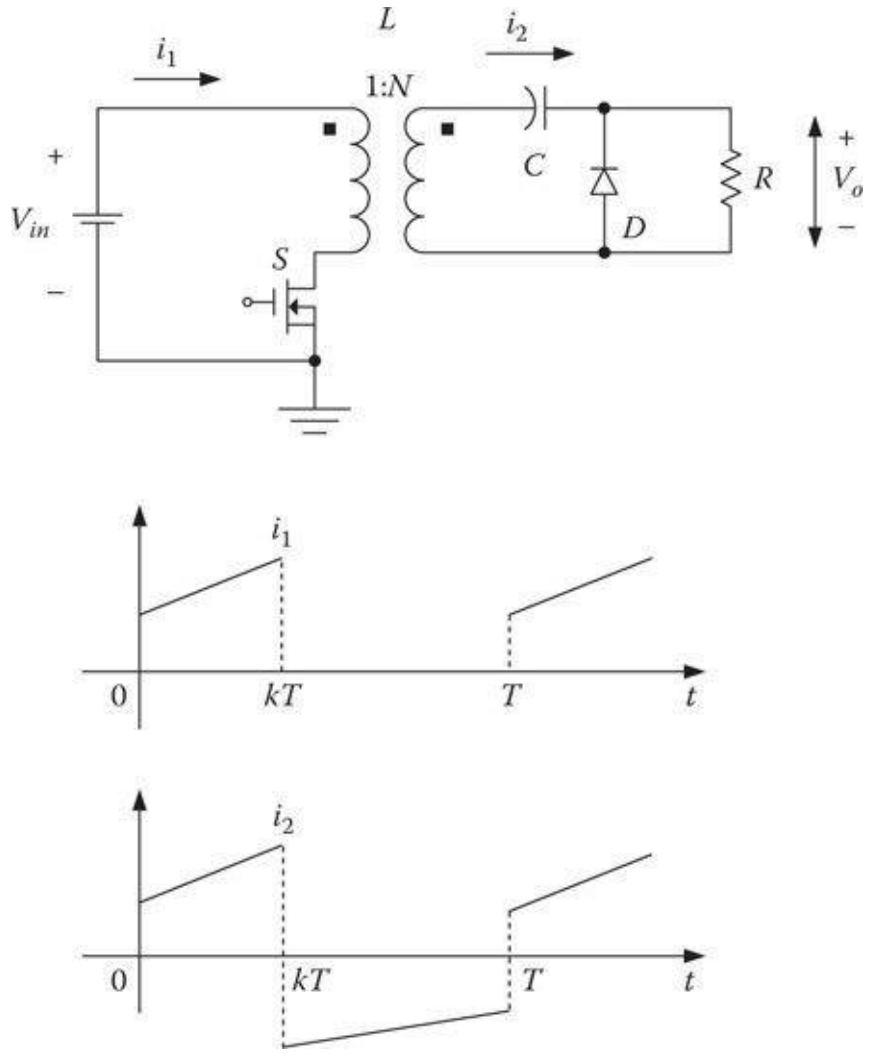


FIGURE 1.15
ZETA pump.

1.3.3.3 ZETA Pump

The circuit diagram of the ZETA pump and some current waveforms are shown in Figure 1.15. Switch *S* and diode *D* are alternatively on and off. Usually, the ZETA pump works in discontinuous operation mode; input current is discontinuous in this case.

1.3.4 SL Pumps

SL pumps are developed from corresponding SL DC/DC converters, indicated by their names:

- Positive super Luo-pump
- Negative super Luo-pump
- Positive push-pull pump
- Negative push-pull pump
- Double/enhanced circuit (DEC)

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All SL pumps consist of more components like switches, diodes, capacitors, and sometimes an inductor.

1.3.4.1 Positive Super Luo-Pump

The circuit diagram of the positive SL pump and some current waveforms are shown in Figure 1.16. Switch S and diode D_1 are synchronously on and off, but diode D_2 is alternatively off and on. Usually, the positive SL pump works in continuous conduction mode (CCM); inductor current is continuous in this case.

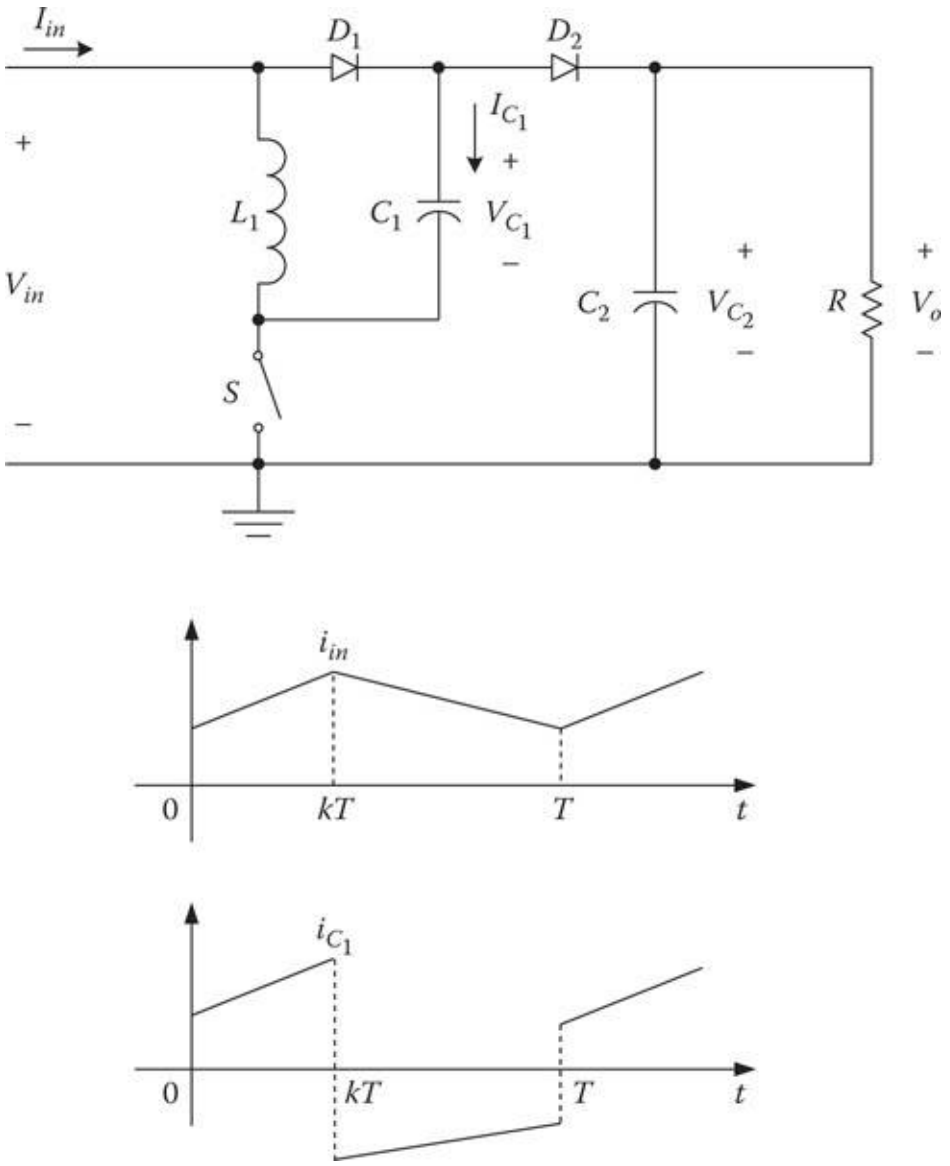


FIGURE 1.16
Positive super Luo-pump.

1.3.4.2 Negative Super Luo-Pump

The circuit diagram of the negative SL pump and some current waveforms are shown in Figure 1.17. Switch S and diode D_1 are synchronously on and off, but diode D_2 is alternatively

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off and on. Usually, the negative SL pump works in CCM, but input current is discontinuous in this case.

1.3.4.3 Positive Push-Pull Pump

All push-pull pumps consist of two switches without any inductor. They can be employed in multiple-lift switched-capacitor converters. The circuit diagram of positive push-pull pump and some current waveforms are shown in Figure 1.18. Since there is no inductor in the pump, it is particularly applied in switched-capacitor converters. The main switch S and diode D_1 are synchronously on and off, but the slave switch S_1 and diode D_2 are alternatively off and on. Usually, the positive push-pull pump works in push-pull-state continuous operation mode.

1.3.4.4 Negative Push-Pull Pump

The circuit diagram of this push-pull pump and some current waveforms are shown in Figure 1.19. Similar to push-pull pumps, there is no inductor in the pump, and it is particularly used in switched-capacitor converters. The main switch S and diode D are synchronously on and off, but the slave switch S_1 is alternatively off and on. Usually, the SL pump works in push-pull-state continuous operation mode; inductor current is continuous in this case.

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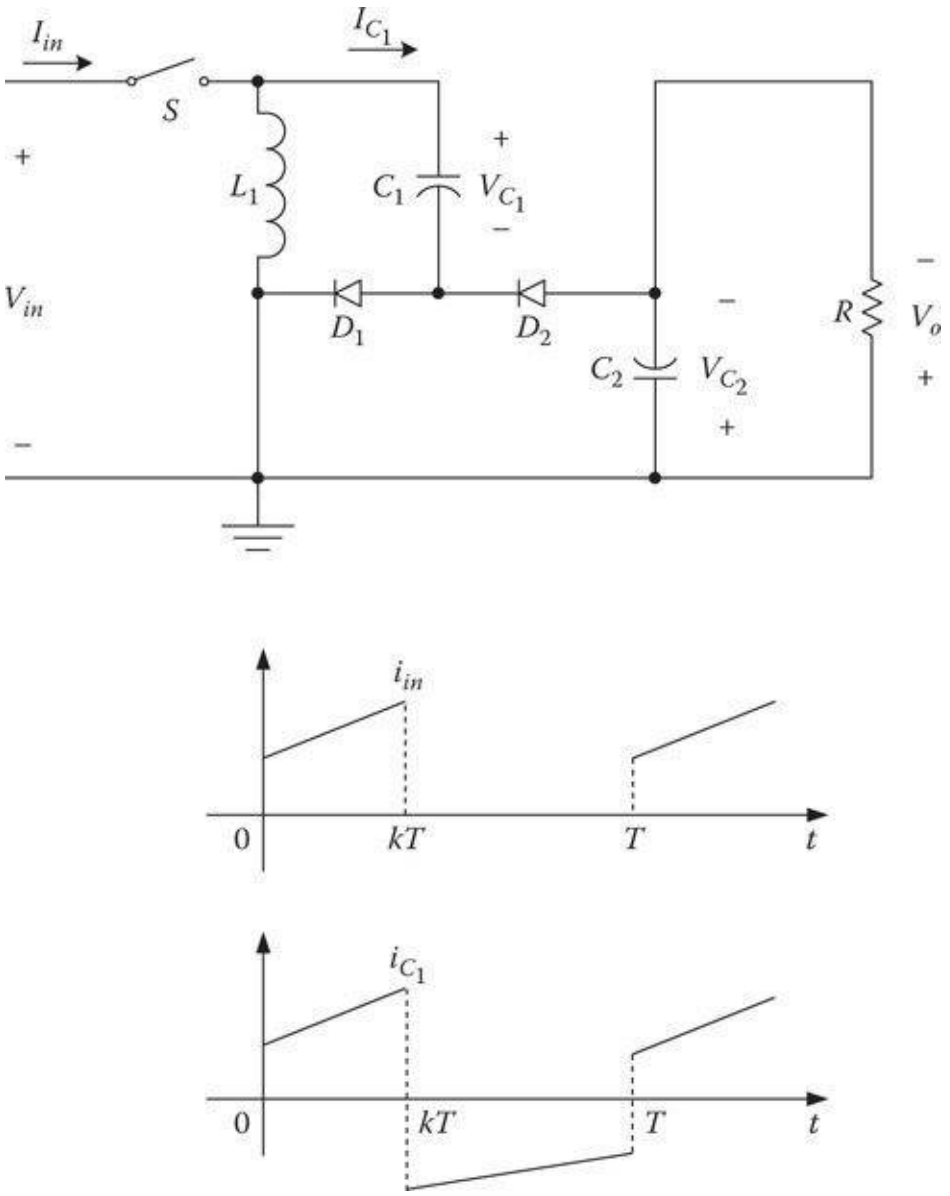


FIGURE 1.17
Negative super Luo-pump.

1.3.4.5 DEC

The circuit diagram of the DEC and some current waveforms are shown in Figure 1.20. This circuit is particularly used in lift, SL, and push-pull converters. These two diodes are alternatively on and off so that two capacitors are alternatively charging and discharging. Usually, this circuit can enhance the voltage twice or more at certain times.

1.4 Development of DC/DC Conversion Technique

According to an incomplete statistics, there are more than 800 existing prototypes of DC/DC converters. The main purpose of this book is to categorize all existing prototypes of DC/DC

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converters. It is of vital importance for future development of DC/DC conversion techniques. The authors have devoted more than 30 years in conversion techniques, and their work has been recognized and assessed by experts worldwide. The authors classify all existing prototypes of DC/DC converters into six generations:

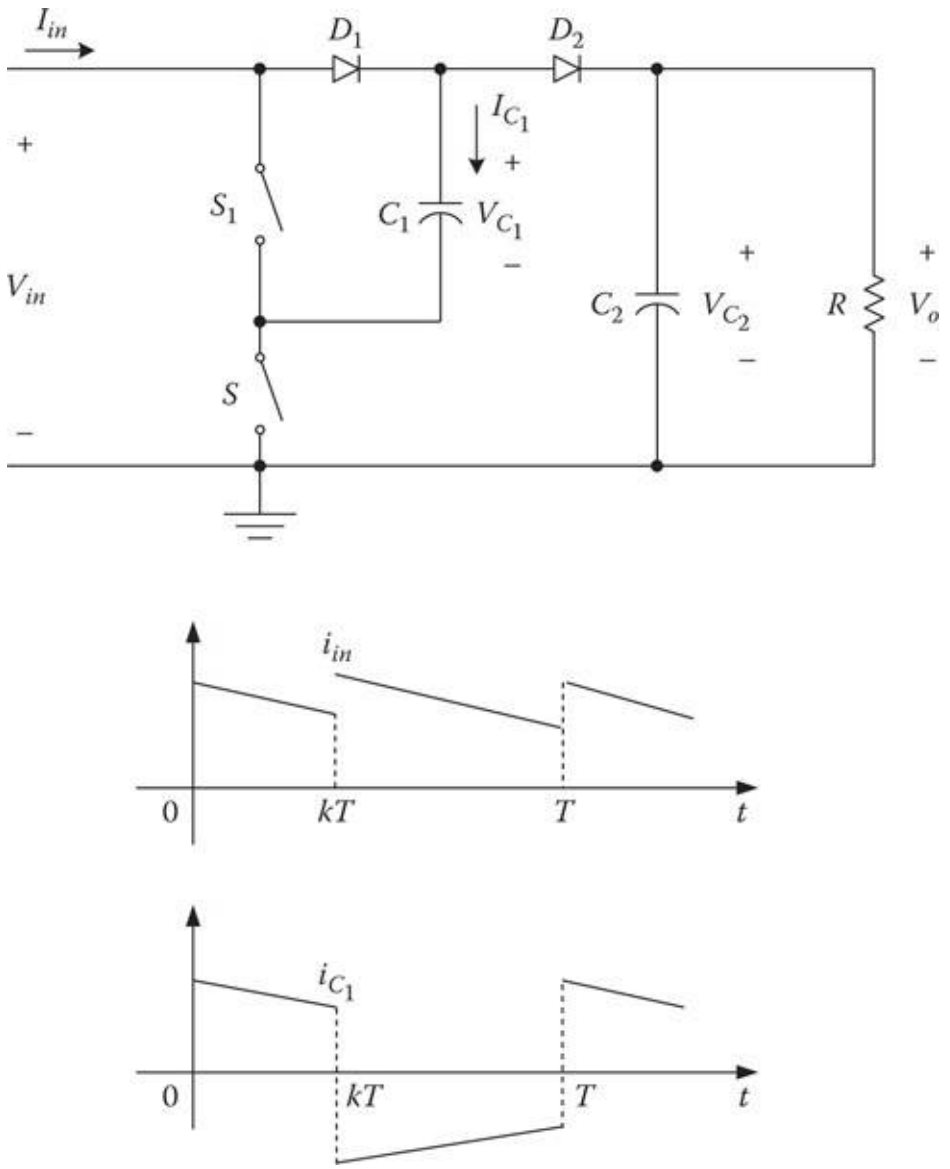


FIGURE 1.18
Positive push–pull pump.

- First-generation (classical/traditional) converters
- Second-generation (multiquadrant) converters
- Third-generation (switched-component: *SI/SC*) converters
- Fourth-generation (soft-switching: *ZCS/ZVS/zero-transition* [*ZT*]) converters
- Fifth-generation (*SR*) converters
- Sixth-generation (multiple-energy-storage-element resonant [*MER*]) converters

1.4.1 First-Generation Converters

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The first-generation converters perform in a single-quadrant mode and in a low power range (up to around 100 W). Since their development lasts a long time, they have, briefly, five categories:

1. Fundamental converters
2. Transformer-type converters
3. Developed converters
4. Voltage-lift (VL) converters
5. SL converters

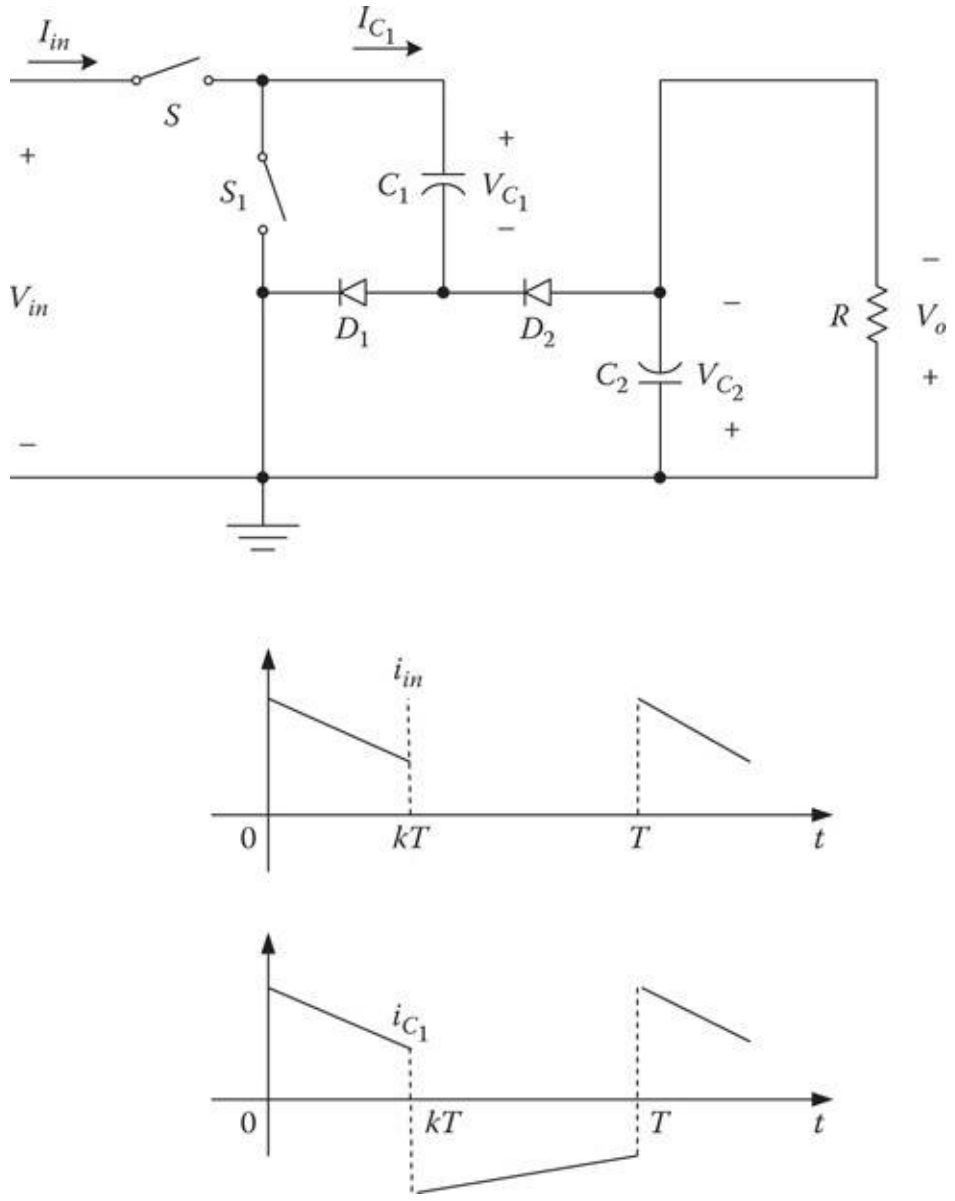


FIGURE 1.19
Negative push-pull pump.

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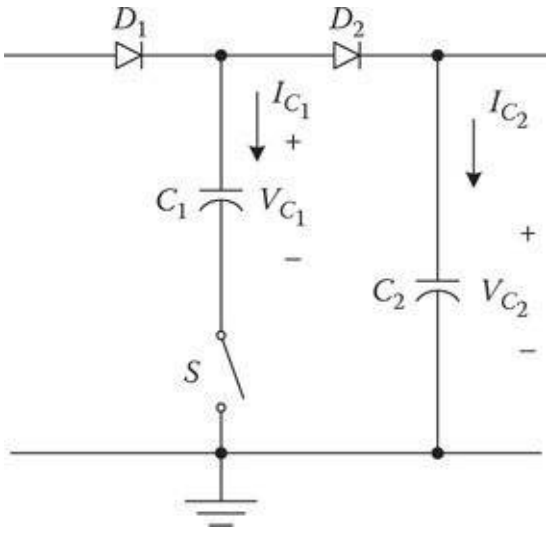


FIGURE 1.20
Double/enhanced circuit.

1.4.1.1 Fundamental Converters

Three types of fundamental DC/DC topologies were constructed: *buck* converter, *boost* converter, and *buck-boost* converter. They can be derived from single-quadrant operation choppers. For example, the buck converter was derived from A-type chopper. These converters have two main problems: linkage between input and output and very large output voltage ripple.

1.4.1.1.1 Buck Converter

Buck converter is a step-down DC/DC converter. It works in first-quadrant operation. It can be derived from quadrant I chopper. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 1.21. The output voltage is calculated by the formula

$$V_o = \frac{t_{on}}{T} V_{in} = kV_{in} \tag{1.8}$$

where

T is the repeating period, $T = 1/f$ (where f is the chopping frequency)

t_{on} is the switch-on time

k is the conduction duty cycle, $k = t_{on}/T$

1.4.1.1.2 Boost Converter

Boost converter is a step-up DC/DC converter. It works in second-quadrant operation. It can be derived from quadrant II chopper. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 1.22. The output voltage is calculated as

$$V_o = \frac{T}{T - t_{on}} V_{in} = \frac{1}{1-k} V_{in} \tag{1.9}$$

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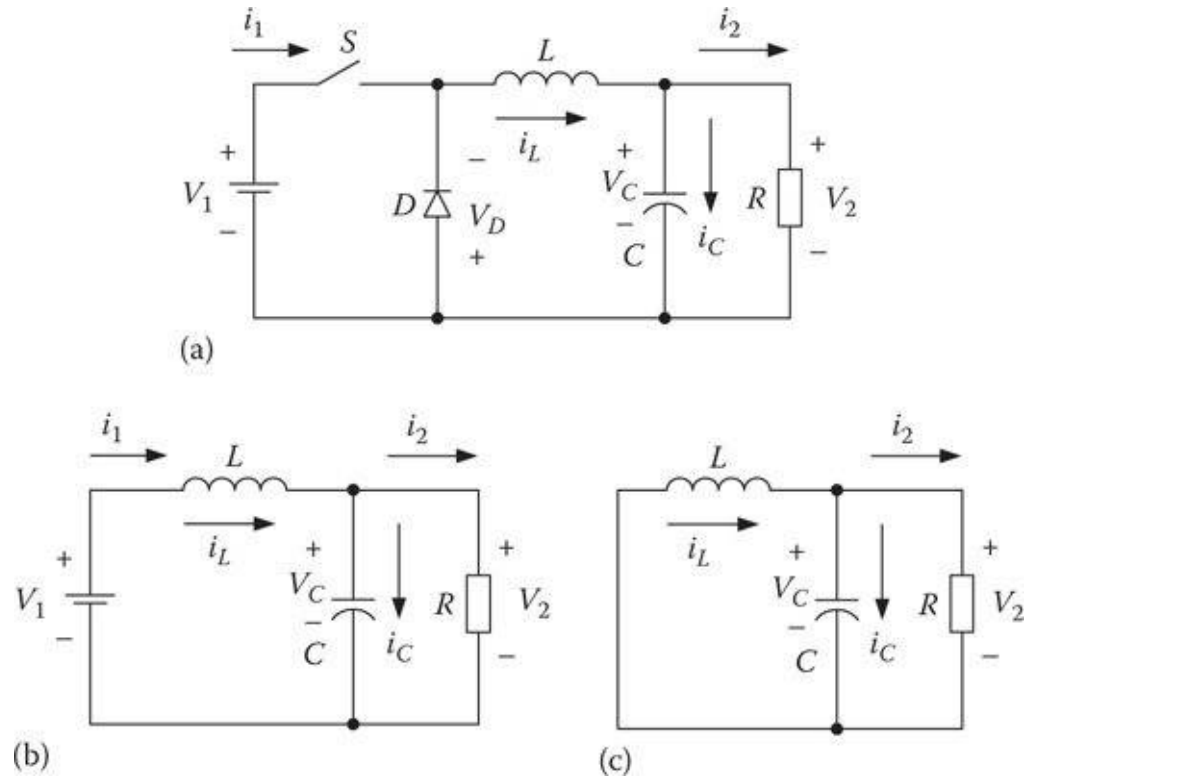


FIGURE 1.21
Buck converter: (a) circuit diagram; (b) switch-on; and (c) switch-off.

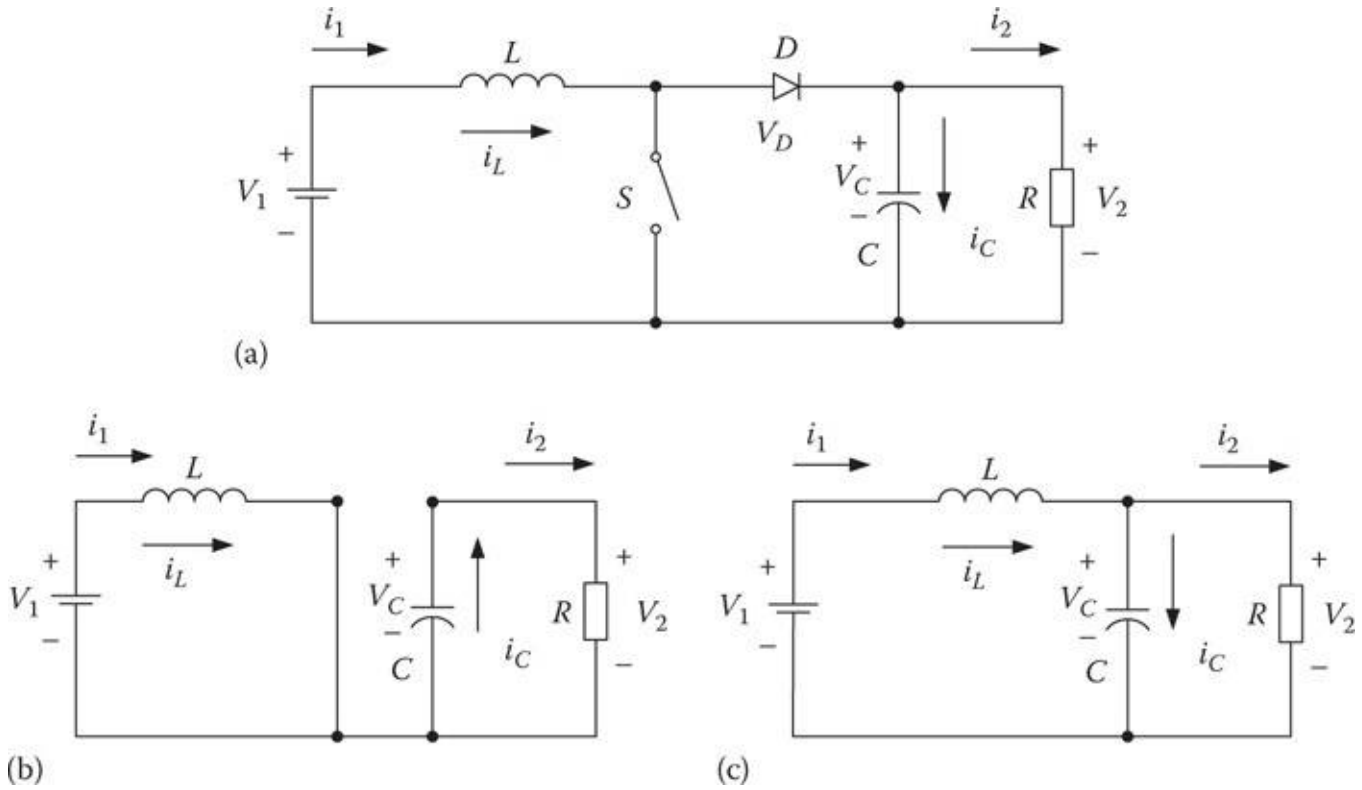


FIGURE 1.22
Boost converter: (a) circuit diagram; (b) switch-on; and (c) switch-off.

1.4.1.1.3 Buck-Boost Converter

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Buck-boost converter is a step-down/step-up DC/DC converter. It works in third-quadrant operation. Its circuit diagram, switch-on and switch-off equivalent circuits, and waveforms are shown in Figure 1.23. The output voltage is calculated by the formula

$$V_o = \frac{t_{on}}{T - t_{on}} V_{in} = \frac{k}{1-k} V_{in} \tag{1.10}$$

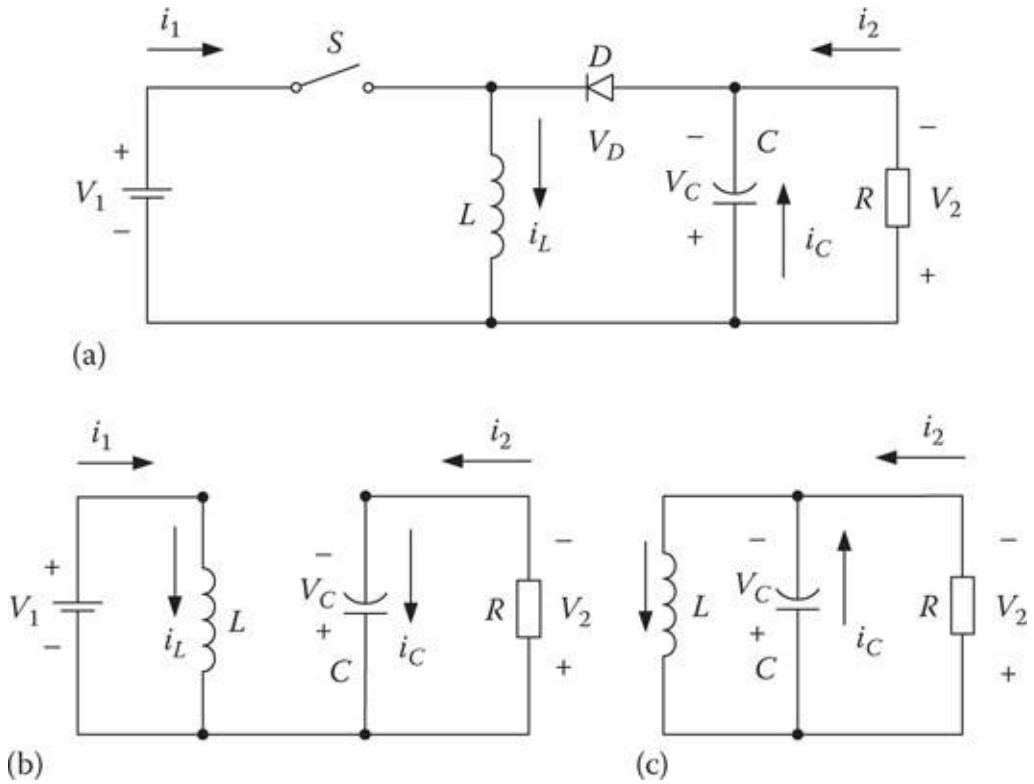


FIGURE 1.23
Buck-boost converter: (a) circuit diagram; (b) switch-on; and (c) switch-off.

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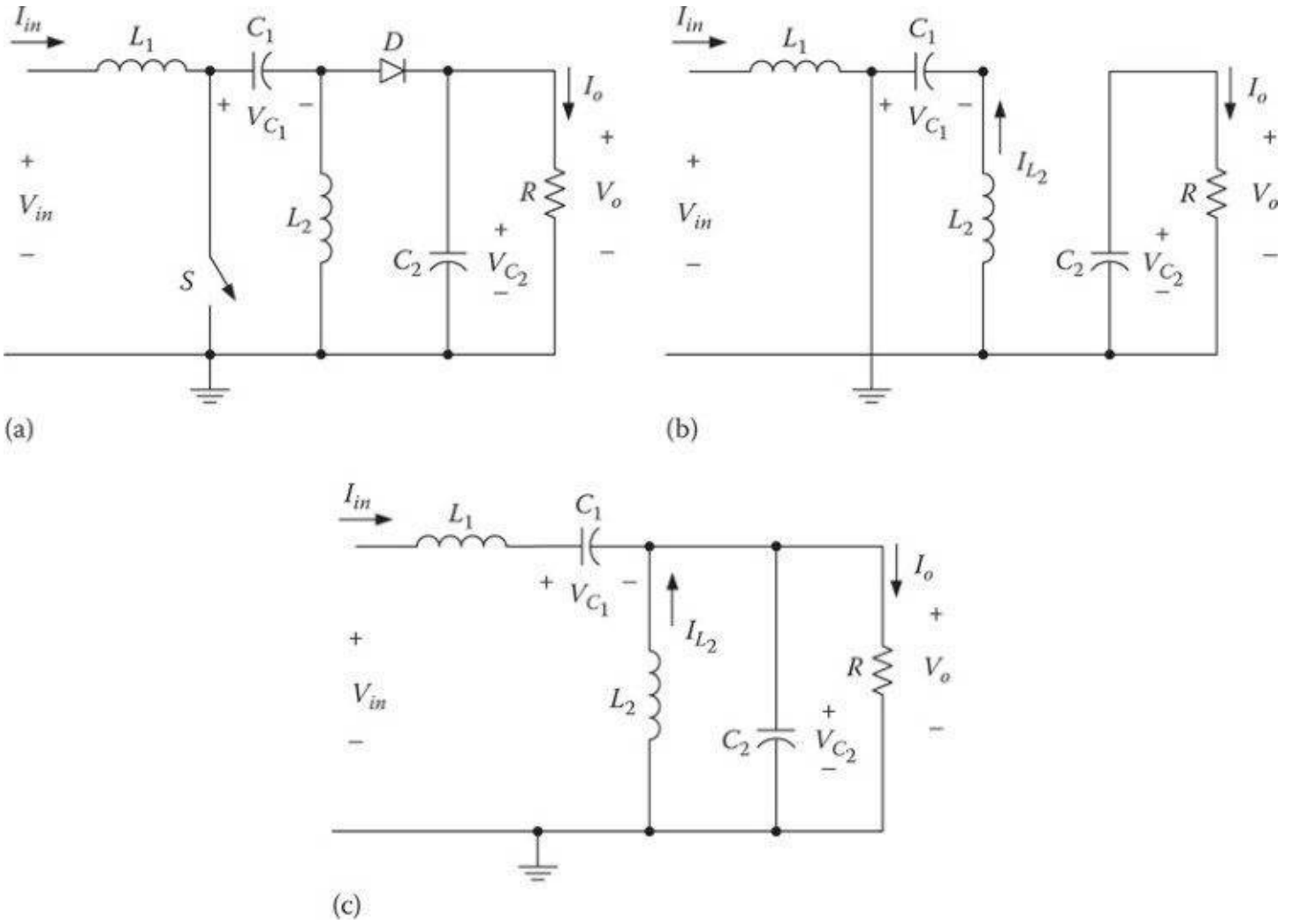


FIGURE 1.24
Positive buck-boost converter: (a) circuit diagram; (b) equivalent circuit in switch-on; and (c) equivalent circuit in switch-off.

1.4.1.1.4 Positive Buck-Boost Converter

The output voltage of the traditional buck-boost converter can be lower, equal to, or higher than the input voltage, but the output voltage polarity is negative. This is not suitable for some industrial applications. Therefore, positive buck-boost converter was invented. Its circuit is shown in Figure 1.24a. The equivalent circuit during the switching-on is shown in Figure 1.24b; the equivalent circuit during the switching-off is shown in Figure 1.24c. The output voltage is calculated by the formula

$$V_o = \frac{t_{on}}{T - t_{on}} V_{in} = \frac{k}{1-k} V_{in} \tag{1.11}$$

By using this converter, it is easy to obtain a random P/O voltage, higher or lower than, or equal to the input voltage. It provides great convenience for industrial applications.

1.4.1.1.5 Positive Buck-Boost Converter

In the meantime, a positive buck-boost converter was invented. It is another converter that can

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produce a P/O voltage, either lower or higher than the input voltage. Its circuit is shown in Figure 1.25a. If S_2 is open and D_2 conducted, the converter operates buck model; if S_1 is on and D_1 blocked, the converter operates boost model. The equivalent circuit during buck operation is shown in Figure 1.25b; the equivalent circuit during boost operation is shown in Figure 1.25c.

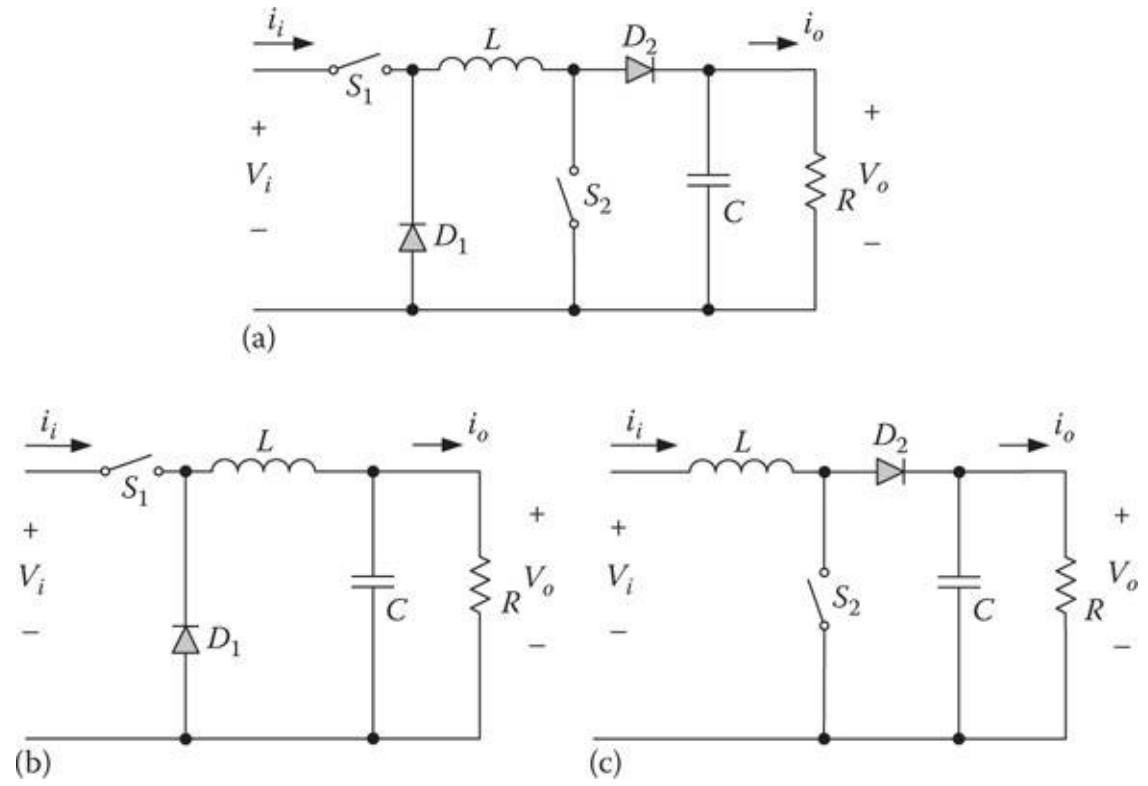


FIGURE 1.25
Positive buck and boost converter: (a) circuit diagram; (b) buck operation (S_2 open, D_2 conducted); and (c) boost operation (S_1 on, D_1 blocked).

1.4.1.2 Transformer-Type Converters

Since all fundamental DC/DC converters keep the linkage from the input side to the output side and the voltage transfer gain is comparably low, transformer-type converters were developed in the 1960s through the 1980s. These are a large number of converters such as *forward* converter, *push-pull* converter, *flyback* converter, *half-bridge* converter, *bridge* converter, and *Zeta* (or *ZETA*) converter. Usually, these converters have high transfer voltage gain and high insulation between both sides. Their gain usually depends on the transformer's turns ratio *N*, which can be thousands times.

1.4.1.2.1 Forward Converter

Forward converter is a transformer-type buck converter with the turns ratio *N*. It works in first-quadrant operation. Its circuit diagram is shown in Figure 1.26a. The output voltage is calculated by the formula

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$$V_o = kNV_{in} \tag{1.12}$$

In order to exploit the magnetic ability of the transformer iron core, a tertiary winding can be employed in the transformer. Its corresponding circuit diagram is shown in Figure 1.26b.

Some industrial applications require multiple outputs. This requirement is easily realized by constructing multiple secondary windings and the corresponding conversion circuit. For example, a forward converter with tertiary winding and three (3) outputs is shown in Figure 1.26c. The output voltage is calculated by the formula

$$V_o = kN_iV_{in} \tag{1.13}$$

where

N_i is the transformer turns ratio to the secondary winding, i = 1, 2, and 3, respectively

k is the conduction duty cycle, $k = t_{on}/T$

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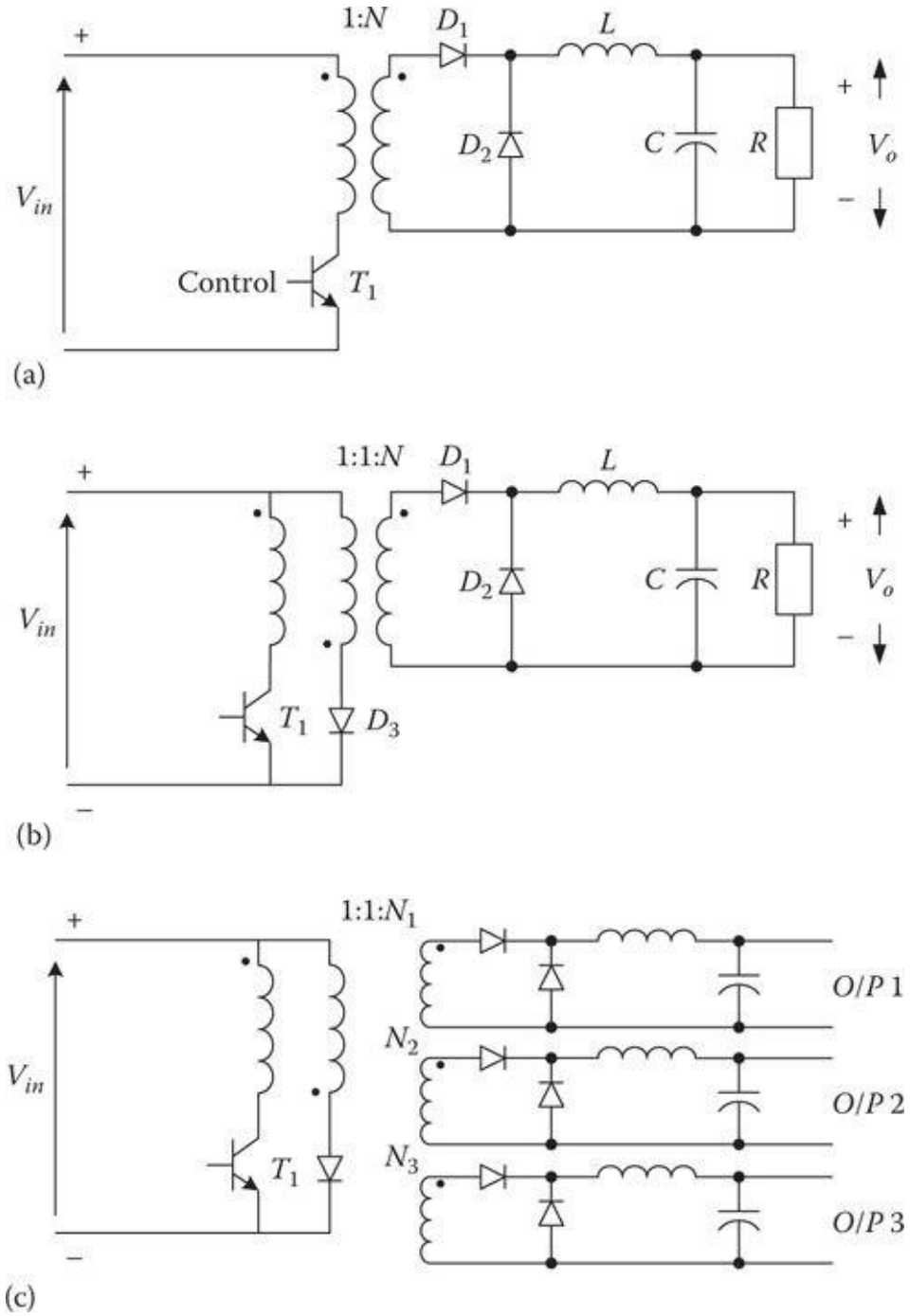


FIGURE 1.26
Forward converters: (a) fundamental circuit; (b) forward converter with tertiary winding; and (c) forward converter with tertiary winding and three outputs.

In principle, this structure is available for all transformer-type DC/DC converters for multiple output applications.

1.4.1.2.2 Push-Pull Converter

Boost converter works in a push-pull state, which effectively avoids the iron core saturation. Its circuit diagram is shown in Figure 1.27a. Since there are two switches working alternatively, the output voltage is doubled. The output voltage is calculated by the formula

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$$V_o = 2kNV_{in} \tag{1.14}$$

1.4.1.2.3 Flyback Converter

Flyback converter is a transformer-type converter using the demagnetizing effect. Its circuit diagram is shown in Figure 1.27b. The output voltage is calculated by the formula

$$V_o = \frac{k}{1-k} NV_{in} \tag{1.15}$$

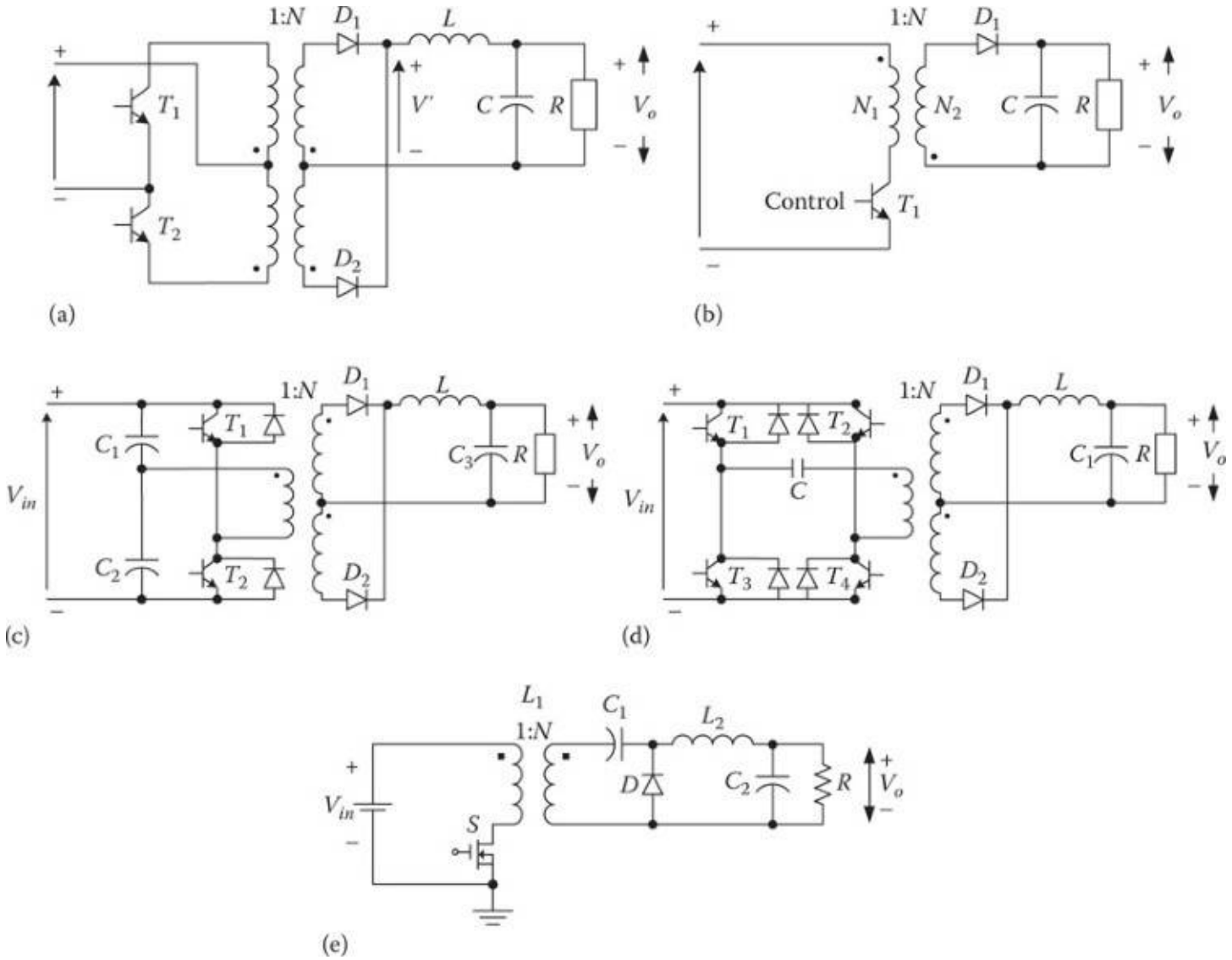


FIGURE 1.27
Other transformer-type converters: (a) push-pull converter; (b) flyback converter; (c) half-bridge converter; (d) bridge converter; and (e) ZETA converter.

1.4.1.2.4 Half-Bridge Converter

In order to reduce the primary side in one winding, half-bridge converter was constructed. Its circuit diagram is shown in Figure 1.27c. The output voltage is calculated by the formula

$$V_o = kNV_{in} \tag{1.16}$$

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1.4.1.2.5 Bridge Converter

Bridge converter employs more switches and therefore gains double-output voltage. Its circuit diagram is shown in Figure 1.27d. The output voltage is calculated by the formula

$$V_o = 2kNV_{in} \tag{1.17}$$

1.4.1.2.6 ZETA Converter

The ZETA converter is a transformer-type converter with a low-pass filter. Its output voltage ripple is small. Its circuit diagram is shown in Figure 1.27e. The output voltage is calculated by the formula

$$V_o = \frac{k}{1-k} NV_{in} \tag{1.18}$$

1.4.1.3 Developed Converters

Developed-type converters overcome the second fault of the fundamental DC/DC converters by adding a low-pass filter to reduce the output voltage ripple. The preliminary prototype was published in a conference in 1977. This conversion technique was very popular between 1970 and 1990. The typical converters are P/O *Luo*-converter, negative-output (N/O) *Luo*-converter, double-output (D/O) *Luo*-converter, Cúk converter, *SEPIC*, and Watkins-Johnson converter. The output voltage ripple of all developed-type converters is usually small and can be lower than 1%.

Developed converters can obtain a random output voltage, which can be higher or lower than the input voltage, and provide ease of application for industry. The output voltage transfer gain of all developed converters is

$$V_o = \frac{k}{1-k} V_{in} \tag{1.19}$$

1.4.1.3.1 P/O Luo-Converter

P/O Luo-converter is the elementary circuit of the series “P/O Luo-converters.” It can be derived from buck-boost converter. Its circuit diagram is shown in Figure 1.28a. The output voltage is calculated using formula (1.19).

1.4.1.3.2 N/O Luo-Converter

N/O Luo-converter is the elementary circuit of the series “N/O Luo-converters.” It can also be derived from buck-boost converter. Its circuit diagram is shown in Figure 1.28b. The output voltage is calculated using formula (1.19).

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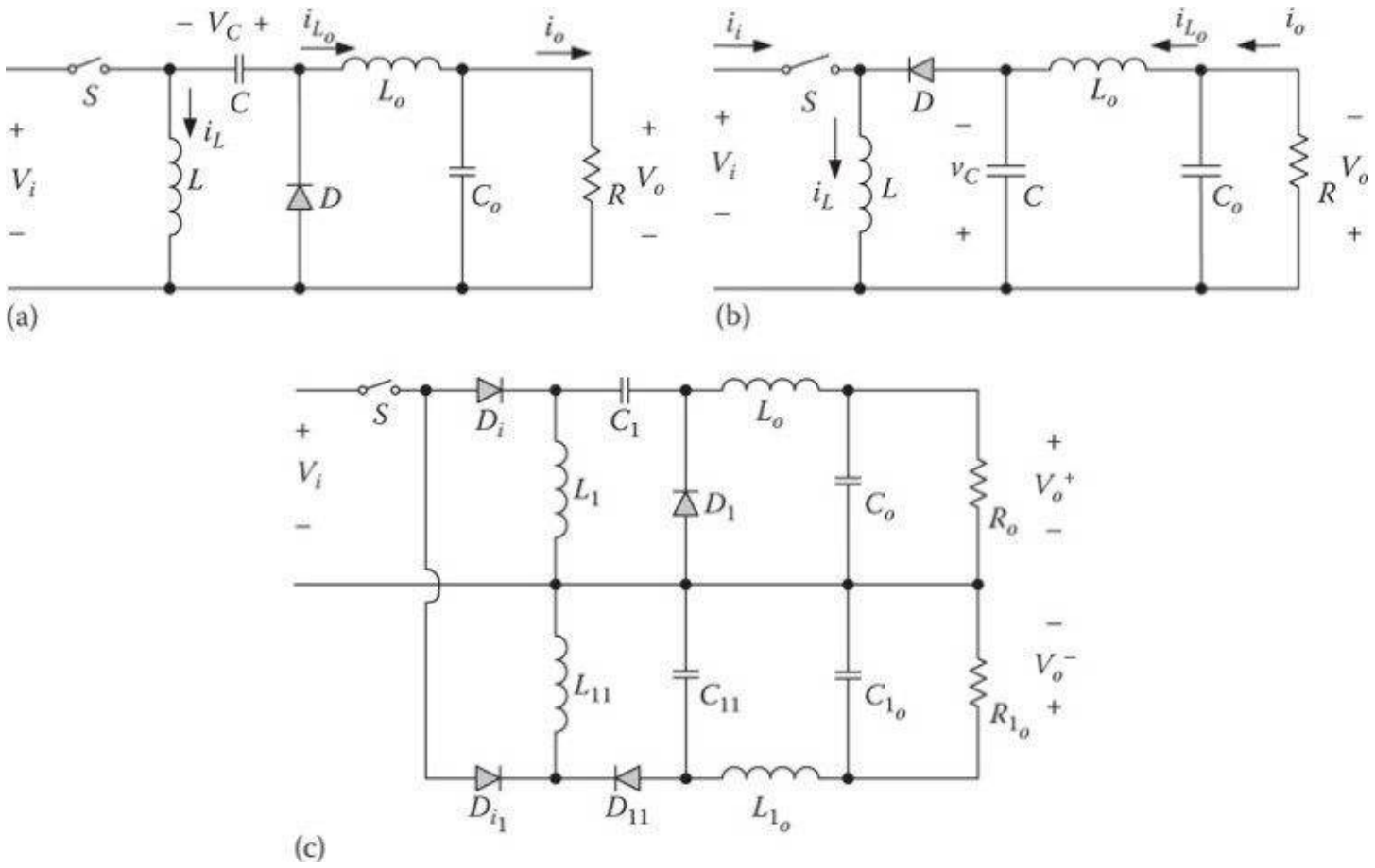


FIGURE 1.28
Luo-converters: (a) P/O Luo-converter; (b) N/O Luo-converter; and (c) D/O Luo-converter.

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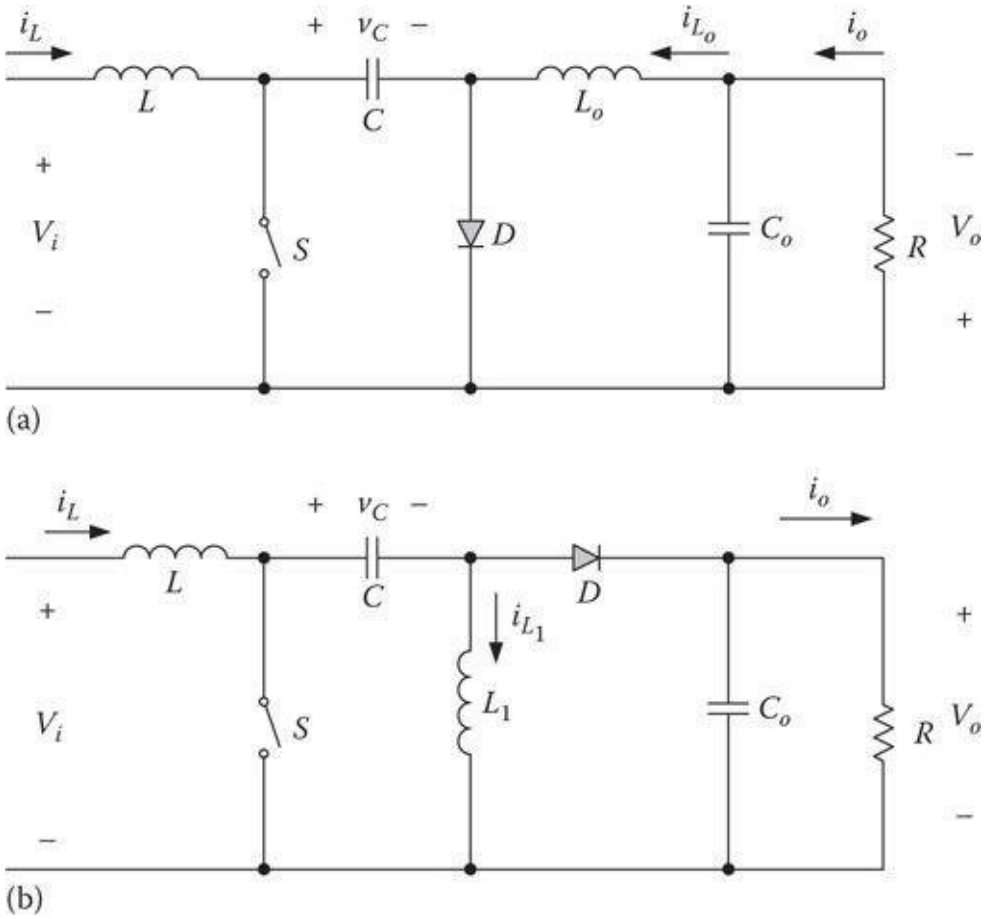


FIGURE 1.29
Other developed converters: (a) Cúk converter and (b) SEPIC.

1.4.1.3.3 D/O Luo-Converter

In order to obtain mirror symmetrical P/O and N/O voltage, D/O Luo-converter was constructed. D/O Luo-converter is the elementary circuit of the series "D/O Luo-converters." Its circuit diagram is shown in Figure 1.28c. The output voltage is calculated using formula (1.19).

1.4.1.3.4 Cúk Converter

Cúk converter is derived from boost converter. Its circuit diagram is shown in Figure 1.29a. The output voltage is calculated using formula (1.19).

1.4.1.3.5 SEPIC

The *SEPIC* is derived from boost converter. Its circuit diagram is shown in Figure 1.29b. The output voltage is calculated using formula (1.19).

1.4.1.3.6 Tapped Inductor Converter

These converters have been derived from fundamental converters. The circuit diagrams are shown in Table 1.2. The voltage transfer gains are shown in Table 1.3. Here, the tapped inductor ratio is $n = n_1/(n_1 + n_2)$.

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TABLE 1.2
Circuit Diagrams of the Tapped Inductor Fundamental Converters

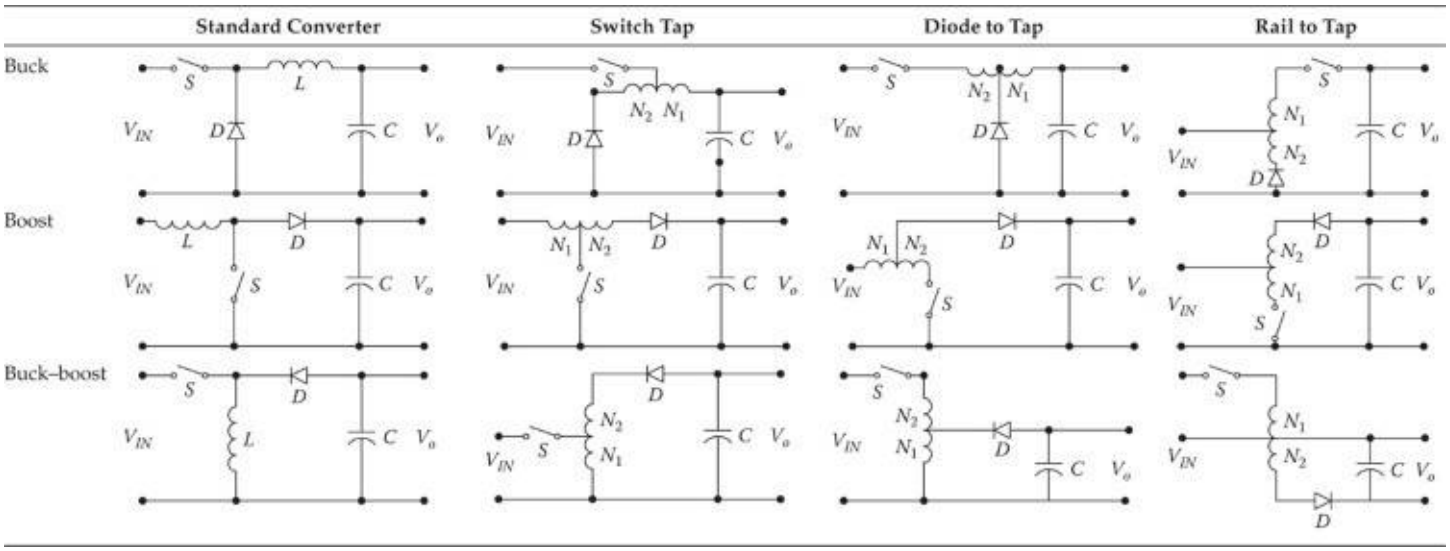


TABLE 1.3
Voltage Transfer Gains of the Tapped Inductor Fundamental Converters

Converter	No Tap	Switched to Tap	Diode to Tap	Rail to Tap
Buck	k	$\frac{k}{n+k(1-n)}$	$\frac{nk}{1+k(n-1)}$	$\frac{k-n}{k(1-n)}$
Boost	$\frac{1}{1-k}$	$\frac{n+k(1-n)}{n(1-k)}$	$\frac{1+k(n-1)}{1-k}$	$\frac{n-k}{n(1-k)}$
Buck–boost	$\frac{k}{1-k}$	$\frac{k}{n(1-k)}$	$\frac{nk}{1-k}$	$\frac{k}{1-k}$

1.4.1.4 VL Converters

VL technique is a good method to lift the output voltage and is widely applied in electronic circuit design. After long-term industrial application and research, this method had been successfully used in DC/DC conversion technique. Using this method, the output voltage can be easily lifted by tens to hundreds times. VL converters can be classed into self-lift, *re-lift*, *triple-lift*, *quadruple-lift*, and *high-stage-lift* converters. The main contributors in this area are the authors of this book. These circuits will be introduced in Chapter 2 in detail.

1.4.1.5 SL Converters

VL technique is a popular method that is widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years and has opened a way to design high-voltage-gain converters. Three-series Luo-converters are examples of VL technique implementations. However, the output voltage increases stage by stage just along the arithmetic progression. A novel approach—SL technique—has been developed, which

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implements the output voltage increasing stage by stage along in geometric progression. It effectively enhances the voltage transfer gain in power law. The typical circuits are sorted into five series: P/O *SL Luo-converters*, N/O *SL Luo-converters*, P/O *cascaded boost converters*, N/O *cascaded boost converters*, and *ultra-lift Luo-converter*. These circuits will be introduced in Chapters 3, 4, 5, 6 and 7 in detail.

1.4.2 Second-Generation Converters

The second-generation converters are called multiple-quadrant operation converters. These converters perform in two-quadrant operation and four-quadrant operation with medium output power range (hundreds of watts or higher). The topologies can be sorted into two main categories: first are the converters derived from the multiple-quadrant choppers and/or from the first-generation converters and second are constructed with transformers. Usually, one-quadrant operation requires at least one switch. Therefore, a two-quadrant operation converter has at least two switches, and a four-quadrant operation converter has at least four switches. Multiple-quadrant choppers were employed in industrial applications for a long time. They can be used to implement the DC motor multiple-quadrant operation. As the chopper titles indicate, there are class-A converters (one-quadrant operation), class-B converters (two-quadrant operation), class-C converters, class-D converters, and class-E (four-quadrant operation) converters. These converters are derived from multiquadrant choppers, for example, class-B converters are derived from B-type choppers and class-E converters are derived from E-type choppers. The class-A converter works in quadrant I, which corresponds to the forward-motoring operation of a DC motor drive. The class-B converter works in quadrant I and II operation, which corresponds to the forward-running motoring and regenerative braking operation of a DC motor drive. The class-C converter works in quadrant I and VI operation. The class-D converter works in quadrant III and VI operation, which corresponds to the reverse-running motoring and regenerative braking operation of a DC motor drive. The class-E converter works in four-quadrant operation, which corresponds to the four-quadrant operation of a DC motor drive. In recent years, many papers have investigated the class-E converters for industrial applications. Multiquadrant operation converters can be derived from the first-generation converters. For example, multiquadrant Luo-converters are derived from P/O Luo-converters and N/O Luo-converters. These circuits will be introduced in Chapter 10 in detail. The transformer-type multiquadrant converters easily change the current direction by transformer polarity and diode rectifier. The main types of such converters can be derived from the *forward* converter, *half-bridge* converter, and *bridge* converter.

1.4.3 Third-Generation Converters

The third-generation converters are called switched-component converters and are made of either inductors or capacitors, the so-called switched inductor and switched capacitors. They can perform in two- or four-quadrant operation with high output power range (thousands of watts). Since they are made of only inductors or capacitors, they are small. Consequently, the power density and efficiency are high.

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1.4.3.1 Switched-Capacitor Converters

Switched-capacitor DC/DC converters consist of only capacitors. Because there is no inductor in the circuit, their size is small. They have outstanding advantages such as low power losses and low electromagnetic interference. Since their electromagnetic radiation is low, switched-capacitor DC/DC converters are required in certain equipment. The switched capacitor can be integrated into an integrated chip (IC). Hence, its size is largely reduced. Much attention has been drawn to the switched-capacitor converter since its development. Many papers have been published discussing its characteristics and advantages. However, most of the converters in the literature perform a single-quadrant operation. Some of them work in the push-pull status. In addition, their control circuit and topologies are very complex, especially for the large difference between input and output voltages. These circuits will be introduced in Chapter 11 in detail.

1.4.3.2 Multiple-Quadrant Switched-Capacitor Luo-Converters

Switched-capacitor DC/DC converters consist of only capacitors. Since their power density is very high, they are widely applied in industrial applications. Some industrial applications require multiple-quadrant operation, so multiple-quadrant switched-capacitor Luo-converters have been developed. There are two-quadrant operation types and four-quadrant operation types discussed in detail.

1.4.3.3 Multiple-Lift Push-Pull Switched-Capacitor Converters

VL technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent years and has opened a way to design high-voltage-gain converters. Three-series Luo-converters are examples of VL technique implementation. However, the output voltage increases stage by stage just along the arithmetic progression. A novel approach—multiple-lift push-pull technique—has been developed, which implements the output voltage, which increases stage by stage along the arithmetic progression. It effectively enhances the voltage transfer gain. The typical circuits are sorted into two series: *P/O multiple-lift push-pull switched-capacitor Luo-converters* and *N/O multiple-lift push-pull switched-capacitor Luo-converters*. These circuits will be introduced in Chapters 9 and 13 in detail.

1.4.3.4 Switched-Inductor Converters

The switched capacitors have many advantages, but their circuits are not simple. If the difference of input and output voltages is large, many capacitors are required. The switched inductor has the outstanding advantage that only one inductor is required for one switched-inductor converter no matter how large the difference between input and output voltages is. This characteristic is very important for large power conversion. At the present time, large power conversion equipment is close to using switched-inductor converters. For example, the MIT DC/DC converter designed by Prof. John G. Kassakian for his new system in the 2005 automobiles is a two-quadrant switched-inductor DC/DC converter. These circuits will be introduced in Chapter 11 in detail.

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1.4.4 Fourth-Generation Converters

The fourth-generation DC/DC converters are called soft-switching converters. There are four types of soft-switching methods:

1. Resonant-switch converters
2. Load-resonant converters
3. Resonant-DC-link converters
4. High-frequency-link integral-half-cycle converters

Until now attention has been paid only to the resonant-switch conversion method. This resonance method is available for working independently to load. There are three main categories: ZCS, ZVS, and ZT converters. Most topologies usually perform in single-quadrant operation in the literature. Actually, these converters can perform in two- and four-quadrant operation with high output power range (thousands of watts). When the transferred power becomes large, the power losses increase largely. Main power losses are produced during the switch-on and switch-off period. How to reduce the power losses across the switch is the clue to increasing the power transfer efficiency. Soft-switching technique successfully solved this problem. Professor Fred Lee is the pioneer of the soft-switching technique. He established a research center and manufacturing base to realize the ZCS and ZVS DC/DC converters. His first paper introduced his research in 1984. ZCS and ZVS converters have three resonant states: over resonance (completed resonance), optimum resonance (critical resonance), and quasi-resonance (subresonance). Only the quasi-resonance state has two clear zero-cross points in a repeating period. Many papers after 1984 have been published that develop the ZCS quasi-resonant converters (QRCs) and ZVS-QRCs.

1.4.4.1 ZCS-QRCs

ZCS-QRC equips resonant circuit in the switch side to keep the switch-on and switch-off at zero-current condition. There are two states: full-wave state and half-wave state. Most of the engineers enjoy the half-wave state. This technique has half-wave current resonance waveform with two zero-cross points.

1.4.4.2 ZVS-QRCs

ZVS-QRC equips resonant circuit in the switch side to keep the switch-on and switch-off at zero-voltage condition. There are two states: full-wave state and half-wave state. Most of the engineers enjoy the half-wave state. This technique has half-wave voltage resonance waveform with two zero-cross points.

1.4.4.3 ZT Converters

Using ZCS-QRC and ZVS-QRC largely reduces the power losses across the switches. Consequently, the switch device power rates become lower and converter power efficiency is increased. However, ZCS-QRC and ZVS-QRC have large current and voltage stresses. Therefore, the device's current and voltage peak rates usually are three to five times higher

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than the working current and voltage. It is not only costly but also ineffective. ZT technique overcomes this fault. It implements zero-voltage plus ZCS technique without significant current and voltage stresses. These circuits will be introduced in Chapter 14 in detail.

1.4.5 Fifth-Generation Converters

The fifth-generation converters are called SR DC/DC converters. This type of converter was required by the development of computing technology. Corresponding to the development of the micropower consumption technique and high-density IC manufacture, the power supplies with low output voltage and strong current are widely used in communications, computer equipment, and other industrial applications. Intel, which developed the Zelog-type computers, governed the world market for a long time. Inter-80 computers used the 5 V power supply. In order to increase the memory size and operation speed, large-scale integrated chip technique has been quickly developed. As the amount of IC manufacturing increased, the gaps between the layers became narrower. At the same time, the micropower consumption technique was completed. Therefore, new computers, such as those using Pentium I, II, III, and IV, use a 3.3 V power supply. Future computers will have larger memory and will require lower power supply voltages, for example, 2.5, 1.8, 1.5, and even 1.1 V. Such low power supply voltage cannot be obtained by the traditional diode rectifier bridge because the diode voltage drop is too large. Because of this requirement, new types of MOSFET were developed. They have very low conduction resistance (6–8 mΩ) and forward voltage drop (0.05−0.2 V). Many papers have been published since 1990, and many prototypes have been developed. The fundamental topology is derived from the forward converter. Active-clamped circuit, flat transformers, double-current circuit, soft-switching methods, and multiple-current methods can be used in SR DC/DC converters. These circuits will be introduced in Chapter 15 in detail.

1.4.6 Sixth-Generation Converters

The sixth-generation converters are called MER converters. Current source resonant inverters are the heart of many systems and equipment, for example, uninterruptible power supply and high-frequency annealing apparatus. Many topologies shown in the literature are the series resonant converters and parallel resonant converters that consist of two or three or four energy-storage elements. However, they have limitations. These limitations of two-, three-, and/or four-element resonant topologies can be overcome by special design. These converters have been categorized into three main types:

- Two-energy-storage-element resonant DC/AC and DC/AC/DC converters
- Three-energy-storage-element resonant DC/AC and DC/AC/DC converters
- Four-energy-storage-element (2L-2C) resonant DC/AC and DC/AC/DC converters

By mathematical calculation, there are *8* prototypes of two-element converters, *38* prototypes of three-element converters, and *98* prototypes of four-element (2L-2C) converters. With the careful analysis of these prototypes, we can find out that not many circuits can be realized. If we keep the output in low-pass bandwidth, the series components must be inductors and shunt components be capacitors. Through further analysis, the first component of the resonant-filter

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network can be an inductor in series or a capacitor in shunt. In the first case, only alternative (square wave) voltage source can be applied to the network. In the second case, only alternative (square wave) current source can be applied to the network. These circuits will be introduced in Chapters 16, 17, 18 and 19 in detail.

1.5 Categorizing Prototypes and DC/DC Converter Family Tree

There are more than 800 topologies of DC/DC converters existing. It is urgently necessary to categorize all prototypes. From accumulated knowledge, we can build a DC/DC converter family tree, which is shown in Figure 1.30. In each generation of the family tree, we introduce some circuits to readers to promote the understanding of the characteristics.

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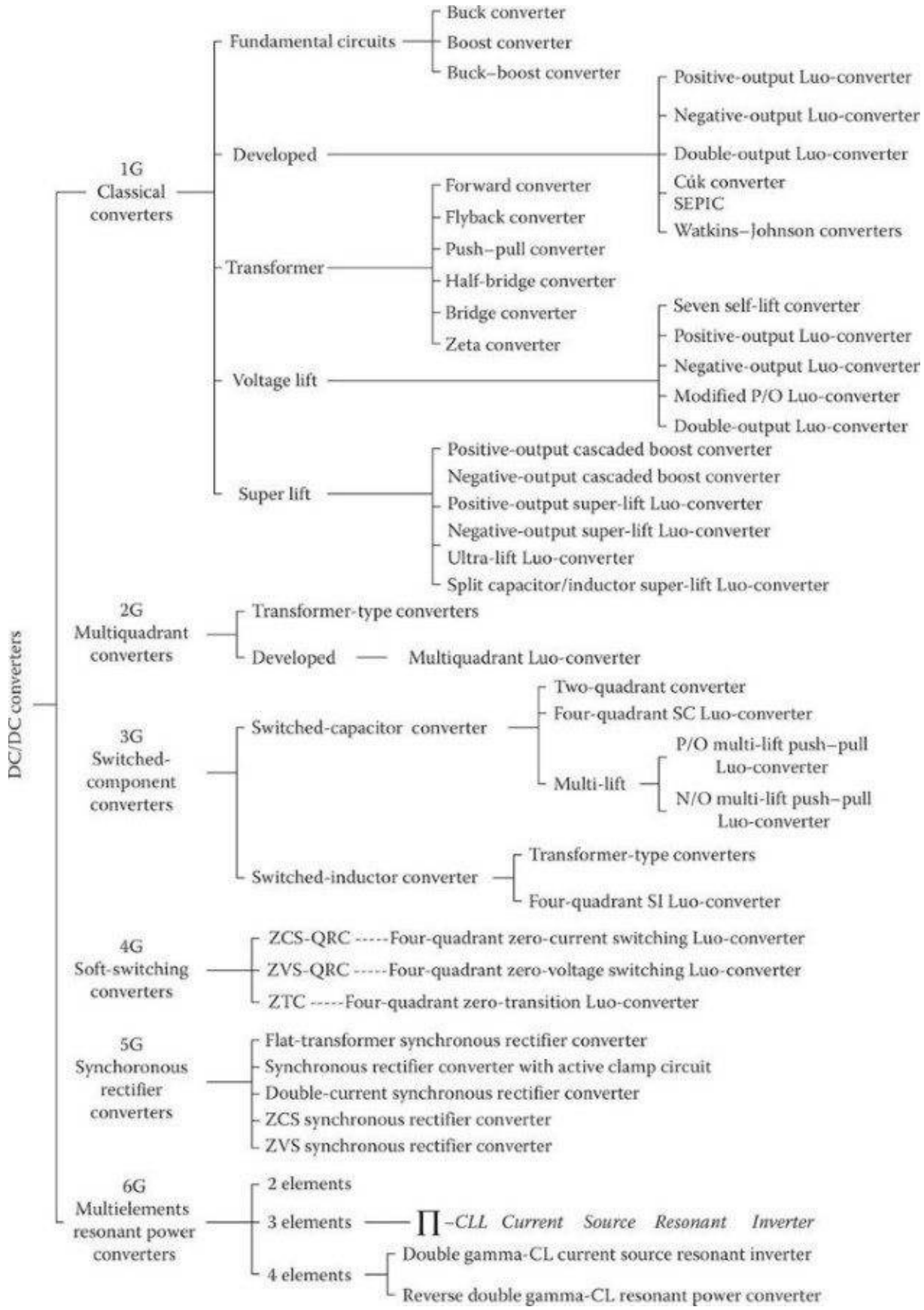


FIGURE 1.30
DC/DC converter family tree.

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Voltage-Lift Converters

The voltage-lift (VL) technique is a popular method that is widely applied in electronic circuit design. This technique effectively overcomes the effects of parasitic elements and greatly increases the output voltage transfer gains. Therefore, DC/DC converters using VL technique can convert the source voltage into a higher output voltage with high power efficiency and high power density and with a simple structure.

2.1 Introduction

The voltage-lift (VL) technique is applied in the periodical switching circuit. Usually, a capacitor is charged during switch-on by certain voltages, for example, source voltage. This charged capacitor voltage can be arranged on top-up to some parameter, for example, output voltage during switch-off. Therefore, the output voltage can be lifted higher. Consequently, this circuit is called a self-lift circuit. A typical example is the sawtooth- wave generator with self-lift circuit.

Repeating this operation, another capacitor can be charged by a certain voltage, which may possibly be the input voltage or other equivalent voltage. The second capacitor charged voltage is also possibly arranged on top-up to some parameter, especially output voltage. Therefore, the output voltage can be higher than that of the self-lift circuit. As usual, this circuit is called re-lift circuit.

Analogously, this operation can be repeated many times. Consequently, the series circuits are called triple-lift circuit, quadruple-lift circuit, and so on.

Because of the effect of parasitic elements, the output voltage and power transfer efficiency of DC/DC converters are limited. The VL technique opens a good way to improve circuit characteristics. After long-term research, this technique has been successfully applied to DC/DC converters by the authors of the book. Three-series Luo-converters are the new DC/DC converters developed using VL technique. These converters perform DC/DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure. They are different from any other DC/DC step-up converters and possess many advantages including a high output voltage with small ripples. Therefore, these converters are widely used in computer peripheral equipment and industrial applications, especially for high-output-voltage projects. The contents of this chapter are arranged as follows:

1. Seven types of self-lift converters
2. Positive-output (P/O) Luo-converters
3. Negative-output (N/O) Luo-converters
4. Modified P/O Luo-converters
5. Double-output Luo-converters

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2.2 Seven Self-Lift Converters

The seven types of self-lift converters are

- Self-lift Cúk converter
- Self-lift P/O Luo-converter
- Reverse self-lift P/O Luo-converter
- Self-lift N/O Luo-converter
- Reverse self-lift Luo-converter
- Self-lift single-ended primary inductance converter (SEPIC)
- Enhanced self-lift P/O Luo-converter

The first six self-lift converters are derived from developed converters such as Luo-converters, Cúk converter, and SEPIC in Section 1.3. The seventh converter *enhanced self-lift P/O Luo-converters* is a completely new design. These converters perform DC/DC voltage increasing conversion in simple structures. Usually, only one more capacitor and diode are added for the output voltage to be higher than an input voltage. The output voltage is calculated by the formula

$$V_o = \left(\frac{k}{1-k} + 1\right) V_{in} = \frac{1}{1-k} V_{in} \tag{2.1}$$

In these circuits, the switch S is a semiconductor device (MOSFET, BJT, IGBT, and so on). It is driven by a pulse-width-modulated (PWM) switching signal with variable frequency f and conduction duty k. For all circuits, the load is usually resistive, that is, $R = V_o/I_o$

The normalized load is

$$z_N = \frac{R}{fL_{eq}} \tag{2.2}$$

where L_{eq} is the equivalent inductance.

We concentrate on the absolute values rather than on the polarity in the following description and calculations. The directions of all voltages and currents are defined and shown in the corresponding figures. We also assume that the semiconductor switch and the passive components are all ideal. All capacitors are assumed to be large enough that the ripple voltage across the capacitors can be negligible in one switching cycle for the average value discussions.

For any component X (e.g., C, L), its instantaneous current and voltage are expressed as i_X and υ_X; its average current and voltage values are expressed as I_x and V_x. The input voltage and current are V_o and I_o; the output voltage and current are V_i and I_i. T and f are the switching period and frequency, respectively.

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The voltage transfer gain for the CCM is

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o} \tag{2.3}$$

The variation of the current i_L is

$$\zeta_1 = \frac{\Delta i_L/2}{I_L} \tag{2.4}$$

The variation of the current i_{L_o} is

$$\zeta_2 = \frac{\Delta i_{L_o}/2}{I_{L_o}} \tag{2.5}$$

The variation of the current i_D is

$$\xi = \frac{\Delta i_D/2}{I_D} \tag{2.6}$$

The variation of the voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} \tag{2.7}$$

The variation of the voltage v_{C_1} is

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{v_{C_1}} \tag{2.8}$$

The variation of the voltage v_{C_2} is

$$\sigma_2 = \frac{\Delta v_{C_2}/2}{v_{C_2}} \tag{2.9}$$

The variation of the output voltage v_o is

$$\varepsilon = \frac{\Delta V_o/2}{V_o} \tag{2.10}$$

Here, I_D refers to the average current i_D that flows through the diode D during the switch-off period, not its average current over the whole period.

Detailed analysis of the seven self-lift DC/DC converters will be given in the following sections. Due to the length limit of this book, only the simulation and experimental results of the self-lift Cúk converter are given. However, the results and conclusions of other self-lift converters are similar to those of the self-lift Cúk converter.

2.2.1 Self-Lift Cúk Converter

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The self-lift Cúk converter and its equivalent circuits during switch-on and switch-off period are shown in Figure 2.1. It is derived from the Cúk converter. During switch-on period, S and D_1 are on, and D is off. During switch-off period, D is on, and S and D_1 are off.

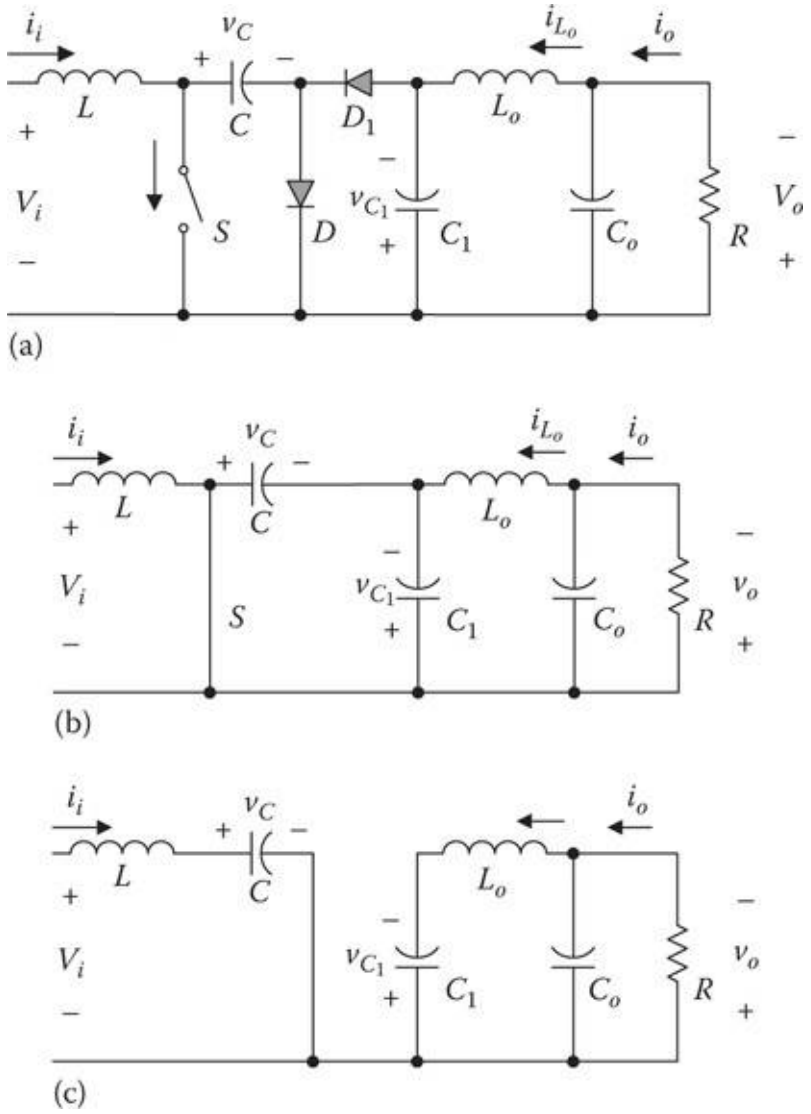


FIGURE 2.1
Self-lift Cúk converter and equivalent circuits. (a) The self-lift Cúk converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

2.2.1.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus,

$$V_{C_1} = V_{C_o} = V_o \tag{2.11}$$

During switch-on period, the voltage across capacitors C and C_1 are equal. Since we assume that C and C_1 are sufficiently large,

$$V_C = V_{C_1} = V_o \tag{2.12}$$

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The inductor current i_L increases during switch-on and decreases during switch-off. The corresponding voltages across L are V_i and $-(V_C - V_i)$.

Therefore,

$$kTV_i = (1-k)T(V_C - V_i)$$

Hence,

$$V_o = V_C = V_{C_1} = V_{C_o} = \frac{1}{1-k}V \tag{2.13}$$

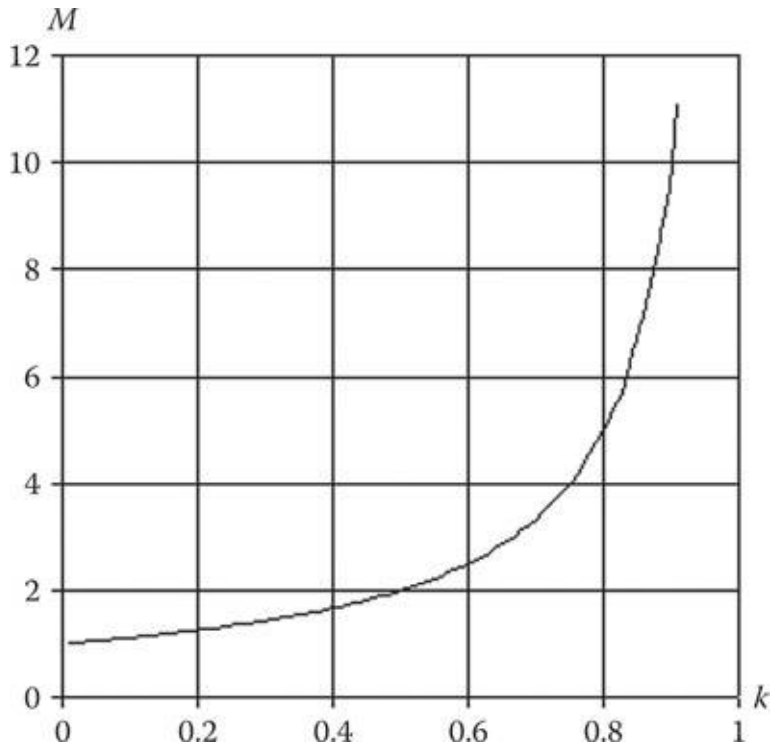


FIGURE 2.2
Voltage transfer gain M versus k.

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{1}{1-k} \tag{2.14}$$

The characteristics of M versus conduction duty cycle k are shown in Figure 2.2.

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

Thus,

$$I_L = I_i = \frac{1}{1-k}I_o$$

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During switch-off,

$$i_D = i_L \quad I_D = \frac{1}{1-k} I_o \tag{2.15}$$

The capacitor C_o acts as a low-pass filter so that

$$I_{L_o} = I_o$$

The current i_L increases during switch-on. The voltage across it during switch-on is V_i; therefore, its peak-to-peak current variation is

$$\Delta i_L = \frac{kTV_i}{L}$$

The variation ratio of the current i_L is

$$\zeta_1 = \frac{\Delta i_L/2}{I_L} = \frac{kTV_i}{2I_L} = \frac{k(1-k)^2 R}{2fL} = \frac{kR}{2M^2 fL} \tag{2.16}$$

The variation of current i_D is

$$\xi = \zeta_1 = \frac{kR}{2M^2 fL} \tag{2.17}$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{I_L(1-k)T}{C} = \frac{I_o}{fC} \tag{2.18}$$

The variation ratio of the voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{I_o}{2fCV_o} = \frac{1}{2fRC} \tag{2.19}$$

The peak-to-peak variation of the voltage v_{C_1} is

$$\Delta v_{C_1} = \frac{I_{L_o}(1-k)T}{C_1} = \frac{I_o(1-k)}{fC_1} \tag{2.20}$$

The variation ratio of the voltage v_{C_1} is

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{I_o(1-k)}{2fC_1V_o} = \frac{1}{2MfRC_1} \tag{2.21}$$

The peak-to-peak variation of the current i_{L_o} is approximately

$$\Delta i_{L_o} = \frac{\frac{1}{2}\frac{\Delta v_{C_1}}{2}\frac{T}{2}}{L_o} = \frac{I_o(1-k)}{8f^2 L_o C_1} \tag{2.22}$$

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The variation ratio of the current i_{L_o} is approximately:

$$\zeta_2 = \frac{\Delta i_{L_o}/2}{I_{L_o}} = \frac{I_o(1-k)}{16f^2L_oC_1I_o} = \frac{1}{16Mf^2L_oC_1} \tag{2.23}$$

The peak-to-peak variation of voltage v_o and v_{C_o} is

$$\Delta v_o = \Delta v_{C_o} = \frac{\frac{1}{2}\frac{\Delta i_{L_o}}{2}\frac{T}{2}}{C_o} = \frac{I_o(1-k)}{64f^3L_oC_1C_o} \tag{2.24}$$

The variation ratio of the output voltage is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{I_o(1-k)}{128f^3L_oC_1C_oV_o} = \frac{1}{128Mf^3L_oC_1C_oR} \tag{2.25}$$

The voltage transfer gain of the self-lift Cúk converter is the same as the original boost converter. However, the output current of the self-lift Cúk converter is continuous with small ripple.

The output voltage of the self-lift Cúk converter is higher than the corresponding Cúk converter by an input voltage. It retains one of the merits of the Cúk converter, the smooth output voltage. They both have continuous input and output current in CCM. As for component stress, it can be seen that the self-lift converter has a smaller voltage and current stresses than the original Cúk converter.

2.2.1.2 Discontinuous Conduction Mode

The self-lift Cúk converter operates in the DCM if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at t = T, then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2}\frac{R}{M^2fL} = 1 \tag{2.26}$$

Therefore, the boundary between CCM and DCM is

$$M_B = \sqrt{k}\sqrt{\frac{R}{2fL}} = \sqrt{\frac{kz_N}{2}} \tag{2.27}$$

where z_N is the normalized load $R/(fL)$.

The boundary between CCM and DCM is shown in Figure 2.3a. The curve that describes the relationship between M_B and z_N has the minimum value M_B = 1.5 and k = 1/3 when the normalized load z_N is 13.5.

When $M > M_B$, the circuit operates in the DCM. In this case, the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $kT < t_1 < T$ and $0 < m < 1$.

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Define *m* as the current filling factor (FF). After mathematical manipulation

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2f_L}} \tag{2.28}$$

From this equation, we can see that the DCM is caused by the following factors:

- The switching frequency f is too low.
- The duty cycle k is too small.
- The inductance L is too small.
- The load resistor R is too big.

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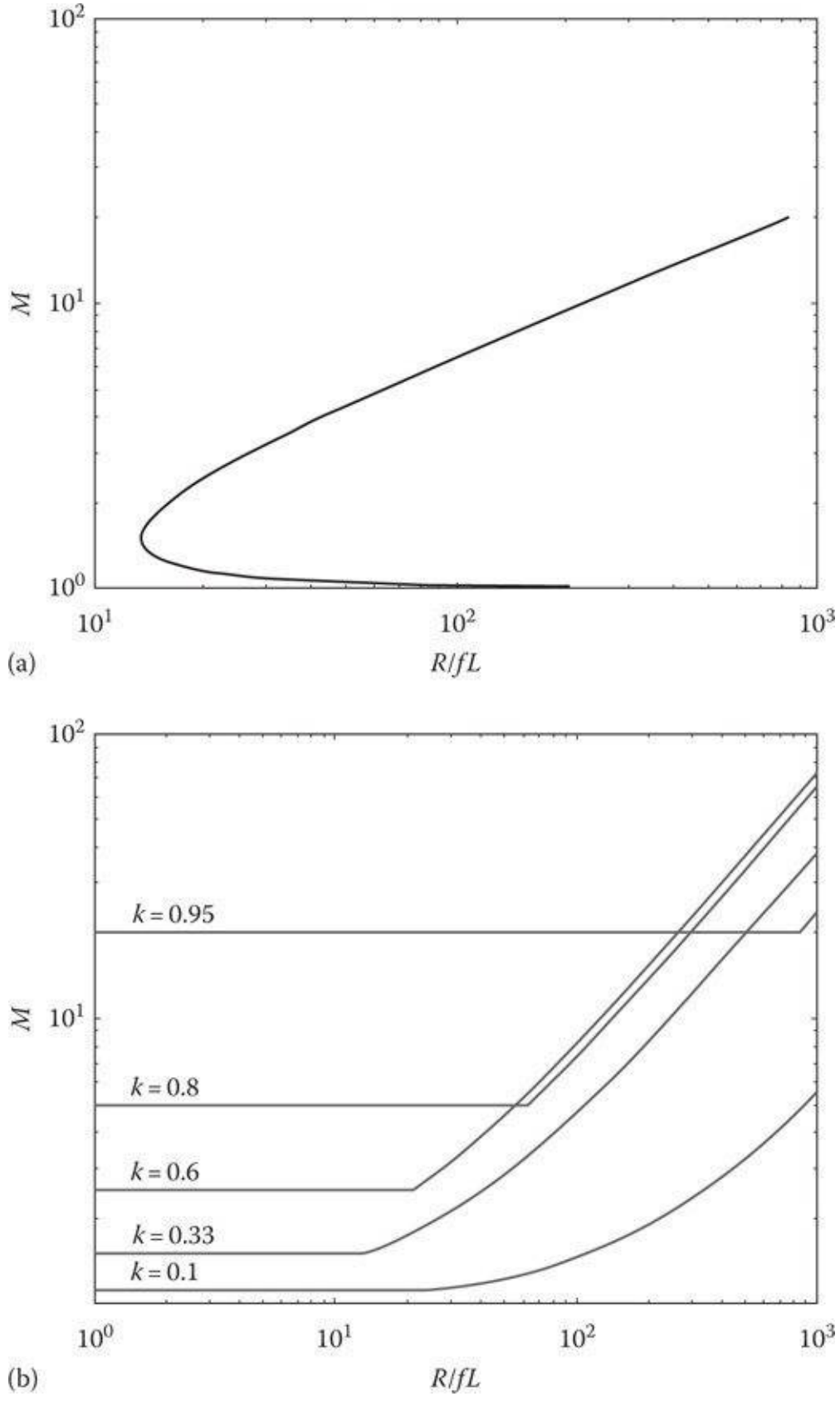


FIGURE 2.3
Boundary between continuous conduction mode and discontinuous conduction mode and DC voltage transfer gain *M* versus the normalized load at various *k*. (a) Boundary between CCM and DCM. (b) The voltage transfer gain *M* versus the normalized load at various *k*.

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In the DCM, current i_L increases during switch-on and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_i and $-(V_C - V_i)$. Therefore,

$$kTV_i = (1-k)mT(V_C - V_i)$$

Hence,

$$V_C = \left[1 + \frac{k}{(1-k)m}\right] V_i \tag{2.29}$$

Since we assume that C, C_1, and C_o are large enough,

$$V_o = V_C = V_{C_o} = \left[1 + \frac{k}{(1-k)m}\right] V_i \tag{2.30}$$

or

$$V_o = \left[1 + k^2(1-k)\frac{R}{2fL}\right] V_i \tag{2.31}$$

The voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL} \tag{2.32}$$

The relation between DC voltage transfer gain M and the normalized load at various k in the DCM is also shown in Figure 2.3b. It can be seen that in DCM, the output voltage increases as the load resistance R increases.

2.2.2 Self-Lift P/O Luo-Converter

The self-lift P/O Luo-converter and the equivalent circuits during switch-on and switch-off period are shown in Figure 2.4. It is the self-lift circuit of the P/O Luo-converter. It is derived from the elementary circuit of P/O Luo-converter. During switch-on period, S and D_1 are on, and D is switch-off. During switch-off period, D is on, and S and D_1 are off.

2.2.2.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus,

$$V_C = V_{C_o} = V_o$$

During switch-on period, the voltage across capacitor C_1 is equal to the source voltage. Since we assume that C and C_1 are sufficiently large,

$$V_{C_1} = V_i$$

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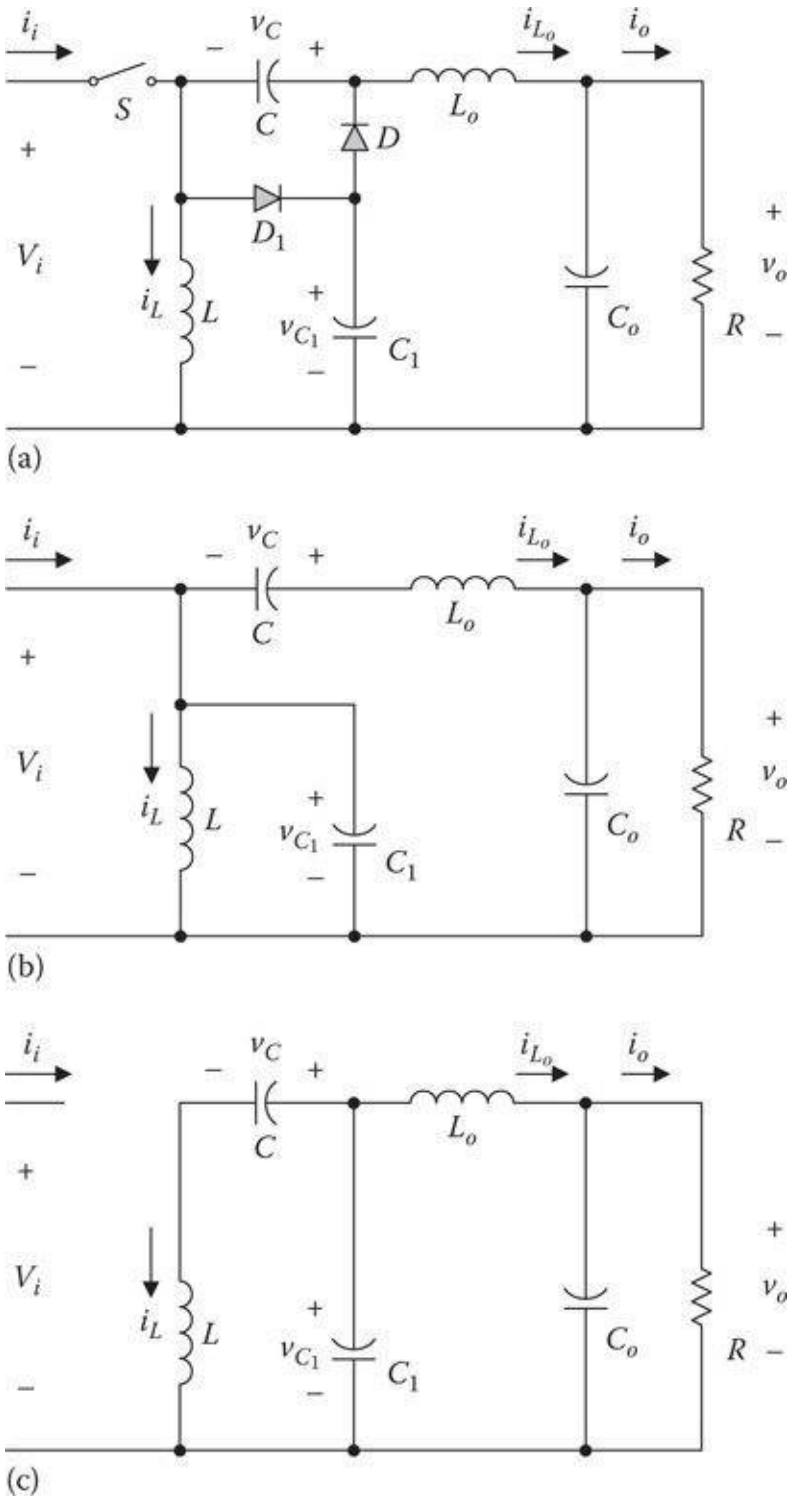


FIGURE 2.4
Self-lift positive-output Luo-converter and its equivalent circuits. (a) Self-lift positive-output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

The inductor current i_L increases in the switch-on period, and it decreases in the switch-off period. The corresponding voltages across L are V_i and $-(V_C - V_{C_1})$.
Therefore,

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$$kTV_i = (1-k)T(V_C - V_{C_1}) \tag{2.33}$$

Hence,

$$V_o = \frac{1}{1-k} V_i$$

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.34}$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

Thus,

$$I_i = \frac{1}{1-k} I_o$$

The capacitor C_o acts as a low-pass filter so that

$$I_{L_o} = I_o$$

The charge of capacitor C increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C-on} kT = I_o kT \quad Q_- = I_{C-off}(1-k)T = I_L(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_L = \frac{k}{1-k} I_o$$

During switch-off period,

$$i_D = i_L + i_{L_o}$$

Therefore,

$$I_D = I_L + I_{L_o} = \frac{1}{1-k} I_o$$

For the current and voltage variations and boundary condition, we can get the following equations using a similar method that was used in the analysis of self-lift Cúk converter.

The current variations are

$$\zeta_1 = \frac{1}{2M^2} \frac{R}{fL} \quad \zeta_2 = \frac{k}{2M} \frac{R}{fL_o} \quad \xi = \frac{k}{2M^2} \frac{R}{fL_{eq}}$$

where L_{eq} refers to

$$L_{eq} = \frac{LL_o}{L + L_o}$$

The voltage variations are

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$$\rho = \frac{k}{2}\frac{1}{fCR} \quad \sigma_1 = \frac{M}{2}\frac{1}{fC_1R} \quad \varepsilon = \frac{k}{8M}\frac{1}{f^2L_oC_o}$$

2.2.2.2 Discontinuous Conduction Mode

A self-lift P/O Luo-converter operates in the DCM if the current i_D reduces to zero during switch-off. As the critical case, when i_D decreases to zero at t = T, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2}\frac{R}{fL_{eq}} = 1$$

Therefore, the boundary between CCM and DCM is

$$M_B = \sqrt{k}\sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \tag{2.35}$$

where

z_N is the normalized load $R/(fL_{eq})$

L_{eq} refers to $L_{eq} = \dfrac{LL_o}{L+L_o}$

When $M > M_B$, the circuit operates at the DCM. In this case, the circuit operates in the diode current i_D that decreases to zero at $t = t_1 = [k + (1 - k)m]T$, where $kT < t_1 < T$ and $0 < m < 1$, with m as the current FF. We define m as

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2fL_{eq}}} \tag{2.36}$$

In the DCM, current i_L increases in the switch-on period kT and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_i and $-(V_C - V_{C_1})$

Therefore,

$$kTV_I = (1-k)mT(V_C - V_{C_1})$$

and

$$V_C = V_{C_o} = V_o \quad V_{C_1} = V_i$$

Hence,

$$V_o = \left[1 + \frac{k}{(1-k)m}\right]V_i \quad \text{or} \quad V_o = \left[1 + k^2(1-k)\frac{R}{2fL_{eq}}\right]V_i \tag{2.37}$$

So the real DC voltage transfer gain in the DCM is

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$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL_{eq}} \tag{2.38}$$

In DCM, the output voltage increases as the load resistance R increases.

2.2.3 Reverse Self-Lift P/O Luo-Converter

The reverse self-lift P/O Luo-converter and the equivalent circuits during switch-on and switch-off period are shown in Figure 2.5. It is derived from the elementary circuit of P/O Luo-converters. During switch-on period, S and D_1 are on, and D is off. During switch-off period, D is on, and S and D_1 are off.

2.2.3.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero.

Thus,

$$V_{C_1} = V_{C_o} = V_o$$

During switch-on period, the voltage across capacitor C is equal to the source voltage plus the voltage across C_1. Since we assume that C and C_1 are sufficiently large,

$$V_{C_1} = V_i + V_C$$

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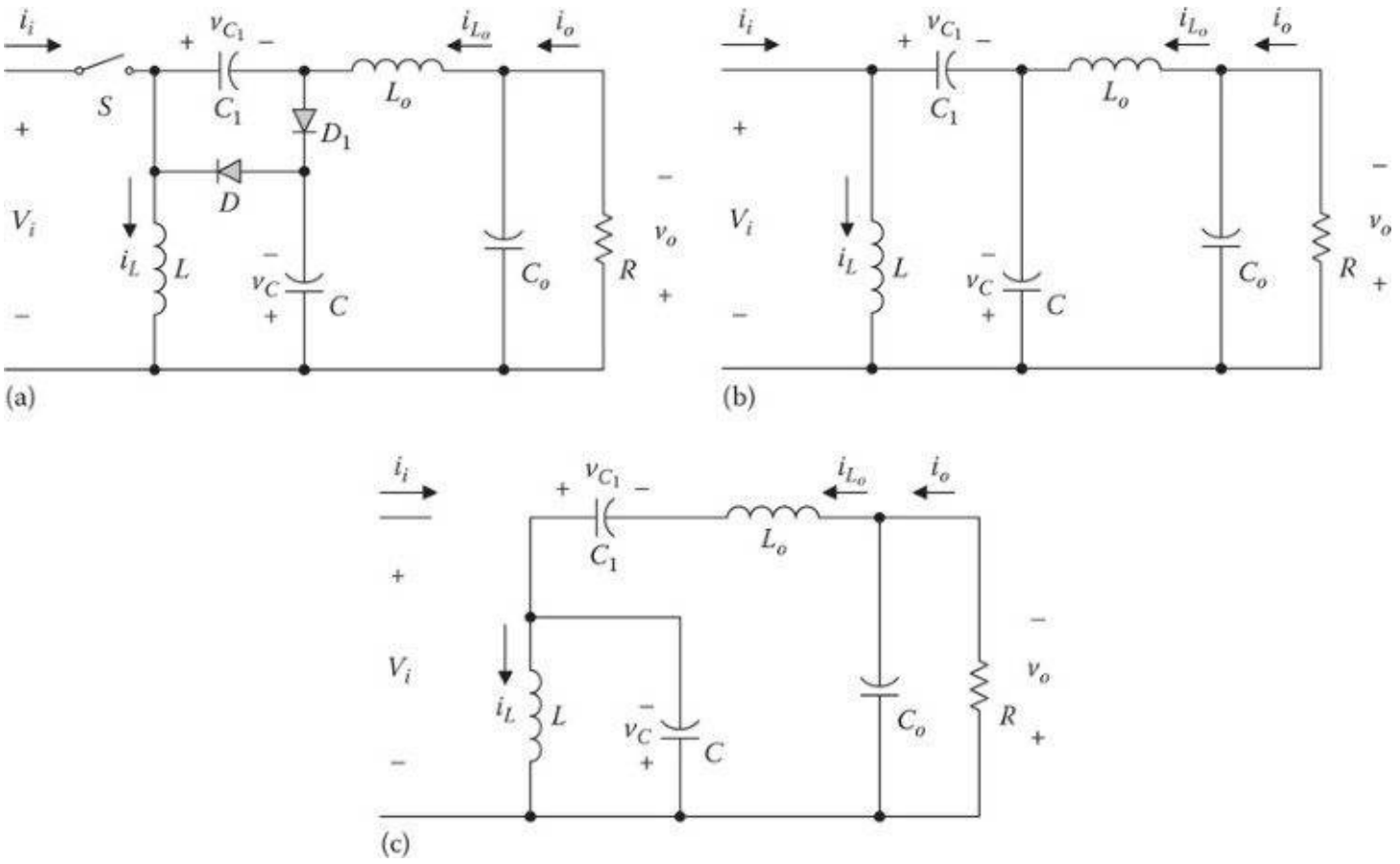


FIGURE 2.5
Reverse self-lift positive-output Luo-converter and its equivalent circuits. (a) Reverse self-lift positive-output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

Therefore,

$$V_{C_1} = V_i + \frac{k}{1-k}V_i = \frac{1}{1-k}V_i \quad V_o = V_{C_o} = V_{C_1} = \frac{1}{1-k}V_i \tag{2.39}$$

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.40}$$

Since all the components are considered ideal, the power losses on all the circuit elements are neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

Thus,

$$I_i = \frac{1}{1-k}I_o$$

The capacitor C_o acts as a low-pass filter so that

$$I_{L_o} = I_o$$

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The charge of capacitor C_1 increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C_1-on}kT$$

$$Q_- = I_{L_o}(1-k)T = I_o(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_{C_1-on} = \frac{1-k}{k} I_o$$

$$I_{C-on} = I_{Lo} + I_{C_1-on} = I_o + \frac{1-k}{k} I_o = \frac{1}{k} I_o \tag{2.41}$$

The charge of capacitor C increases during switch-off and decreases during switch-on.

$$Q_+ = I_{C-off}(1-k)T \quad Q_- = I_{C-on}kT = \frac{1}{k} I_o kT$$

In a switching period,

$$Q_+ = Q_- \quad I_{C-off} = \frac{1-k}{k} I_{C-on} = \frac{1}{1-k} I_o \tag{2.42}$$

Therefore,

$$I_L = I_{Lo} + I_{C-off} = I_o + \frac{1}{1-k} I_o = \frac{2-k}{1-k} I_o = I_o + I_i$$

During switch-off,

$$i_D = i_L - i_{L_o}$$

Therefore,

$$I_D = I_L - I_{L_o} = I_o$$

The following equations are used for current and voltage variations and boundary conditions.

The current variations are

$$\zeta_1 = \frac{k}{(2-k)M^2} \frac{R}{fL} \quad \zeta_2 = \frac{k}{2M} \frac{R}{fL_o} \quad \xi = \frac{1}{2M^2} \frac{R}{fL_{eq}}$$

where L_{eq} refers to $L_{eq} = \dfrac{LL_o}{L+L_o}$

The voltage variations are

$$\rho = \frac{1}{2k} \frac{1}{fCR} \quad \sigma_1 = \frac{1}{2M} \frac{1}{fC_1R} \quad \varepsilon = \frac{k}{16M} \frac{1}{f^2C_oL_o}$$

2.2.3.2 Discontinuous Conduction Mode

The reverse self-lift P/O Luo-converter operates in the DCM if the current i_D reduces to zero during switch-off at $t = T$; then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

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$$\xi = \frac{k}{2M^2}\frac{R}{fL_{eq}} = 1$$

Therefore, the boundary between CCM and DCM is

$$M_B = \sqrt{k}\sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \tag{2.43}$$

where

z_N is the normalized load R/(fL_{eq})

L_{eq} refers to $L_{eq} = \dfrac{LL_o}{L+L_o}$

When $M > M_B$, the circuit operates in the DCM. In this case, the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$, where $kT < t_1 < T$ and $0 < m < 1$. m is the current FF:

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2fL_{eq}}} \tag{2.44}$$

In the DCM, current i_L increases during switch-on and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_i and $-V_C$.

Therefore,

$$kTV_i = (1-k)mTV_C$$

and

$$V_{C_1} = V_{C_o} = V_o \quad V_{C_1} = V_i + V_C$$

Hence,

$$V_o = \left[1 + \frac{k}{(1-k)m}\right]V_i$$

or

$$V_o = \left(1 + k^2(1-k)\frac{R}{2fL_{eq}}\right)V_i \tag{2.45}$$

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL} \tag{2.46}$$

In DCM, the output voltage increases as the load resistance R increases.

2.2.4 Self-Lift N/O Luo-Converter

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The self-lift N/O Luo-converter and the equivalent circuits during switch-on and switch-off period are shown in Figure 2.6. It is the self-lift circuit of the N/O Luo-converter. The function of capacitor C_1 is to lift the voltage V_C by a source voltage V_i. S and D_1 are on, and D is off during switch-on period. D is on, and S and D_1 are off during switch-off period.

2.2.4.1 Continuous Conduction Mode

In the steady state, the average inductor voltages over a period are zero. Thus,

$$V_C = V_{C_o} = V_o$$

During switch-on period, the voltage across capacitor C_1 is equal to the source voltage. Since we assume that C and C_1 are sufficiently large,

$$V_{C_1} = V_i$$

Inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_i and $-(V_C - V_{C_1})$.

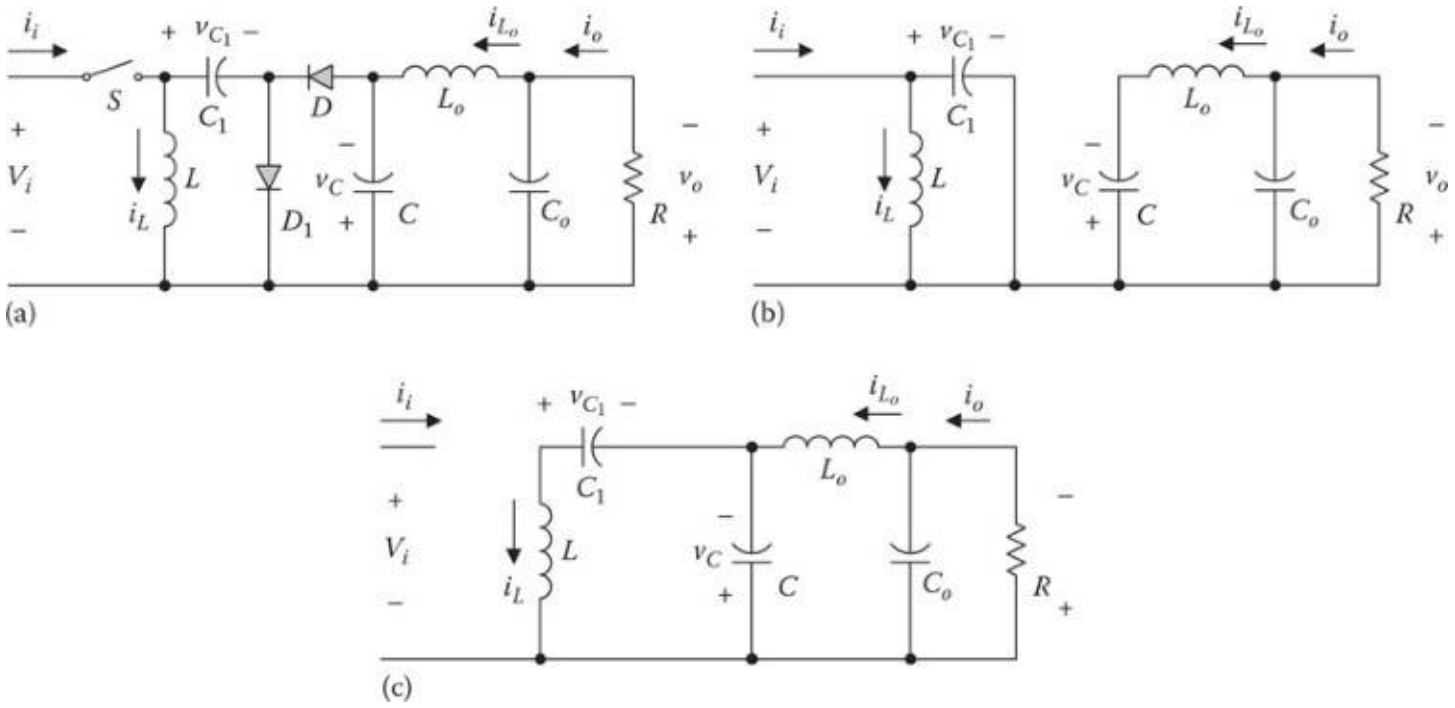


FIGURE 2.6
Self-lift negative-output Luo-converter and its equivalent circuits. (a) Self-lift negative-output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

Therefore,

$$kTV_i = (1-k)T(V_C - V_{C_1})$$

Hence,

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$$V_o = V_C = V_{C_o} = \frac{1}{1-k} V_i \tag{2.47}$$

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.48}$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

Thus,

$$I_i = \frac{1}{1-k} I_o$$

The capacitor C_o acts as a low-pass filter so that

$$I_{L_o} = I_o$$

For the current and voltage variations and boundary condition, the following equations can be obtained by using a similar method that was used in the analysis of self-lift Cúk converter.

The current variations are

$$\zeta_1 = \frac{k}{2M^2} \frac{R}{fL}, \quad \zeta_2 = \frac{k}{16} \frac{1}{f^2 L_o C} \quad \xi = \frac{k}{2M^2} \frac{R}{fL}$$

The voltage variations are

$$\rho = \frac{k}{2} \frac{1}{fCR}, \quad \sigma_1 = \frac{M}{2} \frac{1}{fC_1 R} \quad \varepsilon = \frac{k}{128} \frac{1}{f^3 L_o C C_o R}$$

2.2.4.2 Discontinuous Conduction Mode

The self-lift N/O Luo-converter operates in the DCM if the current i_D reduces to zero at $t = T$; then the circuit operates at the boundary of CCM and DCM. The variation ratio of the current i_D is 1 when the circuit works at the boundary state.

$$\xi = \frac{k}{2M^2} \frac{R}{fL} = 1$$

Therefore, the boundary between CCM and DCM is

$$M_B = \sqrt{k} \sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \tag{2.49}$$

where L_{eq} refers to $L_{eq} = L$ and z_N is the normalized load $R/(fL_{eq})$.

When $M > M_B$, the circuit operates in the DCM. In this case, the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$, where $kT < t_1 < T$ and $0 < m < 1$. m is the current FF and is

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defined as

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2fL}} \tag{2.50}$$

In the DCM, current i_L increases during switch-on and decreases during period from kT to $(1 - k)mT$. The voltages across L are V_i and $-(V_C - V_{C_1})$.

$$kTV_i = (1-k)mT(V_C - V_{C_1})$$

and

$$V_{C_1} = V_i \quad V_C = V_{C_o} = V_o$$

Hence,

$$V_o = \left[1 + \frac{k}{(1-k)m}\right] V_i$$

or

$$V_o = \left[1 + k^2(1-k)\frac{R}{2fL}\right] V_i$$

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL} \tag{2.51}$$

We can see that in DCM, the output voltage increases as the load resistance R increases.

2.2.5 Reverse Self-Lift N/O Luo-Converter

The reverse self-lift N/O Luo-converter and the equivalent circuits during switch-on and switch-off period are shown in Figure 2.7. It is derived from the Zeta converter. During switch-on period, S and D_1 are on, and D is off. During switch-off period, D is on, and S and D_1 are off.

2.2.5.1 Continuous Conduction Mode

In steady state, the average inductor voltages over a period are zero. Thus,

$$V_{C_1} = V_{C_o} = V_o$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_i and $-V_C$.

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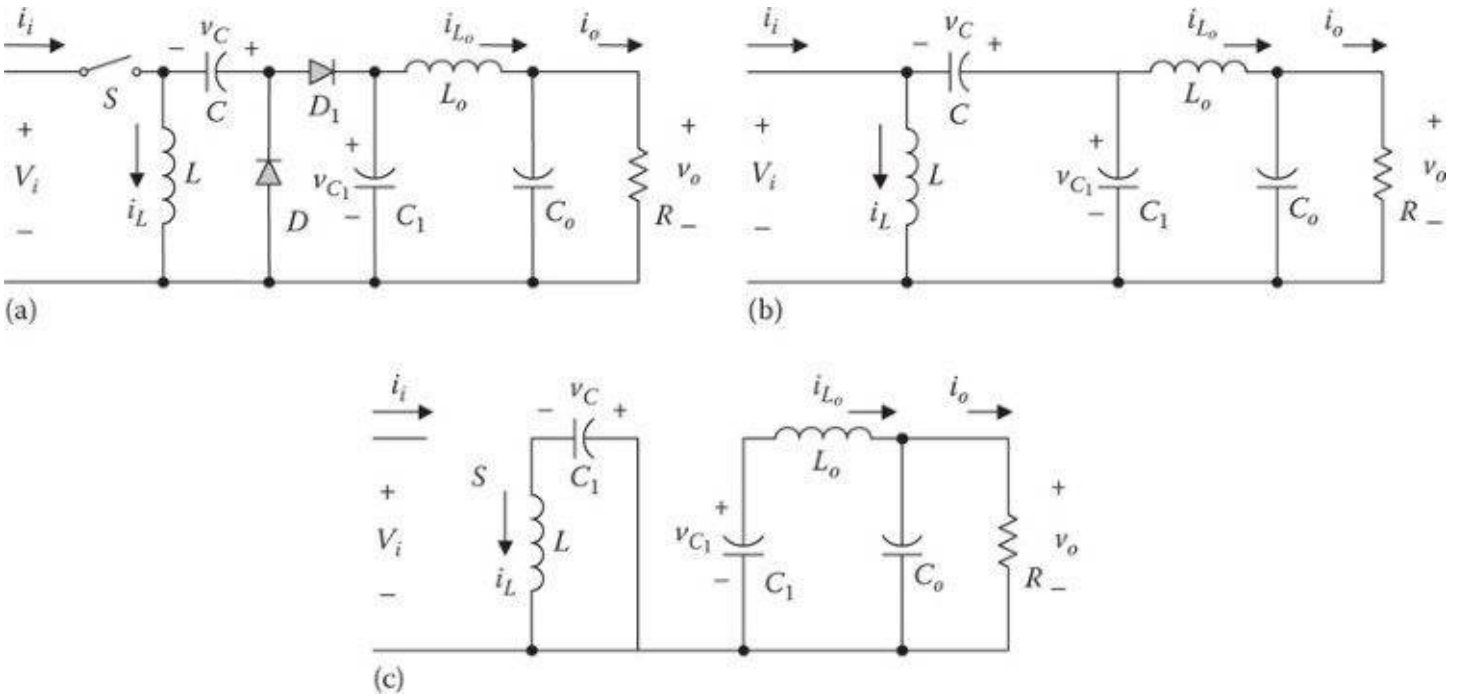


FIGURE 2.7
Reverse self-lift negative-output Luo-converter and its equivalent circuits. (a) Reverse self-lift negative-output Luo-converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

Therefore,

$$kTV_i = (1-k)TV_C$$

Hence,

$$V_C = \frac{k}{1-k} V_i \tag{2.52}$$

is the voltage across C. Since we assume that C and C_1 are sufficiently large,

$$V_{C_1} = V_i + V_C$$

Therefore,

$$V_{C_1} = V_i + \frac{k}{1-k} V_i = \frac{1}{1-k} V_i \quad V_o = V_{C_o} = V_{C_1} = \frac{1}{1-k} V_i$$

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.53}$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

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Thus,

$$I_i = \frac{1}{1-k} I_o$$

The capacitor C_o acts as a low-pass filter so that

$$I_{L_o} = I_o$$

The charge of capacitor C_1 increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C_1-on} kT \quad Q_- = I_{C_1-off}(1-k)T = I_o(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_{C_1-on} = \frac{1-k}{k} I_{C-off} = \frac{1-k}{k} I_o$$

The charge of capacitor C increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C-on} kT \quad Q_- = I_{C-off}(1-k)T$$

In a switching period,

$$Q_+ = Q_-$$

$$I_{C-on} = I_{C_1-on} + I_{Lo} = \frac{1-k}{k} I_o + I_o = \frac{1}{k} I_o \quad I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k}\frac{1}{k} I_o = \frac{1}{1-k} I_o$$

Therefore,

$$I_L = I_{C-off} = \frac{1}{1-k} I_o$$

During switch-off period,

$$i_D = i_L \quad I_D = I_L = \frac{1}{1-k} I_o$$

For the current and voltage variations and the boundary condition, we can get the following equations using a similar method that was used in the analysis of self-lift Cúk converter.

The current variations are

$$\zeta_1 = \frac{k}{2M^2}\frac{R}{fL} \quad \zeta_2 = \frac{1}{16M}\frac{R}{f^2 L_o C_1} \quad \xi = \frac{k}{2M^2}\frac{R}{fL}$$

The voltage variations are

$$\rho = \frac{1}{2k}\frac{1}{fCR} \quad \sigma_1 = \frac{1}{2M}\frac{1}{fC_1 R} \quad \varepsilon = \frac{1}{128M}\frac{1}{f^3 L_o C_1 C_o R}$$

2.2.5.2 Discontinuous Conduction Mode

The reverse self-lift N/O Luo-converter operates in the DCM if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

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$$\xi = \frac{k}{2M^2}\frac{R}{fL_{eq}} = 1$$

The boundary between CCM and DCM is

$$M_B = \sqrt{k}\sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}}$$

where

z_N is the normalized load $R/(fL_{eq})$

L_{eq} refers to $L_{eq} = L$

When $M > M_B$, the circuit operates at the DCM. In this case, diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $kT < t_1 < T$ and $0 < m < 1$ with m as the current FF:

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2fL_{eq}}} \tag{2.54}$$

In the DCM, current i_L increases in the switch-on period kT and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_i and $-V_C$.

Therefore,

$$kTV_i = (1-k)mTV_C$$

and

$$V_{C_1} = V_{C_o} = V_o \quad V_{C_1} = V_i + V_C$$

Hence,

$$V_o = \left[1 + \frac{k}{(1-k)m}\right]V_i \quad \text{or} \quad V_o = \left(1 + k^2(1-k)\frac{R}{2fL}\right)V_i \tag{2.55}$$

The voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL} \tag{2.56}$$

It can be seen that in DCM, the output voltage increases as the load resistance R increases.

2.2.6 Self-Lift SEPIC

The self-lift SEPIC and its equivalent circuits during switch-on and switch-off period are shown in Figure 2.8. It is derived from SEPIC (with output filter). S and D_1 are on, and D is off during switch-on period. D is on, and S and D_1 are off during switch-off period.

2.2.6.1 Continuous Conduction Mode

In steady state, the average voltage across inductor L over a period is zero. Thus, $V_C = V_i$.

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During switch-on period, the voltage across capacitor C_1 is equal to the voltage across C. Since we assume that C and C_1 are sufficiently large, $V_{C_1} = V_C = V_i$.

In steady state, the average voltage across inductor L_o over a period is also zero.

Thus,

$$V_{C_2} = V_{C_o} = V_o.$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_i and $-(V_C - V_{C_1} + V_{C_2} - V_i)$.

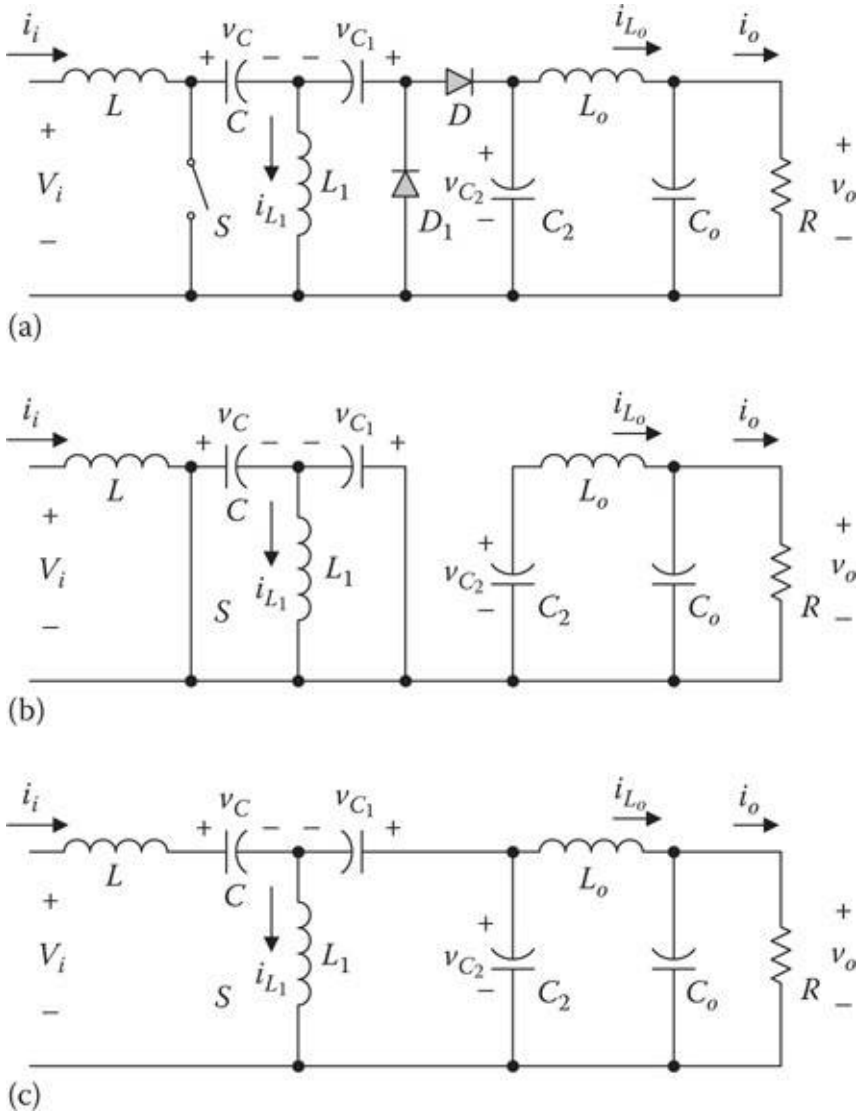


FIGURE 2.8
Self-lift single-ended primary inductance converter and its equivalent circuits. (a) Self-lift SEPIC converter. (b) The equivalent circuit during switch-on. (c) The equivalent circuit during switch-off.

Therefore,

$$kTV_i = (1-k)T(V_C - V_{C_1} + V_{C_2} - V_i)$$

or

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$$kTV_i = (1-k)T(V_o - V_i)$$

Hence,

$$V_o = \frac{1}{1-k}V_i = V_{C_o} = V_{C_2} \tag{2.57}$$

The voltage transfer gain in the CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.58}$$

Since all the components are considered ideal, the power loss associated with all the circuit elements is neglected. Therefore, the output power P_o is considered to be equal to the input power P_{in}:

$$V_o I_o = V_i I_i$$

Thus,

$$I_i = \frac{1}{1-k}I_o = I_L$$

The capacitor C_o acts as a low-pass filter so that $I_{L_o} = I_o$.

The charge of capacitor C increases during switch-off and decreases during switch-on.

$$Q_- = I_{C-on}kT \quad Q_+ = I_{C-off}(1-k)T = I_i(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_{C-on} = \frac{1-k}{k}I_{C-off} = \frac{1-k}{k}I_i$$

The charge of capacitor C_2 increases during switch-off and decreases during switch-on.

$$Q_- = I_{C_2-on}kT = I_o kT \quad Q_+ = I_{C_2-off}(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_{C_2-off} = \frac{k}{1-k}I_{C-N} = \frac{k}{1-k}I_o$$

The charge of capacitor C_1 increases during switch-on and decreases during switch-off.

$$Q_+ = I_{C_1-on}kT \quad Q_- = I_{C_1-off}(1-k)T$$

In a switching period,

$$Q_+ = Q_- \quad I_{C_1-off} = I_{C_2-off} + I_{L_o} = \frac{k}{1-k}I_o + I_o = \frac{1}{1-k}I_o$$

Therefore,

$$I_{C_1-on} = \frac{1-k}{k}I_{C_1-off} = \frac{1}{k}I_o \quad I_{L_1} = I_{C_1-on} - I_{C-on} = 0$$

During switch-off,

$$i_D = i_L - i_{L_1}$$

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Therefore,

$$I_D = I_i = \frac{1}{1-k} I_o$$

For the current and voltage variations and the boundary condition, we can get the following equations using a similar method that is used in the analysis of self-lift Cúk converter.

The current variations are

$$\zeta_1 = \frac{k}{2M^2}\frac{R}{fL} \quad \zeta_2 = \frac{k}{16}\frac{R}{f^2 L_o C_2} \quad \xi = \frac{k}{2M^2}\frac{R}{fL_{eq}}$$

where L_{ea} refers to

$$L_{eq} = \frac{LL_o}{L+L_o}$$

The voltage variations are

$$\rho = \frac{M}{2}\frac{1}{fCR} \quad \sigma_1 = \frac{M}{2}\frac{1}{fC_1 R} \quad \sigma_2 = \frac{k}{2}\frac{1}{fC_2 R} \quad \varepsilon = \frac{k}{128}\frac{1}{f^3 L_o C_2 C_o R}$$

2.2.6.2 Discontinuous Conduction Mode

The self-lift SEPIC converter operates in the DCM if the current i_D reduces to zero during switch-off. As a special case, when i_D decreases to zero at $t = T$, then the circuit operates at the boundary of CCM and DCM.

The variation ratio of the current i_D is 1 when the circuit works in the boundary state.

$$\xi = \frac{k}{2M^2}\frac{R}{fL_{eq}} = 1$$

Therefore, the boundary between CCM and DCM is

$$M_B = \sqrt{k}\sqrt{\frac{R}{2fL_{eq}}} = \sqrt{\frac{kz_N}{2}} \tag{2.59}$$

where

z_N is the normalized load $R/(fL_{eq})$

L_{eq} refers to $L_{eq} = \dfrac{LL_o}{L+L_o}$

When $M > M_B$, the circuit operates in the DCM. In this case, the diode current i_D decreases to zero at $t = t_1 = [k + (1 - k)m]T$ where $kT < t_1 < T$ and $0 < m < 1$. m is defined as

$$m = \frac{1}{\xi} = \frac{M^2}{k\dfrac{R}{2fL_{eq}}} \tag{2.60}$$

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In the DCM, current i_L increases during switch-on and decreases in the period from kT to $(1 - k)mT$. The corresponding voltages across L are V_i and $-(V_C - V_{C_1} + V_{C_2} - V_i)$.

Thus,

$$kTV_i = (1-k)T(V_C - V_{C_1} + V_{C_2} - V_i)$$

and

$$V_C = V_i \quad V_{C_1} = V_C = V_i \quad V_{C_2} = V_{C_o} = V_o$$

Hence,

$$V_o = \left[1 + \frac{k}{(1-k)m}\right] V_i$$

or

$$V_o = \left(1 + k^2(1-k)\frac{R}{2fL_{eq}}\right) V_i$$

So the real DC voltage transfer gain in the DCM is

$$M_{DCM} = 1 + k^2(1-k)\frac{R}{2fL_{eq}} \tag{2.61}$$

In DCM, the output voltage increases as the load resistance R increases.

2.2.7 Enhanced Self-Lift P/O Luo-Converters

Enhanced self-lift P/O Luo-converters are shown in Figure 2.9. *Type A* is derived from the self-lift P/O Luo-converter in Figure 2.4 with swapping the positions of switch S and inductor L (renumbered L to L_1).

Type *A* is shown in Figure 2.9a. During switch-on period, S and D_2 are on, and D_1 is off. We obtain

$$V_{C_1} = V_{C_2}$$

and

$$\Delta i_L = \frac{V_i}{L} kT$$

During switch-off period, D_1 is on, and S and D_2 are off.

$$\Delta i_L = \frac{V_{C_2} - V_i}{L}(1-k)T$$

so that

$$V_{C_1} = V_{C_2} = \frac{1}{1-k} V_i \tag{2.62}$$

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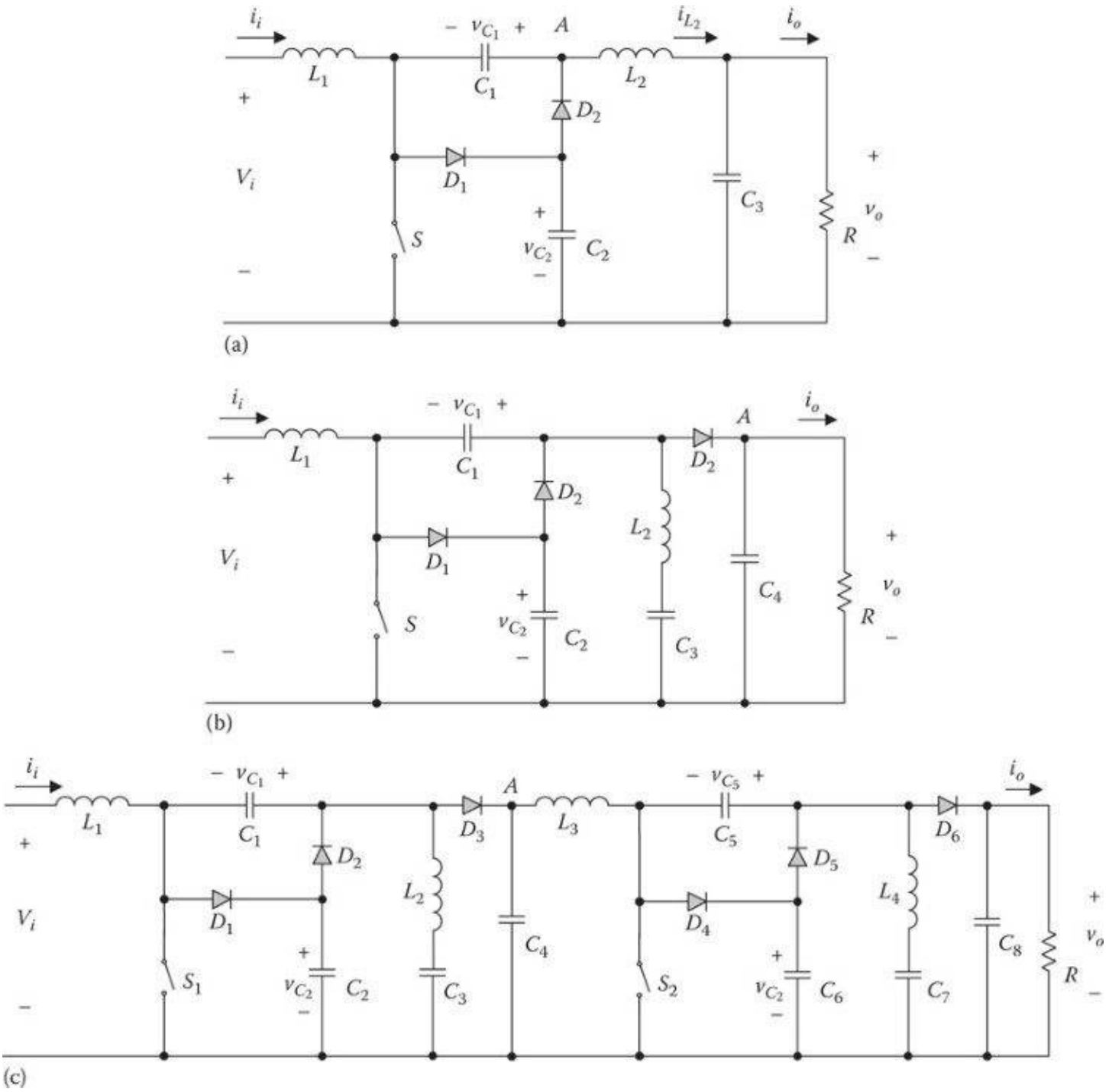


FIGURE 2.9
Enhanced self-lift positive-output Luo-converters. (a) Type *A*. (b) Type *B*. (c) Type *C*.

The output voltage and current and the voltage transfer gain are

$$V_o = V_i + V_{C_1} = \left(1 + \frac{1}{1-k}\right) V_i = \frac{2-k}{1-k} V_i \tag{2.63}$$

$$I_o = \frac{1-k}{2-k} I_i \quad M_A = \frac{V_o}{V_i} = \frac{2-k}{1-k} \tag{2.64}$$

For average currents,

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$$I_{L_2} = I_o \quad I_L = \frac{2-k}{1-k} I_o = I_i \tag{2.65}$$

Type *B* is shown in Figure 2.9b, which is similar to Type *A*. The voltage at Point *A* is higher than the output voltage in Figure 2.9a during switch-off. The voltage drop across inductor L_1 is

$$V_{L_1-off} = \frac{k}{1-k} V_i \tag{2.66}$$

During switch-off period, the voltage at Point *A* is

$$V_{A-off} = V_i + V_{L_1-off} + V_{C_1} = \left(1 + \frac{k}{1-k} + \frac{1}{1-k}\right) V_i = \frac{2}{1-k} V_i$$

The output voltage and the voltage transfer gain are

$$V_o = V_{A-off} = \frac{2}{1-k} V_i \tag{2.67}$$

$$M_B = \frac{2}{1-k} \tag{2.68}$$

Type *C* is shown in Figure 2.9c. Both switches S_1 and S_2 are synchronously switching-on and switching-off. The output voltage and the voltage transfer gain are

$$V_o = \frac{2}{1-k} V_A = \left(\frac{2}{1-k}\right)^2 V_i \quad M_C = \left(\frac{2}{1-k}\right)^2 \tag{2.69}$$

Type *C* is a cascaded circuit of Type *B*. If some industrial applications require higher-voltage transfer gain, Type *B* can be cascaded multiple times. Assuming the stage number is *n*, the output voltage and the voltage transfer gain are

$$V_o = \left(\frac{2}{1-k}\right)^n V_i \quad M_N = \left(\frac{2}{1-k}\right)^n \tag{2.70}$$

2.3 P/O Luo-Converters

P/O Luo-converters perform the voltage conversion from positive to positive voltages using VL technique. They work in the first quadrant with large voltage amplification. Five circuits have been introduced in the literature:

- Elementary circuit
- Self-lift circuit
- Re-lift circuit

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- Triple-lift circuit
- Quadruple-lift circuit

The elementary circuit can perform step-down and step-up DC/DC conversion, which was introduced in the previous section. Other P/O Luo-converters are derived from this elementary circuit; they are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits) shown in the corresponding figures. Switch S in these diagrams is a P-channel power MOSFET (PMOS) device, and S_1 is an N-channel power MOSFET (NMOS) device. They are driven by a PWM switching signal with repeating frequency f and conduction duty k. The switch repeating period is $T = 1/f$ so that the switch-on period is kT and switch-off period is $(1 - k)T$. For all circuits, the load is usually resistive, $R = V_o/I_o$; the combined inductor $L = L_1L_2/(L_1 + L_2)$; the normalized load is $z_N = R/fL$. Each converter consists of a positive Luo-pump and a low-pass filter $L_2 - C_o$ and lift circuit (introduced in the following sections). The pump inductor L_1 transfers the energy from source to capacitor C during switch-off, and then the stored energy on capacitor C is delivered to load R during switch-on. Therefore, if the voltage V_C is higher, the output voltage V_o should be higher.

When the switch S is turned off, the current i_D flows through the freewheeling diode D. This current descends in whole switch-off period $(1 - k)T$. If current i_D does not become zero before switch S turned on again, this working state is defined as the CCM. If current i_D becomes zero before switch S turned on again, this working state is defined as the DCM.

Assuming that the output power is equal to the input power,

$$P_o = P_{in} \quad \text{or} \quad V_oI_o = V_iI_i$$

The voltage transfer gain in continuous mode is

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o}$$

The variation ratio of current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}}$$

The variation ratio of current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D/2}{I_{L_1} + I_{L_2}}$$

The variation ratio of current i_{L_2+j} is

$$\chi_j = \frac{\Delta i_{L_2+j}/2}{I_{L_2+j}} \quad j = 1, 2, 3, \ldots$$

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The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C}$$

The variation ratio of voltage v_{C_j} is

$$\sigma_j = \frac{\Delta v_{C_j}/2}{V_{C_j}} \quad j = 1,2,3,4,\ldots$$

The variation ratio of output voltage v_{C_o} is

$$\varepsilon = \frac{\Delta v_o/2}{V_o}$$

2.3.1 Elementary Circuit

The elementary circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.10. Capacitor C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor L_1. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$ even though it stores and transfers energy from the input to the output.

2.3.1.1 Circuit Description

When switch S is on, the source current $i_i = i_{L_1} + i_{L_2}$ Inductor L_1 absorbs energy from the source. In the meantime, inductor L_2 absorbs energy from source and capacitor C, both currents i_{L_1} and i_{L_2} increase. When switch S is off, source current i_i = 0. Current i_{L_1} flows through the freewheeling diode D to charge capacitor C. Inductor L_1 transfers its stored energy to capacitor C. In the meantime, current i_{L_2} flows through the (C_0 – R) circuit and freewheeling diode D to keep itself continuous. Both currents i_{L_1} and i_{L_2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-on and switch-off states are shown in Figure 2.10b, c and d.

Actually, the variations of currents i_{L_1} and i_{L_2} are small so that $i_{L_1} \approx I_{L_1}$ and $i_{L_2} \approx I_{L_2}$.

The charge on capacitor C increases during switch-off:

$$Q_+ = (1-k)TI_{L_1}.$$

It decreases during switch-on:

$$Q_- = kTI_{L_2}.$$

In a whole period investigation, $Q_+ = Q_-$. Thus,

$$I_{L_2} = \frac{1-k}{k} I_{L_1} \tag{2.71}$$

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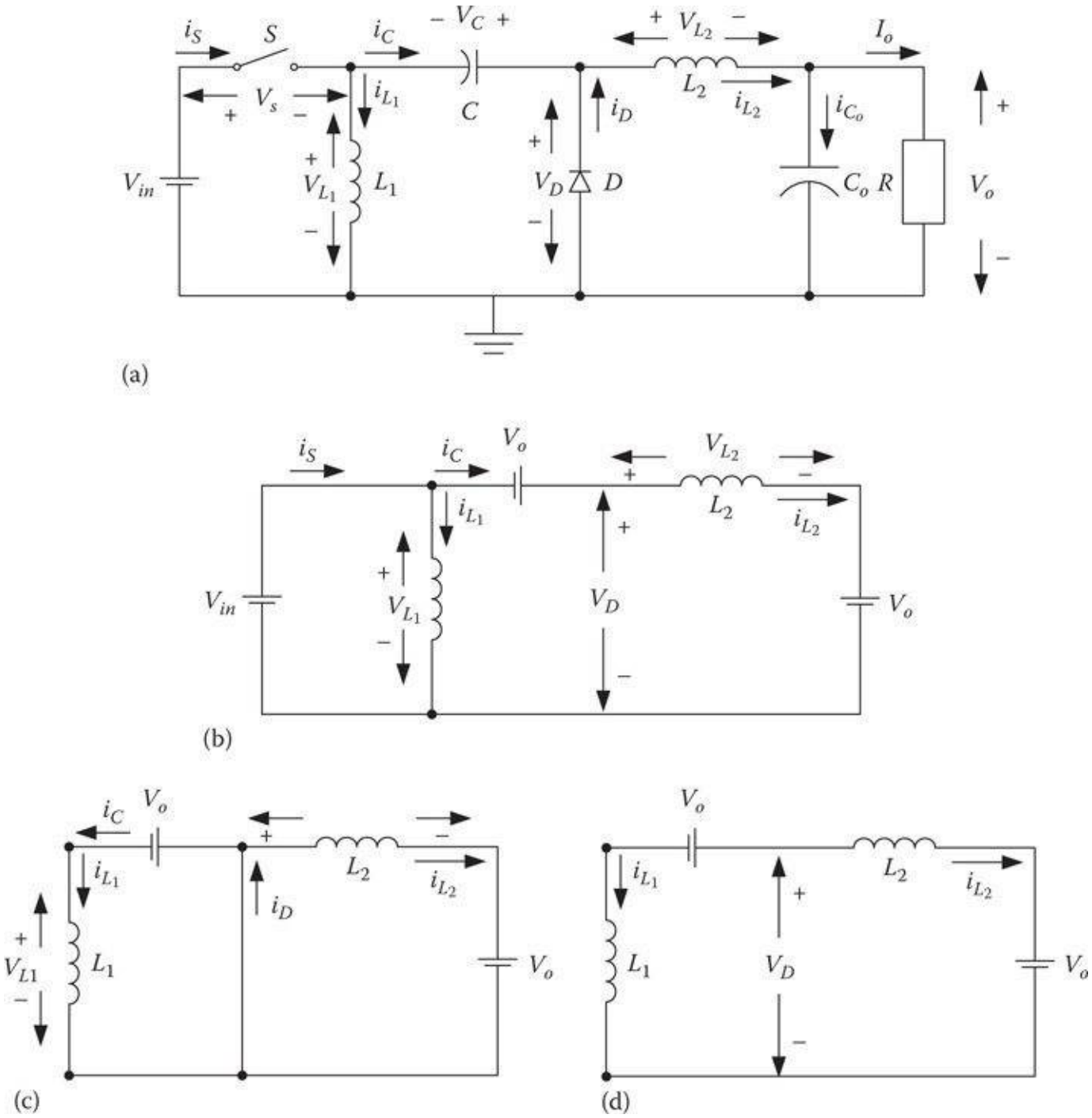


FIGURE 2.10
Elementary circuit: (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

Since capacitor C_o performs as a low-pass filter, the output current

$$I_{L_2} = I_o \tag{2.72}$$

These two Equations 2.71 and 2.72 are available for all P/O Luo-converters.

The source current $i_i = i_{L_1} + i_{L_2}$ during switch-on period and $i_i = 0$ during switch-off. Thus, the average source current I_i is

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$$I_i = k \times i_i = k(i_{L_1} + i_{L_2}) = k\left(1 + \frac{1-k}{k}\right) I_{L_1} = I_{L_1} \tag{2.73}$$

Therefore, the output current is

$$I_o = \frac{1-k}{k} I_i \tag{2.74}$$

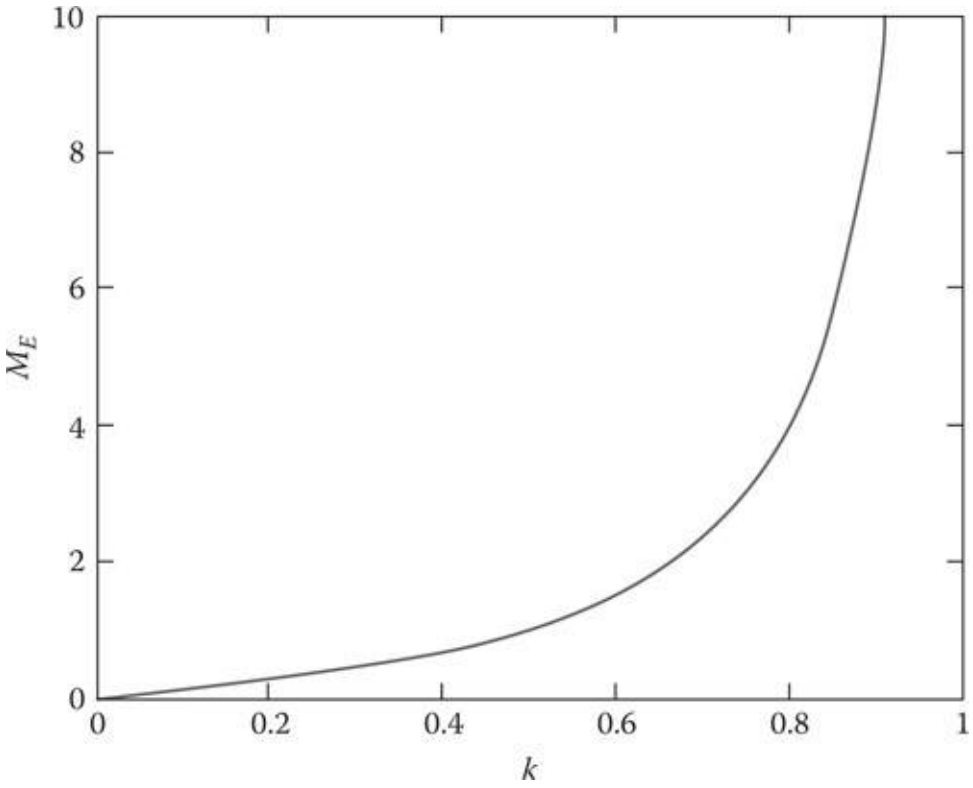


FIGURE 2.11
Voltage transfer gain M_E versus k.

Hence, the output voltage is

$$V_o = \frac{k}{1-k} V_i \tag{2.75}$$

The voltage transfer gain in continuous mode is

$$M_E = \frac{V_o}{V_i} = \frac{k}{1-k} \tag{2.76}$$

The curve of M_E versus k is shown in Figure 2.11.

Current i_{L_1} increases and is supplied by V_i during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off. Therefore,

$$kTV_i = (1-k)TV_C$$

The average voltage across capacitor C is

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$$V_C = \frac{k}{1-k} V_i = V_o \tag{2.77}$$

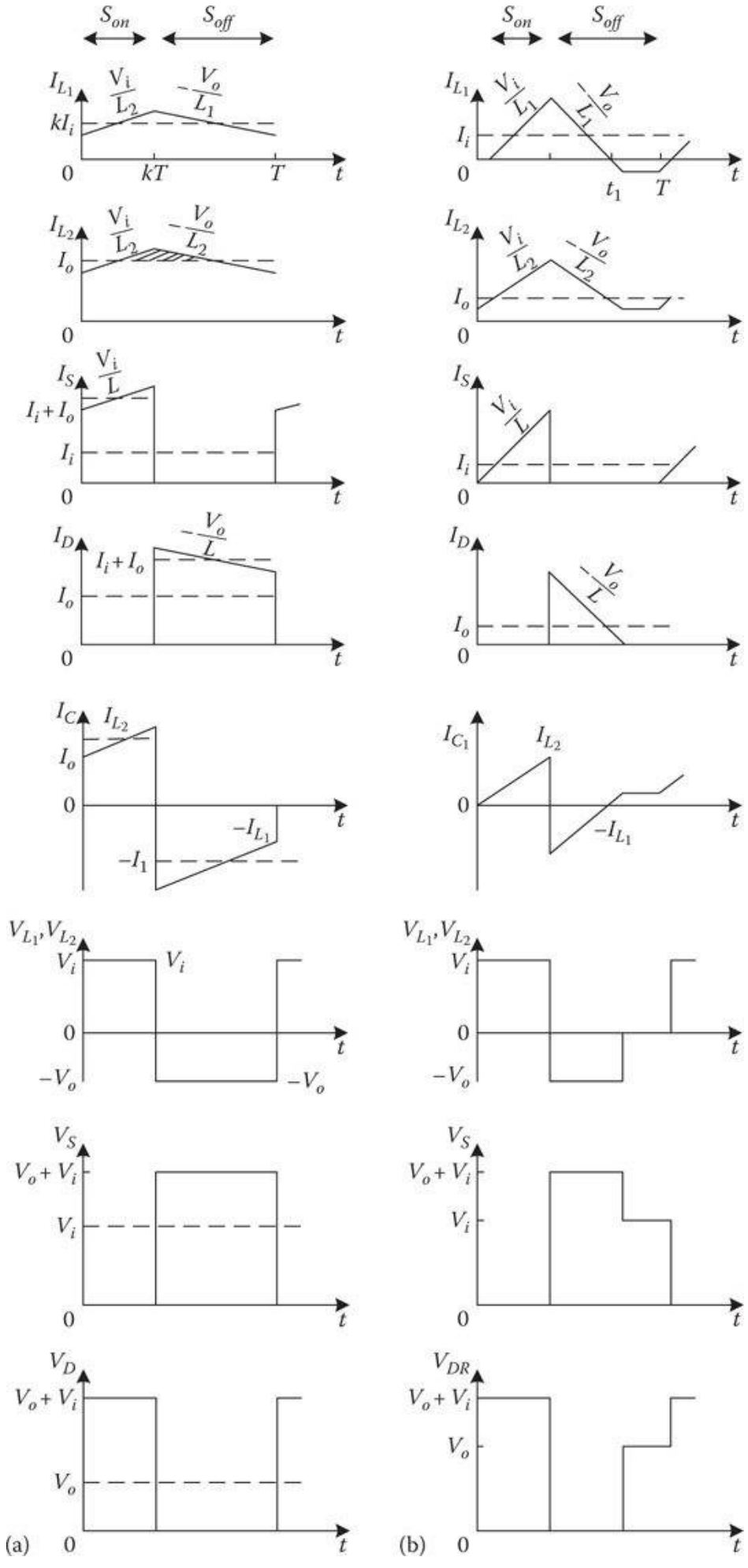
2.3.1.2 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.12.

Current i_{L_1} increases and is supplied by V_i during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L_1} = \frac{kTV_i}{L_1}$$

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FIGURE 2.12
Some voltage and current waveforms of elementary circuit. (a) CCM operation. (b) DCM operation.

Considering Equation 2.73, the variation ratio of the current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_i}{2L_1 I_i} = \frac{1-k}{2M_E}\frac{R}{fL_1} \tag{2.78}$$

Current i_{L_2} increases and is supplied by the voltage $(V_i + V_C - V_o) = V_i$ during switch-on. It decreases and is inversely biased by $-V_o$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L_2} = \frac{kTV_i}{L_2} \tag{2.79}$$

Considering Equation 2.72, the variation ratio of current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{kTV_i}{2L_2 I_o} = \frac{k}{2M_E}\frac{R}{fL_2} \tag{2.80}$$

When switch is off, the freewheeling diode current $i_D = i_{L_1} + i_{L_2}$ and

$$\Delta i_D = \Delta i_{L_1} + \Delta i_{L_2} = \frac{kTV_i}{L_1} + \frac{kTV_i}{L_2} = \frac{kTV_i}{L} = \frac{(1-k)TV_o}{L} \tag{2.81}$$

Considering Equations 2.71 and 2.72, the average current in switch-off period is

$$I_D = I_{L_1} + I_{L_2} = \frac{I_o}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D/2}{I_D} = \frac{(1-k)^2 TV_o}{2LI_o} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2}\frac{R}{2fL} \tag{2.82}$$

The peak-to-peak variation of v_C is

$$\Delta v_C = \frac{Q_+}{C} = \frac{1-k}{C}TI_i$$

Considering Equation 2.77, the variation ratio of v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{(1-k)TI_i}{2CV_o} = \frac{k}{2}\frac{1}{fCR} \tag{2.83}$$

If $L_1 = L_2 = 1$ mH, $C = C_o = 20$ μF, $R = 10\ \Omega$, $f = 50$ kHz, and $k = 0.5$,, we get that $\xi_1 = \xi_2 = 0.05$, $\zeta = 0.025$, and $\rho = 0.025$. Therefore, the variations of i_{L_1}, i_{L_2},, and v_C are

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small.

In order to investigate the variation of output voltage v_0, we have to calculate the charge variation on the output capacitor C_0, because $Q = C_0V_0$ and $\Delta Q = C_0\Delta v_0$.

ΔQ is caused by Δi_{L_2} and corresponds to the *area* of the triangle with the *height* of half of Δi_{L_2} and the *width* of half of the repeating period $T/2$, which is shown in Figure 2.12. Considering Equation 2.79,

$$\Delta Q = \frac{1}{2}\frac{\Delta i_{L_2}}{2}\frac{T}{2} = \frac{T}{8}\frac{kTV_i}{L_2}$$

Thus, the half peak-to-peak variation of output voltage v_o and v_{C_O} is

$$\frac{\Delta v_o}{2} = \frac{\Delta Q}{2C_o} = \frac{kT^2V_i}{16C_oL_2}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{kT^2}{16C_oL_2}\frac{V_i}{V_o} = \frac{k}{16M_E}\frac{1}{f^2C_oL_2} \tag{2.84}$$

If $L_2 = 1$ mH, $C_o = 20$ μF, $f = 50$ kHz, and $k = 0.5$, we obtain that $\varepsilon = 0.00125$. Therefore, the output voltage V_o is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and $I_o = V_o/R$.

2.3.1.3 Instantaneous Values of Currents and Voltages

Referring to Figure 2.12, the instantaneous values of the currents and voltages are listed as follows:

$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o + V_i & \text{for } kT < t \le T \end{cases} \tag{2.85}$$

$$v_D = \begin{cases} V_i + V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.86}$$

$$v_{L_1} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -V_o & \text{for } kT < t \le T \end{cases} \tag{2.87}$$

$$v_{L_2} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -V_o & \text{for } kT < t \le T \end{cases} \tag{2.88}$$

$$i_i = i_S = \begin{cases} i_{L_1}(0) + i_{L_2}(0) + \dfrac{V_i}{L}t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.89}$$

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$$i_{L_1} = \begin{cases} i_{L_1}(0) + \dfrac{V_i}{L_1} t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.90}$$

$$i_{L_2} = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t & \text{for } 0 < t \le kT \\ i_{L_2}(kT) - \dfrac{V_o}{L_2}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.91}$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_{L_1}(kT) + i_{L_2}(kT) - \dfrac{V_o}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.92}$$

$$i_C \approx \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) + \dfrac{V_o}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.93}$$

$$i_{C_o} \approx \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t - I_o & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) + \dfrac{V_o}{L_1}(t - kT) - I_o & \text{for } kT < t \le T \end{cases} \tag{2.94}$$

where

$$i_{L_1}(0) = \frac{kI_o}{1-k} - \frac{(1-k)V_o}{2fL_1}$$

$$i_{L_1}(kT) = \frac{kI_o}{1-k} + \frac{(1-k)V_o}{2fL_1}$$

$$i_{L_2}(0) = I_o - \frac{(1-k)V_o}{2fL_2}$$

$$i_{L_2}(kT) = I_o + \frac{(1-k)V_o}{2fL_2}$$

2.3.1.4 Discontinuous Conduction Mode

Referring to Figure 2.10d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

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$$\frac{k^2}{M_E^2}\frac{R}{2fL} \geq 1$$

or

$$M_E \leq k\sqrt{\frac{R}{2fL}} = k\sqrt{\frac{z_N}{2}} \tag{2.95}$$

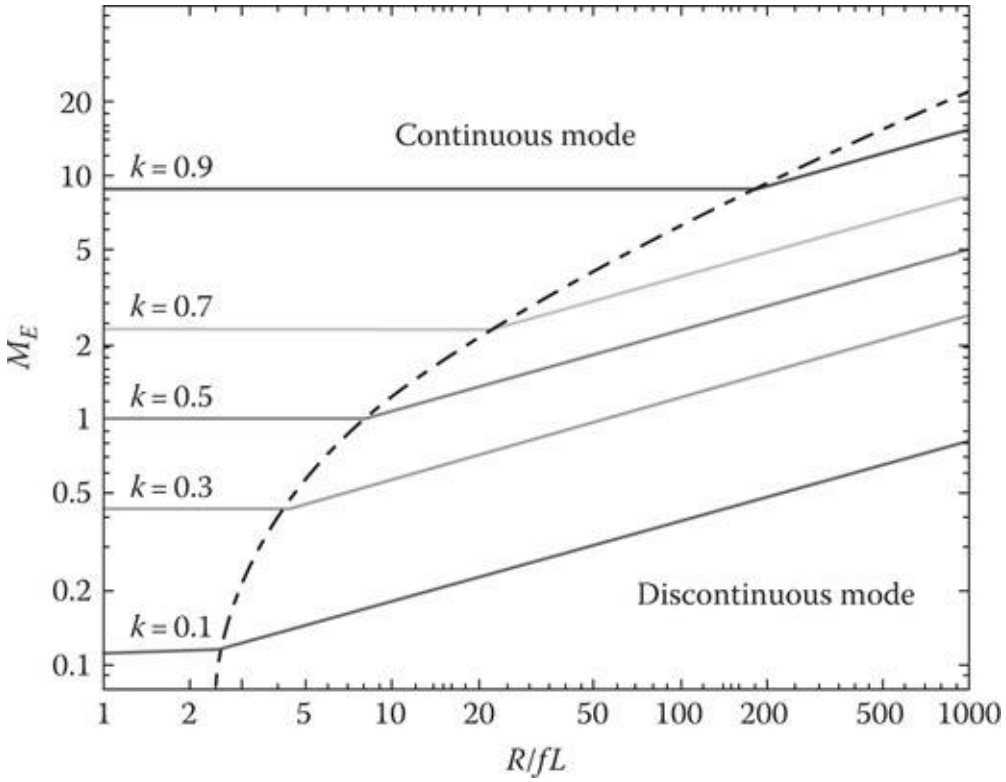


FIGURE 2.13
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$.

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.13. It can be seen that the boundary curve is a monorising function of the parameter k.

In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - 1k)m_E]T$, where m_E is the *filling efficiency*, and it is defined as

$$m_E = \frac{1}{\zeta} = \frac{M_E^2}{k^2\dfrac{R}{2fL}} \tag{2.96}$$

Considering Equation 2.95, therefore $0 < m_E < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_E T$, for the current i_L

$$kTV_i = (1 - k)m_E TV_C$$

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or

$$V_C = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{R}{2fL} V_i \quad \text{with} \quad \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

and for the current i_{Lo}

$$kT(V_i + V_C - V_o) = (1-k)m_E T V_o$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{R}{2fL} V_i \quad \text{with} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \tag{2.97}$$

that is, the output voltage will linearly increase when load resistance R increases. The output voltage versus the normalized load $z_N = R/fL$ is shown in Figure 2.13. It can be seen that larger load resistance R may cause higher output voltage in DCM.

2.3.1.5 Stability Analysis

Stability analysis is of vital importance for any converter circuit. Considering the various methods including the Bode plot, the root-locus method in s-plane is used for this analysis. According to the circuit network and control system theory, the transfer functions in s-domain for switch-on and switch-off are obtained:

$$G_{on} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{on} = \frac{sCR}{s^3 CC_o L_2 R + s^2 CL_2 + s(C+C_o)R + 1} \tag{2.98}$$

$$G_{off} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{off} = \frac{sCR}{s^3 CC_o L_2 R + s^2 CL_2 + s(C+C_o)R + 1} \tag{2.99}$$

where s is the Laplace operator.

From these equations in Laplace transform, it can be seen that the elementary converter is a third-order control circuit. The zero is determined by the equations where the numerator is equal to zero, and the poles are determined by the equation where the denominator is equal to zero. There is a zero at original point (0, 0) and three poles located in the left-hand half plane in Figure 2.14 so that this converter is stable.

Since the equations to determine the poles are the equations with all positive real coefficients, according to the *Gauss theorem*, the three poles are one negative real pole and a pair of conjugate complex poles with negative real part. When the load resistance R increases and tends toward infinity, the three poles move. The real pole goes to the original point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles located on the image axis. Assuming $C = C_o$ and $L_1 = L_2\{L = L_1L_2/(L_1 + L_2)$ *or* $L_2 = 2L\}$, the pair of imaginary poles is given as follows:

$$s = \pm j\sqrt{\frac{C+C_o}{CC_oL_2}} = \pm j\sqrt{\frac{1}{CL}} = \pm j\omega_n \quad \text{for switch-on} \tag{2.100}$$

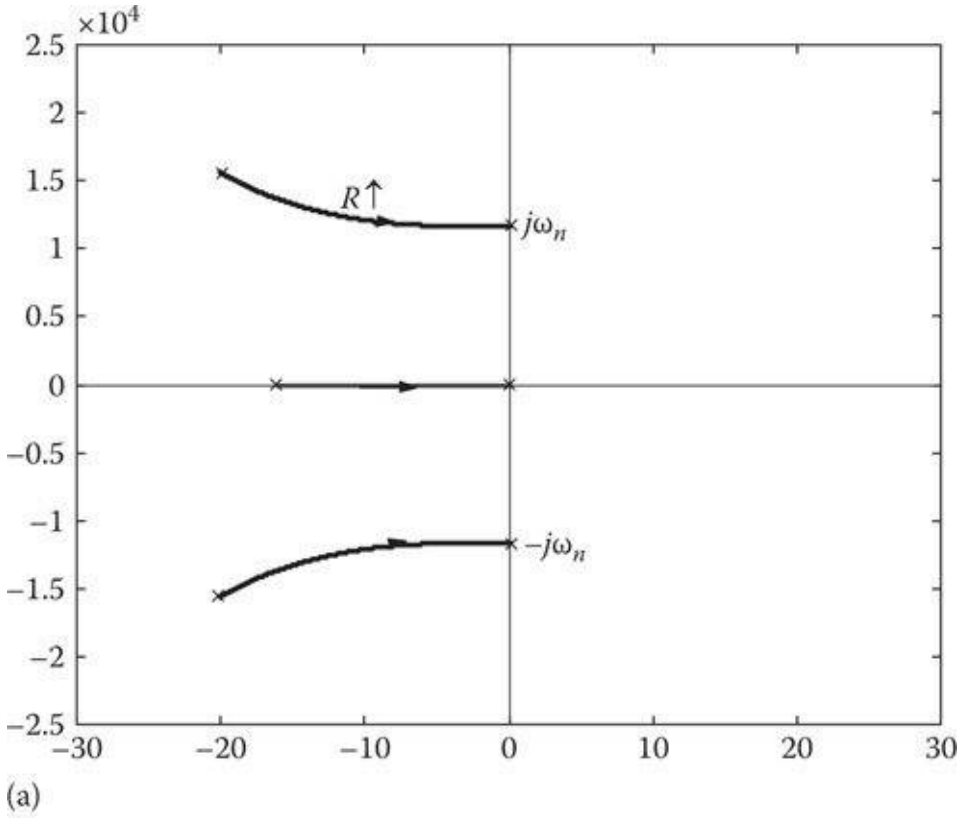
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$$s = \pm j\sqrt{\frac{C + C_o}{CC_oL_2}} = \pm j\sqrt{\frac{1}{CL}} = \pm j\omega_n \quad \text{for switch-off} \tag{2.101}$$

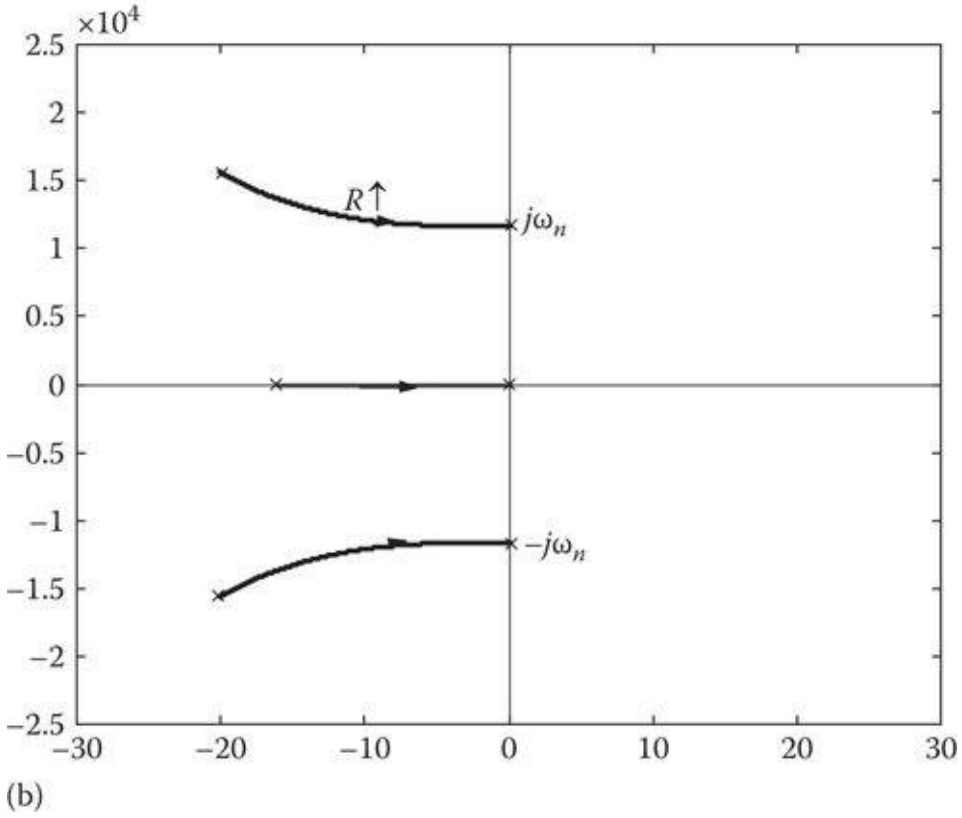
where $\omega_n = \sqrt{\frac{1}{CL}}$ is the converter normal angular frequency.

They are locating on the stability boundary. Therefore, the circuit works in the critical state. This fact is verified by experiment and computer simulation. When $R = \infty$, the output voltage v_o intends to be very high value. The output voltage V_o cannot be infinity because of the leakage current penetrating the capacitor C_o.

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(a)



(b)

FIGURE 2.14
Stability analysis of elementary circuit. (a) Switch-on. (b) Switch-off.

2.3.2 Self-Lift Circuit

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The self-lift circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.15, which is derived from the elementary circuit. Comparing to Figures 2.10 and 2.15, it can be seen that the pump circuit and filter are retained and there are only one more capacitor C_1 and one diode D_1 more, as a lift circuit added into the circuit. Capacitor C_1 functions to lift the capacitor voltage V_C by a source voltage V_{in}. Current $i_{C_1}(t) = \delta(t)$ is an exponential function. It has a large value at the power on moment, but it is small in the steady state because $V_{C_1} = V_{in}$.

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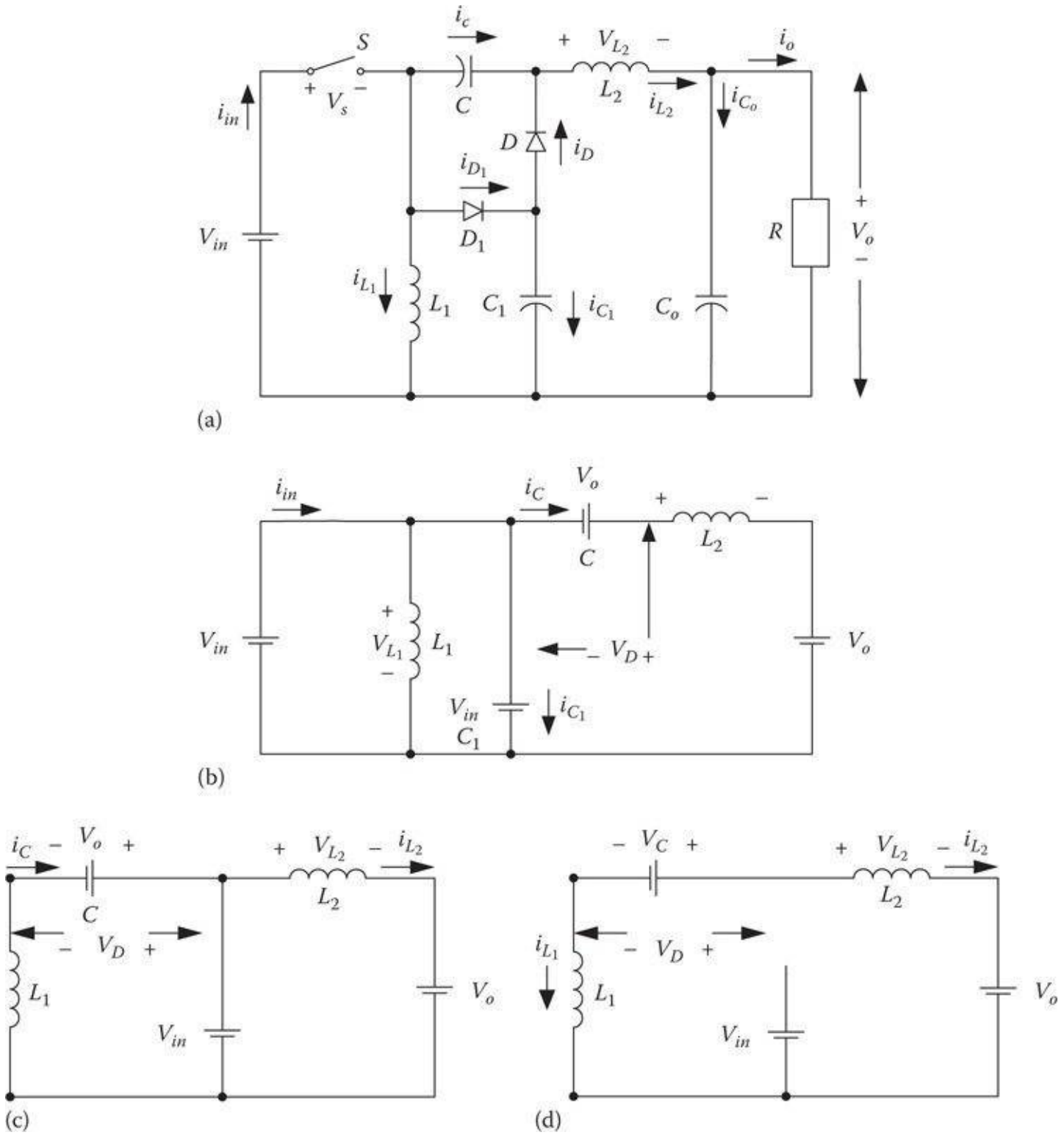


FIGURE 2.15
Self-lift circuit: (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

2.3.2.1 Circuit Description

When switch *S* is on, the instantaneous source current is $i_i = i_{L_1} + i_{L_2} + i_{C_1}$. Inductor L_1absorbs energy from the source. In the meantime, inductor L_2 absorbs energy from source and capacitor *C*. Both currents i_{L_1} and i_{L_2} increase, and C_1 is charged to $v_{C_1} = V_i$. When switch *S* is

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off, the instantaneous source current is $i_i = 0$. Current i_{L1} flows through capacitor C_1 and diode D to charge capacitor C. Inductor L_1 transfers its stored energy to capacitor C. In the meantime, current i_{L2} flows through the $(C_0 - R)$ circuit, capacitor C_1, and diode D to keep itself continuous. Both currents i_{L_1} and i_{L_2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-on and switch-off states are shown in Figure 2.15b, c and d. Assuming that capacitor C_1 is sufficiently large, voltage V_{C_1} is equal to V_i in steady state.

Current i_{L_1} increases in switch-on period kT and decreases in switch-off period $(1 - k)T$. The corresponding voltages applied across L_1 are V_i and $-(V_C - V_i)$, respectively. Therefore,

$$kTV_i = (1-k)T(V_C - V_i)$$

Hence,

$$V_C = \frac{1}{1-k}V_i \tag{2.102}$$

Current i_{L_2} increases in switch-on period kT and decreases in switch-off period $(1 - k)T$. The corresponding voltages applied across L_2 are $(V_i + V_C - V_0)$ and $-(V_0 - V_i)$. Therefore,

$$kT(V_C + V_i - V_o) = (1-k)T(V_o - V_i)$$

Hence,

$$V_o = \frac{1}{1-k}V_i \tag{2.103}$$

and the output current is

$$I_o = (1-k)I_i \tag{2.104}$$

Therefore, the voltage transfer gain in continuous mode is

$$M_S = \frac{V_o}{V_i} = \frac{1}{1-k} \tag{2.105}$$

The curve of M_S versus k is shown in Figure 2.16.

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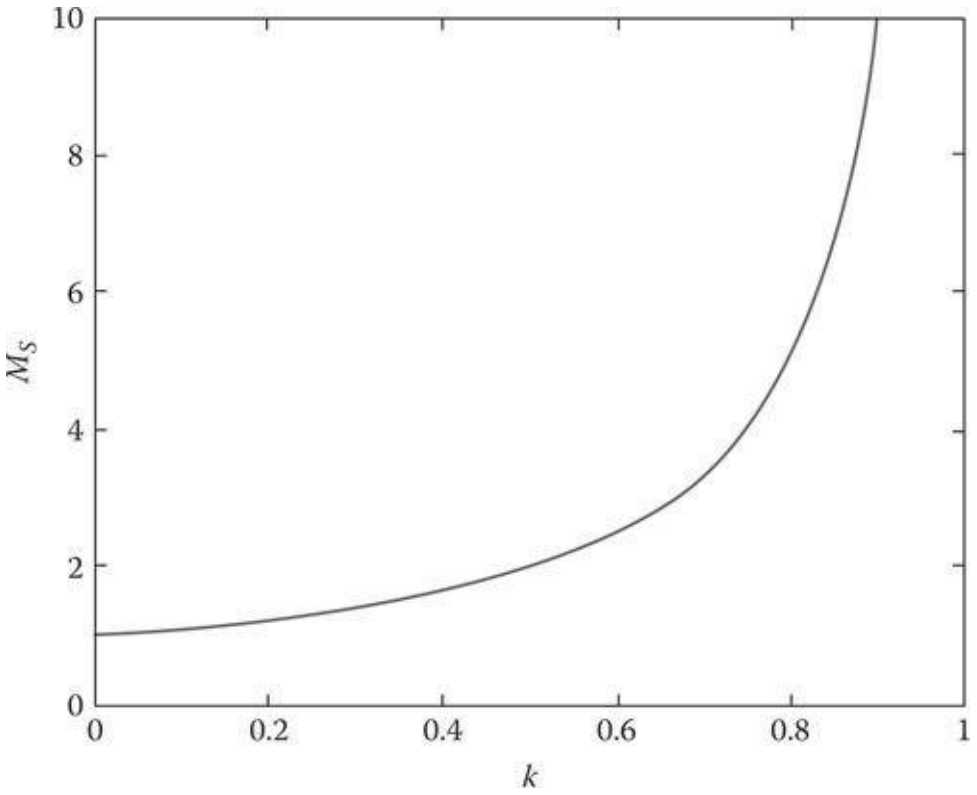


FIGURE 2.16
Voltage transfer gain M_S versus k.

2.3.2.2 Average Current I_{C_1} and Source Current I_S

During switch-off period $(1 - k)T$, current i_{C_1} is equal to $(i_{L_1} + i_{L_2})$, and the charge on capacitor C_1 decreases. During switch-on period kT, the charge increases, so its average current in switch-on period is

$$I_{C_1} = \frac{1-k}{k}(i_{L_1} + i_{L_2}) = \frac{1-k}{k}(I_{L_1} + I_{L_2}) = \frac{I_o}{k} \tag{2.106}$$

During switch-off period $(1 - k)T$, the source current i_i is 0, and in the switch-on period kT,

$$i_i = i_{L_1} + i_{L_2} + i_{C_1}$$

Hence,

$$I_i = k(i_{L_1} + i_{L_2} + i_{C_1}) = k(I_{L_1} + I_{L_2} + I_{C_1})$$

$$= k(I_{L_1} + I_{L_2})\left(1 + \frac{1-k}{k}\right) = k\frac{I_{L_2}}{1-k}\frac{1}{k} = \frac{I_o}{1-k} \tag{2.107}$$

2.3.2.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.17. Current i_{L_1} increases and is supplied by V_i during switch-on period kT. It

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decreases and is reversely biased by $-(V_C - V_i)$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L_1} = \frac{kTV_i}{L_1}$$

Hence, the variation ratio of current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kV_iT}{2kL_1I_i} = \frac{1-k}{2M_S}\frac{R}{fL_1} \tag{2.108}$$

Current i_{L_2} increases and is supplied by the voltage $(V_i + V_C - V_0) = V_i$ in switch-on period kT. It decreases and is inversely biased by $-(V_C - V_i)$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L_2} = \frac{kTV_i}{L_2}$$

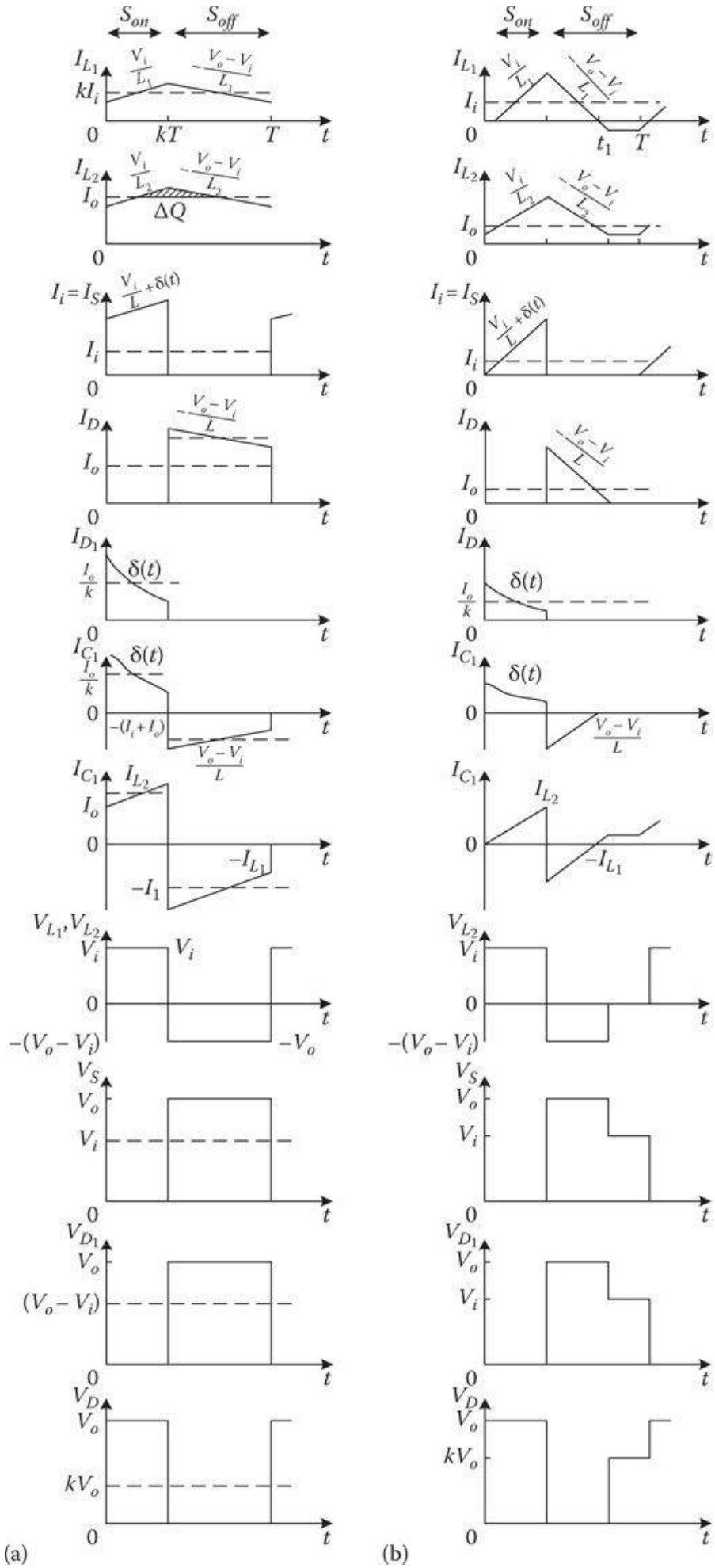
Thus, the variation ratio of current i_{L2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{kV_iT}{2L_2I_o} = \frac{k}{2M_S}\frac{R}{fL_2} \tag{2.109}$$

When switch is off, the freewheeling diode current $(I_{L_1} + I_{L_2})$ and

$$\Delta i_D = \Delta i_{L_1} + \Delta i_{L_2} = \frac{kTV_i}{L} = \frac{k(1-k)V_o}{L}T \tag{2.110}$$

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FIGURE 2.17
Some voltage and current waveforms of self-lift circuit. (a) CCM operation. (b) DCM operation.

Considering Equations 2.71 and 2.72,

$$I_D = I_{L_1} + I_{L_2} = \frac{I_o}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D/2}{I_D} = \frac{k(1-k)^2 TV_o}{2LI_o} = \frac{k}{M_S^2}\frac{R}{2fL} \tag{2.111}$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_+}{C} = \frac{(1-k)TI_{L_1}}{C} = \frac{1-k}{C}kTI_i$$

Hence, its variation ratio is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{(1-k)^2 kI_i T}{2CV_i} = \frac{k}{2fCR} \tag{2.112}$$

The charge on capacitor C_1 increases during switch-on and decreases during switch-off period $(1-k)T$ by the current $(I_{L_1} + I_{L_2})$. Therefore, its peak-to-peak variation is

$$\Delta v_{C_1} = \frac{(1-k)T(I_{L_1} + I_{L_2})}{C_1} = \frac{I_o}{fC_1}$$

Considering $V_{C_1} = V_i$, the variation ratio of voltage v_{C_1} is

$$\sigma = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{I_o}{2fC_1V_i} = \frac{M_S}{2fC_1R} \tag{2.113}$$

If $L_1 = L_2 = 1$ mH, $C = C_1 = C_o = 20$ μF, $R = 40\ \Omega$, $f = 50$ kHz, and $k = 0.5$, we obtain that $\xi_1 = 0.1$, $\xi_2 = 0.1$, $\zeta = 0.1$, $\rho = 0.006$, and $\sigma = 0.025$. Therefore, the variations of i_{L_1}, i_{L_2}, v_{C_1}, and v_C are small.

Considering Equations 2.84 and 2.105, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{kT^2}{16C_oL_2}\frac{V_i}{V_o} = \frac{k}{16M_S}\frac{1}{f^2C_oL_2} \tag{2.114}$$

If $L_2 = 1$ mH, $C_o = 20$ μE, $f = 50$ kHz, and $k = 0.5$, $\varepsilon = 0.0006$. Therefore, the output voltage V_o is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and $I_o = V_o/R$.

2.3.2.4 Instantaneous Value of the Currents and Voltages

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Referring to Figure 2.17, the instantaneous values of the currents and voltages are listed here:

$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.115}$$

$$v_D = \begin{cases} V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.116}$$

$$v_{D_1} = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.117}$$

$$v_{L_1} = v_{L_2} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -(V_o - V_i) & \text{for } kT < t \le T \end{cases} \tag{2.118}$$

$$i_i = i_S = \begin{cases} i_{L_1}(0) + i_{L_2}(0) + \delta(t) + \dfrac{V_i}{L} t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.119}$$

$$i_{L_1} \begin{cases} i_{L_1}(0) + \dfrac{V_i}{L_1} t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o - V_i}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.120}$$

$$i_{L_2} = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t & \text{for } 0 < t \le kT \\ i_{L_2}(kT) - \dfrac{V_o - V_i}{L_2}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.121}$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_{L_1}(kT) + i_{L_2}(kT) - \dfrac{V_o - V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.122}$$

$$i_{D_1} = \begin{cases} \delta(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.123}$$

$$i_C = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o - V_i}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.124}$$

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$$i_{C_1} = \begin{cases} \delta(t) & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) - i_{L_2}(kT) + \dfrac{V_o - V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.125}$$

$$i_{C_o} = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2}t - I_o & \text{for } 0 < t \le kT \\ i_{L_2}(kT) - \dfrac{V_o - (2 + \dfrac{k}{1-k})V_i}{L_2}(t - kT) - I_o & \text{for } kT < t \le T \end{cases} \tag{2.126}$$

where

$$i_{L_1}(0) = kI_i - kV_i/2fL_1$$

$$i_{L_1}(kT) = kI_i + kV_i/2fL_1$$

$$i_{L_2}(0) = I_o - kV_o/2fML_2$$

$$i_{L_2}(kT) = I_o + kV_o/2fML_2$$

2.3.2.5 Discontinuous Conduction Mode

Referring to Figure 2.15d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

$$\frac{k}{M_S^2}\frac{R}{2fL} \ge 1$$

or

$$M_S \le \sqrt{k}\sqrt{\frac{R}{2fL}} = \sqrt{k}\sqrt{\frac{z_N}{2}} \tag{2.127}$$

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.18. It can be seen that the boundary curve has a minimum value of 1.5 at $k = 1/3$.

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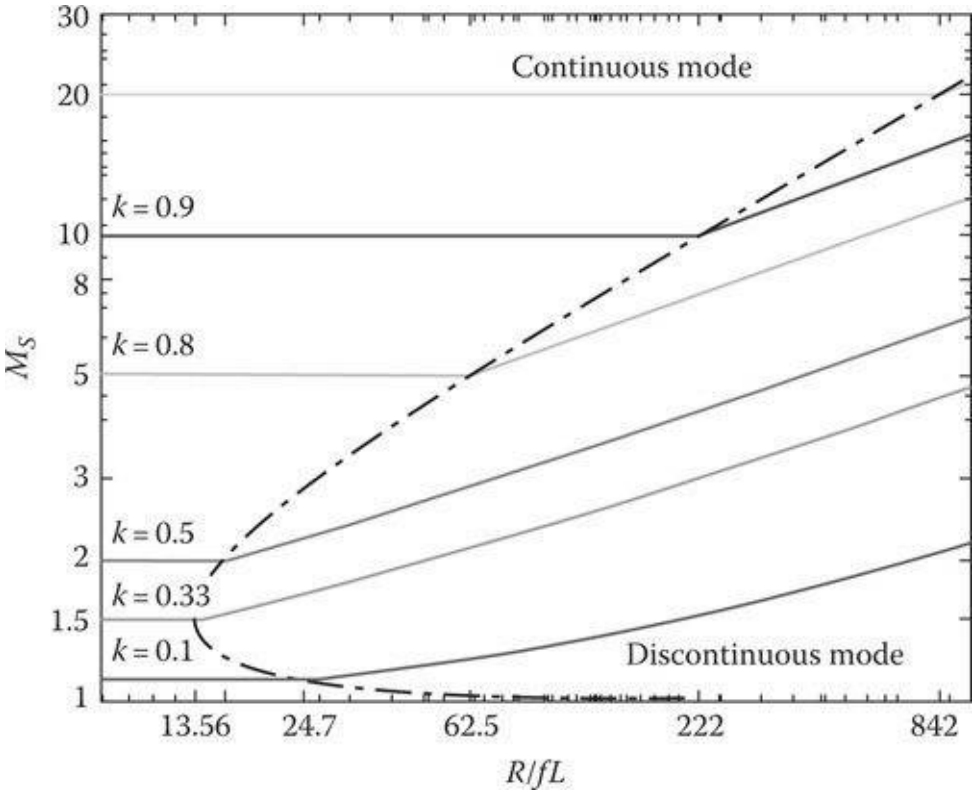


FIGURE 2.18
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$.

In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - 0\ k)m_S]T$, where m_S is the *filling efficiency*, and it is defined as

$$m_S = \frac{1}{\zeta} = \frac{M_S^2}{k\dfrac{R}{2fL}} \tag{2.128}$$

Considering Equation 2.127, therefore $0 < m_S < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_S T$, for the current i_L

$$kTV_i = (1 - k)m_S T(V_C - V_i)$$

or

$$V_C = \left[1 + \frac{k}{(1-k)m_S}\right]V_i = \left[1 + k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

and for the current i_{L_o}

$$kT(V_i + V_C - V_o) = (1 - k)m_S T(V_o - V_i)$$

Therefore, the output voltage in discontinuous mode is

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$$V_o = \left[1 + \frac{k}{(1-k)m_S}\right] V_i = \left[1 + k^2(1-k)\frac{R}{2fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \tag{2.129}$$

that is, the output voltage will linearly increase while load resistance R increases. The output voltage V_0 versus the normalized load $z_N = R/fL$ is shown in Figure 2.18. Larger load resistance R causes higher output voltage in DCM.

2.3.2.6 Stability Analysis

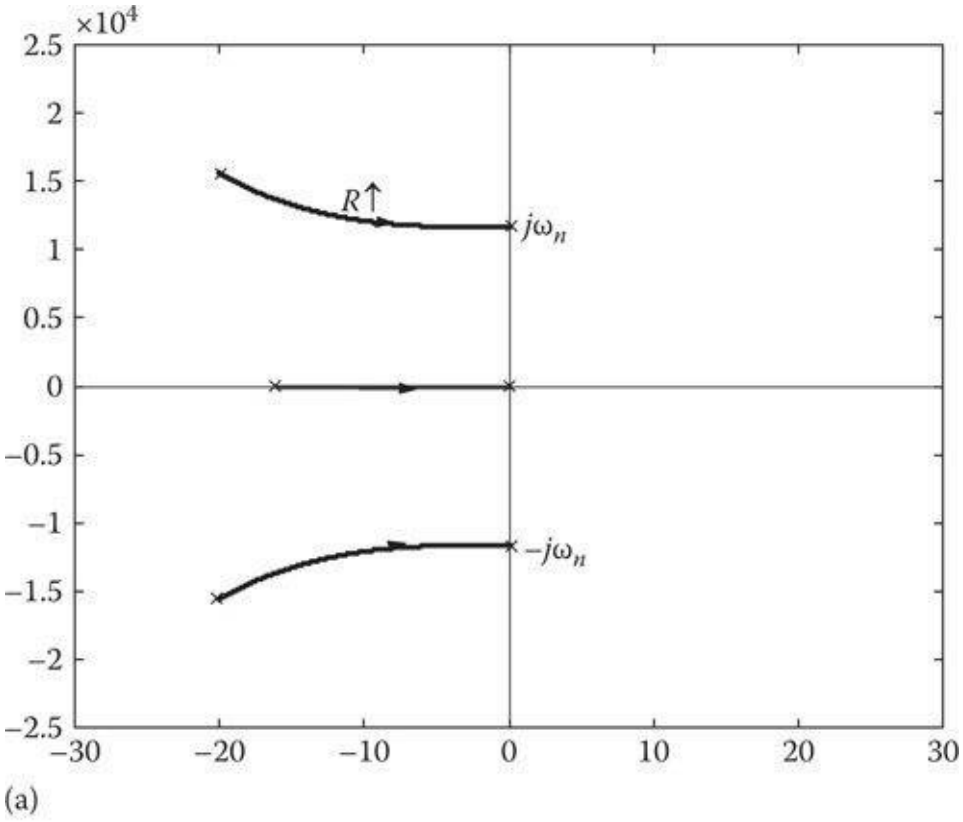
Taking the root-locus method in s-plane for stability analysis, the transfer functions in s-domain for switch-on and switch-off are obtained:

$$G_{on} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{on} = \frac{sCR}{s^3 CC_o L_2 R + s^2 CL_2 + s(C + C_o)R + 1} \tag{2.130}$$

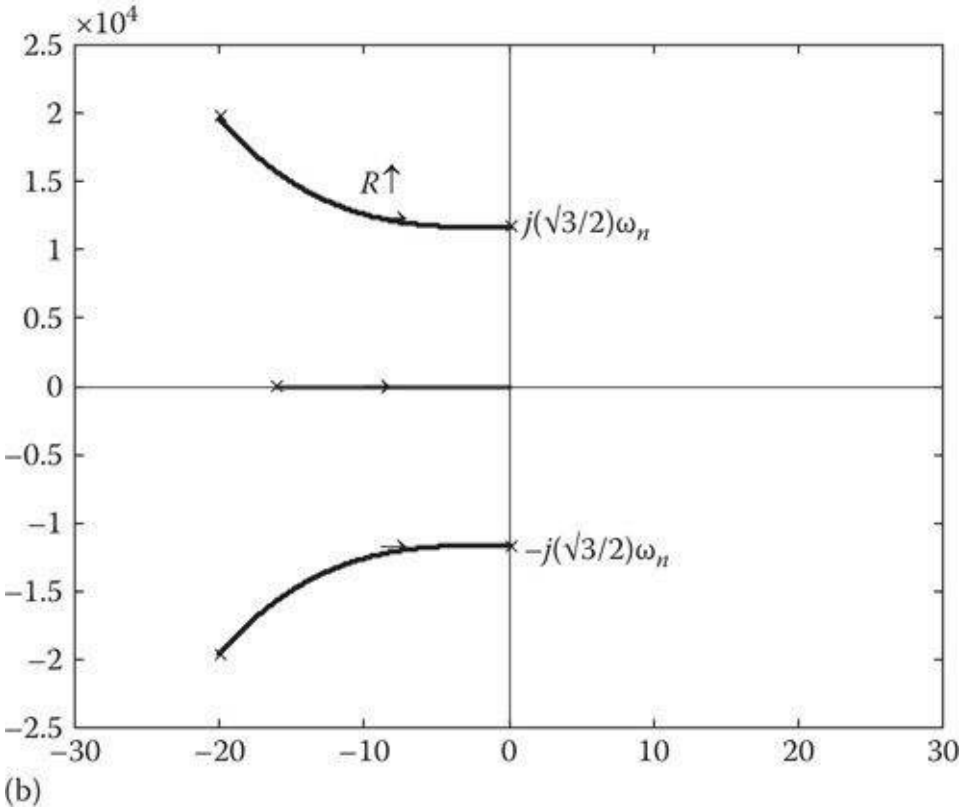
$$G_{off} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{off} = \frac{sCR}{s^3 (C + C_1)C_o L_2 R + s^2 (C + C_1)L_2 + s(C + C_1 + C_o)R + 1} \tag{2.131}$$

where s is the Laplace operator. From Equations 2.130 and 2.131 in Laplace transform, it can be seen that the self-lift converter is a third-order control circuit. The zero is determined by the equation when the numerator is equal to zero, and the poles are determined by the equation when the denominator is equal to zero. There is a zero at origin point (0, 0) and three poles located in the left-hand half plane in Figure 2.19 so that the self-lift converter is stable.

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(a)



(b)

FIGURE 2.19
Stability analysis of self-lift circuit. (a) Switch-on. (b) Switch-off.

Since the equations to determine the poles are the equations with all positive real coefficients, according to the *Gauss theorem*, the three poles are one negative real pole and a

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pair of conjugate complex poles with negative real part. When the load resistance R increases and tends toward infinity, the three poles move. The real pole goes to the origin point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles locating on the image axis. Assuming $C = C_1 = C_o$ and $L_1 = L_2$ $\{L = L_1 L_2/(L_1 + L_2)$ *or* $L_2 = 2L\}$, the pair of imaginary poles are

$$s = \pm j\sqrt{\frac{C + C_o}{CC_oL_2}} = \pm j\sqrt{\frac{1}{CL}} = \pm j\omega_n \quad \text{for switch-on} \tag{2.132}$$

$$s = \pm j\sqrt{\frac{C + C_1 + C_o}{(C + C_o)C_oL_2}} = \pm j\sqrt{\frac{3}{4CL}} = \pm j\frac{\sqrt{3}}{2}\omega_n \quad \text{for switch-off} \tag{2.133}$$

where $\omega_n = \sqrt{1/CL}$ is the self-lift converter normal angular frequency. They are locating on the stability boundary. Therefore, the circuit works in the critical state. This fact is verified by experiment and computer simulation. When $R = \infty$, the output voltage v_o intends to be very high value. The output voltage V_o cannot be infinity because of the leakage current penetrating the capacitor C_o.

2.3.3 Re-Lift Circuit

The re-lift circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.20, which is derived from the self-lift circuit. It consists of two static switches S and S_1; three diodes D, D_1, and D_2; three inductors L_1, L_2, and L_3; and four capacitors C, C_1, C_2, and C_o. From Figures 2.10, 2.15, and 2.20, it can be seen that the pump circuit and filter are retained and there are one capacitor C_2, one inductor L_3, and one diode D_2 added into the re-lift circuit. The lift circuit consists of D_1–C_1–L_3–D_2–S_1–C_2. Capacitors C_1 and C_2 perform characteristics to lift the capacitor voltage V_C by twice of source voltage V_i L_3 performs the function as a ladder joint to link the two capacitors C_1 and C_2 and lift the capacitor voltage V_C up. Current $i_{C_1}(t) = \delta_1(t)$ and $i_{C_2}(t) = \delta_2(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C_1} = v_{C_2} = V_i$ in steady state.

2.3.3.1 Circuit Description

When switches S and S_1 turn on, the source instantaneous current $i_I = i_{L_1} + i_{L_2} + i_{C_1} + i_{L_3} + i_{C_2}$. Inductors L_1 and L_3 absorb energy from the source. In the meantime, inductor L_2 absorbs energy from source and capacitor C. Three currents i_{L_1}, i_{L_3}, and i_{L_2} increase. When switches S and S_1 turn off, source current $i_i = 0$. Current i_{L_1} flows through capacitor C_1, inductor L_3, capacitor C_2, and diode D to charge capacitor C. Inductor L_1 transfers its stored energy to capacitor C. In the meantime, current i_{L_2} flows through the (C_o – R) circuit, capacitor C_1, inductor L_3, capacitor C_2, and diode D to keep itself continuous. Both currents i_{L_1} and i_{L_2} decrease. In order to analyze the circuit working procession, the equivalent circuits in switch-

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on and switch-off states are shown in Figure 2.20b, c and d. Assuming capacitor C_1 and C_2 are sufficiently large, and the voltages V_{C1} and V_{C2} across them are equal to $V_i$in steady state.

Voltage v_{L_3} is equal to V_i during switch-on. The peak-to-peak variation of current i_{L_3} is

$$\Delta i_{L_3} = \frac{V_i kT}{L_3} \tag{2.134}$$

This variation is equal to the current reduction when switch-off. Suppose its voltage is $-V_{L_3-off}$ So

$$\Delta i_{L_3} = \frac{V_{L_3-off}(1-k)T}{L_3}$$

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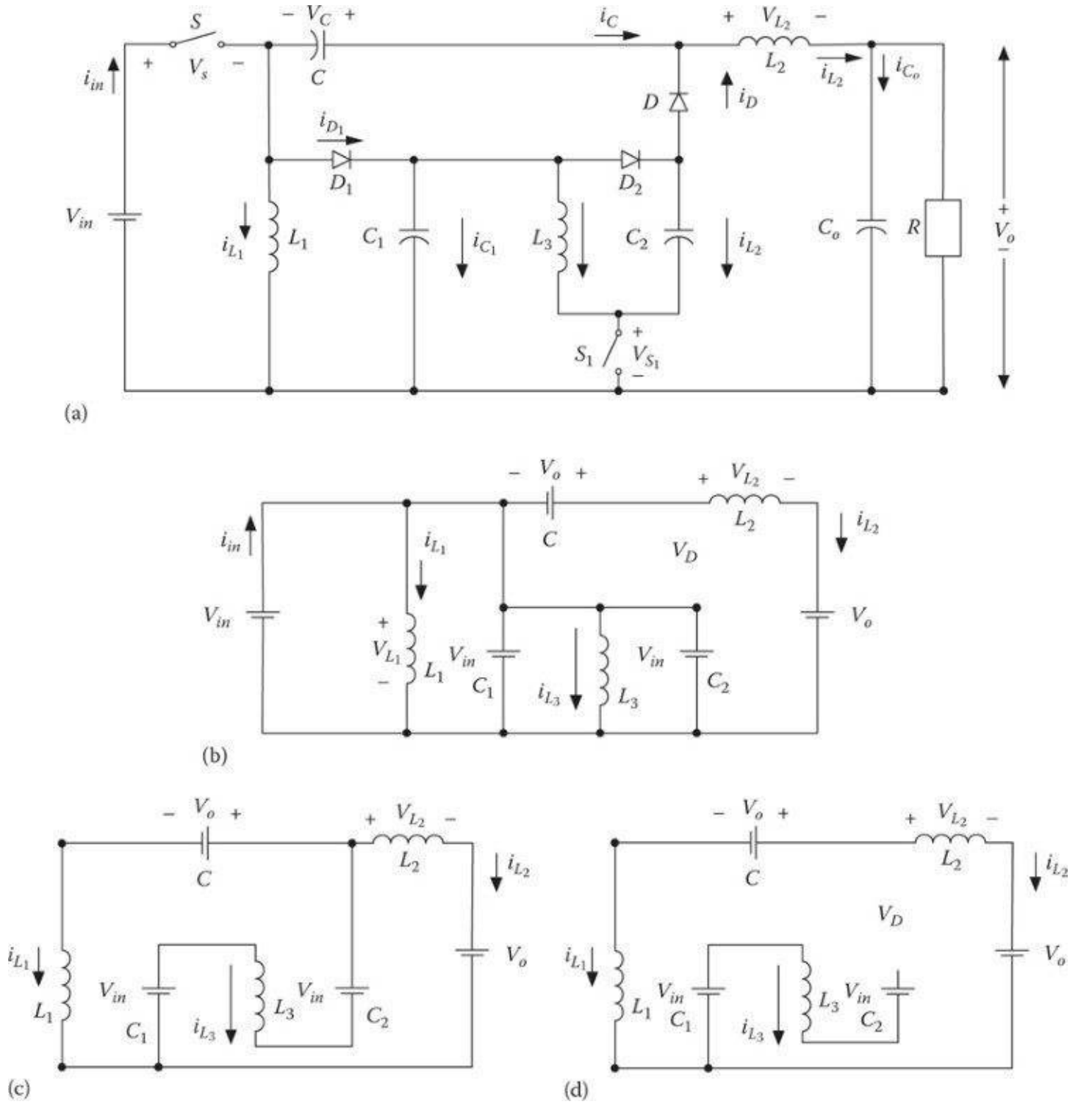


FIGURE 2.20
Re-lift circuit: (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

Thus, during switch-off, the voltage drop across inductor L_3 is

$$V_{L_3-off} = \frac{k}{1-k} V_i \tag{2.135}$$

Current i_{L_1} increases in switch-on period kT and decreases in switch-off period $(1 - k)T$. The corresponding voltages applied across L_1 are V_i and $-(V_C - 2V_i - V_{L_3-off})$. Therefore,

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$$kTV_i = (1-k)T(V_C - 2V_i - V_{L3-off})$$

Hence,

$$V_C = \frac{2}{1-k} V_i \tag{2.136}$$

Current i_{L_2} increases in switch-on period kT, and it decreases in switch-off period $(1 - k)T$. The corresponding voltages applied across L_2 are $(V_i + V_C - V_o)$ and $-(V_o - 2V_i - V_{L3-off})$. Therefore,

$$kT(V_C + V_i - V_o) = (1-k)T(V_o - 2V_i - V_{L3-off})$$

Hence,

$$V_o = \frac{2}{1-k} V_i \tag{2.137}$$

and the output current is

$$I_o = \frac{1-k}{2} I_i \tag{2.138}$$

The voltage transfer gain in continuous mode is

$$M_R = \frac{V_o}{V_i} = \frac{2}{1-k} \tag{2.139}$$

The curve of M_R versus k is shown in Figure 2.21.

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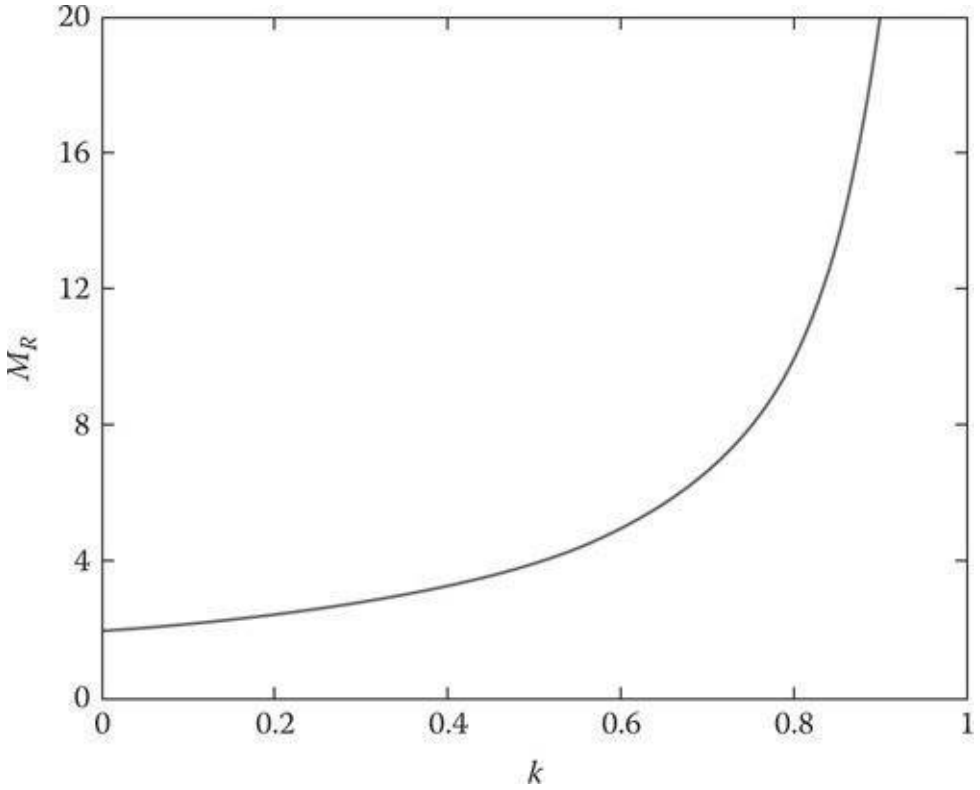


FIGURE 2.21
Voltage transfer gain M_R versus k.

2.3.3.2 Other Average Currents

Considering Equation 2.71,

$$I_{L_1} = \frac{k}{1-k} I_o = \frac{k}{2} I_i \tag{2.140}$$

and

$$I_{L_3} = I_{L_1} + I_{L_2} = \frac{1}{1-k} I_o \tag{2.141}$$

Currents i_{C_1} and i_{C_2} are equal to $(i_{L_1} + i_{L_2})$ during *switch-off* period $(1 - k)T$, and the charges on capacitors C_1 and C_2 decrease, that is,

$$i_{C_1} = i_{C_2} = (i_{L_1} + i_{L_2}) = \frac{1}{1-k} I_o$$

The charges increase during *switch-on* period kT, so their average currents are

$$I_{C_1} = I_{C_2} = \frac{1-k}{k}(I_{L_1} + I_{L_2}) = \frac{1-k}{k}\left(\frac{k}{1-k} + 1\right) I_o = \frac{I_o}{k} \tag{2.142}$$

During switch-off, the source current i_i is 0, and in the switch-on period kT, it is

$$i_i = i_{L_1} + i_{L_2} + i_{C_1} + i_{L_3} + i_{C_2}$$

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Hence,

$$I_i = ki_i = k(I_{L_1} + I_{L_2} + I_{C_1} + I_{L_3} + I_{C_2}) = k\left[2(I_{L_1} + I_{L_2}) + 2I_{C_1}\right]$$

$$= 2k(I_{L_1} + I_{L_2})\left(1 + \frac{1-k}{k}\right) = 2k\frac{I_{L_2}}{1-k}\frac{1}{k} = \frac{2}{1-k}I_o \tag{2.143}$$

2.3.3.3 Variations of Currents and Voltages

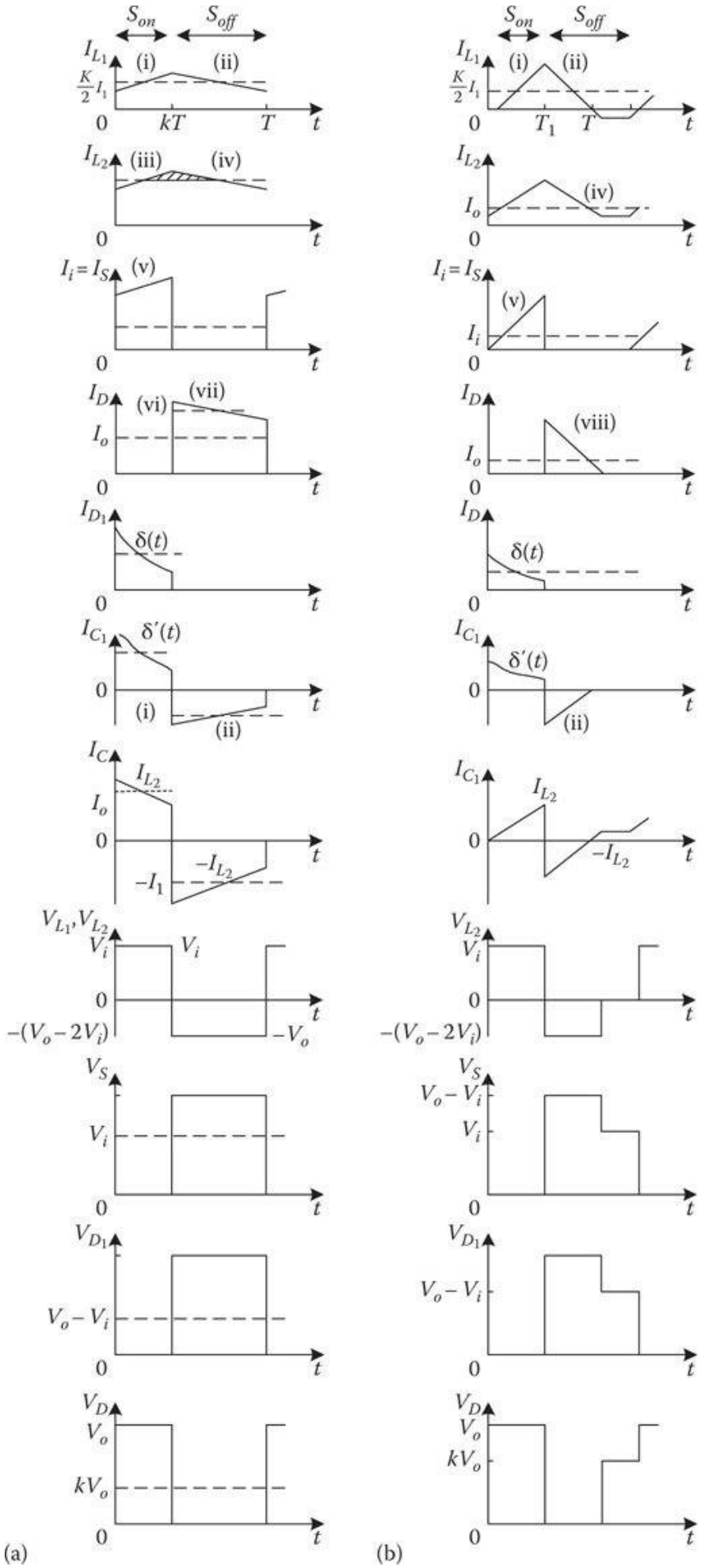
To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.22. Current i_{L_1} increases and is supplied by V_i during switch-on period kT. It decreases and is reversely biased by $-(V_C - 2V_i - V_{L_3})$ during switch-off period $(1 - k)T$. Therefore, its peak-to-peak variation is

$$\Delta i_{L_1} = \frac{kTV_i}{L_1}$$

Considering Equation 2.140, the variation ratio of current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kV_iT}{kL_1I_i} = \frac{1-k}{2M_R}\frac{R}{fL_1} \tag{2.144}$$

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FIGURE 2.22
Some voltage and current waveforms of re-lift circuit: (a) CCM operation. (b) DCM operation.

Current i_{L_2} increases and is supplied by the voltage $(V_i + V_C - V_o) = V_i$ during switch-on period kT. It decreases and is reversely biased by $-(V_o - 2V_i - V_{L_3})$ during switch-off. Therefore, its peak-to-peak variation is

$$\Delta i_{L_2} = \frac{kTV_i}{L_2}$$

Considering Equation 2.72, the variation ratio of current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{kTV_i}{2L_2 I_o} = \frac{k}{2M_R}\frac{R}{fL_2} \tag{2.145}$$

When switch is off, the freewheeling diode current is $i_D = i_{L_1} + i_{L_2}$ and

$$\Delta i_D = \Delta i_{L_1} + \Delta i_{L_2} = \frac{kTV_i}{L} = \frac{k(1-k)V_o}{2L}T \tag{2.146}$$

Considering Equations 2.71 and 2.72,

$$I_D = I_{L_1} + I_{L_2} = \frac{I_o}{1-k}$$

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D/2}{I_D} = \frac{k(1-k)^2 TV_o}{4LI_o} = \frac{k(1-k)R}{2M_R fL} = \frac{k}{M_R^2}\frac{R}{fL} \tag{2.147}$$

Considering Equations 2.134 and 2.141, the variation ratio of current i_{L_3} is

$$\chi_1 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{kV_i T}{2L_3\frac{1}{1-k}I_o} = \frac{k}{M_R^2}\frac{R}{fL_3} \tag{2.148}$$

If $L_1 = L_2 = 1$ mH, $L_3 = 0.5$ mH, $R = 160\ \Omega$, $f = 50$ kHz, and $k = 0.5$, we obtain that $\xi_1 = 0.2$, $\xi_2 = 0.2$, $\zeta = 0.1$, and $\chi_1 = 0.2$ Therefore, the variations of i_{L_1}, i_{L_2} and i_{L_3} are small.

The peak-to-peak variation of v_C is

$$\Delta v_C = \frac{Q_+}{C} = \frac{1-k}{C}TI_{L_1} = \frac{k(1-k)}{2C}TI_i$$

Considering Equation 2.136, the variation ratio is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{k(1-k)TI_i}{4CV_o} = \frac{k}{2fCR} \tag{2.149}$$

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The charges on capacitors C_1 and C_2 increase during switch-on period kT and decrease during switch-off period $(1 - k)T$ by the current $(I_{L_1} + I_{L_2})$. Therefore, their peak-to-peak variations are

$$\Delta v_{C_1} = \frac{(1-k)T(I_{L_1} + I_{L_2})}{C_1} = \frac{(1-k)I_i}{2C_1 f}$$

$$\Delta v_{C_2} = \frac{(1-k)T(I_{L_1} + I_{L_2})}{C_2} = \frac{(1-k)I_i}{2C_2 f}$$

Considering $V_{C_1} = V_{C_2} = V_i$ the variation ratios of voltages V_{C_1} and V_{C_2} are

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{(1-k)I_i}{4fC_1V_i} = \frac{M_R}{2fC_1R} \tag{2.150}$$

$$\sigma_2 = \frac{\Delta v_{C_2}/2}{V_{C_2}} = \frac{(1-k)I_i}{4V_iC_2f} = \frac{M_R}{2fC_2R} \tag{2.151}$$

Considering Equation 2.84, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{kT^2}{16C_oL_2}\frac{V_i}{V_o} = \frac{k}{16M_R}\frac{1}{f^2C_oL_2} \tag{2.152}$$

If $C = C_1 = C_2 = C_o = 20$ μF, $L_2 = 1$ mH, $R = 160$ Ω, $f = 50$ kHz, and $k = 0.5$, we obtain that $\rho = 0.0016$, $\sigma_1 = \sigma_2 = 0.0125$, and $\varepsilon = 0.0003$ The ripples of v_C, v_{C_1}, v_{C_2}, and v_{C_o} are small. Therefore, the output voltage v_o is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and $I_0 = V_0/R$.

2.3.3.4 Instantaneous Value of the Currents and Voltages

Referring to Figure 2.22, the instantaneous current and voltage values are listed here:

$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.153}$$

$$v_D = \begin{cases} V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.154}$$

$$v_{D_1} + v_{D_2} = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.155}$$

$$v_{L_3} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -\dfrac{k}{1-k}V_i & \text{for } kT < t \le T \end{cases} \tag{2.156}$$

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$$v_{L_1} = v_{L_2} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -\left[V_o - \left(2 - \dfrac{k}{1-k}\right)V_i\right] & \text{for } kT < t \le T \end{cases} \tag{2.157}$$

$$i_i = i_S = \begin{cases} i_{L_1}(0) + i_{L_2}(0) + i_{L_3}(0) + \delta_1(t) + \delta_2(t) + \dfrac{V_i}{L}t + \dfrac{V_i}{L_3}t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.158}$$

$$i_{L_1} = \begin{cases} i_{L_1}(0) + \dfrac{V_i}{L_1}t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right)V_i}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.159}$$

$$i_{L_2} = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2}t & \text{for } 0 < t \le kT \\ i_{L_2}(kT) - \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right)V_i}{L_2}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.160}$$

$$i_{L_3} = \begin{cases} i_{L_3}(0) + \dfrac{V_i}{L_3}t & \text{for } 0 < t \le kT \\ i_{L_3}(kT) - \dfrac{\dfrac{k}{1-k}V_i}{L_3}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.161}$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_{L_1}(kT) + i_{L_2}(kT) - \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right)V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.162}$$

$$i_{D_1} = \begin{cases} \delta_1(t) + \delta_2(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.163}$$

$$i_{D_2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.164}$$

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$$i_C = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o - V_i}{L_1}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.165}$$

$$i_{C_1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) - i_{L_2}(kT) + \dfrac{V_o - \left(2 + \dfrac{k}{1-k}\right) V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.166}$$

$$i_{C_2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) - i_{L_2}(kT) + \dfrac{V_o - \left(2 + \dfrac{k}{1-k}\right) V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.167}$$

$$i_{C_o} = \begin{cases} i_{L_2}(0) + \dfrac{V_i}{L_2} t - I_o & \text{for } 0 < t \le kT \\ i_{L_2}(kT) - \dfrac{V_o - \left(2 + \dfrac{k}{1-k}\right) V_i}{L_2}(t - kT) - I_o & \text{for } kT < t \le T \end{cases} \tag{2.168}$$

where

$$i_{L_1}(0) = kI_i/2 - kV_i/2fL_1$$

$$i_{L_1}(kT) = kI_i/2 + kV_i/2fL_1$$

$$i_{L_2}(0) = I_o - kV_i/2fL_2$$

$$i_{L_2}(kT) = I_o + kV_i/2fL_2$$

$$i_{L_3}(0) = I_o + kI_i/2 - kV_i/2fL_3$$

$$i_{L_3}(kT) = I_o + kI_i/2 + kV_i/2fL_3$$

2.3.3.5 Discontinuous Conduction Mode

Referring to Figure 2.20d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

$$\frac{k}{M_R^2}\frac{R}{fL} \ge 1$$

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or

$$M_R \le \sqrt{k}\sqrt{\frac{R}{fL}} = \sqrt{k}\sqrt{z_N} \tag{2.169}$$

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.23. It can be seen that the boundary curve has a minimum value of 3.0 at $k = 1/3$.

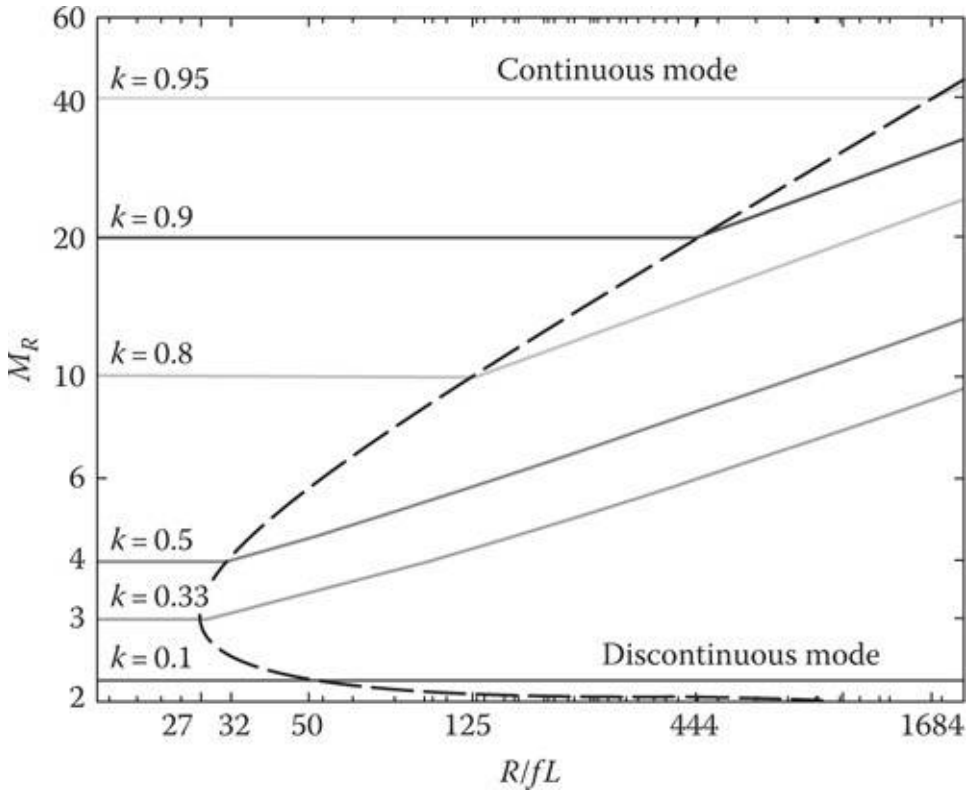


FIGURE 2.23
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$.

In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_R]T$, where m_R is the *filling efficiency*, and it is defined as

$$m_R = \frac{1}{\zeta} = \frac{M_R^2}{k\dfrac{R}{fL}} \tag{2.170}$$

Considering Equation 2.169, therefore $0 < m_R < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_RT$, for the current i_L

$$kTV_i = (1-k)m_RT\left(V_C - 2V_i - V_{L3-off}\right)$$

or

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$$V_C = \left[2 + \frac{k}{1-k} + \frac{k}{(1-k)m_R}\right] V_i = \left[2 + \frac{k}{1-k} + k^2(1-k)\frac{R}{4fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{fL}} \geq \frac{2}{1-k}$$

and for the current i_{L_o}

$$kT\left(V_i + V_C - V_o\right) = (1-k)m_R T\left(V_o - 2V_i - V_{L3-off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[2 + \frac{k}{1-k} + \frac{k}{(1-k)m_R}\right] V_i = \left[2 + \frac{k}{1-k} + k^2(1-k)\frac{R}{4fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{fL}} \geq \frac{2}{1-k} \tag{2.171}$$

that is, the output voltage will linearly increase when load resistance R increases. The output voltage versus the normalized load $z_N = R/fL$ is shown in Figure 2.23. Larger load resistance R may cause higher output voltage in discontinuous mode.

2.3.3.6 Stability Analysis

Stability analysis is of vital importance for any converter circuit. According to the circuit network and control systems theory, the transfer functions in s-domain for switch-on and switch-off states are obtained:

$$G_{on} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{on} = \frac{sCR}{s^3 L_2 C C_o R + s^2 L_2 C + s(C + C_o)R + 1} \tag{2.172}$$

$$G_{off} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{off}$$

$$= \frac{\dfrac{R}{1+sC_oR} sC \dfrac{s(C_1+C_2)+s^3L_3C_1C_2}{s^2C_1C_2}}{sC\dfrac{s(C_1+C_2)+s^3L_3C_1C_2}{s^2C_1C_2}\dfrac{R+sL_2+s^2L_2C_oR}{1+sC_oR} + \dfrac{s(C_1+C_2)+s^3L_3C_1C_2}{s^2C_1C_2} + \dfrac{R+sL_2+s^2L_2C_oR}{1+sC_oR}}$$

$$= \frac{sCR[(C_1+C_2)+s^2L_3C_1C_2]}{sC[(C_1+C_2)+s^2L_3C_1C_2][R+sL_2+s^2L_2C_oR]+(1+sC_oR)[(C_1+C_2)+s^2L_3C_1C_2] + sC_1C_2[R+sL_2+s^2L_2C_oR]} \tag{2.173}$$

where s is the Laplace operator. From Equations 2.172 and 2.173 in Laplace transform, we can see that the re-lift converter is a third-order control circuit for switch-on state and a fifth-order control circuit for switch-off state.

For the switch-on state, the zeros are determined by the equation when the numerator of Equation 2.172 is equal to zero, and the poles are determined by the equation when the denominator of Equation 2.172 is equal to zero. There is a zero at the origin point (0, 0). Since the equation to determine the poles is the equation with all positive real coefficients, according to the *Gauss theorem*, the three poles are one negative real pole (p_3) and a pair of

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conjugate complex poles with negative real part ($p_{1,2}$). The three poles are located in the left half plane in Figure 2.24 so that the re-lift converter is stable.

When the load resistance R increases and intends toward infinity, the three poles move. The real pole goes to the origin point and eliminates with the zero. The pair of conjugate complex poles becomes a pair of imaginary poles locating on the imaginary axis. Assuming that all capacitors have the same capacitance C and $L_1 = L_2\{L = L_1L_2/(L_1 + L_2)$ *or* $L_2 = 2L\}$ and $L_3 = L$, Equation 2.172 becomes

$$G_{on} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{on} = \frac{1}{s^2 L_2 C_o + \dfrac{C + C_o}{C}} = \frac{1}{2s^2 LC + 2} \tag{2.174}$$

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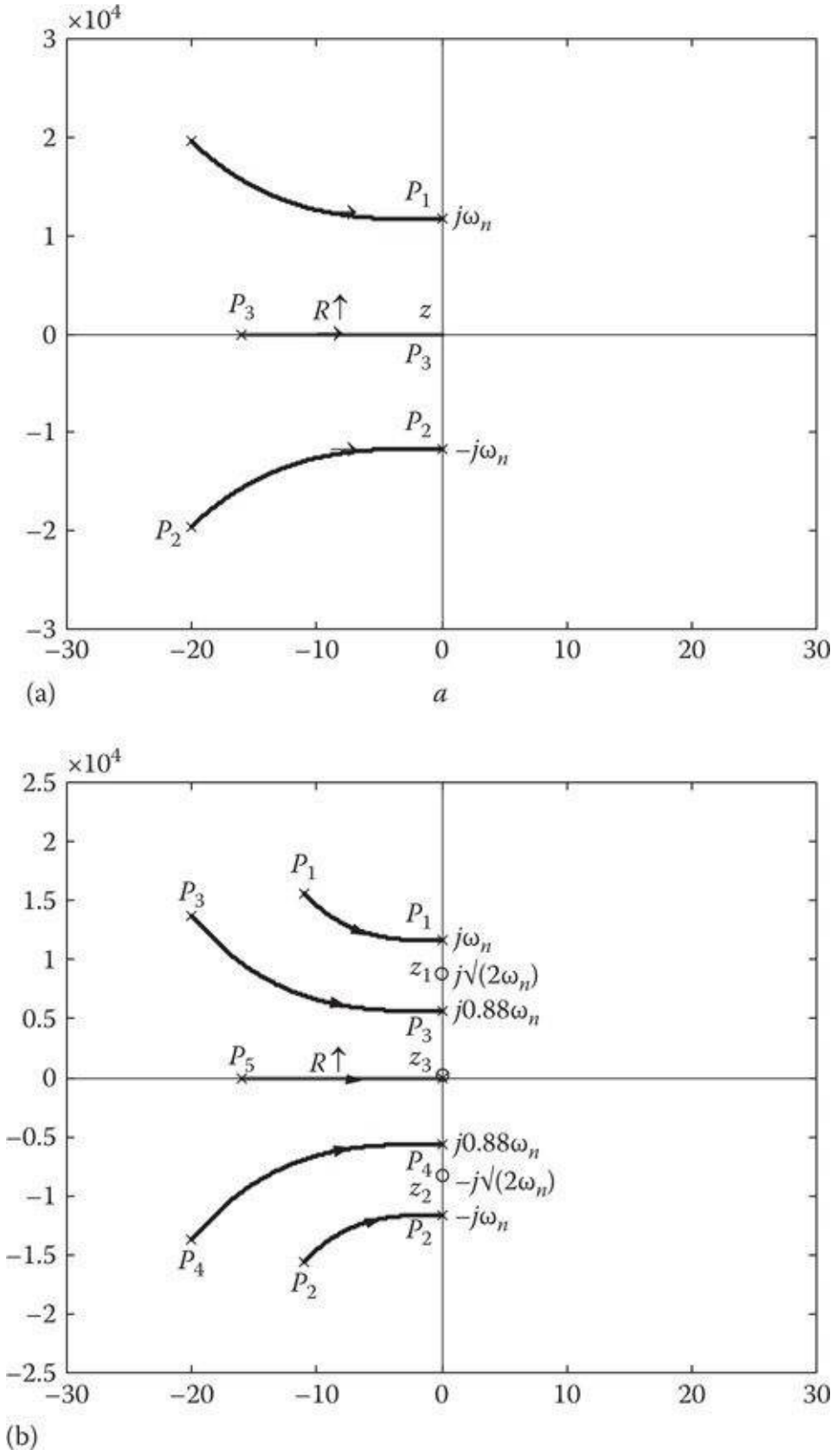


FIGURE 2.24
Stability analysis of re-lift circuit. (a) Switch-on. (b) Switch-off.

and the pair of imaginary poles is

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$$p_{1,2} = \pm j\sqrt{\frac{C + C_0}{L_2 C C_0}} = \pm j\sqrt{\frac{1}{LC}} = \pm j\omega_n \quad \text{poles for switch-on} \tag{2.175}$$

where $\omega_n = (LC)^{-1/2}$ is the re-lift converter normal angular frequency.

For the switch-off state, the zeros are determined by the equation when the numerator of Equation 2.173 is equal to zero, and the poles are determined by the equation when the denominator of Equation 2.173 is equal to zero. There are three zeros: one (z_3) at the origin point (0, 0) and two zeros ($z_{1,2}$) on the imaginary axis that are

$$z_{1,2} = \pm j\sqrt{\frac{C_1 + C_2}{L_3 C_1 C_2}} = \pm j\sqrt{\frac{2}{LC}} = \pm j\sqrt{2}\omega_n \quad \text{zeros for switch-off} \tag{2.176}$$

Since the equation to determine the poles is the equation with all positive real coefficients, according to the *Gauss theorem*, the five poles are one negative real pole (p_5) and two pairs of conjugate complex poles with negative real parts (p_{12} and $p_{3,4}$). There are five poles located in the left-hand half plane in Figure 2.24 so that the re-lift converter is stable. When the load resistance R increases and intends toward infinity, the five poles move. The real pole goes to the origin point and eliminates with the zero. The two pairs of conjugate complex poles become two pairs of imaginary poles locating on the imaginary axis. Assuming that all capacitors have the same capacitance C and $L_1 = L_2\{L = L_1 L_2/(L_1 + L_2)$ *or* $L_2 = 2L\}$ and $L_3 = L$, Equation 2.173 becomes

$$G_{off} = \left\{\frac{\delta V_o(s)}{\delta V_i(s)}\right\}_{off} = \frac{C(C_1 + C_2) + s^2 L_3 C C_1 C_2}{(CC_1 + CC_2 + C_1 C_2 + s^2 L_3 C C_1 C_2)(1 + s^2 L_2 C_o) + (C_o C_1 + C_o C_2 + s^2 L_3 C_o C_1 C_2)}$$

$$= \frac{2C^2 + s^2 LC^3}{(3C^2 + s^2 LC^3)(1 + 2s^2 LC) + (2C^2 + s^2 LC^3)} = \frac{2 + s^2 LC}{2s^4 L^2 C^2 + 8s^2 LC + 5} \tag{2.177}$$

and the two pairs of imaginary poles are

$$s^2 LC = \frac{-8 \pm \sqrt{64 - 40}}{4} = -2 \pm \frac{\sqrt{6}}{2} = \begin{cases} -3.225 \\ -0.775 \end{cases} \quad \text{poles for switch-off}$$

so that

$$p_{1,2} = \pm j1.8\omega_n \quad \text{and} \quad p_{3,4} = \pm j0.88\omega_n \tag{2.178}$$

For both states when R tends to infinity, all poles are locating on the stability boundary. Therefore, the circuit works in the critical state. From Equation 2.171, the output voltage will be infinity. This fact is verified by the experimental results and computer simulation results. When $R = \infty$, the output voltage v_o tends to be very high value. In this particular circuit since there is some leakage current across the capacitor C_o, the output voltage $v_o$cannot be infinity.

2.3.4 Multiple-Lift Circuits

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Referring to Figure 2.20a, it is possible to build multiple-lift circuits using the parts (L_3–C_2–S_1–D_2) multiple times. For example, in Figure 2.25, the parts (L_4–C_3–D_3–D_4) were added in the triple-lift circuit. Because the voltage at the point of the joint (L_4–C_3) is positive value and higher than that at the point of the joint (L_3–C_2), so that we can use a diode D_3 to replace the switch (S_2). For multiple-lift circuits, all further switches can be replaced by diodes. According to this principle, triple-lift circuit and quadruple-lift circuit were built as shown in Figures 2.25 and 2.28. In this book, it is not necessary to introduce the particular analysis and calculations one by one to the readers. However, their calculation formulae are shown in this section.

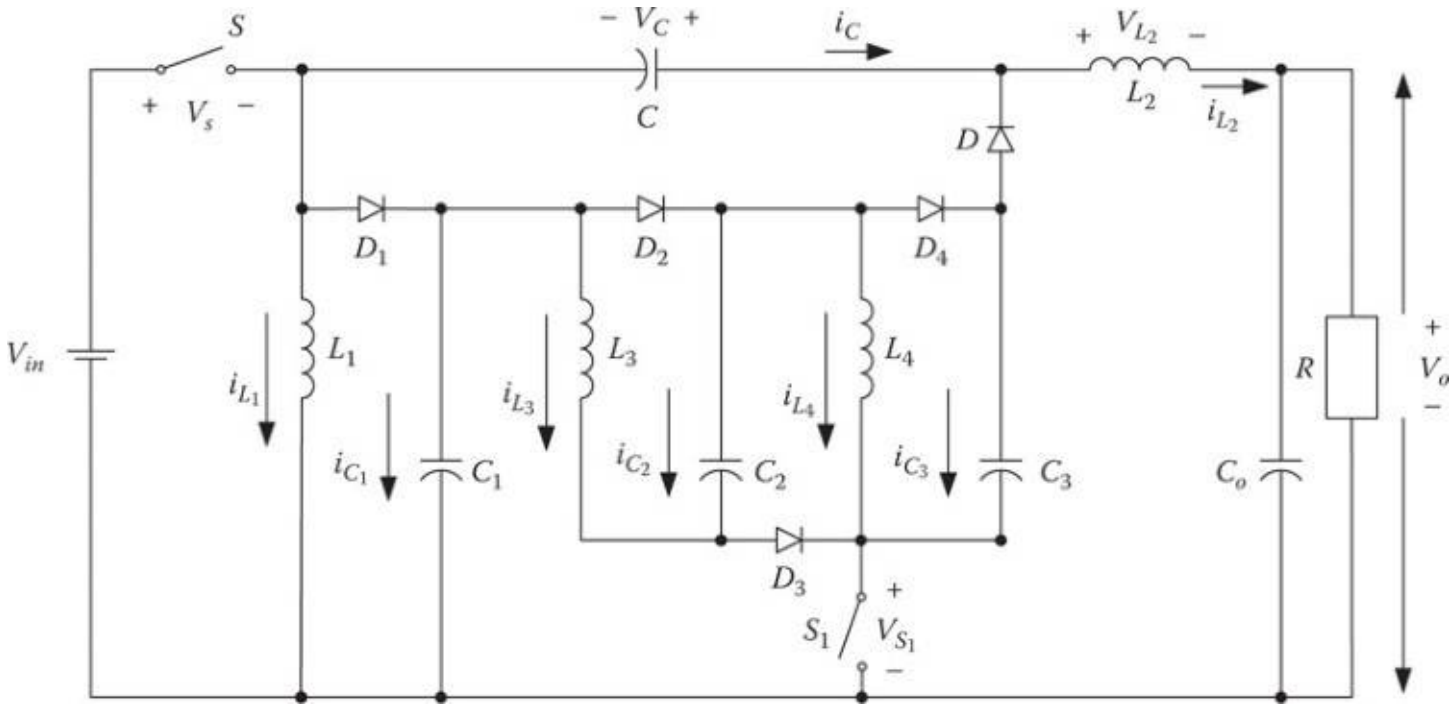


FIGURE 2.25
Triple-lift circuit.

2.3.4.1 Triple-Lift Circuit

A triple-lift circuit is shown in Figure 2.25, and it consists of two static switches S and S_1; four inductors L_1, L_2, L_3, and L_4; five capacitors C, C_1, C_2, C_3, and C_o; and five diodes. Capacitors C_1, C_2, and C_3 perform characteristics to lift the capacitor voltage V_C by three times the source voltage V_i. L_3 and L_4 perform the function as ladder joints to link the three capacitors C_1, C_2, and C_3 and lift the capacitor voltage V_C up. Currents $i_{C_1}(t)$, $i_{C_2}(t)$, and $i_{C_3}(t)$ (t) are exponential functions. They have large values at the moment of power on, but they are small because $v_{C_1} = v_{C_2} = v_{C_3} = V_i$ in steady state.

The output voltage and current are

$$V_o = \frac{3}{1-k} V_i \tag{2.179}$$

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and

$$I_o = \frac{1-k}{3} I_i \tag{2.180}$$

The voltage transfer gain in continuous mode is

$$M_T = \frac{V_o}{V_i} = \frac{3}{1-k} \tag{2.181}$$

The curve of M_T versus k is shown in Figure 2.26.

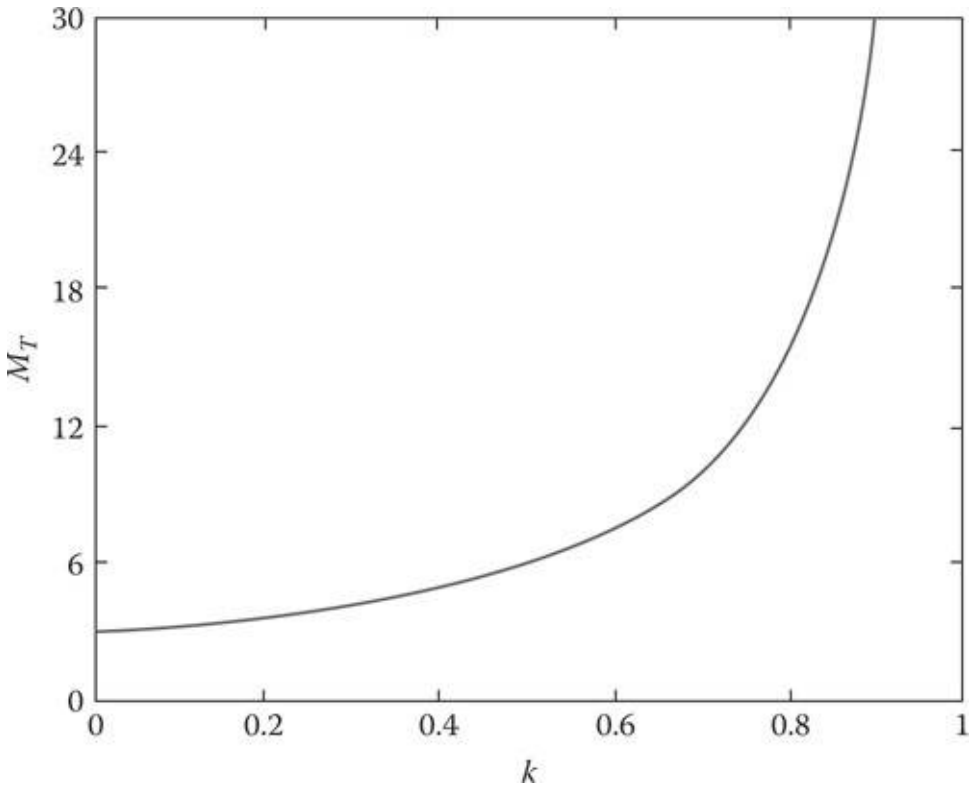


FIGURE 2.26
Voltage transfer gain M_T versus k.

Other average voltages are

$$V_C = V_o$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_i$$

Other average currents are

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$$I_{L_2} = I_o$$

$$I_{L_1} = \frac{k}{1-k} I_o$$

$$I_{L_3} = I_{L_4} = I_{L_1} + I_{L_2} = \frac{1}{1-k} I_o$$

The current variations are

$$\xi_1 = \frac{1-k}{2M_T} \frac{R}{fL_1} \quad \xi_2 = \frac{k}{2M_T} \frac{R}{fL_2} \quad \zeta = \frac{k(1-k)R}{2M_T fL} = \frac{k}{M_T^2} \frac{3R}{2fL}$$

$$\chi_1 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{kV_i T}{2L_3} \frac{1-k}{I_o} = \frac{k \frac{V_o}{M_T} T}{\frac{2}{1-k} L_3 I_o} = \frac{k}{M_T^2} \frac{3R}{2fL_3} \quad \chi_2 = \frac{k}{M_T^2} \frac{3R}{2fL_4}$$

The voltage variations are

$$\rho = \frac{k}{2fCR} \quad \sigma_1 = \frac{M_T}{2fC_1 R}$$

$$\sigma_2 = \frac{M_T}{2fC_2 R} \quad \sigma_3 = \frac{M_T}{2fC_3 R}$$

The variation ratio of output voltage v_C is

$$\varepsilon = \frac{k}{16M_T} \frac{1}{f^2 C_o L_2} \tag{2.182}$$

The output voltage ripple is very small.

The boundary between continuous mode and DCM is

$$M_T \le \sqrt{k} \sqrt{\frac{3R}{2fL}} = \sqrt{\frac{3kz_N}{2}} \tag{2.183}$$

This boundary curve is shown in Figure 2.27. Comparing with Equations 2.95, 2.165, 2.169, and 2.183, it can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to $k = 1/3$.

In discontinuous mode, the current i_D exists in the period between kT and $[k + (1 - k)m_T]T$, where m_T is the filling efficiency, that is,

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$$m_T = \frac{1}{\zeta} = \frac{M_T^2}{k\dfrac{3R}{2fL}} \tag{2.184}$$

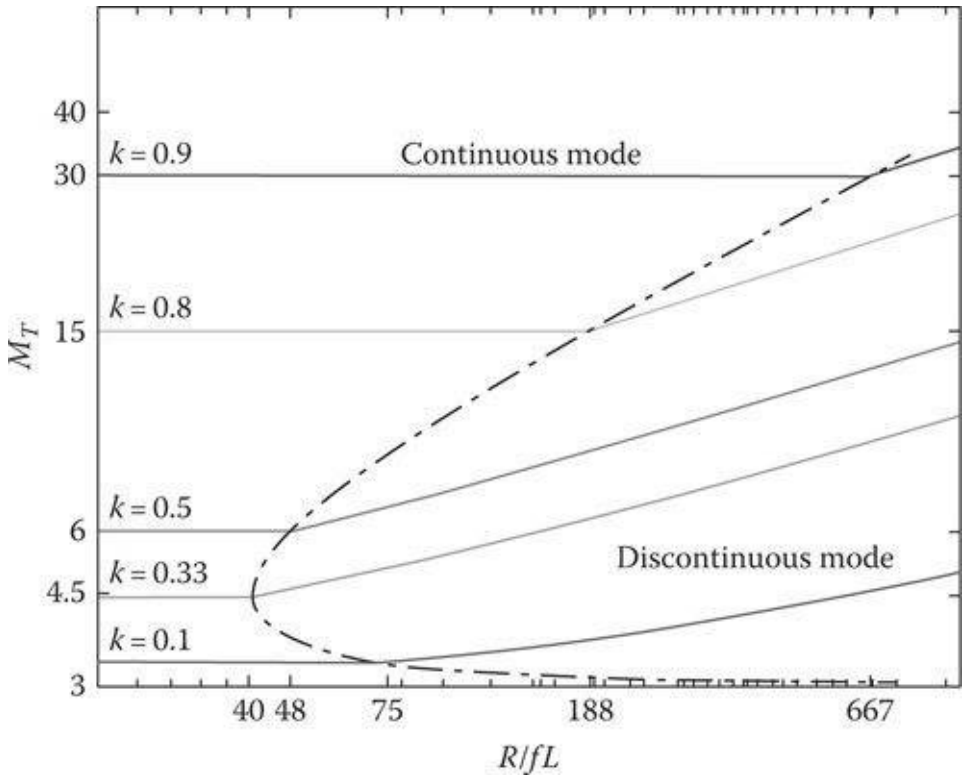


FIGURE 2.27
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$.

Considering Equation 2.183, therefore, $0 < m_T < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_T T$, for the current i_{L_1},

$$kTV_i = (1-k)m_T T\left(V_C - 3V_i - V_{L_3-off} - V_{L_4-off}\right)$$

or

$$V_C = \left[3 + \frac{2k}{1-k} + \frac{k}{(1-k)m_T}\right]V_i = \left[3 + \frac{2k}{1-k} + k^2(1-k)\frac{R}{6fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k}$$

and for the current iL_2,

$$kT\left(V_i + V_C - V_o\right) = (1-k)m_T T\left(V_o - 2V_i - V_{L_3-off} - V_{L_4-off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[3 + \frac{2k}{1-k} + \frac{k}{(1-k)m_T}\right]V_i = \left[3 + \frac{2k}{1-k} + k^2(1-k)\frac{R}{6fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k} \tag{2.185}$$

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that is, the output voltage will linearly increase when load resistance R increases, as shown in Figure 2.27.

2.3.4.2 Quadruple-Lift Circuit

A quadruple-lift circuit shown in Figure 2.28 consists of two static switches S and S_1; five inductors L_1, L_2, L_3, L_4, and L_5; six capacitors C, C_1, C_2, C_3, C_4, and C_o; and seven diodes. Capacitors C_1, C_2, C_3, and C_4 perform characteristics to lift the capacitor voltage V_C by four times the source voltage V_i. L_3, L_4, and L_5 perform the function as ladder joints to link the four capacitors C_1, C_2, C_3, and C_4 and lift the output capacitor voltage V_C up. Currents $i_{C_1}(t)$, $i_{C_2}(t)$, $i_{C_3}(t)$, and $i_{C_4}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C_1} = v_{C_2} = v_{C_3} = v_{C_4} = V_i$ in steady state.

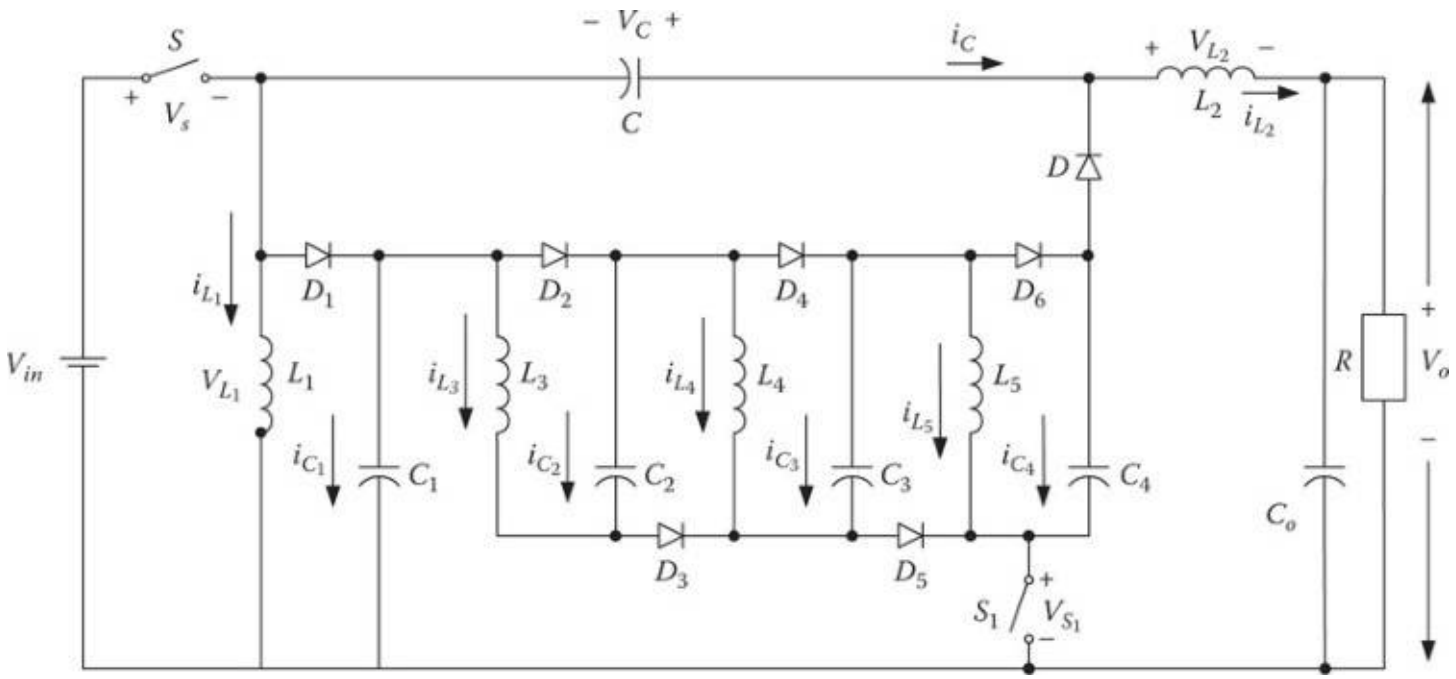


FIGURE 2.28
Quadruple-lift circuit.

The output voltage and current are

$$V_o = \frac{4}{1-k} V_i \tag{2.186}$$

and

$$I_o = \frac{1-k}{4} I_i \tag{2.187}$$

The voltage transfer gain in continuous mode is

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$$M_Q = \frac{V_o}{V_i} = \frac{4}{1-k} \tag{2.188}$$

The curve of M_Q versus k is shown in Figure 2.29.

Other average voltages are

$$V_C = V_o$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{C_4} = V_i$$

Other average currents are

$$I_{L_2} = I_o$$

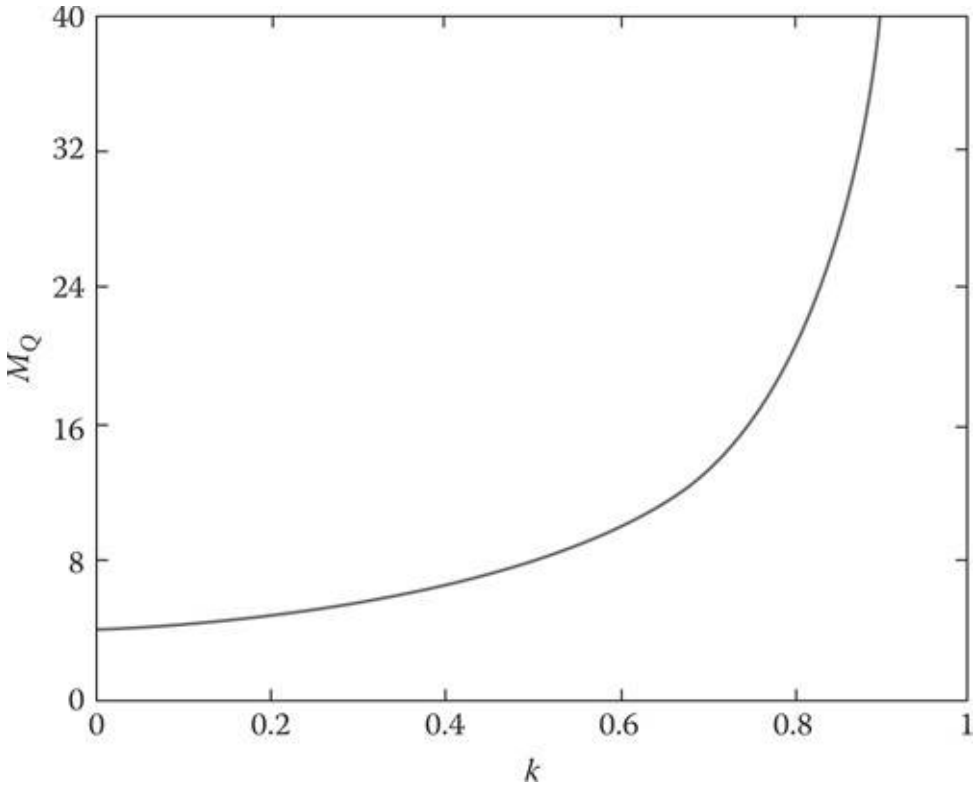


FIGURE 2.29
Voltage transfer gain M_Q versus k.

$$I_{L_1} = \frac{k}{1-k} I_o$$

$$I_{L_3} = I_{L_4} = L_{L_5} = I_{L_1} + I_{L_2} = \frac{1}{1-k} I_o$$

The current variations are

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$$\xi_1 = \frac{1-k}{2M_Q}\frac{R}{fL_1} \quad \xi_2 = \frac{k}{2M_Q}\frac{R}{fL_2} \quad \zeta = \frac{k(1-k)R}{2M_Q fL} = \frac{k}{M_Q^2}\frac{2R}{fL}$$

$$\chi_1 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{kV_1T}{2L_3\dfrac{I_o}{1-k}} = \frac{k\dfrac{V_o}{M_Q}T}{2L_3\dfrac{I_o}{1-k}} = \frac{k}{M_Q^2}\frac{2R}{fL_3} \quad \chi_2 = \frac{k}{M_Q^2}\frac{2R}{fL_4} \quad \chi_3 = \frac{k}{M_Q^2}\frac{2R}{fL_5}$$

The voltage variations are

$$\rho = \frac{k}{2fCR} \quad \sigma_1 = \frac{M_Q}{2fC_1R}$$

$$\sigma_2 = \frac{M_Q}{2fC_2R} \quad \sigma_3 = \frac{M_Q}{2fC_3R} \quad \sigma_4 = \frac{M_Q}{2fC_4R}$$

The variation ratio of output voltage V_C is

$$\varepsilon = \frac{k}{16M_Q}\frac{1}{f^2C_oL_2} \tag{2.189}$$

The output voltage ripple is very small.

The boundary between continuous and discontinuous modes is

$$M_Q \le \sqrt{k}\sqrt{\frac{2R}{fL}} = \sqrt{2kz_N} \tag{2.190}$$

This boundary curve is shown in Figure 2.30. Comparing with Equations 2.95, 2.127, 2.169, 2.183, and 2.190, it can be seen that this boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$.

In discontinuous mode, the current i_D exists in the period between kT and $[k + (1 - k)m_Q]T$, where m_Q is the filling efficiency, that is,

$$m_Q = \frac{1}{\zeta} = \frac{M_Q^2}{k\dfrac{2R}{fL}} \tag{2.191}$$

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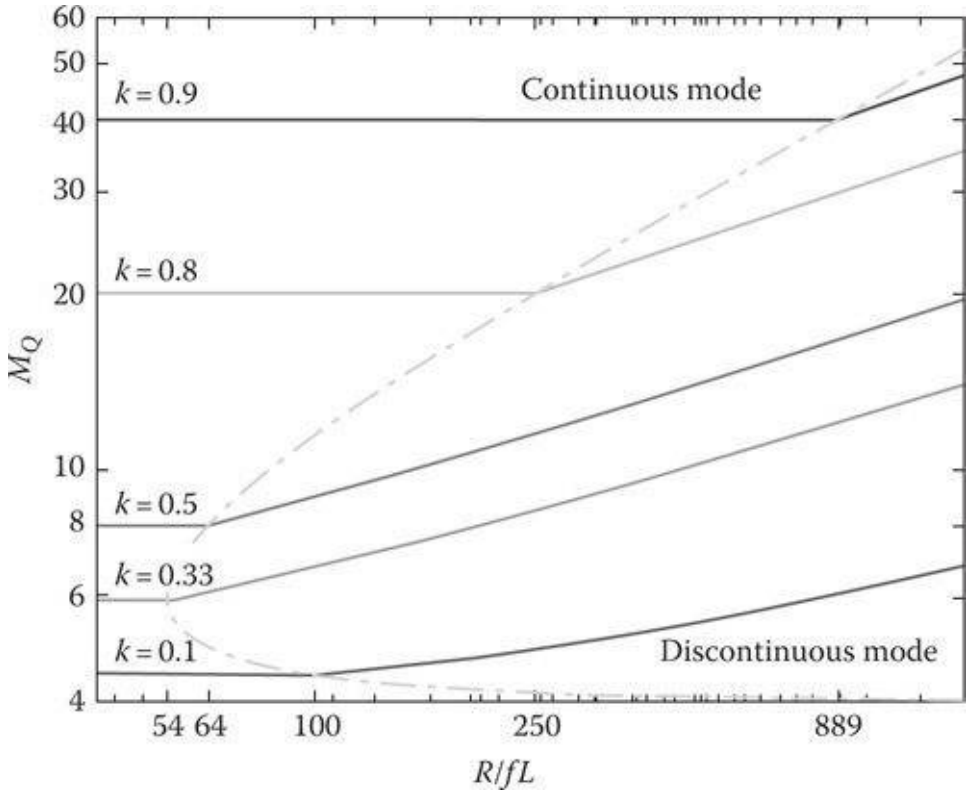


FIGURE 2.30
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$.

Considering Equation 2.190, therefore $0 < m_Q < 1$ Since the current i_D becomes zero at $t = kT + (1 - k)m_Q T$, for the current i_{L_1}, we have

$$kTV_i = (1-k)m_Q T\left(V_C - 4V_i - V_{L_3-off} - V_{L_4-off} - V_{L_5-off}\right)$$

or

$$V_C = \left[4 + \frac{3k}{1-k} + \frac{k}{(1-k)m_Q}\right]V_i = \left[4 + \frac{3k}{1-k} + k^2(1-k)\frac{R}{8fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k}$$

and for current i_{L_2}, we have

$$kT\left(V_i + V_C - V_o\right) = (1-k)m_Q T\left(V_o - 2V_i - V_{L_3-off} - V_{L_4-off} - V_{L_5-off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[4 + \frac{3k}{1-k} + \frac{k}{(1-k)m_Q}\right]V_i = \left[4 + \frac{3k}{1-k} + k^2(1-k)\frac{R}{8fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k} \qquad (2.192)$$

that is, the output voltage will linearly increase when load resistance R increases, as shown in Figure 2.30.

2.3.5 Summary

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From the analysis and calculation in the previous sections, the common formulae for all circuits can be obtained:

$$M=\frac{V_o}{V_i}=\frac{I_i}{I_o}\quad L=\frac{L_1L_2}{L_1+L_2}\quad z_N=\frac{R}{fL}\quad R=\frac{V_o}{I_o}$$

The current variations are

$$\xi_1=\frac{1-k}{2M}\frac{R}{fL_1}\quad \xi_2=\frac{k}{2M}\frac{R}{fL_2}\quad \chi_j=\frac{k}{M^2}\frac{n}{2}\frac{R}{fL_{i+2}}\quad (i=1,2,3,\ldots,n-1)\,n\geq 2$$

The voltage variations are

$$\rho=\frac{k}{2fCR}\quad \varepsilon=\frac{k}{16M}\frac{1}{f^2C_oL_2}\quad \sigma_j=\frac{M}{2fC_jR}\quad (j=1,2,3,4,\ldots,n)\,n\geq 1$$

where

i and *j* are inductors' and capacitors' number

n is the stage number

In order to write common formulae for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript $n = 0$ means the elementary circuit, subscript $n = 1$ means the self-lift circuit, subscript $n = 2$ means the re-lift circuit, subscript $n = 3$ means the triple-lift circuit, subscript $n = 4$ means the quadruple-lift circuit, and so on.

The voltage transfer gain is

$$M_n=\frac{n+kh(n)}{1-k}\quad n=0,1,2,3,4,\ldots \tag{2.193}$$

The freewheeling diode current i_D's variation is

$$\zeta_n=\frac{k^{[1+h(n)]}}{M_n{}^2}\frac{n+h(n)}{2}z_N \tag{2.194}$$

The boundaries are determined by the following condition:

$$\zeta_n\geq 1$$

or

$$\frac{k^{[1+h(n)]}}{M_n{}^2}\frac{n+h(n)}{2}z_N\geq 1\quad n=0,1,2,3,4,\ldots \tag{2.195}$$

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

$$M_n=k^{\frac{1+h(n)}{2}}\sqrt{\frac{n+h(n)}{2}z_N}\quad n=0,1,2,3,4,\ldots \tag{2.196}$$

The filling efficiency is

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$$m_n = \frac{1}{\zeta_n} = \frac{M_n^2}{k^{[1+h(n)]}} \frac{2}{n+h(n)} \frac{1}{z_N} \tag{2.197}$$

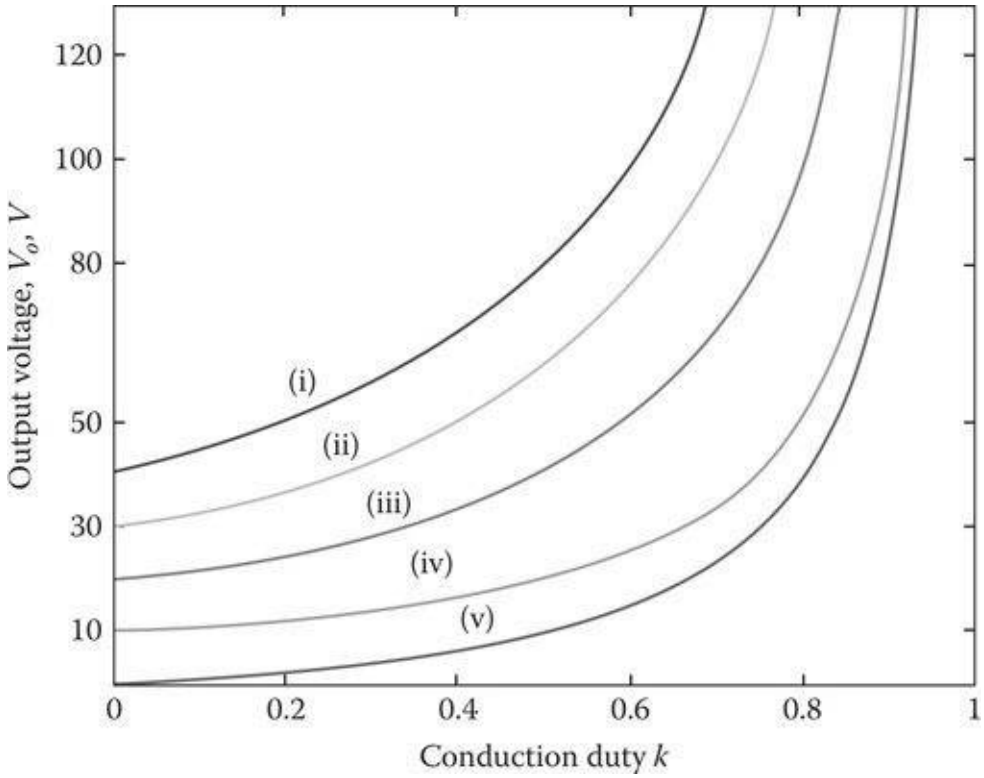


FIGURE 2.31
Output voltages of all positive-output Luo-converters (V_i = 10 V).

The output voltage in discontinuous mode for all circuits

$$V_{o-n} = \left[n + \frac{n+h(n)-1}{1-k} + k^{[2-h(n)]} \frac{1-k}{2[n+h(n)]} z_N \right] V_i \quad n = 0,1,2,3,4,\ldots \tag{2.198}$$

where

$$h(n) = \begin{cases} 0 & \text{if} \quad n \geq 1 \\ 1 & \text{if} \quad n = 0 \end{cases} \quad \text{is the } \textit{Hong function} \tag{2.199}$$

Assuming that f = 50 kHz, $L_1 = L_2$ = 1 mH, $L_2 = L_3 = L_4 = L_5$ = 0.5 mH, $C = C_1 = C_2 = C_3 = C_4 = C_o$ = 20 μF, and the source voltage V_i = 10 V, the value of the output voltage V_o with various conduction duty k in continuous mode is shown in Figure 2.31. Typically, some values of the output voltage V_o and its ripples in conduction duty k = 0.33, 0.5, 0.75, and 0.9 are listed in Table 2.1. From these data, it states the fact that the output voltage of all Luo-converters is almost a real DC voltage with very small ripple.

TABLE 2.1
Comparison among Five Positive-Output Luo-Converters

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Positive-Output Luo-Converters	I_o	V_o	V_o (V_i = 10 V)			
			k = 0.33	k = 0.5	k = 0.75	k = 0.9
Elementary circuit	$I_o = \frac{1-k}{k} I_i$	$V_o = \frac{k}{1-k} V_i$	5 V	10 V	30 V	90 V
Self-lift circuit	$I_o = (1-k) I_i$	$V_o = \frac{1}{1-k} V_i$	15 V	20 V	40 V	100 V
Re-lift circuit	$I_o = \frac{1-k}{2} I_i$	$V_o = \frac{2}{1-k} V_i$	30 V	40 V	80 V	200 V
Triple-lift circuit	$I_o = \frac{1-k}{3} I_i$	$V_o = \frac{3}{1-k} V_i$	45 V	60 V	120 V	300 V
Quadruple-lift circuit	$I_o = \frac{1-k}{4} I_i$	$V_o = \frac{4}{1-k} V_i$	60 V	80 V	160 V	400 V

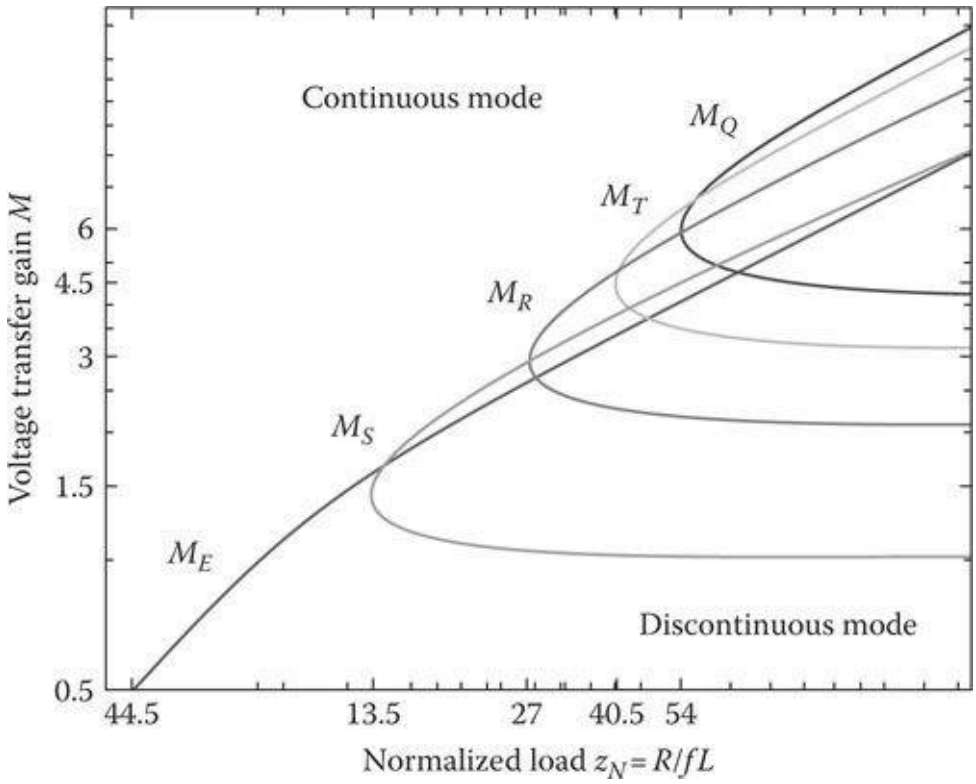


FIGURE 2.32
Boundaries between continuous and discontinuous modes of all positive-output Luo-converters.

The boundaries between continuous and discontinuous modes of all circuits are shown in Figure 2.32. The curves of all M versus z_N state that the continuous mode area increases from M_E via M_S, M_R, and M_T to MQ. The boundary of the elementary circuit is a monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other circuits, which of M_S, M_R, M_T, and MQ correspond at k = 1/3.

2.3.6 Discussions

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Some important points are vital for particular circuit design. They are discussed in the following sections.

2.3.6.1 Discontinuous Conduction Mode

Usually, the industrial applications require the DC/DC converters to work in continuous conduction mode. However, it is irresistible that DC/DC converter works in discontinuous mode sometimes. The analysis in Sections 2.3.2, 2.3.3, 2.3.4 and 2.3.5 shows that during switch-off if current i_D becomes zero before the next period switch-on, the state is called DCM. The following factors affect the diode current i_D to become discontinuous:

1. The switching frequency f is too low.
2. The conduction duty cycle k is too small.
3. The combined inductor L is too small.
4. The load resistance R is too big.

Discontinuous mode means i_D is discontinuous during switch-off. The output current $i_o(t)$ is still continuous if L_2 and C_o are large enough.

2.3.6.2 Output Voltage V_o versus Conduction Duty Cycle k

Output voltage V_o is a positive value and is usually greater than the source voltage V_i when the conduction duty ratio is $k > 0.5$ for the elementary circuit and any value in the range of $0 < k < 1$ for self-lift, re-lift, and multiple-lift circuits. Although small k results that the output voltage V_o of self-lift and re-lift circuits is greater than V_i and 2 V_i and so on, when $k = 0$, it results in $V_o = 0$ because switch S is never turned on.

If k is close to the value of 1, the ideal output voltage V_o should be a very big value. Unfortunately, Mohan advised that because of the effect of parasitic elements, output voltage V_o falls down very quickly. Finally, $k = 1$ results in $V_o = 0$, not infinity for all circuits. In this case, the accident of i_{L_1} toward infinity will happen. The recommended value range of the conduction duty k is

$$0 < k < 0.9$$

2.3.6.3 Switching Frequency f

In this book, the repeating frequency $f = 50$ kHz was selected. Actually, switching frequency f can be selected in the range between 10 and 500 kHz. Usually, the higher the frequency, the lower the ripples.

2.4 N/O Luo-Converters

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N/O Luo-converters perform the voltage conversion from positive to negative voltages using VL technique. They work in the third quadrant with large voltage amplification. Five circuits have been introduced. They are as follows:

- Elementary circuit
- Self-lift circuit
- Re-lift circuit
- Triple-lift circuit
- Quadruple-lift circuit

As the P/O Luo-converters, the N/O *Luo-converters* are another series of DC/DC step-up converters, which were developed from prototypes using VL technique. These converters perform positive to negative DC/DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure.

The elementary circuit can perform step-down and step-up DC/DC conversion. The other N/O Luo-converters are derived from this elementary circuit, which are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits) shown in the corresponding figures and introduced in the next sections, respectively. Switch *S* in these diagrams is a PMOS. It is driven by a PWM switch signal with repeating frequency *f* and conduction duty *k*. In this book, the switch repeating period is $T = 1/f$ so that the switch-on period is kT and the switch-off period is $(1 - k)T$. For all circuits, the load is usually resistive, that is, $R = V_o/I_o$; the normalized load is $z_N = R/fL$. Each converter consists of a negative Luo-pump and a "Π"-type filter $C–L_o–C_o$ and a lift circuit (except elementary circuit). The pump inductor L absorbs the energy from source during switch-on and transfers the stored energy to capacitor C during switch-off. The energy on capacitor C is then delivered to load during switch-on. Therefore, if the voltage V_C is high, the output voltage V_o is correspondingly high.

When the switch *S* turned off, the current i_D flows through the freewheeling diode D. This current descends in whole switch-off period $(1 – k)T$. If current i_D does not become zero before switch *S* is turned on again, we define this working state to be continuous mode. If current i_D becomes zero before switch *S* is turned on again, we define this working state to be discontinuous mode.

The directions of all voltages and currents are indicated in the figures. All descriptions and calculations in the text are concentrated to the absolute values. In this book, for any component *X*, its instantaneous current and voltage values are expressed as i_X and v_X or $i_X(t)$ and $v_X(t)$, and its average current and voltage values are expressed as I_X and V_X. For general description, the output voltage and current are V_o and I_o; the input voltage and current are V_i and I_i Assuming the output power equals to the input power,

$$P_o = P_{in} \quad \text{or} \quad V_o I_o = V_i I_i$$

The following symbols are used in the text of this book.

The voltage transfer gain is in *CCM*:

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o}$$

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The variation ratio of current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L}$$

The variation ratio of current i_{L_o} is

$$\xi = \frac{\Delta i_{L_o}/2}{I_{L_o}}$$

The variation ratio of current i_D is $\zeta = \frac{\Delta i_D/2}{I_L}$ during switching-off, $i_D = i_L$.

The variation ratio of current i_{L_j} is

$$\chi_j = \frac{\Delta i_{L_j}/2}{I_{L_j}} \quad j = 1,2,3,\ldots$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C}$$

The variation ratio of voltage v_{C_j}, is

$$\sigma_j = \frac{\Delta v_{C_j}/2}{V_{C_j}} \quad j = 1,2,3,4,\ldots$$

The variation ratio of output voltage $v_o = v_{C_o}$ is

$$\varepsilon = \frac{\Delta v_o/2}{V_o}$$

2.4.1 Elementary Circuit

The elementary circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.33. This circuit can be considered as a combination of an electronic pump *S*–*L*–*D*–(*C*) and a "Π"-type low-pass filter *C*–L_0–C_0. The electronic pump injects certain energy to the low-pass filter every cycle. Capacitor *C* in Figure 2.33 acts as the primary means of storing and transferring energy from the input source to the output load. Assuming capacitor *C* to be sufficiently large, the variation of the voltage across capacitor *C* from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$ even though it stores and transfers energy from the input to the output.

2.4.1.1 Circuit Description

When switch *S* is on, the equivalent circuit is shown in Figure 2.33b. In this case, the source current $i_i = i_L$. Inductor *L* absorbs energy from the source, and current i_L linearly increases with slope V_i/L. In the meantime, the diode *D* is blocked since it is inversely biased. Inductor L_o keeps the output current I_o continuous and transfers energy from capacitor *C* to the load *R*, that is, $i_{C-on} = i_{L_o}$. When switch *S* is off, the equivalent circuit is shown in Figure 2.33c. In this

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case, the source current i_i = 0. Current i_L flows through the freewheeling diode D to charge capacitor C and enhances current i_{L_o}. Inductor L transfers its stored energy to capacitor C and load R via inductor L_0, that is, $i_L = i_{C-off} + i_{L_o}$ Thus, current i_L decreases.

2.4.1.2 Average Voltages and Currents

The output current $I_o = I_{L_o}$ because the capacitor C_o does not consume any energy in the steady state. The average output current is

$$I_o = I_{Lo} = I_{C-on}. \tag{2.200}$$

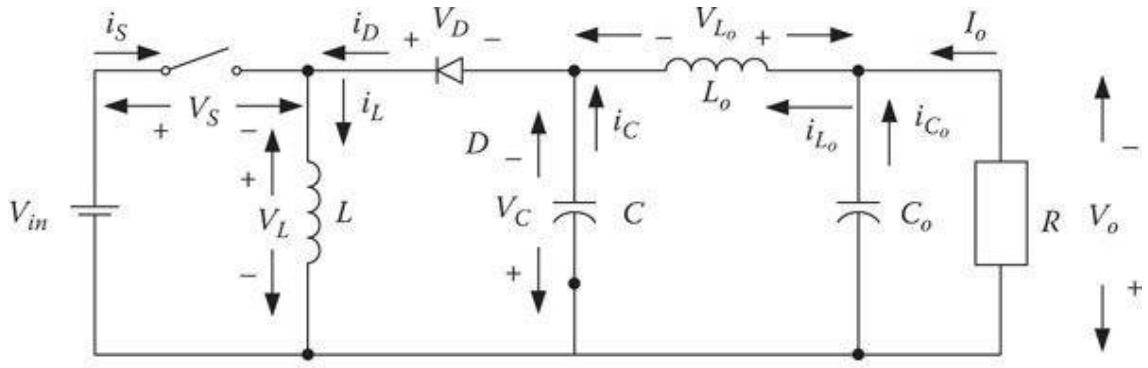
The charge on the capacitor C increases during switch-off:

$$Q_+ = (1-k)TI_{C-off}.$$

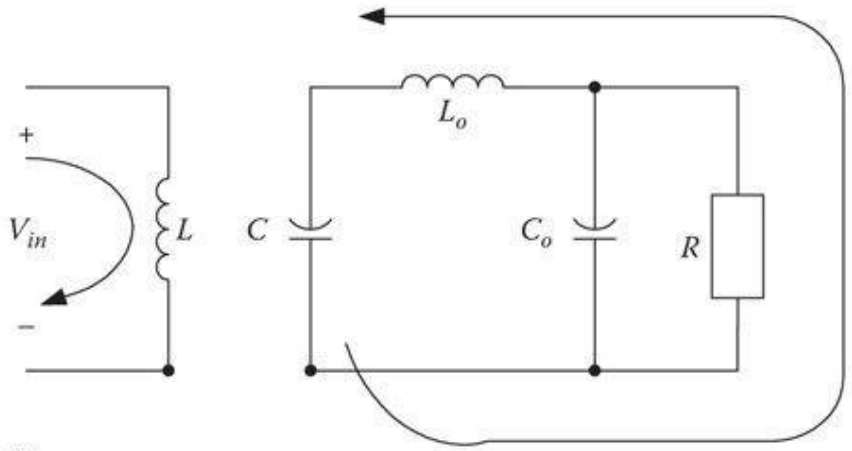
And it decreases during switch-on:

$$Q_- = kTI_{C-on}. \tag{2.201}$$

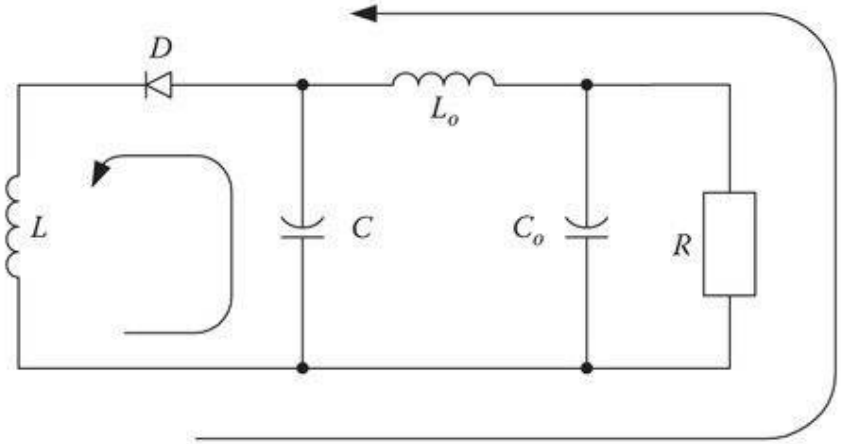
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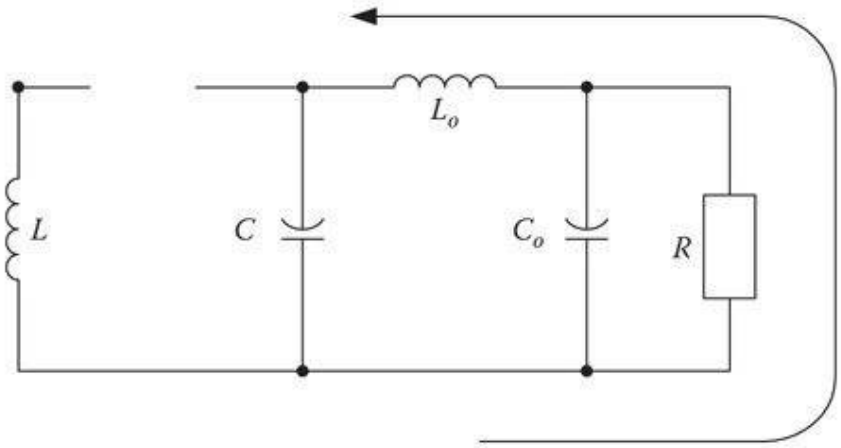
(a)



(b)



(c)



(d)

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FIGURE 2.33
Elementary circuit. (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

In a whole repeating period T, $Q_+ = Q_-$:

$$I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_o$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_o = \frac{I_o}{1-k} \tag{2.202}$$

Equations 2.200 and 2.202 are available for all circuit of N/O Luo-converters.

The source current is $i_i = i_L$ during switch-on period. Therefore, its average source current I_i is

$$I_i = k \times i_i = k i_L = k I_L = \frac{k}{1-k} I_o$$

or

$$I_o = \frac{1-k}{k} I_i \tag{2.203}$$

and the output voltage is

$$V_o = \frac{k}{1-k} V_i \tag{2.204}$$

The voltage transfer gain in continuous mode is

$$M_E = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{k}{1-k} \tag{2.205}$$

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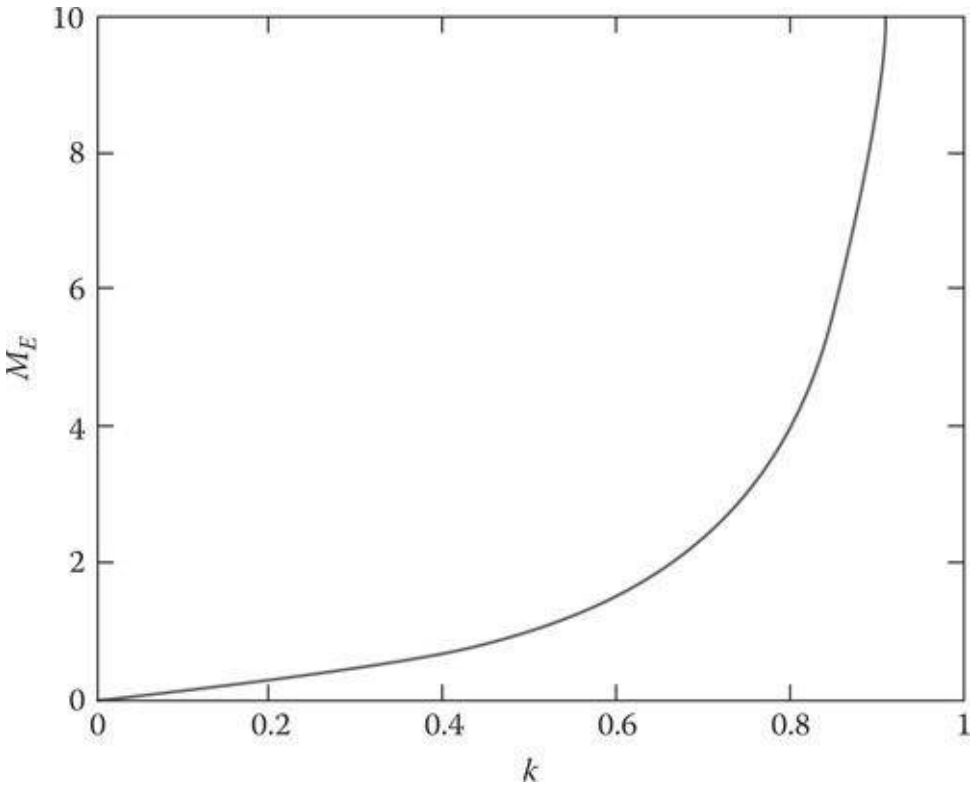


FIGURE 2.34
Voltage transfer gain M_E versus k.

The curve of M_E versus k is shown in Figure 2.34. Current i_L increases and is supplied by V_i during switch-on. It decreases and is inversely biased by $-V_C$ during switch-off:

$$kTV_i = (1-k)TV_C \tag{2.206}$$

Therefore,

$$V_C = V_o = \frac{k}{1-k}V_i \tag{2.207}$$

2.4.1.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.35.

Current i_L increases and is supplied by V_i during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_i}{L}$$

Considering Equations 2.202 and 2.205 and $R = V_o/I_o$, the variation ratio of the current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_iT}{2LI_o} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2}\frac{R}{2fL} \tag{2.208}$$

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Considering Equation 2.201, the peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k}{C} T I_o \tag{2.209}$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C / 2}{V_C} = \frac{k I_o T}{2 C V_o} = \frac{k}{2} \frac{1}{fCR} \tag{2.210}$$

Since voltage V_o variation is very small, the peak-to-peak variation of current i_{L_o} is calculated by the area (B) of the triangle with the width of $T/2$ and height $\Delta v_C/2$:

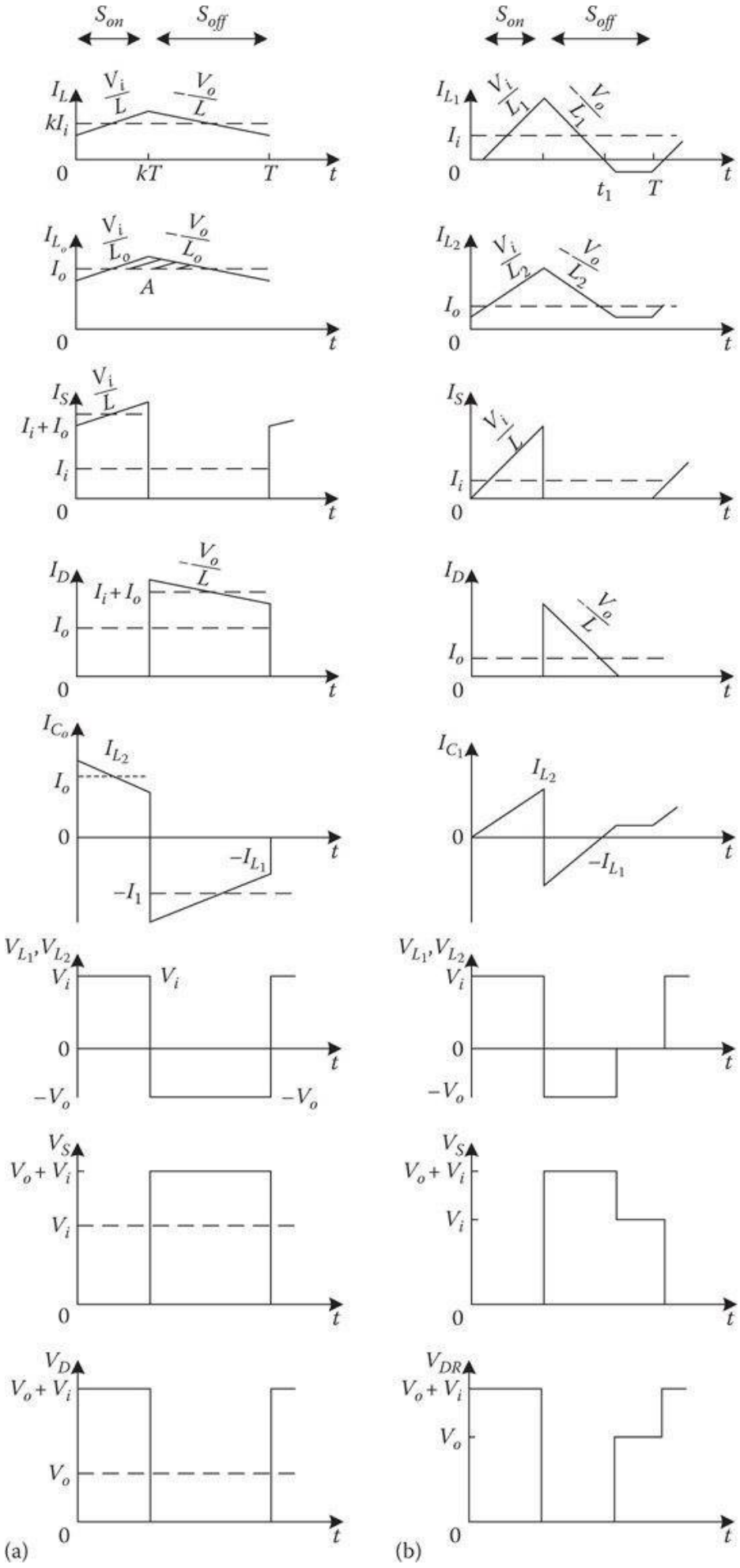
$$\Delta i_{L_o} = \frac{B}{L_o} = \frac{1}{2} \frac{T}{2} \frac{k}{2CL_o} T I_o = \frac{k}{8 f^2 C L_o} I_o \tag{2.211}$$

Considering Equation 2.200, the variation ratio of current i_{L_o} is

$$\xi = \frac{\Delta i_{L_o} / 2}{I_{L_o}} = \frac{k}{16} \frac{1}{f^2 C L_o} \tag{2.212}$$

Since the voltage v_C is a triangle waveform, the difference between v_C and output voltage V_o causes the ripple of current i_{L_o}, and the difference between i_{L_o} and output current I_o causes the ripple of output voltage v_o. The ripple waveform of current i_{L_o} should be a partial parabola in Figure 2.35 because of the triangle waveform of ΔV_C. To simplify the calculation, we can treat the ripple waveform of current i_{L_o} as a triangle waveform in Figure 2.35 because the ripple of the current i_{L_o} is very small. Therefore, the peak-to-peak variation of voltage v_{C_o} is calculated by the area (A) of the triangle with the width of T/2 and height $\Delta i_{L_o}/2$:

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FIGURE 2.35
Some voltage and current waveforms of elementary circuit. (a) CCM operation. (b) DCM operation.

$$\Delta v_{C_o} = \frac{A}{C_o} = \frac{1}{2}\frac{T}{2}\frac{k}{16f^2CC_oL_o}I_o = \frac{k}{64f^3CC_oL_o}I_o \tag{2.213}$$

The variation ratio of current v_{C_o} is

$$\varepsilon = \frac{\Delta v_{C_o}/2}{V_{C_o}} = \frac{k}{128f^3CC_oL_o}\frac{I_o}{V_o} = \frac{k}{128}\frac{1}{f^3CC_oL_oR} \tag{2.214}$$

Assuming that $f = 50$ kHz, $L = L_o = 100$ μH, $C = C_o = 5$ μF, $R = 10$ Ω, and $k = 0.6$, we obtain

$$M_E = 1.5 \quad \zeta = 0.16, \quad \zeta = 0.03, \quad \rho = 0.12, \quad \text{and} \quad \varepsilon = 0.0015.$$

The output voltage V_o is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_0=V_0/R$.

2.4.1.4 Instantaneous Values of Currents and Voltages

Referring to Figure 2.35, the instantaneous current and voltage values are listed here:

$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.215}$$

$$v_D = \begin{cases} V_i + V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.216}$$

$$v_L = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -V_o & \text{for } kT < t \le T \end{cases} \tag{2.217}$$

$$i_i = i_S = \begin{cases} i_L(0) + \dfrac{V_i}{L}t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.218}$$

$$i_L = \begin{cases} i_L(0) + \dfrac{V_i}{L}t & \text{for } 0 < t \le kT \\ i_L(kT) - \dfrac{V_o}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.219}$$

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$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_L(kT) - \dfrac{V_o}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.220}$$

$$i_C \approx \begin{cases} -I_{C-on} & \text{for } 0 < t \le kT \\ I_{C-off} & \text{for } kT < t \le T \end{cases} \tag{2.221}$$

where

$$i_L(0) = kI_i - kV_i/2fL$$

$$i_L(kT) = kI_i + kV_i/2fL$$

Since the instantaneous current i_{L_o} and voltage v_{C_o} are partial parabolas with very small ripples, they can be treated as a DC and voltage.

2.4.1.5 Discontinuous Mode

Referring to Figure 2.33d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

$$\frac{k^2}{M_E^2}\frac{R}{2fL} \ge 1$$

or

$$M_E \le k\sqrt{\frac{R}{2fL}} = k\sqrt{\frac{z_N}{2}} \tag{2.222}$$

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.36. It can be seen that the boundary curve is a monorising function of the parameter k.

In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_E]T$, where m_E is the *filling efficiency*, and it is defined as

$$m_E = \frac{1}{\zeta} = \frac{M_E^2}{k^2\dfrac{R}{2fL}} \tag{2.223}$$

Considering Equation 2.222, therefore $0 < m_E < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_E$, for the current i_L

$$kTV_i = (1 - k)m_E TV_C$$

or

$$V_C = \frac{k}{(1-k)m_E}V_i = k(1-k)\frac{R}{2fL}V_i \quad \text{with} \sqrt{\frac{R}{2fL}} \ge \frac{1}{1-k}$$

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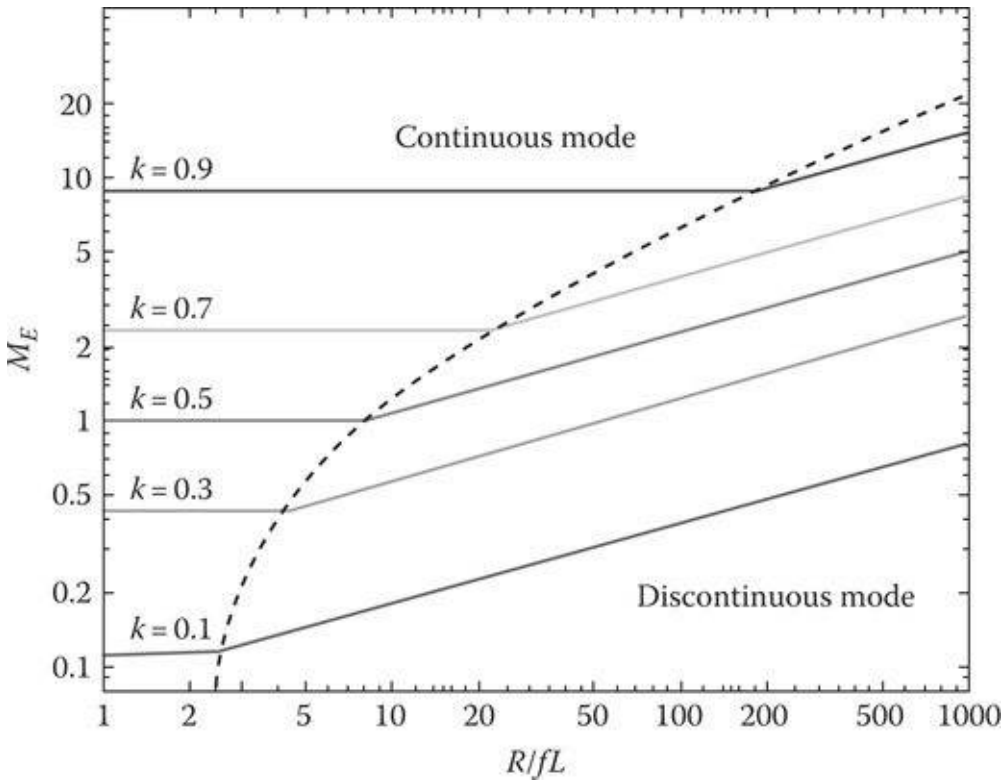


FIGURE 2.36
The boundary between continuous and discontinuous modes and output voltage versus the normalized load $z_N = \sqrt{R/fL}$ (elementary circuit).

and for the current i_{L_o}

$$kT(V_i + V_C - V_o) = (1-k)m_E T V_o$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{R}{2fL} V_i \quad \text{with} \sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \tag{2.224}$$

that is, the output voltage will linearly increase when load resistance R increases. The output voltage versus the normalized load $Z_N = R/fL$ is shown in Figure 2.36. Larger load resistance R may cause higher output voltage in discontinuous mode.

2.4.2 Self-Lift Circuit

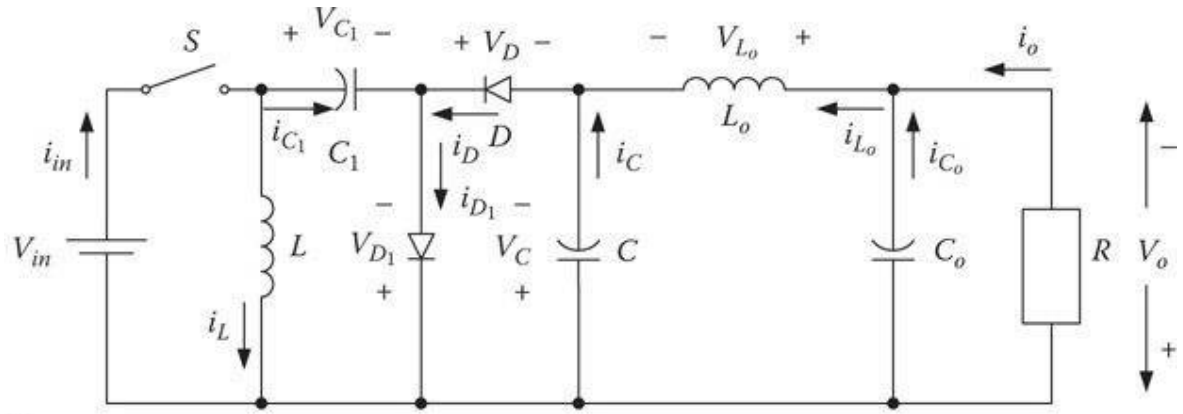
The self-lift circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.37, which is derived from the elementary circuit. It consists of eight passive components. They are one static switch S; two inductors L and L_0; three capacitors C, C_1, and C_0; and two diodes D, D_1. Comparing with Figures 2.33 and 2.37, it can be seen that there are only one more capacitor C_1 and one more diode D_1 added into the self-lift circuit. Circuit C_1–D_1 is the lift circuit. Capacitor C_1 functions to lift the capacitor voltage V_C by a source voltage V. Current $i_{C_1}(t)$ is an exponential function $\delta(t)$. It has a large value at the moment of power on, but it is small in the steady state because $V_{C_1} = V_i$.

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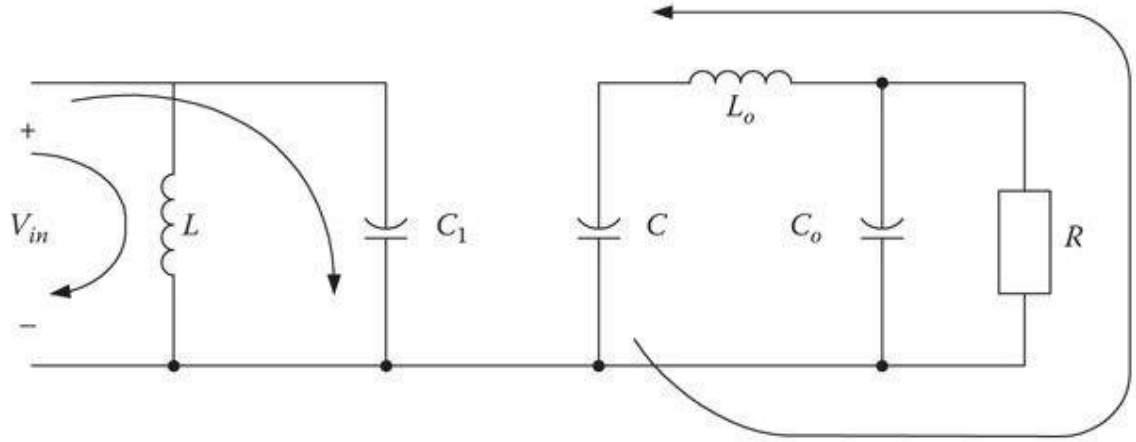
2.4.2.1 Circuit Description

When switch S is on, the equivalent circuit is shown in Figure 2.37b. In this case, the source current $i_I = i_L + i_{C_1}$. Inductor L absorbs energy from the source, and current i_i linearly increases with slope V_i/L. In the meantime, the diode D_1 is conducted and capacitor C_1 is charged by the current i_{C_1}. Inductor L_o keeps the output current I_o continuous and transfers energy from capacitor C to the load R, that is, $i_{C-on} = i_{L_o}$. When switch S is off, the equivalent circuit is shown in Figure 2.37c. In this case, the source current i_i = 0. Current i_L flows through the freewheeling diode D to charge capacitor C and enhances current i_{L_o} Inductor L transfers its stored energy via capacitor C_1 to capacitor C and load R (via inductor L_o), that is, $i_L = i_{C_1-off} = i_{C-off} + i_{L_o}$. Thus, current i_L decreases.

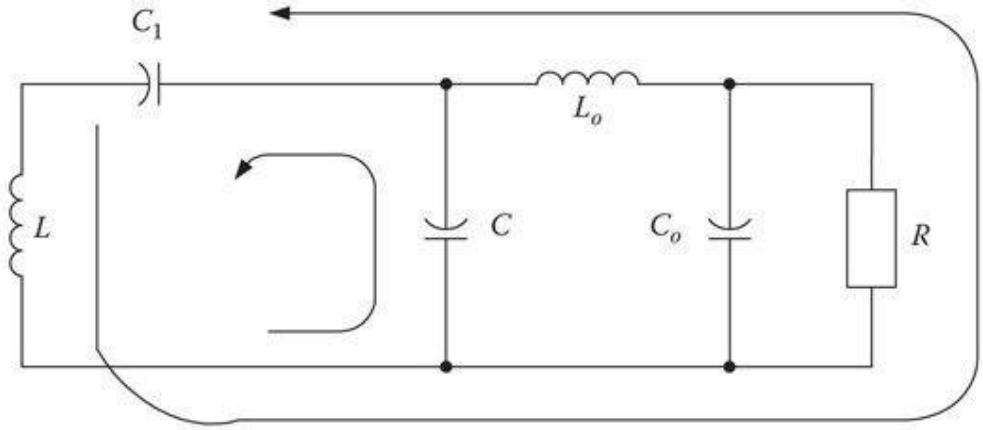
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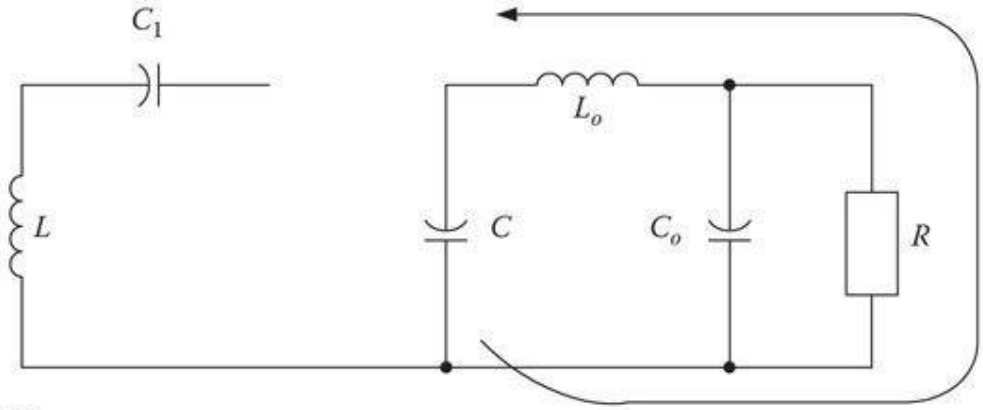
(a)



(b)



(c)



(d)

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FIGURE 2.37
Self-lift circuit. (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

2.4.2.2 Average Voltages and Currents

The output current $I_o = I_{L_o}$ because the capacitor C_0 does not consume any energy in the steady state. The average output current is

$$I_o = I_{L_o} = I_{C-on}. \tag{2.225}$$

The charge of the capacitor C increases during switch-off:

$$Q_+ = (1-k)TI_{C-off}.$$

And it decreases during switch-on:

$$Q_- = kTI_{C-on}. \tag{2.226}$$

In a whole repeating period T, $Q_+ = Q_-$.

Thus,

$$I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_o$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_o = \frac{I_o}{1-k} \tag{2.227}$$

From Figure 2.37,

$$I_{C_1-off} = I_L = \frac{1}{1-k} I_o \tag{2.228}$$

and

$$I_{C_1-on} = \frac{1-k}{k} I_{C_1-off} = \frac{1}{k} I_o \tag{2.229}$$

In steady state, we can use

$$V_{C_1} = V_i$$

Investigate current i_L; it increases during switch-on with slope V_i/L and decreases during switching-off with slope $-(V_o - V_{C_1})/L = -(V_o - V_i)/L$.

Therefore,

$$kV_i = (1-k)(V_o - V_i)$$

or

$$V_o = \frac{1}{1-k} V_i \tag{2.230}$$

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and

$$I_o = (1-k)I_i \tag{2.231}$$

The voltage transfer gain in continuous mode is

$$M_S = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{1}{1-k} \tag{2.232}$$

The curve of M_S versus k is shown in Figure 2.38.

Circuit $(C–L_o–C_o)$ is a "Π"-type low-pass filter.

Therefore,

$$V_C = V_o = \frac{k}{1-k}V_i \tag{2.233}$$

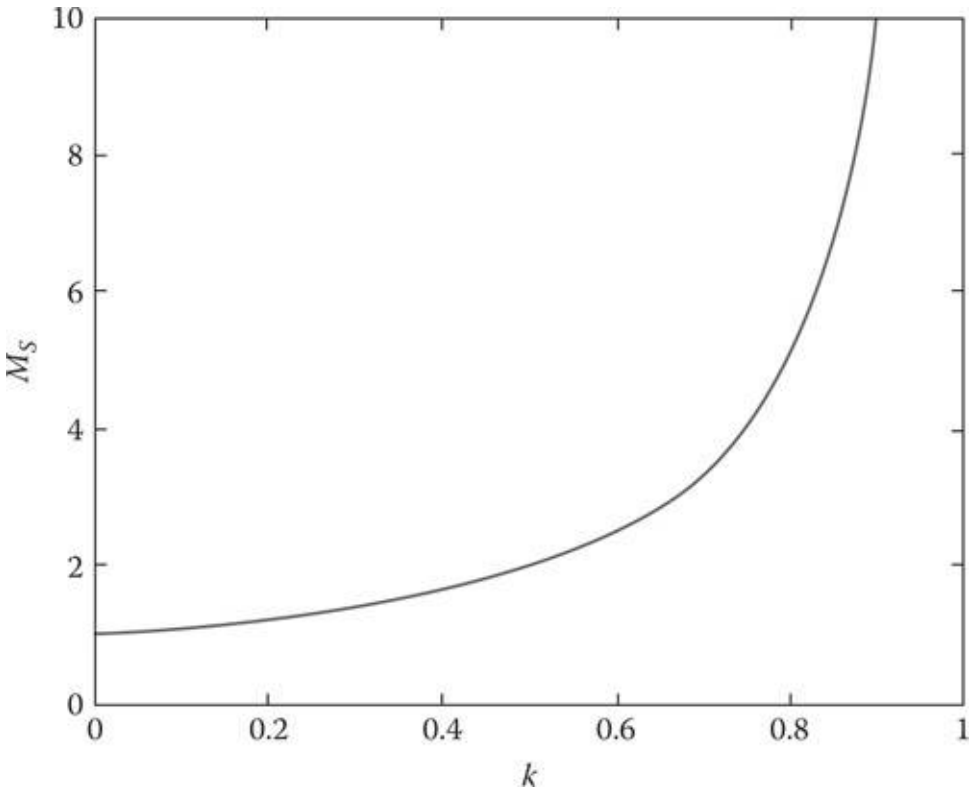


FIGURE 2.38
Voltage transfer gain M_S versus k.

2.4.2.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.39.

Current i_L increases and is supplied by V_i during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_i}{L}$$

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Considering Equation 2.227 and $R = V_o/I_o$, the variation ratio of the current i_L is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_i T}{2LI_o} = \frac{k(1-k)R}{2M_S fL} = \frac{k}{M_S^2}\frac{R}{2fL} \tag{2.234}$$

Considering Equation 2.226, the peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k}{C}TI_o$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_o T}{2CV_o} = \frac{k}{2}\frac{1}{fCR} \tag{2.235}$$

The peak-to-peak variation of voltage v_{C_1} is

$$\Delta v_{C_1} = \frac{kT}{C_1} I_{C_1-on} = \frac{1}{fC} I_o$$

The variation ratio of voltage v_{C_1} is

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{I_o}{2fC_1V_i} = \frac{M_S}{2}\frac{1}{fC_1R} \tag{2.236}$$

Considering Equation 2.211,

$$\Delta i_{Lo} = \frac{1}{2}\frac{T}{2}\frac{k}{2CL_o}TI_o = \frac{k}{8f^2CL_o}I_o$$

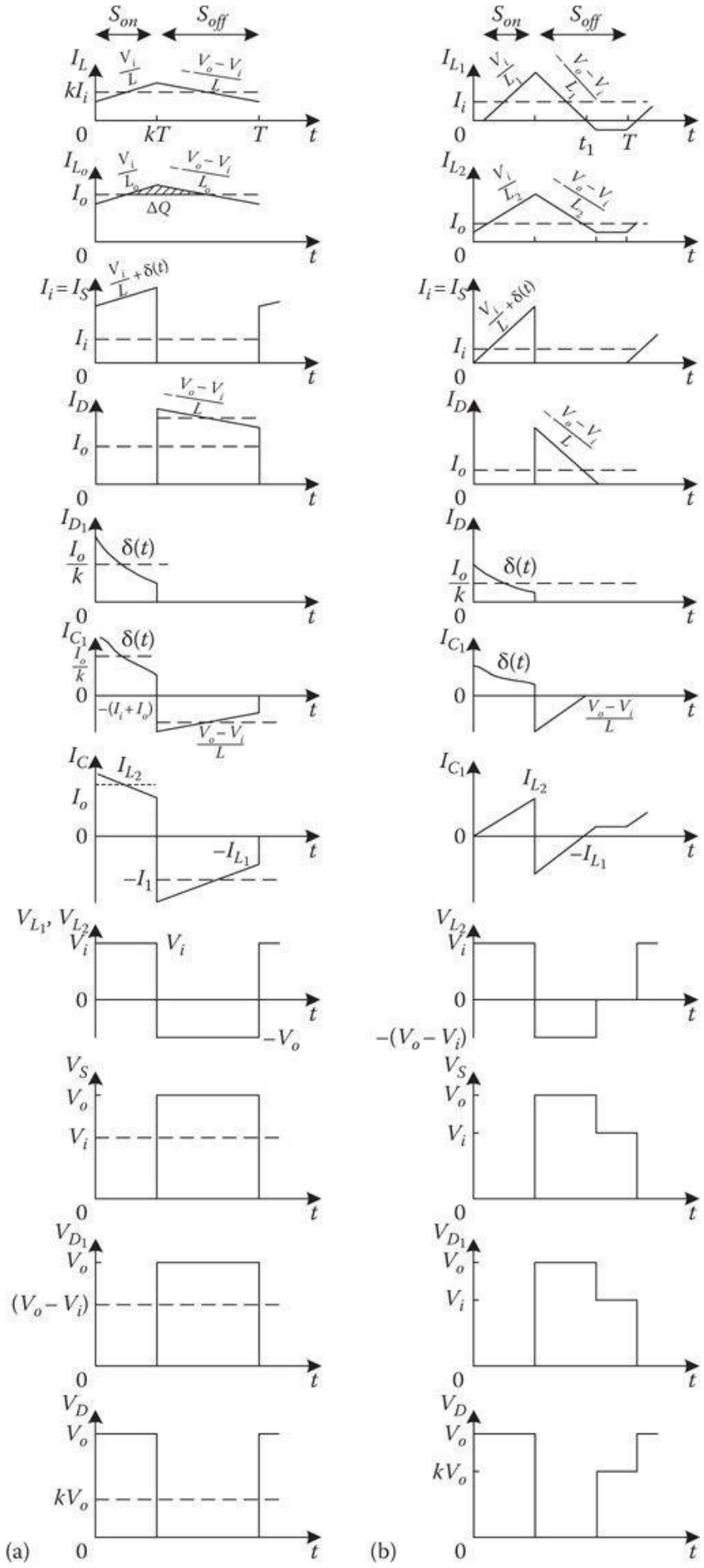
The variation ratio of current i_{L_o} is

$$\xi = \frac{\Delta i_{L_o}/2}{I_{L_o}} = \frac{k}{16}\frac{1}{f^2CL_o} \tag{2.237}$$

Considering Equation 2.213,

$$\Delta v_{C_o} = \frac{B}{C_o} = \frac{1}{2}\frac{T}{2}\frac{k}{16f^2CC_oL_o}I_o = \frac{k}{64f^3CC_oL_o}I_o$$

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FIGURE 2.39
Some voltage and current waveforms of self-lift circuit. (a) CCM operation. (b) DCM operation.

The variation ratio of current v_{C_o} is

$$\varepsilon = \frac{\Delta v_{C_o}/2}{V_{C_o}} = \frac{k}{128 f^3 C C_o L_o} \frac{I_o}{V_o} = \frac{k}{128} \frac{1}{f^3 C C_o L_o R} \tag{2.238}$$

Assuming that $f = 50$ kHz, $L = L_o = 100$ μH, $C = C_o = 5$ μF, $R = 10$ Ω, and $k = 0.6$, we obtain

$$M_S = 2.5 \quad \zeta = 0.096, \quad \xi = 0.03, \quad \rho = 0.12, \quad \text{and} \quad \varepsilon = 0.0015.$$

The output voltage V_o is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_o = V_o/R$.

2.4.2.4 Instantaneous Value of the Currents and Voltages

Referring to Figure 2.39, the instantaneous values of the currents and voltages are listed here:

$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o - V_I & \text{for } kT < t \le T \end{cases} \tag{2.239}$$

$$v_D = \begin{cases} V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.240}$$

$$v_{D_1} = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.241}$$

$$v_L = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -(V_o - V_i) & \text{for } kT < t \le T \end{cases} \tag{2.242}$$

$$i_i = i_S = \begin{cases} i_{L_1}(0) + \delta(t) + \dfrac{V_i}{L} t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.243}$$

$$i_L = \begin{cases} i_L(0) + \dfrac{V_i}{L} t & \text{for } 0 < t \le kT \\ i_L(kT) - \dfrac{V_o - V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.244}$$

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$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{V_o - V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.245}$$

$$i_{D_1} = \begin{cases} \delta(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.246}$$

$$i_{C_1} = \begin{cases} \delta(t) & \text{for } 0 < t \le kT \\ -i_L(kT) + \dfrac{V_o - V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.247}$$

$$i_C \approx \begin{cases} -I_{C-on} & \text{for } 0 < t \le kT \\ I_{C-off} & \text{for } kT < t \le T \end{cases} \tag{2.248}$$

where

$$i_L(0) = kI_i - kV_i/2fL$$

$$i_L(kT) = kI_i + kV_i/2fL$$

Since the instantaneous current i_{L_o} and voltage v_{C_o} are partial parabolas with very small ripples, they can be treated as a DC and voltage.

2.4.2.5 Discontinuous Mode

Referring to Figure 2.37d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

$$\frac{k}{M_S^2}\frac{R}{2fL} \ge 1$$

or

$$M_S \le \sqrt{k}\sqrt{\frac{R}{2fL}} = \sqrt{k}\sqrt{\frac{z_N}{2}} \tag{2.249}$$

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.40. It can be seen that the boundary curve has a minimum value of 1.5 at $k = 1/3$.

In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_S]T$, where m_s is the *filling efficiency*, and it is defined as

$$m_S = \frac{1}{\zeta} = \frac{M_S^2}{k\dfrac{R}{2fL}} \tag{2.250}$$

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Considering Equation 2.249, therefore $0 < m_S < 1$. Since the diode current i_D becomes zero at $t = kT + (1 - k)m_S T$ for the current i_L

$$kTV_i = (1 - k)m_S T(V_C - V_i)$$

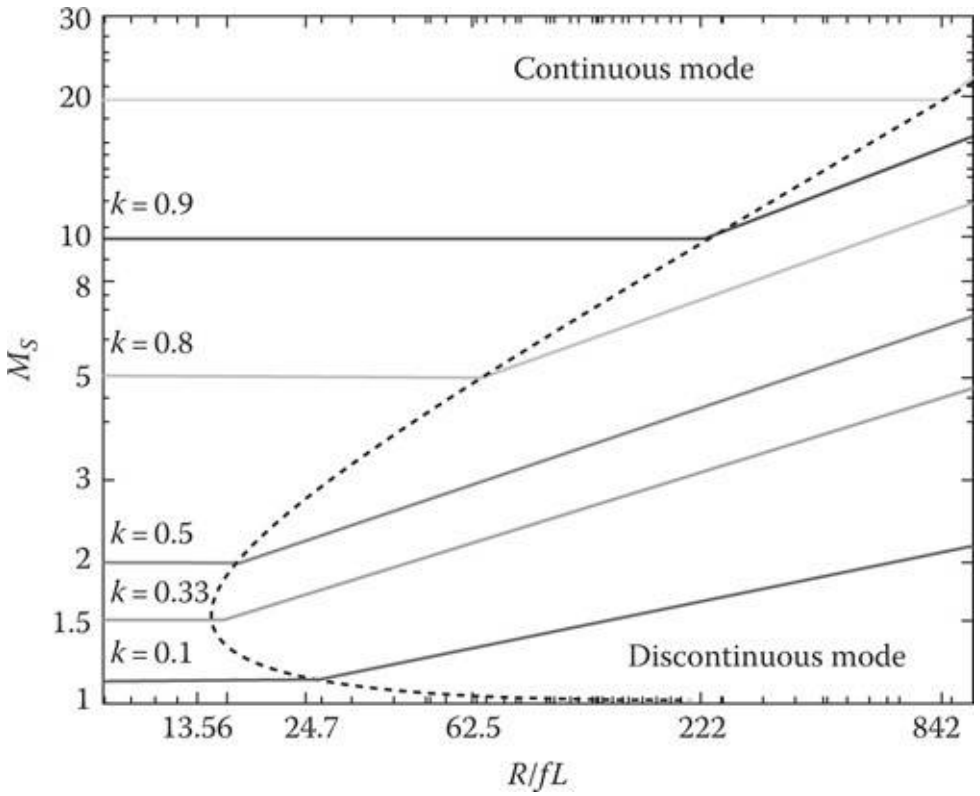


FIGURE 2.40
The boundary between continuous and discontinuous modes and output voltage versus the normalized load $z_N = R/fL$ (self-lift circuit).

or

$$V_C = \left[1 + \frac{k}{(1-k)m_S}\right]V_i = \left[1 + k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k}$$

and for the current i_{L_o}

$$kT(V_i + V_C - V_o) = (1 - k)m_S T(V_o - V_i)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[1 + \frac{k}{(1-k)m_S}\right]V_i = \left[1 + k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{2fL}} \geq \frac{1}{1-k} \tag{2.251}$$

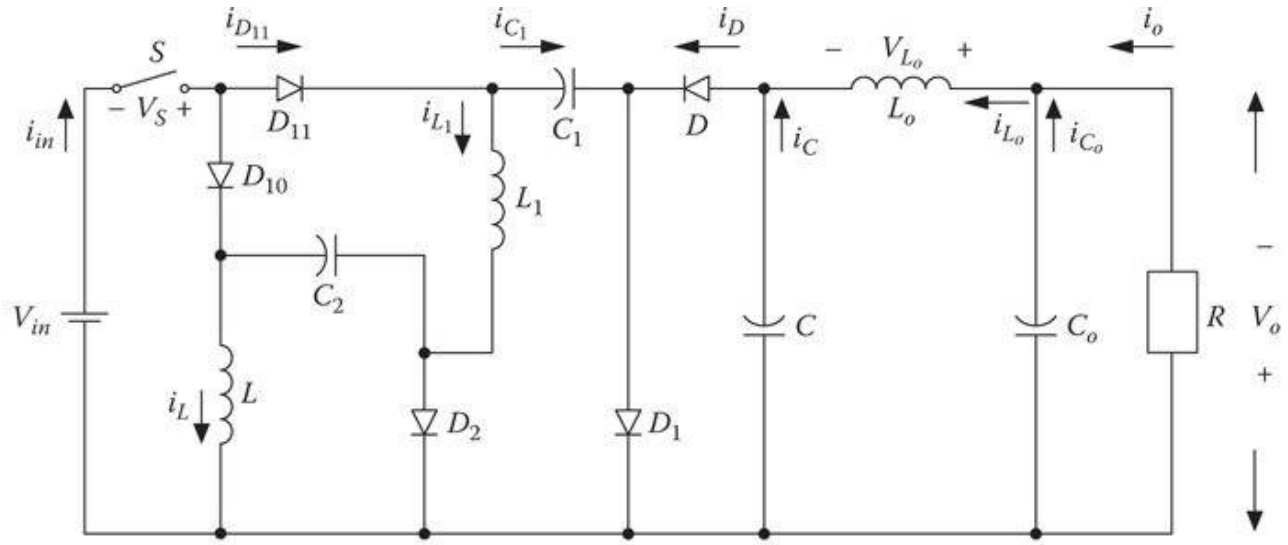
that is, the output voltage will linearly increase when load resistance R increases. The output voltage V_o versus the normalized load $z_N = R/fL$ is shown in Figure 2.40. Larger load resistance R causes higher output voltage in discontinuous mode.

2.4.3 Re-Lift Circuit

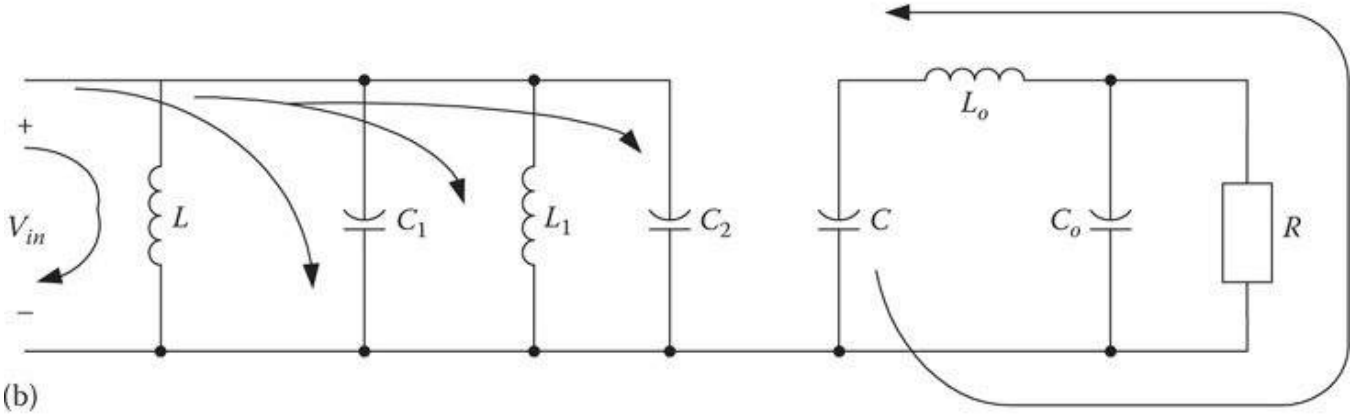
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The re-lift circuit and its switch-on and switch-off equivalent circuits are shown in Figure 2.41, which is derived from the self-lift circuit. It consists of one static switch S; three inductors L, L_1, and L_o; four capacitors C, C_1, C_2, and C_o; and diodes. From Figures 2.33, 2.37, and 2.41, it can be seen that there are one capacitor C_2, one inductor L_1, and two diodes D_2 and D_{11} added into the re-lift circuit. Circuit C_1–D_1–D_{11}–L_1–C_2–D_2 is the lift circuit. Capacitors C_1 and C_2 perform characteristics to lift the capacitor voltage V_C by twice that of source voltage $2V_i$. Inductor L_1 performs the function as a ladder joint to link the two capacitors C_1 and C_2 and lift the capacitor voltage V_C up. Currents $i_{C_1}(t)$ and $i_{C_2}(t)$ are exponential functions $\delta_1(t)$ and $\delta_2(t)$ They have large values at the moment of power on, but they are small because $v_{C_1} = v_{C_2} \cong V_i$ in steady state.

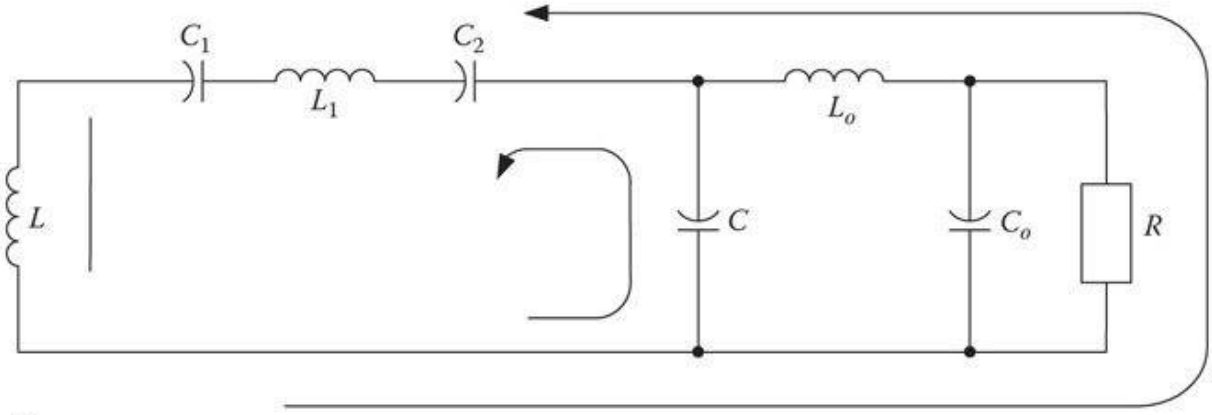
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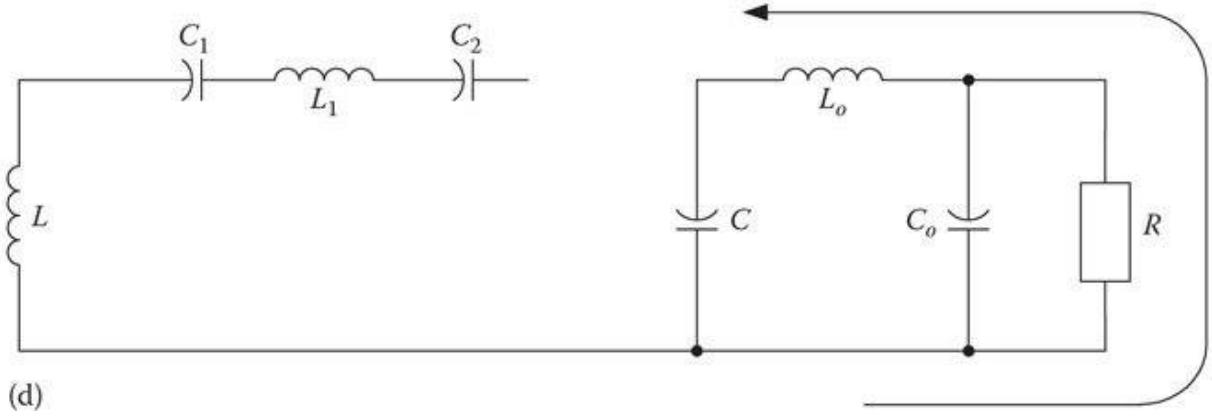
(a)



(b)



(c)



(d)

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FIGURE 2.41
Re-lift circuit. (a) Circuit diagram. (b) Switch-on. (c) Switch-off. (d) Discontinuous mode.

2.4.3.1 Circuit Description

When switch S is on, the equivalent circuit is shown in Figure 2.41b. In this case, source current $i_i = i_L + i_{C_1} + i_{C_2}$. Inductor L absorbs energy from the source, and current i_L linearly increases with slope V_i/L. In the meantime, diodes D_1 and D_2 are conducted so that capacitors C_1 and C_2 are charged by currents i_{C_1} and i_{C_2}. Inductor L_o keeps output current I_o continuous and transfers energy from capacitors C to load R, that is, $i_{C-on} = i_{L_o}$. When switch S is off, the equivalent circuit is shown in Figure 2.41c. In this case, source current $i_i = 0$. Current i_L flows through the freewheeling diode D, capacitors C_1 and C_2, and inductor L_1 to charge capacitor C and enhances current i_{L_o} Inductor L transfers its stored energy to capacitor C and load R via inductor L_o, that is, $i_L = i_{C_1-off} = i_{C_2-off} = i_{L_1-off} = i_{C-off} + i_{L_o}$. Thus, current i_L decreases.

2.4.3.2 Average Voltages and Currents

The output current $I_o = I_{L_o}$ because the capacitor C_o does not consume any energy in the steady state. The average output current is

$$I_o = I_{Lo} = I_{C-on}. \tag{2.252}$$

The charge of the capacitor C increases during switch-off:

$$Q_+ = (1-k)TI_{C-off}.$$

And it decreases during switch-on:

$$Q_- = kTI_{C-on}.$$

In a whole repeating period T, $Q_+ = Q_-$. Thus,

$$I_{C-off} = \frac{k}{1-k} I_{C-on} = \frac{k}{1-k} I_o$$

Therefore, the inductor current I_L is

$$I_L = I_{C-off} + I_o = \frac{I_o}{1-k} \tag{2.253}$$

We know from Figure 2.41c that

$$I_{C_1-off} = I_{C_2-off} = I_{L_1} = I_L = \frac{1}{1-k} I_o \tag{2.254}$$

and

$$I_{C_1-on} = \frac{1-k}{k} I_{C_1-off} = \frac{1}{k} I_o \tag{2.255}$$

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and

$$I_{C_2-on} = \frac{1-k}{k} I_{C_2-off} = \frac{1}{k} I_o \tag{2.256}$$

In steady state, we can use

$$V_{C_1} = V_{C_2} = V_i$$

and

$$V_{L_1-on} = V_i \quad V_{L_1-off} = \frac{k}{1-k} V_i$$

Investigate current i_L; it increases during switching-on with slope V_i/L and decreases during switching-off with slope $-(V_o - V_{C_1} - V_{C_2} - V_{L_1-off})/L = -[V_o - 2V_i - kV_i/(1-k)]/L$. Therefore,

$$kTV_i = (1-k)T\left(V_o - 2V_i - \frac{k}{1-k} V_i\right)$$

or

$$V_o = \frac{2}{1-k} V_i \tag{2.257}$$

and

$$I_o = \frac{1-k}{2} I_i \tag{2.258}$$

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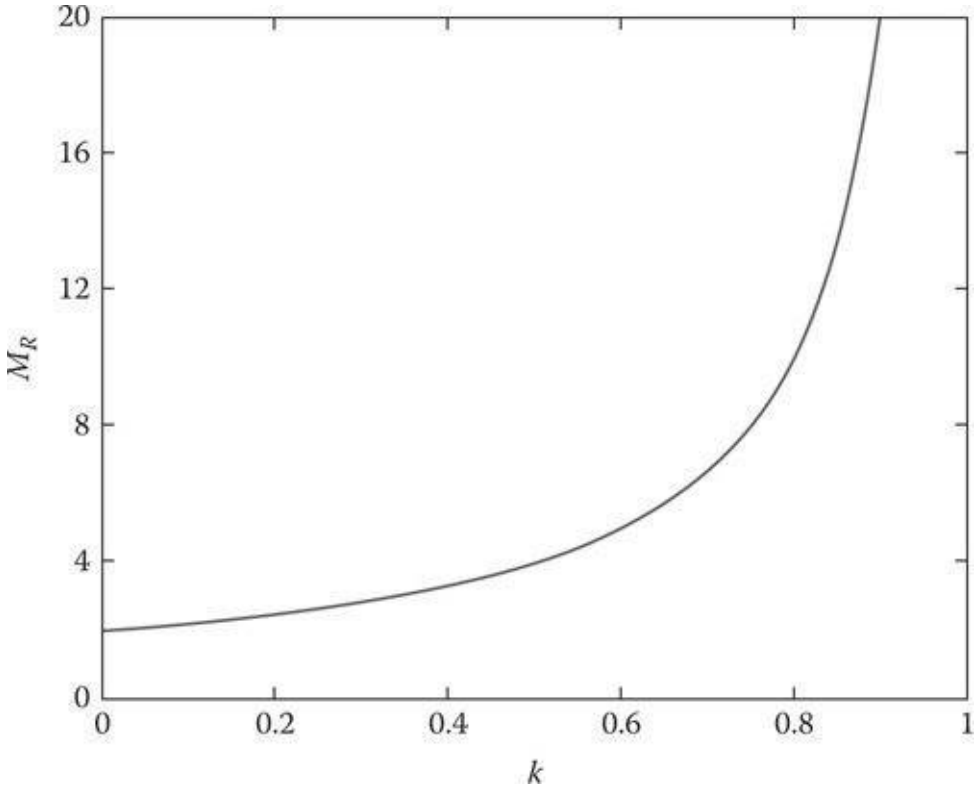


FIGURE 2.42
Voltage transfer gain M_R versus k.

The voltage transfer gain in continuous mode is

$$M_R = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{2}{1-k} \tag{2.259}$$

The curve of M_S versus k is shown in Figure 2.42.

Circuit *(C–LO–CO)* is a "Π"-type low-pass filter.

Therefore,

$$V_C = V_o = \frac{2}{1-k} V_i \tag{2.260}$$

2.4.3.3 Variations of Currents and Voltages

To analyze the variations of currents and voltages, some voltage and current waveforms are shown in Figure 2.43.

Current i_L increases and is supplied by V_i during switch-on. Thus, its peak-to-peak variation is

$$\Delta i_L = \frac{kTV_i}{L}$$

Considering Equation 2.253 and $R = V_o/I_o$, the variation ratio of the current i_L is

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$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_i T}{2LI_o} = \frac{k(1-k)R}{2M_R fL} = \frac{k}{M_R^2}\frac{R}{fL} \tag{2.261}$$

The peak-to-peak variation of current i_{L_1} is

$$\Delta i_{L_1} = \frac{k}{L_1} TV_i$$

The variation ratio of current i_{L_1} is

$$\chi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_i}{2L_1 I_o}(1-k) = \frac{k(1-k)}{2M_R}\frac{R}{fL_1} \tag{2.262}$$

The peak-to-peak variation of voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{k}{C} TI_o$$

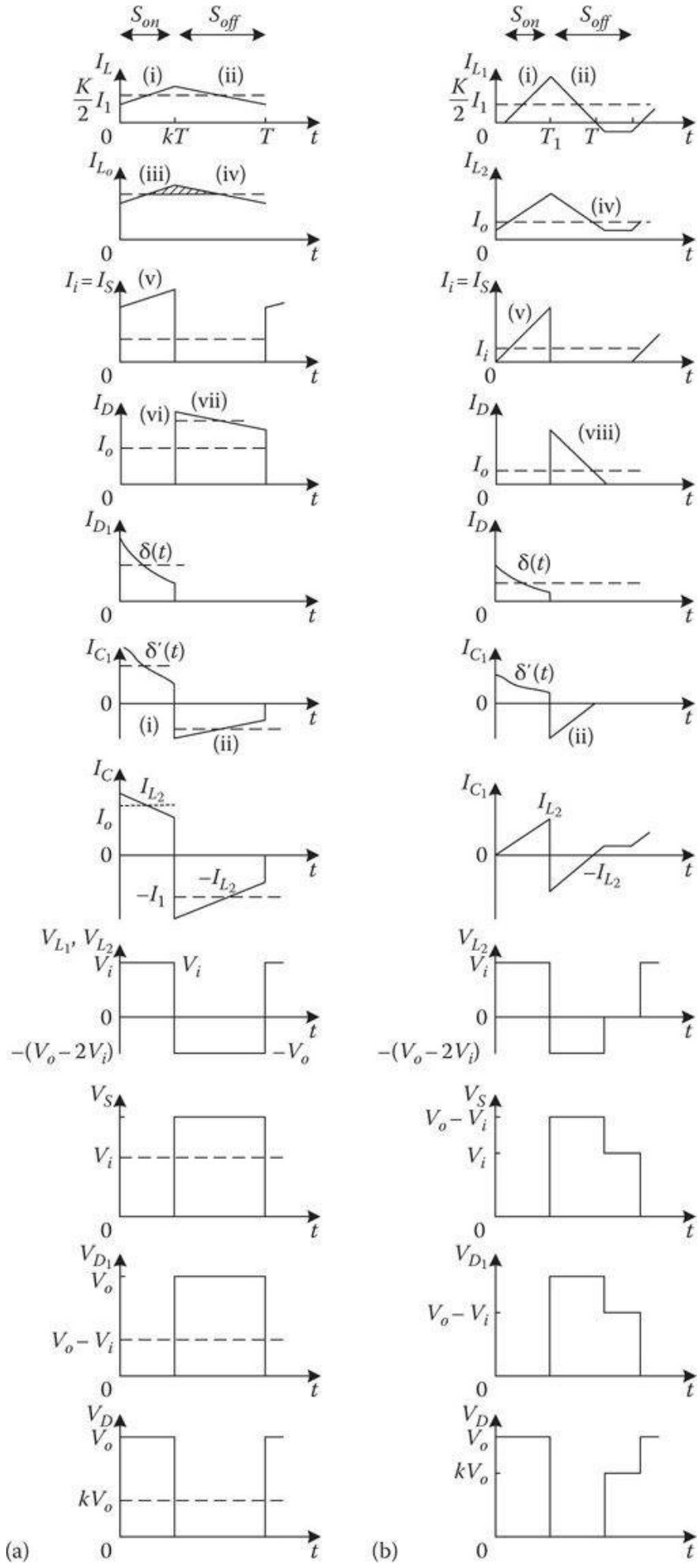
The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_o T}{2CV_o} = \frac{k}{2}\frac{1}{fCR} \tag{2.263}$$

The peak-to-peak variation of voltage v_{C_1} is

$$\Delta v_{C_1} = \frac{kT}{C_1} I_{C_1-on} = \frac{1}{fC} I_o$$

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FIGURE 2.43
Some voltage and current waveforms of re-lift circuit. (a) CCM operation. (b) DCM operation.

The variation ratio of voltage v_{C_1} is

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{I_o}{2fC_1V_i} = \frac{M_R}{2}\frac{1}{fC_1R} \tag{2.264}$$

Taking into account the same operation, the variation ratio of voltage v_{C_2} is

$$\sigma_2 = \frac{\Delta v_{C_2}/2}{V_{C_2}} = \frac{I_o}{2fC_2V_i} = \frac{M_R}{2}\frac{1}{fC_2R} \tag{2.265}$$

Considering Equation 2.211,

$$\Delta i_{L_o} = \frac{1}{2}\frac{T}{2}\frac{k}{2CL_o}TI_o = \frac{k}{8f^2CL_o}I_o$$

The variation ratio of current i_{L_o} is

$$\xi = \frac{\Delta i_{L_o}/2}{I_{L_o}} = \frac{k}{16}\frac{1}{f^2CL_o} \tag{2.266}$$

Considering Equation 2.213,

$$\Delta v_{C_o} = \frac{B}{C_o} = \frac{1}{2}\frac{T}{2}\frac{k}{16f^2CC_oL_o}I_o = \frac{k}{64f^3CC_oL_o}I_o$$

The variation ratio of current v_{C_o} is

$$\varepsilon = \frac{\Delta v_{C_o}/2}{V_{C_o}} = \frac{k}{128f^3CC_oL_o}\frac{I_o}{V_o} = \frac{k}{128}\frac{1}{f^3CC_oL_oR} \tag{2.267}$$

Assuming that $f = 50$ kHz, $L = L_o = 100$ μH, $C = C_o = 5$ μF, $R = 10$ Ω, and $k = 0.6$, we obtain

$$M_R = 5 \quad \zeta = 0.048, \quad \xi = 0.03, \quad \rho = 0.12, \quad \text{and} \quad \varepsilon = 0.0015.$$

The output voltage V_o is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_o(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_o = V_o/R$.

2.4.3.4 Instantaneous Values of the Currents and Voltages

Referring to Figure 2.43, the instantaneous current and voltage values are listed here:

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$$v_S = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o - \left(2 - \dfrac{k}{1-k}\right) V_i & \text{for } kT < t \le T \end{cases} \tag{2.268}$$

$$v_D = \begin{cases} V_o & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.269}$$

$$v_{D_1} = v_{D_2} = \begin{cases} 0 & \text{for } 0 < t \le kT \\ V_o & \text{for } kT < t \le T \end{cases} \tag{2.270}$$

$$v_{L_1} = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -\dfrac{k}{1-k} V_i & \text{for } kT < t \le T \end{cases} \tag{2.271}$$

$$v_L = \begin{cases} V_i & \text{for } 0 < t \le kT \\ -\left[V_o - \left(2 - \dfrac{k}{1-k}\right) V_i\right] & \text{for } kT < t \le T \end{cases} \tag{2.272}$$

$$i_i = i_S = \begin{cases} i_L(0) + \dfrac{V_i}{L} t + \delta_1(t) + \delta_2(t) + i_{L_1}(0) + \dfrac{V_i}{L_1} t & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.273}$$

$$i_L = \begin{cases} i_L(0) + \dfrac{V_i}{L} t & \text{for } 0 < t \le kT \\ i_L(kT) - \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right) V_i}{L} (t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.274}$$

$$i_{L_1} = \begin{cases} i_{L_1}(0) + \dfrac{V_i}{L_1} t & \text{for } 0 < t \le kT \\ i_{L_1}(kT) - \dfrac{\dfrac{k}{1-k} V_i}{L_1} (t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.275}$$

$$i_D = \begin{cases} 0 & \text{for } 0 < t \le kT \\ i_L(kT) - \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right) V_i}{L} (t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.276}$$

$$i_{D_1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.277}$$

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$$i_{D_2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \le kT \\ 0 & \text{for } kT < t \le T \end{cases} \tag{2.278}$$

$$i_{C_1} = \begin{cases} \delta_1(t) & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) + \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right)V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.279}$$

$$i_{C_2} = \begin{cases} \delta_2(t) & \text{for } 0 < t \le kT \\ -i_{L_1}(kT) + \dfrac{V_o - \left(2 - \dfrac{k}{1-k}\right)V_i}{L}(t - kT) & \text{for } kT < t \le T \end{cases} \tag{2.280}$$

$$i_C = \begin{cases} -I_{C-on} & \text{for } 0 < t \le kT \\ I_{C-off} & \text{for } kT < t \le T \end{cases} \tag{2.281}$$

where

$$i_L(0) = kI_i - kV_i/2fL$$

$$i_L(kT) = kI_i + kV_i/2fL$$

$$i_{L_1}(0) = kI_i - kV_i/2fL_1$$

$$i_{L_1}(kT) = kI_i + kV_i/2fL_1$$

Since the instantaneous currents i_{L_o} and i_{C_o} are partial parabolas with very small ripples, they are very nearly DC currents.

2.4.3.5 Discontinuous Mode

Referring to Figure 2.41d, we can see that the diode current i_D becomes zero during switch-off before the next period switch-on. The condition for discontinuous mode is $\zeta \ge 1$, that is,

$$\frac{k}{M_R^2}\frac{R}{fL} \ge 1$$

or

$$M_R \le \sqrt{k}\sqrt{\frac{R}{fL}} = \sqrt{k}\sqrt{z_N} \tag{2.282}$$

The graph of the boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.44. It can be seen that the boundary curve has a minimum value of 3.0 at $k = 1/3$.

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In this case, the current i_D exists in the period between kT and $t_1 = [k + (1 - k)m_R]T$, where m_R is the *filling efficiency*, and it is defined as

$$m_R = \frac{1}{\zeta} = \frac{M_R^2}{k\dfrac{R}{fL}} \tag{2.283}$$

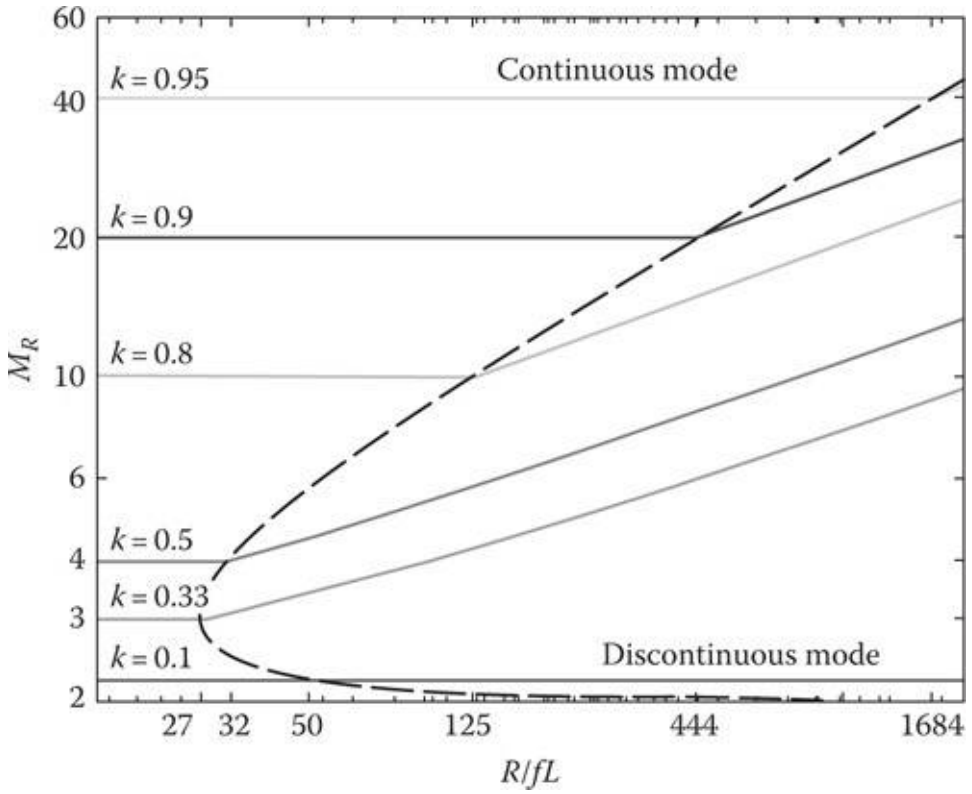


FIGURE 2.44
The boundary between continuous and discontinuous modes and output voltage versus the normalized load $z_N = R/fL$ (re-lift circuit).

Considering Equation 2.282, therefore $0 \le m_R < 1$. Because inductor current $i_{L_1} = 0$ at $t = t_1$, so that

$$V_{L_1-off} = \frac{k}{(1-k)m_R} V_i$$

Since the current i_D becomes zero at $t = t_1 = [k + (1 - k)m_R]T$, for the current i_L,

$$kTV_i = (1-k)m_R T\left(V_C - 2V_i - V_{L_1-off}\right)$$

or

$$V_C = \left[2 + \frac{2k}{(1-k)m_R}\right]V_i = \left[2 + k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{fL}} \ge \frac{2}{1-k}$$

and for the current i_{L_0},

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$$kT\left(V_i+V_C-V_o\right)=\left(1-k\right)m_R T\left(V_o-\ 2V_i-V_{L_1-off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o=\left[2+\frac{2k}{(1-k)m_R}\right]V_i=\left[2+k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{R}{fL}}\geq\frac{2}{1-k} \tag{2.284}$$

that is, the output voltage will linearly increase when load resistance R increases. The output voltage versus the normalized load $z_N = R/fL$ is shown in Figure 2.44. Larger load resistance R may cause higher output voltage in discontinuous mode.

2.4.4 Multiple-Lift Circuits

Referring to Figure 2.45, it is possible to build a multiple-lift circuit just only using the parts (L_1–C_2–D_2–D_{11}) multiple times. For example, in Figure 2.16, the parts (L_2–C_3–D_3–D_{12}) were added in the triple-lift circuit. According to this principle, triple-lift circuit and quadruple-lift circuit were built as shown in Figures 2.45 and 2.48. In this book, it is not necessary to introduce the particular analysis and calculations one by one to the readers. However, their calculation formulae are shown in this section.

2.4.4.1 Triple-Lift Circuit

The triple-lift circuit is shown in Figure 2.45. It consists of one static switch S; four inductors L, L_1, L_2, and L_o; five capacitors C, C_1, C_2, C_3, and C_o; and diodes. Circuit C_1–D_1– L_1–C_2–D_2–D_{11}–L_2–C_3–D_3–D_{12} is the lift circuit. Capacitors C_1, C_2, and C_3 perform characteristics to lift the capacitor voltage V_C by three times that of the source voltage V_i. L_1 and L_2 perform the function as ladder joints to link the three capacitors C_1, C_2, and C_3 and lift the capacitor voltage V_C up. Currents $i_{C_1}(t)$, $i_{C_2}(t)$, and $i_{C_3}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C_1}=v_{C_2}=v_{C_3}\cong V_i$ in steady state.

The output voltage and current are

$$V_o=\frac{3}{1-k}V_i \tag{2.285}$$

and

$$I_o=\frac{1-k}{3}I_i \tag{2.286}$$

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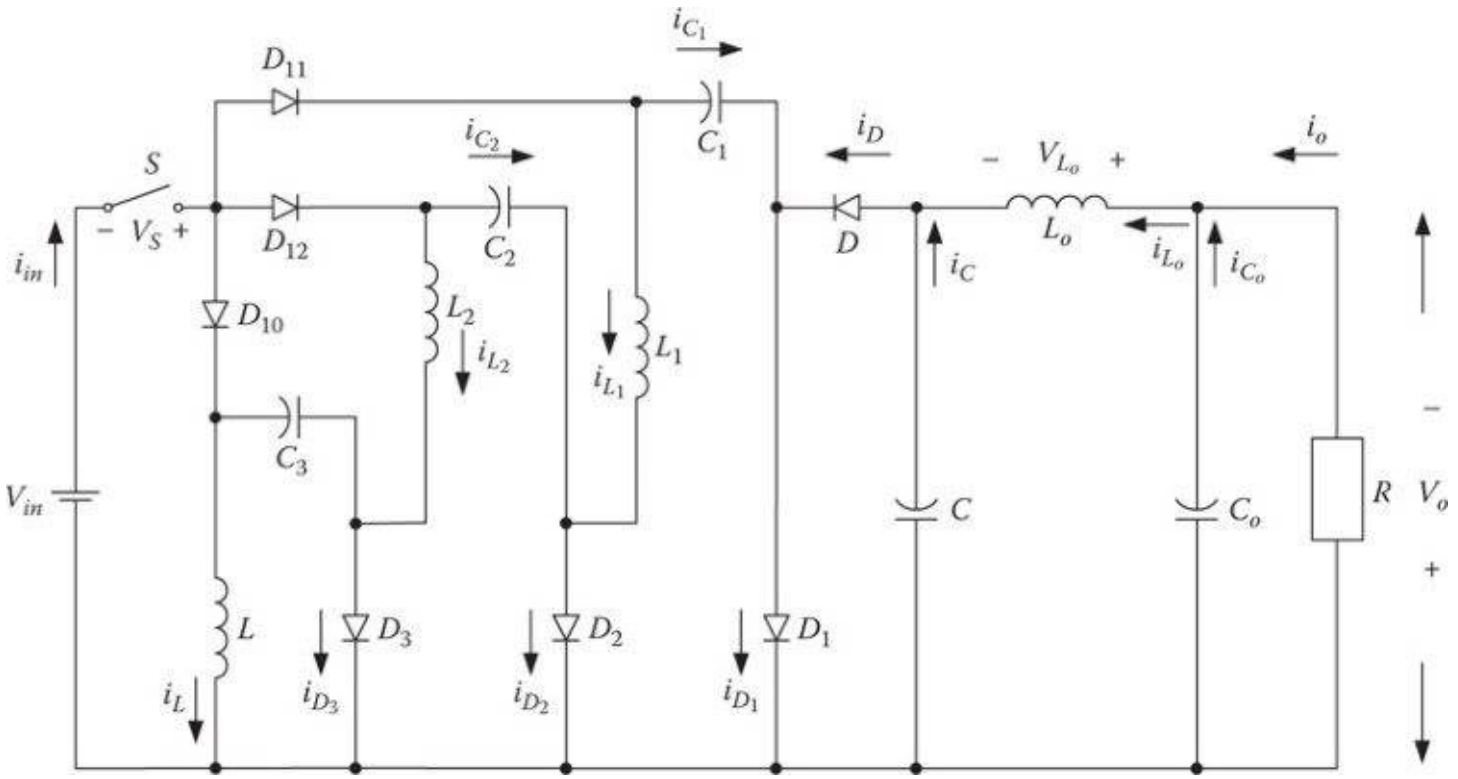


FIGURE 2.45
Triple-lift circuit.

The voltage transfer gain in continuous mode is

$$M_T = V_o / V_i = \frac{3}{1-k} \tag{2.287}$$

The curve of M_T versus k is shown in Figure 2.46.

Other average voltages are

$$V_C = V_o$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_i$$

Other average currents are

$$I_{L_o} = I_o$$

$$I_L = I_{L_1} = I_{L_2} = \frac{1}{1-k} I_o$$

The current variation ratios are

$$\zeta = \frac{k}{M_T^2} \frac{3R}{2fL} \qquad \xi = \frac{k}{16} \frac{1}{f^2 C L_o}$$

$$\chi_1 = \frac{k(1-k)}{2M_T} \frac{R}{fL_1} \qquad \chi_2 = \frac{k(1-k)}{2M_T} \frac{R}{fL_2}$$

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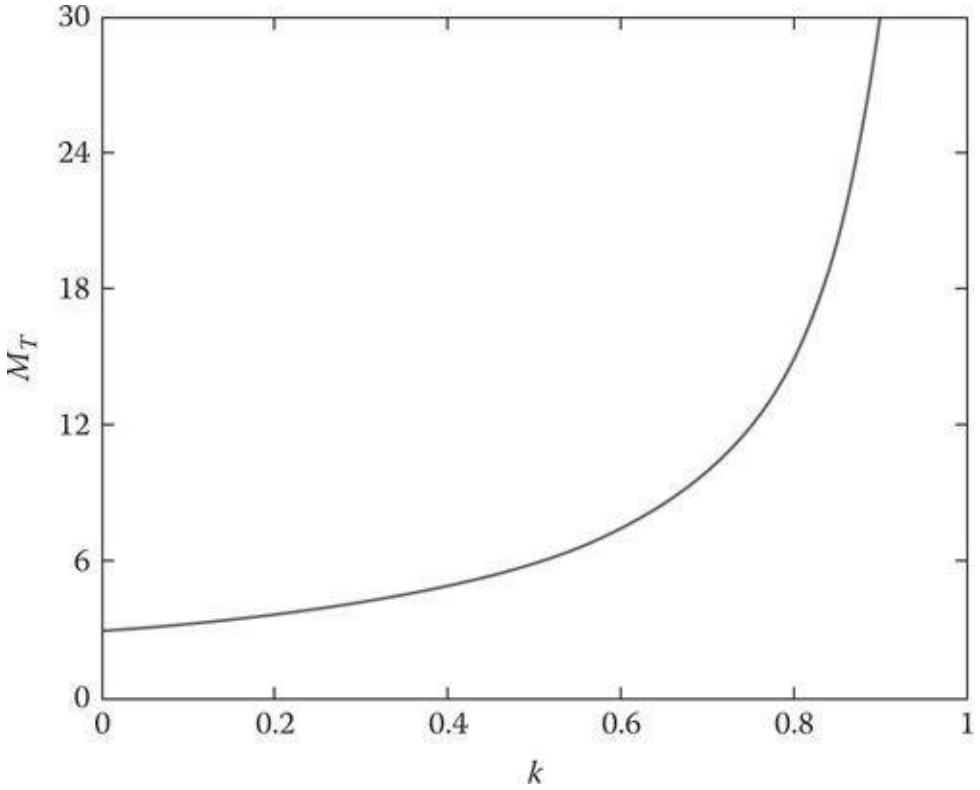


FIGURE 2.46
Voltage transfer gain of triple-lift circuit.

The voltage variation ratios are

$$\rho = \frac{k}{2}\frac{1}{fCR} \quad \sigma_1 = \frac{M_T}{2}\frac{1}{fC_1R}$$

$$\sigma_2 = \frac{M_T}{2}\frac{1}{fC_2R} \quad \sigma_3 = \frac{M_T}{2}\frac{1}{fC_3R}$$

The variation ratio of output voltage V_C is

$$\varepsilon = \frac{k}{128}\frac{1}{f^3CC_oL_oR} \tag{2.288}$$

The output voltage ripple is very small. The boundary between continuous and discontinuous modes is

$$M_T \le \sqrt{k}\sqrt{\frac{3R}{2fL}} = \sqrt{\frac{3kz_N}{2}} \tag{2.289}$$

It can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to k = 1/3. The boundary curve versus the normalized load $z_N = R/fL$ is shown in Figure 2.47.

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In discontinuous mode, the current i_D exists in the period between kT and $[k + (1 - k)m_T]T$, where m_T is the filling efficiency, that is,

$$m_T = \frac{1}{\zeta} = \frac{M_T^2}{k\dfrac{3R}{2fL}} \tag{2.290}$$

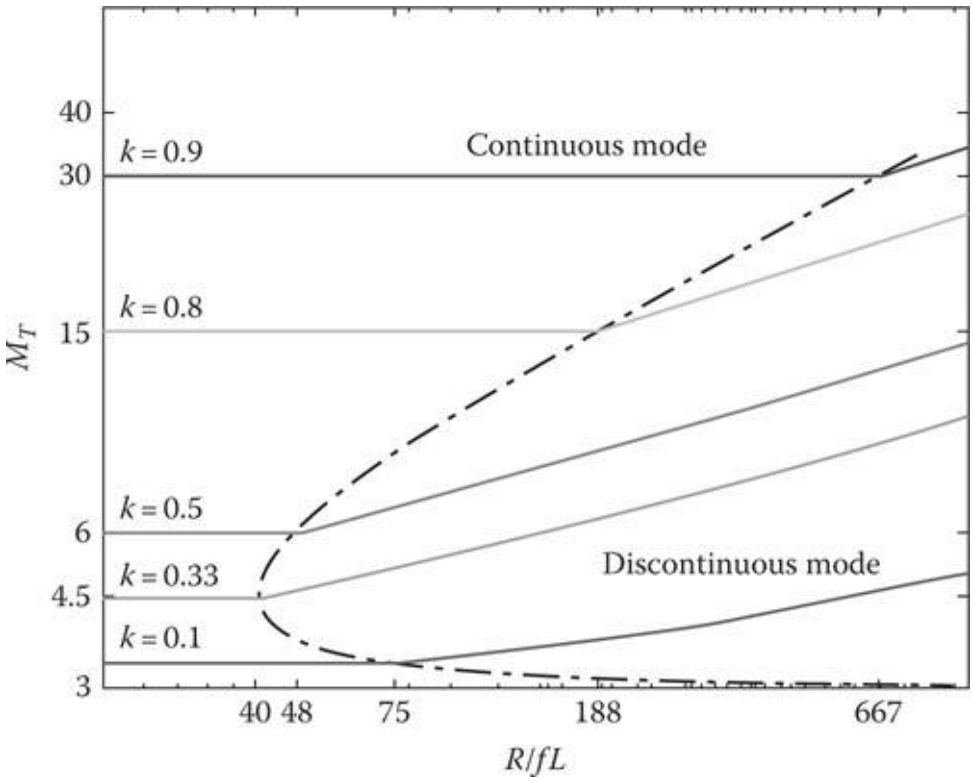


FIGURE 2.47
The boundary between continuous and discontinuous modes and output voltage versus the normalized load $z_N = R/fL$ (triple-lift circuit).

Considering Equation 2.289, therefore $0 < m_T < 1$. Because inductor current $i_{L_1} = i_{L_2} = 0$ at $t = t_1$, so that

$$V_{L_1-off} = V_{L_2-off} = \frac{k}{(1-k)m_T} V_i$$

Since the current i_D becomes zero at $t = t_1 = [k + (1 - k)m_T]T$, for the current i_L, we have

$$kTV_i = (1-k)m_T T\left(V_C - 3V_i - V_{L_1-off} - V_{L_2-off}\right)$$

or

$$V_C = \left[3 + \frac{3k}{(1-k)m_T}\right]V_i = \left[3 + k^2(1-k)\frac{R}{2fL}\right]V_i \quad \text{with } \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k}$$

and for the current i_{L_o}, we have

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$$kT\left(V_i + V_C - V_o\right) = \left(1-k\right) m_T T\left(V_o - 2V_i - V_{L_1\text{-}off} - V_{L_2\text{-}off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[3 + \frac{3k}{(1-k)m_T}\right] V_i = \left[3 + k^2(1-k)\frac{R}{2fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{3R}{2fL}} \geq \frac{3}{1-k} \tag{2.291}$$

that is, the output voltage will linearly increase when load resistance R increases. The output voltage versus the normalized load $z_N = R/fL$ is shown in Figure 2.47. We can see that the output voltage will increase when the load resistance R increases.

2.4.4.2 Quadruple-Lift Circuit

The quadruple-lift circuit is shown in Figure 2.48. It consists of one static switch S; five inductors L, L_1, L_2, L_3, and L_o; and six capacitors C, C_1, C_2, C_3, C_4, and C_0. Capacitors C_1, C_2, C_3, and C_4 perform characteristics to lift the capacitor voltage V_C by four times of source voltage V_i. L_1, L_2, and L_3 perform the function as ladder joints to link the four capacitors C_1, C_2, C_3, and C_4 and lift the output capacitor voltage V_C up. Currents $i_{C_1}(t)$, $i_{C_2}(t)$, $i_{C_3}(t)$ and $i_{C_4}(t)$ are exponential functions. They have large values at the moment of power on, but they are small because $v_{C_1} = v_{C_2} = v_{C_3} = v_{C_4} \cong V_i$ in steady state.

The output voltage and current are

$$V_o = \frac{4}{1-k} V_i \tag{2.292}$$

and

$$I_o = \frac{1-k}{4} I_i \tag{2.293}$$

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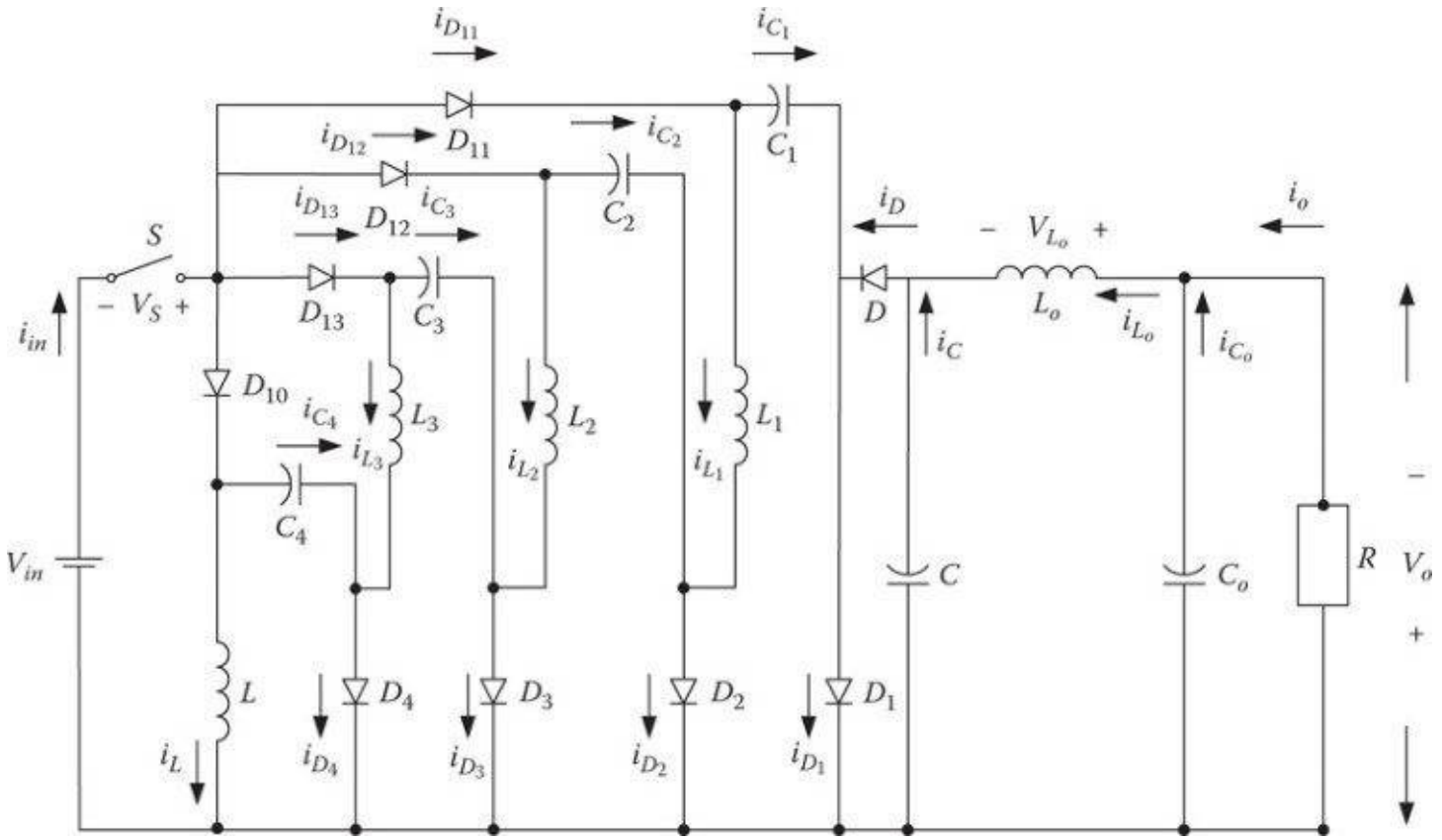


FIGURE 2.48
Quadruple-lift circuit.

The voltage transfer gain in continuous mode is

$$M_Q = \frac{V_o}{V_i} = \frac{4}{1-k} \tag{2.294}$$

The curve of M_Q versus k is shown in Figure 2.49.

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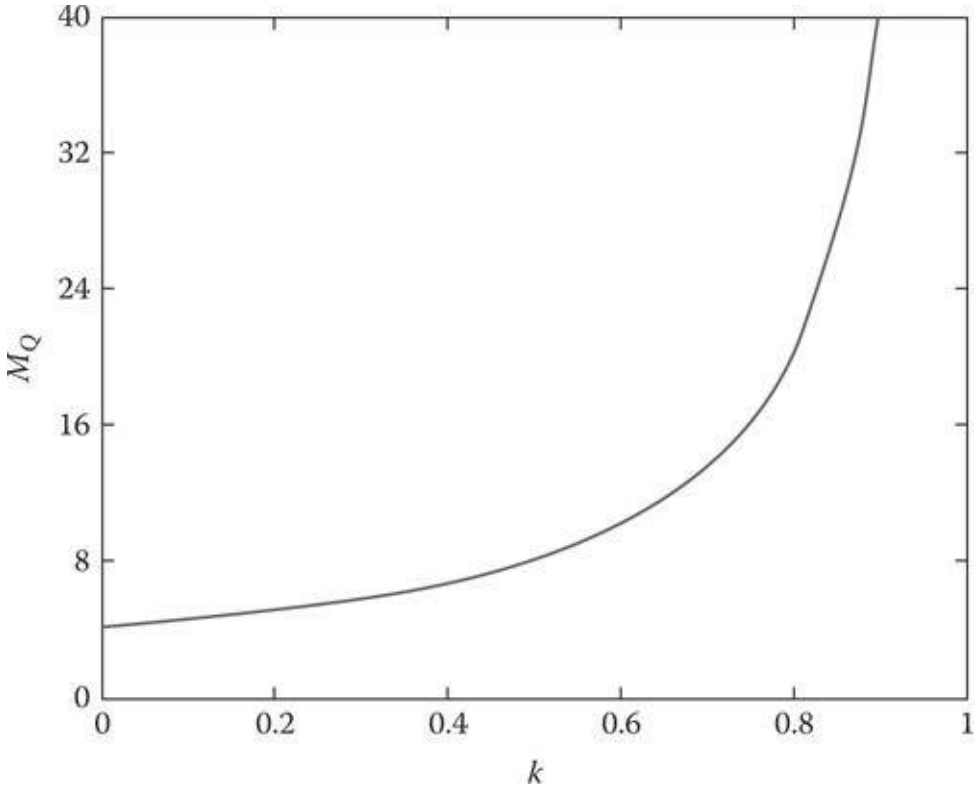


FIGURE 2.49
Voltage transfer gain of quadruple-lift circuit.

Other average voltages are

$$V_C = V_o$$

$$V_{C_1} = V_{C_2} = V_{C_3} = V_{C_4} = V_i$$

Other average currents are

$$I_{L_o} = I_o$$

$$I_L = I_{L_1} = I_{L_2} = I_{L_3} = \frac{1}{1-k} I_o$$

The current variation ratios are

$$\zeta = \frac{k}{M_Q^2} \frac{2R}{fL} \quad \xi = \frac{k}{16} \frac{1}{f^2 C L_o}$$

$$\chi_1 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_1} \quad \chi_2 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_2} \quad \chi_3 = \frac{k(1-k)}{2M_Q} \frac{R}{fL_3}$$

The voltage variation ratios are

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$$\rho = \frac{k}{2}\frac{1}{fCR} \quad \sigma_1 = \frac{M_Q}{2}\frac{1}{fC_1R}$$

$$\sigma_2 = \frac{M_Q}{2}\frac{1}{fC_2R} \quad \sigma_3 = \frac{M_Q}{2}\frac{1}{fC_3R} \quad \sigma_4 = \frac{M_Q}{2}\frac{1}{fC_4R}$$

The variation ratio of output voltage V_C is

$$\varepsilon = \frac{k}{128}\frac{1}{f^3CC_oL_oR} \tag{2.295}$$

The output voltage ripple is very small. The boundary between continuous mode and DCM is

$$M_Q \le \sqrt{k}\sqrt{\frac{2R}{fL}} = \sqrt{2kz_N} \tag{2.296}$$

It can be seen that the boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$. The boundary curve is shown in Figure 2.50.

In discontinuous mode, the current i_D exists in the period between kT and $[k + (1 - k)m_Q]T$, where m_Q is the filling efficiency, that is,

$$m_Q = \frac{1}{\zeta} = \frac{M_Q^2}{k\dfrac{2R}{fL}} \tag{2.297}$$

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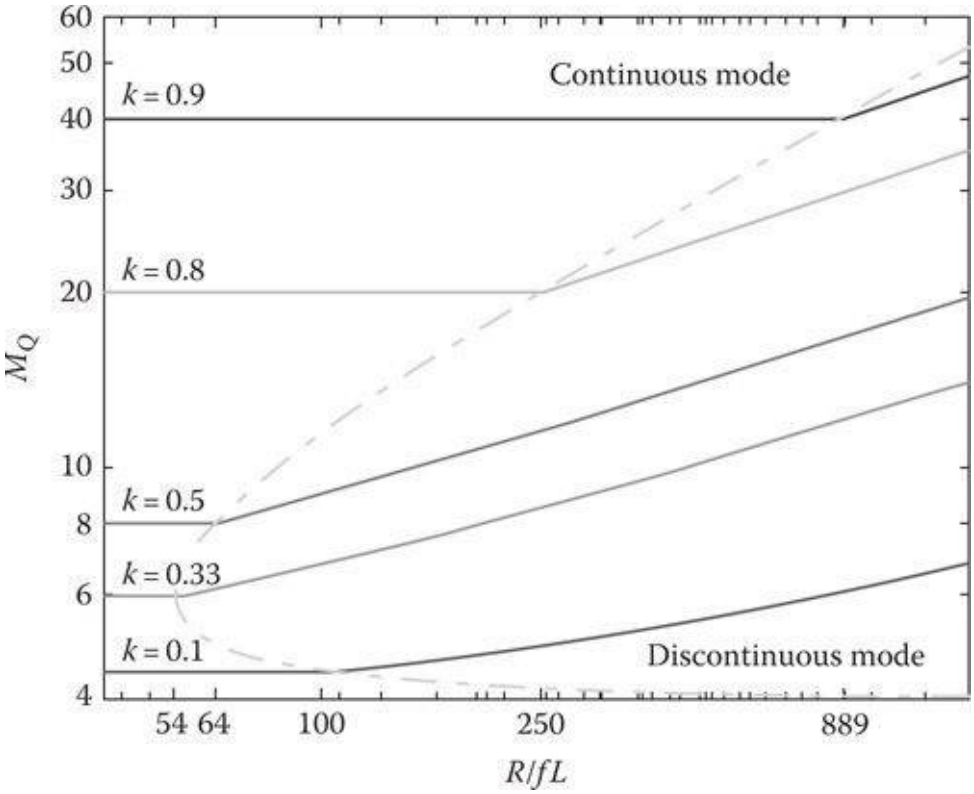


FIGURE 2.50
The boundary between continuous and discontinuous modes and output voltage versus the normalized load $z_N = R/fL$ (quadruple-lift circuit).

Considering Equation 2.296, therefore $0 < M_Q < 1$. Because inductor current $i_{L_1} = i_{L_2} = i_{L_3} = 0$ at $t = t_1$, so that

$$V_{L_1-off} = V_{L_2-off} = V_{L_3-off} = \frac{k}{(1-k)m_Q} V_i$$

Since the current i_D becomes zero at $t = t_1 = kT + (1-k)m_Q T$, for the current i_L, we have

$$kTV_i = (1-k)m_Q T\left(V_C - 4V_i - V_{L_1-off} - V_{L_2-off} - V_{L_3-off}\right)$$

or

$$V_C = \left[4 + \frac{4k}{(1-k)m_Q}\right] V_i = \left[4 + k^2(1-k)\frac{R}{2fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k}$$

and for the current i_{L_o}, we have

$$kT\left(V_i + V_C - V_o\right) = (1-k)m_Q T\left(V_o - 2V_i - V_{L_1-off} - V_{L_2-off} - V_{L_3-off}\right)$$

Therefore, the output voltage in discontinuous mode is

$$V_o = \left[4 + \frac{4k}{(1-k)m_Q}\right] V_i = \left[4 + k^2(1-k)\frac{R}{2fL}\right] V_i \quad \text{with } \sqrt{k}\sqrt{\frac{2R}{fL}} \geq \frac{4}{1-k} \qquad (2.298)$$

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that is, the output voltage will linearly increase while load resistance R increases. The output voltage versus the normalized load $Z_N = R/fL$ is shown in Figure 2.50. We can see that the output voltage will increase while the load resistance R increases.

2.4.5 Summary

From the analysis and calculation in the previous sections, the common formulae can be obtained for all circuits:

$$M = \frac{V_o}{V_i} = \frac{I_i}{I_o} \quad z_N = \frac{R}{fL} \quad R = \frac{V_o}{I_o}$$

The current variation ratios are

$$\zeta = \frac{k(1-k)R}{2MfL} \quad \xi = \frac{k}{16f^2CL_o}$$

$$\chi_i = \frac{k(1-k)R}{2MfL_i} \quad (i = 1,2,3,\ldots,n-1)\, n \geq 2$$

The voltage variation ratios are

$$\rho = \frac{k}{2fCR} \quad \varepsilon = \frac{k}{128f^3CC_oL_oR} \quad \sigma_j = \frac{M}{2fC_jR} \quad (j = 1,2,3,4,\ldots,n)\, n \geq 1$$

where

i and j are the inductors' and capacitors' number
n is the stage number

In order to write common formulae for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript $n = 0$ means the elementary circuit, subscript $n = 1$ means the self-lift circuit, subscript $n = 2$ means the self-lift circuit, subscript $n = 3$ means the triple-lift circuit, subscript $n = 4$ means the quadruple-lift circuit, and so on. Therefore, the voltage transfer gain in the continuous CCM for all circuits is

$$M_n = \frac{n + kh(n)}{1-k} \quad n = 0,1,2,3,4,\ldots \tag{2.299}$$

The variation of the freewheeling diode current i_D is

$$\zeta_n = \frac{k^{[1+h(n)]}}{M_n^2} \frac{n + h(n)}{2} z_N \tag{2.300}$$

The boundaries are determined by the condition

$$\zeta_n \geq 1$$

or

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$$\frac{k^{[1+h(n)]}}{M_n^2}\frac{n+h(n)}{2}z_N \geq 1 \quad n=0,1,2,3,4,\ldots \tag{2.301}$$

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

$$M_n = k^{\frac{1+h(n)}{2}}\sqrt{\frac{n+h(n)}{2}z_N} \quad n=0,1,2,3,4,\ldots \tag{2.302}$$

The filling efficiency is

$$m_n = \frac{1}{\zeta_n} = \frac{M_n^2}{k^{[1+h(n)]}}\frac{2}{n+h(n)}\frac{1}{z_N} \tag{2.303}$$

The voltage across the capacitor C in discontinuous mode for all circuits is

$$V_{C-n} = \left[n + k^{[2-h(n)]}\frac{1-k}{2}z_N\right]V_i \quad n=0,1,2,3,4,\ldots \tag{2.304}$$

The output voltage in discontinuous mode for all circuits is

$$V_{o-n} = \left[n + k^{[2-h(n)]}\frac{1-k}{2}z_N\right]V_i \quad n=0,1,2,3,4,\ldots \tag{2.305}$$

where $h(n) = \begin{cases} 0 & \text{if} \quad n \geq 1 \\ 1 & \text{if} \quad n = 0 \end{cases}$ is the *Hong function*.

The voltage transfer gains in continuous mode for all circuits are shown in Figure 2.51. The boundaries between continuous and discontinuous modes of all circuits are shown in Figure 2.52. The curves of all M versus z_N state that the continuous mode area increases from M_E via M_S, M_r, and M_T to M_Q. The boundary of elementary circuit is monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other circuits, which of M_S, M_R, M_T, and M_Q correspond at $k = 1/3$.

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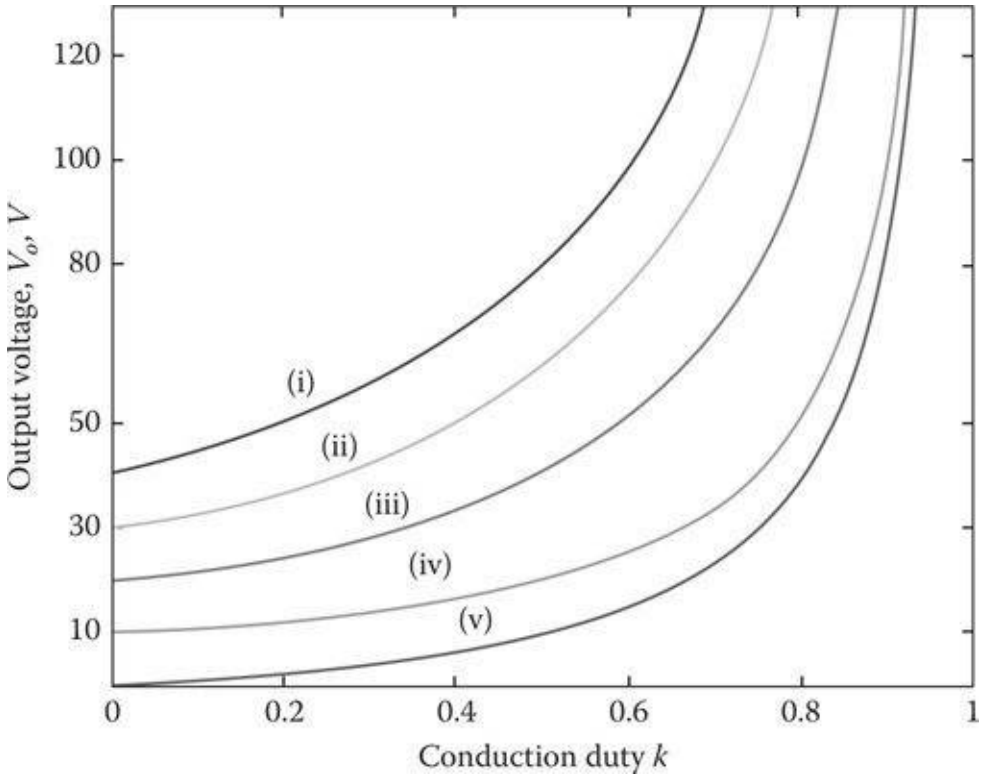


FIGURE 2.51
Output voltages of all negative-output Luo-converters (V_i = 10 V).

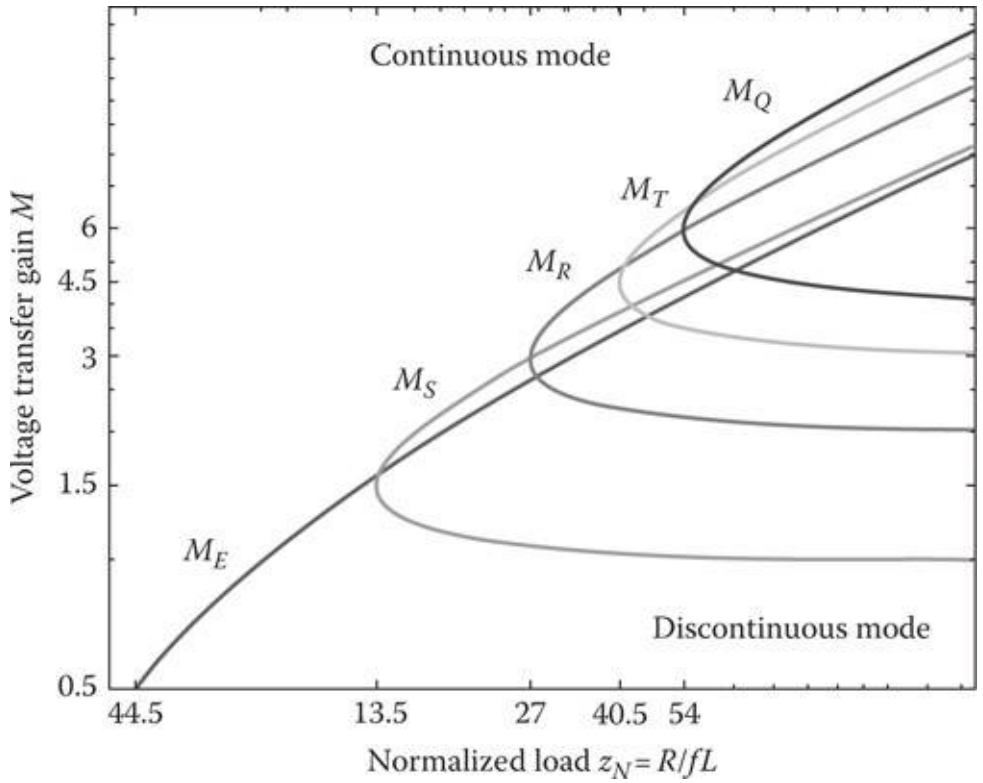


FIGURE 2.52
Boundaries between continuous and discontinuous modes of all negative-output Luo-converters.

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Assuming that $f = 50$ kHz, $L = L_o = L_1 = L_2 = L_3 = L_4 = 100$ μH, $C = C_1 = C_2 = C_3 = C_4 = C_o = 5$ μF, and the source voltage $V_i = 10$ V, the value of the output voltage V_o in various conduction duty k is shown in Figure 2.22. Typically, some values of the output voltage V_o in conduction duty k = 0.33, 0.5, 0.75, and 0.9 are listed in Table 2.2. The ripple of the output voltage is very small, say smaller than 1%. For example, using the data given earlier and $R = 10$ Ω, the variation ratio of the output voltage is $\varepsilon = 0.0025 \times k = 0.0008$, 0.0012, 0.0019, and 0.0023, respectively. From these data, the fact we find is that the output voltage of all N/O Luo-converters is almost a real DC voltage with very small ripple.

TABLE 2.2
Comparison among Five Negative-Output Luo-Converters

			V_o (V_i = 10 V)			
Negative-Output Luo-Converters	I_o	V_o	k = 0.33	k = 0.5	k = 0.75	k = 0.9
Elementary circuit	$I_o = \frac{1-k}{k} I_i$	$V_o = \frac{k}{1-k} V_i$	5 V	10 V	30 V	90 V
Self-lift circuit	$I_o = (1-k) I_i$	$V_o = \frac{1}{1-k} V_i$	15 V	20 V	40 V	100 V
Re-lift circuit	$I_o = \frac{1-k}{2} I_i$	$V_o = \frac{2}{1-k} V_i$	30 V	40 V	80 V	200 V
Triple-lift circuit	$I_o = \frac{1-k}{3} I_i$	$V_o = \frac{3}{1-k} V_i$	45 V	60 V	120 V	300 V
Quadruple-lift circuit	$I_o = \frac{1-k}{4} I_i$	$V_o = \frac{4}{1-k} V_i$	60 V	80 V	160 V	400 V

2.5 Modified P/O Luo-Converters

N/O Luo-converters perform the voltage conversion from positive to negative voltages using VL technique with only one switch S. This section introduces the technique to modify P/O Luo-converters that can employ only *one* switch for all circuits. Five circuits have been introduced in the literature:

1. Elementary circuit
2. Self-lift circuit
3. Re-lift circuit
4. Triple-lift circuit
5. Quadruple-lift circuit

There are five circuits introduced in this section, namely, the elementary circuit, self-lift circuit, re-lift circuit, and multiple-lift circuit (triple-lift and quadruple-list circuits). In all

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circuits, the switch S is a PMOS. It is driven by PWM switching signal with variable frequency f and conduction duty k. For all circuits, the load is usually resistive, $R = V_o/I_o$. We concentrate on the absolute values rather than on the polarity in the following descriptions and calculations. The directions of all voltages and currents are defined and shown in the figures. We will assume that all the components are ideal and the capacitors are large enough. We also assume that the circuits operate in CCM. The output voltage and current are V_o and I_o; the input voltage and current are V_i and I_i.

2.5.1 Elementary Circuit

The elementary circuit is shown in Figure 2.10. It is the elementary circuit of P/O Luo-converters. The output voltage and current and the voltage transfer gain are

$$V_o = \frac{k}{1-k} V_i$$

$$I_o = \frac{1-k}{k} I_i$$

$$M_E = \frac{k}{1-k}$$

The average voltage is

$$V_C = V_o.$$

The average currents are

$$I_{L_o} = I_o \quad I_L = \frac{k}{1-k} I_o.$$

2.5.2 Self-Lift Circuit

The self-lift circuit is shown in Figure 2.53. It is derived from the elementary circuit. In steady state, the average inductor voltages over a period are zero. Thus,

$$V_{C_1} = V_{C_o} = V_o \tag{2.306}$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_i and $-V_C$.

Therefore,

$$kTV_i = (1-k)TV_C$$

Hence,

$$V_C = \frac{k}{1-k} V_i \tag{2.307}$$

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During switch-on period, the voltage across capacitor C_1 is equal to the source voltage plus the voltage across C. Since we assume that C and C_1 are sufficiently large,

$$V_{C_1} = V_i + V_C$$

Therefore,

$$V_{C_1} = V_i + \frac{k}{1-k} V_i = \frac{1}{1-k} V_i$$

$$V_o = V_{C_o} = V_{C_1} = \frac{1}{1-k} V_i$$

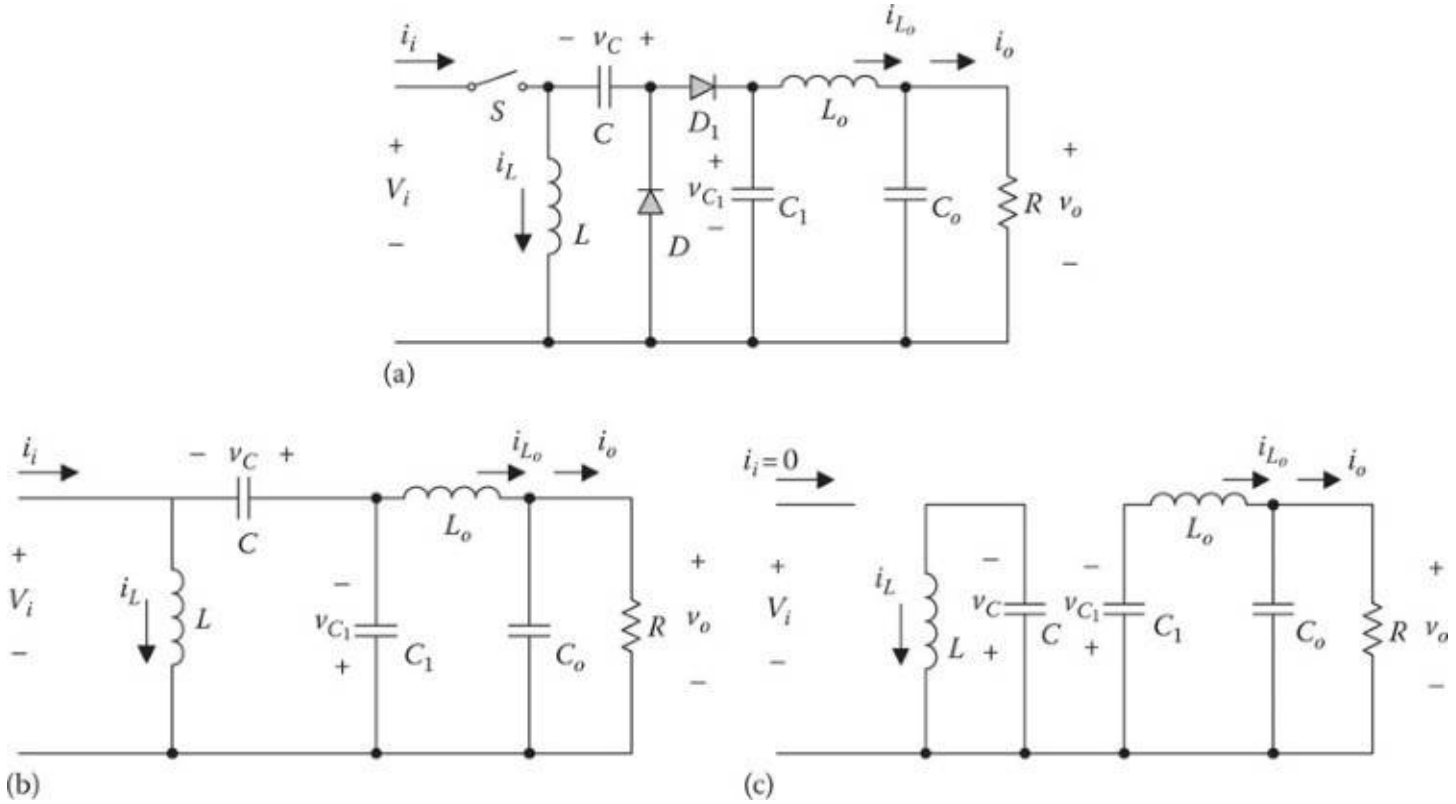


FIGURE 2.53
Modified self-lift circuit and its equivalent circuit. (a) Self-lift circuit. (b) Switch-on equivalent circuit. (c) Switch-off equivalent circuit.

The voltage transfer gain of CCM is

$$M = \frac{V_o}{V_i} = \frac{1}{1-k}$$

The output voltage and current and the voltage transfer gain are

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$$V_o = \frac{1}{1-k} V_i$$

$$I_o = (1-k) I_i$$

$$M_S = \frac{1}{1-k} \tag{2.308}$$

The average voltages are

$$V_C = kV_o$$

$$V_{C_1} = V_o$$

The average currents are

$$I_{L_o} = I_o$$

$$I_L = \frac{1}{1-k} I_o$$

We also implement the breadboard prototype of the proposed self-lift circuit. NMOS IRFP460 is used as the semiconductor switch. The diode is MR824. The other parameters are

$$V_i = 0 \sim 30 \text{ V}$$

$$R = 30 \sim 340\ \Omega$$

$$k = 0.1 \sim 0.9$$

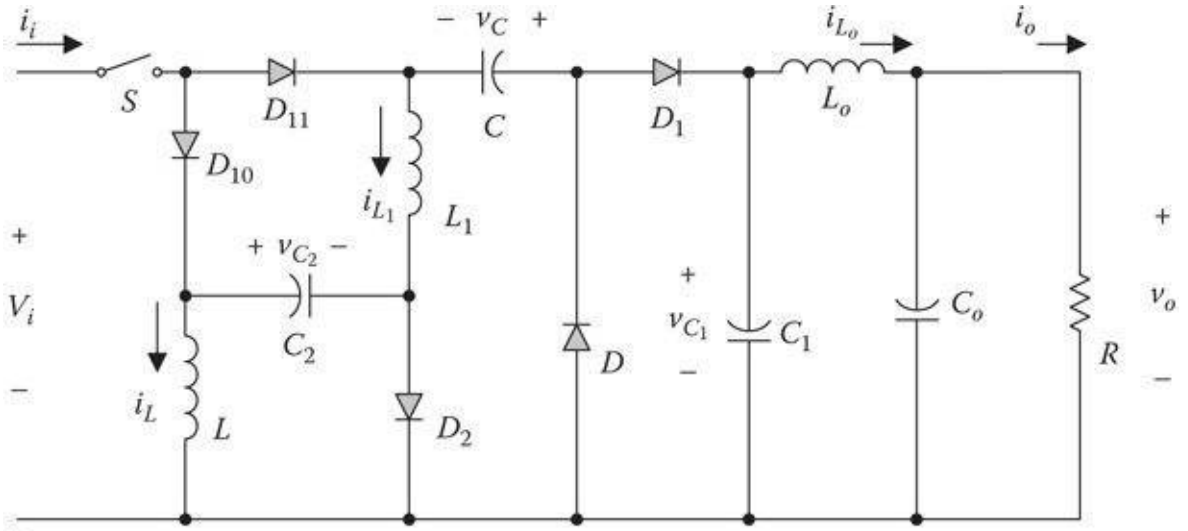
$$C = C_o = 100\ \mu\text{F}$$

$$L = 470\ \mu\text{H}$$

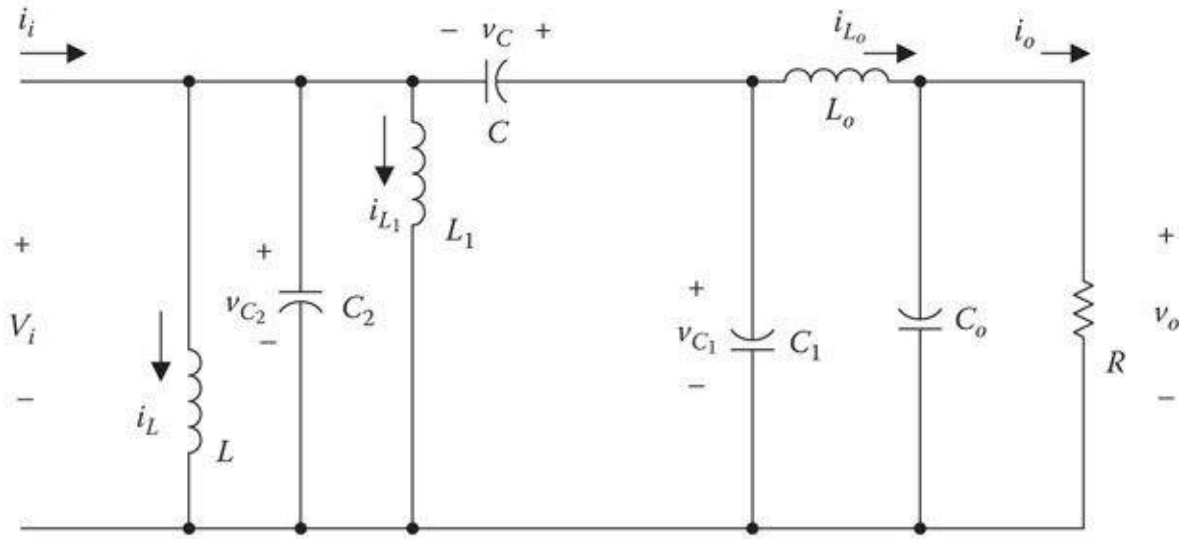
2.5.3 Re-Lift Circuit

The re-lift circuit and its equivalent circuits are shown in Figure 2.54. It is derived from the self-lift circuit. The function of capacitors C_2 is to lift the voltage v_c by source voltage V_i; the function of inductor L_1 acts like a hinge of the foldable ladder (capacitor C_2) to lift the voltage v_c during switch-off.

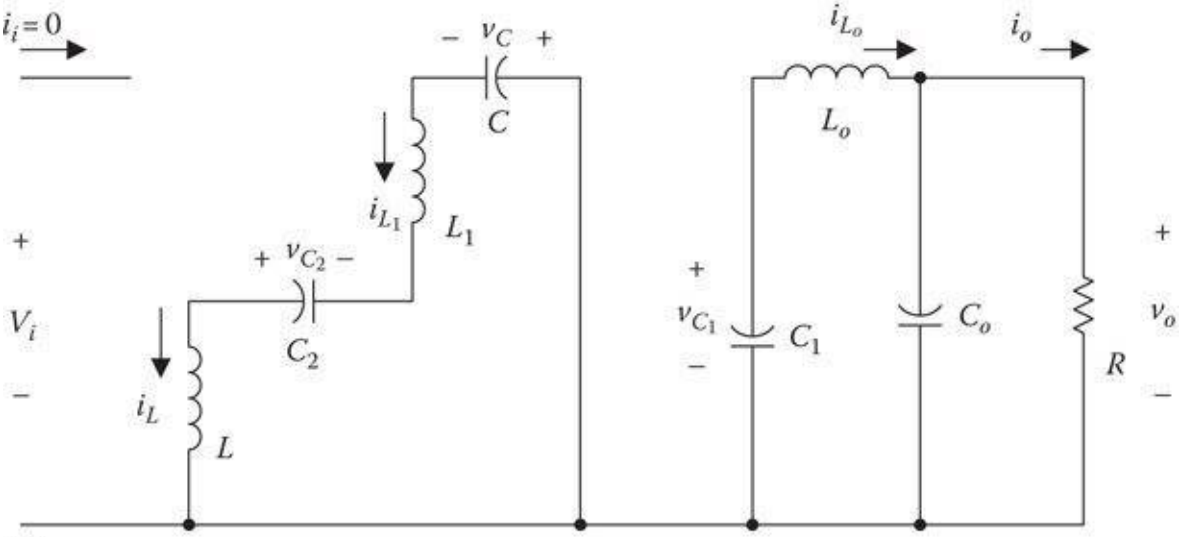
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(a)



(b)



(c)

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FIGURE 2.54
Modified re-lift circuit. (a) Re-lift circuit. (b) Switch-on equivalent circuit. (c) Switch-off equivalent circuit.

In steady state, the average inductor voltages over a period are zero. Thus,

$$V_{C_1} = V_{C_o} = V_o$$

Since we assume C_2 is large enough and C_2 is biased by the source voltage V_i during switch-on period, thus

$$V_{C_2} = V_i$$

From the switch-on equivalent circuit, another capacitor voltage equation can also be derived since we assume all the capacitors to be large enough,

$$V_o = V_{C_1} = V_C + V_i$$

The inductor current i_L increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L are V_i and $-V_{L-off}$.

Therefore,

$$kTV_i = (1-k)TV_{L-off}$$

Hence,

$$V_{L-off} = \frac{k}{1-k}V_i$$

The inductor current i_{L_1} increases in the switch-on period and decreases in the switch-off period. The corresponding voltages across L_1 are V_i and $-V_{L-off}$.

Therefore,

$$kTV_i = (1-k)TV_{L_1-off}$$

Hence,

$$V_{L_1-off} = \frac{k}{1-k}V_i$$

From the switch-off period equivalent circuit,

$$V_C = V_{C-off} = V_{L-off} + V_{L_1-off} + V_{C_2}$$

Therefore,

$$V_C = \frac{k}{1-k}V_i + \frac{k}{1-k}V_i + V_i = \frac{1+k}{1-k}V_i \tag{2.309}$$

$$V_o = \frac{1+k}{1-k}V_i + V_i = \frac{2}{1-k}V_i$$

Then we get the voltage transfer ratio in CCM:

$$M = M_R = \frac{2}{1-k} \tag{2.310}$$

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The following is a brief summary of the main equations for the re-lift circuit. The output voltage and current and gain are

$$V_o = \frac{2}{1-k} V_i$$

$$I_o = \frac{1-k}{2} I_i$$

$$M_R = \frac{2}{1-k}$$

The average voltages are

$$V_C = \frac{1+k}{1-k} V_i$$

$$V_{C_1} = V_{C_o} = V_o$$

$$V_{C_2} = V_i$$

The average currents are

$$I_{L_o} = I_o$$

$$I_L = I_{L_1} = \frac{1}{1-k} I_o$$

2.5.4 Multiple-Lift Circuit

Multiple-lift circuits are derived from re-lift circuits by repeating the section of L_1–C_1–$D_1$by multiple times. For example, triple-lift circuit is shown in Figure 2.55. The function of capacitors C_2 and C_3 is to lift the voltage v_C across capacitor C by twice the source voltage $2V_i$; the function of inductors L_1 and L_2 acts like hinges of the foldable ladder (capacitors C_2 and C_3) to lift the voltage v_C during switch-off.

The output voltage and current and voltage transfer gain are

$$V_o = \frac{3}{1-k} V_i$$

and

$$I_o = \frac{1-k}{3} I_i$$

$$M_T = \frac{3}{1-k} \tag{2.311}$$

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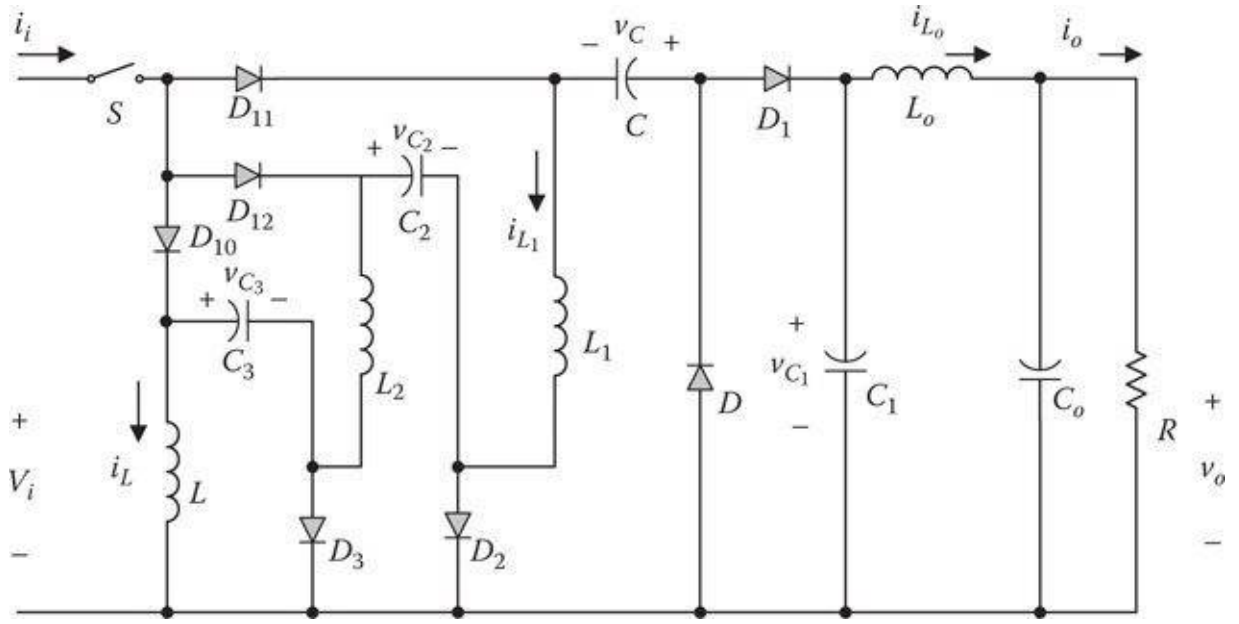


FIGURE 2.55
Modified triple-lift circuit.

Other average voltages are

$$V_C = \frac{2+k}{1-k} V_i$$

$$V_{C_1} = V_o$$

$$V_{C_2} = V_{C_3} = V_i$$

Other average currents are

$$I_{L_o} = I_o$$

$$I_{L_1} = I_{L_2} = I_L = \frac{1}{1-k} I_o$$

The quadruple-lift circuit is shown in Figure 2.56. The function of capacitors C_2, C_3, and C_4 is to lift the voltage v_C across capacitor C by three times of source voltage $3V_i$. The function of inductors L_1, L_2, and L_3 acts like hinges of the foldable ladder (capacitors C_2, C_3, and C_4) to lift the voltage v_C during switching-off. The output voltage and current and voltage transfer gain are

$$V_o = \frac{4}{1-k} V_i$$

and

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$$I_o = \frac{1-k}{4} I_i$$

$$M_Q = \frac{4}{1-k} \tag{2.312}$$

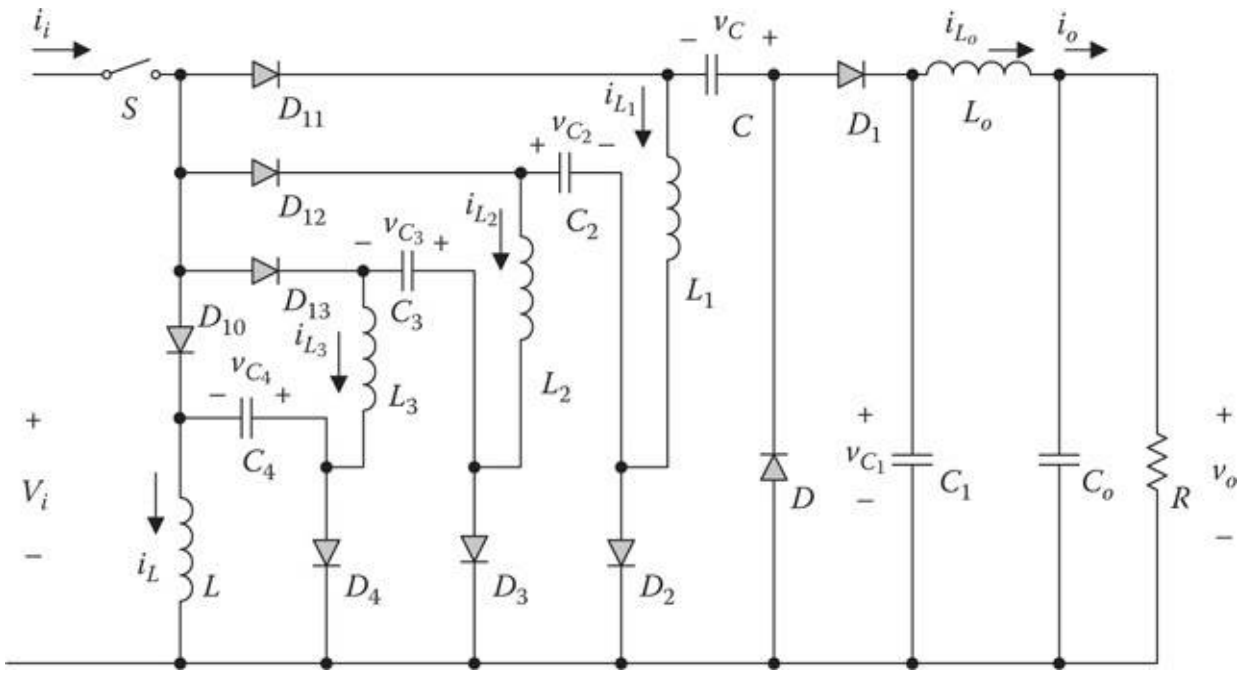


FIGURE 2.56
Modified quadruple-lift circuit.

The average voltages are

$$V_C = \frac{3+k}{1-k} V_i$$

and

$$V_{C_1} = V_o$$

$$V_{C_2} = V_{C_3} = V_{C_4} = V_i$$

The average currents are

$$I_{L_o} = I_o$$

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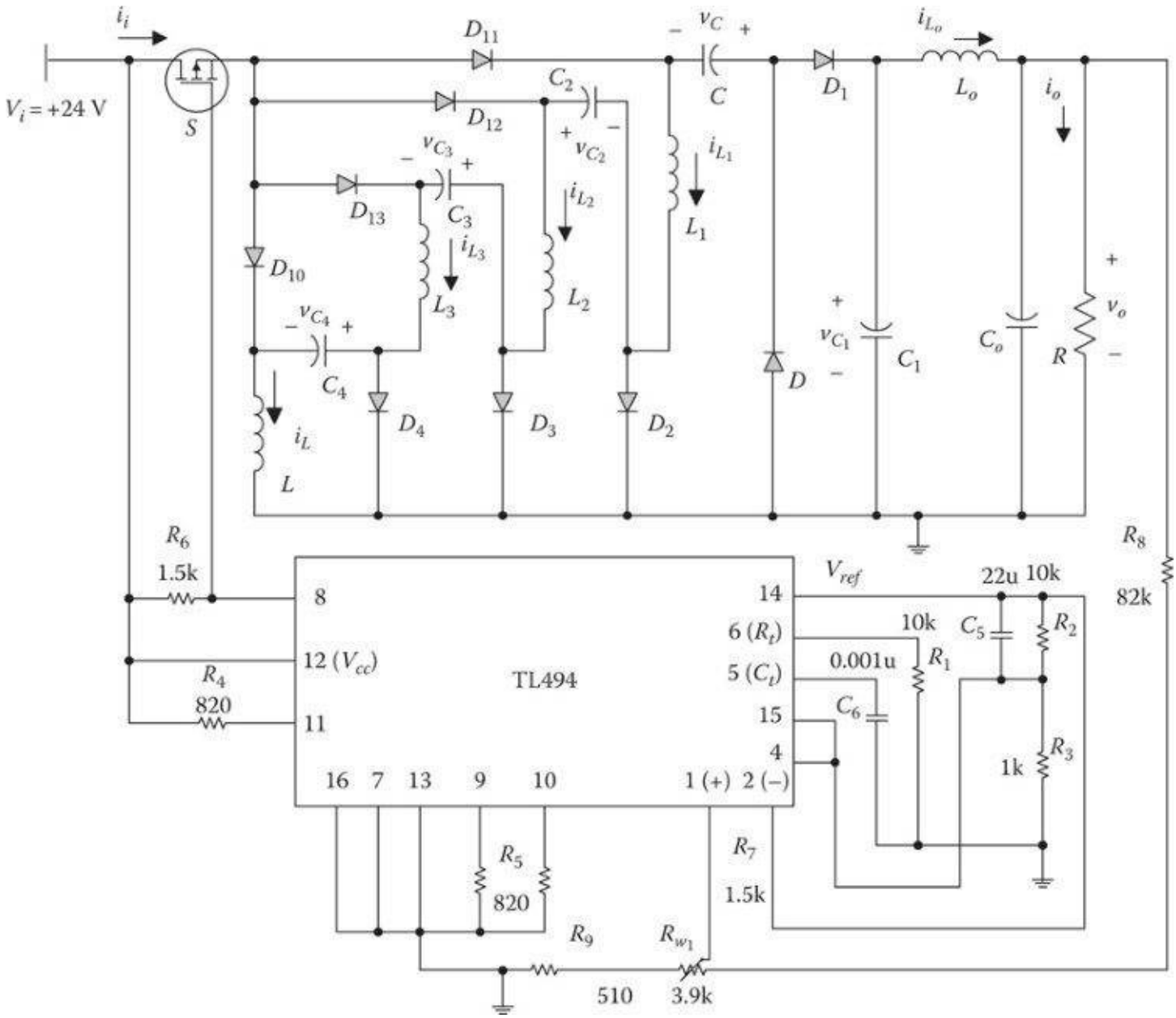


FIGURE 2.57
A high-voltage testing power supply.

and

$$I_L = \frac{k}{1-k} I_o$$

$$I_{L_1} = I_{L_2} = I_{L_3} = I_L + I_{L_o} = \frac{1}{1-k} I_o$$

2.5.5 Application

A high-efficiency, widely adjustable high-voltage-regulated power supply (HVRPS) is designed to use these Luo-converters in a high-voltage test rig. The proposed HVRPS is shown in Figure 2.57. The HVRPS was constructed by using a PWM IC TL494 to implement

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closed-loop control together with the modified P/O Luo-converters. Its output voltage is basically a DC value with small ripple and can be widely adjustable. The source voltage is 24 V DC, and the output voltage can vary from 36 to 1000 V DC. The measured experimental results show that the efficiency can be as high as 95% and the source effect ratio is about 0.001, and the load effect ratio is about 0.005.

2.6 Double-Output Luo-Converters

Mirror-symmetrical double-output voltages are specially required in industrial applications and computer periphery circuits. Double-output DC/DC Luo-converters can convert the positive input source voltage to P/O and N/O voltages. It consists of two conversion paths. Double-output Luo-converters perform from positive to positive and negative DC/DC voltage increasing conversion with high power density, high efficiency, and cheap topology in simple structure.

Double-output DC/DC Luo-converters consist of two conversion paths. Usually, mirror-symmetrical double-output voltages are required in industrial applications and computer periphery circuits such as operational amplifiers, computer periphery power supplies, differential servo-motor drives, and some symmetrical voltage medical equipment. In recent years, the DC/DC conversion technique has been greatly developed. The main objective is to reach a high efficiency, high power density, and cheap topology in simple structure.

The elementary circuit can perform step-down and step-up DC/DC conversion. The other double-output Luo-converters are derived from this elementary circuit: they are the self-lift circuit, re-lift circuit, and multiple-lift circuits (e.g., triple-lift and quadruple-lift circuits). Switch S in these circuits is a PMOS. It is driven by a PWM switching signal with repeating frequency f and conduction duty k In this book, the switch repeating period is $R = V_{o+}/I_{o+}$ and $R_1 = V_{o-}/I_{o-}$; so that the switch-on period is kT and the switch-off period is (l – k)T. For all circuits, the loads are usually resistive, that is, $z_{N+} = R/fL$ (where $L = L_1$ and $L = \dfrac{L_1 L_2}{L_1 + L_2}$ the normalized loads are $z_{N-} = R_1/fL_{11}$. for elementary circuit) and $L = L_{11}$ and $z_{N+} = z_{N-}$.

In order to keep the P/O and N/O voltages to be symmetrically equal to each other, usually, we purposely select that v_{C_1}.

Each converter has two conversion paths. The positive path consists of a positive pump circuit S–L_1–D_0–C_1 and a "**Π**"-type filter (C_2)–L_2–C_o and a lift circuit (except elementary circuit). The pump inductor L_1 absorbs energy from source during switch-on and transfers the stored energy to capacitor C_1 during switch-off. The energy on capacitor C_1 is then delivered to load R during switch-on. Therefore, a high voltage $V_{C_{11}}$ will correspondingly cause a high output voltage V_{o+}.

The negative path consists of a negative pump circuit S–L_{11}–D_{10}–(C_{11}) and a "Π"-type filter C_{11}–L_{12}–C_{10} and a lift circuit (except elementary circuit). The pump inductor L_{11}

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absorbs the energy from source during switch-on and transfers the stored energy to capacitor C_{11} during switch-off. The energy on capacitor C_{11} is then delivered to load R_1 during switch-on. Hence, a high voltage i_{D_0} will correspondingly cause a high output voltage V_{o-}.

When switch S is turned off, the currents flowing though the freewheeling diodes D_0 and D_{10} are existing. If the currents $i_{D_{10}}$ and i_{D_0} do not fall to zero before switch S is turned on again, we define this working state to be CCM. If the currents $i_{D_{10}}$ and V_{o+}, V_{o-}, and I_{o+} and I_{o-}; become zero before switch S is turned on again, we define that working state to be DCM.

The output voltages and currents are V_i and $I_i = I_{i+} + I_{i-}$ the input voltage and current are $P_i = P_o$. Assuming that the power loss can be ignored, $V_i I_i = V_{o+} I_{o+} + V_{o-} I_{o-}$., or i_{D_0} For general description, we have the following definitions in continuous mode:

The voltage transfer gain in the continuous mode is

$$M_+ = \frac{V_{o+}}{V_i} \quad \text{and} \quad M_- = \frac{V_{o-}}{V_i}$$

The variation ratio of the diode's currents is

$$\zeta_+ = \frac{\Delta i_{D_0}/2}{I_{D_0}} \quad \text{and} \quad \zeta_- = \frac{\Delta i_{D_{10}}/2}{I_{L_{11}}}$$

The variation ratio of the pump inductor's currents is

$$\xi_{1+} = \frac{\Delta i_{L_1}/2}{I_{L_1}} \quad \text{and} \quad \zeta_- = \frac{\Delta i_{L_{11}}/2}{I_{L_{11}}}$$

The variation ratio of the filter inductor's currents is

$$\xi_{2+} = \frac{\Delta i_{L_2}/2}{I_{L_2}} \quad \text{and} \quad \xi_- = \frac{\Delta i_{L_{12}}/2}{I_{L_{12}}}$$

The variation ratio of the lift inductor's currents is

$$\chi_{j+} = \frac{\Delta i_{L_2+j}/2}{I_{L_2+j}} \quad \text{and} \quad \chi_{j-} = \frac{\Delta i_{L_{12}+j}/2}{I_{L_{12}+j}} \quad j = 1,2,3,\ldots$$

The variation ratio of the pump capacitor's voltages is

$$\rho_+ = \frac{\Delta v_{C_1}/2}{V_{C_1}} \quad \text{and} \quad \rho_- = \frac{\Delta v_{C_{11}}/2}{V_{C_{11}}}$$

The variation ratio of lift capacitor's voltages

$$\sigma_{j+} = \frac{\Delta v_{C_1+j}/2}{V_{C_1+j}} \quad \text{and} \quad \sigma_{j-} = \frac{\Delta v_{C_{11}+j}/2}{V_{C_{11}+j}} \quad j = 1,2,3,4$$

The variation ratio of output voltages is

$$\varepsilon_+ = \frac{\Delta v_{o+}/2}{V_{o+}} \quad \text{and} \quad \varepsilon_- = \frac{\Delta v_{o-}/2}{V_{o-}}$$

2.6.1 Elementary Circuit

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The elementary circuit is shown in Figure 2.58. Since the positive Luo-converters and negative Luo-converters have been published, this section can be simplified.

2.6.1.1 Positive Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.59a and the equivalent circuit during switch-off in Figure 2.59b. The relations of the average currents and voltages are

$$I_{L_2} = \frac{1-k}{k} I_{L_1} \quad \text{and} \quad I_{L_2} = I_{o+}$$

The positive path input current is

$$I_{i+} = k \times i_{i+} = k(i_{L_1} + i_{L_2}) = k\left(1 + \frac{1-k}{k}\right) I_{L_1} = I_{L_1} \tag{2.313}$$

The output current and voltage are

$$I_{o+} = \frac{1-k}{k} I_{i+} \quad \text{and} \quad V_{o+} = \frac{k}{1-k} V_i$$

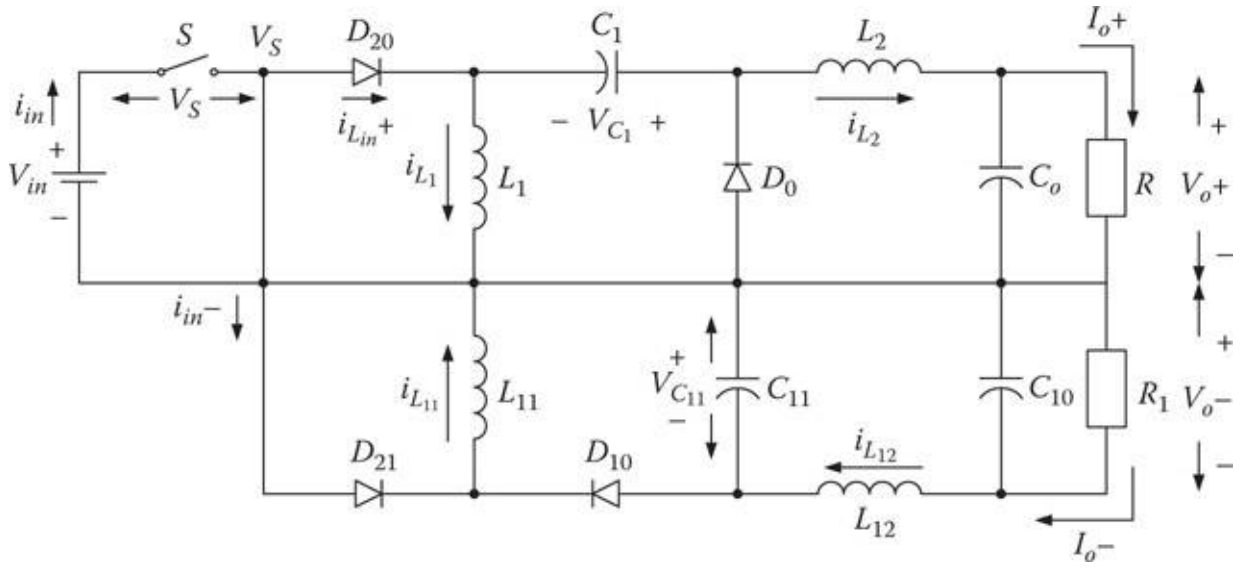


FIGURE 2.58
Elementary circuit.

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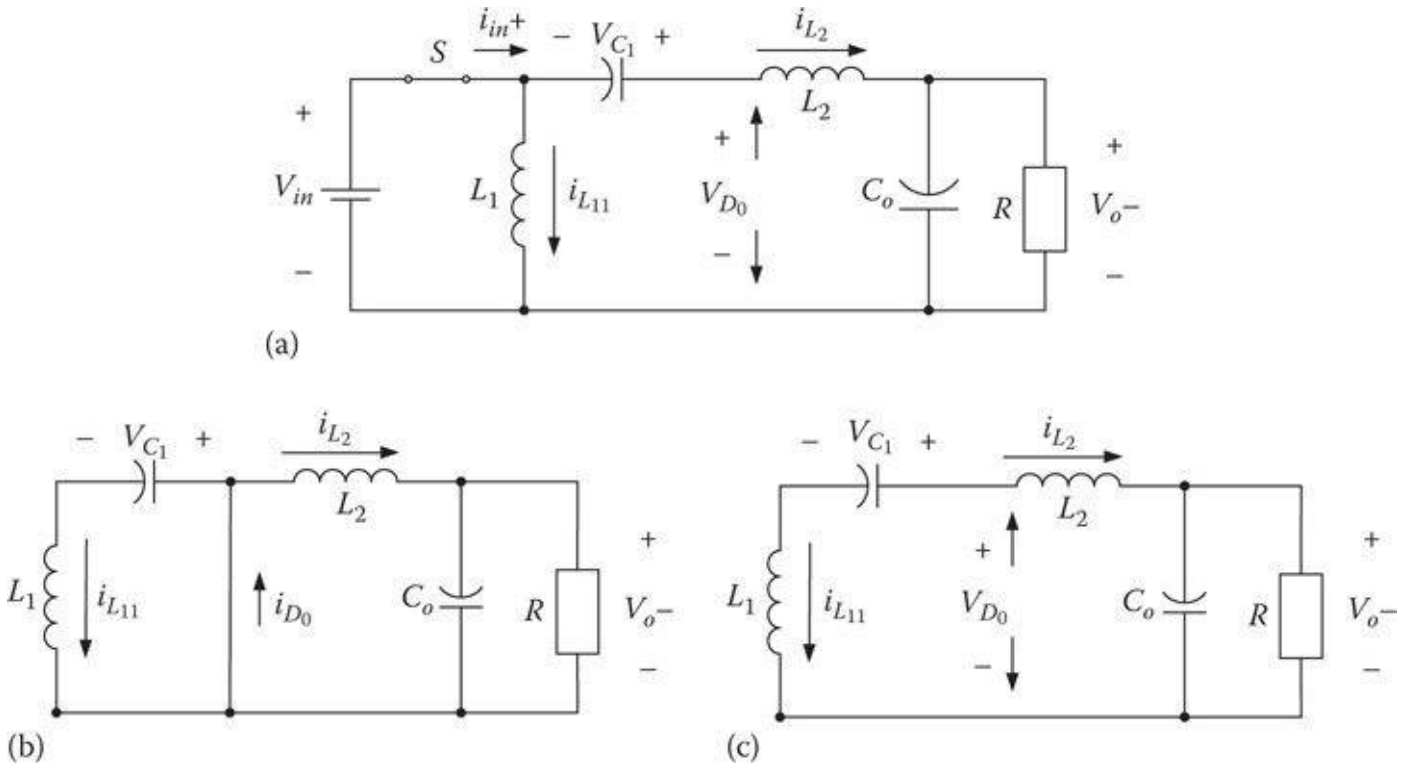


FIGURE 2.59
Equivalent circuits of elementary circuit positive path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

The voltage transfer gain in continuous mode is

$$M_{E_+} = \frac{V_{o_+}}{V_i} = \frac{k}{1-k} \tag{2.314}$$

The average voltage across capacitor C_1 is

$$V_{C_1} = \frac{k}{1-k} V_i = V_{o_+}$$

The variation ratios of the parameters are

$$\xi_{1_+} = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_i}{2L_1 I_{i+}} = \frac{1-k}{2M_E}\frac{R}{fL_1}$$

$$\xi_{2_+} = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{kTV_i}{2L_2 I_{o_+}} = \frac{k}{2M_E}\frac{R}{fL_2}$$

The variation ratio of current i_{D0} is

$$\zeta_+ = \frac{\Delta i_{D_0}/2}{I_{D_0}} = \frac{(1-k)^2 TV_{o_+}}{2LI_{o_+}} = \frac{k(1-k)R}{2M_E fL} = \frac{k^2}{M_E^2}\frac{R}{2fL} \tag{2.315}$$

The variation ratio of v_{C_1} is

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$$\rho_+ = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{(1-k)TI_{i_+}}{2C_1V_{o_+}} = \frac{k}{2}\frac{1}{fC_1R}$$

The variation ratio of output voltage v_{o+} is

$$\varepsilon_+ = \frac{\Delta v_{o_+}/2}{V_{o_+}} = \frac{kT^2}{16C_oL_2}\frac{V_i}{V_{o_+}} = \frac{k}{16M_E}\frac{1}{f^2C_oL_2} \tag{2.316}$$

If $L_1 = L_2 = 1$ mH, $C_1 = C_o = 20$ μF, $R = 10$ Ω, $f = 50$ kHz, and $k = 0.5$, we obtain that $\xi_{1_+} = 0.05, \xi_{2_+} = 0.05, \zeta_+ = 0.05, \rho_+ = 0.025$, and $\varepsilon = 0.00125$. Therefore, the variations of i_{L_1}, i_{L2}, and v_{C_1} are small. The output voltage V_{o+} is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_{o+}(t)$ is almost a real DC waveform with very small ripple as well and is equal to $I_{o+} = V_{o+}/R$.

2.6.1.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.60a, and the equivalent circuit during switch-off is shown in Figure 2.60b. The relations of the average currents and voltages are

$$I_{o_} = I_{L12} \quad \text{and} \quad I_{o_} = I_{L12} = I_{C11-on}$$

Since

$$I_{C11-off} = \frac{k}{1-k}I_{C11-on} = \frac{k}{1-k}I_{o_}$$

the inductor current I_{L11} is

$$I_{L11} = I_{C11-off} + I_{o_} = \frac{I_{o_}}{1-k} \tag{2.317}$$

so that

$$I_{i_} = k \times i_{i_} = ki_{L11} = kI_{L11} = \frac{k}{1-k}I_{o_}$$

The output current and voltage are

$$I_{o_} = \frac{1-k}{k}I_{i_} \quad \text{and} \quad V_{o_} = \frac{k}{1-k}V_i$$

The voltage transfer gain in continuous mode is

$$M_{E_} = \frac{V_{o_}}{V_i} = \frac{k}{1-k} \tag{2.318}$$

and

$$V_{C11} = V_{o_} = \frac{k}{1-k}V_i$$

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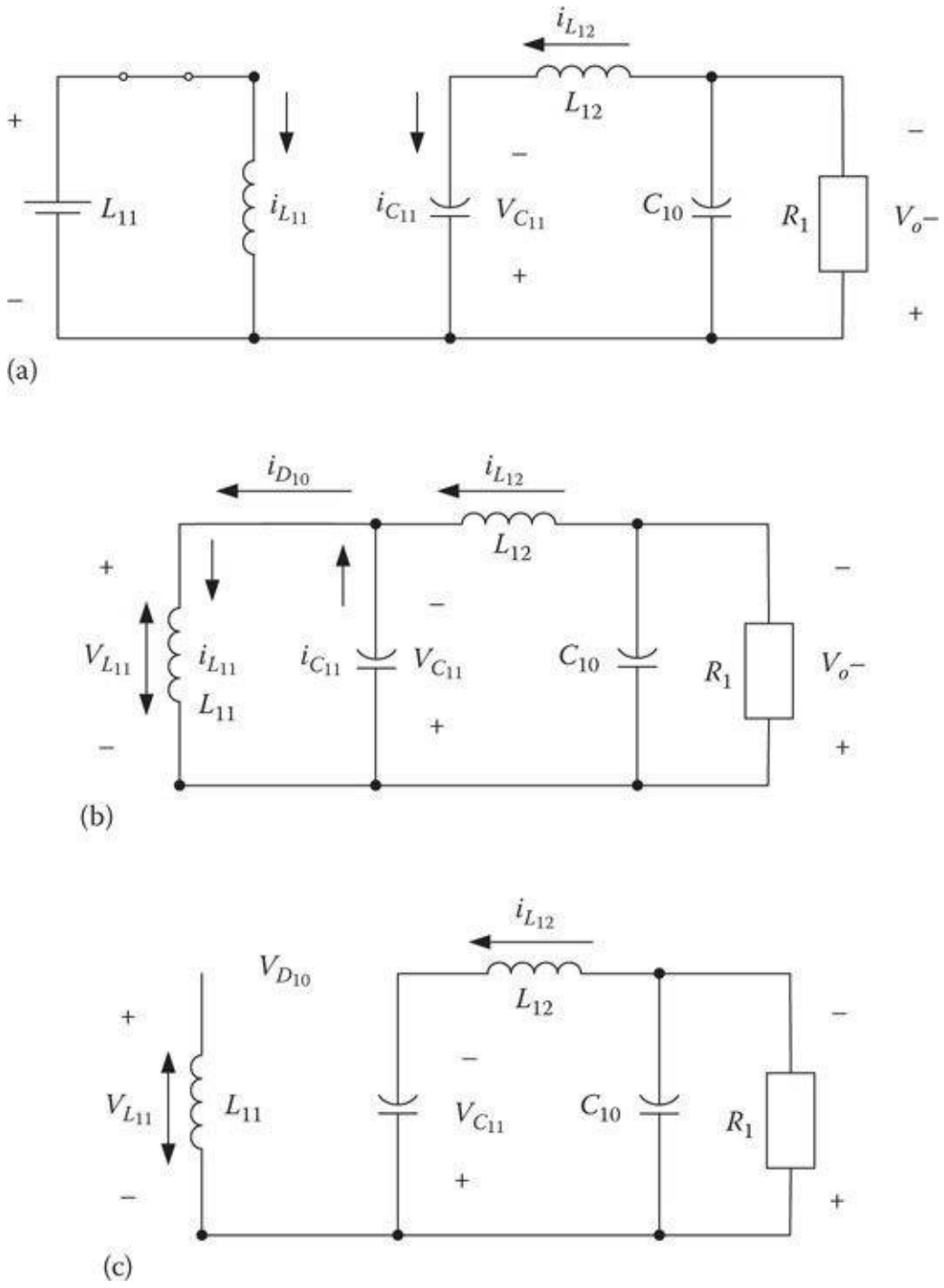


FIGURE 2.60
Equivalent circuits of elementary circuit negative path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

From Equations 2.314 and 2.318, we can define that $M_E = M_{E+} = M_{E-}$. The curve of M_E versus k is shown in Figure 2.61.

The variation ratios of the parameters are

$$\xi_- = \frac{\Delta i_{L12}/2}{I_{L12}} = \frac{k}{16}\frac{1}{f^2 C_{10} L_{12}} \quad \text{and} \quad \rho_- = \frac{\Delta v_{C11}/2}{V_{C11}} = \frac{kI_{o-}T}{2C_{11}V_{o-}} = \frac{k}{2}\frac{1}{fC_{11}R_1}$$

The variation ratio of currents i_{L11} and i_{D10} is

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$$\zeta_{-} = \frac{\Delta i_{L_{11}}/2}{I_{L_{11}}} = \frac{k(1-k)V_i T}{2L_{11}I_{o-}} = \frac{k(1-k)R_1}{2M_E f L_{11}} = \frac{k^2}{M_E{}^2}\frac{R_1}{2fL_{11}} \tag{2.319}$$

The variation ratio of current $v_{C_{10}}$ is

$$\varepsilon_{-} = \frac{\Delta v_{C_{10}}/2}{V_{C_{10}}} = \frac{k}{128 f^3 C_{11} C_{10} L_{12}}\frac{I_{o-}}{V_{o-}} = \frac{k}{128}\frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \tag{2.320}$$

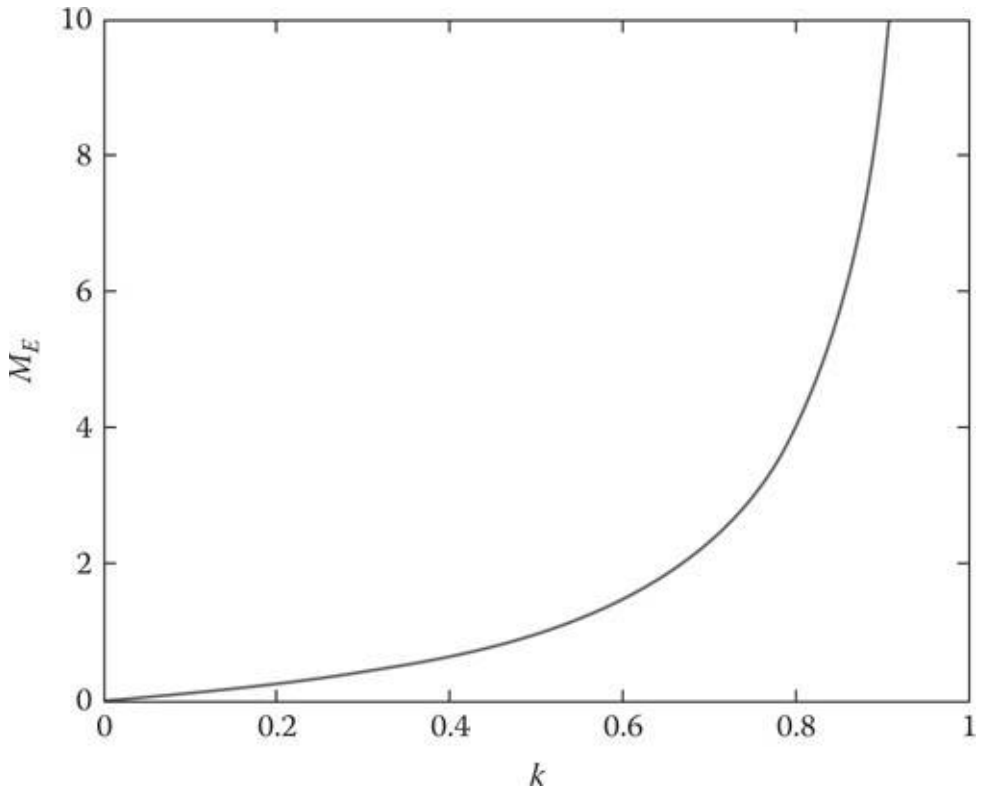


FIGURE 2.61
Voltage transfer gain M_E versus k.

Assuming that $f = 50$ kHz, $L_{11} = L_{12} = 0.5$ mH, $C = C_o = 20$ μF, $R_1 = 10$ Ω, and $k = 0.5$, , we obtained $M_E = 1$, $\zeta_{-} = 0.05$, $\rho_{-} = 0.025$, $\xi_{-} = 0.00125$, and $\varepsilon = 0.0000156$. The output voltage $V_{o_}$ is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{o_}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{o-} = V_{o-}/R_1$.

2.6.1.3 Discontinuous Mode

The equivalent circuits of the discontinuous mode's operation are shown in Figures 2.59c and 2.60c. In order to obtain the mirror-symmetrical double-output voltages, select

$$L = \frac{L_1 L_2}{L_1 + L_2} = L_{11}$$

and

$$R = R_1$$

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Thus, we define

$$V_o = V_{o+} = |V_{o-}| \quad M_E = M_{E+} = M_{E-} = \frac{V_o}{V_i} = \frac{k}{1-k}$$

$$z_N = z_{N+} = z_{N-} \quad \text{and} \quad z = z_+ = z_-$$

The freewheeling diode currents i_{D_0} and $i_{D_{10}}$ become zero during switch-off before the next period switch-on. The boundary between continuous and discontinuous modes is

$$\zeta \geq 1$$

that is,

$$\frac{k^2}{M_E^2}\frac{z_N}{2} \geq 1$$

or

$$M_E \leq k\sqrt{\frac{z_N}{2}} \tag{2.321}$$

The boundary curve is shown in Figure 2.62.

In this case, the freewheeling diode's current exists in the period between kT and $[k + (1 - k)m_E]T$, where m_E is the *filling efficiency*, and it is defined as

$$m_E = \frac{1}{\zeta} = \frac{2M_E^2}{k^2 z_N} \tag{2.322}$$

Considering Equation 2.321, therefore $0 < m_E < 1$. Since the diode current i_{D_0} becomes zero at $t = kT + (1 - k)m_E T$ for the current i_{L_1},

$$kTV_i = (1 - k)m_E TV_C$$

or

$$V_{C_1} = \frac{k}{(1-k)m_E}V_i = k(1-k)\frac{z_N}{2}V_i \quad \text{with} \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \tag{2.323}$$

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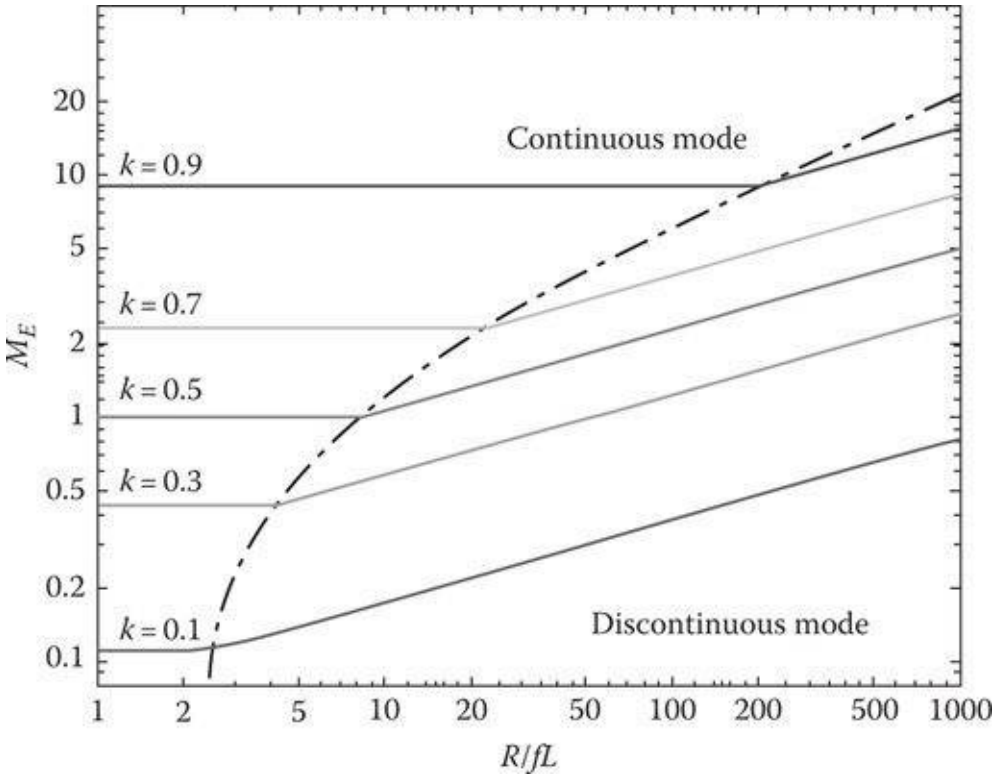


FIGURE 2.62
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$ (elementary circuit).

and for the current i_{L_2}

$$kT\left(V_i + V_{C_1} - V_{o_+}\right) = \left(1-k\right) m_E T V_{o_+}$$

Therefore, the P/O voltage in discontinuous mode is

$$V_{o_+} = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{z_N}{2} V_i \quad \text{with} \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \tag{2.324}$$

For the current $i_{L_{11}}$, we have

$$kTV_i = \left(1-k\right) m_E T V_{C_{11}}$$

or

$$V_{C_{11}} = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{z_N}{2} V_i \quad \text{with} \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \tag{2.325}$$

and for the current $i_{L_{12}}$, we have

$$kT\left(V_i + V_{C_{11}} - V_{o_-}\right) = \left(1-k\right) m_E T V_{o_-}$$

Therefore, the N/O voltage in discontinuous mode is

$$V_{o_-} = \frac{k}{(1-k)m_E} V_i = k(1-k)\frac{z_N}{2} V_i \quad \text{with} \sqrt{\frac{z_N}{2}} \geq \frac{1}{1-k} \tag{2.326}$$

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Then we have

$$V_o = V_{o+} = V_{o-} = k(1-k)\frac{z_N}{2}V_i$$

that is, the output voltage will linearly increase while load resistance increases. It can be seen that larger load resistance may cause higher output voltage in discontinuous mode as shown in Figure 2.62.

2.6.2 Self-Lift Circuit

The self-lift circuit shown in Figure 2.63 is derived from the elementary circuit. The positive conversion path consists of a pump circuit S–L_1–D_0–C_1 and a filter (C_2)–L_2–C_o and a lift circuit D_1–C_2. The negative conversion path consists of a pump circuit S–L_{11}–D_{10}–(C_{11}) and a "Π"-type filter C_{11}–L_{12}–C_{10} and a lift circuit D_{11}–C_{12}.

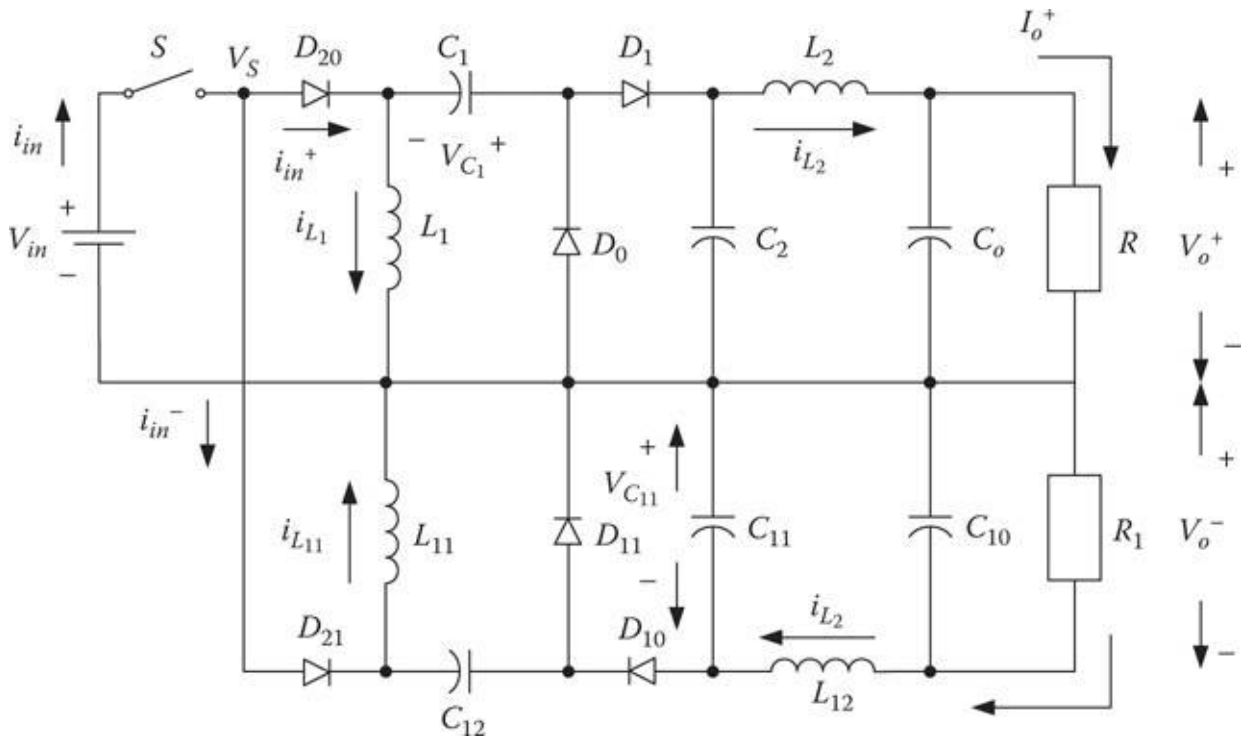


FIGURE 2.63
Self-lift circuit.

2.6.2.1 Positive Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.64a and the equivalent circuit during switch-off in Figure 2.64b. The voltage across inductor L_1 is equal to V_i during switch-on and $-V_{C_1}$ during switch-off. We have the following relations:

$$V_{C_1} = \frac{k}{1-k}V_i$$

Hence,

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$$V_o = V_{C_o} = V_{C_2} = V_i + V_{C_1} = \frac{1}{1-k} V_i$$

and

$$V_{o_+} = \frac{1}{1-k} V_i$$

The output current is

$$I_{o_+} = (1-k) I_{i_+}$$

Other relations are

$$I_{i_+} = k i_{i_+} \; i_{i_+} = I_{L_1} + i_{C_1-on} \quad i_{C_1-off} = \frac{k}{1-k} i_{C_1-on}$$

and

$$I_{L_1} = i_{C_1-off} = k i_{i_+} = I_{i_+} \tag{2.327}$$

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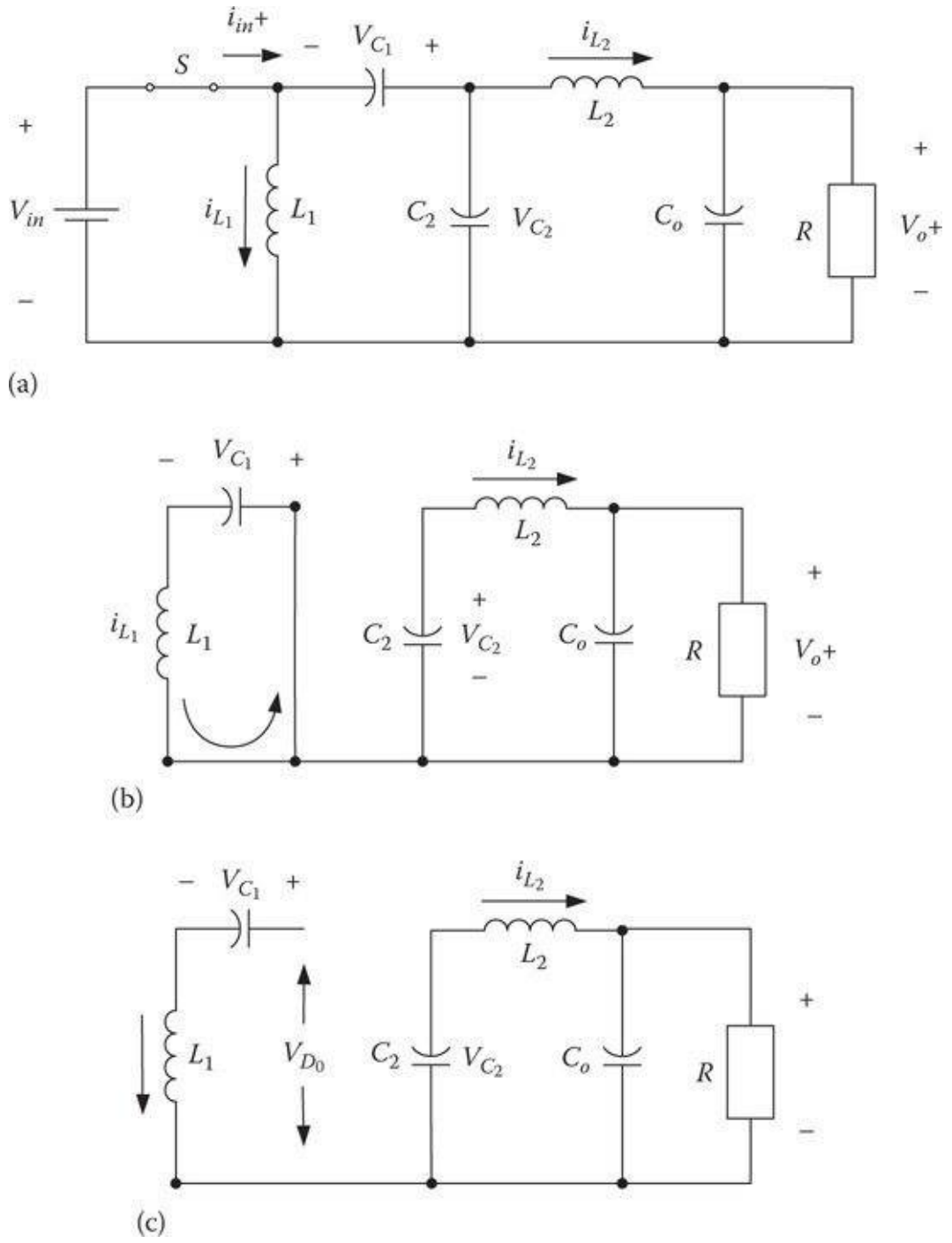


FIGURE 2.64
Equivalent circuits of self-lift circuit positive path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

Therefore, the voltage transfer gain in continuous mode is

$$M_{S_+} = \frac{V_{o_+}}{V_I} = \frac{1}{1-k} \tag{2.328}$$

The variation ratios of the parameters are

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$$\xi_{2+} = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k}{16}\frac{1}{f^2 C_2 L_2}$$

$$\rho_+ = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{(1-k)I_{i+}}{2fC_1\dfrac{k}{1-k}V_i} = \frac{1}{2kfC_1R}$$

and

$$\sigma_{1+} = \frac{\Delta v_{C_2}/2}{V_{C_2}} = \frac{k}{2fC_2R}$$

The variation ratio of the currents i_{D_0} and i_{L_1} is

$$\zeta_+ = \xi_{1+} = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kV_iT}{2L_1I_{i+}} = \frac{k}{M_S^2}\frac{R}{2fL_1} \tag{2.329}$$

The variation ratio of output voltage v_{o+} is

$$\varepsilon_+ = \frac{\Delta v_{o+}/2}{V_{o+}} = \frac{k}{128}\frac{1}{f^3 C_2 C_o L_2 R} \tag{2.330}$$

If $L_1 = L_2 = 0.5$ mH, $C_1 = C_2 = C_o = 20$ μF, $R = 40$ Ω, $f = 50$ kHz, and $k = 0.5$, we obtain that $\xi_{1+} = \zeta_+ = 0.1$ and $\rho_+ = 0.00625$ and $\sigma_{1+} = 0.00625$, $\xi_{2+} = 0.00125$, and $\varepsilon_+ = 0.000004$. Therefore, the variations of i_{L_1}, v_{C_1}, i_{L_2}, and v_{C_2} are small. The output voltage V_{o+} is almost a real DC voltage with very small ripple. Because of the resistive load, the output current $i_{o+}(t)$ is almost a real DC waveform with very small ripple as well, and $I_{o+} = V_{o+}/R$.

2.6.2.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.65a and the equivalent circuit during switch-off in Figure 2.65b. The relations of the average currents and voltages are

$$I_{o-} = I_{L12} = I_{C11-on} \quad I_{C11-off} = \frac{k}{1-k}I_{C11-on} = \frac{k}{1-k}I_{o-}$$

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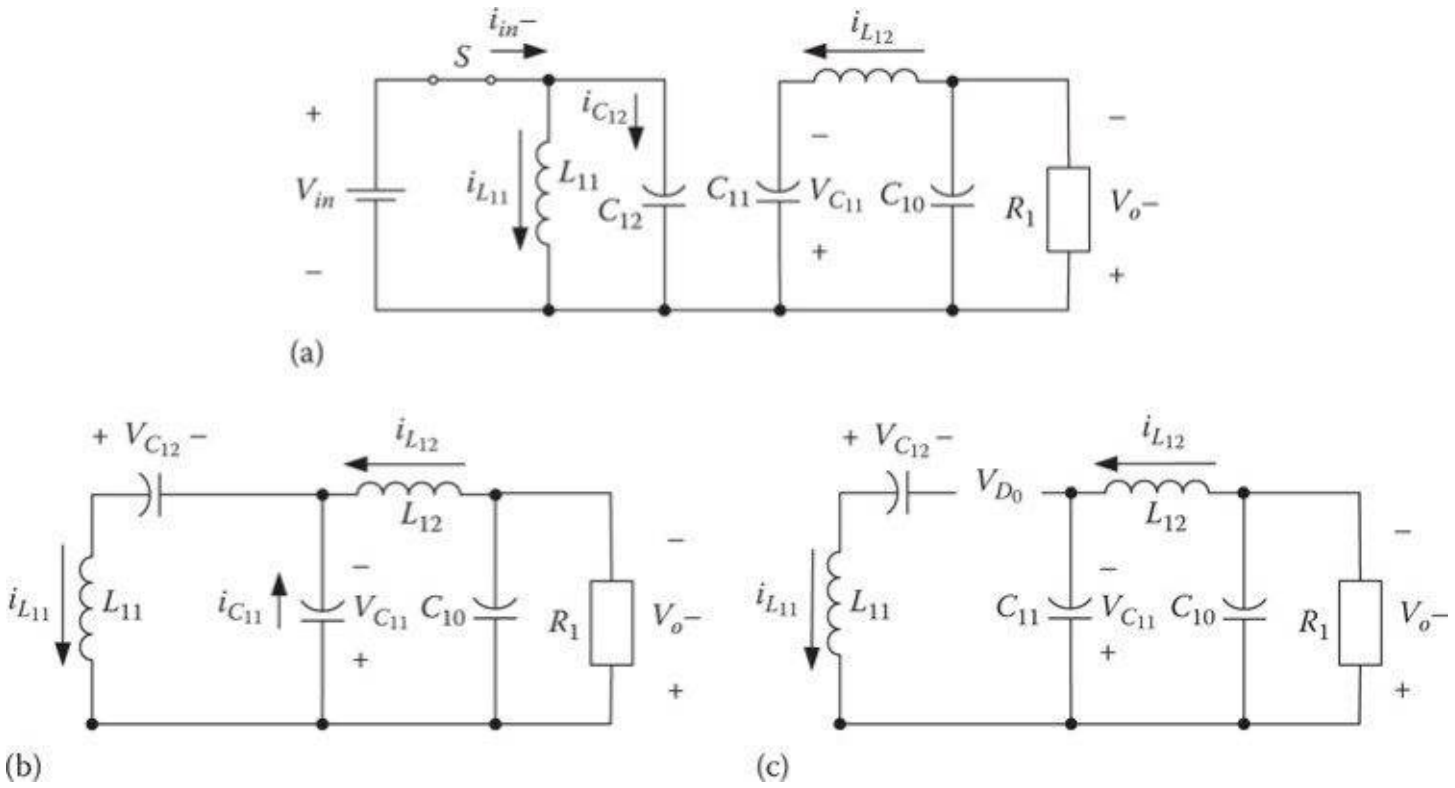


FIGURE 2.65
Equivalent circuits of self-lift circuit negative path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

and

$$I_{L11} = I_{C11-off} + I_{o-} = \frac{I_{o-}}{1-k} \tag{2.331}$$

We know that

$$I_{C12-off} = I_{L11} = \frac{1}{1-k} I_{o-}$$

and

$$I_{C12-on} = \frac{1-k}{k} I_{C12-off} = \frac{1}{k} I_{o-}$$

so that

$$V_{o-} = \frac{1}{1-k} V_i$$

and

$$I_{o-} = (1-k) I_i$$

The voltage transfer gain in continuous mode is

$$M_{S-} = \frac{V_{o-}}{V_i} = \frac{1}{1-k} \tag{2.332}$$

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Circuit C_{11}–L_{12}–C_{10} is a "Π"-type low-pass filter. Therefore,

$$V_{C_{11}} = V_{o_} = \frac{k}{1-k} V_i$$

From Equations 2.328 and 2.332, we define $M_S = M_{S_+} = M_{S_}$. The curve of M_S versus k is shown in Figure 2.66.

The variation ratios of the parameters are

$$\xi_- = \frac{\Delta i_{L_{12}}/2}{I_{L_{12}}} = \frac{k}{16} \frac{1}{f^2 C_{10} L_{12}}$$

$$\rho_- = \frac{\Delta v_{C_{11}}/2}{V_{C_{11}}} = \frac{k I_{o_} T}{2 C_{11} V_{o_}} = \frac{k}{2} \frac{1}{f C_{11} R_1}$$

$$\sigma_{1_} = \frac{\Delta v_{C_{12}}/2}{V_{C_{12}}} = \frac{I_{o_}}{2 f C_{12} V_i} = \frac{M_S}{2} \frac{1}{f C_{12} R_1}$$

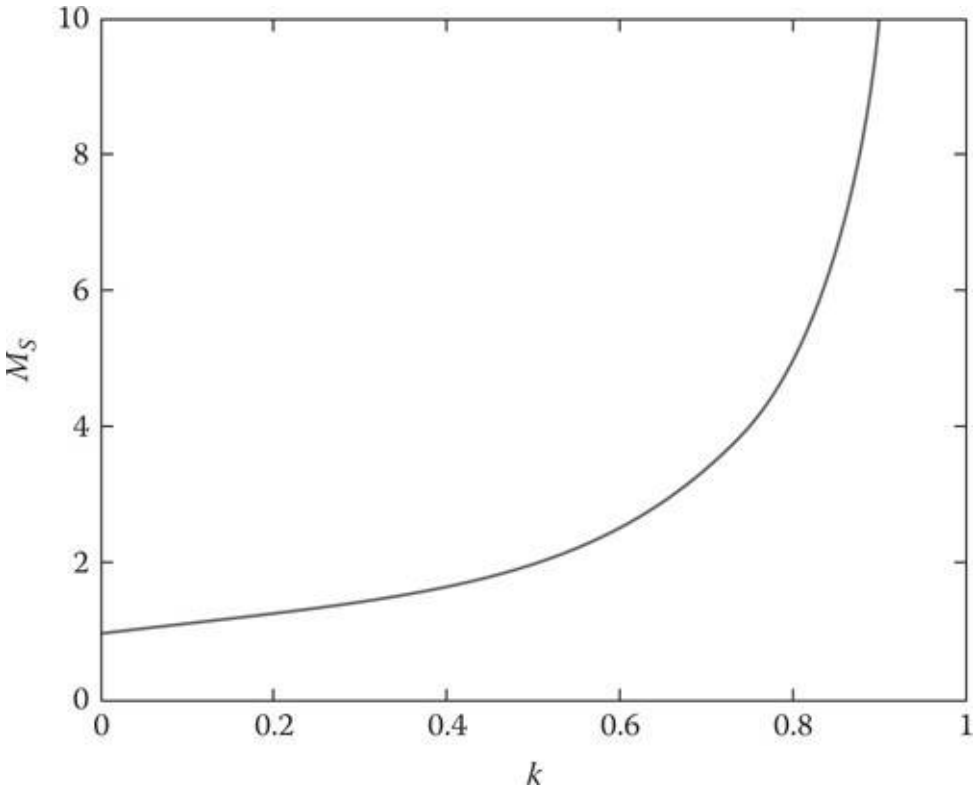


FIGURE 2.66
Voltage transfer gain M_S versus k.

The variation ratio of currents $i_{D_{10}}$ and $i_{L_{11}}$ is

$$\zeta_- = \frac{\Delta i_{L_{11}}/2}{I_{L_{11}}} = \frac{k(1-k) V_i T}{2 L_{11} I_{o_}} = \frac{k(1-k) R_1}{2 M_S f L_{11}} = \frac{k}{M_S^2} \frac{R_1}{2 f L_{11}} \tag{2.333}$$

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The variation ratio of current $v_{C_{10}}$ is

$$\varepsilon_{-} = \frac{\Delta v_{C_{10}}/2}{V_{C_{10}}} = \frac{k}{128 f^3 C_{11} C_{10} L_{12}} \frac{I_{o-}}{V_{o-}} = \frac{k}{128} \frac{1}{f^3 C_{11} C_{10} L_{12} R_1} \tag{2.334}$$

Assuming that $f = 50$ kHz, $L_{11} = L_{12} = 0.5$ μH, $C_{11} = C_{10} = 20$ μF, $R_1 = 40$ Ω, and $k = 0.5$, we obtain $M_S = 2$, $\zeta_{-} = 0.2$, $\rho_{-} = 0.006$, $\sigma_{1-} = 0.025$, $\xi_{-} = 0.0006$, and $\varepsilon_{-} = 0.000004$. The output voltage V_{o-} is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{o-}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{o-} = V_{o-}/R_1$.

2.6.2.3 Discontinuous Conduction Mode

The equivalent circuits of the DCM's operation are shown in Figures 2.64c and 2.65c. Since we select $z_N = z_{N+} = z_{N-}$, $M_S = M_{S+} = M_{S-}$, and $\zeta = \zeta_{+} = \zeta_{-}$ The boundary between continuous mode and DCM is

$$\zeta \geq 1$$

or

$$\frac{k}{M_S^2} \frac{z_N}{2} \geq 1$$

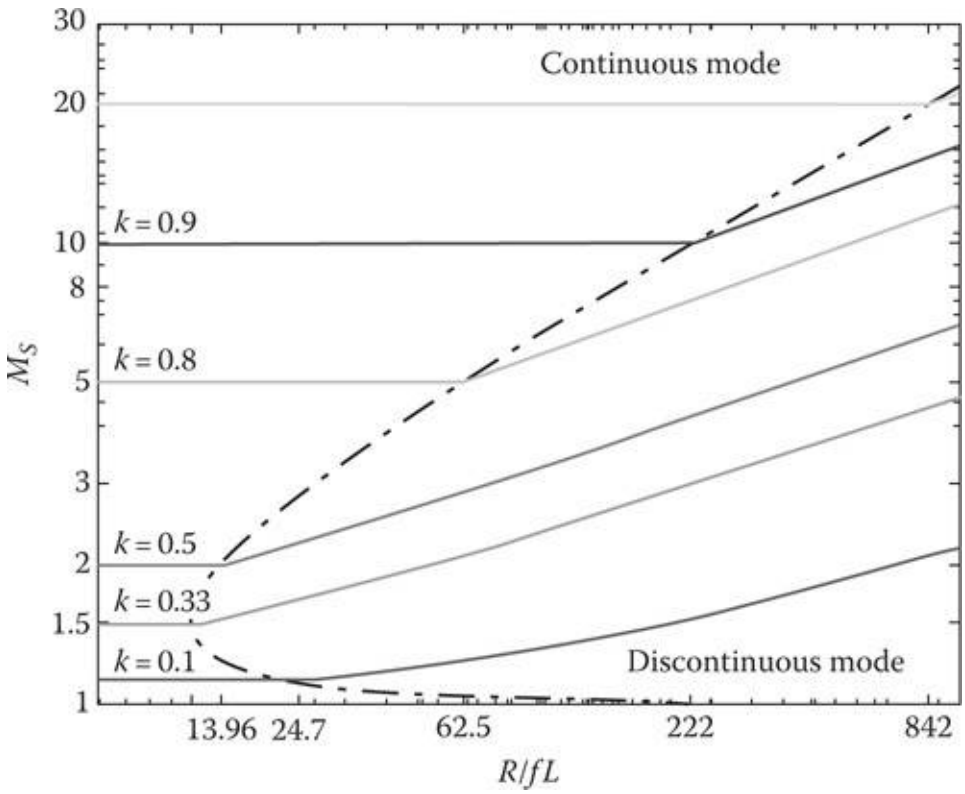


FIGURE 2.67
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$ (self-lift circuit).

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Hence,

$$M_S \le \sqrt{k}\sqrt{\frac{z}{2}} = \sqrt{\frac{kz_N}{2}} \tag{2.335}$$

This boundary curve is shown in Figure 2.67. Compared with Equations 2.321 and 2.335, this boundary curve has a minimum value of M_S that is equal to 1.5 at $k = 1/3$.

The filling efficiency is defined as

$$m_S = \frac{1}{\zeta} = \frac{2M_S^2}{kz_N} \tag{2.336}$$

For the current i_{L_1}, we have

$$kTV_i = (1-k)m_{S_+}TV_{C_1}$$

or

$$V_{C_1} = \frac{k}{(1-k)m_S}V_i = k^2(1-k)\frac{z_N}{2}V_i \quad \text{with} \sqrt{\frac{kz_N}{2}} \ge \frac{1}{1-k} \tag{2.337}$$

Therefore, the P/O voltage in DCM is

$$V_{o_+} = V_{C_1} + V_i = \left[1+\frac{k}{(1-k)m_S}\right]V_i = \left[1+k^2(1-k)\frac{z_N}{2}\right]V_i \quad \text{with} \sqrt{\frac{kz_N}{2}} \ge \frac{1}{1-k} \tag{2.338}$$

For the current $i_{L_{11}}$, we have

$$kTV_i = (1-k)m_S T(V_{C_{11}} - V_i)$$

or

$$V_{C_{11}} = \left[1+\frac{k}{(1-k)m_S}\right]V_i = \left[1+k^2(1-k)\frac{z_N}{2}\right]V_i \quad \text{with} \sqrt{\frac{kz_N}{2}} \ge \frac{1}{1-k} \tag{2.339}$$

and for the current $i_{L_{12}}$, we have

$$kT(V_i + V_{C_{11}} - V_{o_-}) = (1-k)m_{S_-}T(V_{o_-} - V_i)$$

Therefore, the N/O voltage in DCM is

$$V_{o_-} = \left[1+\frac{k}{(1-k)m_S}\right]V_i = \left[1+k^2(1-k)\frac{z_N}{2}\right]V_i \quad \text{with} \sqrt{\frac{kz_N}{2}} \ge \frac{1}{1-k} \tag{2.340}$$

We then have

$$V_o = V_{o_+} = V_{o_-} = \left[1+k^2(1-k)\frac{z_N}{2}\right]V_i$$

that is, the output voltage will linearly increase when load resistance increases. Larger load resistance causes higher output voltage in DCM as shown in Figure 2.67.

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2.6.3 Re-Lift Circuit

The re-lift circuit shown in Figure 2.68 is derived from self-lift circuit. The positive conversion path consists of a pump circuit S–L_1–D_0–C_1 and a filter (C_2)–L_2–C_o and a lift circuit D_1–C_2–D_3–L_3–D_2–C_3. The negative conversion path consists of a pump circuit S–L_{11}–D_{10}– (C_u) and a "Π"-type filter C_n–L_{12}–C_{10} and a lift circuit D_{11}–C_{12}–L_{13}–D_{22}–C_{13}–D_{12}.

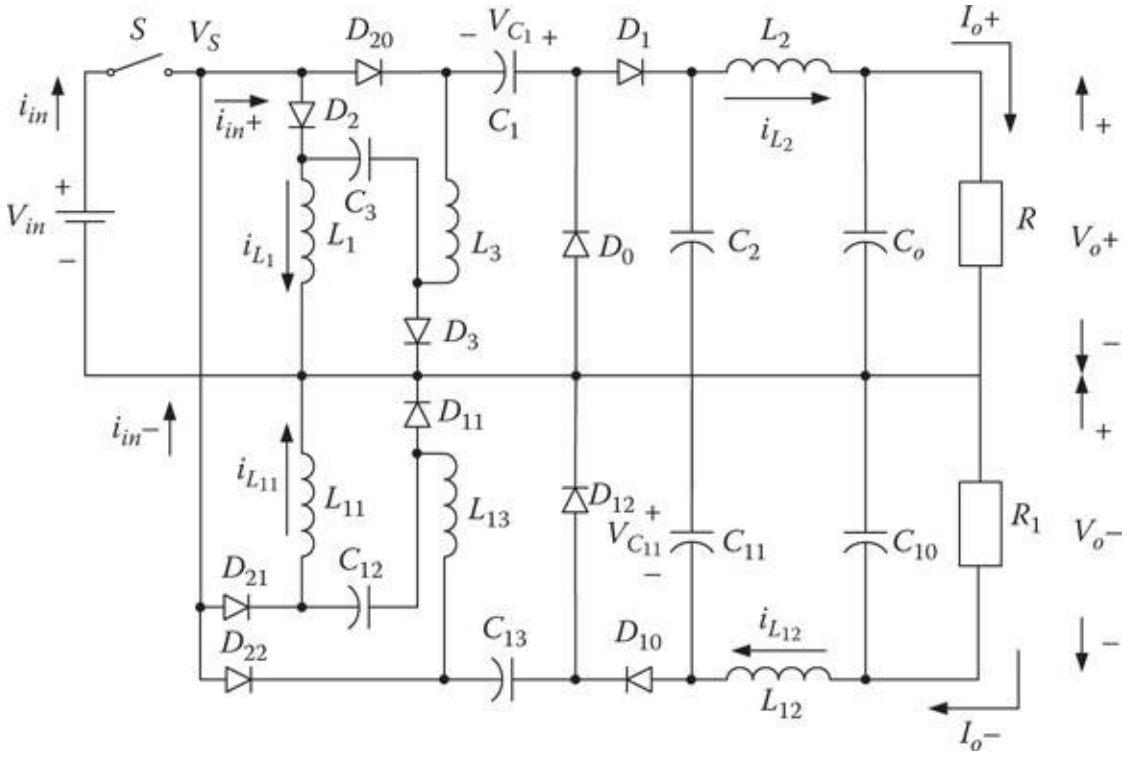


FIGURE 2.68
Re-lift circuit.

2.6.3.1 Positive Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.69a and the equivalent circuit during switch-off in Figure 2.69b. The voltage across inductors L_1 and L_3 is equal to V_i during switch-on and $-(V_{C1} - V_i)$ during switch-off. We have the following relations:

$$V_{C_1} = \frac{1+k}{1-k} V_i$$

and

$$V_o = V_{C_o} = V_{C_2} = V_i + V_{C_1} = \frac{2}{1-k} V_i$$

Thus,

$$V_{o+} = \frac{2}{1-k} V_i$$

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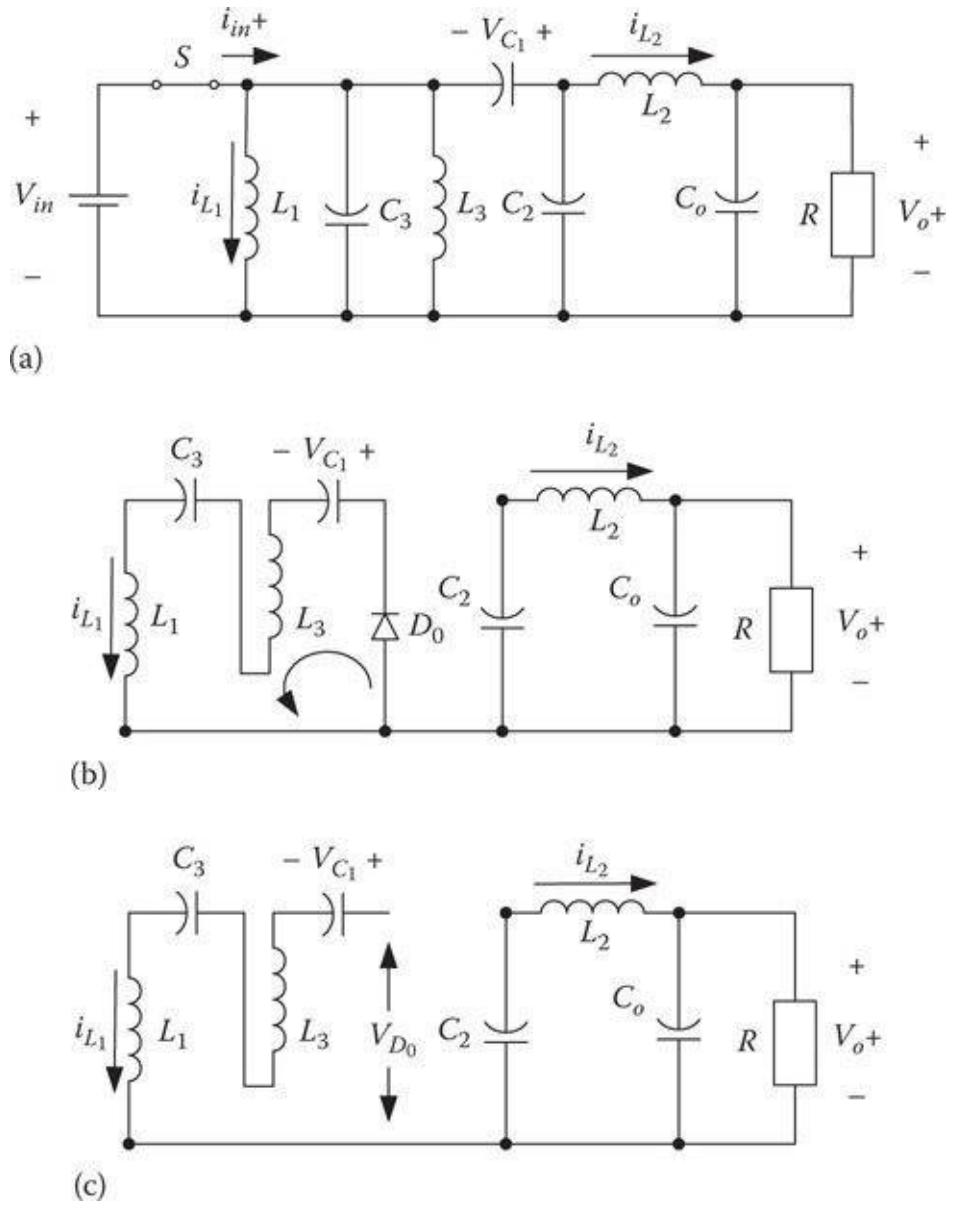


FIGURE 2.69
Equivalent circuits of re-lift circuit positive path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

and

The other relations are

and

The voltage transfer gain in continuous mode is

The variation ratios of the parameters are

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and

The variation ratio of currents i_{D_0} and i_{L_1} is

and the variation ratio of output voltage is

If we obtain that and Therefore, the variations of are small, and the ripples of and are small. The output voltage (and) is almost a real DC voltage with very small ripple. Because of the resistive load, the output current i_{0+} is almost a real DC waveform with very small ripple as well, and .

2.6.3.2 Negative Conversion Path

The equivalent circuit during switch-on is shown in Figure 2.70a and the equivalent circuit during switch-off in Figure 2.70b. The relations of the average currents and voltages are

FIGURE 2.70
Equivalent circuits of re-lift circuit negative path. (a) Switch-on. (b) Switch-off. (c) Discontinuous mode.

and

In steady state, we have

and

and

The voltage transfer gain in continuous mode is

Circuit C_{11}–L_{12}–C_{10} is a "Π"-type low-pass filter.
Therefore,

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From Equations 2.342 and 2.346 we define $M_R = M_R+ = M_{R-}$. The curve of M_R versus k is shown in Figure 2.71.

The variation ratios of the parameters are



FIGURE 2.71
Voltage transfer gain M_R versus k.

and

The variation ratio of the currents $i_{D_{10}}$ and is

The variation ratio of current is

Assuming that we obtain that The output voltage V_{o-} is almost a real DC voltage with very small ripple. Since the load is resistive, the output current $i_{o-}(t)$ is almost a real DC waveform with very small ripple as well, and it is equal to $I_{o-} = V_{o-} / R_1$.

2.6.3.3 Discontinuous Conduction Mode

The equivalent circuits of the DCM are shown in Figures 2.69c and 2.70c. In order to obtain the mirror-symmetrical double-output voltages, we purposely select $z_N = z_{N+} = z_{N-}$ and $\zeta = \zeta+ = \zeta_-$. The freewheeling diode currents and become zero during switch-off before the next period switch-on. The boundary between continuous mode and DCM is

or

Hence,

This boundary curve is shown in Figure 2.71. Comparing with Equations 2.321, 2.335, and 2.349, it can be seen that the boundary curve has a minimum value of M_R that is equal to 3.0, corresponding to $k = 1/3$.

The filling efficiency m_R is

So

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Therefore, the P/O voltage in DCM is

For the current i_{L11} because inductor current
so that

For the current we have



FIGURE 2.72
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$ (re-lift circuit).

or

and for the current

Therefore, the N/O voltage in DCM is

So

that is, the output voltage will linearly increase when load resistance increases. Larger load resistance may cause higher output voltage in discontinuous mode as shown in Figure 2.72.

2.6.4 Multiple-Lift Circuit

Referring to Figure 2.68, it is possible to build a multiple-lift circuit only using the parts L_3–D_{20}–C_3–D_3 multiple times in the positive conversion path and using the parts



FIGURE 2.73
Triple-lift circuit.

D_{22}–L_{13}–C_{13}–D_{12} multiple times in the negative conversion path. For example, in Figure 2.73, the parts L_4–D_4–C_4–D_5 and parts D_{23}–L_{14}–C_{14}–D_{13} were added in the triple-lift circuit.

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According to this principle, triple-lift circuit and quadruple-lift circuit have been built as shown in Figures 2.73 and 2.76. In this book, it is not necessary to introduce the particular analysis and calculations one by one to the readers. However, their calculation formulae are shown in this section.

2.6.4.1 Triple-Lift Circuit

The triple-lift circuit is shown in Figure 2.73. The positive conversion path consists of a pump circuit S–L_1–D_0–C_1 and a filter (C_2)–L_2–C_o and a lift circuit D_1–C_2–D_2–C_3–D_3–L_3–D_4–C_4–D_5–L_4. The negative conversion path consists of a pump circuit S–L_{11}–D_{10}–(C_{11}) and a "Π"-type filter C_{11}–L_{12}–C_{10} and a lift circuit D_{11}–C_{12}–D_{22}–C_{13}–L_{13}–D_{12}–D_{23}–L_{14}–C_{14}–D_{13}.

2.6.4.1.1 Positive Conversion Path

The lift circuit is D_1–C_2–D_2–C_3–D_3–L_3–D_4–C_4–D_5–L_4. Capacitors C_2, C_3, and C_4 perform characteristics to lift the capacitor voltage by three times of source voltage and L_4 perform the function as ladder joints to link the three capacitors C_3 and C_4 and lift the capacitor voltage up. Currents are exponential functions. They have large values at the moment of power on, but they are small because in steady state.

The output voltage and current are

and

The voltage transfer gain in continuous mode is

Other average voltages are

Other average currents are

The current variations are

The voltage variations are

The variation ratio of output voltage V_{C_0} is

2.6.4.1.2 Negative Conversion Path

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Circuit C_{12}–D_{11}–L_{13}–D_{22}–C_{13}–D_{12}–L_{14}–D_{23}–C_{14}–D_{13} is the lift circuit. Capacitors C_{12}, C_{13} and C_{14} perform characteristics to lift the capacitor voltage by three times the source voltage perform the function as ladder joints to link the three capacitors C_{12}, C_{13}, and C_{14} and lift the capacitor voltage up. Currents are exponential functions. They have large values at the moment of power on, but they are small because in steady state.

The output voltage and current are

and

The voltage transfer gain in continuous mode is

From Equations 2.355 and 2.357, we define The curve of M_T versus k is shown in Figure 2.74.

Other average voltages are

Other average currents are



FIGURE 2.74
Voltage transfer gain M_T versus k.

The current variation ratios are

The voltage variation ratios are

The variation ratio of output voltage is

2.6.4.1.3 Discontinuous Mode

To obtain the mirror-symmetrical double-output voltages, we purposely select

and

Define the following:

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The freewheeling diode currents and become zero during switch-off before the next period switch-on. The boundary between continuous mode and DCM is $\zeta \geq 1$.

Then

FIGURE 2.75
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$ (triple-lift circuit).

This boundary curve is shown in Figure 2.75. Comparing with Equations 2.321, 2.335, 2.349, and 2.359, it can be seen that the boundary curve has a minimum value of M_T that is equal to 4.5, corresponding to $k = 1/3$.

In DCM, the currents i_{D0} and i_{D10} exist in the period between kT and $[k + (1 - k)m_T]T$, where m_T is the filling efficiency, that is,

Considering Equation 2.359, therefore $0 < m_T < 1$. Since the current i_{D0} becomes zero at $t = t_1 = [k + (1 - k)m_T]T$ for the currents

or

Therefore, the P/O voltage in discontinuous mode is

Because inductor current , so that

Since i_{D0} becomes for the current

or

for the current

Therefore, the N/O voltage in discontinuous mode is

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So,

that is, the output voltage will linearly increase when load resistance increases. The output voltage will increase when load resistance increases, as shown in Figure 2.75.

2.6.4.2 Quadruple-Lift Circuit

Quadruple-lift circuit is shown in Figure 2.76. The positive conversion path consists of a pump circuit and a filter and a lift circuit The negative conversion path consists of a pump circuit and a "Π"-type filter and a lift circuit

2.6.4.2.1 Positive Conversion Path

Capacitors perform characteristics to lift the capacitor voltage by four times the source voltage perform the function as ladder joints to link the four capacitors and lift the output capacitor voltage up. Currents are exponential functions. They have large values at the moment of power on, but they are small because in steady state.

The output voltage and current are

and



FIGURE 2.76
Quadruple-lift circuit.

The voltage transfer gain in continuous mode is

Other average voltages are

Other average currents

The current variations are

The voltage variations are

The variation ratio of output voltage is

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2.6.4.2.2 Negative Conversion Path

Capacitors C_{12}, C_{13}, C_{14}, and C_{15} perform characteristics to lift the capacitor voltage by four times the source voltage perform the function as ladder joints to link the four capacitors C_{12}, C_{13}, C_{14}, and C_{15} and lift the output capacitor voltage up. Currents are exponential functions. They have large values at the moment of power on, but they are small because in steady state.

The output voltage and current are

and

The voltage transfer gain in continuous mode is

From Equations 2.365 and 2.367, we define $M_Q = M_{Q^+} = M_{Q^-}$. The curve of M_Q versus k is shown in Figure 2.77.

Other average voltages are

Other average currents are

The current variation ratios are

FIGURE 2.77
Voltage transfer gain M_Q versus k.

The voltage variation ratios are

The variation ratio of output voltage is

The output voltage ripple is very small.

2.6.4.2.3 Discontinuous Conduction Mode

In order to obtain the mirror-symmetrical double-output voltages, we purposely select $L_1 = L_{11}$ and $R = R_1$ Therefore, we may define

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The freewheeling diode currents and become zero during switch-off before the next period switch-on. The boundary between continuous mode and DCM is

or

This boundary curve is shown in Figure 2.78. Comparing Equations 2.321, 2.335, 2.349, 2.359, and 2.369, it can be seen that this boundary curve has a minimum value of M_Q that is equal to 6.0, corresponding to $k = 1/3$.

In discontinuous mode, the currents and exist in the period between kT and , where is the filling efficiency, that is,

Considering Equation 2.369, therefore $0 < m_Q < 1$. Since the current becomes zero at , for the currents , and



FIGURE 2.78
The boundary between continuous and discontinuous modes and the output voltage versus the normalized load $z_N = R/fL$ (quadruple-lift circuit).

Therefore, the P/O voltage in DCM is

Because inductor current , so that

Since the current becomes zero at , for the current , we have

So

For the current ,

Therefore, the N/O voltage in DCM is

So

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that is, the output voltage will linearly increase when load resistance increases. It can be seen that the output voltage will increase when load resistance increases, as shown in Figure 2.78.

2.6.5 Summary

2.6.5.1 Positive Conversion Path

From the analysis and calculation in the previous sections, the common formulae can be obtained for all circuits:

for elementary circuit only;

for other lift circuits.

The current variations are

The voltage variations are

2.6.5.2 Negative Conversion Path

From the analysis and calculation in the previous sections, the common formulae can be obtained for all circuits:

The current variation ratios are

The voltage variation ratios are

2.6.5.3 Common Parameters

Usually, we select the loads $R = R_1$, $L = L_{11}$ so that we obtain In order to write common formulae for the boundaries between continuous and discontinuous modes and output voltage for all circuits, the circuits can be numbered. The definition is that subscript $n = 0$ means the elementary circuit, subscript $n = 1$ means the self-lift circuit, subscript $n = 2$ means the self-lift circuit, subscript $n = 3$ means the triple-lift circuit, subscript $n = 4$ means the quadruple-lift circuit, and so on.

The voltage transfer gain is

The characteristics of output voltage of all circuits are shown in Figure 2.79.

The freewheeling diode current's variation is

The boundaries are determined by the condition

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or

FIGURE 2.79
Output voltages of all double-output Luo-converters

Therefore, the boundaries between continuous and discontinuous modes for all circuits are

The filling efficiency is

The output voltage in discontinuous mode for all circuits is

where is the *Hong function*.

The boundaries between continuous and discontinuous modes of all circuits are shown in Figure 2.80. The curves of all M versus z_N state that the continuous mode area increases from M_E via M_S, M_R, and M_T to M_Q. The boundary of elementary circuit is monorising curve, but other curves are not monorising. There are minimum values of the boundaries of other circuits, which of M_S, M_R, M_T, and M_Q correspond at $k = 1/3$. The comparison among five circuits of double-output Luo-converters is shown in Table 2.3.

FIGURE 2.80
Boundaries between continuous and discontinuous modes of all double-output Luo-converters.

TABLE 2.3
Comparison among Five Circuits of Double-Output Luo-Converters

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3

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Positive-Output Super-Lift Luo-Converters

Voltage-lift (VL) technique has been successfully employed in design of DC/DC converters, for example, three-series Luo-converters (i.e., positive-, negative-, and double-output Luo-converters). However, the output voltage increases in *arithmetic progression.* Super-lift (SL) technique is more powerful than VL technique; its voltage transfer gain can be a very large number. SL technique implements the output voltage increasing in *geometric progression.* It effectively enhances the voltage transfer gain in power series.

3.1 Introduction

This chapter introduces positive-output SL Luo-converters, named so in order to differentiate these converters from existing VL converters. There are several subseries:

- Main series: Each circuit of the main series has only one switch *S*, *n* inductors for *n*th stage circuit, 2*n* capacitors, and (3n − 1) diodes.
- Additional series: Each circuit of the additional series has one switch *S*, *n* inductors for *n*th stage circuit, 2(*n* + 1) capacitors, and (3*n* + 1) diodes.
- Enhanced series: Each circuit of the enhanced series has one switch *S*, *n* inductors for *n*th stage circuit, 4*n* capacitors, and (5*n* − 1) diodes.
- Re-enhanced series: Each circuit of the re-enhanced series has one switch *S*, *n* inductors for *n*th stage circuit, 6*n* capacitors, and (7*n* − 1) diodes.
- Multiple (*j*)-enhanced series: Each circuit of the multiple (*j* times)-enhanced series has one switch *S*, *n* inductors for nth stage circuit, 2(1 + *j*)*n* capacitors, and [(3 + 2*j*)*n* − 1] diodes.

In order to concentrate the voltage enlargement, assume the converters are working in steady state with continuous conduction mode. The conduction duty ratio is *k*, the switch frequency is *f*, the switch period is $T = 1/f$, and the load is resistive load R. The input voltage and current are V_{in} and I_{in}, while the output voltage and current are V_o and I_o. Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_o \times I_o$. The voltage transfer gain is *G*: $G = Vo/V_{in}$.

3.2 Main Series

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The first three stages of the main series of positive-output SL Luo-converters are shown in Figures 3.1, 3.2 and 3.3. For convenience to explain, they are called elementary circuit, re-lift circuit, and triple-lift circuit, respectively, and are numbered as n = 1, 2, and 3.

3.2.1 Elementary Circuit

Figure 3.1 shows the elementary circuit and its equivalent circuits during switch-on and switch-off. The voltage across capacitor C_1 is charged to V_{in}. The current i_{L_1} flowing through inductor L_1 increases with voltage $-V_{in}$ during switch-on period kT and decreases with voltage $-(V_o - 2V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_o - 2V_{in}}{L_1}(1-k)T \tag{3.1}$$

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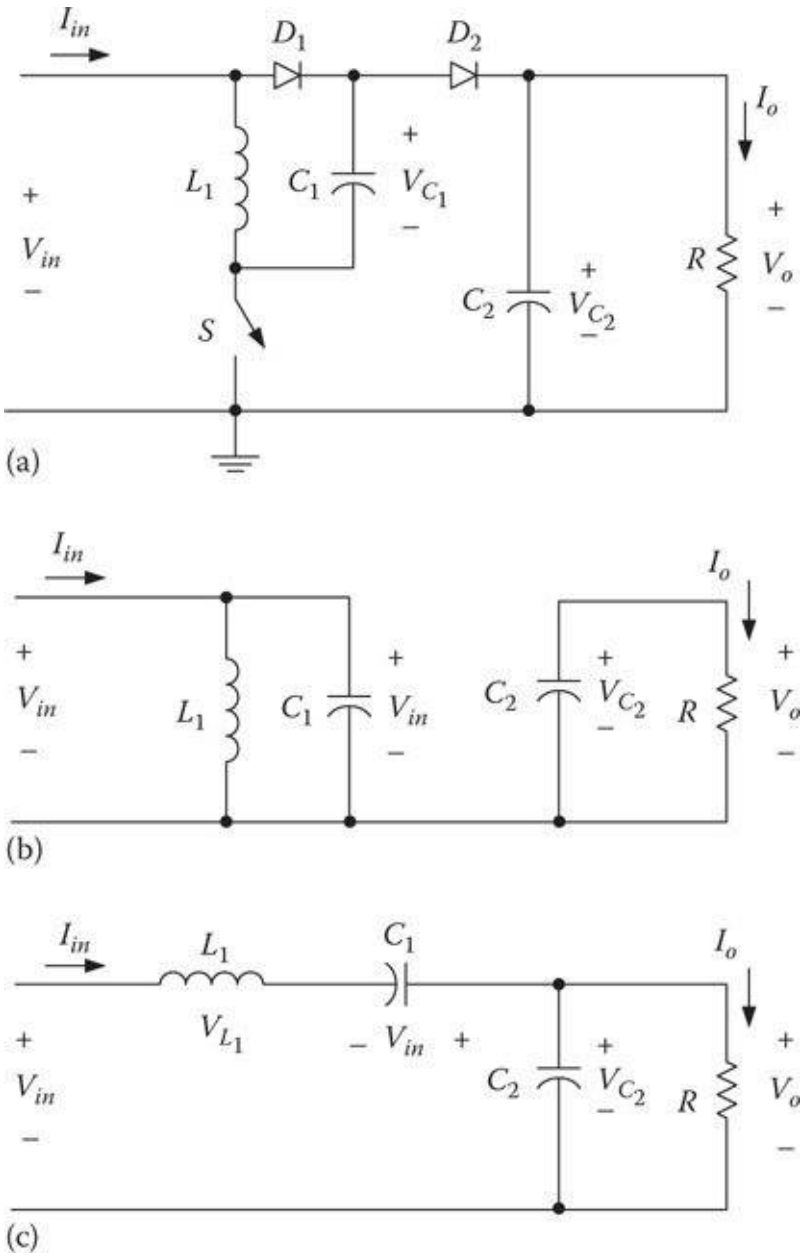


FIGURE 3.1
Elementary circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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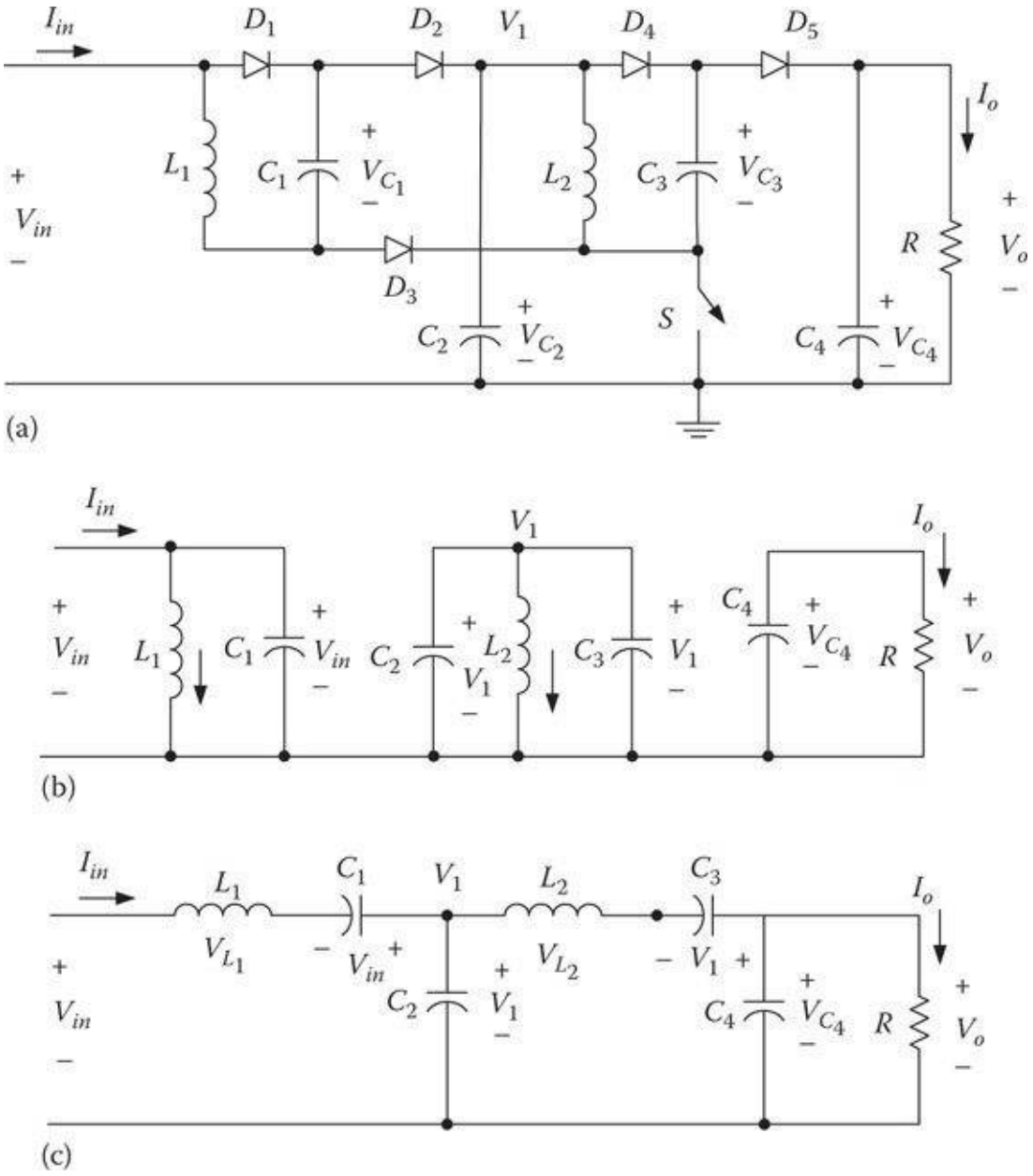


FIGURE 3.2
Re-lift circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$V_o = \frac{2-k}{1-k} V_{in} \tag{3.2}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} \tag{3.3}$$

The input current I_{in} is equal to (i_{L_1}) during switch-on and only equal to i_{C_1} during switch-off. Capacitor current i_{L_1} is equal to i_{L_1} during switching-off. In steady state, the average charge across capacitor C_1 should not change. The following relations are obtained:

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$$i_{in-off} = i_{L_1-off} = i_{C_1-off}$$

$$i_{in-on} = i_{L_1-on} + i_{C_1-on}$$

$$kTi_{C_1-on} = (1-k)Ti_{C_1-off}$$

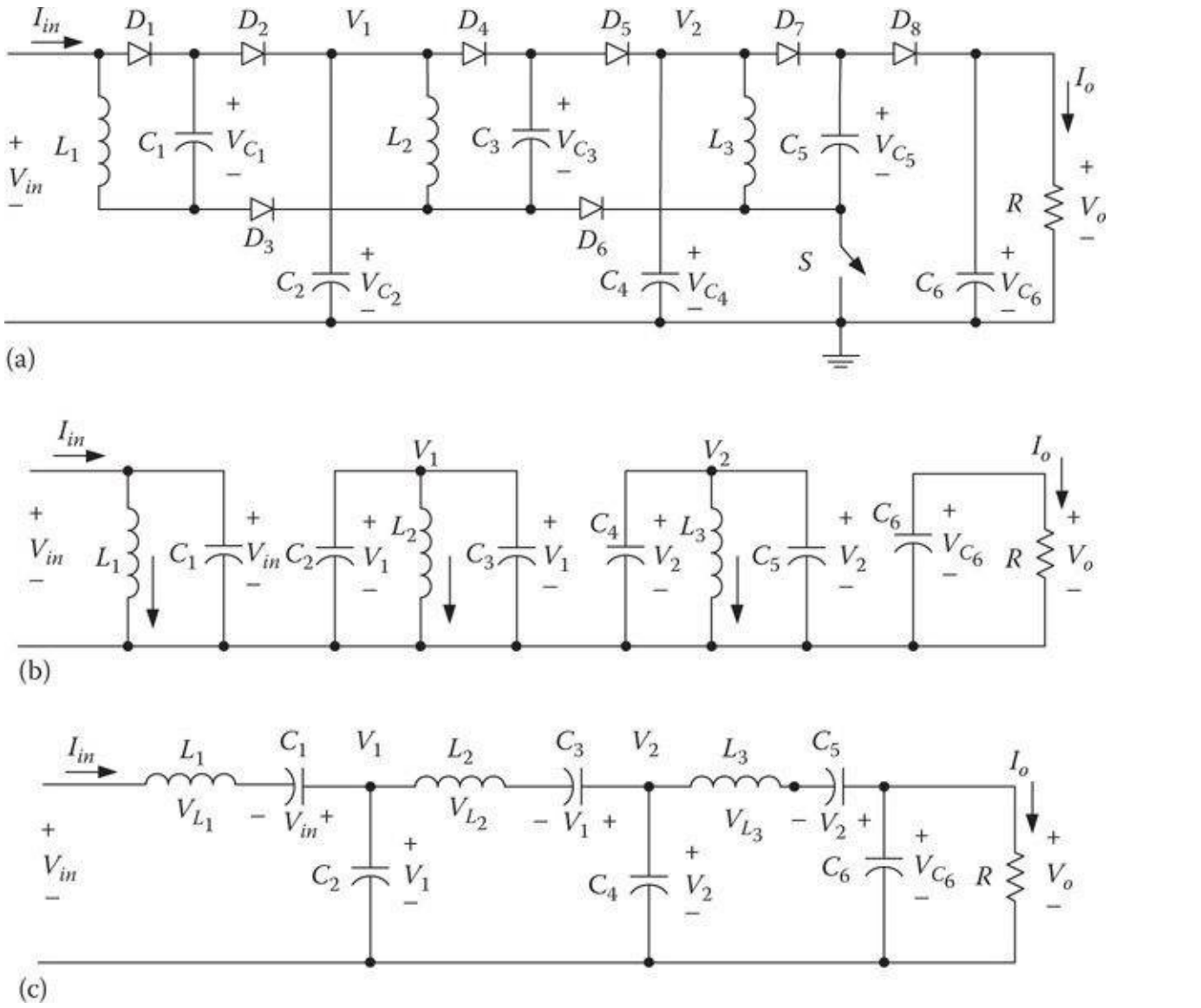


FIGURE 3.3
Triple-lift circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

If inductance L_1 is large enough, i_{L_1} is nearly equal to its average current I_{L_1}. Therefore,

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$$i_{in-off} = i_{C_1-off} = I_{L_1}$$

$$i_{in-on} = I_{L_1} + \frac{1-k}{k} I_{L_1} = \frac{I_{L_1}}{k}$$

$$i_{C_1-on} = \frac{1-k}{k} I_{L_1}$$

and the average input current

$$I_{in} = k i_{in-on} + (1-k) i_{in-off} = I_{L_1} + (1-k) I_{L_1} = (2-k) I_{L_1} \tag{3.4}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^2}{2(2-k)} \frac{R}{fL_1} \tag{3.5}$$

Usually, ξ_1 is small (much lower than unity), it means this converter normally works in the continuous mode.

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_2} = kT \frac{I_o}{C_2} = \frac{k}{fC_2} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_2} \tag{3.6}$$

Usually, R is in kΩ, f in 10 kHz, and C_2 in μF; this ripple is very smaller than 1%.

3.2.2 Re-Lift Circuit

The re-lift circuit is derived from elementary circuit by adding the parts (L_2–D_3–D_4–D_5–C_3–C_4). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.2. The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage V_1 across capacitor C_2 is $V_1 = [(2 - k)/(1 - k)]V_{in}$.

The voltage across capacitor C_3 is charged to V_1. The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_o - 2V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

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$$\Delta i_{L_2} = \frac{V_1}{L_2} kT = \frac{V_o - 2V_1}{L_2}(1-k)T \tag{3.7}$$

$$V_o = \frac{2-k}{1-k} V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in} \tag{3.8}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^2 \tag{3.9}$$

Similarly, the following relations are obtained:

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_{in}}{2-k}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \left(\frac{2-k}{1-k} - 1\right) I_o = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^4}{2(2-k)^3} \frac{R}{fL_1} \tag{3.10}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{2L_2 I_o} = \frac{k(1-k)^2 TV_o}{2(2-k)L_2 I_o} = \frac{k(1-k)^2}{2(2-k)} \frac{R}{fL_2} \tag{3.11}$$

and the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_4} \tag{3.12}$$

3.2.3 Triple-Lift Circuit

Triple-lift circuit is derived from re-lift circuit by double adding the parts (L_2–D_3–D_4–D_5–$C3$–C_4). Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 3.3. The voltage across capacitor C_1 is charged to V_{in}. As described earlier, the voltage V_1 across capacitor C_2 is $V_1 = [(2 - k)/(1 - k)]V_{in}$, and the voltage V_2 across capacitor C_4 is $V_2 = [(2 - k)/(1 - k)]^2 V_{in}$.

The voltage across capacitor C_5 is charged to V_2. The current flowing through inductor L_3increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_o - 2V_2)$ during switch-off $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

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$$\Delta i_{L_3} = \frac{V_2}{L_3} kT = \frac{V_o - 2V_2}{L_3}(1-k)T \tag{3.13}$$

$$V_o = \frac{2-k}{1-k} V_2 = \left(\frac{2-k}{1-k}\right)^2 V_1 = \left(\frac{2-k}{1-k}\right)^3 V_{in} \tag{3.14}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^3 \tag{3.15}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_{in}}{2-k}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(2-k)TV_{in}}{2L_1 I_{in}} = \frac{k(1-k)^6}{2(2-k)^5} \frac{R}{fL_1} \tag{3.16}$$

The variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{2(2-k)L_2 I_o} = \frac{kT(2-k)^4 V_o}{2(1-k)^3 L_2 I_o} = \frac{k(2-k)^4}{2(1-k)^3} \frac{R}{fL_2} \tag{3.17}$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{2L_3 I_o} = \frac{k(1-k)^2 TV_o}{2(2-k)L_2 I_o} = \frac{k(1-k)^2}{2(2-k)} \frac{R}{fL_3} \tag{3.18}$$

and the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_6} \tag{3.19}$$

3.2.4 Higher-Order Lift Circuit

The higher-order lift circuit can be designed by just multiple repeating the parts (L_2–D_3–D_4–D_5–C_3–C_4). For nth-order lift circuit, the final output voltage across capacitor C_{2n} is

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$$V_o = \left(\frac{2-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^n \tag{3.20}$$

The variation ratio of current i_{L_1} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2(2-k)^{2(n-i)+1}} \frac{R}{fL_i} \tag{3.21}$$

and the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{2n}} \tag{3.22}$$

3.3 Additional Series

Using two diodes and two capacitors (D_{11}–D_{12}–C_{11}–C_{12}), a circuit called “double/enhanced circuit” (DEC) can be constructed, which is shown in Figure 3.4. It is same as Figure 1.20 but with components renumbered. If the input voltage is V_{in}, the output voltage V_o can be $2V_{in}$, or other value that is higher than V_{in}. The DEC is very versatile to enhance DC/DC converter’s voltage transfer gain.

All circuits of the additional series of positive-output SL Luo-converters are derived from the corresponding circuits of the main series by adding a DEC. The first three stages of this series are shown in Figures 3.5, 3.6 and 3.7. For convenience to explain, they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit, respectively, and numbered as n = 1, 2, and 3.

3.3.1 Elementary Additional Circuit

This circuit is derived from elementary circuit by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.5. The voltage across capacitor C_1 is charged to V_{in}, and the voltage across capacitors C_2 and C_{11} is charged to V_1. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_o - 2V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$V_1 = \frac{2-k}{1-k} V_{in} \tag{3.23}$$

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and

$$V_{L_1} = \frac{k}{1-k} V_{in} \tag{3.24}$$

The output voltage is

$$V_o = V_{in} + V_{L_1} + V_1 = \frac{3-k}{1-k} V_{in} \tag{3.25}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3-k}{1-k} \tag{3.26}$$

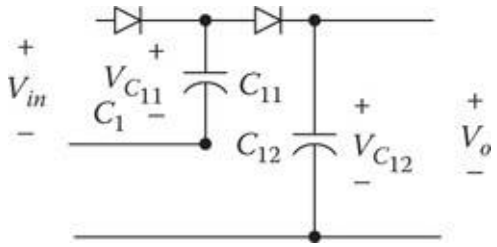


FIGURE 3.4
Double/enhanced circuit.

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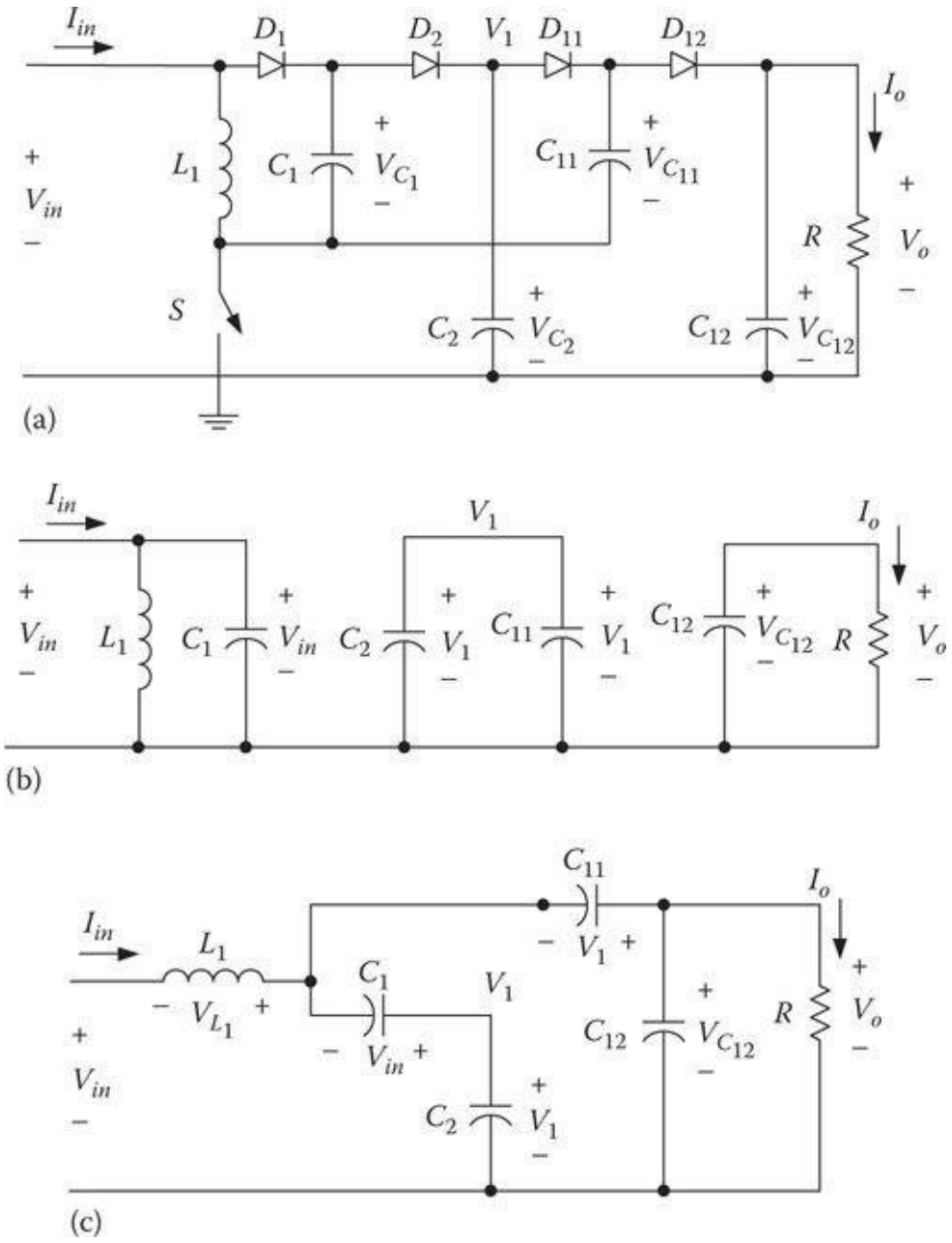


FIGURE 3.5
Elementary additional (enhanced) circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The following relations are derived:

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$$i_{in-off} = I_{L_1} = i_{C_{11}-off} + i_{C_1-off} = \frac{2I_o}{1-k} \qquad i_{in-on} = i_{L_1-on} + i_{C_1-on} = I_{L_1} + \frac{I_o}{k}$$

$$i_{C_1-on} = \frac{1-k}{k} i_{C_1-off} = \frac{I_o}{k} \qquad i_{C_1-off} = i_{C_2-off} = \frac{I_o}{1-k}$$

$$i_{C_2-off} = \frac{k}{1-k} i_{C_2-on} = \frac{k}{1-k} i_{C_{11}-on} = \frac{I_o}{1-k} \qquad i_{C_{11}-on} = \frac{1-k}{k} i_{C_{11}-off} = \frac{I_o}{k}$$

$$i_{C_{11}-off} = I_o + i_{C_{12}-off} = I_o + \frac{k}{1-k} i_{C_{12}-on} = \frac{I_o}{1-k} \qquad i_{C_{12}-off} = \frac{k}{1-k} i_{C_{12}-on} = \frac{kI_o}{1-k}$$

If inductance L_1 is large enough, i_{L_1} is nearly equal to its average current I_{L_1}. Therefore,

$$i_{in-off} = I_{L_1} = \frac{2I_o}{1-k} \qquad i_{in-on} = I_{L_1} + \frac{I_o}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right) I_o = \frac{1+k}{k(1-k)} I_o$$

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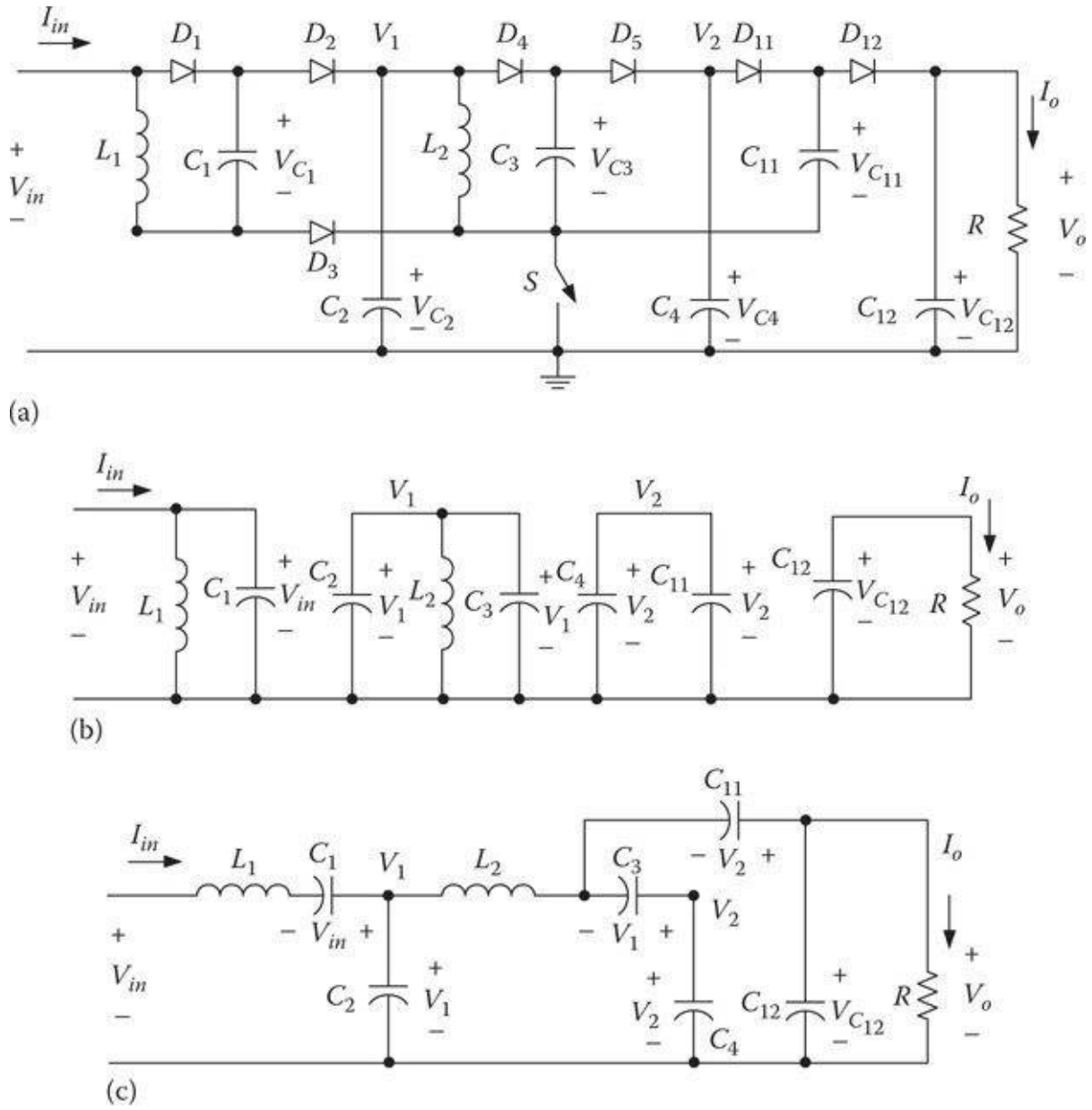


FIGURE 3.6
Re-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Verification:

$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right) I_o = \frac{3-k}{1-k} I_o$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

The variation of current i_{L_1} is

$$\Delta i_{L_1} = \frac{kTV_{in}}{L_1}$$

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Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{4(3-k)}\frac{R}{fL_1} \tag{3.27}$$

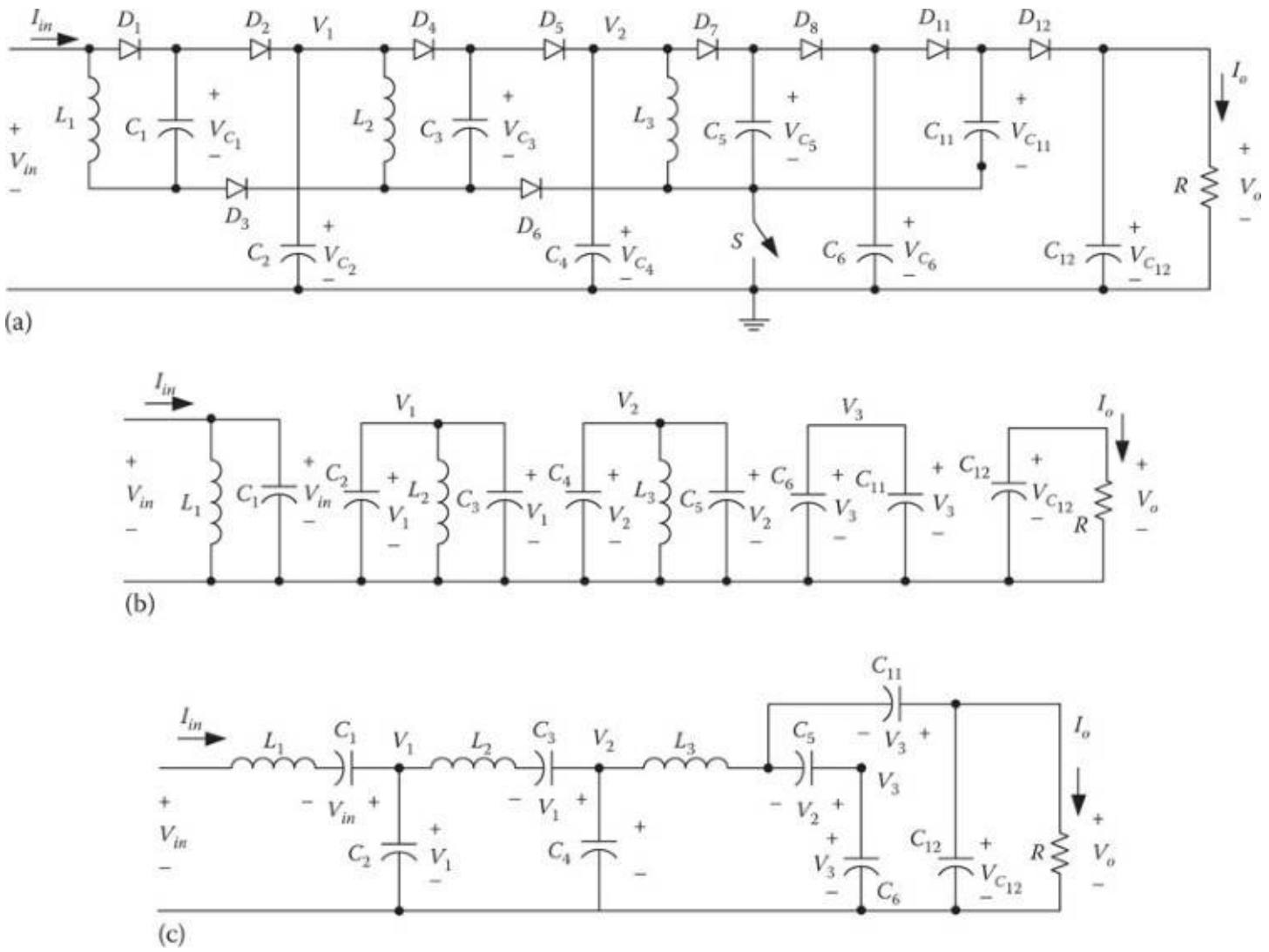


FIGURE 3.7
Triple-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{3.28}$$

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3.3.2 Re-Lift Additional Circuit

This circuit is derived from the re-lift circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 3.6. The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage across C_2 is $V_1 = (2 - k)/(1 - k)V_{in}$.

The voltage across capacitor C_3 is charged to V_1, and the voltage across capacitors C_4 and C_{11} is charged to V_2. The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_o - 2V_1)$ during switch-off $(1 - k)T$. Therefore,

$$V_2 = \frac{2-k}{1-k}V_1 = \left(\frac{2-k}{1-k}\right)^2 V_{in} \tag{3.29}$$

and

$$V_{L2} = \frac{k}{1-k}V_1 \tag{3.30}$$

The output voltage is

$$V_o = V_1 + V_{L2} + V_2 = \frac{2-k}{1-k}\frac{3-k}{1-k}V_{in} \tag{3.31}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k}\frac{3-k}{1-k} \tag{3.32}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1}kT \quad I_{L_1} = \frac{3-k}{(1-k)^2}I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2}kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_o} = \frac{k(1-k)^4}{2(2-k)(3-k)^2}\frac{R}{fL_1} \tag{3.33}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{4(3-k)}\frac{R}{fL_2} \tag{3.34}$$

The ripple voltage of output voltage υ_o is

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$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{3.35}$$

3.3.3 Triple-Lift Additional Circuit

This circuit is derived from the triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.7. The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage across C_2 is $V_1 = (2 - k)/(1 - k)V_{in}$, and the voltage across C_4 is V_2, $= (2 - k)/(1 - k)V_1 = (2 - k)/(1 - k)^2V_{in}$.

The voltage across capacitor C_5 is charged to V_2, and the voltage across capacitors C_6 and C_{11} is charged to V_3. The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_o - 2V_2)$ during switch-off $(1 - k)T$. Therefore,

$$V_3 = \frac{2-k}{1-k}V_2 = \left(\frac{2-k}{1-k}\right)^2 V_1 = \left(\frac{2-k}{1-k}\right)^3 V_{in} \tag{3.36}$$

and

$$V_{L3} = \frac{k}{1-k}V_2 \tag{3.37}$$

The output voltage is

$$V_o = V_2 + V_{L3} + V_3 = \left(\frac{2-k}{1-k}\right)^2 \frac{3-k}{1-k}V_{in} \tag{3.38}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^2 \frac{3-k}{1-k} \tag{3.39}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_o} = \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_o} \frac{(1-k)^3}{(2-k)^2(3-k)} V_o = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \tag{3.40}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_o} = \frac{k(1-k)^2 T}{2(3-k)L_2 I_o} \frac{(1-k)^2}{(2-k)(3-k)} V_o = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \tag{3.41}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)T}{4L_3 I_o} \frac{1-k}{3-k} V_o = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \tag{3.42}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT \frac{I_o}{C_{12}} = \frac{k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{3.43}$$

3.3.4 Higher-Order Lift Additional Circuit

The higher-order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. For *n*th-order lift additional circuit, the final output voltage is

$$V_o = \left(\frac{2-k}{1-k}\right)^{n-1} \frac{3-k}{1-k} V_{in}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^{n-1} \frac{3-k}{1-k} \tag{3.44}$$

Analogously, the variation ratio of current i_{Li} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \tag{3.45}$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \le 0 \end{cases} \quad \text{is the } \textit{Hong function}$$

$$u(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases} \quad \text{is the } \textit{unit-step function}$$

and the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{3.46}$$

3.4 Enhanced Series

All circuits of the enhanced series of positive-output SL Luo-converters are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in Figures 3.5, 3.8, and 3.9. For convenience, they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit, respectively, and numbered as n = 1, 2, and 3.

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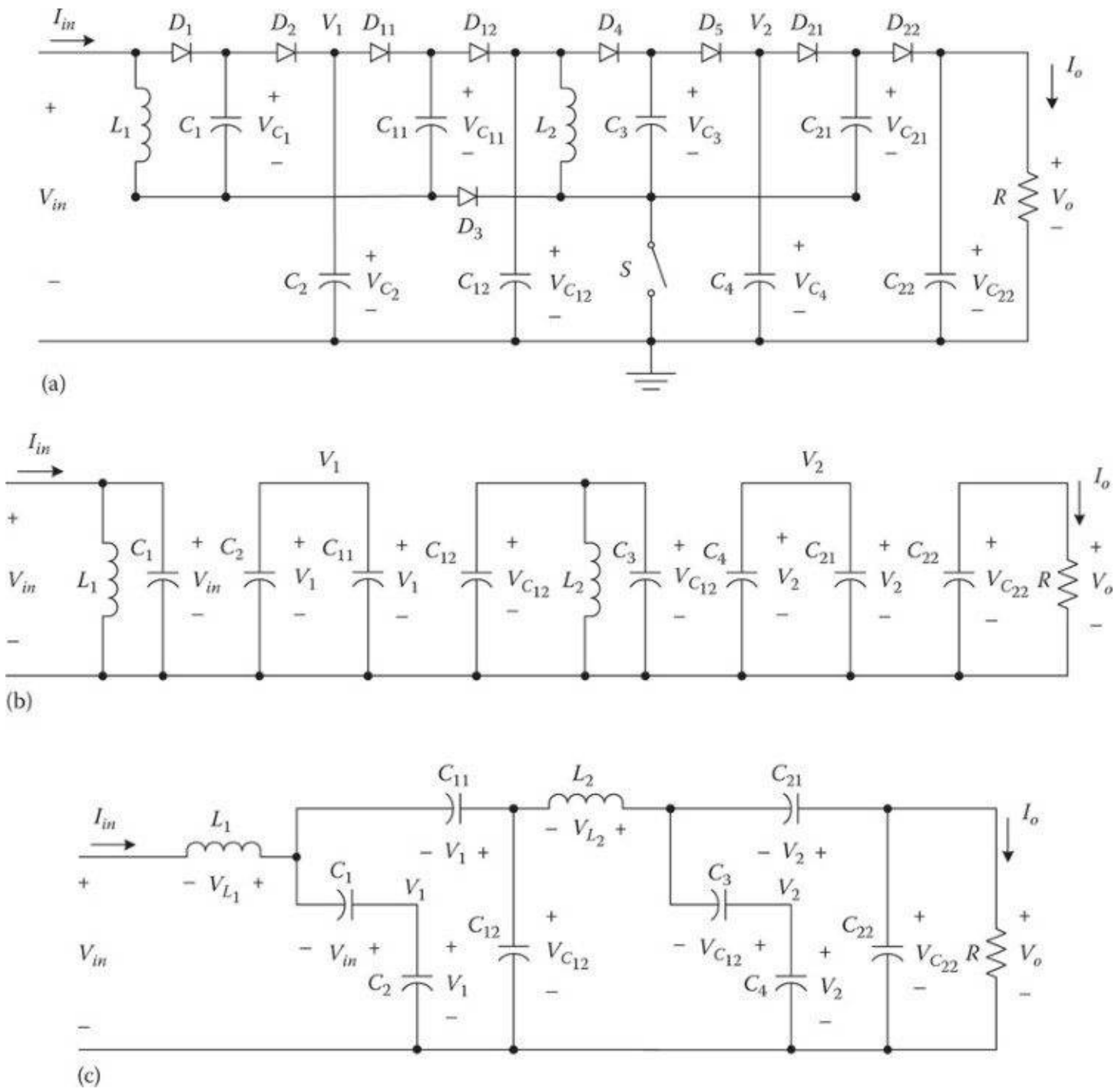


FIGURE 3.8
Re-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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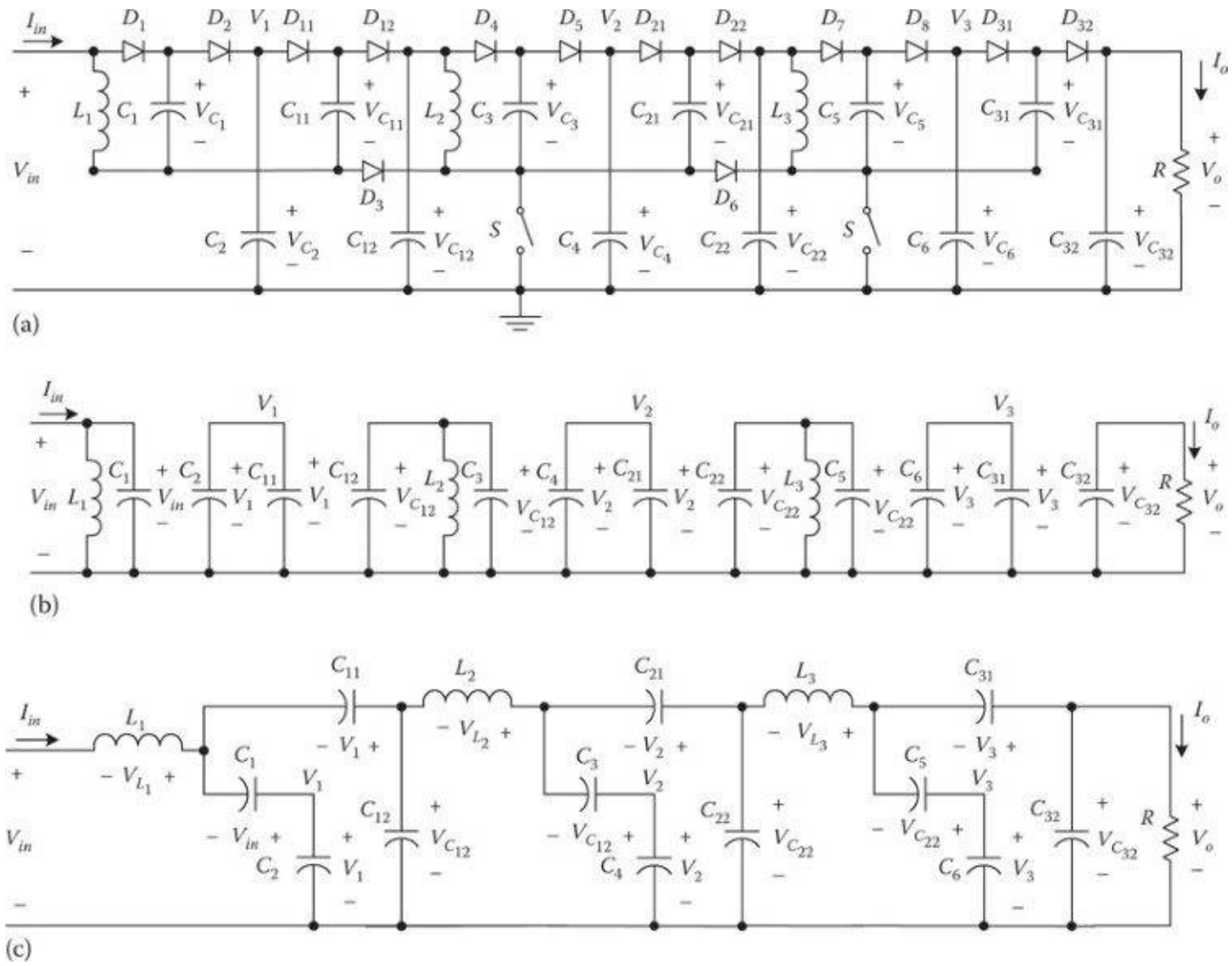


FIGURE 3.9
Triple-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

3.4.1 Elementary Enhanced Circuit

This circuit is same as the elementary additional circuit shown in Figure 3.5.

The output voltage is

$$V_o = V_{in} + V_{L1} + V_1 = \frac{3-k}{1-k} V_{in} \tag{3.25}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3-k}{1-k} \tag{3.26}$$

The variation of current i_{L_1} is

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$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{4(3-k)}\frac{R}{fL_1} \tag{3.27}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{3.28}$$

3.4.2 Re-Lift Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 3.8. As described in the previous section, the voltage across capacitor C_{12} is charged to $V_{C_{12}} = (3-k)/(1-k)V_{in}$.

The voltage across capacitor C_3 is charged to $V_{C_{12}}$, and the voltage across capacitors C_4 and C_{21} is charged to V_{C_4}:

$$V_{C_4} = \frac{2-k}{1-k}V_{C_{12}} = \frac{2-k}{1-k}\frac{3-k}{1-k}V_{in} \tag{3.47}$$

The current flowing through inductor L_2 increases with voltage $V_{C_{12}}$ during switch-on period kT and decreases with voltage $-(i_{L_1})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L_2} = \frac{k}{L_2}V_{C_{12}} = \frac{1-k}{L_2}(V_o - V_{C_4} - V_{C_{12}}) \tag{3.48}$$

$$V_o = \frac{3-k}{1-k}V_{C_{12}} = \left(\frac{3-k}{1-k}\right)^2 V_{in} \tag{3.49}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 \tag{3.50}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_o} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \tag{3.51}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \tag{3.52}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = kT \frac{I_o}{C_{22}} = \frac{k}{fC_{22}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22}} \tag{3.53}$$

3.4.3 Triple-Lift Enhanced Circuit

This circuit is derived from triple-lift circuit of the main series by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 3.9. As described in the previous section, the voltage across capacitor C_{12} is charged to $V_{C_{22}} = (3 - k)/(1 - k)V_{in}$, and the voltage across capacitor C_{22} is charged to $V_{C22} = (3 - k)/(1 - k)^2 V_{in}$.

The voltage across capacitor C_5 is charged to $V_{C_{22}}$, and the voltage across capacitors C_6 and C_{31} is charged to V_{C_6} :

$$V_{C_6} = \frac{2-k}{1-k} V_{C_{22}} = \frac{2-k}{1-k} \left(\frac{3-k}{1-k} \right)^2 V_{in} \tag{3.54}$$

The current flowing through inductor L_3 increases with voltage $V_{C_{22}}$ during switch-on period kT and decreases with voltage $-(V_o - V_{C_6} - V_{C_{22}})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_3} = \frac{k}{L_3} V_{C_{22}} = \frac{1-k}{L_3} (V_o - V_{C_6} - V_{C_{22}}) \tag{3.55}$$

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$$V_o = \frac{3-k}{1-k} V_{C22} = \left(\frac{3-k}{1-k}\right)^3 V_{in} \tag{3.56}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^3 \tag{3.57}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 T V_{in}}{2(2-k)(3-k)L_1 I_o} = \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_o} \frac{(1-k)^3}{(2-k)^2(3-k)} V_o = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \tag{3.58}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 T V_1}{2(3-k)L_2 I_o} = \frac{k(1-k)^2 T}{2(3-k)L_2 I_o} \frac{(1-k)^2}{(2-k)(3-k)} V_o = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \tag{3.59}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)T}{4L_3 I_o} \frac{1-k}{3-k} V_o = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \tag{3.60}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32}} = kT \frac{I_o}{C_{32}} = \frac{k}{fC_{32}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32}} \tag{3.61}$$

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3.4.4 Higher-Order Lift Enhanced Circuit

The higher-order lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage circuit. For the *n*th-order lift enhanced circuit, the final output voltage is

$$V_o = \left(\frac{3-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^n \tag{3.62}$$

Analogously, the variation ratio of current i_{L_1} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \tag{3.63}$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \le 0 \end{cases} \quad \text{is the } \textit{Hong function}$$

$$u(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases} \quad \text{is the } \textit{unit-step function}$$

and the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2}} \tag{3.64}$$

3.5 Re-Enhanced Series

All circuits of the re-enhanced series of positive-output SL Luo-converters are derived from the corresponding circuits of the main series by adding the DEC twice in each stage circuit.

The first three stages of this series are shown in Figures 3.10, 3.11 and 3.12. For convenience to explain, they are named elementary re-enhanced circuit, re-lift re-enhanced circuit, and triple-lift re-enhanced circuit, respectively, and numbered as n = 1, 2, and 3.

3.5.1 Elementary Re-Enhanced Circuit

This circuit is derived from the elementary circuit by adding the DEC twice. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.10.

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The output voltage is

$$V_o = V_{in} + V_{L_1} + V_{C_{12}} = \frac{4-k}{1-k} V_{in} \tag{3.65}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{4-k}{1-k} \tag{3.66}$$

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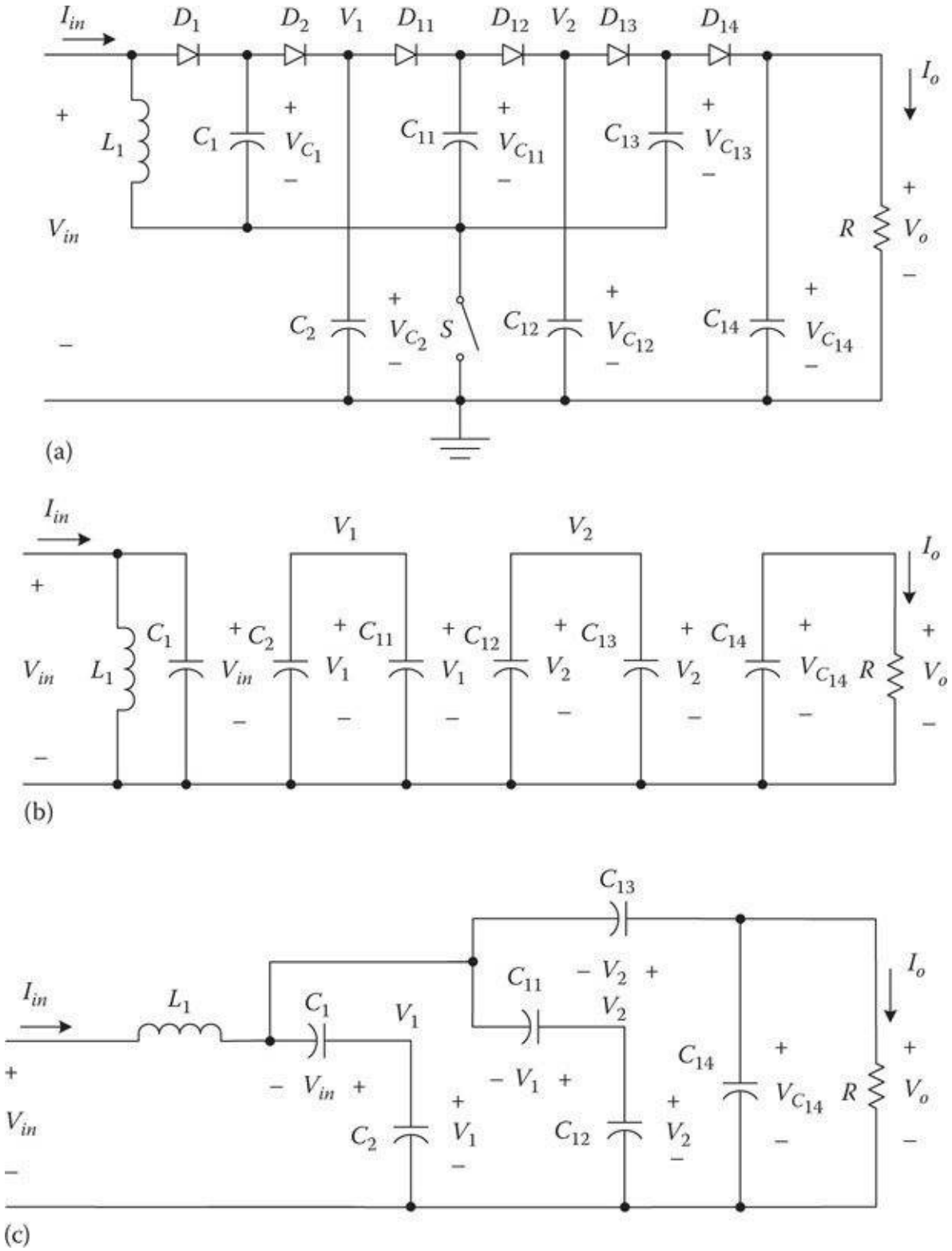


FIGURE 3.10
Elementary re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

where

$$V_{C_2} = \frac{2-k}{1-k} V_{in} \tag{3.67}$$

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$$V_{C_{12}} = \frac{3-k}{1-k} V_{in} \tag{3.68}$$

$$V_{L_1} = \frac{k}{1-k} V_{in} \tag{3.69}$$

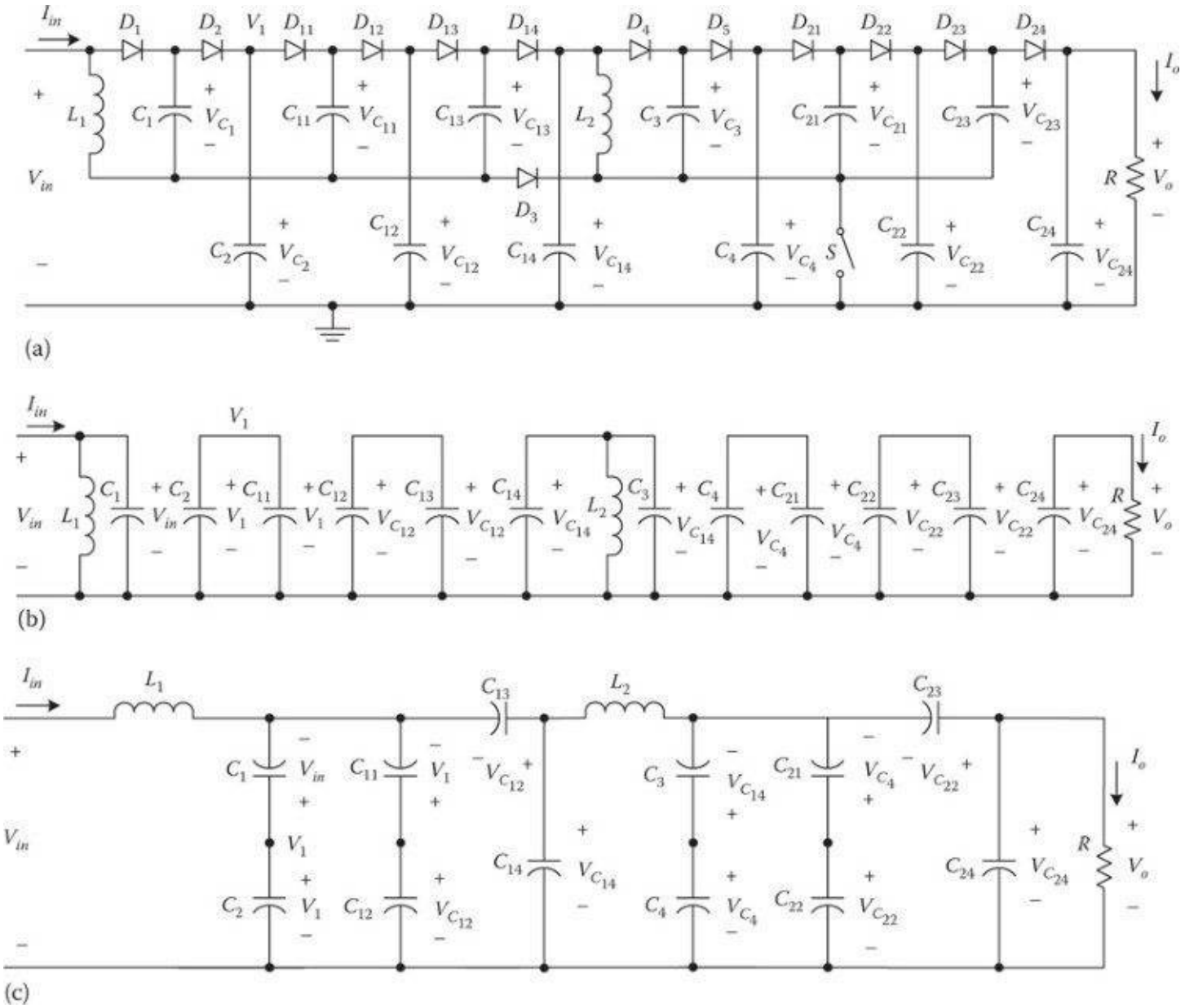


FIGURE 3.11
Re-lift re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The following relations are obtained:

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$$i_{in-off} = I_{L_1} = i_{C_{11}-off} + i_{C_1-off} = \frac{2I_o}{1-k} \qquad i_{in-on} = i_{L_1-on} + i_{C_1-on} = I_{L_1} + \frac{I_o}{k}$$

$$i_{C_1-on} = \frac{1-k}{k} i_{C_1-off} = \frac{I_o}{k} \qquad i_{C_1-off} = i_{C_2-off} = \frac{I_o}{1-k}$$

$$i_{C_2-off} = \frac{k}{1-k} i_{C_2-on} = \frac{k}{1-k} i_{C_{11}-on} = \frac{I_o}{1-k} \qquad i_{C_{11}-on} = \frac{1-k}{k} i_{C_{11}-off} = \frac{I_o}{k}$$

$$i_{C_{11}-off} = I_o + i_{C_{12}-off} = I_o + \frac{k}{1-k} i_{C_{12}-on} = \frac{I_o}{1-k} \qquad i_{C_{12}-off} = \frac{k}{1-k} i_{C_{12}-on} = \frac{kI_o}{1-k}$$

If inductance L_1 is large enough, i_{L_1} is nearly equal to its average current I_{L_1} Therefore,

$$i_{in-off} = I_{L_1} = \frac{2I_o}{1-k} \qquad i_{in-on} = I_{L_1} + \frac{I_o}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right) I_o = \frac{1+k}{k(1-k)} I_o$$

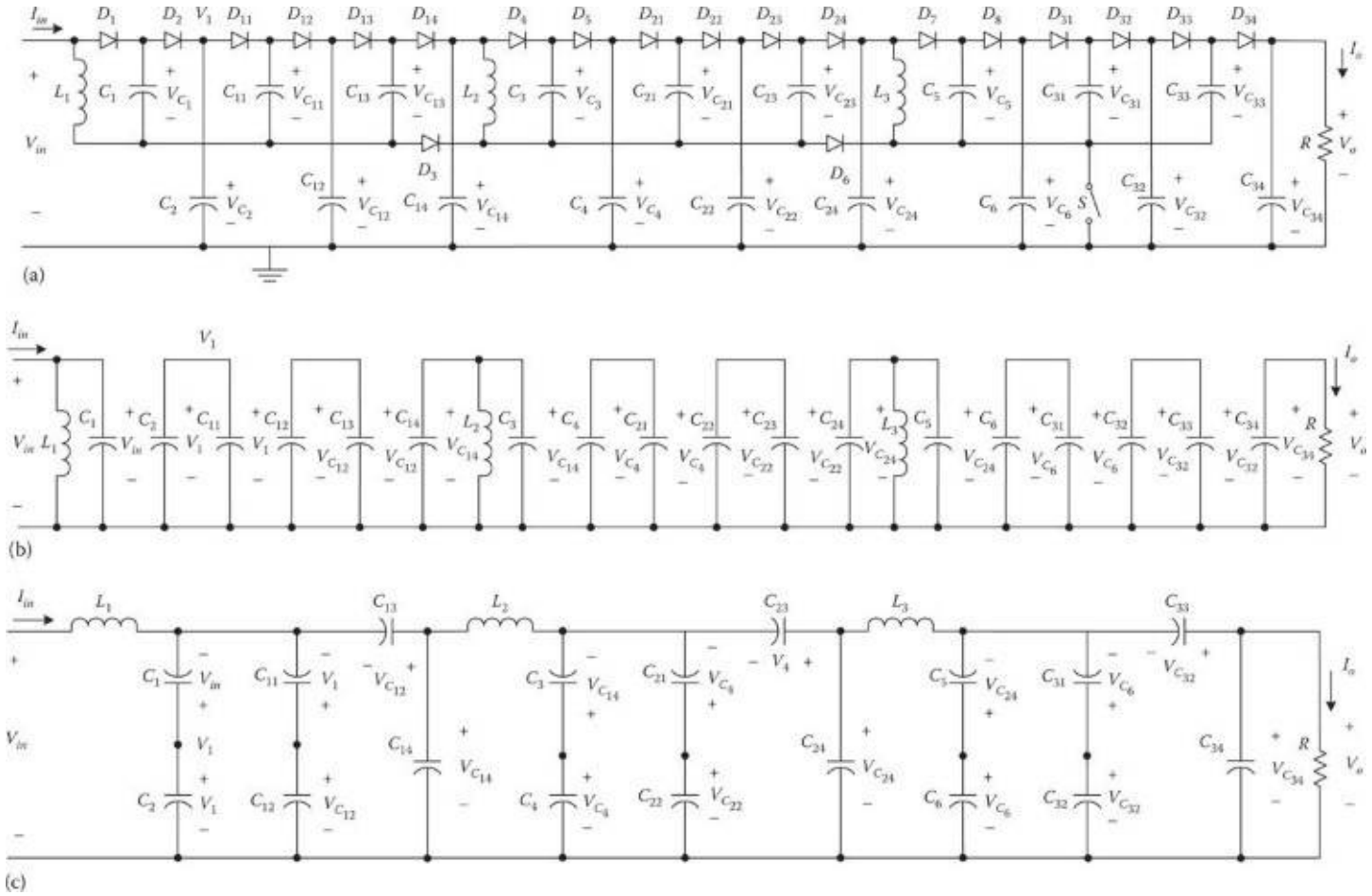


FIGURE 3.12
Triple-lift re-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Verification:

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$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right) I_o = \frac{3-k}{1-k} I_o$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation of current L_l is

$$\Delta i_{L1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \tag{3.70}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{14}} = kT \frac{I_o}{C_{14}} = \frac{k}{fC_{14}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{14}} \tag{3.71}$$

3.5.2 Re-Lift Re-Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC twice in each stage circuit. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.11.

The voltage across capacitor C_{14} is

$$V_{C_{14}} = \frac{4-k}{1-k} V_{in} \tag{3.72}$$

By the same analysis,

$$V_o = \frac{4-k}{1-k} V_{C_{14}} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \tag{3.73}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^2 \tag{3.74}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_o} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \tag{3.75}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \tag{3.76}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{24}} = kT \frac{I_o}{C_{24}} = \frac{k}{fC_{24}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{24}} \tag{3.77}$$

3.5.3 Triple-Lift Re-Enhanced Circuit

This circuit is derived from the triple-lift circuit of the main series by adding the DEC twice in each stage circuit. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.12.

The voltage across capacitor C_{14} is

$$V_{C_{14}} = \frac{4-k}{1-k} V_{in} \tag{3.78}$$

The voltage across capacitor C_{24} is

$$V_{C_{24}} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \tag{3.79}$$

By the same analysis,

$$V_o = \frac{4-k}{1-k} V_{C_{24}} = \left(\frac{4-k}{1-k}\right)^3 V_{in} \tag{3.80}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^3 \tag{3.81}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_o} = \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_o} \frac{(1-k)^3}{(2-k)^2(3-k)} V_o = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \tag{3.82}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_o} = \frac{k(1-k)^2 T}{2(3-k)L_2 I_o} \frac{(1-k)^2}{(2-k)(3-k)} V_o = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \tag{3.83}$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)T}{4L_3 I_o} \frac{1-k}{3-k} V_o = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \tag{3.84}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{34}} = kT \frac{I_o}{C_{34}} = \frac{k}{fC_{34}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{34}} \tag{3.85}$$

3.5.4 Higher-Order Lift Re-Enhanced Circuit

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Higher-order lift additional circuits are derived from the corresponding circuits of the main series by adding DEC twice in each stage circuit. For the *n*th-order lift additional circuit, the final output voltage is

$$V_o = \left(\frac{4-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^n \tag{3.86}$$

Analogously, the variation ratio of current i_{Li} through inductor L_i (i = 1, 2, 3,…, *n*) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \tag{3.87}$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \le 0 \end{cases} \quad \text{is the } \textit{Hong function}$$

$$u(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases} \quad \text{is the } \textit{unit-step function}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n4}} \tag{3.88}$$

3.6 Multiple-Enhanced Series

All circuits of the multiple-enhanced series of positive-output SL Luo-converters are derived from the corresponding circuits of the main series by adding the DEC multiple (*j*) times in each stage circuit. The first three stages of this series are shown in Figures 3.13, 3.14 and 3.15. For convenience to explain, they are called elementary multiple-enhanced circuit, re-lift multiple-enhanced circuit, and triple-lift multiple-enhanced circuit, respectively, and numbered as *n* = 1, 2, and 3.

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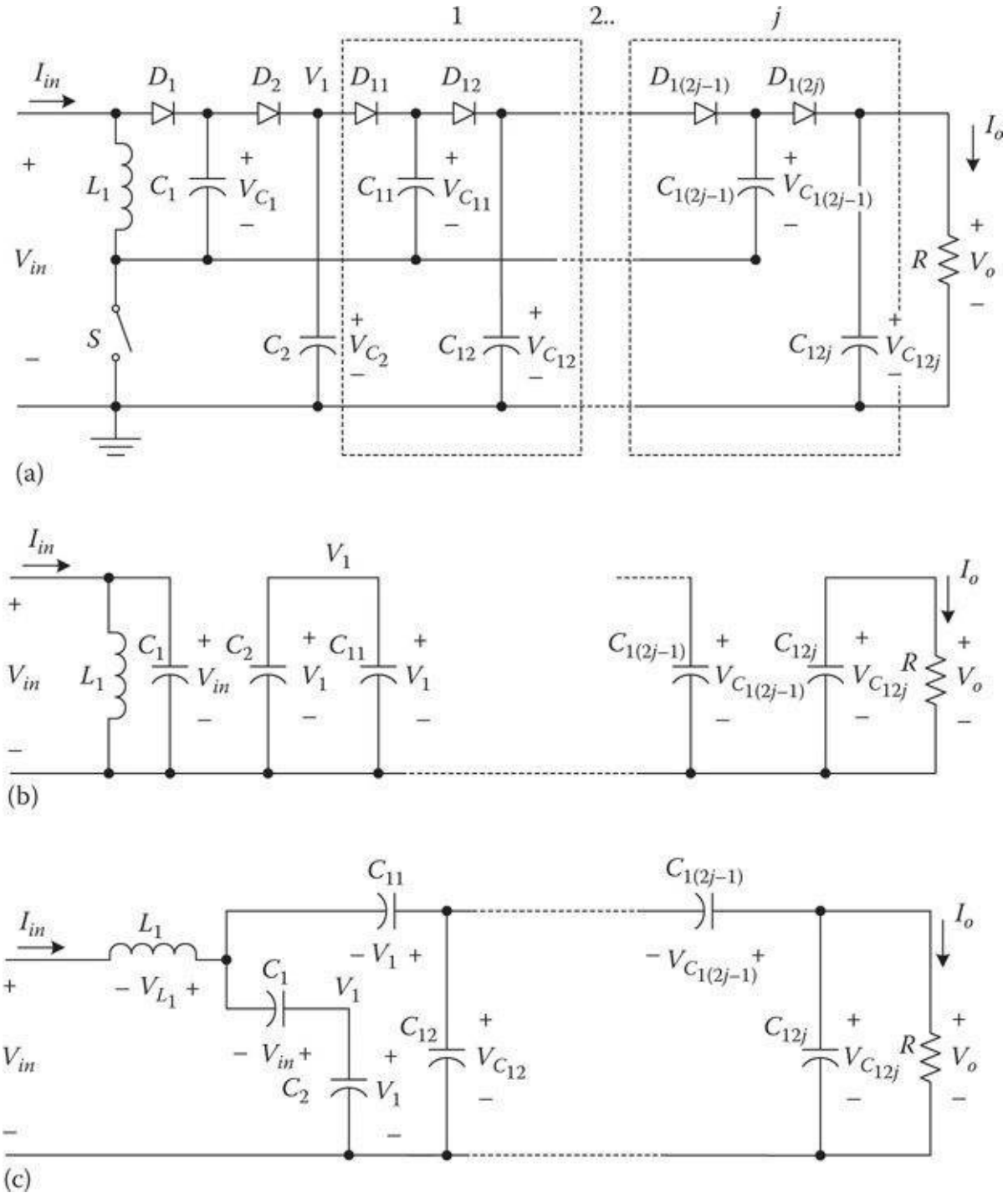


FIGURE 3.13
Elementary multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

3.6.1 Elementary Multiple-Enhanced Circuit

This circuit is derived from the elementary circuit of the main series by adding the DEC multiple (j) times. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.13.

The output voltage is

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$$V_o = \frac{j+2-k}{1-k} V_{in} \tag{3.89}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{j+2-k}{1-k} \tag{3.90}$$

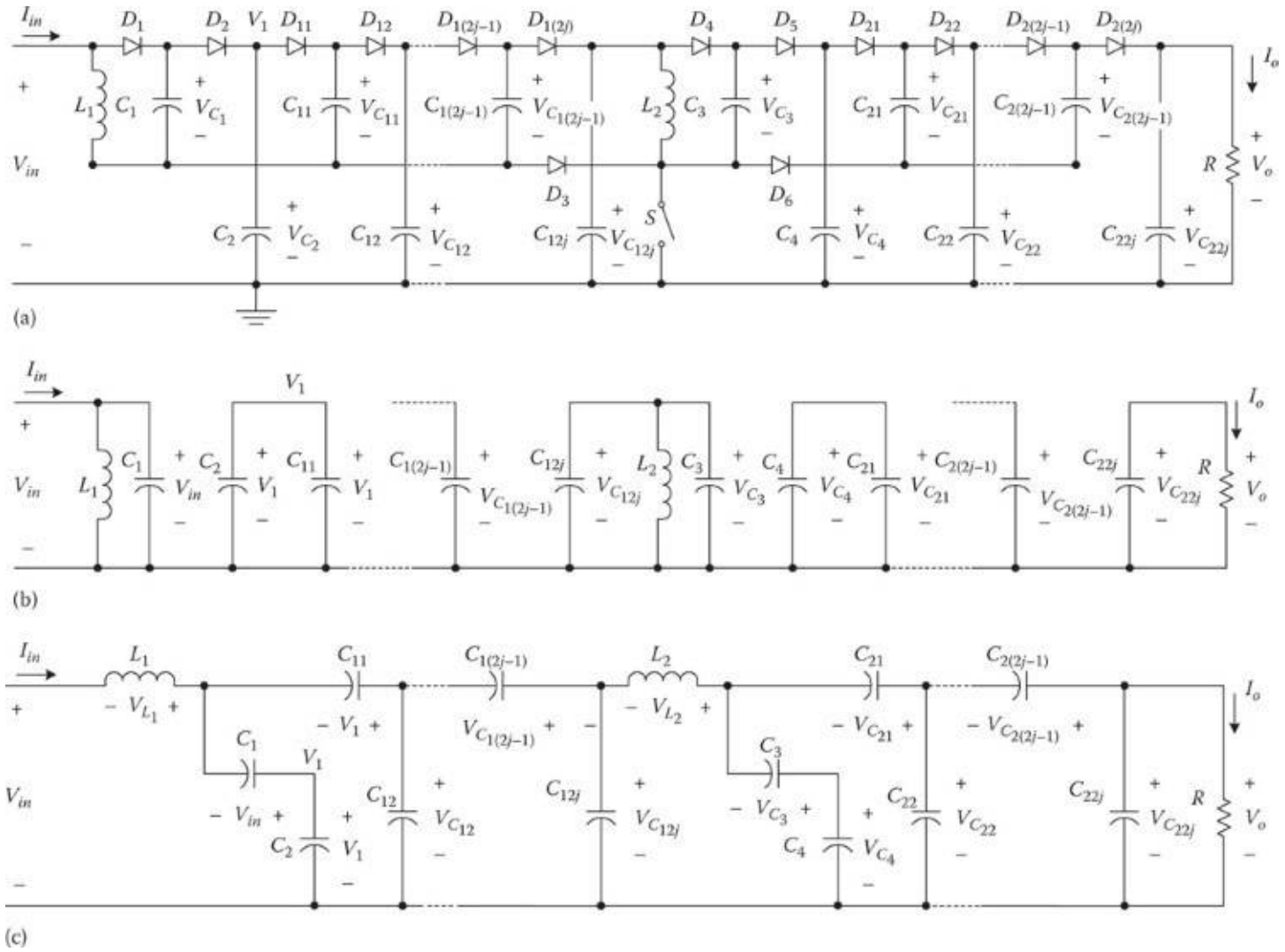


FIGURE 3.14
Re-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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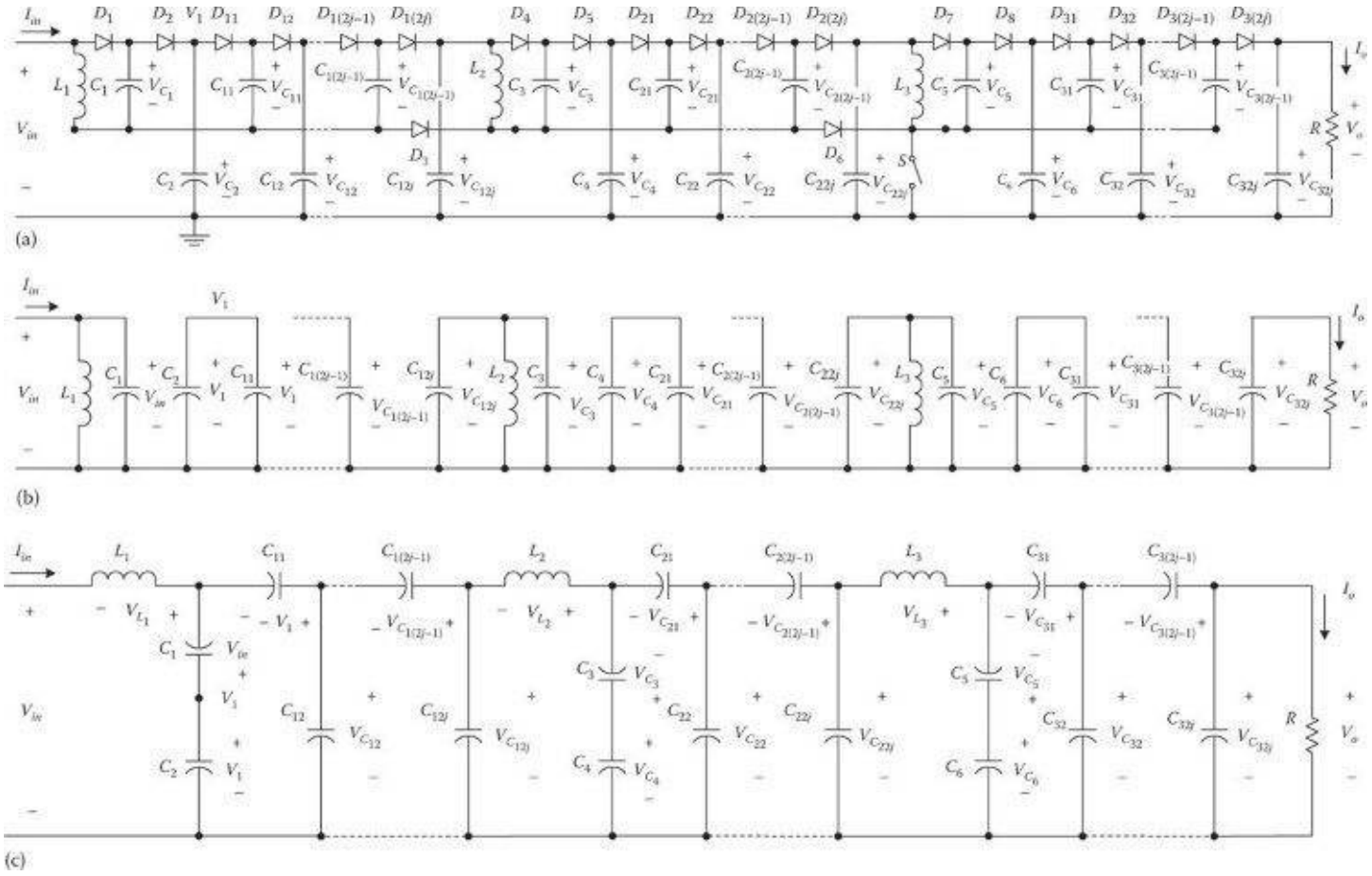


FIGURE 3.15
Triple-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The following relations are obtained:

$$i_{in-off} = I_{L_1} = i_{C_{11}-off} + i_{C_1-off} = \frac{2I_o}{1-k} \qquad i_{in-on} = i_{L_1-on} + i_{C_1-on} = I_{L_1} + \frac{I_o}{k}$$

$$i_{C_1-on} = \frac{1-k}{k} i_{C_1-off} = \frac{I_o}{k} \qquad i_{C_1-off} = i_{C_2-off} = \frac{I_o}{1-k}$$

$$i_{C_2-off} = \frac{k}{1-k} i_{C_2-on} = \frac{k}{1-k} i_{C_{11}-on} = \frac{I_o}{1-k} \qquad i_{C_{11}-on} = \frac{1-k}{k} i_{C_{11}-off} = \frac{I_o}{k}$$

$$i_{C_{11}-off} = I_o + i_{C_{12}-off} = I_o + \frac{k}{1-k} i_{C_{12}-on} = \frac{I_o}{1-k} \qquad i_{C_{12}-off} = \frac{k}{1-k} i_{C_{12}-on} = \frac{kI_o}{1-k}$$

If inductance L_1 is large enough, i_{L_1} is nearly equal to its average current I_{L_1}. Therefore,

$$i_{in-off} = I_{L1} = \frac{2I_o}{1-k} \qquad i_{in-on} = I_{L_1} + \frac{I_o}{k} = \left(\frac{2}{1-k} + \frac{1}{k}\right) I_o = \frac{1+k}{k(1-k)} I_o$$

Verification:

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$$I_{in} = ki_{in-on} + (1-k)i_{in-off} = \left(\frac{1+k}{1-k} + 2\right) I_o = \frac{3-k}{1-k} I_o$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation of current i_{L_1} is

$$\Delta i_{L_1} = \frac{kTV_{in}}{L_1}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_1} \tag{3.91}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12j}} = kT \frac{I_o}{C_{12j}} = \frac{k}{fC_{12j}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12j}} \tag{3.92}$$

3.6.2 Re-Lift Multiple-Enhanced Circuit

This circuit is derived from the re-lift circuit of the main series by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 3.14.

The voltage across capacitor C_{12j} is

$$V_{C_{12j}} = \frac{j+2-k}{1-k} V_{in} \tag{3.93}$$

The output voltage across capacitor C_{22j} is

$$V_o = V_{C_{22j}} = \left(\frac{j+2-k}{1-k}\right)^2 V_{in} \tag{3.94}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^2 \tag{3.95}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{2(3-k)L_1 I_o} = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_1} \tag{3.96}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_2} \tag{3.97}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = kT \frac{I_o}{C_{22j}} = \frac{k}{fC_{22j}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22j}} \tag{3.98}$$

3.6.3 Triple-Lift Multiple-Enhanced Circuit

This circuit is derived from the triple-lift circuit of the main series by adding the DEC multiple (j) times in each stage circuit. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 3.15.

The voltage across capacitor C_{12j} is

$$V_{C12j} = \frac{j+2-k}{1-k} V_{in} \tag{3.99}$$

The voltage across capacitor C_{22j} is

$$V_{C_{22j}} = \left(\frac{j+2-k}{1-k} \right)^2 V_{in} \tag{3.100}$$

By the same analysis,

$$V_o = \frac{j+2-k}{1-k} V_{C_{22j}} = \left(\frac{j+2-k}{1-k} \right)^3 V_{in} \tag{3.101}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^3 \tag{3.102}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Considering

$$\frac{V_{in}}{I_{in}} = \left(\frac{1-k}{2-k}\right)^2 \frac{V_o}{I_o} = \left(\frac{1-k}{2-k}\right)^2 R$$

the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_o} = \frac{k(1-k)^3 T}{2(2-k)(3-k)L_1 I_o} \frac{(1-k)^3}{(2-k)^2(3-k)} V_o = \frac{k(1-k)^6}{2(2-k)^3(3-k)^2} \frac{R}{fL_1} \tag{3.103}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{2(3-k)L_2 I_o} = \frac{k(1-k)^2 T}{2(3-k)L_2 I_o} \frac{(1-k)^2}{(2-k)(3-k)} V_o = \frac{k(1-k)^4}{2(2-k)(3-k)^2} \frac{R}{fL_2} \tag{3.104}$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)T}{4L_3 I_o} \frac{1-k}{3-k} V_o = \frac{k(1-k)^2}{4(3-k)} \frac{R}{fL_3} \tag{3.105}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32j}} = kT \frac{I_o}{C_{32j}} = \frac{k}{fC_{32j}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32j}} \tag{3.106}$$

3.6.4 Higher-Order Lift Multiple-Enhanced Circuit

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Higher-order lift multiple-enhanced circuits can be derived from the corresponding circuits of the main series converters by adding the DEC multiple (j) times in each stage circuit. For the nth-order lift additional circuit, the final output voltage is

$$V_o = \left(\frac{j+2-k}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^n \tag{3.107}$$

Analogously, the variation ratio of current i_{Li} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2[2(2-k)]^{h(n-i)}(2-k)^{2(n-i)+1}(3-k)^{2u(n-i-1)}} \frac{R}{fL_i} \tag{3.108}$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \le 0 \end{cases} \quad \text{is the } \textit{Hong function}$$

$$u(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases} \quad \text{is the } \textit{unit-step function}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2j}} \tag{3.109}$$

3.7 Summary of Positive-Output Super-Lift Luo-Converters

All circuits of positive-output SL Luo-converters can be shown in Figure 3.16 as the family tree.

From the analysis in previous sections, the common formula to calculate the output voltage is presented:

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$$V_o = \begin{cases} \left(\frac{2-k}{1-k}\right)^n V_{in} & main_series \\ \left(\frac{2-k}{1-k}\right)^{n-1}\left(\frac{3-k}{1-k}\right) V_{in} & additional_series \\ \left(\frac{3-k}{1-k}\right)^n V_{in} & enhanced_series \\ \left(\frac{4-k}{1-k}\right)^n V_{in} & re\text{-}enhanced_series \\ \left(\frac{j+2-k}{1-k}\right)^n V_{in} & multiple\text{-}enhanced_series \end{cases} \quad (3.110)$$

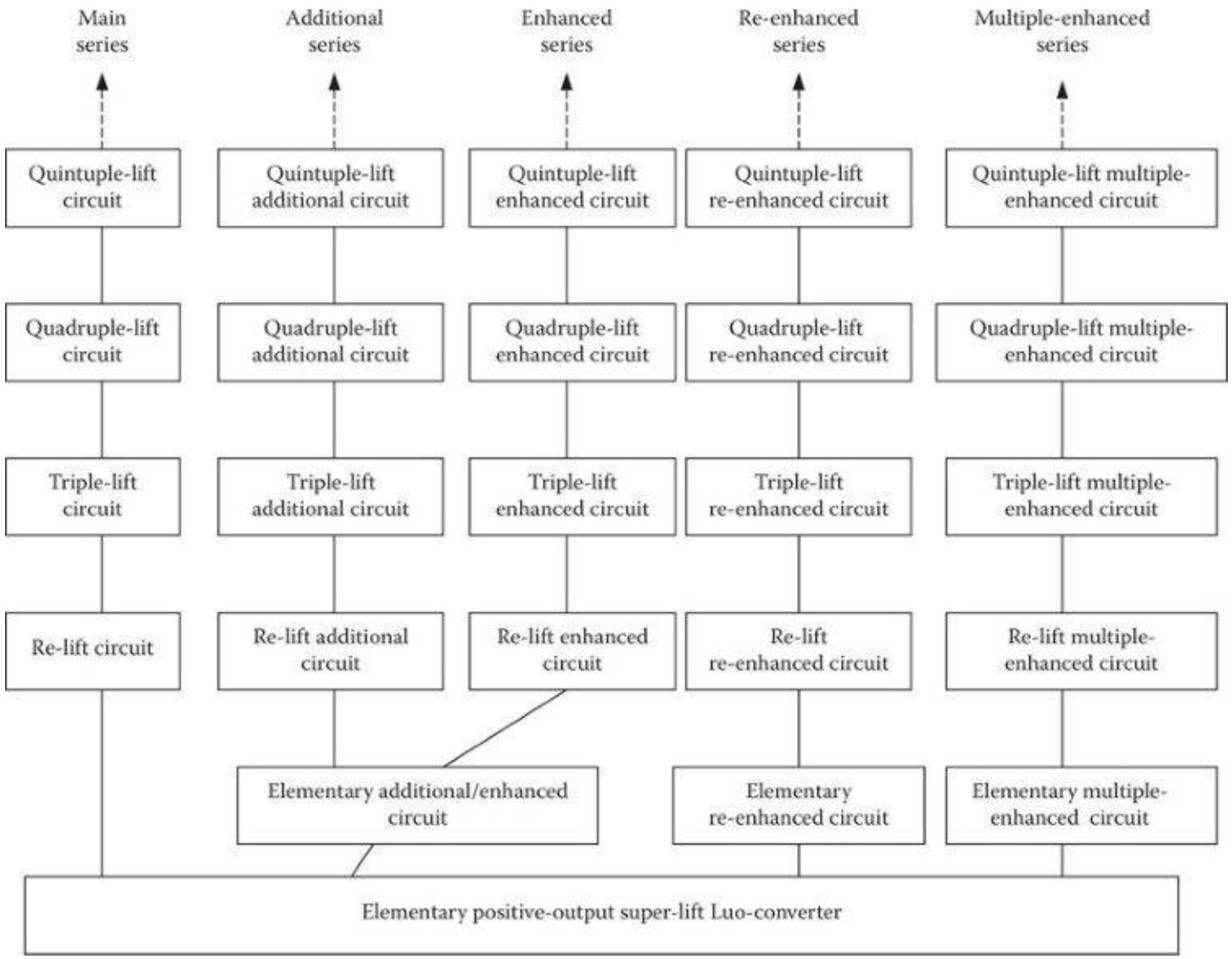


FIGURE 3.16
The family of positive-output super-lift Luo-converters.

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The voltage transfer gain is

$$G=\frac{V_o}{V_{in}}=\begin{cases}\left(\dfrac{2-k}{1-k}\right)^n & main_series\\ \left(\dfrac{2-k}{1-k}\right)^{n-1}\left(\dfrac{3-k}{1-k}\right) & additional_series\\ \left(\dfrac{3-k}{1-k}\right)^n & enhanced_series\\ \left(\dfrac{4-k}{1-k}\right)^n & re-enhanced_series\\ \left(\dfrac{j+2-k}{1-k}\right)^n & multiple-enhanced_series\end{cases} \tag{3.111}$$

In order to show the advantages of SL Luo-converters, their voltage transfer gains can be compared to that of the following:

$$\text{Buck converter,}\quad G=\frac{V_o}{V_{in}}=k$$

$$\text{Forward converter,}\quad G=\frac{V_o}{V_{in}}=kN \quad N \text{ is the transformer turns ratio}$$

$$\text{Cuk converter,}\quad G=\frac{V_o}{V_{in}}=\frac{k}{1-k}$$

$$\text{Flyback converter,}\quad G=\frac{V_o}{V_{in}}=\frac{k}{1-k}N \quad N \text{ is the transformer turns ratio} \tag{3.112}$$

$$\text{Boost converter,}\quad G=\frac{V_o}{V_{in}}=\frac{1}{1-k}$$

$$\text{Positive-output Luo-converters,}\quad G=\frac{V_o}{V_{in}}=\frac{n}{1-k}$$

If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in Table 3.1.

If the conduction duty k is 0.5, the output voltage transfer gains are listed in Table 3.2.

If the conduction duty k is 0.8, the output voltage transfer gains are listed in Table 3.3.

TABLE 3.1
Voltage Transfer Gains of Converters in the Condition $k = 0.2$

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Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter				0.2N (N is the transformer turns ratio)		
Cuk converter				0.25		
Flyback converter				0.25N (N is the transformer turns ratio)		
Boost converter				1.25		
Positive-output Luo-converters	1.25	2.5	3.75	5	6.25	1.25^n
Positive-output super-lift Luo-converters—main series	2.25	5.06	11.39	25.63	57.67	2.25^n
Positive-output super-lift Luo-converters—additional series	3.5	7.88	17.72	39.87	89.7	$3.5 * 2.25^{(n-1)}$
Positive-output super-lift Luo-converters—enhanced series	3.5	12.25	42.88	150	525	3.5^n
Positive-output super-lift Luo-converters—re-enhanced series	4.75	22.56	107.2	509	2418	4.75^n
Positive-output super-lift Luo-converters—multiple (j = 4)—enhanced series	7.25	52.56	381	2,762	20,030	7.25^n

TABLE 3.2
Voltage Transfer Gains of Converters in the Condition k = 0.5

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter				0.5N (N is the transformer turns ratio)		
Cuk converter				1		
Flyback converter				N (N is the transformer turns ratio)		
Boost converter				2		
Positive-output Luo-converters	2	4	6	8	10	2^n
Positive-output super-lift Luo-converters—main series	3	9	27	81	243	3^n
Positive-output super-lift Luo-converters—additional series	5	15	45	135	405	$5 * 3^{(n-1)}$
Positive-output super-lift Luo-converters—enhanced series	5	25	125	625	3125	5^n
Positive-output super-lift Luo-converters—re-enhanced series	7	49	343	2,401	16,807	7^n
Positive-output super-lift Luo-converters—multiple (j = 4)—enhanced series	11	121	1,331	14,641	$16 * 10^4$	11^n

TABLE 3.3
Voltage Transfer Gains of Converters in the Condition k = 0.8

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Stage No. (n)	1	2	3	4	5	n
Buck converter	0.8					
Forward converter	0.8N (N is the transformer turns ratio)					
Cuk converter	4					
Flyback converter	4N (N is the transformer turns ratio)					
Boost converter	5					
Positive-output Luo-converters	5	10	15	20	25	5^n
Positive-output super-lift Luo-converters—main series	6	36	216	1296	7776	6^n
Positive-output super-lift Luo-converters—additional series	11	66	396	2,376	14,256	$11 * 6^{(n-11)}$
Positive-output super-lift Luo-converters—enhanced series	11	121	1,331	14,641	$16 * 10^4$	11^n
Positive-output super-lift Luo-converters—re-enhanced series	16	256	4,096	65,536	$104 * 10^4$	16^n
Positive-output super-lift Luo-converters—multiple (j = 4)—enhanced series	26	676	17,576	$46 * 10^4$	$12 * 10^6$	26^n

3.8 Simulation Results

To verify the design and calculation results, the PSpice simulation package was applied to these converters. Choose V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all C_1–C_8 = 2 μF and R = 30 kΩ, and using k = 0.5 and f = 100 kHz.

3.8.1 Simulation Results of a Triple-Lift Circuit

The voltage values V_1, V_2, and V_o of a triple-lift circuit are 66, 194, and 659 V, respectively, and inductor current waveforms are i_{L_1} (its average value I_{L_1} = 618 mA) i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 3.17. The voltage values are matched to the calculated results.

3.8.2 Simulation Results of a Triple-Lift Additional Circuit

The voltage values V_1, V_2, V_3, and V_o of the triple-lift additional circuit are 57, 165, 538, and 910 V, respectively, and the current waveforms are (its average value I_{L_1} = 1.8 A), i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 3.18. The voltage values are matched to the calculated results.

3.9 Experimental Results

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A test rig was constructed to verify the design and calculation results and compared with PSpice simulation results. The testing conditions were the same: V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all $C_1 - C_8$ = 2 μF and R = 30 kΩ, and using k = 0.5 and f = 100 kHz.

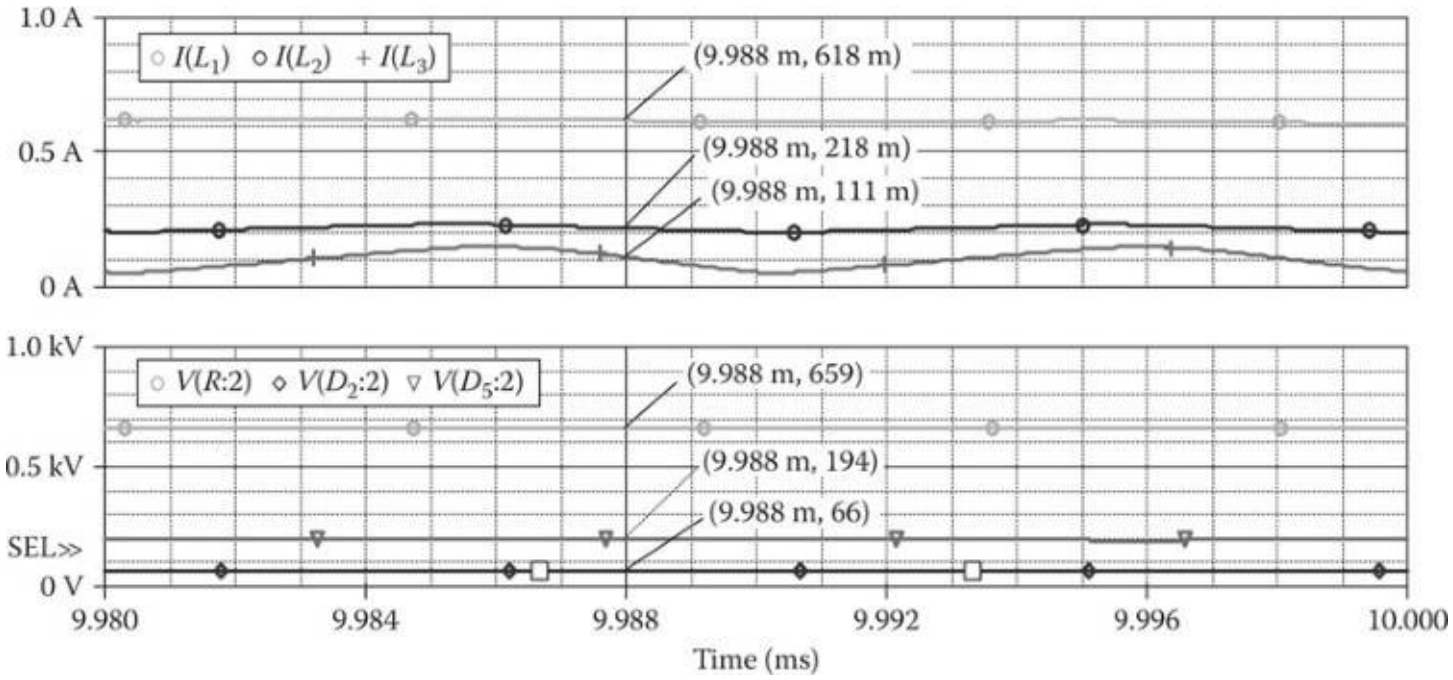


FIGURE 3.17
The simulation results of triple-lift circuit at condition K = 0.5 and F = 100 kHz.

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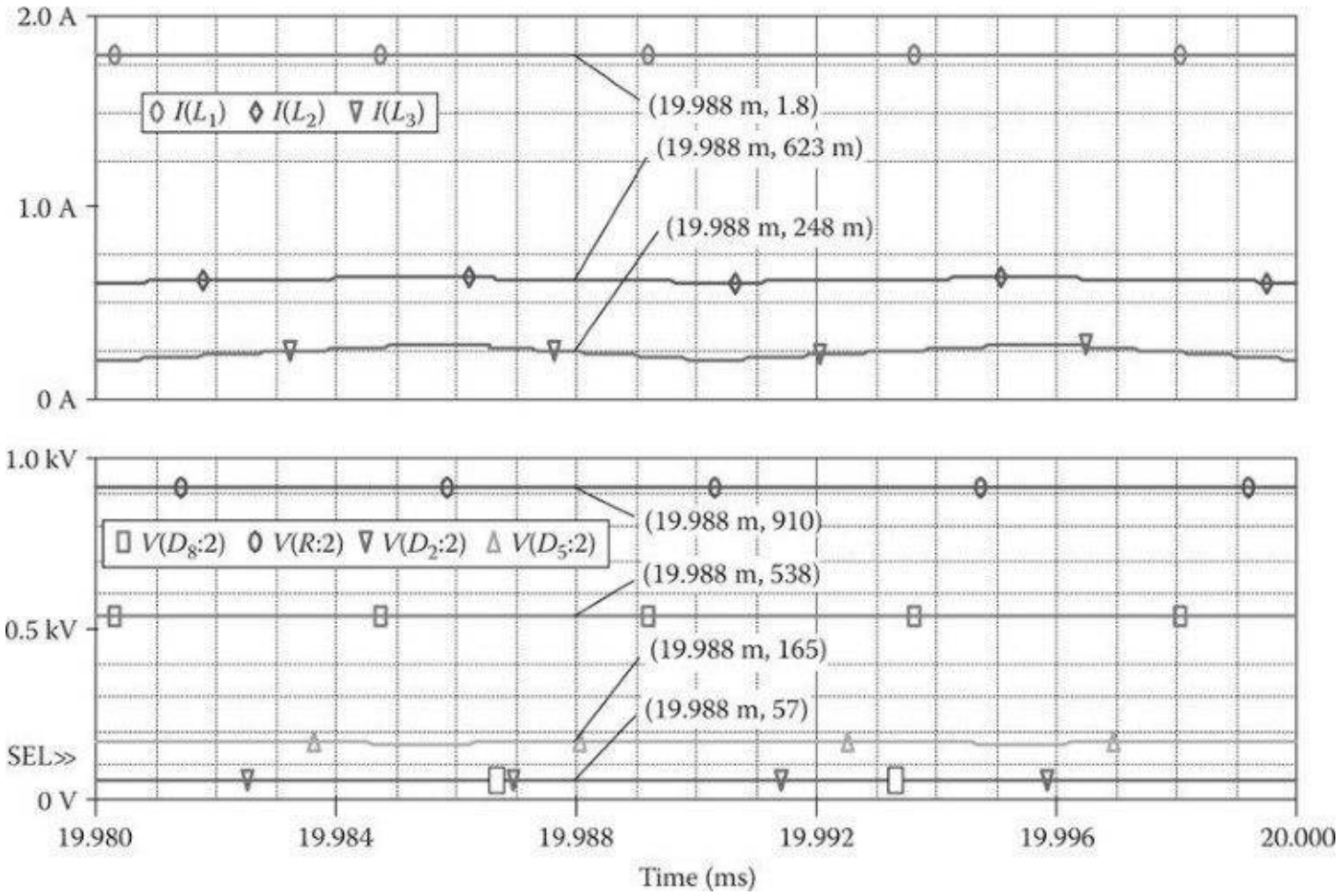


FIGURE 3.18
Simulation results of triple-lift additional circuit at condition $K = 0.5$ and $F = 100$ kHz.

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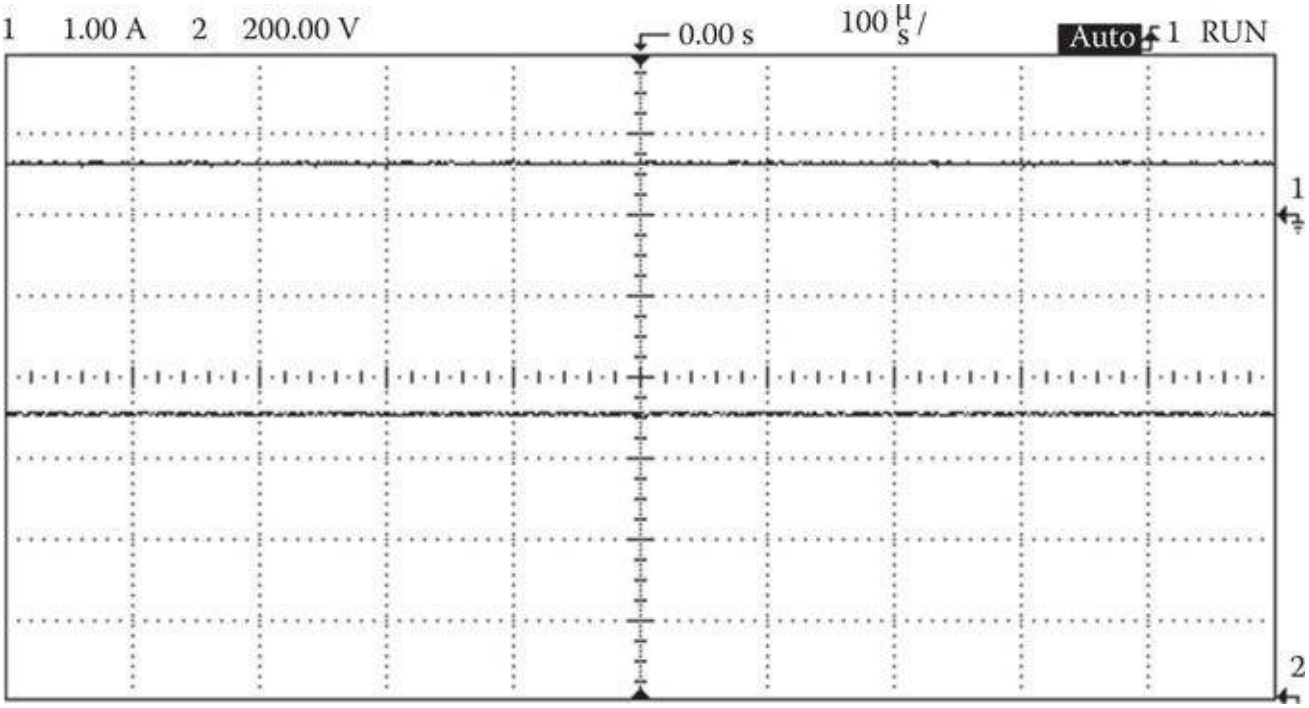


FIGURE 3.19
The experimental results of triple-lift circuit at condition $K = 0.5$ and $f = 100$ kHz.

The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. The values of the output voltage and first inductor current are measured in the following converters.

3.9.1 Experimental Results of a Triple-Lift Circuit

After careful measurement, the current value of $I_{L_1} = 0.62$ A (shown in Channel 1 with 1 A/Div) and voltage value of V_o = 660 V (shown in Channel 2 with 200 V/Div). The experimental results (current and voltage values) are shown in Figure 3.19, which are identically matched to the calculated and simulation results, which are $I_{L_1} = 0.618$ A and V_o = 659 V shown in Figure 3.17.

3.9.2 Experimental Results of a Triple-Lift Additional Circuit

The experimental results are the current value of $I_{L_1} = 1.8$ A (shown in Channel 1 with 1 A/Div) and voltage value of V_o = 910 V (shown in Channel 2 with 200 V/Div) are shown in Figure 3.20, which are identically matched to the calculated and simulation results, which are $I_{L_1} = 1.8$ A and V_o = 910 V shown in Figure 3.18.

3.9.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, but efficiency. Particularly, the efficiencies of the tested circuits are 51%–78%, which is good for high-voltage-output equipment. The simulation and experimental results are listed in Tables 3.4 and 3.5. They demonstrate that all results are well identified to each other.

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Usually, there is high inrush current during the initial power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick in only few milliseconds.

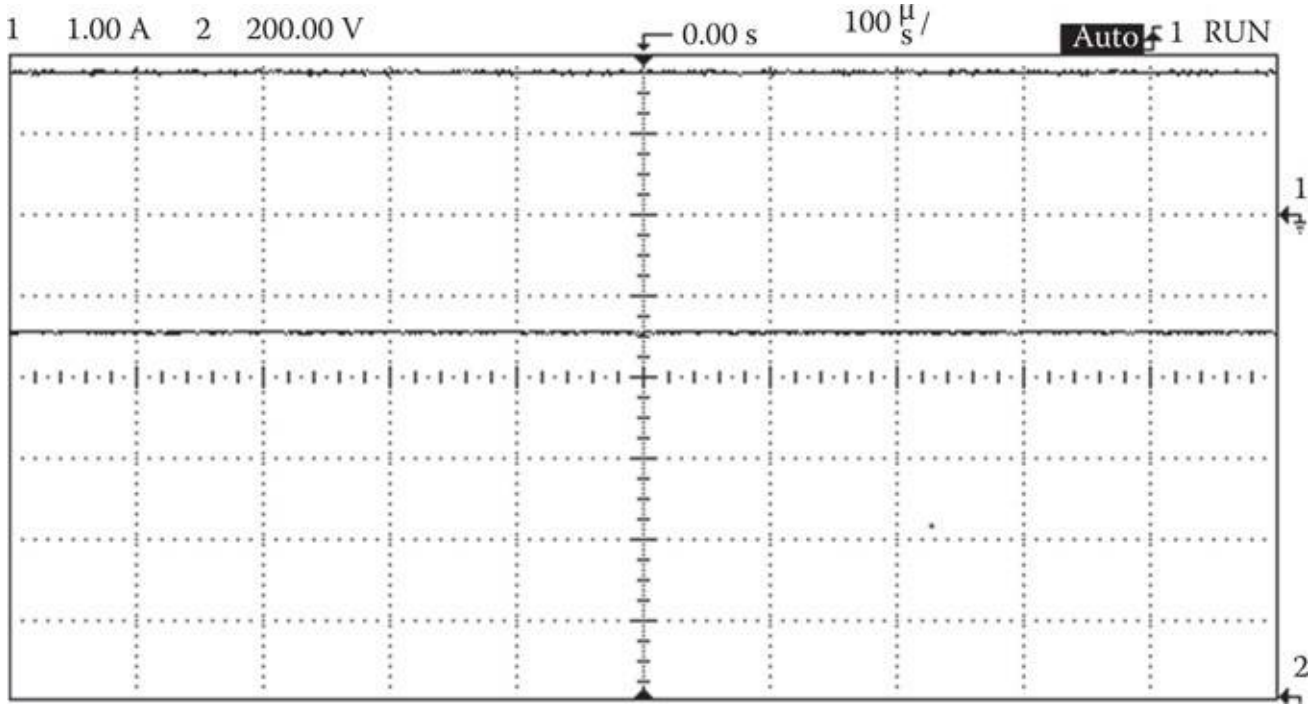


FIGURE 3.20
Experimental results of triple-lift additional circuit at condition $K = 0.5$ and $F = 100$ kHz.

TABLE 3.4
Comparison to Simulation and Experimental Results of a Triple-Lift Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_o (V)	P_o (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

TABLE 3.5
Comparison to Simulation and Experimental Results of a Triple-Lift Additional Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_o (V)	P_o (W)	η (%)
Simulation results	1.8	2.7	20	54	910	27.6	51
Experimental results	1.8	2.7	20	54	910	27.6	51

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4

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Negative-Output Super-Lift Luo-Converters

Along with the positive-output super-lift Luo-converters, negative-output super-lift Luo-converters have also been developed. They perform super-lift technique as well.

4.1 Introduction

Negative-output (N/O) super-lift Luo-converters are sorted into several subseries:

- Main series: Each circuit of the main series has one switch *S*, *n* inductors, *2n* capacitors, and (3n − 1) diodes.
- Additional series: Each circuit of the additional series has one switch *S*, *n* inductors, 2(*n* + 1) capacitors, and (3*n* + 1) diodes.
- Enhanced series: Each circuit of the enhanced series has one switch *S*, *n* inductors, 4n capacitors, and (5*n* + 1) diodes.
- Re-enhanced series: Each circuit of the re-enhanced series has one switch *S*, *n* inductors, 6*n* capacitors, and (7*n* + 1) diodes.
- Multiple-enhanced series: Each circuit of the multiple-enhanced series has one switch *S*, *n* inductors, 2(*n* + *j* + 1) capacitors, and (3*n* + 2*j* + 1) diodes.

All analyses in this section are based on the condition of steady-state operation with continuous conduction mode (CCM).

The conduction duty ratio is *k*, the switch period is $T = 1/f$ (where f is the switch frequency), and the load is resistive load *R*. The input voltage and current are V_{in} and I_{in}, and the output voltage and current are V_o and I_o. Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_o \times I_o$. The voltage transfer gain is *G*: $G = V_o/V_{in}$.

4.2 Main Series

The first three stages of the main series of N/O super-lift Luo-converters are shown in Figures 4.1, 4.2 and 4.3. For convenience to explain, they are called elementary circuit, relift circuit, and triple-lift circuit, respectively, and numbered as $n = 1$, 2, and 3.

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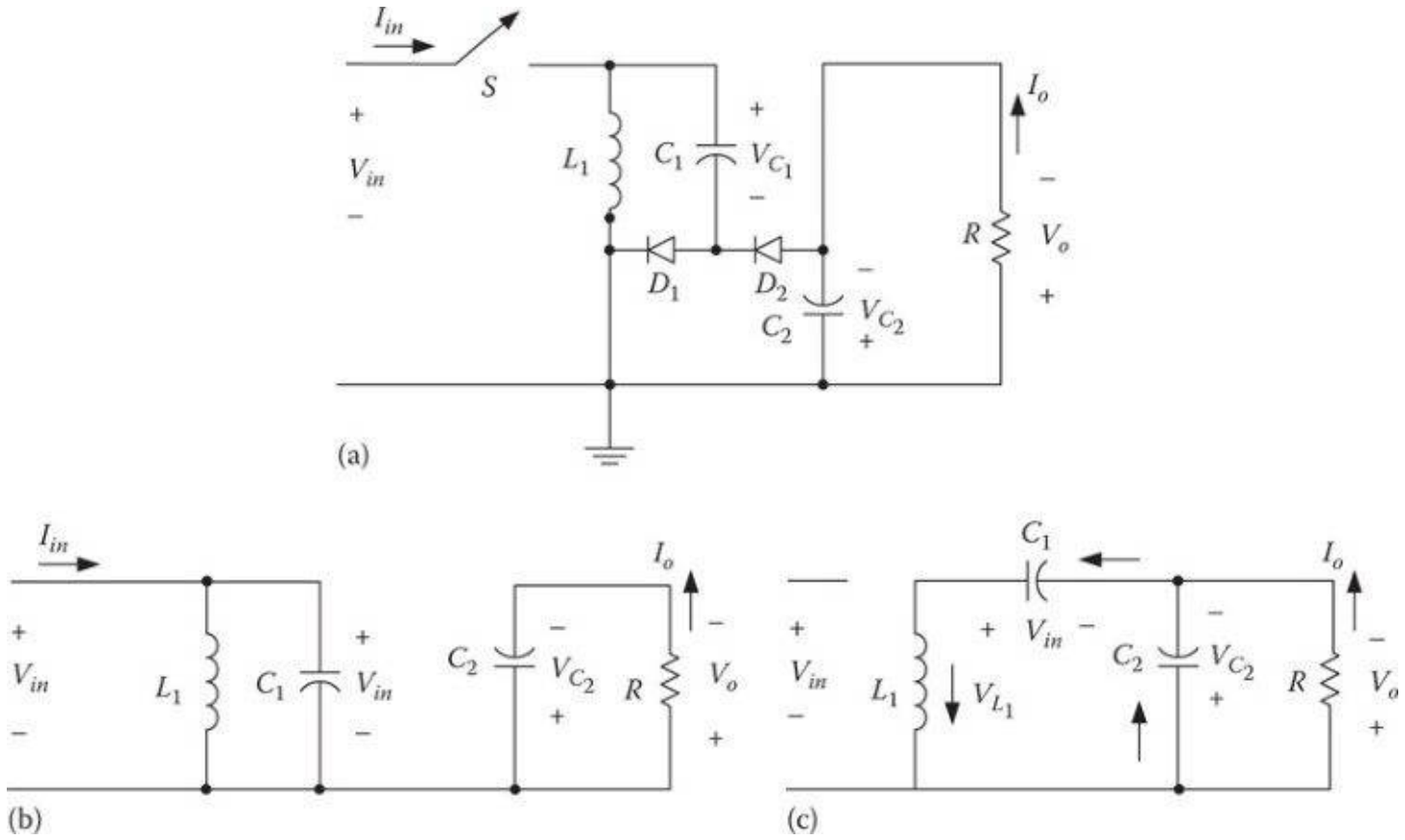


FIGURE 4.1
Negative-output elementary circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

4.2.1 Elementary Circuit

N/O elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 4.1.

The voltage across capacitor C_1 is charged to V_{in}. The current flowing through inductor L_1 increases with slope V_{in}/L_1 during switch-on period kT and decreases with slope $-(V_o - V_{in})/L_1$ during switch-off $(1 - k)T$. Therefore, the variation of current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_o - V_{in}}{L_1}(1-k)T \tag{4.1}$$

$$V_o = \frac{1}{1-k} V_{in} = \left(\frac{2-k}{1-k} - 1\right) V_{in} \tag{4.2}$$

The voltage transfer gain is

$$G_1 = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} - 1 \tag{4.3}$$

In steady state, the average charge across capacitor C_1 in a period should be zero. The relations are available:

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$$kTi_{C_1\text{-}on} = (1-k)Ti_{C_1\text{-}off} \quad \text{and} \quad i_{C_1\text{-}on} = \frac{1-k}{k} i_{C_1\text{-}off}$$

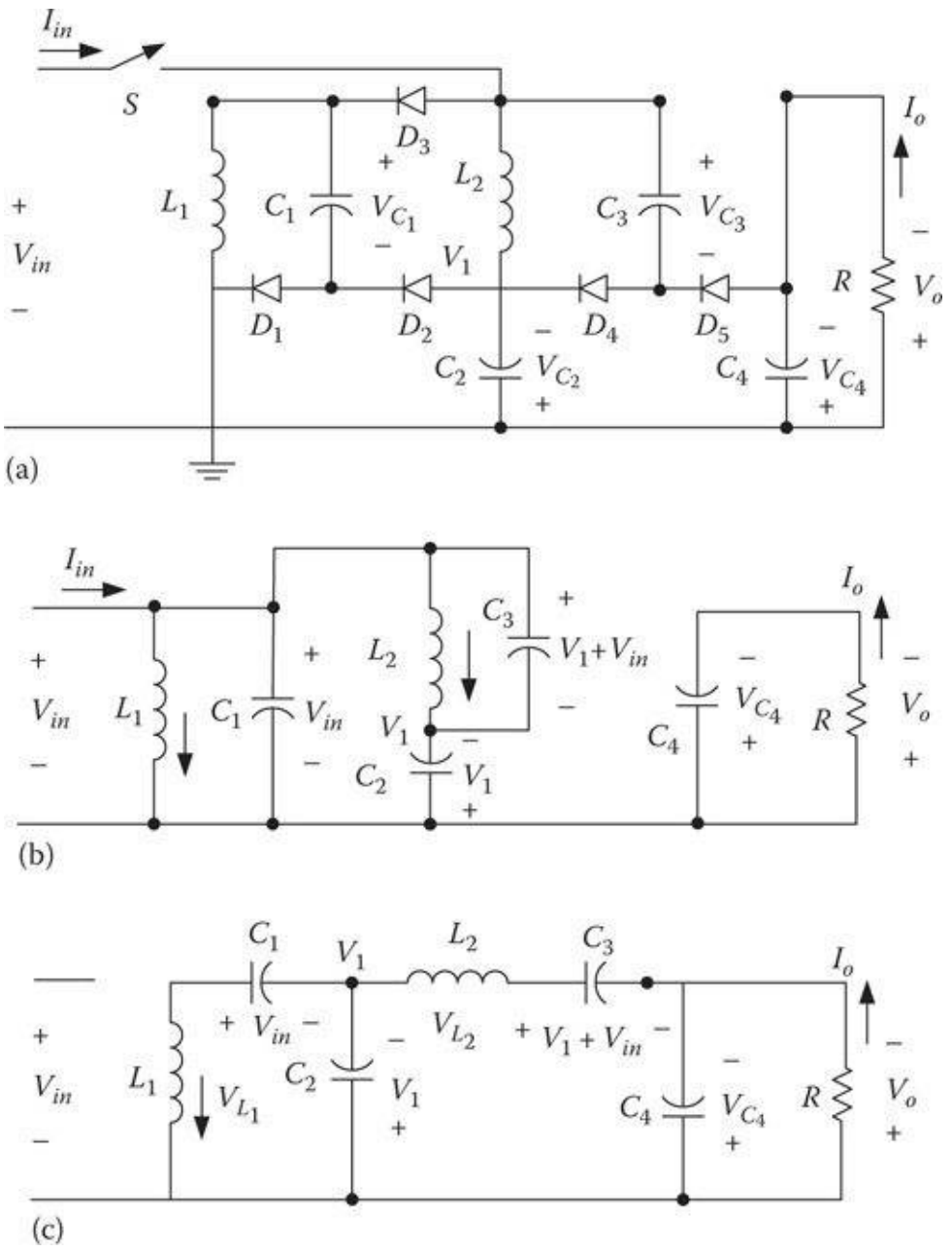


FIGURE 4.2
Negative-output re-lift circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

This relation is available for all capacitor's current in switch-on and switch-off periods. The input current i_{in} is equal to (i_{L_1}+ i_{C_1}) during switch-on and zero during switch-off. Capacitor current i_{C_1} is equal to i_{L_1} during switch-off.

$$i_{in\text{-}on} = i_{L_1\text{-}on} + i_{C_1\text{-}on} \quad i_{L_1\text{-}off} = i_{C_1\text{-}off} = I_{L_1}$$

If inductance L_1 is large enough, i_{L_1} is nearly equal to its average current I_{L_1}.

Therefore,

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$$i_{in-on} = i_{L_1-on} + i_{C_1-on} = i_{L_1-on} + \frac{1-k}{k} i_{C_1-off} = \left(1 + \frac{1-k}{k}\right) I_{L_1} = \frac{1}{k} I_{L_1}$$

and

$$I_{in} = k i_{in-on} = I_{L_1} \tag{4.4}$$

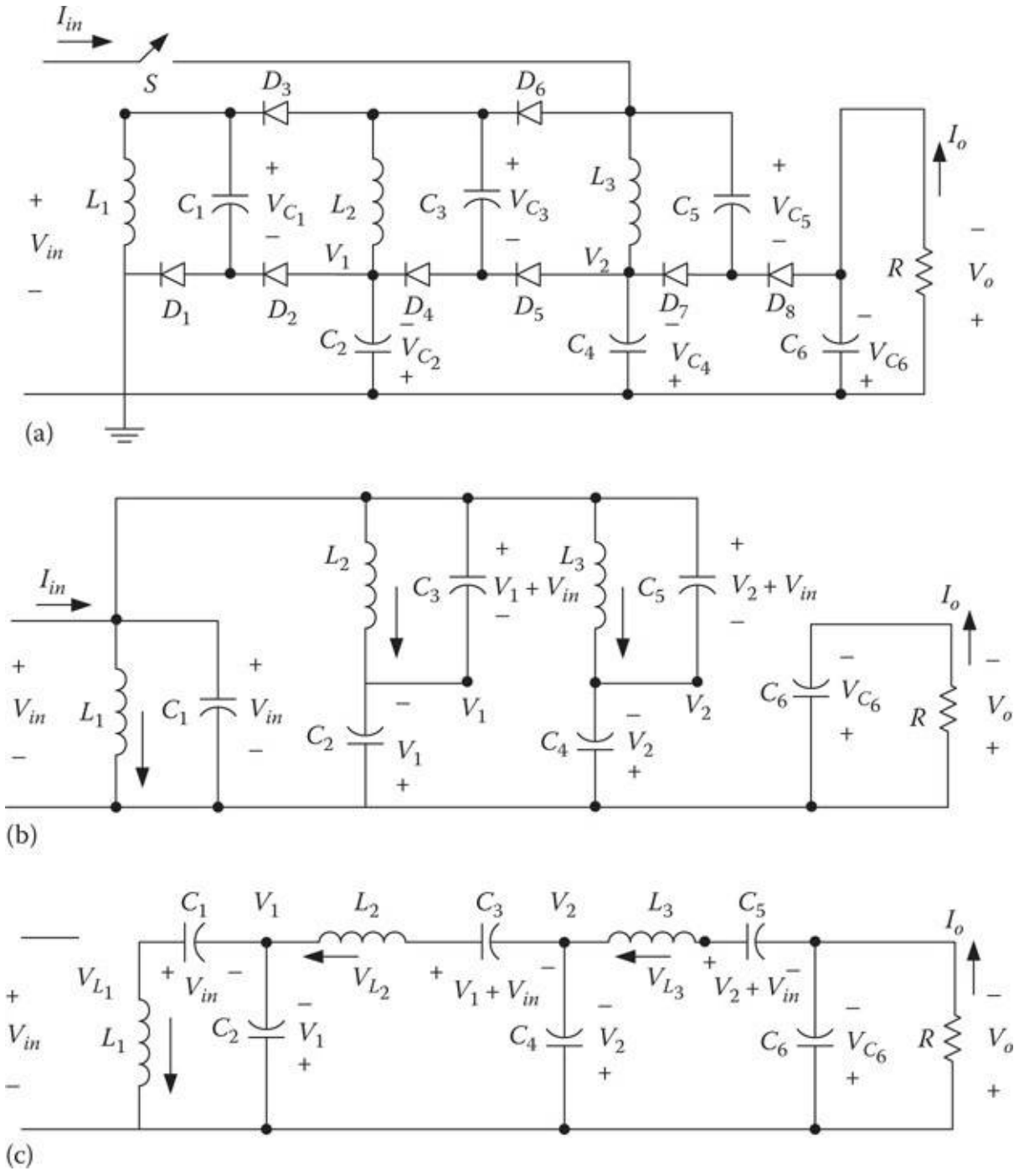


FIGURE 4.3
Negative-output triple-lift circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Further,

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$$i_{C_2-on} = I_o \quad i_{C_2-off} = \frac{k}{1-k} I_o$$

$$I_{L_1} = i_{C_2-off} + I_o = \frac{k}{1-k} i_{C_2-on} + I_o = \frac{1}{1-k} I_o$$

The variation ratio of inductor current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{2L_1 I_o} = \frac{k(1-k)}{G_1} \frac{R}{2fL_1} \tag{4.5}$$

Usually, ξ_1 is small (much lower than unity), it means this converter works in the CCM.

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_2} = kT \frac{I_o}{C_2} = \frac{k}{fC_2} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_2} \tag{4.6}$$

Usually, R is in kΩ, f in 10 kHz, and C_2 in μF; this ripple is very small.

4.2.2 N/O Re-Lift Circuit

N/O re-lift circuit is derived from N/O elementary circuit by adding the parts (L_2–D_3–D_4–D_5–C_3–C_4**).** Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.2.

The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage V_1 across capacitor C_2 is $V_1 = (1/(1 - k))V_{in}$.

The voltage across capacitor C_3 is charged to $(V_1 + V_{in})$. The current flowing through inductor L_2 increases with slope $(V_1 + V_{in})/L_2$ during switch-on period kT and decreases with slope $-(V_o - 2V_1 - V_{in})/L_2$ during switch-off $(1 - k)$T. Therefore, the variation of current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{V_o - 2V_1 - V_{in}}{L_2} (1-k)T \tag{4.7}$$

$$V_o = \frac{(2-k)V_1 + V_{in}}{1-k} = \left[\left(\frac{2-k}{1-k} \right)^2 - 1 \right] V_{in} \tag{4.8}$$

The voltage transfer gain is

$$G_2 = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k} \right)^2 - 1 \tag{4.9}$$

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The input current i_{in} is equal to ($i_{L_1} + i_{C_1} + i_{L_2} + i_{C_3}$) during switch-on and zero during switch-off. In steady state, the following relations are available:

$$i_{in-on} = i_{L_1-on} + i_{C_1-on} + i_{L_2-on} + i_{C_3-on}$$

$$i_{C_4-on} = I_o \qquad i_{C_4-off} = \frac{k}{1-k} I_o$$

$$i_{C_3-off} = I_{L_2} = I_o + i_{C_4-off} = \frac{I_o}{1-k} \qquad i_{C_3-on} = \frac{I_o}{k}$$

$$i_{C_2-on} = I_{L_2} + i_{C_3-on} = \frac{I_o}{1-k} + \frac{I_o}{k} = \frac{I_o}{k(1-k)} \qquad i_{C_2-off} = \frac{I_o}{(1-k)^2}$$

$$i_{C_1-off} = I_{L_1} = I_{L_2} + i_{C_2-off} = \frac{I_o}{1-k} + \frac{I_o}{(1-k)^2} = \frac{2-k}{(1-k)^2} I_o \qquad i_{C_1-on} = \frac{2-k}{k(1-k)} I_o$$

Thus,

$$i_{in-on} = i_{L_1-on} + i_{C_1-on} + i_{L_2-on} + i_{C_3-on} = \frac{1}{k}(I_{L_1} + I_{L_2}) = \frac{3-2k}{k(1-k)^2} I_o$$

Therefore,

$$I_{in} = k i_{in-on} = \frac{3-2k}{(1-k)^2} I_o$$

Since

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \qquad I_{L_1} = \frac{2-k}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{1-k} \frac{kT}{L_2} V_{in} \qquad I_{L_2} = \frac{1}{1-k} I_o$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_{in}}{((2-k)/(1-k)^2)2L_1 I_o} = \frac{k(1-k)^2}{(2-k)G_2} \frac{R}{2fL_1} \tag{4.10}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(2-k)TV_{in}}{2L_2 I_o} = \frac{k(2-k)}{G_2} \frac{R}{2fL_2} \tag{4.11}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_4} = kT \frac{I_o}{C_4} = \frac{k}{fC_4} \frac{V_o}{R}$$

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Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_4} \tag{4.12}$$

4.2.3 N/O Triple-Lift Circuit

N/O triple-lift circuit is derived from N/O re-lift circuit by double adding the parts (L_2–D_3–D_4–D_5–C_3–C_4). Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 4.3.

The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage V_1 across capacitor C_2 is

$$V_1 = \left(\frac{2-k}{1-k} - 1\right) V_{in} = \frac{1}{1-k} V_{in}$$

and the voltage V_2 across capacitor C_4 is

$$V_2 = \left[\left(\frac{2-k}{1-k}\right)^2 - 1\right] V_{in} = \frac{3-2k}{(1-k)^2} V_{in}$$

The voltage across capacitor C_5 is charged to (V_2 + V_{in}). The current flowing through inductor L_3 increases with slope (V_2 + V_{in})/L_3 during switch-on period kT and decreases with slope -(V_o− 2V_2 − V_{in})/L_3 during switch-off period (1 − k)T. Therefore, the variation of current i_{L_3} is

$$\Delta i_{L_3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{V_o - 2V_2 - V_{in}}{L_3} (1-k)T \tag{4.13}$$

$$V_o = \frac{(2-k)V_2 + V_{in}}{1-k} = \left[\left(\frac{2-k}{1-k}\right)^3 - 1\right] V_{in} \tag{4.14}$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^3 - 1 \tag{4.15}$$

The input current i_{in} is equal to ($i_{L_1} + i_{C_1} + i_{L_2} + i_{C_3} + i_{L_3} + i_{C_5}$) during switch-on and zero during switch-off. In steady state, the following relations are available:

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$$i_{in-on} = i_{L_1-on} + i_{C_1-on} + i_{L_2-on} + i_{C_3-on} + i_{L_3-on} + i_{C_5-on}$$

$$i_{C_6-on} = I_o \qquad i_{C_6-off} = \frac{k}{1-k} I_o$$

$$i_{C_5-off} = I_{L_3} = I_o + i_{C_6-off} = \frac{I_o}{1-k} \qquad i_{C_5-on} = \frac{I_o}{k}$$

$$i_{C_4-on} = I_{L_3} + i_{C_5-on} = \frac{I_o}{1-k} + \frac{I_o}{k} = \frac{I_o}{k(1-k)} \qquad i_{C_4-off} = \frac{I_o}{(1-k)^2}$$

$$i_{C_3-off} = I_{L_2} = I_{L_3} + i_{C_4-off} = \frac{2-k}{(1-k)^2} I_o \qquad i_{C_3-on} = \frac{2-k}{k(1-k)} I_o$$

$$i_{C_2-on} = I_{L_2} + i_{C_3-on} = \frac{2-k}{k(1-k)^2} I_o \qquad i_{C_2-off} = \frac{2-k}{(1-k)^3} I_o$$

$$i_{C_1-off} = I_{L_1} = I_{L_2} + i_{C_2-off} = \frac{(2-k)^2}{(1-k)^3} I_o \qquad i_{C_1-on} = \frac{(2-k)^2}{k(1-k)^2} I_o$$

Thus,

$$i_{in-on} = i_{L_1-on} + i_{C_1-on} + i_{L_2-on} + i_{C_3-on} + i_{L_3-on} + i_{C_5-on} = \frac{1}{k}(I_{L_1} + I_{L_2} + I_{L_3}) = \frac{7-9k+3k^2}{k(1-k)^3} I_o$$

Therefore,

$$I_{in} = k i_{in-on} = \frac{7-9k+3k^2}{(1-k)^3} I_o = \left[\left(\frac{2-k}{1-k}\right)^3 - 1\right] I_o$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \qquad I_{L_1} = \frac{(2-k)^2}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in} \qquad I_{L_2} = \frac{2-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2 + V_{in}}{L_3} kT = \left(\frac{2-k}{1-k}\right)^2 \frac{kT}{L_3} V_{in} \qquad I_{L_3} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)^2 L_1 I_o} = \frac{k(1-k)^3}{(2-k)^2 G_3} \frac{R}{2fL_1} \tag{4.16}$$

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The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_{in}}{2L_2 I_o} = \frac{k(1-k)}{G_3}\frac{R}{2fL_2} \tag{4.17}$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(2-k)^2 TV_{in}}{2(1-k)L_3 I_o} = \frac{k(2-k)^2}{(1-k)G_3}\frac{R}{2fL_3} \tag{4.18}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_6} = kT\frac{I_o}{C_6} = \frac{k}{fC_6}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_6} \tag{4.19}$$

4.2.4 N/O Higher-Order Lift Circuit

N/O higher-order lift circuits can be designed by repeating the parts (L_2–D_3–D_4–D_5–C_3–C_4) multiple times. For nth-order lift circuit, the final output voltage across capacitor C_{2n} is

$$V_o = \left[\left(\frac{2-k}{1-k}\right)^n - 1\right]V_{in} \tag{4.20}$$

The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k}\right)^n - 1 \tag{4.21}$$

The variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^n}{(2-k)^{(n-1)}G_n}\frac{R}{2fL_i} \tag{4.22}$$

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(2-k)^{(3-n)}}{(1-k)^{(n-3)}G_n}\frac{R}{2fL_i} \tag{4.23}$$

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(2-k)^{(n-i+2)}}{(1-k)^{(n-i+1)}G_n}\frac{R}{2fL_3} \tag{4.24}$$

The variation ratio of output voltage v_o is

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$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{2n}} \tag{4.25}$$

4.3 Additional Series

All circuits of the additional series of N/O super-lift Luo-converters are derived from the corresponding circuits of the main series by adding a double/enhanced circuit (DEC). The first three stages of this series are shown in Figures 4.4, 4.5 and 4.6. For convenience, they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit, respectively, and numbered as n = 1, 2, and 3.

4.3.1 N/O Elementary Additional Circuit

This circuit is derived from the N/O elementary circuit by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 4.4.

The voltage across capacitor C_1 is charged to V_{in}. The voltage across capacitor C_2 is charged to V_1, and C_{11} is charged to (V_1 + V_{in}). The current i_{L_1} flowing through inductor L_1 increases with slope V_{in}/L_1 during switch-on period kT and decreases with slope -(V_1 − V_{in})/L_1 during switch-off period (1 − k)T.

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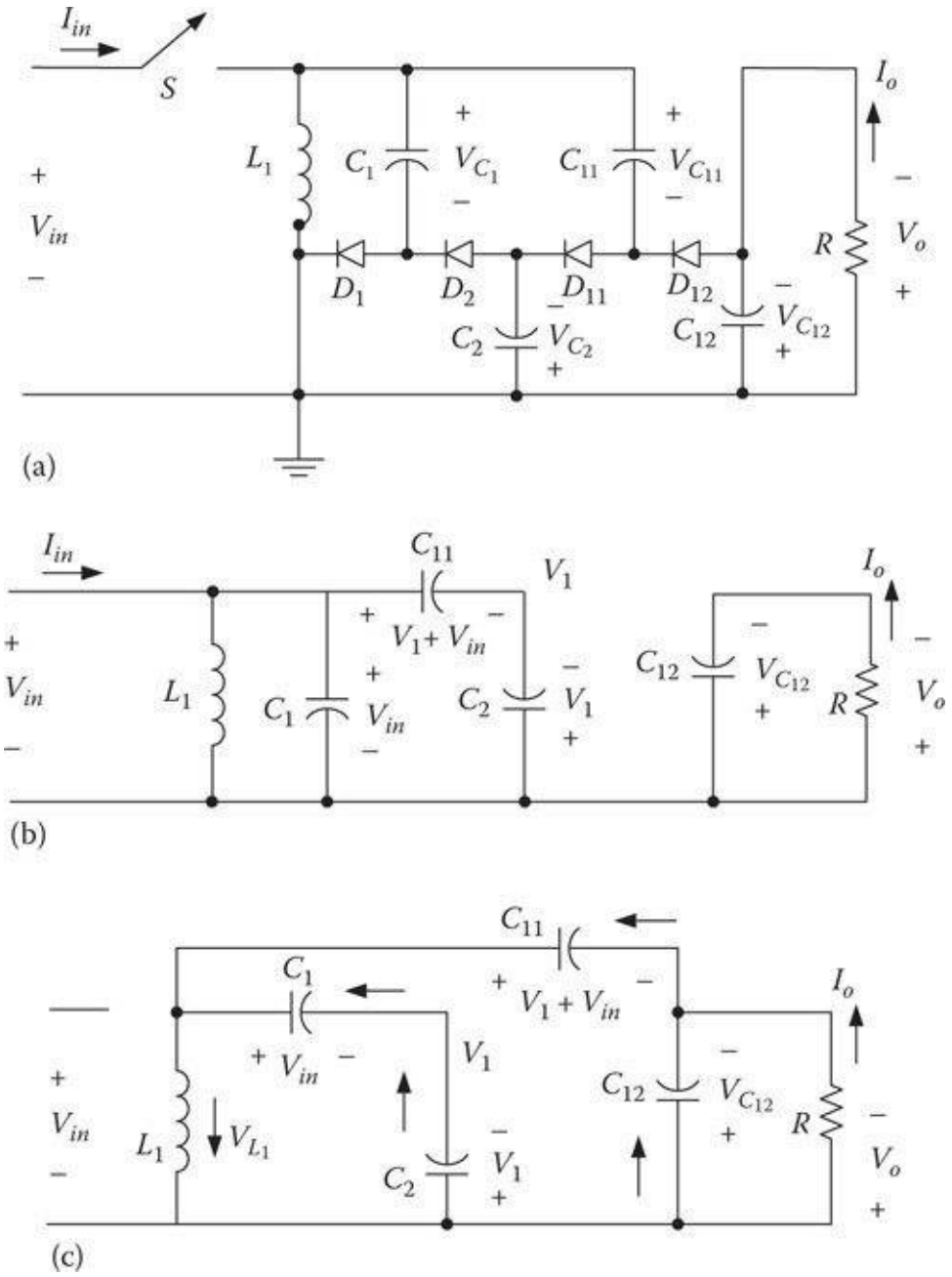


FIGURE 4.4
Negative-output elementary additional (enhanced) circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Therefore,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1}(1-k)T \tag{4.26}$$

$$V_1 = \frac{1}{1-k} V_{in} = \left(\frac{2-k}{1-k} - 1 \right) V_{in}$$

$$V_{L_1-off} = \frac{k}{1-k} V_{in}$$

The output voltage is

$$V_o = V_{in} + V_{L_1} + V_1 = \frac{2}{1-k} V_{in} = \left[\frac{3-k}{1-k} - 1 \right] V_{in} \tag{4.27}$$

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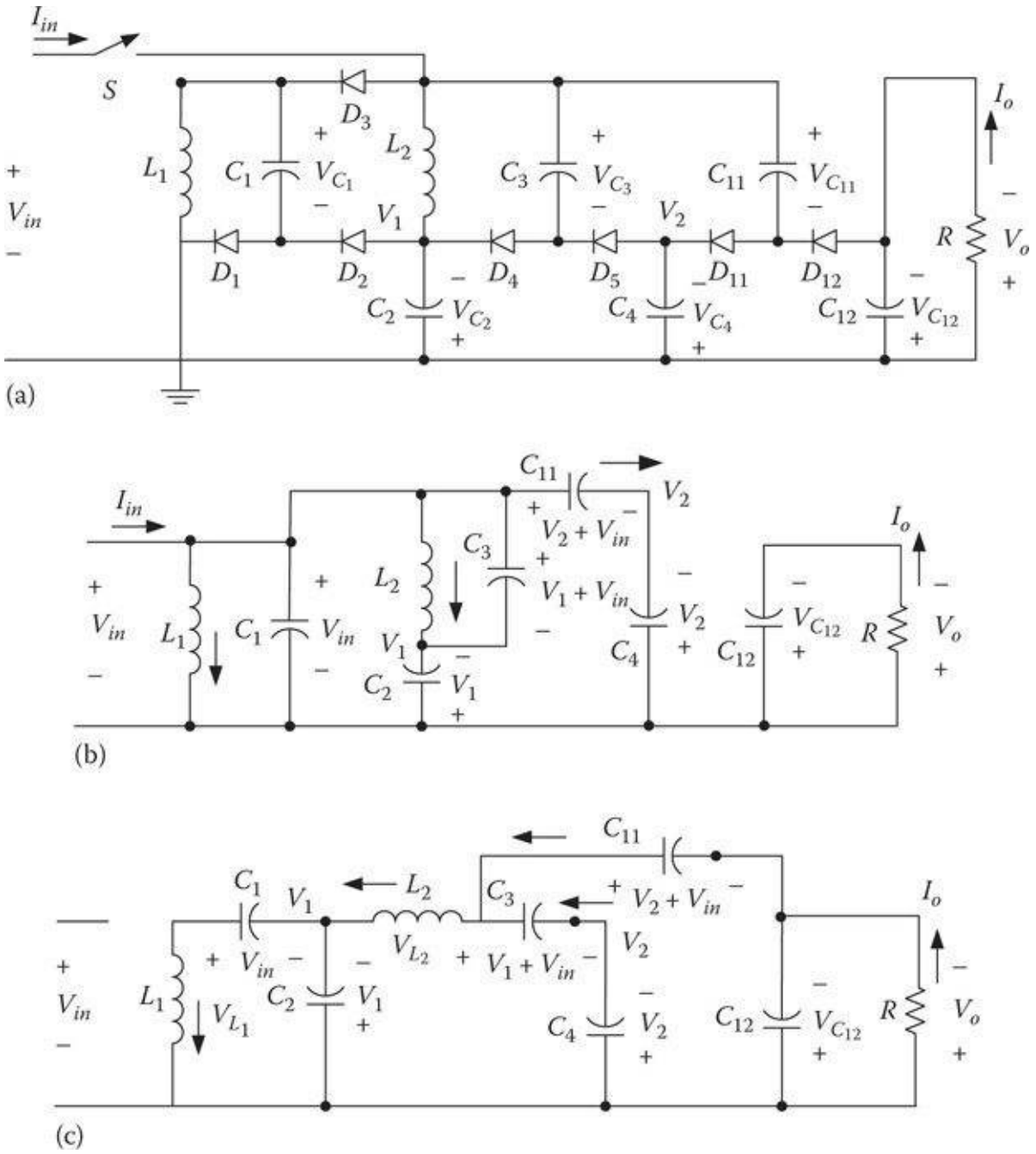


FIGURE 4.5
Negative-output re-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G_1 = \frac{V_o}{V_{in}} = \frac{3-k}{1-k} - 1 \tag{4.28}$$

The following relations are obtained:

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$$i_{C12-on} = I_o \qquad i_{C12-off} = \frac{kI_o}{1-k}$$

$$i_{C11-off} = I_o + i_{C12-off} = \frac{I_o}{1-k} \qquad i_{C11-on} = i_{C2-on} = \frac{I_o}{k}$$

$$i_{C2-off} = i_{C1-off} = \frac{I_o}{1-k} \qquad i_{C1-on} = \frac{I_o}{k}$$

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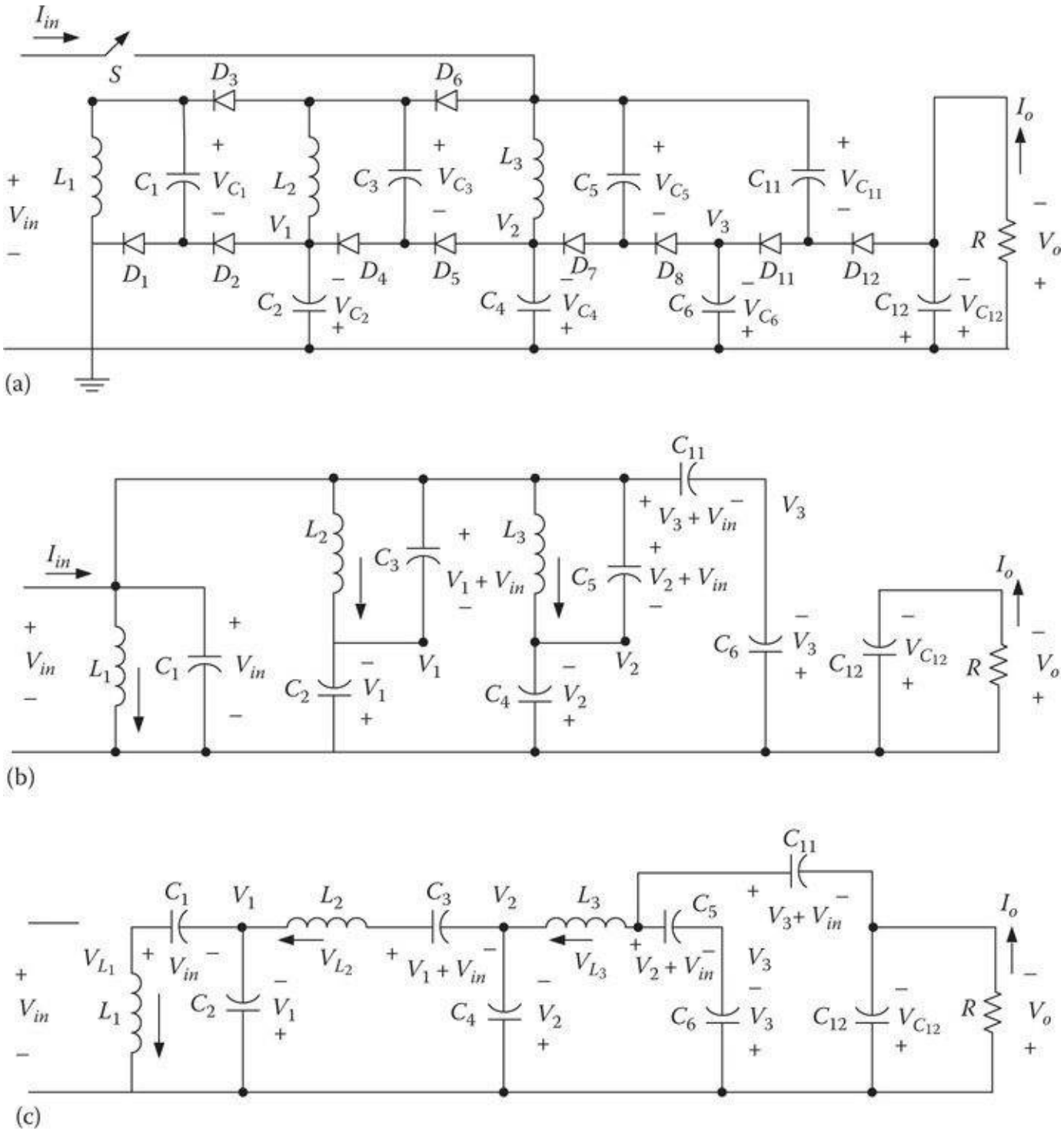


FIGURE 4.6
Negative-output triple-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$I_{L_1} = i_{C_1\text{-}off} + i_{C_{11}\text{-}on} = \frac{2I_o}{1-k}$$

$$i_{in} = I_{L_1} + i_{C_1\text{-}on} + i_{C_{11}\text{-}on} = \left(\frac{2}{1-k} + \frac{1}{k} + \frac{1}{k}\right) I_o = \frac{2}{k(1-k)} I_o$$

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Therefore,

$$I_{in} = ki_{in} = \frac{2}{1-k} I_o = \left[\frac{3-k}{1-k} - 1\right] I_o$$

The variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)}{2G_1} \frac{R}{2fL_1} \tag{4.29}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT \frac{I_o}{C_{12}} = \frac{k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{4.30}$$

4.3.2 N/O Re-Lift Additional Circuit

The N/O re-lift additional circuit is derived from the N/O re-lift circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.5.

The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage across C_2 is $V_1 = (1/(1-k))V_{in}$.

The voltage across capacitor C_3 is charged to $(V_1 + V_{in})$, the voltage across capacitor C_4 is charged to V_2, and the voltage across capacitor C_{11} is charged to $(V_2 + V_{in})$. The current flowing through inductor L_2 increases with voltage $(V_1 + V_{in})$ during switch-on kT and decreases with voltage $-(V_2 - 2V_1 - V_{in})$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{V_2 - 2V_1 - V_{in}}{L_2} (1-k)T \tag{4.31}$$

$$V_2 = \frac{(2-k)V_1 + V_{in}}{1-k} = \frac{3-2k}{(1-k)^2} = \left[\left(\frac{2-k}{1-k}\right)^2 - 1\right] V_{in}$$

and

$$V_{L_2-off} = V_2 - 2V_1 - V_{in} = \frac{k(2-k)}{(1-k)^2} V_{in} \tag{4.32}$$

The output voltage is

$$V_o = V_2 + V_{in} + V_{L_2} + V_1 = \frac{5-3k}{(1-k)^2} V_{in} = \left[\frac{3-k}{1-k}\frac{2-k}{1-k} - 1\right] V_{in} \tag{4.33}$$

The voltage transfer gain is

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$$G_2 = \frac{V_o}{V_{in}} = \frac{2-k}{1-k}\frac{3-k}{1-k} - 1 \tag{4.34}$$

The following relations are obtained:

$$i_{C12-on} = I_o \qquad i_{C12-off} = \frac{kI_o}{1-k}$$

$$i_{C11-off} = I_o + i_{C12-off} = \frac{I_o}{1-k} \qquad i_{C11-on} = i_{C4-on} = \frac{I_o}{k}$$

$$i_{C4-off} = i_{C3-off} = \frac{I_o}{1-k} \qquad i_{C3-on} = \frac{I_o}{k}$$

$$I_{L2} = i_{C11-off} + i_{C3-off} = \frac{2I_o}{1-k}$$

$$i_{C2-on} = I_{L2} + i_{C3-on} = \frac{1+k}{k(1-k)}I_o \qquad i_{C2-off} = \frac{1+k}{(1-k)^2}I_o$$

$$I_{L1} = i_{C1-off} = I_{L2} + i_{C2-off} = \frac{3-k}{(1-k)^2}I_o \qquad i_{C1-on} = \frac{3-k}{k(1-k)}I_o$$

$$i_{in} = I_{L1} + i_{C1-on} + i_{C2-on} + i_{C4-on} = \left[\frac{3-k}{(1-k)^2} + \frac{3-k}{k(1-k)} + \frac{1+k}{k(1-k)} + \frac{1}{k}\right]I_o = \frac{5-3k}{k(1-k)^2}I_o$$

Therefore,

$$I_{in} = ki_{in} = \frac{5-3k}{(1-k)^2}I_o = \left[\frac{3-k}{1-k}\frac{2-k}{1-k} - 1\right]I_o$$

Analogously,

$$\Delta i_{L1} = \frac{V_{in}}{L_2}kT \qquad I_{L1} = \frac{3-k}{(1-k)^2}I_o$$

$$\Delta i_{L2} = \frac{V_1 + V_{in}}{L_2}kT = \frac{2-k}{(1-k)L_2}kTV_{in} \qquad I_{L2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{k(1-k)^2TV_{in}}{2(3-k)L_1I_o} = \frac{k(1-k)^2}{(3-k)G_2}\frac{R}{2fL_1} \tag{4.35}$$

The variation ratio of current i_{L2} through inductor L_2 is

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$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(2-k)TV_{in}}{4L_2I_o} = \frac{k(2-k)}{2G_2}\frac{R}{2fL_2} \tag{4.36}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{4.37}$$

4.3.3 N/O Triple-Lift Additional Circuit

This circuit is derived from N/O triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.6.

The voltage across capacitor C_1 is charged to V_{in}. As described in the previous section, the voltage across C_2 is

$$V_1 = \frac{1}{1-k}V_{in}$$

and the voltage across C_4 is

$$V_2 = \frac{3-2k}{1-k}V_1 = \frac{3-2k}{(1-k)^2}V_{in}$$

The voltage across capacitor C_5 is charged to $(V_2 + V_{in})$, the voltage across capacitor C_6 is charged to V_3, and the voltage across capacitor C_{11} is charged to $(V_3 + V_{in})$. The current flowing through inductor L_3 increases with voltage $(V_2 + V_{in})$ during switch-on period kT and decreases with voltage $-(V_3 - 2V_2 - V_{in})$ during switch-off $(1 - k)$T. Therefore,

$$\Delta i_{L_3} = \frac{V_2 + V_{in}}{L_3}kT = \frac{V_3 - 2V_2 - V_{in}}{L_3}(1-k)T \tag{4.38}$$

$$V_3 = \frac{(2-k)V_2 + V_{in}}{1-k} = \frac{7-9k+3k^2}{(1-k)^3}V_{in} = \left[\left(\frac{2-k}{1-k}\right)^3 - 1\right]V_{in}$$

and

$$V_{L_3-off} = V_3 - 2V_2 - V_{in} = \frac{k(2-k)^2}{(1-k)^3}V_{in} \tag{4.39}$$

The output voltage is

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$$V_o = V_3 + V_{in} + V_{L_3} + V_2 = \frac{11-13k+4k^2}{(1-k)^3} V_{in} = \left[\frac{3-k}{1-k} \left(\frac{2-k}{1-k} \right)^2 - 1 \right] V_{in} \tag{4.40}$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{2-k}{1-k} \right)^2 \frac{3-k}{1-k} - 1 \tag{4.41}$$

The following relations are available:

$$i_{C_{12}-on} = I_o \qquad i_{C_{12}-off} = \frac{kI_o}{1-k}$$

$$i_{C_{11}-off} = I_o + i_{C_{12}-off} = \frac{I_o}{1-k} \qquad i_{C_{11}-on} = i_{C_6-on} = \frac{I_o}{k}$$

$$i_{C_6-off} = i_{C_5-off} = \frac{I_o}{1-k} \qquad i_{C_5-on} = \frac{I_o}{k}$$

$$I_{L_3} = i_{C_{11}-off} + i_{C_5-off} = \frac{2I_o}{1-k}$$

$$i_{C_4-on} = I_{L_3} + i_{C_5-on} = \frac{1+k}{k(1-k)} I_o \qquad i_{C_4-off} = \frac{1+k}{(1-k)^2} I_o$$

$$I_{L_2} = i_{C_3-off} = I_{L_3} + i_{C_4-off} = \frac{3-k}{(1-k)^2} I_o \qquad i_{C_3-on} = \frac{3-k}{k(1-k)} I_o$$

$$i_{C_2-on} = I_{L_2} + i_{C_3-on} = \frac{3-k}{k(1-k)^2} I_o \qquad i_{C_2-off} = \frac{3-k}{(1-k)^3} I_o$$

$$I_{L_1} = i_{C_1-off} = I_{L_2} + i_{C_2-off} = \frac{(3-k)(2-k)}{(1-k)^3} I_o \qquad i_{C_1-on} = \frac{(3-k)(2-k)}{k(1-k)^2} I_o$$

$$i_{in} = I_{L_1} + i_{C_1-on} + i_{C_2-on} + i_{C_4-on} + i_{C_6-on}$$

$$= \left[\frac{(3-k)(2-k)}{(1-k)^3} + \frac{(3-k)(2-k)}{k(1-k)^2} + \frac{3-k}{k(1-k)^2} + \frac{1+k}{k(1-k)} + \frac{1}{k} \right] I_o = \frac{11-13k+4k^2}{k(1-k)^3} I_o$$

Therefore,

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$$I_{in} = ki_{in} = \frac{11-13k+4k^2}{(1-k)^3} I_o = \left[\frac{3-k}{1-k}\left(\frac{2-k}{1-k}\right)^2 - 1\right] I_o.$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_2} kT \qquad I_{L_1} = \frac{(2-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in} \qquad I_{L_2} = \frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{(2-k)^2}{(1-k)^2 L_3} kTV_{in} \qquad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2(2-k)(3-k)L_1 I_o} = \frac{k(1-k)^3}{(2-k)(3-k)G_3} \frac{R}{2fL_1} \tag{4.42}$$

and the variation ratio of current i_{L2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)(2-k)TV_1}{2(3-k)L_2 I_o} = \frac{k(1-k)(2-k)}{(3-k)G_3} \frac{R}{2fL_2} \tag{4.43}$$

and the variation ratio of current i_{L_2} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(2-k)^2 TV_{in}}{4(1-k)L_3 I_o} = \frac{k(2-k)^2}{2(1-k)G_3} \frac{R}{2fL_3} \tag{4.44}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT \frac{I_o}{C_{12}} = \frac{k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{4.45}$$

4.3.4 N/O Higher-Order Lift Additional Circuit

N/O higher-order lift additional circuits can be derived from the corresponding circuits of the main series by adding a DEC. Each stage voltage V_i (i = 1, 2,…, n) is

$$V_i = \left[\left(\frac{2-k}{1-k}\right)^i - 1\right] V_{in} \tag{4.46}$$

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This means V_1 is the voltage across capacitor C_2, V_2 is the voltage across capacitor C_4, and so on.

For nth-order lift additional circuit, the final output voltage is

$$V_o = \left[\frac{3-k}{1-k}\left(\frac{2-k}{1-k}\right)^{n-1} - 1\right] V_{in} \tag{4.47}$$

The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \frac{3-k}{1-k}\left(\frac{2-k}{1-k}\right)^{n-1} - 1 \tag{4.48}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^n}{2^{h(1-n)}[(2-k)^{(n-2)}(3-k)]^{u(n-2)}G_n}\frac{R}{fL_1} \tag{4.49}$$

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^{(n-2)}(2-k)}{2^{h(n-2)}(3-k)^{(n-2)}G_n}\frac{R}{2fL_2} \tag{4.50}$$

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(2-k)^{(n-1)}}{2^{h(n-3)}(1-k)^{(n-2)}G_n}\frac{R}{2fL_3} \tag{4.51}$$

where

$$h(x) = \begin{cases} 0 & x > 0 \\ 1 & x \le 0 \end{cases} \text{ is the } \textit{Hong function}$$

$$u(x) = \begin{cases} 1 & x \ge 0 \\ 0 & x < 0 \end{cases} \text{ is the } \textit{unit-step function}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{4.52}$$

4.4 Enhanced Series

All circuits of the enhanced series of N/O super-lift Luo-converters are derived from the corresponding circuits of the main series by adding the DEC into each stage circuit of all series converters.

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The first three stages of this series are shown in Figures 4.4, 4.7, and 4.8. For convenience to explain, they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit, respectively, and numbered as n = 1, 2, and 3.

4.4.1 N/O Elementary Enhanced Circuit

This circuit is derived from N/O elementary circuit with adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 4.4.

The output voltage is

$$V_o = V_{in} + V_{L_1} + V_1 = \frac{2}{1-k} V_{in} = \left[\frac{3-k}{1-k} - 1\right] V_{in} \tag{4.27}$$

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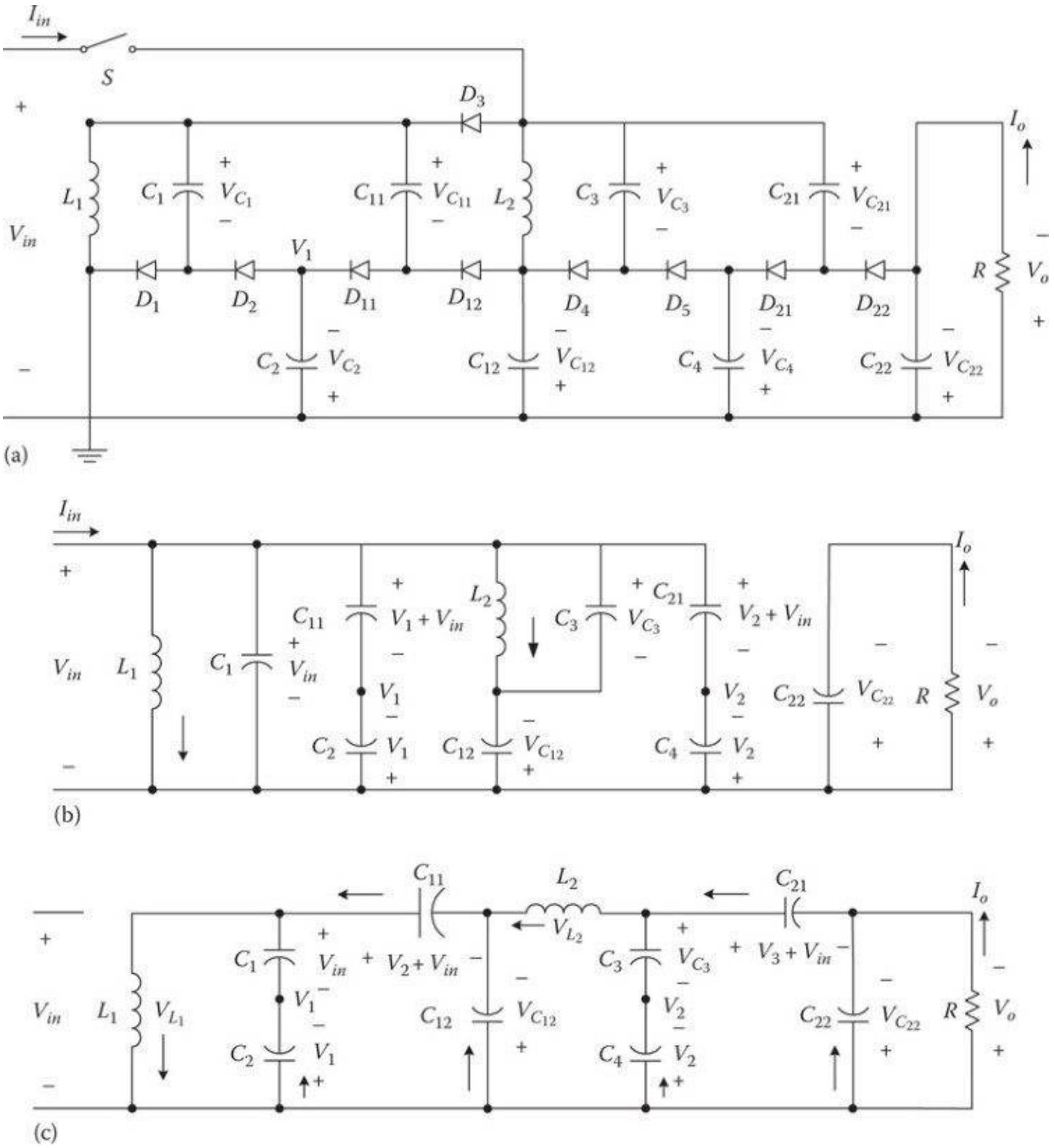


FIGURE 4.7
Negative-output re-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G_1 = \frac{V_o}{V_{in}} = \frac{3-k}{1-k} - 1 \tag{4.28}$$

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4.4.2 N/O Re-Lift Enhanced Circuit

The N/O re-lift enhanced circuit is derived from N/O re-lift circuit of the main series by adding the DEC into each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.7.

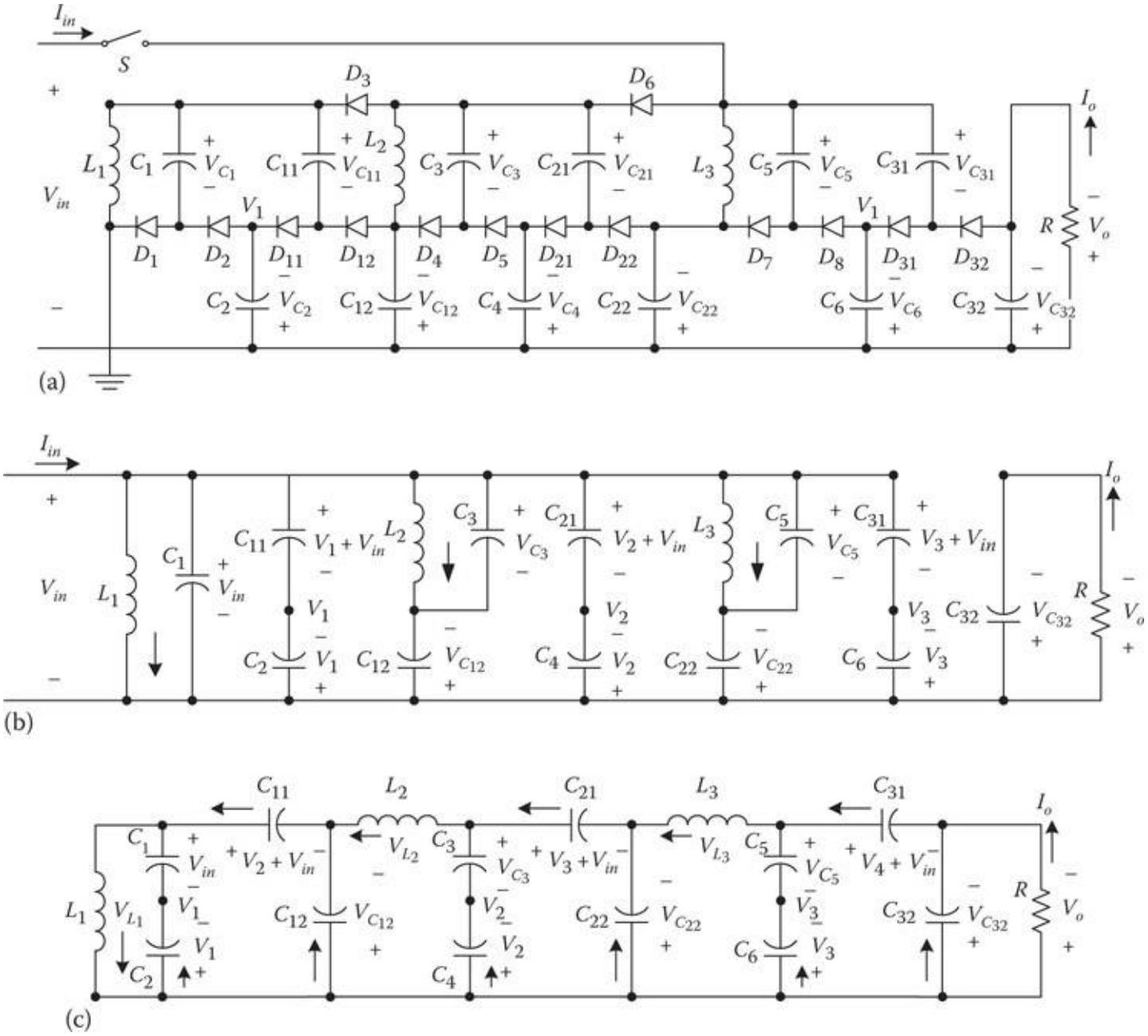


FIGURE 4.8
Negative-output triple-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage across capacitor C_{12} is charged to

$$V_{C_{12}} = \frac{3}{1-k} V_{in} \tag{4.53}$$

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The voltage across capacitor C_3 is charged to $V_{C_{12}}$, and the voltage across capacitors C_4 and C_{12} is charged to V_{C4}

$$V_{C_4} = \frac{2-k}{1-k} V_{C_{12}} = \frac{2-k}{1-k} \frac{3-k}{1-k} V_{in} \tag{4.54}$$

The current flowing through inductor L_2 increases with voltage $V_{C_{12}}$ during switch-on kT and decreases with voltage $-(V_{C_{21}} - V_{C_4} - V_{C_{12}})$ during switch-off $(1 - k)T$.

Therefore,

$$\Delta i_{L_2} = \frac{kT}{L_2}(V_{C_{12}} - V_{in}) = \frac{V_{C_{21}} - V_{C_4} - V_{C_{12}}}{L_2}(1-k)T \tag{4.55}$$

$$V_{C_{21}} = \left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The output voltage is

$$V_o = V_{C_{21}} - V_{in} = \left[\left(\frac{3-k}{1-k}\right)^2 - 1\right] V_{in} \tag{4.56}$$

The voltage transfer gain is

$$G_2 = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 - 1 \tag{4.57}$$

The following relations are obtained:

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$$i_{C_{22}-on} = I_o \qquad i_{C_{22}-off} = \frac{kI_o}{1-k}$$

$$i_{C_{21}-off} = I_o + i_{C_{22}-off} = \frac{I_o}{1-k} \qquad i_{C_{21}-on} = i_{C_4-on} = \frac{I_o}{k}$$

$$i_{C_4-off} = i_{C_3-off} = \frac{I_o}{1-k} \qquad i_{C_3-on} = \frac{I_o}{k}$$

$$I_{L_2} = i_{C_{21}-off} + i_{C_3-off} = \frac{2I_o}{1-k}$$

$$i_{C_{12}-on} = I_{L_2} + i_{C_3-on} = \frac{1+k}{k(1-k)} I_o \qquad i_{C_{12}-off} = \frac{1+k}{(1-k)^2} I_o$$

$$i_{C_{11}-off} = I_{L_2} + i_{C_{12}-off} = \frac{3-k}{(1-k)^2} I_o \qquad i_{C_2-off} = \frac{3-k}{(1-k)^2} I_o$$

$$i_{C_{11}-on} = i_{C_2-on} = \frac{3-k}{k(1-k)} I_o$$

$$I_{L_1} = i_{C_{11}-off} + i_{C_2-off} = 2\frac{3-k}{(1-k)^2} I_o \qquad i_{C_1-on} = \frac{3-k}{k(1-k)} I_o$$

$$i_{in} = I_{L_1} + i_{C_1-on} + i_{C_{11}-on} + i_{C_{12}-on} + i_{C_{21}-on} = \frac{4(2-k)}{k(1-k)^2} I_o$$

Therefore,

$$I_{in} = ki_{in} = \frac{4(2-k)}{(1-k)^2} I_o = \left[\frac{(3-k)^2}{(1-k)^2} - 1\right] I_o$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_2} kT \qquad I_{L_1} = 2\frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_{C_{12}} - V_{in}}{L_2} kT = \frac{2+k}{(1-k)L_2} kTV_{in} \qquad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

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$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 T V_{in}}{4(3-k)L_1 I_o} = \frac{k(1-k)^2}{2(3-k)G_2}\frac{R}{2fL_1} \tag{4.58}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(2+k)TV_{in}}{4L_2 I_o} = \frac{k(2+k)}{2G_2}\frac{R}{2fL_2} \tag{4.59}$$

The ripple voltage of output voltage υ_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = kT\frac{I_o}{C_{22}} = \frac{k}{fC_{22}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage υ_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22}} \tag{4.60}$$

4.4.3 N/O Triple-Lift Enhanced Circuit

This circuit is derived from the N/O triple-lift circuit of main series by adding the DEC into each stage. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.8.

The voltage across capacitor C_{12} is charged to $V_{C_{12}}$. As described in the previous section, the voltage across C_{12} is $V_{C_{12}} = (3-k)/(1-k)V_{in}$ and the voltage across C_4 and C_{22} is

$$V_{C_{22}} = \frac{3-k}{1-k}V_{C_{12}} = \left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The voltage across capacitor C_5 is charged to $V_{C_{22}}$, and the voltage across capacitor C_6 is charged to V_{C_6}

$$V_{C_6} = \frac{2-k}{1-k}V_{C_{22}} = \frac{2-k}{1-k}\left(\frac{3-k}{1-k}\right)^2 V_{in}$$

The current flowing through inductor L_3 increases with voltage $V_{C_{22}}$ during switch-on period kT and decreases with voltage $-(V_{C_{32}} - V_{C_6} - V_{C_{22}})$ during switch-off $(1-k)$T.

Therefore,

$$\Delta i_{L_3} = \frac{kT}{L_3}(V_{C_{22}} - V_{in}) = \frac{V_{C_{31}} - V_{C_6} - V_{C_{22}}}{L_3}(1-k)T \tag{4.61}$$

$$V_{C_{31}} = \left(\frac{3-k}{1-k}\right)^3 V_{in}$$

and

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$$V_o = V_{C31} - V_{in} = \left[\left(\frac{3-k}{1-k}\right)^3 - 1\right] V_{in} \tag{4.62}$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^2 - 1 \tag{4.63}$$

The following relations are obtained:

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$$i_{C_{32}-on} = I_o \qquad i_{C_{32}-off} = \frac{kI_o}{1-k}$$

$$i_{C_{31}-off} = I_o + i_{C_{32}-off} = \frac{I_o}{1-k} \qquad i_{C_{31}-on} = i_{C_6-on} = \frac{I_o}{k}$$

$$i_{C_6-off} = i_{C_5-off} = \frac{I_o}{1-k} \qquad i_{C_6-on} = i_{C_5-on} = \frac{I_o}{k}$$

$$I_{L_3} = i_{C_{31}-off} + i_{C_5-off} = \frac{2I_o}{1-k}$$

$$i_{C_{22}-on} = I_{L_3} + i_{C_5-on} = \frac{1+k}{k(1-k)} I_o \qquad i_{C_{22}-off} = \frac{1+k}{(1-k)^2} I_o$$

$$i_{C_{21}-off} = i_{C_4-off} = I_{L_3} + i_{C_{22}-off} = \frac{3-k}{(1-k)^2} I_o \qquad i_{C_4-on} = \frac{3-k}{k(1-k)} I_o$$

$$I_{L_2} = i_{C_4-off} + i_{C_{21}-off} = 2\frac{3-k}{(1-k)^2} I_o \qquad i_{C_3-on} = \frac{3-k}{k(1-k)} I_o$$

$$i_{C_{12}-on} = I_{L_2} + i_{C_3-on} = \frac{(3-k)(2-k)}{k(1-k)^2} I_o \qquad i_{C_{12}-off} = \frac{(3-k)(2-k)}{(1-k)^3} I_o$$

$$i_{C_{11}-off} = I_{L_2} + i_{C_{12}-off} = \frac{(3-k)(4-3k)}{(1-k)^3} I_o \qquad i_{C_{11}-on} = \frac{(3-k)(4-k)}{k(1-k)^2} I_o$$

$$I_{L_1} = i_{C_{11}-off} + i_{C_1-off} = 2\frac{(3-k)(4-k)}{(1-k)^3} I_o \qquad i_{C_1-on} = i_{C_2-on} = \frac{(3-k)(4-k)}{k(1-k)^2} I_o$$

$$i_{in} = I_{L_1} + i_{C_1-on} + i_{C_2-on} + i_{C_{12}-on} + i_{C_4-on} + i_{C_{22}-on} + i_{C_6-on} = \frac{2(13-12k+3k^2)}{k(1-k)^3} I_o$$

Therefore,

$$I_{in} = ki_{in} = 2\frac{13-12k+3k^2}{(1-k)^3} I_o = \left[\left(\frac{3-k}{1-k}\right)^3 - 1\right] I_o$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_2} kT \qquad I_{L_1} = \frac{2(4-k)(3-k)}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1 + V_{in}}{L_2} kT = \frac{2-k}{(1-k)L_2} kTV_{in} \qquad I_{L_2} = 2\frac{3-k}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2 + V_{in}}{L_3} kT = \frac{(2-k)^2}{(1-k)^2 L_3} kTV_{in} \qquad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{4(4-k)(3-k)L_1 I_o} = \frac{k(1-k)^3}{2(4-k)(3-k)G_3} \frac{R}{2fL_1} \tag{4.64}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)(2-k)TV_1}{4(3-k)L_2 I_o} = \frac{k(1-k)(2-k)}{2(3-k)G_3} \frac{R}{2fL_2} \tag{4.65}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(2-k)^2 TV_{in}}{4(1-k)L_3 I_o} = \frac{k(2-k)^2}{2(1-k)G_3} \frac{R}{2fL_3} \tag{4.66}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32}} = kT \frac{I_o}{C_{32}} = \frac{k}{fC_{32}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32}} \tag{4.67}$$

4.4.4 N/O Higher-Order Lift Enhanced Circuit

N/O higher-order lift enhanced circuits are derived from the corresponding circuits of the main series by adding the DEC in each stage. Each stage final voltage is

$$V_{Ci1} = \left(\frac{3-k}{1-k}\right)^i V_{in} \tag{4.68}$$

For nth-order lift enhanced circuit, the final output voltage is

$$V_o = \left[\left(\frac{3-k}{1-k}\right)^n - 1\right] V_{in} \tag{4.69}$$

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The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \left(\frac{3-k}{1-k}\right)^n - 1 \tag{4.70}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2}} \tag{4.71}$$

4.5 Re-Enhanced Series

All circuits of the re-enhanced series of N/O super-lift Luo-converters are derived from the corresponding circuits of the main series by adding the DEC *twice* in each stage circuit.

The first three stages of this series are shown in Figures 4.9, 4.10 and 4.11. For convenience to explain, they are called elementary re-enhanced circuit, re-lift re-enhanced circuit, and triple-lift re-enhanced circuit, respectively, and numbered as n = 1, 2, and 3.

4.5.1 N/O Elementary Re-Enhanced Circuit

This circuit is derived from the N/O elementary circuit by adding the DEC twice. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 4.9.

The voltage across capacitor C_1 is charged to V_{in}. The voltage across capacitor C_{12} is charged to $V_{C_{12}}$.

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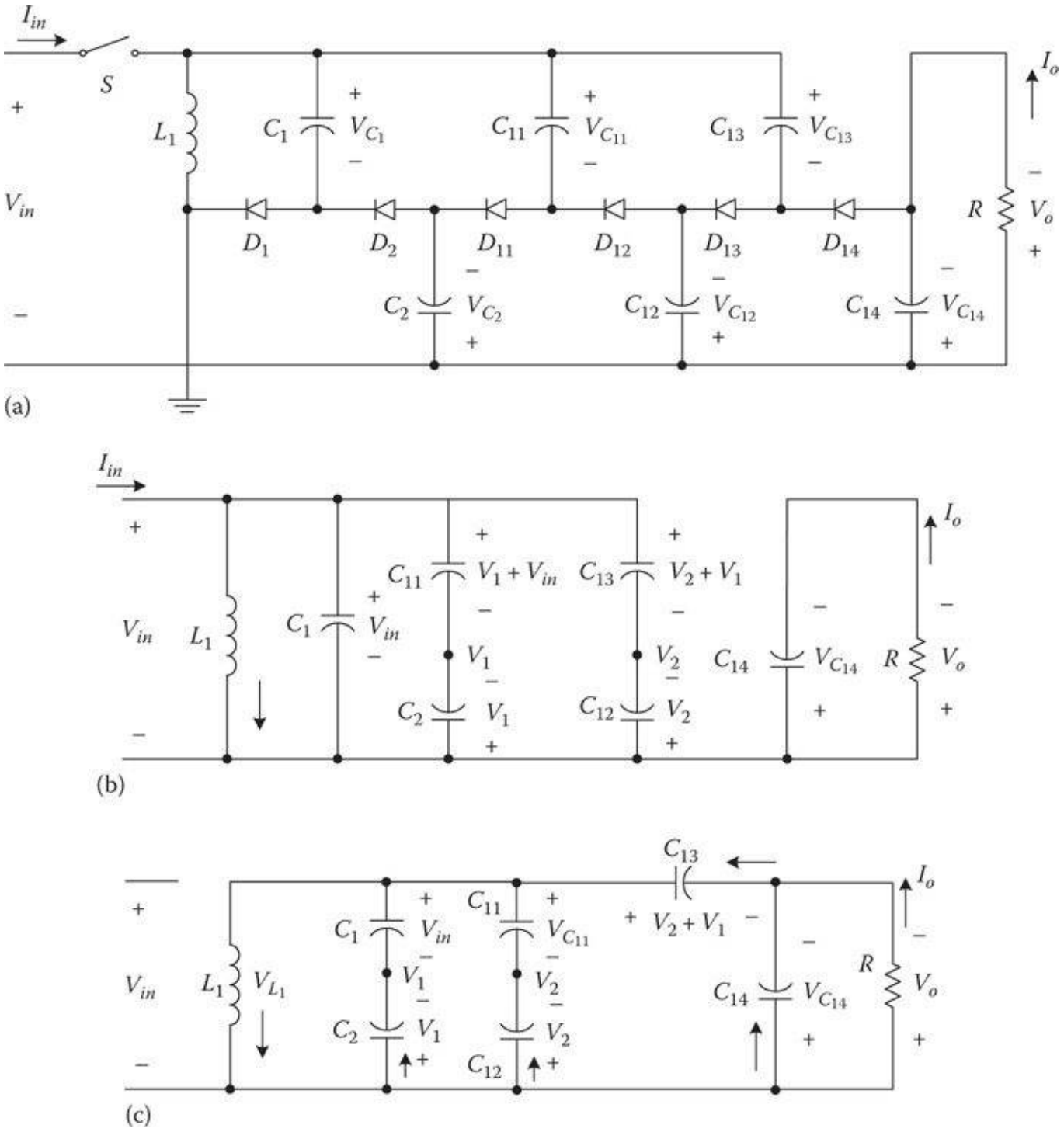


FIGURE 4.9
Negative-output elementary re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage across capacitor C_{13} is charged to $V_{C_{13}}$.

$$V_{C_{13}} = \frac{4-k}{1-k} V_{in} \tag{4.72}$$

The output voltage is

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$$V_o = V_{C13} - V_{in} = \left[\frac{4-k}{1-k} - 1\right] V_{in} \tag{4.73}$$

The voltage transfer gain is

$$G_1 = \frac{V_o}{V_{in}} = \frac{4-k}{1-k} - 1 \tag{4.74}$$

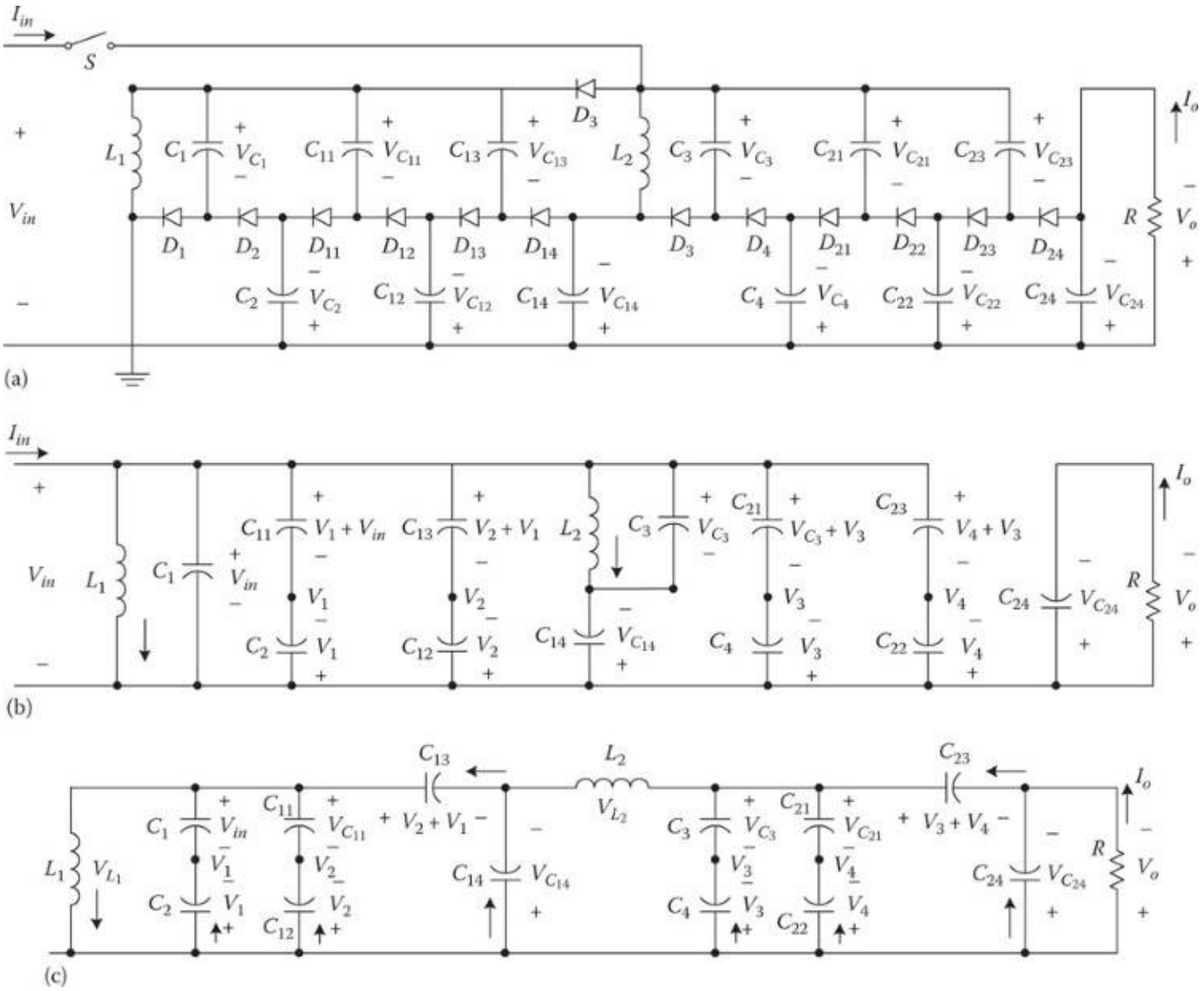


FIGURE 4.10
Negative-output re-lift re-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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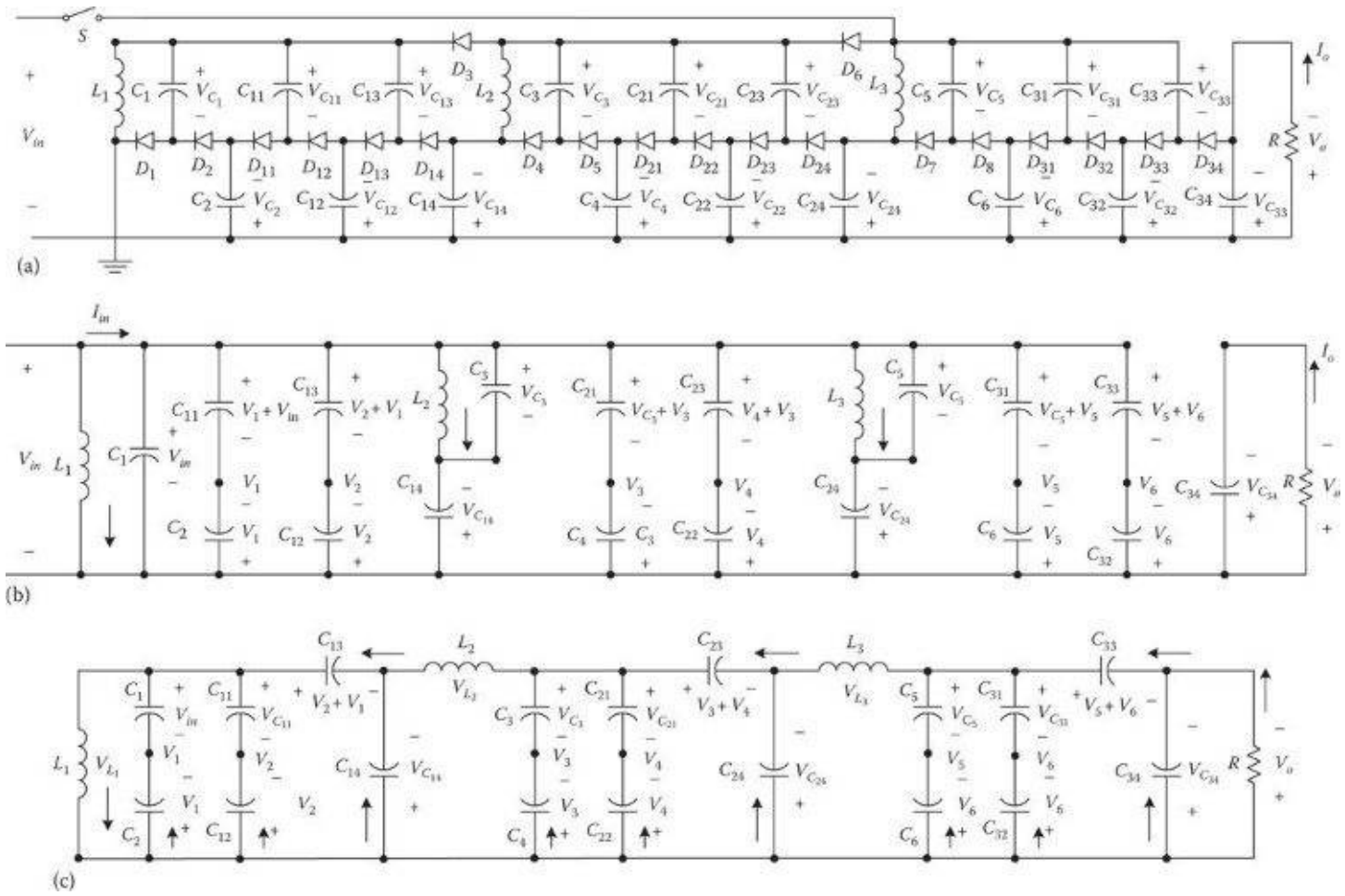


FIGURE 4.11
Negative-output triple-lift re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{14}} = kT\frac{I_o}{C_{14}} = \frac{k}{fC_{14}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{14}} \tag{4.75}$$

4.5.2 N/O Re-Lift Re-Enhanced Circuit

The N/O re-lift re-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC twice in each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.10.

The voltage across capacitor C_{13} is charged to $V_{C_{13}}$. As described in the previous section, the voltage across C_{13} is

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$$V_{C_{13}} = \frac{4-k}{1-k} V_{in}$$

Analogously,

$$V_{C_{23}} = \left(\frac{4-k}{1-k}\right)^2 V_{in} \tag{4.76}$$

The output voltage is

$$V_o = V_{C_{23}} - V_{in} = \left[\left(\frac{4-k}{1-k}\right)^2 - 1\right] V_{in} \tag{4.77}$$

The voltage transfer gain is

$$G_2 = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^2 - 1 \tag{4.78}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{24}} = \frac{I_o kT}{C_{24}} = \frac{k}{fC_{24}} \frac{V_o}{R}.$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o / 2}{V_o} = \frac{k}{2RfC_{24}} \tag{4.79}$$

4.5.3 N/O Triple-Lift Re-Enhanced Circuit

This circuit is derived from N/O triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 4.11.

The voltage across capacitor C_{13} is

$$V_{C_{13}} = \frac{4-k}{1-k} V_{in}$$

The voltage across capacitor C_{23} is

$$V_{C_{23}} = \left(\frac{4-k}{1-k}\right)^2 V_{in}$$

Analogously, the voltage across capacitor C_{33} is

$$V_{C_{33}} = \left(\frac{4-k}{1-k}\right)^3 V_{in} \tag{4.80}$$

The output voltage is

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$$V_o = V_{C33} - V_{in} = \left[\left(\frac{4-k}{1-k}\right)^3 - 1\right] V_{in} \tag{4.81}$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^3 - 1 \tag{4.82}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{34}} = kT\frac{I_o}{C_{34}} = \frac{k}{fC_{34}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{34}} \tag{4.83}$$

4.5.4 N/O Higher-Order Lift Re-Enhanced Circuit

N/O higher-order lift re-enhanced circuit can be derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. Each stage final voltage V_{Ci3} $(i = 1, 2, \ldots, n)$ is

$$V_{Ci3} = \left(\frac{4-k}{1-k}\right)^i V_{in} \tag{4.84}$$

For nth-order lift additional circuit, the final output voltage is

$$V_o = V_{Cn3} - V_{in} = \left[\left(\frac{4-k}{1-k}\right)^n - 1\right] V_{in} \tag{4.85}$$

The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \left(\frac{4-k}{1-k}\right)^n - 1 \tag{4.86}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n4}} \tag{4.87}$$

4.6 Multiple-Enhanced Series

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All circuits of the multiple-enhanced series of N/O super-lift Luo-converters are derived from the corresponding circuits of the main series by adding the DEC multiple (j) times in each stage circuit.

The first three stages of this series are shown in Figures 4.12, 4.13 and 4.14. For convenience to explain, they are called elementary multiple-enhanced circuit, re-lift multiple-enhanced circuit, and triple-lift multiple-enhanced circuit, respectively, and numbered as n = 1, 2, and 3.

4.6.1 N/O Elementary Multiple-Enhanced Circuit

This circuit is derived from the N/O elementary circuit by adding the DEC multiple (j) times. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 4.12.

The voltage across capacitor C_{12j-1} is

$$V_{C_{12j-1}} = \frac{j+2-k}{1-k} V_{in} \tag{4.88}$$

The output voltage is

$$V_o = V_{C_{12j-1}} - V_{in} = \left[\frac{j+2-k}{1-k} - 1 \right] V_{in} \tag{4.89}$$

The voltage transfer gain is

$$G_1 = \frac{V_o}{V_{in}} = \frac{j+2-k}{1-k} - 1 \tag{4.90}$$

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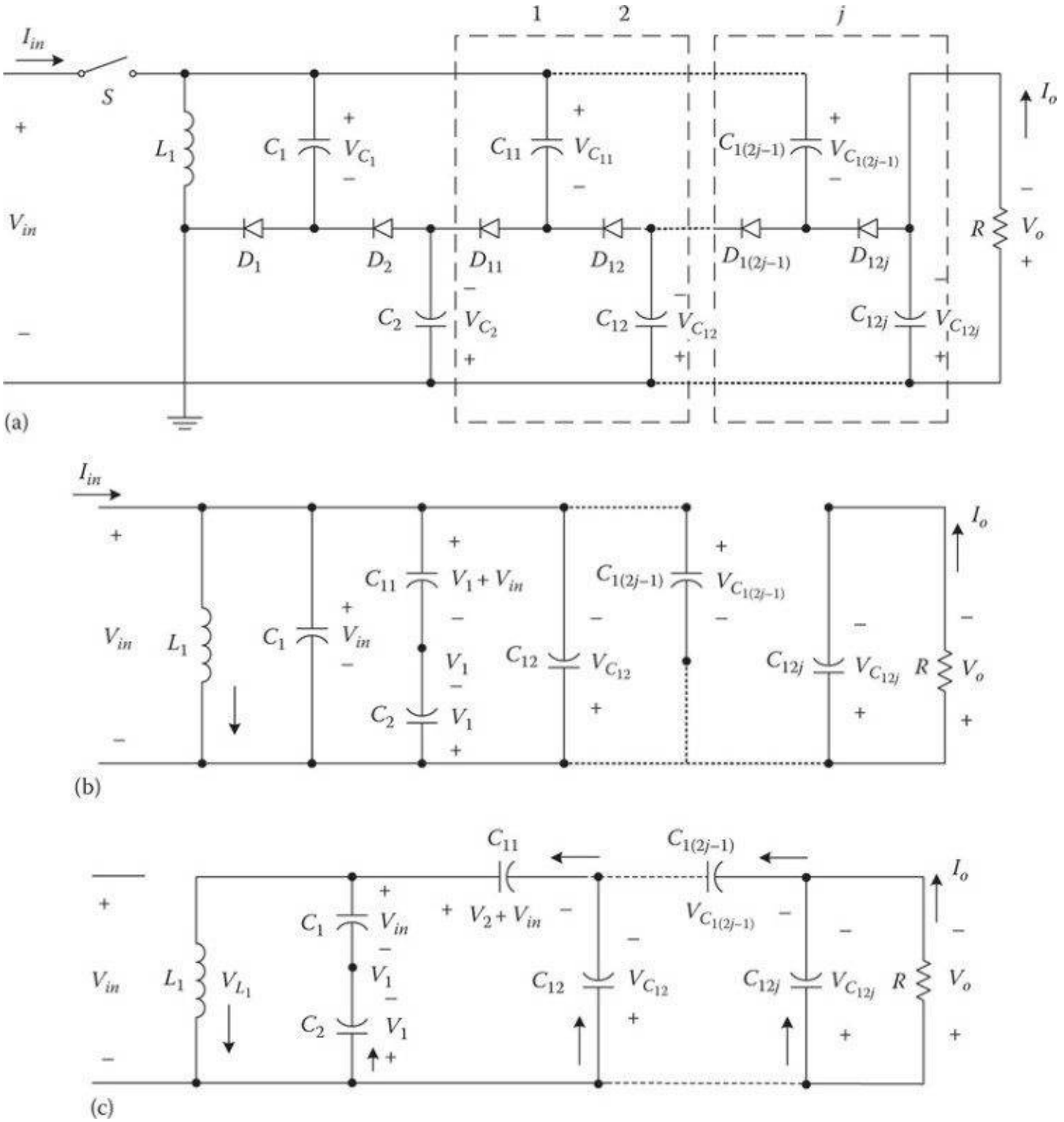


FIGURE 4.12
Negative-output elementary multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12j}} = kT\frac{I_o}{C_{12j}} = \frac{k}{fC_{12j}}\frac{V_o}{R}$$

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Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12j}} \tag{4.91}$$

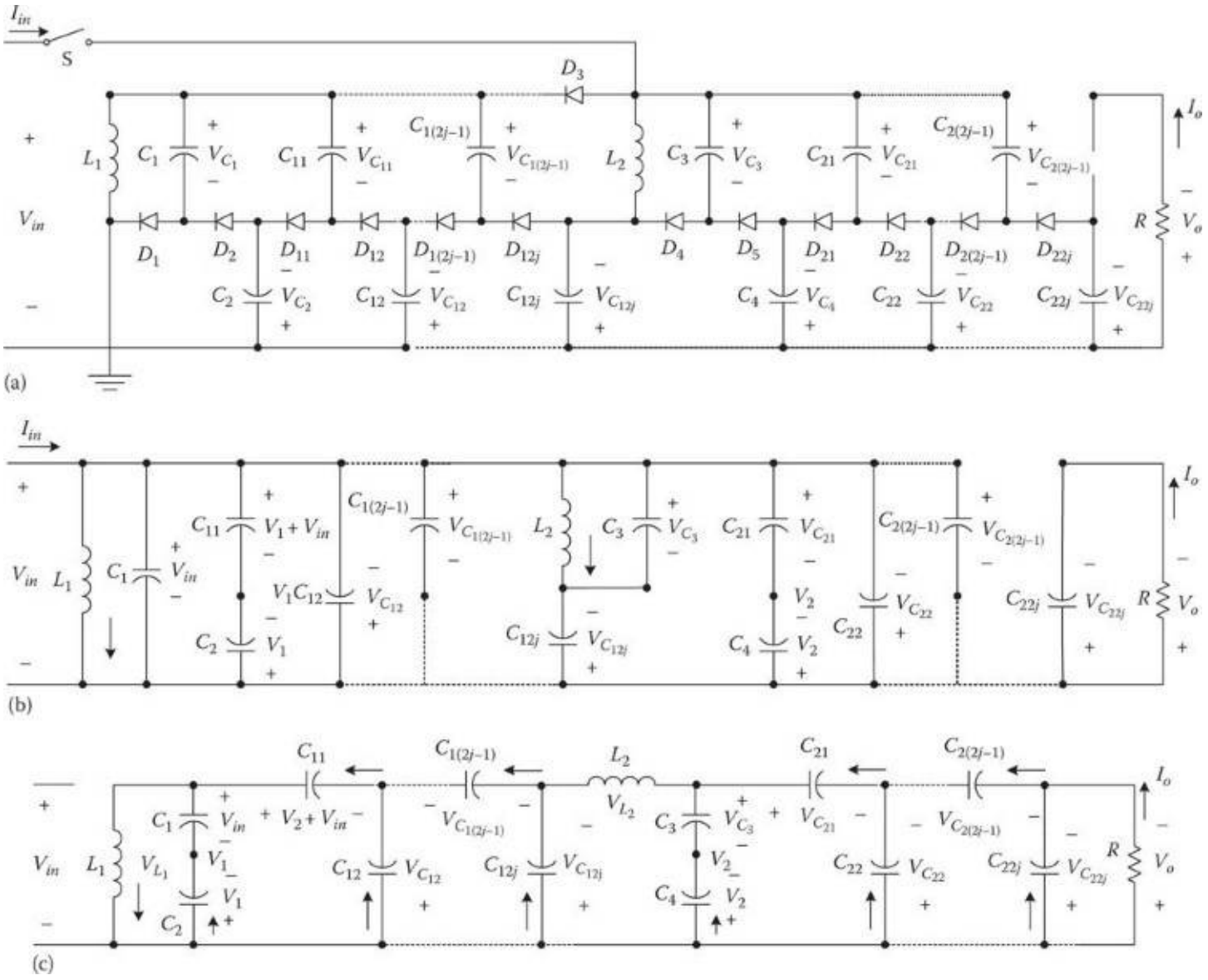


FIGURE 4.13
Negative-output re-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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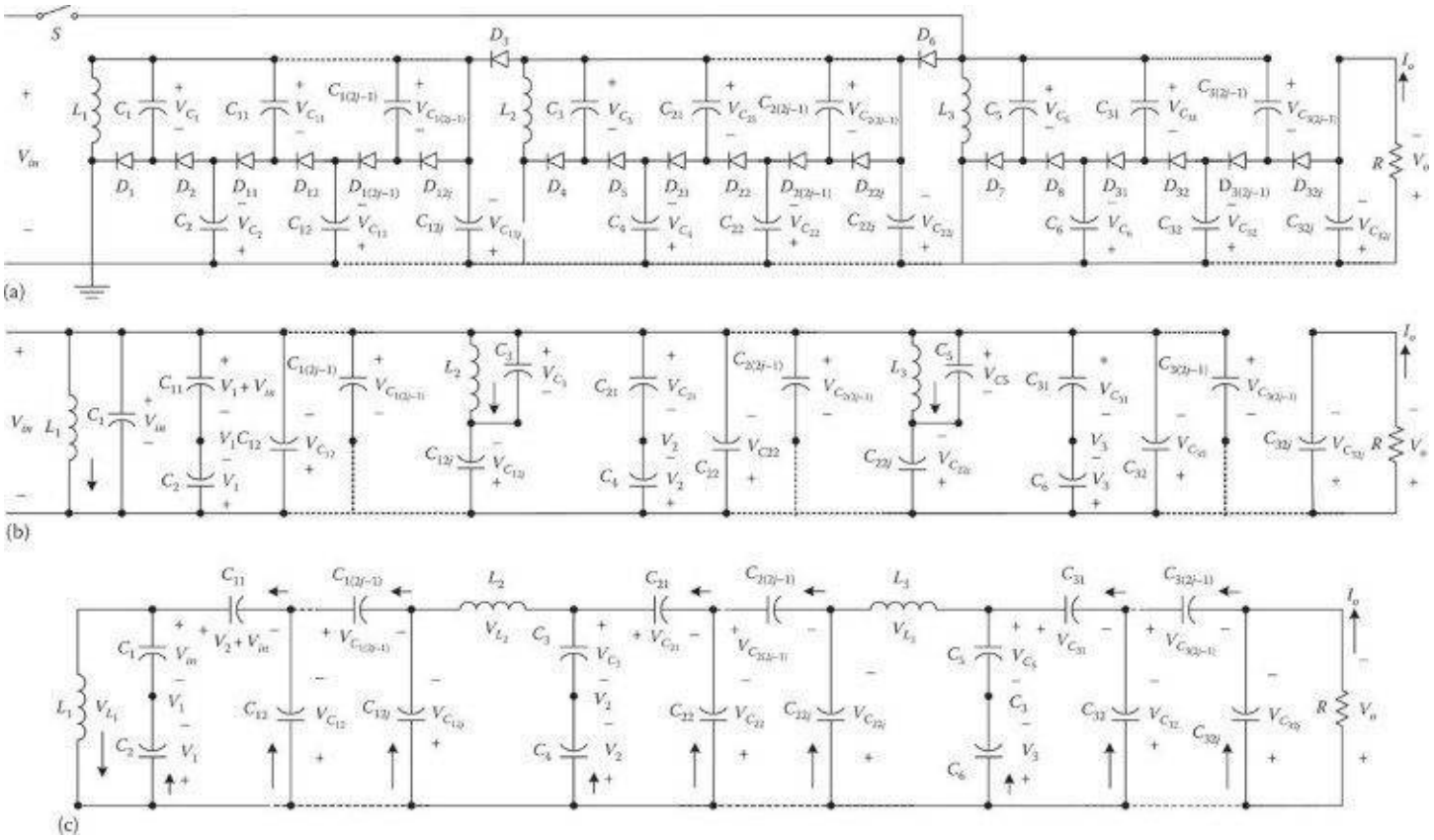


FIGURE 4.14
Negative-output triple-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

4.6.2 N/O Re-Lift Multiple-Enhanced Circuit

The N/O re-lift multiple-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC multiple (j) times into each stage. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 4.13.

The voltage across capacitor C_{22j-1} is

$$V_{C22j-1} = \left(\frac{j+2-k}{1-k}\right)^2 V_{in} \tag{4.92}$$

The output voltage is

$$V_o = V_{C22j-1} - V_{in} = \left[\left(\frac{j+2-k}{1-k}\right)^2 - 1\right] V_{in} \tag{4.93}$$

The voltage transfer gain is

$$G_2 = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^2 - 1 \tag{4.94}$$

The ripple voltage of output voltage v_o is

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$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = kT\frac{I_o}{C_{22j}} = \frac{k}{fC_{22j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22j}} \tag{4.95}$$

4.6.3 N/O Triple-Lift Multiple-Enhanced Circuit

This circuit is derived from N/O triple-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 4.14.

The voltage across capacitor C_{32j-1} is

$$V_{C32j-1} = \left(\frac{j+2-k}{1-k}\right)^3 V_{in} \tag{4.96}$$

The output voltage is

$$V_o = V_{C32j-1} - V_{in} = \left[\left(\frac{j+2-k}{1-k}\right)^3 - 1\right] V_{in} \tag{4.97}$$

The voltage transfer gain is

$$G_3 = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^3 - 1 \tag{4.98}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32j}} = kT\frac{I_o}{C_{32j}} = \frac{k}{fC_{32j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32j}} \tag{4.99}$$

4.6.4 N/O Higher-Order Lift Multiple-Enhanced Circuit

N/O higher-order lift multiple-enhanced circuits are derived from the corresponding circuits of the main series by adding the DEC multiple (j) times in each stage circuit. Each stage final voltage V_{Ci2j-1} $(i = 1, 2, \ldots, n)$ is

$$V_{Ci2j-1} = \left(\frac{j+2-k}{1-k}\right)^i V_{in} \tag{4.100}$$

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For nth-order lift multiple-enhanced circuit, the final output voltage is

$$V_o = \left[\left(\frac{j+2-k}{1-k}\right)^n - 1\right] V_{in} \tag{4.101}$$

The voltage transfer gain is

$$G_n = \frac{V_o}{V_{in}} = \left(\frac{j+2-k}{1-k}\right)^n - 1 \tag{4.102}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2j}} \tag{4.103}$$

4.7 Summary of Negative-Output Super-Lift Luo-Converters

All circuits of N/O super-lift Luo-converters as a family can be shown in Figure 4.15 as the family tree.

From the analysis in previous sections, the common formula to calculate the output voltage can be presented:

$$V_o = \begin{cases} \left[\left(\frac{2-k}{1-k}\right)^n - 1\right] V_{in} & \textit{Main_series} \\ \left[\left(\frac{2-k}{1-k}\right)^{n-1}\left(\frac{3-k}{1-k}\right) - 1\right] V_{in} & \textit{Additional_series} \\ \left[\left(\frac{3-k}{1-k}\right)^n - 1\right] V_{in} & \textit{Enhanced_series} \\ \left[\left(\frac{4-k}{1-k}\right)^n - 1\right] V_{in} & \textit{Re-enhanced_series} \\ \left[\left(\frac{j+2-k}{1-k}\right)^n - 1\right] V_{in} & \textit{Multiple-enhanced_series} \end{cases} \tag{4.104}$$

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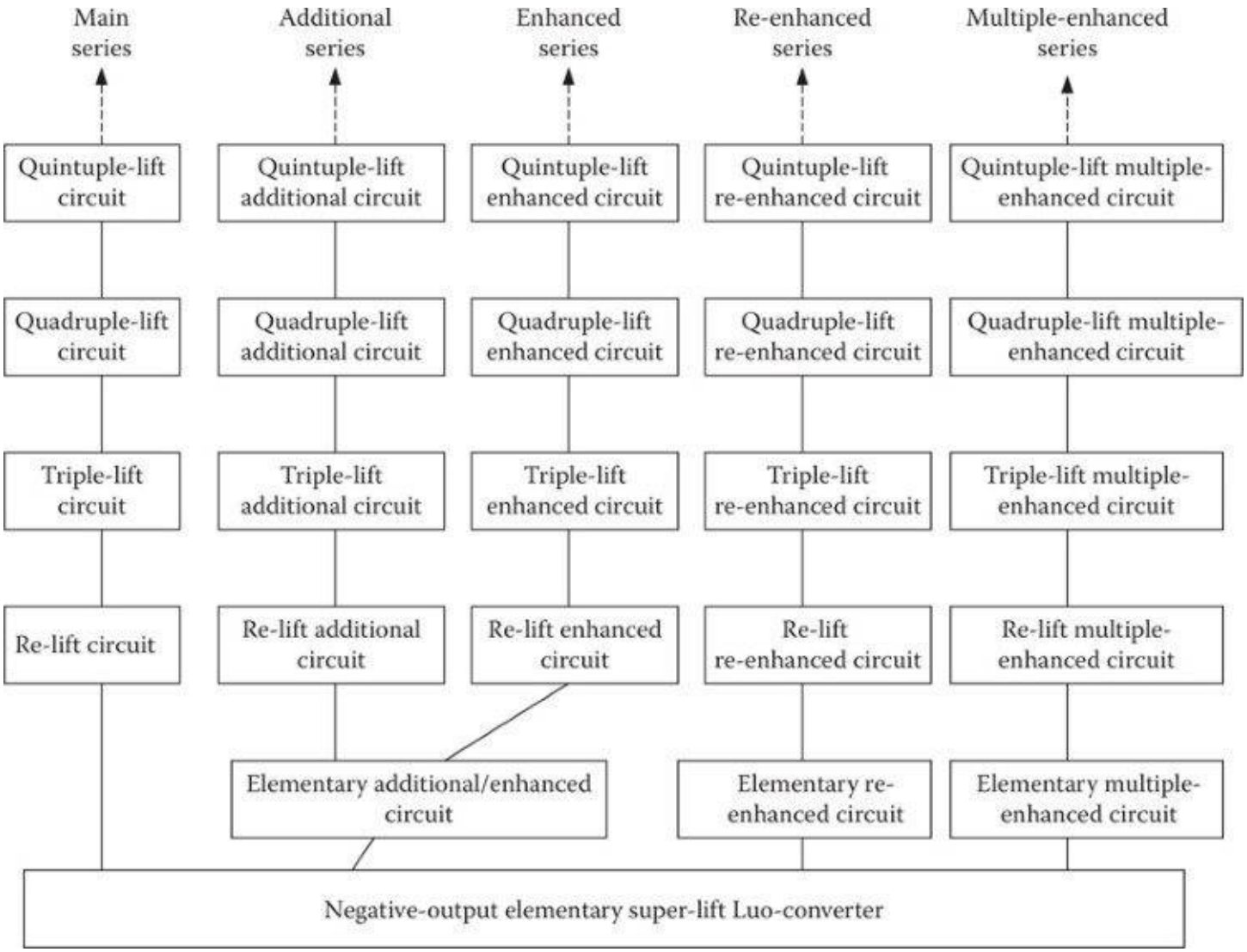


FIGURE 4.15
The family of negative-output super-lift Luo-converters.

The corresponding voltage transfer gain is

$$G=\frac{V_o}{V_{in}}=\begin{cases}\left(\dfrac{2-k}{1-k}\right)^n-1 & Main_series\\ \left(\dfrac{2-k}{1-k}\right)^{n-1}\left(\dfrac{3-k}{1-k}\right)-1 & Additional_series\\ \left(\dfrac{3-k}{1-k}\right)^n-1 & Enhanced_series\\ \left(\dfrac{4-k}{1-k}\right)^n-1 & Re\text{-}enhanced_series\\ \left(\dfrac{j+2-k}{1-k}\right)^n-1 & Multiple\text{-}enhanced_series\end{cases} \tag{4.105}$$

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In order to show the advantages of N/O super-lift converters, their voltage transfer gains can be compared to that of

$$\text{Cúk converter} \qquad G = \frac{V_o}{V_{in}} = \frac{k}{1-k}$$

$$\text{Flyback converter} \qquad G = \frac{V_o}{V_{in}} = \frac{kN}{1-k} \quad (N \text{ is the transformer turns ratio})$$

$$\text{Boost converter} \qquad G = \frac{V_o}{V_{in}} = \frac{1}{1-k}$$

$$\text{N/O Luo-converters} \qquad G = \frac{V_o}{V_{in}} = \frac{n}{1-k} \tag{4.106}$$

If we assume the conduction duty k is 0.2, the output voltage transfer gains are listed in Table 4.1.

If the conduction duty k is 0.5, the output voltage transfer gains are listed in Table 4.2.

If the conduction duty k is 0.8, the output voltage transfer gains are listed in Table 4.3.

TABLE 4.1
Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter	0.2					
Forward converter	0.2N (N is the transformer turns ratio)					
Cuk converter	0.25					
Flyback converter	0.25N (N is the transformer turns ratio)					
Boost converter	1.25					
Negative-output Luo-converters	1.25	2.5	3.75	5	6.25	$1.25n$
Negative-output super-lift converters—main series	1.25	4.06	10.39	24.63	56.67	$2.25^n - 1$
Negative-output super-lift converters—additional series	2.5	6.88	16.72	38.87	88.7	$3.5 * 2.25^{(n-1)} - 1$

TABLE 4.2
Voltage Transfer Gains of Converters in the Condition $k = 0.5$

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Stage No. (n)	1	2	3	4	5	n
Buck converter	0.5					
Forward converter	0.5N (N is the transformer turns ratio)					
Cuk converter	1					
Flyback converter	N (N is the transformer turns ratio)					
Boost converter	2					
Negative-output Luo-converters	2	4	6	8	10	$2n$
Negative-output super-lift converters—main series	2	8	26	80	242	$3^n - 1$
Negative-output super-lift converters—additional series	4	14	44	134	404	$5 * 3^{(n-1)} - 1$

TABLE 4.3
Voltage Transfer Gains of Converters in the Condition $k = 0.8$

Stage No. (n)	1	2	3	4	5	n
Buck converter	0.8					
Forward converter	0.8N (N is the transformer turns ratio)					
Cuk converter	4					
Flyback converter	4N (N is the transformer turns ratio)					
Boost converter	5					
Negative-output Luo-converters	5	10	15	20	25	$5n$
Negative-output super-lift converters—main series	5	35	215	1295	7,775	$6^n - 1$
Negative-output super-lift converters—additional series	10	65	395	2375	14,255	$11 * 6^{(n-1)} - 1$

4.8 Simulation Results

To verify the design and calculation results, PSpice simulation package was applied to these converters. Choose V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all $C_1 - C_8$ = 2 μF and R = 30 k, and using k = 0.5 and f = 100 kHz.

4.8.1 Simulation Results of an N/O Triple-Lift Circuit

The voltage values V_1, V_2, and V_o of a N/O triple-lift circuit are −46, −174, and −639 V, respectively, and the current waveforms are i_{L_1} (its average value $i_{L_1} = 603$ mA), i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 4.16. The voltage values are matched to the calculated results.

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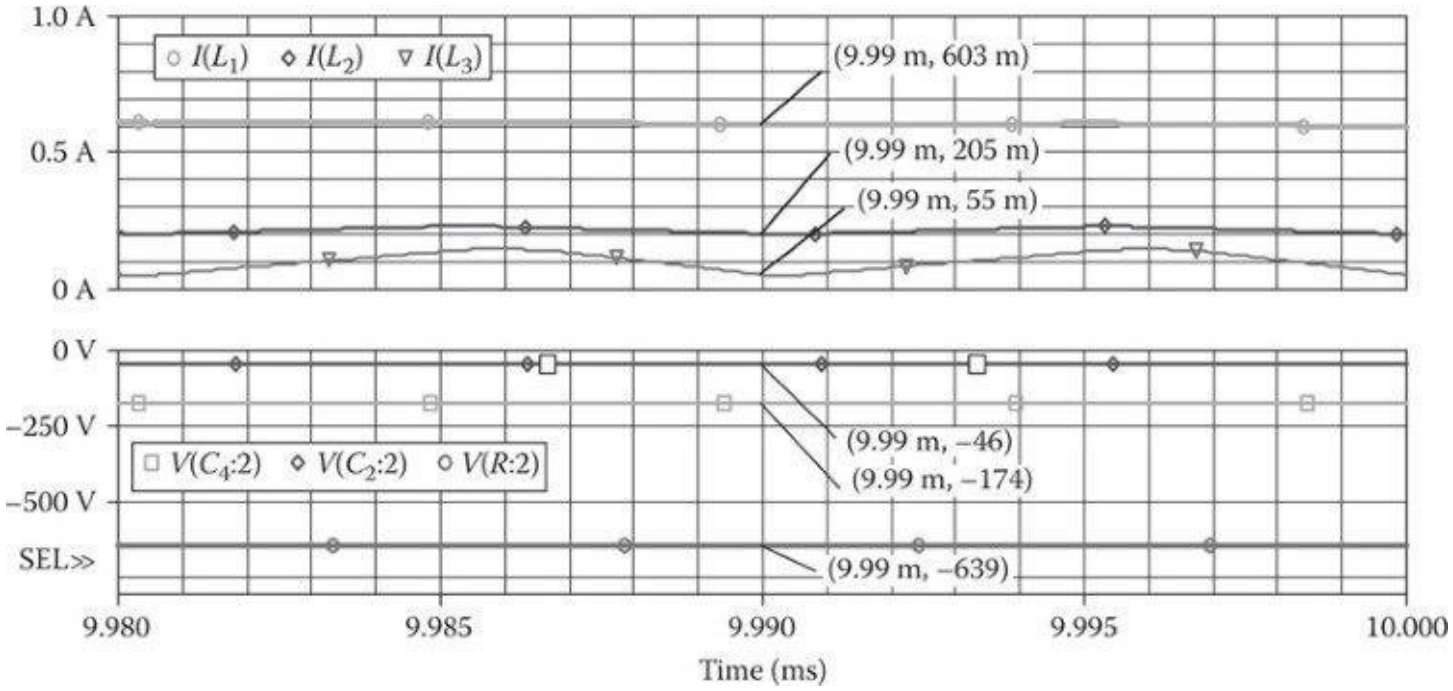


FIGURE 4.16
Simulation results of a negative-output triple-lift circuit at condition **k** = 0.5 and **f** = 100 kHz.

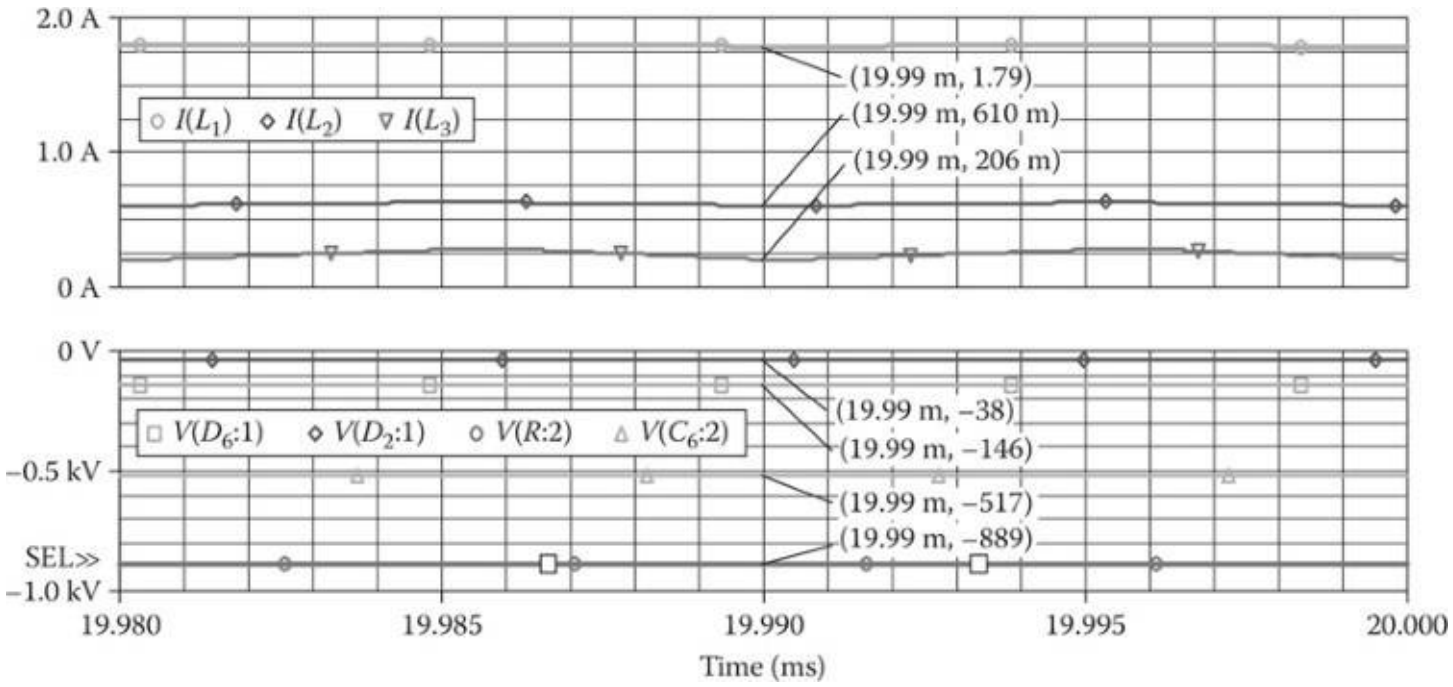


FIGURE 4.17
Simulation results of a negative-output triple-lift additional circuit at condition k = 0.5 and f = 100 kHz.

4.8.2 Simulation Results of an N/O Triple-Lift Additional Circuit

The voltage values V_1, V_2, V_3, and V_o of a N/O triple-lift additional circuit are −38, −146, −517, and −889 V, respectively, and the current waveforms are i_{L_1} (its average value

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$I_{L_1} = 1.79$ A), i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 4.17. The voltage values are matched to the calculated results.

4.9 Experimental Results

A test rig was constructed to verify the design and calculation results and compared with PSpice simulation results. The testing conditions are the same: V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all C_1−C_8 = 2 μF and R = 30 k, and using k = 0.5 and f = 100 kHz. The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. The output voltage and the first diode current values are measured in the following converters.

4.9.1 Experimental Results of an N/O Triple-Lift Circuit

After careful measurement, the current value of $I_{L_1} = 0.6$ A (shown in Channel 1 with 1 A/Div) and voltage value of V_o = –640 V (shown in Channel 2 with 200 V/Div) are obtained. The experimental results (current and voltage values) in Figure 4.18 are identically matched to the calculated and simulation results, which are $I_{L_1} = 0.603$ A and V_o = −639 V shown in Figure 4.16.

4.9.2 Experimental Results of an N/O Triple-Lift Additional Circuit

The experimental results (voltage and current values) are identically matched to the calculated and simulation results as shown in Figure 4.19. The current value of $I_{L_1} = 1.78$ A (shown in Channel 1 with 1 A/Div) and voltage value of V_o = −890 V (shown in Channel 2 with 200 V/Div) are obtained. The experimental results are identically matched to the calculated and simulation results, which are $I_{L_1} = 1.79$ A and V_o = −889 V shown in Figure 4.17.

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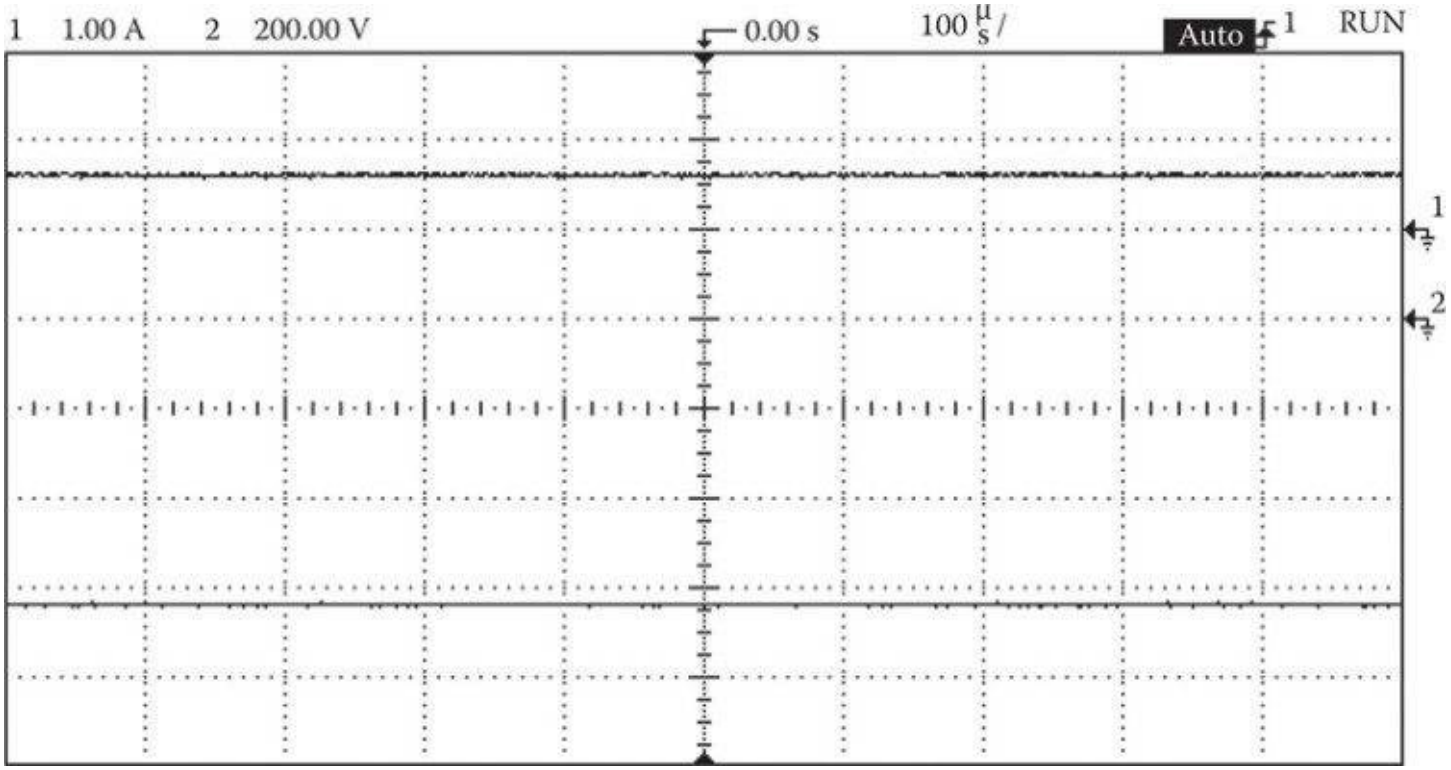


FIGURE 4.18
Experimental results of a negative-output triple-lift circuit at condition **k** = 0.5 and **f** = 100 kHz.

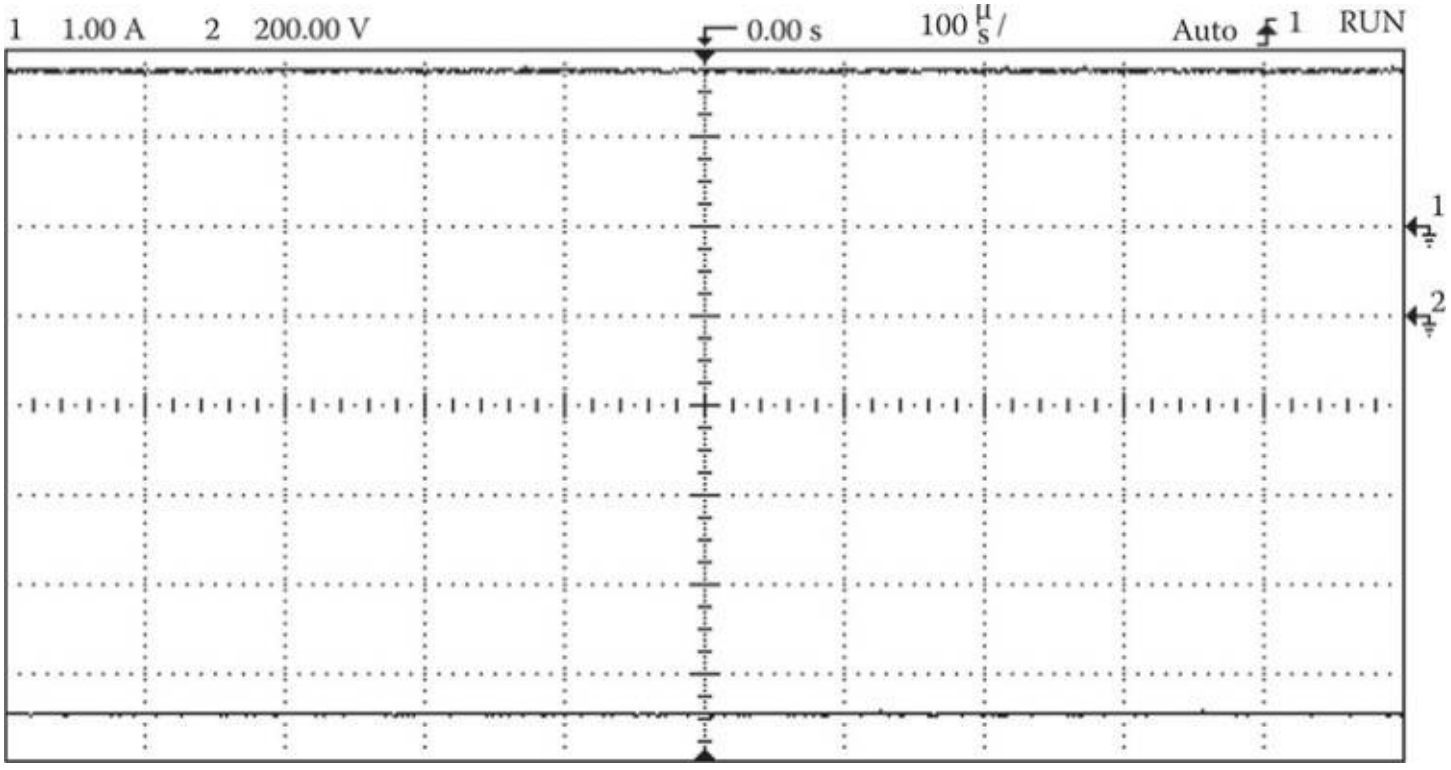


FIGURE 4.19
Experimental results of a negative-output triple-lift additional circuit at condition *k* = 0.5 and *f* = 100 kHz.

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4.9.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully, but efficiency. Particularly, the efficiencies of the tested circuits are 51%–78%, which is good for high-voltage output equipment. The comparison of the simulation and experimental results, which are listed in Tables 4.4 and 4.5, demonstrates that all results are well identified to each other.

TABLE 4.4
Comparison of Simulation and Experimental Results of a Negative-Output Triple-Lift Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	$\lvert V_o \rvert$ (V)	P_o (W)	η (%)
Simulation results	0.603	0.871	20	17.42	639	13.61	78.12
Experimental results	0.6	0.867	20	17.33	640	13.65	78.75

TABLE 4.5
Comparison of Simulation and Experimental Results of a Negative-Output Triple-Lift Additional Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	$\lvert V_o \rvert$ (V)	P_o (W)	η (%)
Simulation results	1.79	2.585	20	51.7	889	26.34	51
Experimental results	1.78	2.571	20	51.4	890	26.4	51

4.9.4 Transient Process and Stability Analysis

Usually, there is high inrush current during the first power on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick lasting only a few milliseconds.

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Positive-Output Cascaded Boost Converters

Super-lift technique largely increases the voltage transfer gain in geometric progression. However, these circuits are bit complex. This chapter introduces a novel approach—the positive-output cascaded boost converters that implement the output voltage increasing in geometric progression, but with simpler structure. They also effectively enhance their Voltage transfer gains in power law.

5.1 Introduction

In order to sort these converters differently from existing voltage-lift and super-lift converters, these converters are entitled "positive-output (P/O) cascaded boost converters." There are several subseries:

- Main series: Each circuit of the main series has one switch *S*, *n* inductors, *n* capacitors, and (2*n* − 1) diodes.
- Additional series: Each circuit of the additional series has one switch *S*, *n* inductors, (*n* + 2) capacitors, and (2*n* + 1) diodes.
- Double series: Each circuit of the double series has one switch *S*, *n* inductors, *n* capacitors, and (3*n* − 1) diodes.
- Triple series: Each circuit of the triple series has one switch S, *n* inductors, 5*n* capacitors, and (5*n* −es.
- Multiple series: Each multiple series circuit has one switch *S* and a higher number of capacitors and diodes.

In order to concentrate the super-lift function, these converters work in the steady state with the condition of continuous conduction mode.

The conduction duty ratio is *k*, the switching frequency is *f*, the switching period is $T = 1/f$, and the load is resistive load *R*. The input voltage and current are V_{in} and I_{in}, and the output voltage and current are V_o and I_o. Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_o \times I_o$. The voltage transfer gain is *G*: $G = V_o/V_{in}$.

5.2 Main Series

The first three stages of the main series of P/O cascaded boost converters are shown in Figures 5.1, 5.2 and 5.3. For convenience to explain, they are called elementary boost

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converter, two-stage circuit, and three-stage circuit, respectively, and numbered as n = 1, 2, and 3.

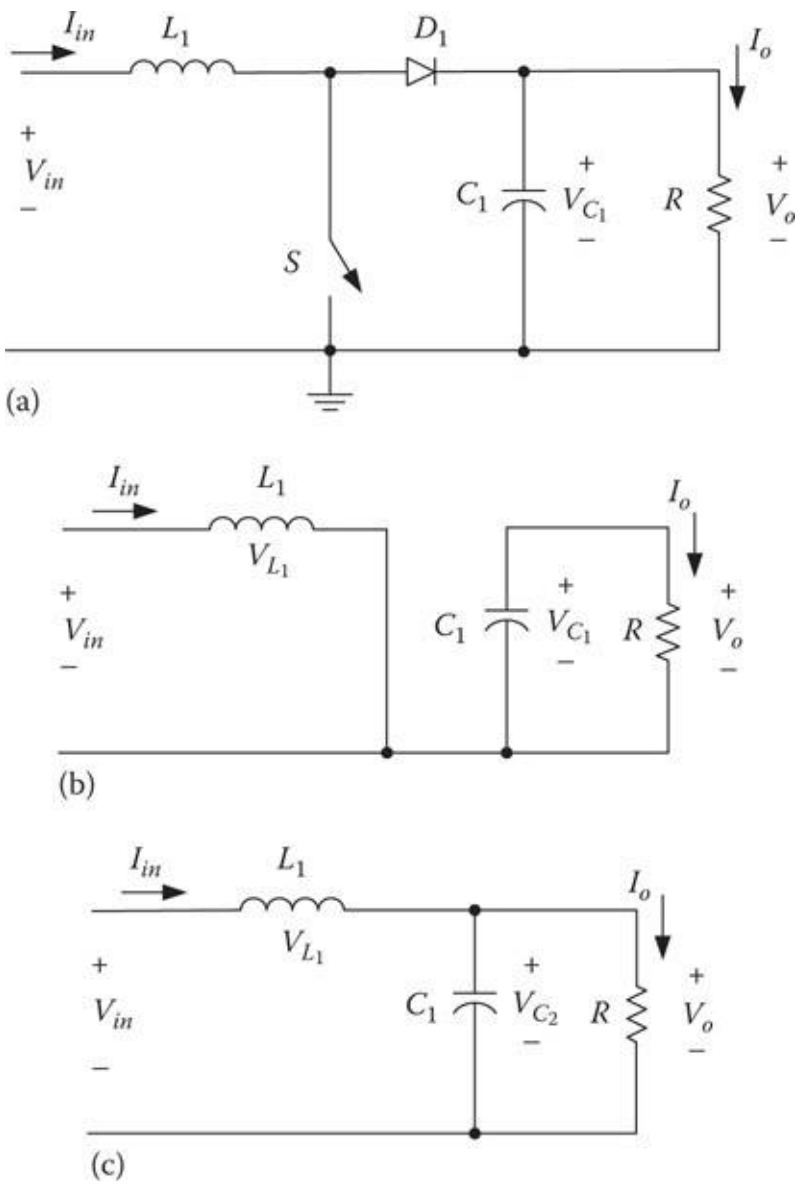


FIGURE 5.1
Elementary boost converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

5.2.1 Elementary Boost Circuit

The elementary boost converter is the fundamental boost converter, and it was also introduced in Chapter 1. Its circuit diagram and its equivalent circuits during switch-on and switch-off are shown in Figure 5.1.

The voltage across capacitor C_1 is charged to V_o. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_o - V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_1} is

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_o - V_{in}}{L_1}(1-k)T \tag{5.1}$$

$$V_o = \frac{1}{1-k} V_{in} \tag{5.2}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-k} \tag{5.3}$$

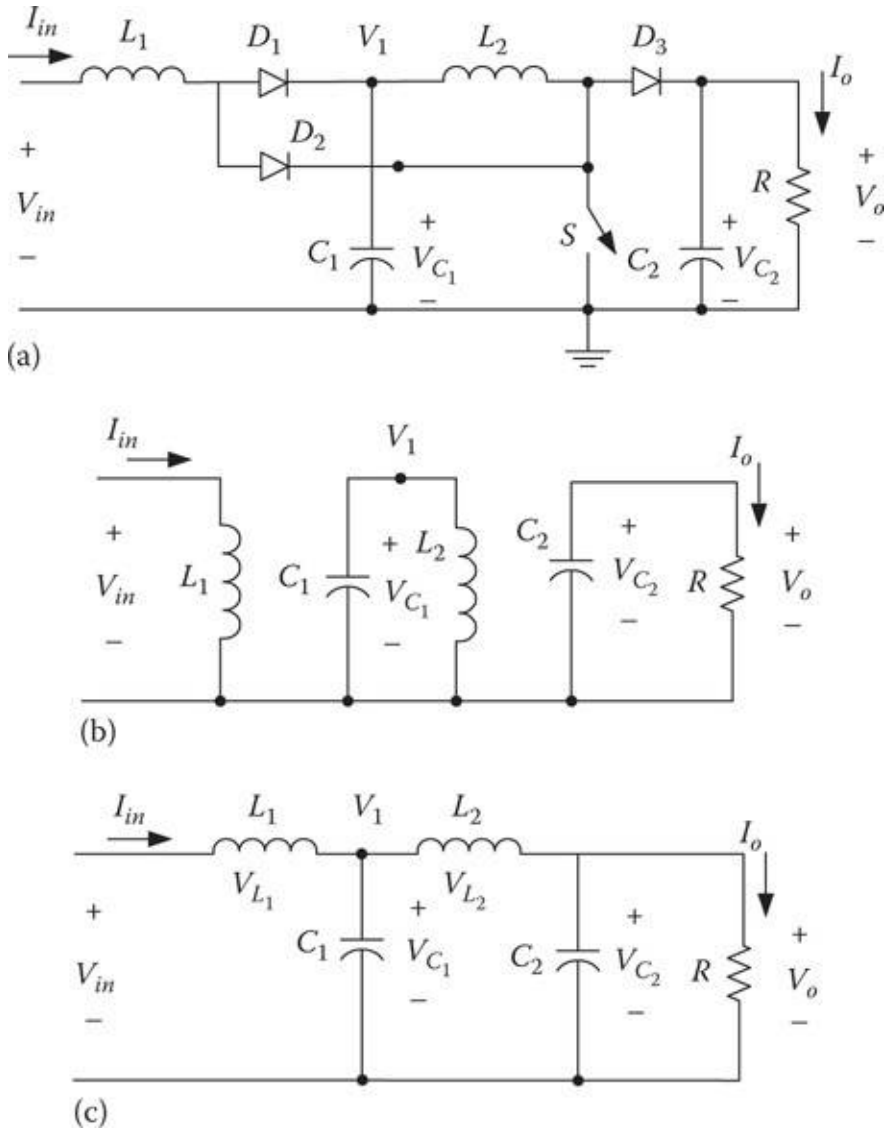


FIGURE 5.2
Two-stage boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The inductor average current is

$$I_{L_1} = \frac{1}{1-k} \frac{V_o}{R} \tag{5.4}$$

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The variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_{in}}{2L_1V_o/(1-k)R} = \frac{k(1-k)^2}{2}\frac{R}{fL_1} \tag{5.5}$$

Usually, ξ_1 is small (much lower than unity), which means this converter works in the continuous mode.

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_1} = kT\frac{I_o}{C_1} = \frac{k}{fC_1}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_1} \tag{5.6}$$

Usually, R is in kΩ, f in 10 kHz, and C_1 in μF; the ripple is smaller than 1%.

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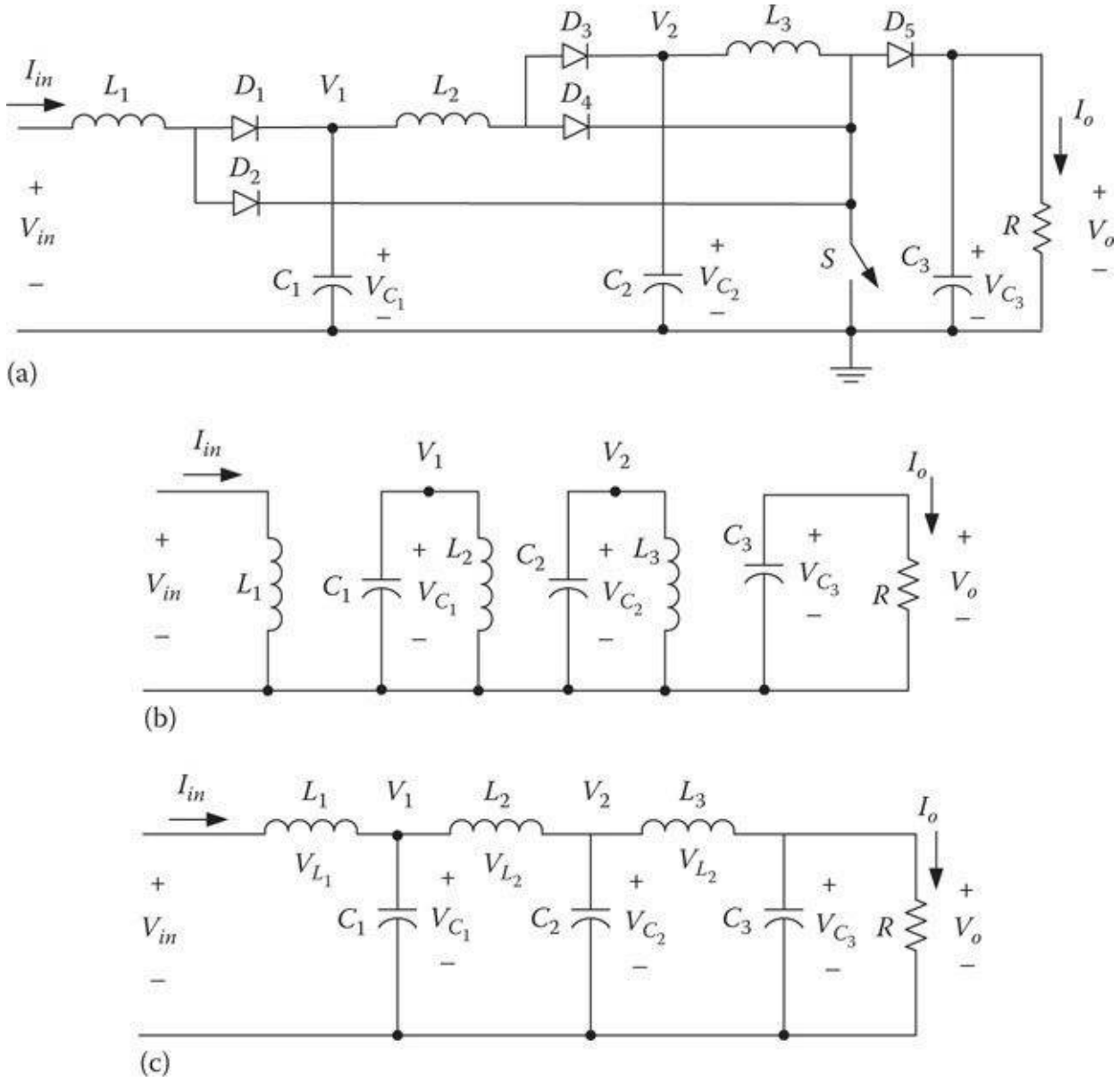


FIGURE 5.3
Three-stage boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

5.2.2 Two-Stage Boost Circuit

The two-stage boost circuit is derived from the elementary boost converter by adding the parts (L_2–D_2–D_3–C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 5.2.

The voltage across capacitor C_1 is charged to V_1. As described in the previous section, the voltage V_1 across capacitor C_1 is $V_1 = 1/(1 - k)V_{in}$.

The voltage across capacitor C_2 is charged to V_o. The current flowing through inductor L_2 increases with voltage V_1 during switching-on period kT and decreases with voltage $-(V_o - V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

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$$\Delta i_{L_2} = \frac{V_1}{L_2} kT = \frac{V_o - V_1}{L_2}(1-k)T \tag{5.7}$$

$$V_o = \frac{1}{1-k} V_1 = \left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.8}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^2 \tag{5.9}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_o}{(1-k)^2}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current I_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 T V_{in}}{2L_1 I_o} = \frac{k(1-k)^4}{2} \frac{R}{fL_1} \tag{5.10}$$

the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{2L_2 I_o} = \frac{k(1-k)^2}{2} \frac{R}{fL_2} \tag{5.11}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_2} \tag{5.12}$$

5.2.3 Three-Stage Boost Circuit

The three-stage boost circuit is derived from the two-stage boost circuit by double adding the parts (L_2–D_2–D_3–C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 5.3.

The voltage across capacitor C_1 is charged to V_1. As described previously, the voltage V_1across capacitor C_1 is $V_1 = 1/(1 - k)V_{in}$, and the voltage V_2 across capacitor C_2 is

$$V_2 = \left(\frac{1}{1-k}\right)^2 V_{in}$$

The voltage across capacitor C_3 is charged to V_o. The current flowing through inductor L_3 increases with voltage V_2 during switching-on period kT and decreases with voltage $-(V_o -$

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V_2) during switching-off (1 − k)T. Therefore, the ripple of the inductor current i_{L_3} is

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT = \frac{V_o - V_2}{L_3}(1-k)T \tag{5.13}$$

$$V_o = \frac{1}{1-k} V_2 = \left(\frac{1}{1-k}\right)^2 V_1 = \left(\frac{1}{1-k}\right)^3 V_{in} \tag{5.14}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^3 \tag{5.15}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_o}{(1-k)^3}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{I_o}{(1-k)^2}$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 T V_{in}}{2L_1 I_o} = \frac{k(1-k)^6}{2} \frac{R}{fL_1} \tag{5.16}$$

The variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 T V_1}{2L_2 I_o} = \frac{k(1-k)^4}{2} \frac{R}{fL_2} \tag{5.17}$$

The variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k) T V_2}{2L_3 I_o} = \frac{k(1-k)^2}{2} \frac{R}{fL_3} \tag{5.18}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_3} \tag{5.19}$$

5.2.4 Higher-Stage Boost Circuit

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The higher-stage boost circuit can be designed by just multiple repeating the parts (L_2–D_2–D_3–C_2). For nth-stage boost circuit, the final output voltage across capacitor C_n is

$$V_o = \left(\frac{1}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^n \tag{5.20}$$

the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2}\frac{R}{fL_i} \tag{5.21}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_n} \tag{5.22}$$

5.3 Additional Series

All circuits of the additional series of P/O cascaded boost converters are derived from the corresponding circuits of the main series by adding a DEC.

The first three stages of this series are shown in Figures 5.4, 5.5 and 5.6. For convenience to explain, they are called elementary additional circuit, two-stage additional circuit, and three-stage additional circuit, respectively, and numbered as n = 1, 2, and 3.

5.3.1 Elementary Boost Additional (Double) Circuit

This elementary boost additional circuit is derived from the elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 5.4.

The voltage across capacitors C_1 and C_{11} is charged to V_1, and the voltage across capacitor C_{12} is charged to $V_o = 2V_1$. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switchoff $(1 - k)T$. Therefore,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1}kT = \frac{V_1 - V_{in}}{L_1}(1-k)T \tag{5.23}$$

$$V_1 = \frac{1}{1-k}V_{in}$$

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The output voltage is

$$V_o = 2V_1 = \frac{2}{1-k} V_{in} \tag{5.24}$$

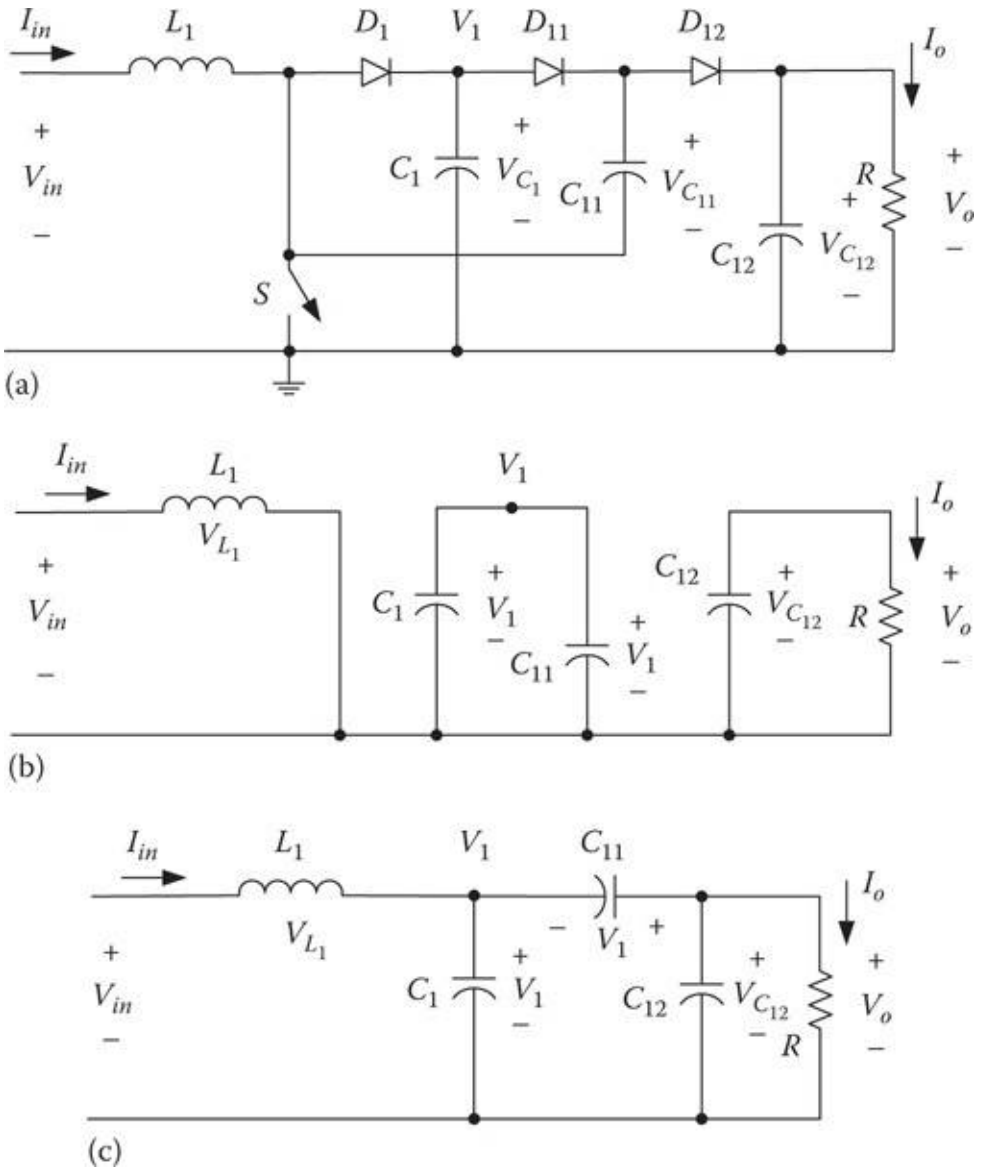


FIGURE 5.4
Elementary boost additional (double) circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2}{1-k} \tag{5.25}$$

and

$$i_{in} = I_{L_1} = \frac{2}{1-k} I_o \tag{5.26}$$

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The variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{8}\frac{R}{fL_1} \tag{5.27}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

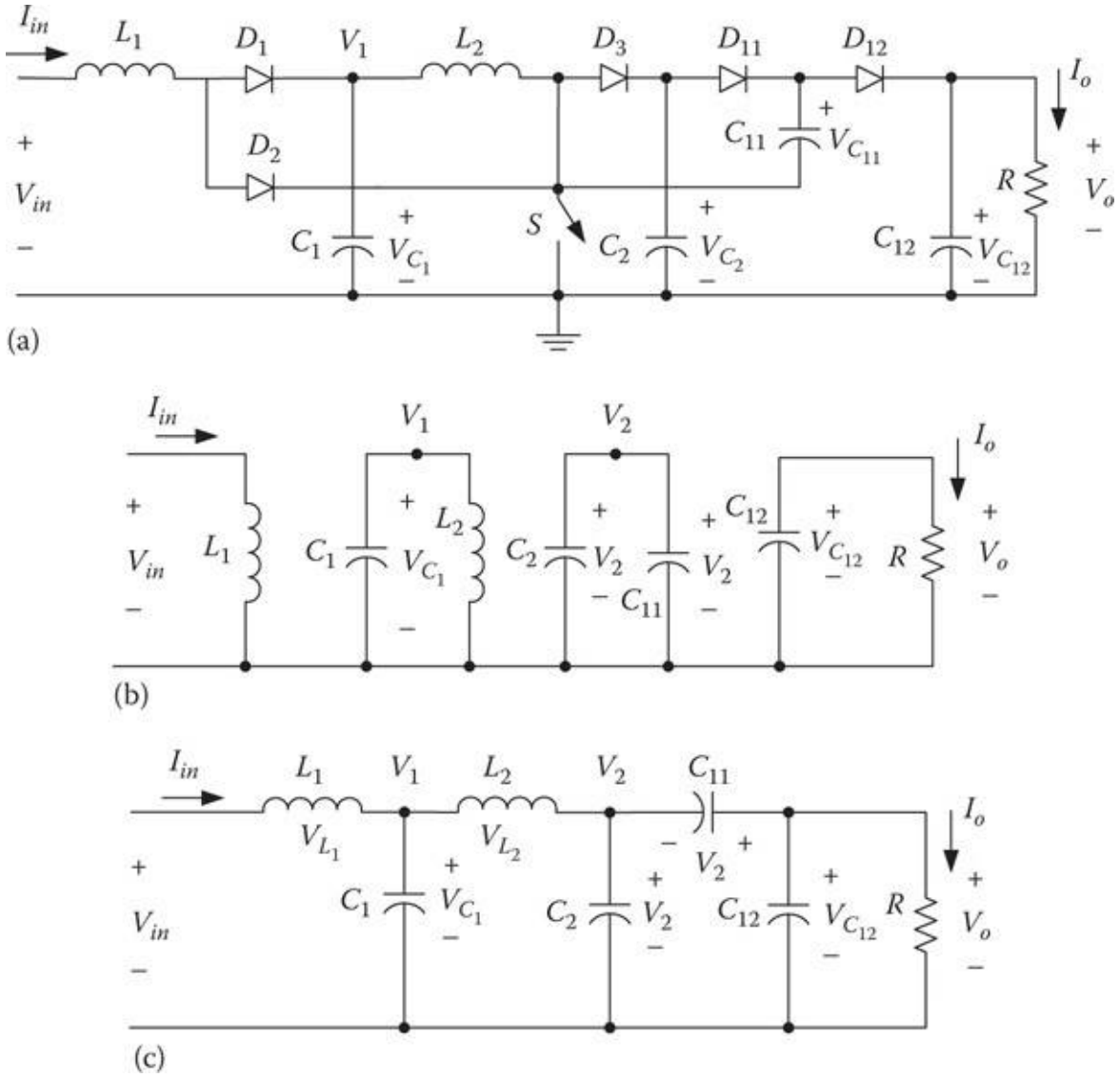


FIGURE 5.5
Two-stage boost additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{5.28}$$

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5.3.2 Two-Stage Boost Additional Circuit

The two-stage additional boost circuit is derived from the two-stage boost circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 5.5.

The voltage across capacitor C_1 is charged to V_1. As described in the previous section, the voltage V_1 across capacitor C_1 is $V_1 = 1/(1 - k)V_{in}$.

The voltage across capacitors C_2 and C_{11} is charged to V_2, and the voltage across capacitor C_{12} is charged to V_o. The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_2 - V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT = \frac{V_2 - V_1}{L_2}(1-k)T \tag{5.29}$$

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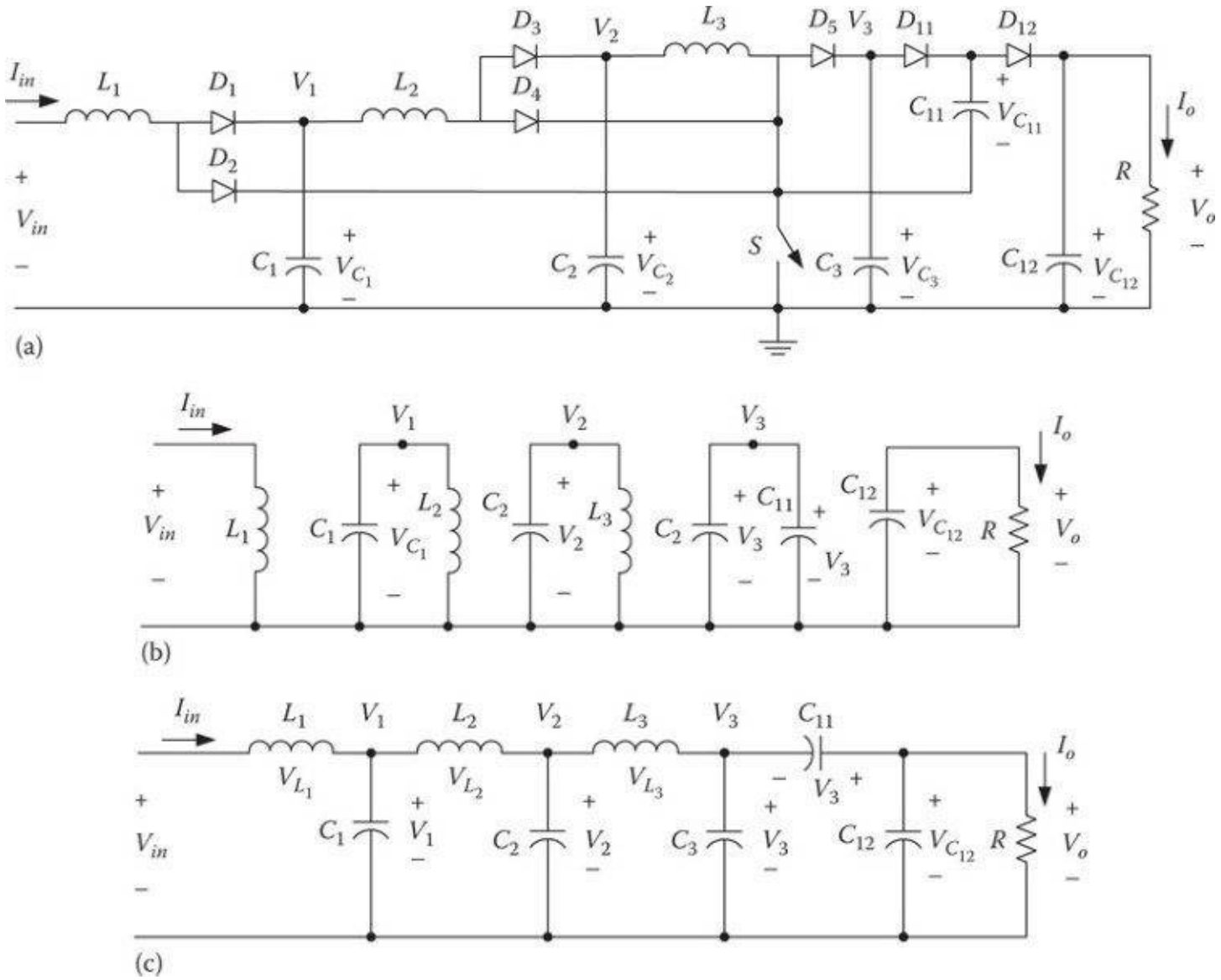


FIGURE 5.6
Three-stage boost additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$V_2 = \frac{1}{1-k} V_1 = \left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.30}$$

The output voltage is

$$V_o = 2V_2 = \frac{2}{1-k} V_1 = 2\left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.31}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^2 \tag{5.32}$$

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Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{2}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{4L_1 I_o} = \frac{k(1-k)^4}{8} \frac{R}{fL_1} \tag{5.33}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \tag{5.34}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT \frac{I_o}{C_{12}} = \frac{k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{5.35}$$

5.3.3 Three-Stage Boost Additional Circuit

This circuit is derived from the three-stage boost circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 5.6.

The voltage across capacitor C_1 is charged to V_1. As described previously, the voltage V_1 across capacitor C_1 is $V_1 = 1/(1 - k)V_{in}$, and the voltage V_2 across capacitor C_2 is $V_2 = (1/(1 - k))^2 V_{in}$.

The voltage across capacitors C_3 and C_{11} is charged to V_3. The voltage across capacitor C_{12} is charged to V_o. The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_3 - V_2)$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT = \frac{V_3 - V_2}{L_3} (1-k)T \tag{5.36}$$

and

$$V_3 = \frac{1}{1-k} V_2 = \left(\frac{1}{1-k}\right)^2 V_1 = \left(\frac{1}{1-k}\right)^3 V_{in} \tag{5.37}$$

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The output voltage is

$$V_o = 2V_3 = 2\left(\frac{1}{1-k}\right)^3 V_{in} \tag{5.38}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^3 \tag{5.39}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{2}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{4L_1 I_o} = \frac{k(1-k)^6}{8}\frac{R}{fL_1} \tag{5.40}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{4L_2 I_o} = \frac{k(1-k)^4}{8}\frac{R}{fL_2} \tag{5.41}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)^2}{8}\frac{R}{fL_3} \tag{5.42}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{5.43}$$

5.3.4 Higher-Stage Boost Additional Circuit

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Higher-stage boost additional circuits can be designed by repeating the parts (L_2–D_2–D_3–C_2) multiple times. For nth-stage additional circuit, the final output voltage is

$$V_o = 2\left(\frac{1}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^n \tag{5.44}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{8}\frac{R}{fL_i} \tag{5.45}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{5.46}$$

5.4 Double Series

All circuits of the double series of P/O cascaded boost converters are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in Figures 5.4, 5.7, and 5.8. For convenience to explain, they are called elementary double circuit, two-stage double circuit, and three-stage double circuit, respectively, and numbered as n = 1, 2, and 3.

5.4.1 Elementary Double Boost Circuit

From the construction principle, the elementary double boost circuit is derived from the elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 5.4, which is the same as the elementary boost additional circuit.

5.4.2 Two-Stage Double Boost Circuit

The two-stage double boost circuit is derived from the two-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 5.7.

The voltage across capacitors C_1 and C_{11} is charged to V_1. As described in the previous section, the voltage V_1 across capacitors C_1 and C_{11} is $V_1 = 1/(1-k)V_{in}$. The voltage across

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capacitor C_{12} is charged to $2V_1$.

The current flowing through inductor L_2 increases with voltage $2V_1$ during switch-on period kT and decreases with voltage $-(V_2 - 2V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{2V_1}{L_2} kT = \frac{V_2 - 2V_1}{L_2}(1-k)T \tag{5.47}$$

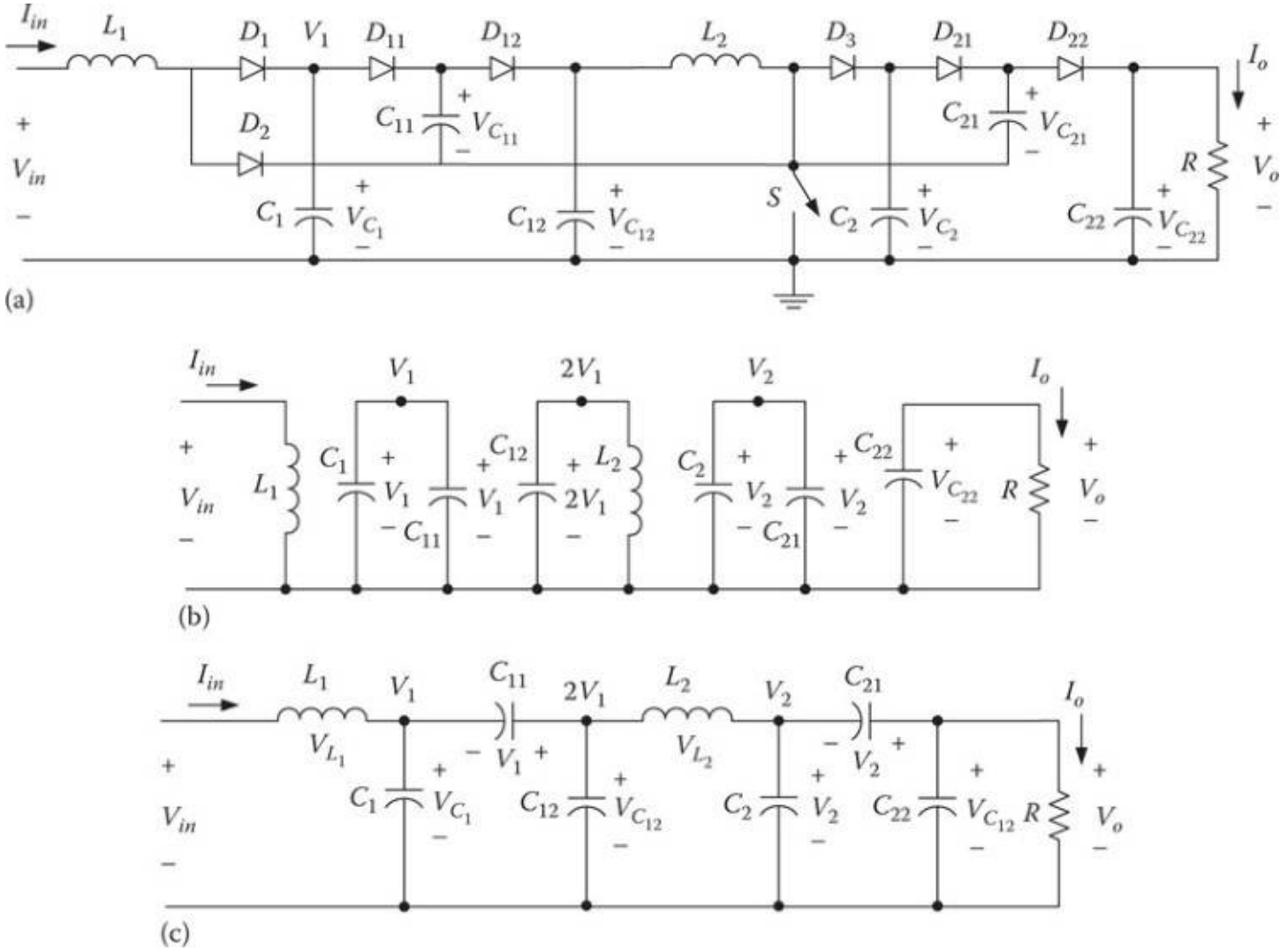


FIGURE 5.7
Two-stage boost double circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$V_2 = \frac{2}{1-k} V_1 = 2\left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.48}$$

The output voltage is

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$$V_o = 2V_2 = \left(\frac{2}{1-k}\right)^2 V_{in} \tag{5.49}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^2 \tag{5.50}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \left(\frac{2}{1-k}\right)^2 I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

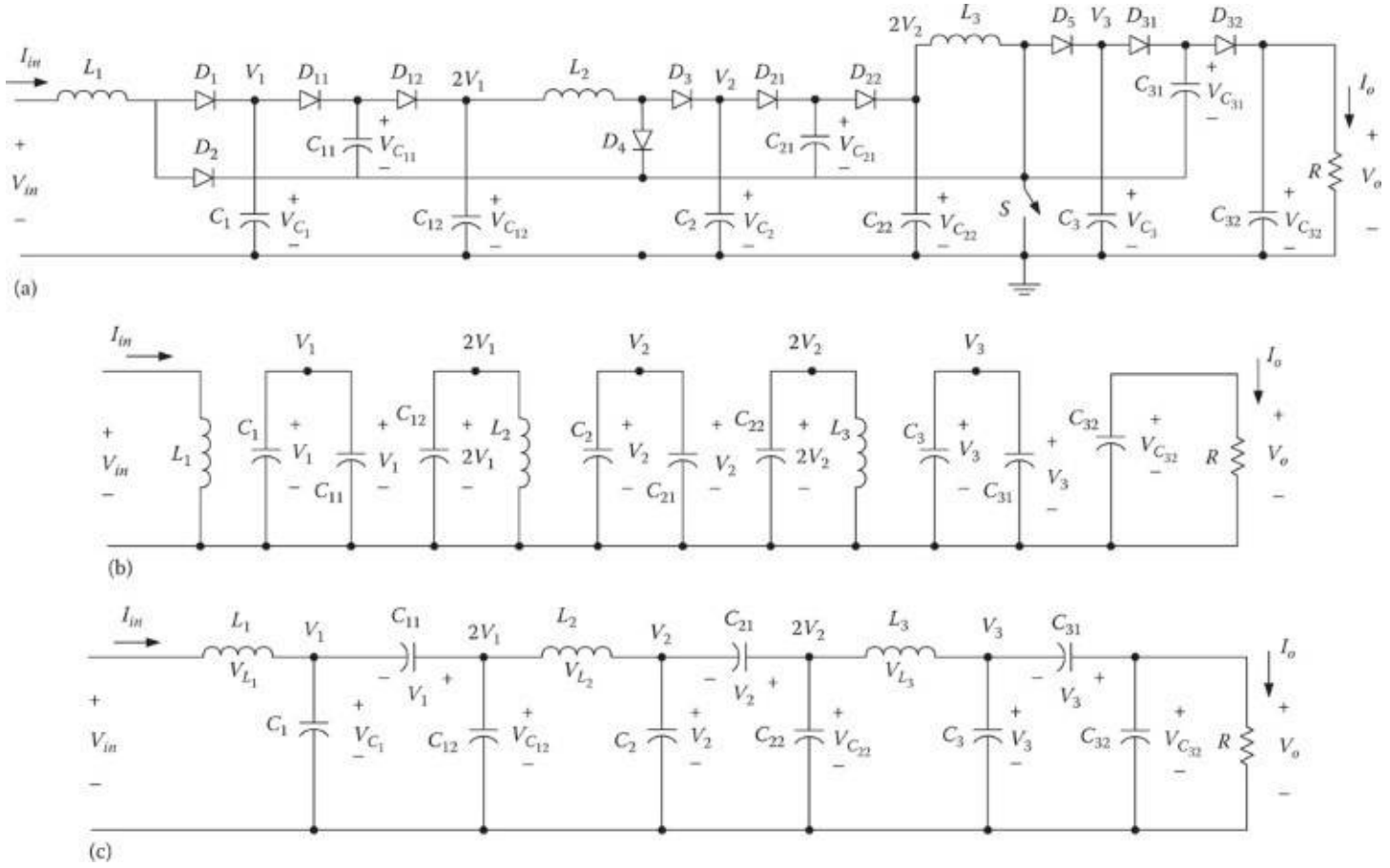


FIGURE 5.8
Three-stage boost double circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

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$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 T V_{in}}{8 L_1 I_o} = \frac{k(1-k)^4}{16}\frac{R}{fL_1} \tag{5.51}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8}\frac{R}{fL_2} \tag{5.52}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = kT\frac{I_o}{C_{22}} = \frac{k}{fC_{22}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22}} \tag{5.53}$$

5.4.3 Three-Stage Double Boost Circuit

This circuit is derived from the three-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 5.8.

The voltage across capacitors C_1 and C_{11} is charged to V_1. As described in the previous section, the voltage V_1 across capacitors C_1 and C_{11} is $V_1 = 1/(1-k)V_{in}$, and the voltage V_2 across capacitors C_2 and C_{12} is $V_2 = 2(1/(1-k))^2 V_{in}$.

The voltage across capacitor C_{22} is $2V_2 = (2/(1-k))^2 V_{in}$. The voltage across capacitors C_3 and C_{31} is charged to V_3. The voltage across capacitor C_{12} is charged to V_o. The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_3 - 2V_2)$ during switch-off $(1-k)T$. Therefore,

$$\Delta i_{L_3} = \frac{2V_2}{L_3}kT = \frac{V_3 - 2V_2}{L_3}(1-k)T \tag{5.54}$$

and

$$V_3 = \frac{2V_2}{(1-k)} = \frac{4}{(1-k)^3}V_{in} \tag{5.55}$$

The output voltage is

$$V_o = 2V_3 = \left(\frac{2}{1-k}\right)^3 V_{in} \tag{5.56}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^3 \tag{5.57}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{8}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{4}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{16L_1 I_o} = \frac{k(1-k)^6}{128} \frac{R}{fL_1} \tag{5.58}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{8L_2 I_o} = \frac{k(1-k)^4}{32} \frac{R}{fL_2} \tag{5.59}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \tag{5.60}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32}} = kT \frac{I_o}{C_{32}} = \frac{k}{fC_{32}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32}} \tag{5.61}$$

5.4.4 Higher-Stage Double Boost Circuit

Higher-stage double boost circuits can be derived from the corresponding main series circuits by adding a DEC in each stage circuit. For nth-stage additional circuit, the final output voltage is $V_o = (2/(1-k))^n V_{in}$.

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^n \tag{5.62}$$

Analogously, the variation ratio of current i_{Li} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2*2^{2n}} \frac{R}{fL_i} \tag{5.63}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2}} \tag{5.64}$$

5.5 Triple Series

All circuits of the triple series of P/O cascaded boost converters are derived from the corresponding circuits of the double series by adding the DEC twice in each stage circuit. The first three stages of this series are shown in Figures 5.9, 5.10 and 5.11. For convenience to explain, they are called elementary triple boost circuit, two-stage triple boost circuit, and three-stage triple boost circuit, respectively, and numbered as n = 1, 2, and 3.

5.5.1 Elementary Triple Boost Circuit

From the construction principle, the elementary triple boost circuit is derived from the elementary double boost circuit by adding another DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 5.9.

The output voltage of first stage boost circuit is V_1, $V_1 = V_{in}/(1 - k)$.

The voltage across capacitors C_1 and C_{11} is charged to V_1, and the voltage across capacitors C_{12} and C_{13} is charged to $V_{C_{13}} = 2V_1$ The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1}(1-k)T \tag{5.65}$$

$$V_1 = \frac{1}{1-k} V_{in}$$

The output voltage is

$$V_o = V_{C_1} + V_{C_{13}} = 3V_1 = \frac{3}{1-k} V_{in} \tag{5.66}$$

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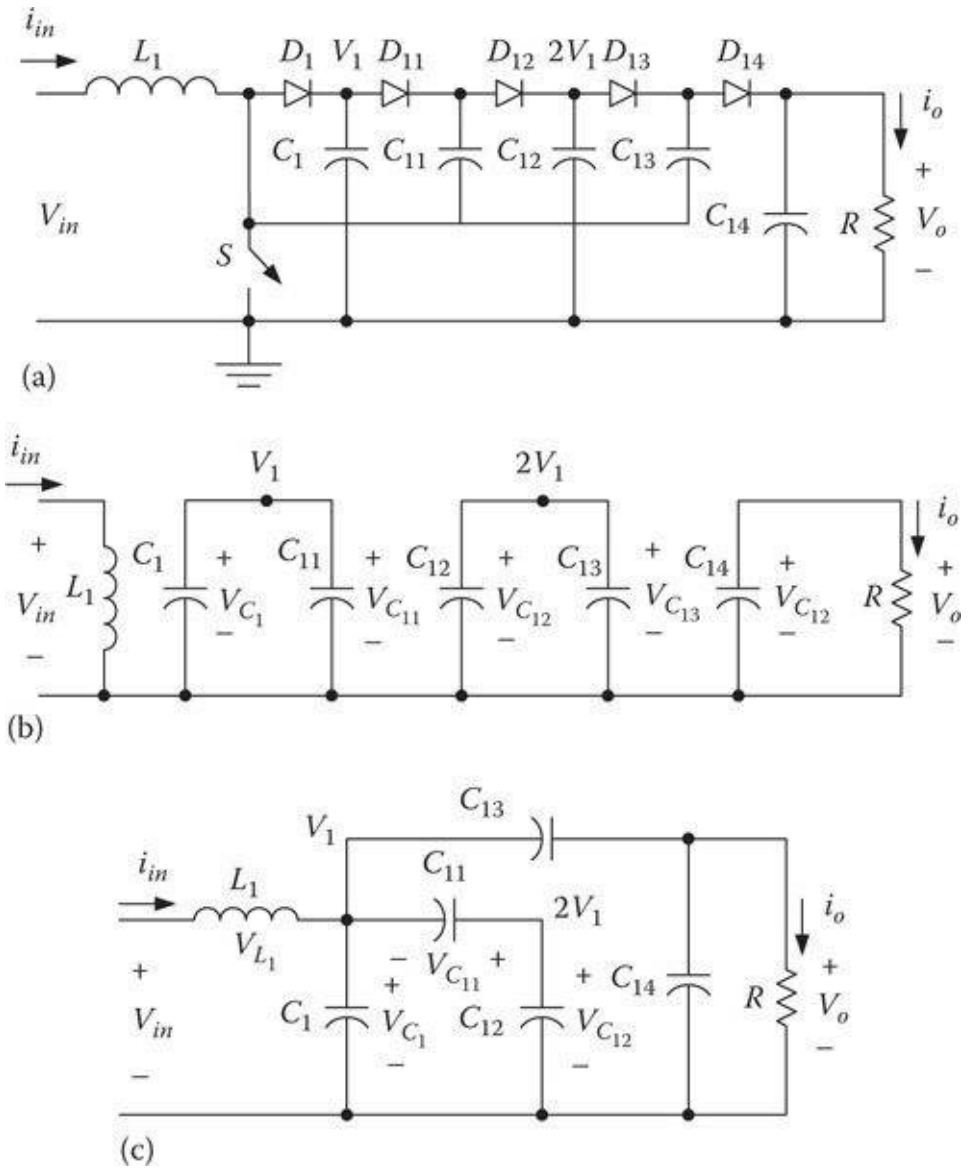


FIGURE 5.9
Elementary triple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3}{1-k} \tag{5.67}$$

5.5.2 Two-Stage Triple Boost Circuit

The two-stage triple boost circuit is derived from the two-stage double boost circuit by adding another DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 5.10.

As described in the previous section, the voltage V_1 across capacitors C_1 and C_{11} is $V_1 = (1/(1-k))V_{in}$. The voltage across capacitor C_{14} is charged to $3V_1$.

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The voltage across capacitors C_2 and C_{21} is charged to V_2, and the voltage across capacitors C_{22} and C_{23} is charged to $V_{C_{23}} = 2V_2$ The current flowing through inductor L_2 increases with voltage $3V_1$ during switch-on period kT and decreases with voltage $-(V_2 - 3V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{3V_1}{L_2} kT = \frac{V_2 - 3V_1}{L_2}(1-k)T \tag{5.68}$$

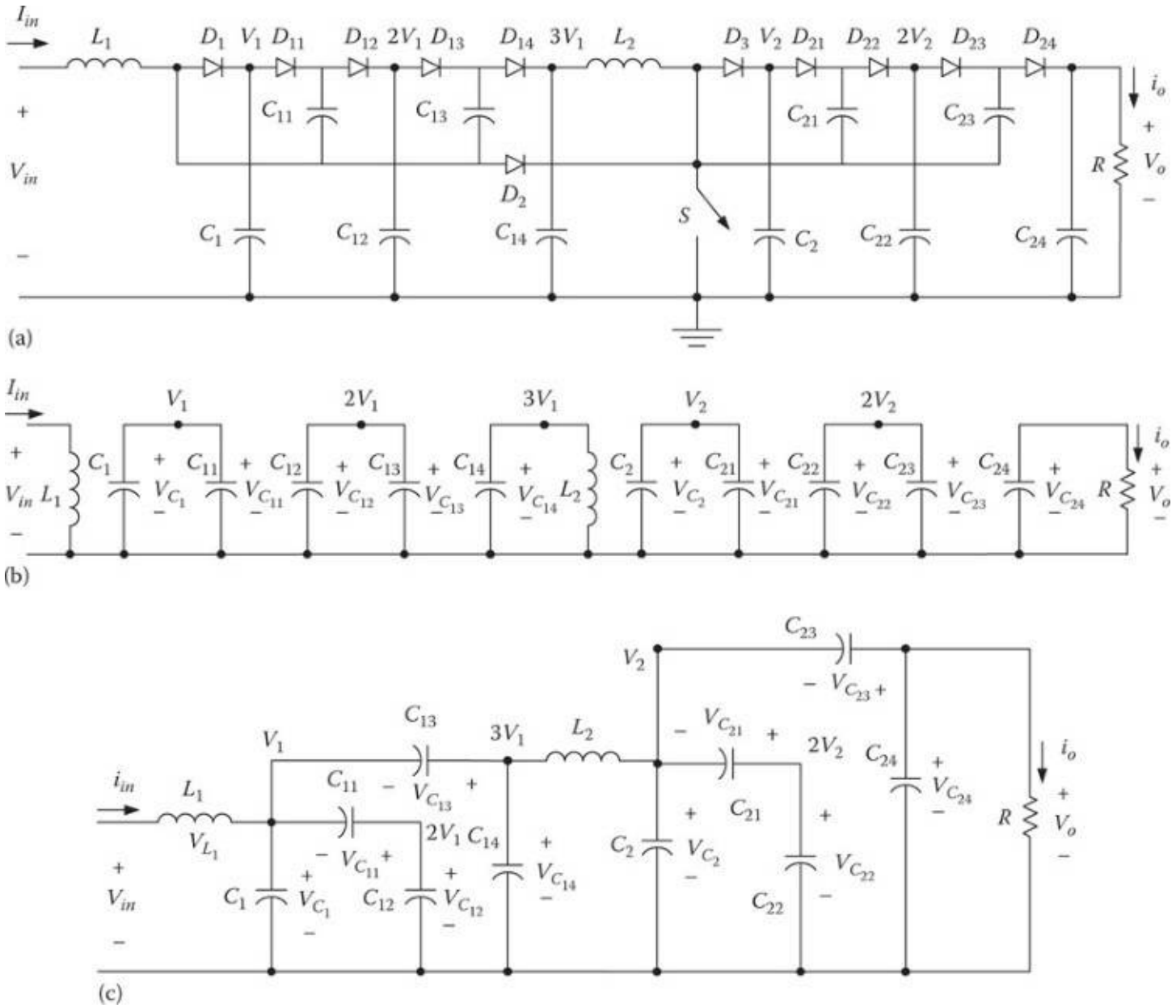


FIGURE 5.10
Two-stage triple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$V_2 = \frac{3}{1-k} V_1 = 3\left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.69}$$

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The output voltage is

$$V_o = V_{C_2} + V_{C_{23}} = 3V_2 = \left(\frac{3}{1-k}\right)^2 V_{in} \tag{5.70}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^2 \tag{5.71}$$

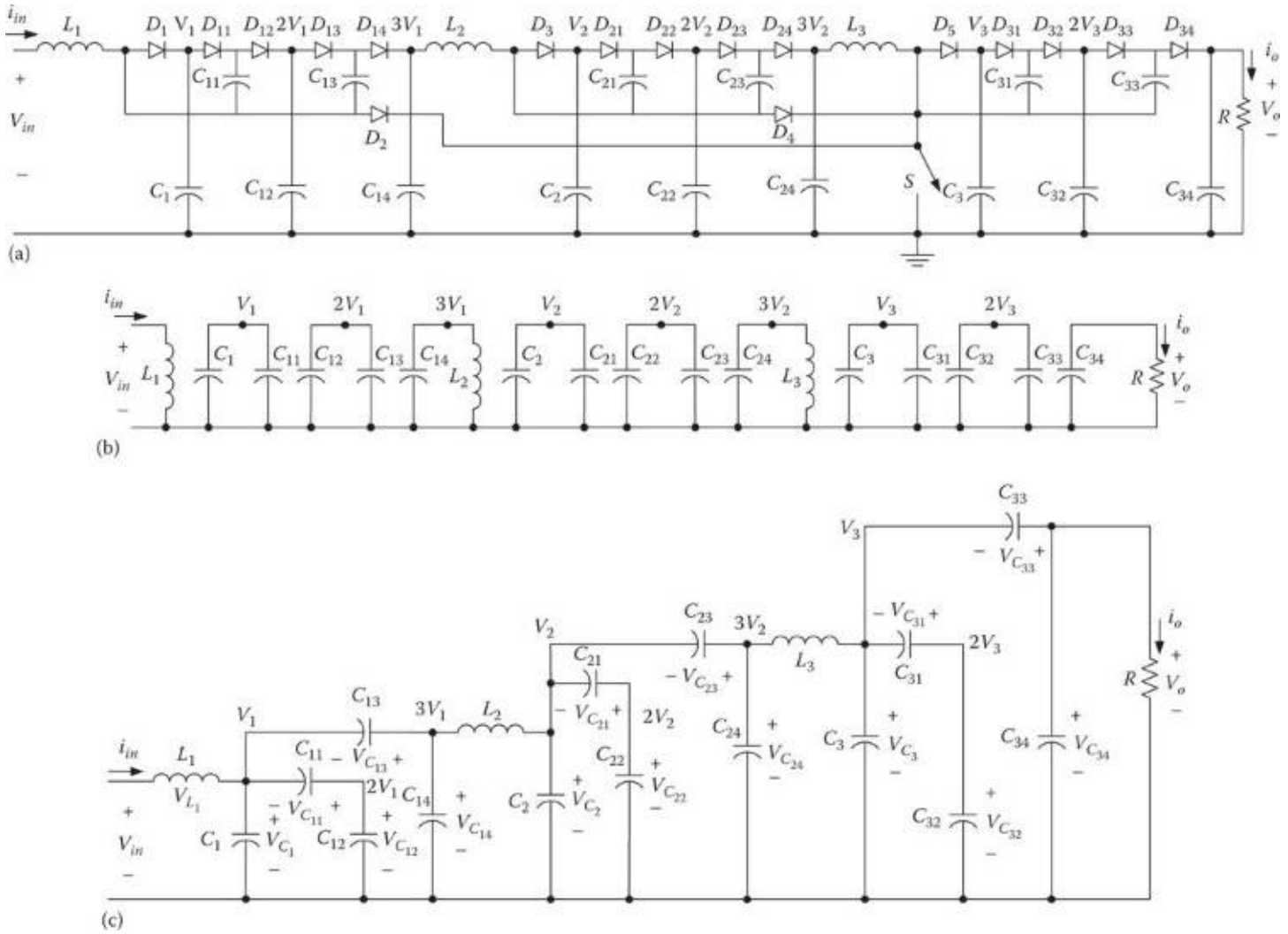


FIGURE 5.11
Three-stage triple boost circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \left(\frac{2}{1-k}\right)^2 I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_o} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \tag{5.72}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \tag{5.73}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{24}} = kT \frac{I_o}{C_{24}} = \frac{k}{fC_{24}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{24}} \tag{5.74}$$

5.5.3 Three-Stage Triple Boost Circuit

This circuit is derived from the three-stage double boost circuit by adding another DEC in each stage circuit. Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 5.11.

As described in the previous section, the voltage V_2 across capacitors C_2 and C_{11} is $V_2 = 3V_1 = 3/(1-k)V_{in}$, and the voltage across capacitor C_{24} is charged to $3V_2$.

The voltage across capacitors C_3 and C_{31} is charged to V_3, and the voltage across capacitors C_{32} and C_{33} is charged to $V_{C_{33}} = 2V_3$ The current flowing through inductor L_3 increases with voltage $3V_2$ during switch-on period kT and decreases with voltage $-(V_3 - 3V_2)$ during switch-off $(1-k)T$. Therefore, the ripple of the inductor current i_{L_3} is

$$\Delta i_{L_3} = \frac{3V_2}{L_3} kT = \frac{V_3 - 3V_2}{L_3}(1-k)T \tag{5.75}$$

and

$$V_3 = \frac{3}{1-k} V_2 = 9\left(\frac{1}{1-k}\right)^3 V_{in} \tag{5.76}$$

The output voltage is

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$$V_o = V_{C_3} + V_{C_{33}} = 3V_3 = \left(\frac{3}{1-k}\right)^3 V_{in} \tag{5.77}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^3 \tag{5.78}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{32}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{8}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2}{1-k} I_o$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{64L_1 I_o} = \frac{k(1-k)^6}{12^3} \frac{R}{fL_1} \tag{5.79}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{16L_2 I_o} = \frac{k(1-k)^4}{12^2} \frac{R}{fL_2} \tag{5.80}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)^2}{12} \frac{R}{fL_3} \tag{5.81}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{34}} = \frac{I_o(1-k)T}{C_{34}} = \frac{1-k}{fC_{34}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{34}} \tag{5.82}$$

5.5.4 Higher-Stage Triple Boost Circuit

Higher-stage triple boost circuits can be derived from the corresponding circuits of double boost series by adding another DEC in each stage circuit. For *n*th-stage additional circuit, the

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final output voltage is

$$V_o = \left(\frac{3}{1-k}\right)^n V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^n \tag{5.83}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{12^{(n-i+1)}} \frac{R}{fL_i} \tag{5.84}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n4}} \tag{5.85}$$

5.6 Multiple Series

All circuits of the multiple series of P/O cascaded boost converters are derived from the corresponding circuits of the main series by adding DEC multiple (j) times in each stage circuit. The first three stages of this series are shown in Figures 5.12, 5.13 and 5.14. For convenience to explain, they are called elementary multiple boost circuit, two-stage multiple boost circuit, and three-stage multiple boost circuit, respectively, and numbered as n = 1, 2, and 3.

5.6.1 Elementary Multiple Boost Circuit

From the construction principle, the elementary multiple boost circuit is derived from the elementary boost converter by adding DEC multiple (j) times in the circuit. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 5.12.

The voltage across capacitors C_1 and C_{11} is charged to V_1, and the voltage across capacitors C_{12} and C_{13} is charged to $V_{C_{13}} = 2V_1$ The voltage across capacitors $C_{1(2j-2)}$ and $C_{1(2j-1)}$ is charged to $V_{C_{1(2j-1)}} = jV_1$. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_1 - V_{in})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_1 - V_{in}}{L_1}(1-k)T \tag{5.86}$$

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$$V_1 = \frac{1}{1-k} V_{in} \tag{5.87}$$

The output voltage is

$$V_o = V_{C_1} + V_{C_{1(2j-1)}} = (1+j)V_1 = \frac{1+j}{1-k} V_{in} \tag{5.88}$$

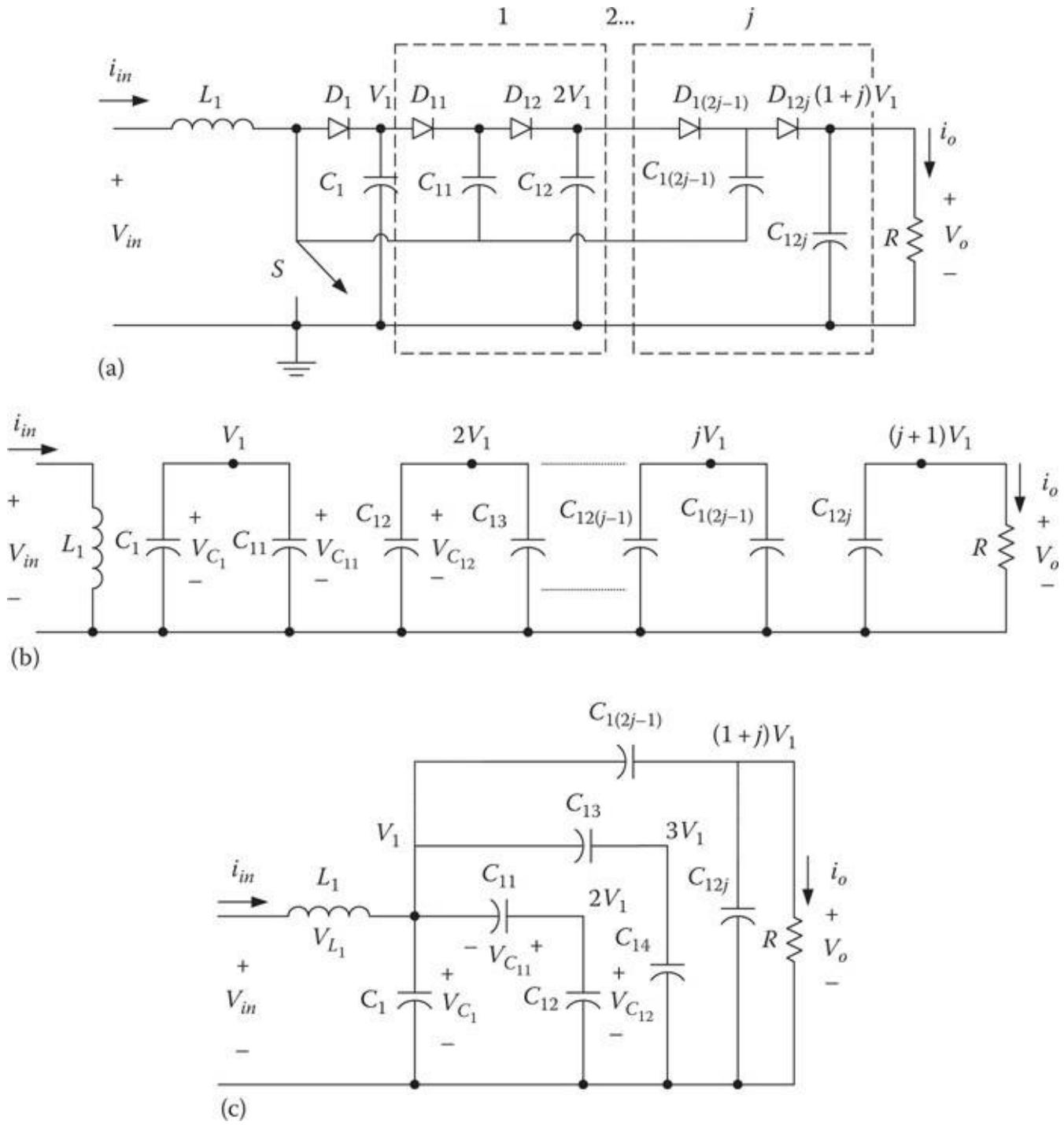


FIGURE 5.12
Cascaded boost multiple-double circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{1+j}{1-k} \tag{5.89}$$

5.6.2 Two-Stage Multiple Boost Circuit

The two-stage multiple boost circuit is derived from the two-stage boost circuit by adding multiple (j) DECs in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 5.13.

The voltage across capacitors C_1 and C_{11} is charged to $V_1 = 1/(1 - k)V_{in}$. The voltage across capacitor $C_{1(2j)}$ is charged to $(1 + j)V_1$.

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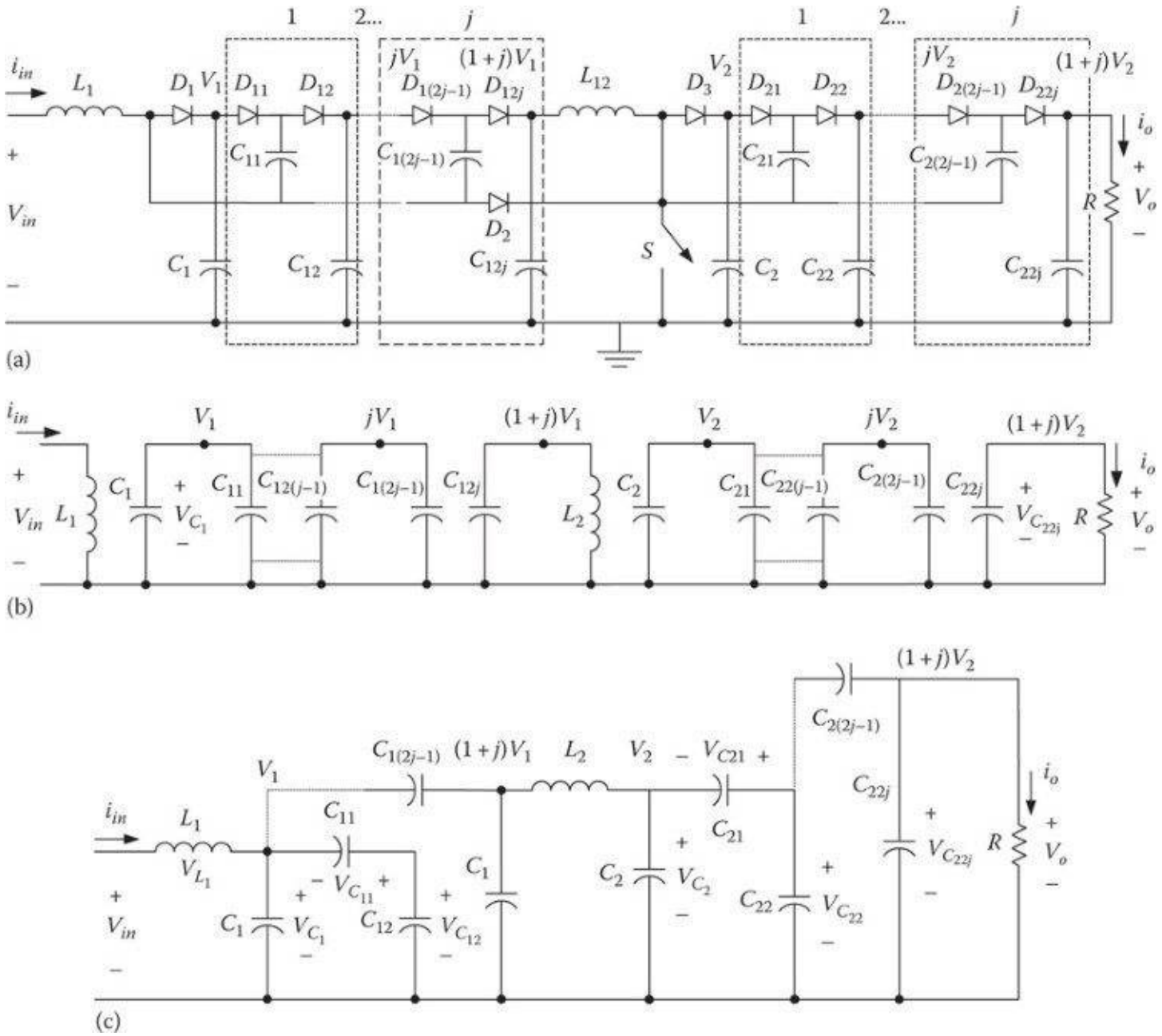


FIGURE 5.13
Two-stage boost multiple-double circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The current flowing through inductor L_2 increases with voltage $(1 + j)V_1$ during switch- on period kT and decreases with voltage $-[V_2 - (1 + j)V_1]$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L2} is

$$\Delta i_{L_2} = \frac{1+j}{L_2} kTV_1 = \frac{V_2 - (1+j)V_1}{L_2}(1-k)T \tag{5.90}$$

$$V_2 = \frac{1+j}{1-k} V_1 = (1+j)\left(\frac{1}{1-k}\right)^2 V_{in} \tag{5.91}$$

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The output voltage is

$$V_o = V_{C_1} + V_{C_{1(2j-1)}} = (1+j)V_2 = \left(\frac{1+j}{1-k}\right)^2 V_{in} \tag{5.92}$$

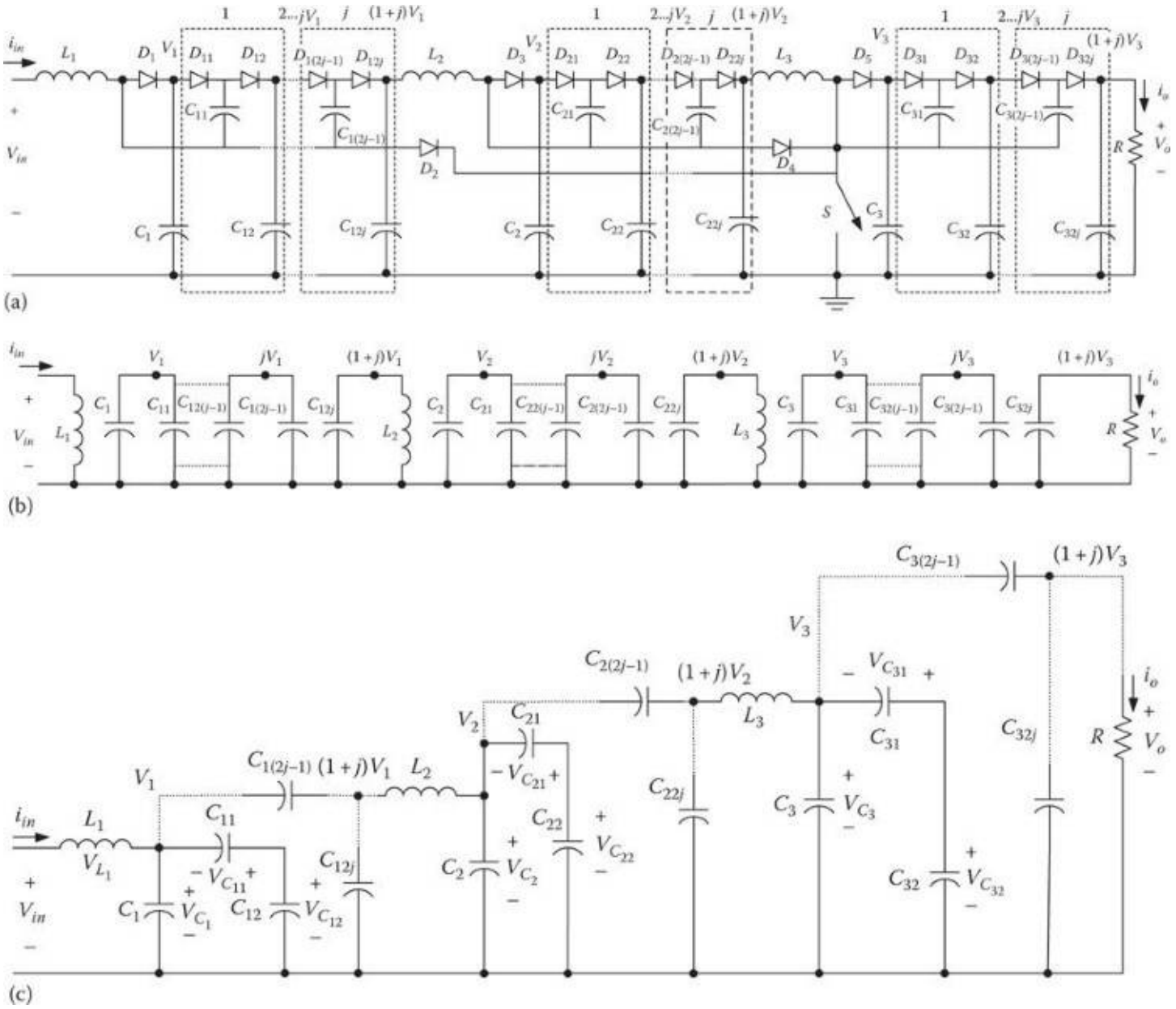


FIGURE 5.14
Three-stage boost multiple-double circuit. (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1+j}{1-k}\right)^2 \tag{5.93}$$

The ripple voltage of output voltage v_o is

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$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = kT\frac{I_o}{C_{22j}} = \frac{k}{fC_{22j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22j}} \tag{5.94}$$

5.6.3 Three-Stage Multiple Boost Circuit

This circuit is derived from the three-stage boost circuit by adding multiple (j) DECs in each stage circuit. Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 5.14.

The voltage across capacitors C_1 and C_{11} is charged to $V_1 = 1/(1 - k)V_{in}$. The voltage across capacitor $C_{1(2j)}$ is charged to $(1 + j)V_1$. The voltage V_2 across capacitors C_2 and $C_{2(2j)}$ is charged to $(1 + J)V_2$.

The current flowing through inductor L_3 increases with voltage $(1 + j)V_2$ during switch-on period kT and decreases with voltage $-[V_3 - (1 + j)V_2]$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_3} = \frac{1+j}{L_3}kTV_2 = \frac{V_3-(1+j)V_2}{L_3}(1-k)T \tag{5.95}$$

and

$$V_3 = \frac{(1+j)V_2}{(1-k)} = \frac{(1+j)^2}{(1-k)^3}V_{in} \tag{5.96}$$

The output voltage is

$$V_o = V_{C_3} + V_{C_{3(2j-1)}} = (1+j)V_3 = \left(\frac{1+j}{1-k}\right)^3 V_{in} \tag{5.97}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1+j}{1-k}\right)^3 \tag{5.98}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32j}} = kT\frac{I_o}{C_{32j}} = \frac{k}{fC_{32j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32j}} \tag{5.99}$$

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5.6.4 Higher-Stage Multiple Boost Circuit

The higher-stage multiple boost circuit is derived from the corresponding circuit of the main series by adding multiple (j) DECs in each stage circuit. For nth-stage additional circuit, the final output voltage is $V_o = ((1 + - j))/((1 + - k))^n V_{in}$.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1+j}{1-k}\right)^n \tag{5.100}$$

Analogously, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2j}} \tag{5.101}$$

5.7 Summary of Positive-Output Cascaded Boost Converters

All circuits of P/O cascaded boost converters as a family can be shown in Figure 5.15 as the family tree. From the analysis of previous two sections, we have the common formula to calculate the output voltage:

$$V_o = \begin{cases} \left(\frac{1}{1-k}\right)^n V_{in} & main_series \\ 2*\left(\frac{1}{1-k}\right)^n V_{in} & additional_series \\ \left(\frac{2}{1-k}\right)^n V_{in} & double_series \\ \left(\frac{3}{1-k}\right)^n V_{in} & triple_series \\ \left(\frac{j+1}{1-k}\right)^n V_{in} & multiple(j)_series \end{cases} \tag{5.102}$$

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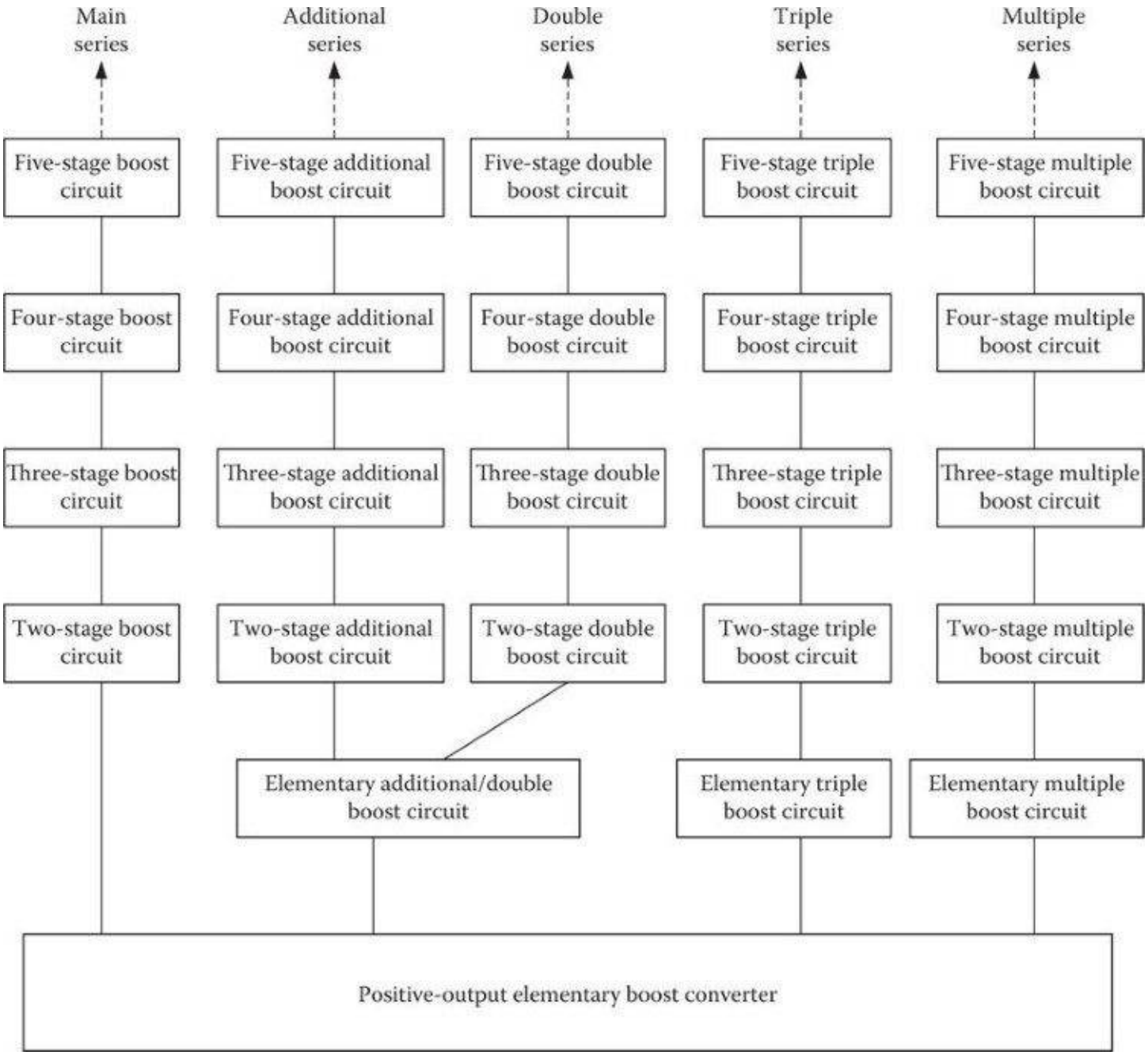


FIGURE 5.15
The family of positive-output cascaded boost converters.

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \begin{cases} \left(\frac{1}{1-k}\right)^n & main_series \\ 2*\left(\frac{1}{1-k}\right)^n & additional_series \\ \left(\frac{2}{1-k}\right)^n & double_series \\ \left(\frac{3}{1-k}\right)^n & triple_series \\ \left(\frac{j+1}{1-k}\right)^n & multiple(j)_series \end{cases} \tag{5.103}$$

In order to show the advantages of the P/O cascaded boost converters, we compare their voltage transfer gains to that of

$$\text{Buck converter} \quad G = \frac{V_o}{V_{in}} = k$$

$$\text{Forwardconverter } G = \frac{V_o}{V_{in}} = kN \ (N \text{ is the transformer turns ratio})$$

$$\text{Cúk converter} \quad G = \frac{V_o}{V_{in}} = \frac{k}{(1-k)}$$

$$\text{Flybackconverter } G = \frac{V_o}{V_{in}} = \frac{k}{(1-k)} N \ (N \text{ isthe transformerturns ratio})$$

$$\text{Boost converter} \quad G = \frac{V_o}{V_{in}} = \frac{1}{(1-k)}$$

$$\text{P/O Luo-converters} \quad G = \frac{V_o}{V_{in}} = \frac{n}{1-k} \tag{5.104}$$

If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in Table 5.1.

If the conduction duty k is 0.5, the output voltage transfer gains are listed in Table 5.2.

If the conduction duty k is 0.8, the output voltage transfer gains are listed in Table 5.3.

TABLE 5.1
Voltage Transfer Gains of Converters in the Condition $k = 0.2$

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Stage No. (n)	1	2	3	4	5	n
Buck converter				0.2		
Forward converter				0.2N (N is the transformer turns ratio)		
Cuk converter				0.25		
Flyback converter				0.25N (N is the transformer turns ratio)		
Boost converter				1.25		
Positive-output Luo-converters	1.25	2.5	3.75	5	6.25	1.25^n
Positive-output cascaded boost converters—main series	1.25	1.563	1.953	2.441	3.052	1.25^n
Positive-output cascaded boost converters—additional series	2.5	2.5	3.125	4.882	6.104	$2*1.25^n$
Positive-output cascaded boost converters—double series	2.5	6.25	15.625	39.063	97.66	$(2*1.25)^n$
Positive-output cascaded boost converters—triple series	5	25	125	625	3,125	$(4*1.25)^n$
Positive-output cascaded boost (j = 3) converters—multiple series	10	100	1000	10,000	100,000	$(8*1.25)^n$

TABLE 5.2
Voltage Transfer Gains of Converters in the Condition k = 0.5

Stage No. (n)	1	2	3	4	5	n
Buck converter				0.5		
Forward converter				0.5N (N is the transformer turns ratio)		
Cuk converter				1		
Flyback converter				N (N is the transformer turns ratio)		
Boost converter				2		
Positive-output Luo-converters	2	4	6	8	10	2^n
Positive-output cascaded boost converters—main series	2	4	8	16	32	2^n
Positive-output cascaded boost converters—additional series	4	8	16	32	64	$2*2^n$
Positive-output cascaded boost converters—double series	4	16	64	256	1,024	$(2*2)^n$
Positive-output cascaded boost converters—triple series	8	64	512	4,096	32,768	$(4*2)^n$
Positive-output cascaded boost (j = 3) converters—multiple series	16	256	4096	65,536	10^6	$(8*2)^n$

TABLE 5.3
Voltage Transfer Gains of Converters in the Condition k = 0.8

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Stage No. (n)	1	2	3	4	5	n
Buck converter	0.8					
Forward converter	0.8N (N is the transformer turns ratio)					
Cuk converter	4					
Flyback converter	4N (N is the transformer turns ratio)					
Boost converter	5					
Positive-output Luo-converters	5	10	15	20	25	5^n
Positive-output cascaded boost converters—main series	5	25	125	625	3,125	5^n
Positive-output cascaded boost converters—additional series	10	50	250	1,250	6,250	$2*5^n$
Positive-output cascaded boost converters—double series	10	100	1000	10,000	100,000	$(2*5)^n$
Positive-output cascaded boost converters—triple series	20	400	8000	160,000	$32*10^5$	$(4*5)^n$
Positive-output cascaded boost converters—multiple series	40	1600	$64*10^3$	$256*10^4$	10^8	$(8*5)^n$

5.8 Simulation and Experimental Results

5.8.1 Simulation Results of a Three-Stage Boost Circuit

To verify the design and calculation results, the PSpice simulation package was applied to a three-stage boost converter. Choose V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all $C_1 - C_8$ = 2 μF and R = 30 kΩ, and using k = 0.7 and f = 100 kHz. The obtained voltage values V_1, V_2, and V_o of a triple-lift circuit are 66, 194, and 659 V, respectively, and the inductor current waveforms are i_{L_1} (its average value $I_{L_1} = 618$ mA), i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 5.16. The voltage values match the calculated results.

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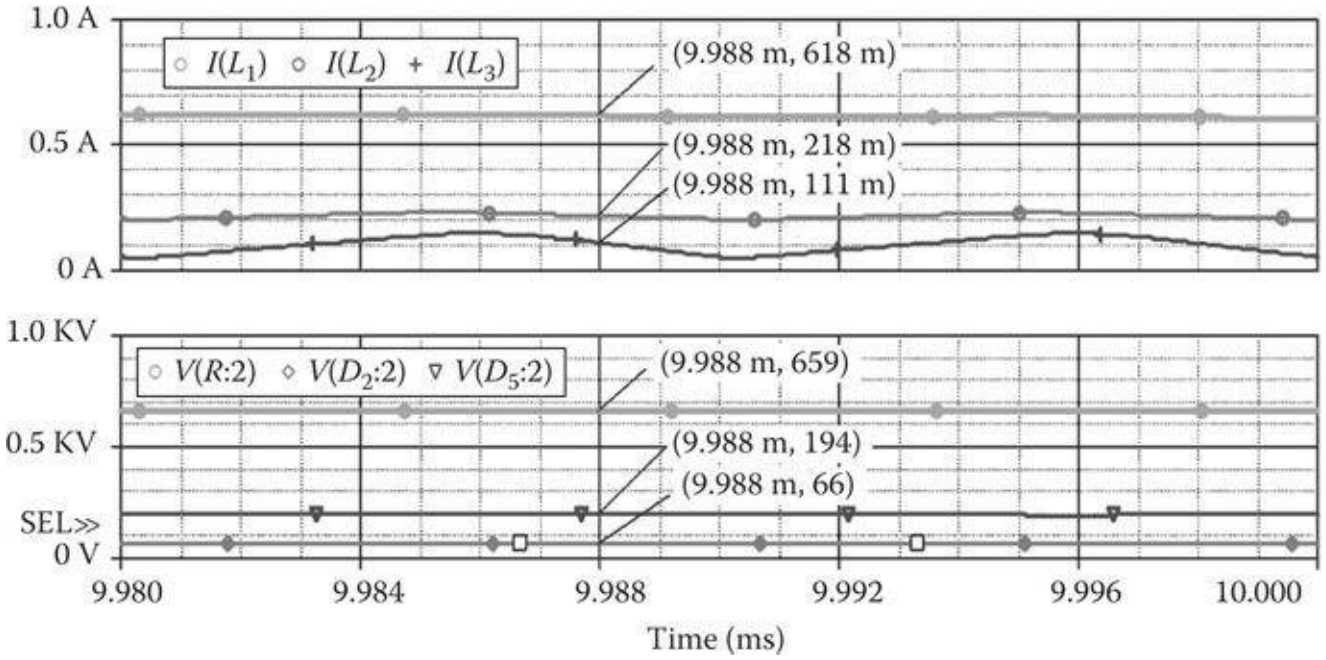


FIGURE 5.16
The simulation results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

5.8.2 Experimental Results of a Three-Stage Boost Circuit

A test rig was constructed to verify the design and calculation results and compared with PSpice simulation results. The test conditions are still $V_{in} = 20$ V, $L_1 = L_2 = L_3 = 10$ mH, all $C_1 - C_8 = 2$ μF and $R = 30$ kΩ, and $k = 0.7$ and $f = 100$ kHz. The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. The measured values of the output voltage and first inductor current were obtained from a three-stage boost converter.

After careful measurement, we obtained the current value of $I_{L_1} = 0.62$ A (shown in Channel 1 with 1 A/Div) and the voltage value of $V_o = 660$ V (shown in Channel 2 with 200 V/Div). The experimental results (current and voltage values) in Figure 5.17 match the calculated and simulation results, which are $I_{L_1} = 0.618$ A and $V_o = 659$ V shown in Figure 5.16.

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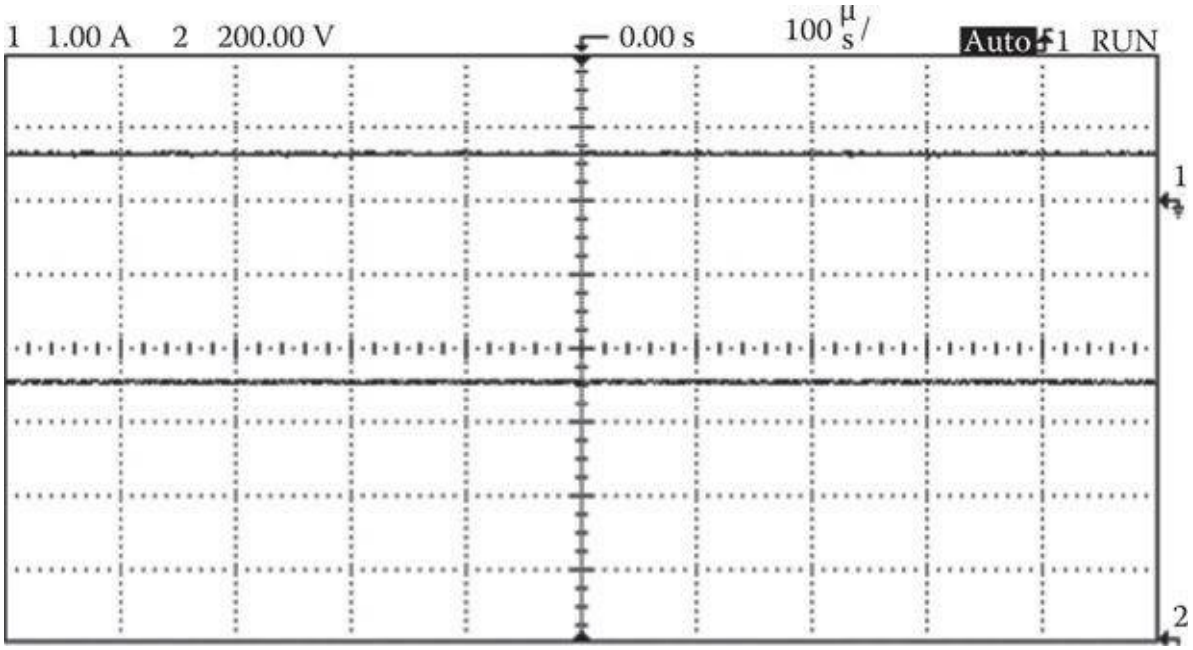


FIGURE 5.17
The experimental results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

TABLE 5.4
Comparison of Simulation and Experimental Results of a Triple-Lift Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_o (V)	P_o (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

5.8.3 Efficiency Comparison of Simulation and Experimental Results

These circuits enhanced the voltage transfer gain successfully and efficiently. Particularly, the efficiency of the tested circuits is 78%, which is good for high-voltage output equipment. Comparison of the simulation and experimental results experimental results is shown in Table 5.4. All results are well identified to each other.

5.8.4 Transient Process

Usually, there is high inrush current during the first power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick taking only a few milliseconds.

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6

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Negative-Output Cascaded Boost Converters

6.1 Introduction

This chapter introduces negative-output (N/O) cascaded boost converters. Just as with positive-output cascaded boost converters, these converters use the super-lift technique. There are several subseries:

- Main series: Each circuit of the main series has one switch S, n inductors, n capacitors, and $(2n - 1)$ diodes.
- Additional series: Each circuit of the additional series has one switch S, n inductors, $(n + 2)$ capacitors, and $(2n + 1)$ diodes.
- Double series: Each circuit of the double series has one switch S, n inductors, $3n$ capacitors, and $(3n - 1)$ diodes.
- Triple series: Each circuit of the triple series has one switch S, n inductors, $5n$ capacitors, and $(5n - 1)$ diodes.
- Multiple series: Multiple series circuits have one switch S and a higher number of capacitors and diodes.

The conduction duty ratio is k, the switching frequency is f, the switching period is $T = 1/f$, and the load is resistive load R. The input voltage and current are V_{in} and I_{in}, and the output voltage and current are V_o and I_o. Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_o \times I_o$. The voltage transfer gain is G: $G = V_o/V_{in}$.

6.2 Main Series

The first three stages of the main series of N/O cascaded boost converters are shown in Figures 6.1, 6.2 and 6.3. For convenience, they are called elementary boost converter, two-stage boost circuit, and three-stage boost circuit, respectively, and numbered as $n = 1$, 2, and 3.

6.2.1 N/O Elementary Boost Circuit

The N/O elementary boost converter and its equivalent circuits during switch-on and switch-off are shown in Figure 6.1.

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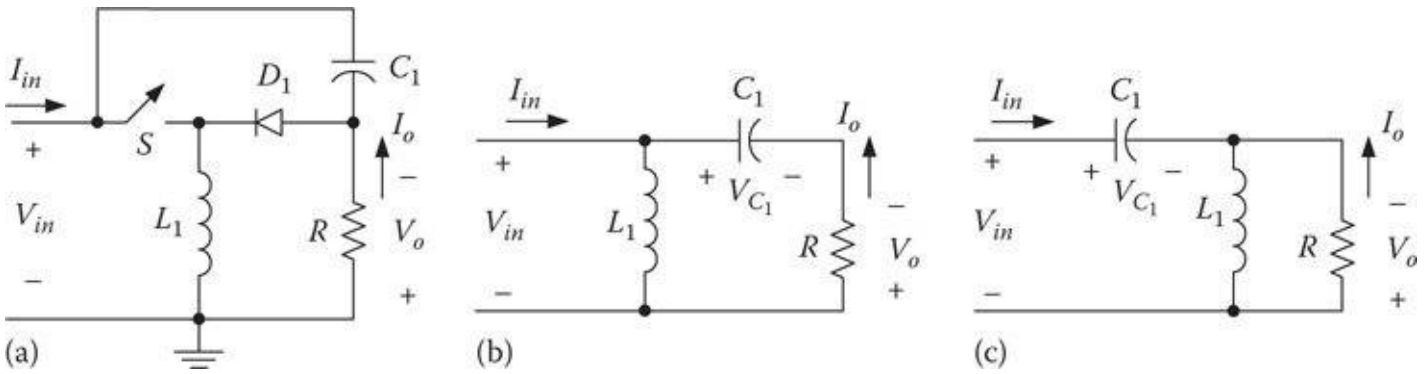


FIGURE 6.1
Elementary boost converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

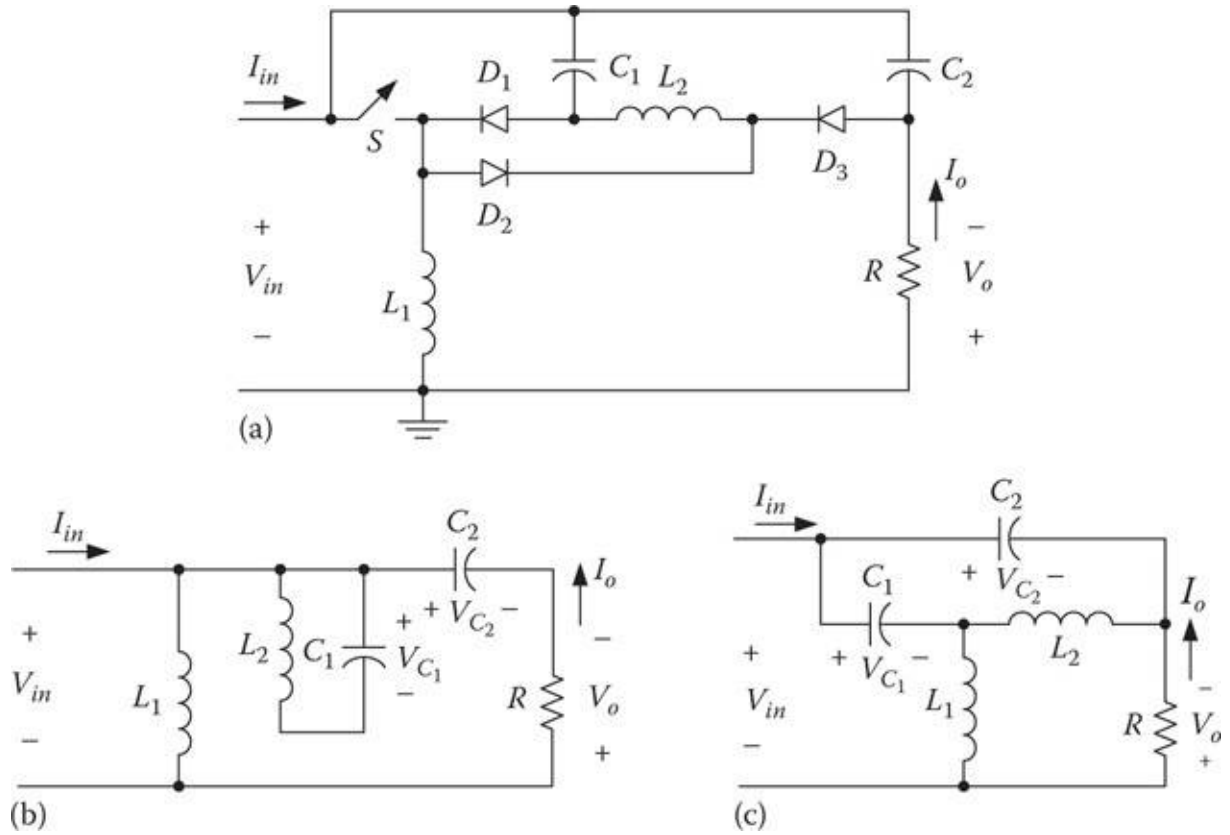


FIGURE 6.2
Two-stage boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage across capacitor C_1 is charged to V_{C_1}. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_{C_1} - V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT = \frac{V_{C_1} - V_{in}}{L_1} (1-k)T \tag{6.1}$$

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$$V_{C_1} = \frac{1}{1-k} V_{in}$$

$$V_o = V_{C_1} - V_{in} = \frac{k}{1-k} V_{in} \tag{6.2}$$

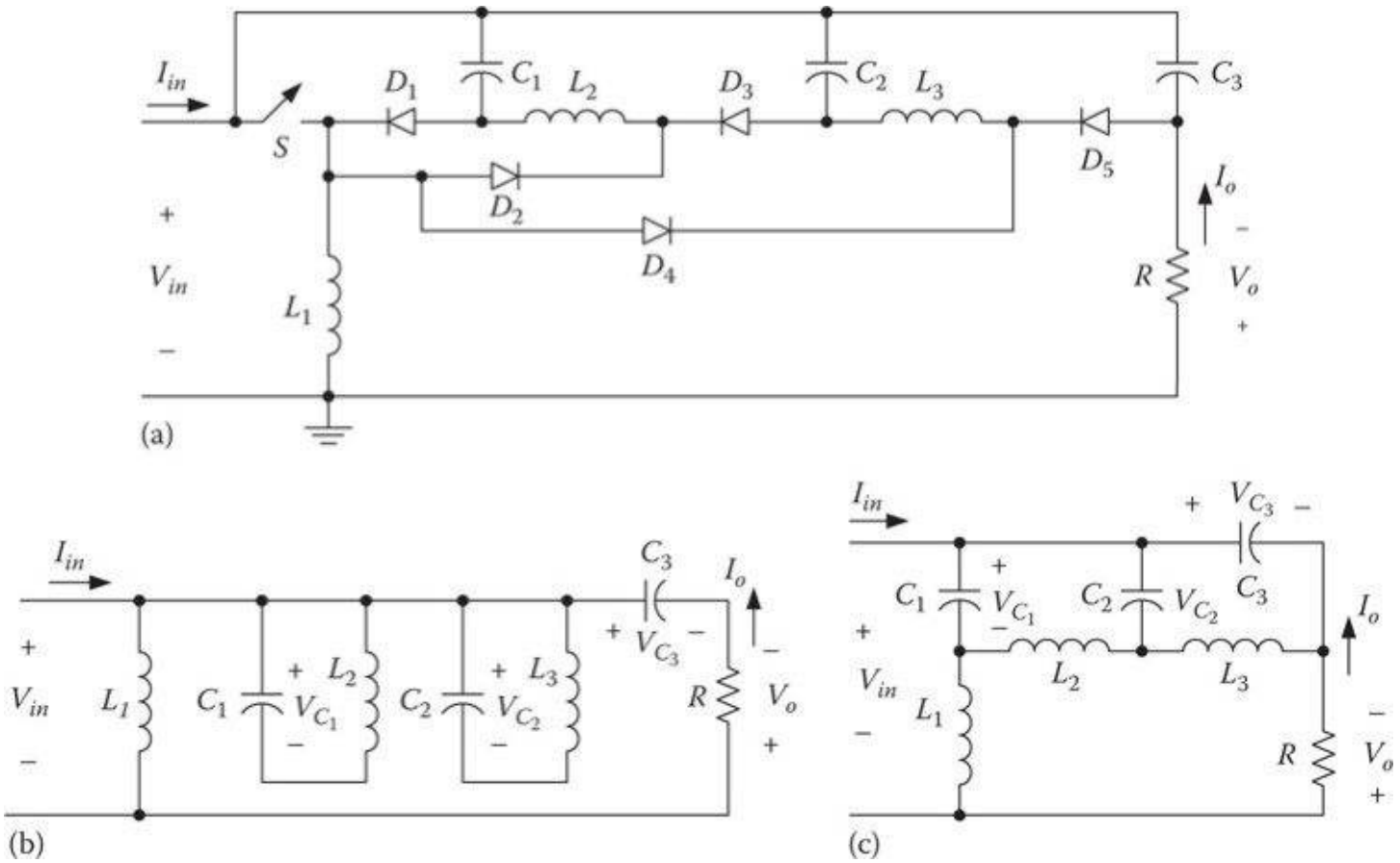


FIGURE 6.3
Three-stage boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{1}{1-k} - 1 = \frac{k}{1-k} \tag{6.3}$$

$$I_{in} = \frac{k}{1-k} I_o$$

The inductor average current is

$$I_{L_1} = \frac{V_o}{(1-k)R} = I_{in} + I_o \tag{6.4}$$

The variation ratio of current i_{L_1} through inductor L_1 is

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$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{kTV_{in}}{2L_1V_o/(1-k)R} = \frac{k(1-k)}{2G}\frac{R}{fL_1} = \frac{(1-k)^2}{2}\frac{R}{fL_1} \tag{6.5}$$

Usually, ξ_1 is small (much lower than unity), and it means this converter works in the continuous mode. The charge variation across the capacitor C_1 is

$$\Delta Q = kTI_o$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_1} = kT\frac{I_o}{C_1} = \frac{k}{fC_1}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_1} \tag{6.6}$$

Usually, R is in kΩ, f in 10 kHz, and C_1 in μF; this ripple is smaller than 1%.

6.2.2 N/O Two-Stage Boost Circuit

The N/O two-stage boost circuit is derived from the elementary boost converter by adding the parts (L_2–D_2–D_3–C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.2.

The voltage across capacitor C_1 is charged to V_1. As described in the previous section, the voltage V_1 across capacitor C_1 is $V_1 = 1/(1 - k)V_{in}$.

The voltage across capacitor C_2 is charged to V_{C_2}. The current flowing through inductor L_2 increases with voltage V_1 during switch-on period kT and decreases with voltage $-(V_{c2} - V_1)$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_1}{L_2}kT = \frac{V_{C_2} - V_1}{L_2}(1-k)T \tag{6.7}$$

$$V_{C_2} = \frac{1}{1-k}V_1 = \left(\frac{1}{1-k}\right)^2 V_{in}$$

$$V_o = V_{C_2} - V_{in} = \left[\left(\frac{1}{1-k}\right)^2 - 1\right]V_{in} \tag{6.8}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^2 - 1 \tag{6.9}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_o}{(1-k)^2}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{2L_1 I_o} = \frac{k(1-k)^4}{2} \frac{R}{fL_1} \tag{6.10}$$

the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{2L_2 I_o} = \frac{k(1-k)^2}{2} \frac{R}{fL_2} \tag{6.11}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_2} \tag{6.12}$$

6.2.3 N/O Three-Stage Boost Circuit

The N/O three-stage boost circuit is derived from the two-stage boost circuit by double adding the parts (L_2–D_2–D_3–C_2). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.3.

The voltage across capacitor C_1 is charged to V_1. As described previously, the voltage V_{C_1} across capacitor C_1 is $V_{C_1} = 1/(1-k)V_{in}$, and the voltage V_{C_2} across capacitor C_2 is $V_{C_2} = (1/(1-k))^2 V_{in}$.

The voltage across capacitor C_3 is charged to v_o. The current flowing through inductor L_3 increases with voltage V_{C_2} during switch-on period kT and decreases with voltage $-(V_{C_3} - V_{C_2})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_3} is

$$\Delta i_{L_3} = \frac{V_{C_2}}{L_3} kT = \frac{V_{C_3} - V_{C_2}}{L_3} (1-k)T \tag{6.13}$$

$$V_{C_3} = \frac{1}{1-k} V_{C_2} = \left(\frac{1}{1-k}\right)^2 V_{C_1} = \left(\frac{1}{1-k}\right)^3 V_{in}$$

$$V_o = V_{C_3} - V_{in} = \left[\left(\frac{1}{1-k}\right)^3 - 1\right] V_{in} \tag{6.14}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^3 - 1 \tag{6.15}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{I_o}{(1-k)^3}$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{I_o}{(1-k)^2}$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{2L_1 I_o} = \frac{k(1-k)^6}{2} \frac{R}{fL_1} \tag{6.16}$$

the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{2L_2 I_o} = \frac{k(1-k)^4}{2} \frac{R}{fL_2} \tag{6.17}$$

the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{2L_3 I_o} = \frac{k(1-k)^2}{2} \frac{R}{fL_3} \tag{6.18}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_3} \tag{6.19}$$

6.2.4 N/O Higher-Stage Boost Circuit

An N/O higher-stage boost circuit can be designed by multiple repetition of the parts (L_2–D_2–D_3–C_2). For nth-stage boost circuit, the final output voltage across capacitor C_n is

$$V_o = \left[\left(\frac{1}{1-k}\right)^n - 1\right] V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{1}{1-k}\right)^n - 1 \tag{6.20}$$

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the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2}\frac{R}{fL_i} \tag{6.21}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_n} \tag{6.22}$$

6.3 Additional Series

All circuits of the additional series of N/O cascaded boost converters are derived from the corresponding circuits of the main series by adding a double/enhanced circuit (DEC).

The first three stages of this series are shown in Figures 6.4, 6.5 and 6.6. For convenience, they are called elementary additional boost circuit, two-stage additional boost circuit, and three-stage additional boost circuit, respectively, and numbered as n = 1, 2, and 3.

6.3.1 N/O Elementary Additional Boost Circuit

This N/O elementary boost additional circuit is derived from the N/O elementary boost converter by adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.4.

The voltage across capacitors C_1 and C_{11} is charged to V_{C_1} and the voltage across capacitor C_{12} is charged to $V_{C_{12}} = 2V_{C_1}$. The current i_{L_1} flowing through inductor L_1 increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_{c1} - V_{in})$ during switch-off period $(1 - k)T$. Therefore,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1}kT = \frac{V_{C_1} - V_{in}}{L_1}(1-k)T \tag{6.23}$$

$$V_{C_1} = \frac{1}{1-k}V_{in}$$

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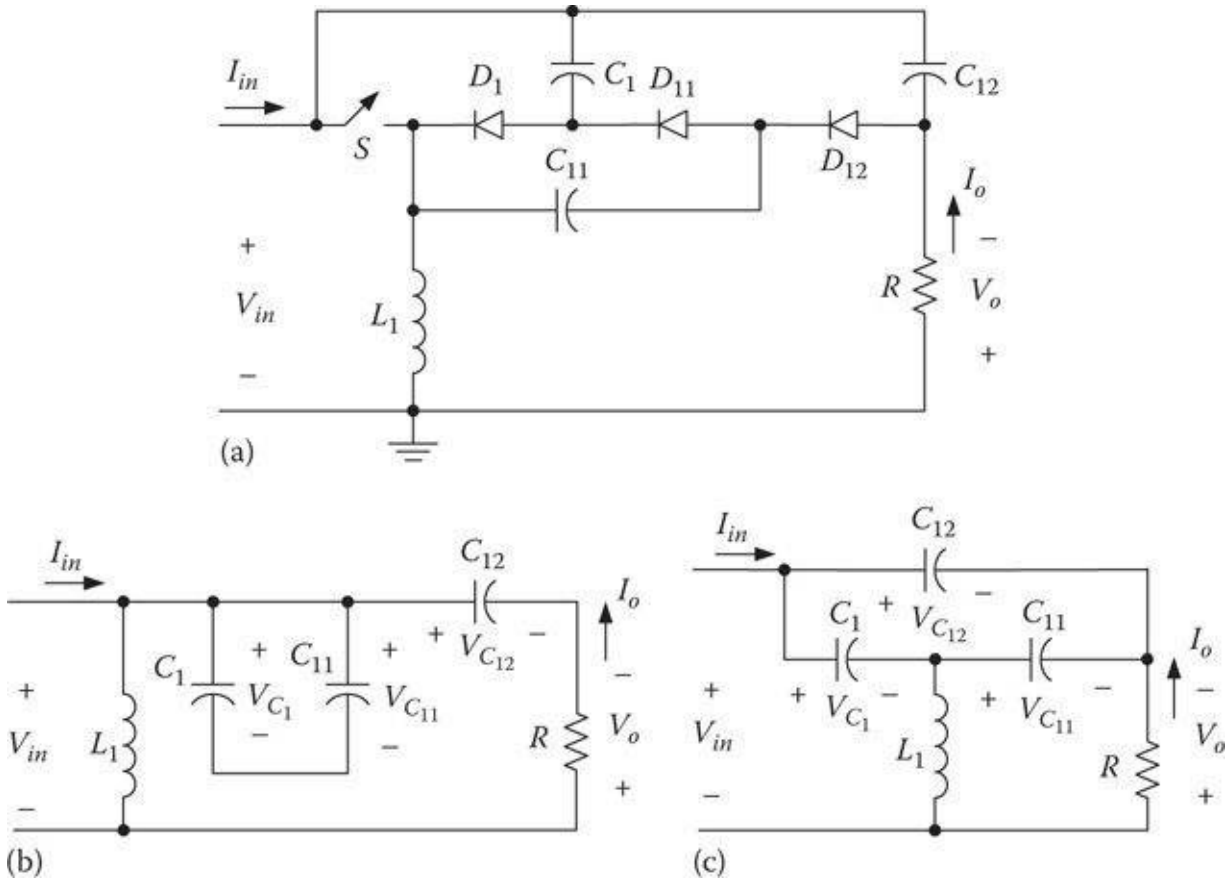


FIGURE 6.4
Elementary boost additional (double) circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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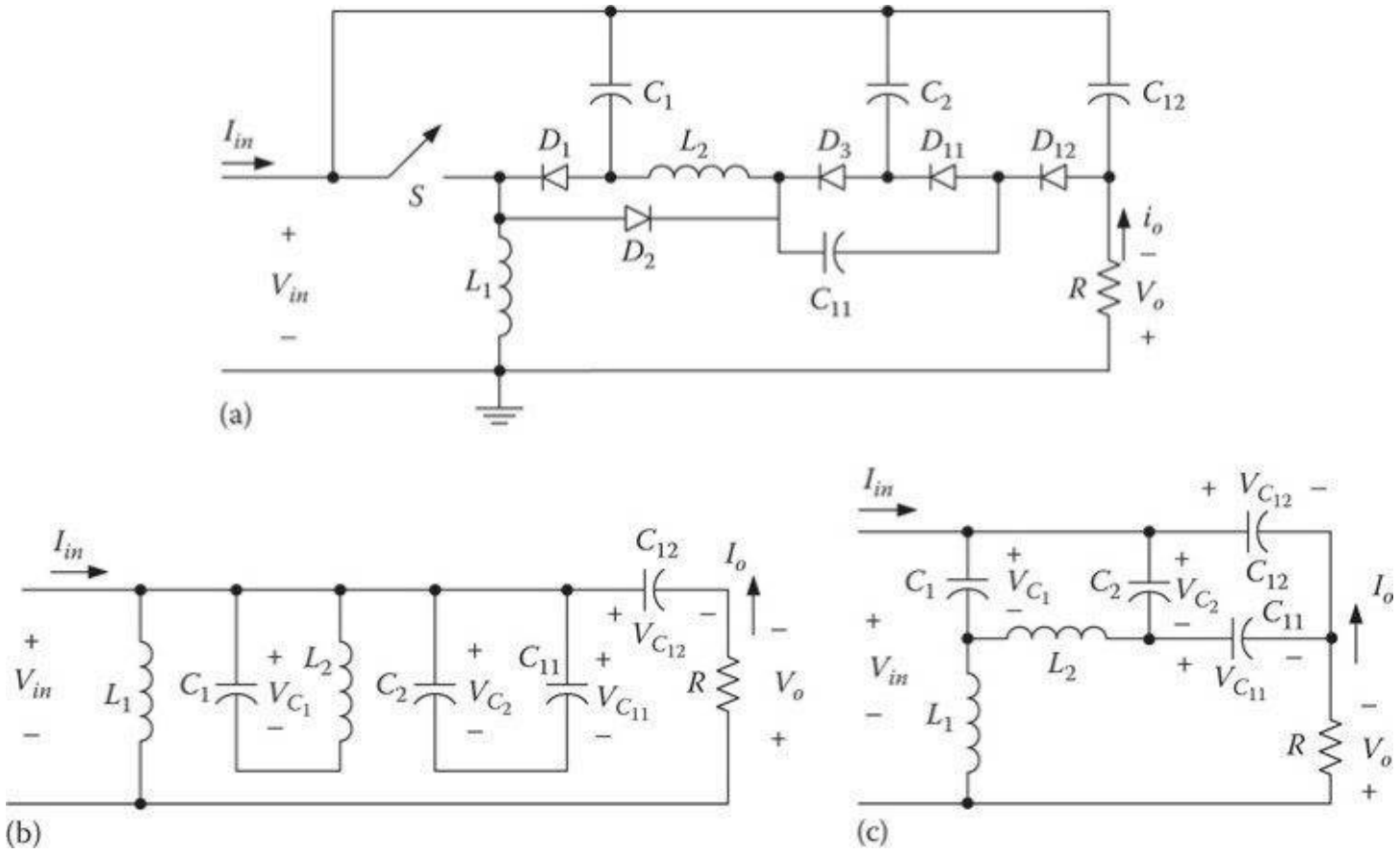


FIGURE 6.5
Two-stage additional boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage V_{C12} is

$$V_{C_{12}} = 2V_{C_1} = \frac{2}{1-k} V_{in} \tag{6.24}$$

The output voltage is

$$V_o = V_{C_{12}} - V_{in} = \left[\frac{2}{1-k} - 1\right] V_{in} \tag{6.25}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2}{1-k} - 1 \tag{6.26}$$

The variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)TV_{in}}{4L_1 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_1} \tag{6.27}$$

The ripple voltage of output voltage v_o is

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$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

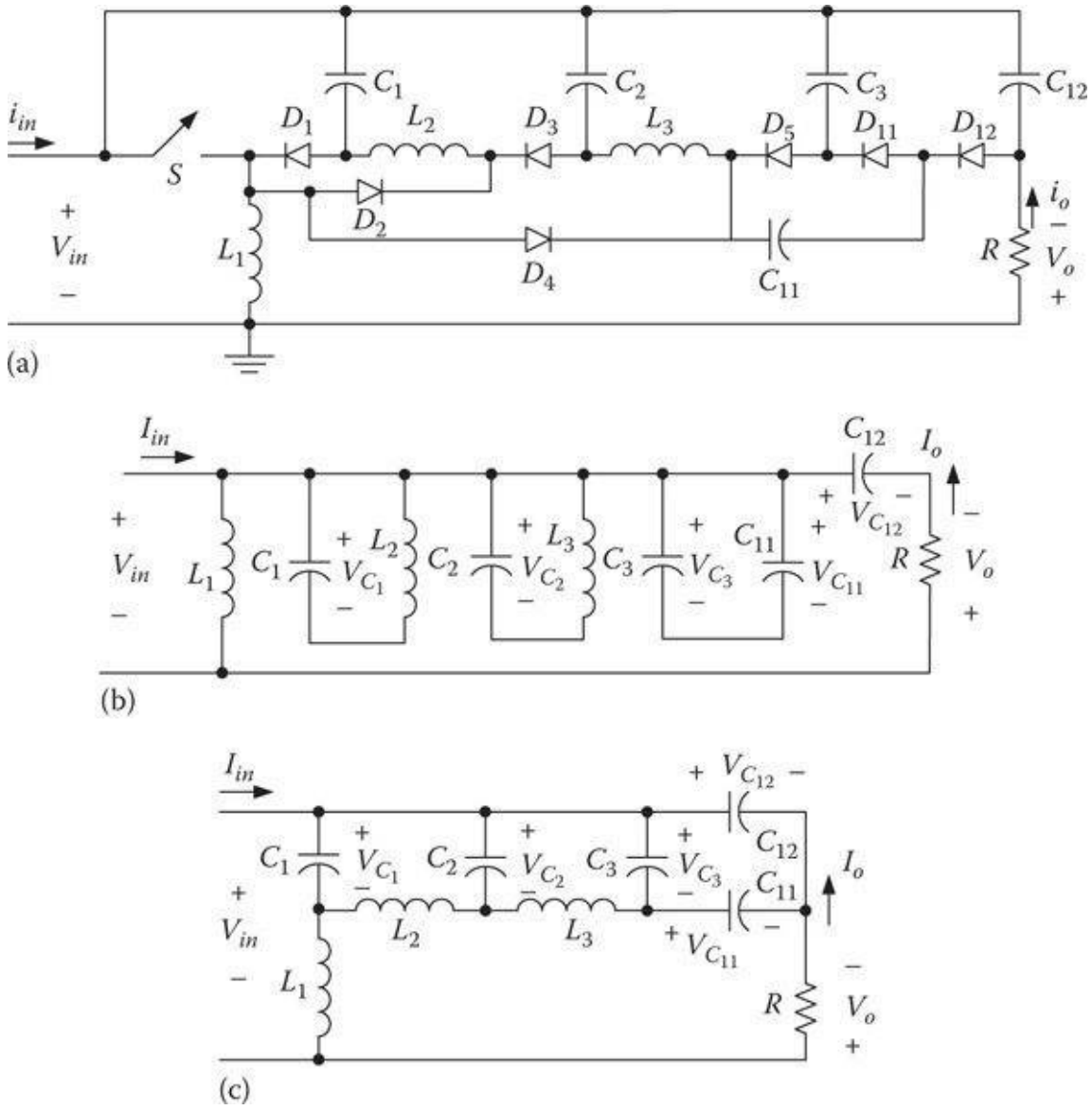


FIGURE 6.6
Three-stage additional boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{6.28}$$

6.3.2 N/O Two-Stage Additional Boost Circuit

The N/O two-stage additional boost circuit is derived from the N/O two-stage boost circuit by adding a DEC. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.5.

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The voltage across capacitor C_1 is charged to V_{C_1}. As described in the previous section, the voltage V_{C_1} across capacitor C_1 is $V_{C_1} = 1/(1-k)V_{in}$.

The voltage across capacitors C_2 and capacitor C_{11} is charged to V_{C_2}, and the voltage across capacitor C_{12} is charged to $V_{C_{12}}$. The current flowing through inductor L_2 increases with voltage V_{C_1} during switch-on period kT and decreases with voltage $-(V_{C_2} - V_{C_1})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_{C_1}}{L_2} kT = \frac{V_{C_2} - V_{C_1}}{L_2}(1-k)T \tag{6.29}$$

$$V_{C_2} = \frac{1}{1-k} V_{C_1} = \left(\frac{1}{1-k}\right)^2 V_{in} \tag{6.30}$$

$$V_{C_{12}} = 2V_{C_2} = \frac{2}{1-k} V_{C_1} = 2\left(\frac{1}{1-k}\right)^2 V_{in}$$

The output voltage is

$$V_o = V_{C_{12}} - V_{in} = \left[2\left(\frac{1}{1-k}\right)^2 - 1\right] V_{in} \tag{6.31}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^2 - 1 \tag{6.32}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{2}{(1-k)^2} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{4L_1 I_o} = \frac{k(1-k)^4}{8} \frac{R}{fL_1} \tag{6.33}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \tag{6.34}$$

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The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT\frac{I_o}{C_{12}} = \frac{k}{fC_{12}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{1-k}{2RfC_{12}} \tag{6.35}$$

6.3.3 N/O Three-Stage Additional Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.6.

The voltage across capacitor C_1 is charged to V_{C_1}. As described previously, the voltage V_{C_1} across capacitor C_1 is $V_{C_1} = 1/(1-k)V_{in}$, and the voltage V_2 across capacitor C_2 is $V_{C_2} = (1/(1-k))^2 V_{in}$.

The voltage across capacitors C_3 and capacitor C_{11} is charged to V_{C_3}. The voltage across capacitor C_{12} is charged to $V_{C_{12}}$. The current flowing through inductor L_3 increases with voltage V_{C_2} during switch-on period kT and decreases with voltage $-(V_{C_3} - V_{C_2})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_3} = \frac{V_{C_2}}{L_3}kT = \frac{V_{C_3} - V_{C_2}}{L_3}(1-k)T \tag{6.36}$$

and

$$V_{C_3} = \frac{1}{1-k}V_{C_2} = \left(\frac{1}{1-k}\right)^2 V_{C_1} = \left(\frac{1}{1-k}\right)^3 V_{in} \tag{6.37}$$

The voltage $V_{C_{12}}$ is

$$V_{C_{12}} = 2V_{C_3} = 2\left(\frac{1}{1-k}\right)^3 V_{in}$$

The output voltage is

$$V_o = V_{C_{12}} - V_{in} = \left[2\left(\frac{1}{1-k}\right)^3 - 1\right]V_{in} \tag{6.38}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^3 - 1 \tag{6.39}$$

Analogously,

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$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{2}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{4L_1 I_o} = \frac{k(1-k)^6}{8} \frac{R}{fL_1} \tag{6.40}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{4L_2 I_o} = \frac{k(1-k)^4}{8} \frac{R}{fL_2} \tag{6.41}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4L_3 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_3} \tag{6.42}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{12}} = kT \frac{I_o}{C_{12}} = \frac{k}{fC_{12}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{6.43}$$

6.3.4 N/O Higher-Stage Additional Boost Circuit

The N/O higher-stage boost additional circuit is derived from the corresponding circuit of the main series by adding a DEC. For the nth-stage additional circuit, the final output voltage is

$$V_o = \left[2\left(\frac{1}{1-k} \right)^n - \right] V_{in}$$

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = 2\left(\frac{1}{1-k}\right)^n - 1 \tag{6.44}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_i (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{8}\frac{R}{fL_i} \tag{6.45}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{12}} \tag{6.46}$$

6.4 Double Series

All circuits of the double series of N/O cascaded boost converters are derived from the corresponding circuits of the main series by adding a DEC in each stage circuit. The first three stages of this series are shown in Figures 6.4, 6.7, and 6.8. For convenience, they are called elementary double boost circuit, two-stage double boost circuit, and three-stage double boost circuit, respectively, and numbered as n = 1, 2, and 3.

6.4.1 N/O Elementary Double Boost Circuit

This N/O elementary double boost circuit is derived from the elementary boost converter with adding a DEC. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.4, which is the same as the elementary boost additional circuit.

6.4.2 N/O Two-Stage Double Boost Circuit

The N/O two-stage double boost circuit is derived from the two-stage boost circuit by adding a DEC in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.7.

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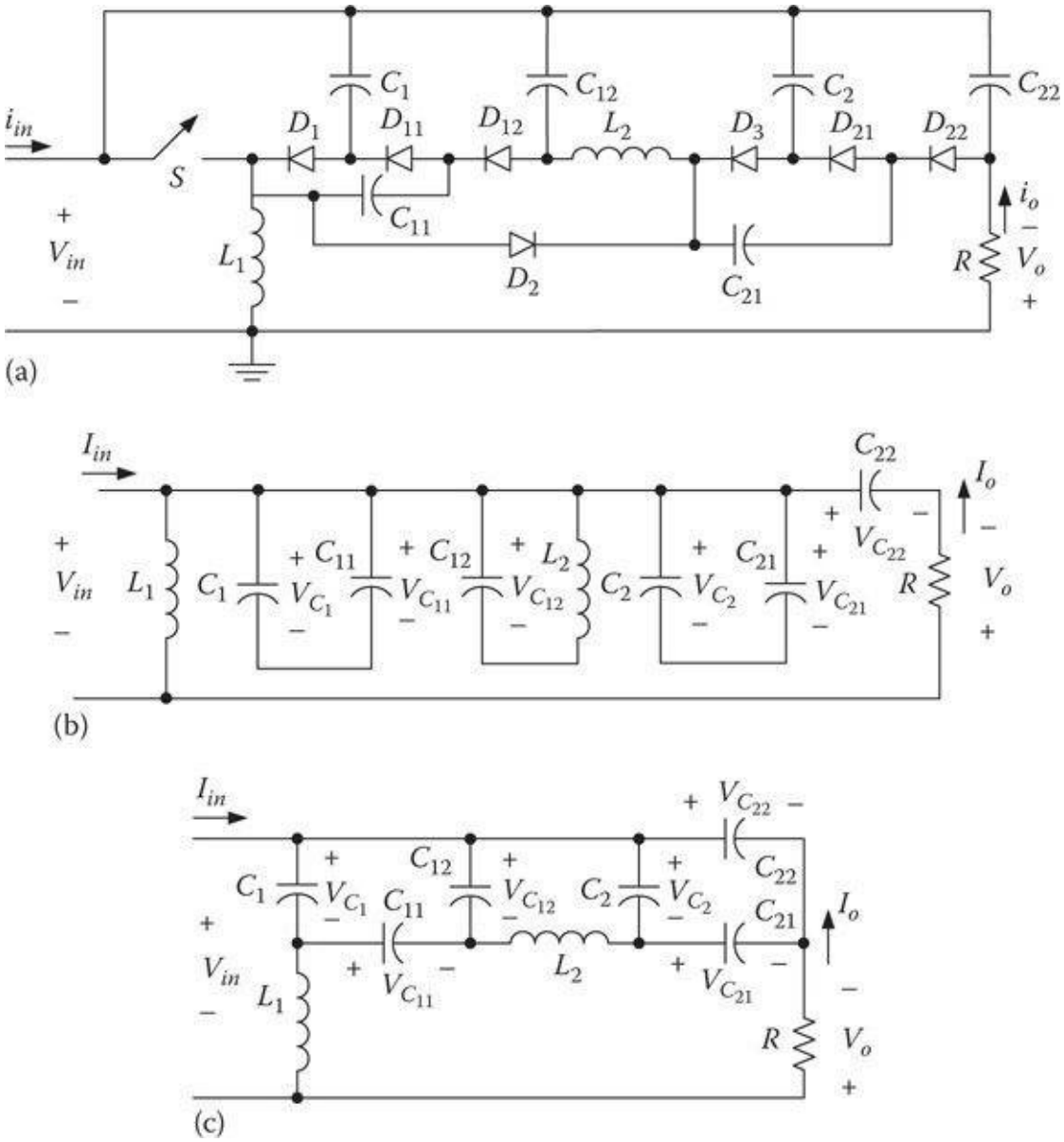


FIGURE 6.7
Two-stage double boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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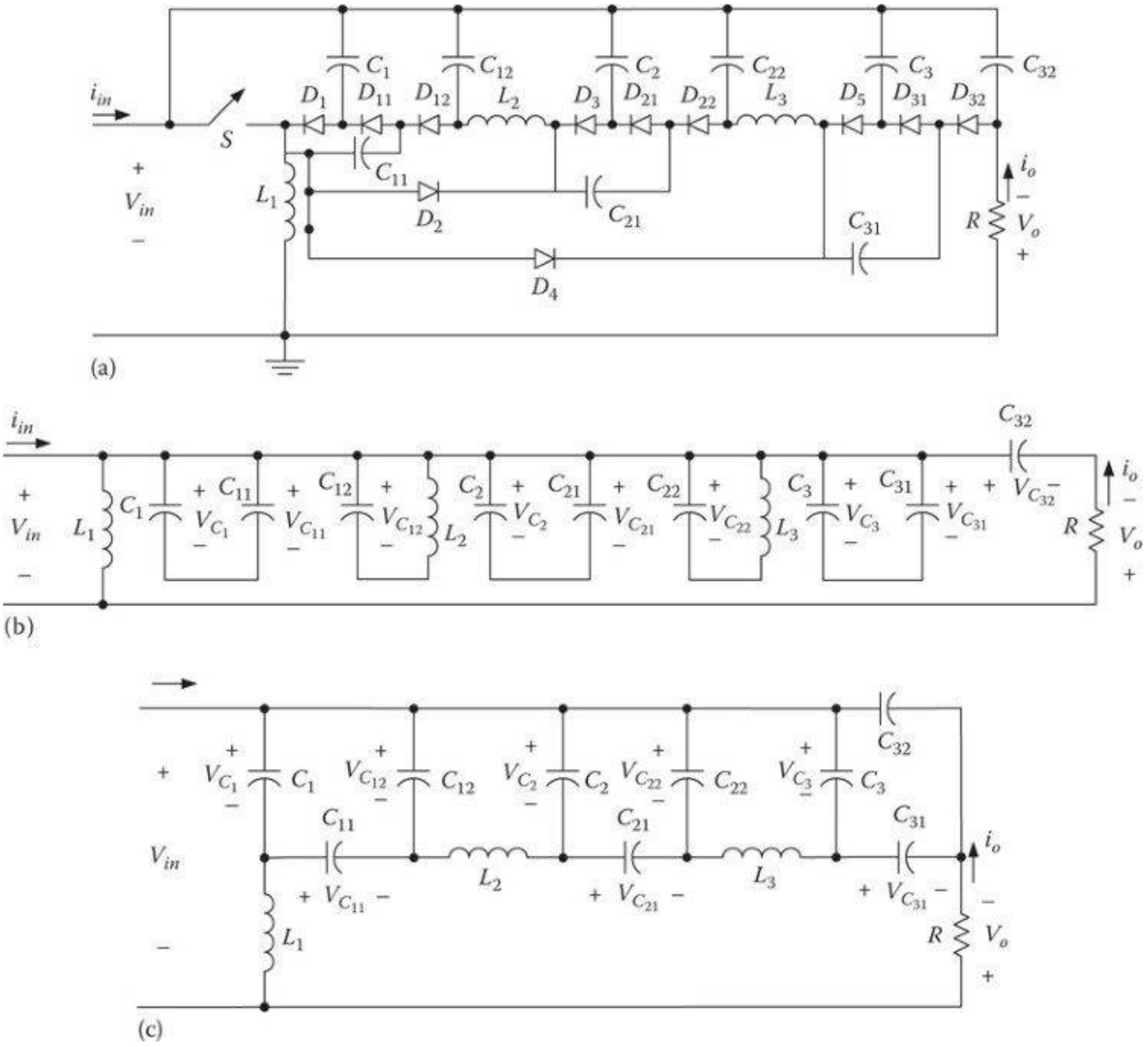


FIGURE 6.8
Three-stage double boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage across capacitors C_1 and C_{11} is charged to V_1. As described in the previous section, the voltage V_{C_1} across capacitors C_1 and C_{11} is $V_{C_1} = 1/(1-k)V_{in}$. The voltage across capacitor C_{12} is charged to $2V_{C_1}$.

The current flowing through inductor L_2 increases with voltage $2V_{C_1}$ during switch-on period kT and decreases with voltage $-(V_{C_2} - 2V_{C_1})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{2V_{C_1}}{L_2} kT = \frac{V_{C_2} - 2V_{C_1}}{L_2}(1-k)T \tag{6.47}$$

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$$V_{C_2} = \frac{2}{1-k} V_{C_1} = 2\left(\frac{1}{1-k}\right)^2 V_{in} \tag{6.48}$$

The voltage $V_{C_{22}}$ is

$$V_{C_{22}} = 2V_{C_2} = \left(\frac{2}{1-k}\right)^2 V_{in}$$

The output voltage is

$$V_o = V_{C_{22}} - V_{in} = \left[\left(\frac{2}{1-k}\right)^2 - 1\right] V_{in} \tag{6.49}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^2 - 1 \tag{6.50}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \left(\frac{2}{1-k}\right)^2 I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_o} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \tag{6.51}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \tag{6.52}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22}} = kT \frac{I_o}{C_{22}} = \frac{k}{fC_{22}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22}} \tag{6.53}$$

6.4.3 N/O Three-Stage Double Boost Circuit

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This N/O circuit is derived from the three-stage boost circuit by adding DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.8.

The voltage across capacitors C_1 and C_{11} is charged to V_{C_1}. As described previously, the voltage V_{C_1} across capacitors C_1 and C_{11} is $V_{C_1} = 1/(1-k)V_{in}$, and the voltage V_{C_2} across capacitors C_2 and C_{12} is $V_{C_2} = 2(1/(1-k))^2 V_{in}$.

The voltage across capacitor C_{22} is $2V_{C_2} = (2/(1-k))^2 V_{in}$. The voltage across capacitors C_3 and C_{31} is charged to V_3. The voltage across capacitor C_{12} is charged to V_o. The current flowing through inductor L_3 increases with voltage V_2 during switch-on period kT and decreases with voltage $-(V_{C_3} - 2V_{C_2})$ during switch-off $(1 - k)T$. Therefore,

$$\Delta i_{L_3} = \frac{2V_{C_2}}{L_3} kT = \frac{V_{C_3} - 2V_{C_2}}{L_3}(1-k)T \tag{6.54}$$

and

$$V_{C_3} = \frac{2V_{C_2}}{(1-k)} = \frac{4}{(1-k)^3} V_{in} \tag{6.55}$$

The voltage $V_{C_{32}}$ is

$$V_{C_{32}} = 2V_{C_3} = \left(\frac{2}{1-k}\right)^3 V_{in}$$

The output voltage is

$$V_o = V_{C_{32}} - V_{in} = \left[\left(\frac{2}{1-k}\right)^3 - 1\right] V_{in} \tag{6.56}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^3 - 1 \tag{6.57}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{8}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{4}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

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$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 T V_{in}}{16 L_1 I_o} = \frac{k(1-k)^6}{128}\frac{R}{fL_1} \tag{6.58}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 T V_1}{8 L_2 I_o} = \frac{k(1-k)^4}{32}\frac{R}{fL_2} \tag{6.59}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k) T V_2}{4 L_3 I_o} = \frac{k(1-k)^2}{8}\frac{R}{fL_3} \tag{6.60}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32}} = kT\frac{I_o}{C_{32}} = \frac{k}{fC_{32}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32}} \tag{6.61}$$

6.4.4 N/O Higher-Stage Double Boost Circuit

The N/O higher-stage double boost circuit is derived from the corresponding circuit of the main series by adding DEC in each stage circuit. For nth-stage additional circuit, the final output voltage is

$$V_o = \left[\left(\frac{2}{1-k}\right)^n - 1\right] V_{in}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{2}{1-k}\right)^n - 1 \tag{6.62}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_t (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{2*2^{2n}}\frac{R}{fL_i} \tag{6.63}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2}} \tag{6.64}$$

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6.5 Triple Series

All circuits of the triple series of N/O cascaded boost converters are derived from the corresponding circuits of the main series by adding DEC twice in each stage circuit. The first three stages of this series are shown in Figures 6.9, 6.10 and 6.11. For convenience, they are called elementary triple boost circuit, two-stage triple boost circuit, and three-stage triple boost circuit, respectively, and numbered as n = 1, 2, and 3.

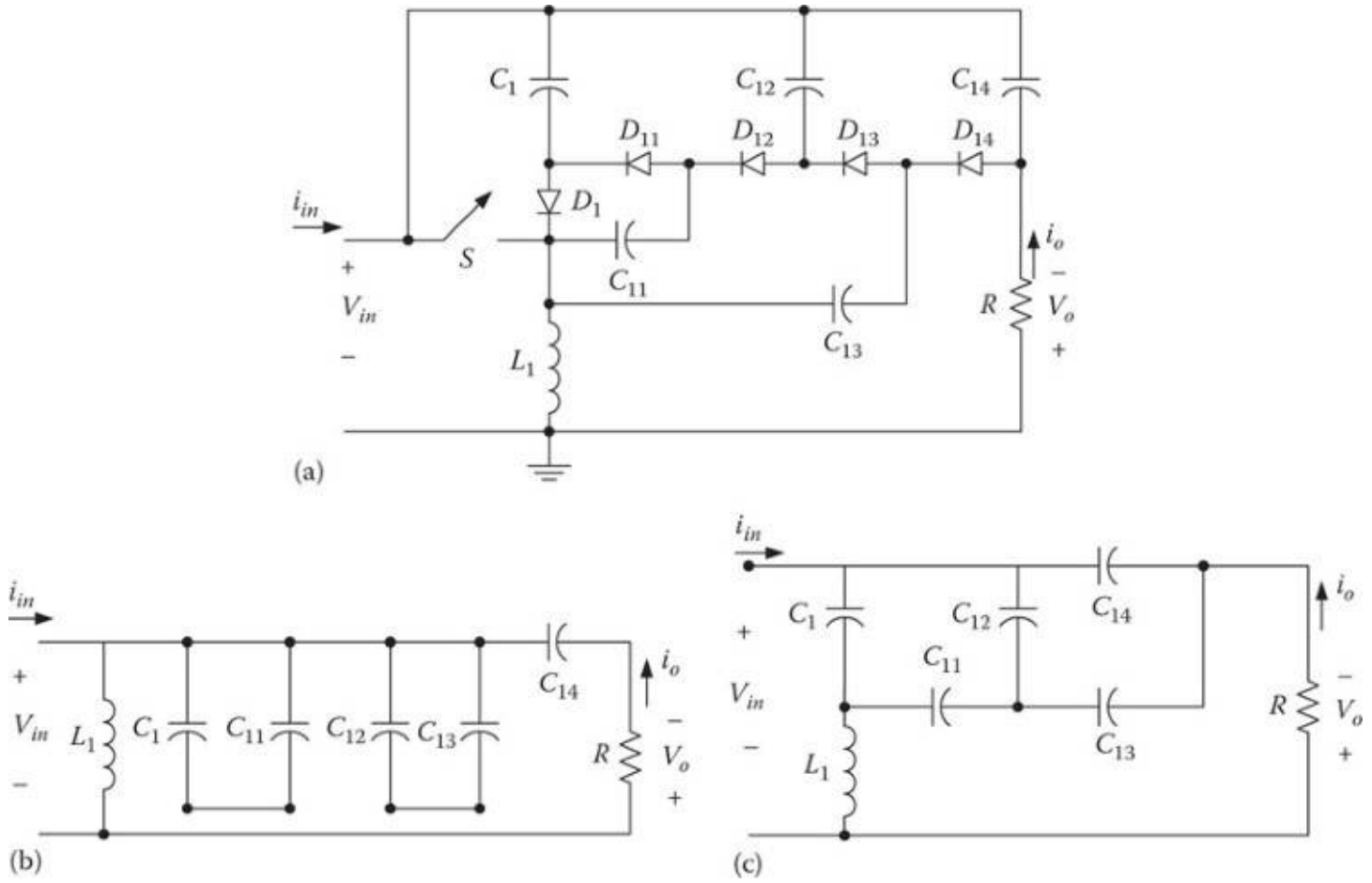


FIGURE 6.9
Elementary triple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

6.5.1 N/O Elementary Triple Boost Circuit

This N/O elementary triple boost circuit is derived from the elementary boost converter by adding DEC twice. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.9. The output voltage of first stage boost circuit is V_{C_1}:

$$V_{C_1} = \frac{V_{in}}{1-k}$$

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After the first DEC, the voltage (across capacitor C_{12}) increases to

$$V_{C_{12}} = 2V_{C_1} = \frac{2}{1-k} V_{in} \tag{6.65}$$

After the second DEC, the voltage (across capacitor C_{14}) increases to

$$V_{C_{14}} = V_{C_{12}} + V_{C_1} = \frac{3}{1-k} V_{in} \tag{6.66}$$

The final output voltage V_o is equal to

$$V_o = V_{C_{14}} - V_{in} = \left[\frac{3}{1-k} - 1 \right] V_{in} \tag{6.67}$$

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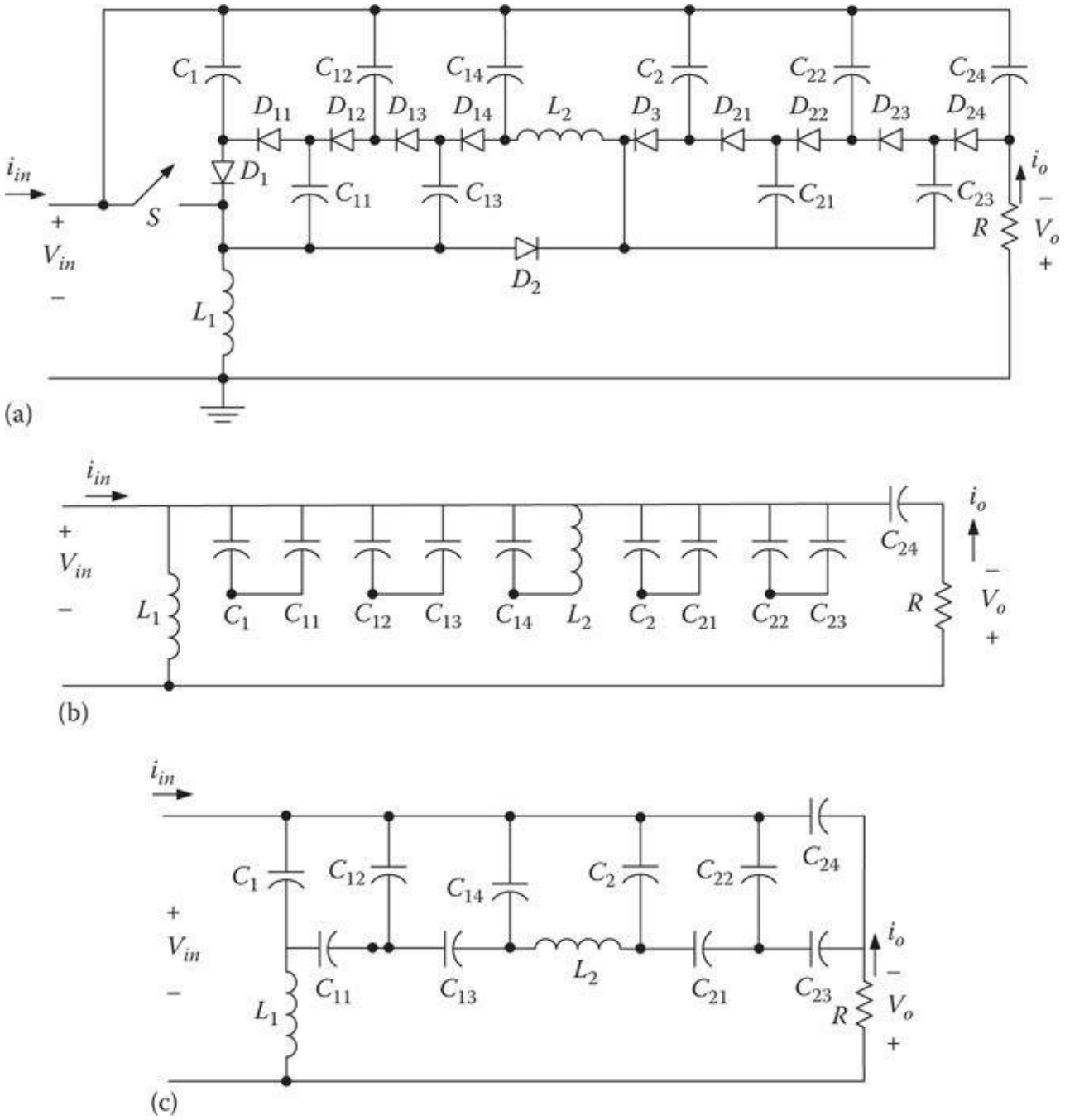


FIGURE 6.10
Two-stage triple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3}{1-k} - 1 \tag{6.68}$$

6.5.2 N/O Two-Stage Triple Boost Circuit

The N/O two-stage triple boost circuit is derived from two-stage boost circuit by adding DEC twice in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits

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are shown in Figure 6.10.

As described in the previous section, the voltage across capacitor C_{14} is $V_{C_{14}} = 3/(1-k)V_{in}$. Analogously, the voltage across capacitor C_{24} is

$$V_{C_{24}} = \left(\frac{3}{1-k}\right)^2 V_{in} \tag{6.69}$$

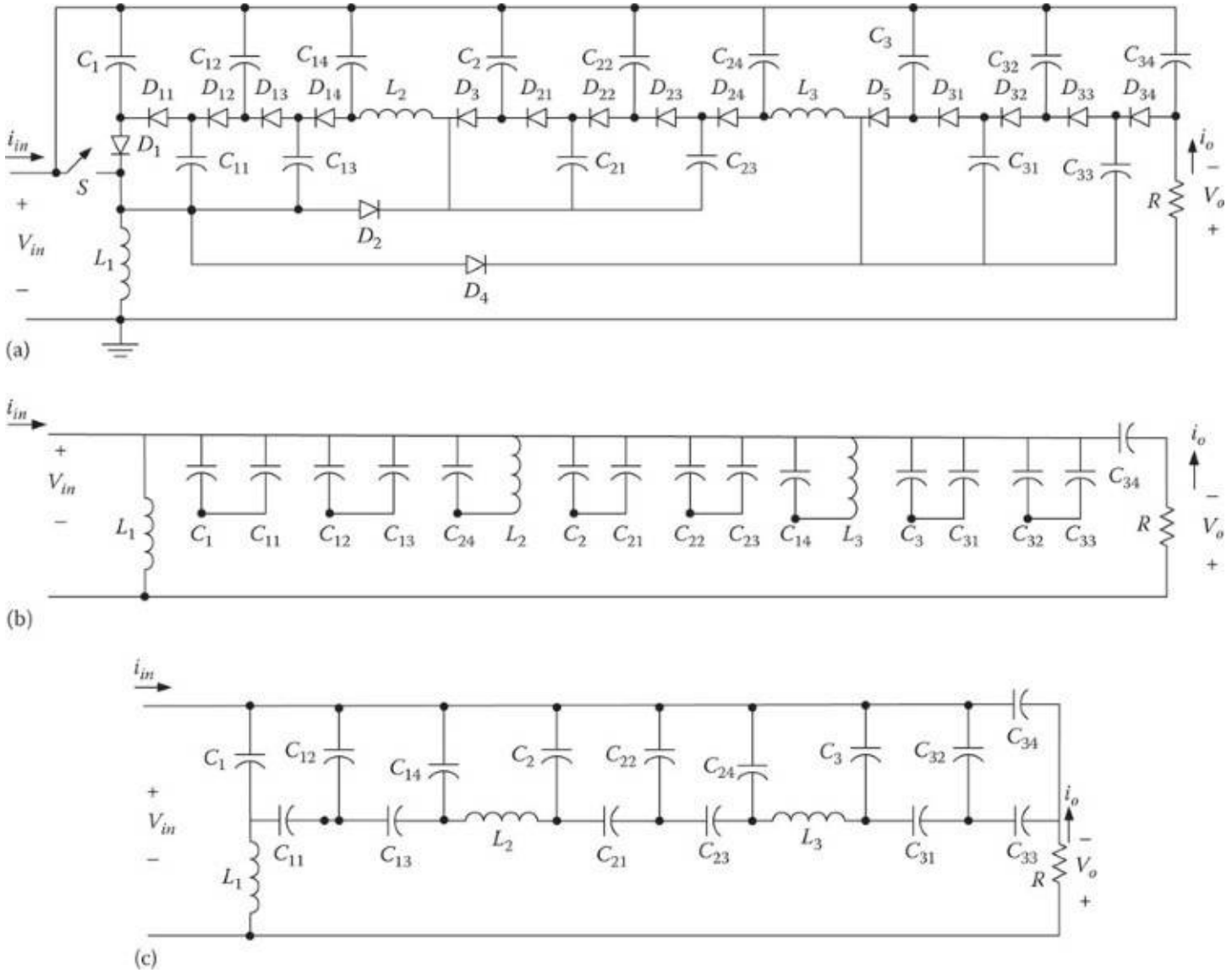


FIGURE 6.11
Three-stage triple boost circuit. (a) Circuit diagram, (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The final output voltage V_o is equal to

$$V_o = V_{C_{24}} - V_{in} = \left[\left(\frac{3}{1-k}\right)^2 - 1\right] V_{in} \tag{6.70}$$

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The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^2 - 1 \tag{6.71}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \left(\frac{2}{1-k}\right)^2 I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{2I_o}{1-k}$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_{in}}{8L_1 I_o} = \frac{k(1-k)^4}{16} \frac{R}{fL_1} \tag{6.72}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)TV_1}{4L_2 I_o} = \frac{k(1-k)^2}{8} \frac{R}{fL_2} \tag{6.73}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{24}} = kT \frac{I_o}{C_{24}} = \frac{k}{fC_{24}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{24}} \tag{6.74}$$

6.5.3 N/O Three-Stage Triple Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.11.

As described in the previous section, the voltage across capacitor C_{14} is $V_{C_{14}} = 3/(1-k)V_{in}$, and the voltage across capacitor C_{24} is $V_{C_{24}} = (3/(1-k))^2 V_{in}$. Analogously, the voltage across capacitor C_{34} is

$$V_{C_{34}} = \left(\frac{3}{1-k}\right)^3 V_{in} \tag{6.75}$$

The final output voltage V_o is equal to

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$$V_o = V_{C34} - V_{in} = \left[\left(\frac{3}{1-k}\right)^3 - 1\right] V_{in} \tag{6.76}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^3 - 1 \tag{6.77}$$

Analogously,

$$\Delta i_{L_1} = \frac{V_{in}}{L_1} kT \quad I_{L_1} = \frac{32}{(1-k)^3} I_o$$

$$\Delta i_{L_2} = \frac{V_1}{L_2} kT \quad I_{L_2} = \frac{8}{(1-k)^2} I_o$$

$$\Delta i_{L_3} = \frac{V_2}{L_3} kT \quad I_{L_3} = \frac{2}{1-k} I_o$$

Therefore, the variation ratio of current i_{L_1} through inductor L_1 is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^3 TV_{in}}{64 L_1 I_o} = \frac{k(1-k)^6}{12^3} \frac{R}{fL_1} \tag{6.78}$$

and the variation ratio of current i_{L_2} through inductor L_2 is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{k(1-k)^2 TV_1}{16 L_2 I_o} = \frac{k(1-k)^4}{12^2} \frac{R}{fL_2} \tag{6.79}$$

and the variation ratio of current i_{L_3} through inductor L_3 is

$$\xi_3 = \frac{\Delta i_{L_3}/2}{I_{L_3}} = \frac{k(1-k)TV_2}{4 L_3 I_o} = \frac{k(1-k)^2}{12} \frac{R}{fL_3} \tag{6.80}$$

Usually, ξ_1, ξ_2, and ξ_3 are small; this means that this converter works in the continuous mode. The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{34}} = kT \frac{I_o}{C_{34}} = \frac{k}{fC_{34}} \frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{34}} \tag{6.81}$$

Usually, R is in kΩ, f in 10 kHz, and C_{34} in μF; this ripple is smaller than 1%.

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6.5.4 N/O Higher-Stage Triple Boost Circuit

The N/O higher-stage triple boost circuit is derived from the corresponding circuit of the main series by adding DEC twice in each stage circuit. For *n*th-stage additional circuit, the voltage across capacitor C_{n4} is

$$V_{C_{n4}} = \left(\frac{3}{1-k}\right)^n V_{in}$$

The output voltage is

$$V_o = V_{C_{n4}} - V_{in} = \left[\left(\frac{3}{1-k}\right)^n - 1\right] V_{in} \tag{6.82}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{3}{1-k}\right)^n - 1 \tag{6.83}$$

Analogously, the variation ratio of current i_{L_i} through inductor L_t (i = 1, 2, 3,…, n) is

$$\xi_i = \frac{\Delta i_{L_i}/2}{I_{L_i}} = \frac{k(1-k)^{2(n-i+1)}}{12^{(n-i+1)}} \frac{R}{fL_i} \tag{6.84}$$

and the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n4}} \tag{6.85}$$

6.6 Multiple Series

All circuits of the multiple series of N/O cascaded boost converters are derived from the corresponding circuits of the main series by adding DEC multiple (j) times in each stage circuit. The first three stages of this series are shown in Figures 6.12, 6.13 and 6.14. For convenience, they are called elementary multiple boost circuit, two-stage multiple boost circuit, and three-stage multiple boost circuit, respectively, and numbered as n = 1, 2, and 3.

6.6.1 N/O Elementary Multiple Boost Circuit

This N/O elementary multiple boost circuit is derived from the elementary boost converter by adding DEC multiple *(j)* times. Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 6.12.

The output voltage of the first DEC (across capacitor C_{12j}) increases to

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$$V_{C_{12j}} = \frac{j+1}{1-k} V_{in} \tag{6.86}$$

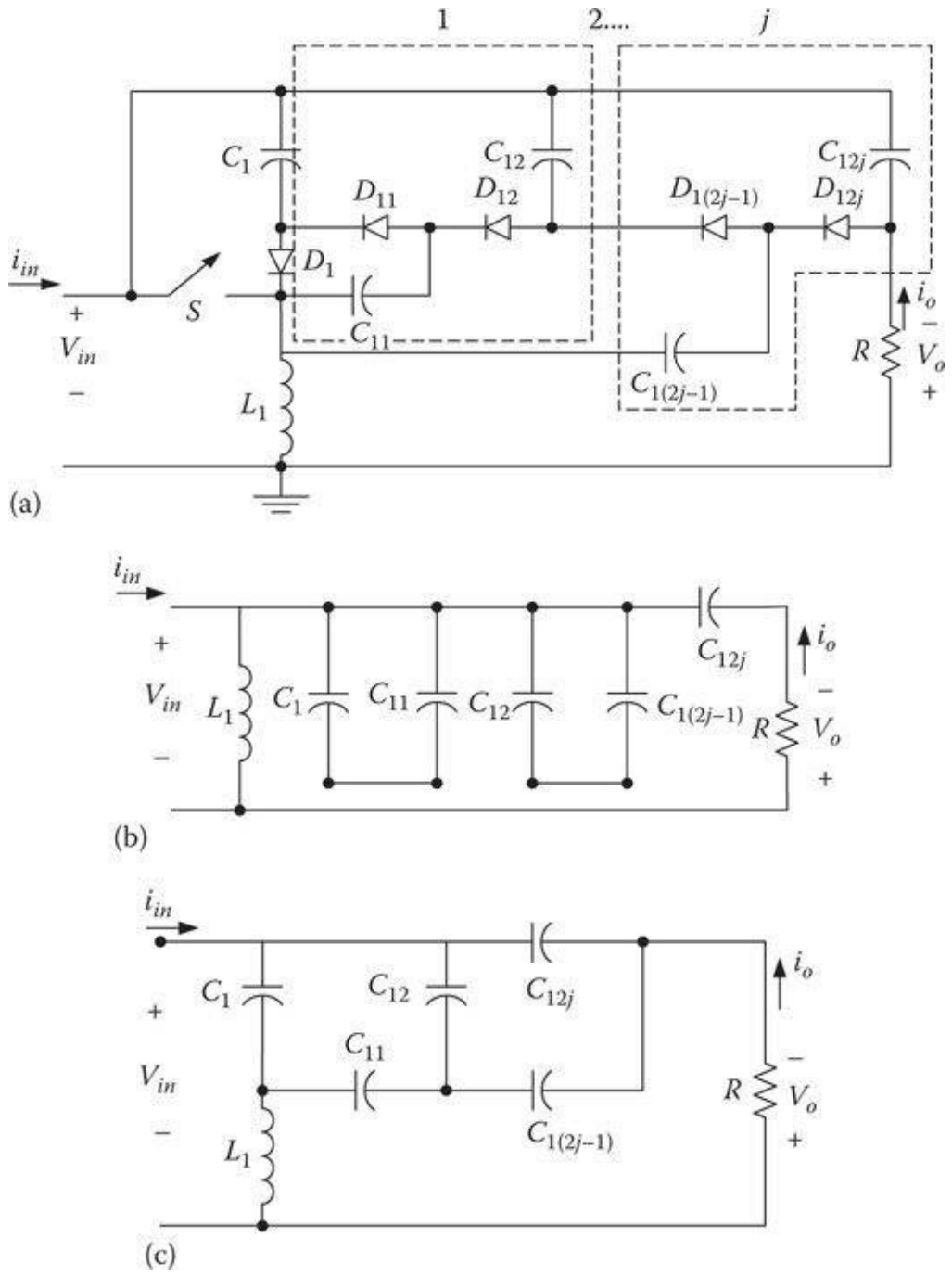


FIGURE 6.12
Elementary multiple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The final output voltage V_o is equal to

$$V_o = V_{C_{12j}} - V_{in} = \left[\frac{j+1}{1-k} - 1\right] V_{in} \tag{6.87}$$

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The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{j+1}{1-k} - 1 \tag{6.88}$$

6.6.2 N/O Two-Stage Multiple Boost Circuit

The N/O two-stage multiple boost circuit is derived from the two-stage boost circuit by adding DEC multiple (j) times in each stage circuit. Its circuit diagram and switch-on and switch-off equivalent circuits are shown in Figure 6.13.

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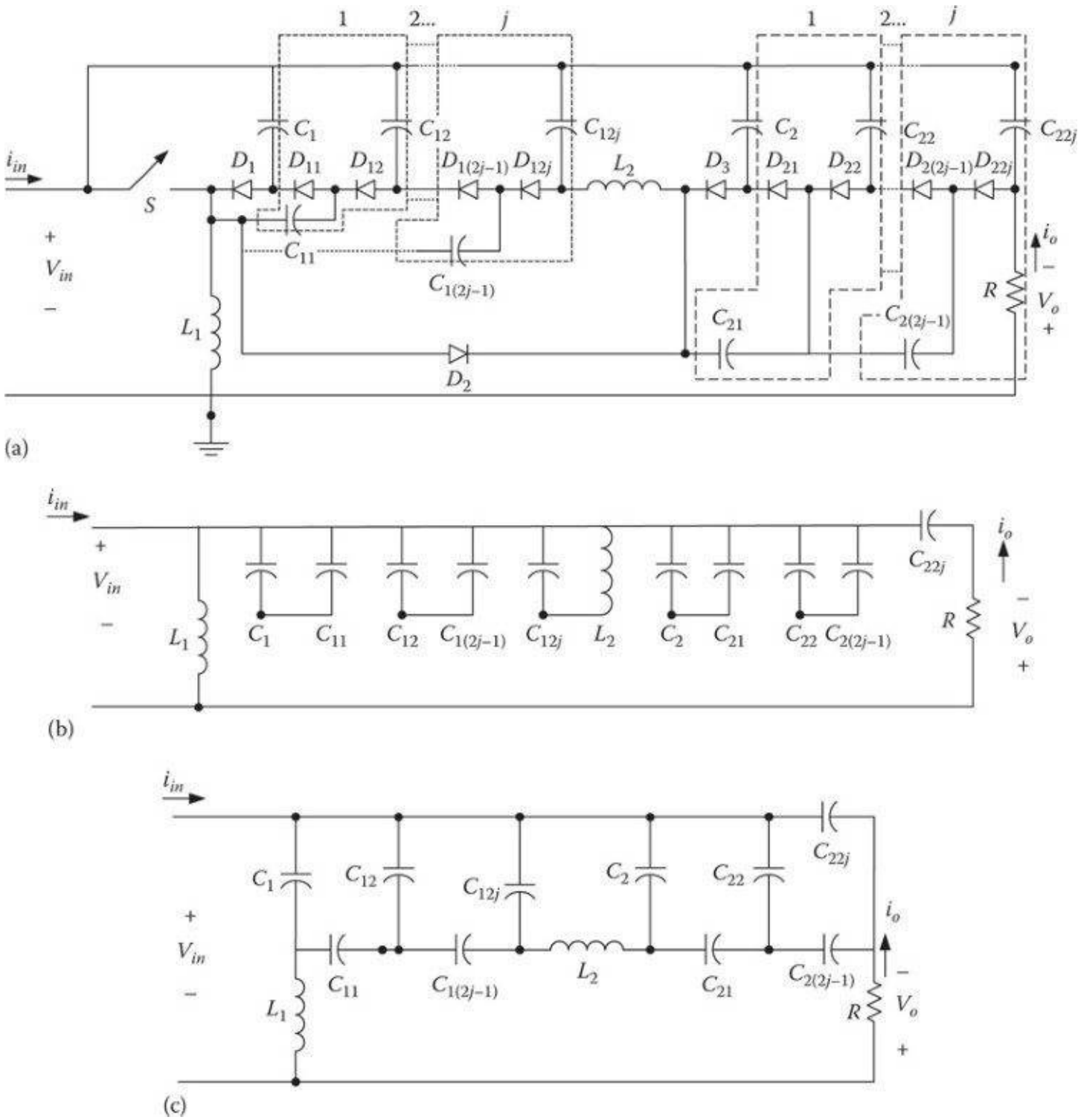


FIGURE 6.13
Two-stage multiple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

As described in the previous section, the voltage across capacitor C_{12j} is $V_{C_{12j}} = ((j+1)/(1-k))V_{in}$. Analogously, the voltage across capacitor C_{22j} is

$$V_{C_{22j}} = \left(\frac{j+1}{1-k}\right)^2 V_{in} \tag{6.89}$$

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The final output voltage V_o is equal to

$$V_o = V_{C22j} - V_{in} = \left[\left(\frac{j+1}{1-k}\right)^2 - 1\right] V_{in} \tag{6.90}$$

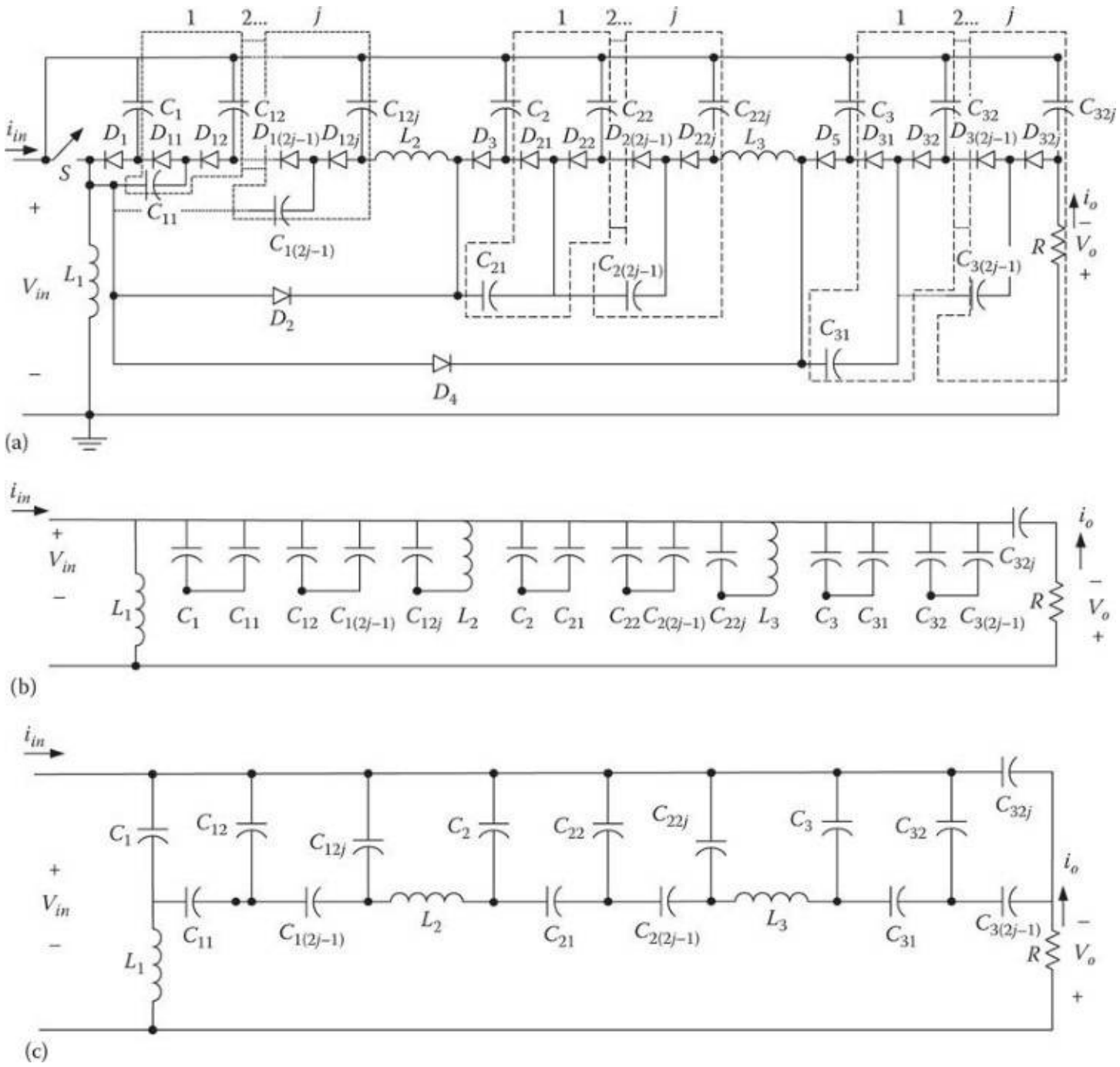


FIGURE 6.14
Three-stage multiple boost circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

The voltage transfer gain is

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$$G = \frac{V_o}{V_{in}} = \left(\frac{j+1}{1-k}\right)^2 - 1 \tag{6.91}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{22j}} = kT\frac{I_o}{C_{22j}} = \frac{k}{fC_{22j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{22j}} \tag{6.92}$$

6.6.3 N/O Three-Stage Multiple Boost Circuit

This N/O circuit is derived from the three-stage boost circuit by adding DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 6.14.

As described in the previous section, the voltage across capacitor C_{12j} is $V_{C_{12j}} = (j+1)/(1-k)V_{in}$, and the voltage across capacitor C_{22j} is $V_{C_{22j}} = ((j+1)/(1-k))^2 V_{in}$. Analogously, the voltage across capacitor C_{32j} is

$$V_{C_{32j}} = \left(\frac{j+1}{1-k}\right)^3 V_{in} \tag{6.93}$$

The final output voltage V_o is equal to

$$V_o = V_{C_{32j}} - V_{in} = \left[\left(\frac{j+1}{1-k}\right)^3 - 1\right] V_{in} \tag{6.94}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{j+1}{1-k}\right)^3 - 1 \tag{6.95}$$

The ripple voltage of output voltage v_o is

$$\Delta v_o = \frac{\Delta Q}{C_{32j}} = kT\frac{I_o}{C_{32j}} = \frac{k}{fC_{32j}}\frac{V_o}{R}$$

Therefore, the variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{32j}} \tag{6.96}$$

6.6.4 N/O Higher-Stage Multiple Boost Circuit

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The N/O higher-stage multiple boost circuit is derived from the corresponding circuit of the main series by adding DEC multiple (j) times in each stage circuit. For nth-stage multiple boost circuit, the voltage across capacitor C_{n2j} is

$$V_{C_{n2j}} = \left(\frac{j+1}{1-k}\right)^n V_{in}$$

The output voltage is

$$V_o = V_{C_{n2j}} - V_{in} = \left[\left(\frac{j+1}{1-k}\right)^n - 1\right] V_{in} \tag{6.97}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \left(\frac{j+1}{1-k}\right)^n - 1 \tag{6.98}$$

The variation ratio of output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{k}{2RfC_{n2j}} \tag{6.99}$$

6.7 Summary of N/O Cascaded Boost Converters

All the circuits of the N/O cascaded boost converters as a family can be shown in Figure 6.15. From the analysis of the previous two sections, we have the common formula to calculate the output voltage:

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$$V_o = \begin{cases} \left[\left(\frac{1}{1-k}\right)^n - 1\right] V_{in} & main_series \\ \left[2*\left(\frac{1}{1-k}\right)^n - 1\right] V_{in} & additional_series \\ \left[\left(\frac{2}{1-k}\right)^n - 1\right] V_{in} & double_series \\ \left[\left(\frac{3}{1-k}\right)^n - 1\right] V_{in} & triple_series \\ \left[\left(\frac{j+1}{1-k}\right)^n - 1\right] V_{in} & multiple(j)_series \end{cases} \quad (6.100)$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \begin{cases} \left(\frac{1}{1-k}\right)^n - 1 & main_series \\ 2*\left(\frac{1}{1-k}\right)^n - 1 & additional_series \\ \left(\frac{2}{1-k}\right)^n - 1 & double_series \\ \left(\frac{3}{1-k}\right)^n - 1 & triple_series \\ \left(\frac{j+1}{1-k}\right)^n - 1 & multiple(j)_series \end{cases} \quad (6.101)$$

In order to show the advantages of the N/O cascaded boost converters, we compare their voltage transfer gains to that of the

$$\text{Buck converter} \quad G = \frac{V_o}{V_{in}} = k$$

$$\text{Forward converter} \quad G = \frac{V_o}{V_{in}} = kN \quad (N \text{ is the transformer turns ratio})$$

$$\text{Cúk converter} \quad G = \frac{V_o}{V_{in}} = \frac{k}{1-k}$$

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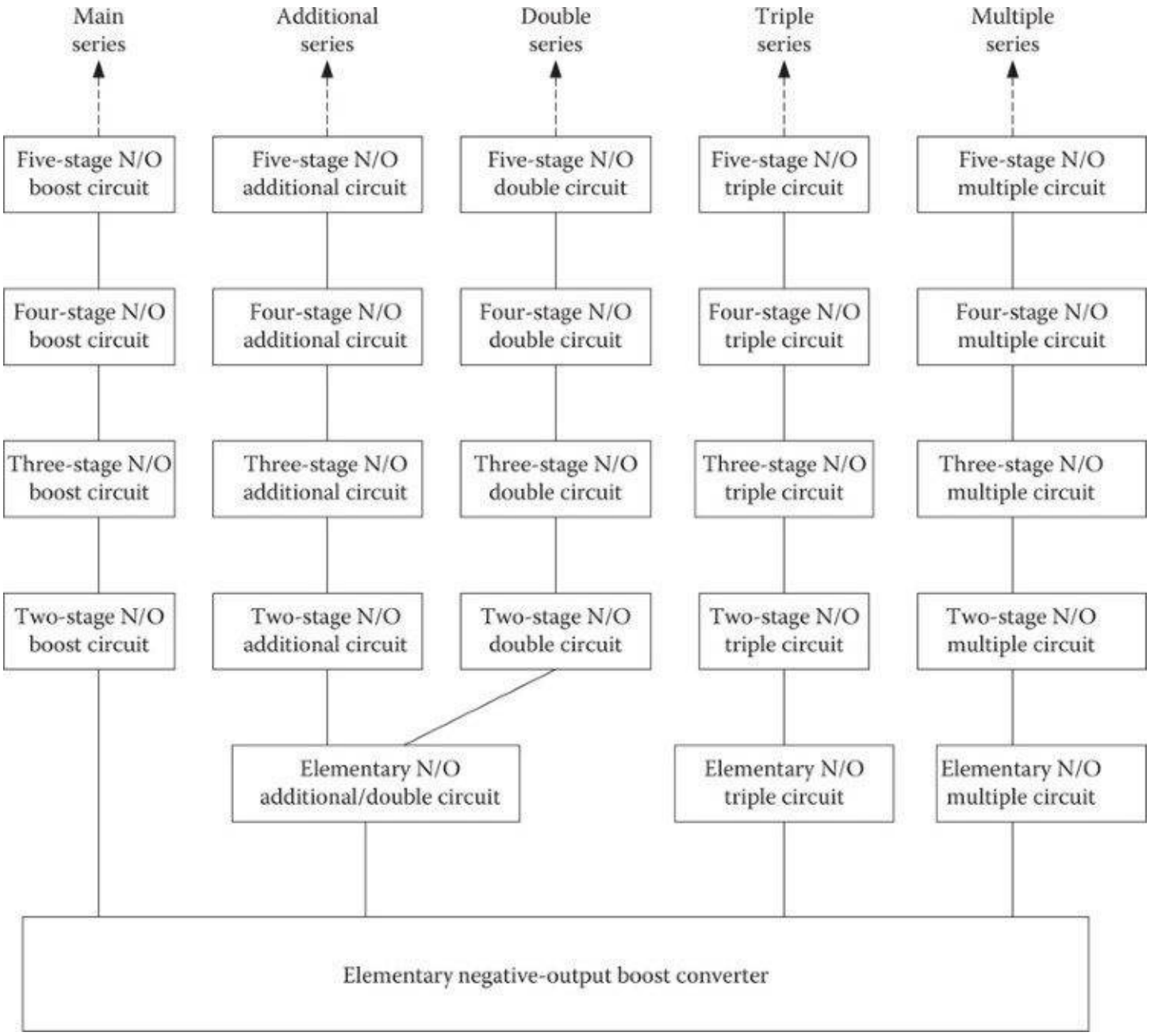


FIGURE 6.15
The family of negative-output cascaded boost converters.

$$\text{Flyback converter} \quad G = \frac{V_o}{V_{in}} = \frac{k}{1-k} N \quad (N \text{ is the transformer turns ratio})$$

$$\text{Boost converter} \quad G = \frac{V_o}{V_{in}} = \frac{1}{1-k}$$

$$\text{N/O Luo-converters} \quad G = \frac{V_o}{V_{in}} = \frac{n}{1-k} \tag{6.102}$$

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If we assume that the conduction duty k is 0.2, the output voltage transfer gains are listed in Table 6.1.

If the conduction duty k is 0.5, the output voltage transfer gains are listed in Table 6.2.

If the conduction duty k is 0.8, the output voltage transfer gains are listed in Table 6.3.

TABLE 6.1
Voltage Transfer Gains of Converters in the Condition $k = 0.2$

Stage No. (n)	1	2	3	4	5	n
Buck converter	0.2					
Forward converter	0.2N (N is the transformer turns ratio)					
Cuk converter	0.25					
Flyback converter	0.25N (N is the transformer turns ratio)					
Boost converter	1.25					
Negative-output Luo-converters	1.25	2.5	3.75	5	6.25	1.25^n
Negative-output cascaded boost converters—main series	0.25	1.563	1.953	2.441	3.052	1.25^n
Negative-output cascaded boost converters—additional series	1.5	3.126	3.906	4.882	6.104	$2*1.25^n$
Negative-output cascaded boost converters—double series	2.5	6.25	15.625	39.063	97.66	$(2*1.25)^n$
Negative-output cascaded boost converters—triple series	2.5	6.25	15.625	39.063	97.66	$(2*1.25)^n$
Negative-output cascaded boost converters—multiple series	2.5	6.25	15.625	39.063	97.66	$(2*1.25)^n$

TABLE 6.2
Voltage Transfer Gains of Converters in the Condition $k = 0.5$

Stage No. (n)	1	2	3	4	5	n
Buck converter	0.5					
Forward converter	0.5N (N is the transformer turns ratio)					
Cuk converter	1					
Flyback converter	N (N is the transformer turns ratio)					
Boost converter	2					
Negative-output Luo-converters	2	4	6	8	10	2^n
Negative-output cascaded boost converters—main series	2	4	8	16	32	2^n
Negative-output cascaded boost converters—additional series	4	8	16	32	64	$2*2^n$
Negative-output cascaded boost converters—double series	4	16	64	256	1024	$(2*2)^n$
Negative-output cascaded boost converters—triple series	4	16	64	256	1024	$(2*2)^n$
Negative-output cascaded boost converters—multiple series	4	16	64	256	1024	$(2*2)^n$

TABLE 6.3
Voltage Transfer Gains of Converters in the Condition $k = 0.8$

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Stage No. (n)	1	2	3	4	5	n
Buck converter	0.8					
Forward converter	0.8N (N is the transformer turns ratio)					
Cuk converter	4					
Flyback converter	4N (N is the transformer turns ratio)					
Boost converter	5					
Negative-output Luo-converters	5	10	15	20	25	5^n
Negative-output cascaded boost converters—main series	5	25	125	625	3,125	5^n
Negative-output cascaded boost converters—additional series	10	50	250	1,250	6,250	$2*5^n$
Negative-output cascaded boost converters—double series	10	100	1,000	10,000	100,000	$(2*5)^n$
Negative-output cascaded boost converters—triple series	10	100	1,000	10,000	100,000	$(2*5)^n$
Negative-output cascaded boost converters—multiple series	10	100	1,000	10,000	100,000	$(2*5)^n$

6.8 Simulation and Experimental Results

6.8.1 Simulation Results of a Three-Stage Boost Circuit

To verify the design and calculation results, PSpice simulation package was applied to a three-stage boost circuit. Choose V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all C_1−C_8 = 2 μF and R = 30 kΩ, and using k = 0.7 and f = 100 kHz. The voltage values V_1, V_2, and V_o of a triple-lift circuit are 66, 194, and 659 V, respectively, and the inductor current waveforms are i_{L_1} (its average value i_{L_1} = 6l8 mA), i_{L_2}, and i_{L_3}. The simulation results are shown in Figure 6.16. The voltage values are matched to the calculated results.

6.8.2 Experimental Results of a Three-Stage Boost Circuit

A test rig was constructed to verify the design and calculation results and compared with PSpice simulation results. The test conditions are still V_{in} = 20 V, $L_1 = L_2 = L_3$ = 10 mH, all C_1−C_8 = 2 μF and R = 30 kΩ, and using k = 0.7 and f = 100 kHz. The component of the switch is a MOSFET device IRF950 with the rates 950 V/5 A/2 MHz. We measured the values of the output voltage and first inductor current in the following converters.

After careful measurement, the current value of $I_{L_1} = 0.62$ A (shown in Channel 1 with 1 A/Div) and the voltage value of V_o = 660 V (shown in Channel 2 with 200 V/Div) are obtained. The experimental results (current and voltage values) in Figure 6.17 match the calculated and simulation results, which are $I_{L_1} = 0.618$ A and V_o = 659 V shown in Figure 6.16.

6.8.3 Efficiency Comparison of Simulation and Experimental Results

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These circuits enhanced the voltage transfer gain successfully and efficiently. Particularly, the efficiency of the tested circuits is 78%, which is good for high output voltage equipment. To compare the simulation and experimental results, see Table 6.4. All results are well identified to each other.

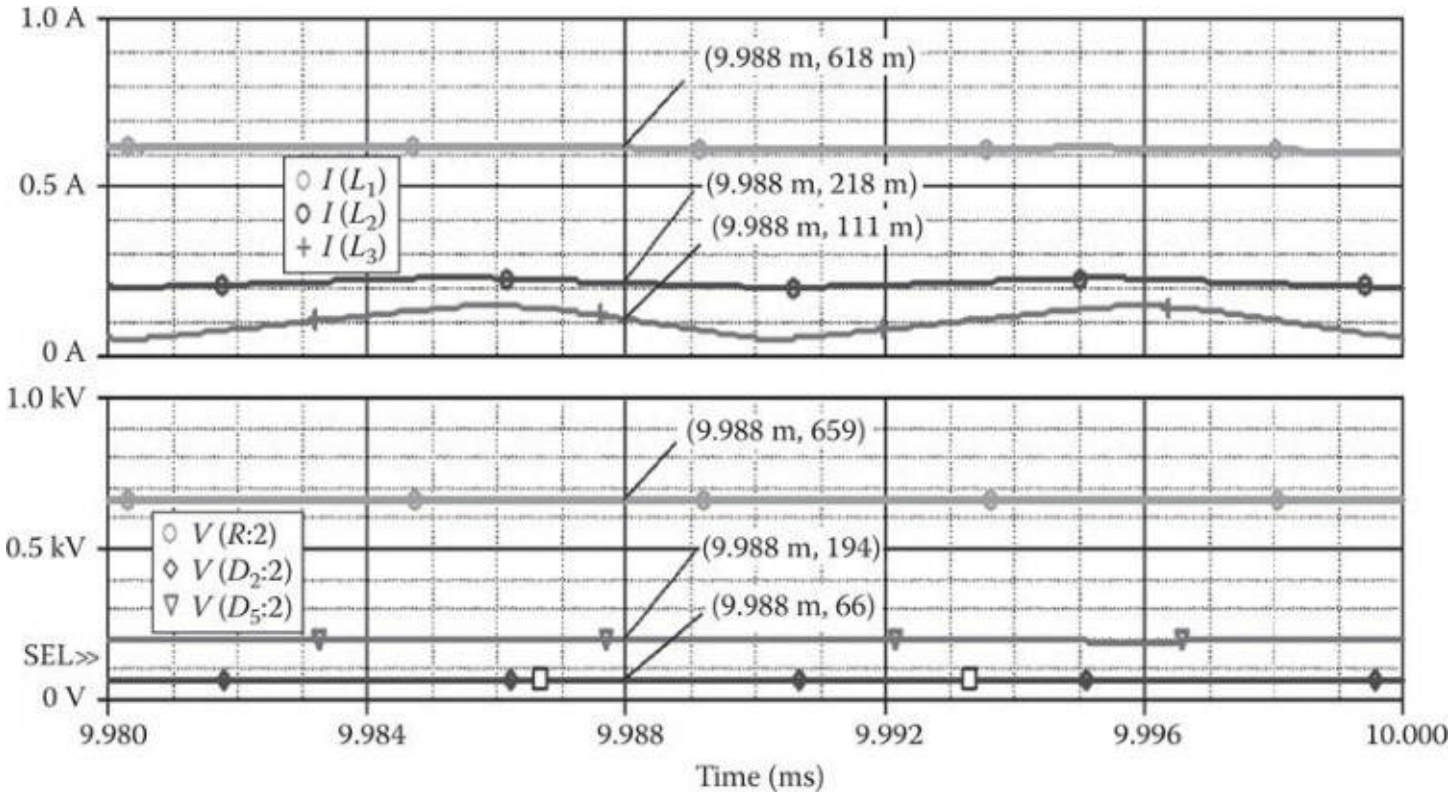


FIGURE 6.16
The simulation results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

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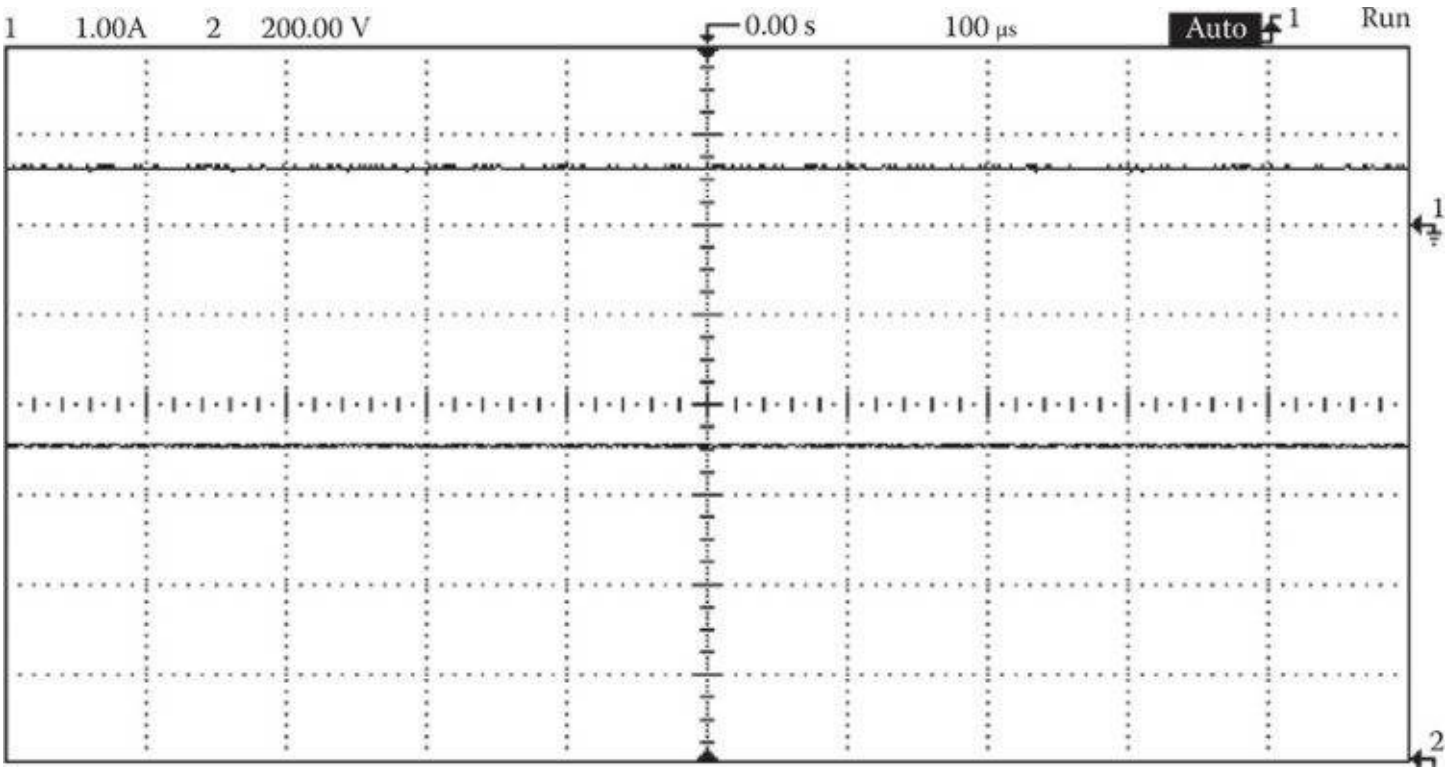


FIGURE 6.17
The experimental results of a three-stage boost circuit at condition $k = 0.7$ and $f = 100$ kHz.

TABLE 6.4
Comparison of Simulation and Experimental Results of a Triple-Lift Circuit

Stage No. (n)	I_{L_1} (A)	I_{in} (A)	V_{in} (V)	P_{in} (W)	V_o (V)	P_o (W)	η (%)
Simulation results	0.618	0.927	20	18.54	659	14.47	78
Experimental results	0.62	0.93	20	18.6	660	14.52	78

6.8.4 Transient Process

Usually, there is high inrush current during the first power-on. Therefore, the voltage across capacitors is quickly changed to certain values. The transient process is very quick taking only a few milliseconds. It is difficult to demonstrate it in this section.

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7

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Ultra-Lift Luo-Converter

Voltage-lift (VL) technique has been successfully applied in the design of power DC/DC converters. Good examples are the three-series Luo-converters: positive-output Luo-converters, negative-output Luo-converters, and double-output Luo-converters. Using VL technique, we can obtain high-voltage transfer gain. Super-lift (SL) technique has been given much attention since it yields high-voltage transfer gain. This chapter introduces the ultra-lift (UL) Luo-converter, as a novel approach within the new UL technique, which produces even higher-voltage transfer gain. Our analysis and calculation illustrated the advanced characteristics of this converter.

7.1 Introduction

Voltage-lift (VL) technique has been widely applied in the electronic circuit design. Since the last century, it has been successfully applied in the design of power DC/DC converters. Good examples are the three-series Luo-converters. Using VL technique, one can obtain the converter's voltage transfer gain stage by stage in arithmetical series; this gain is higher than that of classical converters such as buck converter, boost converter, and buck-boost converter. Assume the input voltage and current of a DC/DC converter are V_1 and I_1, the output voltage and current are V_2 and I_2, and the conduction duty cycle is k. In order to compare these converters' transfer gains, we list the following formulae:

$$\text{Buck converter} \quad G = \frac{V_2}{V_1} = k \tag{7.1}$$

$$\text{Boost converter} \quad G = \frac{V_2}{V_1} = \frac{1}{1-k} \tag{7.2}$$

$$\text{Buck-boost converter} \quad G = \frac{V_2}{V_1} = \frac{k}{1-k} \tag{7.3}$$

$$\text{Luo-converters} \quad G = \frac{V_2}{V_1} = \frac{k^{h(n)}[n+h(n)]}{1-k} \tag{7.4}$$

where

n is the stage number

$h(n)$ is the Hong function

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$$h(n)=\begin{cases}1 & n=0\\ 0 & n>0\end{cases} \tag{7.5}$$

$n = 0$ for the elementary circuit with the voltage transfer gain

$$G=\frac{V_2}{V_1}=\frac{k}{1-k} \tag{7.6}$$

Super-lift (SL) technique has been paid much more attention because it yields higher-voltage transfer gain. Good examples are the VL Luo-converters. Using this technique, one can obtain the converter's voltage transfer gain stage by stage in geometrical series. The voltage transfer gain calculation formulae are

$$G=\frac{V_2}{V_1}=\left(\frac{j+2-k}{1-k}\right)^n \tag{7.7}$$

where

n is the stage number

j is the multiple-enhanced number

$n = 1$ and $j = 0$ for the elementary circuit, yielding

$$G=\frac{V_2}{V_1}=\frac{2-k}{1-k} \tag{7.8}$$

This chapter introduces the ultra-lift (UL) Luo-converter as a novel approach of the new technology—UL technique—which produces even higher-voltage transfer gain. Simulation results verified our analysis and calculation and illustrated the advanced characteristics of this converter.

7.2 Operation of Ultra-Lift Luo-Converter

The circuit diagram is shown in Figure 7.1a, which consists of one switch S, two inductors L_1 and L_2, two capacitors C_1 and C_2, three diodes, and the load R. Its switch-on equivalent circuit is shown in Figure 7.1b. Its switch-off equivalent circuit for the continuous conduction mode (CCM) is shown in Figure 7.1c, and its switch-off equivalent circuit for the discontinuous conduction mode (DCM) is shown in Figure 7.1d.

It is a very simple structure converter in comparison with other converters. As usual, the input voltage and current of the UL Luo-converter are V_1 and I_1, the output voltage and current are V_2 and I_2, the conduction duty cycle is k, and the switching frequency is f. Consequently, the repeating period $T = 1/f$ the switch-on period is kT, and the switch-off period is $(1 - k)T$. To concentrate the operation process, we assume that all components

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except load R are ideal ones. Therefore, no power losses are considered during power transformation, that is, $P_{in} = P_o$ or $V_1 \times I_1 = V_2 \times I_2$.

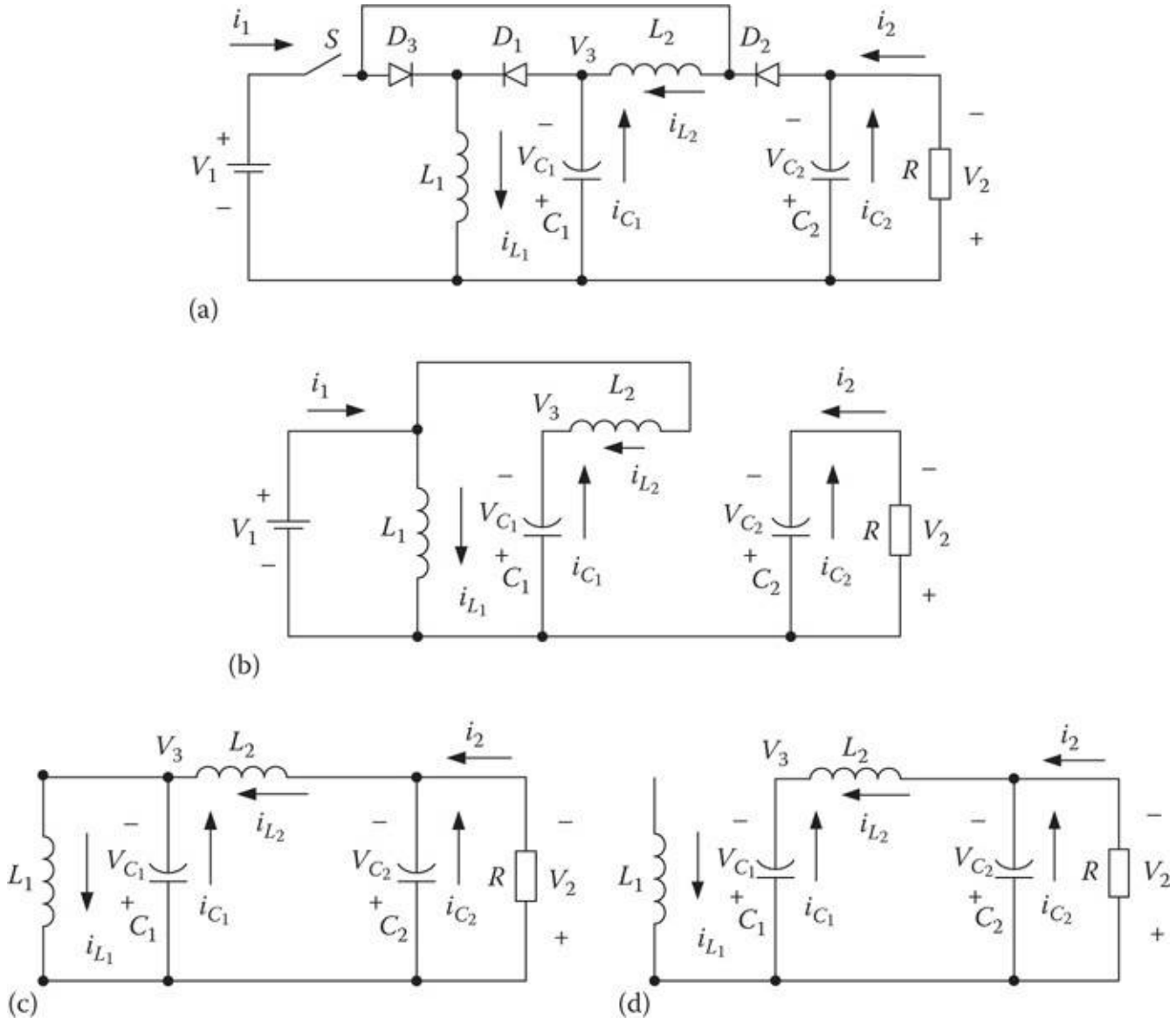


FIGURE 7.1
Ultra-lift Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off (CCM). (d) Equivalent circuit during switch-off (DCM).

7.2.1 Continuous Conduction Mode

Referring to Figure 7.1b and c, we see that the current i_{L_1} increases with the slope $+V_1/L_1$ during switch-on and decreases with the slope $-V_3/L_1$ during switch-off. In the steady state, the current increment is equal to the decrement in a whole period T. This gives the relation

$$kT\frac{V_1}{L_1} = (1-k)T\frac{V_3}{L_1}$$

Thus,

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$$V_{C_1} = V_3 = \frac{k}{1-k} V_1 \tag{7.9}$$

The current i_{L_2} increases with the slope $+(V_1 - V_3)/L_2$ during switch-on and decreases with the slope $-(V_3 - V_2)/L_2$ during switch-off. In the steady state, the current increment is equal to the decrement in a whole period T. We obtain the relation

$$kT \frac{V_1 + V_3}{L_2} = (1-k)T \frac{V_2 - V_3}{L_2}$$

$$V_2 = V_{C_2} = \frac{2-k}{1-k} V_3 = \frac{k}{1-k} \frac{2-k}{1-k} V_1 = \frac{k(2-k)}{(1-k)^2} V_1 \tag{7.10}$$

The voltage transfer gain is

$$G = \frac{V_2}{V_1} = \frac{k}{1-k} \frac{2-k}{1-k} = \frac{k(2-k)}{(1-k)^2} \tag{7.11}$$

It is much higher than the voltage transfer gains of the VL Luo-converter and SL Luo-converter in Equations 7.6 and 7.8. Actually, the gain in Equation 7.11 is the product of those in Equations 7.6 and 7.8. Another advantage is the starting output voltage of zero. The curve of the voltage transfer gain M versus the conduction duty cycle k is shown in Figure 7.2.

The relation between input and output average currents is

$$I_2 = \frac{(1-k)^2}{k(2-k)} I_1 \tag{7.12}$$

The relation between average currents I_{L_2} and I_{L_1} is

$$I_{L_2} = (1-k) I_{L_1} \tag{7.13}$$

Other relations are

$$I_{L_2} = \left(1 + \frac{k}{1-k}\right) I_2 = \frac{1}{1-k} I_2 \tag{7.14}$$

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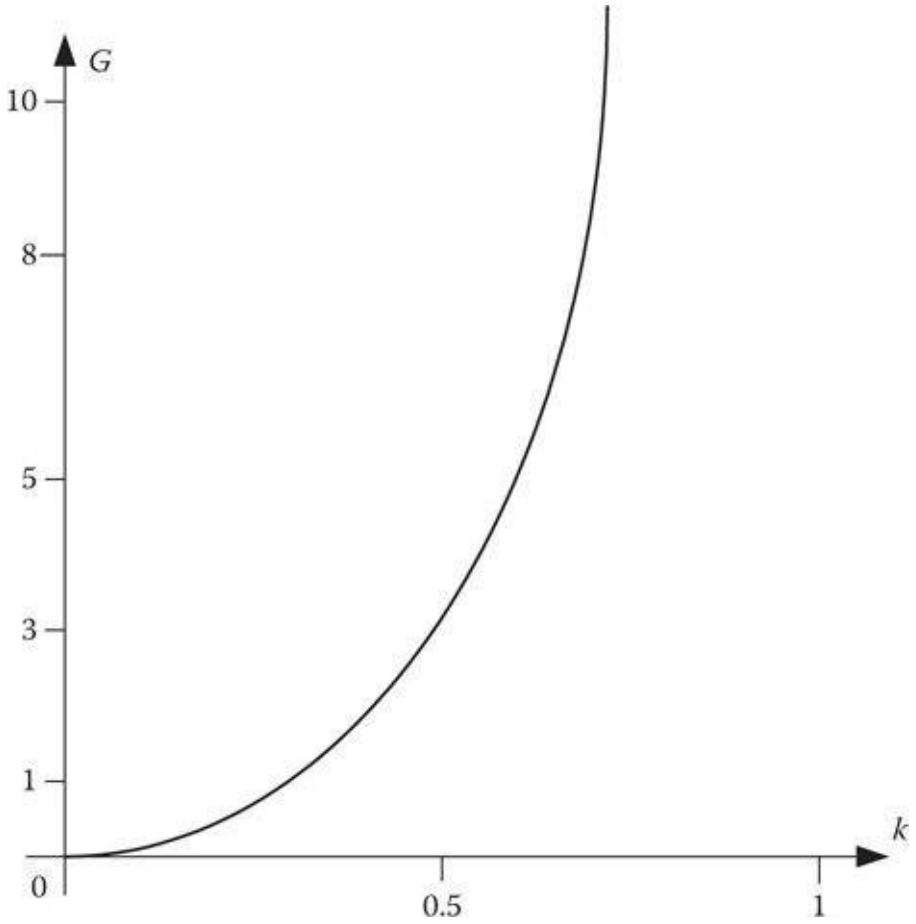


FIGURE 7.2
The voltage transfer gain *M* versus conduction duty cycle *k*.

$$I_{L_1} = \frac{1}{1-k} I_{L_2} = \left(\frac{1}{1-k}\right)^2 I_2 \tag{7.15}$$

The variation of inductor current i_{L_1} is

$$\Delta i_{L_1} = kT \frac{V_1}{L_1} \tag{7.16}$$

and its variation ratio is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = \frac{k(1-k)^2 TV_1}{2L_1 I_2} = \frac{k(1-k)^2 TR}{2L_1 M} = \frac{(1-k)^4 TR}{2(2-k) fL_1} \tag{7.17}$$

The diode current i_{D_1} is the same as the inductor current i_{L_1} during the switching-off period. For the CCM operation, both currents do not descend to zero, that is,

$$\xi_1 \le 1$$

The variation of inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{kTV_1}{(1-k)L_2} \tag{7.18}$$

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and its variation ratio is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{kTV_1}{2L_2I_2} = \frac{kTR}{2L_2M} = \frac{(1-k)^2TR}{2(2-k)fL_2} \tag{7.19}$$

The variation of capacitor voltage v_{C_1} is

$$\Delta v_{C_1} = \frac{\Delta Q_{C_1}}{C_1} = \frac{kTI_{L_2}}{C_1} = \frac{kTI_2}{(1-k)C_1} \tag{7.20}$$

and its variation ratio is

$$\sigma_1 = \frac{\Delta v_{C_1}/2}{V_{C_1}} = \frac{kTI_2}{2(1-k)V_3C_1} = \frac{k(2-k)}{2(1-k)^2fC_1R} \tag{7.21}$$

The variation of capacitor voltage v_{C_2} is

$$\Delta v_{C_2} = \frac{\Delta Q_{C_2}}{C_2} = \frac{kTI_2}{C_2} \tag{7.22}$$

and its variation ratio is

$$\varepsilon = \sigma_2 = \frac{\Delta v_{C_2}/2}{V_{C_2}} = \frac{kTI_2}{2V_2C_2} = \frac{k}{2fC_2R} \tag{7.23}$$

From the analysis and calculations, we can see that all variations are very small. A design example is that V_1 = 10 V, $L_1 = L_2$ = 1 mH, $C_1 = C_2$ = 1 μF, R = 3000 Ω, f = 50 kHz, and conduction duty cycle k varies from 0.1 to 0.9. The output voltage variation ratio ε is less than 0.003. The output voltage is a very smooth DC voltage with nearly no ripple.

7.2.2 Discontinuous Conduction Mode

Referring to Figure 7.1b, 7.1c and d, we see that the current i_{L_1} increases with the slope $+V_1/L_1$ during switch-on and decreases with the slope $-V_3/L_1$ during switch-off. The inductor current i_{L_1} decreases to zero before $t = T$, that is, the current becomes zero before the next time the switch is turned on.

The current waveform is shown in Figure 7.3. The DCM operation condition is defined as

$$\xi_1 \geq 1$$

or

$$\xi_1 = \frac{k(1-k)^2TR}{2L_1M} = \frac{(1-k)^4TR}{2(2-k)fL_1} \geq 1 \tag{7.24}$$

Taking the equal mark, we obtain the boundary between CCM and DCM operations. Here, we define the normalized impedance Z_n:

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$$Z_n = \frac{R}{fL_1} \tag{7.25}$$

The boundary equation is

$$G = \frac{k(1-k)^2}{2} Z_n \tag{7.26}$$

or

$$\frac{G}{Z_n} = \frac{k(1-k)^2}{2}$$

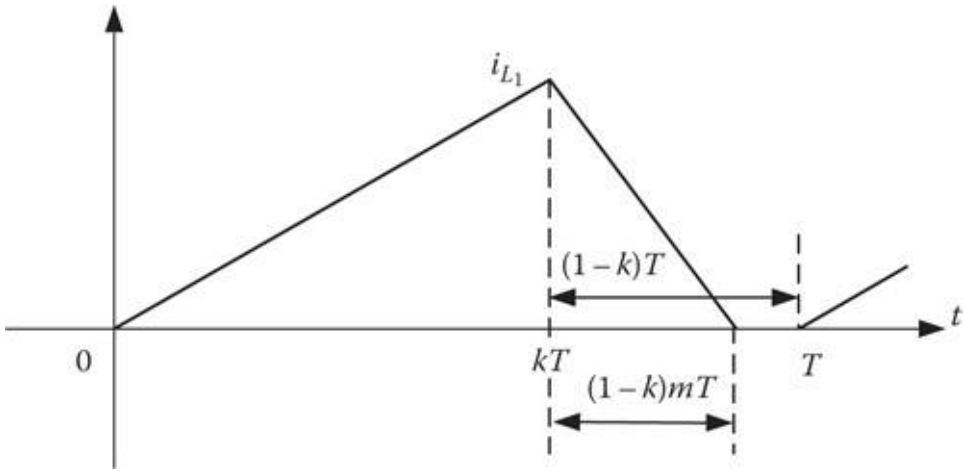


FIGURE 7.3
Discontinuous inductor current i_{L_1}.

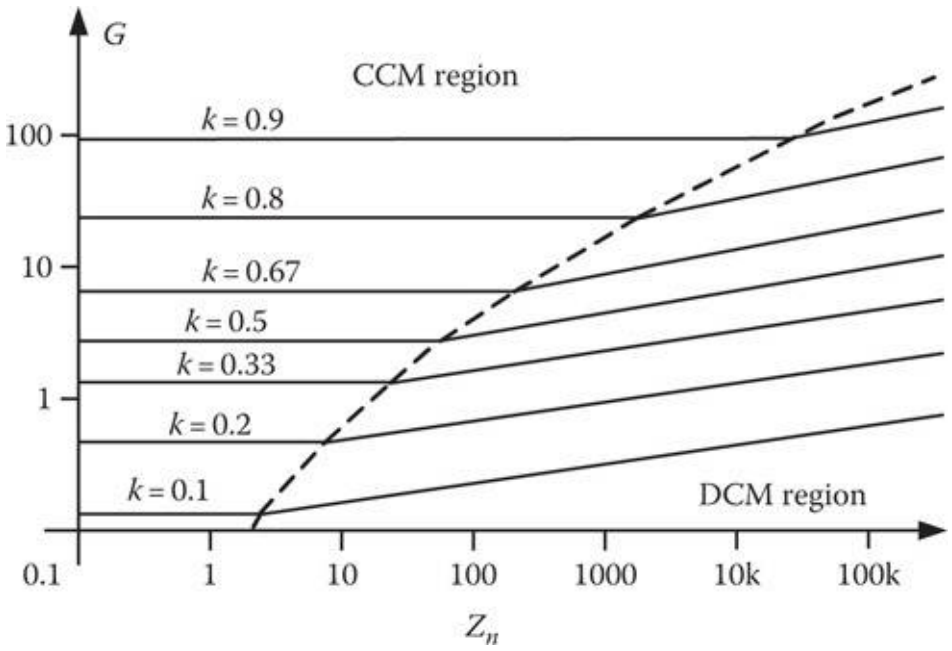


FIGURE 7.4
Boundary between continuous conduction mode and discontinuous conduction mode.

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The corresponding Z_n is

$$Z_n = \frac{k(2-k)}{(1-k)^2} \Big/ \frac{k(1-k)^2}{2} = \frac{2(2-k)}{(1-k)^4} \tag{7.27}$$

The curve is shown in Figure 7.4 and Table 7.1.

We define the filling factor m to describe the current existing time. For DCM operation,

$$0 < m \leq 1$$

In the steady state, the current increment is equal to the decrement in a whole period T. The following relation is obtained:

$$kT\frac{V_1}{L_1} = (1-k)mT\frac{V_3}{L_1}$$

Thus,

$$V_{C_1} = V_3 = \frac{k}{(1-k)m}V_1 \tag{7.28}$$

TABLE 7.1
Boundary between Continuous Conduction Mode and Discontinuous Conduction Mode

k	0.2	0.33	0.5	0.67	0.8	0.9
G	0.5625	1.25	3	8	24	99
G/Z_n	0.064	2/27	1/16	1/27	0.016	0.0045
Z_n	8.8	16.9	48	216	1,500	22,000

Comparing Equations 7.9 and 7.28, we find that the voltage V_3 is higher during DCM operation since $m < 1$. Its expression is

$$m = \frac{1}{\xi_1} = \frac{2L_1G}{k(1-k)^2TR} = \frac{2(2-k)}{(1-k)^4Z_N} \tag{7.29}$$

The current i_{L_2} increases with the slope $+(V_1 - V_3)/L_2$ during switch-on and decreases with the slope $-(V_3 - V_2)/L_2$ during switch-off. In the steady state, the current increment is equal to the decrement in a whole period T. We obtain the relationship

$$kT\frac{V_1+V_3}{L_2} = (1-k)T\frac{V_2-V_3}{L_2}$$

$$V_2 = V_{C_2} = \frac{2-k}{1-k}V_3 = \frac{k(2-k)}{m(1-k)^2}V_1 \tag{7.30}$$

The voltage transfer gain in DCM is

$$G_{DCM} = \frac{V_2}{V_1} = \frac{k(2-k)}{m(1-k)^2} = \frac{k(1-k)^2}{2}Z_N \tag{7.31}$$

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It is higher than that of the voltage transfer gain during CCM operation since $m < 1$. We can see that the voltage transfer gain G_{DwM} increases linearly with, and is proportional to, the normalized impedance Z_n and is shown in Figure 7.4.

7.3 Instantaneous Values

Instantaneous values of the voltage and current of each component are very important in describing the converter operation. By referring to Figure 7.1, we can obtain these values in CCM and DCM operations.

7.3.1 Continuous Conduction Mode

Referring to Figure 7.1b and c, we obtain the instantaneous values of the voltage and current of each component in CCM operation as follows:

$$i_{L_1}(t) = \begin{cases} I_{L_1-\min} + \dfrac{V_1}{L_1}t & 0 \le t \le kT \\ I_{L_1-\max} - \dfrac{V_3}{L_1}t & kT \le t \le T \end{cases} \tag{7.32}$$

$$i_{L_2}(t) = \begin{cases} I_{L_2-\min} + \dfrac{V_1 - V_3}{L_2}t & 0 \le t \le kT \\ I_{L_2-\max} - \dfrac{V_2 - V_1}{L_2}t & kT \le t \le T \end{cases} \tag{7.33}$$

$$i_1(t) = i_s = \begin{cases} I_{1-\min} + \left(\dfrac{V_1}{L_1} + \dfrac{V_1 - V_3}{L_2}\right)t & 0 \le t \le kT \\ 0 & kT \le t \le T \end{cases} \tag{7.34}$$

$$i_{D_1}(t) = \begin{cases} 0 & 0 \le t \le kT \\ I_{L_1-\max} - \dfrac{V_3}{L_1}t & kT \le t \le T \end{cases} \tag{7.35}$$

$$i_{C_1}(t) = \begin{cases} -\left(I_{L_2-\min} + \dfrac{V_1 - V_3}{L_2}t\right) & 0 \le t \le kT \\ I_{C_1} & kT \le t \le T \end{cases} \tag{7.36}$$

$$i_{C_2}(t) = \begin{cases} -I_2 & 0 \le t \le kT \\ I_{C_2} & kT \le t \le T \end{cases} \tag{7.37}$$

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$$v_{L_1}(t)=\begin{cases}V_1 & 0\le t\le kT\\ V_3 & kT\le t\le T\end{cases} \tag{7.38}$$

$$v_{L_2}(t)=\begin{cases}V_1-V_3 & 0\le t\le kT\\ V_2-V_3 & kT\le t\le T\end{cases} \tag{7.39}$$

$$v_s=\begin{cases}0 & 0\le t\le kT\\ V_1-V_3 & kT\le t\le T\end{cases} \tag{7.40}$$

$$v_{D_1}(t)=\begin{cases}V_1-V_3 & 0\le t\le kT\\ 0 & kT\le t\le T\end{cases} \tag{7.41}$$

$$v_{C_1}(t)=\begin{cases}V_3-\dfrac{I_{L_2}}{C_1}t & 0\le t\le kT\\ V_3+\dfrac{I_{C_1}}{C_1}t & kT\le t\le T\end{cases} \tag{7.42}$$

$$v_{C_2}(t)=\begin{cases}V_2-\dfrac{I_2}{C_2}t & 0\le t\le kT\\ V_2+\dfrac{I_{C_2}}{C_2}t & kT\le t\le T\end{cases} \tag{7.43}$$

7.3.2 Discontinuous Conduction Mode

Referring to Figure 7.1b, 7.1c and d, we obtain the instantaneous values of the voltage and current of each component in DCM operation. Since inductor current i_{L_1} is discontinuous, some parameters have three states with T′ = kT + (1 − k)mT < T :

$$i_{L_1}(t)=\begin{cases}\dfrac{V_1}{L_1}t & 0\le t\le kT\\ I_{L_1-\max}-\dfrac{V_3}{L_1}t & kT\le t\le T'\\ 0 & T'\le t\le kT\end{cases} \tag{7.44}$$

$$i_{L_2}(t)=\begin{cases}I_{L_2-\min}+\dfrac{V_1-V_3}{L_2}t & 0\le t\le kT\\ I_{L_2-\max}-\dfrac{V_2-V_1}{L_2}t & kT\le t\le T\end{cases} \tag{7.45}$$

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$$i_1(t) = i_s = \begin{cases} I_{1-\min} + \left(\dfrac{V_1}{L_1} + \dfrac{V_1 - V_3}{L_2}\right)t & 0 \le t \le kT \\ 0 & kT \le t \le T \end{cases} \tag{7.46}$$

$$i_{D_1}(t) = \begin{cases} 0 & 0 \le t \le kT \\ I_{L_1-\max} - \dfrac{V_3}{L_1}t & kT \le t \le T' \\ 0 & T' \le t \le kT \end{cases} \tag{7.47}$$

$$i_{C_1}(t) = \begin{cases} -\left(I_{L_2-\min} + \dfrac{V_1 - V_3}{L_2}t\right) & 0 \le t \le kT \\ I_{C_1} & kT \le t \le T \end{cases} \tag{7.48}$$

$$i_{C_2}(t) = \begin{cases} -I_2 & 0 \le t \le kT \\ I_{C_2} & kT \le t \le T \end{cases} \tag{7.49}$$

$$v_{L_1}(t) = \begin{cases} V_1 & 0 \le t \le kT \\ V_3 & kT \le t \le T' \\ 0 & T' \le t \le kT \end{cases} \tag{7.50}$$

$$v_{L_2}(t) = \begin{cases} V_1 - V_3 & 0 \le t \le kT \\ V_2 - V_3 & kT \le t \le T \end{cases} \tag{7.51}$$

$$v_s(t) = \begin{cases} 0 & 0 \le t \le kT \\ V_1 - V_3 & kT \le t \le T' \\ V_1 & T' \le t \le kT \end{cases} \tag{7.52}$$

$$v_{D_1}(t) = \begin{cases} V_1 - V_3 & 0 \le t \le kT \\ 0 & kT \le t \le T' \\ -V_3 & T' \le t \le kT \end{cases} \tag{7.53}$$

$$v_{C_1}(t) = \begin{cases} V_3 - \dfrac{I_{L_2}}{C_1}t & 0 \le t \le kT \\ V_3 + \dfrac{I_{C_1}}{C_1}t & kT \le t \le T \end{cases} \tag{7.54}$$

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$$v_{C_2}(t) = \begin{cases} V_2 - \dfrac{I_2}{C_2} t & 0 \le t \le kT \\ V_2 + \dfrac{I_{C_2}}{C_2} t & kT \le t \le T \end{cases} \tag{7.55}$$

7.4 Comparison of the Gain to Other Converters' Gains

The UL Luo-converter has been successfully developed using the novel approach of the new technology—UL technique. Table 7.2 lists the voltage transfer gains of various converters at k = 0.2, 0.33, 0.5, 0.67, 0.8, and 0.9. The outstanding characteristics of the UL Luo-converter are very well presented. From the comparison, we can obviously see that the UL Luo-converter has a very high-voltage transfer gain: $G(k)|_{k\ =\ 0.5} = 3$, $G(k)|_{k\ =\ 0.667} = 8$, $G(k)|_{k\ =\ 0.8} = 24$, $G(k)|_{k}$=0.9 = 99.

TABLE 7.2
Comparison of Various Converters' Gains

k	0.2	0.33	0.5	0.67	0.8	0.9
Buck	0.2	0.33	0.5	0.67	0.8	0.9
Boost	1.25	1.5	2	3	5	10
Buck–boost	0.25	0.5	1	2	4	9
Luo-converter	0.25	0.5	1	2	4	9
Super-lift Luo-converter	2.25	2.5	3	4	6	11
Ultra-lift Luo-converter	0.56	1.25	3	8	24	99

7.5 Simulation Results

To verify the advantages of the UL Luo-converter, a PSpice simulation method is applied. We choose the parameter's values: V_1 = 10 V, $L_1 = L_2$ = 1 mH, $C_1 = C_2$ = 1 μF, R = 3 kΩ, f = 50 kHz, and conduction duty cycle k = 0.6 and 0.66. The output voltage V_2 = 52.5 and 78 V, correspondingly. The first waveform is the inductor's current i_{L_1}, which flows through the inductor L_1. The second and third waveforms are the voltage V_3 and output voltage V_2. These simulation results are identical to the calculation results. The results are shown in Figures 7.5 and 7.6, respectively.

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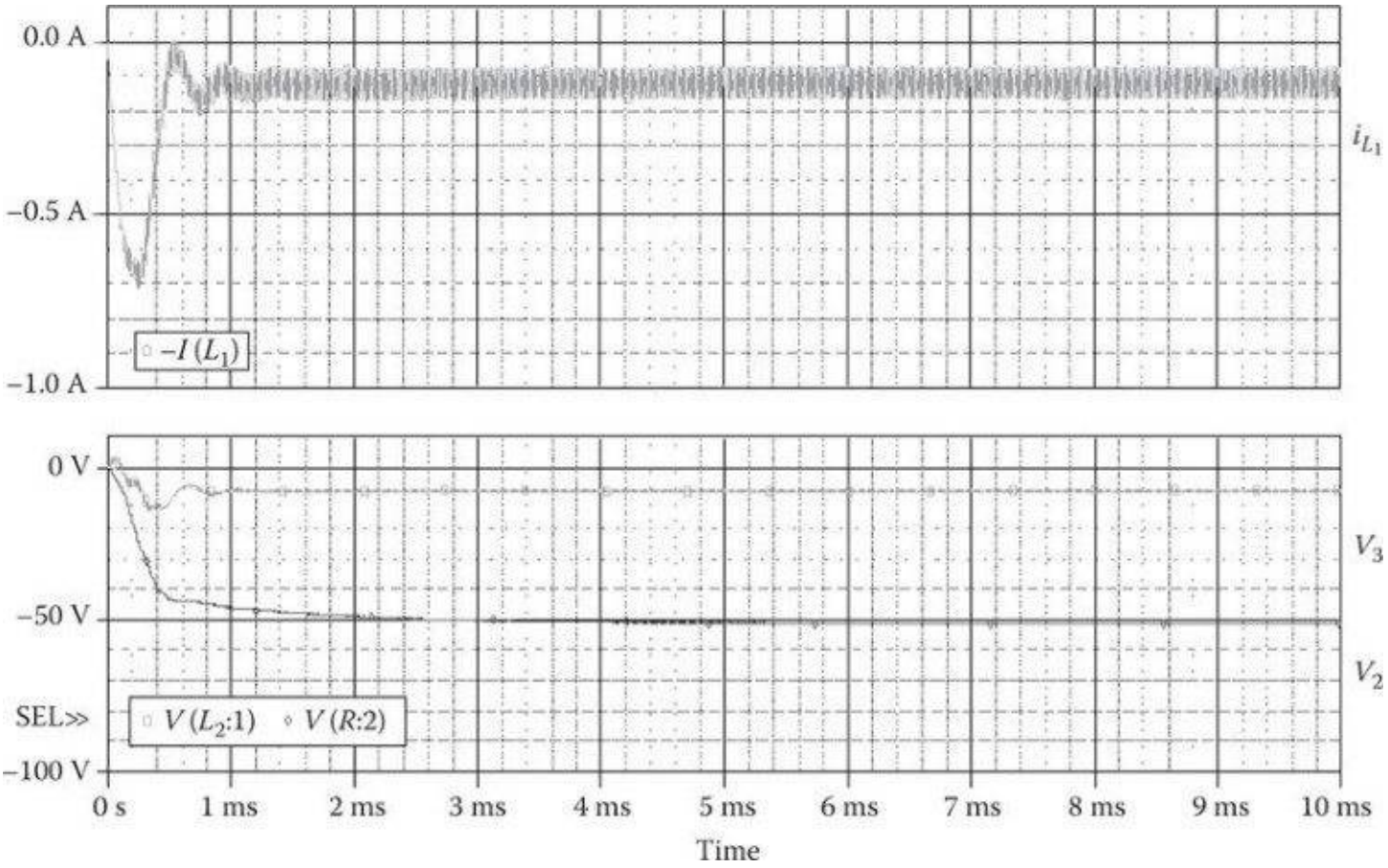


FIGURE 7.5
Simulation results for $k = 0.6$.

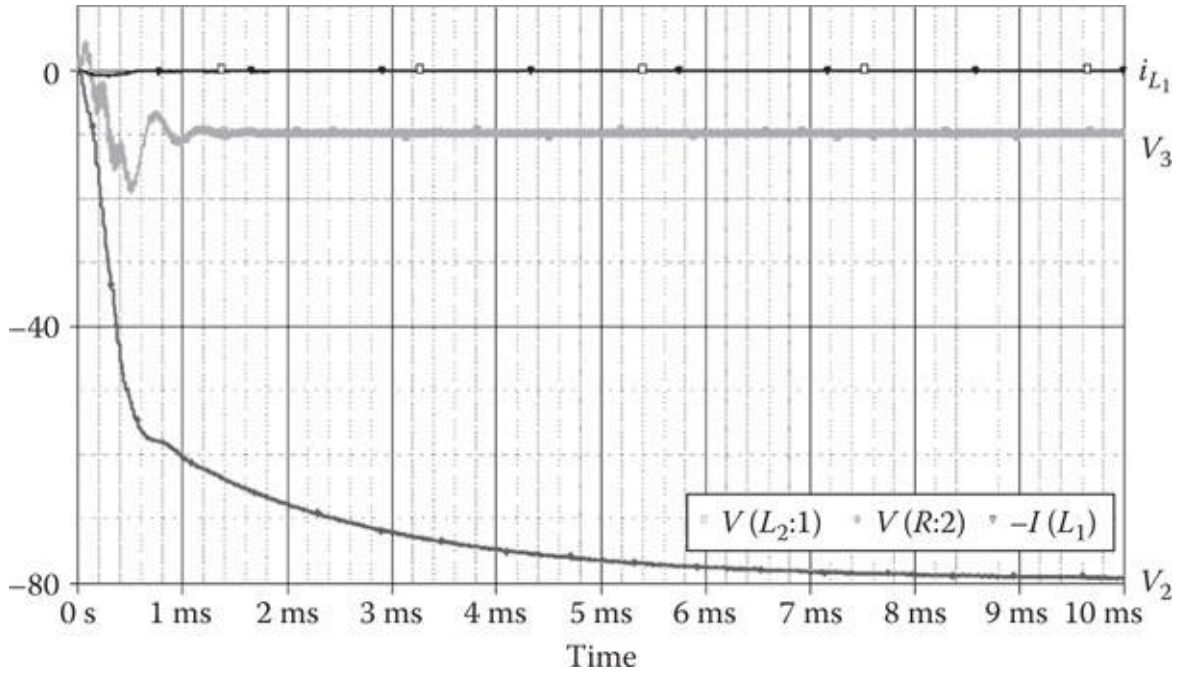


FIGURE 7.6
Simulation results for $k = 0.66$.

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7.6 Experimental Results

To verify the advantages and design of the UL Luo-converter and compare them with the simulation results, we constructed a test rig with the components: V_1 = 10 V, $L_1 = L_2$ = 1 mH, $C_1 = C_2$ = 1 μF, R = 3 kΩ, f = 50 kHz, and conduction duty cycle k = 0.6 and 0.66. The output voltage V_2 = 52 and 78 V, correspondingly. The first waveform is the inductor's current i_{L_1}, which flows through the inductor L_1. The second waveform is the output voltage V_2. The experimental results are shown in Figures 7.7 and 7.8, respectively. The test results are identical to those of the simulation results shown in Figures 7.5 and 7.6 and verify both the calculation results and our design.

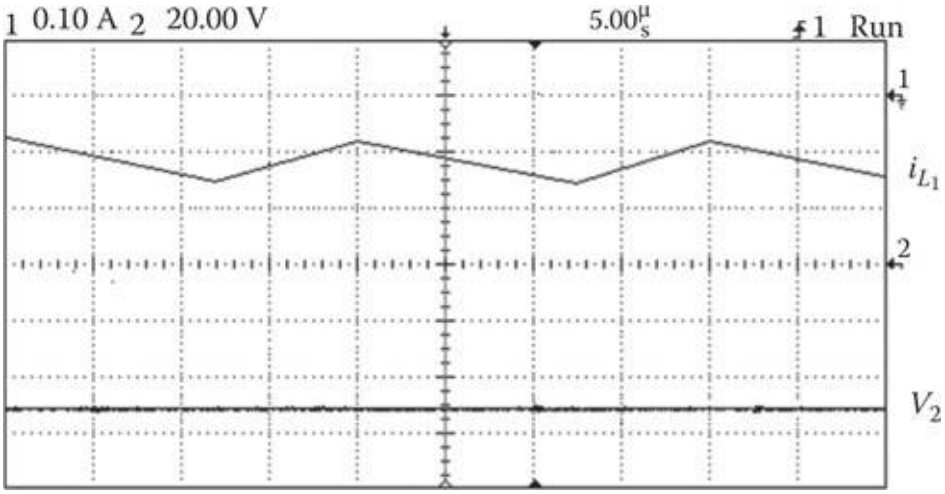


FIGURE 7.7
Experimental results for k = 0.6.

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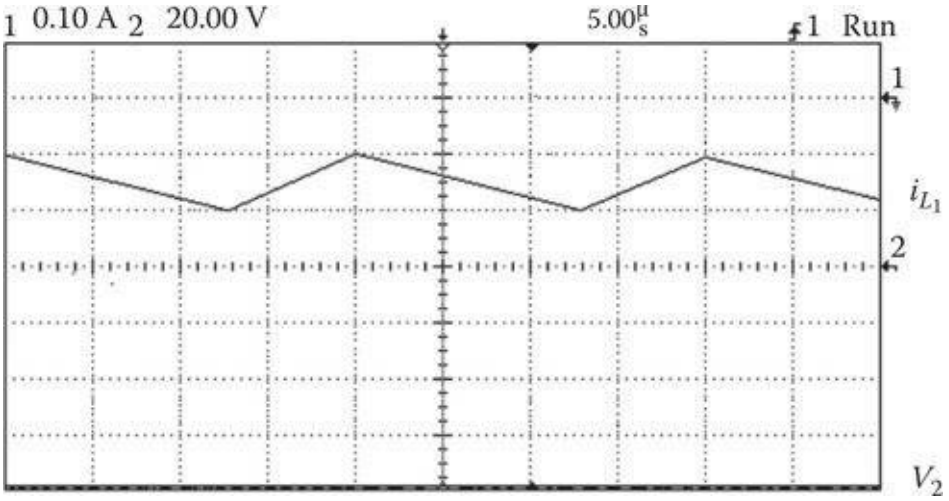


FIGURE 7.8
Experimental results for $k = 0.66$.

7.7 Summary

The UL Luo-converter has been successfully developed using the novel approach of the new technology, the UL technique, which produces especially high-voltage transfer gain. It is much higher than that of VL Luo-converters and SL Luo-converters. This chapter introduced the operation and characteristics of this converter in detail. This converter will be applied in industrial applications entailing high output voltages.

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8

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Hybrid Split Capacitors and Split Inductors Applied in Positive-Output Super-Lift Luo-Converters

Voltage-lift technique has been successfully employed in the design of DC/DC converters, for example, three-series Luo-converters. However, the output voltage increases in arithmetic progression. Super-lift (SL) technique is the most significant contribution in power electronics, for example, four-series SL converters. Their output voltage increases in geometric progression. This chapter introduces a novel approach—SL technique armed by split capacitors and split inductors that implement the output voltage increasing in especially high geometric progression. It effectively enhances the voltage transfer gain in power series as well. The simulation and experimental results verified the inventing design, and the power rates of these converters can be a few kWs.

8.1 Introduction

Voltage-lift (VL) technique is a popular method widely used in electronic circuit design. It has been successfully employed in DC/DC converter applications in recent decades and opened a way to design high-voltage-gain converters. Three-series Luo-converters are the examples of VL technique implementations. However, the output voltage increases stage by stage just along the arithmetic progression. Super-lift (SL) technique is the significant contribution in power electronics, for example, four-series SL converters. Their voltage transfer gains are high. Their output voltage increases stage by stage in geometric progression. This chapter introduces a novel approach—SL technique armed by split capacitors and split inductors that implement the output voltage increasing stage by stage along higher geometric progression. It effectively enhances the voltage transfer gain in power series as well.

In order to sort these converters from existing VL converters, we entitle these converters “positive-output super-lift Luo-converters armed by split capacitors.” There are a few subseries, and we only introduce two subseries, the main and additional series, in detail in this chapter and summarize other subseries. Each circuit of the main series and additional series has one switch S, n inductors (where n is the stage number), and some capacitors and diodes. The conduction duty ratio is k, switching frequency is f, switching period is $T = 1/f$ and the load is resistive load R. The input voltage and current are V_{in} and I_{in}, respectively; the output voltage and current are V_o and I_o, respectively. Assume no power losses during the conversion process, $V_{in} \times I_{in} = V_o \times I_o$. The voltage transfer gain is G:

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$$G = \frac{V_o}{V_{in}}$$

8.2 Split Capacitors and Split Inductors

8.2.1 Split Capacitors

A capacitor can be split into a few parts, as shown in Figure 8.1. For example, a capacitor C_1, as shown in Figure 8.1a, can be split into two parts, two capacitors C_1 and C_2, as shown in Figure 8.1b, and three parts, three capacitors C_1, C_2, and C_3, as shown in Figure 8.1c. Furthermore, a capacitor can also be split into a parts that are shown in Figure 8.1d.

The split stage can be defined as a-times. Now, we define the single capacitor to be α = 1 split stage as shown in Figure 8.1a and the two split capacitors to be α = 2 split stage as shown in Figure 8.1b, while the slave S_1 switch in the circuit is exclusively switched with the main switch; we define the three split capacitors to be α = 3 split stage as shown in Figure 8.1c, while the slave switches S_1 and S_2 are exclusively switched with the main switch. We symbolize the a split capacitors by **αC**. These capacitors can be charged by a DC voltage V_{in}. In the steady state, assume each capacitor is charged to the source voltage V_{in}. All split capacitors are charged by source voltage V_{in} in parallel. When the capacitors are discharged, all split capacitors are discharged by an external voltage in series.

8.2.2 Split Inductors

An inductor can be split into few parts, as shown in Figure 8.2. For example, an inductor L_1 as shown in Figure 8.2a can be split into two parts, two inductors L_1 and L_2, as shown in Figure 8.2b and three parts, three capacitors L_1, L_2, and L_3, as shown in Figure 8.2c. Furthermore, it can be split into ß parts that are shown in Figure 8.2d with symbolic βL.

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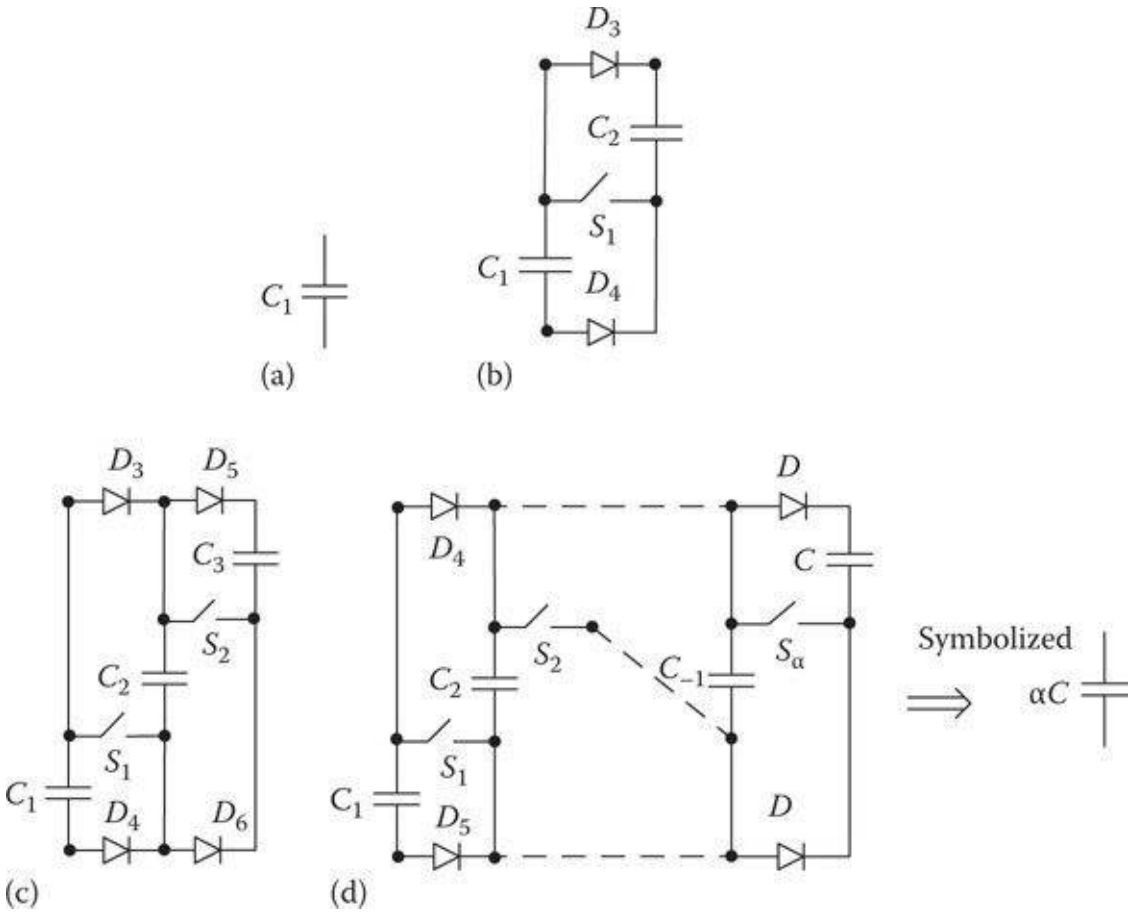


FIGURE 8.1
The single capacitor and a split capacitors. (a) One capacitor. (b) Two split capacitors. (c) Three split capacitors. (d) α split capacitors.

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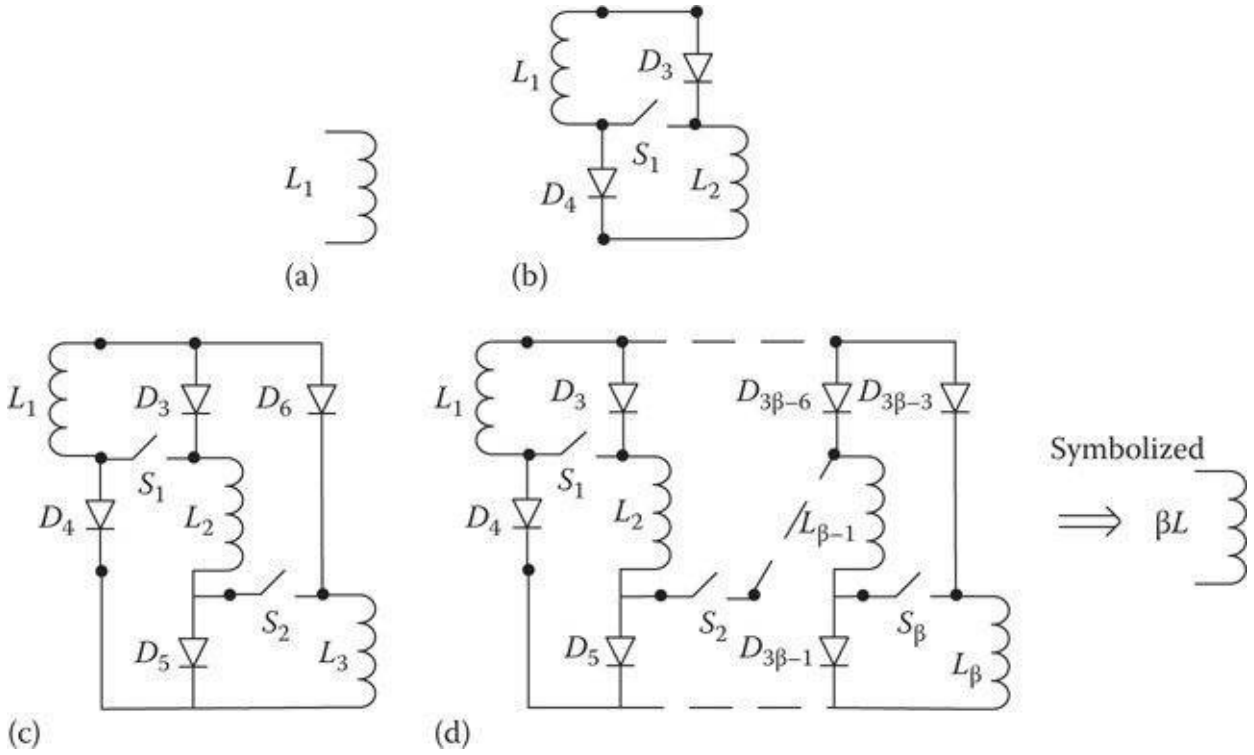


FIGURE 8.2
The single inductor and β split inductors. (a) One inductor. (b) Two split inductors. (c) Three split inductors. (d) β split inductors.

The split stage can be defined as β-times. Now, we define the single inductor to be β = 1 split stage as shown in Figure 8.2a; the two split inductors to be β = 2 split stage as shown in Figure 8.2b, while the slave switch S_1 is exclusively switched with the main switch. We define the three split inductors to be β = 3 split stage as shown in Figure 8.2c, while the slave switches S_1 and S_2 are exclusively switched with the main switch. We symbolize the β split inductors by **βL**. These inductors can be charged by a DC voltage V_n in parallel during switch-on. When the inductors are discharged, all split inductors are discharged in series.

8.3 Split Capacitors and Split Inductors Applied in the P/O Elementary Super-Lift Luo-Converter

Positive-output (P/O) elementary SL Luo-converter is shown in Figure 8.3. Its circuit diagram is shown in Figure 8.3a. Its equivalent circuits during switch-on and switch-off are shown in Figure 8.3b and c, respectively.

The voltage across capacitor C_1 is charged to V_{in} in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_0 - 2V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is

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$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_o - 2V_{in}}{L}(1-k)T \tag{8.1}$$

$$V_o = \frac{2-k}{1-k} V_{in} \tag{8.2}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2-k}{1-k} \tag{8.3}$$

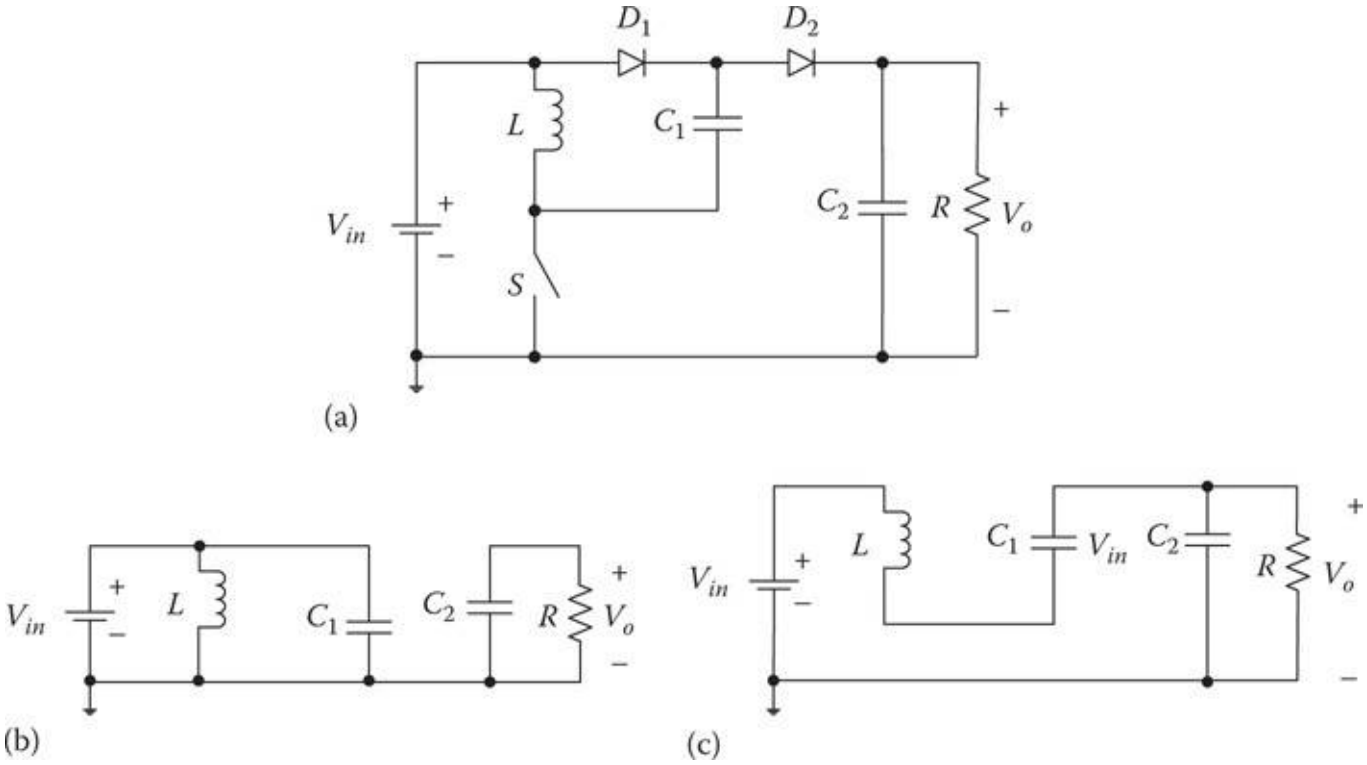


FIGURE 8.3
Positive-output elementary super-lift Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

8.3.1 Two Split Capacitors (α = 2) Applied in the P/O Elementary SL Circuit

If a capacitor C_1 is split into two capacitors C_1 and C_2, the circuit and its equivalent circuits during switch-on and switch-off will be as shown in Figure 8.4 (as mentioned, the slave switch exclusively switches with the main switch S).

The voltage across capacitors C_1 and C_2 are charged to V_{in} in the steady state. The current i_L flowing through inductor L increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_0 - 3V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_o - 3V_{in}}{L}(1-k)T \tag{8.4}$$

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$$V_o = \frac{3-2k}{1-k} V_{in} \tag{8.5}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{3-2k}{1-k} \tag{8.6}$$

8.3.2 Two Split Inductors (β = 2) Applied in the Elementary P/O SL Circuit

If the inductor L is split into two inductors L_1 and L_2, the circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 8.5 (as mentioned that the slave switch S_1 exclusively switches with the main switch S).

The inductors L_1 and L_2 are charged to V_{in} in the steady state. The current i_L flowing through each inductor increases with voltage V_{in} during switch-on period kT and decreases with voltage $-(V_0 - 2V_{in})$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is

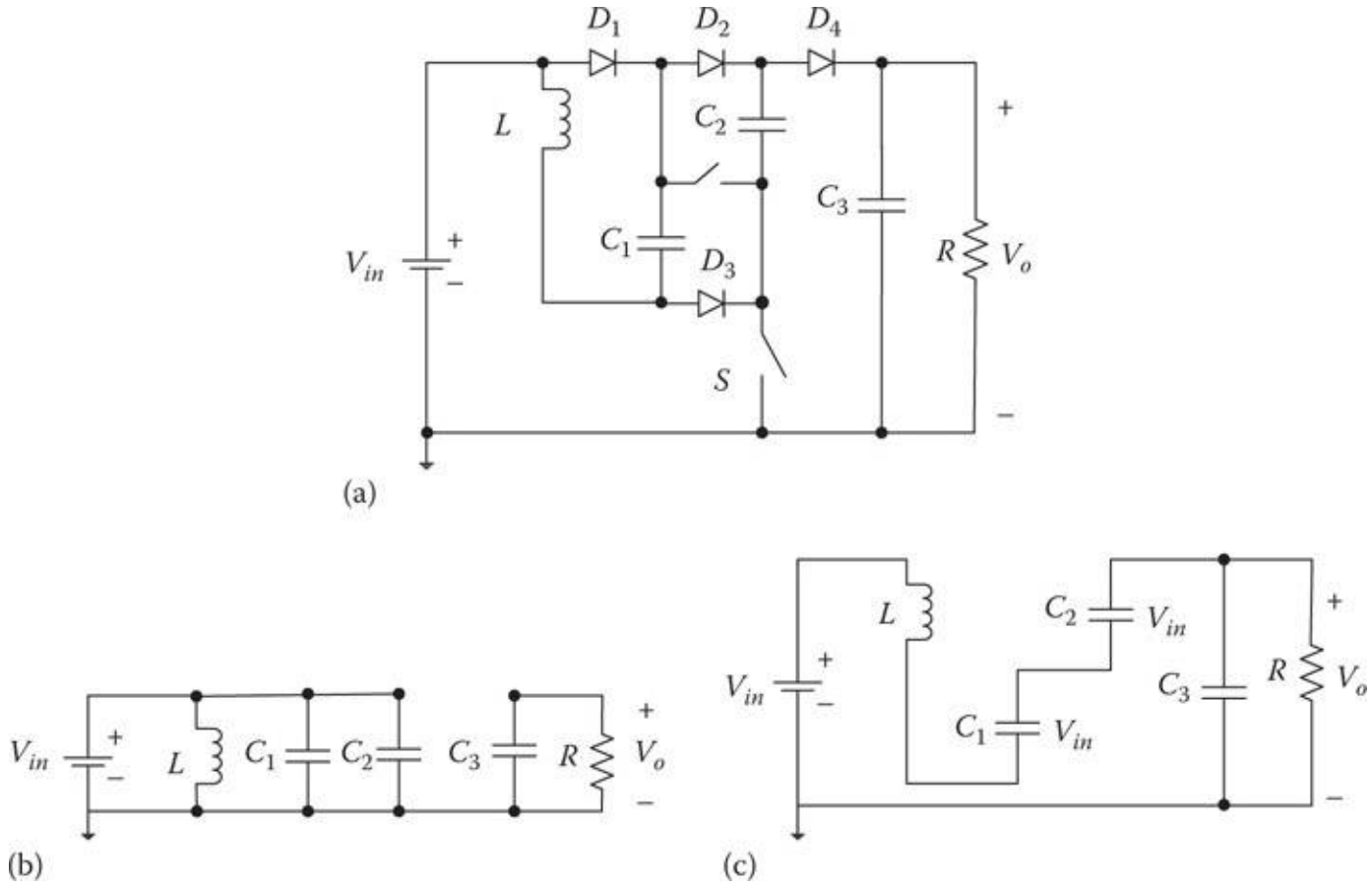


FIGURE 8.4
Two split capacitors applied in the elementary positive-output super-lift Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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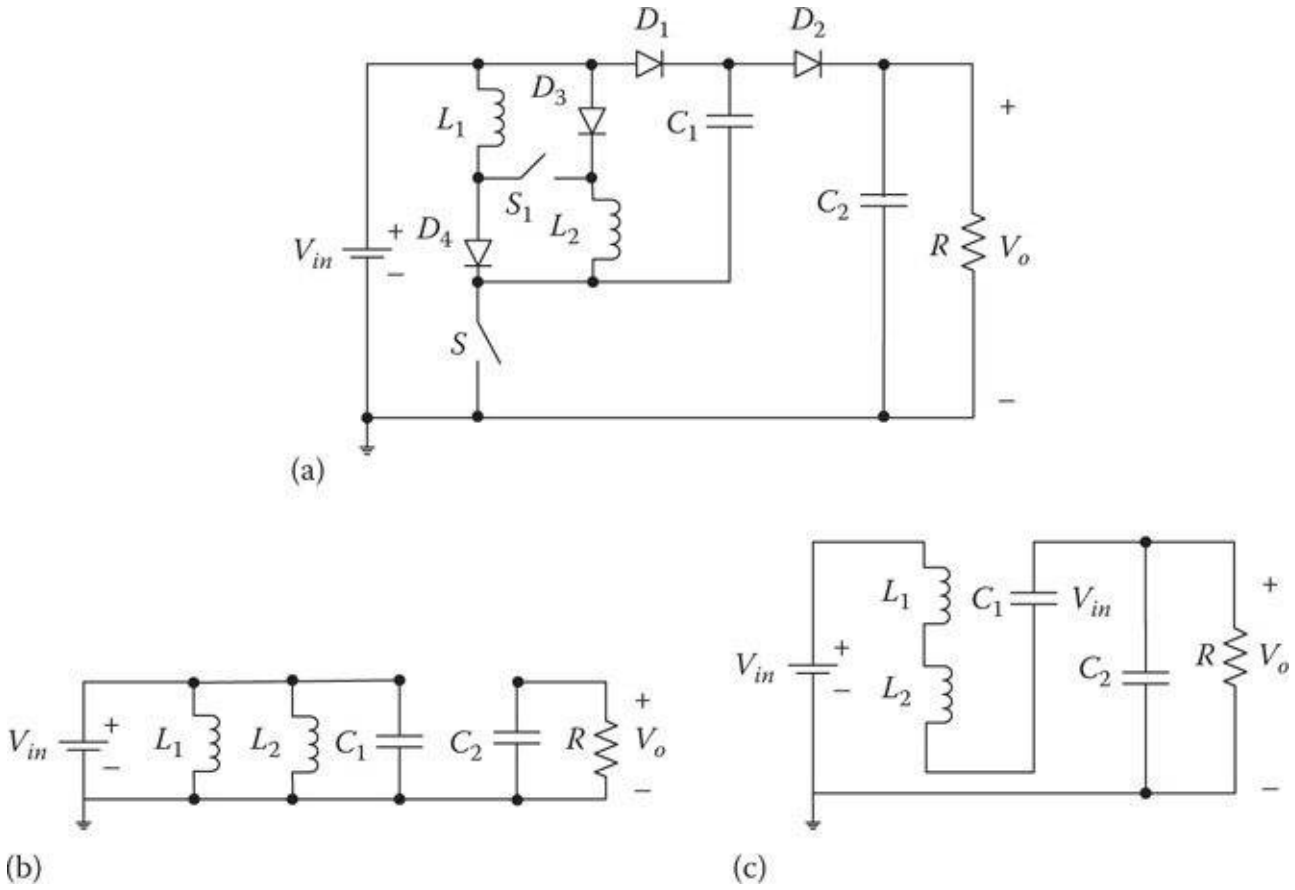


FIGURE 8.5
Two split inductors applied in the elementary positive-output super-lift Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_o - 2V_{in}}{2L}(1-k)T \tag{8.7}$$

$$V_o = \frac{2}{1-k} V_{in} \tag{8.8}$$

The voltage transfer gain is

$$G = \frac{V_o}{V_{in}} = \frac{2}{1-k} \tag{8.9}$$

8.3.3 α Split Capacitors and β Split Inductors Applied in the Elementary P/O SL Circuit

If the capacitor C_1 is split into a capacitors and the inductor L_1 is split into β inductors, the circuit is shown in Figure 8.6.

The voltage across the a capacitors is charged to V_{in} in parallel during switch-on in the steady state. The current i_L flowing through inductor β increases with voltage V_{in} during

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switch-on period kT and decreases with voltage $-[V_0 - (\alpha + 1)V_{in})]$ during switch-off period $(1 - k)T$. Therefore, the ripple of the inductor current i_L is

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_o - (\alpha + 1)V_{in}}{\beta L}(1 - k)T \tag{8.10}$$

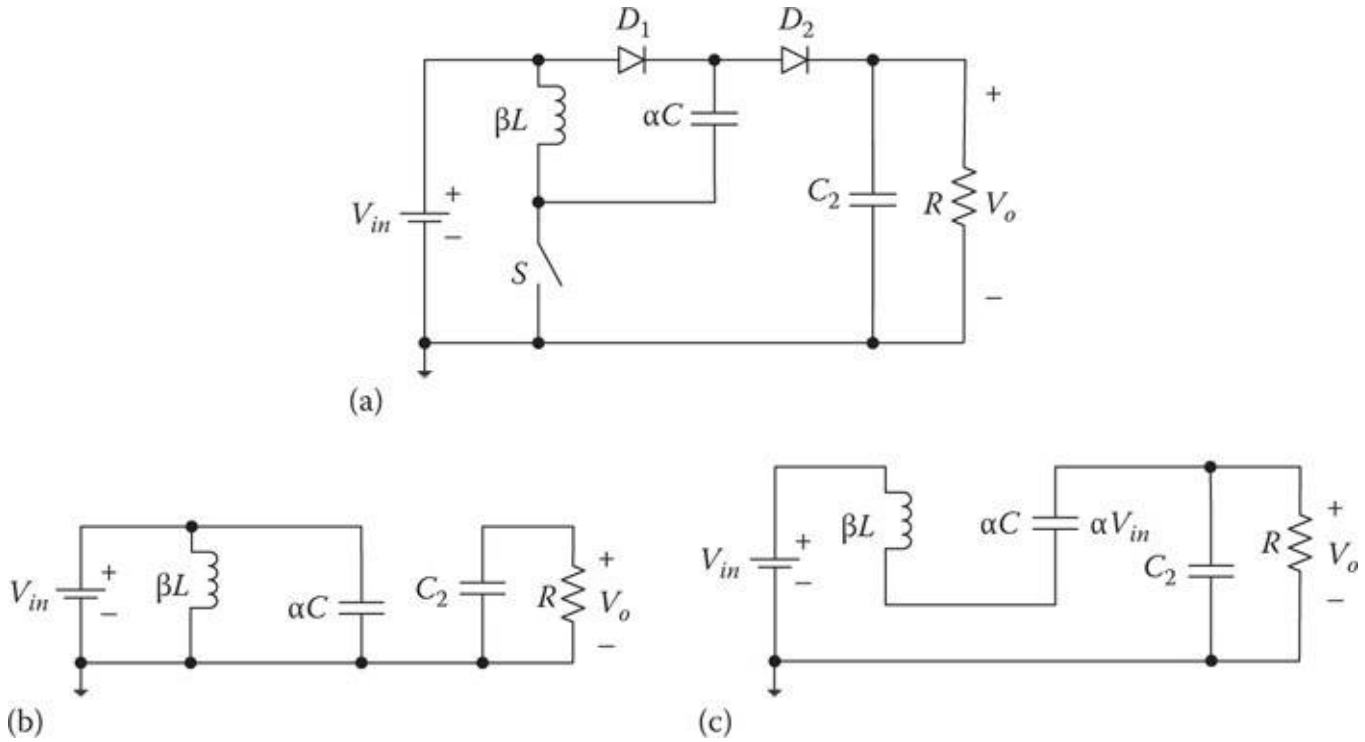


FIGURE 8.6
The a split capacitors and β split inductors applied in the elementary positive-output super-lift Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

$$V_o = \left(\alpha + 1 + \frac{\beta k}{1 - k}\right) V_{in} = \frac{(\alpha + 1) + (\beta - \alpha - 1)k}{1 - k} V_{in} \tag{8.11}$$

The voltage transfer gain is

$$G_E = \frac{V_o}{V_{in}} = \frac{\alpha + 1 + (\beta - \alpha - 1)k}{1 - k} \tag{8.12}$$

We define a new factor as

$$A = \frac{\alpha + 1 + (\beta - \alpha - 1)k}{1 - k} \tag{8.13}$$

The voltage transfer gain is

$$G_E = \frac{V_o}{V_{in}} = A$$

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8.4 Main Series

The main series has several circuits such as the elementary circuit, re-lift circuit, triple-lift circuit, and high-order lift circuits. We defined that the stage $n = 1$ means elementary circuit, $n = 2$ means re-lift circuit, $n = 3$ means triple-lift circuit, and n being a higher number means high-order lift circuit. Figure 8.7a shows the elementary circuit. Figure 8.7b shows the re-lift circuit, and Figure 8.7c shows the triple-lift circuit.

The voltage transfer gain of the re-lift circuit is

$$G_R = \frac{V_o}{V_{in}} = \left[\frac{\alpha + 1 + (\beta - \alpha - 1)k}{1 - k}\right]^2 = A^2 \tag{8.14}$$

The voltage transfer gain of the triple-lift circuit is

$$G_T = \frac{V_o}{V_{in}} = \left[\frac{\alpha + 1 + (\beta - \alpha - 1)k}{1 - k}\right]^3 = A^3 \tag{8.15}$$

If each stage uses a split capacitor αC and a split inductor βL, the voltage transfer gain of the nth-order lift circuit is

$$G_n = \frac{V_o}{V_{in}} = \left[\frac{\alpha + 1 + (\beta - \alpha - 1)k}{1 - k}\right]^n = A^n \tag{8.16}$$

It is a very high-voltage transfer gain. For example, if $V_{in} = 20$ V, $n = 3$, $\alpha = 3$, $\beta = 3$, and $k = 0.5$, we obtain $A = 7$, and the voltage transfer gain G_T is equal to 343. The output voltage is 6860 V.

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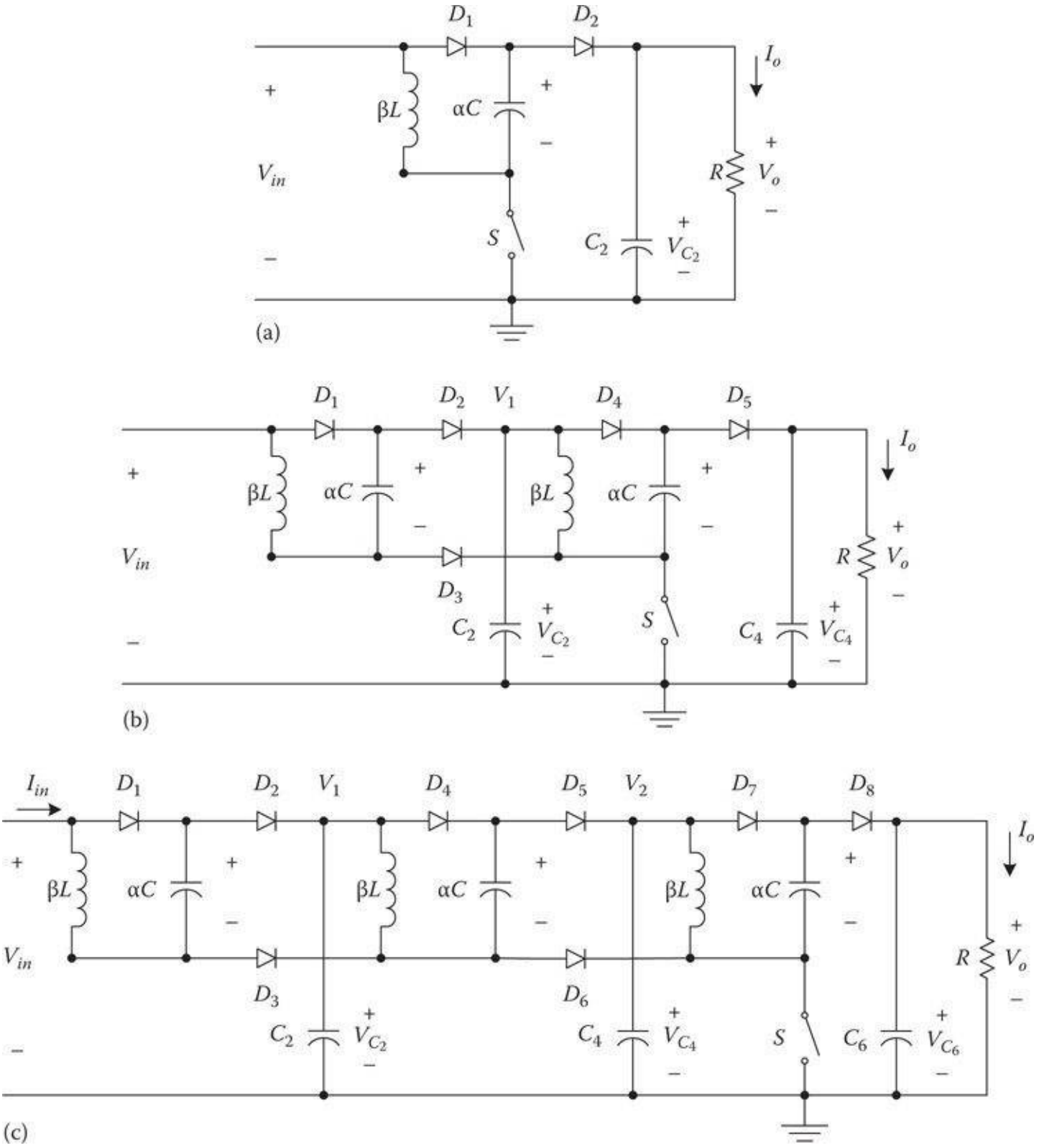


FIGURE 8.7
The elementary, re-lift, and triple-lift circuits. (a) The elementary circuit. (b) The re-lift circuit. (c) The triple-lift circuit.

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8.5 MEC, Split Capacitors Used in DEC

The original double/enhanced circuit is shown in Figure 8.8a, which consists of two diodes (D_{11} and D_{12}) and two capacitors (C_{11} and C_{12}). During switch-on period kT, capacitor C_{11} is charged to the source voltage V_{in}. During switch-off period $(1 - k)T$, the source voltage V_{in} and capacitor C_{11} is in series to supply capacitor C_{12}. Therefore, the output voltage is

$$V_o = 2V_{in} \tag{8.17}$$

If the capacitor C_{11} is replaced by a γ-split capacitor γC and the switch S is a two-pole and two-throw switch (as shown in Figure 8.8b), we call it multiple-enhanced circuit (MEC).

The output voltage will be

$$V_o = (\gamma + 1)V_{in} \tag{8.18}$$

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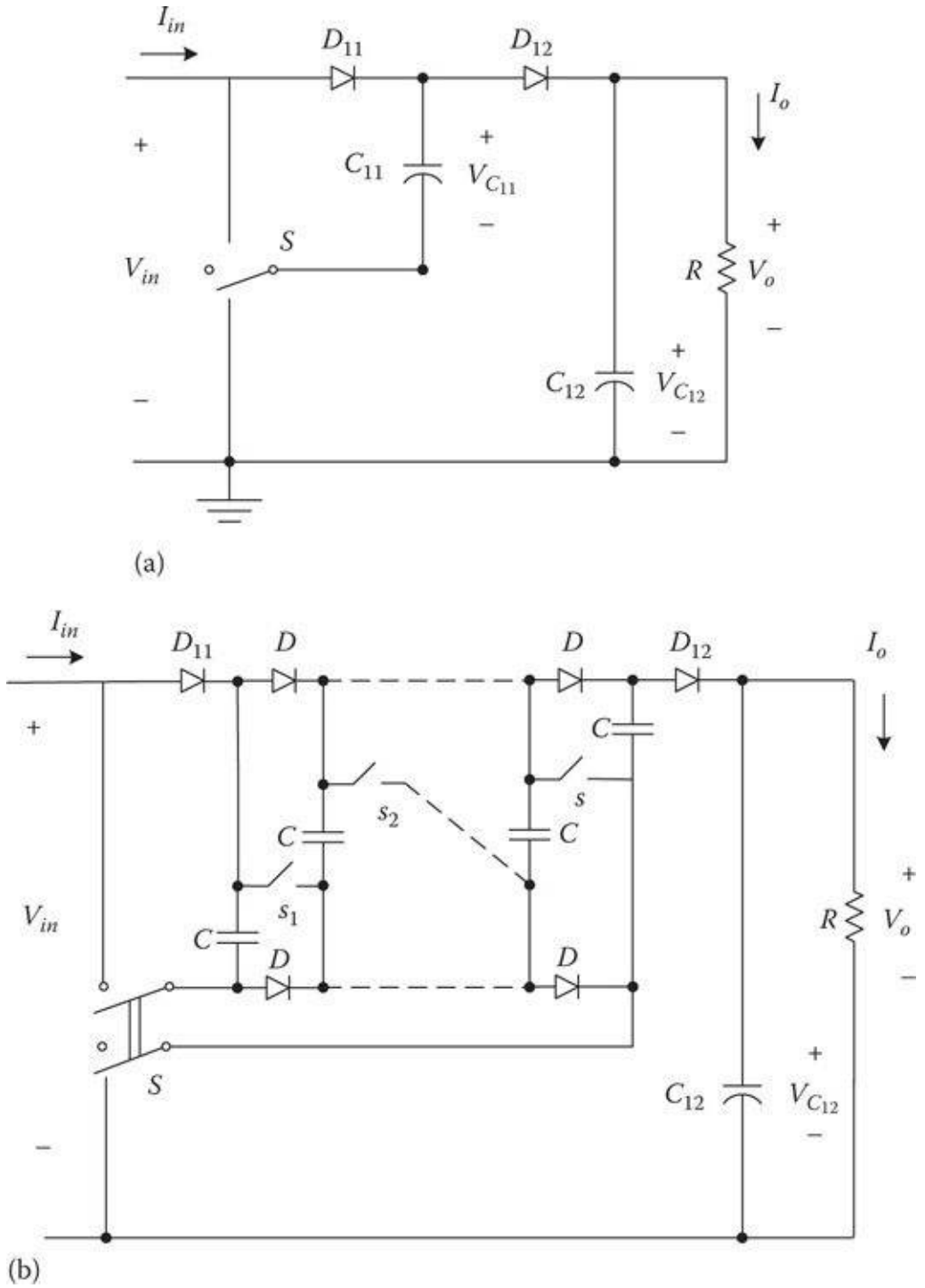


FIGURE 8.8
The double/enhanced circuit and multiple-enhanced circuit. (a) The double/enhanced circuit (DEC). (b) Multiple/enhanced circuit (MEC).

8.6 Additional Series

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All circuits of P/O SL converters—additional series—are derived from the corresponding circuits of the main series. By adding an MEC after the main circuits, we obtain the circuits of the additional series.

The first three stages of this series are shown in Figures 8.9 and 8.10a and b. For convenience, we call them elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit, respectively, with $n = 1, 2$, and 3.

8.6.1 Elementary Additional Circuit

This circuit is derived from an elementary circuit by adding an MEC (D_{11}–D_{12}–γCγC_{12}). Its circuit and switch-on and switch-off equivalent circuits are shown in Figure 8.9.

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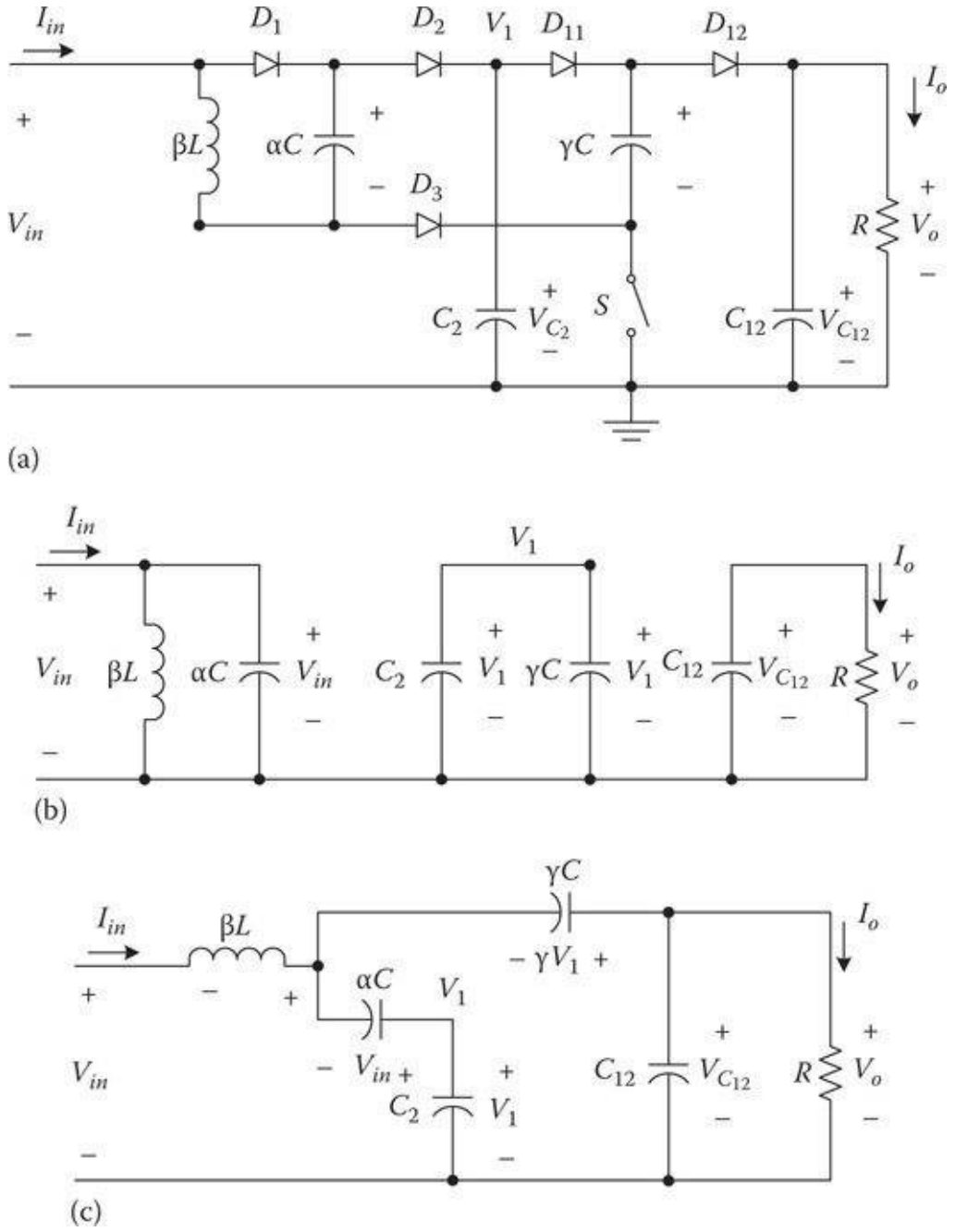


FIGURE 8.9
Elementary additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on. (c) Equivalent circuit during switch-off.

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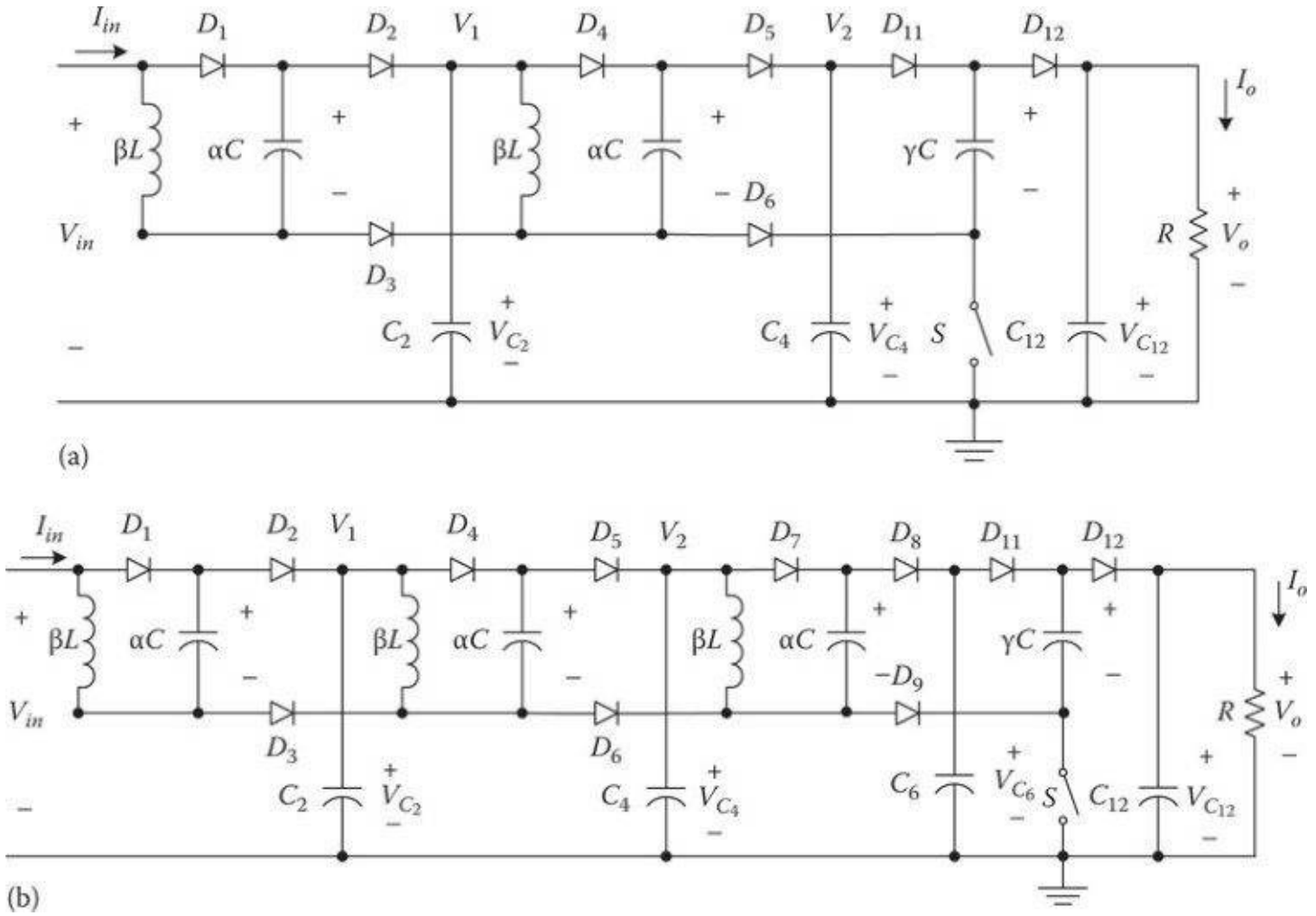


FIGURE 8.10
Re-lift and triple-lift additional circuits. (a) Re-lift additional circuit. (b) Triple-lift additional circuit.

The voltage across all capacitor αC_2 is V_1 in steady state as shown in Equation 8.11. The inductor current increases during switch-on S and decreases during switch-off S. The current variation is

$$\frac{V_{in}}{L}kT = \frac{V_o - \gamma V_1 - V_{in}}{\beta L}(1-k)T \tag{8.19}$$

and

$$V_1 = \frac{\alpha + 1 + (\beta - \alpha - 1)k}{1-k} V_{in} = AV_{in}$$

Therefore, the output voltage V_o is

$$V_o = \left[\frac{\beta k}{1-k} + 1 + \gamma \frac{\alpha + 1 + (\beta - \alpha - 1)k}{1-k}\right] V_{in} \tag{8.20}$$

We define another new factor as

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$$B=\frac{\beta k}{1-k}+1+\gamma\frac{\alpha+1+(\beta-\alpha-1)k}{1-k} \tag{8.21}$$

The voltage transfer gain G is

$$G_{E-A}=\frac{V_o}{V_{in}}=B$$

8.6.2 Re-Lift Additional Circuit

This circuit is derived from an elementary additional circuit by adding MEC parts ($\beta L-D_3-D_4-D_5-\alpha C-C_4$). Its circuit diagram is shown in Figure 8.10a.

The voltage across capacitor C_2 is charged to V_1, and the voltage across capacitor C_4 is charged to V_2. All yC is charged to V_2. The V_2 is shown in Equation 8.14. The second inductor current increases during switch-on S and decreases during switch-off S. The current variation is

$$\frac{V_1}{L_2}kT=\frac{V_o-\gamma V_2-V_1}{\beta L_2}(1-k)T \tag{8.22}$$

and

$$V_2=\frac{\alpha+1+(\beta-\alpha-1)k}{1-k}V_1=AV_1$$

Therefore, the output voltage V_o is

$$\begin{aligned}V_o&=\frac{V_1}{1-k}+\gamma V_2=\left[\frac{\beta k}{1-k}+1+\gamma\frac{\alpha+1+(\beta-\alpha-1)k}{1-k}\right]V_1\\&=\left[\frac{\beta k}{1-k}+1+\gamma\frac{\alpha+1+(\beta-\alpha-1)k}{1-k}\right]\left[\frac{\alpha+1+(\beta-\alpha-1)k}{1-k}\right]V_{in}=BAV_{in}\end{aligned} \tag{8.23}$$

The voltage transfer gain G is

$$G_{R-A}=\frac{V_o}{V_{in}}=BA$$

8.6.3 Triple-Lift Additional Circuit

This circuit is derived from the re-lift additional circuit by adding the MEC parts ($\beta L-D_6-D_7-D_8-\alpha C-C_6$). Its circuit diagram is shown in Figure 8.10b.

The voltage across capacitor C_2 is charged to V_1. The voltage across capacitor C_4 is charged to V_2, and the voltage across capacitor C_6 is charged to V_3. All γC is charged to V_3, as shown in Equation 8.16. The inductor current increases during switch-on S and decreases during switch-off S. The current variation is

$$\frac{V_2}{L_3}kT=\frac{V_o-\gamma V_3-V_2}{\beta L_3}(1-k)T \tag{8.24}$$

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and

$$V_3 = \frac{\alpha + 1 + (\beta - \alpha - 1)k}{1-k} V_2 = AV_2$$

$$V_2 = \left[\frac{\alpha + 1 + (\beta - \alpha - 1)k}{1-k}\right]^2 V_{in} = A^2 V_{in}$$

Therefore, the output voltage V_o is

$$V_o = \frac{\beta k}{1-k} V_2 + V_2 + \gamma V_3 = \left[\frac{\beta k}{1-k} + 1 + \gamma\left(\frac{\alpha + 1 - \alpha k}{1-k}\right)\right] V_2 = BA^2 V_{in} \tag{8.25}$$

The voltage transfer gain G is

$$G_{T-A} = \frac{V_o}{V_{in}} = BA^2$$

8.6.4 Higher-Order Lift Additional Circuits

Higher-order lift additional circuits can be designed by multiply repeating the MEC parts "$\beta L - D_{3n-3} - D_{3n-2} - D_{3n-1} - \alpha C - C_{2n}$, where n = 2, 3, 4…." For nth-order lift additional circuit, the final voltage transfer gain is

$$G_{n-A} = \frac{V_o}{V_{in}} = BA^{n-1} \tag{8.26}$$

8.7 Synthesis of Main Series and Additional Series P/O SL Luo-Converters

All circuits of P/O SL Luo-converters using split capacitors αC, split inductors βL, and MEC (with γC) as a family can be shown in Figure 8.11 (the family tree). From the analysis of the previous two sections, we can have the following common formula to calculate the output voltage:

$$V_o = \begin{cases} A^n V_{in} & \text{Main_series} \\ BA^{n-1} V_{in} & \text{Additional_series} \end{cases} \tag{8.27}$$

The voltage transfer gain is

$$G = \begin{cases} A^n & \text{Main_series} \\ BA^{n-1} & \text{Additional_series} \end{cases} \tag{8.28}$$

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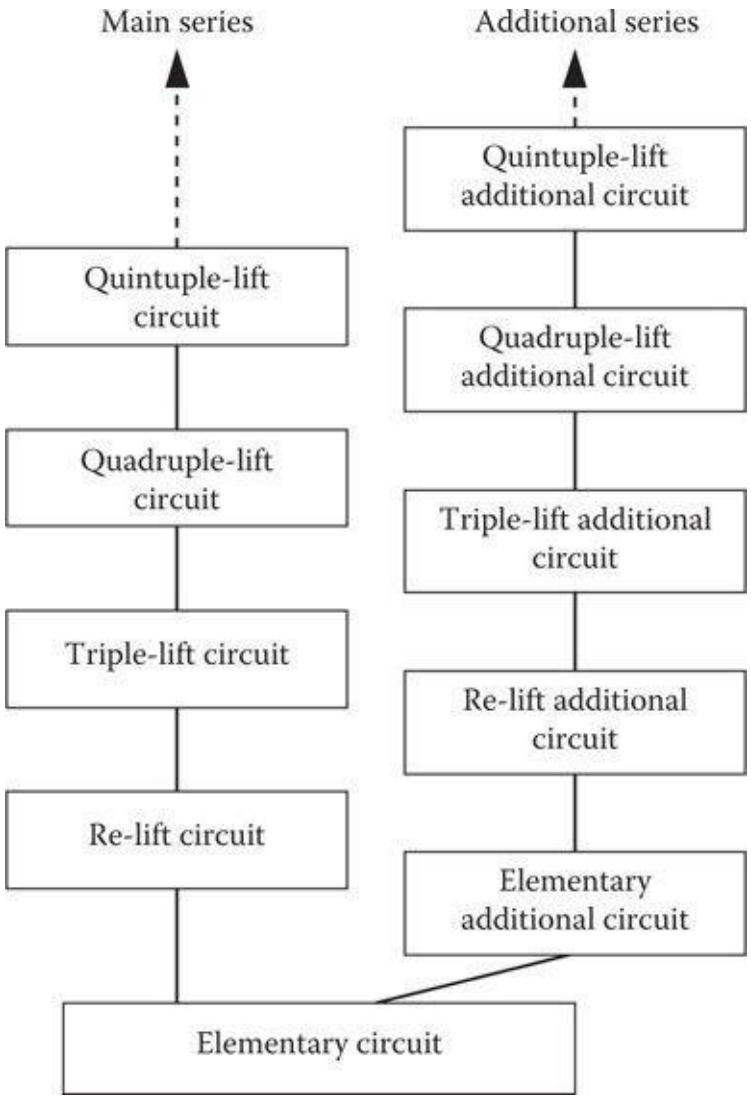


FIGURE 8.11
The family tree of positive-output super-lift Luo-converters applying capacitors and split inductors.

8.8 Simulation Results

To verify the design and calculation results, PSim simulation package was applied to these converters. For all circuits under simulation test, we choose V_{in} = 20 V, all inductors are 10 mH, all capacitances are 2 μF, R = 10 ~ 50 kΩ, k = 0.5, and f = 50 kHz.

8.8.1 Simulation Results of a Re-Lift Circuit

We apply V_{in} = 20 V to a re-lift circuit (with n = 2, α = 2, and β = 2) (see Figure 8.7a) and obtain the output voltage V_o = 500 V. The simulation results are shown in Figure 8.12a. The voltage values match the calculated results.

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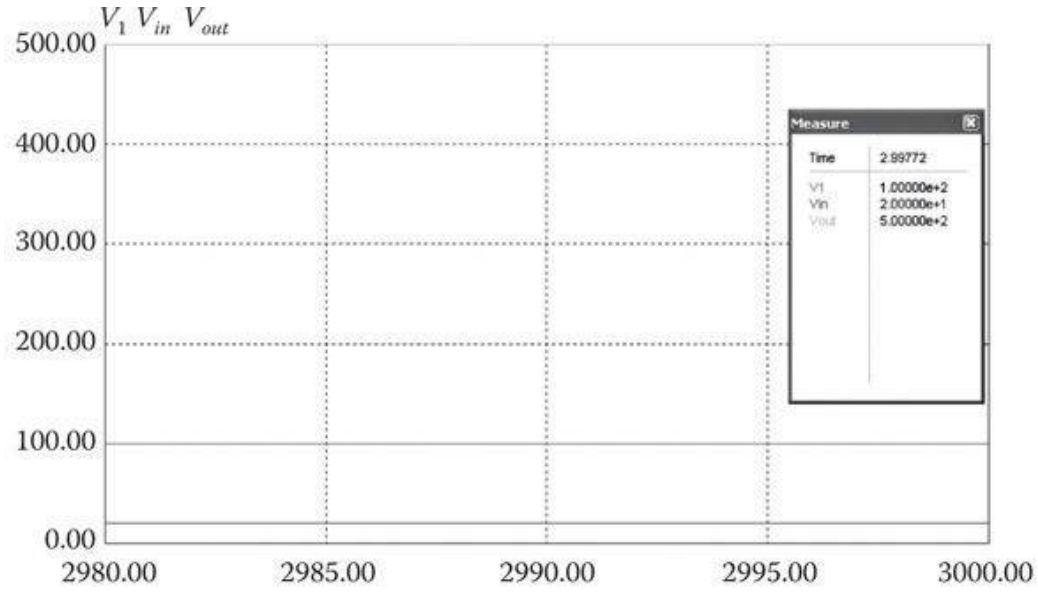
8.8.2 Simulation Results of a Triple-Lift Circuit

We apply V_{in} = 20 V to a triple-lift circuit (with n = 3, α = 2, and β = 2) (see Figure 8.7b) and obtain the output voltage V_o = 2500 V. The simulation results are shown in Figure 8.12b. The voltage values match the calculated results.

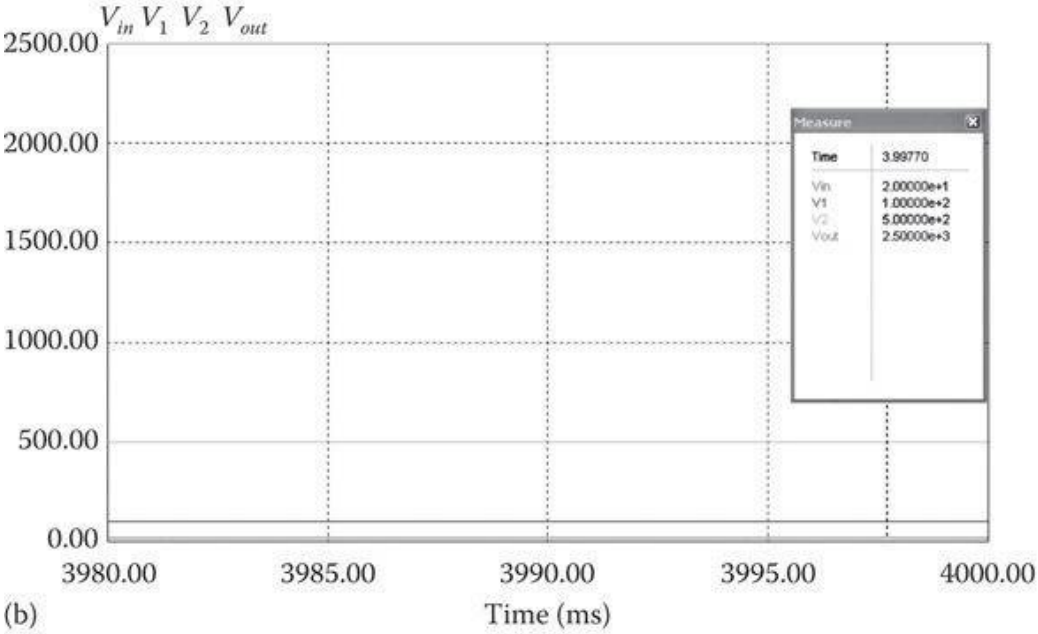
8.8.3 Simulation Results of a Re-Lift Additional Circuit

We apply V_{in} = 20 V to a re-lift additional circuit (with n = 2, α = 2, β = 2, and γ = 2) (see Figure 8.10a) and obtain the output voltage V_o = 1300 V. The simulation results are shown in Figure 8.12c. The voltage values are equal to the calculated results.

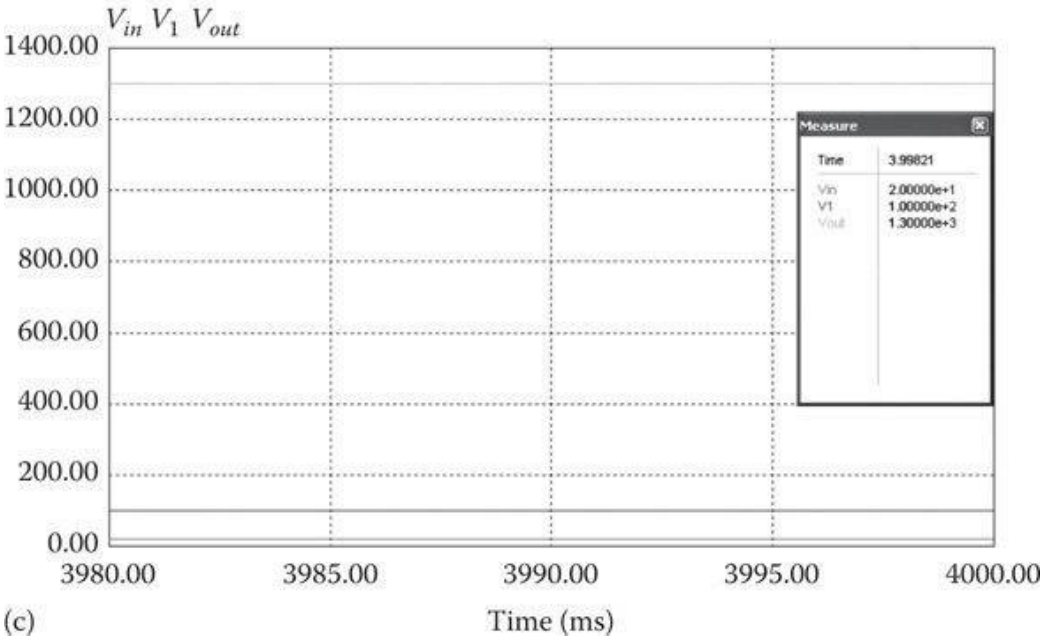
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(a)



(b)



(c)

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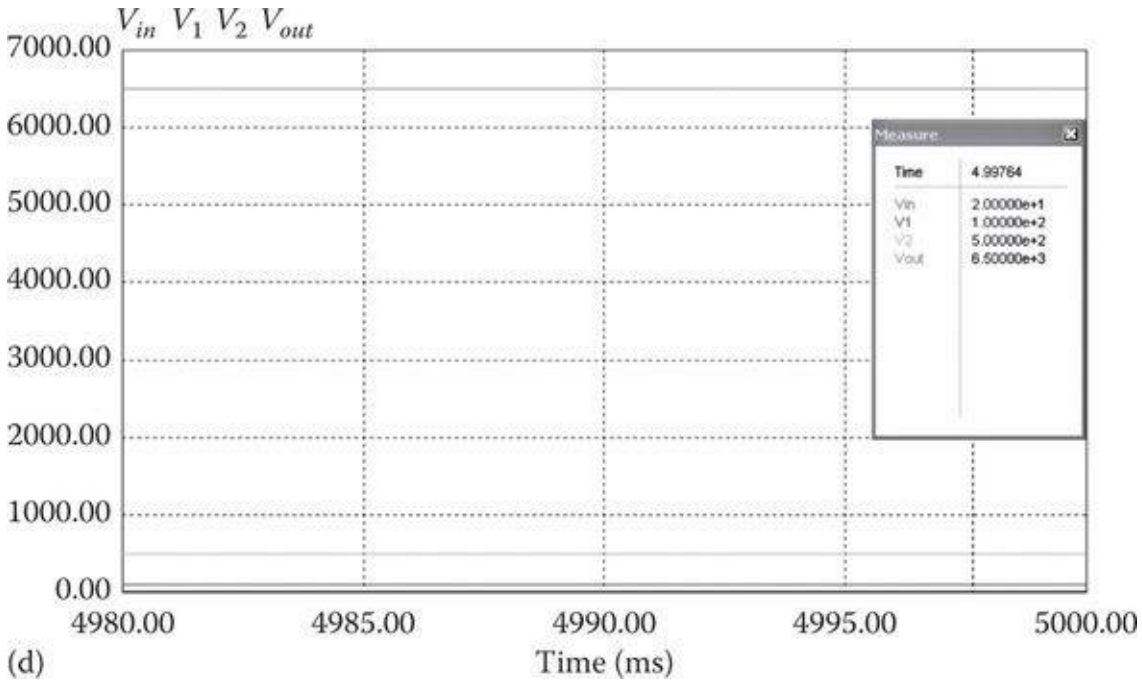


FIGURE 8.12
Simulation results. (a) Re-lift circuit. (b) Triple-lift circuit. (c) Re-lift additional circuit. Simulation results. (d) Triple-lift additional circuit.

8.8.4 Simulation Results of a Triple-Lift Additional Circuit

We apply V_{in} = 20 V to a re-lift additional circuit (with n = 3, α = 2, β = 2, and ms = 2) (see Figure 8.10b) and obtain the output voltage V_o = 6500 V. The simulation results are shown in Figure 8.12d. The voltage values match well the calculated results.

8.9 Experimental Result

A test rig was constructed to verify the design and calculation results and compared with PSim simulation results. We still choose V_{in} = 20 V, all inductors are 10 mH, all capacitances are 2 μF, R = 10 ~ 50 kΩ, k = 0.5, and f = 50 kHz. The component of the switch is a MOSFET device IRF950 with the rates 7500 V/5 A/2 MHz. We measured the values of the input and output voltages in the following converters. We showed the input and output voltages as the oscilloscope has only two channels.

8.9.1 Experimental Results of a Re-Lift Circuit

After carefully measuring a re-lift circuit (with n = 2, α = 2, and β = 2), we obtained the input voltage value V_{in} = 20 V (shown in Channel 1 with 5.0 V/Div) and the output voltage value V_o = 500 V (shown in Channel 2 with 50 V/Div). The experimental results, shown in Figure

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8.13a, are identical to the calculated and simulation results with V_{in} = 20 V and V_o = 500 V, as shown in Figure 8.12a.

8.9.2 Experimental Results of a Triple-Lift Circuit

After carefully measuring a triple-lift circuit (with n = 3, α = 2, and β = 2), we obtained the input voltage value V_{in} = 20 V (shown in Channel 1 with 5.0 V/Div) and the output voltage value V_o = 2500 V (shown in Channel 2 with 500 V/Div). The experimental results are shown in Figure 8.13b, which are the same as the calculated and simulation results (V_{in} = 20 V and V_o = 2500 V, as shown in Figure 8.12b).

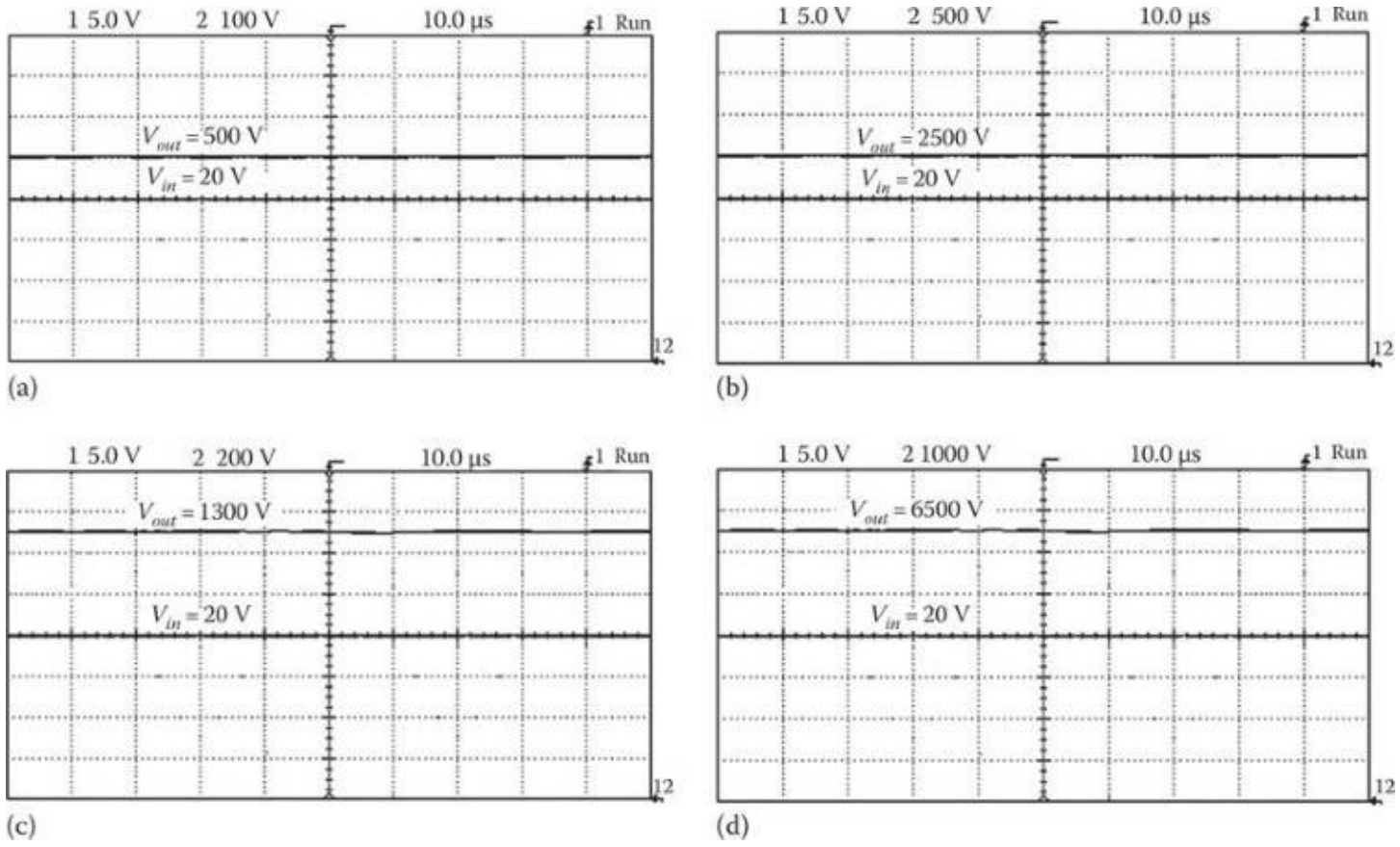


FIGURE 8.13
Experimental results. (a) Re-lift circuit. (b) Triple-lift circuit. (c) Re-lift additional circuit. (d) Triple-lift additional circuit.

8.9.3 Experimental Results of a Re-Lift Additional Circuit

After carefully measuring a re-lift additional circuit (with n = 2, α = 2, β = 2, and γ = 2), we obtained the input voltage value V_{in} = 20 V (shown in Channel 1 with 5.0 V/Div) and the output voltage value V_o = 1300 V (shown in Channel 2 with 200 V/Div). The experimental results are shown in Figure 8.13c, which are identically equal to the calculated and simulation results (V_{in} = 20 V and V_o = 1300 V, as shown in Figure 8.12c).

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8.9.4 Experimental Results of a Triple-Lift Additional Circuit

After carefully measuring a re-lift additional circuit (with n = 3, α = 2, β = 2, and γ = 2), we obtained the input voltage value V_{in} = 20 V (shown in Channel 1 with 5.0 V/Div) and the output voltage value V_o = 6500 V (shown in Channel 2 with 1000 V/Div). The experimental results are shown in Figure 8.13d, which are the same as the calculated and simulation results (V_{in} = 20 V and V_o = 6500 V, as shown in Figure 8.12d).

8.10 Transient Process Waveforms

The transient process waveforms are shown in Figure 8.14. We still choose the same condition V_{in} = 20 V, all inductors are 10 mH, all capacitances are 2 μF, R = 10 kΩ, k = 0.5, and f = 50 kHz. The component of the switch is a MOSFET device IRF950 with the rates 7500 V/5 A/2 MHz. We measured the input and output voltages and the input and output currents of a re-lift converter (with n = 2, α = 2, and β = 2). Very heavy vibration is in the first few seconds. We obtained the input voltage value V_{in} = 20 V and the output voltage V_o = 500 V at t = 2.5 s in screen 1 (top in Figure 8.14). We also obtained the input current i_{in} and the output current i_o in screen 2 (bottom in Figure 8.14). The output current i_o = 0.05 A at t = 2.5 s. The input current i_{in} looks as a pulse train with a peak value of about 11.2 A (the average value is about 1.25−1.3 A). The efficiency η is about 80%–90%.

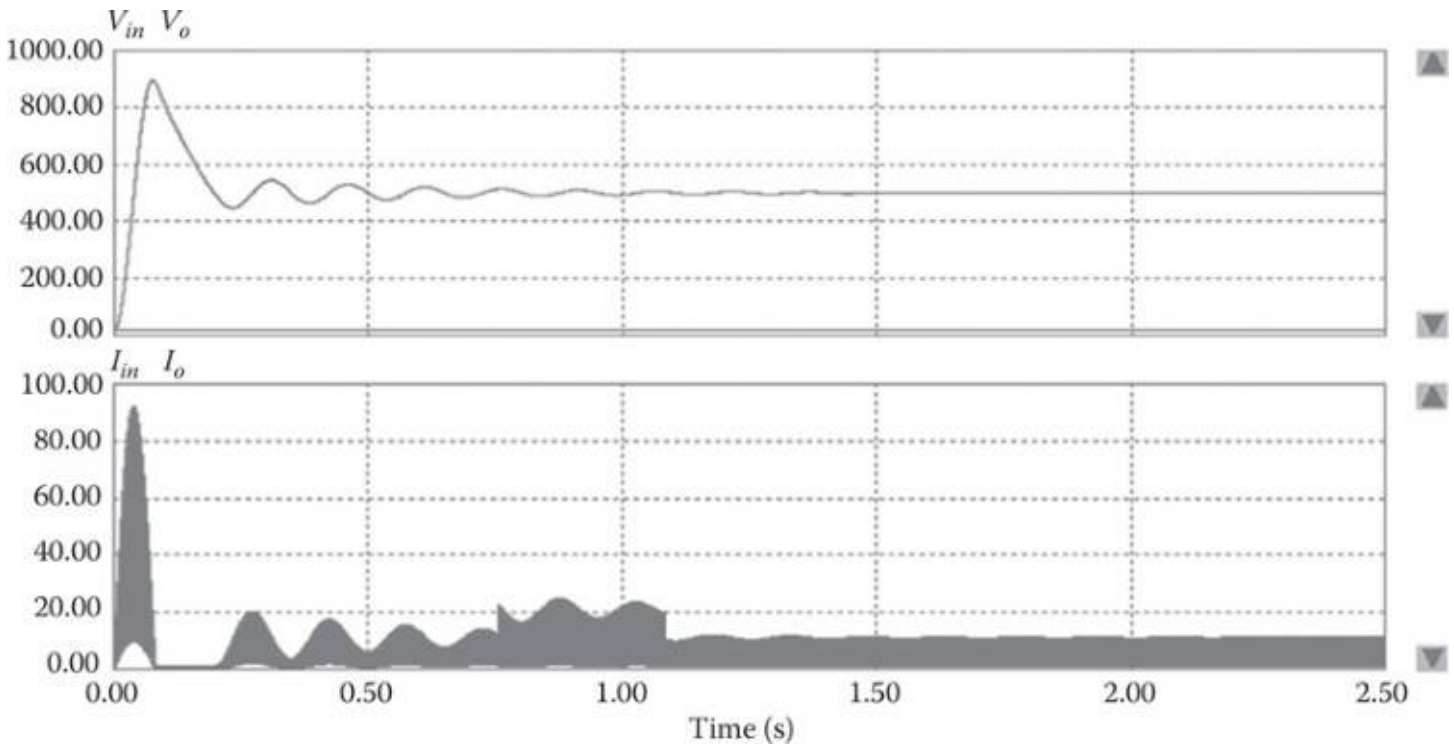


FIGURE 8.14
The transient waveforms of a re-lift circuit.

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8.11 Summary

A new method to enhance the voltage transfer gain of DC/DC converters—split capacitors and split inductors applied in P/O SL Luo-converters—has been successfully created. It largely increases the voltage transfer gain in power series. Very high output voltage is easily obtained. Simulation and experimental results verified our design and calculations. These series Luo-converters can be applied in industrial applications with very high output voltage. From our experimental results, the power rates of these converters can be a few kWs.

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9

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Mathematical Modeling of Power DC/DC Converters

Mathematical modeling for power DC/DC converters is a historical problem accompanying DC/DC conversion technology since 1940s. Many experts such as Sira-Ramirez, Cúk, Middlebrook, Smedley, and Lee have contributed in this area. The traditional mathematical modeling is not available for complex structure converters since their differential equations' order increases very high. We have to search other way to establish mathematical modeling for power DC/DC converters.

Energy storage in power DC/DC converters has been paid attention long time ago. Unfortunately, there is no clear concept to describe the phenomena and reveal the relationship between the stored energy (SE) and the characteristics of power DC/DC converters. We have theoretically defined a new concept—*energy factor (EF)* in this chapter—and researched the relations between EF and the mathematical modeling for power DC/DC converters. EF is a new concept in power electronics and conversion technology, which completely differs from the traditional concepts such as power factor, power transfer efficiency (η), total harmonic distortion, and ripple factor. EF and the subsequential EF_V (and EF_{VD}) can illustrate the system stability, reference response, and interference recovery. This investigation is very helpful for system design and characteristics foreseeing of DC/DC converters. Two DC/DC converters, namely, buck converter and super-lift Luo-converter, as the examples are analyzed in this chapter to demonstrate the applications of *EF*, EF_V (and EF_{VD}), pumping energy, SE, variation of stored energy (and VE_D), time constant τ, and damping time constant τ_d.

9.1 Introduction

Mathematical modeling for power DC/DC converters is a historical problem accompanying DC/DC conversion technology development since the 1940s. Fundamental DC/DC converters have been derived from choppers. The preliminary work on the mathematical modeling for power DC/DC converters followed the traditional calculation manner using impedance analysis to write transfer function in s-domain (Laplace transform). For example, a buck converter shown in Figure 9.1 consists of one inductor *L* and one capacitor *C* with load *R* and has the transfer function

$$G(s) = \frac{M}{1 + s(L/R) + s^2 LC} = \frac{M}{1 + s\tau + s^2 \tau\tau_d} \tag{9.1}$$

where *M* is the voltage transfer gain in steady state.

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$$M = \frac{V_2}{V_1} = k \tag{9.2}$$

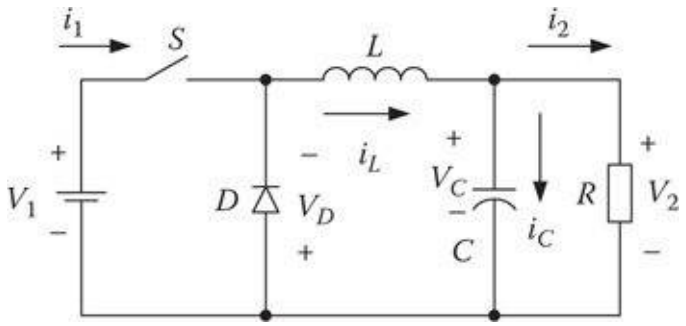


FIGURE 9.1
Buck converter.

τ is the time constant

$$\tau = \frac{L}{R} \tag{9.3}$$

τ_d is the damping time constant

$$\tau_d = RC \tag{9.4}$$

s is the Laplace operator in *s*-domain.

It is a second-order transfer function in *s*-domain. The corresponding dynamic equation is a second-order differential equation. This mathematical model is available for the case with *no* power losses during the conversion process. It describes the characteristics of a buck converter: stability, transient process, unit-step response (settling time), and impulse response (interference recovering time). For example, if the values of the components are V_1 = 40 V, L = 250 μH, C = 60 μF, R = 10 Ω, and the switching frequency f = 20 kHz ($T = 1/f$ = 50 μs), the conduction duty cycle k = 0.4. Therefore, we have obtained the voltage transfer gain $M = k$ = 0.4, that is, $V_2 = kV_1$ = 16 V, the time constant $\tau = L/R$ = 25 μs, and the damping time constant $\tau_d = RC$ = 600 μs. From cybernetic theory, this buck converter is stable since the two poles ($-s_1$ and $-s_2$) are located in the left-hand half plane (LHHP).

$$G(s) = \frac{M}{1 + s\tau + s^2\tau\tau_d} = \frac{M/\tau\tau_d}{(s + s_1)(s + s_2)} \tag{9.5}$$

where

$$s_1 = \sigma + j\omega_0$$

and

$$s_2 = \sigma - j\omega_0$$

with

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$$\sigma = \frac{1}{2\tau_d} = \frac{1}{1200\ \mu s} = 833.33\ \text{Hz} \tag{9.6}$$

and

$$\omega_0 = \frac{\sqrt{4\tau\tau_d - \tau^2}}{2\tau\tau_d} = \frac{\sqrt{60,000 - 625}}{30,000\mu} = \frac{243.67}{30,000\mu} = 8.122\ \text{krad/s} \tag{9.7}$$

Correspondingly,

$$f_0 = \frac{\omega_0}{2\pi} = 1292.7\ \text{Hz} \tag{9.8}$$

that is,

$$T_0 = \frac{1}{f_0} = 0.774\ \text{ms}$$

There is a couple of conjugated complex poles s_1 and s_2 in the transfer function. The unit-step function response in the time domain is

$$V_2(t) = 16[1 - e^{-t/0.0012}(\cos 8122t - 0.1026 \sin 8122t)]\ \text{V} \tag{9.9}$$

The unit-step function response (transient process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.2.

The impulse interference response in the time domain is

$$\Delta V_2(t) = 0.205Ue^{-t/0.0012} \sin 8122t \tag{9.10}$$

where U is the interference signal. The impulse response (interference recovery process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.3.

If there are some power losses and considering a resistance r_L of inductor L existing, we have the following transfer function:

$$G(s) = \frac{M\dfrac{R}{R + r_L}}{1 + s\dfrac{L + RCr_L}{R + r_L} + s^2LC\dfrac{R}{R + r_L}} = \frac{pM}{1 + s\tau + s^2\tau\tau_d} \tag{9.11}$$

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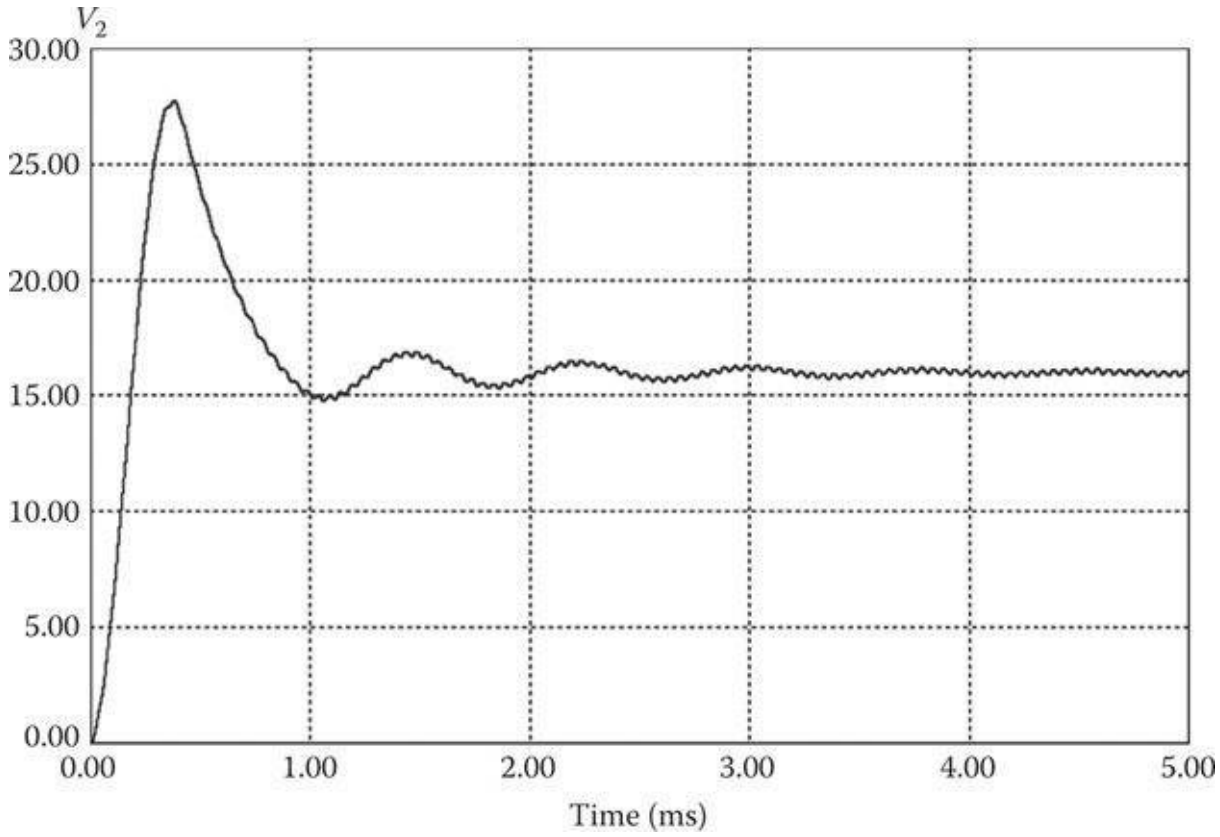


FIGURE 9.2
Unit-step function response of a buck converter without power losses.

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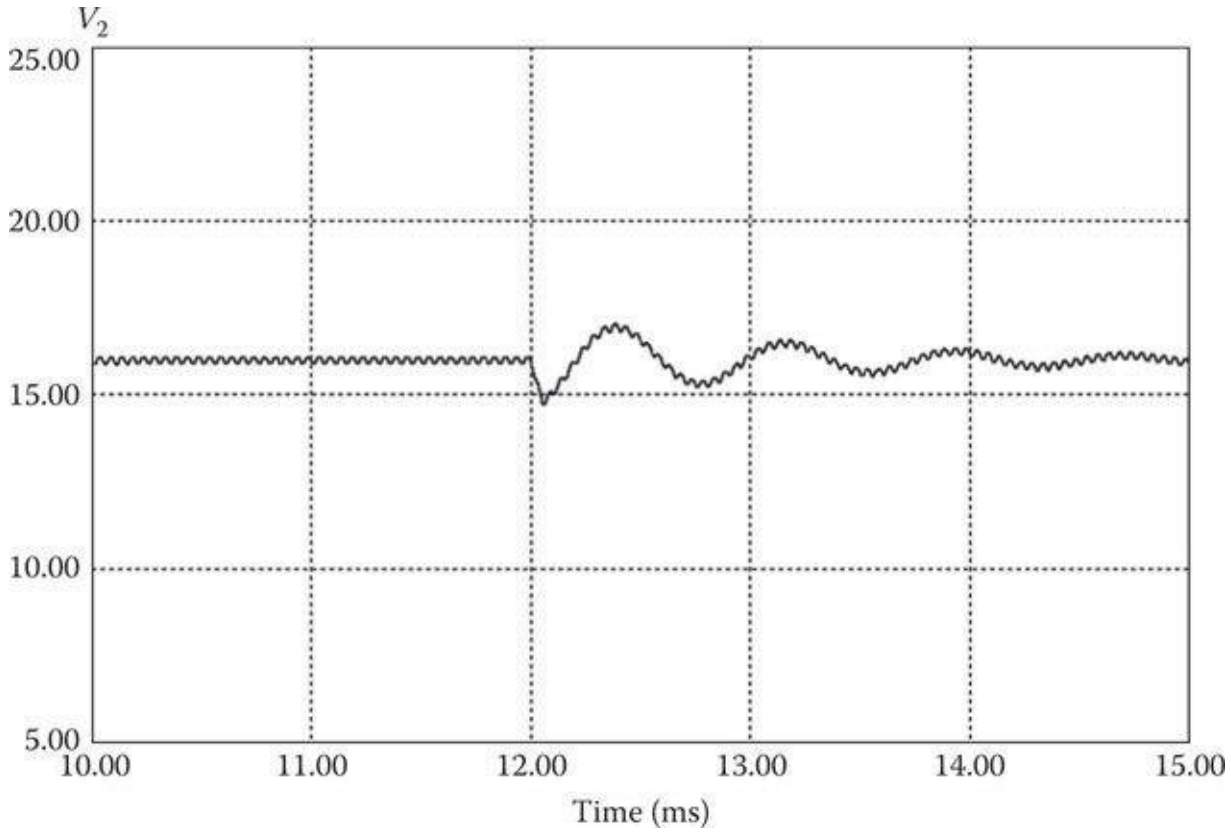


FIGURE 9.3
Impulse response of a buck converter without power losses.

where M is the voltage transfer gain in steady state.

$$M = \frac{V_2}{V_1} = k = 0.4 \tag{9.12}$$

τ is the time constant,

$$\tau = \frac{L + RCr_L}{R + r_L} \tag{9.13}$$

τ_d is the damping time constant

$$\tau_d = \frac{LRC}{L + RCr_L} \tag{9.14}$$

p is the proportional constant

$$p = \frac{R}{R + r_L} \tag{9.15}$$

s is the Laplace operator in s-domain.

If the resistance r_L of inductor L is zero, Equations 9.11, 9.12, 9.13 and 9.14 return back to Equations 9.1, 9.2, 9.3 and 9.4 and $p = 1$. To verify the correction of this mathematical model, we take the value of the resistance $r_L = 1.5\ \Omega$ without changing other parameters and obtain

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$$\tau = \frac{L + RCr_L}{R + r_L} = \frac{250\mu + 15 \times 60\mu}{11.5} = 100\ \mu s$$

$$\tau_d = \frac{LRC}{L + RCr_L} = \frac{250\mu \times 10 \times 60\mu}{250\mu + 15 \times 60\mu} = \frac{150{,}000\mu}{1{,}150} = 130.4\ \mu s$$

$$p = \frac{R}{R + r_L} = 0.87$$

Therefore,

$$\tau_d = 130.4\mu = 1.304\tau$$

$$V_2 = pMV_1 = 0.87 \times 0.4 \times 40 = 13.9\ V$$

This transfer function in *s*-domain is still a second-order function. Since $\tau_d = 1.304\ \tau > 0.25\ \tau$, this buck converter is stable, and the two poles ($-s_1$ and $-s_2$) are located in the LHHP.

$$G(s) = \frac{pM}{1 + s\tau + s^2\tau\tau_d} = \frac{pM/\tau\tau_d}{(s + s_1)(s + s_2)} \tag{9.16}$$

where

$$s_1 = \sigma + j\omega_0$$

and

$$s_2 = \sigma - j\omega_0$$

with

$$\sigma = \frac{1}{2\tau_d} = \frac{1}{260\ \mu s} = 3.85\ kHz \tag{9.17}$$

and

$$\omega_0 = \frac{\sqrt{4\tau\tau_d - \tau^2}}{2\tau\tau_d} = \frac{\sqrt{52{,}000 - 10{,}000}}{26{,}000} = \frac{204.94}{26{,}000} = 7.88\ krad/s \tag{9.18}$$

Correspondingly,

$$f_0 = \frac{\omega_0}{2\pi} = 1.255\ kHz$$

that is,

$$T_0 = \frac{1}{f_0} = 0.797\ ms$$

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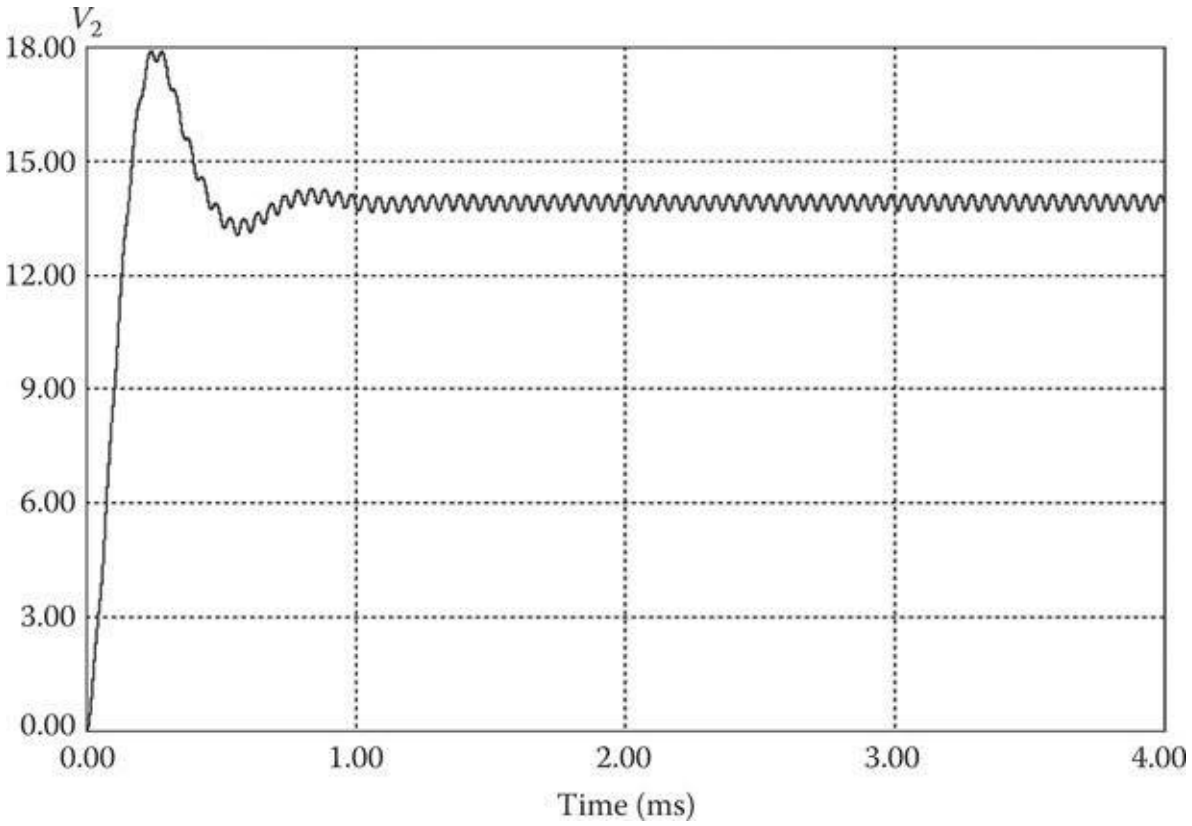


FIGURE 9.4
Unit-step function response of a buck converter with r_L = 1.5 Ω.

The unit-step function response in the time domain is

$$V_2(t) = 13.9[1 - e^{-t/0.00026}(\cos 7880t - 0.487 \sin 7880t)] \text{ V} \tag{9.19}$$

The unit-step function response (transient process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.4.

The impulse interference response in the time domain is

$$\Delta V_2(t) = 0.974Ue^{-t/0.00026} \sin 7880t \tag{9.20}$$

where U is the interference signal. The impulse response (interference recovery process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.5.

If the value of the resistance r_L = 4 Ω, without changing other parameters, we obtain

$$\tau = \frac{L + RCr_L}{R + r_L} = \frac{250\mu + 40 \times 60\mu}{14} = 189.3 \text{ μs}$$

$$\tau_d = \frac{LRC}{L + RCr_L} = \frac{250\mu \times 10 \times 60\mu}{250\mu + 40 \times 60\mu} = \frac{150,000\mu}{2,650} = 56.6 \text{ μs}$$

$$p = \frac{R}{R + r_L} = 0.714$$

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Therefore,

$$\tau_d = 189.3\mu = 0.3\tau$$

$$V_2 = pMV_1 = 0.714 \times 0.4 \times 40 = 11.4 \text{ V}$$

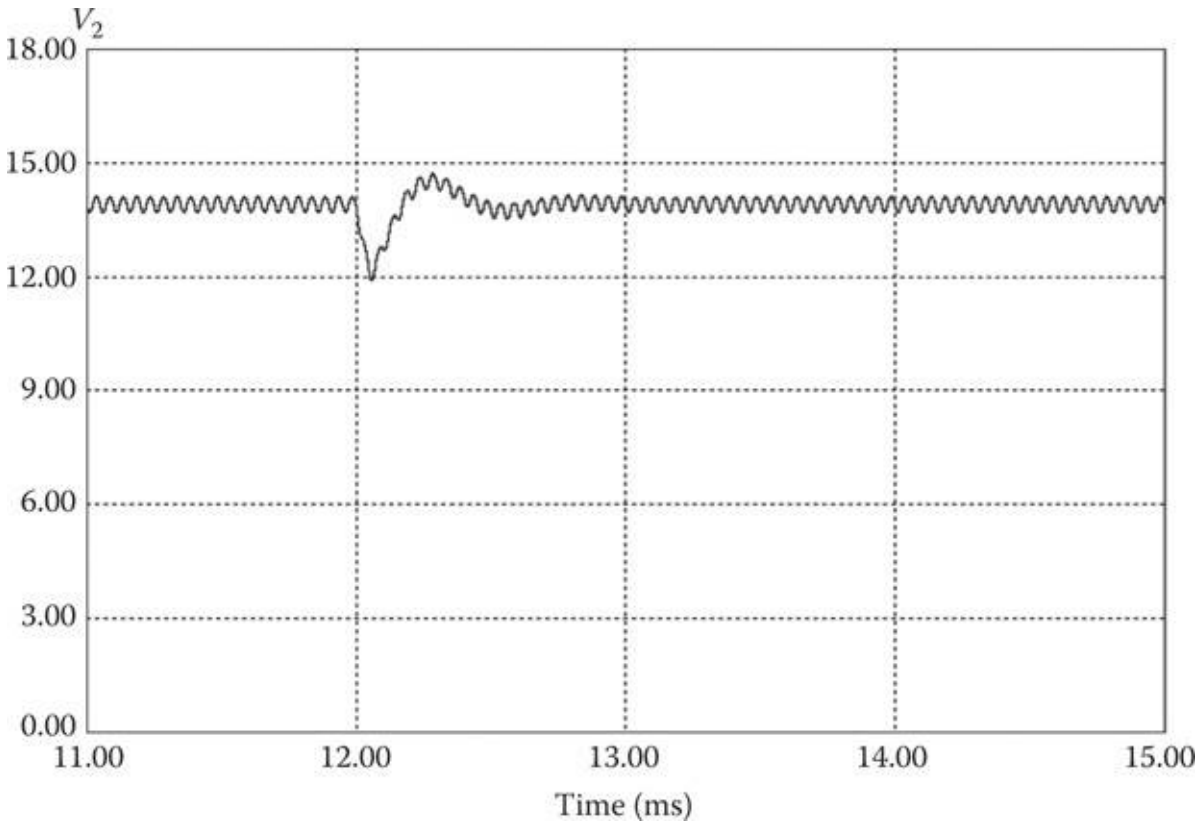


FIGURE 9.5
Impulse response of a buck converter with r_L = 1.5 Ω.

This transfer function in *s*-domain is still a second-order function. Since $\tau_d > 0.25\tau$, this buck converter is stable, and the two poles ($-s_1$ and $-s_2$) are located in the LHHP.

$$G(s) = \frac{pM}{1 + s\tau + s^2\tau\tau_d} = \frac{pM/\tau\tau_d}{(s + s_1)(s + s_2)} \tag{9.21}$$

where

$$s_1 = \sigma + j\omega_0$$

and

$$s_2 = \sigma - j\omega_0$$

with

$$\sigma = \frac{1}{2\tau_d} = \frac{1}{113.2\ \mu\text{s}} = 8.83 \text{ kHz} \tag{9.22}$$

and

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$$\omega_0 = \frac{\sqrt{4\tau\tau_d - \tau^2}}{2\tau\tau_d} = \frac{\sqrt{42,857.5 - 35,834.5}}{21,428.76} = \frac{73.8}{21,428.76\mu} = 3.911\ \text{krad/s} \tag{9.23}$$

Correspondingly,

$$f_0 = \frac{\omega_0}{2\pi} = 622.4\ \text{Hz}$$

that is,

$$T_0 = \frac{1}{f_0} = 1.607\ \text{ms}$$

The unit-step function response in the time domain is

$$V_2(t) = 11.4[1 - e^{-t/0.000113}(\cos 3911t - 2.26 \sin 3911t)]\ \text{V} \tag{9.24}$$

The unit-step function response (transient process) has vibration progress with damping factor σ and frequency ω_0, and is shown in Figure 9.6.

The impulse interference response in the time domain is

$$\Delta V_2(t) = 4.52Ue^{-t/0.000113} \sin 3911t \tag{9.25}$$

where U is the interference signal. The impulse response (interference recovery process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.7.

If the value of the resistance r_L = 4.5 Ω, without changes to other parameters, we have

$$\tau = \frac{L + RCr_L}{R + r_L} = \frac{250\mu + 45 \times 60\mu}{14.5} = 203.45\ \mu\text{s}$$

$$\tau_d = \frac{LRC}{L + RCr_L} = \frac{250\mu \times 10 \times 60\mu}{250\mu + 45 \times 60\mu} = \frac{150,000\mu}{2,770} = 50.85\ \mu\text{s}$$

$$p = \frac{R}{R + r_L} = 0.69$$

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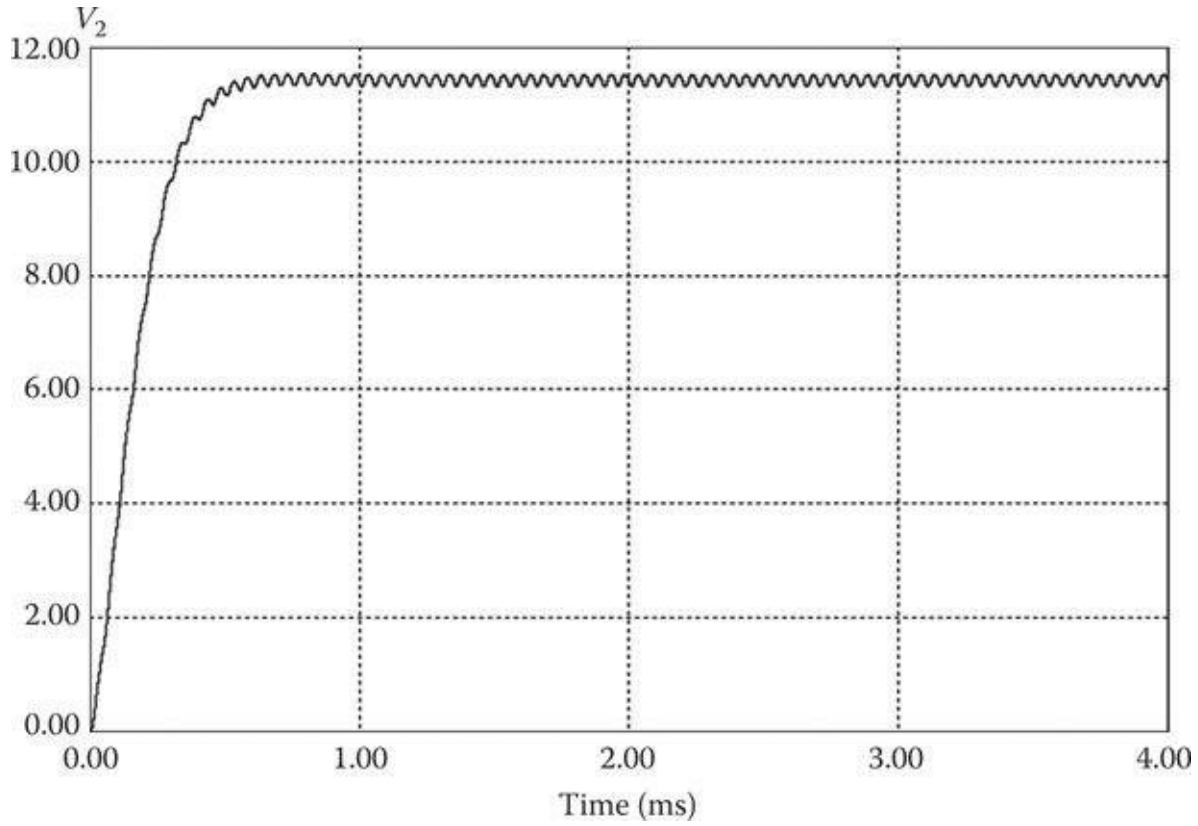


FIGURE 9.6
Unit-step function response of a buck converter with $r_L = 4\ \Omega$.

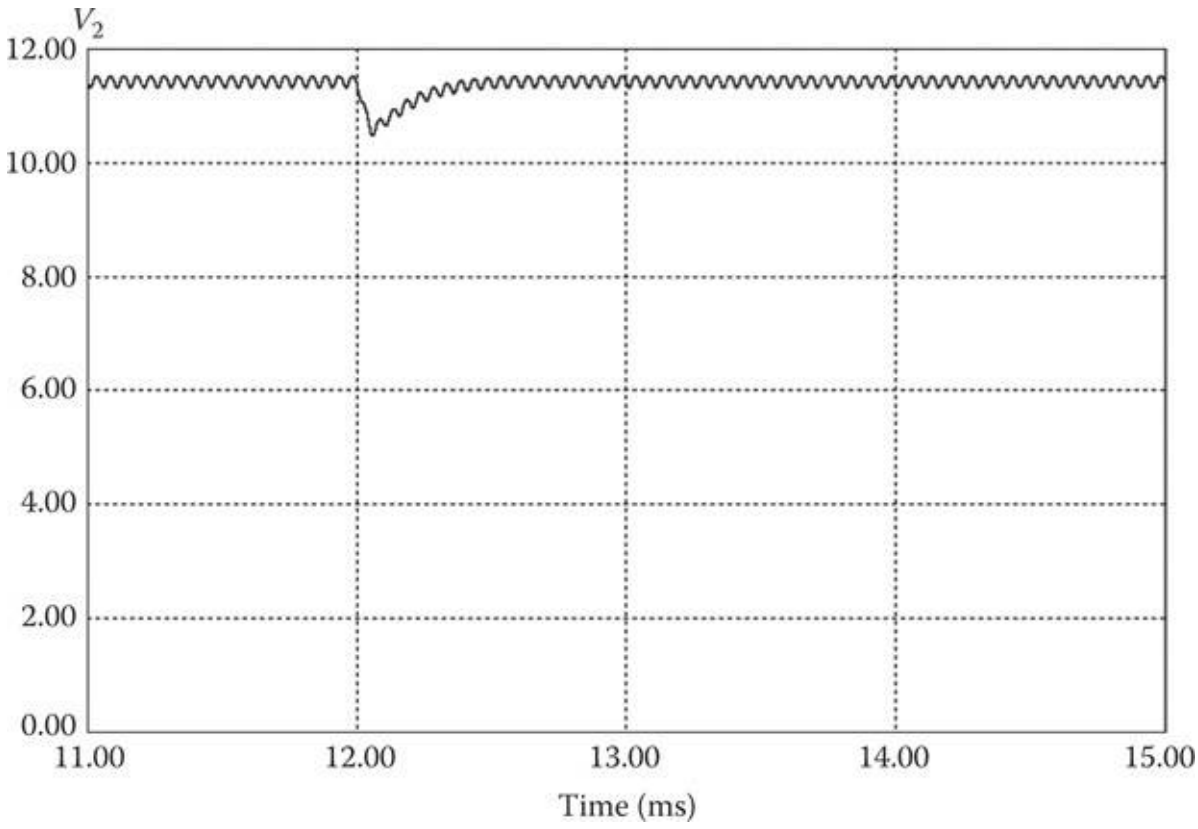


FIGURE 9.7
Impulse response of a buck converter with $r_L = 4\ \Omega$.

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Therefore,

$$\tau_d = 203.45\mu = 0.24994\tau$$

$$V_2 = pMV_1 = 0.69 \times 0.4 \times 40 = 11.04 \text{ V}$$

This transfer function in *s*-domain is still a second-order function. Since $\tau_d < 0.25\tau$, this buck converter is stable, and the two poles ($-\sigma_1$ and $-\sigma_2$) are real numbers located in the LHHP.

$$G(s) = \frac{pM}{1 + s\tau + s^2\tau\tau_d} = \frac{pM/\tau\tau_d}{(s+\sigma_1)(s+\sigma_2)} \tag{9.26}$$

where

$$\sigma_1 = \frac{\tau + \sqrt{\tau^2 - 4\tau\tau_d}}{2\tau\tau_d} = \frac{203.45 + \sqrt{41,392 - 41,382}}{20,691\mu} = \frac{203.45 + 3.16}{20,691\mu} = 9,986 \tag{9.27}$$

and

$$\sigma_2 = \frac{\tau - \sqrt{\tau^2 - 4\tau\tau_d}}{2\tau\tau_d} = \frac{203.45 - \sqrt{41,392 - 41,382}}{20,691\mu} = \frac{203.45 - 3.16}{20,691\mu} = 9,680 \tag{9.28}$$

The unit-step function response in the time domain is

$$K_1 = -\frac{1}{2} + \frac{\tau}{2\sqrt{\tau^2 - 4\tau\tau_d}} = -0.5 + \frac{203.45}{2\sqrt{41,392 - 41,382}} = -0.5 + 32.1 = 31.6$$

$$K_2 = -\frac{1}{2} - \frac{\tau}{2\sqrt{\tau^2 - 4\tau\tau_d}} = -0.5 - \frac{203.45}{2\sqrt{41,392 - 41,382}} = -0.5 - 32.1 = -32.6$$

$$\Delta V_2(t) = 11\left(1 + 31.6e^{-9986t} - 32.6e^{-9680t}\right) \text{V} \tag{9.29}$$

The unit-step function response (transient process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.8.

The impulse interference response in the time domain is

$$\Delta V_2(t) = \frac{U}{\sqrt{1 - 4\tau_d/\tau}}\left(e^{-\sigma_2 t} - e^{-\sigma_1 t}\right) = 63.8U\left(e^{-9680t} - e^{-9986t}\right) \text{V} \tag{9.30}$$

where *U* is the interference signal. The impulse response (interference recovery process) has vibration progress with damping factor σ and frequency ω_0 and is shown in Figure 9.9.

Many traditional parameters such as power factor (PF), power transfer efficiency (η), total harmonic distortion (THD), and ripple factor (RF) have been successfully applied in power electronics and conversion technology. By using these parameters, one can describe the characteristics of a system. Power DC/DC converters usually possess DC input and DC output.

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Consequently, some parameters such as PF and THD are not applicable to describe the characteristics of power DC/DC converters.

Energy storage in power DC/DC converters has been paid attention long time ago. Unfortunately, there is no clear concept to describe the phenomena and reveal the relationship between the stored energy (SE) and the characteristics of power DC/DC converters. We have theoretically defined a new concept—energy factor (EF)—in this chapter and researched the relations between EF and the mathematical modeling for power DC/DC converters. EF is a new parameter in power electronics and DC/DC conversion technology, which completely differs from the traditional concepts such as PF, efficiency n, THD, and RF. EF and the subsequential parameters such as EF for variation of stored energy (EF_V and EF_{VD}), pumping energy (PE), SE, variation of stored energy (VE) in continuous conduction mode (CCM), and variation stored energy (VE_D) in discontinuous conduction mode (DCM) can illustrate the system stability, reference response, and interference recovery. This investigation is very helpful for system design and characteristics foreseeing of DC/DC converters. Two DC/DC converters, namely, *buck* converter and *super-lift Luo-converter*, as the samples are analyzed in this chapter to demonstrate the applications of *EF*, EF_V (and EF_{VD}), *PE*, *SE*, and *VE* (and VE_D). In convenience, the input voltage and current are defined as V_1 and I_1, and the output voltage and current are defined as V_2 and I_2. Switching frequency is f and period $T = 1/f$. The conduction duty cycle is k.

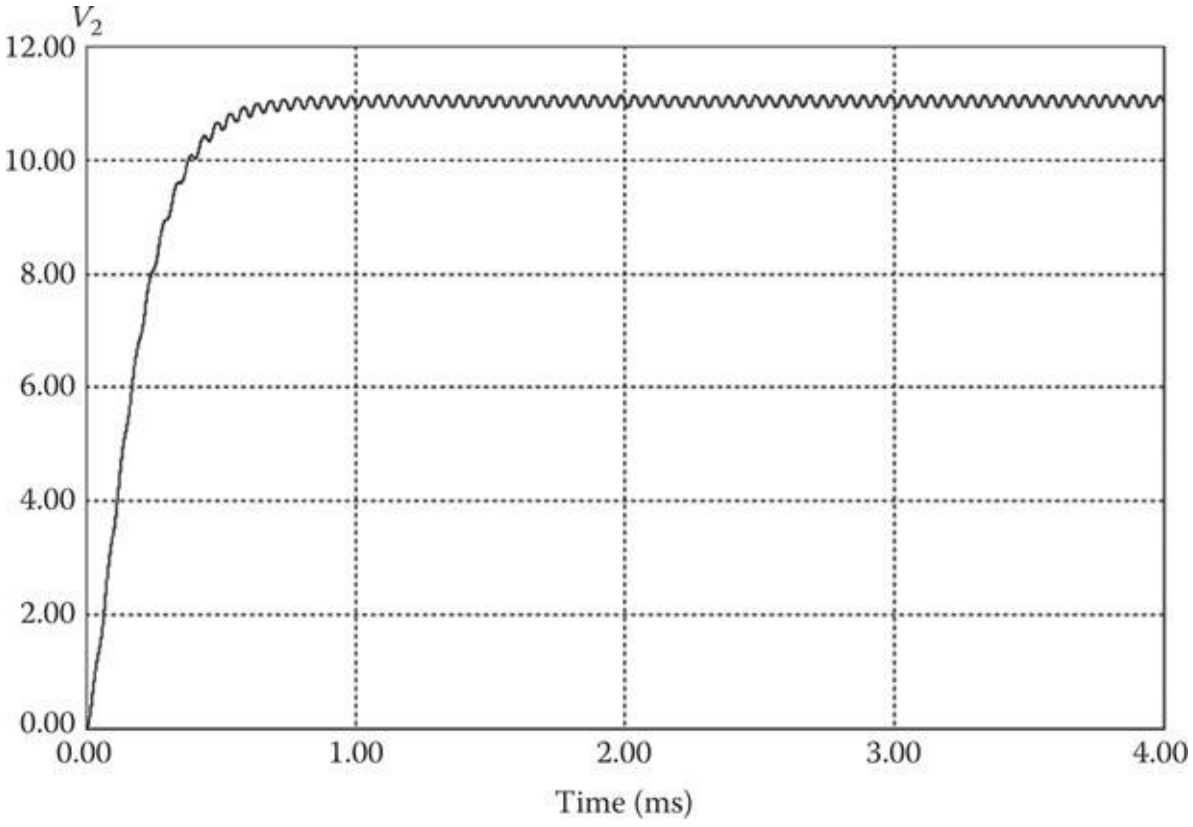


FIGURE 9.8
Unit-step function response of a buck converter with $r_L = 4.5\ \Omega$.

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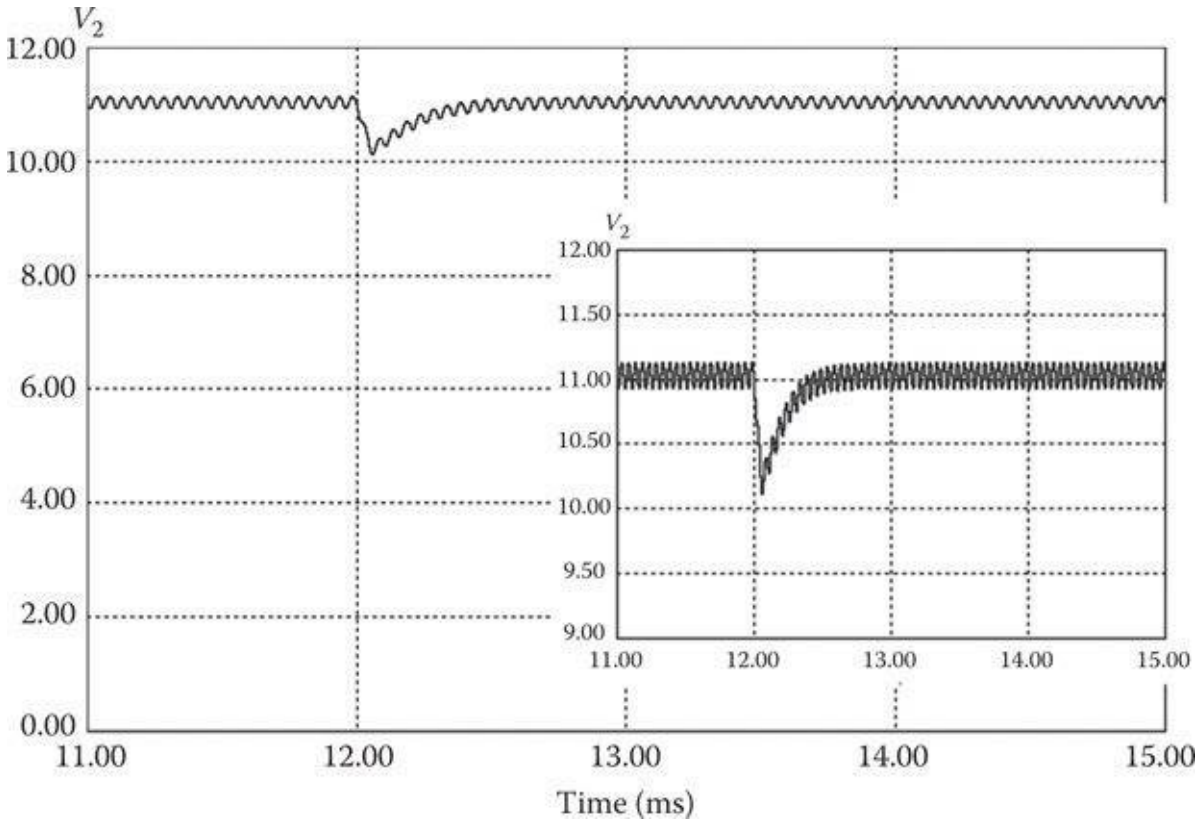


FIGURE 9.9
Impulse response of a buck converter with $r_L = 4.5\ \Omega$.

9.2 Energy Factor and Relevant Parameters

All power DC/DC converters have pumping circuit to transfer the energy from the source to energy-storage passive elements, for example, inductors and capacitors. The PE is used to count the input energy in a switching period T. Its calculation formula is

$$PE = \int_0^T V_1 i_1(t)dt = V_1 I_1 T \tag{9.31}$$

The stored energy in an inductor is

$$W_L = \frac{1}{2} L I_L^2$$

The stored energy across a capacitor is

$$W_C = \frac{1}{2} C V_C^2$$

If there are n_L inductors and n_C capacitors, the total stored energy in a DC/DC converter is

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$$SE = \sum_{j=1}^{n_L} W_{L_j} + \sum_{j=1}^{n_C} W_{C_j} \tag{9.32}$$

n_L and n_C can be zero. For example, switched-capacitor converters have no inductor, and switched-inductor converters have no capacitor. Most power DC/DC converters consist of inductors and capacitors. Therefore, we define the capacitor–inductor stored energy ratio (CIR)

$$CIR = \frac{\sum_{j=1}^{n_C} W_{C_j}}{\sum_{j=1}^{n_L} W_{L_j}} \tag{9.33}$$

Another factor is proportional power losses. The energy losses in a period T is $EL = P_{loss} \times T$. We define the (inductor stored energy)/(energy losses) ratio *ILR*:

$$ILR = \frac{\sum_{j=1}^{n_L} W_{L_j}}{P_{loss} \times T + \sum_{j=1}^{n_L} W_{L_j}} = \frac{\sum_{j=1}^{n_L} W_{L_j}}{EL + \sum_{j=1}^{n_L} W_{L_j}} \tag{9.34}$$

This ratio is a scalar quantity to measure the energy losses during conversion process. The larger the power losses, the lower the ILR. If power losses are zero, this assumption is widely applied for most DC/DC converter investigations, $ILR = 1$.

From investigations, we can see that

- The larger the CIR, the higher the vibration
- The lower the ILR, the lower the vibration

Combining both factors, we can get the vibration ratio *VR*:

$$VR = CIR \times ILR = \frac{\sum_{j=1}^{n_C} W_{C_j}}{\sum_{j=1}^{n_L} W_{L_j}} \frac{\sum_{j=1}^{n_L} W_{L_j}}{P_{loss} \times T + \sum_{j=1}^{n_L} W_{L_j}} = \frac{\sum_{j=1}^{n_C} W_{C_j}}{EL + \sum_{j=1}^{n_L} W_{L_j}} \tag{9.35}$$

Finally, the vibration does not solely rely on the energy storage across inductors. Therefore, this analysis is available for all switched-capacitor converters.

The current flowing through an inductor has variation (ripple) Δi_L, and the variation of the stored energy in an inductor is

$$\Delta W_L = \frac{1}{2} L (I_{\max}^2 - I_{\min}^2) = L I_L \Delta i_L \tag{9.36}$$

where

$$I_{\max} = I_L + \frac{\Delta i_L}{2} \quad \text{and} \quad I_{\min} = I_L - \frac{\Delta i_L}{2}$$

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The voltage across a capacitor has variation (ripple) Δv_C, and the variation of the stored energy across a capacitor is

$$\Delta W_C = \frac{1}{2}C(V_{\max}^2 - V_{\min}^2) = CV_C\Delta v_C \tag{9.37}$$

where

$$V_{\max} = V_C + \frac{\Delta v_C}{2} \quad \text{and} \quad V_{\min} = V_C - \frac{\Delta v_C}{2}$$

In the steady state of CCM, the total variation of the stored energy is

$$VE = \sum_{j=1}^{n_L} \Delta W_{L_j} + \sum_{j=1}^{n_C} \Delta W_{C_j} \tag{9.38}$$

In the steady state of DCM, some of the minimum current and/or voltage become zero. We define the filling coefficients m_L and m_C to describe the discontinuous situation. Usually, if the switching frequency f is high enough, the inductor's current is a triangle waveform. It increases and reaches $I_{\max}$ during the switching-on period kT and decreases during the switching-off period $(1 - k)T$. It becomes zero at $t = t_1$ before next switching-on in DCM. The waveform is shown in Figure 9.10a. The time t_1 should be $kT < t_1 < T$, and the filling coefficient m_L is

$$m_L = \frac{t_1 - kT}{(1-k)T} \tag{9.39}$$

where $0 < m_L < 1$. It means that the inductor's current only can fill the time period $m_L(1 - k)T$ during switch-off. In this case, $I_{\min}$ equals zero, and the average current I_L is

$$I_L = I_{\max}[m_L + (1 - m_L)k] \tag{9.40}$$

and

$$\Delta i_L = I_{\max} \tag{9.41}$$

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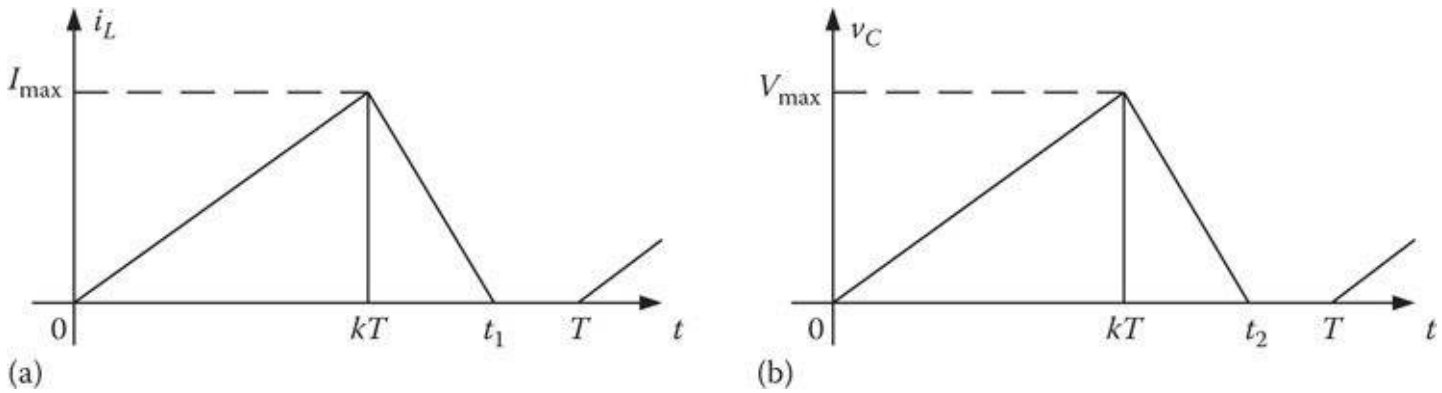


FIGURE 9.10
Discontinuous inductor current and capacitor voltage. (a) Discontinuous inductor current. (b) Discontinuous capacitor voltage.

Therefore,

$$\Delta W_L = LI_L\Delta i_L = LI_{\max}^2[m_L + (1-m_L)k] \tag{9.42}$$

Analogously, we define the filling coefficient m_C to describe the capacitor voltage discontinuity. The waveform is shown in Figure 9.10b. The time t_2 should be $kT < t_2 < T$, and the filling coefficient m_C is

$$m_C = \frac{t_2 - kT}{(1-k)T} \tag{9.43}$$

where $0 < m_C < 1$. It means that the capacitor's voltage only can fill the time period $m_C(1 - k)T$ during switch-off. In this case, $V_{\min}$ equals zero, and the average voltage V_C is

$$V_C = V_{\max}[m_C + (1-m_C)k] \tag{9.44}$$

and

$$\Delta v_C = V_{\max} \tag{9.45}$$

Therefore,

$$\Delta W_C = CV_C\Delta v_C = CV_{\max}^2[m_C + (1-m_C)k] \tag{9.46}$$

If a converter works in DCM, it usually means only one or two storage elements voltage/current discontinuous, not all elements. We use the parameter VE_D to present the total variation of the stored energy:

$$VE_D = \sum_{j=1}^{n_{L-d}} \Delta W_{L_j} + \sum_{j=n_{L-d}+1}^{n_L} \Delta W_{L_j} + \sum_{j=1}^{n_{C-d}} \Delta W_{C_j} + \sum_{j=n_{C-d}+1}^{n_C} \Delta W_{C_j} \tag{9.47}$$

where

n_{L-d} is the number of discontinuous inductor currents

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n_{C-d} is the number of discontinuous capacitor voltages

This formula form is the same as Equation 9.38. For convenience, if not especially necessary, we use Equation 9.38 to cover both CCM and CDM.

The input energy in a period T is $PE = P_{in} \times T = V_1 I_1 \times T$, and we define the EF that is the ratio of stored energy and pumping energy:

$$EF = \frac{SE}{PE} = \frac{SE}{V_1 I_1 T} = \frac{\sum_{j=1}^{m} W_{L_j} + \sum_{j=1}^{n} W_{C_j}}{V_1 I_1 T} \tag{9.48}$$

We also define the EF for the variation of stored energy (EF_V), that is, the ratio of the variation of stored energy and pumping energy:

$$EF_V = \frac{VE}{PE} = \frac{VE}{V_1 I_1 T} = \frac{\sum_{j=1}^{m} \Delta W_{L_j} + \sum_{j=1}^{n} \Delta W_{C_j}}{V_1 I_1 T} \tag{9.49}$$

Energy factor EF and variation energy factor EF_V are applicable to describe the characteristics of power DC/DC converters. The applications will be listed in next sections.

9.3 Applications of Parameters

9.3.1 Power Efficiency η

We can use these parameters to describe the characteristics of DC/DC converters. Usually, most analysis applied in DC/DC converters assumes that the input power is equal to the output power, $P_{in} = P_o$ or $V_1 I_1 = V_2 I_2$, so that pumping energy is equal to output energy in a period $PE = V_1 I_1 T = V_2 I_2 T$. It corresponds to the efficiency $\eta = V_2 I_2 T/PE = 100\%$.

If the load is a pure resistive load, R, $V_2 = I_2 R$, the voltage transfer gain of a DC/DC converter is M:

$$M = \frac{V_2}{V_1} = \frac{I_2 R}{V_1} \tag{9.50}$$

Particularly, power losses always exist during the conversion process. They are caused by the resistance of the connection cables, resistance of the inductor and capacitor wire, and power losses across the semiconductor devices (diode, IGBT, MOSFET, and so on). We can sort them as the resistance power losses P_r, passive element power losses P_e, and device power losses P_d. The total power losses are P_{loss}:

$$P_{loss} = P_r + P_e + P_d \tag{9.51}$$

Therefore,

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$$P_{in} = P_o + P_{loss} = P_o + P_e + P_e + P_d = V_2 I_2 + P_e + P_e + P_d \tag{9.52}$$

So that $P_{in} > P_o$, the efficiency $\eta = V_2 I_2 T/PE < 100\%$. If the load is a pure resistive load, R, $V_2 = \sqrt{P_o R} = \sqrt{\eta P_{in} R}$, the voltage transfer gain of a DC/DC converter M is

$$M = \frac{V_2}{V_1} = \frac{\sqrt{\eta P_o R}}{V_1} \tag{9.53}$$

9.3.2 System Stability

After investigation, we found that all existing power DC/DC converters are stable and have the condition $EF > EF_V$. If $EF < EF_V$, it means that variation reaches 100% or higher and the converter is unstable.

9.3.3 Time Constant τ of a Power DC/DC Converter

The *time constant* τ is a new concept to describe the transient process of a DC/DC converter and is defined as

$$\tau = EF \times T = \frac{SE}{P_{in} \times T} \times T = \frac{SE}{V_1 I_1} \tag{9.54}$$

The time constant can estimate the converter response for a small-signal analysis. It is the process time under the first-order differential operation. It means that if there is no output energy, the stored energy will be accumulated up to its rated value (steady-state value) in the time constant τ.

9.3.4 Damping Time Constant τ_d of a Power DC/DC Converter

Since a DC/DC converter usually consists of multiple passive energy-storage elements, for this investigation the converter response should involve vibration components. The vibration time constant τ*v* of a DC/DC converter is defined as

$$\tau_v = EF_V \times T = \frac{VE}{P_{in} \times T} \times T = \frac{VE}{V_1 I_1} \tag{9.55}$$

From investigation, the vibration of power DC/DC converters is relative to the *damping time constant* τ_d. The damping time constant τ_d is a new concept to describe the transient process of a DC/DC converter with vibration response and is defined as

$$\tau_d = VR \times \tau_V = VR \times \frac{VE}{P_{in} \times T} \times T = \frac{VR \times VE}{V_1 I_1} \tag{9.56}$$

The damping time constant can estimate the converter response for a small-signal analysis. It is the process time under the second-order differential operation. It may cause the converter transient process with vibration and overshot.

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9.4 Transfer Function of Power DC/DC Converters

A DC/DC converter usually has two or more energy-storage elements. The *time constant* τ and *damping time constant* τ_d are now available to form the transfer function of a power DC/DC converter to describe its characteristics in the second-order differential operation for a small-signal analysis. The voltage transfer gain of the DC/DC converter is $M = V_2/V_1$. The transfer function of the DC/DC converter can be mathematically modeled as

$$G(s) = \frac{M}{1 + s\tau + s^2\tau\tau_d} \tag{9.57}$$

where

M is the voltage transfer gain V_2/V_1

τ is the time constant in (9.54)

τ_d is the damping time constant in (9.56)

s is the Laplace operator in s-domain

This mathematical model for power DC/DC converters is significantly easy to describe the characteristics of power DC/DC converters. It will be used to discuss different cases in the following sections.

9.4.1 Very Small Variation of Storage Energy

If the variation of storage energy is very small (i.e., $\tau_d \ll \tau$) and ignorable, the value of the damping time constant τ_d is omitted (i.e., $\tau_d = 0$). The transfer function (9.57) is downgraded from the second order to the first order as

$$G(s) = \frac{M}{1 + s\tau} \tag{9.58}$$

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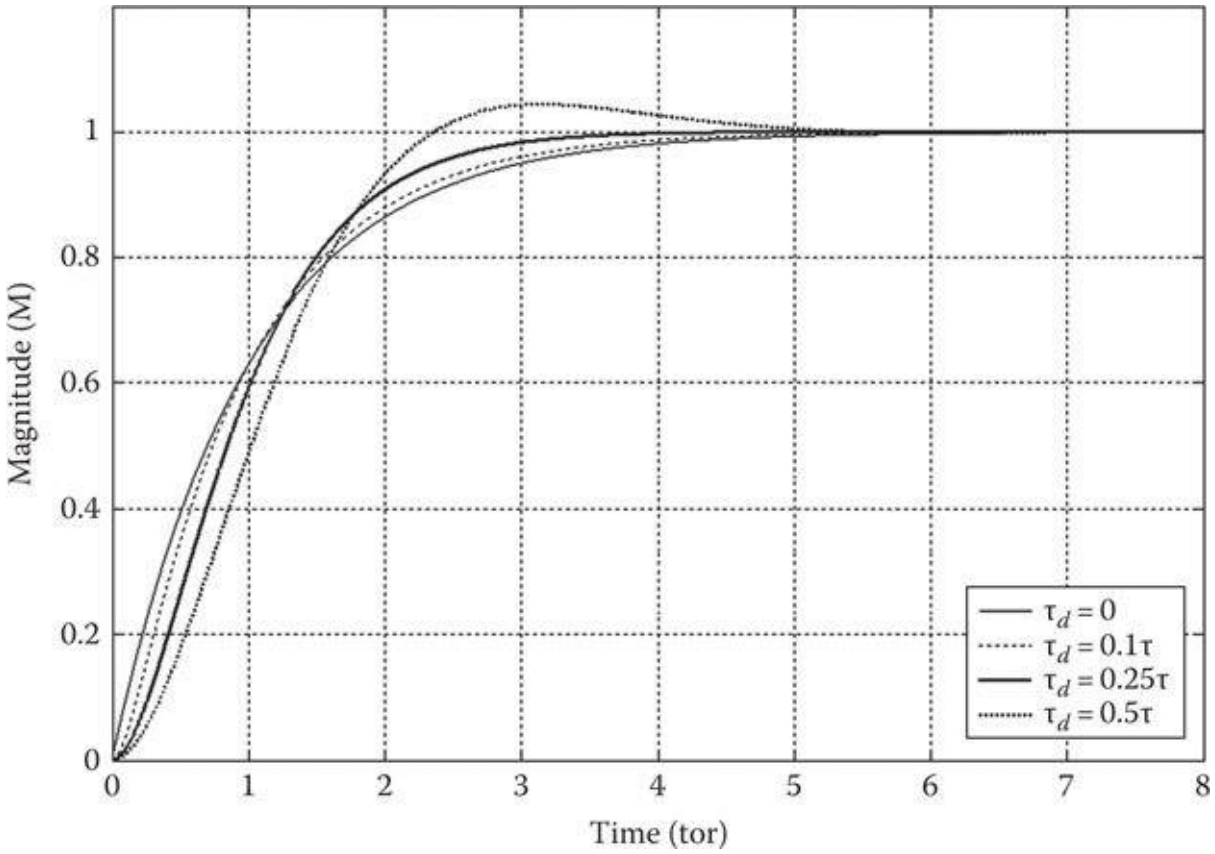


FIGURE 9.11
Unit-step function responses (τ_d = 0, 0.1τ, 0.25τ, and 0.5τ).

This is the transfer function of the first inertia element. This expression describes the characteristics of the DC/DC converter as a first inertia element. The unit-step function response in the time domain is

$$g(t) = M(1 - e^{-t/\tau}) \tag{9.59}$$

The transient process (settling time) is nearly three times of the time constant, 3τ to produce $g(t) = g(3\tau) = 0.95M$. The response waveform in time domain is shown in Figure 9.11 with $\tau_d = 0$.

The impulse interference response in the time domain is

$$\Delta g(t) = U \cdot e^{-t/\tau} \tag{9.60}$$

where U is the interference signal. The interference recovering progress is nearly three times of the time constant, 3τ. The response waveform in time domain is shown in Figure 9.12 with $\tau_d = 0$.

9.4.2 Small Variation of Storage Energy

If the variation of storage energy is small (i.e., $\tau_d < \tau/4$), the value of the damping time constant τ_d is not omitted. The transfer function (9.57) is retained the second-order function with two real poles σ_1 and σ_2 as

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$$G(s) = \frac{M}{1 + s\tau + s^2\tau\tau_d} = \frac{M/\tau\tau_d}{(s+\sigma_1)(s+\sigma_2)} \tag{9.61}$$

where

$$\sigma_1 = \frac{\tau + \sqrt{\tau^2 - 4\tau\tau_d}}{2\tau\tau_d}$$

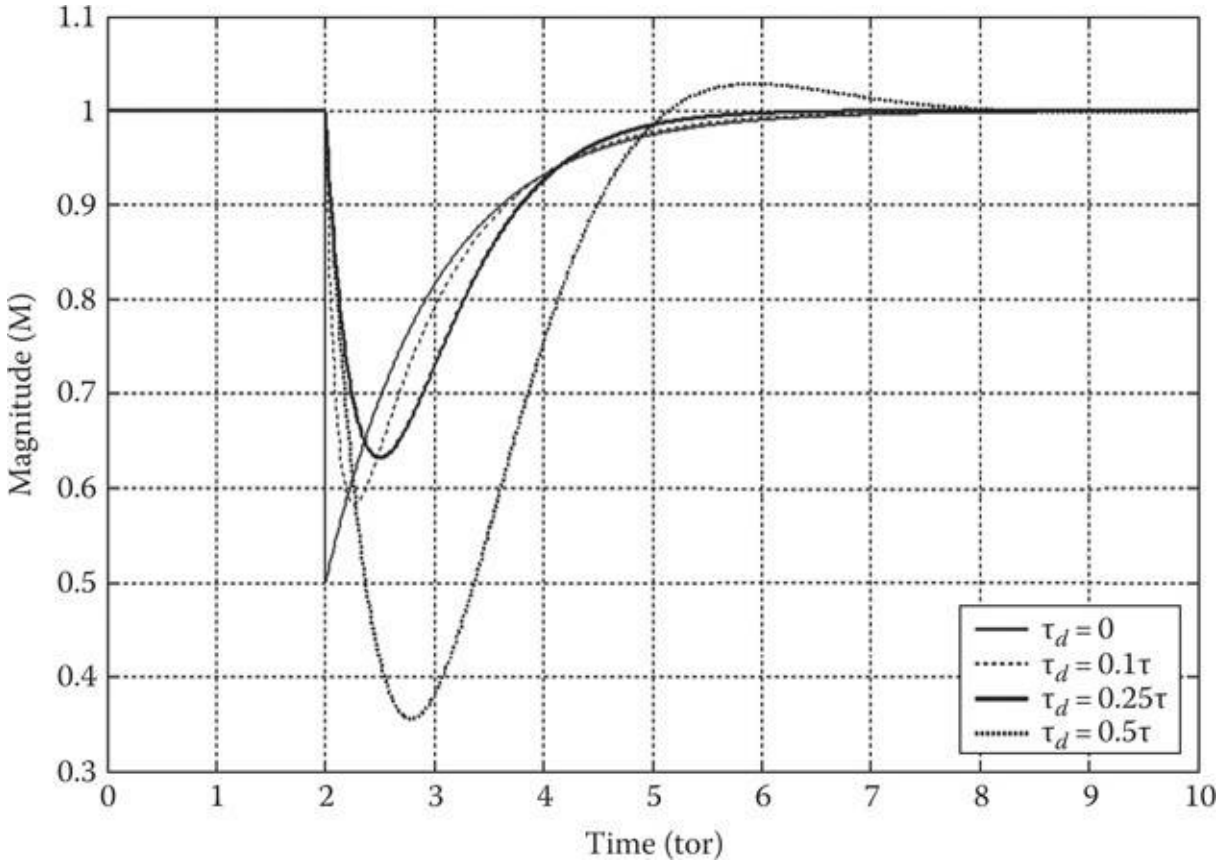


FIGURE 9.12
Impulse responses (τ_d = 0, 0.1τ, 0.25τ, and 0.5τ).

and

$$\sigma_2 = \frac{\tau - \sqrt{\tau^2 - 4\tau\tau_d}}{2\tau\tau_d}$$

There are two real poles in the transfer function, and $\sigma_1 > \sigma_2$. This expression describes the characteristics of the DC/DC converter. The unit-step function response in the time domain is

$$g(t) = M(1 + K_1 e^{-\sigma_1 t} + K_2 e^{-\sigma_2 t}) \tag{9.62}$$

where

$$K_1 = -\frac{1}{2} + \frac{\tau}{2\sqrt{\tau^2 - 4\tau\tau_d}}$$

and

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$$K_2 = -\frac{1}{2} - \frac{\tau}{2\sqrt{\tau^2 - 4\tau\tau_d}}$$

The transient process is nearly three times of the time value $1/\sigma_1$, $3/\sigma_1 < 3\tau$. The response process is quick without vibration. The corresponding waveform in time domain is shown in Figure 9.11 with $\tau_d = 0.1\tau$.

The impulse interference response in the time domain is

$$\Delta g(t) = \frac{U}{\sqrt{1 - 4\tau_d/\tau}}(e^{-\sigma_2 t} - e^{-\sigma_1 t}) \tag{9.63}$$

where U is the interference signal. The transient process is nearly three times of the time value $1/\sigma_1$, $3/\sigma_1 < 3\tau$. The response waveform in time domain is shown in Figure 9.12 with $\tau_d = 0.1\tau$.

9.4.3 Critical Variation of Storage Energy

If the variation of storage energy is equal to the critical value (i.e., $\tau_d = \tau/4$), the transfer function (9.57) is retained the second-order function with two equaled real poles $\sigma_1 = \sigma_2 = \sigma$ as

$$G(s) = \frac{M}{1 + s\tau + s^2\tau\tau_d} = \frac{M/\tau\tau_d}{(s+\sigma)^2} \tag{9.64}$$

where

$$\sigma = \frac{1}{2\tau_d} = \frac{2}{\tau}$$

There are two folded real poles in the transfer function. This expression describes the characteristics of the DC/DC converter. The unit-step function response in the time domain is

$$g(t) = M\left[1 - \left(1 + \frac{2t}{\tau}\right)e^{-2t/\tau}\right] \tag{9.65}$$

The transient process is nearly 2.4 times of the time constant τ, 2.4τ. The response process is quick without vibration. The response waveform in time domain is shown in Figure 9.11 with $\tau_d = 0.25\tau$.

The impulse interference response in the time domain is

$$\Delta g(t) = \frac{4U}{\tau} te^{-2t/\tau} \tag{9.66}$$

where U is the interference signal. The transient process is still nearly 2.4 times of the time constant, 2.4τ. The response waveform in time domain is shown in Figure 9.12 with $\tau_d = 0.25\tau$.

9.4.4 Large Variation of Storage Energy

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If the variation of storage energy is large (i.e., $\tau_d > \tau/4$), the transfer function (9.57) is a second-order function with a couple of conjugated complex poles s_1 and s_2 in the left-hand half plane in *s*-domain as

$$G(s) = \frac{M}{1 + s\tau + s^2\tau\tau_d} = \frac{M/\tau\tau_d}{(s + s_1)(s + s_2)} \tag{9.67}$$

where

$$s_1 = \sigma + j\omega \quad \text{and} \quad s_2 = \sigma - j\omega$$

$$\sigma = \frac{1}{2\tau_d} \quad \text{and} \quad \omega = \frac{\sqrt{4\tau\tau_d - \tau^2}}{2\tau\tau_d}$$

There is a couple of conjugated complex poles s_1 and s_2 in the transfer function. This expression describes the characteristics of the DC/DC converter. The unit-step function response in the time domain is

$$g(t) = M\left[1 - e^{-t/2\tau_d}\left(\cos \omega t - \frac{1}{\sqrt{4\tau_d/\tau - 1}} \sin \omega t\right)\right] \tag{9.68}$$

The transient response has vibration progress with damping factor σ and frequency ω. The corresponding waveform in time domain is shown in Figure 9.11 with $\tau_d = 0.5\tau$ and in Figure 9.13 with τ, 2τ, 5τ, and 10τ.

The impulse interference response in the time domain is

$$\Delta g(t) = \frac{U}{\sqrt{\frac{\tau_d}{\tau} - \frac{1}{4}}} e^{-t/2\tau_d} \sin(\omega t) \tag{9.69}$$

where *U* is the interference signal. The recovery process is a curve with damping factor G and frequency ω. The response waveform in time domain is shown in Figure 9.12 with $\tau_d = 0.5\tau$ and in Figure 9.14 with τ, 2τ, 5τ, and 10τ.

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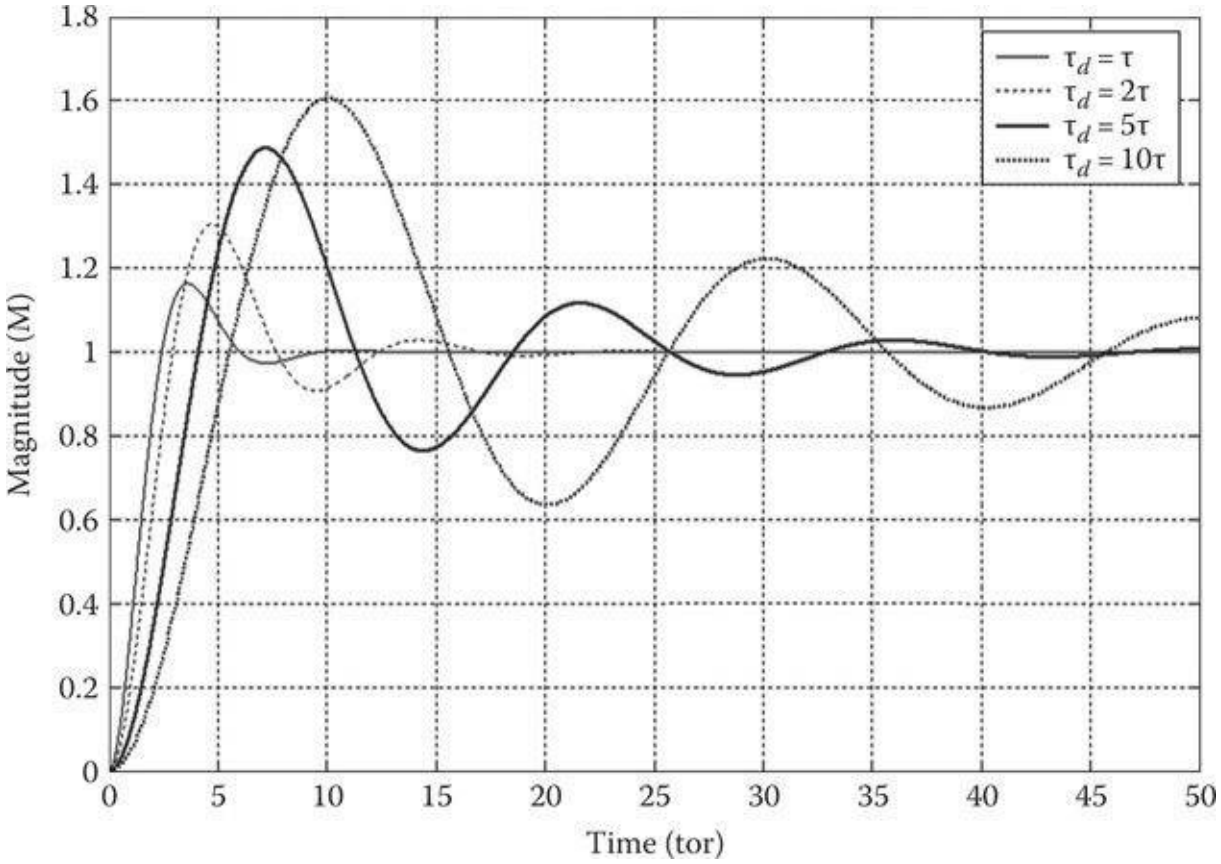


FIGURE 9.13
Unit-step function responses ($\tau_d = \tau$, 2τ, 5τ, and 10τ).

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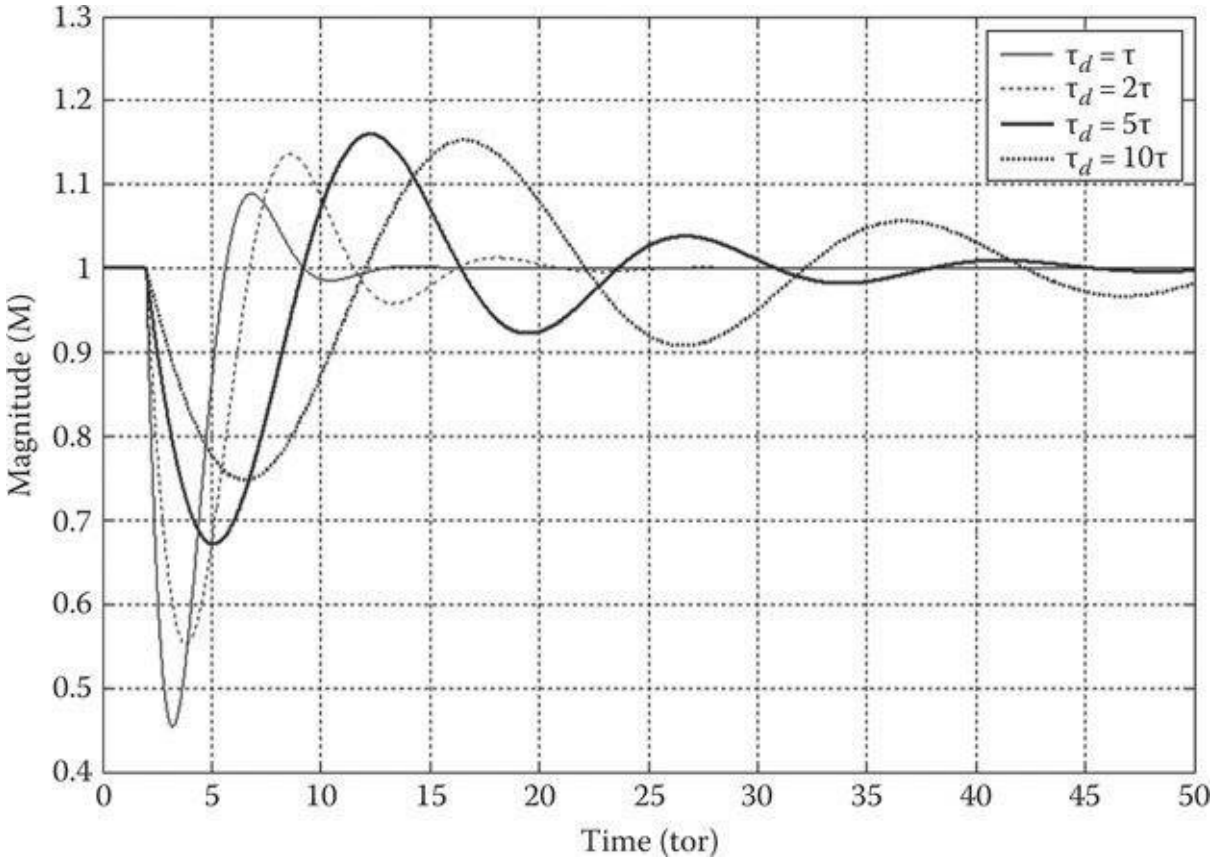


FIGURE 9.14
Impulse responses ($\tau_d = \tau$, 2τ, 5τ, and 10τ).

9.4.5 Explanation of This Mathematical Modeling

Mathematical modeling for power DC/DC converter is very challenging for converter characteristics investigation. People used to follow the traditional manner without any flexibility by applying the impedance calculation in *s*-domain or in frequency domain to analyze the characteristics of power DC/DC converters. For example, inductor's impedance is $Z_L = sL$ or $j\omega L$, and capacitor's impedance is $Z_C = 1/sC$ or $-j/\omega C$. It means that the mathematical model is in *n*th order if the converter possesses *n* passive energy-storage components, and the corresponding dynamic equation is an *n*th-order differential equation. This investigation was restricted in simple structure converters with two energy-storage elements only (one inductor and one capacitor) such as buck, boost, and buck-boost converters. The traditional method is difficult for even a little more complicated converters, for example, Luo-converters and Cúk converters with two inductors and two capacitors, as the transfer function is upgraded to the fourth-order function.

We carefully investigated the responses of all converters by using our new mathematical modeling. Most converters are stable in open-loop operation, and the unit-step function and impulse interference responses are likely second-order function. We confidently claim that the mathematical modeling in Equation 9.57 is a general transfer function with a second order for all DC/DC converters. This mathematical model simplifies the complexity in higher-order operation with very high accuracy.

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9.5 Design Examples of This Theory

In order to verify this theory and offer examples to readers, we analyze two converters to demonstrate the characteristics of power DC/DC converters and applicability of the theory.

9.5.1 Buck Converter

Figure 9.1 shows a buck converter with the conduction duty k. The values are V_1 = 40 V, f = 20 kHz (T = 50 μs), k = 0.4, L = 250 μH, C = 60 μF, and R = 10 Ω. Assume power loss in the inductor resistance r_L = 1.5 Ω. We obtain V_2 = 14 V, $I_2 = I_L$ = 1.4 A, $P_{loss} = I_L^2 r_L = 1.4^2 \times 1.5 = 2.94$ W, I_1 = 0.564 A, Δi_L = 1.68 A, and Δv_C = 0.175 V. Since it is operating in CCM, the parameters are

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$$PE = V_1 I_1 T = 40 \times 0.564 \times 50\mu = 1.128 \text{ mJ}$$

$$W_L = \frac{1}{2} L I_L^2 = 0.5 \times 250\mu \times 1.4^2 = 0.245 \text{ mJ}$$

$$W_C = \frac{1}{2} C V_C^2 = 0.5 \times 60\mu \times 14^2 = 5.88 \text{ mJ}$$

$$SE = W_L + W_C = 6.125 \text{ mJ}$$

$$EL = P_{loss} \times T = 2.94 \times 50 = 0.147 \text{ mJ}$$

$$ILR = \frac{0.245}{0.245 + 0.147} = 0.625$$

$$\Delta W_L = L I_L \Delta i_L = 250\mu \times 1.4 \times 1.68 = 0.588 \text{ mJ}$$

$$\Delta W_C = C V_C \Delta v_C = 60\mu \times 14 \times 0.175 = 0.147 \text{ mJ}$$

$$VE = \Delta W_L + \Delta W_C = 0.735 \text{ mJ}$$

$$EF = \frac{SE}{PE} = \frac{6.125}{1.128} = 5.43$$

$$EF_V = \frac{VE}{PE} = \frac{0.735}{1.128} = 0.65$$

$$\tau = EF \times T = 271.5 \text{ µs}$$

$$CIR = \frac{5.88}{0.245} = 24$$

$$VR = CIR \times ILR = 24 \times 0.625 = 15$$

$$\tau_V = EF_V \times T = 0.65 \times 50 = 32.5 \text{ µs}$$

$$\tau_d = VR \times \tau_V = 15 \times 32.5 = 487.5 \text{ µs}$$

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As $EF > EF_V$, this converter is stable. Its time constant $\tau = EF \times T = 271.5\ \mu s$ and damping time constant $\tau_d = VR \times \tau_V = 487.5\ \mu s = 1.8\tau$. The transfer function of this converter is

$$G(s) = \frac{1}{1 + s\tau + s^2\tau\tau_d} \approx \frac{1}{1 + 2.71\times10^{-4}s + 1.32\times10^{-7}s^2} \tag{9.70}$$

Corresponding unit-step function and impulse interference responses are shown in Figures 9.15 and 9.16. In this case, this buck converter is operating in the second order. The power transfer efficiency $\eta = P_o/P_{in} = 19.6/22.54 = 87\%$.

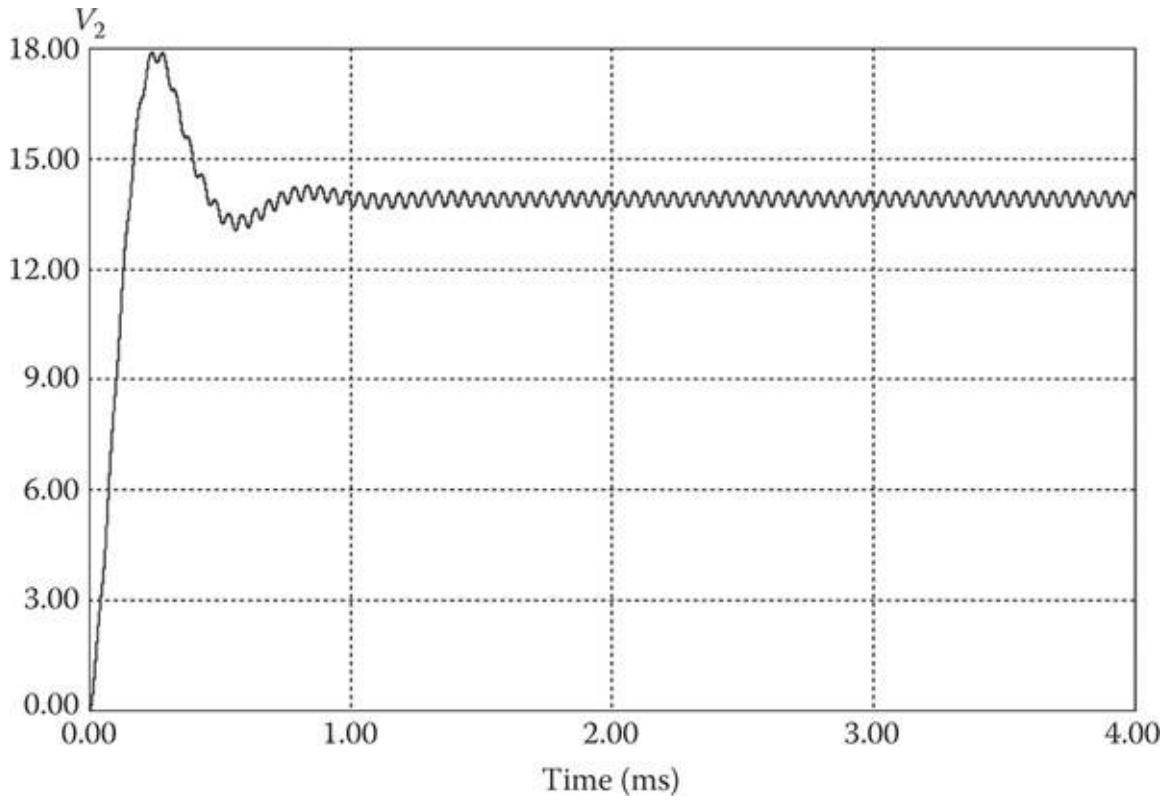


FIGURE 9.15
Unit-step function responses of buck converter.

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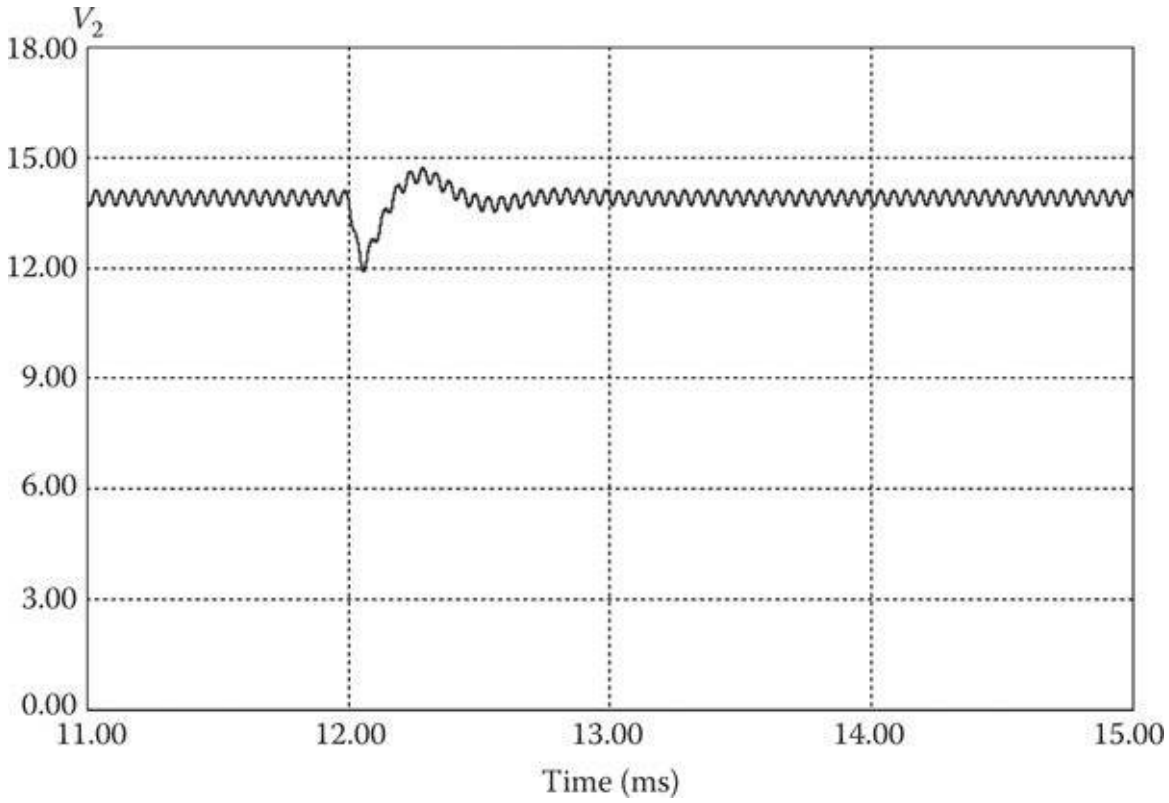


FIGURE 9.16
Impulse responses of buck converter.

9.5.2 Super-Lift Luo-Converter

Figure 9.17 shows a super-lift Luo-converter with the conduction duty k. The values are V_1 = 20 V, f = 50 kHz (T = 20 μs), L = 100 μH, k = 0.5, C_1 = 750 μF, C_2 = 200 μF, and R = 10 Ω. Assume power loss in the inductor resistance r_L = 0.12 Ω. We obtain V_2 = 57.2 V, I_2 = 5.72 A, I_1 = 17.1 A, I_L = 11.4 A, $P_{loss} = I_L^2 \times r_L = 11.4^2 \times 0.12 = 15.6$ W, Δi_L = 1.8 A, $V_{C_1} = V_1$ = 20 V, $V_{C_2} = V_2 = 57.2$ V, $\Delta v_{C_1} = 0.42$ V and $\Delta v_{C_2} = 1.05$ V. It is operating in CCM, and the parameters are

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$$PE = V_1 I_1 T = 20 \times 17.1 \times 20\mu = 6.84 \text{ mJ}$$

$$W_L = \frac{1}{2} L I_L{}^2 = 0.5 \times 100\mu \times 11.4^2 = 6.5 \text{ mJ}$$

$$W_{C_1} = \frac{1}{2} C_1 V_{C_1}^2 = 0.5 \times 750\mu \times 20^2 = 150 \text{ mJ}$$

$$W_{C_2} = \frac{1}{2} C_2 V_{C_2}^2 = 0.5 \times 200\mu \times 57.2^2 = 327 \text{ mJ}$$

$$SE = W_L + W_{C1} + W_{C2} = 483.5 \text{ mJ}$$

$$EL = P_{loss} \times T = 15.6 \times 20 = 0.312 \text{ mJ}$$

$$ILR = \frac{6.5}{6.5 + 0.312} = 0.954$$

$$\Delta W_L = L I_L \Delta i_L = 100\mu \times 11.4 \times 1.8 = 2.05 \text{ mJ}$$

$$\Delta W_{C_1} = C_1 V_{C_1} \Delta v_{C_1} = 750\mu \times 20 \times 0.42 = 6.3 \text{ mJ}$$

$$\Delta W_{C_2} = C_2 V_{C_2} \Delta v_{C_2} = 200\mu \times 57.2 \times 1.05 = 12.01 \text{ mJ}$$

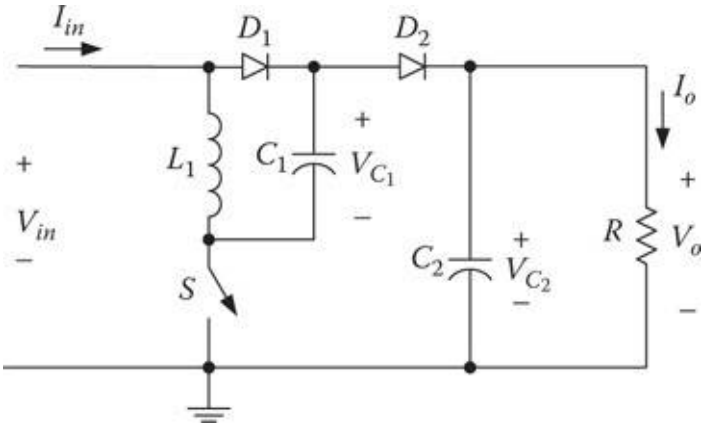


FIGURE 9.17
Super-lift Luo-converter.

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$$VE = \Delta W_L + \Delta W_{C_1} + \Delta W_{C_1} = 20.36 \text{ mJ}$$

$$EF = \frac{SE}{PE} = \frac{483.5}{6.84} = 70.7$$

$$EF_V = \frac{VE}{PE} = \frac{20.36}{6.84} = 2.98$$

$$\tau = EF \times T = 70.7 \times 20 = 1.414 \text{ ms}$$

$$CIR = \frac{477}{6.5} = 73.4$$

$$VR = CIR \times ILR = 73.4 \times 0.954 = 70$$

$$\tau_V = EF_V \times T = 2.98 \times 20 = 59.6 \text{ μs}$$

$$\tau_d = VR \times \tau_V = 70 \times 59.6\mu = 4.172 \text{ ms}$$

Since $EF > EF_V$, this converter is stable. Its time constant τ = 1.414 ms and damping time constant τ_d = 4.172 ms = 2.95τ. The transfer function of this converter is

$$G(s) = \frac{1}{1 + s\tau + s^2\tau\tau_d} \approx \frac{1}{1 + 1.414 \times 10^{-3} s + 5.9 \times 10^{-6} s^2} \tag{9.71}$$

Corresponding unit-step function and impulse interference responses are shown in Figures 9.18 and 9.19. In this case, super-lift Luo-converter is operating in the second order. The power transfer efficiency $\eta = P_o/P_{in}$ = 327.2/342.8 = 95.4%.

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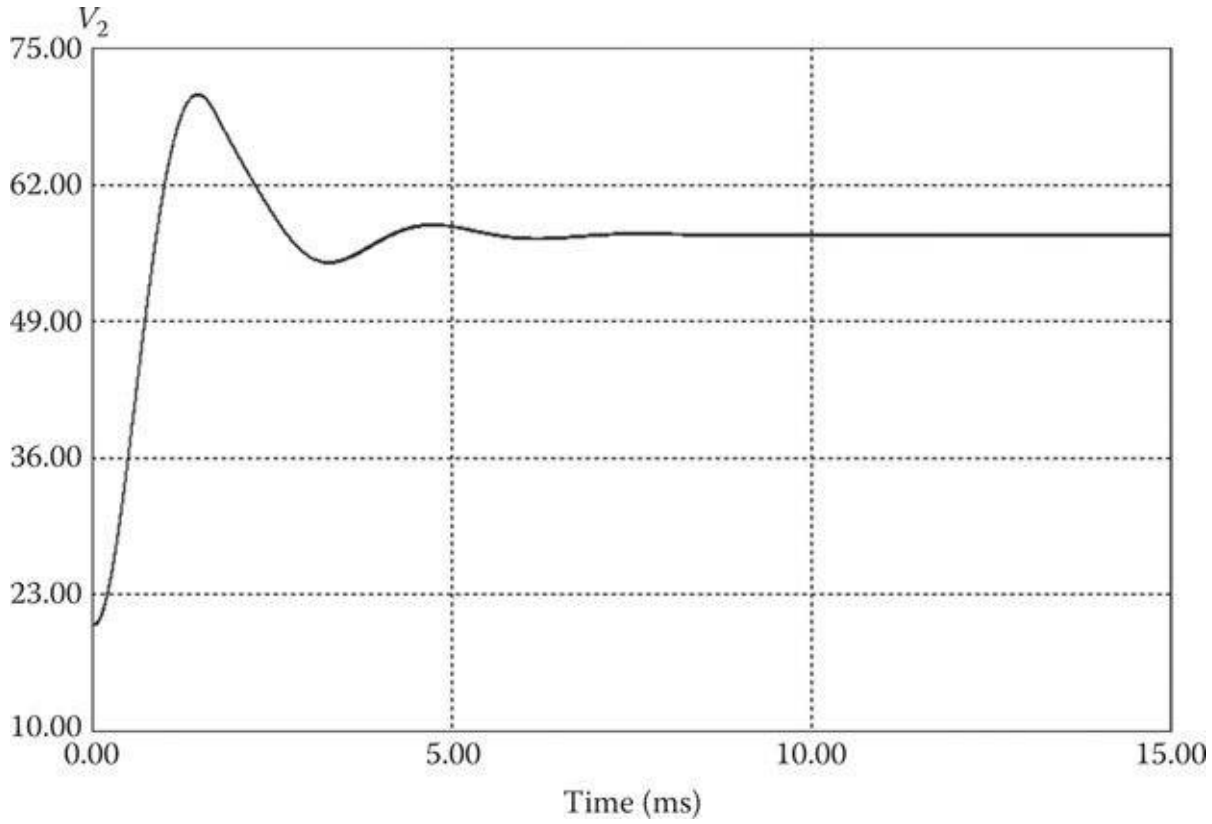


FIGURE 9.18
Unit-step function responses of super-lift Luo-converter.

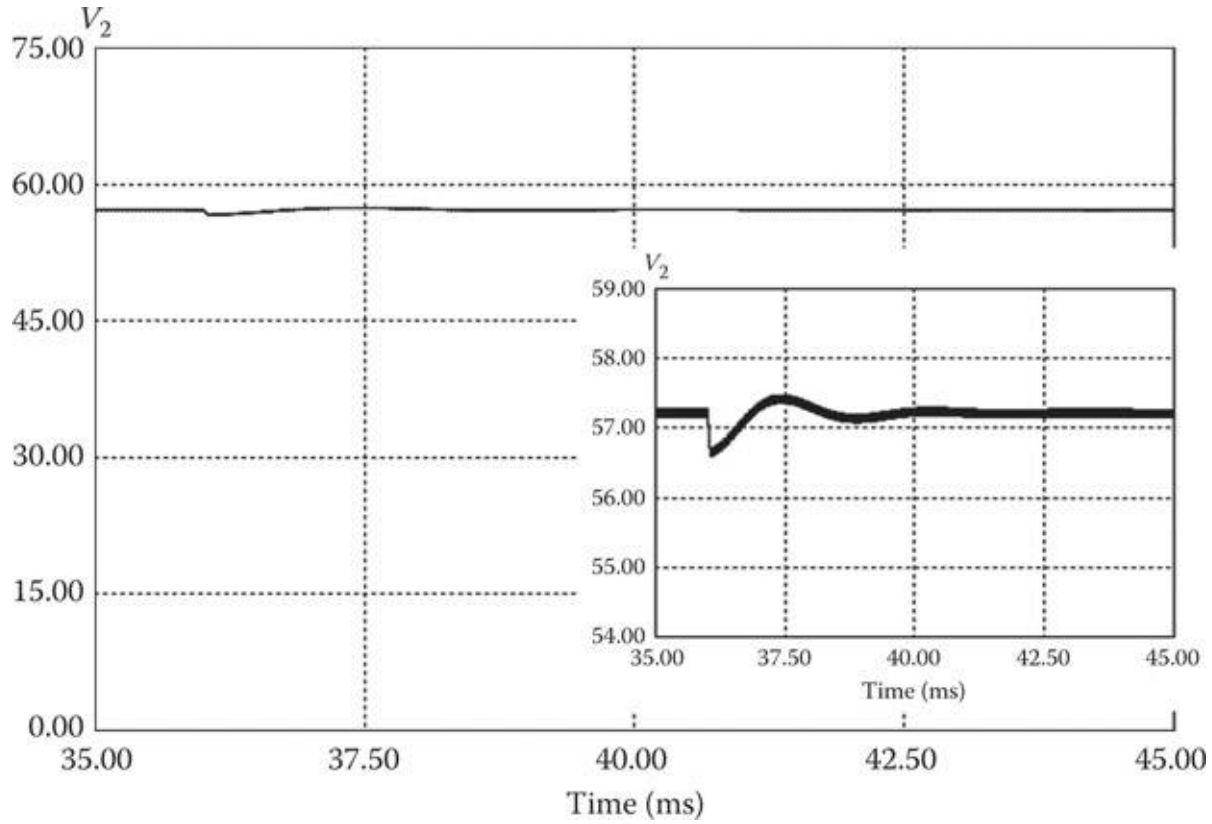


FIGURE 9.19
Impulse responses of super-lift Luo-converter.

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9.6 Summary

This chapter offers a mathematical model (9.57) generally applicable to all power DC/DC converters. The parameters of this model are determined by completely new concepts: *EF* and sequential parameters EF_V (and EF_{VD}), *PE, SE, VE* (and VE_D), time constant τ, and damping time constant τ_d.

Traditional parameters of mathematical modeling such as efficiency (η), PF, THD, and RF are not applicable to power DC/DC converters. The authors are the pioneers to define the new concept EF and other parameters to describe all characteristics of power DC/DC converters. These parameters have been successfully demonstrated on power DC/DC converters. Two typical converters, buck converter and super-lift Luo-converter, are analyzed as examples in this chapter to perform the new modeling method, and satisfactory results are obtained. EF and other parameters are very helpful in DC/DC conversion technology.

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10

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Multiple-Quadrant Operating Luo-Converters

Classical DC/DC converters usually perform in single-quadrant operation, such as buck converter and Luo-converters. Multiple-quadrant operation is required in industrial applications, for example, a DC motor running forward and reverse in motoring and regenerative braking states. This chapter introduces three new converters that can perform two- and four-quadrant DC/DC conversion. One particular application is the MIT 42/±14 V DC/DC converter used for new car power supply systems. Because this converter implements dual-direction energy transference, it is a second-generation DC/DC converter. The simulation and experimental results have verified its characteristics.

10.1 Introduction

Multiple-quadrant operation converters can be derived from the multiple-quadrant chopper. Correspondingly, Class B converter can be derived from Type B chopper (two-quadrant operation), Class E converter from Type E chopper (four-quadrant operation), and so on. Also, multiple-quadrant operating converters can be derived from other first-generation converters. This chapter introduces two- and four-quadrant operation Luo-converters that are derived from positive-, negative-, and double-output Luo-converters. They correspond to a DC motor drive in forward and reverse running with motoring and regenerative braking states. These converters are shown in Figure 10.1.

The input source and output load are usually certain voltages shown as V_1 and V_2. Switches S_1 and S_2 in this diagram are power MOSFET devices and driven by a pulse-width-modulated switching signal with repeating frequency f and conduction duty k. In this chapter, the switch repeating period is $T = 1/f$, the switch-on period is kT, and the switch-off period is $(1 - k)T$. The equivalent resistance is R for each inductor. During switch-on, the voltage drops across the switches and diodes are V_S and V_D. When the switch is turned off, the freewheeling diode current descends in whole switch-off period $(1 - k)T$. If the diode current does not become zero before the switch is turned on again, we define this working state to be the continuous region. If the current becomes zero before the switch is turned on again, this working state is the discontinuous conduction region.

In this chapter, we have the following for general description:

The variation ratio of current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}}$$

The variation ratio of current i_{L_2} is

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$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}}$$

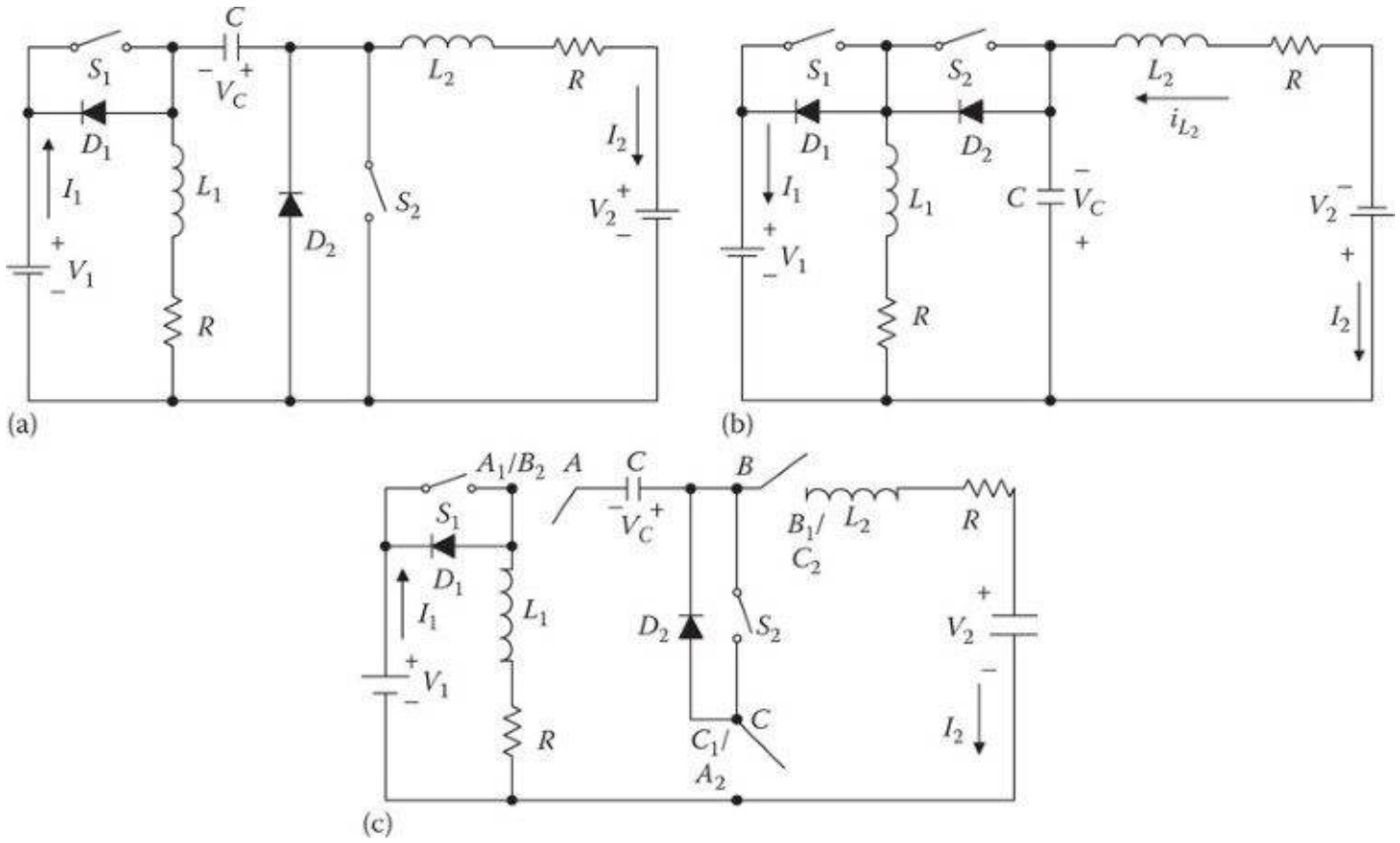


FIGURE 10.1
Multiple-quadrant operating Luo-converters. (a) Circuit 1. (b) Circuit 2. (c) Circuit 3.

The variation ratio of current i_D is

$$\zeta = \frac{\Delta i_D/2}{I_D}$$

The variation ratio of voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C}$$

10.2 Circuit Explanation

Each converter shown in Figure 10.1 consists of two switches with two passive diodes, two inductors, and one capacitor. Circuit 1 performs a two-quadrant (forward) operation, and Circuit 2 performs 2 two-quadrant (reverse) operation. Circuit 1 and Circuit 2 can be converted to each other by a three-pole (A, B, and C) double-through (A1/A2, B1/B2, and

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C1/C2) auxiliary changeover switch as Circuit 3. Circuit 3 performs a four-quadrant operation. Since the changeover process between forward and reverse operations is not very frequent, the auxiliary changeover switch can be an isolated gate bipolar transistor, a power relay, and a contactor. The source voltage (V_1) and load voltage (V_2) are usually considered as constant voltages. The load can be a battery or motor back electromotive force, for example, when the source voltage is 42 V and the load voltage is ±14 V. There are four modes of operation:

1. *Mode A* (*quadrant I*): Electrical energy is transferred from source side V_1 to load side V_2.
2. *Mode B* (*quadrant II*)*:* Electrical energy is transferred from load side V_2 to source side V_1.
3. *Mode C* (*quadrant III*)*:* Electrical energy is transferred from source side V_1 to load side $-V_2$.
4. *Mode D* (*quadrant IV*)*:* Electrical energy is transferred from load side $-V_2$ to source side V_1.

Each mode has two states: “on” and “off.” Circuit 1 in Figure 10.1a implements Modes A and B, and Circuit 2 in Figure 10.1b implements Modes C and D.

10.2.1 Mode A

Mode A implements the characteristics of the buck-boost conversion. For Mode A, state-on is shown in Figure 10.2a: switch S_1 is closed, and switch S_2 and diodes D_1 and D_2 are not conducted. In this case, inductor currents i_{L_1} and i_{L_2} increase, and $i_1 = i_{L_1} + i_{L_2}$. State-*off* is shown in Figure 10.2b: switches S_1 and S_2 and diode D_1 are off, and diode D_2 is conducted.

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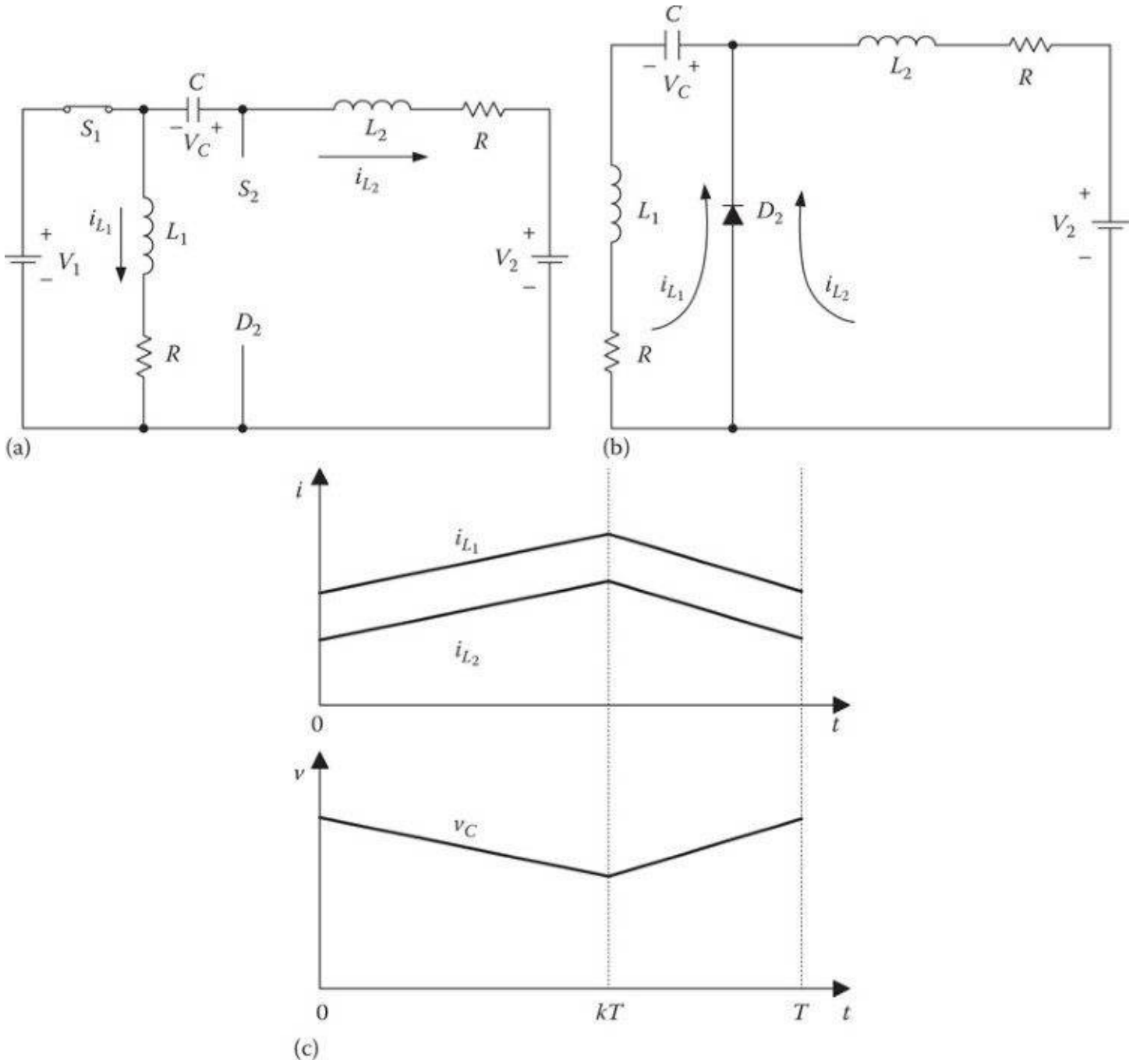


FIGURE 10.2
Mode A. (a) Switch-on. (b) Switch-off. (c) Waveforms with enlarged variations.

In this case, current i_{L_1} flows via diode D_2 to charge capacitor C; in the meantime, current i_{L_2} is kept to flow through load battery V_2. The freewheeling diode current $i_{D2} = i_{L_1} + i_{L_2}$. Some currents' and voltages' waveforms are shown in Figure 10.2c.

10.2.2 Mode B

Mode B implements the characteristics of the boost conversion. For Mode B, state-*on* is shown in Figure 10.3a: switch S_2 is closed; switch S_1 and diodes D_1 and D_2 are not conducted. In this case, inductor current i_{L_2} increases by biased V_2, and inductor current i_{L_1} increases by

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biased V_C. Therefore, capacitor voltage V_C reduces. State-*off* is shown in Figure 10.3b: switches S_1 and S_2 and diode D_2 are not on, and only diode D_1 is on. In this case, source current $i_1 = i_{L_1} + i_{L_2}$, which is a negative value to perform the regenerative operation. Inductor current i_{L_2} flows through capacitor C; it is charged by current i_{L_2}. After capacitor C, i_{L_2} then flows through the source V_1. Inductor current i_{L_1} flows through the source V_1 via diode D_1. Some currents' and voltages' waveforms are shown in Figure 10.3c.

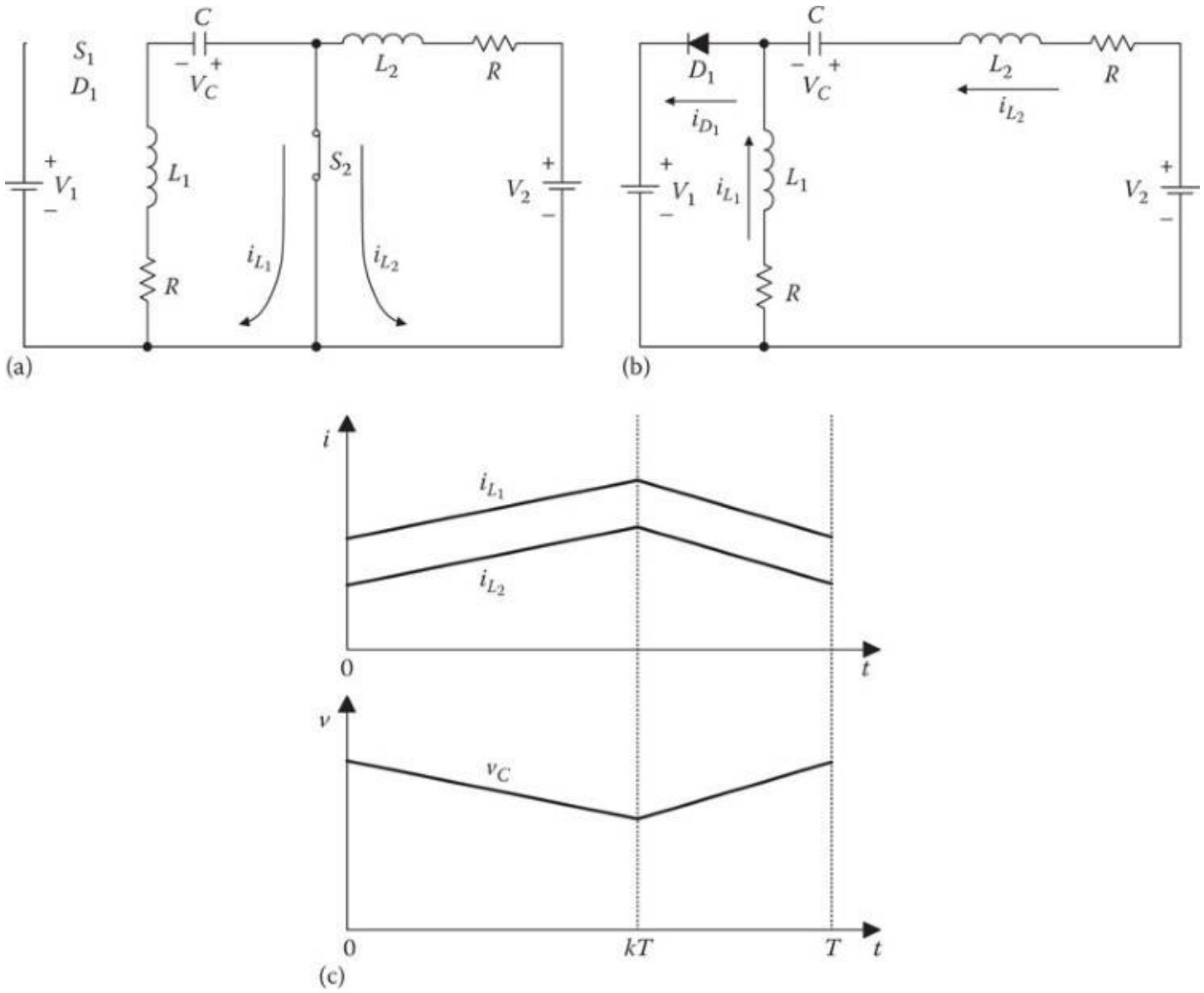


FIGURE 10.3
Mode B. (a) Switch-on. (b) Switch-off. (c) Waveforms with enlarged variations.

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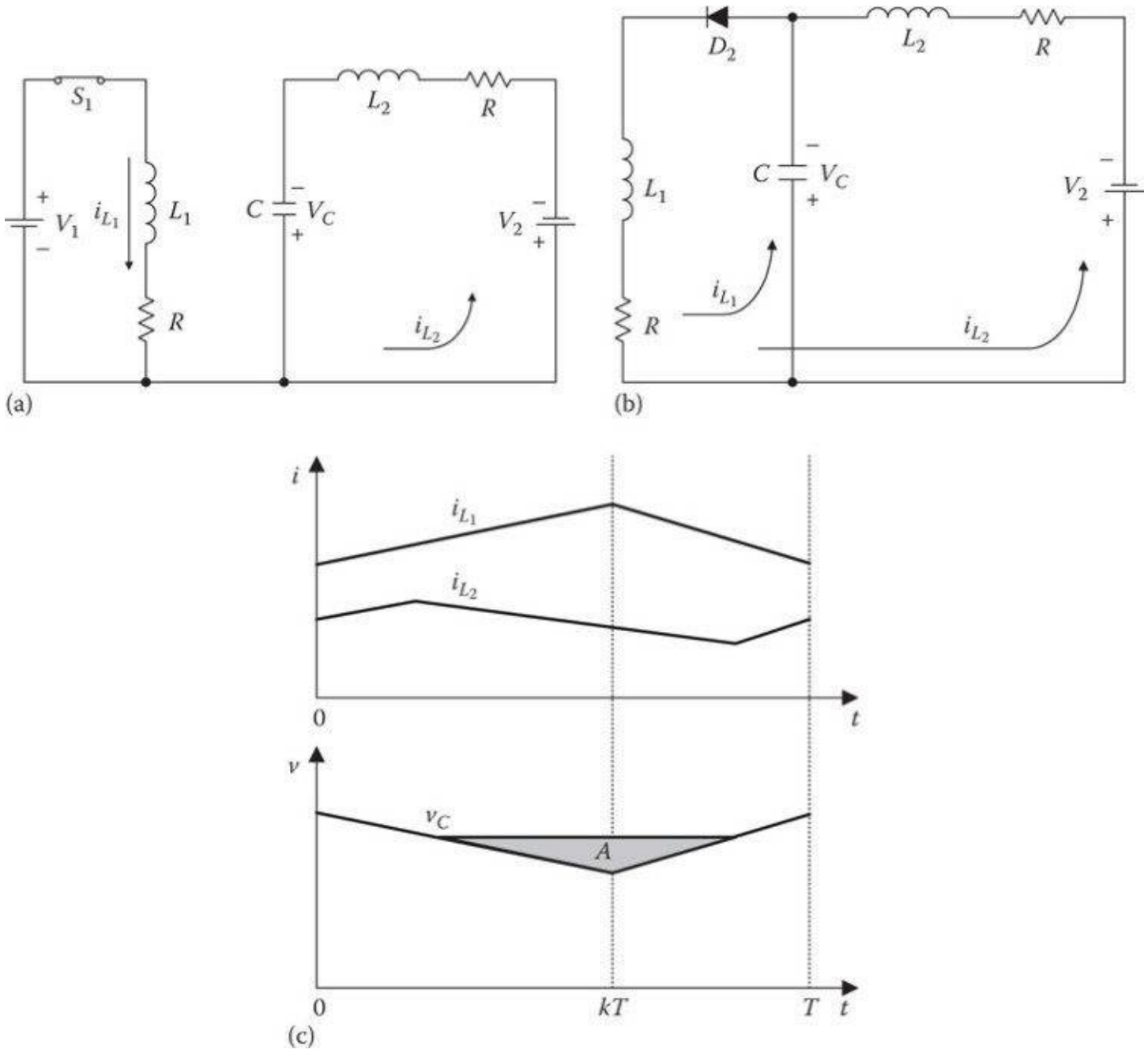


FIGURE 10.4
Mode C. (a) Switch-on. (b) Switch-off. (c) Waveforms with enlarged variations.

10.2.3 Mode C

Mode C implements the characteristics of the buck-boost conversion. For Mode C, state-*on* is shown in Figure 10.4a: switch S_1 is closed; switch S_2 and diodes D_1 and D_2 are not conducted. In this case, inductor currents i_{L_1} and i_{L_2} increase, and $i_1 = i_{L_1}$. State-*off* is shown in Figure 10.4b: switches S_1 and S_2 and diode D_1 are off, and diode D_2 is conducted. In this case, current i_{L_1} flows via diode D_2 to charge capacitor C and the load battery V_2 via inductor L_2. The freewheeling diode current $i_{D_2} = i_{L_1} = i_C + i_2$. Some waveforms are shown in Figure 10.4c.

10.2.4 Mode D

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Mode D implements the characteristics of the boost conversion. For Mode D, state-*on* is shown in Figure 10.5a: switch S_2 is closed; switch S_1 and diodes D_1 and D_2 are not conducted. In this case, inductor current i_{L_1} increases by biased V_2, and inductor current i_{L_2} decreases by biased ($V_2 - V_C$). Therefore, capacitor voltage V_C reduces. Current $i_{L_1} = i_{C\text{-}on} + i_2$. State-*off* is shown in Figure 10.5b: switches S_1 and S_2 and diode D_2 are not on, and only diode D_1 is on. In this case, source current $i_1 = i_{L_1}$, which is a negative value to perform the regenerative operation. Inductor current i_2 flows through capacitor C that is charged by current i_2, that is, $i_{C\text{-}off} = i_2$. Some currents' and voltages' waveforms are shown in Figure 10.5c.

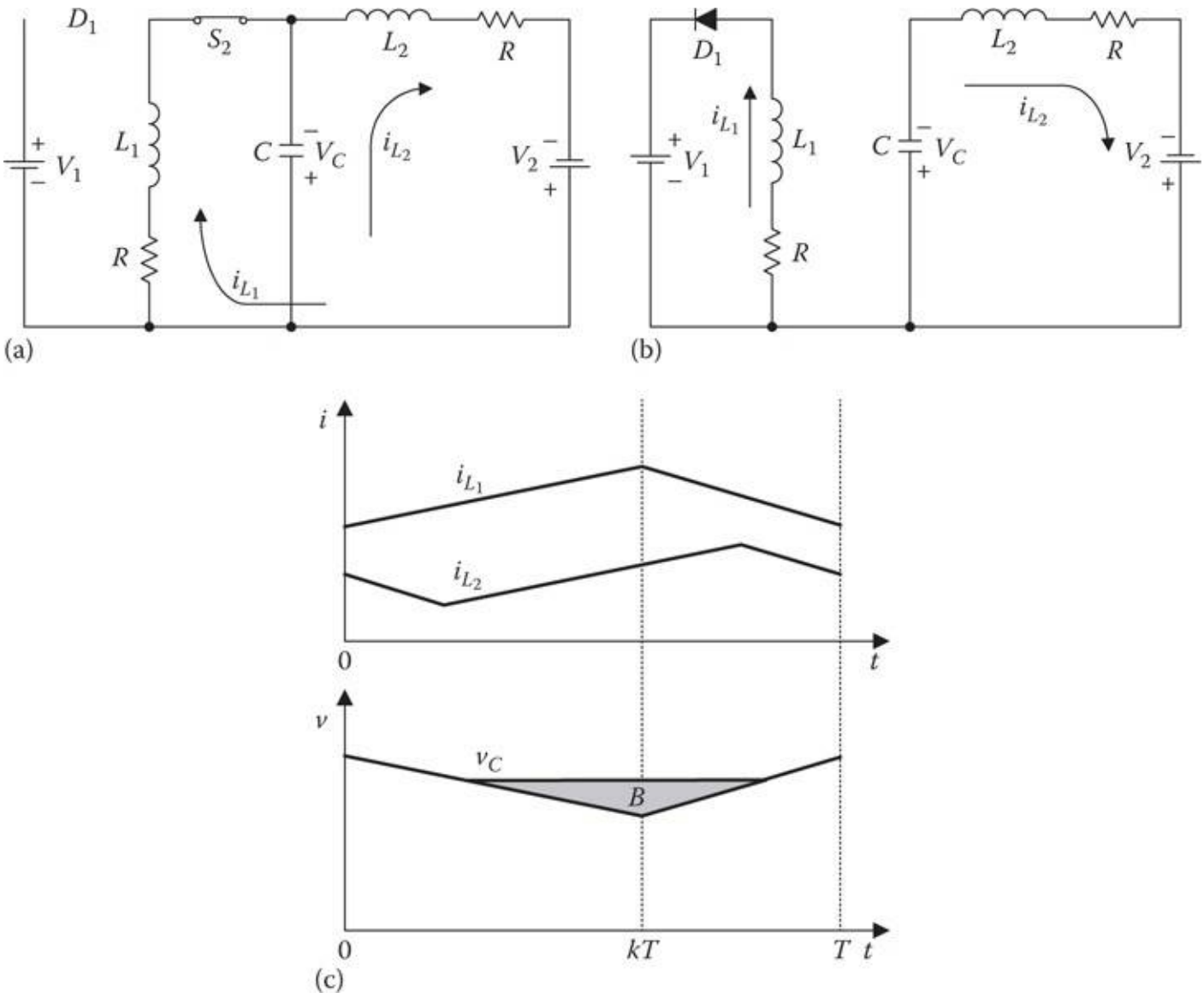


FIGURE 10.5
Mode D. (a) Switch-on. (b) Switch-off. (c) Waveforms with enlarged variations.

10.2.5 Summary

The switch status of all modes is listed in Table 10.1. From the table, it can be seen that only one switch works in one mode so that this converter becomes very simple and effective.

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TABLE 10.1
Switch's Status

Switch or Diode	Mode A (QI)		Mode B (QII)		Mode C (QIII)		Mode D (QIV)	
	State-On	State-Off	State-On	State-Off	State-On	State-Off	State-On	State-Off
Circuit	Circuit 1				Circuit 2			
S_1	ON				ON			
D_1				ON				ON
S_2			ON				ON	
D_2		ON				ON		

Note: The blank status means off.

10.3 Mode A (Quadrant I Operation)

As shown in Figure 10.2a and b, the voltage across capacitor C increases during switch-on and decreases during switch-off. Capacitor C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor L_1. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

10.3.1 Circuit Description

When switch S_1 is on, the source current $i_1 = i_{L_1} + i_{L_2}$. Inductor L_1 absorbs energy from the source. In the meantime, inductor L_2 absorbs energy from source and capacitor C, and both currents i_{L_1} and i_{L_2} increase. When switch S_1 is off, source current $i_i = 0$. Current i_{L_1} flows through the freewheeling diode D_2 to charge capacitor C. Inductor L_1 transfers its stored energy to capacitor C. In the meantime, current i_{L_2} flows through the load V_2 and freewheeling diode D_2 to keep itself continuous. Both currents i_{L_1} and i_{L_2} decrease. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 10.2c. The equivalent circuits in switch-on and switch-off states are shown in Figure 10.2a and b.

Actually, the variations of currents i_{L_1} and i_{L_2} are small so that

$$i_{L_1} \approx I_{L_1} \quad \text{and} \quad i_{L_2} \approx I_{L_2}$$

The charge on capacitor C increases during switch-off and switch-on:

$$Q_+ = (1-k)T\, I_{L_1}$$

$$Q_- = kT\, I_{L_2}$$

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In a whole period investigation, $Q_+ = Q_-$.

Thus,

$$I_{L_2} = \frac{1-k}{k} I_{L_1} \tag{10.1}$$

Since capacitor C performs as a low-pass filter, the output current $I_{L_2} = I_2$.

The source current $i_1 = i_{L_1} + i_{L_2}$ during switch-on, and $i_1 = 0$ during switch-off. The average source current I_1 is

$$I_1 = k \times i_1 = k(i_{L_1} + i_{L_2}) = k\left(1 + \frac{1-k}{k}\right) I_{L_1} = I_{L_1}$$

Hence, the output current is

$$I_2 = \frac{1-k}{k} I_1 \tag{10.2}$$

The input and output powers are

$$P_i = V_1 I_1$$

and

$$P_o = V_2 I_2$$

The power losses are as follows:

$V_S I_1$: Switch power loss

$RI_{L_1}^2$: Power loss across inductor L_1

$V_D I_1$: Diode power loss

$RI_{L_2}^2$: Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_1^2 + I_2^2) \tag{10.3}$$

Since

$$P_i = P_o + P_{loss}$$

hence

$$V_1 I_1 = V_2 I_2 + (V_S + V_D) I_1 + R(I_1^2 + I_2^2) \tag{10.4}$$

or

$$V_1 = V_2 \frac{1-k}{k} + (V_S + V_D) + RI_2\left(\frac{k}{1-k} + \frac{1-k}{k}\right) \tag{10.5}$$

The output current is

$$I_2 = \frac{V_1 - V_S - V_D - V_2((1-k)/k)}{R(k/(1-k) + (1-k)/k)} \tag{10.6}$$

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The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{\min} = \frac{V_2}{V_1 + V_2 - V_S - V_D} \tag{10.7}$$

The power transfer efficiency is

$$\eta_A = \frac{P_o}{P_i} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + \left((V_S + V_D)/V_2\right)\left(k/(1-k)\right) + \left(RI_2/V_2\right)\left[1 + \left((1-k)/k\right)^2\right]} \tag{10.8}$$

10.3.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_1 - RI_1)$ during switch-on and $(V_C + RI_1)$ during switch-off, the average voltage across capacitor C is

$$kT(V_1 - RI_1) = (V_C + RI_1)(1-k)T$$

Hence,

$$V_C = \frac{k}{1-k}V_1 - \frac{1}{1-k}RI_1 = \frac{k}{1-k}V_1 - RI_2\frac{k}{(1-k)^2} = \frac{k}{1-k}\left(V_1 - \frac{RI_2}{1-k}\right) \tag{10.9}$$

The peak-to-peak variation of capacitor voltage v_C is

$$\Delta v_C = \frac{Q}{C} = \frac{kTI_2}{C} = \frac{kI_2}{fC}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{(1-k)I_2}{2fC(V_1 - RI_2(1/(1-k)))} \tag{10.10}$$

The peak-to-peak variation of inductor current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_1 - V_S - RI_1}{L_1}kT$$

The variation ratio of inductor current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = k\frac{V_1 - V_S - RI_1}{2fL_1 I_1} \tag{10.11}$$

The peak-to-peak variation of inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_1 - V_S - V_2 + V_C - RI_2}{L_2}kT = \frac{V_1 - V_S - RI_1}{L_2}kT$$

The variation ratio of inductor current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = k\frac{V_1 - V_S - RI_1}{2fL_2 I_2} \tag{10.12}$$

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The freewheeling diode's current i_{D_2} during switch-off is $i_{D_2} = i_{L_1} + i_{L_2}$. Its peak-to-peak variation is

$$\Delta i_{D_2} = \Delta i_{L_1} + \Delta i_{L_2} = \frac{V_1 - V_S - RI_1}{L} kT$$

where $L = L_1L_2/(L_1 + L_2)$.

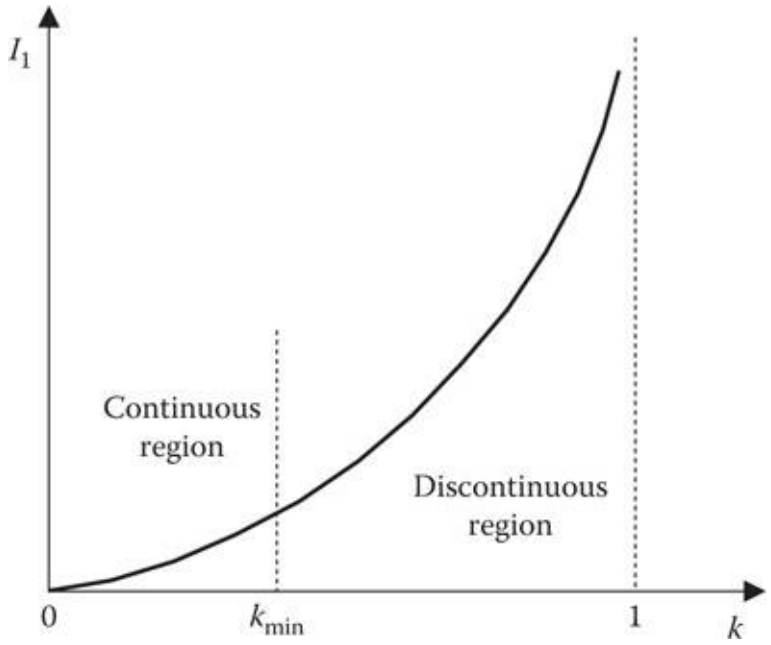


FIGURE 10.6
Boundary between continuous and discontinuous regions of Mode A.

The variation ratio of the diode current i_{D_2} is

$$\zeta_{D_2} = \frac{\Delta i_{D_2}/2}{I_{L_1} + I_{L_2}} = k\frac{V_1 - V_S - RI_1}{2fL(I_1 + I_2)} = k^2\frac{V_1 - V_S - RI_1}{2fLI_1} \tag{10.13}$$

10.3.3 Discontinuous Region

If the diode current becomes zero before S_1 switch is on again, the converter works in discontinuous region. The condition is $\zeta_{D_2} = 1$, that is,

$$k^2 = \frac{2fLI_1}{V_1 - V_S - RI_1} \tag{10.14}$$

From Equations 10.7 and 10.14, the boundary between continuous and discontinuous regions is shown in Figure 10.6. Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

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10.4 Mode B (Quadrant II Operation)

As shown in Figure 10.3a and b, the voltage across capacitor C decreases during switch-on and increases during switch-off. Capacitor C acts as the primary means of storing and transferring energy from the load battery to the source via inductor L_2. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$, even though it stores and transfers energy from the load V_2 to the source V_1.

10.4.1 Circuit Description

When switch S_2 is off, source current $i_1 = 0$. Current i_{L_1} flows through the switch S_2 and capacitor C and increases. Current i_{L_1} flows through the switch S_2 and increases. When switch S_2 is off, the source current $i_1 = i_{L_1} + i_{L_2}$. The freewheeling diode D_1 is conducted. Both currents i_{L_1} and i_{L_2} decrease. Inductor L_1 transfers its stored energy to capacitor C. In the meantime, current i_{L_2} flows through the source V_1. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 10.3c. The equivalent circuits in switch-on and switch-off states are shown in Figure 10.3a and b.

Actually, the variations of currents i_{L1} and i_{L2} are small so that

$$i_{L_1} \approx I_{L_1} \quad \text{and} \quad i_{L_2} \approx I_{L_2}$$

The charge on capacitor C increases during switch-off and switch-on:

$$Q+ = (1-k)TI_{L_2}$$

$$Q- = kTI_{L_1}$$

In a whole period investigation, Q+ = Q−.
Thus,

$$I_{L_1} = \frac{1-k}{k} I_{L_2} \tag{10.15}$$

Since capacitor C performs as a low-pass filter, the output current $I_{L_2} = I_2$.

The source current $i_1 = i_{L_1} + i_{L_2}$ during switch-on, and $i_1 = 0$ during switch-off. The average source current I_1 is

$$I_1 = (1-k)i_1 = (1-k)(i_{L_1} + i_{L_2}) = (1-k)\left(1 + \frac{1}{1-k}\right) I_{L_1} = I_{L_1}$$

Hence, the output current is

$$I_1 = \frac{1-k}{k} I_2 \tag{10.16}$$

The input and output powers are

$$P_i = V_2 I_2$$

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and

$$P_o = V_1 I_1$$

The power losses are as follows:

$V_S I_1$: Switch power loss

$RI_{L_1}^2$: Power loss across inductor L_1

$V_D I_1$: Diode power loss

$RI_{L_2}^2$: Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_1^2 + I_2^2) \tag{10.17}$$

Since

$$P_i = P_o + P_{loss}$$

hence

$$V_2 I_2 = V_1 I_1 + (V_S + V_D) I_1 + R(I_1^2 + I_2^2) \tag{10.18}$$

or

$$V_2 = \frac{1-k}{k}(V_1 + V_S + V_D) + RI_1\left(\frac{k}{1-k} + \frac{1-k}{k}\right) \tag{10.19}$$

The output current is

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D)((1-k)/k)}{R((k/(1-k)) + ((1-k)/k))} \tag{10.20}$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + V_D} \tag{10.21}$$

The power transfer efficiency is

$$\eta_B = \frac{P_o}{P_i} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + ((V_S + V_D / V_1)) + (RI_1 / V_1)[1 + ((1-k)/k)^2]} \tag{10.22}$$

10.4.2 Variations of Currents and Voltages

Because the voltage across the inductor L_2 is $(V_2 - RI_2)$ during switch-on and $(V_1 - V_2 + V_C + RI_2)$ during switch-off, the average voltage across capacitor C is

$$kT(V_2 - RI_2) = (V_1 - V_2 + V_C + RI_2)(1-k)T$$

Hence,

$$V_C = \frac{V_2}{1-k} - V_1 - \frac{1}{1-k} RI_2 = \frac{V_2}{1-k} - V_1 - RI_1 \frac{k}{(1-k)^2} \tag{10.23}$$

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The peak-to-peak variation of capacitor voltage v_C is

$$\Delta v_C = \frac{Q_-}{C} = \frac{kTI_1}{C} = \frac{kI_1}{fC}$$

The variation ratio of capacitor voltage v_C is

$$\Delta i_{L_1} = \frac{V_C - V_S - RI_1}{L_1} kT = \frac{V_2 - V_S - RI_2}{L_1} kT$$

The peak-to-peak variation of current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_C - V_S - RI_1}{L_1} kT = \frac{V_2 - V_S - RI_2}{L_1} kT$$

The variation ratio of inductor current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = k\frac{V_2 - V_S - RI_2}{2fL_1I_1} \tag{10.25}$$

The peak-to-peak variation of inductor current i_{L_2} is

$$\Delta i_{L_2} = \frac{V_2 - V_S - RI_2}{L_2} kT$$

The variation ratio of inductor current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = k\frac{V_2 - V_S - RI_2}{2fL_2I_2} \tag{10.26}$$

The freewheeling diode's current i_{D_1} during switch-off is $i_{D_1} = i_{L_1} + i_{L_2}$. Its peak-to-peak variation is

$$\Delta i_{D_2} = \Delta i_{L_1} + \Delta i_{L_2} = \frac{V_2 - V_S - RI_2}{L} kT$$

where $L = L_1L_2/(L_1 + L_2)$.
The variation ratio of diode current i_{D_1} is

$$\zeta_{D_1} = \frac{\Delta i_{D_2}/2}{I_{L_1} + I_{L_2}} = k\frac{V_2 - V_S - RI_2}{2fL(I_1 + I_2)} = k^2\frac{V_2 - V_S - RI_2}{2fLI_2} \tag{10.27}$$

10.4.3 Discontinuous Region

If the diode current becomes zero before S_2 is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D_1} = 1$, that is,

$$k^2 = \frac{2fLI_2}{V_2 - V_S - RI_2} \tag{10.28}$$

From Equations 10.21 and 10.28, the boundary between continuous and discontinuous regions is shown in Figure 10.7. Particularly, since conduction duty k is greater than $k_{\min}$ and the

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current is high, the converter usually works in the continuous region.

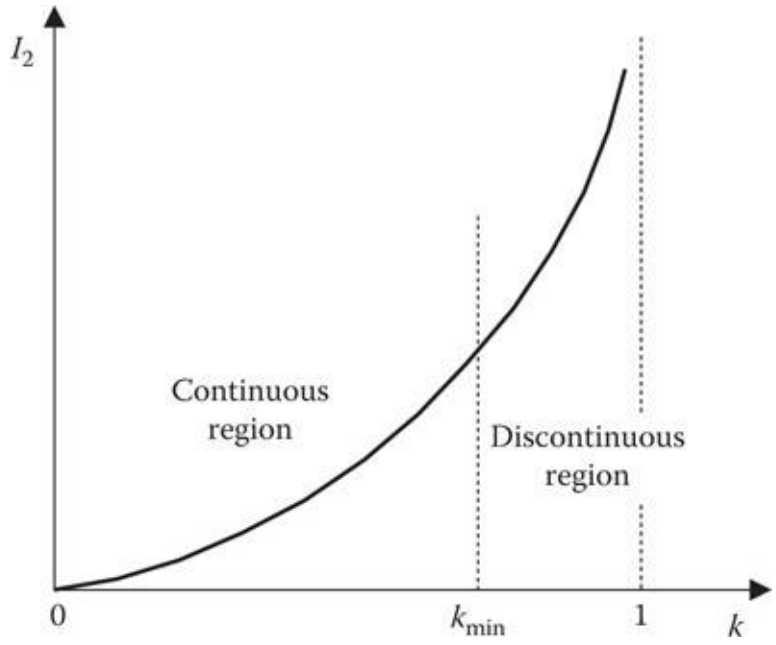


FIGURE 10.7
Boundary between continuous and discontinuous regions of Mode B.

10.5 Mode C (Quadrant III Operation)

As shown in Figure 10.4a and b, the voltage across capacitor C increases during switch-off and decreases during switch-on. Capacitor C acts as the primary means of storing and transferring energy from the input source to the output load via the pump inductor L_1. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$, even though it stores and transfers energy from the input to the output.

10.5.1 Circuit Description

The equivalent circuits in switch-on and switch-off states are shown in Figure 10.4a and b. When switch S_1 is on, the source current $i_1 = i_{L_1}$. Inductor L_1 absorbs energy from the source. In the meantime, the inductor L_2 absorbs energy from capacitor C, current i_{L_1} increases, and i_2 decreases. When switch S_1 is off, the source current $i_1 = 0$. Current i_{L_1} flows through the freewheeling diode D_2 to charge capacitor C and current i_2 increases. Inductor L_1 transfers its stored energy to capacitor C and the load V_2. Current i_{L_1} decreases and i_2 increases. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 10.4c.

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Actually, the variations of currents i_{L_1} and i_{L_2} are small so that $i_{L_1} \approx I_{L_1}$ and $i_{L_2} \approx I_{L_2} = I_2$. Since the capacitor current $i_{C\text{-}on}$ is equal to I_2 during switch-on, $i_{C\text{-}off}$ should be

$$i_{C\text{-}off} = \frac{k}{1-k} I_2 \tag{10.29}$$

Inductor current i_{L_1} during switching-off is

$$i_{L_1} = I_2 + i_{C\text{-}off} = (1 + (k/(1-k)))I_2 = \frac{1}{1-k} I_2 \tag{10.30}$$

The source average current I_1 is

$$I_1 = k i_{L_1} = \frac{k}{1-k} I_2 \quad \text{or} \quad I_{L_1} = \frac{1}{k} I_1 \tag{10.31}$$

The input and output powers are

$$P_i = V_1 I_1$$

and

$$P_o = V_2 I_2$$

The power losses are as follows:

$V_S I_1$: Switch power loss

$R I_{L_1}^2$: Power loss across inductor L_1

$V_D I_1$: Diode power loss

$R I_{L_2}^2$: Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R\left[\left(\frac{I_1}{k}\right)^2 + I_2^2\right] \tag{10.32}$$

Since

$$P_i = P_o + P_{loss}$$

hence

$$V_1 I_1 = V_2 I_2 + (V_S + V_D) I_1 + R\left[\left(\frac{I_1}{k}\right)^2 + I_2^2\right] \tag{10.33}$$

or

$$V_1 = V_2 \frac{1-k}{k} + (V_S + V_D) + R I_2 \left[\frac{1}{k(1-k)} + \frac{1-k}{k}\right] \tag{10.34}$$

The output current is

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$$I_2 = \frac{V_1 - V_S - V_D - V_2((1-k)/k)}{R[(1/(k(1-k))) + ((1-k)/k)]} \tag{10.35}$$

The minimum conduction duty k corresponding to $I_2 = 0$ is

$$k_{\min} = \frac{V_2}{V_1 + V_2 - V_S - V_D} \tag{10.36}$$

The power transfer efficiency is

$$\eta_C = \frac{P_o}{P_i} = \frac{V_2 I_2}{V_1 I_1} = \frac{1}{1 + ((V_S + V_D)/V_2)(k/(1-k)) + (RI_2/V_2)[1 + (1/(1-k))^2]} \tag{10.37}$$

10.5.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_1 - RI_{L_1})$ during switch-on and $(V_C + RI_{L_1})$ during switch-off, the average voltage across capacitor C is

$$kT(V_1 - RI_{L_1}) = (V_C + RI_{L_1})(1-k)T$$

Hence,

$$V_C = \frac{k}{1-k}V_1 - \frac{1}{1-k}RI_{L_1} = \frac{k}{1-k}V_1 - RI_2\frac{1}{(1-k)^2} \tag{10.38}$$

The peak-to-peak variation of capacitor voltage v_C is

$$\Delta v_C = \frac{kTI_2}{C} = \frac{kI_2}{fC}$$

The variation ratio of capacitor voltage v_C is

$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_2}{2fC[(k/(1-k))V_1 - (RI_2/(1-k)^2)]} \tag{10.39}$$

The peak-to-peak variation of inductor current i_{L_1} is

$$\Delta i_{L_1} = \frac{V_1 - V_S - RI_1}{L_1}kT$$

The variation ratio of inductor current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = k\frac{V_1 - V_S - RI_1}{2fL_1I_1} \tag{10.40}$$

Diode's current i_{D_2} during switch-off is $i_{D_2} = i_{L_1}$. Its peak-to-peak variation is

$$\Delta i_{D_2} = \Delta i_{L_1} = \frac{V_1 - V_S - RI_1}{L_1}kT$$

and the variation ratio of inductor current i_{D_2} is

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$$\zeta_{D_2} = \xi_1 = \frac{\Delta i_{D_2}/2}{I_{L_1}} = k\frac{V_1 - V_S - RI_1}{2fL_1I_1} \tag{10.41}$$

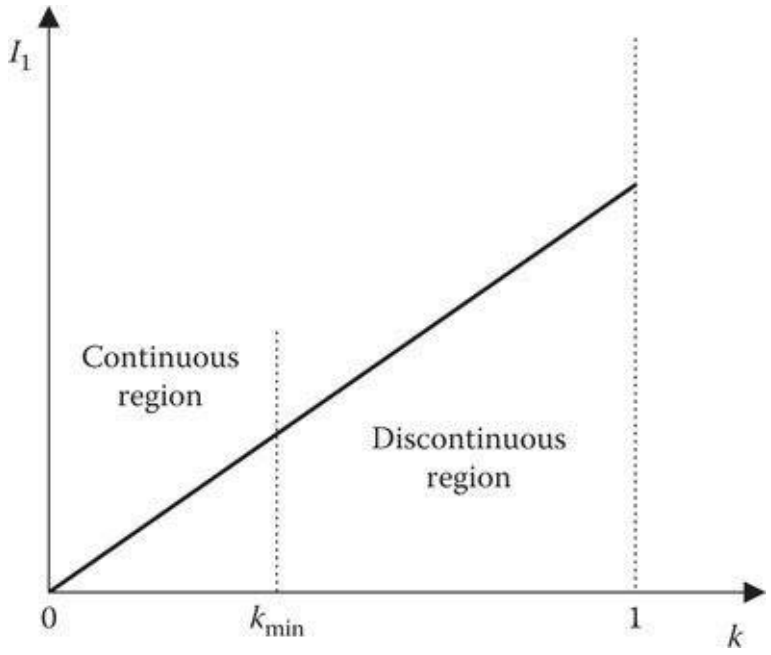


FIGURE 10.8
Boundary between continuous and discontinuous regions of Mode C.

Since voltage v_C varies very little, the peak-to-peak variation of inductor current i_{L_o} is calculated by the area A of a triangle with width $T/2$ and height $\Delta v_C/2$:

$$\Delta i_{L_2} = \frac{A}{L_2} = \frac{1}{2}\frac{T}{2}\frac{kTI_2}{2CL_2} = \frac{k}{8f^2CL_2}I_2$$

The variation ratio of inductor current i_{L_2} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_2} = \frac{k}{16f^2CL_2} \tag{10.42}$$

10.5.3 Discontinuous Region

If the diode current becomes zero before S_1 is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D_2} = 1$, that is,

$$k = \frac{2fL_1I_1}{V_1 - V_S - RI_1} \tag{10.43}$$

From Equations 10.36, 10.37, 10.38, 10.39, 10.40, 10.41, 10.42 and 10.43, the boundary between continuous and discontinuous regions is shown in Figure 10.8. Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

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10.6 Mode D (Quadrant IV Operation)

As shown in Figure 10.5a and b, the voltage across capacitor C decreases during switch-on and increases during switch-off. Capacitor C acts as the primary means of storing and transferring energy from the load battery to the source via inductor L_1. Assuming capacitor C to be sufficiently large, the variation of the voltage across capacitor C from its average value V_C can be neglected in steady state, that is, $v_C(t) \approx V_C$, even though it stores and transfers energy from the load V_2 to the source V_1.

10.6.1 Circuit Description

When switch S_2 is on, source current $i_1 = 0$. Current i_{L_1} flows through the switch S_2 and then capacitor C and load battery V_2. It increases and $i_{L_1} = i_{C\text{-}on} + i_2$. When switch S_2 is off, the source current is $i_1 = i_{L_1}$. The freewheeling diode D_1 is conducted. Current i_{L_1} decreases. Inductor L_1 transfers its stored energy to source V_1. In order to analyze the circuit working procession, these waveforms with enlarged variations are shown in Figure 10.5c. The equivalent circuits in switch-on and switch-off states are shown in Figure 10.5a and b.

Actually, the variations of currents i_{L_1} and i_{L_2} are small so that $i_{L_1} \approx I_{L_1}$ and $i_{L_2} \approx I_2$. Since the capacitor current $i_{C\text{-}off}$ is equal to I_2 during switching-off, $i_{C\text{-}on}$ should be

$$i_{C\text{-}on} = \frac{1-k}{k} I_2 \tag{10.44}$$

Inductor current i_{L_1} during switch-on is

$$i_{L_1} = I_2 + i_{C\text{-}on} = \left(1 + \frac{1-k}{k}\right) I_2 = \frac{1}{k} I_2 \tag{10.45}$$

The source average current I_1 is

$$I_1 = (1-k) i_{L_1} = \frac{1-k}{k} I_2 \quad \text{or} \quad I_{L_1} = \frac{1}{1-k} I_1 \tag{10.46}$$

The input and output powers are

$$P_i = V_2 I_2$$

and

$$P_o = V_1 I_1$$

The power losses are as follows:

$V_S I_1$: Switch power loss

$R I_{L_1}^2$: Power loss across inductor L_1

$V_D I_1$: Diode power loss

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$RI_{L_2}^2$: Power loss across inductor L_2

The total power losses are

$$P_{loss} = V_S I_1 + V_D I_1 + R(I_{L1}^2 + I_2^2) \tag{10.47}$$

Since

$$P_i = P_o + P_{loss}$$

Hence,

$$V_2 I_2 = V_1 I_1 + (V_S + V_D) I_1 + R(I_{L1}^2 + I_2^2) \tag{10.48}$$

or

$$V_2 = \frac{1-k}{k}(V_1 + V_S + V_D) + RI_1\left[\frac{1}{k(1-k)} + \frac{k}{1-k}\right] \tag{10.49}$$

The output current is

$$I_1 = \frac{V_2 - (V_1 + V_S + V_D)((1-k)/k)}{R[(1/(k(1-k))) + (k/(1-k))]} \tag{10.50}$$

The minimum conduction duty k corresponding to $I_1 = 0$ is

$$k_{\min} = \frac{V_1 + V_S + V_D}{V_1 + V_2 + V_S + V_D} \tag{10.51}$$

The power transfer efficiency is

$$\eta_D = \frac{P_o}{P_i} = \frac{V_1 I_1}{V_2 I_2} = \frac{1}{1 + ((V_S + V_D)/V_1) + (RI_1/V_1)[(1/(1-k)^2) + (k/(1-k))^2]} \tag{10.52}$$

10.6.2 Variations of Currents and Voltages

Because the voltage across the inductor L_1 is $(V_C - RI_{L_1})$ during switch-on and $(V_1 + RI_{L_1})$ during switch-off, the average voltage across capacitor C is

$$kT(V_C - RI_{L_1}) = (V_1 + RI_{L_1})(1-k)T$$

Hence,

$$V_C = \frac{1-k}{k}V_1 + \frac{1}{k}RI_{L_1} = \frac{1-k}{k}V_1 + RI_1\frac{1}{k(1-k)} \tag{10.53}$$

The peak-to-peak variation of capacitor voltage v_C is

$$\Delta v_C = \frac{(1-k)TI_2}{C} = \frac{kI_1}{fC}$$

The variation ratio of capacitor voltage v_C is

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$$\rho = \frac{\Delta v_C/2}{V_C} = \frac{kI_1}{2fC[((1-k)/k)V_1 + (RI_1/(k(1-k)))]} \tag{10.54}$$

The peak-to-peak variation of current i_{L_1} is

$$\Delta i_{L_1} = kT\frac{V_C - V_S - RI_1}{L_1} = (1-k)\frac{V_2 - V_S - RI_2}{fL_1}$$

The variation ratio of inductor current i_{L_1} is

$$\xi_1 = \frac{\Delta i_{L_1}/2}{I_{L_1}} = (1-k)\frac{V_2 - V_S - RI_2}{2fL_1I_1} \tag{10.55}$$

Current i_{D_1} during switch-off is $i_{D_1} = i_{L_1}$. Its peak-to-peak variation is

$$\Lambda i_{D_1} = \Delta i_{L_1} = (1-k)\frac{V_C - V_S - RI_2}{fL_1}$$

And the variation ratio of inductor current i_{D_1} is

$$\zeta_{D_1} = \xi_1 = \frac{\Delta i_{D_1}/2}{I_{L_1}} = k\frac{V_2 - V_S - RI_2}{2fL_1I_2} \tag{10.56}$$

Since voltage v_C varies very little, the peak-to-peak variation of inductor current i_{L_2} is calculated by the area B of a triangle with width $T/2$ and height $\Delta v_C/2$:

$$\Delta i_{L_2} = \frac{B}{L_2} = \frac{1}{2}\frac{T}{2}\frac{kTI_1}{2CL_2} = \frac{k}{8f^2CL_2}I_1$$

The variation ratio of inductor current i_{L1} is

$$\xi_2 = \frac{\Delta i_{L_2}/2}{I_2} = \frac{1-k}{16f^2CL_2} \tag{10.57}$$

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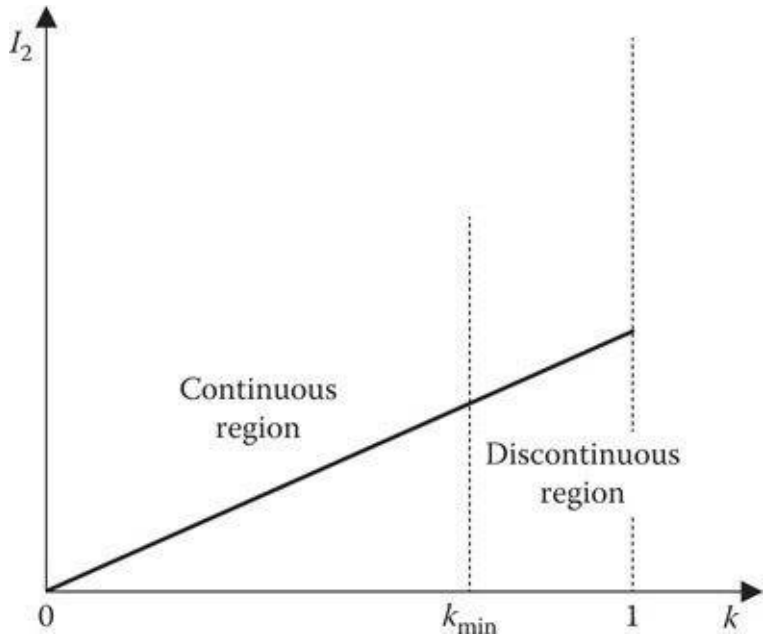


FIGURE 10.9
Boundary between continuous and discontinuous regions of Mode D.

10.6.3 Discontinuous Region

If the diode current becomes zero before S_2 is switched on again, the converter works in discontinuous region. The condition is $\zeta_{D_1} = 1$, that is,

$$k = \frac{2fL_1I_2}{V_2 - V_S - RI_2} \tag{10.58}$$

From Equations 10.51, 10.52, 10.53, 10.54, 10.55, 10.56, 10.57 and 10.58, the boundary between continuous and discontinuous regions is shown in Figure 10.9. Particularly, since conduction duty k is greater than k_{min} and the current is high, the converter usually works in the continuous region.

10.7 Simulation Results

In order to verify the previous analysis and calculation formulae and the characteristics of this converter, we applied the PSpice simulation methodology to obtain the results shown in Figures 10.10, 10.11, 10.12 and 10.13. The first plot is current i_{L_1}, the second plot is current i_{L_2}, and the third plot is voltage v_C. The repeating frequency f = 50 Hz. The conduction duty cycle k = 0.4 for Modes A and C and 0.8 for Modes B and D. These results agree with the analysis and calculations in the previous sections.

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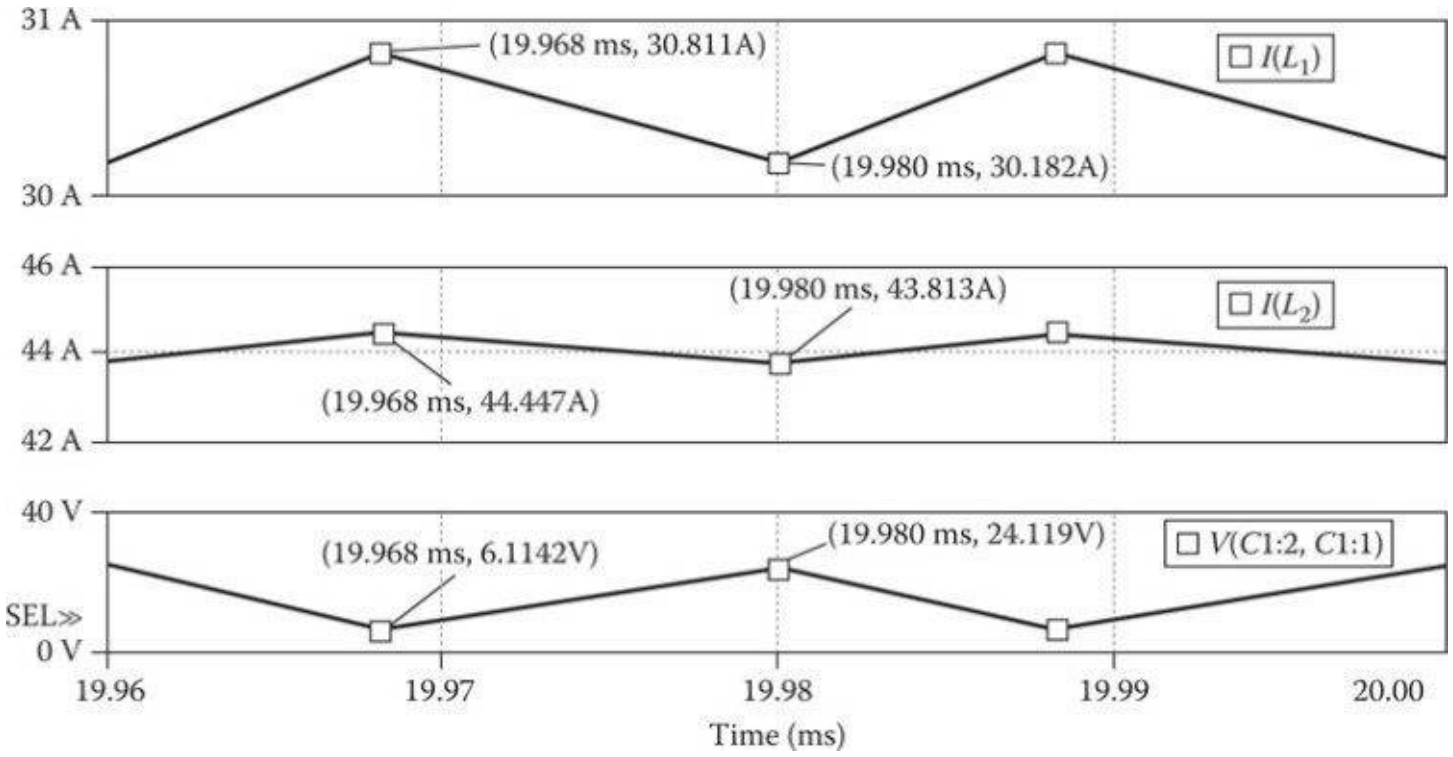


FIGURE 10.10
Simulation results of Mode A.

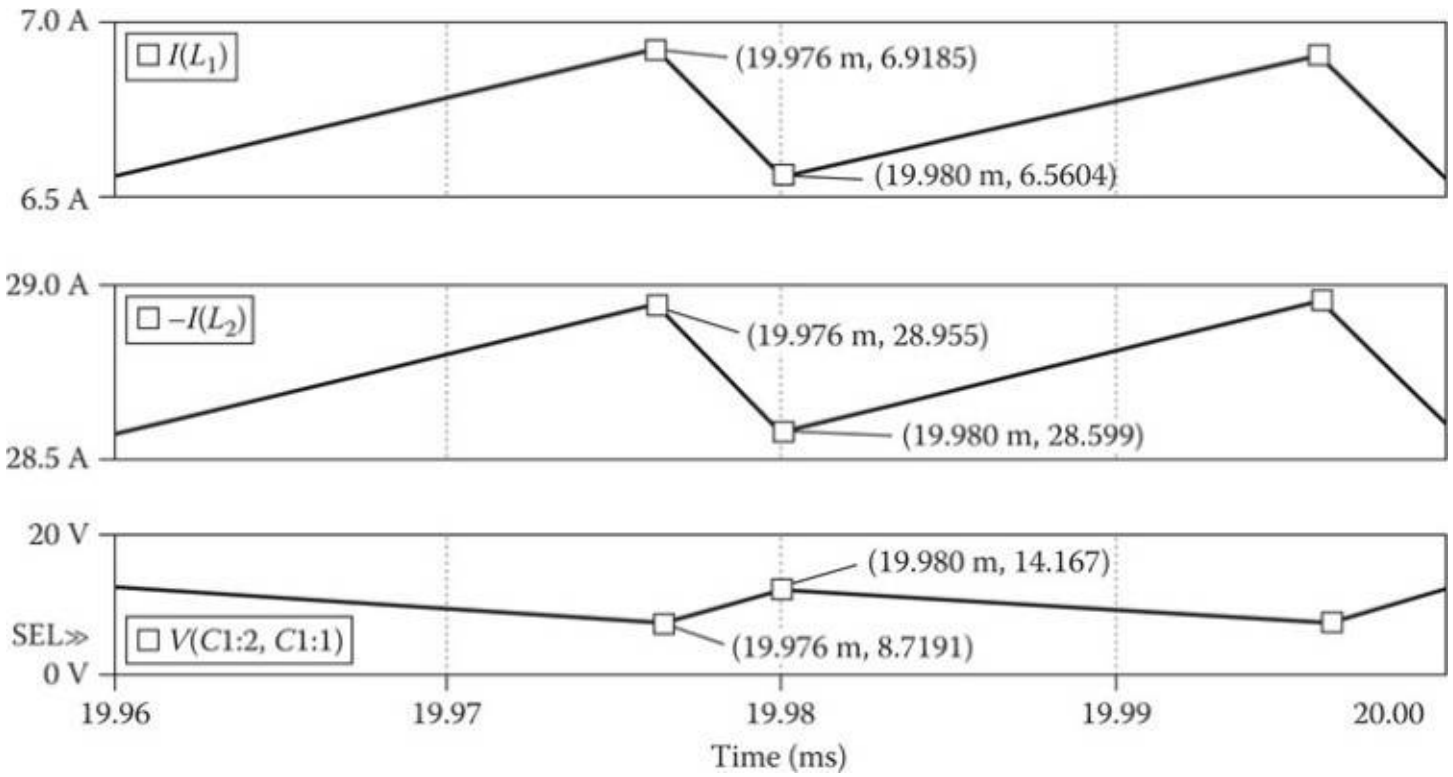


FIGURE 10.11
Simulation results of Mode B.

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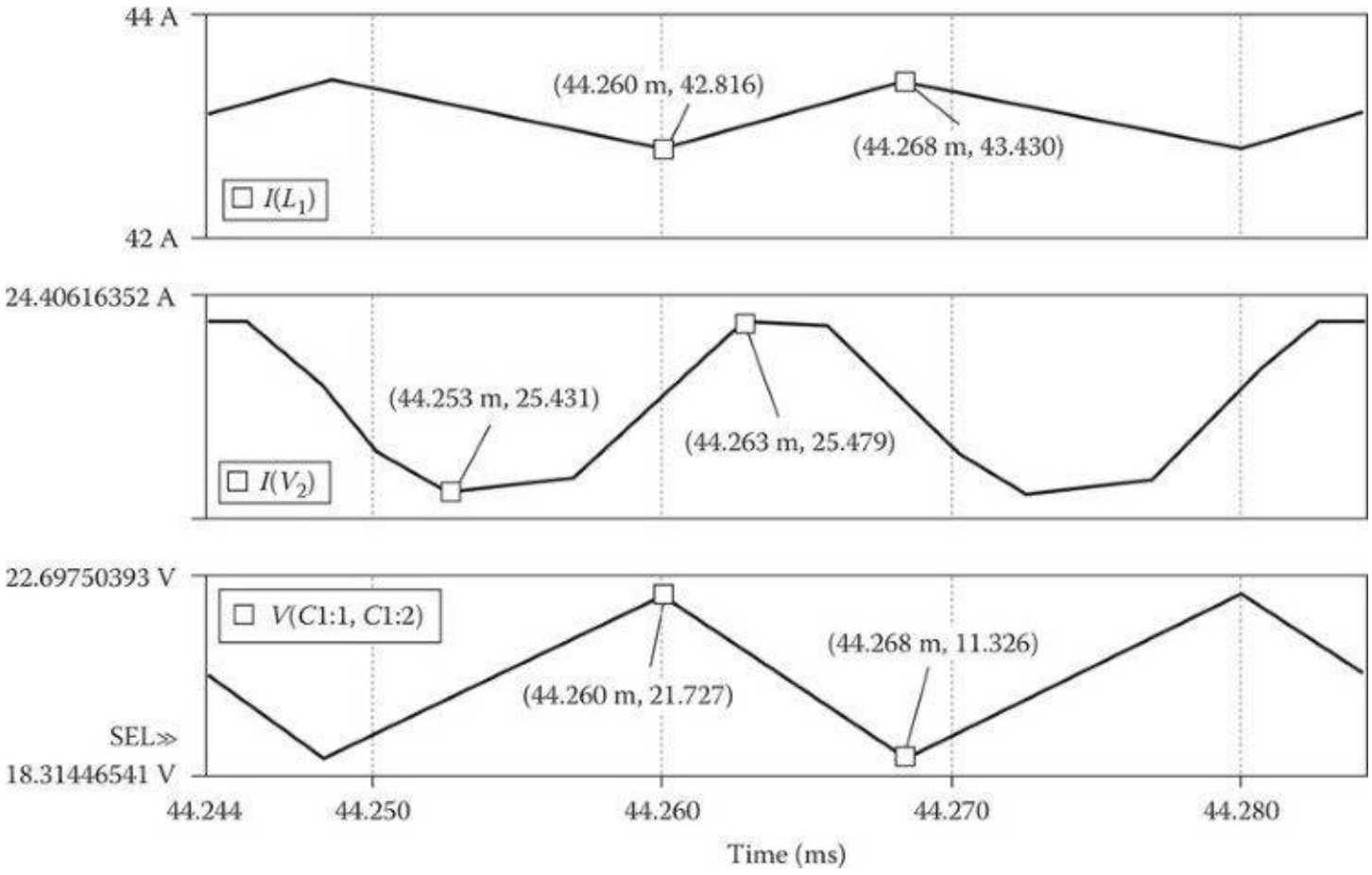


FIGURE 10.12
Simulation results of Mode C.

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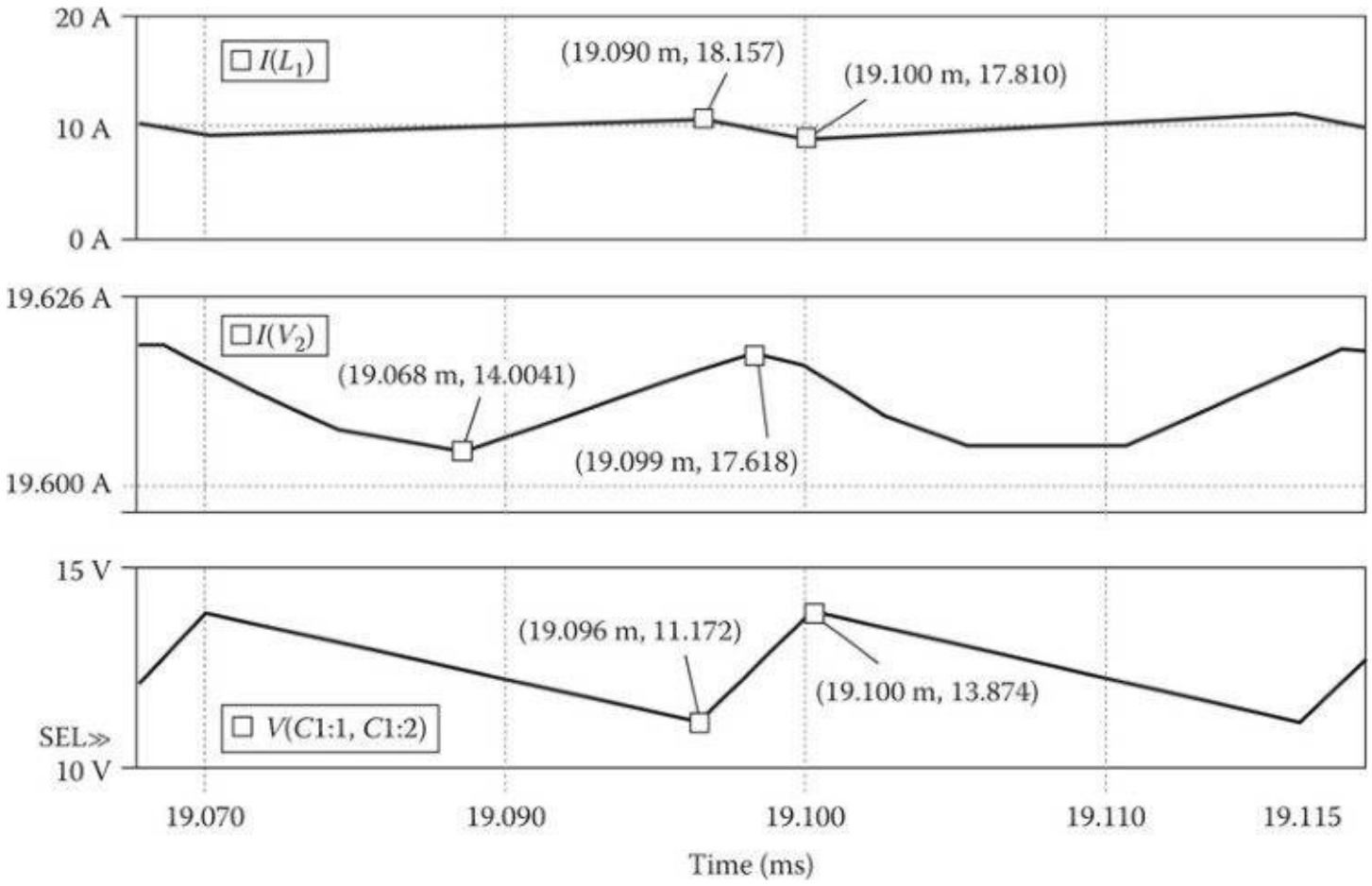


FIGURE 10.13
Simulation results of Mode D.

10.8 Experimental Results

In order to verify the previous analysis and calculation formulae and the characteristics of this converter, we collected the following experimental results. The experimental testing conditions are V_1 = 42 V, V_2 = 14 V, V_S = 0.3 V, V_D = 0.5 V, R = 0.05 Ω $L_1 = L_2 = L = L_o$ = 0.5 mH, C = 20 μF, and f = 50 kHz.

The experimental results corresponding to various conduction duty k are shown in Table 10.2 for the Mode A, Table 10.3 for the Mode B, Table 10.4 for the Mode C, and Table 10.5 for the Mode D.

When compared with the analysis and calculations, the experimental results are reasonable. From these data, we can see that the function of this converter has been verified.

TABLE 10.2
Experimental Results for Mode A (Quadrant QI) with k_{min} = 0.2536

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k	I_1 (A)	I_2 (A)	V_C (V)	P_i (W)	P_o (W)	η_A (%)
0.26	3.0	8.5	14.28	126	119	94.4
0.28	13.7	35.1	15.07	575	491	85.4
0.30	26.5	61.8	15.77	1113	865	77.7
0.32	41.5	88.2	16.33	1743	1235	70.8
0.34	58.8	114.2	18.77	2470	1599	64.7

TABLE 10.3
Experimental Results for Mode B (Quadrant QII) with $k_{min} = 0.7535$

k	I_2 (A)	I_1 (A)	V_C (V)	P_i (W)	P_o (W)	η_B
0.76	8.81	2.78	13.70	123	117	94.9
0.78	35.72	10.08	12.72	500	423	84.6
0.80	62.0	15.5	11.67	870	652	75.0
0.82	87.7	19.3	10.57	1230	810	65.9
0.84	112.9	21.5	9.43	1580	903	57.1

TABLE 10.4
Experimental Results for Mode C (Quadrant QIII) with $k_{min} = 0.2536$

k	I_1 (A)	I_2 (A)	V_C (V)	P_i (W)	P_o (W)	η_C (%)
0.26	3.0	8.5	14.28	126	119	94.4
0.28	13.7	35.1	15.07	575	491	85.4
0.30	26.5	61.8	15.77	1113	865	77.7
0.32	41.5	88.2	16.33	1743	1235	70.8
0.34	58.8	114.2	18.77	2470	1599	64.7

TABLE 10.5
Experimental Results for Mode D (Quadrant QIV) with $k_{min} = 0.7535$

k	I_2 (A)	I_1 (A)	V_C (V)	P_i (W)	P_o (W)	η_D
0.76	8.81	2.78	13.70	123	117	94.9
0.78	35.72	10.08	12.72	500	423	84.6
0.80	62.0	15.5	11.67	870	652	75.0
0.82	87.7	19.3	10.57	1230	810	65.9
0.84	112.9	21.5	9.43	1580	903	57.1

10.9 Discussion

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10.9.1 Discontinuous Conduction Mode

Usually, the industrial applications require the DC/DC converters working in continuous conduction mode. However, it is irresistible that DC/DC converter works in discontinuous conduction mode sometimes. The analysis in Sections 3.3, 4.3, 5.3, and 6.3 shows that during switch-off if currents i_{D_1} and i_{D_2} become zero before the next period switch-on, the state is called discontinuous conduction mode. The following factors affect the diode current to become discontinuous:

1. The switching frequency f is too low.
2. The conduction duty cycle k is too small and close $k_{\min}$.
3. The inductor L is too small.

10.9.2 Comparison with the Double-Output Luo-Converter

The analysis of the double-output Luo-converter is based on the ideal components. For example, all voltage drops are zero and inductor resistance is zero, that is, $V_S = V_D = 0$ and $R = 0$. If we use these conditions, the corresponding formulae will return back to those forms for double-output Luo-converter:

From Equation 7.5:

$$k = \frac{V_2}{V_1 + V_2} \quad \text{or} \quad V_2 = \frac{k}{1-k} V_1 \quad \text{and} \quad I_2 = \frac{1-k}{k} I_1$$

From Equation 7.19:

$$k = \frac{V_1}{V_1 + V_2} \quad \text{or} \quad V_1 = \frac{k}{1-k} V_2 \quad \text{and} \quad I_1 = \frac{1-k}{k} I_2$$

From Equation 7.34:

$$k = \frac{V_2}{V_1 + V_2} \quad \text{or} \quad V_2 = \frac{k}{1-k} V_1 \quad \text{and} \quad I_2 = \frac{1-k}{k} I_1$$

From Equation 7.48:

$$k = \frac{V_1}{V_1 + V_2} \quad \text{or} \quad V_1 = \frac{k}{1-k} V_2 \quad \text{and} \quad I_1 = \frac{1-k}{k} I_2$$

Because the power losses are zero, the power transfer efficiency is 100%.

10.9.3 Conduction Duty k

Since the source and load voltages are fixed, conduction duty k does not affect the voltage transfer gain. We have considered the power losses on the switches, diodes, and inductors. Therefore, the conduction duty k affects the output and input currents and power transfer efficiency. Usually, large k causes large currents and power losses. For each mode, there is a minimum conduction duty $k_{\min}$. When $k = k_{\min}$, the input and output currents are zero. In order to limit the overcurrent, the values of the conduction duty k are usually selected in the range of $k_{\min} < k < k_{\min} + 0.12$.

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10.9.4 Switching Frequency *f*

In this chapter, the repeating frequency f = 50 kHz was selected. Actually, the switching frequency f can be selected in the range between 10 and 500 kHz. Usually, the higher the frequency, the lower the current ripples.

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11

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Switched-Component Converters

Classic DC/DC converters consist of inductors and capacitors. They are large because of the mixture of inductors and capacitors. On engineering design experience, a circuit constructed by only an inductor or a capacitor may be small in size. In order to reduce the converter size and enlarge the power density (PD), a third generation of DC/DC converters have been developed, and they are called switched-component converters. Particularly, they are switched-capacitor (SC) DC/DC converters and switched-inductor (SI) DC/DC converters. The SC DC/DC converter is a new prototype of DC/DC conversion technology. Since an SC can be integrated into a power IC chip, these converters are small and have a high PD. However, most of the published papers avoid discussing the efficiency because most SC converters possess low power transfer efficiency. This section introduces an SC two-quadrant DC/DC converter implementing voltage-lift and current-amplification techniques with high efficiency, high PD, and low electromagnetic interference. Experimental results verified the advantages of this converter. Four-quadrant operation is required by industrial applications. SC converters can perform four-quadrant operations as well.

SC converters always perform in push–pull state, and the control circuitry is complex. A large number of capacitors are required, especially in the case of large differences between input and output voltages.

SI DC/DC converters are different prototypes of DC/DC conversion technology from SC converters. SI DC/DC converters have advantages such as simple structure, simple control circuitry, high efficiency, large power, and high PD. Usually, one inductor is required for an SI DC/DC converter. Since it consists of only one inductor, its size is small. This type of converter has outstanding advantages: no matter how many quadrant operations were used and how large the difference between input and output voltages is, only one inductor is usually employed in one SI DC/DC converter.

11.1 Introduction

A new type of DC/DC converter consisting of capacitors only was developed around 1980. Since it can be integrated into a power semiconductor IC chip, it has attracted much attention in recent years. However, most of the converters introduced in the literature perform single-quadrant operation. Some of them work in the flip-flop status, and their control circuit and topologies are very complex.

A newly designed DC/DC converter *two-quadrant DC/DC converter with SCs* was developed from the prototype of the authors' research work. This converter implements the voltage-lift and current-amplification techniques, so that it reaches the real high power density

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(PD) and high power transfer efficiency. In order to successfully reduce electromagnetic interference, a lower switching frequency f = 5 kHz was applied in this converter. It can perform step-down and step-up two-quadrant positive to positive DC/DC voltage conversion with high PD, low electromagnetic interference (EMI), and cheap topology in simple structure.

The conduction duty k is usually selected to be k = 0.5 in most of the papers in the literature. We have carefully analyzed this problem and verified its reasonableness.

Multiple-quadrant operation is required by industrial applications. Switched-capacitor (SC) multiple-quadrant converters and switched-inductor (SI) multiple-quadrant converters will be introduced in this chapter as well.

11.2 Two-Quadrant SC DC/DC Converter

A two-quadrant SC converter is shown in Figure 11.1. It consists of nine switches, seven diodes, and three capacitors. The high-voltage (HV) source and low-voltage (LV) load are usually constant voltages. The load can be a battery or motor back electromotive force (EMF). For example, the source voltage is 48 V and the load voltage is 14 V. There are two modes of operation:

1. *Mode A* (*quadrant I*)*:* Electrical energy is transferred from HV side to LV side.
2. *Mode B* (*quadrant II*)*:* Electrical energy is transferred from LV side to HV side.

11.2.1 Circuit Description

Each mode has two states: “on” and “off.” Usually, each state operates in different conduction duty *k*. The switching period is T where $T = 1/f$. The parasitic resistance of all switches is r_S, the equivalent resistance of all capacitors is r_C, and the equivalent voltage drop of all diodes is V_D. Usually, we select the three capacitors having the same capacitance $C = C_1 = C_2 = C_3$. Some reference data are useful: r_S = 0.03 Ω, r_C = 0.02 Ω and V_D = 0.5 V, f = 5 kHz, and C = 5000 μF.

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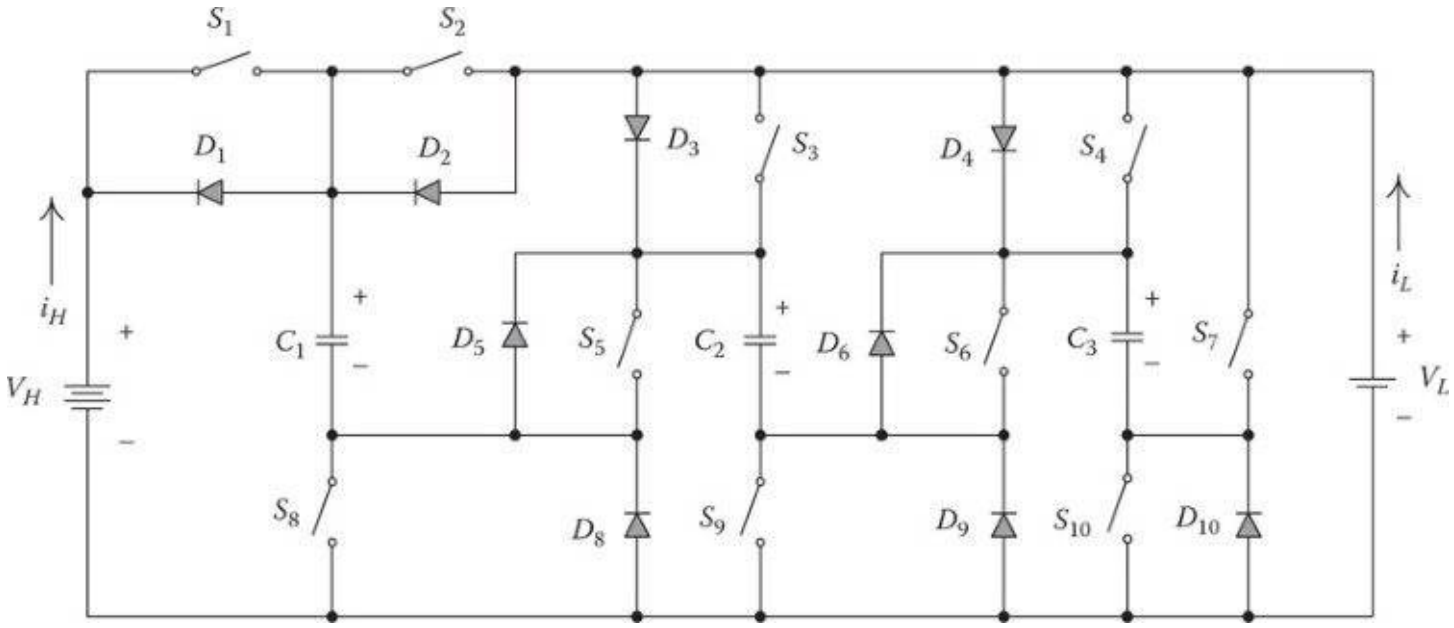


FIGURE 11.1
Two-quadrant DC/DC switched-capacitor converter.

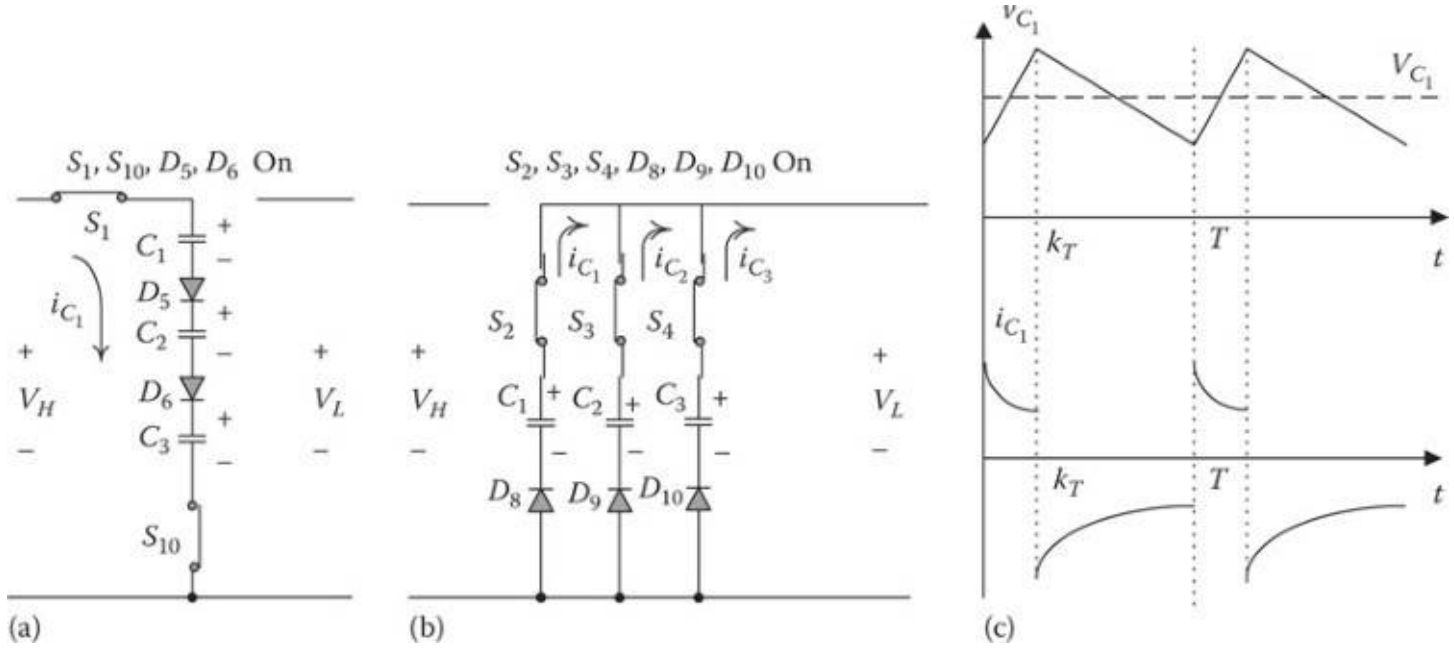


FIGURE 11.2
Mode A operation. (a) Switch-on. (b) Switch-off. (c) Some voltage and current waveforms.

11.2.1.1 Mode A

For Mode A, state-*on* state is shown in Figure 11.2a: switches S_1 and S_{10} are closed and diodes D_5 and D_6 are conducted. Other switches and diodes are open. In this case, capacitors C_1, C_2, and C_3 are charged via the circuit V_H–S_1–C_1–D_5–C_2–D_6–C_3–S_{10}, and the voltage across capacitors C_1, C_2, and C_3 is increasing. The equivalent circuit resistance is $R_{AN} = (2r_S + 3r_C) = 0.12\ \Omega$, and the voltage deduction is $2V_D = 1$ V. State-*off* state is shown in Figure 11.2b:

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switches S_2, S_3, and S_4 are closed and diodes D_8, D_9, and D_{10} are conducted. Other switches and diodes are open. In this case, capacitor C_1 (C_2 and C_3) is discharged via the circuit S_2(S_3 and S_4)−V_L−D_8(D_9 and D_{10})−C_1(C_2 and C_3), and the voltage across capacitor C_1 (C_2 and C_3) is decreasing. The equivalent circuit resistance is $R_{AF} = r_S + r_C = 0.05\Omega$, and the voltage deduction is $V_D = 0.5$ V. Capacitors C_1, C_2, and C_3 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 11.2c.

Mode A uses the *current-amplification technique*. All three capacitors are charged in series during state-on. The input current flows through the three capacitors and the charges accumulated on the three capacitors should be the same. These three capacitors are discharged in parallel during state-off. Therefore, the output current is amplified by three.

11.2.1.2 Mode B

For Mode B, state-*on* is shown in Figure 11.3a: switches S_8, S_9, and S_{10} are closed and diodes D_2, D_3, and D_4 are conducted. Other switches and diodes are off. In this case, all three capacitors are charged via each circuit V_L−D_2(and D_3, D_4)−C_1(and C_2, C_3)−S_8(and S_9, S_{10}), and the voltage across the three capacitors is increasing. The equivalent circuit resistance is $R_{BN} = r_S + r_C$ and the voltage deduction is V_D. State-*off* is shown in Figure 11.3b: switches S_5, S_6, and S_7 are closed and diode D_1 is on. Other switches and diodes are open. In this case, all capacitors are discharged via the circuit V_L−S_7−C_3−S_6−C_2−S_5−C_1−D_1−V_H, and the voltage across all capacitors is decreasing. The equivalent circuit resistance is $R_{BF} = 3\ (r_S + r_C)$ and the voltage deduction is V_D. The voltage waveform across capacitor C_1 is shown in Figure 11.3c.

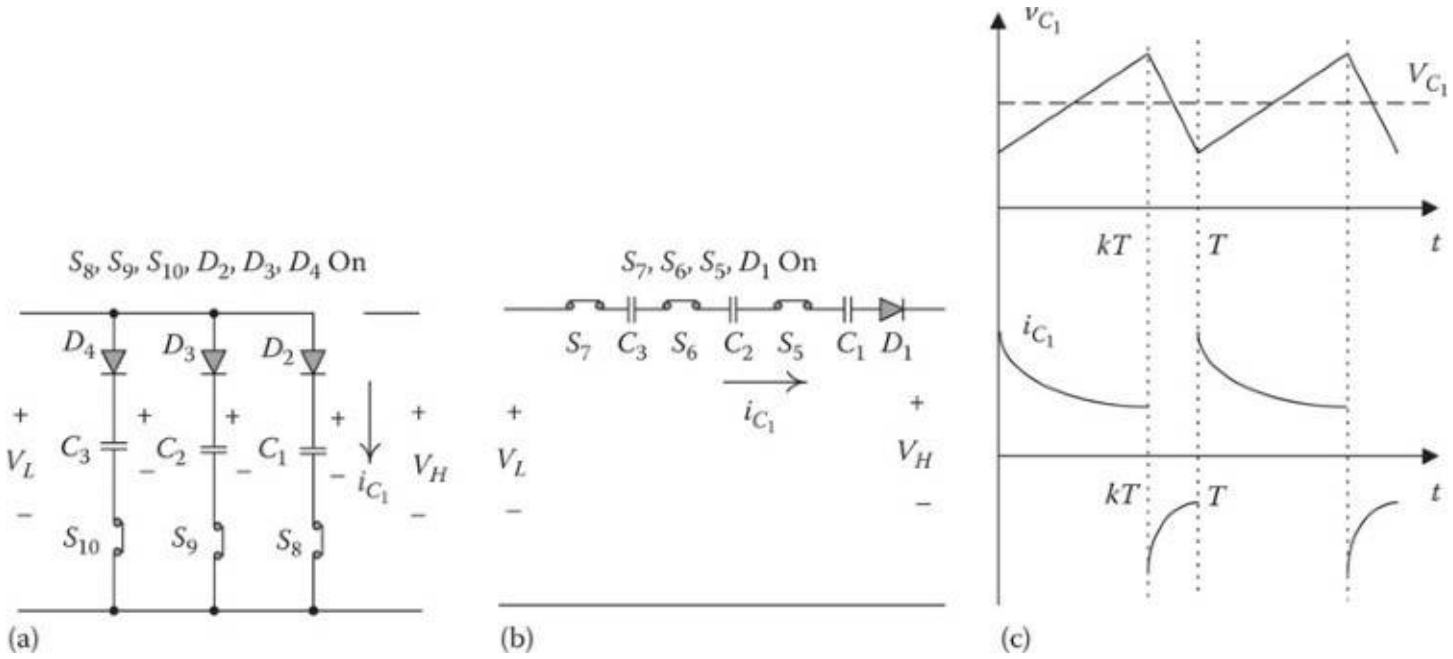


FIGURE 11.3
Mode B operation. (a) Switch-on. (b) Switch-off. (c) Some voltage and current waveforms.

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TABLE 11.1
Switch's Status (the Blank Status Means *Off*)

	Mode A		Mode B	
Switches and Diodes	**State-On**	**State-Off**	**State-On**	**State-Off**
S_1	On			
D_1				On
S_2, S_3, S_4		On		
D_2, D_3, D_4			On	
S_5, S_6, S_7				On
D_5, D_6	On			
S_8, S_9			On	
S_{10}	On		On	
D_8, D_9, D_{10}		On		

Mode B implements the *voltage-lift technique.* All three capacitors are charged in parallel during state-on. The input voltage is applied to the three capacitors symmetrically, so that the voltages across these three capacitors should be the same. They are discharged in series during state-off. Therefore, the output voltage is lifted by three.

Summary: In this circuit, we have $R_{AN} = 0.12\ \Omega$, $R_{AF} = 0.05\ \Omega$., $R_{BN} = 0.05\ \Omega$, and $R_{BF} = 0.15\ \Omega$.

The switch status is shown in Table 11.1.

11.2.2 Mode A (Quadrant I Operation)

Refer to Figure 11.2a and b; the voltage across capacitor C_1 increases during switch-on and decreases during switch-off according to the integration of the current i_{C_1}. If the switching period T is small enough (comparing with the circuit time constant), we can use average current to replace its instantaneous value for the integration. Therefore, the voltage across capacitor C_1 is

$$v_{C_1}(t) = \begin{cases} v_{C_1}(0) + \dfrac{1}{C}\displaystyle\int_0^t i_{C_1}(t)dt \approx v_{C_1}(0) + \dfrac{t}{C}\overline{i_H} & 0 \le t < kT \\ v_{C_1}(kT) + \dfrac{1}{C}\displaystyle\int_{kT}^t i_{C_1}(t)dt \approx v_{C_1}(kT) - \dfrac{t-kT}{C}\overline{i_L} & kT \le t < T \end{cases} \tag{11.1}$$

The current flowing through the three capacitors is an exponential function. If the switching period T is small enough (comparing with the circuit time constant), we can use their initial values while ignoring their variations. Therefore, the current flowing through capacitor C_1 is

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$$\Delta v_{C_1} = \frac{1}{C}\int_{kT}^{T} i_{C_1}(t)dt = \frac{(1-k)T}{C}\overline{i_L} = \frac{(1-k)(V_{C_1} - V_L - V_D)}{fCR_{AF}} \quad kT \le t < (1-k)T$$

Therefore,

$$\overline{i_H} = 3\frac{1-k}{k}\overline{i_L} \tag{11.3}$$

where

$\overline{i_H}$ is the average input current in the switch-on period kT, which is equal to I_H/k

$\overline{i_L}$ is the average output current in the switch-off period $(1 - k)T$, which is equal to $I_L/3(1 - k)$

Therefore, we have $3I_H = I_L$.

The variation of the voltage across capacitor C_1 is

$$\Delta v_{C_1} = \frac{1}{C}\int_{0}^{kT} i_{C_1}(t)dt = \frac{kT}{C}\overline{i_H} = \frac{k(V_H - 3V_{C_1} - 2V_D)}{fCR_{AN}} \quad 0 \le t < kT$$

or

$$\Delta v_{C_1} = \frac{1}{C}\int_{kT}^{T} i_{C_1}(t)dt = \frac{(1-k)T}{C}\overline{i_L} = \frac{(1-k)(V_{C_1} - V_L - V_D)}{fCR_{AF}} \quad kT \le t < (1-k)T$$

After calculation,

$$V_{C_1} = \frac{k(V_H - 2V_D) + 2.4(1-k)(V_L + V_D)}{2.4 + 0.6k} \tag{11.4}$$

Hence,

$$\Delta v_{C_1} = \frac{k(V_H - 3V_{C_1} - 2V_D)}{fCR_{AN}} = \frac{2.4k(1-k)(V_H - 3V_L - 5V_D)}{(2.4 + 0.6k)fCR_{AN}} \tag{11.5}$$

We have

$$v_{C_1}(0) = V_{C_1} - \frac{\Delta v_{C_1}}{2} \quad \text{and} \quad v_{C_1}(kT) = V_{C_1} + \frac{\Delta v_{C_1}}{2}$$

The average output current is

$$I_L = \frac{3}{T}\int_{kT}^{T} i_{C_1}(t)dt \approx 3(1-k)\frac{V_{C_1} - V_L - V_D}{R_{AF}} \tag{11.6}$$

The average input current is

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$$I_H = \frac{1}{T}\int_0^{kT} i_{C_1}(t)dt \approx k\frac{V_H - 3V_{C_1} - 2V_D}{R_{AN}} \tag{11.7}$$

The output power is

$$P_o = V_L I_L = 3(1-k)V_L \frac{V_{C_1} - V_L - V_D}{R_{AF}} \tag{11.8}$$

The input power is

$$P_i = V_H I_H = kV_H \frac{V_H - 3V_{C_1} - V_D}{R_{AN}} \tag{11.9}$$

The transfer efficiency is

$$\eta_A = \frac{P_o}{P_i} = \frac{1-k}{k}\frac{3V_L}{V_H}\frac{V_{C_1} - V_L - V_D}{V_H - 3V_{C_1} - V_D}\frac{R_{AN}}{R_{AF}} = \frac{3V_L}{V_H} \tag{11.10}$$

If f = 5 kHz, V_H = 48 V and V_L = 14 V, and all C = 5000 μF, for the various k values, the data are shown in Table 11.2.

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. The conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds to k = 0.5.

TABLE 11.2
Calculation Results for Mode A

k	V_{C_1} (V)	Δv_{C_1} (V)	I_H (A)	I_L (A)	P_i (W)	P_o (W)	η_A
0.4	15.03	0.255	6.36	19.08	305.3	267.1	0.875
0.5	15.15	0.259	6.48	19.44	311.0	272.2	0.875
0.6	15.26	0.243	6.08	18.24	291.8	255.4	0.875

11.2.3 Mode B (Quadrant II Operation)

Refer to Figure 11.3a and b; the voltage across capacitor C_1 increases during switch-on and decreases during switch-off according to the integration of the current i_{C_1}. If the switching period T is small enough, we can use average current to replace its instantaneous value for the integration. Therefore, the voltage across capacitor C_1 is

$$v_{C_1}(t) = \begin{cases} v_{C_1}(0) + \dfrac{1}{C}\displaystyle\int_0^t i_{C_1}(t)dt \approx v_{C_1}(0) + \frac{t}{C}\overline{i_L} & 0 \le t < kT \\ v_{C_1}(kT) + \dfrac{1}{C}\displaystyle\int_{kT}^t i_{C_1}(t)dt \approx v_{C_1}(kT) - \frac{t-kT}{C}\overline{i_H} & kT \le t < T \end{cases} \tag{11.11}$$

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The current flowing through the three capacitors is an exponential function. If the switching period T is small enough, we can use their initial values and ignore their variations. Therefore, the current flowing through capacitor C_1 is

$$i_{C_1}(t)=\begin{cases}\dfrac{V_L-v_{C_1}(0)-V_D}{R_{BN}}(1-e^{-t/R_{BN}C})\approx\dfrac{V_L-V_{C_1}-V_D}{R_{BN}}=\overline{i_L} & 0\le t<kT\\ -\dfrac{3v_{C_1}(kT)+V_L-V_H-V_D}{R_{BF}}e^{-t/R_{BF}C}\approx-\dfrac{3V_{C_1}+V_L-V_H-V_D}{R_{BF}}=-\overline{i_H} & kT\le t<T\end{cases} \tag{11.12}$$

Therefore,

$$\overline{i_L}=\frac{1-k}{k}\overline{i_H} \tag{11.13}$$

where

$\overline{i_L}$ is the average input current in the switch-on period kT, which is equal to I_L/k

$\overline{i_H}$ is the average output current in the switch-off period $(1-k)T$, which is equal to $I_H/3(1-k)$

Therefore, we have $4I_H = I_L$.

The variation of the voltage across capacitor C is

$$\Delta v_{C_1}=\frac{1}{C}\int_0^{kT}i_{C_1}(t)dt=\frac{kT}{C}\overline{i_L}=\frac{k(V_L-V_{C_1}-V_D)}{fCR_{BN}}\quad 0\le t<kT$$

or

$$\Delta v_{C_1}=\frac{1}{C}\int_{kT}^{T}i_{C_1}(t)dt=\frac{(1-k)T}{C}\overline{i_H}=\frac{(1-k)(3V_C+V_L-V_H-V_D)}{fCR_{BF}}\quad kT\le t<(1-k)T$$

After calculation,

$$V_{C_1}=k(V_L-V_D)+\frac{1-k}{3}(V_H-V_L+V_D) \tag{11.14}$$

Hence,

$$\Delta v_{C_1}=\frac{k(1-k)[4(V_L-V_D)-V_H]}{fCR_{BN}} \tag{11.15}$$

$$v_{C_1}(0)=V_{C_1}-\frac{\Delta v_{C_1}}{2}\quad\text{and}\quad v_{C_1}(kT)=V_{C_1}+\frac{\Delta v_{C_1}}{2}$$

The average input current is

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$$I_L = \frac{1}{T}\left[3\int_0^{kT} i_{C_1}(t)dt + \int_{kT}^{T} i_{C_1}(t)dt\right] \approx 3k\frac{V_L - V_{C_1} - V_D}{R_{BN}} + (1-k)\frac{3V_{C_1} + V_L - V_H - V_D}{R_{BF}} \tag{11.16}$$

The average output current is

$$I_H = \frac{1}{T}\int_{kT}^{T} i_{C_1}(t)dt \approx (1-k)\frac{3V_{C_1} + V_L - V_H - V_D}{R_{BF}} \tag{11.17}$$

The input power is

$$P_i = V_L I_L = V_L\left[3k\frac{V_L - V_C - V_D}{R_{BN}} + (1-k)\frac{3V_C + V_L - V_H - V_D}{R_{BF}}\right] \tag{11.18}$$

The output power is

$$P_o = V_H I_H = V_H(1-k)\frac{3V_C + V_L - V_H - V_D}{R_{BF}} \tag{11.19}$$

The transfer efficiency is

$$\eta_B = \frac{P_o}{P_i} = \frac{V_H}{4V_L} \tag{11.20}$$

If f = 5 kHz, V_H = 48 V and V_L = 14 V, and all C = 5000 μF, for the various k values, the data are shown in Table 11.3.

From this analysis, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. The conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds to k = 0.5.

TABLE 11.3
Calculation Results for Mode B

k	V_{C_1} (V)	Δv_{C_1} (V)	I_H (A)	I_L (A)	P_i (W)	P_o (W)	η_B
0.4	12.3	1.152	9.6	38.4	537.6	460.8	0.857
0.5	12.5	1.2	10	40	560	480	0.857
0.6	12.7	1.152	9.6	38.4	537.6	460.8	0.857

TABLE 11.4
Experimental Results

Mode	I_L (A)	I_H (A)	V_{C_1} (V)	P_i (W)	P_o (W)	η (%)	$\bar{P}$ (W)	Volume (in.^{3})	PD (W/in.^{3})
A	18.9	6.4	15.15	307	264	86	286	24	11.9
B	40	9.8	12.5	560	470	84	515	24	21.5
Average	29.45	8.1	13.8	434	367	85	400	24	16.7

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11.2.4 Experimental Results

A two-quadrant DC/DC converter operates the conversion between 14 V and 48 VDC. The converter has been developed and is introduced in this chapter. This converter is a two-quadrant DC/DC converter with SCs for the dual-direction conversion between 14 V and 48 VDC. A testing rig was constructed and consists of a modern car battery 14 VDC as a load and a 48 VDC source power supply. The testing conditions are

Switching frequency: f = 5 kHz
Conduction duty: k = 0.5
HV and LV: V_H = 48 V and V_L = 14 V
All capacitance: C = 5000 μF

The experimental results are shown in Table 11.4. The average power transfer efficiency is 85%. The total average PD is 16.7 W/in.^{3}. This figure is much higher than the PD of classical converters that are usually less than 5 W/in.^{3}. Since the switching frequency is low, the EMI is weak.

11.2.5 Discussion

11.2.5.1 Efficiency

From theoretical analysis and experimental results, we find that the power transfer efficiency of SC converters is limited. The reason to spoil the power transfer efficiency is the power consumption on the circuit parasitic resistance and the diodes.

In steady state, the increase and decrease of the charge across a capacitor should be equal to each other. Therefore, its average input current I_i must be equal to the average output current I_o. If only one capacitor is applied in an SC DC/DC converter, its power transfer efficiency is

$$\eta = \frac{P_o}{P_i} = \frac{V_o I_o}{V_i I_i} = \frac{V_o}{V_i} \tag{11.21}$$

Since the voltage-lift and current-amplification techniques are applied, in the circuit the power transfer efficiency is around 86.6%, which is much higher than those of the circuits introduced by the literature.

11.2.5.2 Conduction Duty k

From the data calculated in the previous sections, it can be seen that if k = 0.4, 0.5, or 0.6, the efficiencies η_A and η_B are not changed. The output power is slightly affected by k, and its maximum value corresponds to k = 0.5. Therefore, we can take the typical data corresponding to k = 0.5.

11.2.5.3 Switching Frequency f

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Because the switching frequency f = 5 kHz is very low, its EMI is much lower than that of the traditional classical converters. The switching frequency applied in the traditional classical converters normally arranges between 50 and 200 kHz.

11.3 Four-Quadrant Switched-Capacitor DC/DC Luo-Converter

Since most SC DC/DC converters published in the literature perform in single-quadrant operation working in the push-pull status, their control circuit and topologies are very complex. This section introduces an SC four-quadrant DC/DC Luo-converter. The experimental results verified our analysis and calculation. This converter shown in Figure 11.4 consists of eight switches and two capacitors. The source voltage V_1 and load voltage V_2 (e.g., a battery or DC motor back EMF) are usually constant voltages. In this circuit, they are assumed to be 21 and 14 V. Capacitors C_1 and C_2 are the same, $C_1 = C_2$ = 2000 μF. The circuit equivalent resistance R = 50 mΩ. Therefore, there are four modes of operation for this converter:

- *Mode A* (*quadrant I, Q_I):* Energy is transferred from source to positive voltage load.
- *Mode B* (*quadrant II, Q_{II}*): Energy is transferred from positive voltage load to source.
- *Mode C* (*quadrant III, Q_{III}*): Energy is transferred from source to negative voltage load.
- *Mode D* (*quadrant IV, Q_{IV}*): Energy is transferred from negative voltage load to source.

The first quadrant is called the forward motoring (Forw. Mot.) operation. V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. V_1 and I_2 are positive, and I_1 and V_2 are negative.

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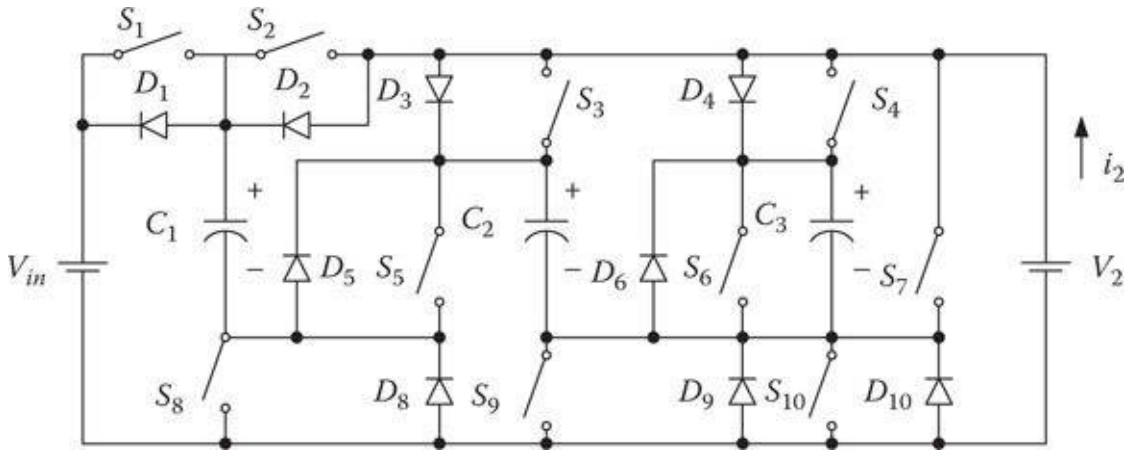


FIGURE 11.4
Four-quadrant switched-capacitor DC/DC Luo-converters.

Each mode has two conditions: $V_1 > V_2$ and $V_1 < V_2$. Each condition has two states: *on* and *off*. Usually, each state operates in a different conduction duty *k*. The switching period is *T* where $T = 1/f$ The switch status is shown in Table 11.5.

For Mode A1, condition $V_1 < V_2$ is shown in Figure 11.5. Since $V_1 < V_2$, two capacitors C_1 and C_2 can be used in parallel. During switch-on state shown in Figure 11.5a, switches S_1, S_4, S_6, and S_8 are closed and other switches are open. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-off state shown in Figure 11.5b, switches S_2, S_4, S_6, and S_8 are closed and other switches are open. In this case, capacitors $C_1//C_2$ are discharged via the circuit $S_2-V_2-S_4-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 11.5c.

For Mode A2, condition $V_1 < V_2$ is shown in Figure 11.6. Since $V_1 < V_2$, two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off. This is the so-called voltage-lift technique. During switch-on state shown in Figure 11.6a, switches S_1, S_4, S_6, and S_8 are closed and other switches are open. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state shown in Figure 11.6b, switches S_2, S_4, and S_7 are closed and other switches are open. In this case, capacitors C_1 and C_2 are discharged via the circuit $S_2-V_2-S_4-C_1-S_7-C_2$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 11.6c.

TABLE 11.5
Switch's Status (No Mentioned Switches Are Off)

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Q No.	Condition	On	Off	Source	Load
Quadrant I, Mode A	$V_1 > V_2$	$S_{1,4,6,8}$	$S_{2,4,6,8}$	V_1+	V_2+
Forw. Mot.	$V_1 < V_2$	$S_{1,4,6,8}$	$S_{2,4,7}$	I_1+	I_2+
Quadrant II, Mode B	$V_1 > V_2$	$S_{2,4,6,8}$	$S_{1,4,7}$	V_1+	V_2+
Forw. Reg.	$V_1 < V_2$	$S_{2,4,6,8}$	$S_{1,4,6,8}$	I_1-	I_2-
Quadrant III, Mode C	$V_1 > \lvert V_2 \rvert$	$S_{1,4,6,8}$	$S_{3,5,6,8}$	V_1+	V_2-
Rev. Mot	$V_1 < \lvert V_2 \rvert$	$S_{1,4,6,8}$	$S_{3,5,7}$	I_1+	I_2-
Quadrant IV, Mode D	$V_1 > \lvert V_2 \rvert$	$S_{3,5,6,8}$	$S_{1,4,7}$	V_1+	V_2-
Rev. Reg.	$V_1 < \lvert V_2 \rvert$	$S_{3,5,6,8}$	$S_{1,4,6,8}$	I_1-	I_2+

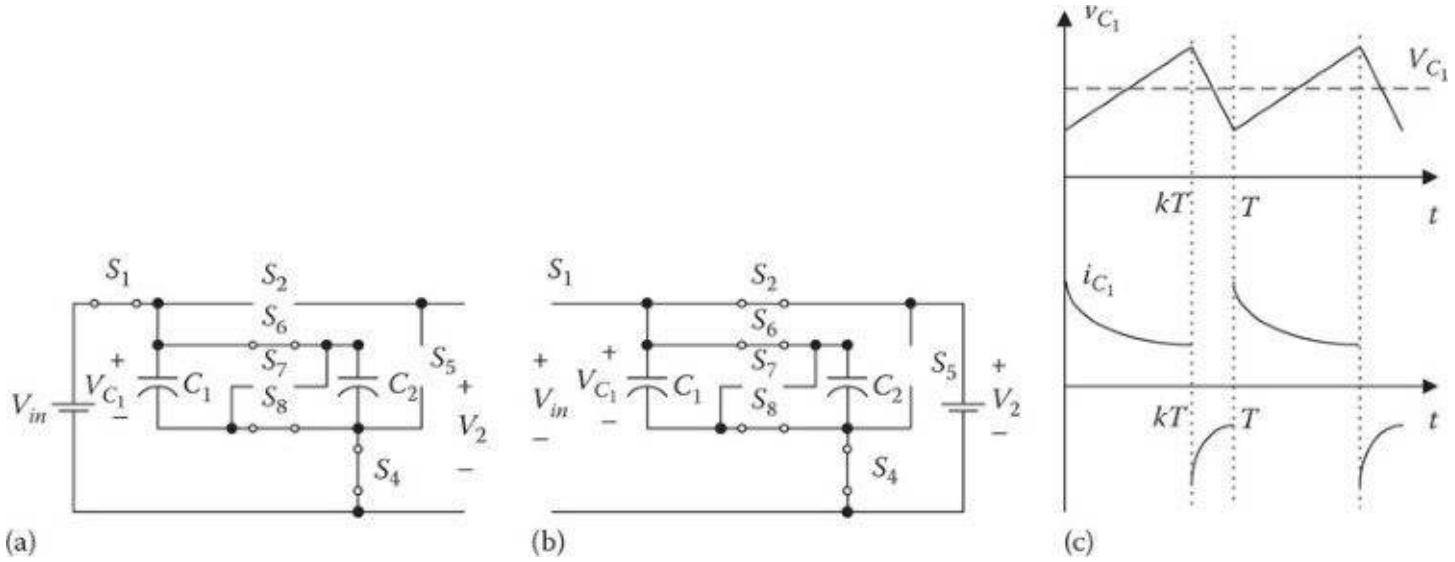


FIGURE 11.5
Mode A1 (quadrant I) forward motoring operation with $V_1 > V_2$. (a) Switch-on: S_1, S_4, S_6, and S_8. (b) Switch-off: S_2, S_4, S_6, and S_8 on. (c) Some waveforms.

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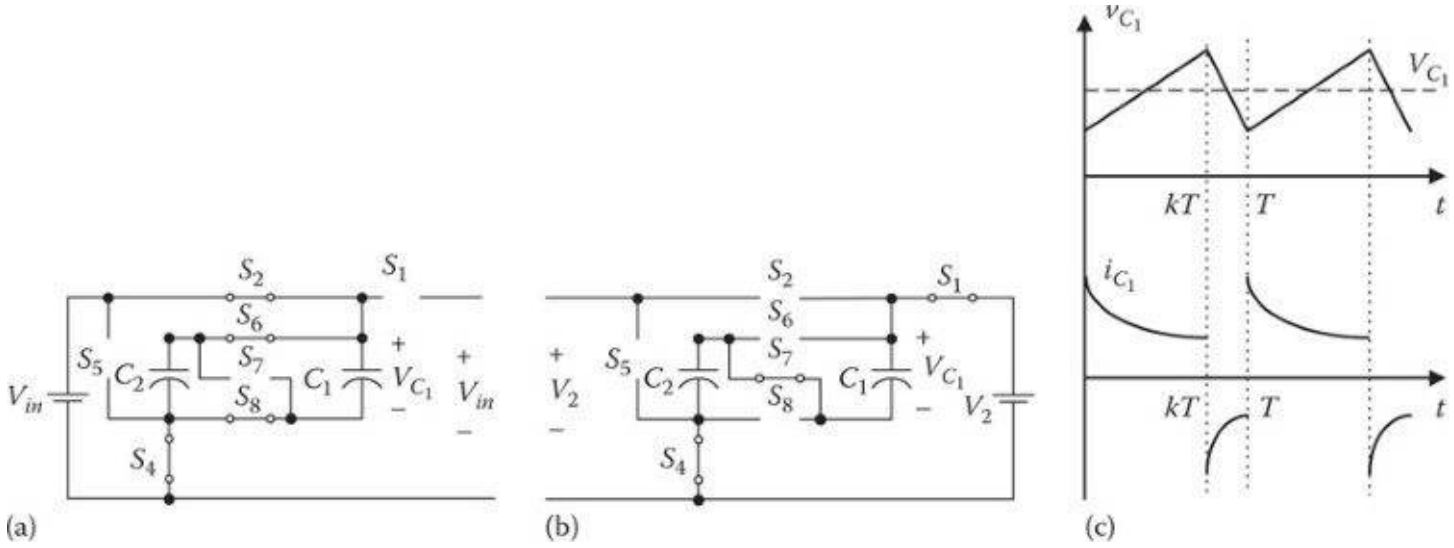


FIGURE 11.6
Mode A2 (quadrant I) forward motoring operation with $V_1 < V_2$. (a) Switch-on: S_2, S_4, S_6, and S_8 on. (b) Switch-off: S_1, S_4 (S_5), and S_7 on. (c) Some waveforms.

For Mode B1, condition $V_1 > V_2$ is shown in Figure 11.7. Since $V_1 > V_2$, two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off. The voltage-lift technique is applied. During switch-*on* state, switches S_2, S_4, S_6, and S_8 are closed. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_2-S_2-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_1, S_4, and S_7 are closed. In this case, capacitors C_1 and C_2 are discharged via the circuit $S_1-V_1-S_4-C_2-S_7-C_1$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 11.7c.

For Mode B2, condition $V_1 > V_2$ is shown in Figure 11.8. Since $V_1 > V_2$, two capacitors C_1 and C_2 can be used in parallel. During switch-on state, switches S_2, S_4, S_6, and S_8 are closed.

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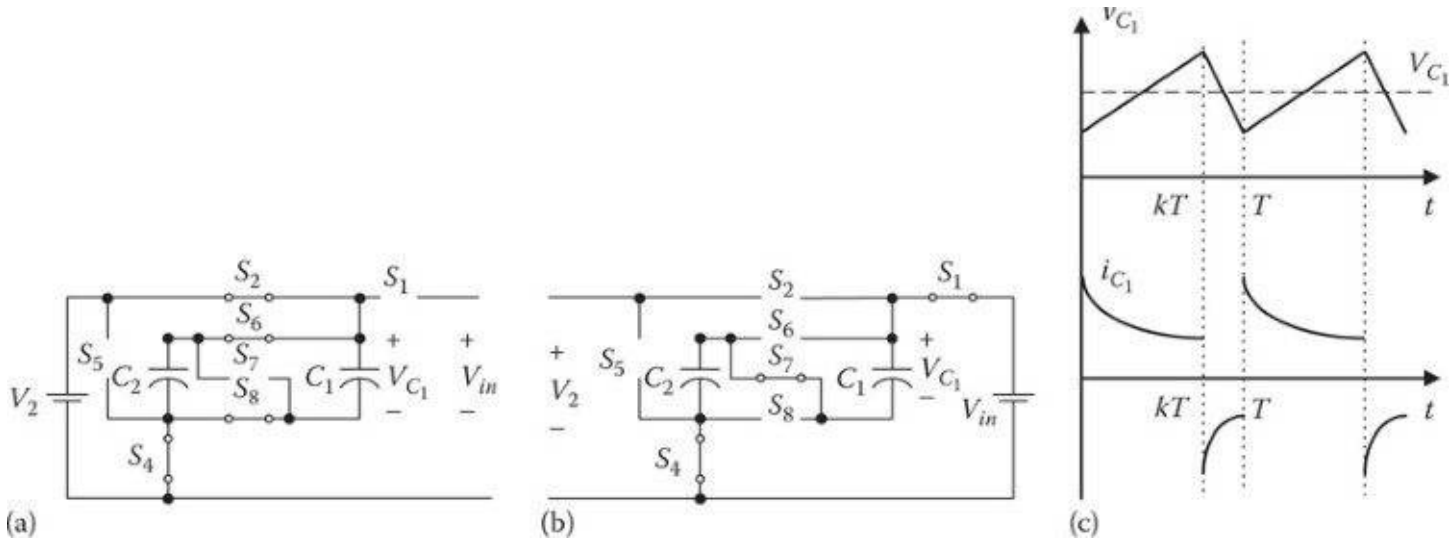


FIGURE 11.7
Mode B1 (quadrant II) forward motoring operation with $V_1 > V_2$. (a) Switch-on: S_2, S_4, S_6, and S_8 on. (b) Switch-off: S_1, S_4 (S_5), and S_7 on. (c) Some waveforms.

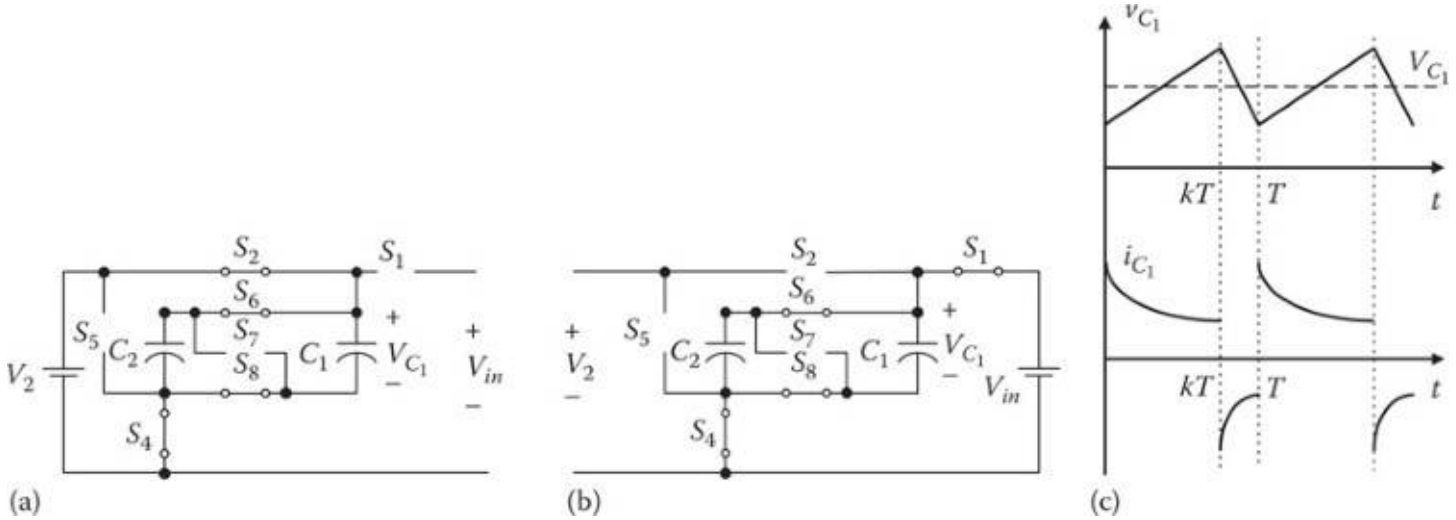


FIGURE 11.8
Mode B2 (quadrant II) forward motoring operation with $V_1 < V_2$. (a) Switch-on: S_2, S_4, S_6, and S_8 on. (b) Switch-off: S_2, S_4, S_6, and S_8 on. (c) Some waveforms.

In this case, capacitors $C_1//C_2$ are charged via the circuit $V_2-S_2-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_1, S_4, S_6, and S_8 are closed. In this case, capacitors $C_1//C_2$ are discharged via the circuit $S_1-V_1-S_4-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 11.8c.

For Mode C1, condition $V_1 > |V_2|$ is shown in Figure 11.9. Since $V_1 > |V_2|$, two capacitors C_1 and C_2 can be used in parallel. During switch-*on* state, switches S_1, S_4, S_6, and S_8 are

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closed. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_3, S_5, S_6, and S_8 are closed. Capacitors C_1 and C_2 are discharged via the circuit $S_3-V_2-S_5-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 11.9c.

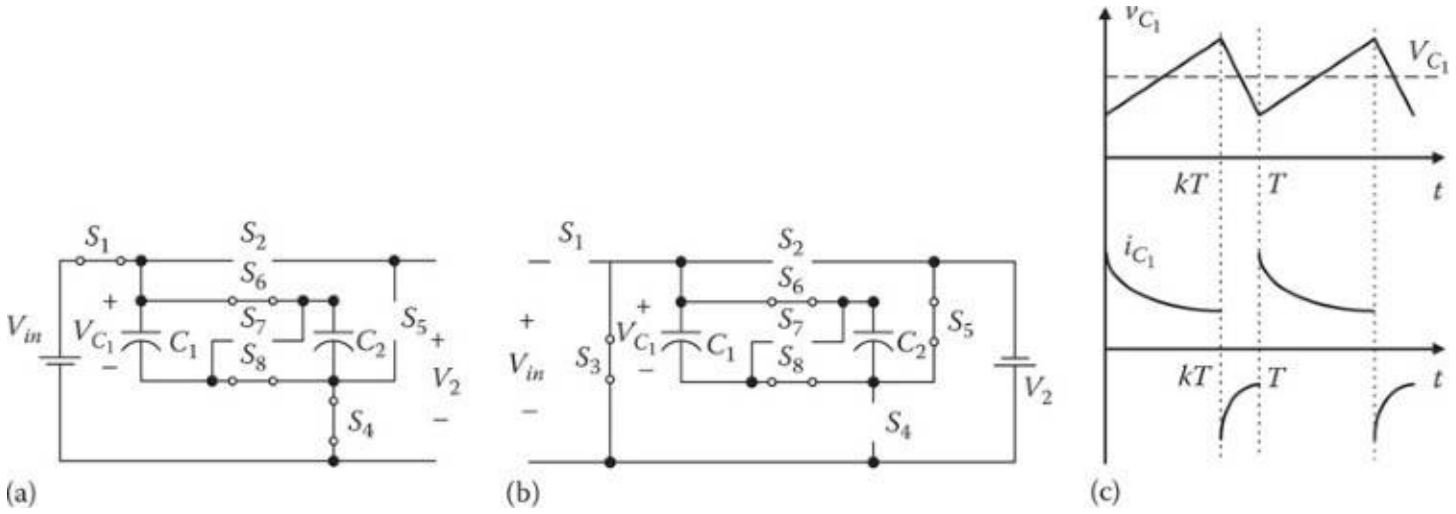


FIGURE 11.9
Mode C1 (quadrant III) forward motoring operation with $V_1 > V_2$. (a) Switch-on: S_1, S_4, S_6, and S_8 on. (b) Switch-off: S_3, S_5, S_6, and S_8 on. (c) Some waveforms.

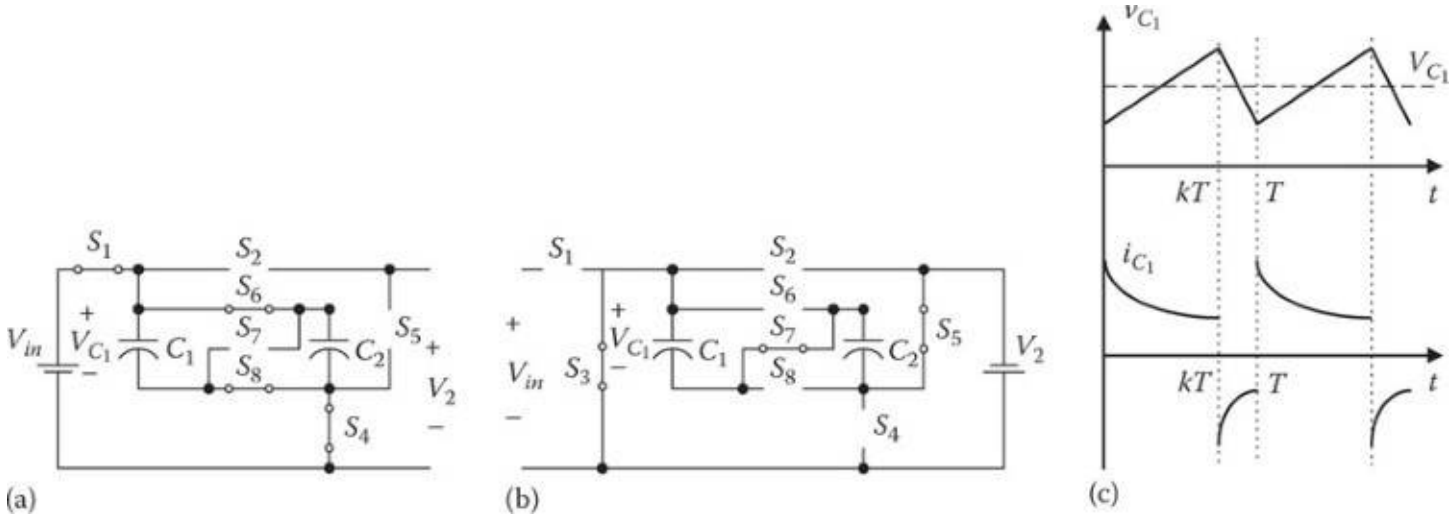


FIGURE 11.10
Mode C2 (quadrant III) forward motoring operation with $V_1 < V_2$. (a) Switch-on: S_1, S_4, S_6, and S_8 on. (b) Switch-off: S_3, S_5, and S_7 on. (c) Some waveforms.

For Mode C2, condition $V_1 < |V_2|$ is shown in Figure 11.10. Since $V_1 < |V_2|$, two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off, applying the

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voltage-lift technique. During switch-on state, switches S_1, S_4, S_6, and S_8 are closed. Capacitors C_1 and C_2 are charged via the circuit $V_1 - S_1 - C_1//C_2 - S_4$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_3, S_5, and S_7 are closed. Capacitors C_1 and C_2 are discharged via the circuit $S_3 - V_2 - S_5 - C_1 - S_7 - C_2$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the source to the load. The voltage waveform across capacitor C_1 is shown in Figure 11.10c.

For Mode D1, condition $V_1 > |V_2|$ is shown in Figure 11.11. Since $V_1 > |V_2|$, two capacitors C_1 and C_2 are in parallel during switch-on and in series during switch-off, applying the voltage-lift technique. During switch-*on* state, switches S_3, S_5, S_6, and S_8 are closed. In this case capacitors $C_1//C_2$ are charged via the circuit $V_2 - S_3 - C_1//C_2 - S_5$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_1, S_4, and $S_7$are closed. Capacitors C_1 and C_2 are discharged via the circuit $S_1 - V_1 - S_4 - C_2 - S_7 - C_1$, and the voltage across capacitor C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 11.11c.

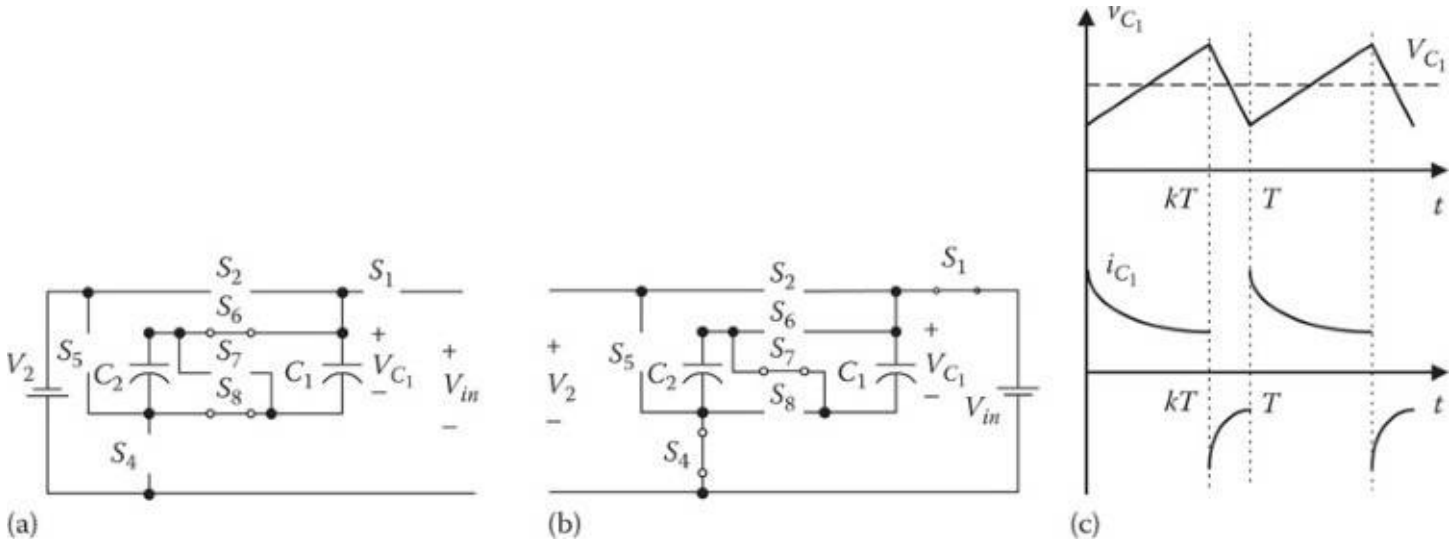


FIGURE 11.11
Mode D1 (quadrant IV) forward motoring operation with $V_1 > V_2$. (a) Switch-on: S_3, S_5, S_6, and S_8 on. (b) Switch-off: S1, S4, and S7 on. (c) Some waveforms.

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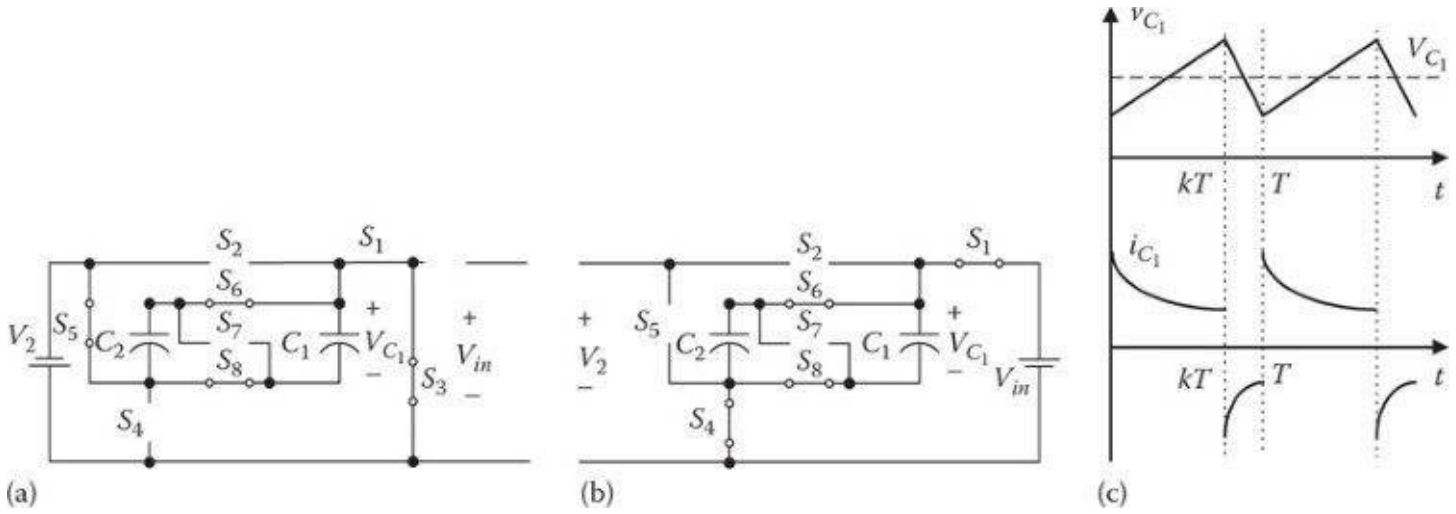


FIGURE 11.12
Mode D2 (quadrant IV) forward motoring operation with $V_1 < V_2$. (a) Switch-on: S_3, S_5, S_6, and S_8 on. (b) Switch-off: S1, S4, S6, and S8 on. (c) Some waveforms.

For Mode D2, condition $V_1 < |V_2|$ is shown in Figure 11.12. Since $V_1 < |V_2|$, two capacitors C_1 and C_2 can be used in parallel. During switch-*on* state, switches S_3, S_5, S_6, and S_8 are closed. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_2-S_3-C_1//C_2-S_5$, and the voltage across capacitors C_1 and C_2 is increasing. During switch-*off* state, switches S_1, S_4, S_6, and S_8 are closed. Capacitors C_1 and C_2 is discharged via the circuit $S_1-V_1-S_4-C_1//C_2$, and the voltage across capacitors C_1 and C_2 is decreasing. Capacitors C_1 and C_2 transfer the energy from the load to the source. The voltage waveform across capacitor C_1 is shown in Figure 11.12c.

11.3.1 Mode A (QI: Forward Motoring)

11.3.1.1 Mode A1: Condition $V_1 > V_2$

For mode A1, condition $V_1 > V_2$ is shown in Figure 11.5. Because two capacitors are connected in parallel, the total capacitance $C = C_1 + C_2 = 4000\ \mu$F. Suppose that the equivalent circuit resistance $R = 50\ m\Omega$. $V_1 = 21$ V and $V_2 = 14$ V and the switching frequency $f = 5$ kHz. The voltage and current across the capacitors are

$$v_C(t) = \begin{cases} v_C(0) + \dfrac{1}{C}\displaystyle\int_0^t i_C(t)dt \approx v_C(0) + \frac{t}{C}\bar{i}_1 & 0 \le t < kT \\ v_C(kT) + \dfrac{1}{C}\displaystyle\int_{kT}^t i_C(t)dt \approx v_C(kT) - \frac{t-kT}{C}\bar{i}_2 & kT \le t < T \end{cases} \tag{11.22}$$

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$$i_C(t)=\begin{cases}\dfrac{V_1-v_C(0)}{R}(1-e^{-t/RC})\approx\dfrac{V_1-V_C}{R}=\bar{i}_1 & 0\le t<kT\\ -\dfrac{v_C(kT)-V_2}{R}e^{-t/RC}\approx-\dfrac{V_C-V_2}{R}=-\bar{i}_2 & kT\le t<T\end{cases} \tag{11.23}$$

Therefore,

$$\bar{i}_1=\frac{1-k}{k}\bar{i}_2 \tag{11.24}$$

where

$\bar{i}_1$ is the average input current in the switch-on period kT, which is equal to I_1/k

$\bar{i}_2$ is the average output current in the switch-off period $(1-k)T$, which is equal to $I_2/(1-k)$

Therefore, we have $I_1 = I_2$. The variation of the voltage across capacitor C is

$$\Delta v_C=\frac{1}{C}\int_0^{kT}i_C(t)dt=\frac{kT}{C}\bar{i}_1=\frac{k(V_1-V_C)}{fCR}\quad 0\le t<kT$$

or

$$\Delta v_C=\frac{1}{C}\int_{kT}^{T}i_C(t)dt=\frac{(1-k)T}{C}\bar{i}_2=\frac{(1-k)(V_C-V_2)}{fCR}\quad kT\le t<T$$

After calculation,

$$V_C=kV_1+(1-k)V_2 \tag{11.25}$$

Hence,

$$\Delta v_C=\frac{k(1-k)(V_1-V_2)}{fCR} \tag{11.26}$$

We then have

$$v_C(0)=V_C-\frac{\Delta v_C}{2}$$

and

$$v_C(kT)=V_C+\frac{\Delta v_C}{2}$$

The average output current is

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$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_2}{R} \tag{11.27}$$

$$I_1 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R} \tag{11.28}$$

TABLE 11.6
Calculation Results for Mode A1 ($V_1 > V_2$)

k	V_C (V)	Δv_C (V)	I_1 (A)	I_2 (A)	η_{A1}
0.4	16.8	1.68	33.6	33.6	0.67
0.5	17.5	1.75	35	35	0.67
0.6	18.2	1.68	33.6	33.6	0.67

The output power is

$$P_o = V_2 I_2 = (1-k)V_2\frac{V_C - V_2}{R} \tag{11.29}$$

The input power is

$$P_i = V_1 I_1 = kV_1\frac{V_1 - V_C}{R} \tag{11.30}$$

The transfer efficiency is

$$\eta_{A1} = \frac{P_o}{P_i} = \frac{1-k}{k}\frac{V_2}{V_1}\frac{V_C - V_2}{V_1 - V_C} = \frac{V_2}{V_1} \tag{11.31}$$

From this equation, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. If f = 5 kHz, V_1 = 21 V and V_2 = 14 V, and total C = 4000 μF, R = 50 mΩ. For three k values, the data are found in Table 11.6.

From the analysis and calculation, it can be seen that the conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds to k = 0.5.

11.3.1.2 Mode A2: Condition $V_1 < V_2$

For mode A2, condition $V_1 < V_2$ is shown in Figure 11.6. Because two capacitors are connected in parallel during switch-on, the total capacitance $C = 2 \times C_1 = 4000$ μF. The input current i_1 is two times capacitor current i_{C_1}. Two capacitors are connected in series during switch-off; the total capacitance $C' = C_1/2 = 1000$ μF. The output current i_2 is equal to capacitor current i_{C_1}. Suppose that the equivalent circuit resistance R = 50 mΩ. V_1 = 14 V and V_2 = 21 V, and the switching frequency is f = 5 kHz. The voltage and current across each

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capacitor are

$$v_{C_1}(t)=\begin{cases} v_{C_1}(0)+\dfrac{1}{C_1}\displaystyle\int_0^t i_{C_1}(t)dt \approx v_{C_1}(0)+\dfrac{t}{2C_1}\bar{i}_1 & 0\le t<kT \\ v_{C_1}(kT)+\dfrac{1}{C_1}\displaystyle\int_{kT}^t i_{C_1}(t)dt \approx v_{C_1}(kT)-\dfrac{t-kT}{C_1}\bar{i}_2 & kT\le t<T \end{cases} \tag{11.32}$$

$$i_{C_1}(t)=\begin{cases} \dfrac{V_1-v_{C_1}(0)}{R}(1-e^{-t/RC}) \approx \dfrac{V_1-V_{C_1}}{R}=\dfrac{\bar{i}_1}{2} & 0\le t<kT \\ -\dfrac{2v_{C_1}(kT)-V_2}{R}e^{-t/RC} \approx -\dfrac{2V_{C_1}-V_2}{R}=-\bar{i}_2 & kT\le t<T \end{cases} \tag{11.33}$$

Therefore,

$$\bar{i}_1=2\frac{1-k}{k}\bar{i}_2 \tag{11.34}$$

where

$\bar{i}_1$ is the average input current in the switch-on period kT, which is equal to I_1/k

$2\bar{i}_2$ is the average output current in the switch-off period $(1-k)T$, which is equal to $I_2/(1-k)$

Therefore, we have $I_1 = 2I_2$. The variation of the voltage across capacitor C is

$$\Delta v_C=\frac{1}{C}\int_0^{kT} i_C(t)dt=\frac{kT}{2C}\bar{i}_1=\frac{k(V_1-V_C)}{2fCR} \quad 0\le t<kT$$

or

$$\Delta v_C=\frac{1}{C}\int_{kT}^{T} i_C(t)dt=\frac{(1-k)T}{C}\bar{i}_2=\frac{(1-k)(2V_C-V_2)}{fCR} \quad kT\le t<T$$

To simplify the calculation, setting $k = 0.5$, we have

$$V_C=\frac{0.5V_1+V_2}{2.5}=11.2\text{ V} \tag{11.35}$$

Hence,

$$\Delta v_C=\frac{k(V_1-V_C)}{2fCR}=0.7\text{ V} \tag{11.36}$$

We then have

$$v_C(0) = V_C - (\Delta v_C/2) = 10.85\text{ V}$$

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and

$$v_C(kT) = V_C + (\Delta v_C/2) = 11.55 \text{ V}$$

The average output current is

$$I_2 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_2}{R} \tag{11.37}$$

TABLE 11.7
Calculation Results for Mode A2 ($V_1 < V_2$)

k	V_C (V)	Δv_C (V)	I_1 (A)	I_2 (A)	P_1 (W)	P_o (W)	η_{A2}
0.5	11.2	0.7	28	14	392	294	0.75

The average input current is

$$I_1 = \frac{1}{T}\int_{0}^{kT} i_C(t)dt \approx k\frac{V_1 - V_C}{R} \tag{11.38}$$

The output power is

$$P_o = V_2 I_2 = (1-k)V_2\frac{2V_C - V_2}{R} \tag{11.39}$$

The input power is

$$P_i = V_1 I_1 = kV_1\frac{V_1 - V_C}{R} \tag{11.40}$$

The transfer efficiency is

$$\eta_{A2} = \frac{P_o}{P_i} = \frac{1-k}{k}\frac{V_2}{V_1}\frac{2V_C - V_2}{V_1 - V_C} = \frac{V_2}{2V_1} \tag{11.41}$$

From this equation, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. If f = 5 kHz, V_1 = 14 V and V_2 = 21 V, and total C = 4000 μF, R = 50 mΩ. For k = 0.5, the data are listed in Table 11.7.

From the analysis and calculation, it can be seen that the power transfer efficiency only depends on the source and load voltages.

11.3.1.3 Experimental Results

A testing rig of two batteries 14 VDC and 21 VDC was prepared. The testing conditions were f = 5 kHz, V**1** = 21 V and V**2** = 14 V, total C = 4000 | F, and R = 50 mQ. The experimental results for Mode A are shown in Table 11.8. The equipment volume is 24 in.^{3}. The total average PD is 23.8 W/in.^{3}. This figure is much higher than the classical converters whose PD is usually less than 5 W/in.^{3}. Since the switching frequency is low, the EMI is weak.

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TABLE 11.8
Experimental Results

I_1 (A)	I_2 (A)	V_C (V)	P_i (W)	P_o (W)	η	$\bar{P}$ (W)	PD (W/in.^{3})
33	32	17.5	693	448	0.646	571	23.8

11.3.2 Mode B (Q_{II}: Forward Regenerative Braking)

11.3.2.1 Mode B1: Condition $V_1 > V_2$

For Mode B1, condition $V_1 > V_2$ is shown in Figure 11.7. This mode operation is similar to Mode A2. Because two capacitors are connected in parallel during switch-on, the total capacitance $C = 2 \times C_1 = 4000$ μF. The input current i_1 is two times the capacitor current i_{C_1}. Two capacitors are connected in series during switch-off; the total capacitance $C' = C_1/2 = 1000$ μF. The output current i_2 is equal to the capacitor current i_{C_1}. Suppose that the equivalent circuit resistance $R = 50$ mΩ. $V_1 = 21$ V and $V_2 = 14$ V, and the switching frequency $f = 5$ kHz. In order to save the description, we quote the results as follows. The voltage and current across each capacitor are

$$v_{C_1}(t) = \begin{cases} v_{C_1}(0) + \dfrac{1}{C_1}\displaystyle\int_0^t i_{C_1}(t)dt \approx v_{C_1}(0) + \dfrac{t}{2C_1}\bar{i}_2 & 0 \le t < kT \\ v_{C_1}(kT) + \dfrac{1}{C_1}\displaystyle\int_{kT}^t i_{C_1}(t)dt \approx v_{C_1}(kT) - \dfrac{t-kT}{C_1}\bar{i}_1 & kT \le t < T \end{cases} \tag{11.42}$$

$$i_{C_1}(t) = \begin{cases} \dfrac{V_2 - v_{C_1}(0)}{R}(1 - e^{-t/RC}) \approx \dfrac{V_2 - V_{C_1}}{R} = \bar{i}_2/2 & 0 \le t < kT \\ -\dfrac{2v_{C_1}(kT) - V_1}{R}e^{-t/RC} \approx -\dfrac{2V_{C_1} - V_1}{R} = -\bar{i}_1 & kT \le t < T \end{cases} \tag{11.43}$$

Therefore,

$$\bar{i}_2 = 2\frac{1-k}{k}\bar{i}_1 \tag{11.44}$$

where

$\bar{i}_2$ is the average input current in the switch-on period kT, which is equal to I_2/k

$2\bar{i}_1$ is the average output current in the switch-off period (1 − k)T, which is equal to $I_1/(1 - k)$

Therefore, we have $I_2 = 2I_1$. The variation of the voltage across capacitor C is

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$$\Delta v_C = \frac{1}{C}\int_0^{kT} i_C(t)dt = \frac{kT}{2C}\bar{i}_2 = \frac{k(V_2 - V_C)}{2fCR} \quad 0 \le t < kT$$

or

$$\Delta v_C = \frac{1}{C}\int_{kT}^{T} i_C(t)dt = \frac{(1-k)T}{C}\bar{i}_1 = \frac{(1-k)(2V_C - V_1)}{fCR} \quad kT \le t < T$$

To simplify the calculation, setting $k = 0.5$, we have

$$V_C = \frac{0.5V_2 + V_1}{2.5} = 11.2 \text{ V} \tag{11.45}$$

Hence,

$$\Delta v_C = \frac{k(V_2 - V_C)}{2fCR} = 0.7 \text{ V} \tag{11.46}$$

$$v_C(0) = V_C - \frac{\Delta v_C}{2} = 10.85 \text{ V}$$

and

$$v_C(kT) = V_C + \frac{\Delta v_C}{2} = 11.55 \text{ V}$$

The average output current is

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{2V_C - V_1}{R} \tag{11.47}$$

The average input current is

$$I_2 = \frac{1}{T}\int_0^{kT} i_C(t)dt \approx k\frac{V_2 - V_C}{R} \tag{11.48}$$

The output power is

$$P_o = V_1 I_1 = (1-k)V_1\frac{2V_C - V_1}{R} \tag{11.49}$$

The input power is

$$P_i = V_2 I_2 = kV_2\frac{V_2 - V_C}{R} \tag{11.50}$$

The transfer efficiency is

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$$\eta_{B1} = \frac{P_o}{P_i} = \frac{1-k}{k}\frac{V_1}{V_2}\frac{2V_C - V_1}{V_2 - V_C} = \frac{V_1}{2V_2} \tag{11.51}$$

From this equation, it can be seen that the transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. If f = 5 kHz, V_1 = 21 V and V_2 = 14 V, and total C = 4000 μ, R = 50 mΩFor k = 0.5, the data are listed in Table 11.9.

From the analysis and calculation, it can be seen that the power transfer efficiency only depends on the source and load voltages.

TABLE 11.9
Calculation Results for Mode B1 ($V_1 > V_2$)

k	V_C (V)	Δv_C (V)	I_1 (W)	I_2 (W)	P_1 (W)	P_o (W)	η_{B1}
0.5	11.2	0.7	28	14	392	294	0.75

11.3.2.2 Mode B2: Condition $V_1 < V_2$

For Mode B2, condition $V_1 < V_2$ is shown in Figure 11.8. This mode is similar to Mode A1. Because two capacitors are connected in parallel, the total capacitance $C = C_1 + C_2$ = 4000 μ*F*. Suppose that the equivalent circuit resistance R = 50 mΩ. V_2 = 21 V and V_1 = 14 V, and the switching frequency f = 5 kHz. The voltage and current across the capacitors are

$$v_C(t) = \begin{cases} v_C(0) + \dfrac{1}{C}\displaystyle\int_0^t i_C(t)dt \approx v_C(0) + \frac{t}{C}\bar{i}_2 & 0 \le t < kT \\ v_C(kT) + \dfrac{1}{C}\displaystyle\int_{kT}^t i_C(t)dt \approx v_C(kT) - \frac{t-kT}{C}\bar{i}_1 & kT \le t < T \end{cases} \tag{11.52}$$

$$i_C(t) = \begin{cases} \dfrac{V_2 - v_C(0)}{R}(1 - e^{-t/RC}) \approx \dfrac{V_2 - V_C}{R} = \bar{i}_2 & 0 \le t < kT \\ -\dfrac{v_C(kT) - V_1}{R}e^{-t/RC} \approx -\dfrac{V_C - V_1}{R} = -\bar{i}_1 & kT \le t < T \end{cases} \tag{11.53}$$

Therefore,

$$\bar{i}_2 = \frac{1-k}{k}\bar{i}_1 \tag{11.54}$$

where

$\bar{i}_2$ is the average input current in the switch-on period kT, which is equal to I_2/k

$\bar{i}_1$ is the average output current in the switch-off period $(1 - k)T$, which is equal to $(I–k)$

Therefore, we have $I_2 = I_1$. The variation of the voltage across capacitor C is

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$$\Delta v_C = \frac{1}{C}\int_0^{kT} i_C(t)dt = \frac{kT}{C}\bar{i}_2 = \frac{k(V_2 - V_C)}{fCR} \quad 0 \le t < kT$$

or

$$\Delta v_C = \frac{1}{C}\int_{kT}^{T} i_C(t)dt = \frac{(1-k)T}{C}\bar{i}_1 = \frac{(1-k)(V_C - V_1)}{fCR} \quad kT \le t < T$$

After calculation,

$$V_C = kV_2 + (1-k)V_1 \tag{11.55}$$

Hence,

$$\Delta v_C = \frac{k(1-k)(V_2 - V_1)}{fCR} \tag{11.56}$$

We then have

$$v_C(0) = V_C - \frac{\Delta v_C}{2}$$

and

$$v_C(kT) = V_C + \frac{\Delta v_C}{2}$$

The average output current is

$$I_1 = \frac{1}{T}\int_{kT}^{T} i_C(t)dt \approx (1-k)\frac{V_C - V_1}{R} \tag{11.57}$$

The average input current is

$$I_2 = \frac{1}{T}\int_0^{kT} i_C(t)dt \approx k\frac{V_2 - V_C}{R} \tag{11.58}$$

The output power is

$$P_o = V_1 I_1 = (1-k)V_1\frac{V_C - V_1}{R} \tag{11.59}$$

The input power is

$$P_i = V_2 I_2 = kV_2\frac{V_2 - V_C}{R} \tag{11.60}$$

The transfer efficiency is

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$$\eta_{B2} = \frac{P_o}{P_i} = \frac{1-k}{k}\frac{V_1}{V_2}\frac{V_C - V_1}{V_2 - V_C} = \frac{V_1}{V_2} \tag{11.61}$$

The transfer efficiency only relies on the ratio of the source and load voltages, and it is independent of R, C, f, and k. If f = 5 kHz, V_2 = 21 V and V_1 = 14 V, and total C = 4000 μF,

R = 50 mΩ. For three k values, we obtain the data in Table 11.10.

TABLE 11.10
Calculation Results for Mode B2 ($V_1 < V_2$)

k	V_C (V)	Δv_C (V)	I_1 (A)	I_2 (A)	η_{A1}
0.4	16.8	1.68	33.6	33.6	0.67
0.5	17.5	1.75	35	35	0.67
0.6	18.2	1.68	33.6	33.6	0.67

From the analysis and calculation, it can be seen that the conduction duty k does not affect the power transfer efficiency. It affects the input and output power in a small region. The maximum output power corresponds to k = 0.5.

11.3.3 Mode C (Q_{III}: Reverse Motoring)

This mode is similar to Mode A.

11.3.4 Mode D (Q_{IV}: Reverse Regenerative Braking)

This mode is similar to Mode B.

11.4 Switched-Inductor Four-Quadrant DC/DC Luo-Converter

Although SC DC/DC converters can reach high PD, their circuits are always very complex with difficult control. If the difference between input and output voltages is large, multiple switch-capacitor stages must be employed. SI DC/DC converters successfully overcome this disadvantage. Usually, only one inductor is required for each converter with one-quadrant, two-quadrant, or four-quadrant operation, no matter how large the difference between the input and output voltages is. Therefore, the SI converter is a very simple circuit and consequently has high PD. This section introduces an SI four-quadrant DC/DC Luo-converter working in four-quadrant operation.

This converter is shown in Figure 11.13a consisting of three switches, two diodes, and only one inductor L. The source voltage V_1 and load voltage V_2 (e.g., a battery or DC motor back EMF) are usually constant voltages. R is the equivalent resistance of the circuit and is usually small. Its equivalent circuits for quadrant I and II and quadrant III and IV operation are shown

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in Figure 11.13b and c. Assuming the condition $V_1 > |V_2|$, they are supposed +42 and ±14 V, respectively. Therefore, there are four quadrants (modes) of operation as follows:

- *Mode A* (*quadrant I, Q_I*)*:* The energy is transferred from source to positive voltage load.
- *Mode B* (*quadrant II, Q_{II}*)*:* The energy is transferred from positive voltage load to source.
- *Mode C* (*quadrant III, Q_{III}*)*:* The energy is transferred from source to negative voltage load.
- *Mode D* (*quadrant IV, Q_{IV}*)*:* The energy is transferred from negative voltage load to source.

The first quadrant is called the forward motoring (Forw. Mot.) operation. V_1 and V_2 are positive, and I_1 and I_2 are positive as well. The second quadrant is called the forward regenerative (Forw. Reg.) braking operation. V_1 and V_2 are positive, and I_1 and I_2 are negative. The third quadrant is called the reverse motoring (Rev. Mot.) operation. V_1 and I_1 are positive, and V_2 and I_2 are negative. The fourth quadrant is called the reverse regenerative (Rev. Reg.) braking operation. V_1 and I_2 are positive, and I_1 and V_2 are negative. Each mode has two states: *on* and *off*. Usually, each state is operating in different conduction duty *k*. The switching period is T where $T = 1/f$. The switch status is shown in Table 11.11.

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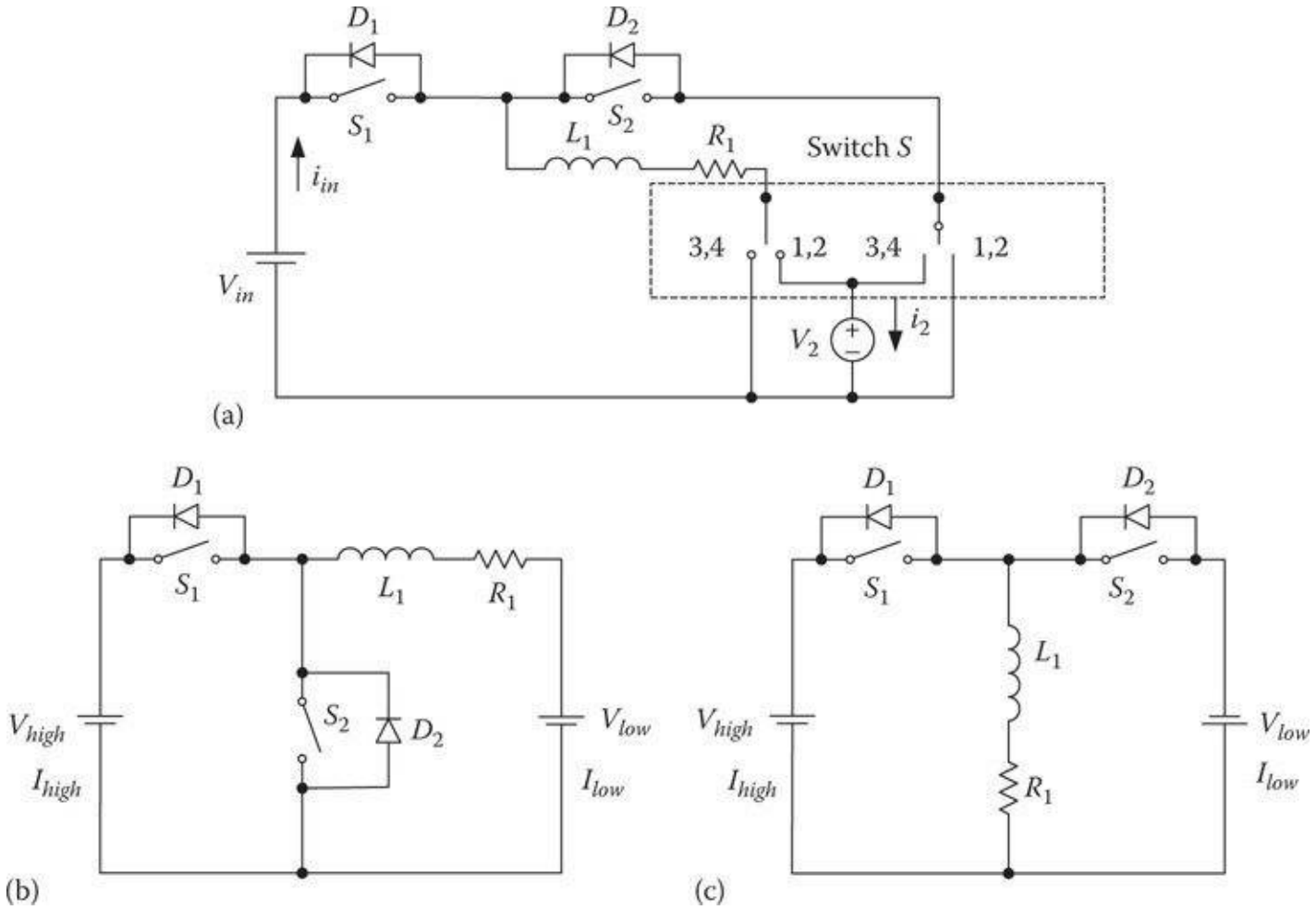


FIGURE 11.13
Four-quadrant switched-inductor DC/DC Luo-converters. (a) Circuit diagram. (b) Quadrant I and II operation circuit. (c) Quadrant III and IV operation circuit.

TABLE 11.11
Switch's Status (No Mentioned Switches Are Off)

Q No.	State	S_1	D_1	S_2	D_2	S_3	Source	Load
Quadrant I, Mode A	On	On				On 1/2	V_1+	V_2+
Forw. Mot.	Off				On	On 1/2	I_1+	I_2+
Quadrant II, Mode B	On			On		On 1/2	V_1+	V_2+
Forw. Reg.	Off		On			On 1/2	I_1-	I_2-
Quadrant III, Mode C	On	On				On 3/4	V_1+	V_2-
Rev. Mot.	Off				On	On 3/4	I_1+	I_2-
Quadrant IV, Mode D	On			On		On 3/4	V_1+	V_2-
Rev. Reg.	Off		On			On 3/4	I_1-	I_2+

Mode A operation is shown in Figure 11.14a (switch-on) and b (switch-off). During switch-*on* state, switch S_1 is closed. In this case, the source voltage V_1 supplies the load V_2 and inductor L, and the inductor current i_L increases. During switch-off state, diode D_2 is on. In

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this case, the current i_L flows through the load V_2 via the freewheeling diode D_2, and it decreases.

Mode B operation is shown in Figure 11.15a (switch-on) and b (switch-off). During switch-*on* state, switch S_2 is closed. In this case, the load voltage V_2 supplies the inductor L, and the inductor current i_L increases. During switch-off state, the diode D_1 is on, and the current i_L flows through the source V_1 and load V_2 via the diode D1 and decreases.

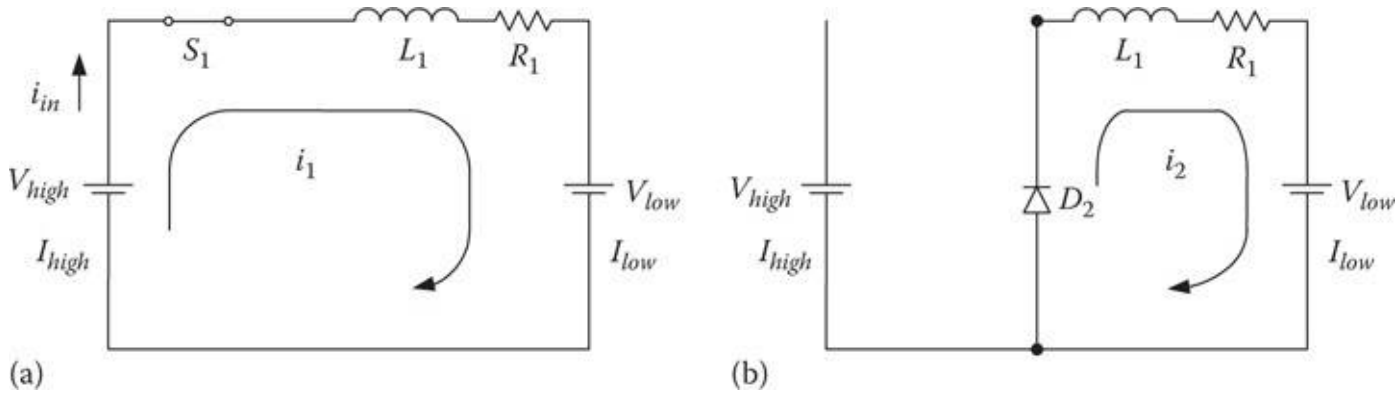


FIGURE 11.14
Mode A (quadrant I) operation. (a) Switch-on. (b) Switch-off.

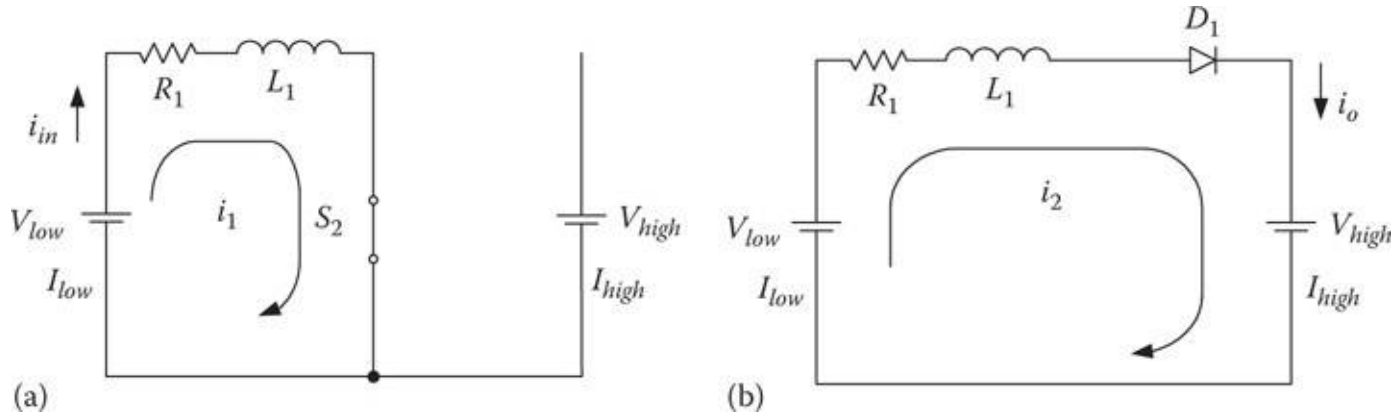


FIGURE 11.15
Mode B (quadrant II) operation. (a) Switch-on. (b) Switch-off.

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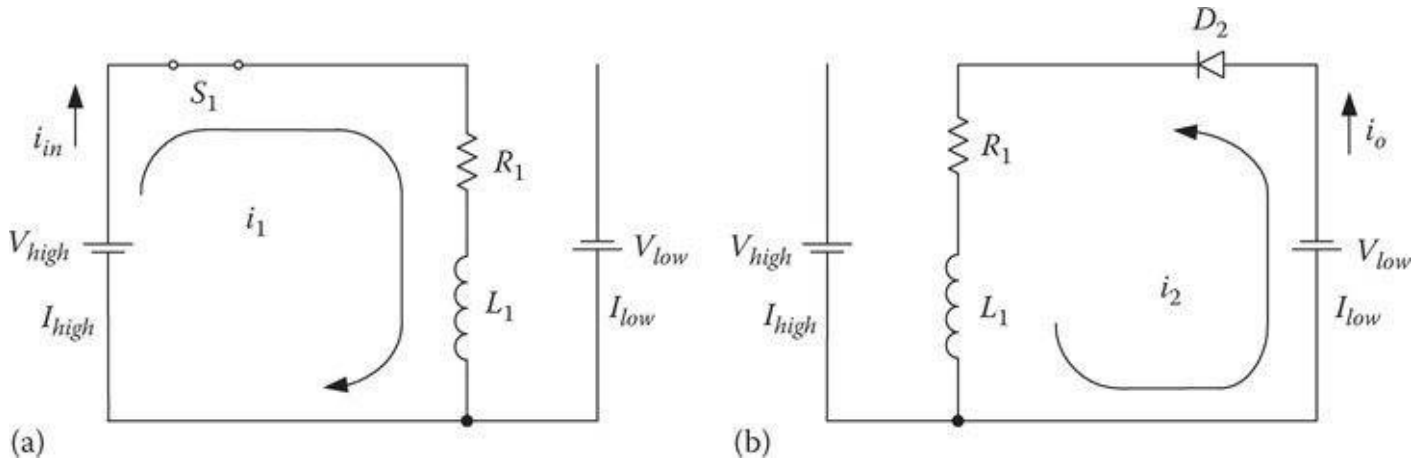


FIGURE 11.16
Mode C (quadrant III) operation. (a) Switch-on. (b) Switch-off.

Mode C operation is shown in Figure 11.16a (switch-on) and b (switch-off). During switch-on state, the switch S_1 is closed. The source voltage V_1 supplies the inductor L, and the inductor current i_L increases. During switch-*off* state, the diode D_2 is on. The current i_L flows through the load V_2 via the freewheeling diode D_2, and it decreases.

Mode D operation is shown in Figure 11.17a (switch-on) and b (switch-off). During switch-on state, the switch S_2 is closed. The load voltage V_2 supplies the inductor L, and the inductor current i_L increases. During switch-*off* state, the diode D_1 is on. The current i_L flows through the source V_1 via the diode D_1, and it decreases.

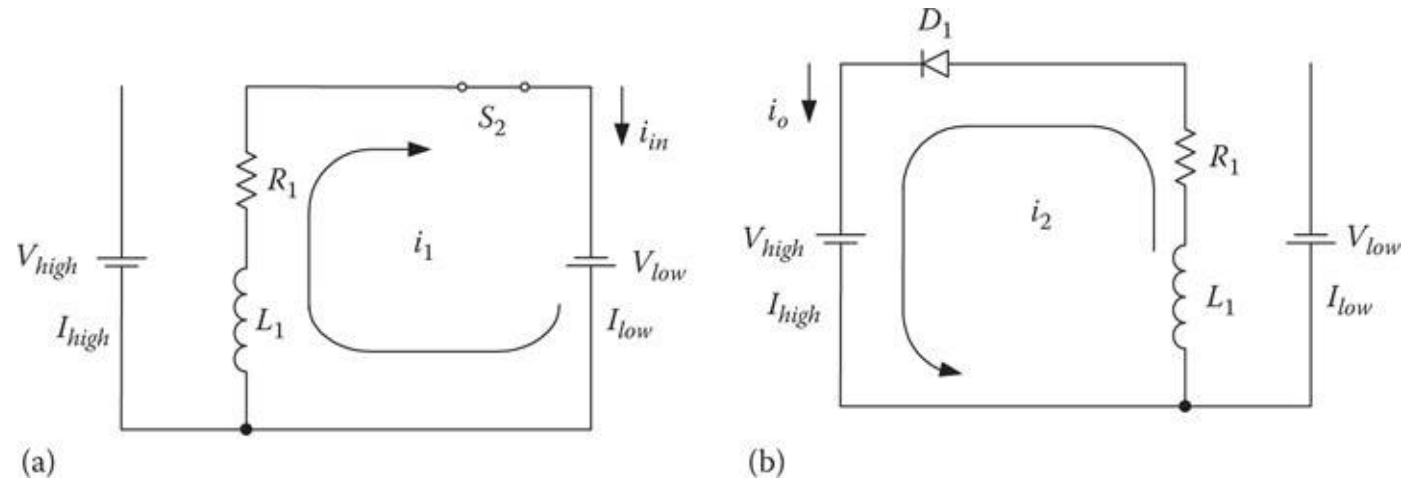


FIGURE 11.17
Mode D (quadrant IV) operation. (a) Switch-on. (b) Switch-off.

11.4.1 Mode A (Q|: Forward Motoring)

11.4.1.1 Continuous Mode

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Refer to Figure 11.14a and suppose that V_1 = +42 V and V_2 = +14 V, L = 0.3 mH, and the parasitic resistance R = 3 mΩ.

$$v_L(t) = \begin{cases} V_1 - V_2 - RI_L & 0 \le t < kT \\ -(V_2 + RI_L) & kT \le t < T \end{cases} \tag{11.62}$$

$$i_L(t) = \begin{cases} i_L(0) + \dfrac{V_1 - V_2 - RI_L}{L} t & 0 \le t < kT \\ i_L(kT) - \dfrac{V_2 + RI_L}{L}(t - kT) & kT \le t < T \end{cases} \tag{11.63}$$

where

$$i_L(0) = I_L - \frac{\Delta i_L}{2} \tag{11.64}$$

$$i_L(kT) = I_L + \frac{\Delta i_L}{2} \tag{11.65}$$

From Equations 11.62 and 11.63, the average inductor current is

$$I_L = \frac{kV_1 - V_2}{R} \tag{11.66}$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)V_1}{fL} \tag{11.67}$$

The variation ratio is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2} \frac{R}{2fL} \tag{11.68}$$

Substituting Equations 11.66 and 11.67 into Equations 11.64 and 11.65, we have

$$i_L(0) = \frac{kV_1 - V_2}{R} - \frac{k(1-k)V_1}{2fL} \tag{11.69}$$

and

$$i_L(kT) = \frac{kV_1 - V_2}{R} + \frac{k(1-k)V_1}{2fL} \tag{11.70}$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt \approx k\frac{kV_1 - V_2}{R} \tag{11.71}$$

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The average output current is

$$I_o = \frac{1}{T}\int_0^T i_L(t)dt \approx \frac{kV_1 - V_2}{R} \tag{11.72}$$

The input power is

$$P_i = V_1 I_i = kV_1 \frac{kV_1 - V_2}{R} \tag{11.73}$$

The output power is

$$P_o = V_2 I_o = V_2 \frac{kV_1 - V_2}{R} \tag{11.74}$$

The transfer efficiency is

$$\eta_A = \frac{P_o}{P_i} = \frac{V_2}{kV_1} \tag{11.75}$$

The transfer efficiency only relies on conduction duty k, the source, and load voltages. It is independent of *R*, *L*, and *f*.

If f = 1 kHz, L = 300 μH, R = 3 mΩ, k = 0.35, and V_1 = 42 V and V_2 = 14 V, we find that

$$I_L = 233 \text{ A}$$

$$\Delta i_L = 31.85 \text{ A}$$

$$\zeta = 6.83\%$$

$$I_i = I_1 = 81.6 \text{ A}$$

$$I_o = I_2 = 233 \text{ A}$$

$$P_o = 32{,}672 \text{ W}$$

$$P_i = 3{,}427 \text{ W}$$

$$\eta_A = 95\%$$

11.4.1.2 Discontinuous Mode

From Equation 11.68, when ζ ≥1, the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined as

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$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_1}{kV_1 - V_2}\frac{R}{2fL} \geq 1$$

that is,

$$\frac{k(1-k)V_1}{kV_1 - V_2}\frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_2}{V_1} + k(1-k)\frac{R}{2fL} \tag{11.76}$$

From this, the discontinuous conduction region is caused by the following factors:

- The switching frequency *f* is too low.
- The duty cycle *k* is too small.
- The inductance *L* is too small.
- The load resistor *R* is too big.

The whole conduction period is smaller than *T*. Assuming the conduction period is in the region between 0 and t_1 that is smaller than *T*. The filling coefficient m_A is defined as

$$m_A = \frac{t_1 - kT}{(1-k)T} \quad kT < t_1 \leq T \tag{11.77}$$

The voltage and current across inductor *L* are

$$v_L(t) = \begin{cases} V_1 - V_2 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < t_1 \\ 0 & t_1 \leq t < T \end{cases} \tag{11.78}$$

$$i_L(t) = \begin{cases} \dfrac{V_1 - V_2 - RI_L}{L}t & 0 \leq t < kT \\ \dfrac{V_1}{L}kT - \dfrac{V_2 + RI_L}{L}t & kT \leq t < t_1 \\ 0 & t_1 \leq t < T \end{cases} \tag{11.79}$$

because $i_L(0) = 0$

$$i_L(kT) = \frac{V_1 - V_2 - RI_L}{L}kT$$

and $i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L. From Equation 11.79 when $t = t_1$, $i_L(t_1) = 0$. Therefore, we have the following relation:

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$$i_L(t_1) = \frac{V_1}{L}kT - \frac{V_2 + RI_L}{L}t_1 = 0$$

Therefore,

$$t_1 = \frac{V_1}{V_2 + RI_L}kT \tag{11.80}$$

Considering Equation 11.76, $kT < t_1 < T$.

Since R is usually small, we can get

$$t_1 \approx (V_1/V_2)kT$$

The average inductor current is

$$I_L = \frac{1}{T}\int_0^{t_1} i_L(t)dt = \frac{t_1}{2T}i_L(kT_s) = \frac{V_1}{V_2 + RI_L}\frac{V_1 - V_2 - RI_L}{2fL}k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1}{V_2}\frac{V_1 - V_2}{2fL}k^2$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt = \frac{i_L(kT)}{2T}kT = \frac{V_1 - V_2 - RI_L}{2fL}k^2$$

The average output current is

$$I_o = \frac{1}{T}\int_0^{t_1} i_L(t)dt = \frac{i_L(kT)}{2T}t_1 = \frac{V_1 - V_2 - RI_L}{2fL}\frac{V_1}{V_2 + RI_L}k^2$$

The input power is

$$P_i = V_1 I_i = V_1\frac{V_1 - V_2 - RI_L}{2fL}k^2$$

The output power is

$$P_o = V_2 I_o = V_2\frac{V_1 - V_2 - RI_L}{2fL}\frac{V_1}{V_2 + RI_L}k^2$$

The transfer efficiency is

$$\eta_{A\text{-}dis} = \frac{P_o}{P_i} = \frac{V_2}{V_2 + RI_L} \tag{11.81}$$

with

$$k \le \frac{V_2}{V_1} + k(1-k)\frac{R}{2fL}$$

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11.4.2 Mode B (Q_{III}: Forward Regenerative Braking)

11.4.2.1 Continuous Mode

Refer to Figure 11.15a and suppose that V_1 = +42 V and V_2 = +14 V, L = 0.3 mH, and the parasitic resistance R = 3 mΩ.

$$V_L(t) = \begin{cases} V_2 - RI_L & 0 \le t < kT \\ -(V_1 - V_2 + RI_L) & kT \le t < T \end{cases} \tag{11.82}$$

$$i_L(t) = \begin{cases} i_L(0) + \dfrac{V_2 - RI_L}{L} t & 0 \le t < kT \\ i_L(kT) - \dfrac{V_1 - V_2 + RI_L}{L}(t - kT) & kT \le t < T \end{cases} \tag{11.83}$$

where

$$i_L(0) = I_L - \frac{\Delta i_L}{2} \tag{11.84}$$

$$i_L(kT) = I_L + \frac{\Delta i_L}{2} \tag{11.85}$$

Since the inductor average voltage is zero, we have

$$k(V_2 - RI_L) = (1-k)(V_1 - V_2 + RI_L)$$

then

$$I_L = \frac{V_2 - (1-k)V_1}{R} \tag{11.86}$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)V_1}{fL} \tag{11.87}$$

The variation ratio is

$$\zeta = \frac{\Delta i_L / 2}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1} \frac{R}{2fL} \tag{11.88}$$

Substituting Equations 11.86 and 11.87 into Equations 11.84 and 11.85, we have

$$i_L(0) = \frac{V_2 - (1-k)V_1}{R} - \frac{k(1-k)V_1}{2fL} \tag{11.89}$$

and

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$$i_L(kT) = \frac{V_2 - (1-k)V_1}{R} + \frac{k(1-k)V_1}{2fL} \tag{11.90}$$

The average input current is

$$I_i = \frac{1}{T}\int_0^T i_L(t)dt = \frac{V_2 - (1-k)V_1}{R} \tag{11.91}$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^T i_L(t)dt = (1-k)\frac{V_2 - (1-k)V_1}{R} \tag{11.92}$$

The input power is

$$P_i = V_2 I_i = V_2 \frac{V_2 - (1-k)V_1}{R} \tag{11.93}$$

The output power is

$$P_o = V_1 I_o = (1-k)V_1 \frac{V_2 - (1-k)V_1}{R} \tag{11.94}$$

The transfer efficiency is

$$\eta_B = \frac{P_o}{P_i} = \frac{(1-k)V_1}{V_2} \tag{11.95}$$

The transfer efficiency only relies on conduction duty *k*, the source, and load voltages. It is independent of *R*, *L*, and *f*.

11.4.2.2 Discontinuous Mode

From Equation 11.88, when $\zeta \geq 1$, the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined as

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)V_1}{V_2 - (1-k)V_1}\frac{R}{2fL} \geq 1$$

that is,

$$\frac{k(1-k)V_1}{V_2 - (1-k)V_1}\frac{R}{2fL} \geq 1$$

or

$$k \leq \left(1 - \frac{V_2}{V_1}\right) + k(1-k)\frac{R}{2fL} \tag{11.96}$$

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The whole conduction period is smaller than T. Assume that the conduction period is in the region between 0 and t_2 that is smaller than T. The filling coefficient m_B is defined as

$$m_B = \frac{t_2 - kT}{(1-k)T} \quad kT < t_2 \le T \tag{11.97}$$

The voltage and current across inductor L are

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \le t < kT \\ -(V_1 - V_2 + RI_L) & kT \le t < t_2 \\ 0 & t_2 \le t < T \end{cases} \tag{11.98}$$

$$i_L(t) = \begin{cases} \dfrac{V_2 - RI_L}{L} t & 0 \le t < kT \\ \dfrac{V_1}{L} kT - \dfrac{V_1 - V_2 + RI_L}{L} t & kT \le t < t_2 \\ 0 & t_2 \le t < T \end{cases} \tag{11.99}$$

because $i_L(0) = 0$

$$i_L(kT) = \frac{V_2 - RI_L}{L} kT$$

and $i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L. From Equation 11.99 when $t = t_2$, $i_L(t_2) = 0$. Therefore, we have the following relation:

$$i_L(t_2) = \frac{V_1}{L} kT - \frac{V_1 - V_2 + RI_L}{L} t_2 = 0$$

Therefore,

$$t_2 = \frac{V_1}{V_1 - V_2 + RI_L} kT \tag{11.100}$$

Considering Equation 11.86, $kT < t_2 < T$.

Since R is usually small,

$$t_2 \approx V_1/(V_1 - V_2)kT$$

The average inductor current is

$$I_L = \frac{1}{T}\int_0^t i_L(t)dt = \frac{t_2}{2T} i_L(kT) = \frac{V_1}{V_1 - V_2 + RI_L} \frac{V_2 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1}{V_1 - V_2} \frac{V_2}{2fL} k^2$$

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The average input current is

$$I_i = \frac{1}{T}\int_0^t i_L(t)dt = \frac{i_L(kT)}{2T}t_2 = \frac{V_1}{V_1 - V_2 + RI_L}\frac{V_2 - RI_L}{2fL}k^2$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^{t_2} i_L(t)dt = \frac{i_L(kT)}{2T}(t_2 - kT) = \frac{1}{2fL}\frac{(V_2 - RI_L)^2}{V_1 - V_2 + RI_L}k^2$$

The input power is

$$P_i = V_2 I_i = V_2 \frac{V_1}{V_1 - V_2 + RI_L}\frac{V_2 - RI_L}{2fL}k^2$$

The output power is

$$P_o = V_1 I_o = V_1 \frac{V_2 - RI_L}{2fL}\frac{V_2 - RI_L}{V_1 - V_2 + RI_L}k^2$$

The transfer efficiency is

$$\eta_{B\text{-}dis} = \frac{P_o}{P_i} = \frac{V_2 - RI_L}{V_2} \tag{11.101}$$

with

$$k \le \left(1 - \frac{V_2}{V_1}\right) + k(1-k)\frac{R}{2fL}$$

11.4.3 Mode C (Q_{III}: Reverse Motoring)

11.4.3.1 Continuous Mode

Refer to Figure 11.16a and suppose that V_1 = +42 V and V_2 = −14 V, L = 0.3 mH, and the parasitic resistance R = 3 mΩ

$$v_L(t) = \begin{cases} V_1 - RI_L & 0 \le t < kT \\ -(V_2 + RI_L) & kT \le t < T \end{cases} \tag{11.102}$$

$$i_L(t) = \begin{cases} i_L(0) + \dfrac{V_1 - RI_L}{L}t & 0 \le t < kT \\ i_L(kT) - \dfrac{V_2 + RI_L}{L}(t - kT) & kT \le t < T \end{cases} \tag{11.103}$$

where

$$i_L(0) = I_L - \frac{\Delta i_L}{2} \tag{11.104}$$

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$$i_L(kT) = I_L + \frac{\Delta i_L}{2} \tag{11.105}$$

Since the inductor average voltage is zero, we have

$$k(V_1 - RI_L) = (1-k)(V_2 + RI_L)$$

$$I_L = \frac{kV_1 - (1-k)V_2}{R} \tag{11.106}$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)(V_1 + V_2)}{fL} \tag{11.107}$$

The variation ratio is

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1 + V_2)}{kV_1 - (1-k)V_2} \frac{R}{2fL} \tag{11.108}$$

Substituting Equations 11.106 and 11.107 into Equations 11.104 and 11.105, we have

$$i_L(0) = \frac{kV_1 - (1-k)V_2}{R} - \frac{k(1-k)(V_1 + V_2)}{2fL} \tag{11.109}$$

and

$$i_L(kT) = \frac{kV_1 - (1-k)V_2}{R} + \frac{k(1-k)(V_1 + V_2)}{2fL} \tag{11.110}$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt = k\frac{kV_1 - (1-k)V_2}{R} \tag{11.111}$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^{T} i_L(t)dt = (1-k)\frac{kV_1 - (1-k)V_2}{R} \tag{11.112}$$

The input power is

$$P_i = V_1 I_i = kV_1 \frac{kV_1 - (1-k)V_2}{R} \tag{11.113}$$

The output power is

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$$P_o = V_2 I_o = (1-k)V_2 \frac{kV_1 - (1-k)V_2}{R} \tag{11.114}$$

The transfer efficiency is

$$\eta_C = \frac{P_o}{P_i} = \frac{(1-k)V_2}{kV_1} \tag{11.115}$$

The transfer efficiency only relies on conduction duty k, the source, and load voltages. It is independent of R, L, and f.

11.4.3.2 Discontinuous Mode

From Equation 11.108, when $\zeta \geq 1$, the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined as

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1+V_2)}{kV_1-(1-k)V_2}\frac{R}{2fL} \geq 1$$

that is,

$$\frac{k(1-k)(V_1+V_2)}{kV_1-(1-k)V_2}\frac{R}{2fL} \geq 1$$

or

$$k \leq \frac{V_2}{V_1+V_2} + k(1-k)\frac{R}{2fL} \tag{11.116}$$

The whole conduction period is smaller than T. Assume that the conduction period is in the region between 0 and t_3. The filling coefficient m_C is defined as

$$m_C = \frac{t_3 - kT}{(1-k)T} \quad kT < t_3 \leq T \tag{11.117}$$

The voltage and current across indictor L are

$$v_L(t) = \begin{cases} V_1 - RI_L & 0 \leq t < kT \\ -(V_2 + RI_L) & kT \leq t < t_3 \\ 0 & t_3 \leq t < T \end{cases} \tag{11.118}$$

$$i_L(t) = \begin{cases} \dfrac{V_1 - RI_L}{L}t & 0 \leq t < kT \\ \dfrac{V_1+V_2}{L}kT - \dfrac{V_2+RI_L}{L}t & kT \leq t < t_3 \\ 0 & t_3 \leq t < T \end{cases} \tag{11.119}$$

because $i_L(0) = 0$

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$$i_L(kT) = \frac{V_1 - RI_L}{L} kT$$

and $i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L. From Equation 11.119 when $t = t_3$, $i_L(t_3) = 0$. Therefore, we have the following relation:

$$i_L(t_3) = \frac{V_1 + V_2}{L} kT - \frac{V_2 + RI_L}{L} t_3 = 0$$

Therefore,

$$t_3 = \frac{V_1 + V_2}{V_2 + RI_L} kT \tag{11.120}$$

Considering Equation 11.80, $kT < t_3 < T$.

Since R is usually small,

$$t_1 \approx \frac{V_1}{V_2} kT$$

The average inductor current is

$$I_L = \frac{1}{T}\int_0^{t_3} i_L(t)dt = \frac{t_3}{2T} i_L(kT) = \frac{V_1 + V_2}{V_2 + RI_L} \frac{V_1 - RI_L}{2fL} k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1 + V_2}{V_2} \frac{V_1}{2fL} k^2$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt = \frac{i_L(kT)}{2T} kT = \frac{V_1 - RI_L}{2fL} k^2$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^{t_3} i_L(t)dt = \frac{i_L(kT)}{2T}(t_3 - kT) = \frac{(V_1 - RI_L)^2}{2fL(V_2 + RI_L)} k^2$$

The input power is

$$P_i = V_1 I_i = V_1 \frac{V_1 - RI_L}{2fL} k^2$$

The output power is

$$P_o = V_2 I_o = V_2 \frac{(V_1 - RI_L)^2}{2fL(V_2 + RI_L)} k^2$$

The transfer efficiency is

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$$\eta_{C\text{-}dis} = \frac{P_o}{P_i} = \frac{V_2}{V_1}\frac{V_1 - RI_L}{V_2 + RI_L}$$

with

$$i_L(t) = \begin{cases} i_L(0) + \dfrac{V_2 - RI_L}{L}t & 0 \le t < kT \\ i_L(kT) - \dfrac{V_1 + RI_L}{L}(t - kT) & kT \le t < T \end{cases} \tag{11.123}$$

11.4.4 Mode D (Q_{IV}: Reverse Regenerative Braking)

11.4.4.1 Continuous Mode

Refer to Figure 11.17a and suppose that V_1 = +42 V and V_2 = –14 V, L = 0.3 mH, and the parasitic resistance R = 3 mΩ.

$$v_L(t) = \begin{cases} V_2 - RI_L & 0 \le t < kT \\ -(V_1 + RI_L) & kT \le t < T \end{cases} \tag{11.122}$$

$$i_L(t) = \begin{cases} i_L(0) + \dfrac{V_2 - RI_L}{L}t & 0 \le t < kT \\ i_L(kT) - \dfrac{V_1 + RI_L}{L}(t - kT) & kT \le t < T \end{cases} \tag{11.123}$$

where

$$i_L(kT) = \frac{kV_2 - (1-k)V_1}{R} + \frac{k(1-k)(V_1 + V_2)}{2fL} \tag{11.130}$$

$$i_L(kT) = I_L + \frac{\Delta i_L}{2} \tag{11.125}$$

Since the inductor average voltage is zero, we have

$$k(V_2 - RI_L) = (1-k)(V_1 + RI_L)$$

then

$$I_L = \frac{kV_2 - (1-k)V_1}{R} \tag{11.126}$$

The peak-to-peak variation of inductor current i_L is

$$\Delta i_L = \frac{k(1-k)(V_1 + V_2)}{fL} \tag{11.127}$$

The variation ratio is

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$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1+V_2)}{kV_2-(1-k)V_1}\frac{R}{2fL} \tag{11.128}$$

Substituting Equations 11.126 and 11.127 into Equations 11.124 and 11.125, we have

$$i_L(0) = \frac{kV_2-(1-k)V_1}{R} - \frac{k(1-k)(V_1+V_2)}{2fL} \tag{11.129}$$

and

$$i_L(kT) = \frac{kV_2-(1-k)V_1}{R} + \frac{k(1-k)(V_1+V_2)}{2fL} \tag{11.130}$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt = k\frac{kV_2-(1-k)V_1}{R} \tag{11.131}$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^{T} i_L(t)dt = (1-k)\frac{kV_2-(1-k)V_1}{R} \tag{11.132}$$

The input power is

$$P_i = V_2 I_i = kV_2\frac{kV_2-(1-k)V_1}{R} \tag{11.133}$$

The output power is

$$P_o = V_1 I_o = (1-k)V_1\frac{kV_2-(1-k)V_1}{R} \tag{11.134}$$

The transfer efficiency is

$$\eta_D = \frac{P_o}{P_i} = \frac{(1-k)V_1}{kV_2} \tag{11.135}$$

The transfer efficiency only relies on conduction duty k, the source, and load voltages. It is independent of R, L, and f.

11.4.4.2 Discontinuous Mode

From Equation 11.118, when $\zeta \geq 1$, the current i_L is discontinuous. The boundary between continuous and discontinuous regions is defined as

$$\zeta = \frac{\Delta i_L/2}{I_L} = \frac{k(1-k)(V_1+V_2)}{kV_2-(1-k)V_1}\frac{R}{2fL} \geq 1$$

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that is,

$$\frac{k(1-k)(V_1+V_2)}{kV_2-(1-k)V_1}\frac{R}{2fL}\geq 1$$

or

$$k\leq \frac{V_1}{V_1+V_2}+k(1-k)\frac{R}{2fL} \tag{11.136}$$

The whole conduction period is smaller than T. Assume that the conduction period is in the region between 0 and t_4. The filling coefficient m_D is defined as

$$m_D=\frac{t_4-kT}{(1-k)T}\quad kT<t_4\leq T \tag{11.137}$$

The voltage and current across inductor L are

$$v_L(t)=\begin{cases} V_2-RI_L & 0\leq t<kT \\ -(V_1+RI_L) & kT\leq t<t_4 \\ 0 & t_4\leq t<T \end{cases} \tag{11.138}$$

$$i_L(t)=\begin{cases} \dfrac{V_2-RI_L}{L}t & 0\leq t<kT \\ \dfrac{V_1+V_2}{L}kT-\dfrac{V_1+RI_L}{L}t & kT\leq t<t_4 \\ 0 & t_4\leq t<T \end{cases} \tag{11.139}$$

because $i_L(0) = 0$

$$i_L(kT)=\frac{V_2-RI_L}{L}kT$$

and $i_L(kT)$ is the peak value of inductor current $i_L(t)$. It is also the peak-to-peak variation Δi_L. From Equation 11.139 when $t = t_4$, $i_L(t_4) = 0$. Therefore, we have the following relation:

$$i_L(t_4)=\frac{V_1+V_2}{L}kT-\frac{V_1+RI_L}{L}t_4=0$$

Therefore,

$$t_4=\frac{V_1+V_2}{V_1+RI_L}kT \tag{11.140}$$

Considering Equation 11.136, $kT < t_4 < T$.

Since R is usually small, we can get

$$t_4\approx((V_1+V_2)/V_1)kT$$

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The average inductor current is

$$I_L = \frac{1}{T}\int_0^{t_4} i_L(t)dt = \frac{t_4}{2T} i_L(kT) = \frac{V_1 + V_2}{V_1 + RI_L}\frac{V_2 - RI_L}{2fL}k^2$$

Since R is usually small, it can be rewritten as

$$I_L \approx \frac{V_1 + V_2}{V_1}\frac{V_2}{2fL}k^2$$

The average input current is

$$I_i = \frac{1}{T}\int_0^{kT} i_L(t)dt = \frac{i_L(kT)}{2T}kT = \frac{V_2 - RI_L}{2fL}k^2$$

The average output current is

$$I_o = \frac{1}{T}\int_{kT}^{t_4} i_L(t)dt = \frac{i_L(kT)}{2T}(t_4 - kT) = \frac{1}{2fL}\frac{(V_2 - RI_L)^2}{V_1 + RI_L}k^2$$

The input power is

$$P_i = V_2 I_i = V_2\frac{V_2 - RI_L}{2fL}k^2$$

The output power is

$$P_o = V_1 I_o = V_1\frac{1}{2fL}\frac{(V_2 - RI_L)^2}{V_1 + RI_L}k^2$$

The transfer efficiency is

$$\eta_{D\text{-}dis} = \frac{P_o}{P_i} = \frac{V_1}{V_2}\frac{V_2 - RI_L}{V_1 + RI_L} \tag{11.141}$$

with

$$k \le \frac{V_1}{V_1 + V_2} + k(1-k)\frac{R}{2fL}$$

11.4.5 Experimental Results

A testing rig of a battery 14 VDC as a load and a source 42 VDC as the power supply was tested. The testing conditions were f = 1–5 kHz, V_H = 42 V, V_L = −14 V, L = 0.3 mH, and R = 3 mΩ, and the volume is 2750 in.^{3}. The experimental results show that the total average PD is 28.8 W/in.^{3}. This figure is much higher than the classical converters whose PD is usually less than 5 W/in.^{3}. Since the switching frequency is low, the EMI is weak.

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12

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Positive-Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

The micro-power-consumption technique requires high-power-density DC/DC converters and power supply sources. The voltage-lift (VL) technique is a popular application in electronic circuit design. Since the switched-capacitor (SC) can be integrated into the power integrated circuit chip, its size is small. Combining the SC and VL technique creates a DC/DC converter with small size, high power density, high voltage transfer gain, high power efficiency, and low EMI.

12.1 Introduction

Switched-capacitor (SC) converters can perform in push-pull state with conduction duty cycle $k = 0.5$. Voltage-lift (VL) technique is a popular method widely used in electronic circuit design. Combining SC and VL technique can construct the DC/DC converters with small size, high power density, high voltage transfer gain, high power efficiency, and low EMI. This chapter introduces a new series DC/DC converters—positive-output multiple-lift push–pull SC DC/DC Luo-converters. These converters can be sorted into several subseries as follows:

- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series

Each circuit has one main switch S and several slave switches as S_i ($i = 1, 2, 3, \ldots, n$). The number n is called stage number. The main switch S is on and slaves off during switch-on period kT, and S is off and slaves on during switch-off period $(1 - k)T$. The load is resistive load R. The input voltage and current are V_{in} and I_{in}, and the output voltage and current are V_o and I_o.

12.2 Main Series

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The first three stages of the main series are shown in Figures 12.1, 12.2 and 12.3. For the convenience of explaining, they are called elementary circuit, re-lift circuit, and triple-lift circuit, respectively, and are numbered as n = 1, 2, and 3.

12.2.1 Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and switch-off period are shown in Figure 12.1. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitor C_2 is charged to $V_o = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = 2V_{in} \tag{12.1}$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1. The real output voltage is

$$V_o = 2V_{in} - \Delta V_1 \tag{12.2}$$

12.2.2 Re-Lift Circuit

The re-lift circuit is derived from the elementary circuit by adding a parts-set: one slave switch, two SCs, and three diodes (S_2–C_3–C_4–D_3–D_4–D_5). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.2. The switches S and

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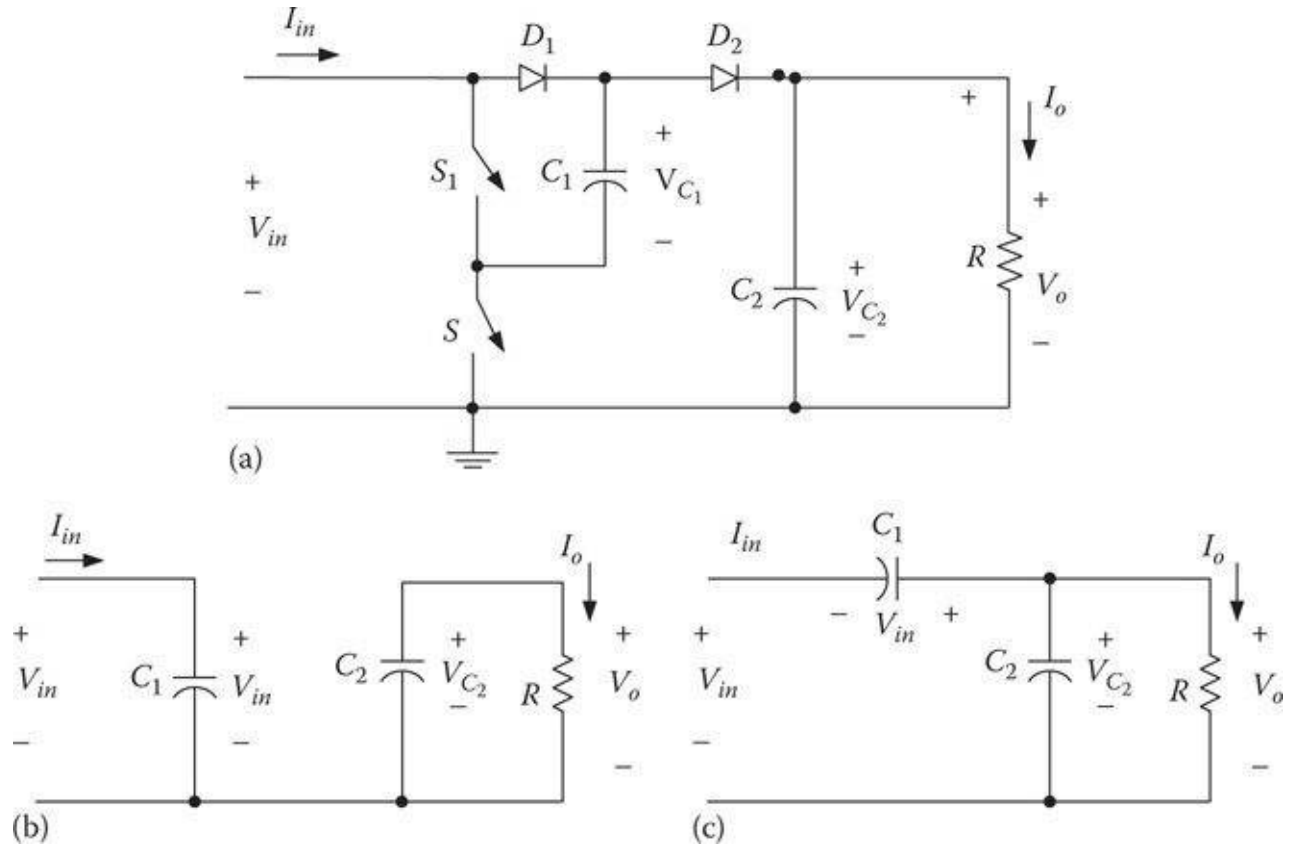


FIGURE 12.1
Elementary circuit of positive-output push-pull switched-capacitor Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 on).

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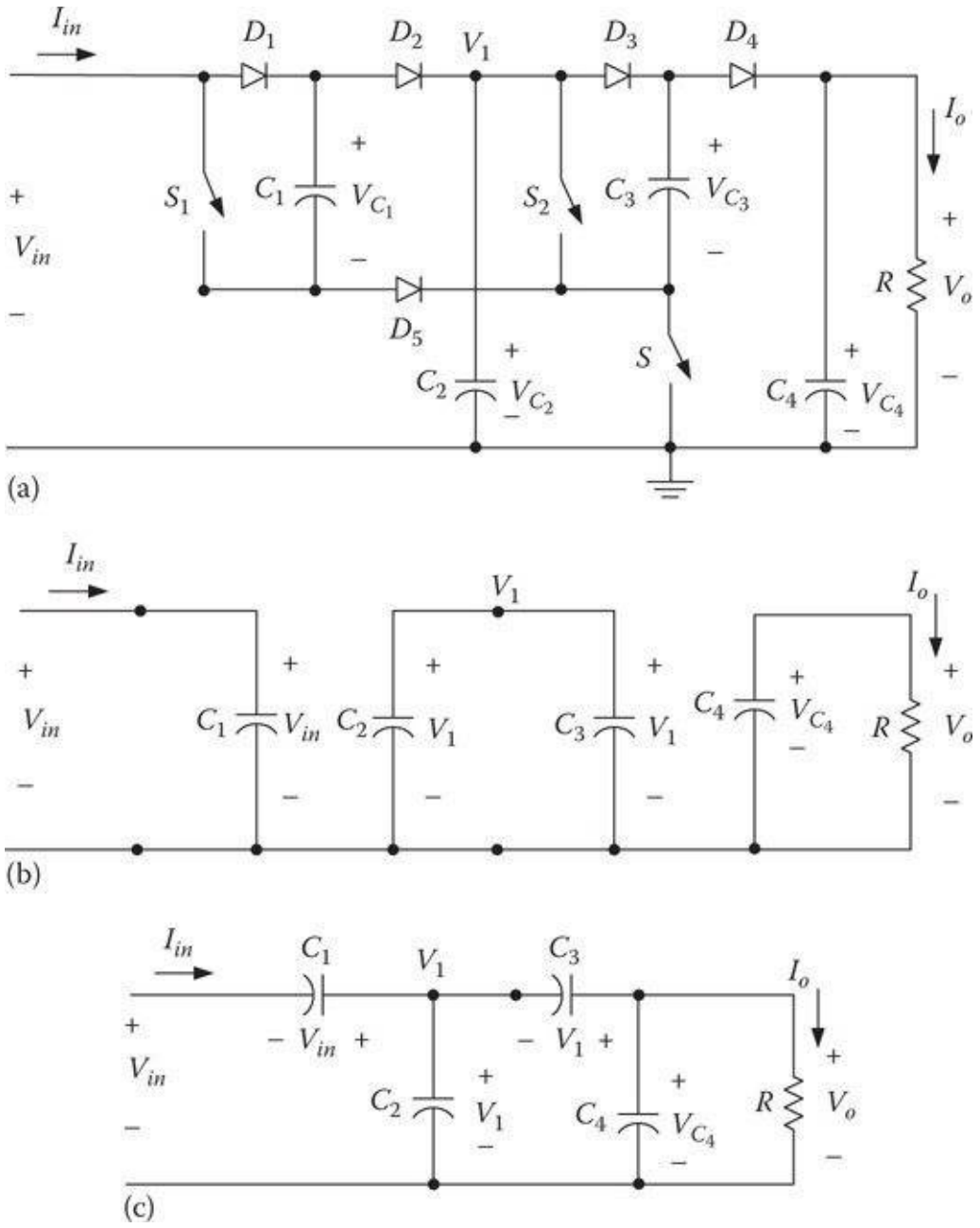


FIGURE 12.2
Re-lift push-pull switched-capacitor circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on *(S* on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

(S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} and voltage across capacitor C_3 is charged to V_1 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$ and voltage across capacitor C_4 is charged to $V_o = 2V_1 - \Delta V_2$ during switch-off. Therefore, the output voltage is

$$V_o = 2V_1 - \Delta V_2 = 4V_{in} - 2\Delta V_1 - \Delta V_2 \tag{12.3}$$

where ΔV_2 is set for the same reason as ΔV_1.

12.2.3 Triple-Lift Circuit

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The triple-lift circuit is derived from re-lift circuit by adding a parts-set: one more slave switch, two SCs, and three diodes (S_3−C_5−C_6−D_6−D_7−D_8). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.3. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_5 is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in}$, the voltage

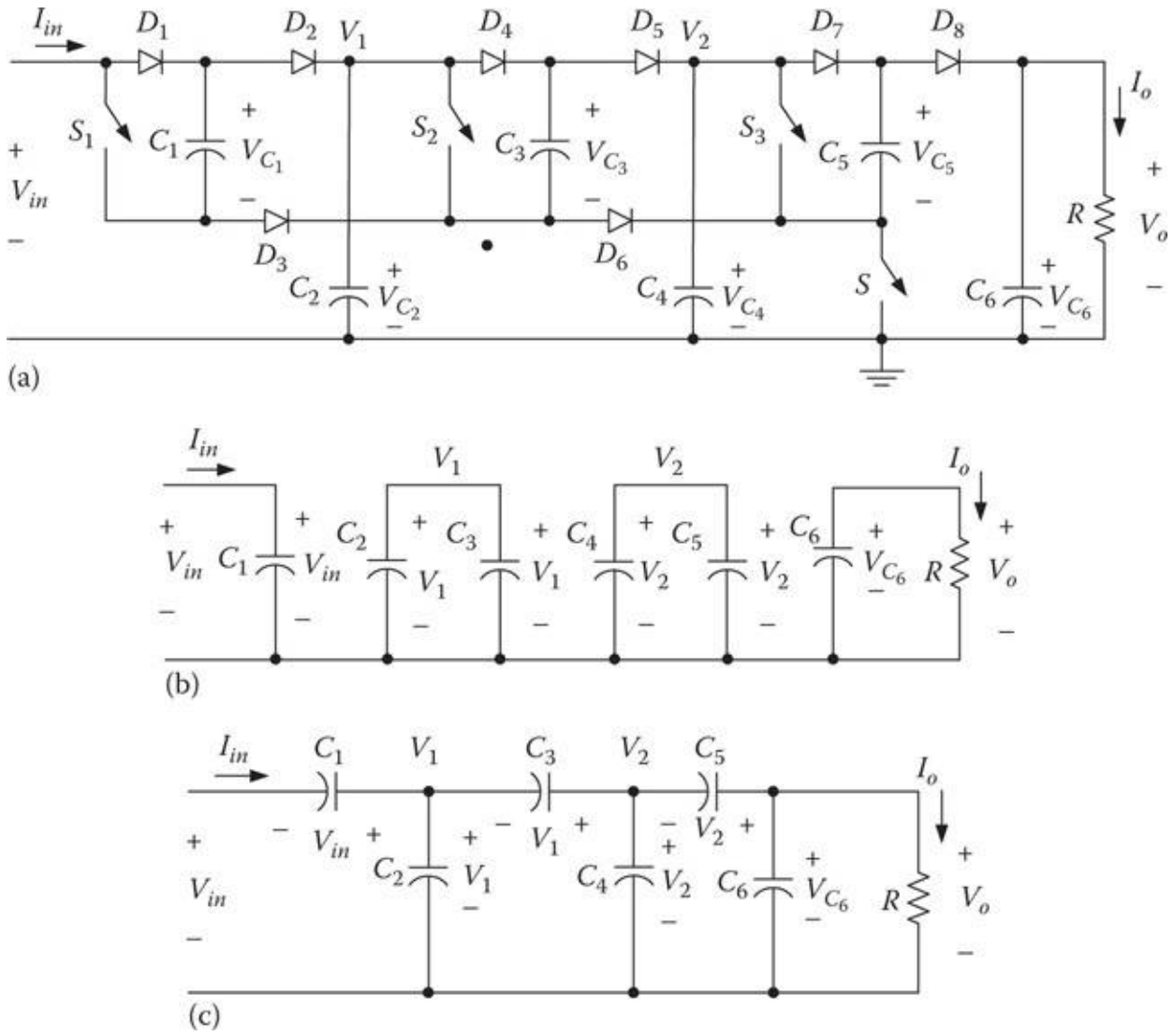


FIGURE 12.3
Triple-lift push-pull switched-capacitor circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_o = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = 2V_2 - \Delta V_3 = 4V_1 - 2\Delta V_2 - \Delta V_3 = 8V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3 \qquad (12.4)$$

where ΔV_3 is set for the same reason as ΔV_1.

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12.2.4 Higher-Order Lift Circuit

The higher-order lift circuit is designed by just multiple repeating of the parts mentioned in the previous sections. The output voltage of the nth-order lift circuit is

$$V_o = 2^n V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i} \tag{12.5}$$

12.3 Additional Series

The first three stages of the additional series are shown in Figures 12.4, 12.5, and 12.6. For the convenience of explaining, they are called elementary additional circuit, re-lift additional circuit, and triple-lift additional circuit, respectively, and are numbered as n = 1, 2, and 3.

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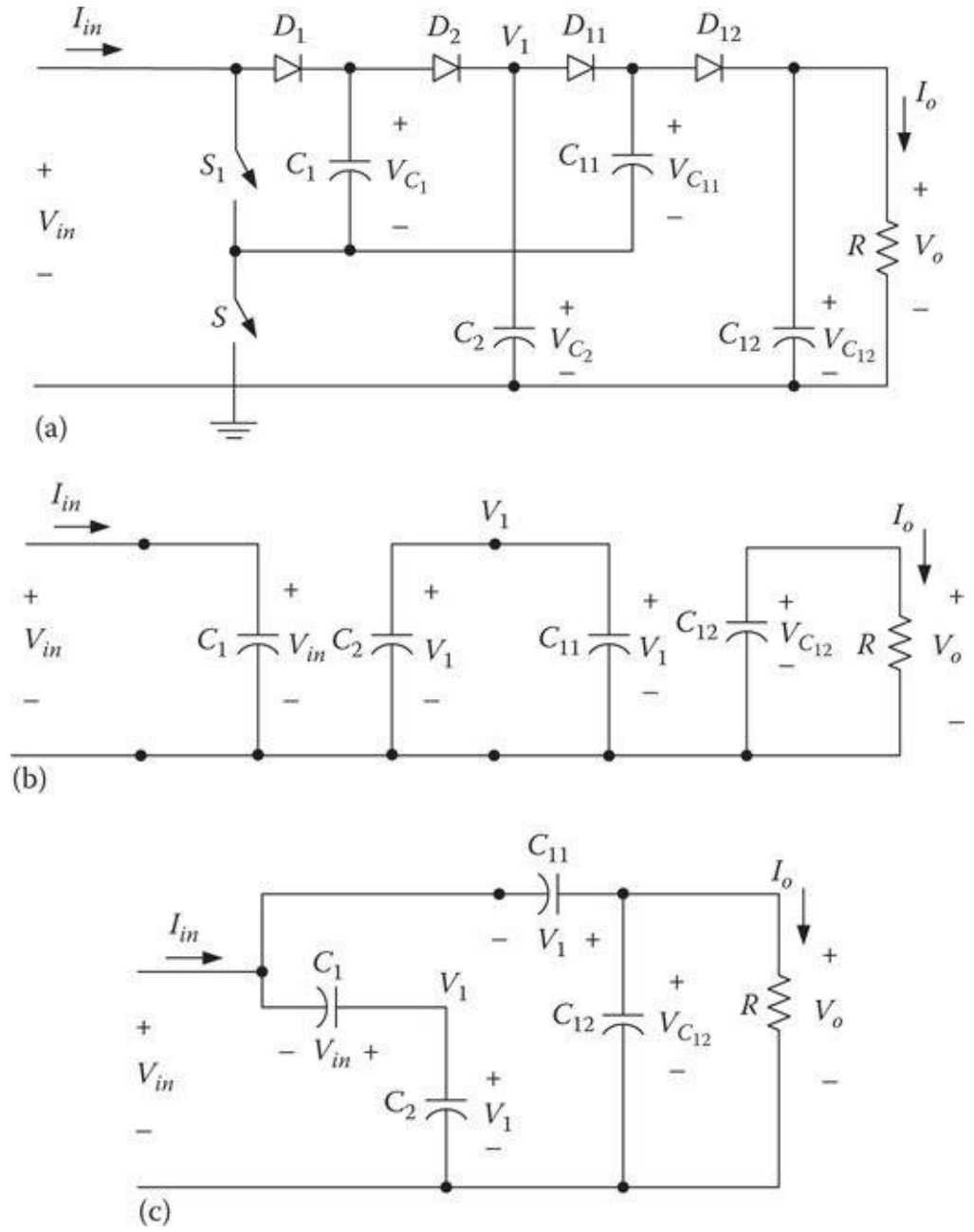


FIGURE 12.4
Elementary additional/enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 on).

12.3.1 Elementary Additional Circuit

The elementary additional circuit is derived from elementary circuit by adding a double/enhanced circuit (DEC). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.4. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_1 + V_{in} = 3V_{in} \tag{12.6}$$

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Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_0 (for additional output parts). The real output voltage is

$$V_o = 3V_{in} - \Delta V_1 - \Delta V_o \tag{12.7}$$

12.3.2 Re-Lift Additional Circuit

The re-lift additional circuit is derived from re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.5.

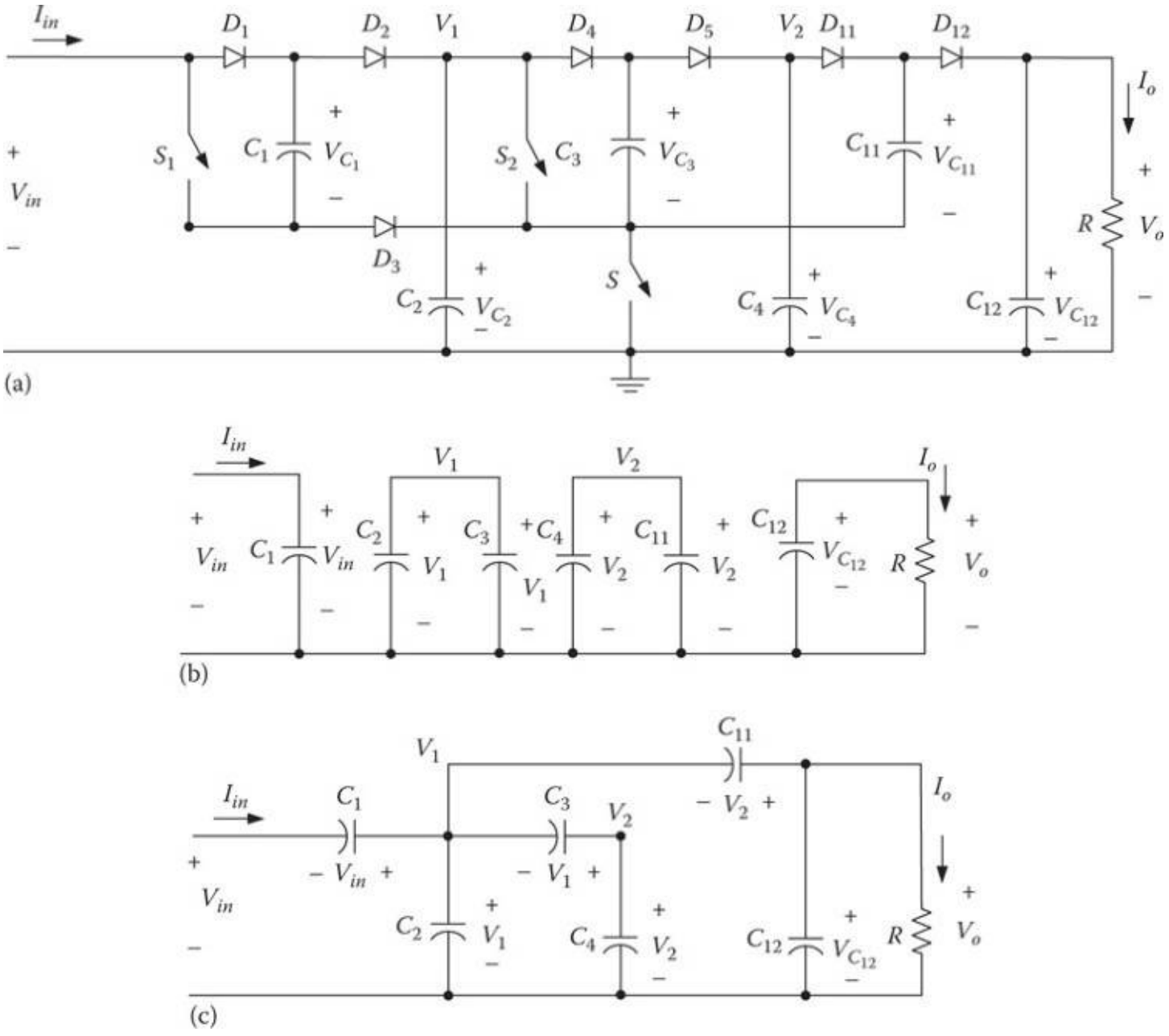


FIGURE 12.5
Re-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

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The switches S and (S_1 S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{12.8}$$

where ΔV_2 is set for the same reason as ΔV_1.

12.3.3 Triple-Lift Additional Circuit

The triple-lift additional circuit is derived from triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.6. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor

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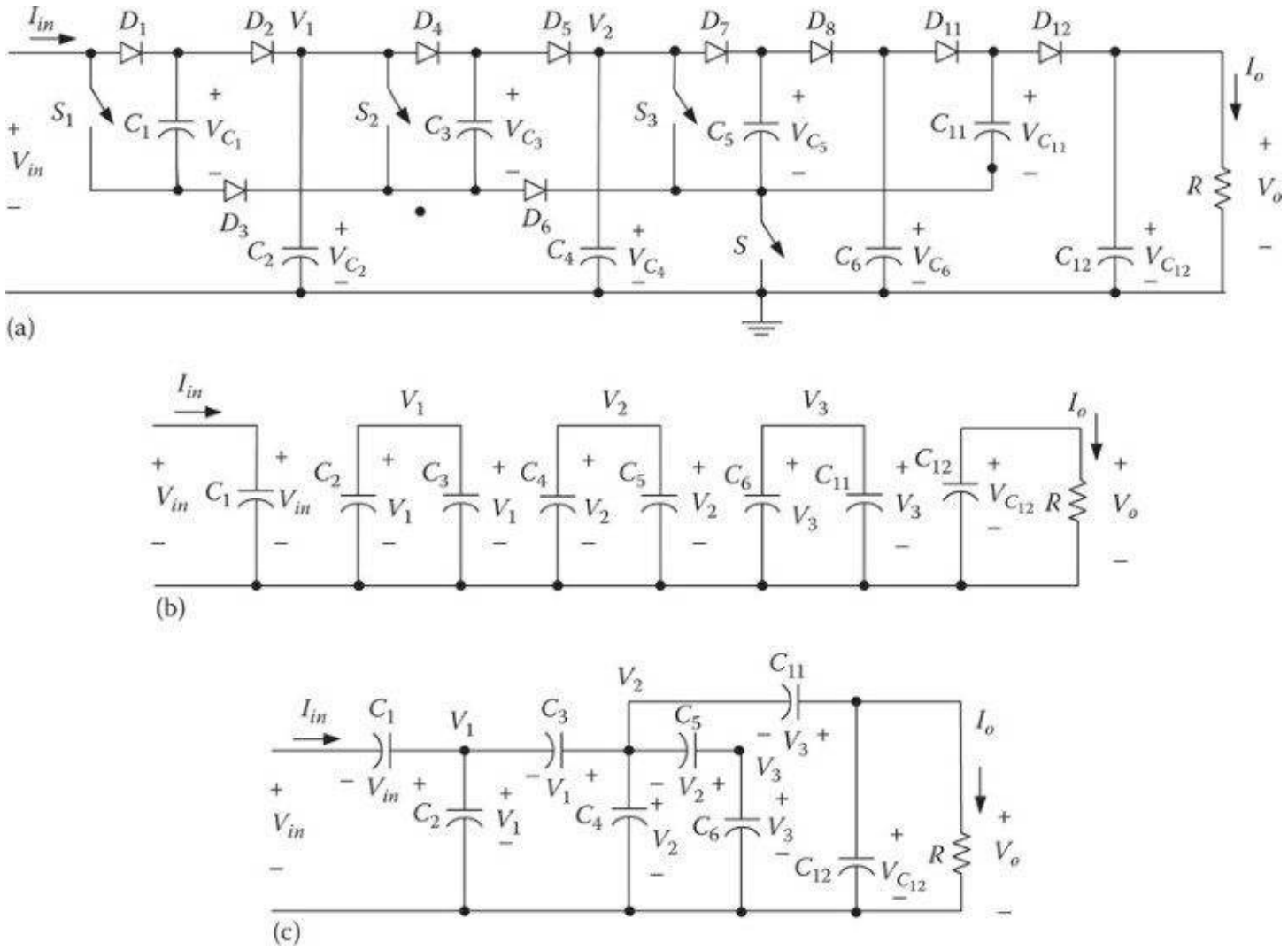


FIGURE 12.6
Triple-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{12.9}$$

where ΔV_3 is set for the same reason as ΔV_1.

12.3.4 Higher-Order Lift Additional Circuit

The higher-order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of nth-lift additional circuit is

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$$V_{o-m} = 1.5 \times \left(2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} \right) - \Delta V_n - \Delta V_o \tag{12.10}$$

12.4 Enhanced Series

The first three stages of the enhanced series are shown in Figures 12.4, 12.7, and 12.8, respectively. For the convenience of explaining, they are called elementary enhanced circuit, re-lift enhanced circuit, and triple-lift enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

12.4.1 Elementary Enhanced Circuit

The elementary enhanced circuit is derived from elementary circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.4. The output voltage is

$$V_o = V_1 + V_{in} = 3V_{in} \tag{12.6}$$

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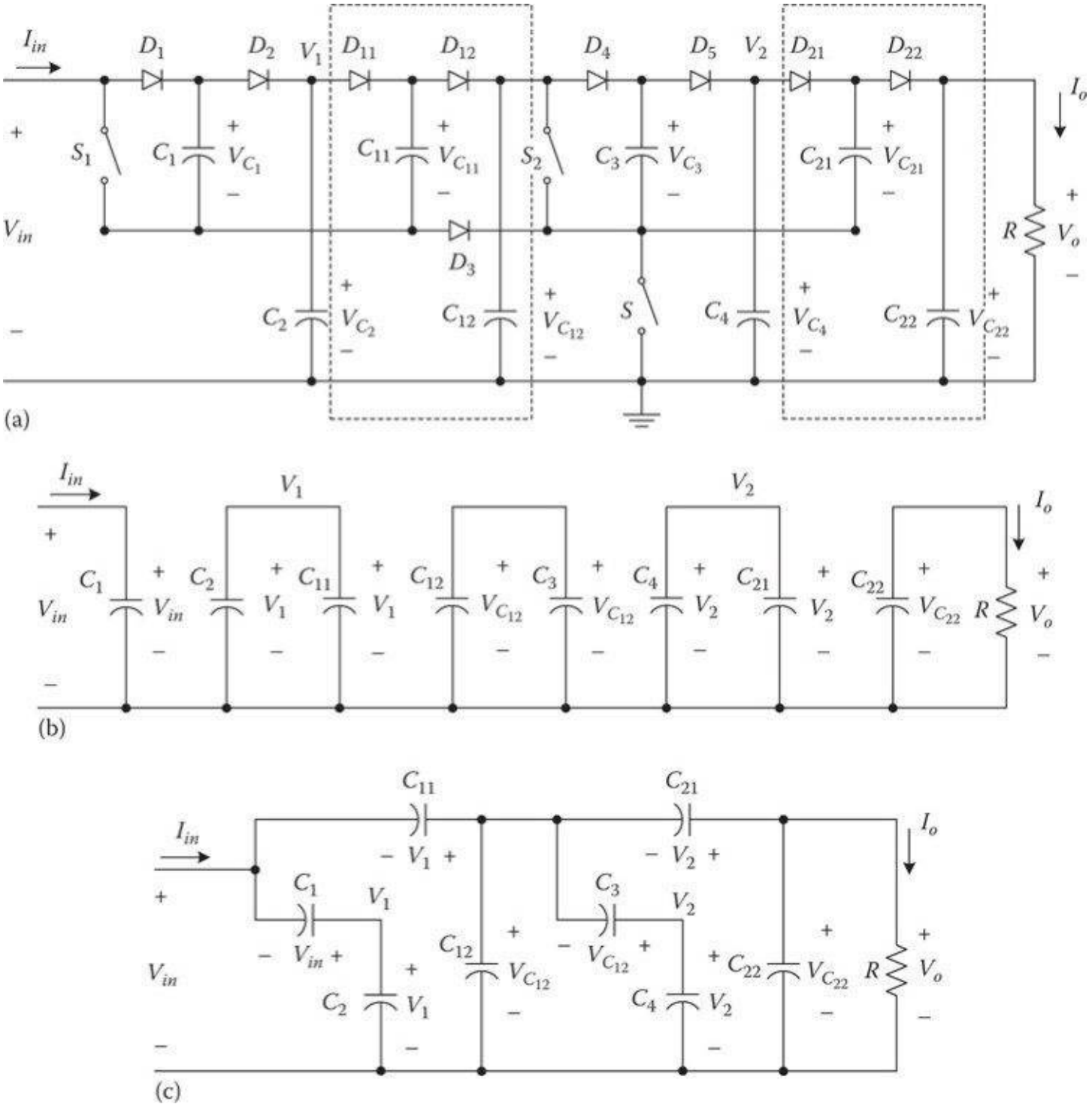


FIGURE 12.7
Re-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

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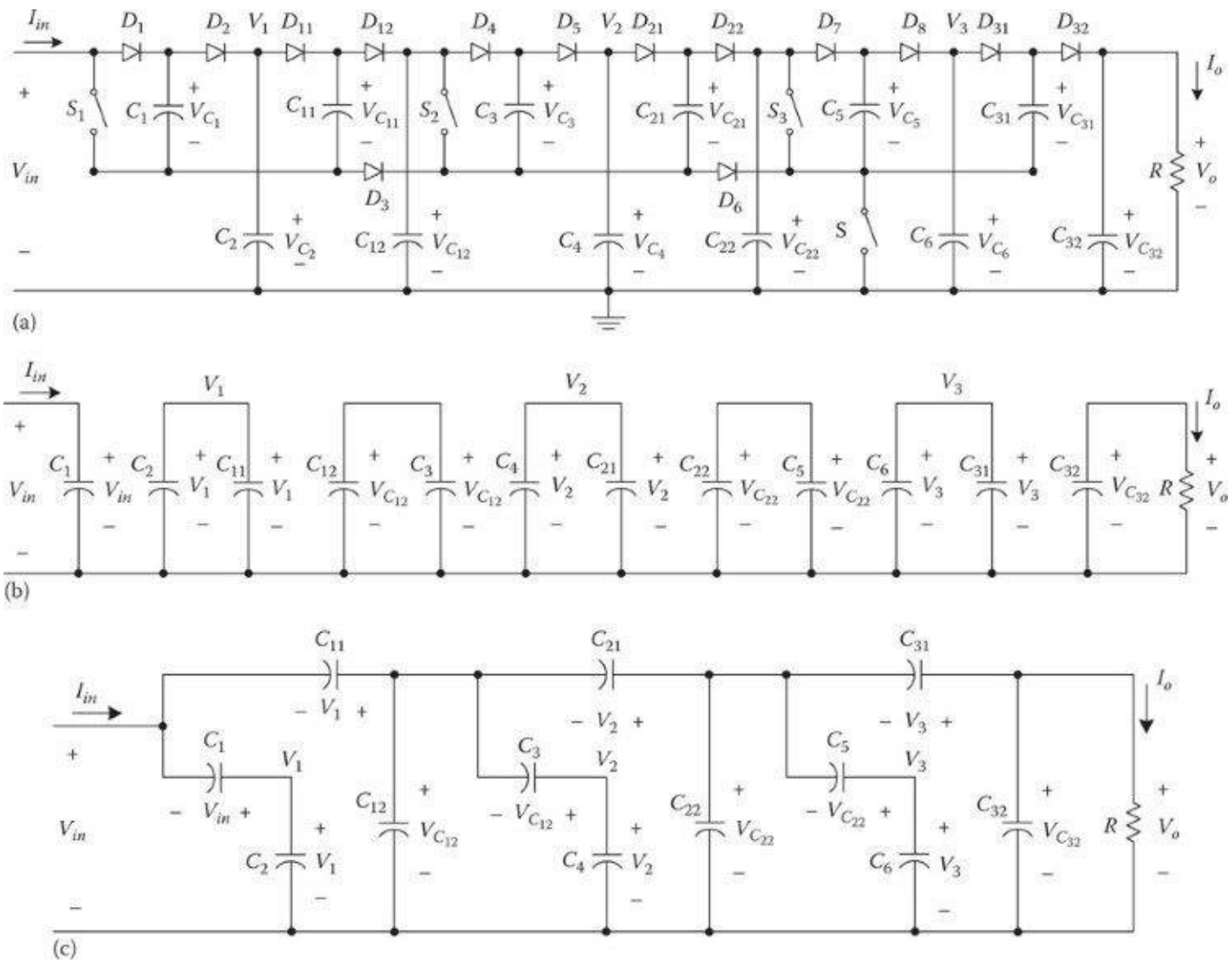


FIGURE 12.8
Triple-lift enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on (*S* on), (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_o (for additional output parts). The real output voltage is

$$V_o = 3V_{in} - \Delta V_1 - \Delta V_o \tag{12.7}$$

12.4.2 Re-Lift Enhanced Circuit

The re-lift enhanced circuit is derived from re-lift circuit by adding a DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.7. The switches *S* and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 -$

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ΔV_2, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o = 9V_{in} - 6\Delta V_1 - 2\Delta V_2 - \Delta V_o \tag{12.11}$$

where ΔV_2 is set for the same reason as ΔV_1.

12.4.3 Triple-Lift Enhanced Circuit

The triple-lift enhanced circuit is derived from re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.8. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o = 27V_{in} - 18\Delta V_1 - 6\Delta V_2 - 2\Delta V_3 - \Delta V_o \tag{12.12}$$

where ΔV_3 is set for the same reason as ΔV_1.

12.4.4 Higher-Order Enhanced Lift Circuit

The higher-order enhanced lift circuit is derived from the corresponding circuit of the main series circuit by adding the DEC in each stage circuit. The output voltage of the *n*th-order lift enhanced circuit is

$$V_o = 1.5 \times \left(2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} \right) - \Delta V_n - \Delta V_o \tag{12.13}$$

12.5 Re-Enhanced Series

The first three stages of the re-enhanced series are shown in Figures 12.9, 12.10 and 12.11. For the convenience of explaining, they are called elementary re-enhanced circuit, relift re-enhanced circuit, and triple-lift re-enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

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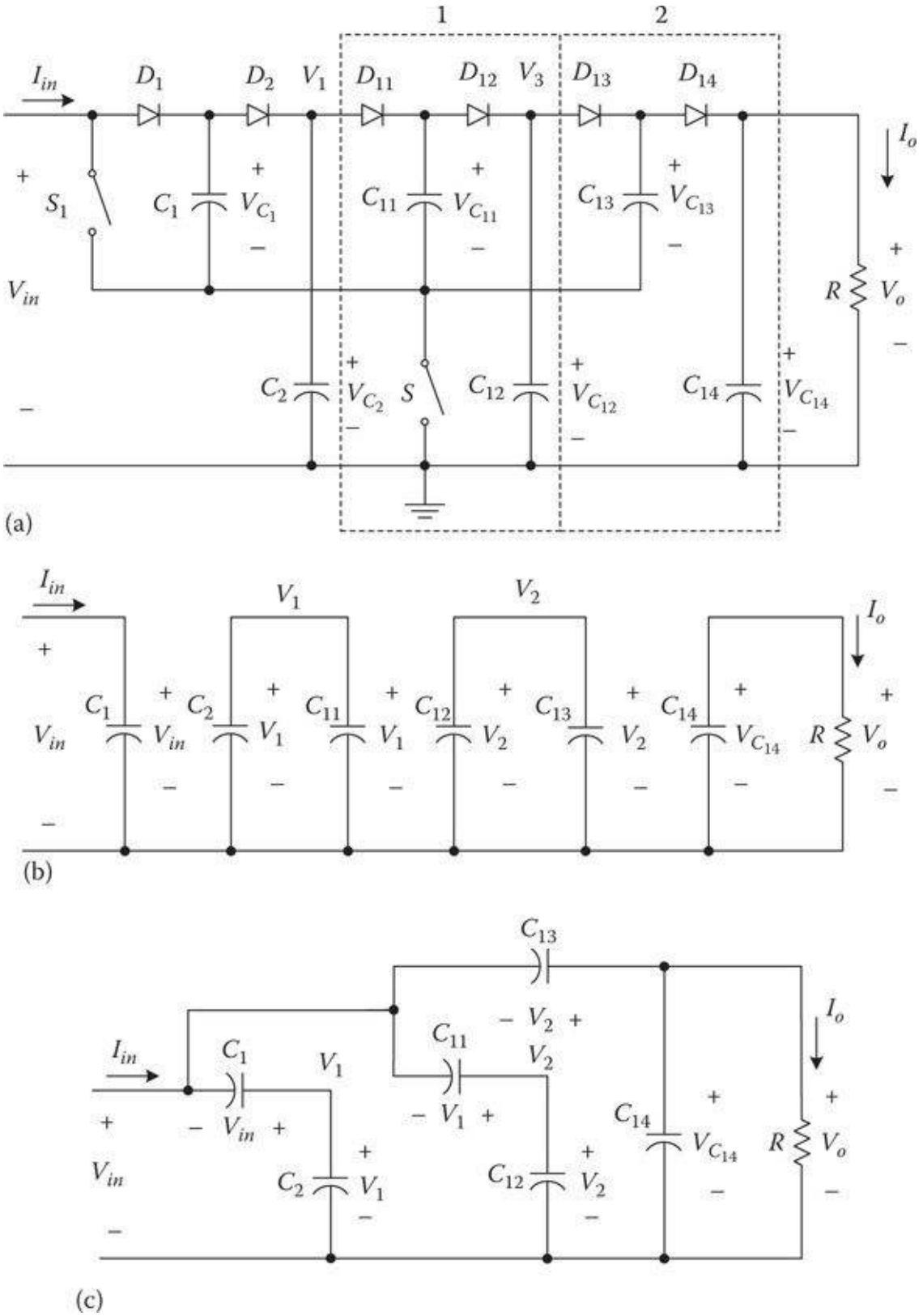


FIGURE 12.9
Elementary re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 on).

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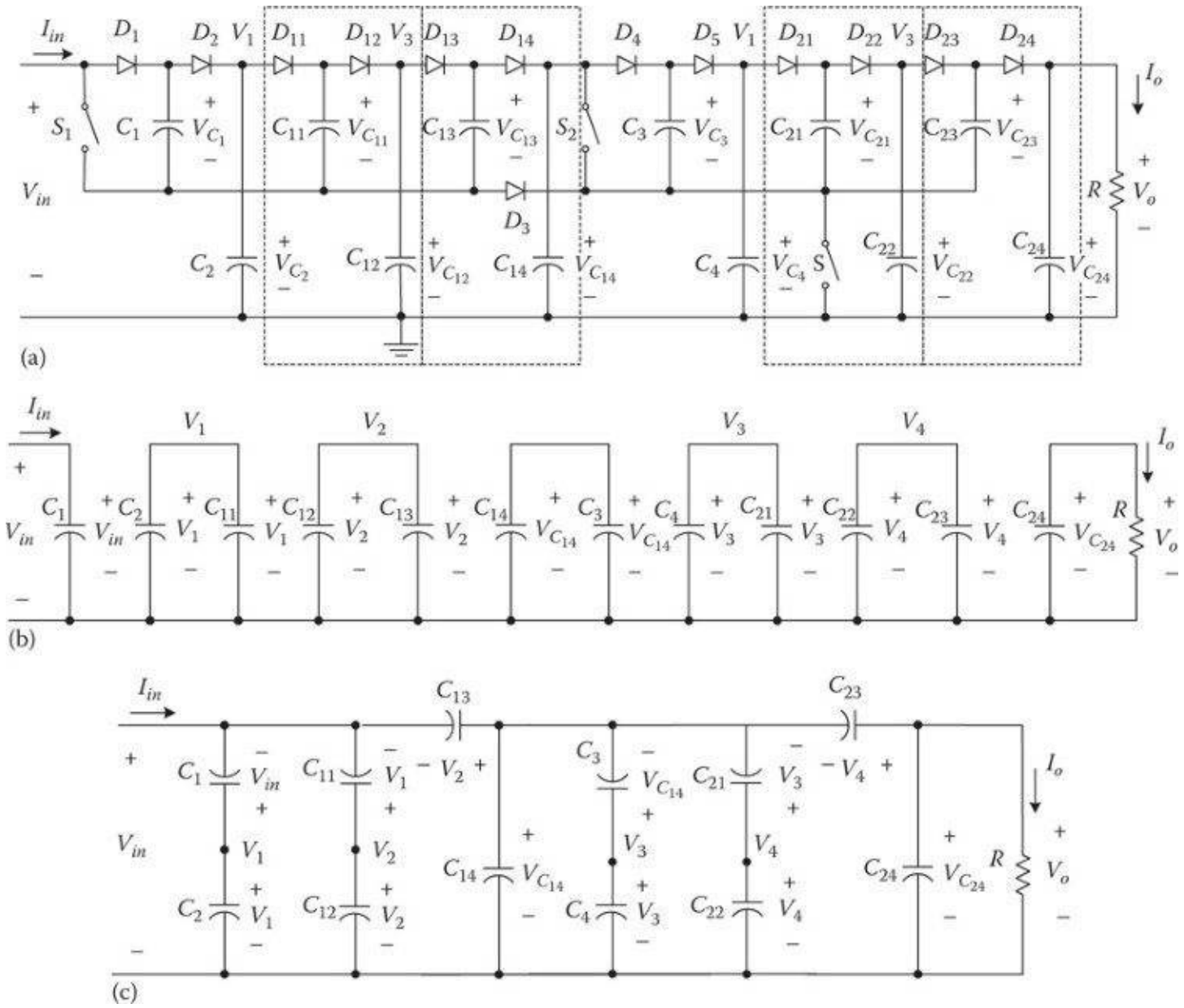


FIGURE 12.10
Re-lift re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

12.5.1 Elementary Re-Enhanced Circuit

The elementary re-enhanced circuit is derived from elementary circuit by adding the DEC twice. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.9. Two switches *S* and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_1 + V_{in} = 4V_{in} \tag{12.14}$$

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Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_0 (for additional output parts). The real output voltage is

$$V_o = 4V_{in} - \Delta V_1 - \Delta V_o \tag{12.15}$$

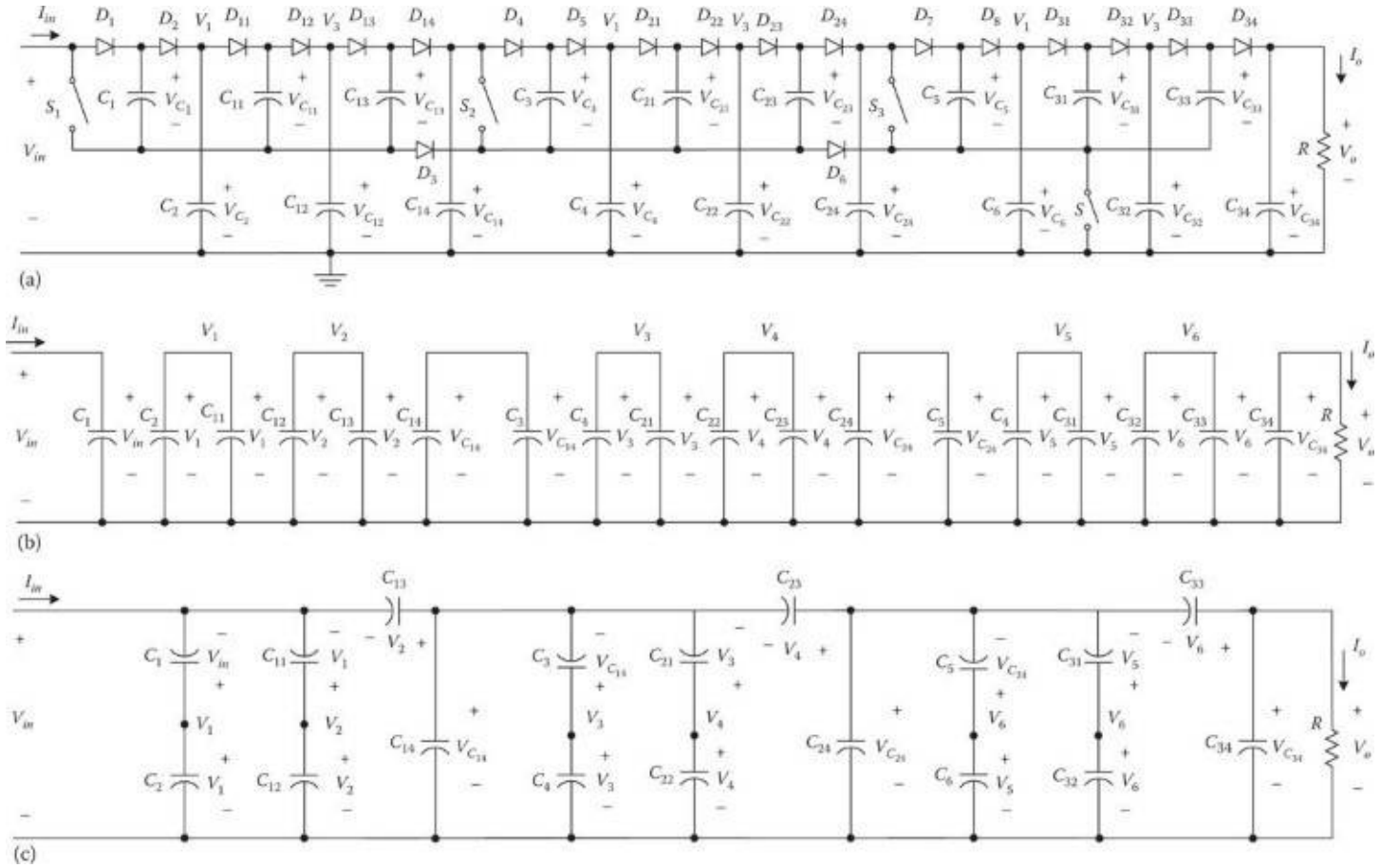


FIGURE 12.11
Triple-lift re-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on (*S* on), (c) Equivalent circuit during switch-off (S_1, S_2) and S_3 on).

12.5.2 Re-Lift Re-Enhanced Circuit

The re-lift re-enhanced circuit is derived from re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch- off are shown in Figure 12.10. The switches *S* and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$ the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{12.16}$$

where ΔV_2 is set for the same reason as ΔV_1.

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12.5.3 Triple-Lift Re-Enhanced Circuit

The triple-lift re-enhanced circuit is derived from triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.11. The switches S and (S_1, S_2, S_3) operate in push- pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{12.17}$$

where ΔV_3 is set for the same reason as ΔV_1.

12.5.4 Higher-Order Lift Re-Enhanced Circuit

The higher-order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the nth-lift re-enhanced circuit is

$$V_o = (1.5\times 2)^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} - \Delta V_m - \Delta V_o \tag{12.18}$$

12.6 Multiple-Enhanced Series

The first three stages of the multiple-enhanced series are shown in Figures 12.12, 12.13 and 12.14. For the convenience of explaining, they are called elementary multiple-enhanced circuit, re-lift multiple-enhanced circuit, and triple-lift multiple-enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

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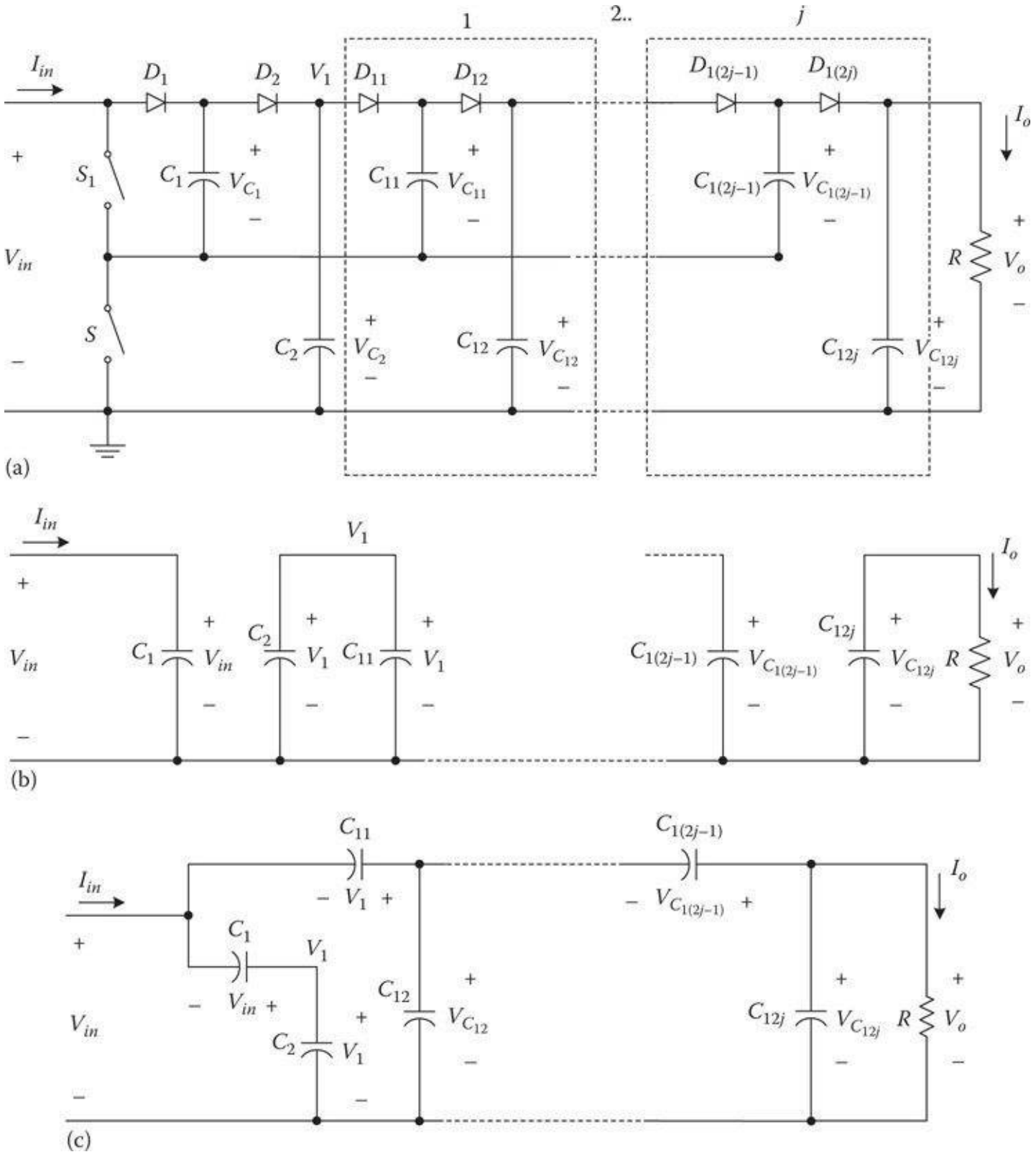


FIGURE 12.12
Elementary multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 on).

12.6.1 Elementary Multiple-Enhanced Circuit

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The elementary multiple-enhanced circuit is derived from elementary circuit by adding the DEC multiple (j) times. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.12. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_1 + V_{in} = (1 + j)V_{in} \tag{12.19}$$

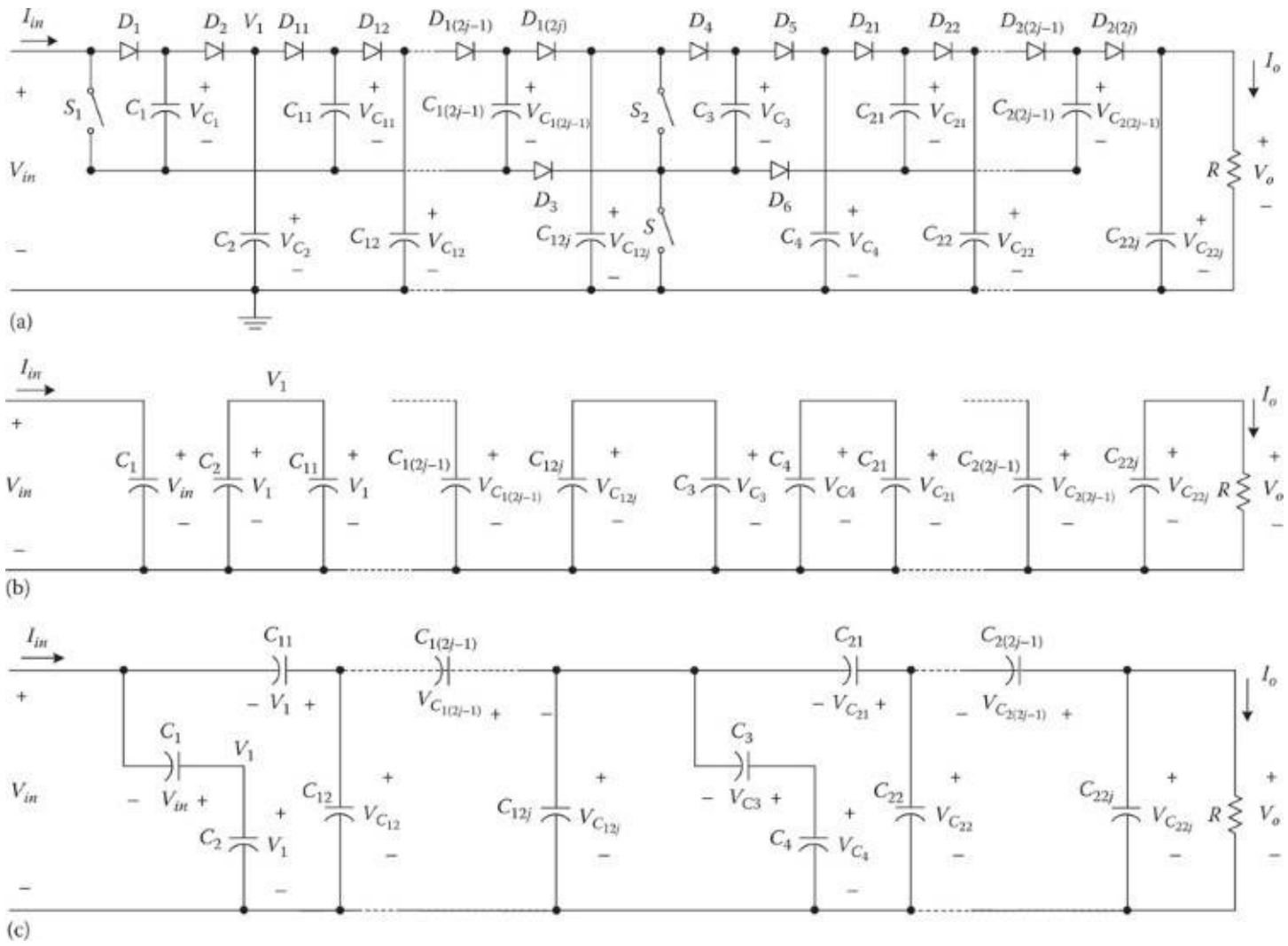


FIGURE 12.13
Re-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on (S on), (c) Equivalent circuit during switch-off (S_1 and S_2 on).

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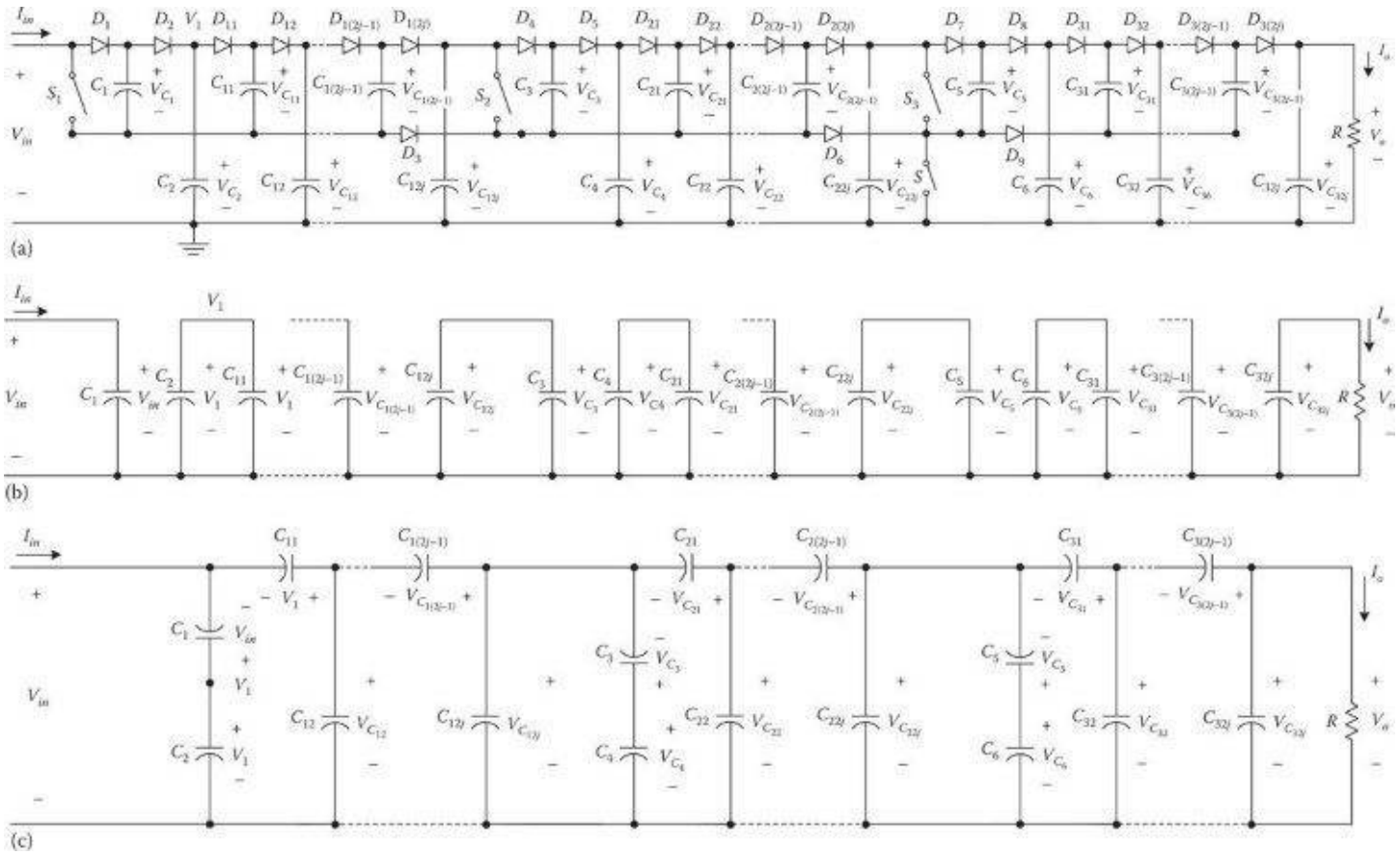


FIGURE 12.14
Triple-lift multiple-enhanced circuit, (a) Circuit diagram, (b) Equivalent circuit during switch-on (S on), (c) Equivalent circuit during switch-off (S_1 S_2) and S_3 on).

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_o (for additional output parts). The real output voltage is

$$V_o = (1+j)V_{in} - \Delta V_1 - \Delta V_o \tag{12.20}$$

12.6.2 Re-Lift Multiple-Enhanced Circuit

The re-lift multiple-enhanced circuit is derived from re-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.13. The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch- on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o = 6V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{12.21}$$

where ΔV_2 is set for the same reason as ΔV_1.

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12.6.3 Triple-Lift Multiple-Enhanced Circuit

The triple-lift multiple-enhanced circuit is derived from triple-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 12.14. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o = 12V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{12.22}$$

where ΔV_3 is set for the same reason as ΔV_1.

12.6.4 Higher-Order Lift Multiple-Enhanced Circuit

The higher-order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple (j) times in each stage circuit. The output voltage of the nth-lift multiple-enhanced circuit is

$$V_o = 1.5\times\left(2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i}\right) - \Delta V_n - \Delta V_o \tag{12.23}$$

12.7 Theoretical Analysis

The maximum output current is a key parameter of the DC–DC converter. The output voltage of DC-DC step-up converter can be shown as

$$V_o = \frac{k_s V_{in} - k_d V_d}{1 + (T/R)\sum_{i=1}^{m+1}(n_i/C_i)[1 - e^{-kTn_i/R_iC_i}]\prod_{j=1}^{m+1} n_j^2} \tag{12.24}$$

where

$$k_s = \frac{1 + \sum_{i=1}^{m+1}\prod_{j=1}^{i} n_j}{\prod_{i=1}^{m+1} n_i}$$

and

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$$k_d = \sum_{i=1}^{m+1} \frac{n_i(n_i+1)}{\prod_{j=1}^{m+1} n_j}$$

In Equation 12.24, m and n are the step number of the converter and the number of the serial-parallel capacitor network, respectively. T and k are the switch period and the duty-cycle ratio in the state 1, respectively. For the three-lift circuit, $m = 1$, $n_1 = n_2 = 1$, and $f = 1/T$, we can write Equation 12.24 as follows:

$$V_o = \frac{3V_{in} - 4V_d}{1 + \frac{1}{fR}\left(\frac{1/C_2}{1 - e^{-\frac{1}{2fR_2C_2}}} + \frac{1/C_1}{1 - e^{-\frac{1}{2fR_1C_1}}}\right)} \tag{12.25}$$

Since $I_o = V_o/R$, we can write the output current of this three-lift circuit as follows:

$$I_o = \frac{3V_{in} - 4V_d - V_o}{\frac{1/C_2}{1 - e^{-\frac{1}{2fR_2C_2}}} + \frac{1/C_1}{1 - e^{-\frac{1}{2fR_1C_1}}}} f \tag{12.26}$$

where

V_{in} is the source voltage assuming 10 V

V_o is the output voltage assuming 21.6 V

V_d is the voltage drop across diode R_i, which corresponds to the wire resistor of capacitor Ci

In order to increase the output current of the converter, we selected Schottky barrier diode (V_d = 0.4 V), and then

$$3V_{in} - 4V_d - V_o = 6.8 \text{ V} \tag{12.27}$$

For getting the maximum output current, $C_1 = C_2 = C$ have to be chosen. In addition, we assumed $R_1 = R_2 = R$. Therefore, the description of the output current can be simplified as

$$I_o = 0.9fC\,[1 - \exp(-1/2RfC)] \tag{12.28}$$

Figure 12.15 shows the relationship among output current I_o, operation frequency f, and capacitance C on the basis of the equation. From the result, the following can be concluded:

1. Higher frequency can result in bigger output current, especially the capacitance of C if the serial-parallel capacitors are not elevated for integration.
2. For a certain capacitor, there is a maximum frequency restriction, and it reduces when the capacitance is raised.

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3. The output current can be up to 1 A if the operation frequency f of the converter and the capacitance C of the serial–parallel capacitors are suitably chosen.

In addition, it can be shown from the equation deducing that the maximum ratio P_o/C can be obtained by using the same capacitance of the serial-parallel capacitors in the structure. The theoretical analysis for the higher-order lift circuits is similar to the previously given description.

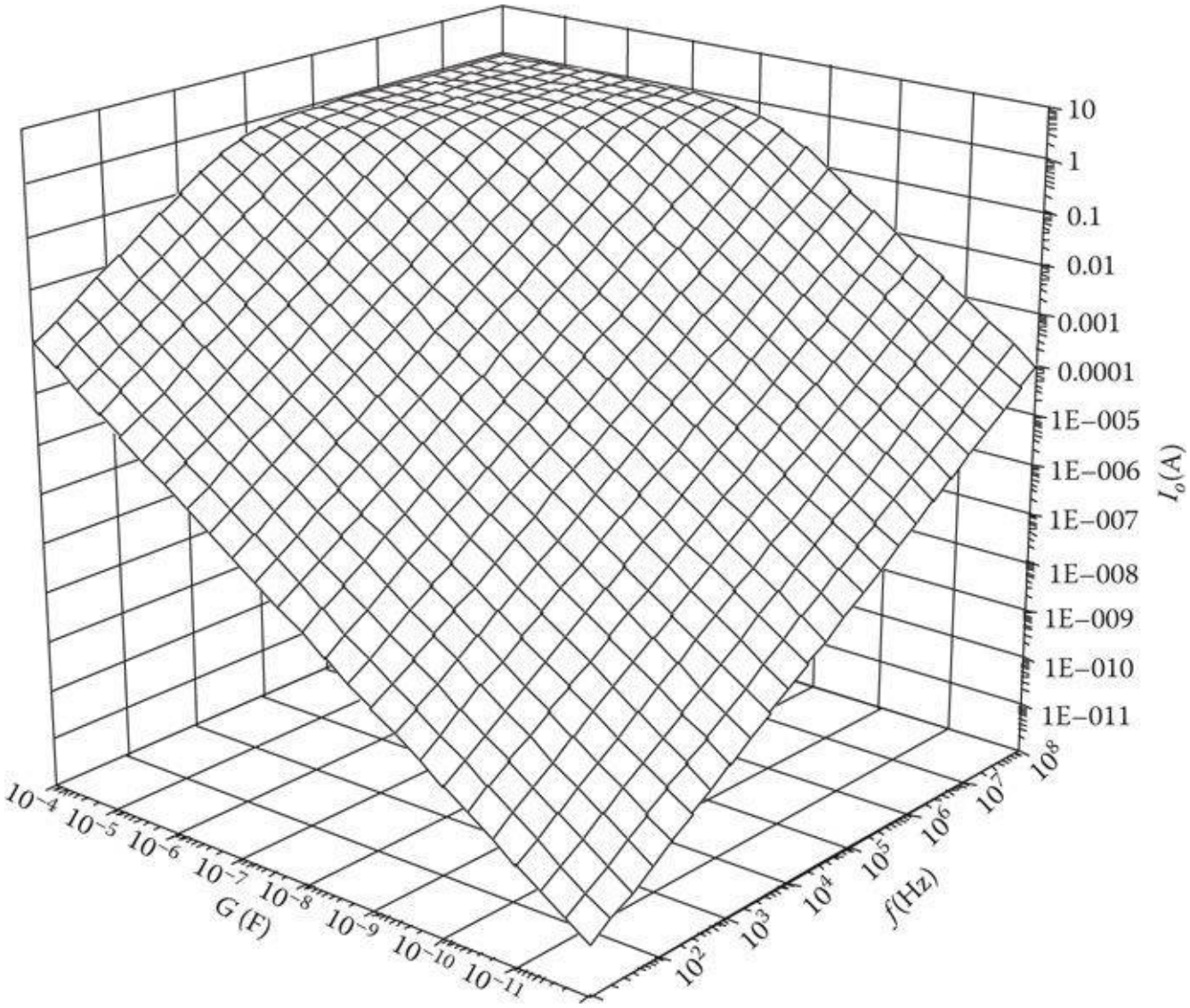


FIGURE 12.15
Relationship among output current I_o, operation frequency f, and capacitance C.

12.8 Summary of This Technique

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Using this technique, it is easy to design the higher-order lift circuit to obtain high output voltage. All these converters can be sorted in several subseries: main series, additional series, enhanced series, re-enhanced series, and multiple-enhanced series. The output voltage of the *n*th-lift circuit is

$$V_o = \begin{cases} 2^m V_{in} - \sum_{i=0}^{m-1} 2^i \Delta V_{m-i} & \text{Main series} \\ 1.5 * \left(2^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} \right) - \Delta V_m - \Delta V_o & \text{Additional series} \\ \left(3^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} \right) - \Delta V_m - \Delta V_o & \text{Enhanced series} \\ \left(4^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} \right) - \Delta V_m - \Delta V_o & \text{Reenhanced series} \\ \left[(j+2)^m V_{in} - \sum_{i=1}^{m-1} 2^i \Delta V_{m-i} \right] - \Delta V_m - \Delta V_o & \text{Multiple-enhanced series} \end{cases} \quad (12.29)$$

From this formula, the family tree of positive-output multiple-lift push-pull SC Luo-converters is shown in Figure 12.16.

12.9 Simulation Results

To verify the design and calculation results, the PSpice simulation package was applied to these circuits. Choose V_{in} = 10 V, all capacitors C_i = 2 μF, R = 60 Ω, k = 0.5, and f = 100 kHz, we obtain the current and voltage values in the following converters.

12.9.1 Triple-Lift Circuit

Assume that the voltage drops ΔV_1, ΔV_2, and ΔV_3 are about 4.2 V, the current waveforms of I_{D2}, I_{D5}, and I_{D8}, then voltage values of V_1, V_2, and V_o are 15.7, 27.2, and 50.7 V. The simulation results (current and voltage values) in Figure 12.17 are identically matched with the calculated results.

12.9.2 Triple-Lift Additional Circuit

Assume that the voltage drops ΔV_1, ΔV_2, ΔV_3, and ΔV_o are about 4.2 V, the current waveforms of I_{D2}, I_{D5}, I_{D8}, and I_{D2}, and then voltage values of V_1, V_2, V_3, and V_o are 15.8, 27.5, 50.8, and

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74.8 V. The simulation results (current and voltage values) shown in Figure 12.18 are identically matched with the calculated results.

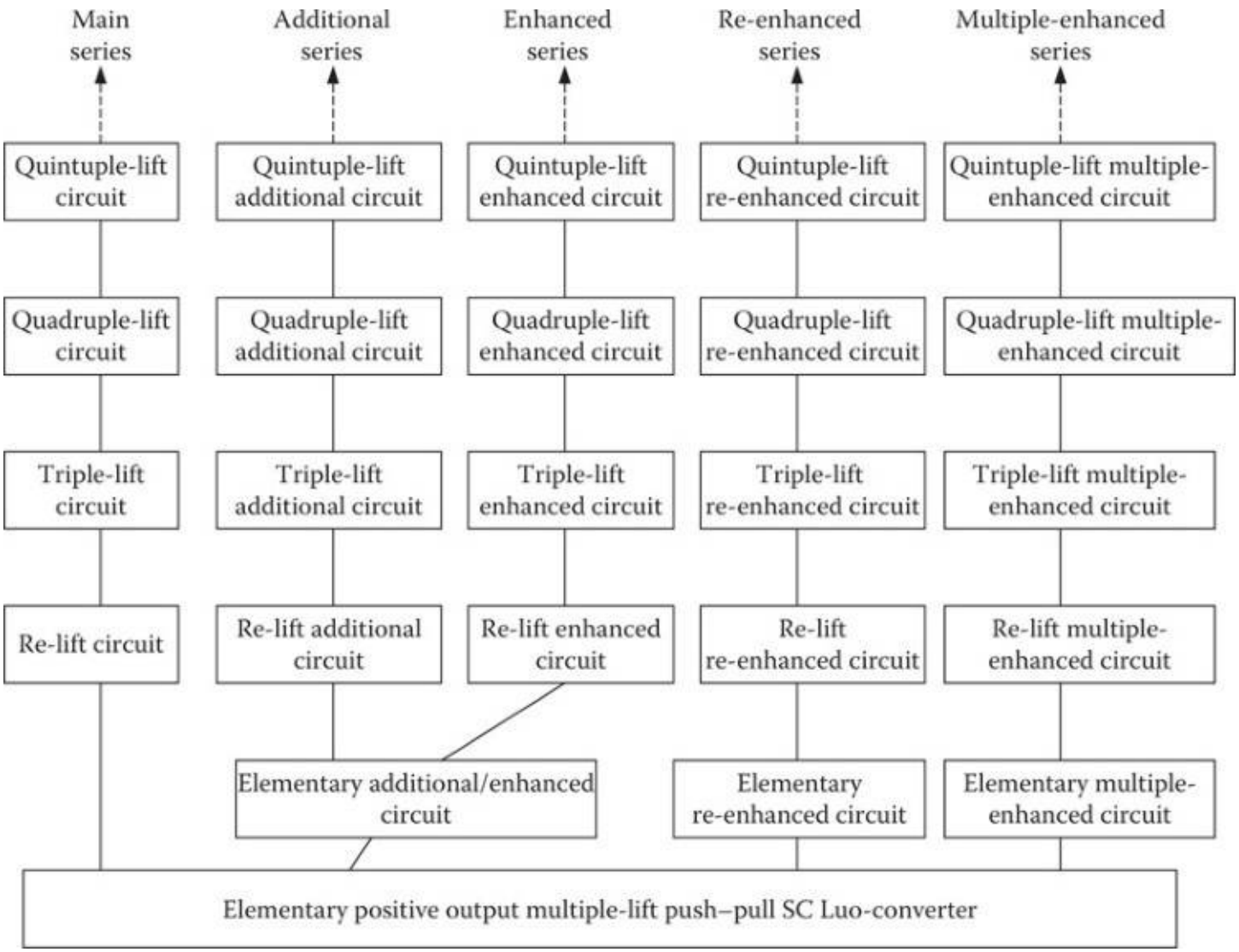


FIGURE 12.16
The family tree of multiple-lift push-pull switched-capacitor Luo-converters.

12.10 Experimental Result

A test rig was constructed to verify the design and calculation results and was compared with PSpice simulation results. With V_{in} = 10 V, all capacitors C_i = 2 μF, R = 60 k, k = 0.5, and f = 100 kHz, we measured the output voltage and the first diode current values in following converters.

12.10.1 Triple-Lift Circuit

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After careful measurement, we obtained the current waveform of I_{D2} (shown in Channel 1 with 5 A/Div in Figure 12.19) and voltage value of V_o of 50.8 V (shown in Channel 2 with 20 V/Div). The experimental results (current and voltage values) in Figure 12.17 are identically matched with the calculated and simulation results.

12.10.2 Triple-Lift Additional Circuit

The experimental results (voltage and current values) are identically matched with the calculated and simulation results, as shown in Figure 12.20. The current waveform of I_{D2} (shown in Channel 1 with 5 A/Div) and voltage value of V_o of 75 V (shown in Channel 2 with 20 V/Div) are obtained.

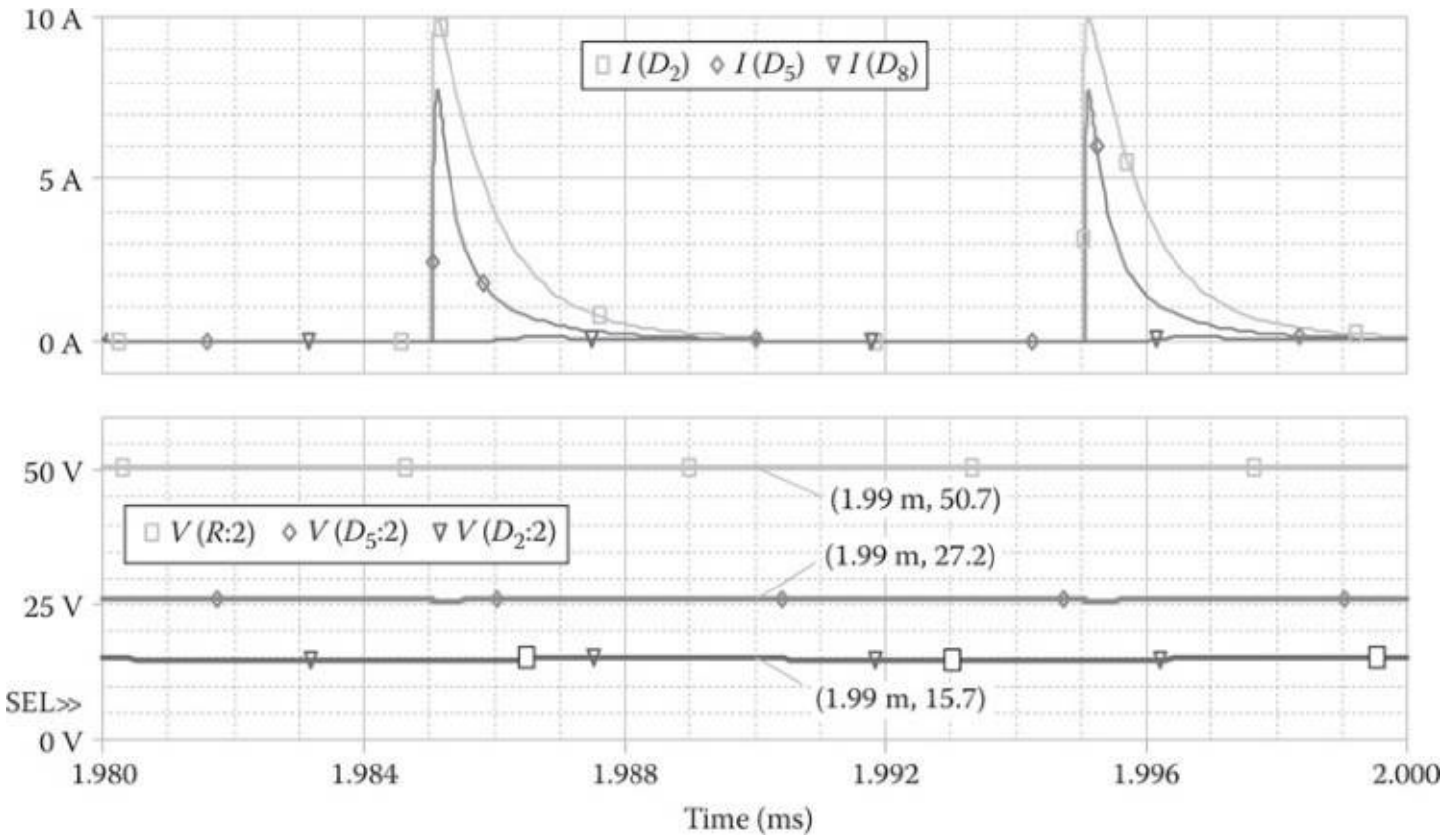


FIGURE 12.17
The simulation result of a triple-lift circuit at condition k = 0.5 and f = 100 kHz.

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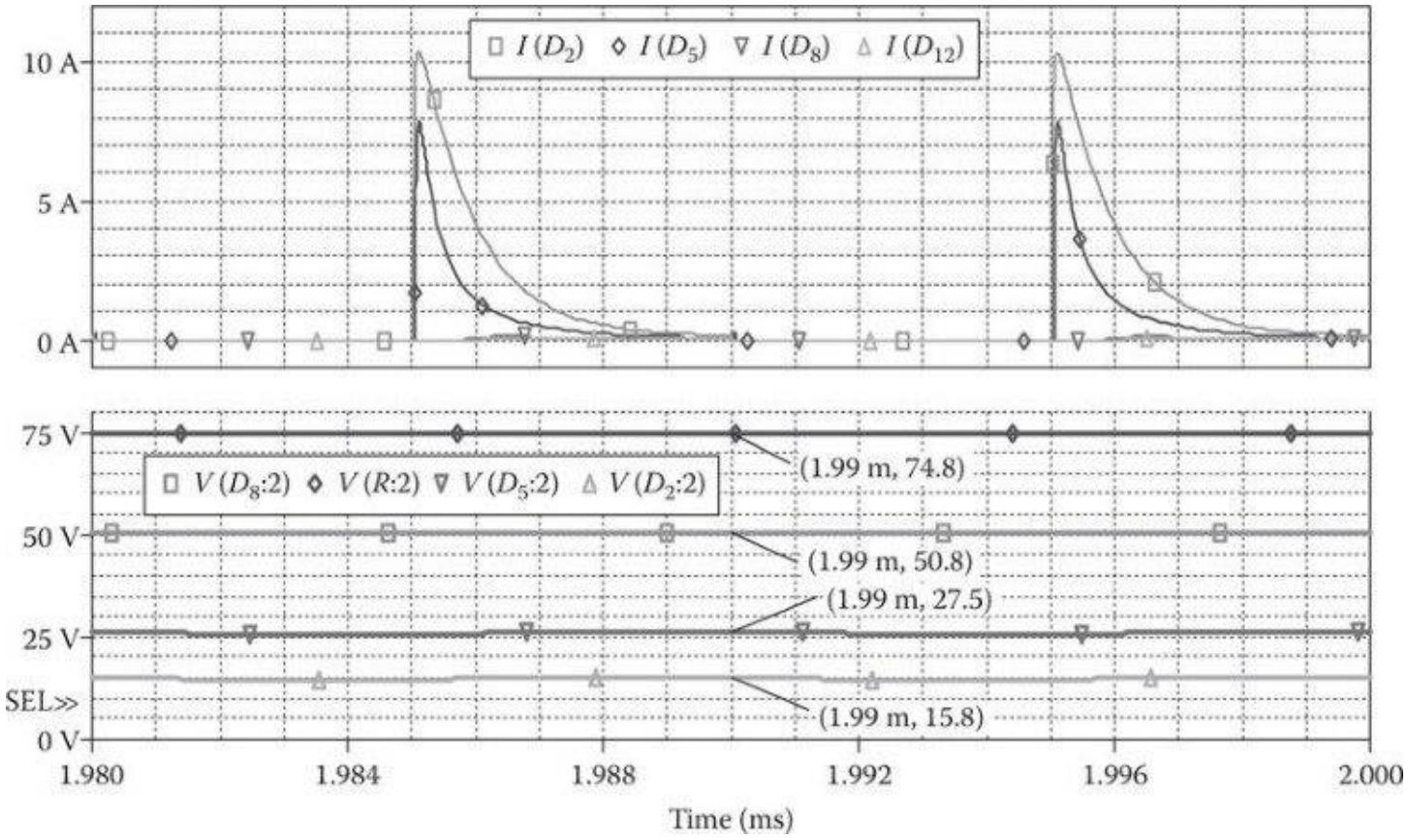


FIGURE 12.18
The simulation result of a triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

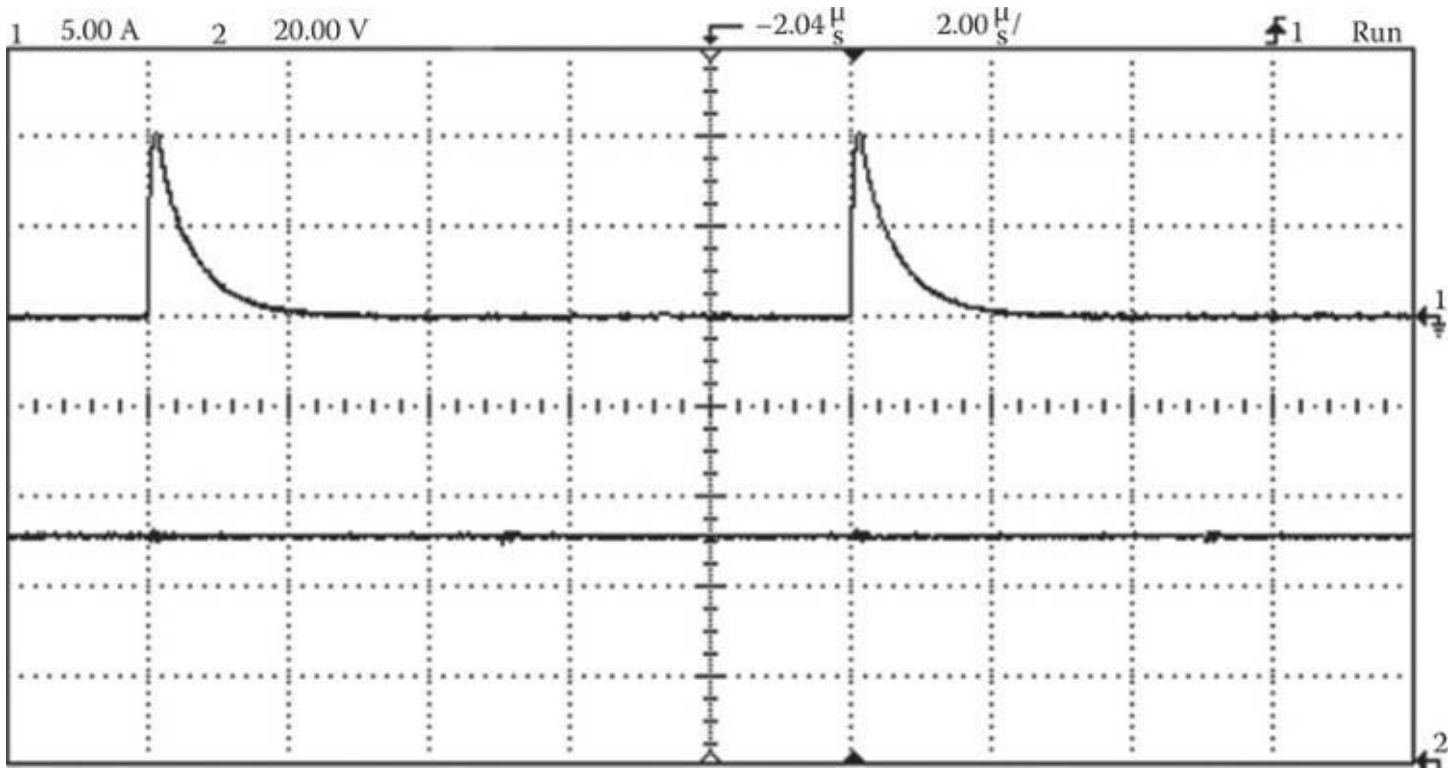


FIGURE 12.19
The experimental result of a triple-lift circuit at condition $k = 0.5$ and $f = 100$ kHz.

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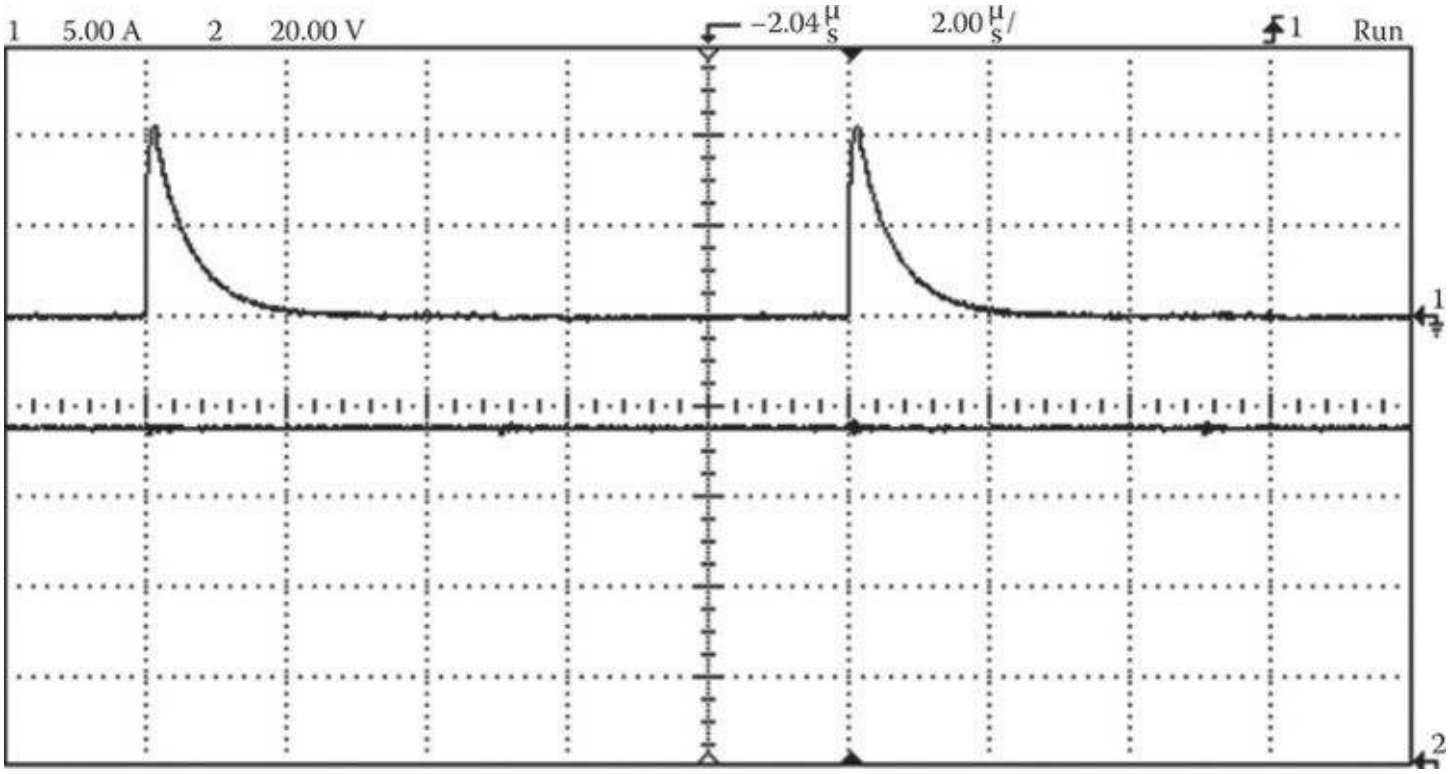


FIGURE 12.20
The experimental result of a triple-lift additional circuit at condition $k = 0.5$ and $f = 100$ kHz.

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13

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Negative-Output Multiple-Lift Push-Pull Switched-Capacitor Luo-Converters

Positive-output multiple-lift push-pull switched-capacitor (SC) Luo-converters have been introduced in Chapter 12. Correspondingly, negative-output multiple-lift push-pull SC Luo-converters will be introduced in this chapter.

13.1 Introduction

Negative-output (N/O) multiple-lift push-pull switched-capacitor (SC) Luo-converters can be sorted into several subseries as follows:

- Main series
- Additional series
- Enhanced series
- Re-enhanced series
- Multiple-enhanced series

Each circuit has one main switch S and several slave switches as S_i (i = 1, 2, 3, … n). The number n is called stage number. The main switch S is on and slaves off during switch-on period kT, and S is off and slaves on during switch-off period $(1 - k)T$. The load is resistive load R. The input voltage and current are V_{in} and I_{in}, and the output voltage and current are V_o and I_o.

Each circuit in the main series has one main switch S and n slave switches for nth stage circuit, $2n$ capacitors, and $(3n - 1)$ diodes. Each circuit in the additional series has one main switch S and n slave switches for nth stage circuit, $2(n + 1)$ capacitors, and $(3n + 1)$ diodes. Each circuit in the enhanced series has one main switch S and n slave switches for nth stage circuit, $4n$ capacitors, and $(5n - 1)$ diodes. Each circuit in the re-enhanced series has one main switch S and n slave switches for nth stage circuit, $6n$ capacitors, and $(7n - 1)$ diodes. Each circuit in the multiple (j times)-enhanced series has one main switch S and n slave switches for nth stage circuit, $2(1 + j)n$ capacitors, and $[(3 + 2j)n - 1]$ diodes. To simplify the calculation and explanation, all output values are the absolute values. The output voltage polarity is shown in the corresponding figure.

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13.2 Main Series

The first three stages of the main series are shown in Figures 13.1, 13.2 and 13.3. For the convenience of explaining, they are called N/O elementary circuit, N/O re-lift circuit, and N/O triple-lift circuit, respectively, and are numbered as n = 1, 2, and 3.

13.2.1 N/O Elementary Circuit

The elementary circuit and its equivalent circuits during switch-on and switch-off are shown in Figure 13.1. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitor C_2 is charged to V_o during switch-off. Therefore, the output voltage is (absolute value)

$$V_o = V_{in} \tag{13.1}$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1. The real output voltage is

$$V_o = V_{in} - \Delta V_1 \tag{13.2}$$

13.2.2 N/O Re-Lift Circuit

The N/O re-lift circuit is derived from N/O elementary circuit by adding one slave switch, two SCs, and three diodes (S_2–C_3–C_4–D_3–D_4–D_5). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.2. The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, and the voltage across capacitor C_3 is charged to V_1 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, and the voltage across capacitor C_4 is charged to $V_o = 2V_1 - \Delta V_2$ during switch-off. Therefore, the output voltage is

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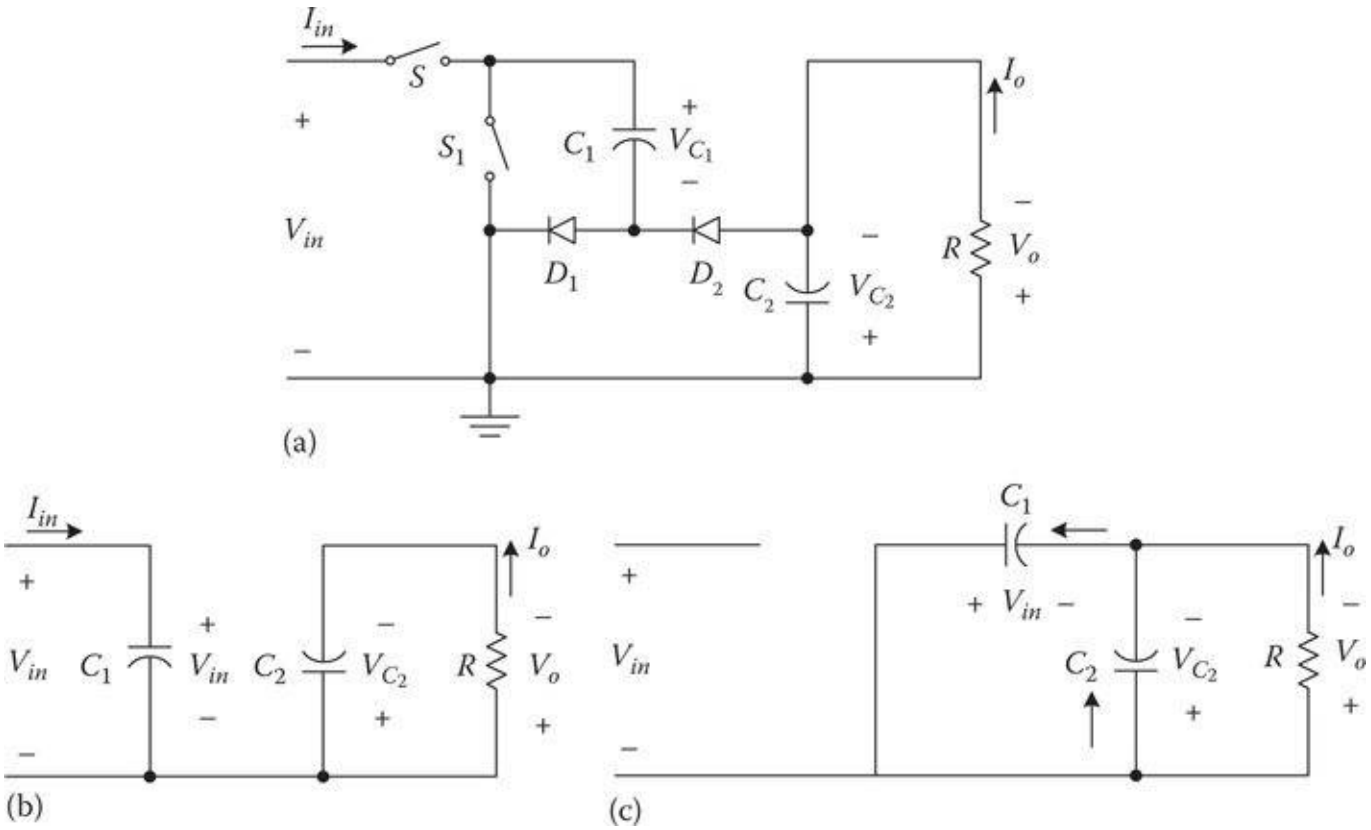


FIGURE 13.1
Elementary circuit of negative-output push-pull switched-capacitor Luo-converter. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 on).

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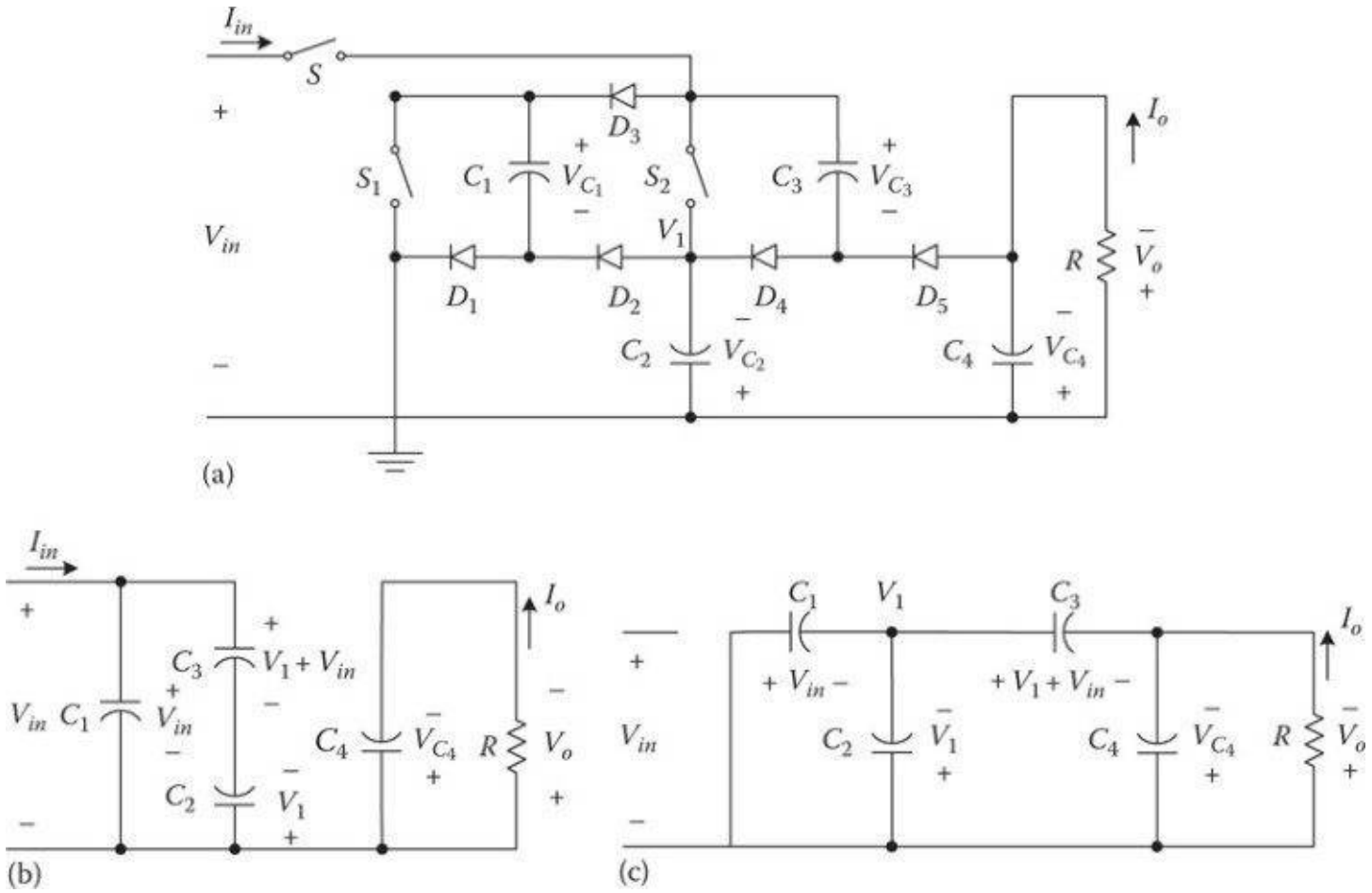


FIGURE 13.2
Negative-output re-lift push-pull switched-capacitor circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

$$V_o = 2V_1 - \Delta V_2 - V_{in} = 3V_{in} - 2\Delta V_1 - \Delta V_2 \tag{13.3}$$

where ΔV_2 is set for the same reason as ΔV_1.

13.2.3 N/O Triple-Lift Circuit

The N/O triple-lift circuit is derived from N/O re-lift circuit by adding one more slave switch, two SCs, and three diodes (S_3–C_5–C_6–D_6–D_7–D_8). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.3. The switches *S* and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_5 is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in}$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_o = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = 2V_2 - \Delta V_3 - V_{in} = 4V_1 - 2\Delta V_2 - \Delta V_3 - V_{in} = 7V_{in} - 4\Delta V_1 - 2\Delta V_2 - \Delta V_3 \tag{13.4}$$

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where ΔV_3 is set for the same reason as ΔV_1.

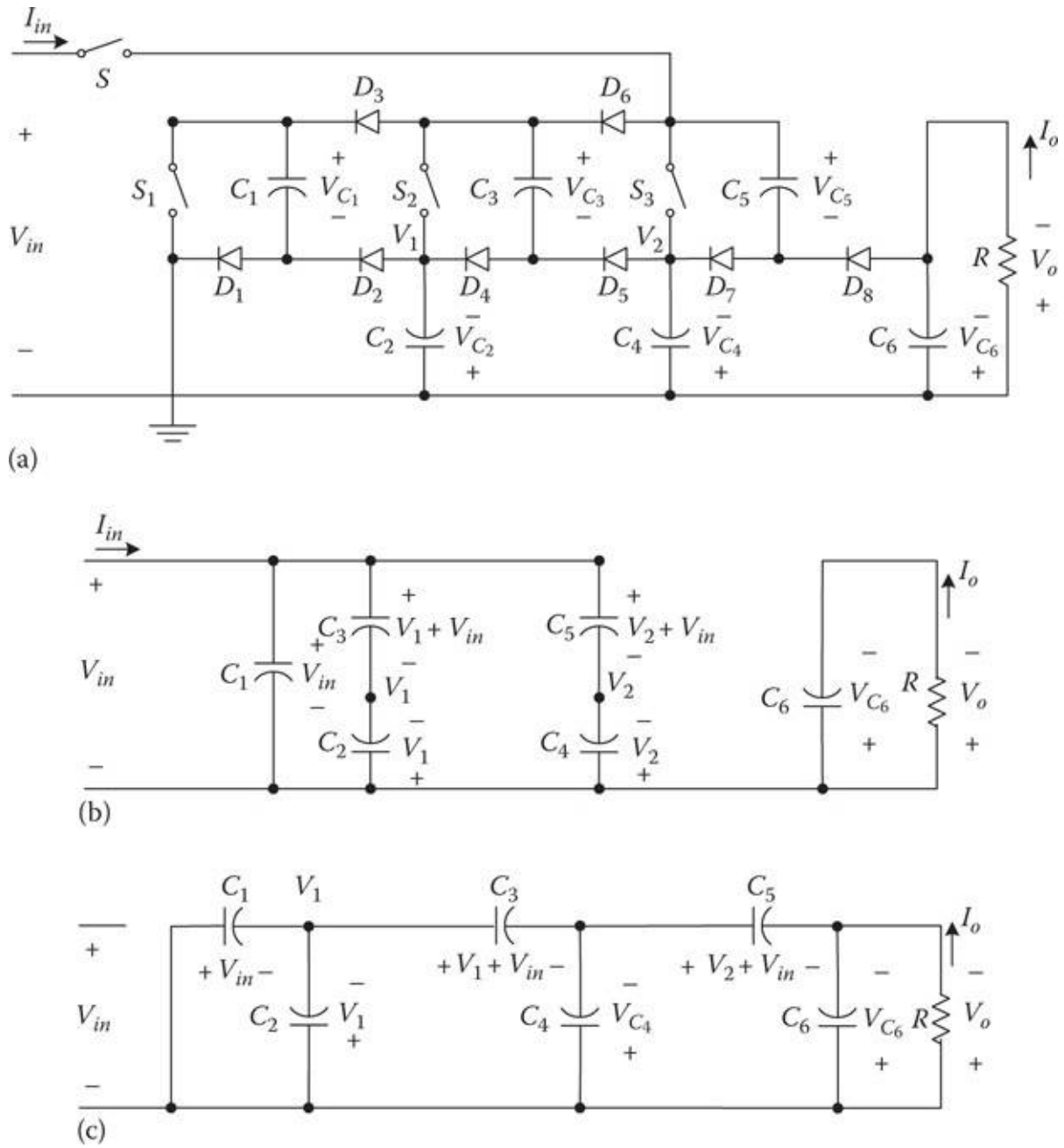


FIGURE 13.3
Negative-output triple-lift push-pull switched-capacitor circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

13.2.4 N/O Higher-Order Lift Circuit

The N/O higher-order lift circuit can be designed by multiple repeating of the parts mentioned in the previous sections. If the slave switches' number is n, the output voltage of the nth-lift circuit is

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$$V_o = (2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i} \tag{13.5}$$

13.3 Additional Series

The first three stages of the additional series are shown in Figures 13.4, 13.5 and 13.6. For the convenience of explaining, they are called N/O elementary additional circuit, N/O re-lift additional circuit, and N/O triple-lift additional circuit, respectively, and are numbered as n = 1, 2, and 3.

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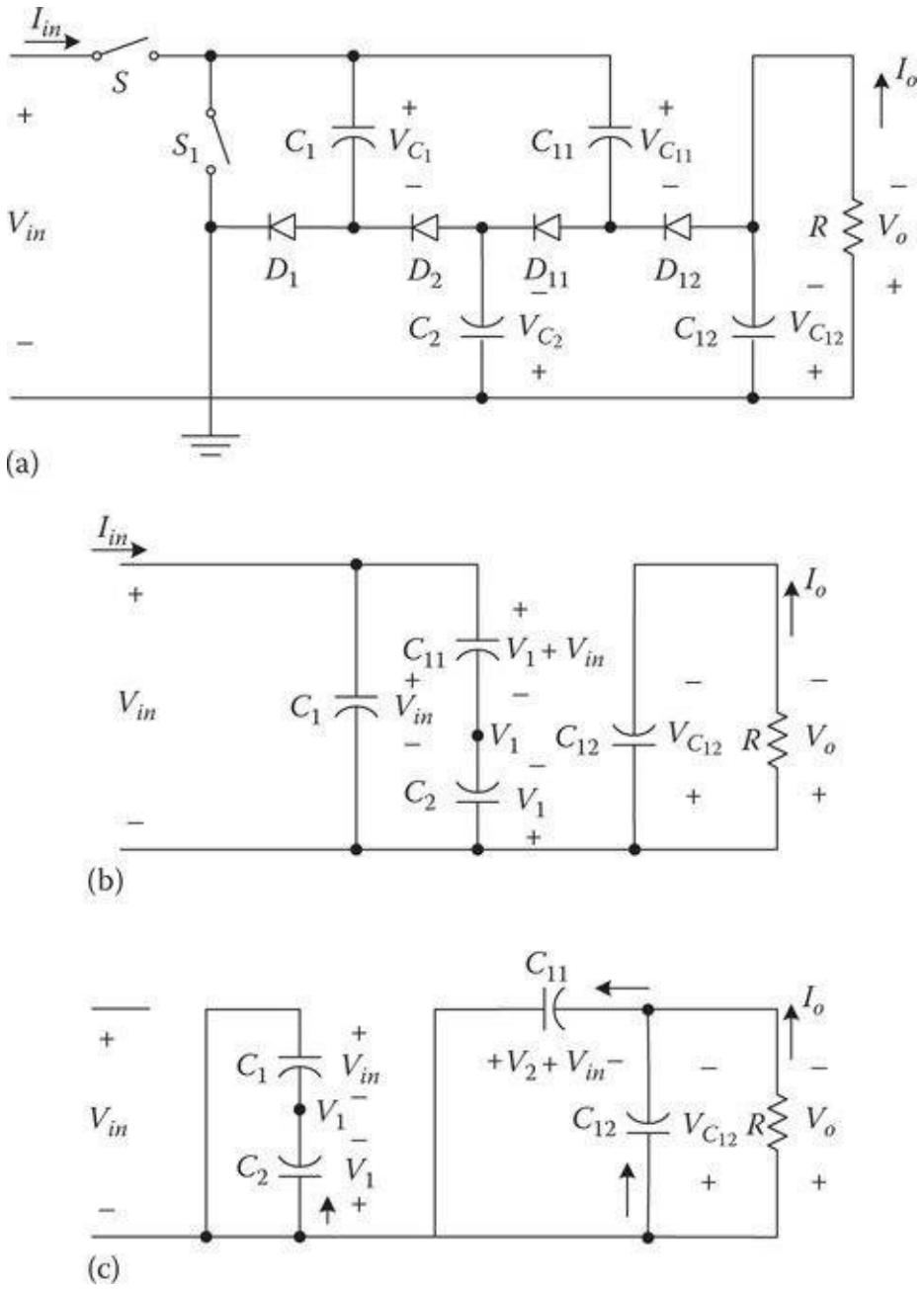


FIGURE 13.4
Negative-output elementary additional/enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 on).

13.3.1 N/O Elementary Additional Circuit

The N/O elementary additional circuit is derived from the N/O elementary circuit by adding a double/enhanced circuit (DEC). Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.4. Two switches *S* and S_1 operate in push- pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_1 + V_{in} - V_{in} = 2V_{in} \tag{13.6}$$

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Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_0 (for additional output parts). The real output voltage is

$$V_o = 2V_{in} - \Delta V_1 - \Delta V_o \tag{13.7}$$

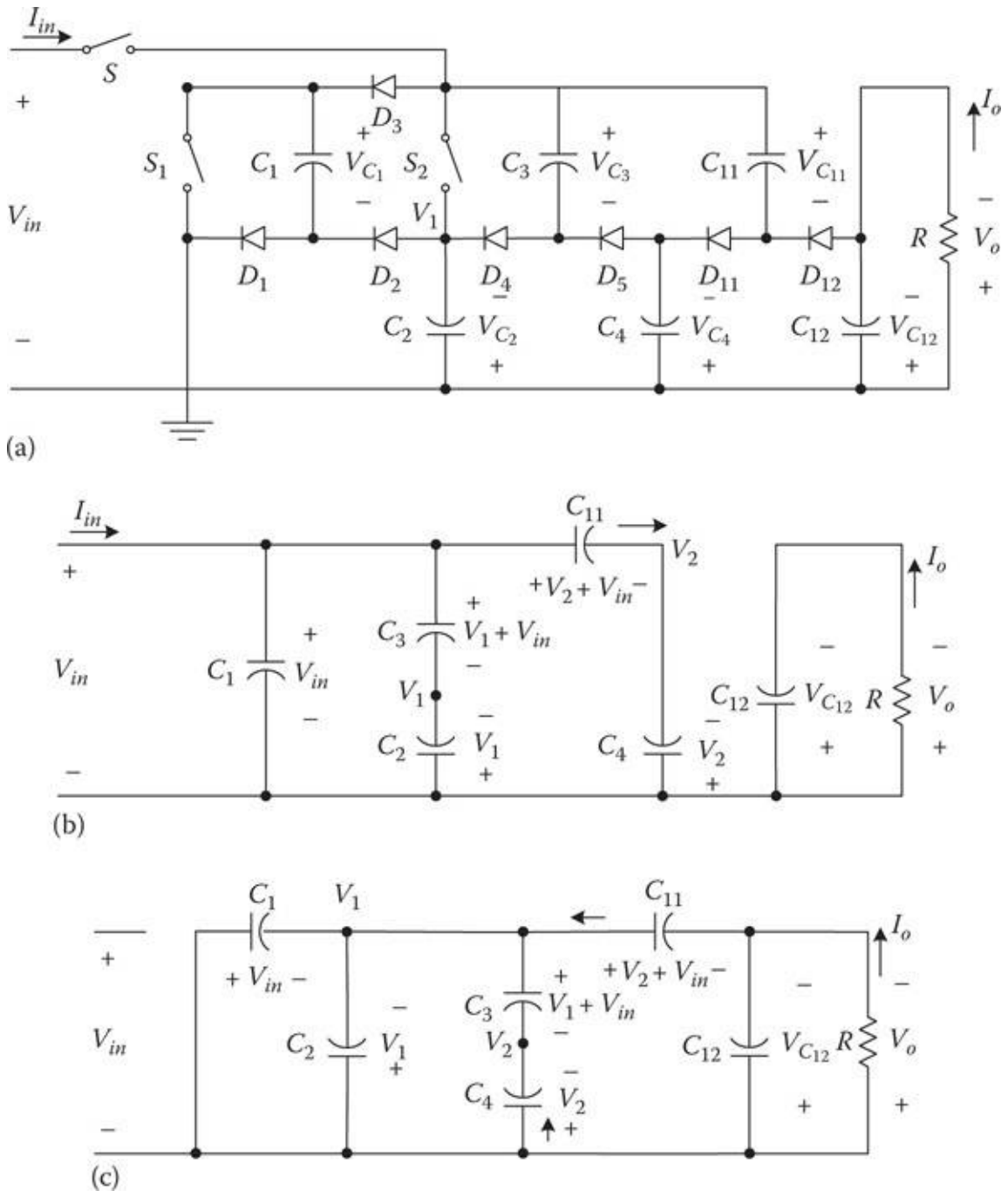


FIGURE 13.5
Negative-output re-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

13.3.2 N/O Re-Lift Additional Circuit

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The N/O re-lift additional circuit is derived from the N/O re-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.5. The switches S and (S_1 S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o - V_{in} = 5V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{13.8}$$

where ΔV_2 is set for the same reason as ΔV_1.

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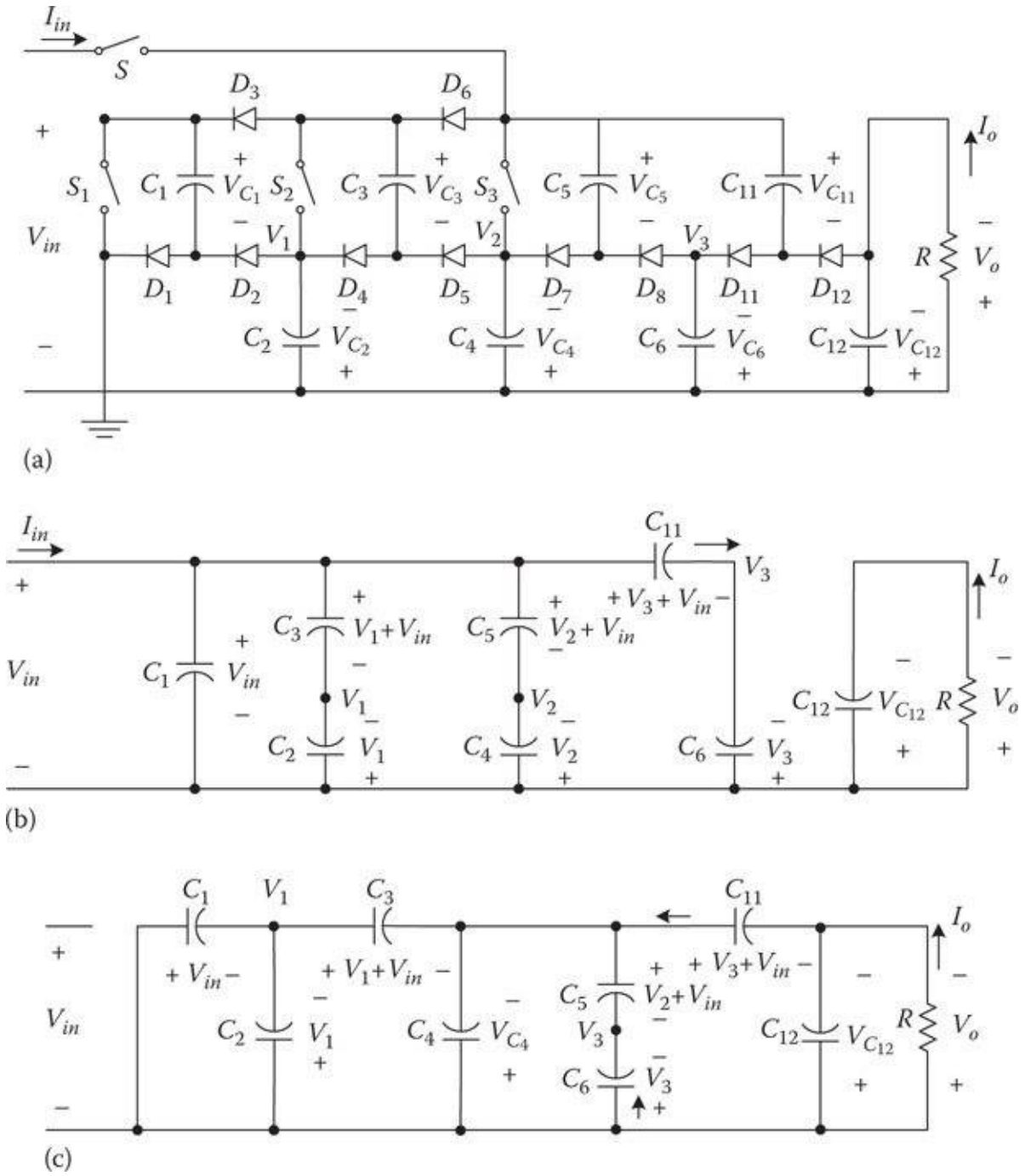


FIGURE 13.6
Negative-output triple-lift additional circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

13.3.3 N/O Triple-Lift Additional Circuit

The N/O triple-lift additional circuit is derived from the N/O triple-lift circuit by adding a DEC. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.6. The switches *S* and (S_1 S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during

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switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o - V_{in} = 11V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{13.9}$$

where ΔV_3 is set for the same reason as ΔV_1.

13.3.4 N/O Higher-Order Lift Additional Circuit

The N/O higher-order lift additional circuit is derived from the corresponding circuit of the main series by adding a DEC. The output voltage of the *n*th-lift circuit is

$$V_o = 1.5 * \left(2^n V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} \right) - V_{in} - \Delta V_n - \Delta V_o \tag{13.10}$$

13.4 Enhanced Series

The first three stages of the enhanced series are shown in Figures 13.4, 13.7, and 13.8, respectively. For convenience to explain, they are called N/O elementary enhanced circuit, N/O re-lift enhanced circuit, and N/O triple-lift enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

13.4.1 N/O Elementary Enhanced Circuit

The N/O elementary enhanced circuit is derived from N/O elementary circuit by adding a DEC. Its circuit diagram and equivalent circuits during switching-on and switching-off are shown in Figure 13.4. Therefore, the output voltage is

$$V_o = V_1 + V_{in} - V_{in} = 2V_{in} \tag{13.6}$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_o (for additional output parts). The real output voltage is

$$V_o = 2V_{in} - \Delta V_1 - \Delta V_o \tag{13.7}$$

13.4.2 N/O Re-Lift Enhanced Circuit

The N/O re-lift enhanced circuit is derived from the N/O re-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.7. The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor

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C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o - V_{in} = 8V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{13.11}$$

where ΔV_2 is set for the same reason as ΔV_1.

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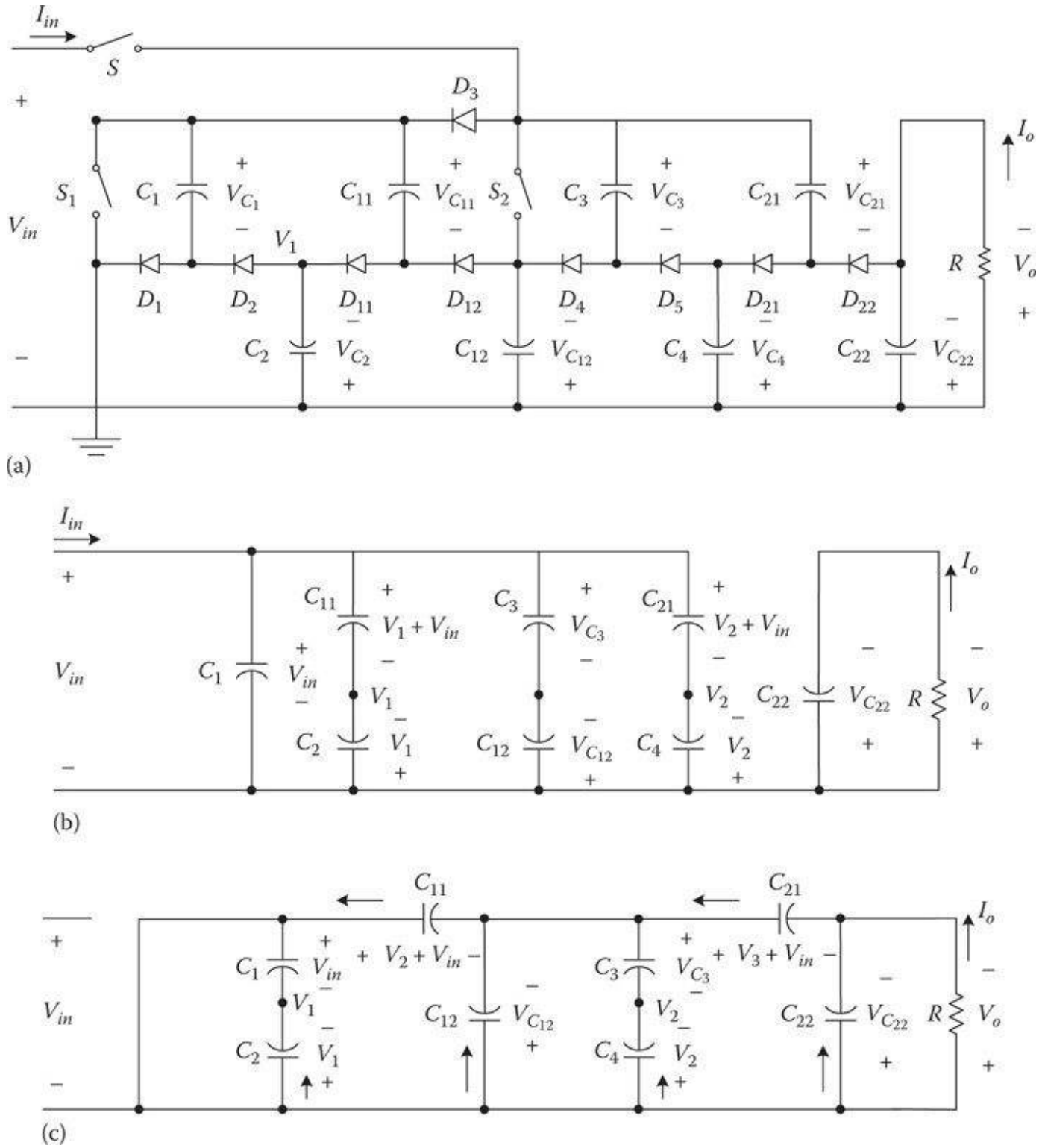


FIGURE 13.7
Negative-output re-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

13.4.3 N/O Triple-Lift Enhanced Circuit

The N/O triple-lift enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and

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switch-off are shown in Figure 13.8. The switches S and (S_1 S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o - V_{in} = 26V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{13.12}$$

where ΔV_3 is set for the same reason as ΔV_1.

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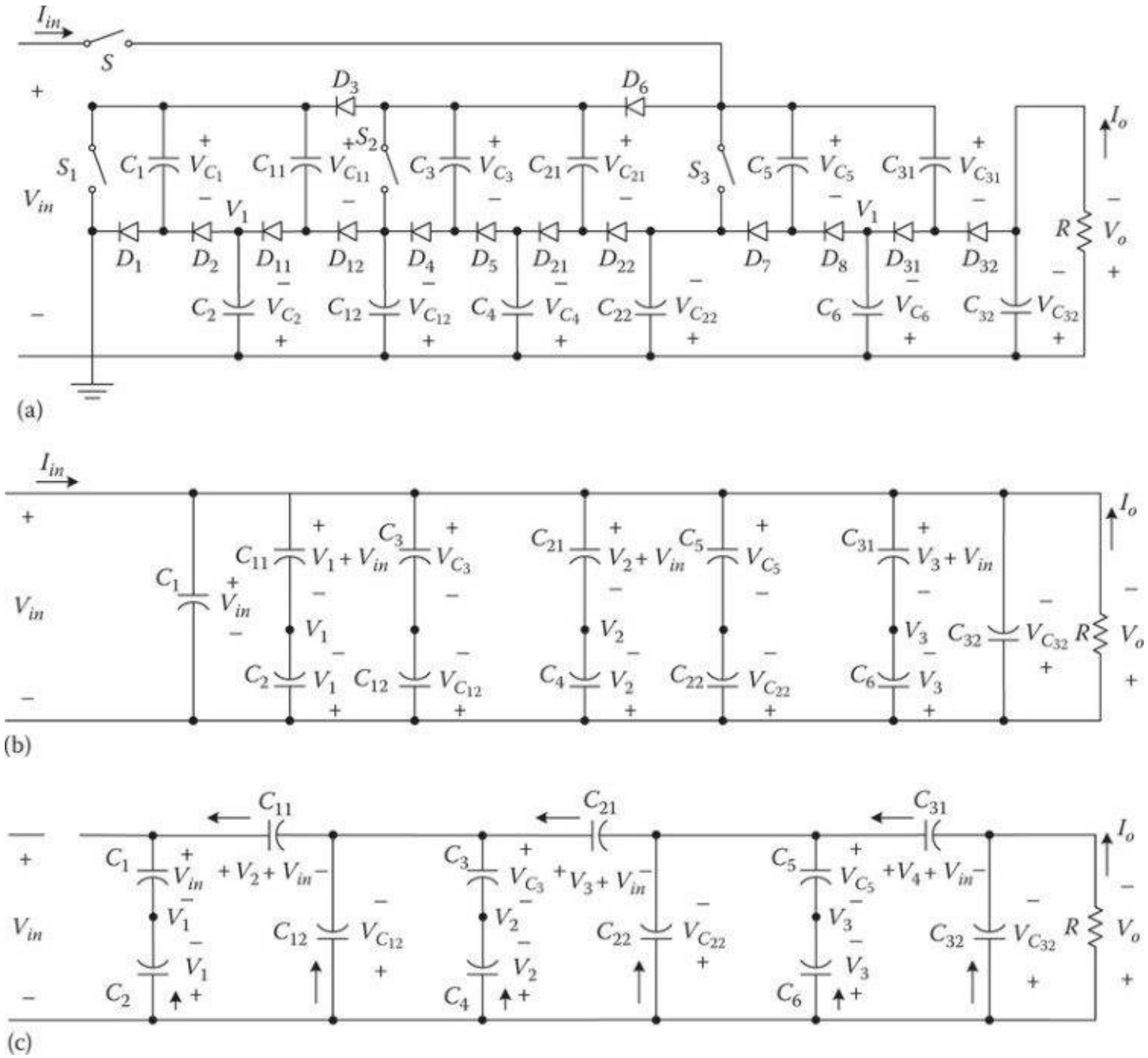


FIGURE 13.8
Negative-output triple-lift enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

13.4.4 N/O Higher-Order Lift Enhanced Circuit

The N/O higher-order lift enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC in each stage circuit. The output voltage of the *n*th-lift circuit is

$$V_o = \left[(3^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} \right] - \Delta V_n - \Delta V_o \tag{13.13}$$

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13.5 Re-Enhanced Series

The first three stages of the re-enhanced series are shown in Figures 13.9, 13.10 and 13.11. For convenience to explain, they are called N/O elementary re-enhanced circuit, N/O re-lift re-enhanced circuit, and N/O triple-lift re-enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

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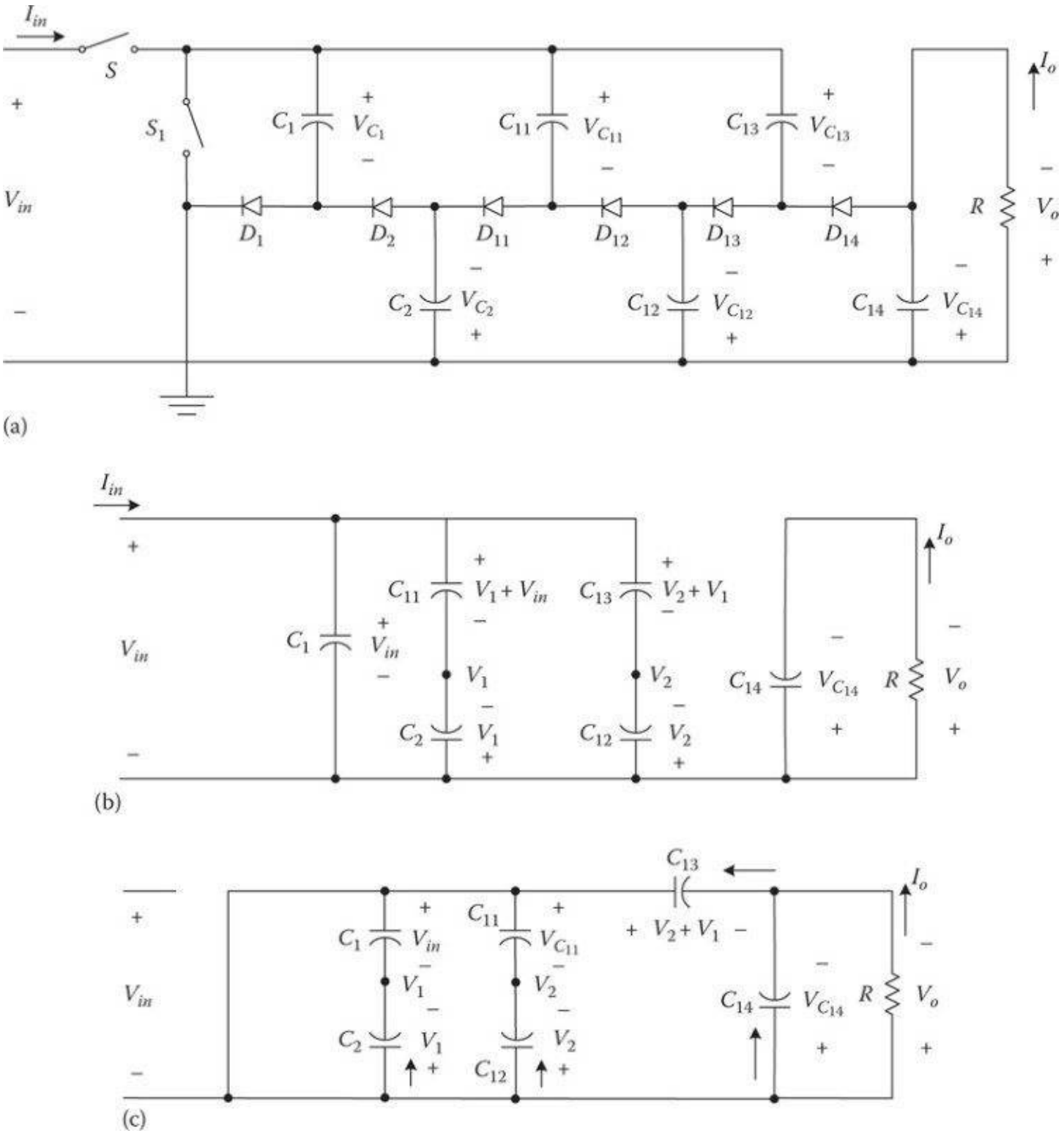


FIGURE 13.9
Negative-output elementary re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 on).

13.5.1 N/O Elementary Re-Enhanced Circuit

The N/O elementary re-enhanced circuit is derived from N/O elementary circuit by adding the DEC twice. Its circuit diagram and equivalent circuits during switch-on and switch-off are

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shown in Figure 13.9. Two switches S and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. The voltage across capacitors C_{12} and C_{13} is charged to $V_{C12} = 4V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_{C_{12}} - V_{in} = 3V_{in} \tag{13.14}$$

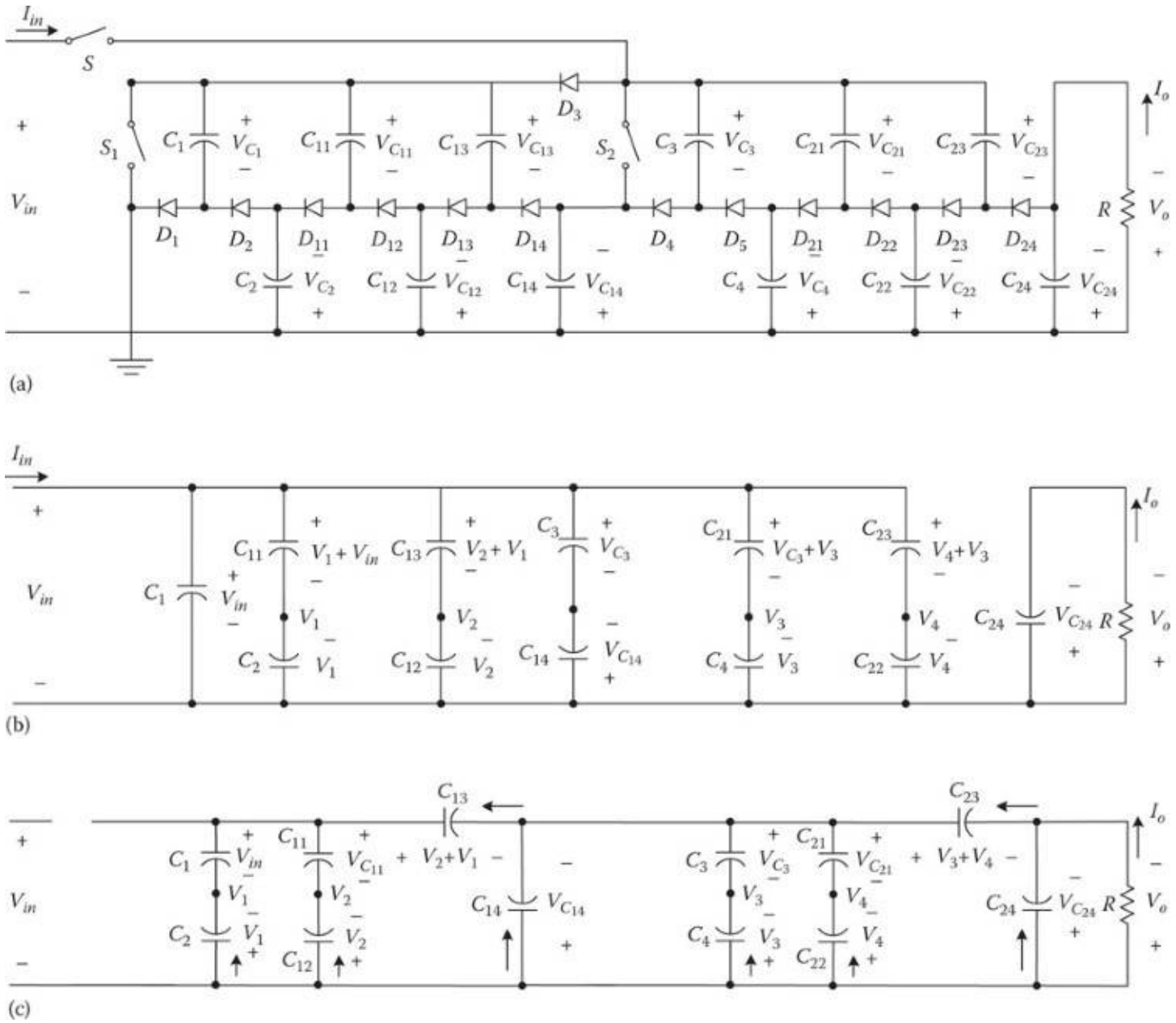


FIGURE 13.10
Negative-output re-lift re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

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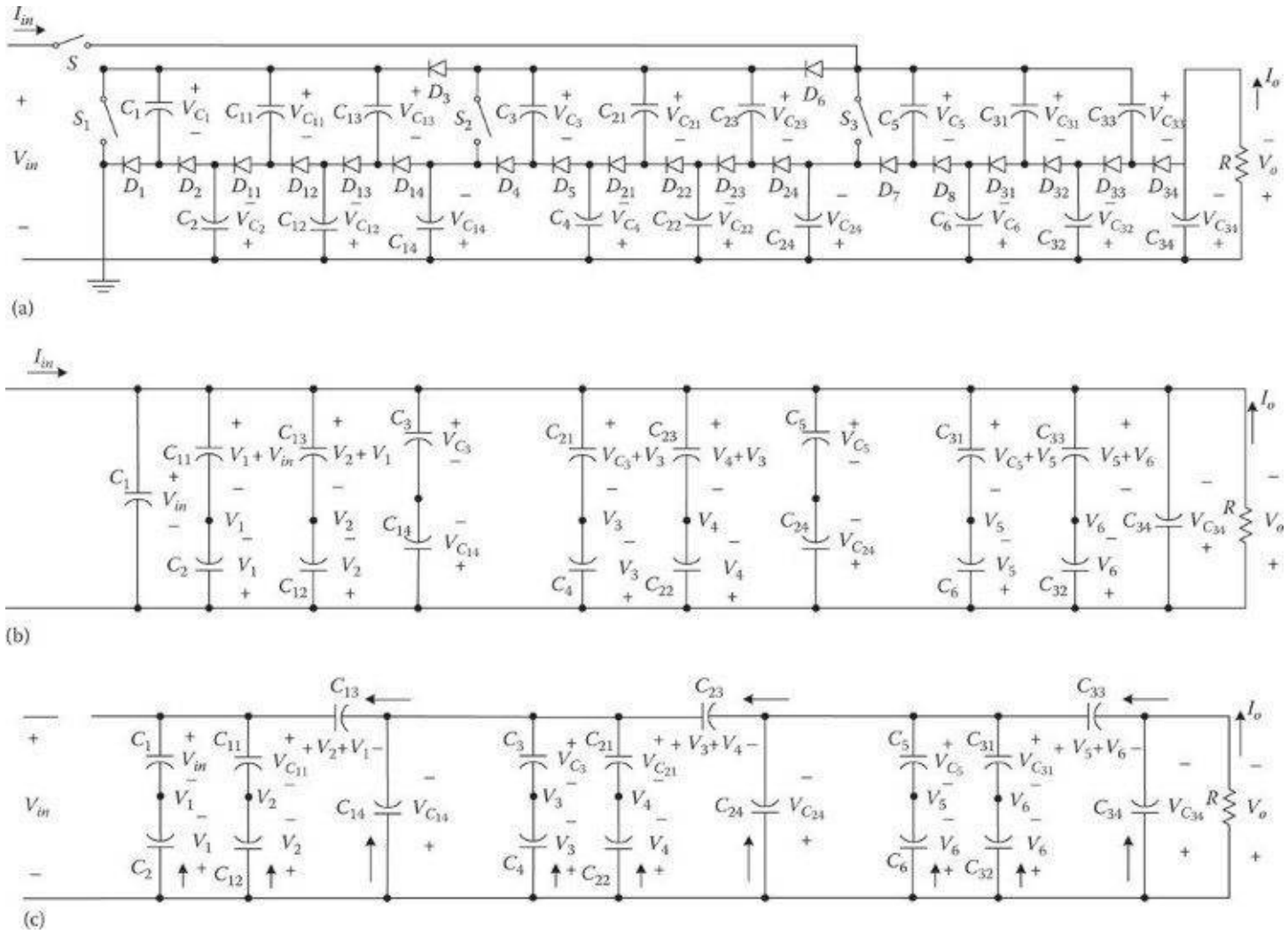


FIGURE 13.11
Negative-output triple-lift re-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_o (for additional output parts). The real output voltage is

$$V_o = 3V_{in} - \Delta V_1 - \Delta V_o \tag{13.15}$$

13.5.2 N/O Re-Lift Re-Enhanced Circuit

The N/O re-lift re-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch- on and switch-off are shown in Figure 13.10. The switches *S* and (S_1, S_2) operate in push- pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

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$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o - V_{in} = 15V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{13.16}$$

where ΔV_2 is set for the same reason as ΔV_1.

13.5.3 N/O Triple-Lift Re-Enhanced Circuit

The N/O triple-lift re-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC twice in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.11. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o - V_{in} = 63V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{13.17}$$

where ΔV_3 is set for the same reason as ΔV_1.

13.5.4 N/O Higher-Order Lift Re-Enhanced Circuit

The N/O higher-order lift re-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC twice in each stage circuit. The output voltage of the *n*th-lift circuit is

$$V_o = \left[(4^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} \right] - \Delta V_n - \Delta V_o \tag{13.18}$$

13.6 Multiple-Enhanced Series

The first three stages of the multiple-enhanced series are shown in Figures 13.12, 13.13 and 13.14. For convenience to explain, they are called N/O elementary multiple-enhanced circuit, N/O re-lift multiple-enhanced circuit, and N/O triple-lift multiple-enhanced circuit, respectively, and are numbered as n = 1, 2, and 3.

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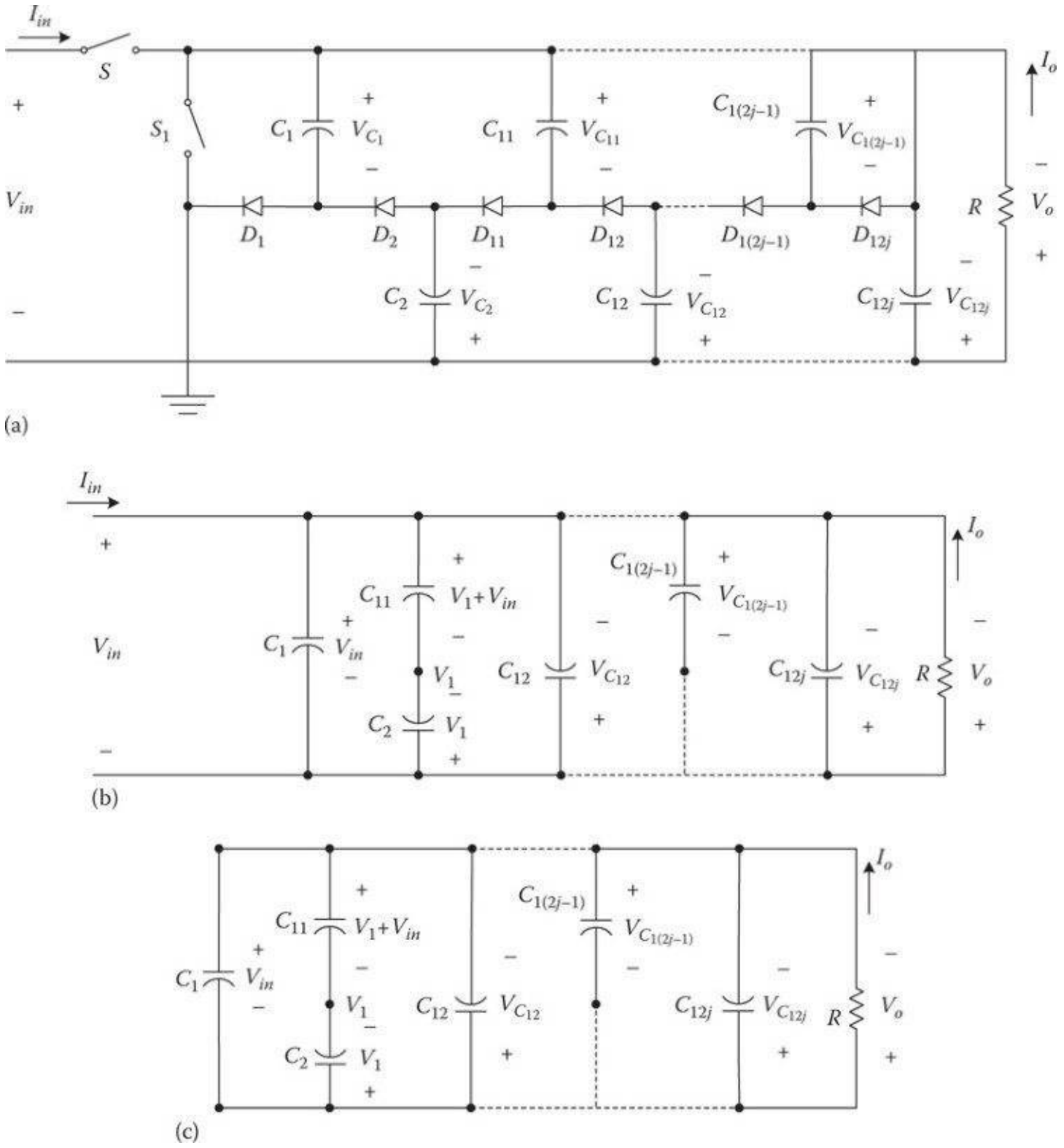


FIGURE 13.12
Negative-output elementary multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (S on). (c) Equivalent circuit during switch-off (S_1 on).

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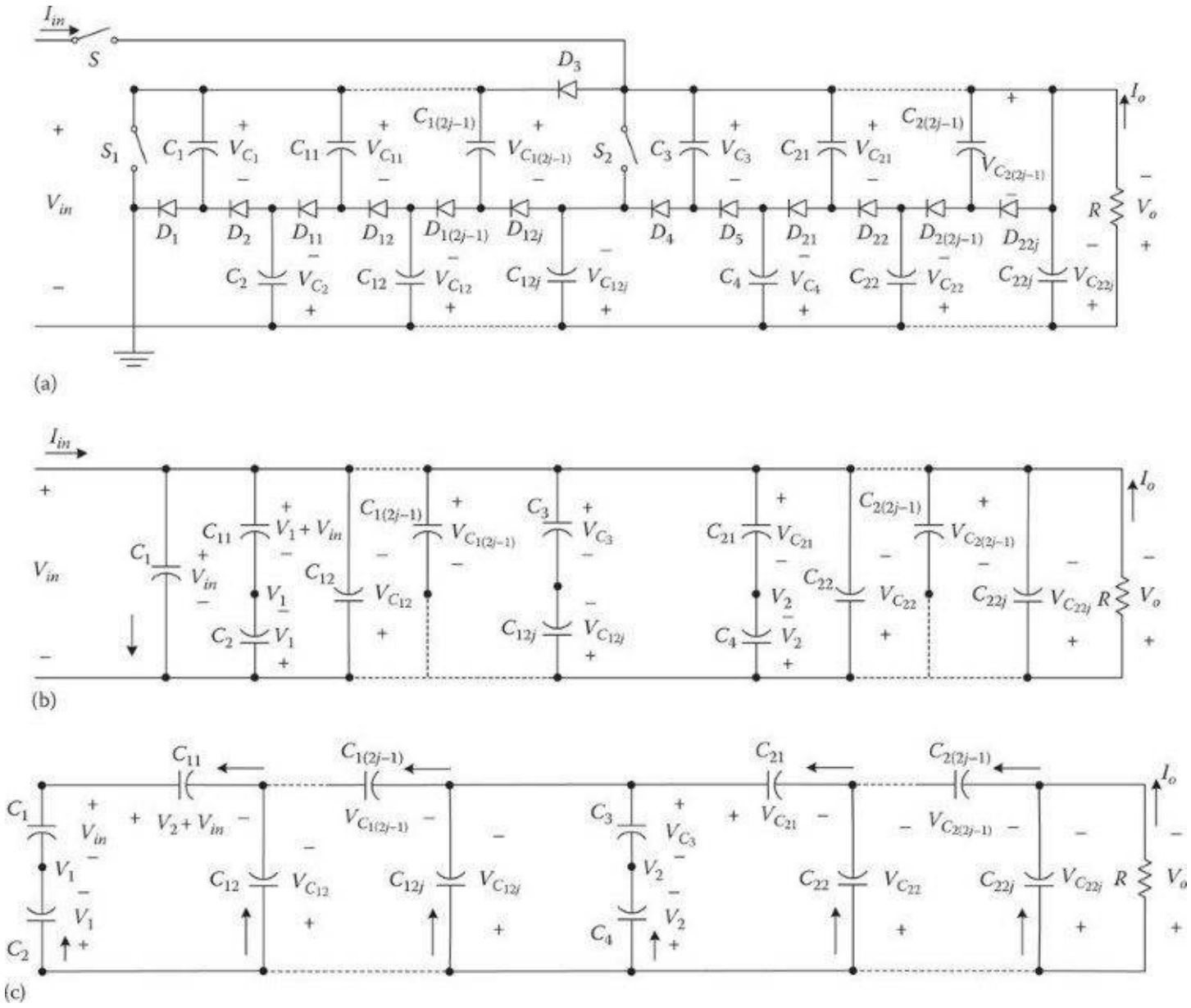


FIGURE 13.13
Negative-output re-lift multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1 and S_2 on).

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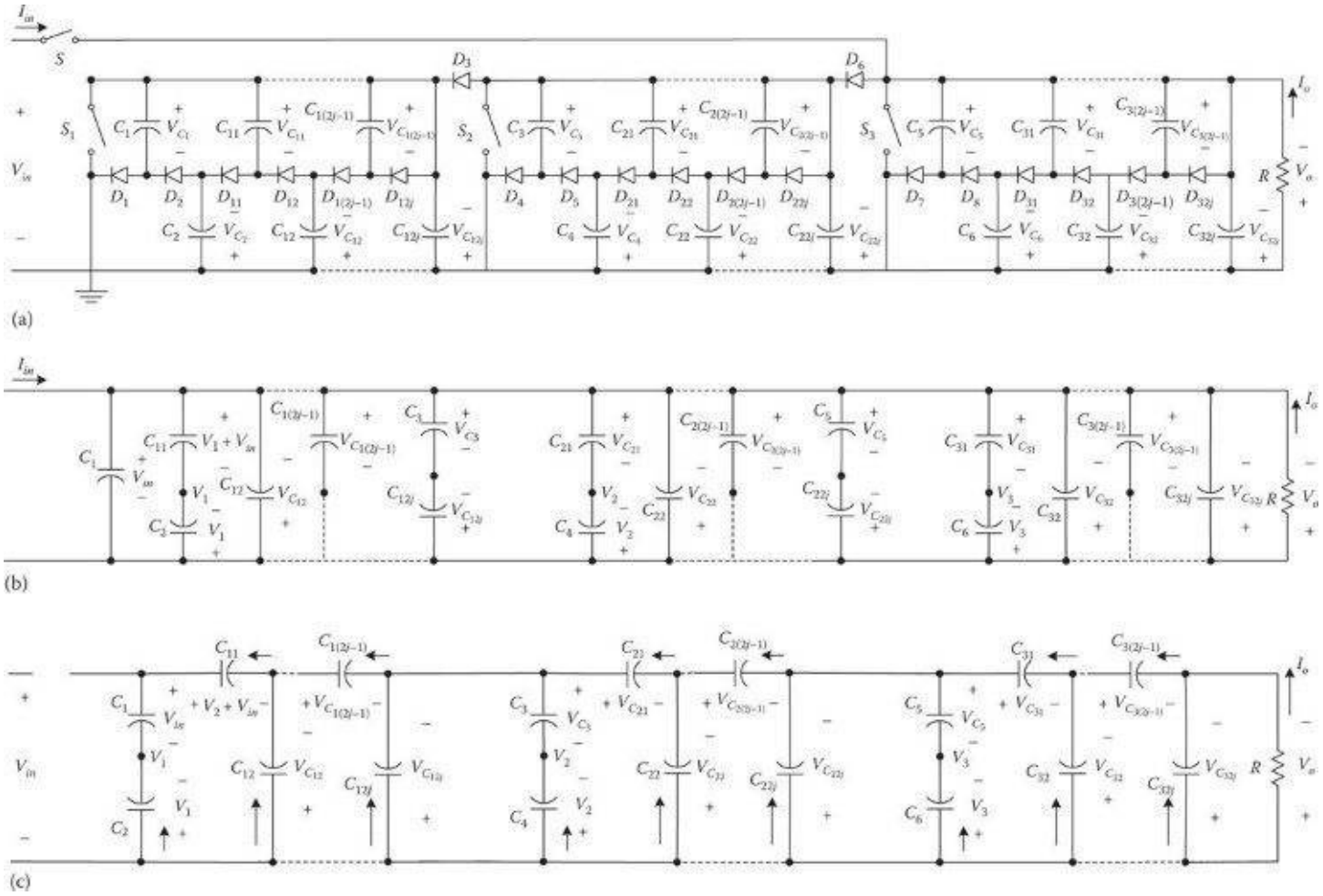


FIGURE 13.14
Negative-output triple-lift multiple-enhanced circuit. (a) Circuit diagram. (b) Equivalent circuit during switch-on (*S* on). (c) Equivalent circuit during switch-off (S_1, S_2, and S_3 on).

13.6.1 N/O Elementary Multiple-Enhanced Circuit

The N/O elementary multiple-enhanced circuit is derived from the N/O elementary circuit by adding the DEC multiple (*j*) times. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.12. Two switches *S* and S_1 operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in} during switch-on. The voltage across capacitors C_2 and C_{11} is charged to $V_1 = 2V_{in}$ during switch-off. The voltage across capacitors $C_{1(2j-1)}$ is charged to $V_{C1(2j-1)} = (1 + j)V_{in}$ during switch-off. Therefore, the output voltage is

$$V_o = V_{C_{1(2j-1)}} - V_{in} = jV_{in} \tag{13.19}$$

Considering the voltage drops across the diodes and switches, we combine all values in a figure of ΔV_1 and ΔV_0 (for additional output parts). The real output voltage is

$$V_o = jV_{in} - \Delta V_1 - \Delta V_o \tag{13.20}$$

13.6.2 N/O Re-Lift Multiple-Enhanced Circuit

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The N/O re-lift multiple-enhanced circuit is derived from the N/O re-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.13. The switches S and (S_1, S_2) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, and the voltage across capacitor C_{11} is charged to V_2 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_{12} is charged to $V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o$ during switch-off. Therefore, the output voltage is

$$V_o = V_2 + V_1 - \Delta V_2 - \Delta V_o - V_{in} = [(1+j)^2 - 1]V_{in} - 3\Delta V_1 - \Delta V_2 - \Delta V_o \tag{13.21}$$

where ΔV_2 is set for the same reason as ΔV_1.

13.6.3 N/O Triple-Lift Multiple-Enhanced Circuit

The N/O triple-lift multiple-enhanced circuit is derived from the N/O triple-lift circuit by adding the DEC multiple (j) times in each stage circuit. Its circuit diagram and equivalent circuits during switch-on and switch-off are shown in Figure 13.14. The switches S and (S_1, S_2, S_3) operate in push-pull state. The voltage across capacitor C_1 is charged to V_{in}, the voltage across capacitor C_3 is charged to V_1, the voltage across capacitor C_5 is charged to V_2, and the voltage across capacitor C_{11} is charged to V_3 during switch-on. The voltage across capacitor C_2 is charged to $V_1 = 2V_{in} - \Delta V_1$, the voltage across capacitor C_4 is charged to $V_2 = 2V_1 - \Delta V_2$, and the voltage across capacitor C_6 is charged to $V_3 = 2V_2 - \Delta V_3$ during switch-off. Therefore, the output voltage is

$$V_o = V_3 + V_2 - \Delta V_3 - \Delta V_o - V_{in} = [(1+j)^3 - 1]V_{in} - 6\Delta V_1 - 3\Delta V_2 - \Delta V_3 - \Delta V_o \tag{13.22}$$

where ΔV_3 is set for the same reason as ΔV_1.

13.6.4 N/O Higher-Order Lift Multiple-Enhanced Circuit

The N/O higher-order lift multiple-enhanced circuit is derived from the corresponding circuit of the main series by adding the DEC multiple (j) times in each stage circuit. The output voltage of the nth order lift circuit is

$$V_o = [(1+j)^n - 1]V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_o \tag{13.23}$$

13.7 Summary of This Technique

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Using this technique, it is easy to design N/O higher-order lift circuits to obtain high output voltage. All these converters can be sorted in several subseries: main series, additional series, enhanced series, re-enhanced series, and multiple-enhanced series. The output voltage of the *n*th-lift circuit is

$$V_o = \begin{cases} (2^n - 1)V_{in} - \sum_{i=0}^{n-1} 2^i \Delta V_{n-i} & \text{Main series} \\ (1.5 * 2^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_o & \text{Additional series} \\ (3^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_o & \text{Enhanced series} \\ (4^n - 1)V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_o & \text{Reenhanced series} \\ [(2 + j)^n - 1]V_{in} - \sum_{i=1}^{n-1} 2^i \Delta V_{n-i} - \Delta V_n - \Delta V_o & \text{Multiple-enhanced series} \end{cases} \quad (13.24)$$

From this formula, the family tree of N/O multiple-lift push-pull SC Luo-converters is shown in Figure 13.15.

13.8 Simulation and Experimental Results

To verify the design and calculation results, PSpice simulation package was applied to these circuits. Choose V_{in} = 10 V, all capacitors C_i = 2 μF, R = 60 Ω., k = 0.5, and f = 100 kHz, the voltage and current values are obtained from an N/O triple-lift circuit. The same conditions are applied to a test rig, and experimental results are then obtained.

13.8.1 Simulation Results

Assume that the voltage drops ΔV_1, ΔV_2, and ΔV_3 are about 4.2 V; the voltage values of V_1, V_2, and V_o are −5.2, −16, and −41 V, respectively; and current waveforms of I_{D2}, I_{D5}, and I_{D8} (the leak values are 103, 6.7, and 0.093 A, respectively) are obtained. The simulation results voltage values in Figure 13.16 are identically matched with the calculated results.

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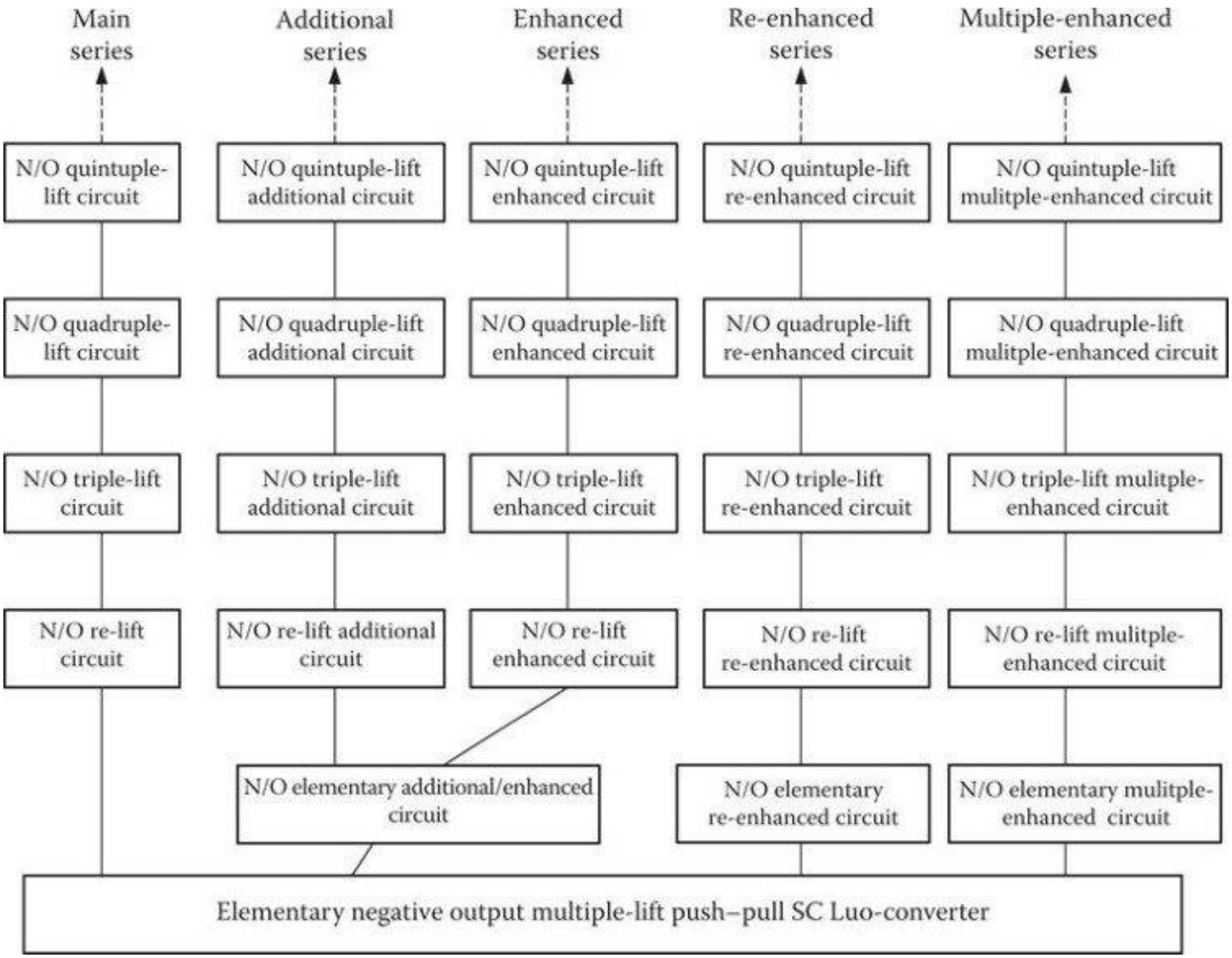


FIGURE 13.15
The family tree of negative-output multiple-lift push-pull switched-capacitor Luo-converters.

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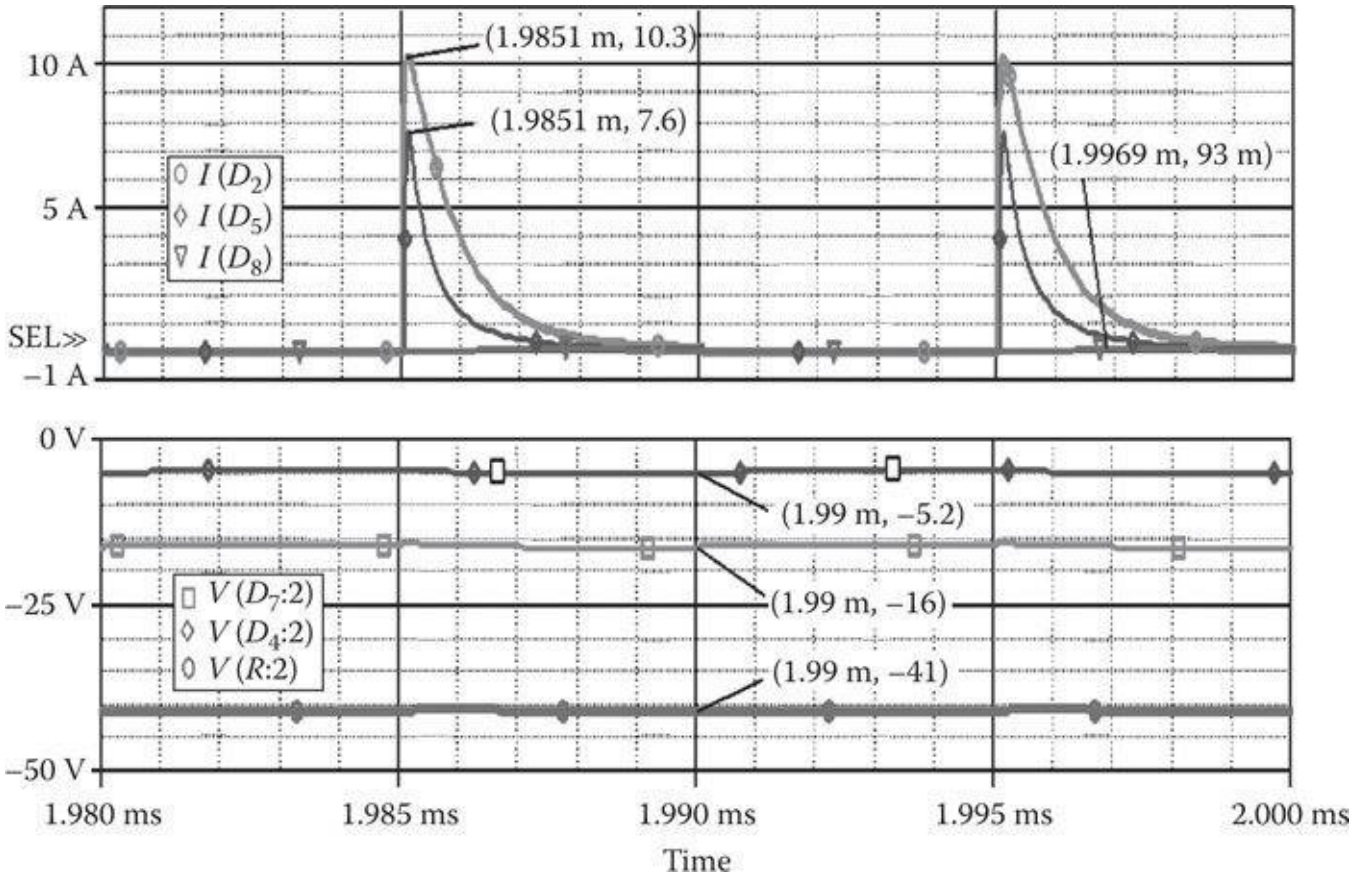


FIGURE 13.16
The simulation results of a negative-output triple-lift circuit at condition k = 0.5 and f = 100 kHz.

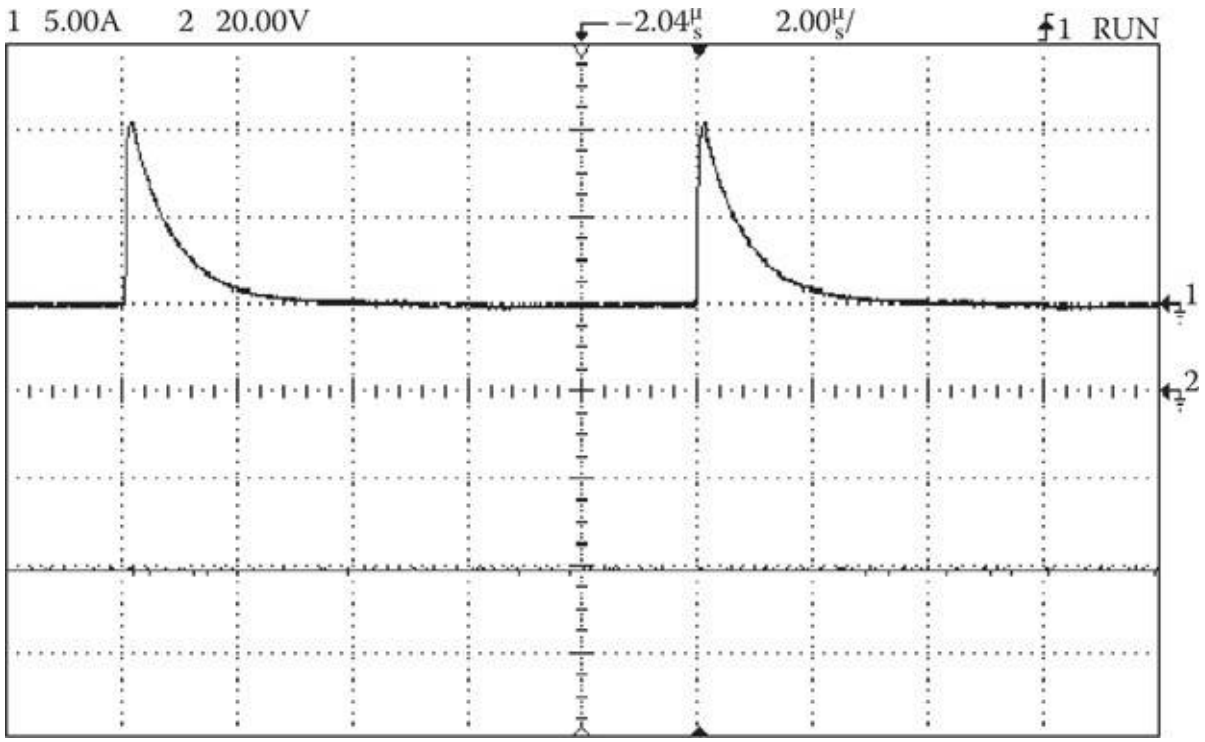


FIGURE 13.17
Experimental result of a negative-output triple-lift circuit at condition k = 0.5 and f = 100 kHz.

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13.8.2 Experimental Results

Assuming that the voltage drops ΔV_1, ΔV_2, and ΔV_3 are still about 4.2 V, the output voltage V_o (−41 V) and current waveform of I_{D2} (leak value is 10.3 A) are obtained and shown in Figure 13.17, which are identically matched with the calculated and simulation results.

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14

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Multiple-Quadrant Soft-Switching Converters

The third-generation converters can transfer large amounts of power with high power density to actuators. However, its power losses are usually high during the transfer of large amounts of power since the power losses across the switch devices are high. The soft-switching technique is an effective way to reduce the converter power losses and improve the efficiency. Therefore, it is a very popular method in industrial applications.

The fourth-generation converters are called soft-switching converters. The soft-switching technique involves many methods implementing resonance characteristics. A popular method is the resonant switch. Soft-switching converters are mainly implemented by the resonant technique. The resonant converters have drawn much attention in research applications. They are sorted into four categories:

1. Load-resonant converters
2. Resonant-DC-link converters
3. High-frequency-link integral-half-cycle converters
4. Resonant-switch converters

The converters of the first, second, and third categories can be applied in those cases depending on the load components and linking cables. The converters of the fourth category are applied in the case depending on the resonant circuit in the switch end, which are independent from the load and link components. After about two decades of investigation and application, most industrial applications use *resonant-switch converters*.

Resonant-switch converters can perform in the overresonant state, critical/optimum-resonant state, and quasi-resonant state. In order to determine two (current/voltage) zero-cross points for switch-on and switch-off, the quasi-resonant state is usually employed. The corresponding converter is called quasi-resonant converter (QRC). The quasi-resonant state can perform in full-waveform mode and half-waveform mode. The clue of soft-switching technique focuses on the zero-cross point rather than the resonance. Consequently, there is no need to perform in full-waveform mode. Most soft-switching converters perform in half-waveform mode.

The zero-current-switch QRCs, zero-voltage-switch QRCs, and zero-transition (ZT) converters will be discussed in this chapter.

14.1 Introduction

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Zero-current-switch (ZCS) quasi-resonant converters (QRCs) implement ZCS operation. Since switches turn on and turn off at the moment that the current is equal to zero, the power losses during switch-on and switch-off become zero. Consequently, these converters have high power density (PD) and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state; the components of higher-order harmonics are very low. Therefore, the electromagnetic interference (EMI) is low, and the electromagnetic susceptibility (EMS) and electromagnetic compatibility (EMC) are reasonable.

Zero-voltage-switch (ZVS) QRCs use the ZVS technique. Since switches turn on and turn off at the moment that the voltage is equal to zero, the power losses during switch-on and switch-off become zero. Consequently, these converters have high PD and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state; the components of higher-order harmonics are very low. Therefore, the EMI is low, and EMS and EMC are reasonable.

ZCS-QRC and ZVS-QRC have large voltage and current stresses. In addition, the conduction duty cycle K and switch frequency f are not individually adjusted. To overcome these drawbacks, we designed zero-voltage plus zero-current-switch and ZT converters, which implement the ZVS and ZCS technique. Since switches turn on and turn off at the moment that the voltage and/or current is equal to zero, the power losses during switch- on and switch-off become zero. Consequently, these converters have high PD and transfer efficiency. Usually, the repeating frequency is not very high and the converter works in the resonance state; the components of higher-order harmonics are very low. Therefore, the EMI is low, and EMS and EMC are reasonable.

The ZCS technique significantly reduces the power losses across the switches during the switch-on and switch-off. Unfortunately, most papers discuss the converters only working at single-quadrant operation. This chapter introduces the multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter. It performs the soft-switching technique with a four-quadrant operation, which effectively reduces the power losses and largely increases the power transfer efficiency. The results obtained from analysis and design were compared and verified by practical test results.

14.2 Multiple-Quadrant DC/DC ZCS Quasi-Resonant Luo-Converters

A multiple-quadrant DC/DC ZCS quasi-resonant Luo-converter is shown in Figure 14.1. Circuit 1 implements the operation in quadrants I and II, that is, two-quadrant (I and II) 2CS quasi-resonant Luo-converters. Circuit 2 implements the operation in quadrants III and IV, that is, two-quadrant (III and IV) 2CS quasi-resonant Luo-converters. Circuit 1 and Circuit 2 can be converted to each other by auxiliary changeover switch S_3. Auxiliary switch S_a assists the two-quadrant operation in the same circuit. It is controlled by a logic quadrant operation controller. Each circuit consists of one main inductor L and two switches. Assuming that the

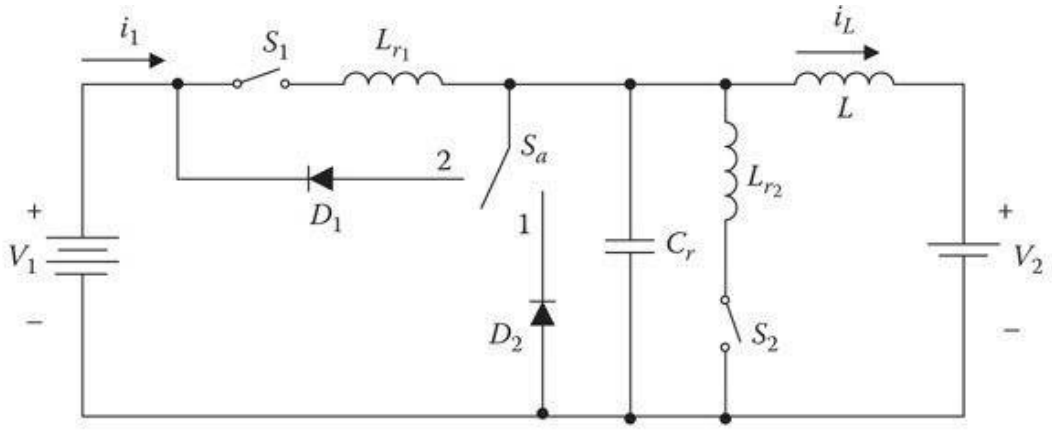
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main inductance L is sufficiently large, the current i_L remains constant. The source and load voltages are usually constant, for example, V_1 = 42 V and V_2 = µ28 V. There are four modes of operation:

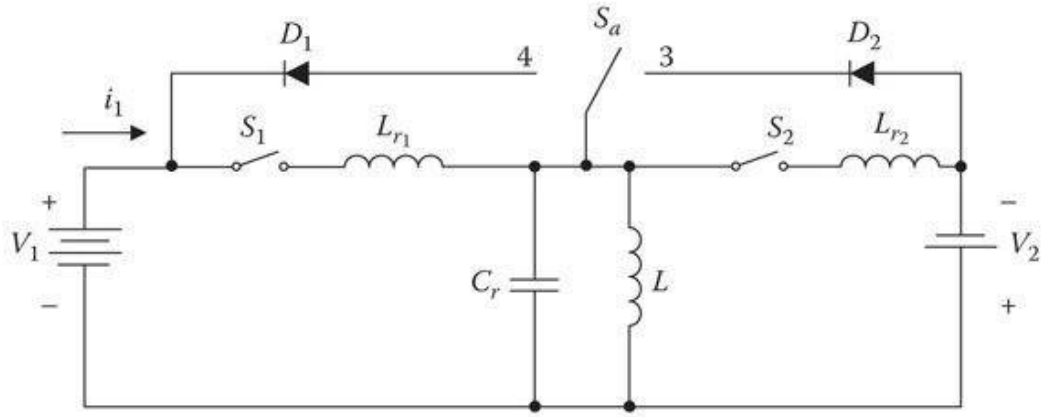
1. *Mode A (quadrant I):* Electrical energy is transferred from V_1 side to V_2 side.
2. *Mode B (quadrant II):* Electrical energy is transferred from V_2 side to V_1 side.
3. *Mode C (quadrant III):* Electrical energy is transferred from V_1 side to $-V_2$ side.
4. *Mode D (quadrant IV):* Electrical energy is transferred from $-V_2$ side to V_1 side.

Each mode has two states: *on* and *off*. The switch status of each state is shown in Table 14.1.

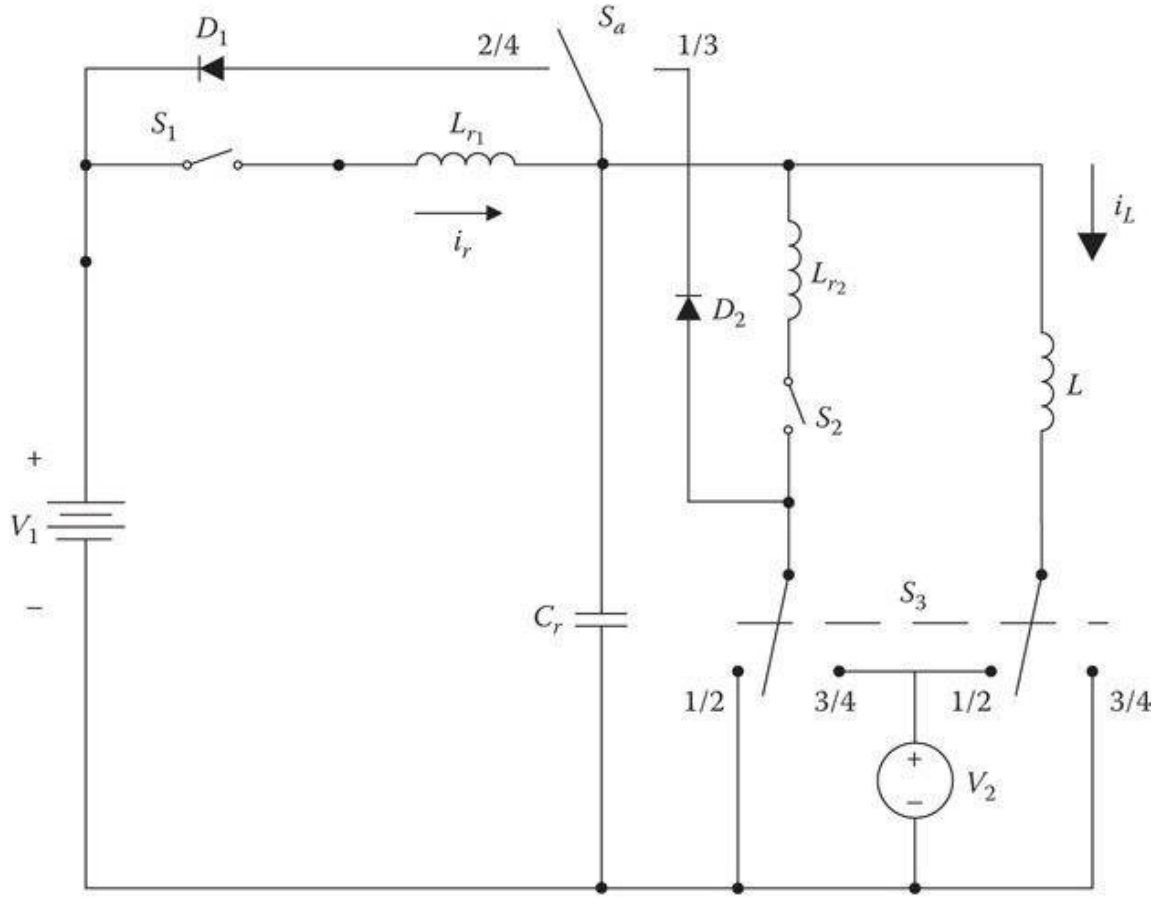
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(a)



(b)



(c)

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FIGURE 14.1
Four-quadrant DC/DC zero-current-switch quasi-resonant Luo-converter. (a) Circuit 1 for the operation in quadrant I and quadrant II. (b) Circuit 2 for the operation in quadrant III and quadrant IV. (c) Circuit 3 for the four quadrants.

TABLE 14.1
Switch's Status (the Blank Status Means Off)

	Mode A (Quadrant I)		Mode B (Quadrant II)		Mode C (Quadrant III)		Mode D (Quadrant IV)	
Switch or Diode	State-On	State-Off	State-On	State-Off	State-On	State-Off	State-On	State-Off
Circuit	Circuit 1				Circuit 2			
S_1	On				On			
D_1			On					On
S_2			On				On	
D_2		On				On		
S_a	Position 1		Position 2		Position 3		Position 4	

14.2.1 Mode A

Mode A is a ZCS buck converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.2. There are four time regions for the switch-on and switch-off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch S_1 and the main inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r_1} - C_r$.

The natural resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_n C_r}} \tag{14.1}$$

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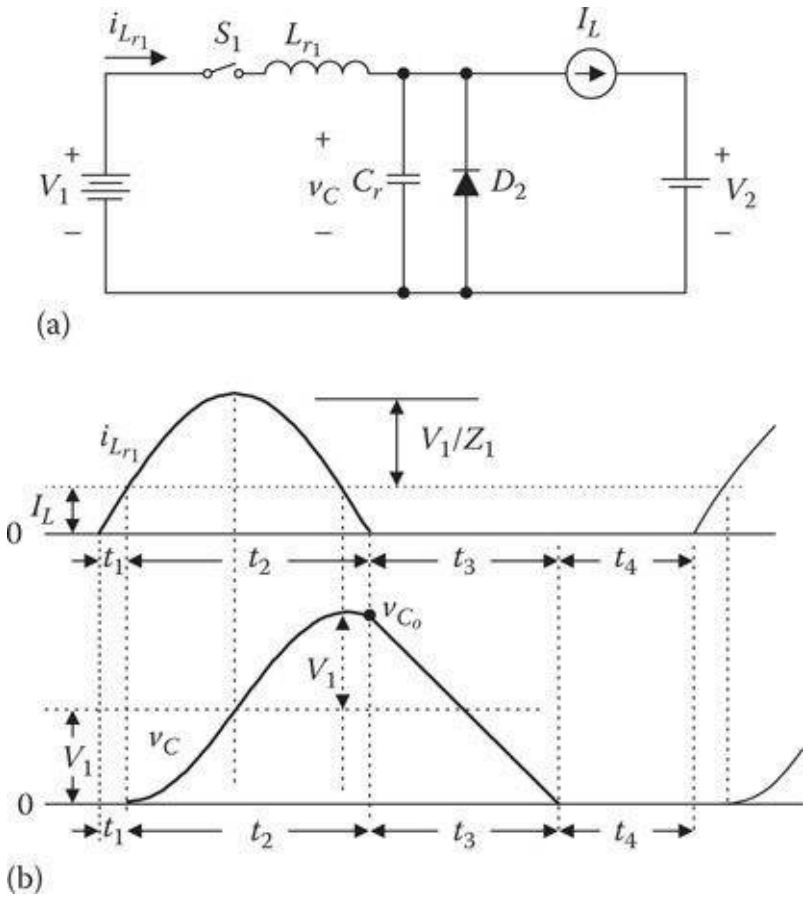


FIGURE 14.2
Mode A operation. (a) Equivalent circuit. (b) Waveforms.

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_{r1}}{C_r}} \tag{14.2}$$

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_1}\sin(\omega_1 t + \alpha_1) \tag{14.3}$$

Considering the DC component I_L, the peak current is

$$i_{1-peak} = I_L + \frac{V_1}{Z_1} \tag{14.4}$$

14.2.1.1 Interval t = 0 − t_1

Switch S_1 turns on at $t = 0$, and the source current increases linearly with the slope V_1/L_{ri}; this is called current linear rising interval. This current is smaller than the constant load current I_L. Therefore, no current flows through the resonant capacitor C_r.

When $t = t_1$, it is equal to I_L. Therefore, the time is

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$$t_1 = \frac{I_L L_{r_1}}{V_1} \tag{14.5}$$

and the corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{I_L Z_1}{V_1}\right) \tag{14.6}$$

14.2.1.2 Interval $t = t_1 - t_2$

In this period, the current flows through the resonant capacitor C_r. Circuit $L_{r_1} - C_r$ resonates; this is called the resonance interval. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L and then 0 if the converter works in the subresonance state. Switch S_1 turns off at $t = t_2$. At this point, we can see that the switch S_1 turns off at zero-current (ZC) condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \tag{14.7}$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{C_o} of the capacitor voltage v_C is

$$v_{C_o} = V_1[1 + \sin(\pi/2 + \alpha_1)] = V_1(1 + \cos\alpha_1) \tag{14.8}$$

14.2.1.3 Interval $t = t_2 - t_3$

Since the switch S_1 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L; this is the linear recovering interval. Because load current I_L is a constant current, the voltage v_C decreases linearly from v_{C_o} to 0 at $t = t_3$:

$$t_3 = \frac{v_{C_o} C_r}{I_L} \tag{14.9}$$

14.2.1.4 Interval $t = t_3 - t_4$

Capacitor voltage v_C cannot decrease to a negative value because of the freewheeling diode D_2; this is called normal switch-off interval. The load current commutates from C_r to D_2 at $t = t_3$. Since then, the load current freewheels through the main inductor L, load voltage source V_2, and freewheeling diode D_2. The time length t_4 of this period depends on the design requirement. Ignoring the power losses and $I_2 = I_L$, we have the input average current I_1:

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$$I_1 = \frac{1}{T}\int_0^{t_1+t_2+t_3+t_4} i_{L_{r1}}dt = \frac{1}{T}\int_0^{t_1+t_2} i_{L_{r1}}dt = \frac{t_1+t_2}{T}I_L + \frac{1}{T}\int_0^{t_1+t_2}(i_{L_{r1}} - I_L)dt$$

$$= \frac{t_1+t_2}{T}I_L + \frac{1}{T}\int_0^{t_1+t_2} i_r dt = \frac{t_1+t_2}{T}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2+\alpha_1}\right)$$

$$\frac{I_L V_2}{V_1} = I_1 = \frac{t_1+t_2}{T}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2+\alpha_1}\right) \tag{14.10}$$

Because

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.11}$$

$$T = t_1 + t_2 + t_3 + t_4 = \frac{t_1+t_2}{I_1}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2+\alpha_1}\right)$$

Therefore,

$$t_4 = \frac{V_1(t_1+t_2)}{V_2 I_L}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2+\alpha_1}\right) - (t_1+t_2+t_3)$$

We have the conduction duty:

$$k = \frac{t_1+t_2}{t_1+t_2+t_3+t_4}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.14}$$

14.2.2 Mode B

Mode B is a ZCS boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.3. There are four time regions for the switch-on and switch-off period. The conduction duty cycle is $kT = (t_1 + t_2)$, but the output current only flows through the source V_1 in the period t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r2} - C_r$.

The resonance frequency is

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$$\omega_2 = \frac{1}{\sqrt{L_{r_2} C_r}} \tag{14.15}$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_{r_2}}{C_r}} \tag{14.16}$$

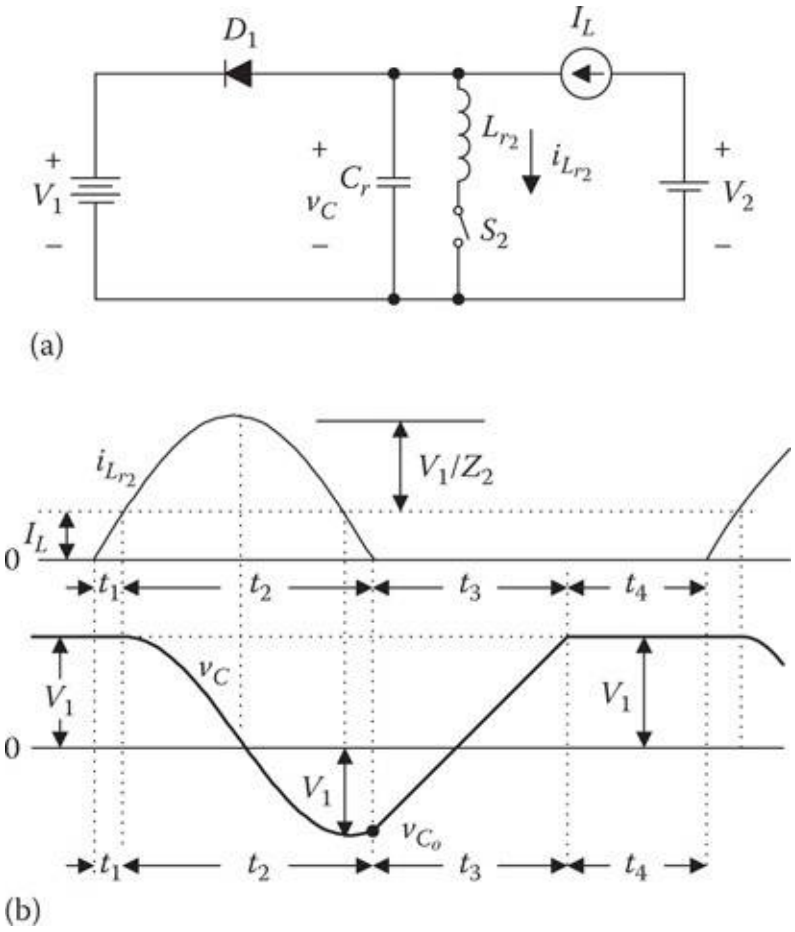


FIGURE 14.3
Mode B operation. (a) Equivalent circuit. (b) Waveforms.

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_2} \sin(\omega_2 t + \alpha_2) \tag{14.17}$$

Considering the DC component I_L, the peak current is

$$i_{2-peak} = I_L + \frac{V_1}{Z_2} \tag{14.18}$$

14.2.2.1 Interval t = 0 − t_1

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Switch S_2 turns on at $t = 0$; the voltage across capacitor C_r is equal to V_1. The inductor current $i_{L_{r2}}$ increases linearly with the slope V_1/L_{r1}. This current is smaller than the constant load current I_L. Therefore, no current flows through the resonant capacitor C_r.

When $t = t_1$, it is equal to I_L. Therefore, the time is

$$t_1 = \frac{I_L L_{r2}}{V_1} \tag{14.19}$$

and the corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_1}\right) \tag{14.20}$$

14.2.2.2 Interval $t = t_1 - t_2$

In this period, the current flows through the resonant capacitor C_r. Circuit $L_{r2} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L and then 0 if the converter works in the subresonance state. Switch S_2 turns off at $t = t_2$.

At this point, we can see that the switch S_2 turns off at ZC condition. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \tag{14.21}$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{C_o} of the capacitor voltage v_C is

$$v_{C_o} = -V_1 \sin(\pi/2 + \alpha_2) = -V_1 \cos\alpha_2 \tag{14.22}$$

14.2.2.3 Interval $t = t_2 - t_3$

Since the switch S_2 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L. Because load current I_L is a constant current, the voltage v_C increases linearly from v_{C_o} to V_1 at $t = t_3$:

$$t_3 = \frac{(V_1 - v_{C_o})C_r}{I_L} \tag{14.23}$$

14.2.2.4 Interval $t = t_3 - t_4$

Capacitor voltage v_C cannot be higher than V_1 because of the diode D_1 conducted. The main inductor current commutates from C_r to D_1 at $t = t_3$. Since then, the load current flows through the main inductor L, diode D_1, source voltage V_1, and load voltage V_2. The time length t_4 of this period depends on the design requirement. Ignoring the power losses and $I_2 = I_L$, we have the output average current I_1 as follows:

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$$I_1 = \frac{I_L V_2}{V_1} = \frac{t_4}{T} I_L \tag{14.24}$$

or

$$\frac{V_2}{V_1} = \frac{t_4}{T} = \frac{t_4}{t_1 + t_2 + t_3 + t_4} \tag{14.25}$$

Therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} \tag{14.26}$$

We have the conduction duty as follows:

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \tag{14.27}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.28}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.29}$$

14.2.3 Mode C

Mode C is a ZCS buck-boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.4. There are four time regions for the switch-on and switch- off period. The conduction duty cycle is $kT = (t_1 + t_2)$ when the input current flows through the switch S_1 and the main inductor L. The output current only flows through V_2 in t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r1} - C_r$.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_n C_r}} \tag{14.30}$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_n}{C_r}} \tag{14.31}$$

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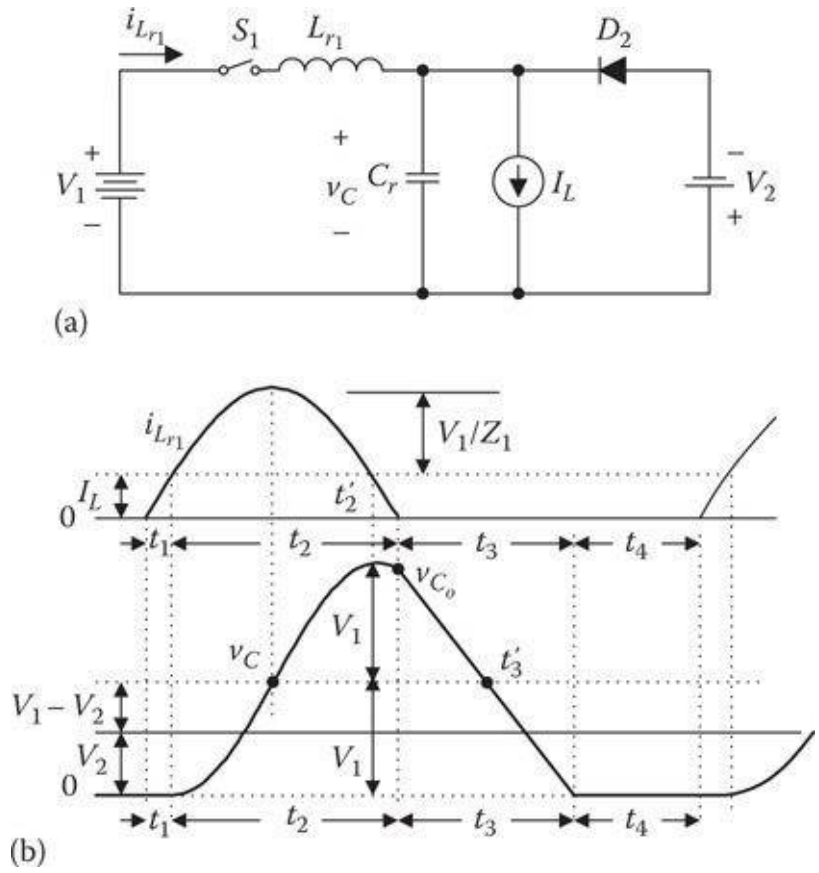


FIGURE 14.4
Mode C operation. (a) Equivalent circuit. (b) Waveforms.

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_1}\sin(\omega_1 t + \alpha_1) \tag{14.32}$$

Considering the DC component I_L, the peak current is

$$i_{1-peak} = I_L + \frac{V_1}{Z_1} \tag{14.33}$$

14.2.3.1 Interval t = 0−t_1

Switch S_1 turns on at $t = 0$, and the voltage across capacitor C_r is equal to V_2. The inductor current $i_{L_{r1}}$ increases linearly with the slope $(V_1 + V_2)/L_{r1}$. This current is smaller than the constant load current I_L. Therefore, no current flows through the resonant capacitor C_r.

When $t = t_1$, it is equal to I_L. Therefore, the time is

$$t_1 = \frac{I_L L_{r1}}{V_1 + V_2} \tag{14.34}$$

and the corresponding angular position is

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$$\alpha_1 = \sin^{-1}\left(\frac{I_L Z_1}{V_1}\right) \tag{14.35}$$

Before S_1 turns on at $t = 0$, freewheeling diode D_2 is conducted. Therefore, the capacitor voltage v_C across the resonant capacitor C_r is equal to V_2 in this interval.

14.2.3.2 Interval $t = t_1 - t_2$

In this period, the current flows through the resonant capacitor C_r. Circuit $L_{r1} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L and then 0 if the converter works in the subresonance state. Switch S_1 turns off at $t = t_2$.

Till this point, we can see that the switch S_1 turns off at ZC condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \tag{14.36}$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. The resonant amplitude is equal to V_1. When $t = t_2$, the corresponding value v_{C0} of the capacitor voltage v_C is

$$v_{C_o} = V_1 - V_2 + V_1 \sin(\pi/2 + \alpha_1) = V_1(1 + \cos\alpha_1) - V_2 \tag{14.37}$$

14.2.3.3 Interval $t = t_2 - t_3$

Since the switch S_1 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L. Because load current I_L is a constant current, the voltage v_C decreases linearly from v_{C_o} to $-|V_2|$ at $t = t_3$. In this interval, the freewheeling diode D_2 does not conduct because it is reversibly biased,

$$t_3 = \frac{(v_{C_o} + V_2)C_r}{I_L} = \frac{V_1(1 + \cos\alpha_1)}{I_L} C_r \tag{14.38}$$

14.2.3.4 Interval $t = t_3 - t_4$

Capacitor voltage v_C is equal to V_2 at $t = t_3$; the freewheeling diode D_2 is then conducted. The main inductor current commutates from C_r to V_2 at $t = t_3$. Since then, the load current freewheels through the main inductor L, load voltage source V_2, and freewheeling diode D_2. The time length t_4 of this period depends on the design requirement. Ignoring the power losses, we have the input average current I_1 as follows:

$$I_1 = \frac{t_1 + t_2}{T}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2 + \alpha_1}\right) \tag{14.39}$$

and

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$$I_2 = \frac{t_4}{T} I_L \tag{14.40}$$

Therefore,

$$t_4 = \frac{V_1(t_1 + t_2)}{V_2 I_L}\left(I_L + \frac{V_1}{Z_1}\frac{\cos\alpha_1}{\pi/2 + \alpha_1}\right) \tag{14.41}$$

We have the conduction duty as follows:

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \tag{14.42}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.43}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.44}$$

14.2.4 Mode D

Mode D is a ZCS buck-boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.5. There are four time regions for the switch-on and switch- off period. The conduction duty cycle is $kT = (t_1 + t_2)$, but the output current only flows through the source V_1 in the period t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_{r2} - C_r$.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_{r_2} C_r}} \tag{14.45}$$

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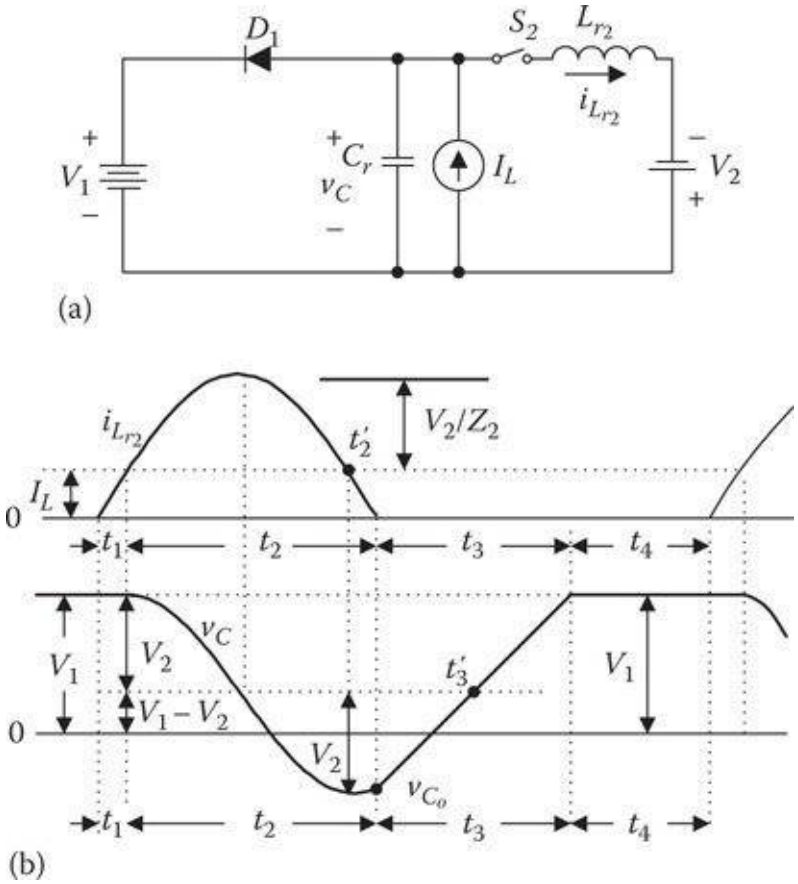


FIGURE 14.5
Mode D operation. (a) Equivalent circuit. (b) Waveforms.

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_{r2}}{C_r}} \tag{14.46}$$

The resonant current (AC component) is

$$i_r(t) = \frac{V_1}{Z_2}\sin(\omega_2 t + \alpha_2) \tag{14.47}$$

Considering the DC component I_L, the peak current is

$$i_{2-peak} = I_L + \frac{V_1}{Z_2} \tag{14.48}$$

14.2.4.1 Interval t = 0 − t_1

Switch S_2 turns on at $t = 0$, and the voltage across capacitor C_r is equal to V_1. The inductor current $i_{L_{r2}}$ increases linearly with the slope $(V_1 + V_2)/L_{r2}$. This current is smaller than the constant load current I_L. Therefore, no current flows through the resonant capacitor C_r.

When $t = t_1$, it is equal to I_L. Therefore, the time is

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$$t_1 = \frac{I_L L_{r2}}{V_1 + V_2} \tag{14.49}$$

and the corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{I_L Z_2}{V_2}\right) \tag{14.50}$$

14.2.4.2 Interval $t = t_1 - t_2$

In this period, the current flows through the resonant capacitor C_r. Circuit $L_{r2} - C_r$ resonates. The current waveform is a sinusoidal function. After its peak value, current descends down to I_L and then 0 if the converter works in the subresonance state. Switch S_2 turns off at $t = t_2$.

At this point, we can see that the switch S_2 turns off at ZC condition. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \tag{14.51}$$

Simultaneously, the voltage across the capacitor C_r is a sinusoidal function as well. When $t = t_2$, the corresponding value v_{C_o} of the capacitor voltage v_C is

$$v_{C_o} = (V_1 - V_2) - V_2 \sin(\pi/2 + \alpha_2) = V_1 - V_2(1 + \cos\alpha_2) \tag{14.52}$$

14.2.4.3 Interval $t = t_2 - t_3$

Since the switch S_2 does not allow the resonant current to flow reversibly, the charge across the capacitor C_r will be discharged by the load current I_L. Because load current I_L is a constant current, the voltage v_C increases linearly from v_{C_o} to V_1 at $t = t_3$ as follows:

$$t_3 = \frac{(V_1 - v_{C_o})C_r}{I_L} = \frac{V_2 C_r}{I_L}(1 + \cos\alpha_2) \tag{14.53}$$

14.2.4.4 Interval $t = t_3 - t_4$

Capacitor voltage v_C cannot be higher than V_1 because of the diode D_1 conducted. The main inductor current commutates from C_r to D_1 at $t = t_3$. Since then, the output current I_1 flows through the main inductor L, diode D_1, source voltage V_1, and load voltage V_2. The time length t_4 of this period depends on the design requirement. Ignoring the power losses, we have the output average current I_1 as follows:

$$I_1 = \frac{I_L V_2}{V_1} = \frac{t_4}{T} I_L \tag{14.54}$$

Also,

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$$I_2 = \frac{t_1 + t_2}{T}\left(I_L + \frac{V_2}{Z_2}\frac{\cos\alpha_2}{\pi/2 + \alpha_2}\right) \tag{14.55}$$

Therefore,

$$t_4 = \frac{V_2(t_1 + t_2)}{V_1 I_L}\left(I_L + \frac{V_2}{Z_2}\frac{\cos\alpha_2}{\pi/2 + \alpha_2}\right) \tag{14.56}$$

We have the conduction duty as follows:

$$k = \frac{t_1 + t_2}{t_1 + t_2 + t_3 + t_4} \tag{14.57}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.58}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.59}$$

14.2.5 Experimental Results

A testing rig with a battery of ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are V_1 = 42 V and V_2 = ±28 V, L = 30 αH, $L_{r1} = L_{r2}$ = 1 μH, and C_r = 4 μF; the volume is 40 in.^{3}. The experimental results are shown in Table 14.2. The average power transfer efficiency is 96.3%, and the total average PD is 17.1 W/in.^{3}. This figure is much higher than the classical converters whose PD is usually less than 5 W/in.^{3}. Since the switch frequency is low (f < 41 kHz) and this converter works at the monoresonance frequency, the components of the high-order harmonics are small. Applying fast Fourier transform (FFT) analysis, the total harmonic distortion (THD) is very small; thus, the EMI is weak, and the EMS and EMC are reasonable.

TABLE 14.2
Experimental Results for Different Frequencies

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Mode	f (kHz)	$L_{r_1} = L_{r_2}$ (μH)	C_r (μF)	I_i (A)	I_o (A)	I_L (A)	P_i (W)	P_o (W)	η (%)	PD (W/in.^{3})
A	20.5	1	4	16.98	25	25	713	700	98.2	17.66
A	21	1	4	17.4	25	25	730.6	700	95.8	17.88
A	21.5	1	4	17.81	25	25	748	700	93.5	18.1
B	16.5	1	4	25	16.4	25	700	688.8	98.4	17.36
B	17	1	4	25	16.2	25	700	680.4	97.2	17.25
B	17.5	1	4	25	15.97	25	700	670.1	95.8	17.13
C	19	1	4	16.17	23.82	35	679.1	667	98.2	16.83
C	19.3	1	4	16.42	23.64	35	689.7	662	96	16.9
C	19.5	1	4	16.59	23.53	35	696.8	658.8	94.5	16.95
D	40	1	4	24.05	15.64	35	663.4	656.8	97.5	16.5
D	40.3	1	4	24.23	15.49	35	678.5	650.6	95.9	16.6
D	40.5	1	4	24.35	15.4	35	681.8	646.7	94.8	16.61

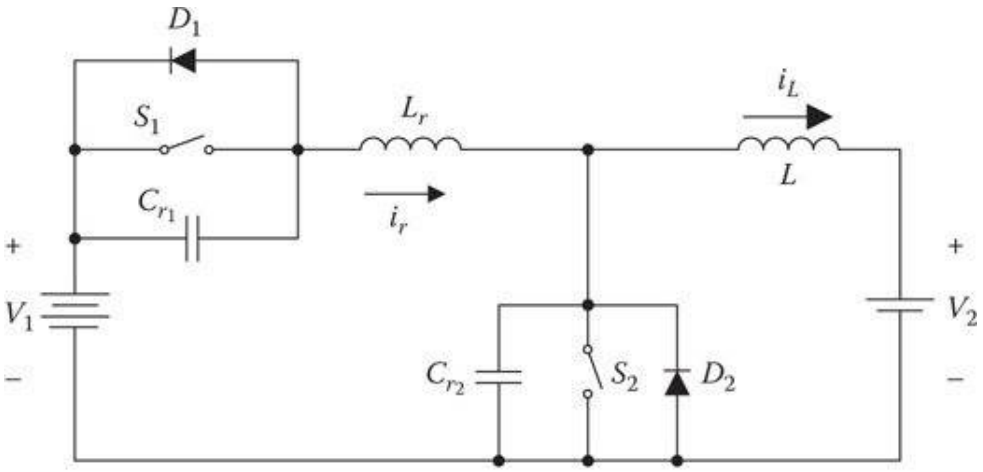
14.3 Multiple-Quadrant DC/DC ZVS Quasi-Resonant Luo-Converters

Many industrial applications require the multiquadrant operation with ZVS technique, since it significantly reduces the power losses. Unfortunately, most of the papers discuss the ZVS converters only working at single-quadrant operation. Four-quadrant DC/DC ZCS quasi-resonant Luo-converter effectively reduces the power losses and largely increases the power transfer efficiency. This is shown in Figure 14.6. Circuit 1 implements the operation in quadrants I and II; Circuit 2 implements the operation in quadrants III and IV. Circuit 1 and Circuit 2 can be converted to each other by an auxiliary changeover switch S_3, which is illustrated in Circuit 3. Each circuit consists of one main inductor L and two switches. Assuming that the main inductance L is sufficiently large, the current i_L is constant. The source and load voltages are usually constant, for example, V_1 = 42 V and V_2 = ±28 V. There are four modes of operation as follows:

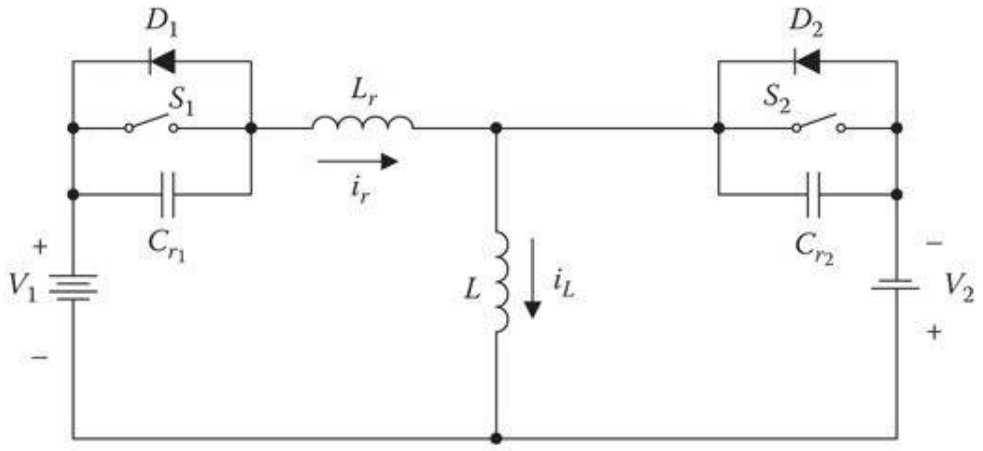
1. *Mode A (quadrant I):* Electrical energy is transferred from V_1 side to V_2 side.
2. *Mode B (quadrant II):* Electrical energy is transferred from V_2 side to V_1 side.
3. *Mode C (quadrant III):* Electrical energy is transferred from V_1 side to $-V_2$ side.
4. *Mode D (quadrant IV):* Electrical energy is transferred from $-V_2$ side to V_1 side.

Each mode has two states: “on” and “off.” The switch/diode status of each state is shown in Table 14.3.

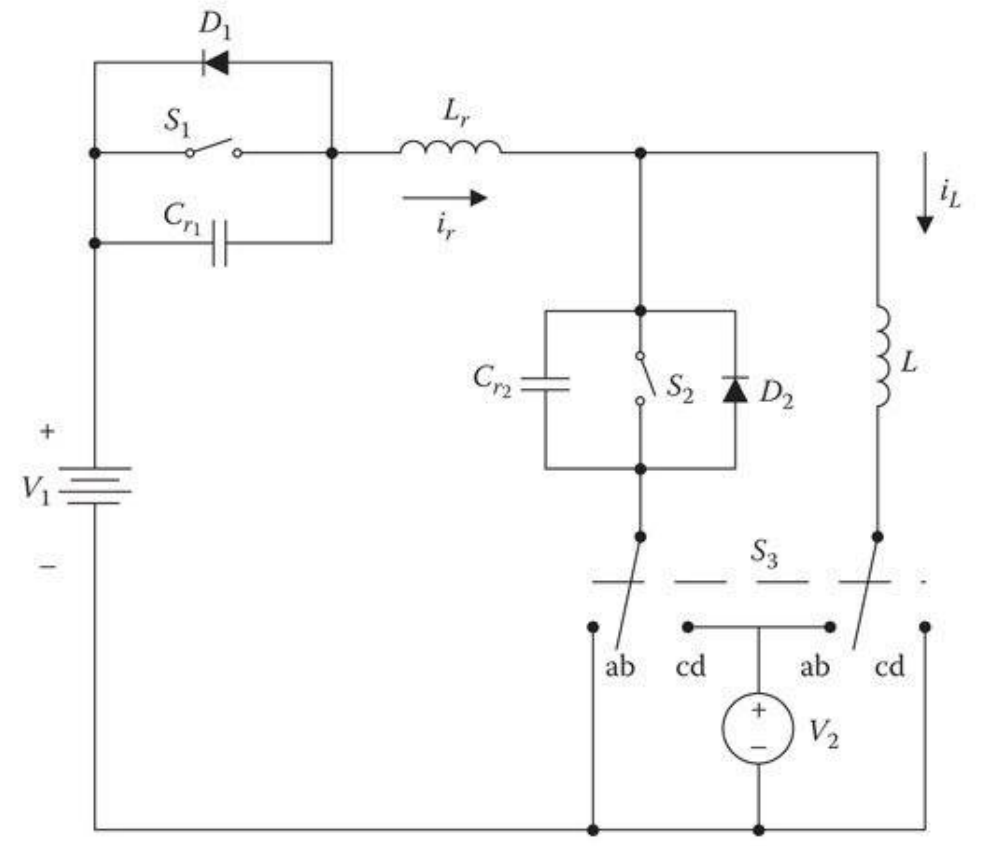
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(a)



(b)



(c)

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FIGURE 14.6
Four-quadrant DC/DC zero-voltage-switch quasi-resonant Luo-converter. (a) Circuit 1 for the operation in quadrant I and quadrant II. (b) Circuit 2 for the operation in quadrant III and quadrant IV. (c) Circuit 3 for the four quadrants.

TABLE 14.3
Switch's Status (the Blank Status Means Off)

Switch or Diode	Mode A (quadrant I)		Mode B (quadrant II)		Mode C (quadrant III)		Mode D (quadrant IV)	
	State-On	State-Off	State-On	State-Off	State-On	State-Off	State-On	State-Off
Circuit	Circuit 1				Circuit 2			
S_1	On				On			
D_1			On					On
S_2			On				On	
D_2		On				On		

14.3.1 Mode A

Mode A is a ZVS buck converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.7. There are four time regions for the switch-off and switch-on period. The conduction duty cycle is $kT = (t_3 + t_4)$ when the input current flows through the switch S_1 and the main inductor L. The whole period is $T = (t_2 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r1}$.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r1}}} \tag{14.60}$$

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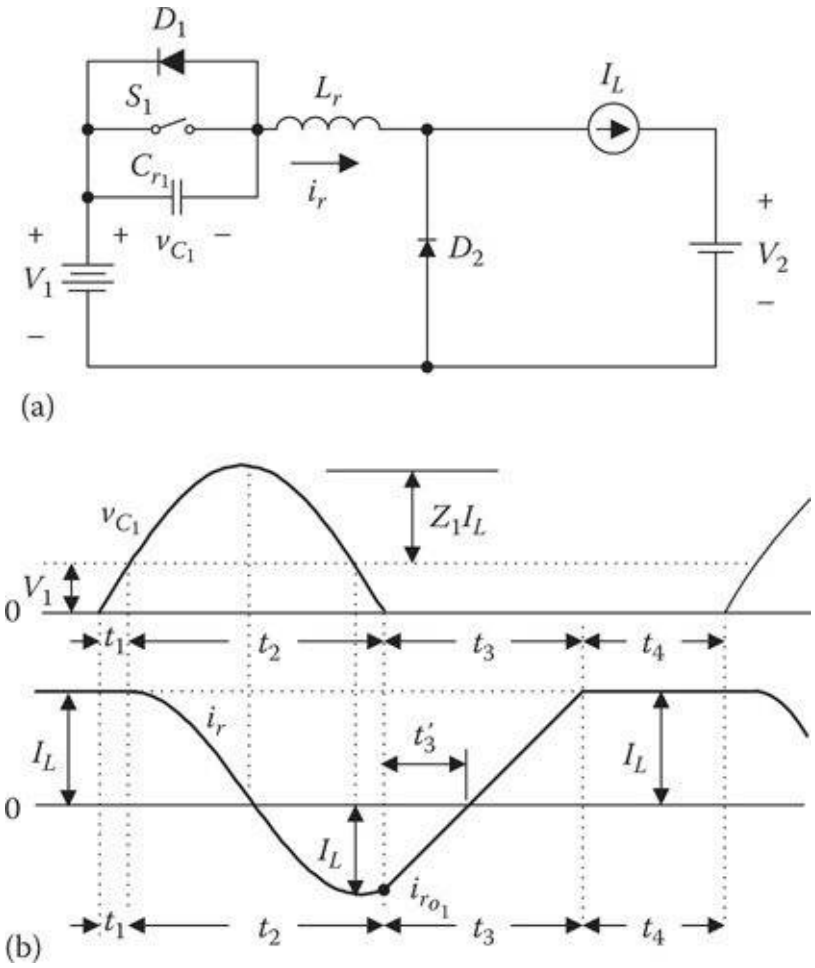


FIGURE 14.7
Mode A operation. (a) Equivalent circuit. (b) Waveforms.

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_r}{C_n}} \tag{14.61}$$

The resonant voltage (AC component) is

$$v_{C_1}(t) = Z_1 I_L \sin(\omega_1 t + \alpha_1) \tag{14.62}$$

Considering the DC component V_1, the peak voltage is

$$v_{C_1-peak} = V_1 + Z_1 I_L \tag{14.63}$$

14.3.1.1 Interval $t = 0 - t_1$

Switch S_1 turns off at $t = 0$, and the capacitor voltage v_{C_1} increases linearly with the slope I_L/C_{r_1}; this is voltage linear rising interval. This voltage is smaller than the source voltage V_1. Therefore, no current flows through the diode D_2.

When $t = t_1$, it is equal to V_1. Therefore, the time is

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$$t_1 = \frac{V_1 C_{r1}}{I_L} \tag{14.64}$$

and the corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{V_1}{Z_1 I_L}\right) \tag{14.65}$$

14.3.1.2 Interval $t = t_1 - t_2$

In this period, since the voltage v_{C_1} is higher than the source voltage V_1, the current flows through the diode D_2. Circuit L_r–C_{r1} resonates; this is called the resonance interval. The voltage waveform is a sinusoidal function. After its peak value v_{C_1-peak}, it descends down to zero ($t = t_2$). If the converter works in the subresonance state, switch S_1 turns on at $t = t_2$. At this point, we can see that the switch S_1 turns off and turns on at zero-voltage condition. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \tag{14.66}$$

Simultaneously, the current i_r flows through the inductor L_r; it is a sinusoidal function as well. When $t = t_2$, the corresponding value $i_{r_{o1}}$ of the inductor current i_r is

$$i_{r_{o1}} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos\alpha_1 \tag{14.67}$$

14.3.1.3 Interval $t = t_2 - t_3$

Since the diode D_1 does not allow the resonant voltage v_{C_1} to become a negative value, then $v_{C_1} = 0$. The freewheeling diode D_2 conducts and the current i_r increases linearly with the slope V_1/L_r; this is the inductor current linear recovering interval. Because load current I_L is a constant current, the current i_r increases linearly from $i_{r_{o1}}$ to 0 at $t = t_3'$, and $i_{r_{o1}} = I_L$ at $t = t_3$.

$$t_3' = -\frac{i_{r_{o1}} L_r}{V_1} \tag{14.68}$$

and

$$t_3 = \frac{(I_L - i_{r_{o1}})L_r}{V_1} = \frac{I_L(1 + \cos\alpha_1)L_r}{V_1} \tag{14.69}$$

14.3.1.4 Interval $t = t_3 - t_4$

In this period, the load current is supplied by the source. Diode D_2 is blocked until $t = t_4$; this is the normal switch-on interval. The output current is equal to the main inductor current I_L, so the average input current I_1 is

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$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L \tag{14.70}$$

Therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1 / V_2 - 1} \tag{14.71}$$

We have the conduction duty as follows:

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \tag{14.72}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.73}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.74}$$

14.3.2 Mode B

Mode B is a ZVS boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.8. There are four time regions for the switch-off and switch-on period. The conduction duty cycle is $kT = (t_3 + t_4)$, but the output current only flows through the source V_1 in the period t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is $L_r - C_{r2}$.

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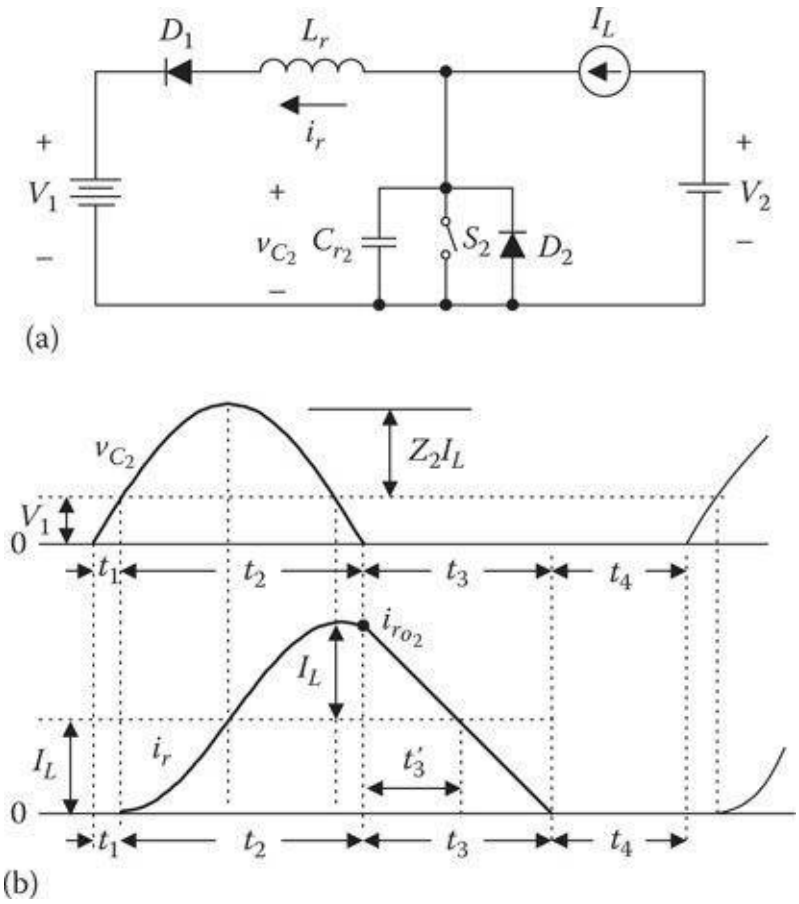


FIGURE 14.8
Mode B operation. (a) Equivalent circuit. (b) Waveforms.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \tag{14.75}$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \tag{14.76}$$

The resonant voltage (AC component) is

$$v_{C_2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \tag{14.77}$$

Considering the DC component V_1, the peak current is

$$v_{C_2\text{-}peak} = V_1 + Z_2 I_L \tag{14.78}$$

14.3.2.1 Interval $t = 0 - t_1$

Switch S_2 turns off at $t = 0$, and the capacitor voltage v_{C_2} increases linearly with the slope I_L/C_{r2}. This voltage is equal to V_1 when $t = t_1$.

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$$t_1 = \frac{V_1 C_{r2}}{I_L} \tag{14.79}$$

and the corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{V_1}{Z_2 I_L}\right) \tag{14.80}$$

14.3.2.2 Interval $t = t_1 - t_2$

In this period, the voltage v_{C_2} is higher than the source voltage V_1. Circuit L_r–C_{r2} resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when $t = t_2$. If the converter works in the subresonance state, switch S_2 turns on at $t = t_2$. Until this point, we can see that the switch S_2 turns off and turns on at zero-voltage condition. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \tag{14.81}$$

Simultaneously, the inductor current i_r flows through inductor L_r; it is a sinusoidal function as well. When $t = t_2$, the corresponding value $i_{r_{o2}}$ of the inductor current i_r is

$$i_{r_{o2}} = I_L[1 + \sin(\pi/2 + \alpha_2)] = I_L(1 + \cos\alpha_2) \tag{14.82}$$

14.3.2.3 Interval $t = t_2 - t_3$

Since the diode D_2 does not allow the resonant voltage to become a negative value, the voltage across the capacitor C_{r2} will be 0. The inductor current i_r decreases linearly with the slope—V_1/L_r. Because load current I_L is a constant current, the current i_r decreases linearly from $i_{r_{o_2}}$ to I_L at $t = t'_3$, and $i_r = 0$ at $t = t_3$.

$$t'_3 = \frac{(i_{r_{o_2}} - I_L)L_r}{V_1} \tag{14.83}$$

$$t_3 = \frac{i_{r_{o_2}} L_r}{V_1} \tag{14.84}$$

14.3.2.4 Interval $t = t_3 - t_4$

In this period, the switch S_2 is on. Load current I_L does not flow through the source. Ignoring the power losses and $I_2 = I_L$, we have the output average current I_1 as follows:

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_1}^{t_3} i_r dt \approx \frac{1}{T}[I_L(t_2 + t_3)] = \frac{t_2 + t_3}{T} I_L \tag{14.85}$$

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or

$$\frac{V_2}{V_1} = \frac{1}{T}(t_2 + t_3) = \frac{t_2 + t_3}{t_1 + t_2 + t_3 + t_4} \tag{14.86}$$

Therefore,

$$t_4 = \left(\frac{V_1}{V_2} - 1\right)(t_2 + t_3) - t_1 \tag{14.87}$$

We have the conduction duty as follows:

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \tag{14.88}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.89}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.90}$$

14.3.3 Mode C

Mode C is a ZVS buck-boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.9. There are four time regions for the switch-off and switch-on period. The conduction duty cycle is $kT = (t_3 + t_4)$ when the input current I_1 flows through the switch S_1 and the main inductor L. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is L_r–C_{r1}.

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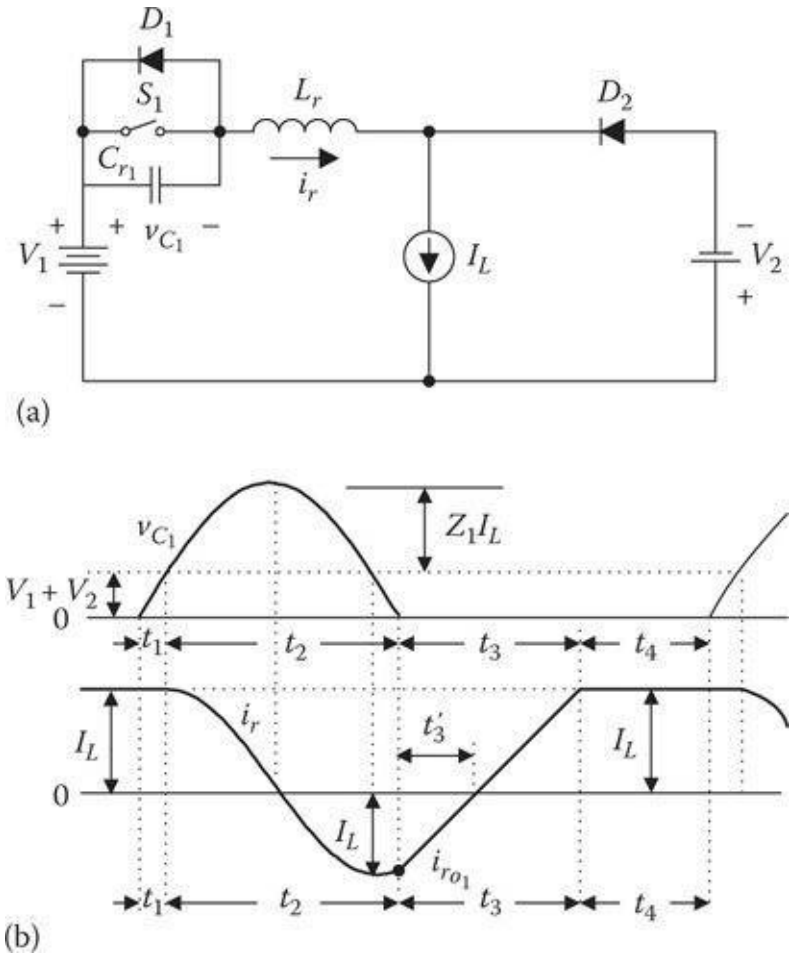


FIGURE 14.9
Mode C operation. (a) Equivalent circuit. (b) Waveforms.

The resonance frequency is

$$\omega_1 = \frac{1}{\sqrt{L_r C_{r_1}}} \tag{14.91}$$

and the normalized impedance is

$$Z_1 = \sqrt{\frac{L_r}{C_{r_1}}} \tag{14.92}$$

The resonant voltage (AC component) is

$$v_{C_1}(t) = Z_1 I_L \sin(\omega_1 t + \alpha_1) \tag{14.93}$$

Considering the DC component V_1, the peak voltage is

$$v_{C_1-peak} = V_1 + V_2 + Z_1 I_L \tag{14.94}$$

14.3.3.1 Interval $t = 0 - t_1$

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Switch S_1 turns off at $t = 0$; the capacitor voltage v_{C_1} increases linearly with the slope I_L/C_{r1}. This voltage v_{C_1} is smaller than $(V_1 + V_2)$. Therefore, no current flows through the diode D_2. When $t = t_1$, it is equal to $(V_1 + V_2)$. Therefore,

$$t_1 = \frac{(V_1 + V_2)C_n}{I_L} \tag{14.95}$$

and the corresponding angular position is

$$\alpha_1 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_1 I_L}\right) \tag{14.96}$$

14.3.3.2 Interval $t = t_1 - t_2$

In this period, since the voltage v_{C_1} is higher than the source voltage V_1, the current flows through the diode D_2. Circuit L_r–C_{r1} resonates. The voltage waveform is a sinusoidal function. After its peak value v_{C_1-peak}, it descends down to zero ($t = t_2$). If the converter works in the subresonance state, switch S_1 turns on at $t = t_2$. This period length is

$$t_2 = \frac{1}{\omega_1}(\pi + \alpha_1) \tag{14.97}$$

Simultaneously, the current i_r flows through the inductor L_r; it is a sinusoidal function as well. When $t = t_2$, the corresponding value $i_{r_{o1}}$ of the inductor current i_r is

$$i_{r_{o1}} = -I_L \sin(\pi/2 + \alpha_1) = -I_L \cos\alpha_1 \tag{14.98}$$

14.3.3.3 Interval $t = t_2 - t_3$

Since the diode D_1 does not allow the resonant voltage v_{C_1} to become a negative value, then $v_{C_1} = 0$. The freewheeling diode D_2 conducts and the current i_r increases linearly with the slope $(V_1 + V_2)/L_r$. Because load current I_L is a constant current, the current i_r increases linearly from $i_{r_{o1}}$ to 0 at $t = t'_3$, and $i_{r_{o1}} = I_L$ at $t = t_3$ as follows:

$$t'_3 = -\frac{i_{r_{o1}} L_r}{V_1 + V_2} \tag{14.99}$$

and

$$t_3 = \frac{(I_L - i_{r_{o1}})L_r}{V_1 + V_2} = \frac{I_L(1 + \cos\alpha_1)L_r}{V_1 + V_2} \tag{14.100}$$

14.3.3.4 Interval $t = t_3 - t_4$

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In this period, the load current is supplied by the source. Diode D_2 is blocked until $t = t_4$. The output current is equal to the main inductor current I_L, so the average input current I_1 is

$$I_1 = \frac{I_L V_2}{V_1} = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L \tag{14.101}$$

and

$$I_2 = \frac{1}{T}\int_{t_1}^{t_3} (I_L - i_r) dt \approx \frac{t_1 + t_2 + t_3}{T} I_L \tag{14.102}$$

Therefore,

$$t_4 = \frac{V_2(t_1 + t_2 + t_3)}{V_1} \tag{14.103}$$

We have the conduction duty as follows:

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \tag{14.104}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.105}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.106}$$

14.3.4 Mode D

Mode D is a cross ZVS buck-boost converter. The equivalent circuit, current, and voltage waveforms are shown in Figure 14.10. There are four time regions for the switch-off and switch-on period. The conduction duty cycle is $kT = (t_3 + t_4)$, but the output current only flows through the source V_1 in the period t_4. The whole period is $T = (t_1 + t_2 + t_3 + t_4)$. The resonance circuit is L_r–C_{r2}.

The resonance frequency is

$$\omega_2 = \frac{1}{\sqrt{L_r C_{r2}}} \tag{14.107}$$

and the normalized impedance is

$$Z_2 = \sqrt{\frac{L_r}{C_{r2}}} \tag{14.108}$$

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The resonant voltage (AC component) is

$$v_{C_2}(t) = Z_2 I_L \sin(\omega_2 t + \alpha_2) \tag{14.109}$$

Considering the DC component (V_1 + V_2), the peak current is

$$v_{C_2-peak} = V_1 + V_2 + Z_2 I_L \tag{14.110}$$

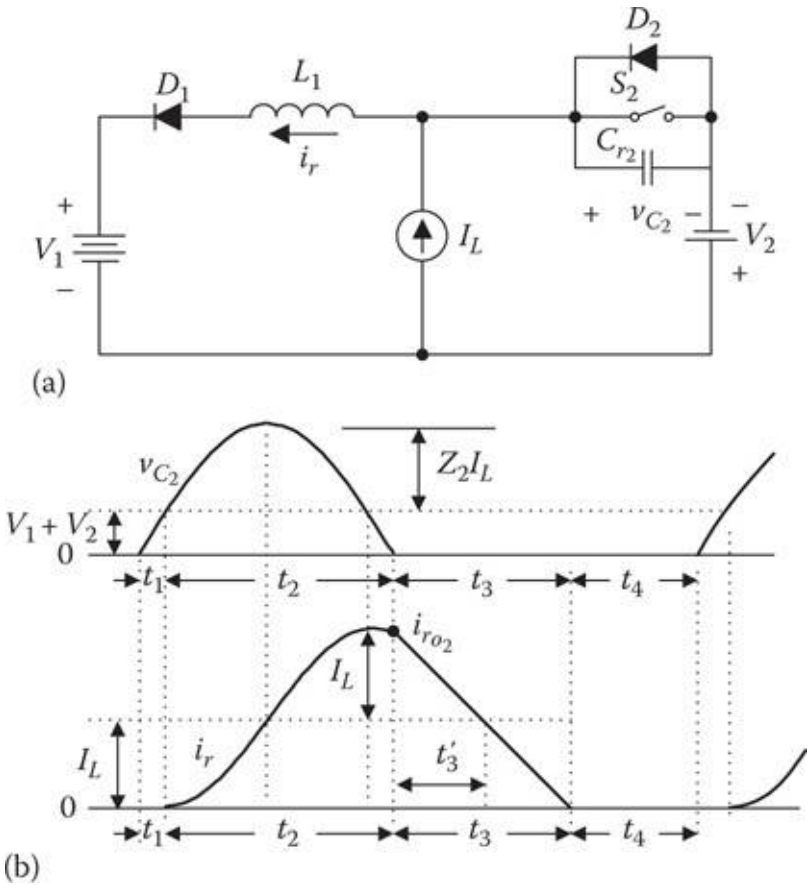


FIGURE 14.10
Mode D operation. (a) Equivalent circuit. (b) Waveforms.

14.3.4.1 Interval t = 0 − t_1

Switch S_2 turns off at t = 0; the capacitor voltage v_{C2} increases linearly with the slope I_L/C_{r2} It is equal to (V_1 + V_2) when $t = t_1$,

$$t_1 = \frac{(V_1 + V_2)C_{r_2}}{I_L} \tag{14.111}$$

The corresponding angular position is

$$\alpha_2 = \sin^{-1}\left(\frac{V_1 + V_2}{Z_2 I_L}\right) \tag{14.112}$$

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14.3.4.2 Interval $t = t_1 - t_2$

In this period, the voltage v_{C_2} is higher than the sum voltage ($V_1 + V_2$). Circuit L_r–C_{r2} resonates. The voltage waveform is a sinusoidal function. After its peak value, it descends down to 0 when $t = t_2$. If the converter works in the subresonance state, switch S_2 turns on at $t = t_2$. This period length is

$$t_2 = \frac{1}{\omega_2}(\pi + \alpha_2) \tag{14.113}$$

Simultaneously, the inductor current i_r flows through inductor L_r; it is a sinusoidal function as well. When $t = t_2$, the corresponding value of the inductor current i_r is

$$i_{r_{o2}} = I_L[1 + \sin(\pi/2 + \alpha_2)] = I_L(1 + \cos\alpha_2) \tag{14.114}$$

14.3.4.3 Interval $t = t_2 - t_3$

Since the diode D_2 does not allow the resonant voltage to become a negative value, the voltage across the capacitor C_{r2} will be 0. The inductor current i_r decreases linearly with the slope $(V_1 + V_2)/L_r$. Because the main inductor current I_L is a constant current, the current i_r decreases linearly from $i_{r_{o2}}$ to I_L at $t = t'_3$, and $i_r = 0$ at $t = t_3$:

$$t'_3 = \frac{(i_{r_{o2}} - I_L)L_r}{V_1 + V_2} \tag{14.115}$$

$$t_3 = \frac{i_{r_{o2}} L_r}{V_1 + V_2} = \frac{I_L(1 + \cos\alpha_2)}{V_1 + V_2} L_r \tag{14.116}$$

14.3.4.4 Interval $t = t_3 - t_4$

In this period, since the switch S_2 is on, the main inductor current I_L does not flow through the source. Ignoring the power losses, we have the output average current I_1 as follows:

$$I_1 = \frac{1}{T}\int_{t_1}^{t_3} i_r dt \approx \frac{1}{T}[I_L(t_1 + t_2 + t_3)] = \frac{t_1 + t_2 + t_3}{T} I_L \tag{14.117}$$

and

$$I_2 = \frac{1}{T}\int_{t_3}^{t_4} i_r dt \approx \frac{1}{T}(I_L t_4) = \frac{t_4}{T} I_L \tag{14.118}$$

Therefore,

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$$t_4 = \left(\frac{V_1}{V_2} - 1\right)(t_1 + t_2 + t_3) \tag{14.119}$$

We have the conduction duty as follows:

$$k = \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} \tag{14.120}$$

The whole repeating period is

$$T = t_1 + t_2 + t_3 + t_4 \tag{14.121}$$

and the corresponding frequency is

$$f = \frac{1}{T} \tag{14.122}$$

14.3.5 Experimental Results

A testing rig with a battery of ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are V_1 = 42 V and V_2 = ±28 V, L = 30 μH, L_r = 4 pH, and C_{r1} = C_{r2} = 1 μF; the volume is 40 in.^{3}. The experimental results are shown in Table 14.4. The average power transfer efficiency is higher than 96%, and the total average PD is 17.6 W/in.^{3}. This figure is much higher than that of the classical converters whose PD is usually less than 5 W/in.^{3}. Since the switch frequency is low (f < 56 kHz) and this converter works at the monoresonance frequency, the components of the high-order harmonics are small. Applying FFT analysis, the THD is very small; thus, the EMI is weak, and the EMS and EMC are reasonable.

TABLE 14.4
Experimental Results for Different Frequencies

Mode	f (kHz)	L_{r_1} (μH)	$C_{r_1} = C_{r_2}$ (μF)	I_i (A)	I_o (A)	I_L (A)	P_i (W)	P_o (W)	η (%)	PD (W/in.^{3})
A	23	4	1	17.16	25	25	720.8	700	97.1	17.76
A	23.5	4	1	16.99	25	25	713.7	700	98.1	17.67
A	24	4	1	16.82	25	25	706.6	700	99	17.58
B	54	4	1	25	16.13	25	700	677.6	96.8	17.22
B	54.5	4	1	25	16.28	25	700	683.8	97.7	17.3
B	55	4	1	25	16.43	25	700	690.1	98.6	17.38
C	44	4	1	17.64	24.27	45	740.9	679.6	91.7	17.76
C	44.5	4	1	17.32	24.55	45	727.6	687.5	94.5	17.69
C	45	4	1	17.01	24.83	45	714.5	695.2	97.3	17.62
D	29.5	4	1	26.65	16.27	45	746.3	683.5	91.6	17.87
D	30	4	1	26.34	16.55	45	737.6	695.1	94.2	17.91
D	30.5	4	1	26.28	16.83	45	735.9	706.7	96	18.03

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14.4 Multiple-Quadrant ZT DC/DC Luo-Converters

ZT technique significantly reduces the power losses across the switches during switch-on and switch-off. Unfortunately, the literature discusses the converters only working at single-quadrant operation. The four-quadrant ZT DC/DC Luo-converters perform soft-switching four-quadrant operation without significant voltage and current stresses. They effectively reduce the power losses and greatly increase the power transfer efficiency.

These converters are shown in Figure 14.11a and b. Circuit 1 implements the operation in quadrants I and II. Circuit 2 implements the operation in quadrants III and IV. Circuit 1 and Circuit 2 can be converted to each other via an auxiliary switch. Each circuit consists of one main inductor L and two main switches. The source and load voltages are usually constant, for example, $V_1 = 42$ V and $V_2 = \pm 28$ V. There are four modes of operation:

1. *Mode A (quadrant I):* Electrical energy is transferred from V_1 side to V_2 side.
2. *Mode B (quadrant II):* Electrical energy is transferred from V_2 side to V_1 side.
3. *Mode C (quadrant III):* Electrical energy is transferred from V_1 side to $-V_2$ side.
4. *Mode D (quadrant IV):* Electrical energy is transferred from $-V_2$ side to V_1 side.

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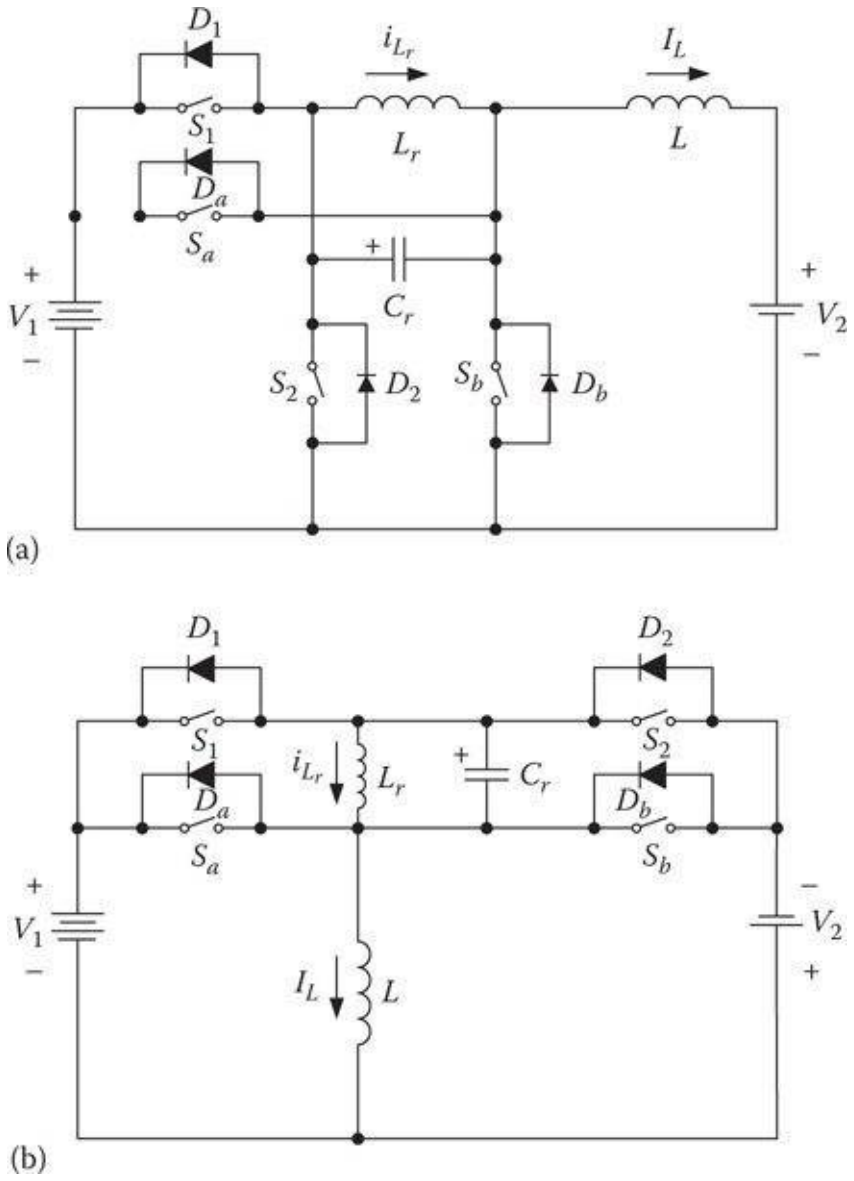


FIGURE 14.11
Four-quadrant zero-transition DC/DC Luo-converters. (a) Circuit 1 for operation Modes A and B. (b) Circuit 2 for operation Modes C and D.

TABLE 14.5
Switch/Diode Status (the Blank Status Means Off) Referring to Circuit 1 of Figure 14.11a

	Mode A (Quadrant I)								Mode B (Quadrant II)							
S* and *D	Δt_1	Δt_2	Δt_3	Δt_4	Δt_5	Δt_6	Δt_7	Δt_8	Δt_1	Δt_2	Δt_3	Δt_4	Δt_5	Δt_6	Δt_7	Δt_8
S_1				*On*	*On*	*On*										
D_1									*On*							*On*
S_a	*On*	*On*	*On*													
D_a															*On*	*On*
S_2												*On*	*On*	*On*		
D_2	*On*							*On*								
S_b									*On*	*On*	*On*					
D_b							*On*	*On*								

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TABLE 14.6
Switch/Diode Status (the Blank Status Means Off) Referring to Circuit 2 of Figure 14.11b

	Mode C (Quadrant III)								Mode D (Quadrant IV)							
S and D	Δt_1	Δt_2	Δt_3	Δt_4	Δt_5	Δt_6	Δt_7	Δt_8	Δt_1	Δt_2	Δt_3	Δt_4	Δt_5	Δt_6	Δt_7	Δt_8
S_1				On	On	On										
D_1									On							On
S_a	On	On	On													
D_a															On	On
S_2												On	On	On		
D_2	On							On								
S_b									On	On	On					
D_b							On	On								

Each mode has two states: "on" and "off." The switch and diode status of each state for Modes A and B are shown in Table 14.5; the status of each state for Modes C and D is shown in Table 14.6.

The equivalent circuits for Modes A, B, C, and D are shown in Figures 14.12, 14.14, 14.16, and 14.18. The corresponding waveforms for each mode are shown in Figures 14.13, 14.15, 14.17, and 14.19, respectively.

14.4.1 Mode A (Quadrant I Operation)

Mode A performs quadrant I operation. The equivalent circuit for Modes A is shown in Figure 14.12. The corresponding waveforms are shown in Figure 14.13.

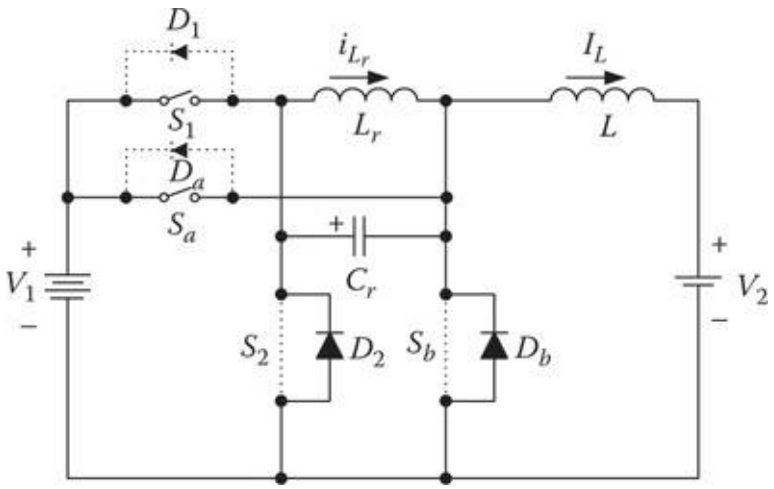


FIGURE 14.12
Mode A (quadrant I) operation.

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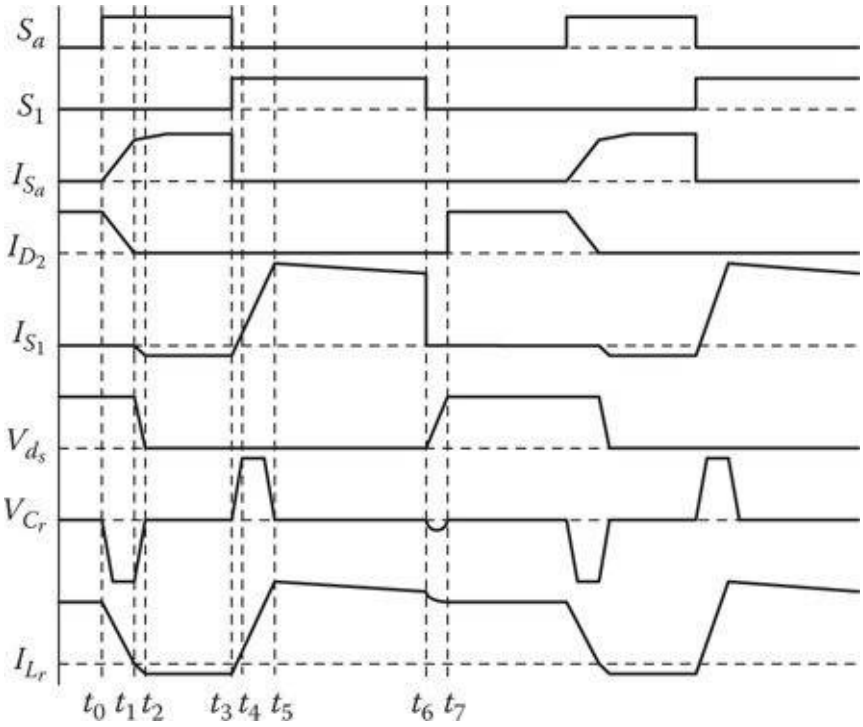


FIGURE 14.13
Waveforms of Mode A (quadrant I).

Stage 1 (t_0 − t_1): Prior to t_0, S_1 and S_a are all off. The circuit current is freewheeling through the antiparallel diode D_b and D_2. C_r voltage is zero; $I_L = I_{L_r} + I_{Db}$. At t_0, the auxiliary switch S_a is turned on with zero current. Capacitor C_r is charged in reverse so that diode D_b is reverse biased in soft commutation. The current of L_r decreases linearly, while the current of S_a increases gradually. At $t = t_1$, the current of L_r falls to zero; D_2 is turned off with soft commutation. Meanwhile, current of S_a reaches to I_L. The current of resonant inductor L_r is $i_{Lr} = (V_1/L_r)t$

The time interval of the first stage Δt_1 is given by the following equation:

$$\Delta t_1 = \frac{I_L L_r}{V_1} \tag{14.123}$$

Stage 2 (t_1−t_3): The main switch S_1's junction capacitor C_j (not shown in Figure 14.12) discharges through L_r, S_a. Capacitor C_r also discharges through L_r. V_{Cr} and V_{ds} fall to zero rapidly at t_2. Thereafter, the antiparallel diode of S_j starts to conduct and a small reverse current flows through L_r. The resonant time interval of stage 2, Δt_2, is given by

$$\Delta t_2 = \frac{\pi}{2}\sqrt{L_r C_j} \tag{14.124}$$

Stage 3 (t_2−t_3): At t_3, S_1 is turned on with zero current and zero voltage. At the same moment, turn off S_a. It should be noted that the turn-on/turn-off point is not critical. S_1 and S_a could be turn on and off prior to t_2. If so, t_2 does not exist in the stage. Therefore,

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$$\Delta t_3 = t_{S_a-on} - \Delta t_1 - \Delta t_2 \tag{14.125}$$

Stage 4 (t_3–t_4): When S_a is turned off, I_L charges C_r and L_r through the conducted S_1. The voltage of C_r increases gradually, enabling S_a to be turned off with zero voltage. After i_{L_r} reaches I_L, capacitor C_r starts to discharge through L_r. At $t = t_4$, V_{C_r} reaches zero again:

$$\Delta t_4 = \frac{V_1 C_r}{I_L} \tag{14.126}$$

Stage 5 (t_4–t_5): During this period, the circuit current flows through the main switch S_1 and inductor L_r, L, like the conventional pulse-width-modulated (PWM) converter. The length is determined by the control of the PWM signal:

$$\Delta t_5 = \frac{\pi}{2}\sqrt{L_r C_r} \tag{14.127}$$

Stage 6 (t_5–t_6): At t_5, main switch S_1 is turned off. Inductor and capacitor C_r are in resonance. The voltage of C_r increases gradually at first, so that the voltage across the main switch S_1 rises gradually. S_1 is, therefore, turned off with zero voltage. At t_6, the voltage of C_r becomes zero; D_2 and D_b start to conduct. The time interval is given by

$$\Delta t_6 = kT - \Delta t_4 - \Delta t_5 \tag{14.128}$$

Stage 7 (t_6–t_7): During this period, the circuit current is freewheeling through D_2 and D_b, like the conventional PWM converter:

$$\Delta t_7 = \pi\sqrt{L_r C_r} \tag{14.129}$$

Stage 8 (t_7–t_0): At t_0, S_a is turned on once more, to start the next switch cycle. The length of this period is determined by the control of the PWM:

$$\Delta t_8 = (1-k)T - t_{S_a-on} - \Delta t_7 \tag{14.130}$$

14.4.2 Mode B (Quadrant II Operation)

Mode B performs quadrant II operation. The equivalent circuit for Mode B is shown in Figure 14.14. The operational process is analogous to Mode A operation. The corresponding waveforms are shown in Figure 14.15. The calculation formulae for Mode B are listed as follows:

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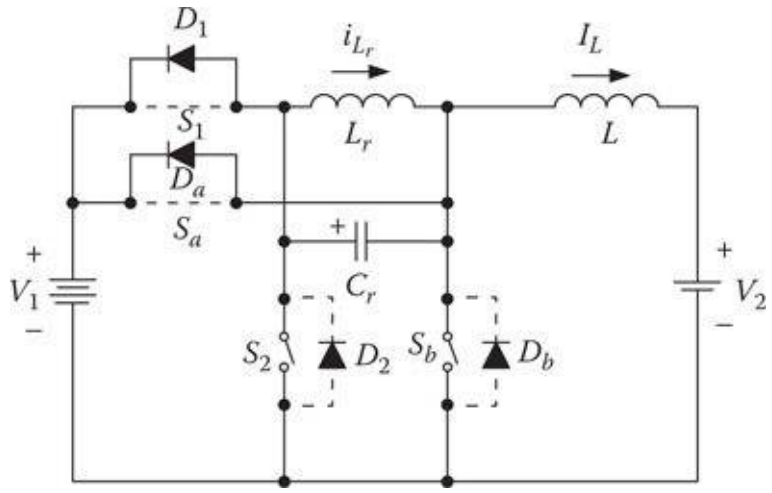


FIGURE 14.14
Mode B (quadrant II) operation.

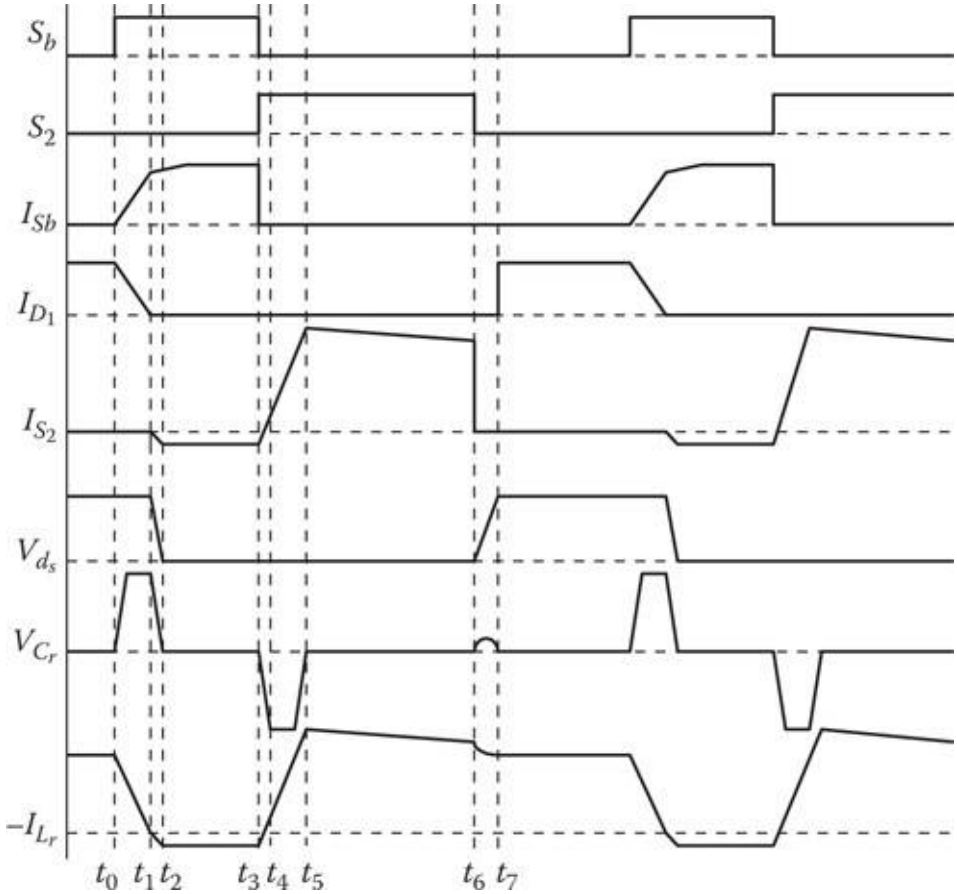


FIGURE 14.15
Waveforms of Mode B (quadrant II).

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$$\Delta t_1 = \frac{I_L L_r}{V_1} \qquad \Delta t_2 = \frac{\pi}{2}\sqrt{L_r C_j}$$

$$\Delta t_3 = t_{S_b\text{-}on} - \Delta t_1 - \Delta t_2 \qquad \Delta t_4 = \frac{V_1 C_r}{I_L}$$

$$\Delta t_5 = \frac{\pi}{2}\sqrt{L_r C_r} \qquad \Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi\sqrt{L_r C_r} \qquad \Delta t_8 = (1-k)T - t_{S_b\text{-}on} - \Delta t_7$$

14.4.3 Mode C (Quadrant III Operation)

Mode C performs quadrant III operation. The equivalent circuit for Mode C is shown in Figure 14.16. The operational process is analogous to Mode A operation. The corresponding waveforms are shown in Figure 14.17. The formulae for calculating Mode C are listed as follows:

$$\Delta t_1 = \frac{I_L L_r}{V_1 + V_2} \qquad \Delta t_2 = \frac{\pi}{2}\sqrt{L_r C_j}$$

$$\Delta t_3 = t_{S_a\text{-}on} - \Delta t_1 - \Delta t_2 \qquad \Delta t_4 = \frac{V_1 + V_2}{I_L} C_r$$

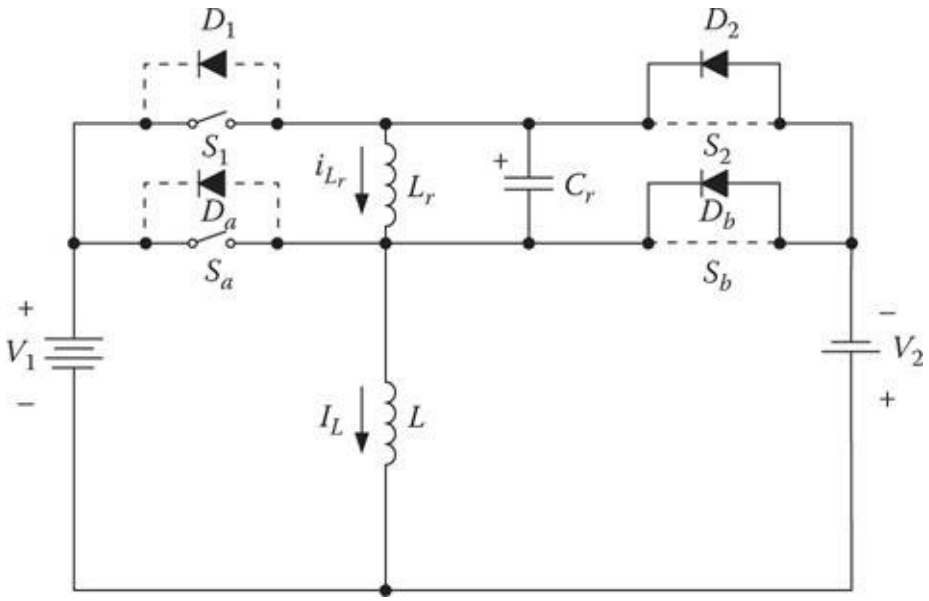


FIGURE 14.16
Mode C (quadrant II) operation.

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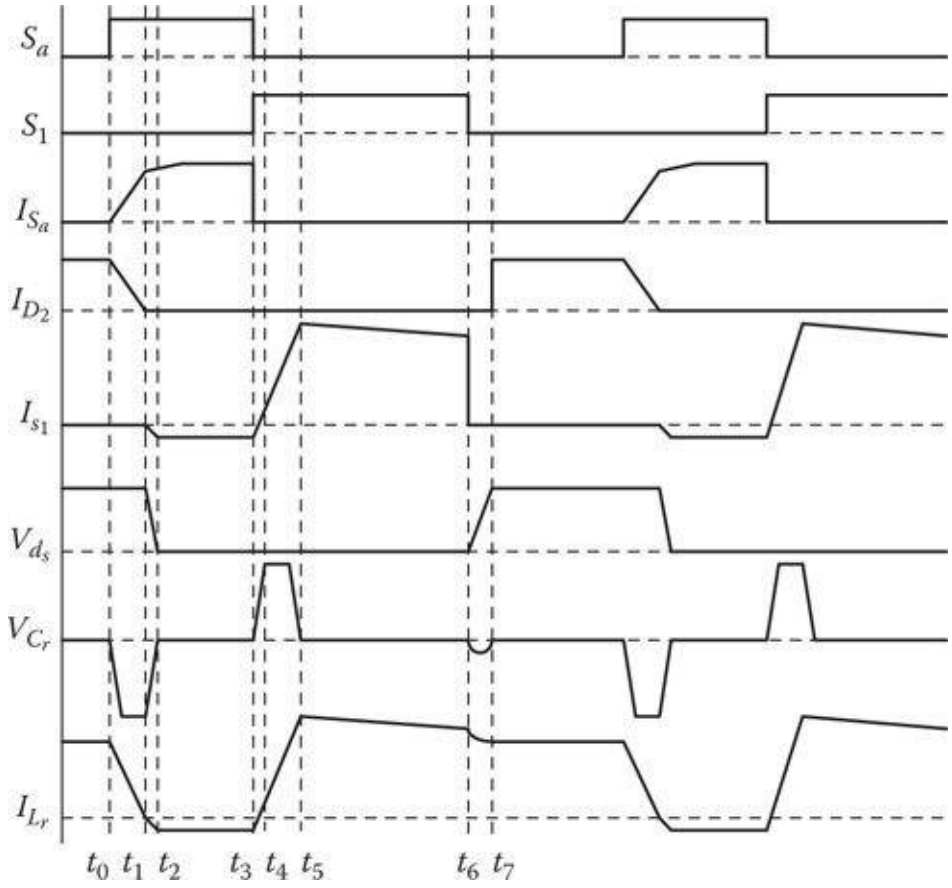


FIGURE 14.17
Waveforms of Mode C (quadrant III).

$$\Delta t_5 = \frac{\pi}{2}\sqrt{L_r C_r} \quad \Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi\sqrt{L_r C_r} \quad \Delta t_8 = (1-k)T - t_{S_a\text{-}on} - \Delta t_7$$

14.4.4 Mode D (Quadrant IV Operation)

Mode D performs in quadrant IV operation. The equivalent circuit for Mode D is shown in Figure 14.18. The operational process is analogous to operation Mode B. The corresponding waveforms are shown in Figure 14.19. The formulae for calculating Mode D are listed as follows:

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$$\Delta t_1 = \frac{I_L L_r}{V_1 + V_2} \qquad \Delta t_2 = \frac{\pi}{2}\sqrt{L_r C_j}$$

$$\Delta t_3 = t_{S_b-on} - \Delta t_1 - \Delta t_2 \qquad \Delta t_4 = \frac{V_1 + V_2}{I_L} C_r$$

$$\Delta t_5 = \frac{\pi}{2}\sqrt{L_r C_r} \qquad \Delta t_6 = kT - \Delta t_4 - \Delta t_5$$

$$\Delta t_7 = \pi\sqrt{L_r C_r} \qquad \Delta t_8 = (1-k)T - t_{S_b-on} - \Delta t_7$$

14.4.5 Simulation Results

PSpice is a popular simulation method to test and verify electronic circuit design. In order to implement this ZV-ZCS two-quadrant DC/DC converter with 3 kW delivery, the rig of a modern car battery ±28 VDC as a load and a 42 VDC as a source power supply was tested.

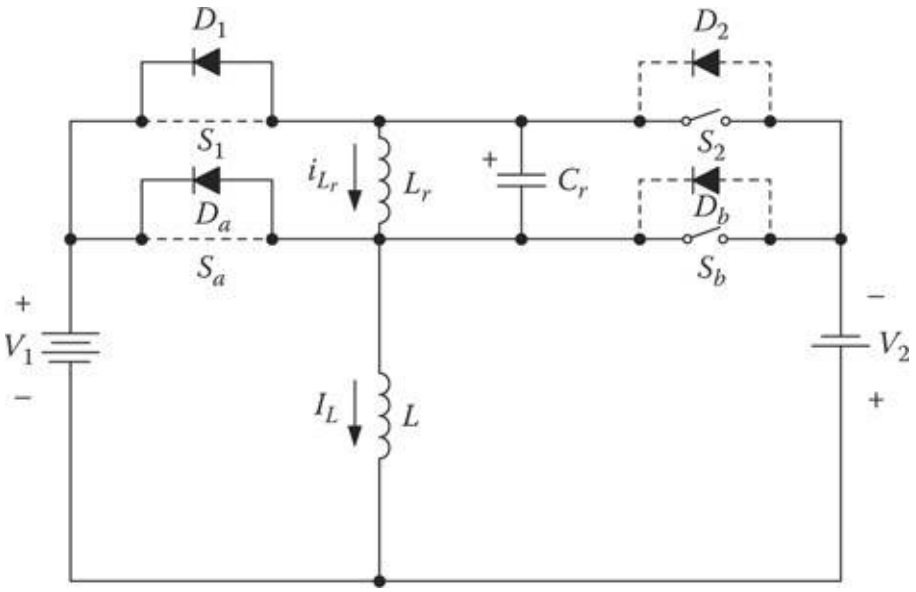


FIGURE 14.18
Mode D (quadrant II) operation.

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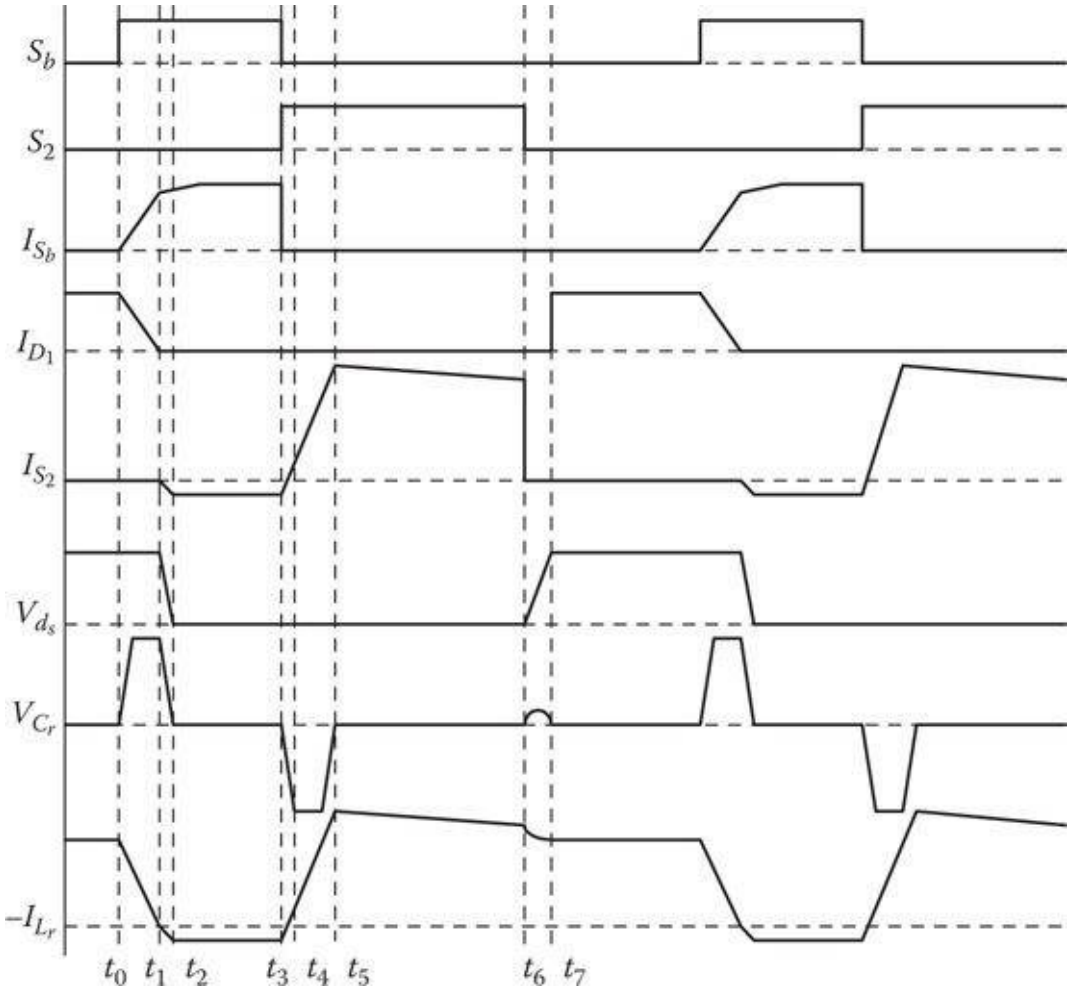


FIGURE 14.19
Waveforms of Mode D (quadrant IV).

The testing conditions are V_1 = 42 V and V_2 = 28 *V*, L_r = 2 μH, C_r = 0.8 nF, L = 550 μH, and f = 100 kHz. The simulation result for quadrant I is shown in Figure 14.20; the simulation result for quadrant II is shown in Figure 14.21. From these waveforms and data, we can see that the main switches in the converter are switched on at ZC and ZVS condition; they are switched off at ZVS condition. Moreover, all the auxiliary switches and diodes are operated under soft commutation.

The testing conditions are V_1 = 42 V and V_2 = −28 *V*, L_r = 2 μH, C_r = 0.8 nF, L = 550 μH, and f = 100 kHz. The simulation results for quadrant III are shown in Figure 14.22; the simulation results for quadrant IV are shown in Figure 14.23. From these waveforms, we can see that the main switches in the converter are switched on at ZC and ZVS condition; they are switched off at ZVS condition. Moreover, all the auxiliary switches and diodes are operated under soft commutation.

14.4.6 Experimental Results

A testing rig battery ±28 VDC as a load and a source of 42 VDC as the power supply was tested. The testing conditions are V_1 = 42 V and V_2 = ±28 V, L = 30 μH, L_{r1} = L_{r2} = 1 pH, C_r =

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4 pF, I_L = 25 A (for quadrant I and quadrant II)/35 A (for quadrant III and quadrant IV), and the volume is 40 (in.^{3}). The experimental results are shown in Table 14.7. The average power transfer efficiency is higher than 89.7% and the total average PD is 17.5 W/in.^{3}. This figure is much higher than the classical converters whose PD is usually less than 5 W/in.^{3}. Since the switching frequency and conduction duty k can be adjusted individually, we chose f = 100 kHz and a suitable conduction duty cycle k to obtain the proper operation state.

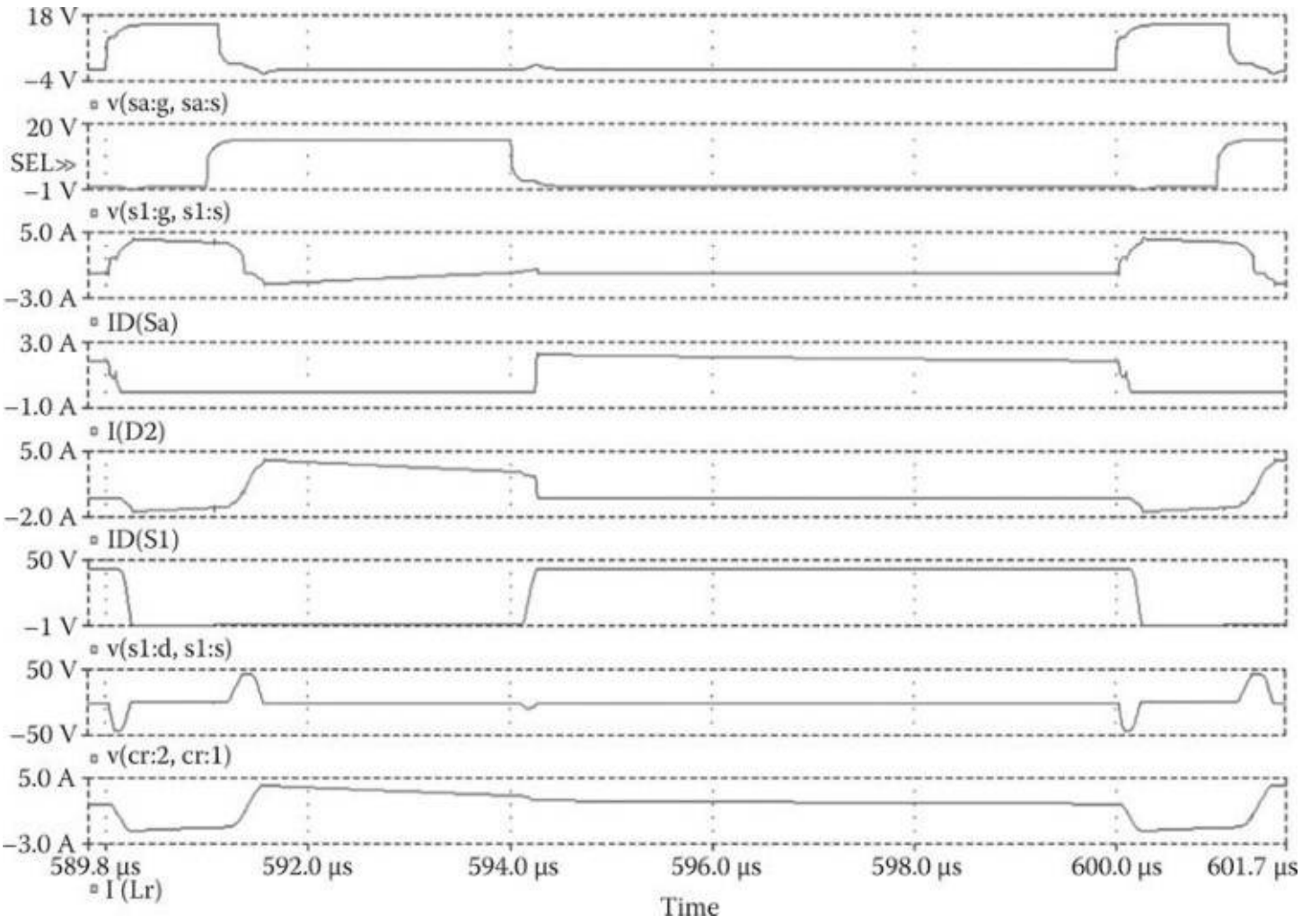


FIGURE 14.20
Simulation result for zero-voltage plus zero-current-switch operation Mode A (f = 100 kHz; k = 30%).

14.4.7 Design Considerations

In a practical design, for ease of implementation, the control of the two switches can adopt the constant time-delay method:

1. Turn-on of the main switch should delay turn-on of the auxiliary switch at least by ΔT_{ON} $_{\text{min}}$. The auxiliary switch could be turned off simultaneously with the turn-on of the main

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switch. But, it is better to turn off S_a shortly after the turn-on of the main switch to secure soft turn-off of the auxiliary switch.

2. For prompt soft turn-off of main switch (S_1 or S_2) and energy recovery, turn-off of the auxiliary switch should precede turn-off of the main switch by a minimum time of $\Delta T_{OFF\,\min}$. This means that for prompt soft switching, the earlier constraint should be met under the minimum duty cycle. The simple timing constraints are calculated as follows:

$$T_D \geq T_{ON\,\min} = \Delta t_1 + \Delta t_2 = \frac{I_L L_r}{V_1} + \frac{\pi}{2}\sqrt{L_r C_j} \tag{14.131}$$

$$T_P \geq \Delta T_{OFF\,\min} = \frac{C_r V_1}{i_P} + \frac{L_r}{V_1} i_P \tag{14.132}$$

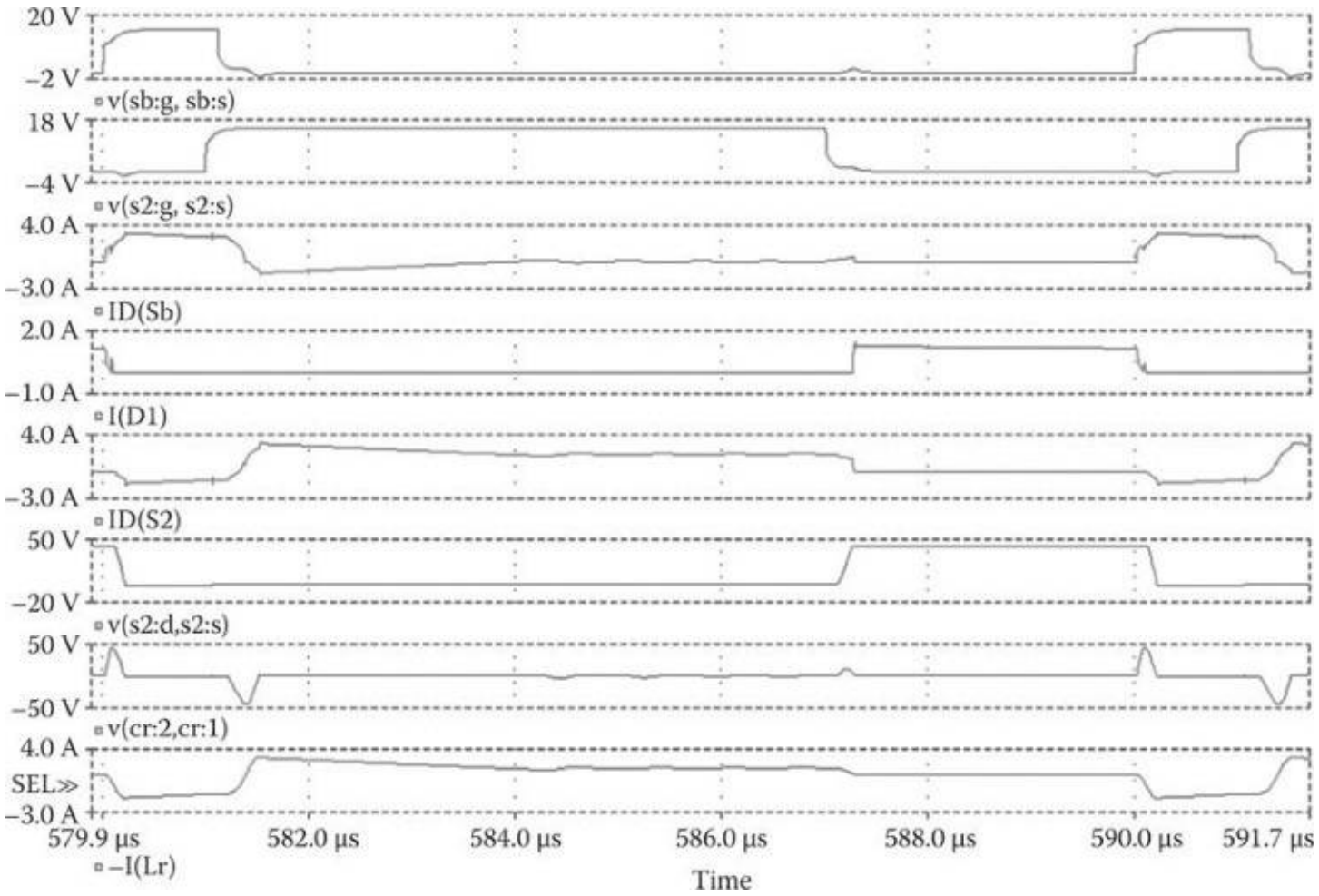


FIGURE 14.21
Simulation result for zero-voltage plus zero-current-switch operation Mode B (f = 100 kHz; k = 60%).

$$i_P = \sqrt{I_L^2 + \frac{V_1^2}{\rho}} \quad \rho = \sqrt{\frac{L_r}{C_j}} \tag{14.133}$$

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where

C_j is the junction capacitor across the main switch's drain and source

T_D is the time that turn-on of the main switch delays turn-on of the auxiliary switch

T_P is the time that turn-off of the auxiliary switch precedes turn-off of the main switch

i_P is the L_r peak current

For engineering implementation, as no capacitor is directly paralleled with the main switch, the time interval Δt_2 is very small; moreover, the turn-on loss caused by the junction capacitor is minimum if the main switch is turned on before V_{d_s} falls to zero. So, Δt_2 in Equation 14.131 can be ignored for simple design:

$$T_D \geq T_{ON\min} = \Delta t_1 = \frac{I_L L_r}{V_1} \tag{14.134}$$

To secure the soft switching under minimum duty cycle $k_{\min}$, Equation 14.132 can be expressed as

$$D_{\min} T_s \geq \Delta T_{OFF\min} = \frac{C_r V_1}{i_P} + \frac{L_r}{V_1} i_P \tag{14.135}$$

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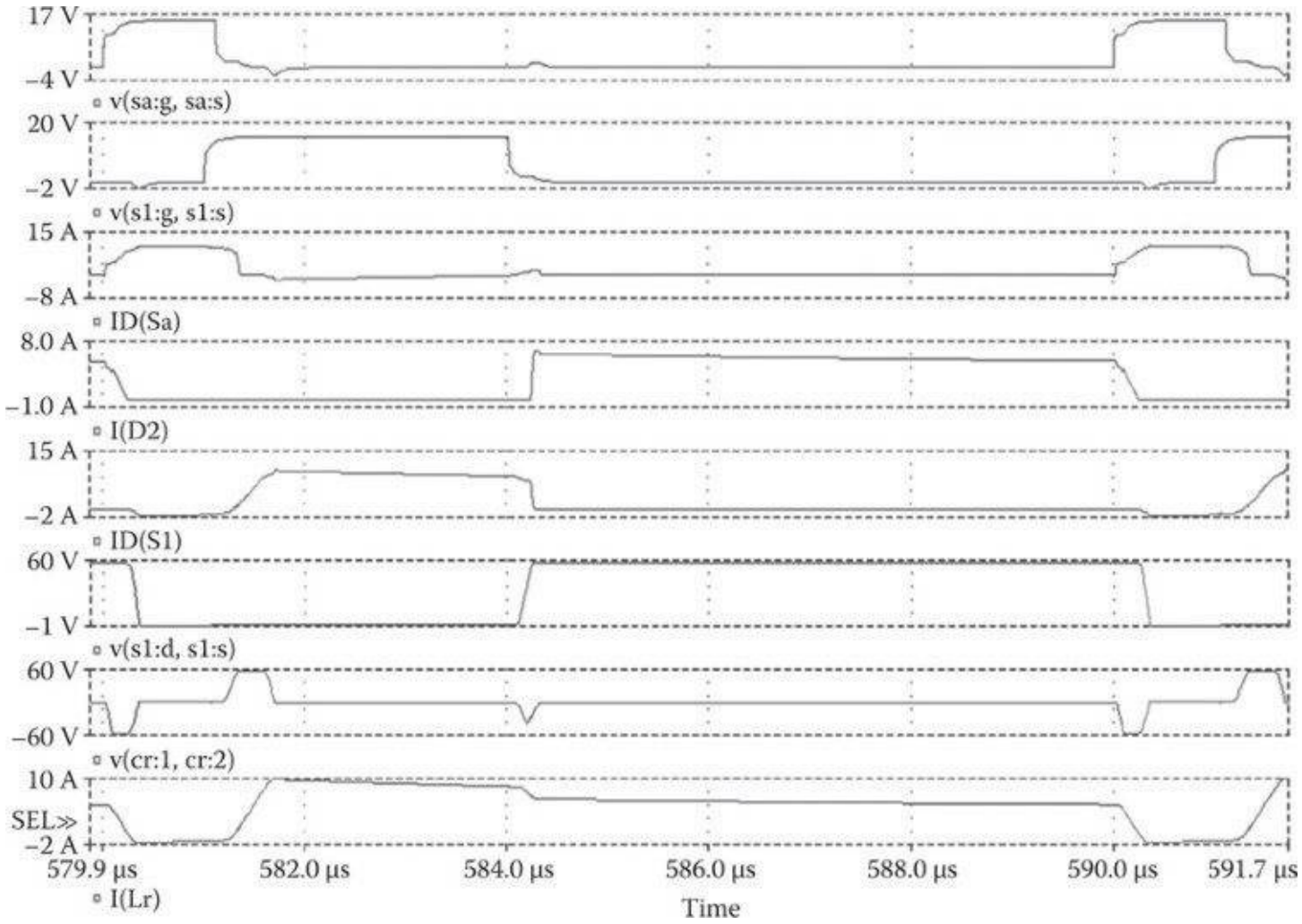


FIGURE 14.22
Simulation result for zero-voltage plus zero-current-switch operation Mode C (f = 100 kHz; k = 30%).

To achieve the similar conversion ratios of its hard-switch PWM counterpart, the commutation transition, that is, $\Delta T_{ON\ \min}$, is normally set as 10%–15% cycle in practical design:

$$T_{ON\min} = \frac{I_{L\max} L_r}{V_1} \le 10\% - 15\% T_s \tag{14.136}$$

From this, L_r can be obtained; for practical implementation, turn-on of the main switch delays turn-on of the auxiliary switch at a constant time T_D:

$$T_D = \frac{I_{L\max} L_r}{V_1} \tag{14.137}$$

To reduce the auxiliary switch's conduction loss, the auxiliary switch is turned off right after the turn-on of the main switch. From Equation 14.133, it is obvious that the peak current of L_r

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does not relate to C_r. Therefore, C_r can be set large enough to reduce the turn-off loss of the main switch most effectively. But C_r should meet the constraint of Equation 14.135 as well.

Compared with other soft-switching circuits, besides the soft switching of the auxiliary switch, the proposed circuit possesses the simplicity in topology. Another merit is that C_r is not directly paralleled with the main switch. It not only provides soft turn-off for all the switches but also does not discharge to L_r. A lower peak current in the auxiliary switch could, therefore, be expected, particularly in cases where a small snubber inductor is used in high-frequency operation. Moreover, as the charge of C_r does not increase L_r current, the design trade-off between C_r and current stress on the auxiliary switch does not exist, and the design of L_r and C_r become easy, as the earlier design analysis indicates. Also, with the help of inductor L_r, the reverse recovery current of the main diode is effectively minimized.

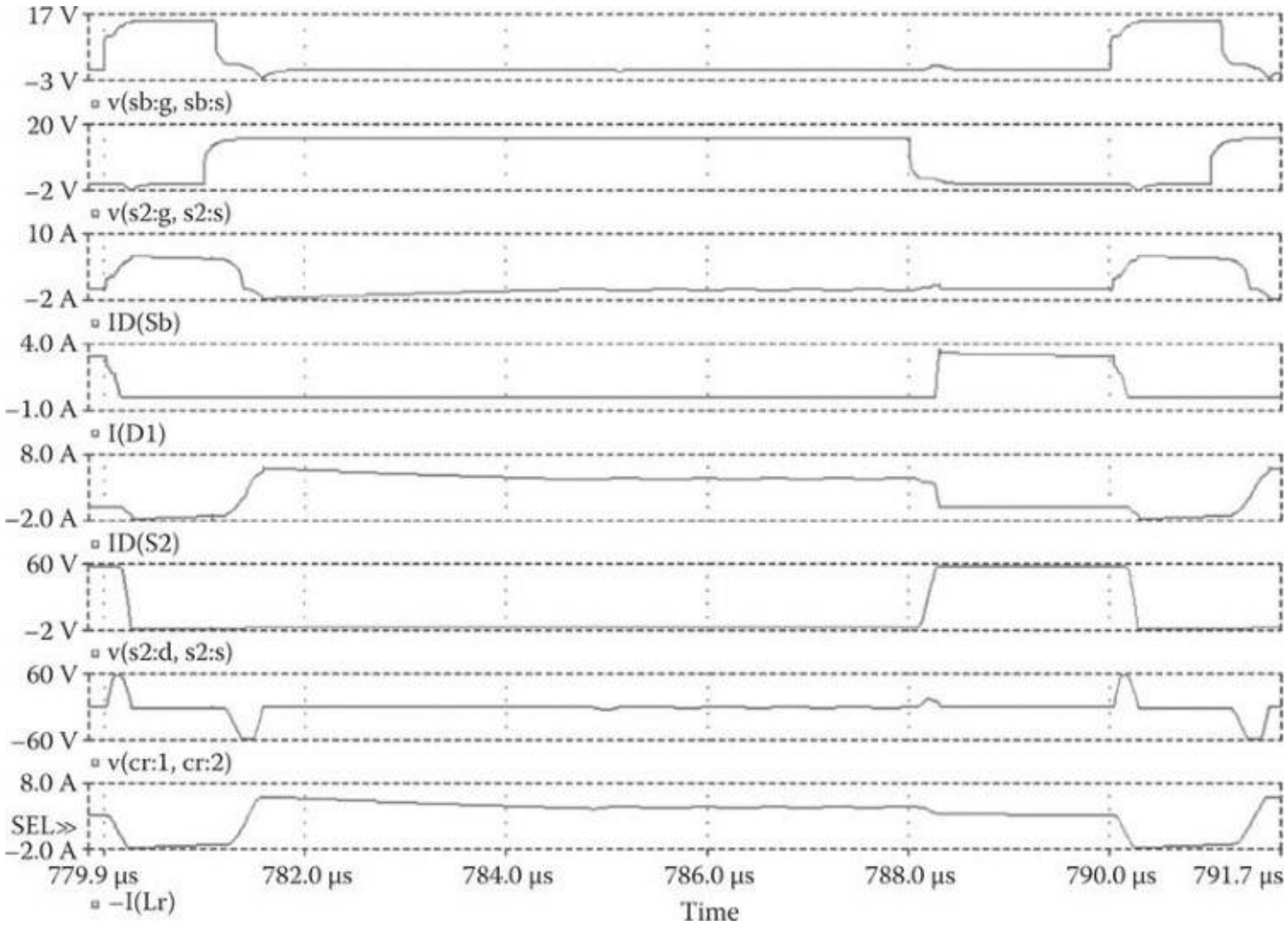


FIGURE 14.23
Simulation result for zero-voltage plus zero-current-switch operation Mode D (f = 100 kHz; k = 70%).

TABLE 14.7
Experimental Results for Different Frequencies

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Mode	f (kHz)	$L_{r1} = L_{r2} = L_{r2}$ (μH)	C_r (μF)	I_i (A)	I_o (A)	I_L (A)	P_i (W)	P_o (W)	η (%)	PD (W/in.^{3})
A	20.5	1	4	16.98	25	25	713	700	98.2	17.66
A	21	1	4	17.4	25	25	730.6	700	95.8	17.88
A	21.5	1	4	17.81	25	25	748	700	93.5	18.1
B	16.5	1	4	25	16.4	25	700	688.8	98.4	17.36
B	17	1	4	25	16.2	25	700	680.4	97.2	17.25
B	17.5	1	4	25	15.97	25	700	670.1	95.8	17.13
C	18.3	1	4	16.24	24.03	35	682.1	672.8	98.6	16.94
C	18.5	1	4	16.42	23.91	35	689.6	669.4	97.1	17
C	18.7	1	4	16.59	23.79	35	696.8	666.1	95.6	17.04
D	37.2	1	4	24.42	16.02	35	683.8	672.7	98.4	16.95
D	37.5	1	4	24.62	15.87	35	689.4	666.4	96.7	16.94
D	37.8	1	4	24.81	15.71	35	694.7	660	95	16.93

It should be also noted here that the turn-on point of the main switch is not critical. The main switch could be turned on prior to t_2 because the turn-on loss caused by the junction capacitor is very small.

The control principle adopted here is simple as it does not need the cross-zero voltage detection of the main switch. It is easy to implement, but it has its limitations in light-load or no-load operation. Since the duty cycle of the main switch may be smaller than the duty cycle of the auxiliary switch at no load or light load, the constant duty cycle of the auxiliary switch will charge up the output capacitor without control. In such a case, certain current or voltage cross-zero detection is required to adjust the duty cycle of the auxiliary switch. On the other hand, the conduction loss is increased as the auxiliary switch is not optimized with the minimum conduction at light load by using this control method.

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15

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Synchronous Rectifier DC/DC Converters

The global merchant dollar market for DC/DC converters is projected to increase from about $3.6 billion in 2001 to about $6.0 billion in 2006, a compound annual growth rate of 10.6%. North American sales of DC/DC converters in networking and telecom equipment are expected to grow from $2.3 billion in 1999 to $4.6 billion in 2004, a yearly compounded growth rate of 15.3%. The first quarter of 1995 was the first time that shipments of 3.3 V microprocessor and memory integrated chips (ICs) exceeded the shipments of 5 V parts. Once this transition occurred in memories and microprocessors, the demand for low-voltage power conversion began to grow at an increasing rate. The primary application of DC/DC converters is in computer power supplies and communication equipment.

The computer power supply shift from 5 to 3.3 V for digital ICs has taken over 5 years to occur, from the first indication that voltages below 5 V would be needed until the realization of volume sales. Now that the 5 V barrier has been broken, the trend toward lower and lower voltages is accelerating. Within 2 years, 2.5 V parts are expected to become common with the introduction of the next-generation microprocessors. In fact, current plans for the next-generation microprocessors call for a dual voltage of 1.5/2.5 V with 1.5 V used for the memory bus and 2.5 V used for logic functions. Within another few years, voltages are expected to move as low as 0.9 V, with mainstream, high-volume parts operating at 1.5 V.

A low-voltage plus high-current DC power supply is urgently required in the next-generation computer and communications equipment. The first idea is to use a forward converter (refer to Figure 1.26), which can perform low-voltage plus high-current output voltage. A modified circuit with dynamic clamp circuit is shown in Figure 15.1. Two diodes D_1 and D_2 can be normal rectifier diode, rectifier Schottky diode, or MOSFET. Figure 15.2 shows the efficiency gain of the following three types of forward converters needed in order to construct a low-voltage high-current power supply:

1. Forward converter using traditional diodes
2. Forward converter using Schottky diode
3. Synchronous rectifier (SR) using low-forward-resistance MOSFET

As the operating voltages ratchet downward, the design of rectifiers requires more attention because the devices' forward voltage drop constitutes an increasing fraction of the output voltage. The forward voltage drop across a switch-mode rectifier is in series with the output voltage, so losses in this rectifier will almost entirely determine its efficiency. The SR circuit has been designed primarily to reduce this loss.

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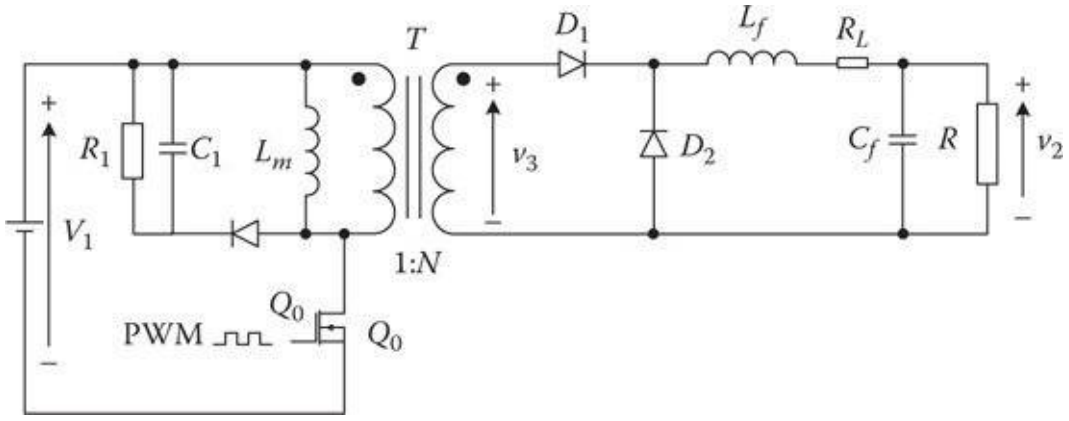


FIGURE 15.1
Forward converter with dynamic clamp circuit.

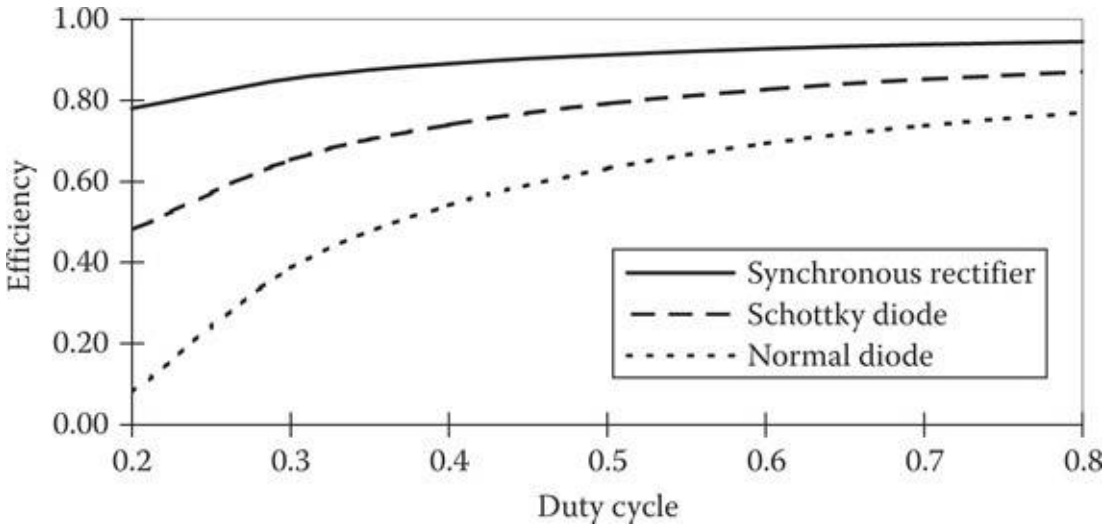


FIGURE 15.2
Efficiencies of different types of forward converter.

15.1. Introduction

A synchronous rectifier (SR) is an electronic switch that improves power conversion efficiency by placing a low-resistance conduction path across the diode rectifier in a switch-mode regulator. At 3.3 V, the traditional diode rectifier loss is significant with very low efficiency (say, less than 70%). For step-down regulators with a 3.3 V output and 12 V battery input voltage, a 0.4 V forward voltage of a *Schottky* diode represents a typical efficiency penalty of about 12%, aside from other loss mechanisms. The losses are not as bad at lower input voltages because the rectifier has a lower duty cycle and, thus, a shorter conduction time. However, the Schottky rectifiers' forward drop is usually the dominant loss mechanism.

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For an input voltage of 7.2 V and output of 3.3 V, an SR improves on the Schottky diode rectifier's efficiency by around 4%. Figure 15.1 also shows that as output voltage decreases, the SR provides even larger gains in efficiency.

A practical circuit arrangement of an SR DC/DC converter with purely resistive load is shown in Figure 15.3. It has one MOSFET switch S on the primary side of the transformer. Two MOSFETs S_1 and S_2 on the secondary side of the transformer function as the SR. T is the isolating transformer with a turn ratio of 1:N. An L–C circuit is the low-pass filter and R is the load. V_1 is the input voltage and V_2 is the output voltage. The main switch S is driven by a pulse-width-modulated (PWM) pulse-train signal. Repeating frequency f and turn-on duty cycle k of the PWM signal can be adjusted.

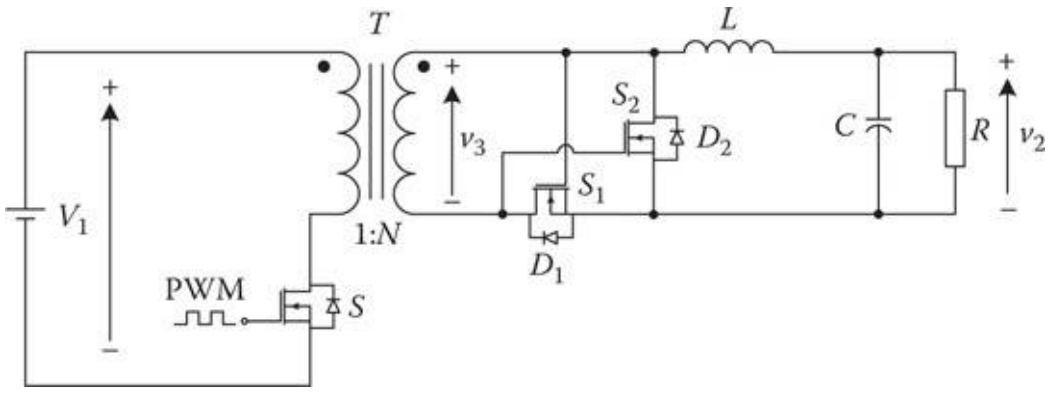


FIGURE 15.3
Synchronous rectifier converter with low-resistance MOSFET.

When the PWM signal is in the positive state, the main switch S conducts. The primary voltage of the transformer is V_1, and subsequently, the secondary voltage of the transformer is $v_3 = NV_1$. In the mean time, the MOSFET S_1 is forward biased, so it turns *on* and inversely conducts.

When the PWM signal is in the negative state, the main switch S is switched off. The voltage of the transformer, v_3, at this moment in time is approximately Nv_{C1} In the mean time, the MOSFET S_2 is forward biased, so it turns on and inversely conducts. It functions as freewheeling diode and lets the load current remain continuous through the filter L–C and load R.

A lot of papers in literature with practical hardware circuit achievements on SR have been presented about the recent IEEE transactions and IEEE proceedings. The paper "Evaluation of synchronous-rectification efficiency improvement limits in forward converters" supported by Virginia Power Electronics Center is one of the few outstanding research publications on SRs. This chapter provides a practical design of a 3.3 V/20 A forward synchronous rectifier (FSR) with an efficiency of 85.5%. Similarly, another paper published in 1991 also showed the principle of an RCD clamp forward converter with an efficiency of 87.3% at low output current. The paper by J. Sebastian is one more piece of excellent paper on FSR. He has built a prototype forward SR 3.3 V/20 A FSR with an efficiency of 87.5%. Another paper published in 1993 also showed the principle of an RCD clamp forward converter with an efficiency of

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87.3% at low output current (Cobos et al., 1993). Two Japanese researchers from Kumamoto Institute of Technology designed an FSR with an additional winding and switching element that is able to hold the gate charge for the freewheeling MOSFET (Sakai and Harada, 1995). Their experimental results for a 5 V/10 A SR gives a maximum efficiency of approximately 91% at a load of 7 A and an efficiency of 89% at 10 A. Another comparable FSR project was made by James Blanc from Siliconix Incorporated (Blanc, 1991). In his paper, he has included a lot of practical and useful simulation and experimental waveform data from his 3.3 V/10 A FSR. As the output voltage decreased, the operating efficiency decreased. Until now, no recent paper has been published on any practical hardware FSR that is able to provide 1.8 V/20 A output current at high efficiency.

The analysis and design of DC/DC converters have been the subject of many papers in the past. From the moment averaging techniques were used to model these converters, interest has been focused on finding the best approach to analyze and predict the behavior of the averaged small-signal or large-signal models. The main difficulty encountered is that the converter models are multiple-input multiple-output nonlinear systems, and thus, using the well-known transfer function control design approach is not straightforward. The most common approach has been that of considering the linearized small-signal model of these converters as a multiloop system, with an outer voltage loop and an inner current loop. Since the current loop has a much faster response than that of the outer loop, the analysis is greatly simplified and the transfer functions obtained allow the designer to predict the closed-loop behavior of the system. Another approach in analysis and design has been that of state-space techniques where the linearized state-space equations are used together with design technique such as pole placement or optimal control.

SR DC/DC converters are called the fifth-generation converters. The developments in microelectronics and computer science require the power supplies with low output voltage and strong current. Traditional diode bridge rectifiers are not available for this requirement. Soft-switching technique can be applied in SR DC/DC converters. We have created converters with very low voltage (5, 3.3, and 1.8 ~ 1.5 V) and strong current (30 A, 60 up to 200 A) and high power transfer efficiency (86%, 90% up to 93%). In this section, new circuits that are different from the ordinary SR DC/DC converters are introduced:

- Flat transformer SR Luo-converter
- Active-clamped flat transformer SR Luo-converter
- Double-current SR Luo-converter with active clamp circuit
- Zero-current-switching (ZCS) SR Luo-converter
- Zero-voltage-switching (ZVS) SR Luo-converter

15.2. Flat Transformer Synchronous Rectifier Luo-Converter

The flat transformer is a new design for AC/AC energy conversion. Since its structure is very compatible and well shielded, its size is very small and likely a flan cardboard. Applying

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frequency can be 100 kHz to 5 MHz; its power density (PD) can be as high as 300 W/in.^{3}. Therefore, it is a good component to use to construct the SR DC/DC converter.

The flat transformer *SR DC/DC Luo*-converter is shown in Figure 15.4. The switches S_2 and S_3 are the low-resistance MOSFET devices with very-low-resistance R_S (6–8 mΩ).

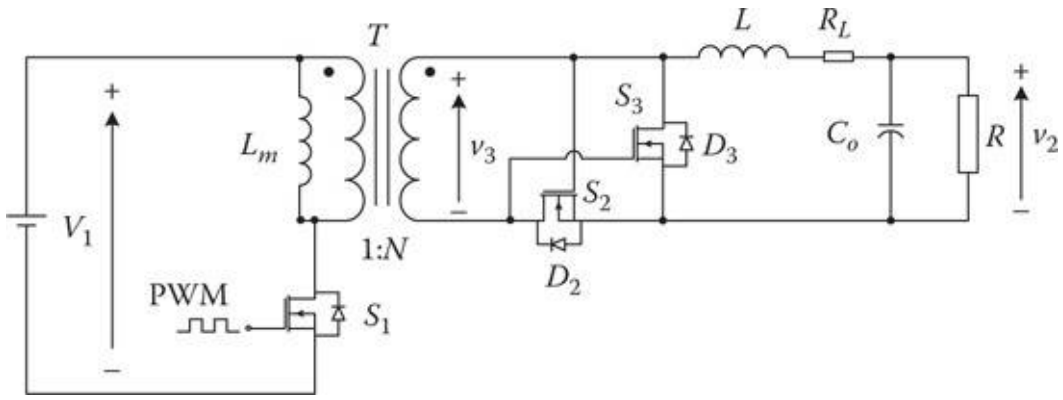


FIGURE 15.4
Flat transformer synchronous rectifier Luo-converter.

Since we use a flat transformer, its leakage inductance L_m = 1 nH and resistance R_L is small. Other parameters are C = 1 μF, L_m = 1 nH, R_L = 2 mΩ, L = 5 μH, and C_o = 10 μF. The input voltage is V_1 = 30 VDC and the output voltage is V_2; the output current is I_o. The transformer turns ratio is N that is usually much smaller than unity in SR DC/DC converters, for example, N = 1:12 or 1/12. The repeating period is $T = 1/f$ and conduction duty is k. There are four working modes:

1. Transformer is in magnetizing process.
2. Forward on.
3. Transformer is in demagnetizing process.
4. Switched off.

15.2.1 Transformer Is in Magnetizing Process

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \tag{15.1}$$

where

L_m is the leakage inductance of the primary winding

C_j is the drain-source junction capacitance of the main switch MOSFET S

If C_j is very small in nF, its charging process is very quickly completed. The primary current increases with slope V_1/L_m, and then the time interval of this period can be estimated

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as

$$t_1 = \frac{L_m}{V_1} NI_o \tag{15.2}$$

This is the process used to establish the primary current from 0 to rated value NI_o.

15.2.2 Switching-On

The switching-on period is controlled by the PWM signal; therefore,

$$t_2 \approx kT \tag{15.3}$$

15.2.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated as

$$t_3 = \sqrt{L_m C_j}\left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + (L_m/C_j)(NI_o)^2}}\right] \tag{15.4}$$

When the main switch is switching-off, there is a voltage stress, which can be very high. The voltage stress is dependent on the energy stored in the inductor and the capacitor:

$$V_{peak} = \sqrt{\frac{L_m}{C_j}} NI_o \tag{15.5}$$

The voltage stress peak value can be tens to hundreds of volts since C_j is small.

15.2.4 Switching-Off

The switching-off period is controlled by the PWM signal; therefore,

$$t_4 \approx (1-k)T \tag{15.6}$$

15.2.5 Summary

The average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - \left(R_L + R_S + \frac{L_m}{T} N^2\right) I_o \tag{15.7}$$

and

$$I_1 = kNI_o \tag{15.8}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_o}{V_1 I_1} = 1 - \frac{R_L + R_S + (L_m/T)N^2}{kNV_1} I_o \tag{15.9}$$

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When we set the frequency f = 150–200 kHz, we obtained the following: V_2 = 1.8 V, N = 1/12, I_o = 0–30 A, and volume = 2.5 (in.^{3}). The average power transfer efficiency is 92.3% and the maximum PD is 21.6 W/in.^{3}.

15.3 Active-Clamped Synchronous Rectifier Luo-Converter

Active-clamped flat transformer SR Luo-converter is shown in Figure 15.5. The clamped circuit effectively suppresses the voltage stress during the main switch turn-off.

Comparing the circuit in Figure 15.5 with the circuit in Figure 15.4, one more switch S_2 is set in the primary side. It switched on and off exclusively to the main switch S_1. When S_1 is turning-off, S_2 is switching-on. A large clamp capacitor C is connected in the primary winding to absorb the energy stored in the leakage inductor L_m. Since the clamp capacitor C is much larger than the drain-source capacitor C_j by usually hundreds of times, the stress voltage peak value remains at only a few volts. There are four working modes:

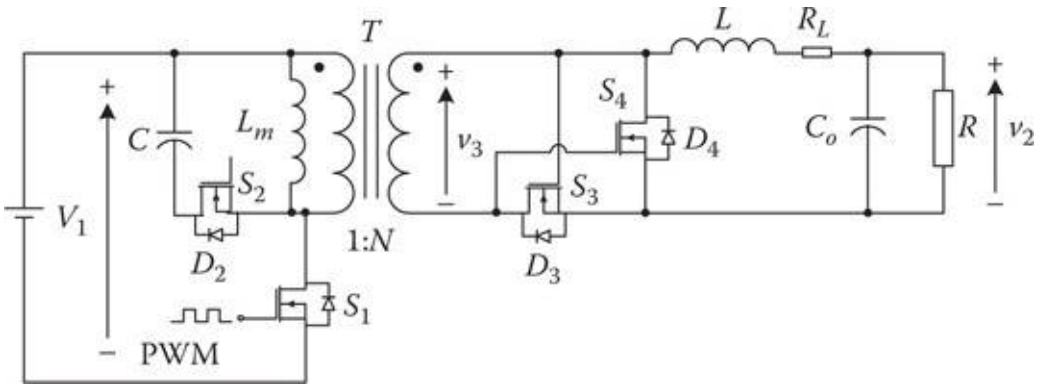


FIGURE 15.5
Active-clamped flat transformer synchronous rectifier Luo-converter.

1. Transformer is in magnetizing process.
2. Forward on.
3. Transformer is in demagnetizing process.
4. Switched off.

15.3.1 Transformer Is in Magnetizing Process

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \tag{15.10}$$

where

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L_m is the leakage inductance of the primary winding
C_j is the drain-source junction capacitance of the main switch MOSFET S

If C_j is very small in nF, its charging process is very quickly completed. The primary current increases with slope V_1/L_m, and then the time interval of this period can be estimated as

$$t_1 = \frac{L_m}{V_1} NI_o \tag{15.11}$$

This is the process to establish the primary current from 0 to rated value NI_0.

15.3.2 Switching-On

The switching-on period is controlled by the PWM signal; therefore,

$$t_2 \approx kT \tag{15.12}$$

15.3.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated as

$$t_3 = \sqrt{L_m C}\left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + (L_m/C)(NI_o)^2}}\right] \tag{15.13}$$

where C is the active clamp capacitor in μF. The voltage stress depends on the energy stored in the inductor and the capacitor:

$$V_{peak} = \sqrt{\frac{L_m}{C}} NI_o \tag{15.14}$$

The voltage stress peak value is very small since capacitor C is large, measured in μF.

15.3.4 Switching-Off

The switching-off period is controlled by the PWM signal; therefore,

$$t_4 \approx (1-k)T \tag{15.15}$$

15.3.5 Summary

The average output voltage V_2 is

$$V_2 = kNV_1 - \left(R_L + R_S + \frac{L_m}{T} N^2\right) I_o \tag{15.16}$$

and input current I_1 is

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$$I_1 = kNI_o \tag{15.17}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_o}{V_1 I_1} = 1 - \frac{R_L + R_S + (L_m/T)N^2}{kNV_1} I_o \tag{15.18}$$

When we set the frequency f = 150–200 kHz, we obtained the following: V_2 = 1.8 V, N = 1/12, I_o = 0–30 A, and volume = 2.5 (in.^{3}). The average power transfer efficiency is 92.3% and the maximum PD is 21.6 W/in.^{3}.

15.4. Double-Current Synchronous Rectifier Luo-Converter

The converter in Figure 15.5 likes a half-wave rectifier. The *double-current SR Luo*-converter with active clamp circuit is shown in Figure 15.6. The switches S_1–S_4 are the low-resistance MOSFET devices with very-low-resistance R_S (6–8 mΩ). Since S_3 and S_4 plus L_1 and L_2 form a double-current circuit and S_2 plus C is the active clamp circuit, this converter likes a full-wave rectifier and obtains a strong output current. Other parameters are C = 1 μF, L_m = 1 nH, R_l = 2 mΩ L = 5 μH, and C_0 = 10 μF. The input voltage is V_1 = 30 VDC and output voltage is V_2; the output current is I_0. The transformer turns ratio is N = 1:12. The repeating period is T = 1/f and conduction duty is k. There are four working modes:

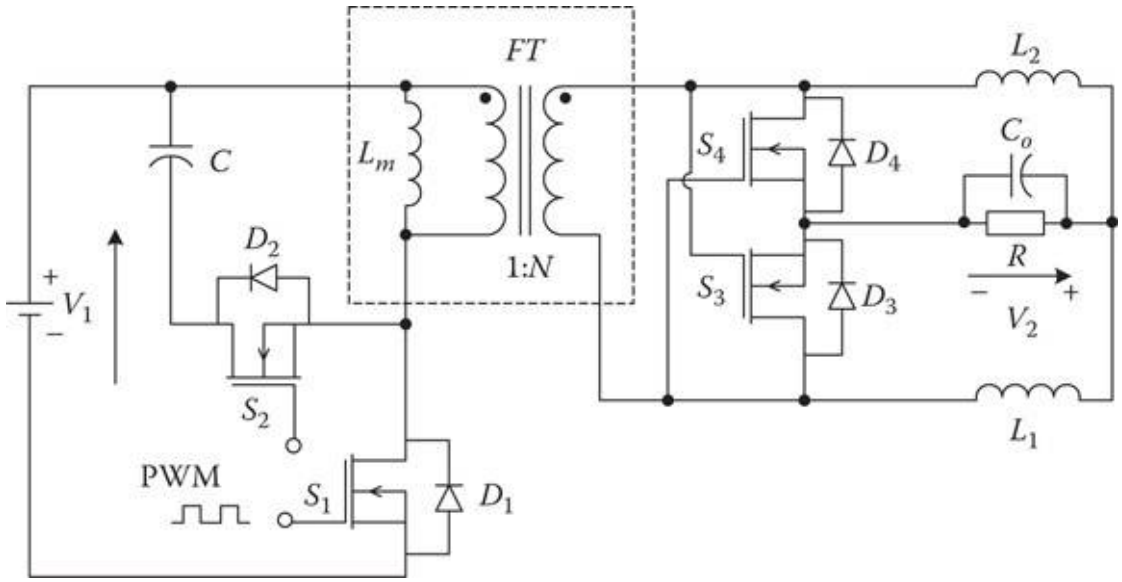


FIGURE 15.6
Double-current synchronous rectifier Luo-converter.

1. Transformer is in magnetizing process.
2. Forward on.

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3. Transformer is in demagnetizing process.
4. Switched off.

15.4.1 Transformer Is in Magnetizing Process

The natural resonant frequency is

$$\omega = \frac{1}{\sqrt{L_m C_j}} \tag{15.19}$$

where

L_m is the leakage inductance of the primary winding

C_j is the drain-source junction capacitance of the main switch MOSFET S

If C_j is very small in nF, its charging process is very quickly completed. The primary current increases with slope V_1/L_m, and the time interval of this period can be estimated as

$$t_1 = \frac{L_m}{V_1} NI_o \tag{15.20}$$

This is the process used to establish the primary current from 0 to rated value NI_o.

15.4.2 Switching-On

The switching-on period is controlled by the PWM signal; therefore,

$$t_2 \approx kT \tag{15.21}$$

15.4.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated as

$$t_3 = \sqrt{L_m C}\left[\frac{\pi}{2} + \frac{V_1}{\sqrt{V_1^2 + (L_m/C)(NI_o)^2}}\right] \tag{15.22}$$

When the main switch is switching-off, there is a very low voltage stress since the active clamp circuit is applied.

15.4.4 Switching-Off

Switching-off period is controlled by the PWM signal; therefore,

$$t_4 \approx (1-k)T \tag{15.23}$$

15.4.5 Summary

The average output voltage V_2 and input current I_1 are

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$$V_2 = kNV_1 - \left(R_L + R_S + \frac{L_m}{T}N^2\right)I_o \tag{15.24}$$

and

$$I_1 = kNI_o \tag{15.25}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_o}{V_1 I_1} = 1 - \frac{R_L + R_S + (L_m/T)N^2}{kNV_1} I_o \tag{15.26}$$

When we set the frequency f = 200–250 kHz, we obtained the following: V_2 = 1.8 V, N = 12, I_o = 0–35 A, and volume = 2.5 (in.^{3}). The average power transfer efficiency is 94% and the maximum PD is 25 W/in.^{3}.

15.5. Zero-Current-Switching Synchronous Rectifier Luo-Converter

The ZCS SR Luo-converter is shown in Figure 15.7. Since the power loss across the main switch S_1 is high in the *double-current SR Luo*-converter, we designed the *ZCS DC SR Luo-converter* shown in Figure 15.7. This converter is based on the *DC SR* Luo-converter plus ZCS technique. It employs a double-core flat transformer. There are four working modes:

1. Transformer is in magnetizing process.
2. Resonant period.
3. Transformer is in demagnetizing process.
4. Switched off.

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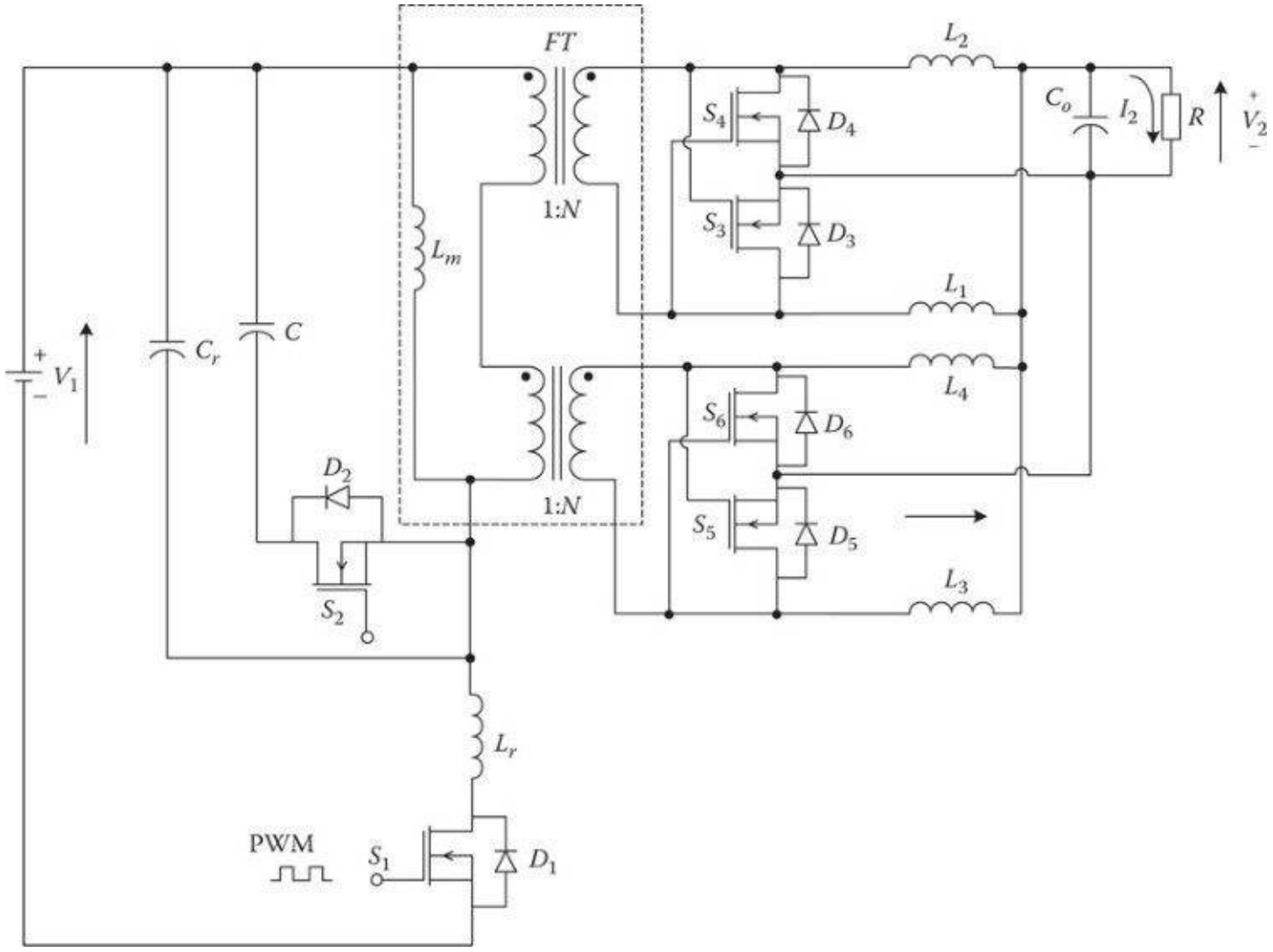


FIGURE 15.7
Zero-current-switching synchronous rectifier Luo-converter.

15.5.1 Transformer Is in Magnetizing Process

The ZCS resonant frequency is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{15.27}$$

The normalized impedance is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{15.28}$$

The shift-angular distance is

$$\alpha = \sin^{-1}\left(\frac{I_1 Z_r}{V_1}\right) \tag{15.29}$$

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where

L_r is the resonant inductor

C_r is the resonant capacitor

The primary current increases with slope V_1/L_r, and then the time interval of this period can be estimated as

$$t_1 = \frac{I_1 L_r}{V_1} \tag{15.30}$$

15.5.2 Resonant Period

The resonant period is

$$t_2 = \frac{1}{\omega_r}(\pi + \alpha) \tag{15.31}$$

15.5.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated as

$$t_3 = \frac{V_1(1+\cos\alpha)C_r}{I_1} \tag{15.32}$$

When the main switch is switching-off, there is a very low-voltage stress since active clamp circuit applied.

15.5.4 Switching-Off

Switching-off period is controlled by the PWM signal; therefore,

$$t_4 = \frac{V_1(t_1+t_2)}{V_2 I_1}\left(I_L + \frac{V_1}{Z_r}\frac{\cos\alpha}{\pi/2+\alpha}\right) - (t_1+t_2+t_3) \tag{15.33}$$

15.5.5 Summary

The average output voltage V_2 and input current I_1 are

$$V_2 = kNV_1 - \left(R_L + R_S + \frac{L_r + L_m}{T}N^2\right)I_o \tag{15.34}$$

and

$$I_1 = kNI_o \tag{15.35}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_o}{V_1 I_1} = 1 - \frac{R_L + R_S + [(L_r + L_m)/T]N^2}{kNV_1} I_o \tag{15.36}$$

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L_r is larger than L_m; therefore, L_m can be ignored in this formulae.

When we set the V_1 = 60 V and frequency f = 200–250 kHz, we obtained the following: V_2 = 1.8 V, N = 1/12, I_o = 0–60 A, and volume = 4 (in.^{3}). The average power transfer efficiency is 94.5% and the maximum PD is 27 W/in.^{3}

15.6 Zero-Voltage-Switching Synchronous Rectifier Luo-Converter

ZVS SR Luo-converter is shown in Figure 15.8, which is derived from the *DC SR Luo*-converter plus ZVS technique. It employs a double-core flat transformer. There are four working modes:

1. Transformer is in magnetizing process.
2. Resonant period.
3. Transformer is in demagnetizing process.
4. Switched off.

15.6.1 Transformer Is in Magnetizing Process

The ZVS resonant frequency is

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{15.37}$$

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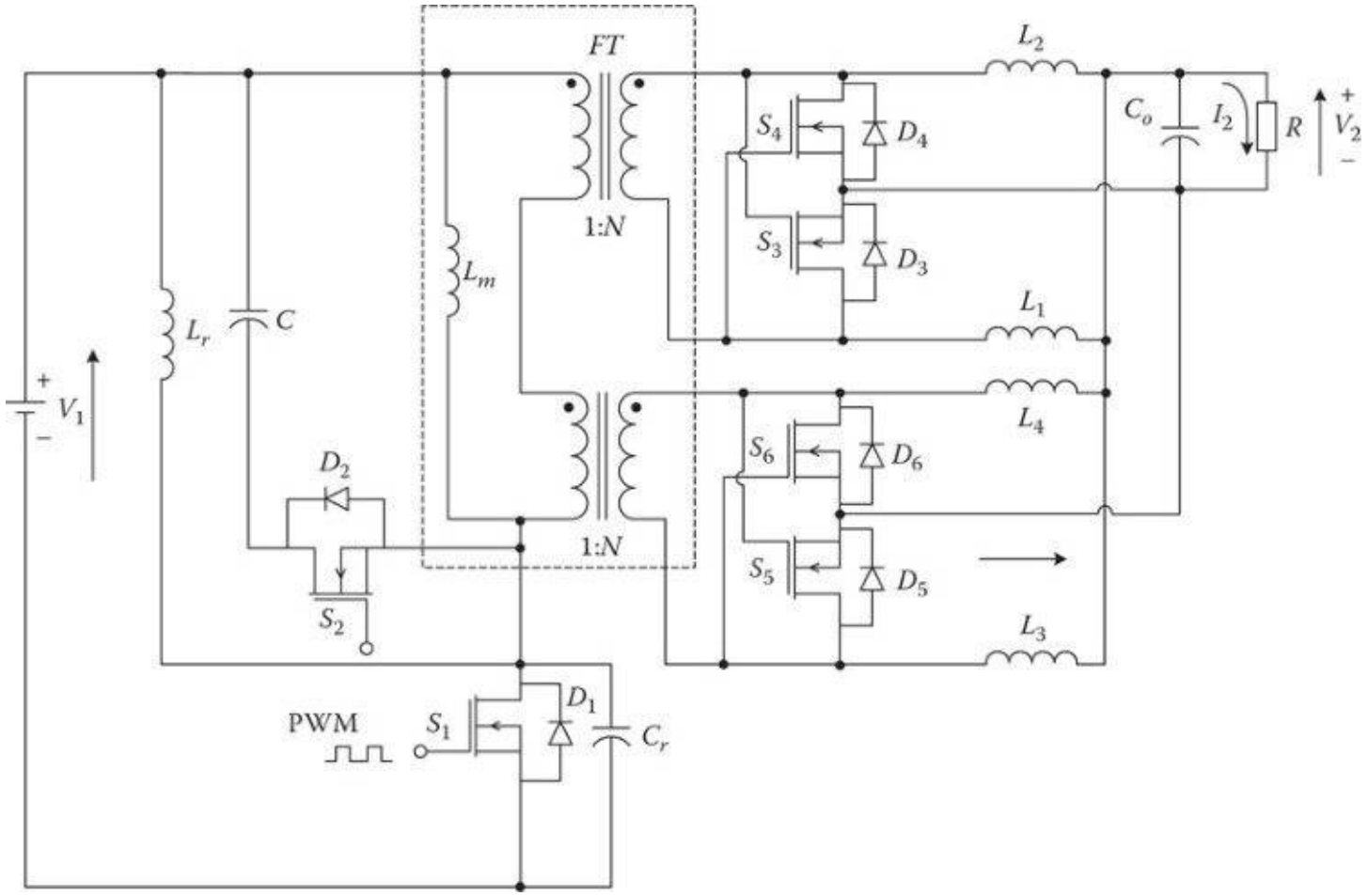


FIGURE 15.8
Zero-voltage-switching synchronous rectifier Luo-converter.

The normalized impedance is

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{15.38}$$

The shift-angular distance is

$$\alpha = \sin^{-1}\left(\frac{V_1}{Z_r I_1}\right) \tag{15.39}$$

where

L_r is the resonant inductor

C_r is the resonant capacitor

The switch voltage increases with slope I_1/C_r, and then the time interval of this period can be estimated as

$$t_1 = \frac{V_1 C_r}{I_1} \tag{15.40}$$

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15.6.2 Resonant Period

The resonant period is

$$t_2 = \frac{1}{\omega_r}(\pi + \alpha) \tag{15.41}$$

15.6.3 Transformer Is in Demagnetizing Process

The transformer demagnetizing process is estimated as

$$t_3 = \frac{I_1(1+\cos\alpha)L_r}{V_1} \tag{15.42}$$

When the main switch is switching-off, there is a very low voltage stress since active clamp circuit is applied.

15.6.4 Switching-Off

Switching-off period is controlled by the PWM signal; therefore,

$$t_4 = \frac{t_1 + t_2 + t_3}{(V_1/V_2) - 1} \tag{15.43}$$

15.6.5 Summary

The average output voltage V_2 and input current is I_1:

$$V_2 = kNV_1 - \left(R_L + R_S + \frac{L_r//L_m}{T}N^2\right)I_o \tag{15.44}$$

and

$$I_1 = kNI_o \tag{15.45}$$

The power transfer efficiency is

$$\eta = \frac{V_2 I_o}{V_1 I_1} = 1 - \frac{R_L + R_S + (L_r//L_m/T)N^2}{kNV_1} I_o \tag{15.46}$$

L_r is larger than L_m; therefore, L_r can be ignored in this formulae.

When we set the V_1 = 60 V and frequency f = 200–250 kHz, we obtained the following: V_2 = 1.8 V, N = 12, I_o = 0–60 A, and volume = 4 (in.^{3}). The average power transfer efficiency is 94.5% and the maximum PD is 27 W/in.^{3}

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16

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Multiple Energy-Storage Element Resonant Power Converters

16.1 Introduction

Multiple energy-storage element resonant power converters (x-element RPCs) are the sixth-generation converters. As the transfer power becomes higher and higher, traditional methods are unable to deliver large amounts of power from the source to the final actuators with high efficiency. In order to reduce the power losses during the conversion process, the sixth-generation converters, x-element RPCs, were created. They can be classified into two main groups:

1. DC/DC resonant converters
2. DC/AC resonant inverters

Both groups consist of multiple energy-storage elements: two elements, three elements, or four elements. These energy-storage elements are passive parts: inductors and capacitors. They can be connected in series or parallel in various methods. The circuits of the multiple energy-storage element converters are as follows

- Eight topologies of two-element RPC shown in Figure 16.1
- Thirty-eight topologies of three-element RPC shown in Figure 16.2
- Ninety-eight topologies of four-element (2L-2C) RPC shown in Figure 16.3

If there is no restriction such as $2L-2C$ for four-element RPC, the number of the topologies of four-element RPC can be very much larger. How to investigate the large quantity of converters is a task of vital importance. This problem was outstanding in the last decade of the last century. Unfortunately, it was not paid very much attention. This generation of converters was not well discussed; only a limited number of papers were published in the literature.

16.1.1 Two-Element RPC

There are eight topologies of two-element RPC that are shown in Figure 16.1. These topologies have simple circuit structure and minimal components. Consequently, they can transfer the power from source to end users with higher power efficiency and lower power losses. A particular circuitry analysis will be carried out in the next section.

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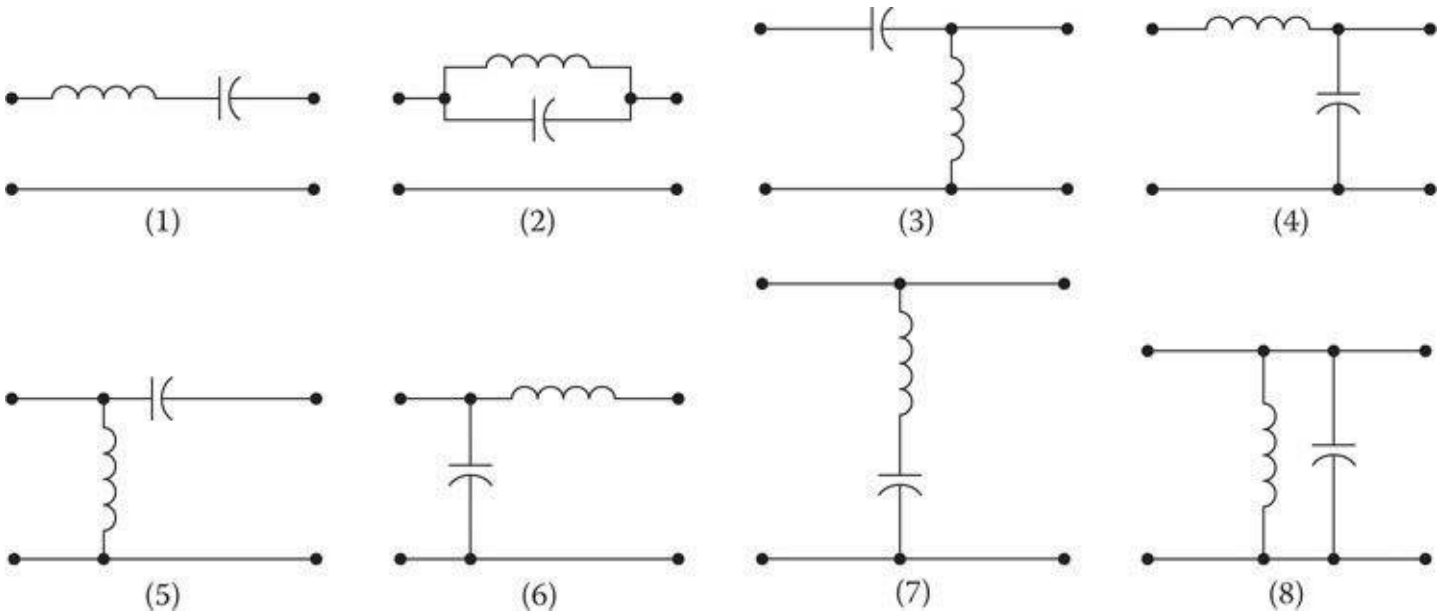


FIGURE 16.1
The eight topologies of two-element resonant power converter.

Usually, the two-element RPC has a very narrow response frequency band, which is defined as the frequency width between the two half-power points. The working point must be selected in the vicinity of the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$.

Another drawback is that the transferred waveform is usually not sinusoidal, that is, the output waveform total harmonic distortion (THD) is not zero.

Since total power losses are mainly contributed by the power losses across the main switches using resonant conversion technique, the two-element RPC has a high power transferring efficiency.

16.1.2 Three-Element RPC

There are 38 topologies of three-element RPC that are shown in Figure 16.2. These topologies have one more component in comparison to the two-element RPC topologies. Consequently, they can transfer the power from source to end users with higher power and high power transfer efficiency. A particular circuitry analysis will be carried out in Chapter 17.

Usually, the three-element RPC has a much wider response frequency band, which is defined as the frequency width between the two half-power points. If the circuit is a low-pass filter, the frequency bands can cover the frequency range from 0 to the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. The working point can be selected in the much wider frequency width that is lower than the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. Another advantage over the two-element RPC topologies is that the transferred waveform can usually be sinusoidal, that is, the output waveform THD is nearly zero. A well-known monofrequency waveform transferring operation has very low electromagnetic interference (EMI).

16.1.3 Four-Element RPC

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There are 98 topologies of four-element RPC (2*L*−2*C*) that are shown in Figure 16.3. Although these topologies have comparable complex circuit structures, they can still transfer the power from source to end users with higher power efficiency and lower power losses. Particular circuitry analysis will be carried out in the next chapters.

Usually, the four-element RPC has a wide response frequency band, which is defined as the frequency width between the two half-power points. If the circuit is a low-pass filter, the frequency bands can cover the frequency range from 0 to the high half-power point that is definitely higher than the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. The working point can be selected in a wide area across (lower and higher than) the natural resonant frequency $\omega_0 = 1/\sqrt{LC}$. Another advantage is that the transferred waveform is sinusoidal, that is, the output waveform THD is very close to zero. As is well-known, the monofrequency waveform transferring operation has a very low EMI and reasonable electromagnetic susceptibility and electromagnetic compatibility.

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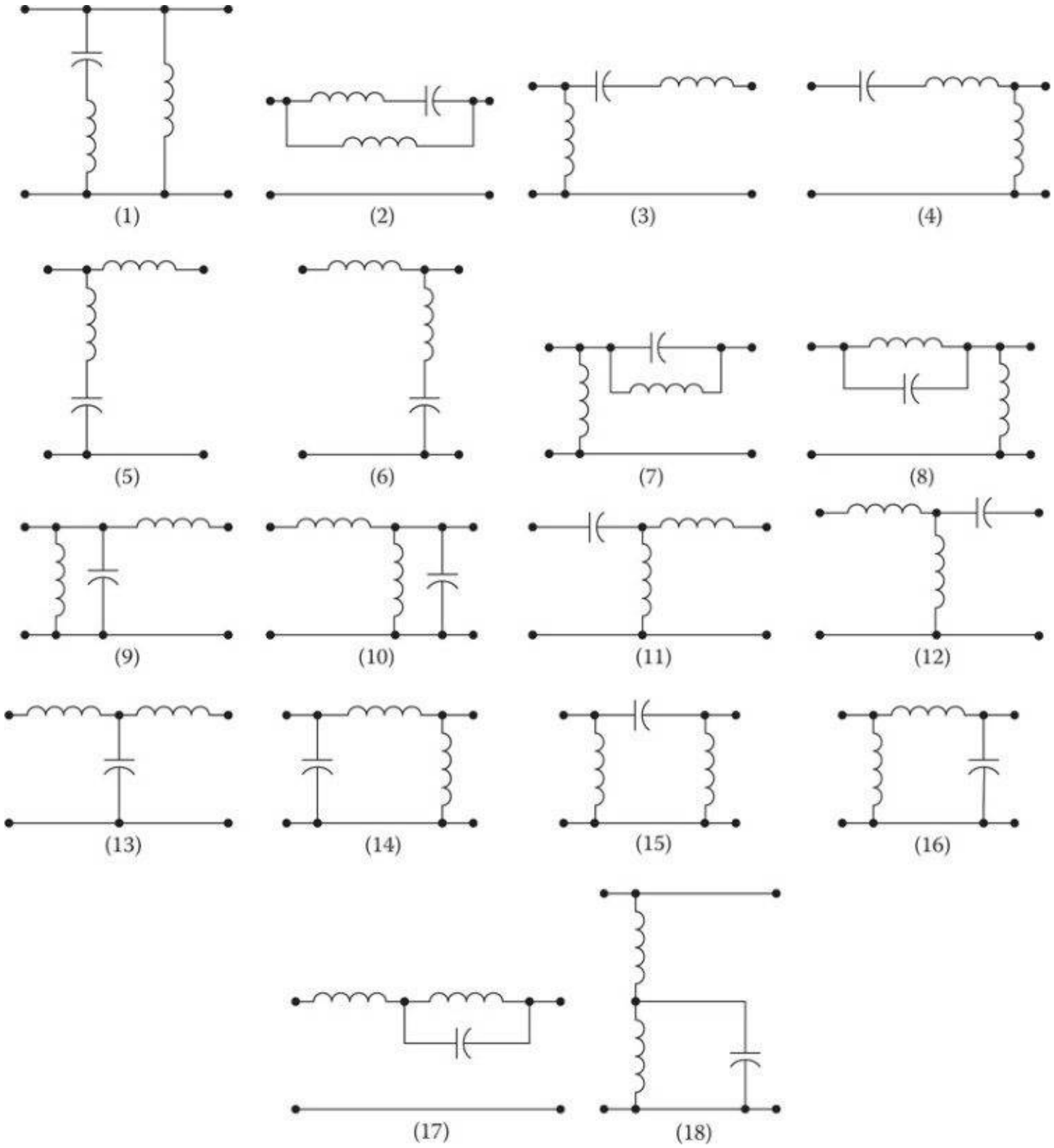
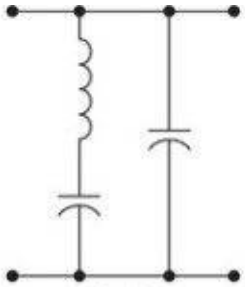
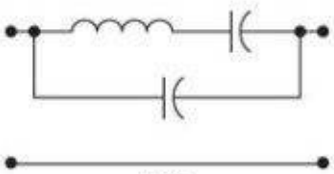
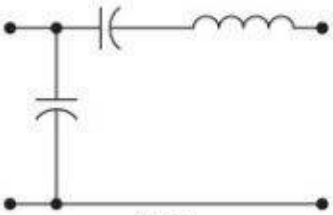


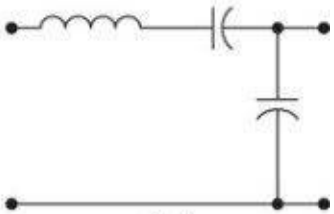
FIGURE 16.2
The 38 topologies of three-element resonant power converter.

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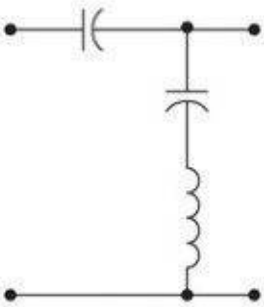

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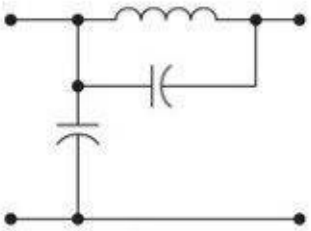

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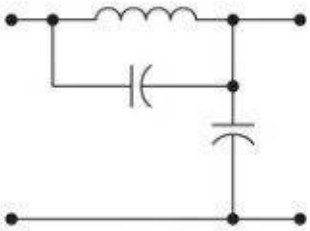

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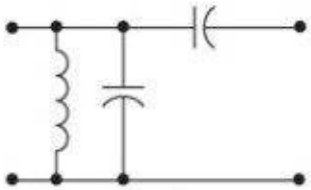

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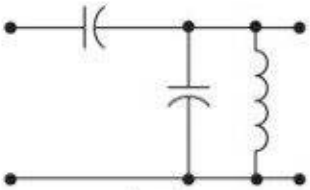

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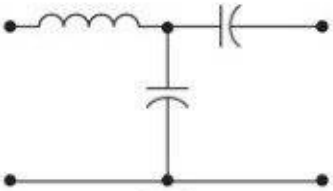

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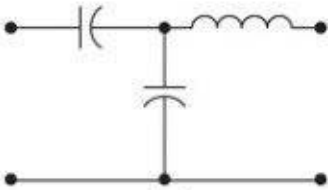

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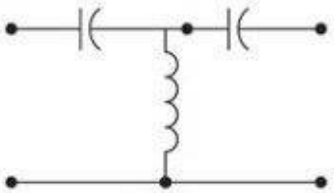

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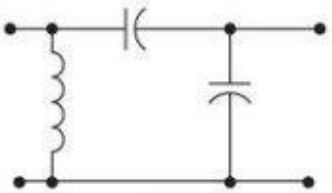

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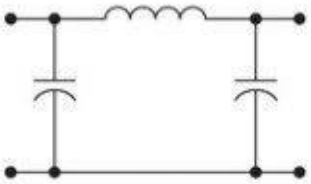

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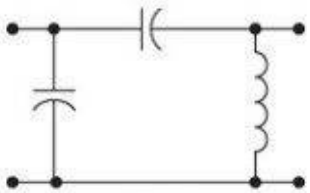

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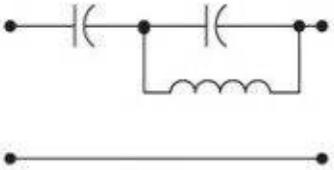

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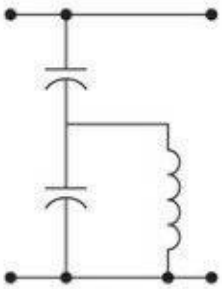

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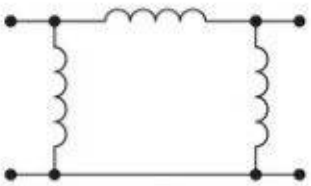

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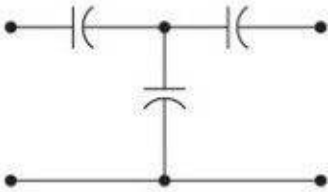

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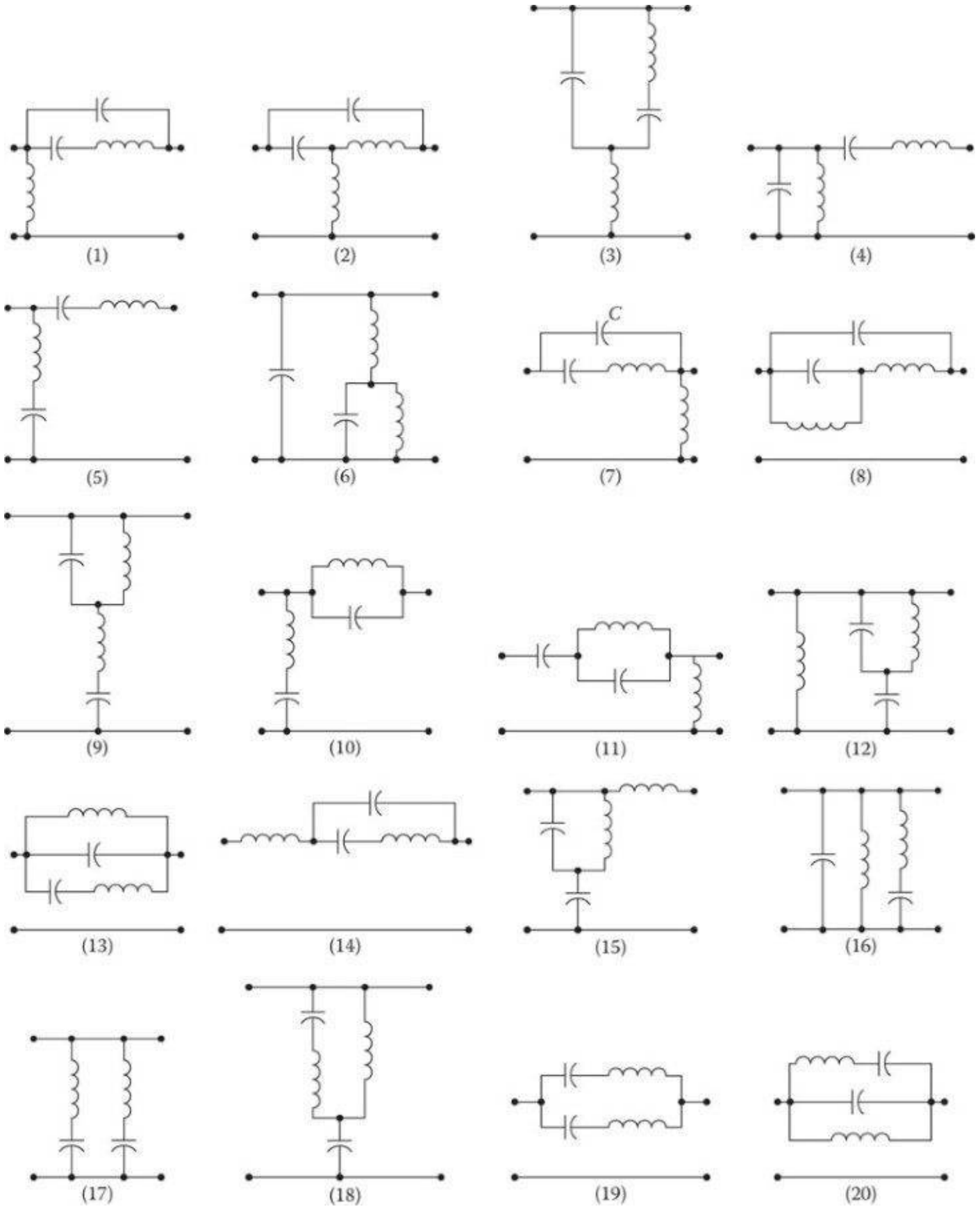
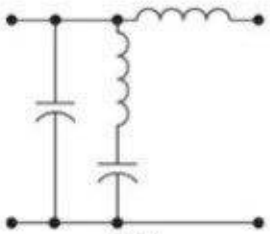
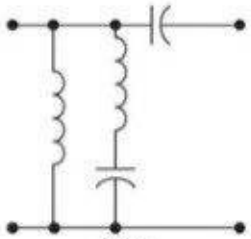


FIGURE 16.3
The 98 topologies of four-element (2*L*–2*C*).

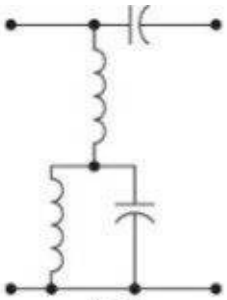
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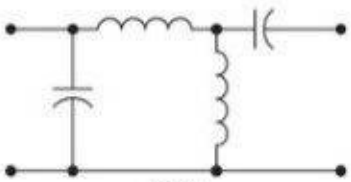
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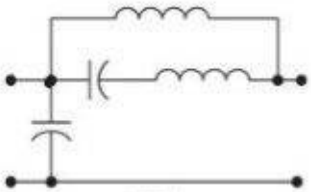
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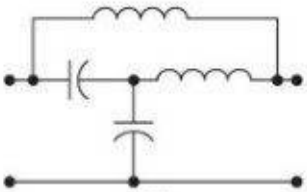
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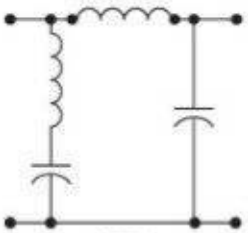
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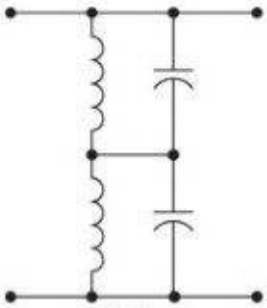
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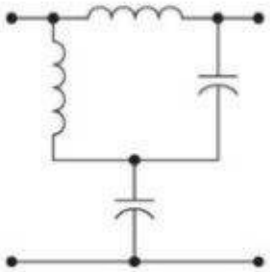
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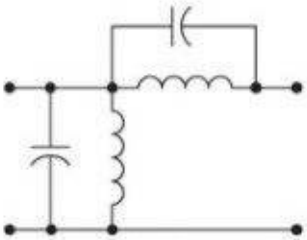
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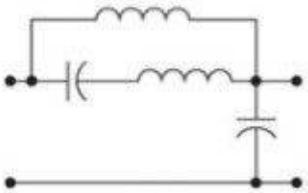
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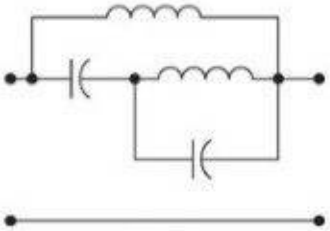
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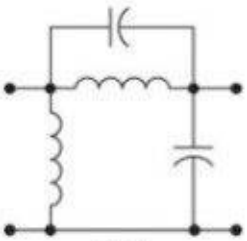
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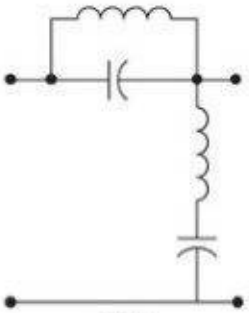
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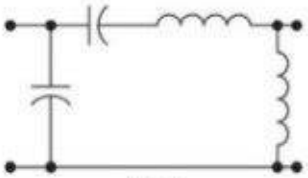
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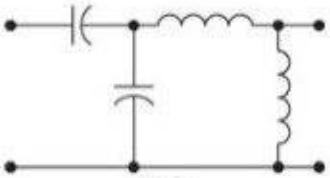
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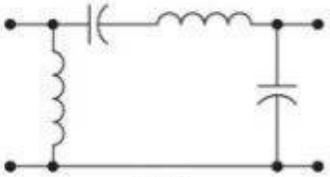
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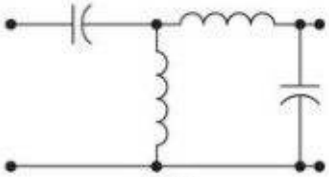
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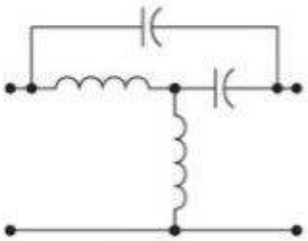
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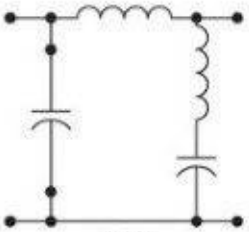
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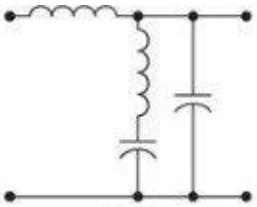


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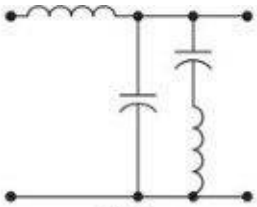


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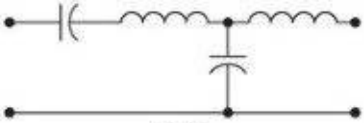
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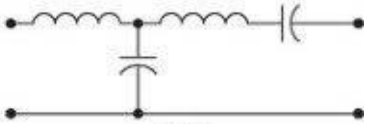
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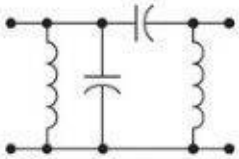
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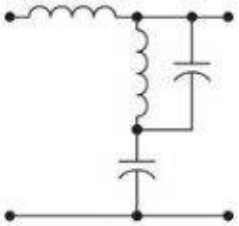
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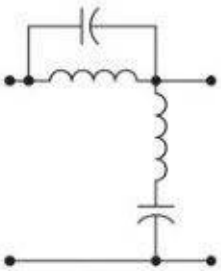
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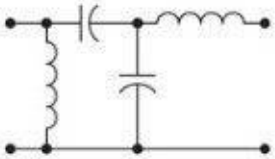
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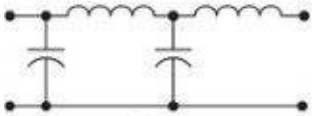
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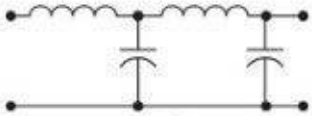
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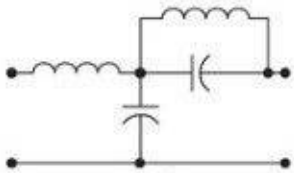
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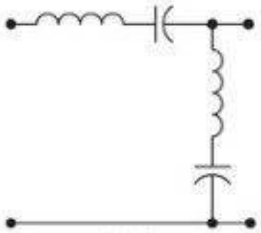
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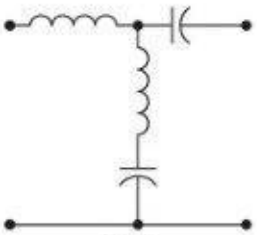
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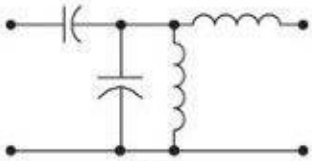
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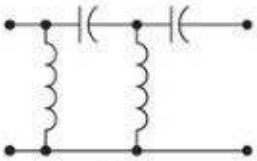
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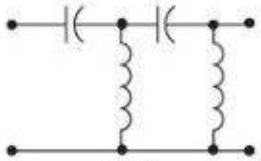
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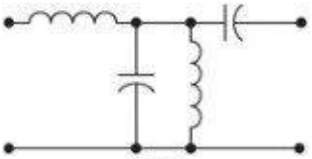
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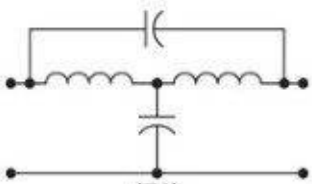
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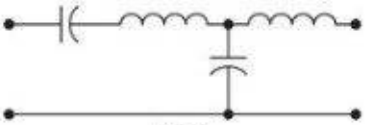
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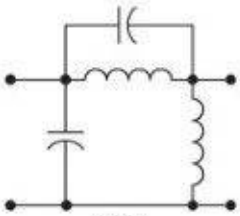
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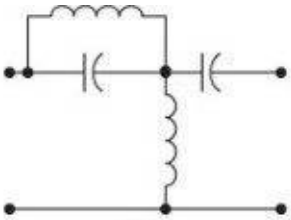


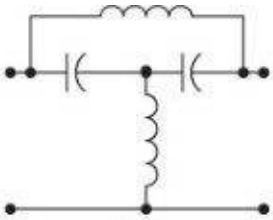
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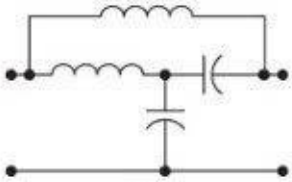


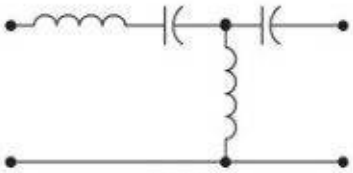
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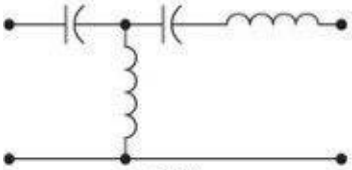
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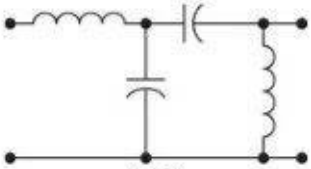

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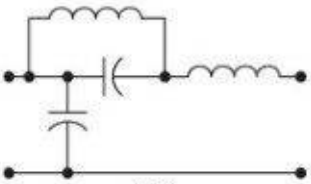

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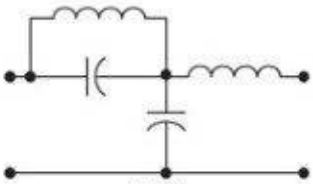

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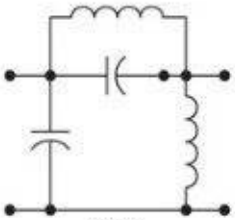

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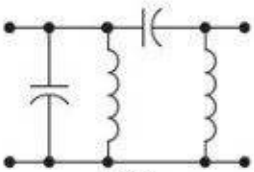

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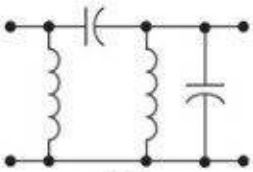

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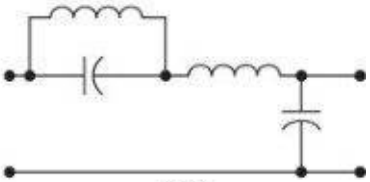

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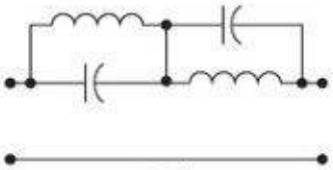

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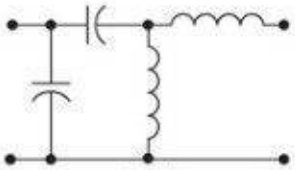

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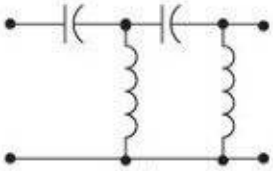

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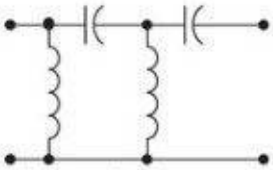

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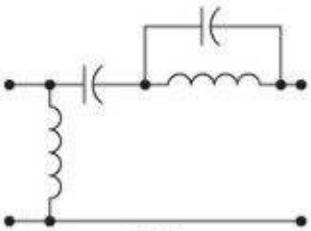

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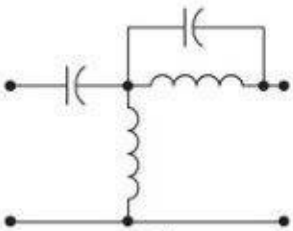

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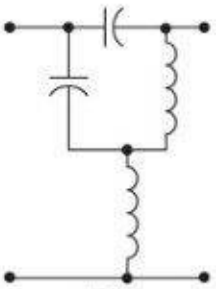

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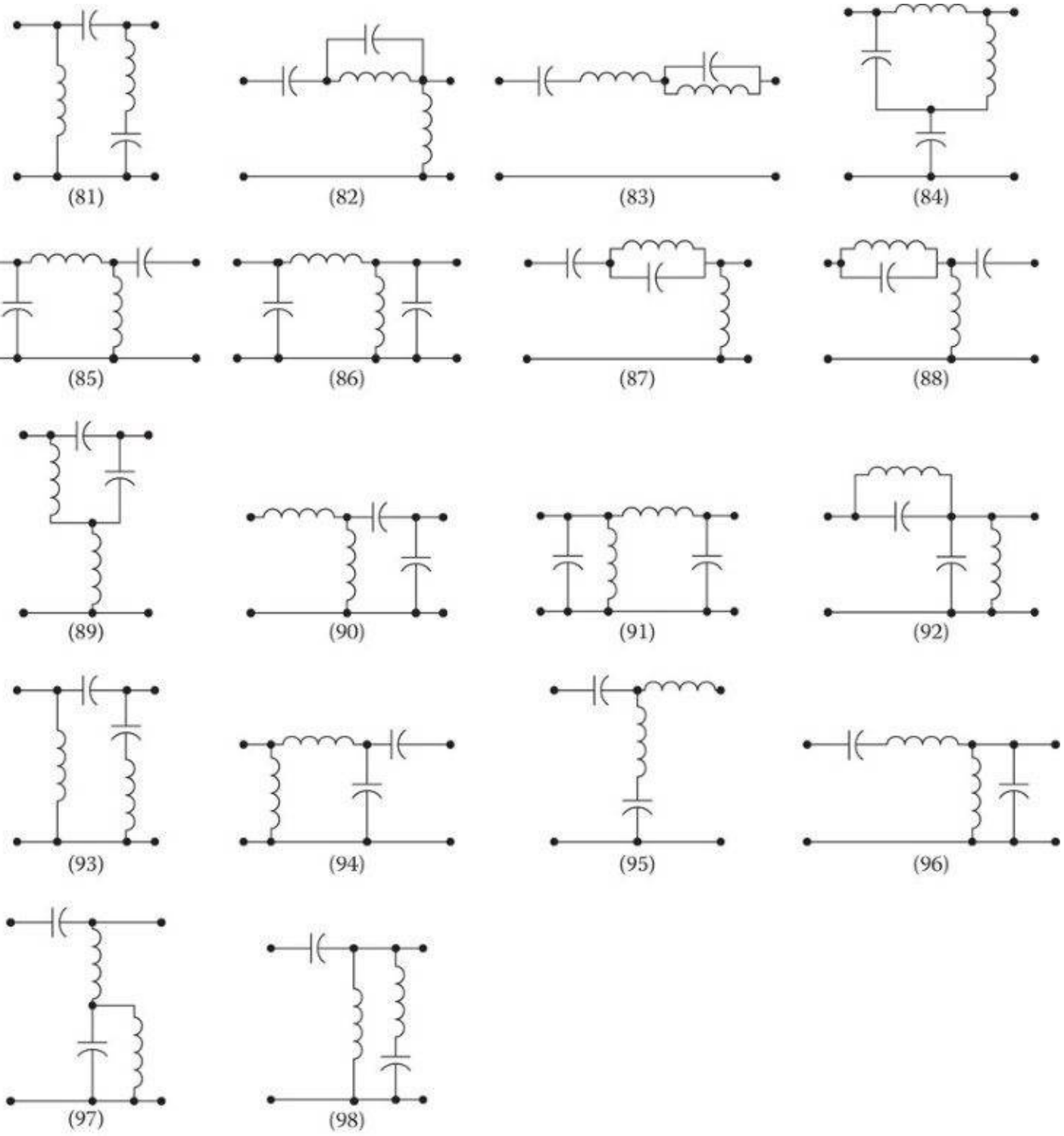

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16.2 Bipolar Current and Voltage Sources

Depending on the application, a resonant network can be low-pass filter, high-pass filter, or band-pass filter. For a large power transferring process, a low-pass filter is usually employed. In this case, inductors are arranged in series arms and capacitors are arranged in shut arms. If the first component is an inductor, only voltage source can be applied since inductor current

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is continuous. Vice versa, if the first component is a capacitor, only current source can be applied since capacitor voltage is continuous. Unipolar current and voltage source are easier to obtain using various pumps, such as buck pump, boost pump, and buck-boost pump, which are introduced in Chapter 1.

Bipolar current and voltage sources are more difficult to obtain using these pumps. There are some fundamental bipolar current and voltage sources listed in the following sections.

16.2.1 Bipolar Voltage Source

There are various methods to obtain bipolar voltage sources using pumps.

16.2.1.1 Two-Voltage Source Circuit

A bipolar voltage source using two voltage sources is shown in Figure 16.4. These two voltage sources have same voltage amplitude and reverse polarity. There are two switches applied alternatively switching-on and switching-off to supply positive and negative voltage to the network. In the figure, the load is a resistance *R*.

The circuit of this voltage source is likely a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons, the particular circuitry design has to consider some small gap between the turnover (commutation) operations to avoid a short circuit.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz and 5 MHz depending on the application conditions.

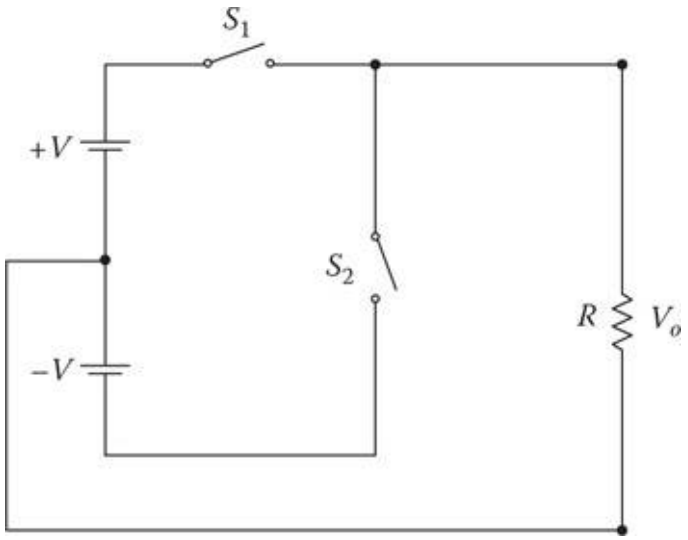


FIGURE 16.4
A bipolar voltage source using two voltage sources.

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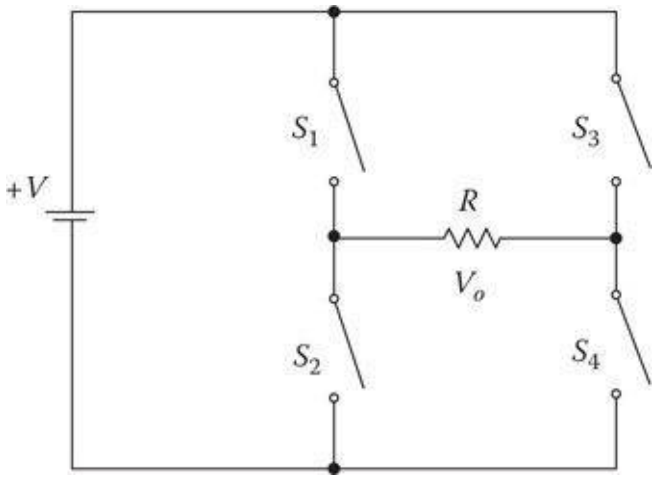


FIGURE 16.5
A bipolar voltage source using single voltage source.

16.2.1.2 One-Voltage Source Circuit

A bipolar voltage source using single voltage source is shown in Figure 16.5. Since only voltage source is applied, there are four switches applied alternatively switching-on and switching-off to supply positive and negative voltage to the network. In the figure, the load is a resistance *R*.

The circuit of this voltage source is likely to be a four-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons, the particular circuitry design has to consider some small gap between the turnover (commutation) operations to avoid a short-circuit incidence.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz and 5 MHz depending to the application conditions.

16.2.2 Bipolar Current Source

There are various methods used to obtain bipolar current sources using the pumps.

16.2.2.1 Two-Voltage Source Circuit

A bipolar current voltage source using two voltage sources is shown in Figure 16.6. These two voltage sources have the same voltage amplitude and reverse polarity. To obtain stable current, each voltage source in series is connected by a large inductor. There are two switches applied alternately switching-on and switching-off to supply positive and negative current to the network. In Figure 16.6, the load is a resistance *R*.

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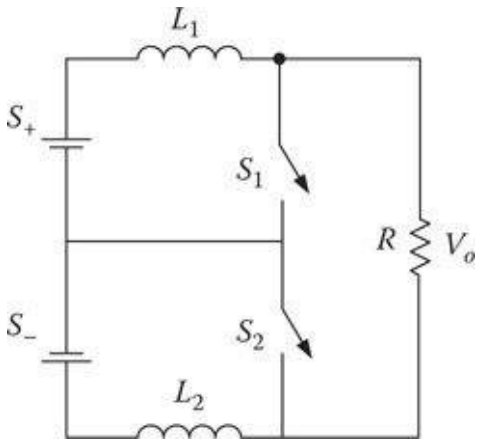


FIGURE 16.6
A bipolar current source using two voltage sources.

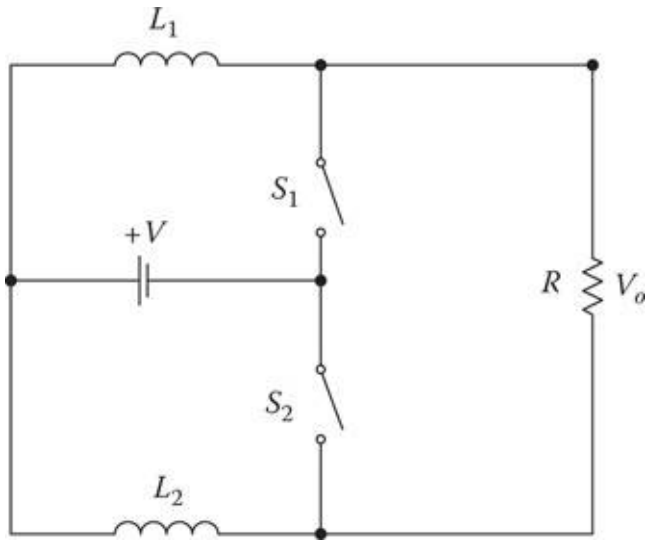


FIGURE 16.7
A bipolar current voltage source using single voltage source.

The circuit of this current source is a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons, the particular circuitry design has to consider some small gap between the turnover (commutation) operations to avoid a short circuit.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz and 5 MHz depending on the application conditions.

16.2.2.2 One-Voltage Source Circuit

A bipolar current voltage source using single voltage sources is shown in Figure 16.7. To obtain stable current, the voltage source in series is connected by a large inductor. There are two switches applied alternately switching-on and switching-off to supply positive and negative current to the network. In the figure, the load is a resistance *R*.

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The circuit of this current source is likely a two-quadrant operational chopper. The conduction duty cycle for each switch is 50%. For safety reasons the particular circuitry design has to consider some small gap between the turnover (commutation) operations to avoid a short circuit.

The repeating frequency is theoretically not restricted. For industrial applications, the operating frequency is usually arranged in the range between 10 kHz and 5 MHz depending on the application conditions.

16.3 Two-Element RPC Analysis

This two-element RPC is the circuit number 6 in Figure 16.1. The network is a low-pass capacitor-inductor (CL) filter, and the first component is a capacitor. By previous analysis, the source should be a bipolar current source. Therefore, the circuit diagram of the two-element RPC is shown in Figure 16.8. To simplify the analysis, the load can be considered resistive R. The energy source V_{in} is chopped by two main switches S_1 and S_2; it is a bipolar current source applied to the two-element filter and load. The whole RPC equivalent circuit diagram is shown in Figure 16.9.

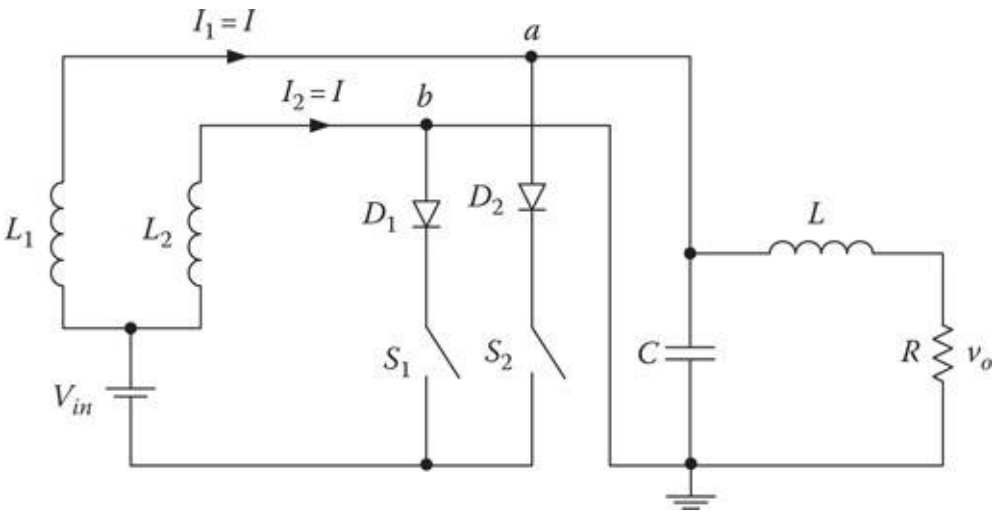


FIGURE 16.8
A two-element resonant power converter.

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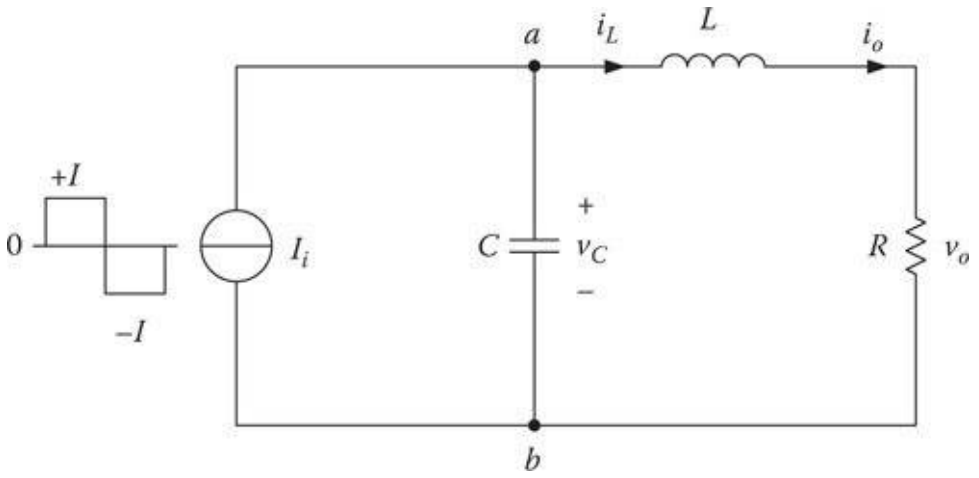


FIGURE 16.9
The equivalent circuit diagram of the two-element resonant power converter.

16.3.1 Input Impedance

The whole network impedance including the load R is calculated by

$$Z = \frac{R + j\omega L}{1 + j\omega C(R + j\omega L)} = \frac{R + j\omega L}{1 - \omega^2 CL + j\omega RC} \tag{16.1}$$

The natural resonance angular frequency is

$$\omega_0 = \frac{1}{\sqrt{CL}} \tag{16.2}$$

Using the relevant frequency β

$$\beta = \frac{\omega}{\omega_0} = \frac{\omega}{\sqrt{CL}} \tag{16.3}$$

and the quality factor Q

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \tag{16.4}$$

we rewrite the input impedance

$$\frac{Z}{R} = \frac{1 + j\beta Q}{1 - \beta^2 + j\beta/Q} = \left|\frac{Z}{R}\right| \angle\phi \tag{16.5}$$

where

$$\left|\frac{Z}{R}\right| = \sqrt{\frac{1 + (\beta Q)^2}{(1 - \beta^2)^2 + (\beta/Q)^2}}$$

$$\phi = \tan^{-1}\beta Q - \tan^{-1}\frac{\beta/Q}{1 - \beta^2}$$

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16.3.2 Current Transfer Gain

The current transfer gain is calculated by

$$G(\omega)=\frac{i_o}{i_{in}}=\frac{1}{1+j\omega C(R+j\omega L)}=\frac{1}{1-\omega^2CL+j\omega RC} \tag{16.6}$$

Defining an auxiliary parameter B,

$$B(\omega)=1+j\omega C(R+j\omega L) \tag{16.7}$$

Hence,

$$G(\omega)=\frac{1}{B(\omega)}=|G|\angle\theta \tag{16.8}$$

Using the relevant frequency and quality factor,

$$G(\beta)=\frac{i_o}{i_{in}}=\frac{1}{1-\beta^2+j(\beta/Q)} \tag{16.9}$$

$$B(\beta)=1-\beta^2+j\frac{\beta}{Q} \tag{16.10}$$

and

$$|G|=\sqrt{\frac{1}{(1-\beta^2)^2+(\beta/Q)^2}}$$

$$\theta=-\tan^{-1}\frac{\beta/Q}{1-\beta^2}$$

16.3.3 Operation Analysis

Based on the equivalent circuit in Figure 16.9, the state equation is established as

$$\begin{pmatrix}\dot{i}_L\\ \dot{v}_C\end{pmatrix}=\begin{pmatrix}-\frac{R}{L} & \frac{1}{L}\\ -\frac{1}{C} & 0\end{pmatrix}\begin{pmatrix}i_L\\ v_C\end{pmatrix}+\begin{pmatrix}0\\ \frac{I}{C}\end{pmatrix} \tag{16.11}$$

By Laplace transform, the state equation in time domain could be transferred into s-domain, given by

$$\begin{cases}sLI_L(s)-LI_L(0)=V_C(s)-I_L(s)R\\ sCV_C(s)-CV_C(0)=I/s-I_L(s)\end{cases} \tag{16.12}$$

yielding

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$$I_L(s) = \frac{sLCI_L(0) + I/s + CV_C(0)}{s^2LC + sRC + 1} = \frac{s[I_L(0) - I] + [V_C(0) - IR]/L}{(s + (R/2L))^2 + (1/LC) - (R^2/4L^2)} + \frac{I}{s} \tag{16.13}$$

The inductor current in time domain is then derived by taking the inverse Laplace transform, giving

$$i_L(t) = a_1 e^{-\alpha t} \cos\beta t + \frac{b_1 - a_1\alpha}{\beta} e^{-\alpha t} \sin\beta t + I \tag{16.14}$$

where

$$a_1 = I_L(0) - I$$

$$b_1 = \frac{V_C(0) - IR}{L}$$

α is the damping ratio, $\alpha = R/2L$
β is the resonant angular frequency, $\beta = \sqrt{(1/LC) - (R^2/4L^2)}$

Similarly, the resonant capacitor voltage in *s*-domain is attained as

$$V_C(s) = \frac{sLCV_C(0) + (IR/s) + [L(I_L(0) - I) + RCV_C(0)]}{s^2LC + sRC + 1}$$

$$= \frac{sLC[V_C(0) - IR] + \{L[I - I_L(0)] + RCV_C(0) - IR^2C\}}{s^2LC + sRC + 1} + \frac{IR}{s} \tag{16.15}$$

The corresponding expression in time domain is written as

$$v_C(t) = a_2 e^{-\alpha t} \cos\beta t + \frac{b_2 - a_2\alpha}{\beta} e^{-\alpha t} \sin\beta t + IR \tag{16.16}$$

where

$$a_2 = V_C(0) - IR$$
$$b_2 = \{L[I - I_L(0)] + RCV_C(0) - IR^2C\}/LC$$

To make the analytic equations (16.14) and (16.16) available, the initial conditions must be known at first. Here, the periodic nature is applied under steady-state operation. Namely, during one switching cycle, the resonant voltage and current at the initial instant should have the same absolute values with negative sign as those at the half cycle, that is,

$$i_L(0) = I_L(0) = -i_L\left(\frac{T_s}{2}\right)$$
$$v_C(0) = V_C(0) = -v_C\left(\frac{T_s}{2}\right) \tag{16.17}$$

Substituting this into Equations 16.14 and 16.16, respectively, yields

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$$\begin{cases} -I_L(0) = a_1 e^{-\frac{\alpha T_s}{2}} \cos\left(\frac{\beta T_s}{2}\right) + \frac{b_1 - a_1\alpha}{\beta} e^{-\frac{\alpha T_s}{2}} \sin\left(\frac{\beta T_s}{2}\right) + I \\ -V_C(0) = a_2 e^{-\frac{\alpha T_s}{2}} \cos\left(\frac{\beta T_s}{2}\right) + \frac{b_2 - a_2\alpha}{\beta} e^{-\frac{\alpha T_s}{2}} \sin\left(\frac{\beta T_s}{2}\right) + IR \end{cases} \tag{16.18}$$

Rearranging,

$$\begin{cases} m_{11} V_C(0) + m_{12} I_L(0) = n_1 \\ m_{21} V_C(0) + m_{22} I_L(0) = n_2 \end{cases} \tag{16.19}$$

where

$$m_{11} = \frac{1}{L} e^{-\frac{\alpha T_s}{2}} \sin\left(\frac{\beta T_s}{2}\right)$$

$$m_{12} = e^{-\frac{\alpha T_s}{2}} \left[\beta \cos\left(\frac{\beta T_s}{2}\right) - \alpha \sin\left(\frac{\beta T_s}{2}\right)\right] + \beta$$

$$n_1 = Ie^{-\frac{\alpha T_s}{2}} \left[\beta \cos\left(\frac{\beta T_s}{2}\right) + \alpha \sin\left(\frac{\beta T_s}{2}\right)\right] - \beta I$$

$$m_{21} = e^{-\frac{\alpha T_s}{2}} \left[\beta \cos\left(\frac{\beta T_s}{2}\right) + \alpha \sin\left(\frac{\beta T_s}{2}\right)\right] + \beta$$

$$m_{22} = -\frac{1}{C} e^{-\frac{\alpha T_s}{2}} \sin\left(\frac{\beta T_s}{2}\right)$$

$$n_2 = Ie^{-\frac{\alpha T_s}{2}} \left[R\beta \cos\left(\frac{\beta T_s}{2}\right) - \frac{1 - \alpha RC}{C} \sin\left(\frac{\beta T_s}{2}\right)\right] - \beta IR$$

Since all the parameters shown in the coefficients of Equation 16.19 are constant for a given circuit, the initial values of the resonant voltage and current can be calculated. Thus, the complete expressions of the resonant voltage and current are obtained by substituting $V_C(0)$ and $I_L(0)$ into Equations 16.14 and 16.16.

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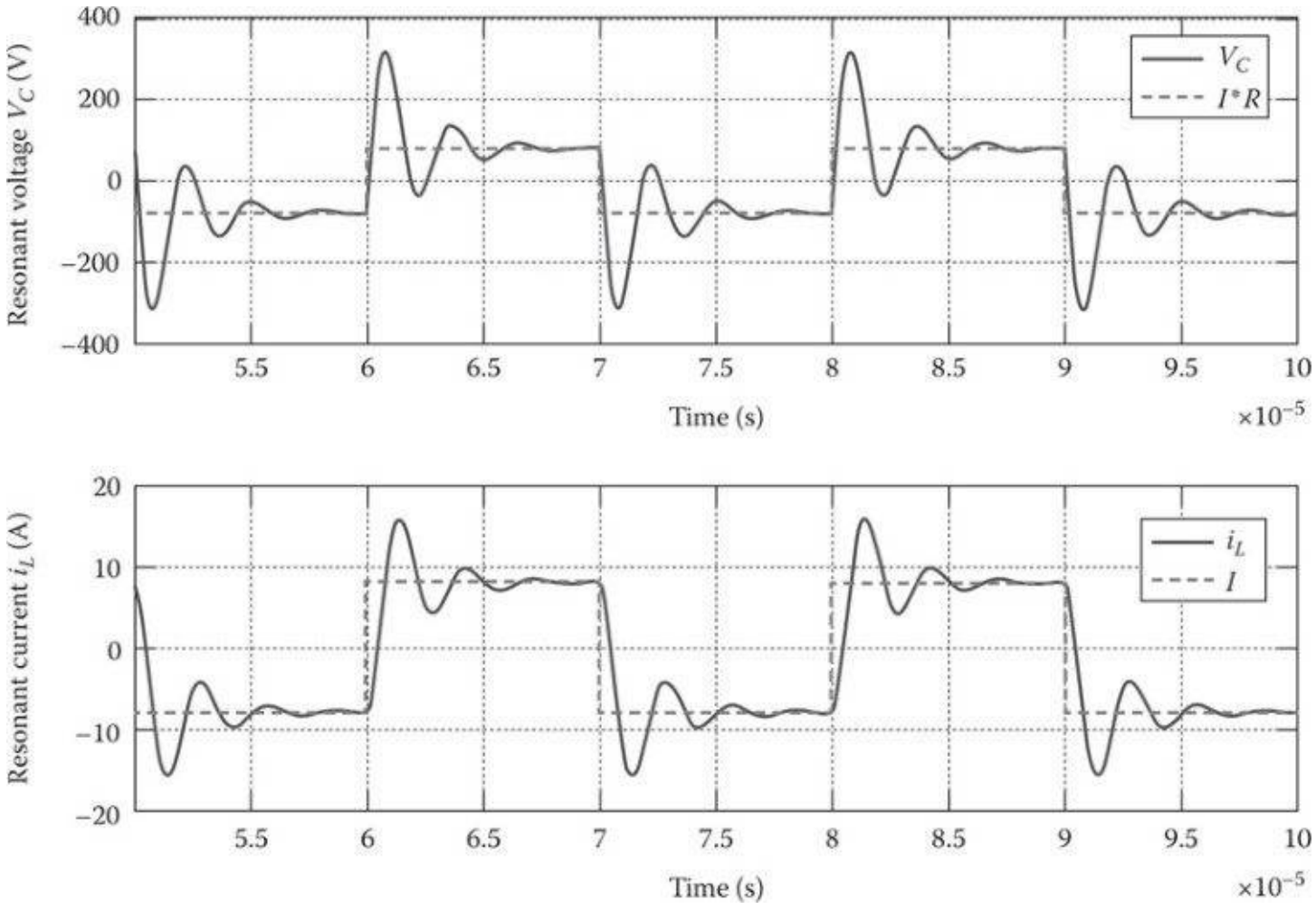


FIGURE 16.10
General waveforms of the resonant voltage v_c and current i_L.

Figure 16.10 shows the general waveforms of resonant voltage $v_C(t)$ and current $i_L(t)$. As seen, both of them are oscillatory and track following. Actually, further investigation of Equation 16.14 states that inductor current can be rewritten as

$$i_L(t) = a_1 e^{-\alpha t}\cos\beta t + \frac{b_1 - a_1\alpha}{\beta} e^{-\alpha t}\sin\beta t + I = Ae^{-\alpha t}\sin(\beta t + \varphi) + I \tag{16.20}$$

where

$$A = \sqrt{a_1^2 + \left(\frac{b_1 - a_1\alpha}{\beta}\right)^2}$$

$$\varphi = \tan^{-1}\left(\frac{a_1\beta}{b_1 - a_1\alpha}\right)$$

It is apparent that the inductor current is composed of two different components. One is the oscillatory component, consisting of the sinusoidal function. The other is the compulsory component, given as the input current I. The oscillatory component is time attenuation. With

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the time increasing, it will be attenuated to zero and the inductor current is then convergent to the compulsory component. The attenuating rate is determined by the damping ratio a. Larger ratios cause faster attenuation. Similar conclusions can also be made about the capacitor voltage $v_C(t)$.

When the value of damping factor $e^{-\alpha T_s/2}$ is approaching 1, the resonant voltage and current will contain an undamped oscillatory component. Hence, the coefficients in Equation 16.19 can be simplified accordingly, giving

$$m'_{11} = \frac{1}{L}\sin\left(\frac{\beta T_s}{2}\right)$$

$$m'_{12} = \beta\cos\left(\frac{\beta T_s}{2}\right) - \alpha\sin\left(\frac{\beta T_s}{2}\right) + \beta$$

$$n'_1 = \beta\left[\cos\left(\frac{\beta T_s}{2}\right) - 1\right]I + \alpha\sin\left(\frac{\beta T_s}{2}\right)I$$

$$m'_{21} = \beta\cos\left(\frac{\beta T_s}{2}\right) + \alpha\sin\left(\frac{\beta T_s}{2}\right) + \beta$$

$$m'_{22} = -\frac{1}{C}\sin\left(\frac{\beta T_s}{2}\right)$$

$$n'_2 = I\left[R\beta\cos\left(\frac{\beta T_s}{2}\right) - \frac{1-\alpha RC}{C}\sin\left(\frac{\beta T_s}{2}\right)\right] - \beta IR$$

16.3.4 Simulation Results

For the purpose of verifying the mathematical derivations, a prototype bipolar current source resonant inverter is proposed for the simulation and experiments. The simulation is carried out by PSpice, and the results are presented in Figure 16.11a, where the upper channel is the input square wave current I_i and the lower channel is the output current i_o, respectively. The corresponding FFT spectrums are shown in Figure 16.11b. From the results obtained, it can be found that the output current is very sleekly sinusoidal with the amplitude larger than the input fundamental current. The THD value is only 1.2%. It is obvious that the resonant network has the capability of attenuating the higher-order harmonics in the input square wave current and transferring their energy into the output current. Due to the advantages of high current transfer gain and negligible output harmonics, this inverter could be widely used in many high-frequency high-current applications.

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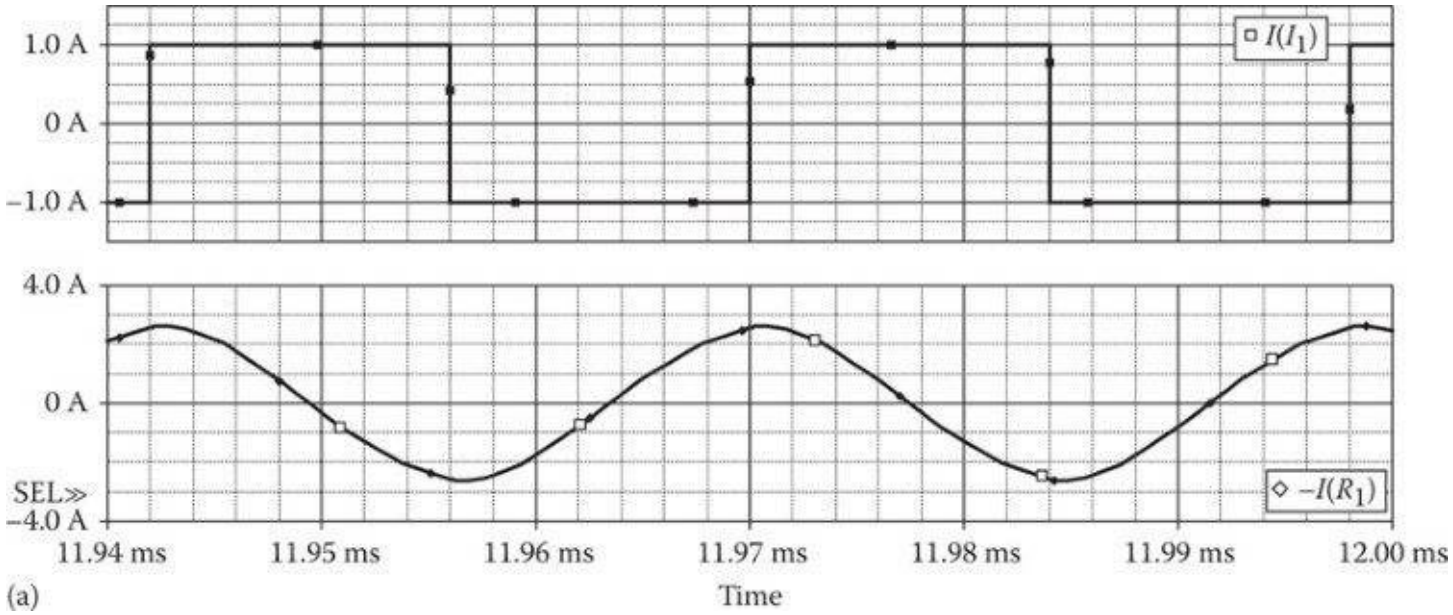
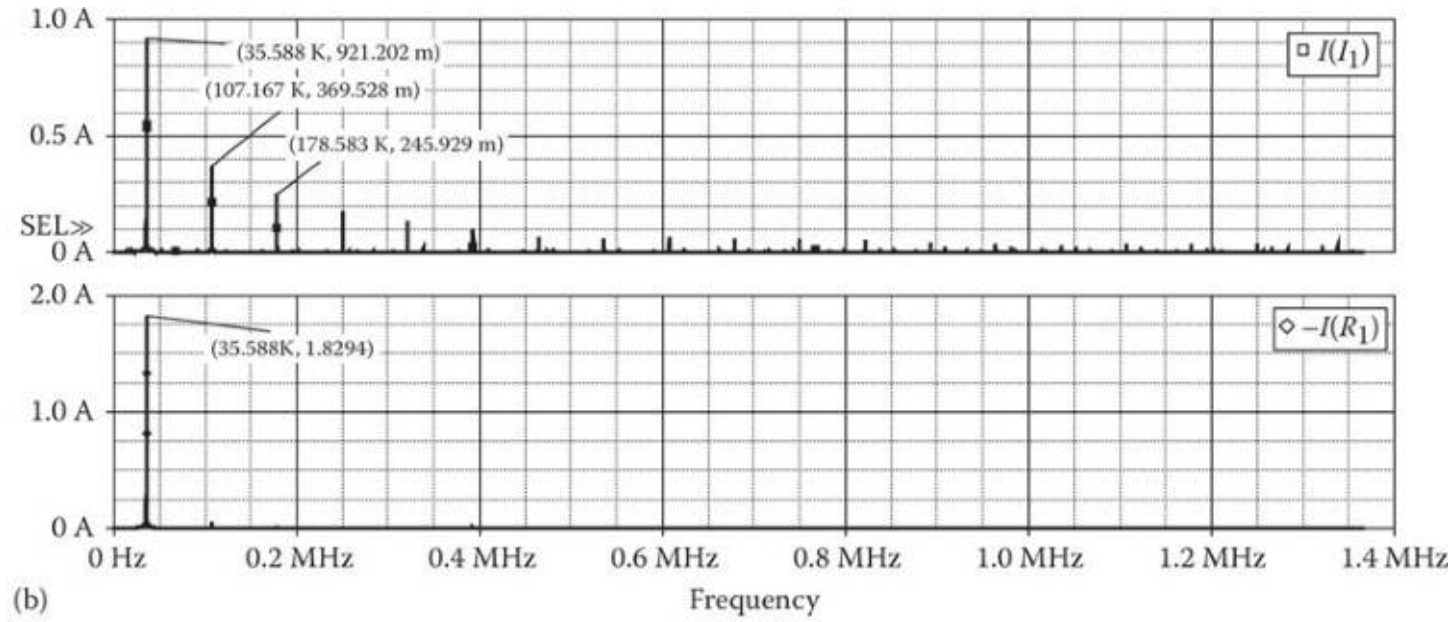


FIGURE 16.11
The simulation waveforms of the input and output currents. (a) Input and output current waveforms.



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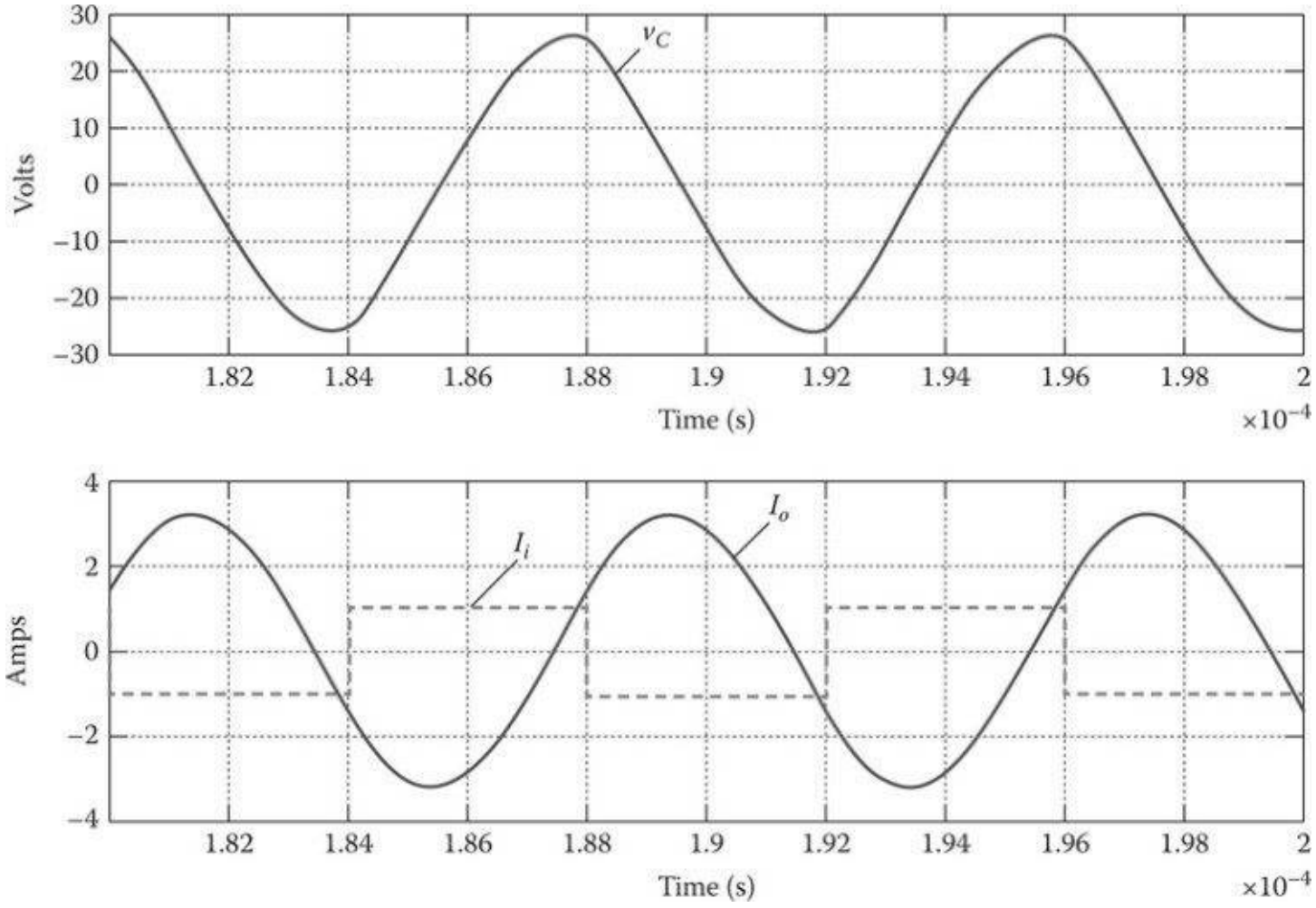


FIGURE 16.12
Tested waveforms of the resonant voltage and current under undamped condition.

16.3.5 Experimental Results

The corresponding resonant waveforms under this condition are shown in Figure 16.12, where both the capacitor voltage and the inductor current, that is, output current, are undamped oscillatory.

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17

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Π-*CLL Current Source Resonant Inverter*

17.1 Introduction

This chapter introduces a three-element current source resonant inverter (CSRI): n-CLL consists of three energy-storage element CLL, the Π-CLL. A bipolar current source is employed in this circuit as described in Chapter 16 and shown in Figure 16.7. Since there is no transformer and the circuit is not working in push-pull operation, the control circuit is very simple and power losses are low. This Π-CLL CSRI is shown in Figure 17.1. The energy source is a DC voltage V_{in}, which is chopped by two main switches S_1 and S_2. The three energy-storing elements are C, L_1, and L_2. Two inductors can be different, that is, $L_2 = pL_1$ with p as a random value. The load can be a coil, transformer, or HF annealing equipment. A resistance R_{eq} is assumed. Its equivalent circuit diagram is shown in Figure 17.2.

17.1.1 Pump Circuits

In this application, two boost pumps are used working at the conduction duty k = 0.5. Each pump consists of the common DC voltage source V_{in}, a switch S, and a large inductor L. The pump out energy is usually measured by output current injection.

17.1.2 Current Source

An ideal current source has infinite impedance and constant output current. If the inductance of the pump circuits is large enough, the current flowing through it may keep a nearly constant value. The internal equivalent impedance of the pump is very high. The ripple of the inductor current depends on the input voltage, inductor's inductance, switching frequency, and conduction duty.

17.1.3 Resonant Circuit

Like other resonant inverters, this Π-CLL CSRI consists of a resonant circuit sandwiched between the current source (input switching circuit) and the output load. The resonant circuit can be considered as a Π-CLL low-pass filter. By network theory, these three components construct a circuit that is no longer a real low-pass filter. Therefore, the Π-CLL circuit has two peak resonant points. It gives more convenience to designers to match in the industrial applications.

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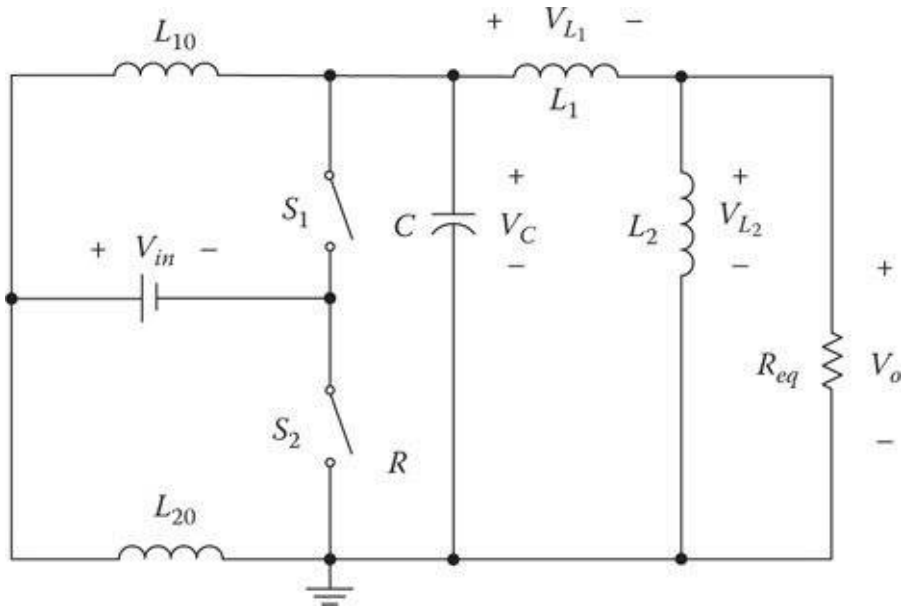


FIGURE 17.1
The Π-CLL current source resonant inverter.

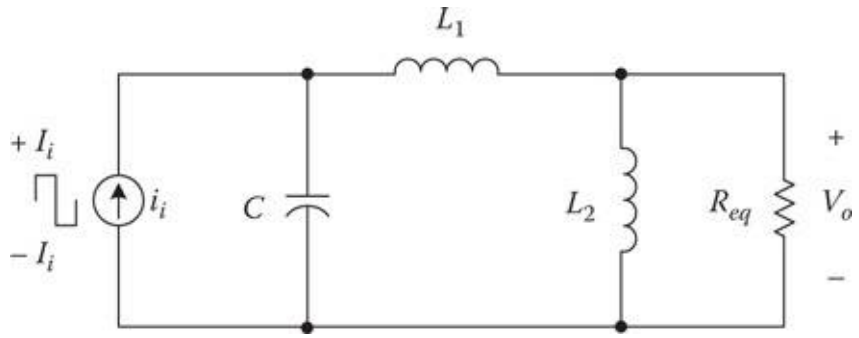


FIGURE 17.2
The equivalent circuit.

17.1.4 Load

Load is usually resistive load or inductive plus resistive load. To simplify the problem, we use R_{eq} to represent either an actual or an equivalent resistance to consume the output power. This assumption is reasonable, because the load inductance can be considered the parallel part to the inductor L_2.

17.1.5 Summary

The switching circuit consists of two pumps (2 boost pumps employed): The R_{eq} is, as mentioned earlier, either an actual or an equivalent AC load resistance. The source current i_i is a constant current yielded by input voltage V_i via large inductors L_{10} and L_{20}. To operate this circuit, S_1 is turned on and off in 180° (S_2 is idle) at the frequency $\omega = 2\pi f$ After the switching circuit, input current can be considered a bipolar square wave current alternating in

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value between $+I_i$ and $-I_i$ that is then input to the resonant circuit section. The equivalent circuit is shown in Figure 17.2.

17.2 Mathematical Analysis

In order to concentrate the function analysis of this Π-CLL, we assume the following:

1. The inverter's source is a constant current source determined by the pump circuits.
2. Two metal–oxide–semiconductor field-effect transistos (MOSFETs) in the switching circuit are turned on and turned off 180° out of phase with each other at the same switching frequency and with a duty cycle of 50%.
3. Two switches are ideal components without switch-on resistance and negligible parasitic capacitance and zero switching time.
4. Two diodes are components having a zero forward voltage drop and forward resistance.
5. Four energy-storage elements are passive, linear, and time invariant and do not have parasitic reactive components.

Using these assumptions, the following analyses are based on using Figure 17.2.

17.2.1 Input Impedance

This CSRI is a third-order system. The mathematical analysis of operation and stability is more complex than three energy-storage element CSRIs. The input impedance is given by

$$Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq}(L_1 + L_2)}{R_{eq}[1-\omega^2(L_1+L_2)C] + j\omega L_2(1-\omega^2 L_1 C)} \tag{17.1}$$

The corresponding phase angle is

$$\phi(\omega) = \tan^{-1}\left\{\frac{\omega R_{eq}(L_1+L_2)}{-\omega^2 L_1 L_2}\right\} - \tan^{-1}\left\{\frac{\omega L_2(1-\omega^2 L_1 C)}{R_{eq}[1-\omega^2(L_1+L_2)C]}\right\} \tag{17.2}$$

Define

$$B(\omega) = R_{eq}[1-\omega^2(L_1+L_2)C] + j\omega L_2(1-\omega^2 L_1 C) \tag{17.3}$$

so that

$$Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq}(L_1+L_2)}{B(\omega)} \tag{17.4}$$

17.2.2 Components' Voltages and Currents

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This Π-CLL CSRI has three resonant components C, L_1 and L_2, and the output equivalent resistance R_{eq}. In order to compare with the parameters easily, all components' voltages and currents are responded to the input fundamental current I_i. All transfer functions are in the frequency domain (ω-domain).

The voltage and current on capacitor C is given by

$$\frac{V_C(\omega)}{I_{in}(\omega)} = Z(\omega) = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq}(L_1 + L_2)}{B(\omega)} \tag{17.5}$$

$$\frac{I_C(\omega)}{I_i(\omega)} = \frac{-\omega^2 R_{eq} C(L_1 + L_2) - j\omega^3 C L_1 L_2}{B(\omega)} \tag{17.6}$$

The voltage and current on inductor L_1 is given by

$$\frac{V_{L_1}(\omega)}{I_{in}(\omega)} = \frac{-\omega^2 L_1 L_2 + j\omega R_{eq} L_1}{B(\omega)} \tag{17.7}$$

$$\frac{I_{L_1}(\omega)}{I_{in}(\omega)} = \frac{R_{eq} + j\omega L_2}{B(\omega)} \tag{17.8}$$

The voltage and current on inductor L_2 is given by

$$\frac{V_{L_2}(\omega)}{I_{in}(\omega)} = \frac{j\omega R_{eq} L_2}{B(\omega)} \tag{17.9}$$

$$\frac{I_{L_2}(\omega)}{I_{in}(\omega)} = \frac{R_{eq}}{B(\omega)} \tag{17.10}$$

The output voltage and current on the resistor R_{eq} is given by

$$\frac{V_o(\omega)}{I_{in}(\omega)} = \frac{V_{L_2}(\omega)}{I_{in}(\omega)} = \frac{j\omega R_{eq} L_2}{B(\omega)} \tag{17.11}$$

The current transfer gain is given by

$$g(\omega) = \frac{I_o(\omega)}{I_{in}(\omega)} = \frac{j\omega L_2}{B(\omega)} = \frac{j\omega L_2}{R_{eq}[1 - \omega^2(L_1 + L_2)C] + j\omega L_2(1 - \omega^2 L_1 C)}$$

$$= \frac{1}{(1 - \omega^2 L_1 C) - j(R_{eq}[1 - \omega^2(L_1 + L_2)C]/\omega L_2)} = |g| \angle\theta \tag{17.12}$$

Thus,

$$|g(\omega)| = \frac{1}{\sqrt{(1 - \omega^2 L_1 C)^2 + R_{eq}{}^2[1 - \omega^2(L_1 + L_2)C]^2/(\omega L_2)^2}} \tag{17.13}$$

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$$\theta(\omega) = \tan^{-1} \frac{R_{eq}[1-\omega^2(L_1+L_2)C]}{\omega L_2(1-\omega^2 L_1 C)} \tag{17.14}$$

17.2.3 Simplified Impedance and Current Gain

Usually, we are interested in the input impedance and output current gain rather than all transfer functions listed in Section 17.2.2. To simplify the operation, we can select

$$\omega_0 = \frac{1}{\sqrt{L_1 C}}$$

$$\beta = \frac{\omega}{\omega_0}$$

$$Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}}$$

and

$$p = \frac{L_2}{L_1}$$

Hence,

$$Z(\omega) = \frac{-\beta^2 {\omega_0}^2 L_1 L_2 + j\beta\omega_0 R_{eq}(L_1+L_2)}{R_{eq}[1-\beta^2{\omega_0}^2(L_1+L_2)C] + j\beta\omega_0 L_2(1-\beta^2{\omega_0}^2 L_1 C)}$$

$$= \frac{-\beta^2{\omega_0}^2 p{L_1}^2 + j\beta\omega_0 R_{eq} L_1(1+p)}{R_{eq}[1-\beta^2{\omega_0}^2 L_1(1+p)C] + j\beta\omega_0 p L_1(1-\beta^2{\omega_0}^2 L_1 C)}$$

$$= \frac{-p(\beta Q R_{eq})^2 + j(1+p)\beta Q {R_{eq}}^2}{R_{eq}\{[1-(1+p)\beta^2] + jp\beta Q(1-\beta^2)\}} = |Z|\angle\phi \tag{17.15}$$

Then, obtain

$$B(\beta) = R_{eq}[1-(1+p)\beta^2 + jp\beta Q(1-\beta^2)] \tag{17.16}$$

and

$$\phi(\omega) = \tan^{-1}\left\{\frac{\beta\omega_0 R_{eq} L_1(1+p)}{-p\beta^2{\omega_0}^2{L_1}^2}\right\} - \tan^{-1}\left\{\frac{p\beta\omega_0 L_1(1-\beta^2{\omega_0}^2 L_1 C)}{R_{eq}[1-\beta^2{\omega_0}^2 L_1(1+p)C]}\right\}$$

$$= \tan^{-1}\frac{1+p}{-p\beta Q} - \tan^{-1}\frac{p\beta Q(1-\beta^2)}{1-\beta^2(1+p)} = \pi - \tan^{-1}\frac{1+p}{p\beta Q} - \tan^{-1}\frac{p\beta Q(1-\beta^2)}{1-\beta^2(1+p)} \tag{17.17}$$

Therefore,

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$$Z = \frac{-p\beta^2Q^2 + j\beta Q(1+p)}{1-(1+p)\beta^2 + jp\beta Q(1-\beta^2)} R_{eq} = |Z| \angle \phi \tag{17.18}$$

where

$$|Z| = \frac{\sqrt{p^2\beta^4Q^4 + \beta^2Q^2(1+p)^2}}{\sqrt{[1-(1+p)\beta^2]^2 + [p\beta Q(1-\beta^2)]^2}} R_{eq}$$

$$\frac{|Z|}{R_{eq}} = \frac{\sqrt{(p\beta^2Q^2)^2 + [\beta Q(1+p)]^2}}{\sqrt{[1-(1+p)\beta^2]^2 + [p\beta Q(1-\beta^2)]^2}} \tag{17.19}$$

and

$$\phi = \pi - \tan^{-1}\frac{1+p}{p\beta Q} - \tan^{-1}\frac{p\beta Q(1-\beta^2)}{1-(1+p)\beta^2}$$

The characteristics of input impedance $|Z|/R_{eq}$ versus relevant frequency β referring to $p = 0.5$ and various Q are shown in Figure 17.3 and Table 17.1.

The characteristics of phase angle ϕ versus relevant frequency β referring to $p = 0.5$ and various Q are shown in Figure 17.4 and Table 17.2.

The current transfer gain becomes

$$g = \frac{1}{1-((1+p)\beta^2/jpQ) + 1 - \beta^2} = |g| \angle \theta \tag{17.20}$$

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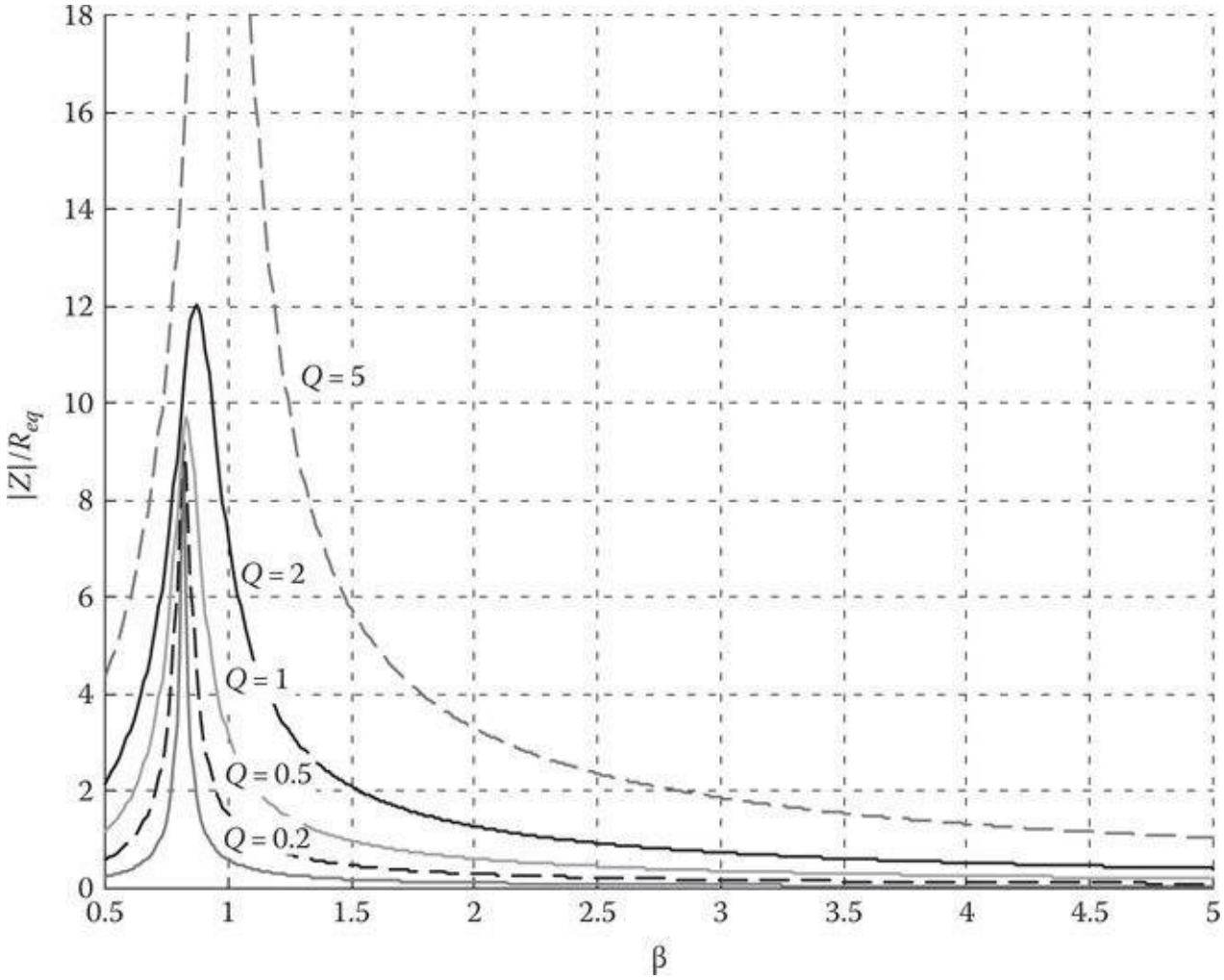


FIGURE 17.3
The curves of $|Z|/R_{eq}$ versus β referring to Q.

TABLE 17.1
$|Z|/R_{eq}$ versus β Referring to $p = 0.5$ and Various Q

	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.2397	0.6513	1.5266	5.9126	0.6013	0.1898	0.1202	0.0721	0.0412
0.5	0.5954	1.5809	3.4353	8.6490	1.5207	0.4790	0.3029	0.1814	0.1033
1	1.1652	2.8924	5.3662	9.6875	3.1623	0.9852	0.6183	0.3673	0.2076
2	2.1693	4.6483	7.1323	10.9302	7.2111	2.1031	1.2804	0.7437	0.4162
5	4.3323	7.9346	11.0396	16.4384	29.1548	5.7645	3.3015	1.8719	1.0415

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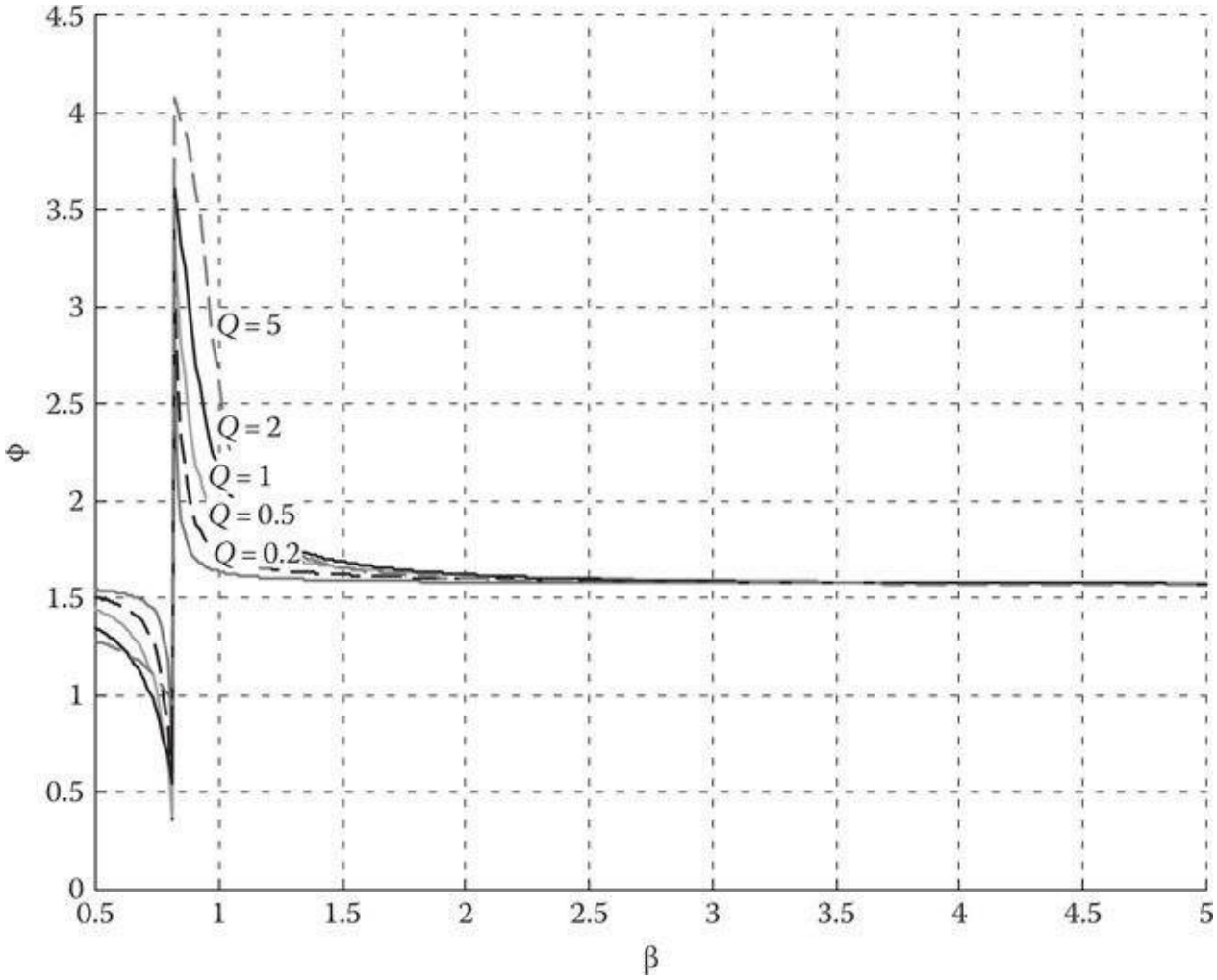


FIGURE 17.4
The curves of ϕ versus β referring to *Q*.

TABLE 17.2
ϕ versus β Referring to $p = 0.5$ and Various Q

	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
Q = 0.2	1.5442	1.4985	1.4008	2.2849	1.6374	1.5917	1.5839	1.5785	1.5749
0.5	1.5050	1.3965	1.1856	2.8022	1.7359	1.6209	1.6011	1.5869	1.5776
1	1.4445	1.2601	0.9755	3.1587	1.8925	1.6585	1.6184	1.5912	1.5769
2	1.3521	1.1276	0.8863	3.5185	2.1588	1.6879	1.6220	1.5873	1.5746
5	1.2827	1.1732	1.0760	4.0348	2.6012	1.6593	1.6011	1.5788	1.5724

where

$$|g| = \frac{1}{\sqrt{[1-(1+p)\beta^2/pQ]^2 + (1-\beta^2)^2}} \tag{17.21}$$

and

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$$\theta = -\tan^{-1}\frac{1-(1+p)\beta^2}{p(1-\beta^2)Q}$$

The characteristics of current transfer gain $|g|$ versus relevant frequency β referring to p = 0.5, 1, and 2 and various Q are shown in Figures 17.5, 17.6 and 17.7 and Tables 17.3, 17.4 and 17.5.

The characteristics of the phase angle θ versus relevant frequency β referring to p = 0.5 and various Q are shown in Figure 17.8 and Table 17.6.

For various β and Q, we have different current transfer gain. For example, when $\beta^2 = 1$ with any p, we have $g = -jQ = Q < 90°$. It means that the output current can be larger than the fundamental harmonic of the input current. The larger the value of Q, the higher the gain g.

Actually, set $\beta^2 = t$, we can find the maximum |g| from

$$\frac{d}{dt}|g| = 0$$

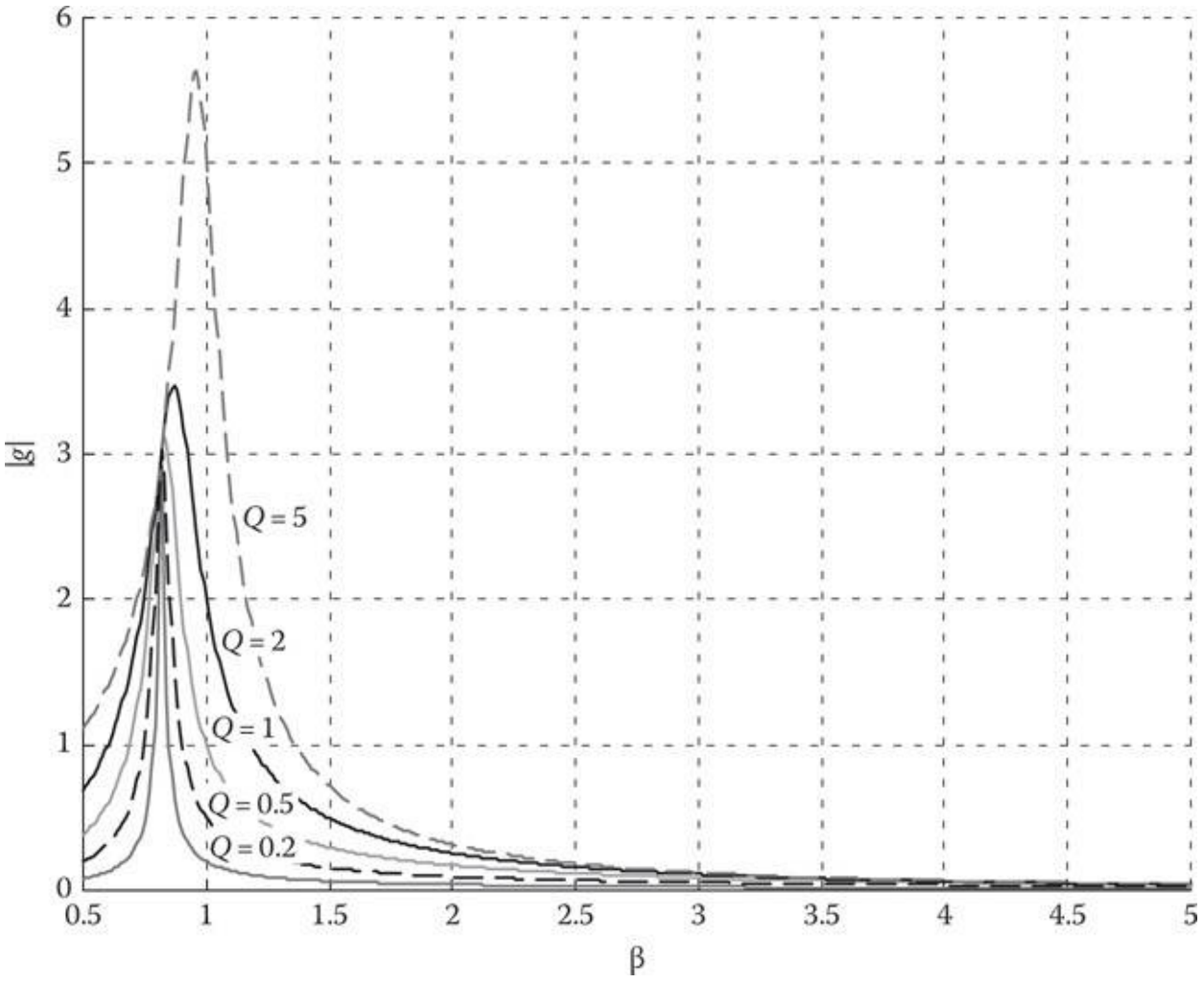


FIGURE 17.5
The curves of $|g|$ versus β referring to Q, p = 0.5.

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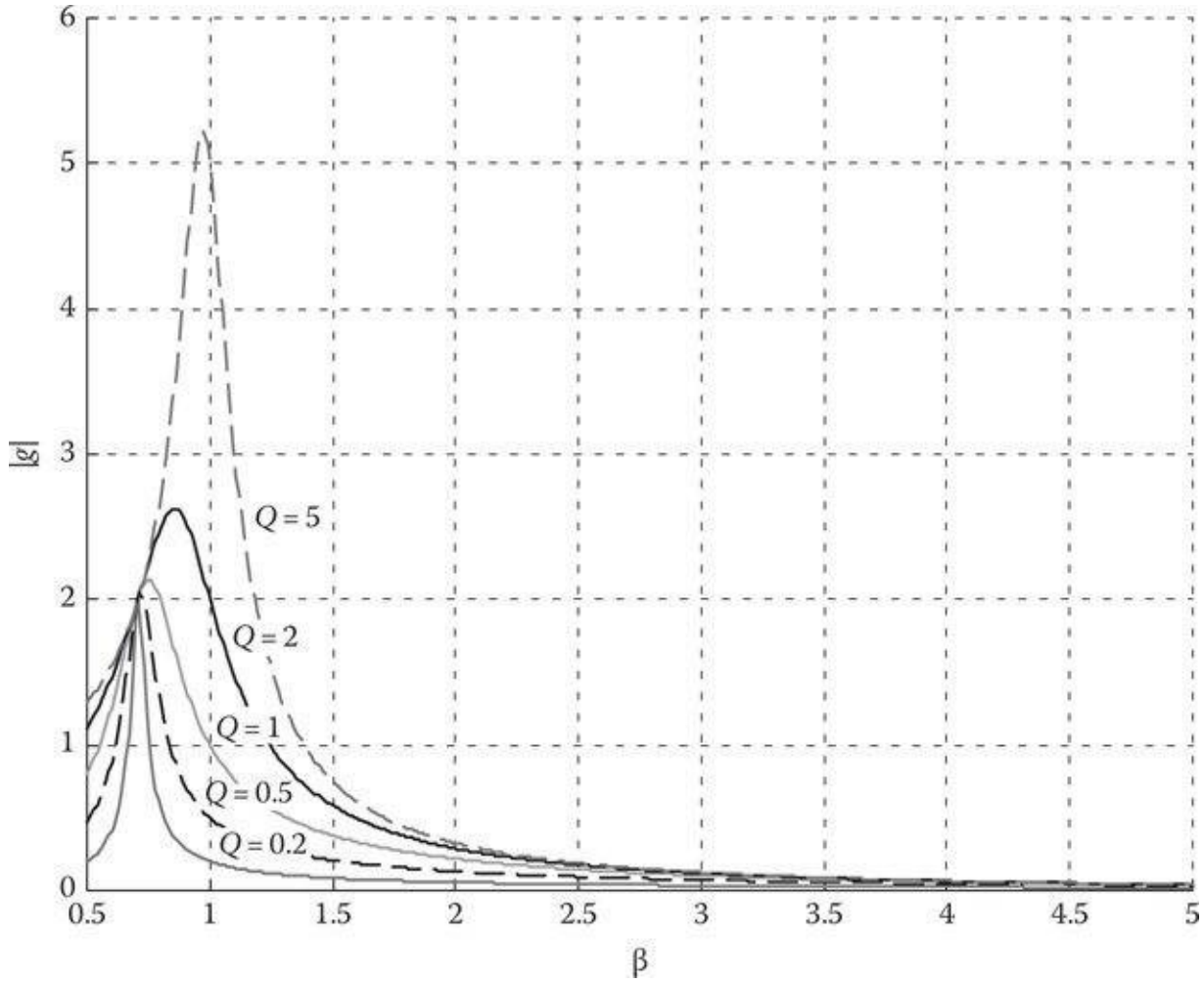


FIGURE 17.6
The curves of $|g|$ versus β referring to Q, $p = 1$.

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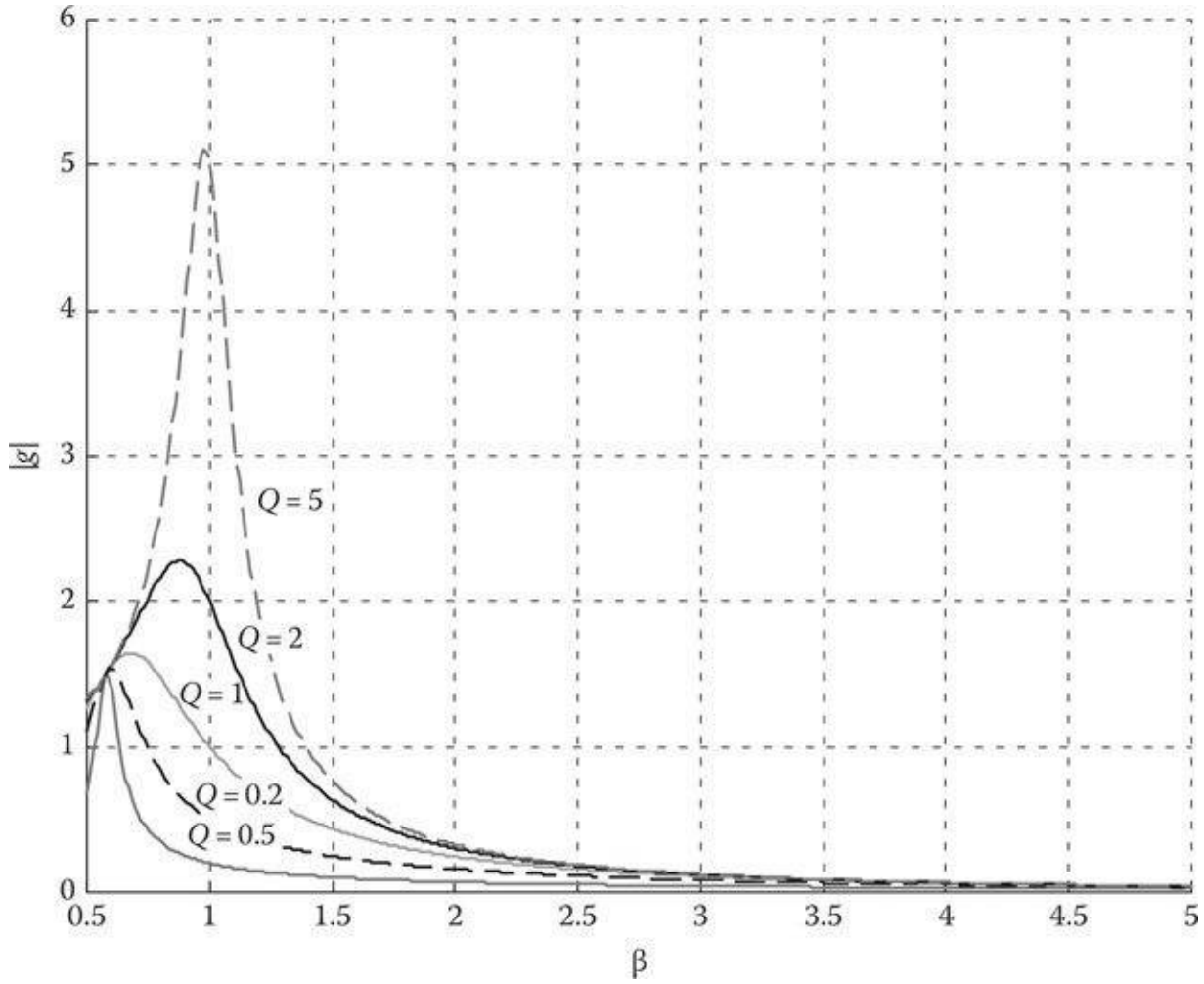


FIGURE 17.7
The curves of $|g|$ versus β referring to Q, $p = 2$.

TABLE 17.3
$|g|$ versus β Referring to $p = 0.5$ and Various Q

	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
Q = 0.2	0.0799	0.2169	0.5082	1.9679	0.2000	0.0630	0.0397	0.0236	0.0130
0.5	0.1978	0.5236	1.1361	2.8558	0.5000	0.1549	0.0958	0.0541	0.0265
1	0.3831	0.9404	1.7346	3.1122	1.0000	0.2937	0.1715	0.0866	0.0356
2	0.6860	1.4119	2.1236	3.1879	2.0000	0.4957	0.2561	0.1109	0.0399
5	1.1094	1.7528	2.2895	3.2101	5.0000	0.7136	0.3162	0.1224	0.0414

TABLE 17.4
$|g|$ versus β Referring to $p = 1$ and Various Q

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	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.1978	1.2446	0.9782	0.4353	0.2000	0.0852	0.0563	0.0340	0.0183
0.5	0.4682	1.6939	1.7609	1.0394	0.5000	0.2070	0.1313	0.0721	0.0323
1	0.8000	1.8075	2.1355	1.8138	1.0000	0.3778	0.2169	0.1020	0.0386
2	1.1094	1.8397	2.2734	2.5943	2.0000	0.5848	0.2879	0.1178	0.0408
5	1.2883	1.8490	2.3171	3.0850	5.0000	0.7495	0.3246	0.1238	0.0415

TABLE 17.5
$|g|$ versus β Referring to $p = 2$ and Various Q

	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
$Q = 0.2$	0.6860	0.6673	0.4184	0.3098	0.2000	0.1035	0.0711	0.0433	0.0227
0.5	1.1094	1.2862	0.9670	0.7563	0.5000	0.2480	0.1596	0.0848	0.0355
1	1.2649	1.6438	1.5694	1.4007	1.0000	0.4370	0.2457	0.1099	0.0398
2	1.3152	1.7918	2.0406	2.2360	2.0000	0.6349	0.3030	0.1207	0.0412
5	1.3304	1.8409	2.2720	2.9709	5.0000	0.7648	0.3279	0.1243	0.0416

or

$$\frac{1-(i+p)t}{pQ}(1+p)+(1-t)=0 \tag{17.22}$$

We obtain

$$t=\frac{1+p+pQ}{1+2p+p^2+pQ}=\frac{1}{1+[(p+p^2)/(1+p+pQ)]}$$

If taking $Q = 1$, $t = \beta^2 = 0.6$, or $\beta = 0.7746$, $|g| = 2.236$.

If this inverter is working at the conditions $\beta = 1$ and $Q \gg 1$,

$$Z=\frac{jQ}{-1+[j(1/Q)]}R_{eq}\doteq -jQR_{eq}$$
$$\phi=\frac{\pi}{2}-\tan^{-1}\frac{1}{-Q}\doteq\frac{\pi}{2}-\pi=-\frac{\pi}{2} \tag{17.23}$$

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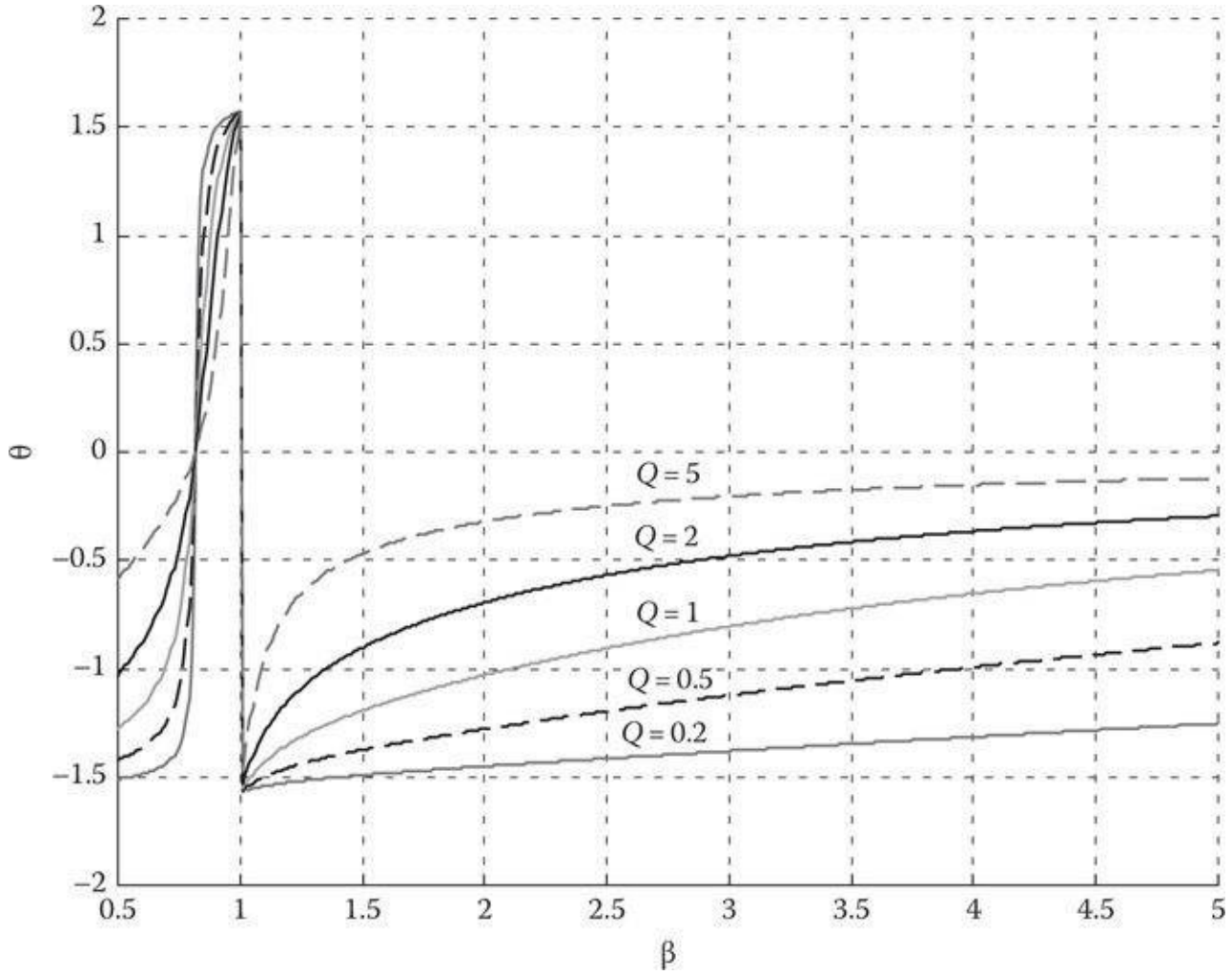


FIGURE 17.8
The curves of θ versus β referring to Q.

TABLE 17.6
θ versus β Referring to $p = 0.5$ and Various Q

	β = 0.5	0.678	0.755	0.83	1.0	1.5	2.0	3.0	5.0
Q = 0.2	−1.5109	−1.4533	−1.3505	0.9120	1.5708	−1.4920	−1.4514	−1.3811	−1.2532
0.5	−1.4219	−1.2840	−1.0604	0.4769	1.5708	−1.3759	−1.2793	−1.1233	−0.8828
1	−1.2793	−1.0378	−0.7290	0.2528	1.5708	−1.1948	−1.0304	−0.8058	−0.5465
2	−1.0304	−0.7030	−0.4200	0.1284	1.5708	−0.9025	−0.6947	−0.4802	−0.2953
5	−0.5880	−0.3268	−0.1768	0.0516	1.5708	−0.4690	−0.3218	−0.2054	−0.1211

Correspondingly,

$$g = \frac{1}{-jp/pQ} \doteq jQ$$

$$\theta = -\pi/2 \tag{17.24}$$

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The Π-CLL circuit is not only the resonant circuit but also the band-pass filter. All higher-order harmonic components in the input current are effectively filtered by the Π-CLL circuit. The output current is nearly a pure sinusoidal waveform with the fundamental frequency $\omega = 2\pi f$

17.2.4 Power Transfer Efficiency

The power transfer efficiency is a very important parameter and is calculated here. From Figure 17.5, we know the input current $i_i(\omega t)$ is

$$i_i(\omega t) = \begin{cases} +I_i & 2n\pi \le \omega t \le (2n+1)\pi \\ -I_i & (2n+1)\pi \le \omega t \le 2(n+1)\pi \end{cases} \quad \text{with } n = 0,1,2,3,\ldots,\infty \tag{17.25}$$

where $I_i = V_1/(Z + j\omega L_{10})$ that varies with different frequency.

This is a square waveform pulse train. Using *fast Fourier transform* (FFT), we have the spectrum form as

$$i_i(\omega t) = \frac{2I_i}{\pi}\sum_{n=1}^{\infty}\frac{\sin(2n+1)\omega t}{2n+1} \tag{17.26}$$

The fundamental frequency component is

$$i_{fund}(\omega t) = \frac{2I_i}{\pi}\sin\omega t \tag{17.27}$$

Output current is

$$i_2(\omega t) = g\frac{2I_i}{\pi}\sin\omega t \tag{17.28}$$

Because of the assumptions, no power losses were considered. The power transfer efficiency from DC source to AC output is calculated in the following equations. The total input power is

$$P_{in} = I_i^2 * real(Z) \tag{17.29}$$

The AC output power is gathered in the fundamental component that is

$$P_{fund} = \left(|g|\frac{2I_i}{\pi\sqrt{2}}\right)^2 R_{eq} \tag{17.30}$$

The power transfer efficiency is

$$\eta = \frac{P_{fund}}{P_{in}} = \frac{[2(I_i|g|)^2/\pi^2]R_{eq}}{I_i^2 * real(Z)} = \frac{2|g|^2}{\pi^2}\cos\phi \tag{17.31}$$

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17.3 Simulation Results

To verify the design and calculation results, PSpice simulation package was applied for these circuits. Choosing V_i = 30 V, all pump inductors L_i = 10 mH, the resonant capacitor C = 0.2 μF, and inductors $L_1 = L_2$ = 70 μH, load R = 10 Ω, k = 0.5, and f = 35 kHz. The input and output current waveforms are shown in Figure 17.9a. Their corresponding FFT spectrums are shown in Figure 17.9b. It is obviously illustrated that the output waveform is nearly a sinusoidal function, and its corresponding THD is nearly unity.

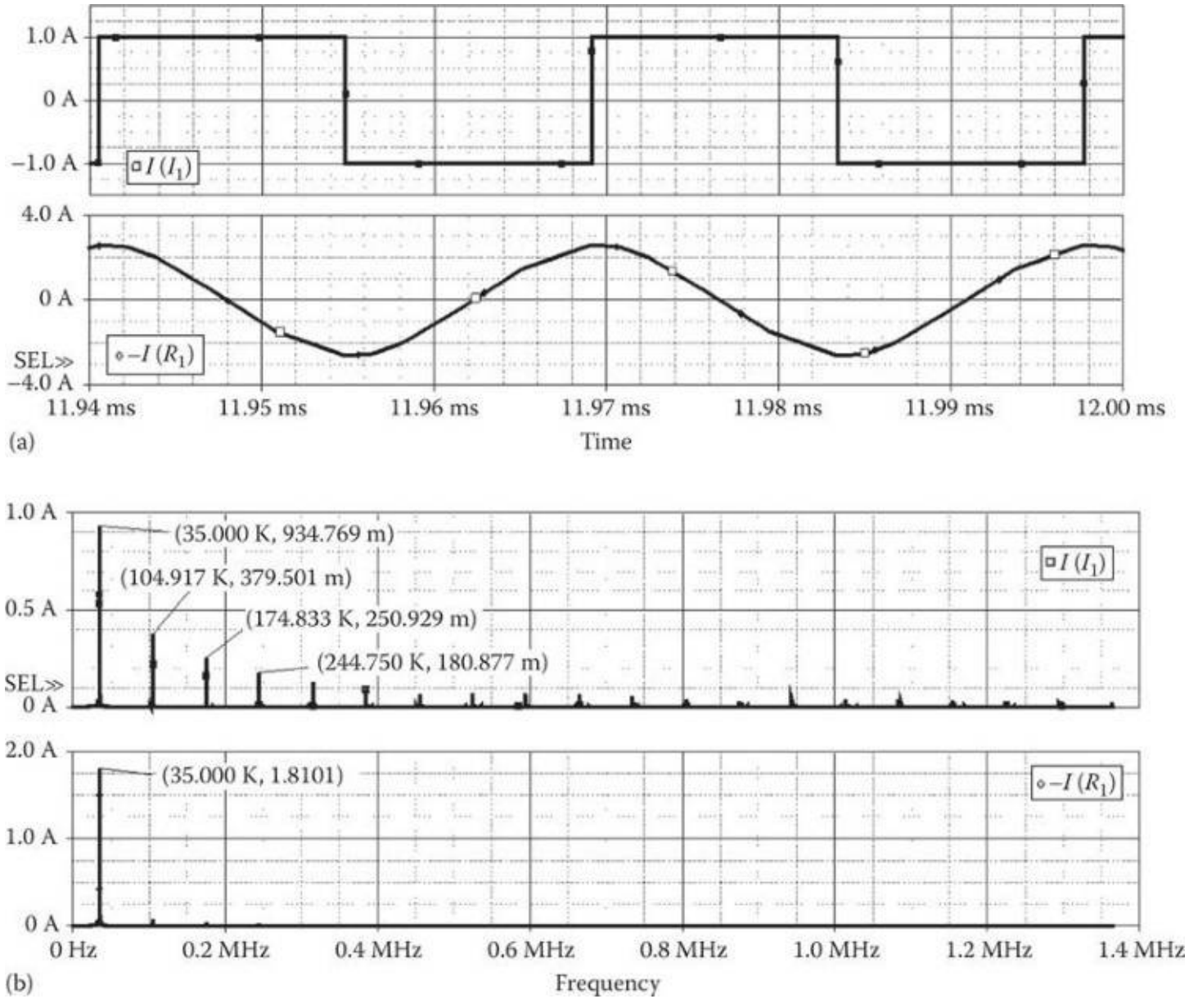


FIGURE 17.9
Input and output current waveforms of Π-CLL circuit at f = 35 kHz. (a) Input and output current waveforms of Π-CLL current source resonant inverter. (b) Corresponding FFI.

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17.4 Discussion

17.4.1 Function of the Π-CLL Circuit

As a Π-CLC filter, it is a typical low-pass filter. All harmonics with frequency $\omega > \omega_0$ will be blocked. Π-CLL filter circuit has thoroughly different characteristics from that of low-pass filters. It allows the signal with higher frequency $\omega > \omega_0$ (it means $\beta > 1$ in Section 17.2), passing it and enlarging the energy.

17.4.2 Applying Frequency to This Π-CLL CSRI

From our analysis and verifications, we found the fact that the effective applying frequency to this Π-CLL CSRI is $(0.8 – 2.0)f_0$. Outside this region, both current transfer gain and efficiency are falling fast.

17.4.3 Explanation of $g > 1$

We recognized the fact that current transfer gain is greater than unity from mathematical analysis and simulation and experimental results. The reason to enlarge the fundamental current is that the resonant circuit transfers the energy of other higher-order harmonics to the fundamental component. Therefore, the gain of the fundamental current can be greater than unity.

17.4.4 DC Current Component Remaining

Since the Π-CLL resonant circuit could not block the DC component, the output current still remains the same DC current component. This is not useful for most ordinary inverter applications.

17.4.5 Efficiency

From mathematical calculation and analysis and simulation and experimental results, we can obtain very high efficiency. Its maximum value can be nearly unity. It means this Π-CLL resonant circuit can transfer the energy from not only higher-order harmonics but also a DC component into the fundamental component.

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Cascade Double Γ-CL Current Source Resonant Inverter

18.1 Introduction

This chapter introduces a four-element current source resonant inverter (CSRI): a cascade double Γ-CL circuit CSRI. Its circuit diagram is shown in Figure 18.1. It consists of four energy-storage elements, the double Γ-CL: C_1−L_1 and C_2ΓL_2. The energy source is a DC voltage V_{in} chopped by two main switches S_1 and S_2 to construct a bipolar current source, i_i = ±I_i The pump inductors L_{10} and L_{20} are equal to each other and are large enough to keep the source current nearly constant during operation. The real load absorbs the delivered energy; its equivalent load should be proposed resistive, R_{eq}. The equivalent circuit diagram is shown in Figure 18.2.

18.2 Mathematical Analysis

In order to concentrate the function analysis of this cascade double Γ-CL CSRI, assume the following:

1. The inverter's source is a constant current source determined by the pump circuits.
2. Two metal–oxide–semiconductor field-effect transistors (MOSFETs) in the switching circuit are turned on and turned off 180° out of phase with each other at the same switching frequency and with a duty cycle of 50%.
3. Two switches are ideal components without switch-on resistance and negligible parasitic capacitance and zero switching time.
4. Two diodes are components having a zero forward voltage drop and forward resistance.
5. Four energy-storage elements are passive, linear, and time invariant and do not have parasitic reactive components.

Based on these assumptions and the equivalent circuit, the following analysis is derived.

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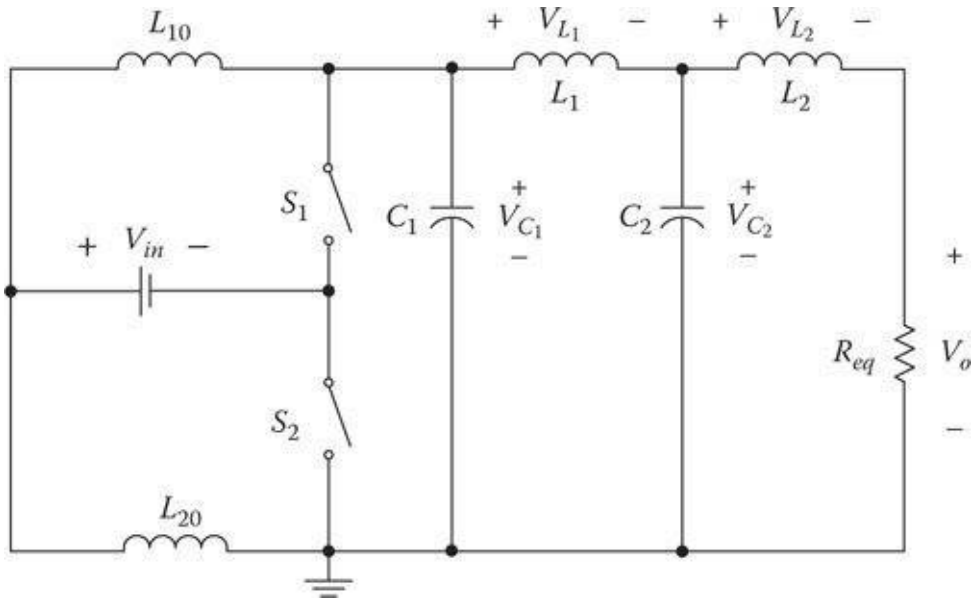


FIGURE 18.1
Cascade double Γ-CL current source resonant inverter.

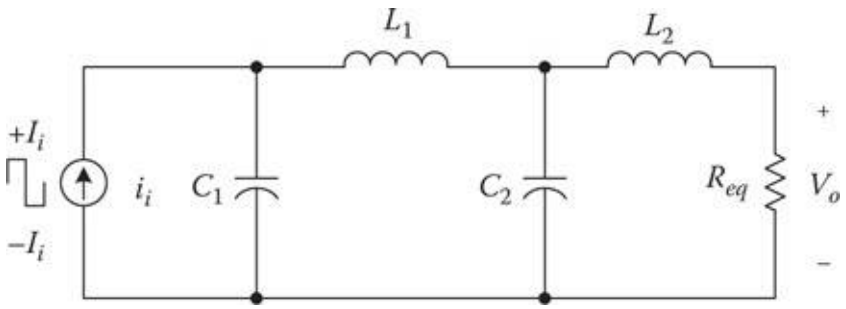


FIGURE 18.2
Equivalent circuit.

18.2.1 Input Impedance

This CSRI is a fourth-order system. The mathematical analysis of operation and stability is more complex than three-energy-storage-element CSRIs. The input impedance is given by

$$Z(\omega) = \frac{R_{eq}(1-\omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{1-\omega^2(L_1C_1 + L_2C_1 + L_2C_2) + \omega^4 L_1 L_2 C_1 C_2 + j\omega R_{eq}(C_1 + C_2 - \omega^2 L_1 C_1 C_2)} \tag{18.1}$$

or

$$Z(\omega) = \frac{R_{eq}(1-\omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{B(\omega)} \tag{18.2}$$

where

$$B(\omega) = 1-\omega^2(L_1C_1 + L_2C_1 + L_2C_2) + \omega^4 L_1 L_2 C_1 C_2 + j\omega R_{eq}(C_1 + C_2 - \omega^2 L_1 C_1 C_2) \tag{18.3}$$

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18.2.2 Components' Voltages and Currents

This CSRI has four resonant components C_1, C_2, L_1, and L_2, plus the output equivalent resistance R_{eq}. In order to compare with the parameters easily, all components' voltages and currents are responded to the input fundamental current I_i.

The voltage and current on capacitor C_1 is

$$\frac{V_{C_1}(\omega)}{I_i(\omega)} = \frac{R_{eq}(1-\omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{B(\omega)} \tag{18.4}$$

$$\frac{I_{C_1}(\omega)}{I_i(\omega)} = \frac{R_{eq}(1-\omega^2 L_1 C_2) + j\omega(L_1 + L_2 - \omega^2 L_1 L_2 C_2)}{B(\omega)/j\omega C_1} \tag{18.5}$$

The voltage and current on inductor L_1 is

$$\frac{V_{L_1}(\omega)}{I_i(\omega)} = \frac{-R_{eq}\omega^2 L_1 C_2 + j\omega L_1(1-\omega^2 L_2 C_2)}{B(\omega)} \tag{18.6}$$

$$\frac{I_{L_1}(\omega)}{I_i(\omega)} = \frac{(1-\omega^2 L_2 C_2) + jR_{eq}\omega C_2}{B(\omega)} \tag{18.7}$$

The voltage and current on capacitor C_2 is

$$\frac{V_{C_2}(\omega)}{I_i(\omega)} = \frac{R_{eq} + j\omega L_2}{B(\omega)} \tag{18.8}$$

$$\frac{I_{C_2}(\omega)}{I_i(\omega)} = \frac{-\omega^2 L_2 C_2 + jR_{eq}\omega C_2}{B(\omega)} \tag{18.9}$$

The voltage and current on inductor L_2 is

$$\frac{V_{L_2}(\omega)}{I_i(\omega)} = \frac{j\omega L_2}{B(\omega)} \tag{18.10}$$

$$\frac{I_{L_2}(\omega)}{I_i(\omega)} = \frac{1}{B(\omega)} \tag{18.11}$$

The output voltage and current on the resistor R_{eq} is

$$\frac{V_o(\omega)}{I_i(\omega)} = \frac{R_{eq}}{B(\omega)} \tag{18.12}$$

The current transfer gain is given by

$$g(\omega) = \frac{I_o(\omega)}{I_i(\omega)} = \frac{1}{B(\omega)} \tag{18.13}$$

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18.2.3 Simplified Impedance and Current Gain

Usually, the input impedance and output current gain are paid more attention rather than other transfer functions listed in the previous section. To simplify the operation, select

$$L_1 = L_2 = L; \quad C_1 = C_2 = C; \quad \omega_0 = \frac{1}{\sqrt{LC}}$$

$$Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}}; \quad \beta = \frac{\omega}{\omega_0}$$

Obtain

$$B(\beta) = 1 - 3\beta^2 + \beta^4 + j\frac{2-\beta^2}{Q}\beta \tag{18.14}$$

Therefore,

$$Z = \frac{(1-\beta^2) + jQ(2-\beta^2)}{1-3\beta^2+\beta^4 + j((2-\beta^2)/Q)\beta} R_{eq} = |Z| \angle \phi \tag{18.15}$$

where

$$|Z| = \frac{\sqrt{(1-\beta^2)^2 + Q^2(2-\beta^2)^2}}{\sqrt{(1-3\beta^2+\beta^4)^2 + \beta^2((2-\beta^2)/Q)^2}} R_{eq}$$

and

$$\phi = \tan^{-1}\frac{2-\beta^2}{1-\beta^2}Q - \tan^{-1}\frac{(2-\beta^2)\beta}{(1-3\beta^2+\beta^4)Q}$$

The characteristics of input impedance $|Z|/R_{eq}$ versus relevant frequency β referring to various Q are shown in Figure 18.3 and Table 18.1.

The characteristics of phase angle ϕ versus relevant frequency β referring to various Q are shown in Figure 18.4 and Table 18.2.

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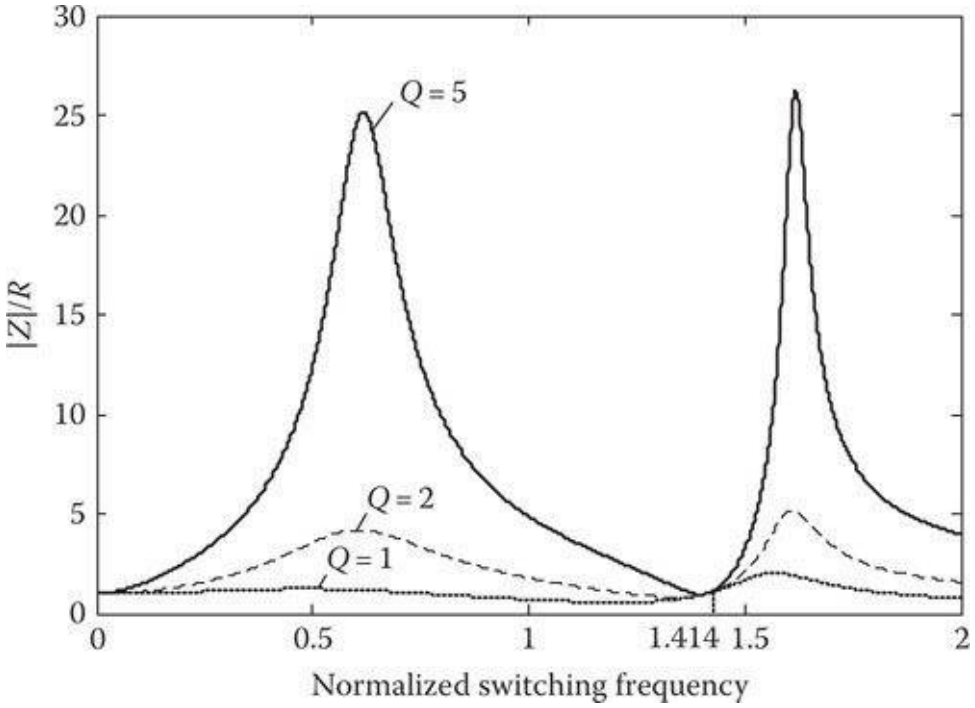


FIGURE 18.3
The curves of $|Z|/R_{eq}$ versus β referring to Q.

TABLE 18.1
$|Z|/R_{eq}$ versus β Referring to Various Q

	β = 0.59	1	1.2	1.414	1.59
$Q = 1$	1.1994	0.7071	0.5672	1.0000	2.0237
2	4.1662	1.7889	1.0955	1.0000	4.9137
5	23.464	4.9029	2.7031	1.0000	17.463

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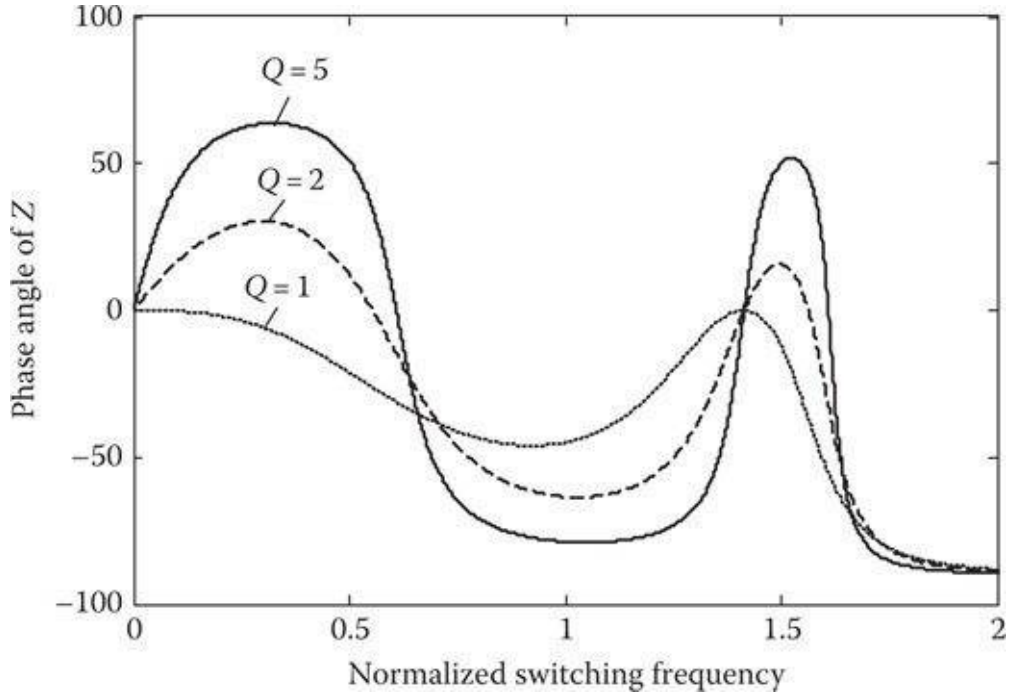


FIGURE 18.4
The curves of ϕ versus β referring to *Q*.

TABLE 18.2
ϕ versus β Referring to Various *Q*

	β = 0.59	1	1.2	1.414	1.59
Q = 1	−29.3	−45.0	−28.5	0.0	−48.3
2	−9.5	−63.4	−56.8	0.0	−17.6
5	13.9	−78.7	−76.4	0.0	29.0

The current transfer gain becomes

$$g = \frac{1}{1-3\beta^2+\beta^4+j((2-\beta^2)/Q)\beta} = |g|\underline{\theta} \tag{18.16}$$

where

$$|g| = \frac{1}{\sqrt{(1-3\beta^2+\beta^4)^2+\beta^2((2-\beta^2)/Q)^2}} \tag{18.17}$$

and

$$\theta = -\tan^{-1}\frac{(2-\beta^2)\beta}{(1-3\beta^2+\beta^4)Q}$$

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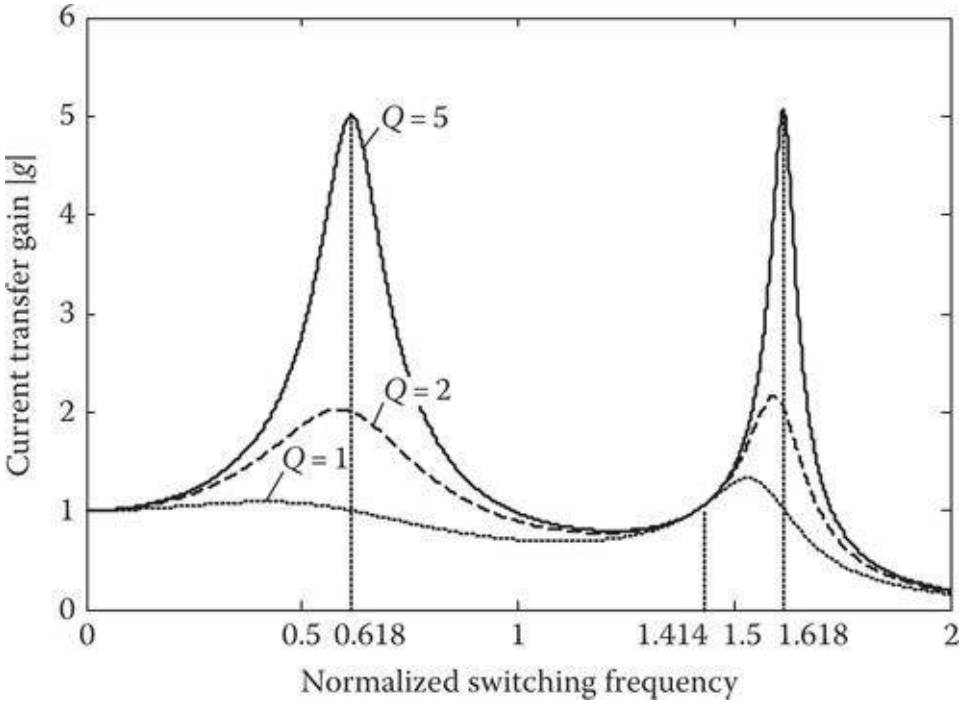


FIGURE 18.5
The curves of $|g|$ versus β referring to Q.

TABLE 18.3
$|g|$versus β Referring to Various Q

	β = 0.59	1	1.2	1.414	1.59
$Q = 1$	1.0229	0.7071	0.7062	0.9994	1.1607
2	2.0270	0.8944	0.7747	0.9994	2.1641
5	4.7725	0.9806	0.7977	0.9994	3.9087

The characteristics of current transfer gain $|g|$ versus relevant frequency β referring to various Q are shown in Figure 18.5 and Table 18.3.

The characteristics of the phase angle θ versus relevant frequency β referring to various Q are shown in Figure 18.6 and Table 18.4.

For various β and Q, a different current transfer gain is obtained. Actually, the maximum $|g|$ can be found from

$$\frac{d}{d\beta^2}|g| = 0$$

or

$$4\beta^6 + \left(\frac{3}{Q^2} - 18\right)\beta^4 + \left(22 - \frac{8}{Q^2}\right)\beta^2 + \left(\frac{4}{Q^2} - 6\right) = 0 \tag{18.18}$$

When $Q = 2$,

$$4\beta^6 - 17.25\beta^4 + 20\beta^2 - 5 = 0 \tag{18.19}$$

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yields $\beta_1 = 0.59$, $\beta_2 = 1.20$, $\beta_3 = 1.59$.

Take $\beta_3 = 1.59$ (the local maximum transfer gain is achieved at $\beta_1 = 0.59$), and the corresponding $|g(\beta)|$ is equal to 2.165.

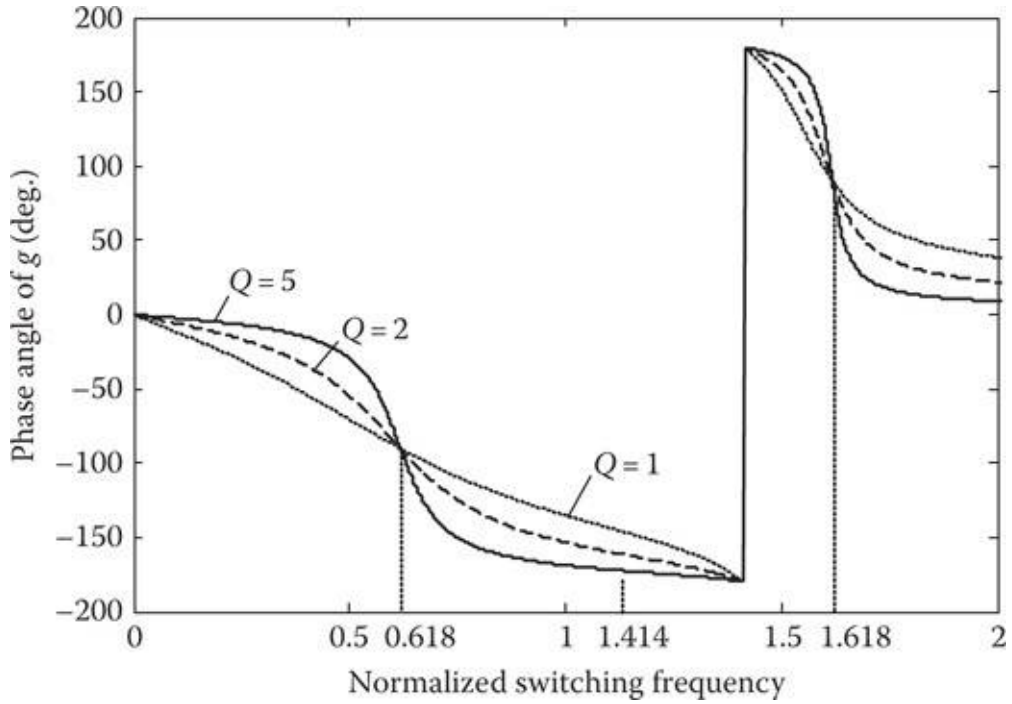


FIGURE 18.6
The curves of θ versus β referring to Q.

TABLE 18.4
θ versus β Referring to Various *Q*

	β = 0.59	1	1.2	1.414	1.59
Q = 0.5	−87.7	−116.6	−132.8	−180.0	96.6
1	−85.5	−135.0	−151.7	−180.0	102.9
2	−81.0	−153.4	−164.9	−180.0	114.7

In practice, Equation 18.19 is dependent on the quality factor *Q*. For various load conditions, the maximum transfer gain will be achieved at different operating frequencies.

When $Q \gg 1$, we have

$$2\beta^6 - 9\beta^4 + 11\beta^2 - 3 = 0 \tag{18.20}$$

or

$$(2\beta^2 - 3)(1 - 3\beta^2 + \beta^4) = 0$$

yields three positive real roots as

$$\beta_4 = 0.618,\ \beta_5 = 1.618,\ \beta_6 = 1.225$$

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It should be noted that two peaks exist in the transfer gain curves with corresponding frequencies at $\beta_4 = 0.618$ and $\beta_5 = 1.618$, respectively. The current transfer gain drops from the peak to the vale at $\beta_6 = 1.225$.

Taking further investigation, it is found that at the frequencies corresponding to peak gain, the following equation can be obtained:

$$1-3\beta^2+\beta^4=0 \tag{18.21}$$

Thus, the current transfer gain at β_4 and β_5 is

$$|g(\beta)| = \left.\frac{1}{\sqrt{(1-3\beta^2+\beta^4)^2+\left(\frac{2-\beta^2}{Q}\right)^2\beta^2}}\right|_{\beta_4,\beta_5} = Q \tag{18.22}$$

The relevant phase angle θ is

$$\theta_4 = -90^\circ \; \theta_5 = 90^\circ$$

The results indicate that the current transfer gain is proportional to the quality factor *Q*. The larger the value of Q, the higher the gain |g(β)|. For instance, when *Q* = 1, 2, and 5 with $\beta_4 = 0.618$ or $\beta_5 = 1.618$, |g(β)| will have the same value. Note that although β_4 and β_5 are derived from the assumption of $Q \gg 1$, Equation 18.22 is still valid for all the values of quality factors.

Furthermore, when $Q \ll 1$, Equation 18.18 can be rearranged as

$$3\beta^4-8\beta^2+4=0 \tag{18.23}$$

giving other two positive real roots as

$$\beta_7 = 0.816, \beta_8 = 1.414$$

As can be seen from Figure 18.5, the minimum transfer gain is achieved at β_7, while the maximum gain is obtained at β_8. These characteristic points will be useful in the estimation of the transfer gain curves. Note that for low *Q* values, the frequency characteristics of cascade double Γ-CL CSRI approach to those of conventional series-loaded resonant inverters, especially when β is near to 1.414.

When $\beta=\beta_c=1.414(\beta^2_c=2)$, all the curves will intersect at one point where the corresponding current transfer gain is

$$|g(\beta_c)| = \frac{1}{\sqrt{\left(1-3\beta_c^2+\beta_c^4\right)^2+\left(\frac{2-\beta_c^2}{Q}\right)^2\beta_c^2}} \equiv 1 \tag{18.24}$$

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This point is always called load-independent point since the current transfer gain keeps constant with any value of quality factor Q.

If the inverter is working at the conditions

$$\beta = 1 \quad \text{and} \quad Q \gg 1$$

we then have

$$Z = \frac{jQ}{-1 + j/Q} R_{eq} \approx -jQR_{eq}$$
$$\varphi = \frac{\pi}{2} - \tan^{-1}\frac{1}{-Q} \approx \frac{\pi}{2} - \pi \approx -\frac{\pi}{2} \tag{18.25}$$

and correspondingly

$$g(\beta) = \frac{1}{-1 + j/Q} = -1$$
$$\theta = -\pi \tag{18.26}$$

The double Γ-CL circuit is not only the resonant circuit but the band-pass filter as well. All higher-order harmonic components in the input current are effectively filtered by the double Γ-CL circuit. The output current is nearly a pure sinusoidal waveform with the fundamental frequency $\omega = 2\pi f$

18.2.4 Power Transfer Efficiency

The power transfer efficiency is a very important parameter and it is calculated here. From Figure 18.2, the input current is a bipolar value $i_i(\omega t)$:

$$i_i(\omega t) = \begin{cases} I_i & 2n\pi \le \omega t \le (2n+1)\pi \\ -I_i & (2n+1)\pi \le \omega t \le 2(n+1)\pi \end{cases} \quad \text{with } n = 0,1,2,3,\ldots,\infty \tag{18.27}$$

where

$$I_i = \frac{V_1}{(Z + j\omega L_{10})} \quad (L_{10} = L_{20})$$

that varies with operating frequency.

This is a square waveform pulse train. Applying fast Fourier transform (FFT), the spectrum form is

$$i_i(\omega t) = \frac{4I_i}{\pi} \sum_{n=0}^{\infty} \frac{\sin(2n+1)\omega t}{2n+1} \tag{18.28}$$

The fundamental frequency component is

$$i_{fund}(\omega t) = \frac{4I_i}{\pi} \sin \omega t \tag{18.29}$$

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The output current is

$$i_0(\omega t) = g\frac{4I_i}{\pi}\sin\omega t \tag{18.30}$$

The power transfer efficiency from input current source to AC output load is analyzed and calculated. Since the input current is a square waveform, the total input power is

$$P_{in} = I_i^2 |Z| \tag{18.31}$$

The output current is nearly a pure sinusoidal waveform; its root-mean-square value is its peak value times 1/√2. Therefore, the output power is

$$P_o = \left(|g|\frac{4I_i}{\pi\sqrt{2}}\right)^2 R_{eq} = 8\left(|g|\frac{I_i}{\pi}\right)^2 R_{eq} \tag{18.32}$$

We can get the power transfer efficiency as follows:

$$\eta = \frac{P_o}{P_{in}} = \frac{8(I_i|g|)^2/\pi^2 R_{eq}}{I_i^2|Z|} = \frac{8|g|^2 R_{eq}}{\pi^2|Z|} \tag{18.33}$$

Considering Equations 18.15 and 18.17, we obtain

$$\eta = \frac{8}{\pi^2}\frac{1}{\sqrt{(1-\beta^2)^2+Q^2\beta^2(2-\beta^2)^2}\sqrt{(1-3\beta^2+\beta^4)^2+\beta^2((2-\beta^2)/Q)^2}} \tag{18.34}$$

If $\beta^2 = 2$ ($\beta = 1.414$) with any Q, $\eta = 0.8106$.
If $\beta^2 = 1$ ($\beta = 1$) and $Q = 1$, $\eta = 0.5732$.
If $\beta^2 = 2.5$ ($\beta = 1.581$) and $Q = 1$, $\eta = 0.5771$.
If $\beta^2 = 2.618$ ($\beta = 1.618$) and $Q = 1$, $\eta = 0.4263$.

Therefore, the characteristics of efficiency η versus relevant frequency β referring to various Q are obtained and shown in Figure 18.7 and Table 18.5.

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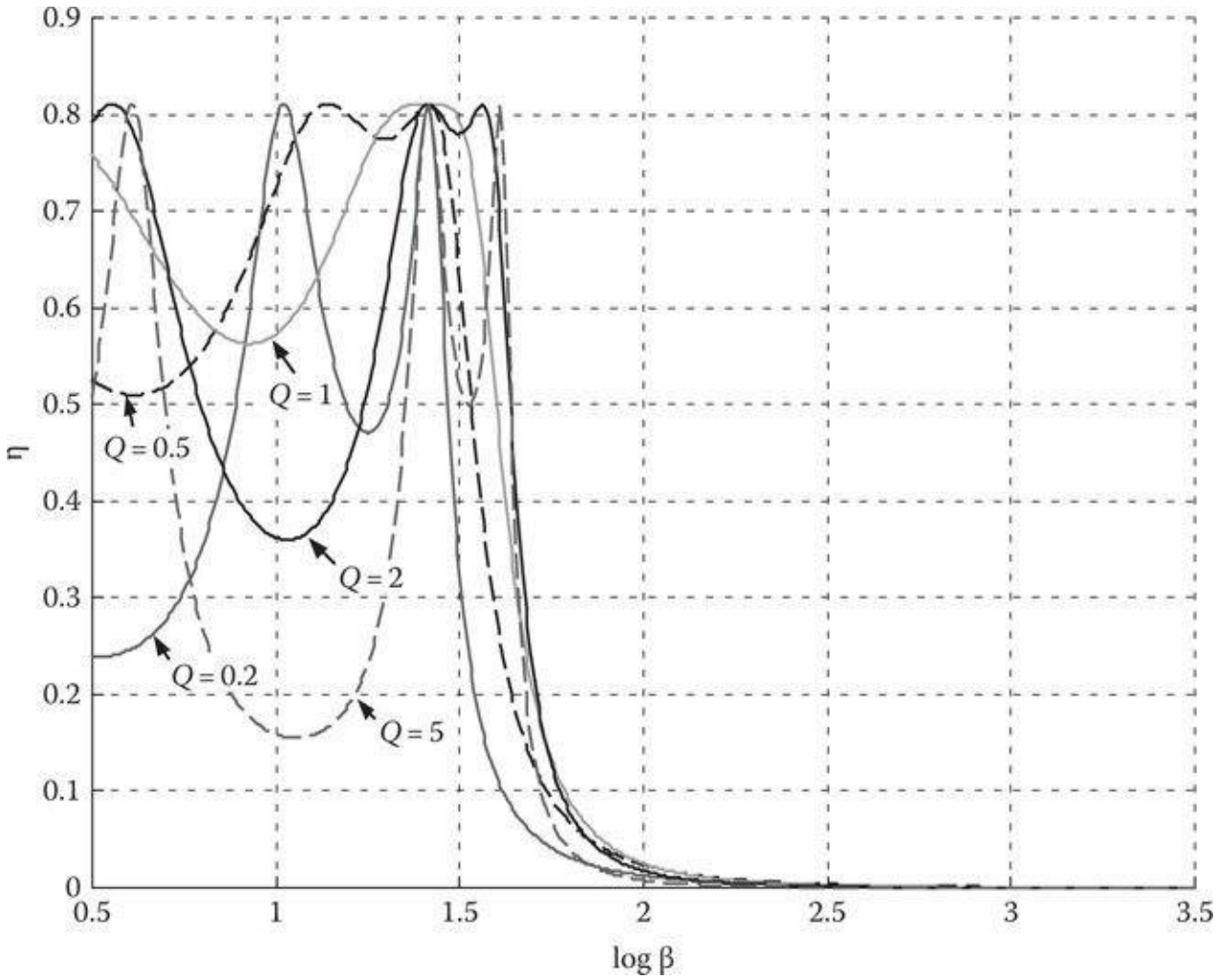


FIGURE 18.7
Curves of η versus β referring to *Q*.

TABLE 18.5
η versus β Referring to Various *Q*

	β = 0.618	0.8	1	1.414	1.581	1.618	2	3	4	5
Q = 0.2	0.2496	0.3527	0.7948	0.8106	0.1359	0.0995	0.0127	0.0008	0.0001	0.0000
0.5	0.5098	0.5559	0.7250	0.8106	0.3268	0.2394	0.0238	0.0009	0.0001	0.0000
1	0.6895	0.5885	0.5732	0.8106	0.5771	0.4263	0.0253	0.0006	0.0001	0.0000
2	0.7745	0.4927	0.3625	0.8106	0.7955	0.6304	0.0176	0.0003	0.0000	0.0000
5	0.8045	0.2680	0.1590	0.8106	0.6473	0.7715	0.0079	0.0001	0.0000	0.0000

18.3 Simulation Result

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In order to verify analysis and calculation, PSpice software simulation method is used to obtain a set of simulation waveforms as shown in Figures 18.8, 18.9 and 18.10 corresponding to $Q = 2$ and $\beta = 1$, 1.414, and 1.59. The parameter values are set as follows:

$$I = 1 \text{ A}, V_1 = 30 \text{ V}, L_{10} = L_{20} = 20 \text{ mH}, R_{eq} = 10 \ \Omega, C_1 = C_2 = C = 0.22 \ \mu\text{F}, \text{ and } L_1 = L_2 = L = 100 \ \mu\text{H}$$

Therefore, $\omega_0 = 213$ krad/s, $f_0 = 33.93$ kHz, and $Q = 2$. The particular frequencies for the figures are $f = 33.9$, 48.0, and 54.0 kHz. In order to pick the input current, a small resistance $R_0 = 0.001 \ \Omega$ is employed. The load in the simulation circuit is R rather than R_{eq}.

Figures 18.8, 18.9 and 18.10 have two parts a and b. Part a shows the input and output current waveforms, and part b shows the corresponding FFT spectrum. The first channel of Figures 18.8a, 18.9a and 18.10a is the input current that is a square waveform pulse train with the pulse-width $\omega t = \pi$. The second channel of Figures 18.8a, 18.9a and 18.10a is the output current flowing through resistance R_{eq}, which is a sine waveform. In Figures 18.8b, 18.9b and 18.10b, the first channel waveform of each figure is the corresponding input current's FFT spectrum; the second channel waveform of each figure is the corresponding output current's FFT spectrum. From the spectra, it can be clearly seen that there is only monofrequency existing in output currents.

The waveforms in Figures 18.11, 18.12 and 18.13 are the output voltages at $\beta = 1$, 1.414, and 1.59, respectively, which are corresponding to the input currents $i_i(\omega t)$. All the input currents $i_i(\omega t)$ are square waveform pulse train with the pulse-width $\omega t = \pi$. All output current waveforms are very pure sinusoidal function.

18.3.1 $\beta = 1$, $f = 33.9$ kHz, and $T = 29.5$ μs

The waveforms and corresponding FFT spectra are shown in Figure 18.8. The total harmonic distortion (THD) = 0 and current transfer gain is

$$g = \frac{I(R)}{I(R0)_1}\Big|_{f=33.9 \text{ kHz}} = \frac{1.145}{1.272} = 0.9002$$

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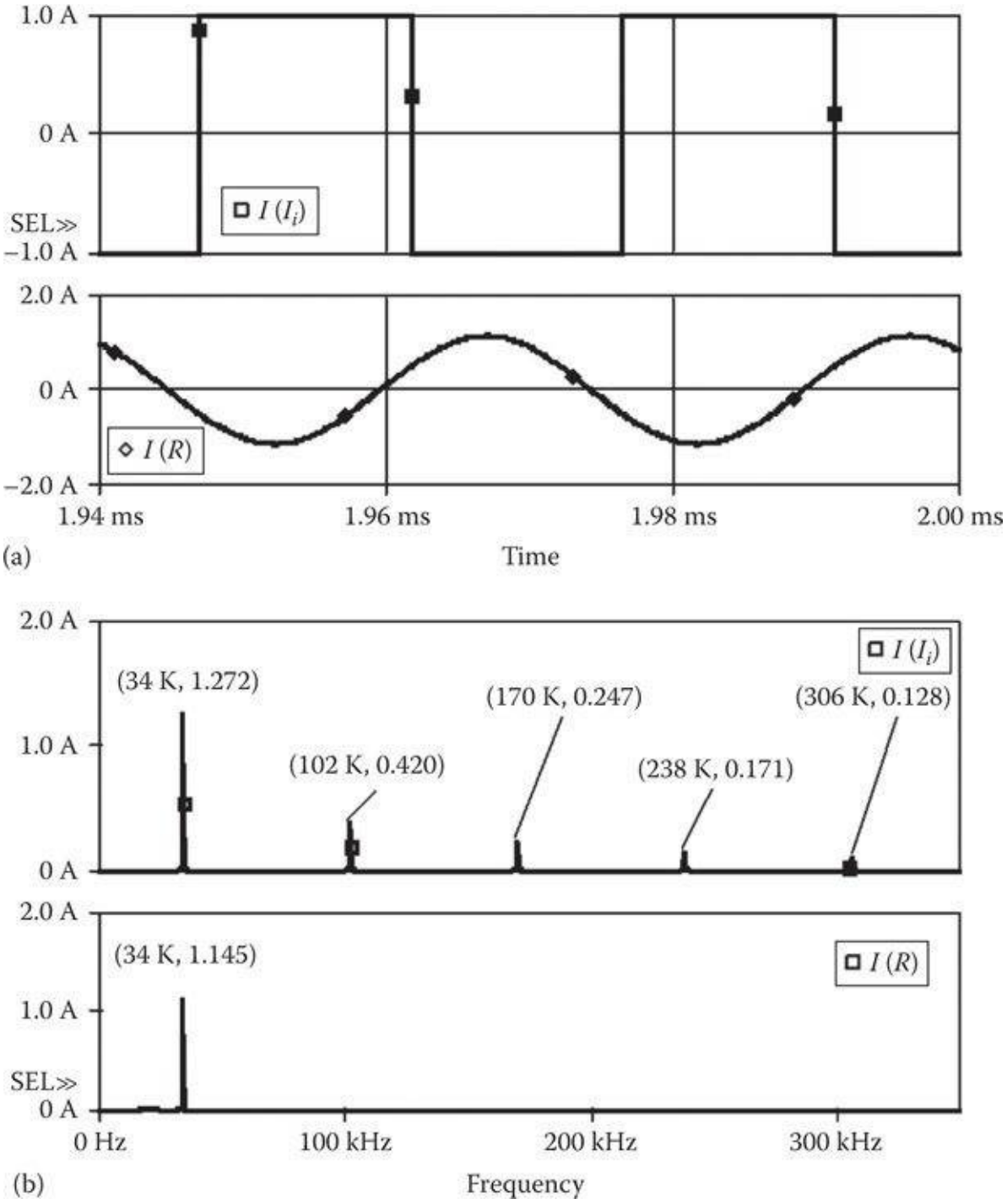


FIGURE 18.8
Input and output current waveforms at f = 33.9 kHz. (a) Input and output current waveforms. (b) The corresponding fast Fourier transform spectra of input and output current waveforms.

18.3.2 β = 1.4142, f = 48.0 kHz, and T = 20.83μs

The waveforms and corresponding FFT spectra are shown in Figure 18.9. The THD = 0 and current transfer gain is

$$g = \frac{I(R)}{I(R0)_1}\Big|_{f=48\text{ kHz}} = \frac{1.271}{1.271} = 1.00$$

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18.3.3 β = 1.59, f = 54 kHz, and T = 18.52 μs

The waveforms and corresponding FFT spectra are shown in Figure 18.10. The THD = 0 and current transfer gain is

$$g = \frac{I(R)}{I(R0)_1}\Big|_{f=54\text{ kHz}} = \frac{2.752}{1.273} = 2.162$$

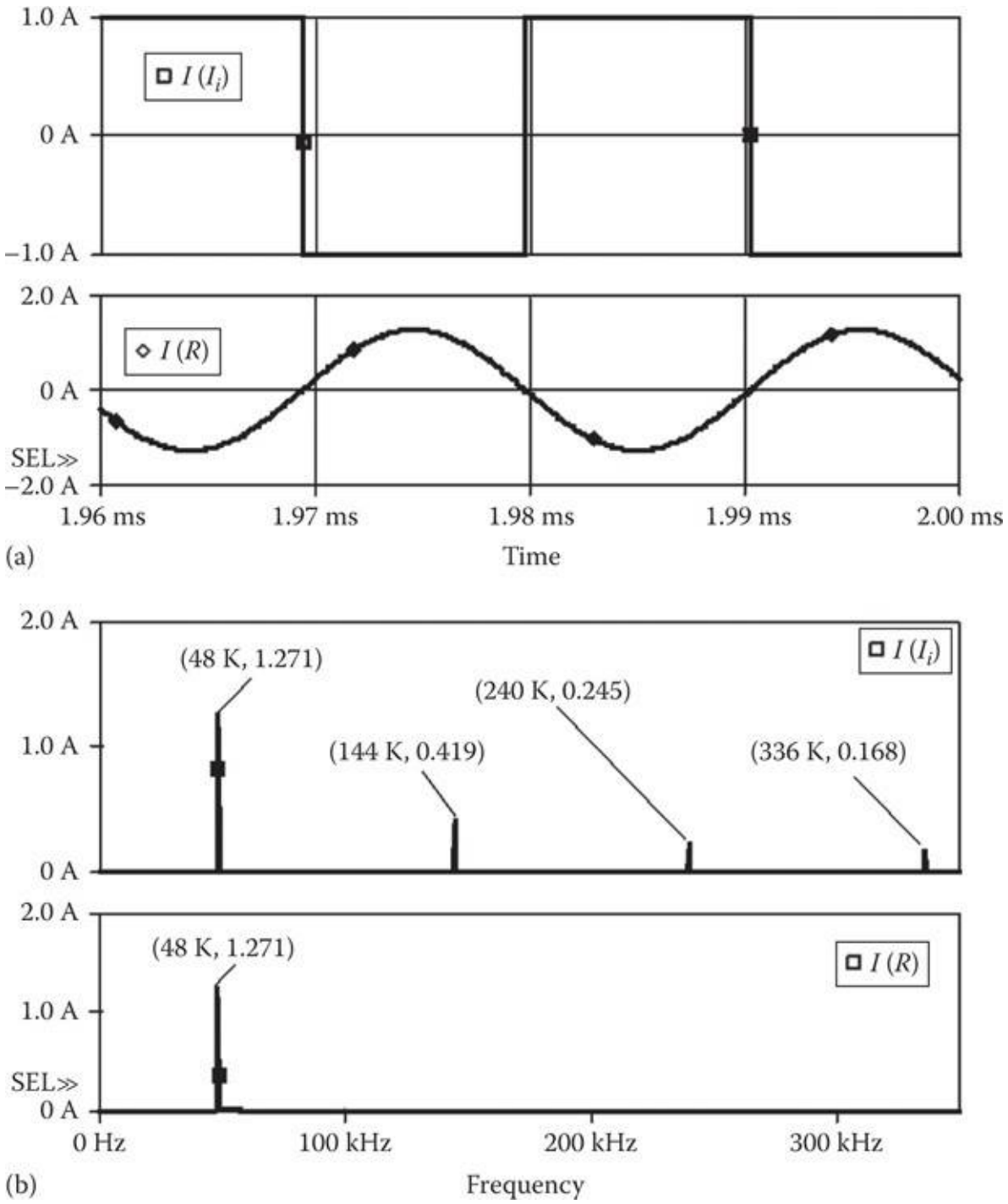


FIGURE 18.9
Input and output current waveforms at f = 48 kHz. (a) Input and output current waveforms. (b) The corresponding fast Fourier transform spectra of input and output current waveforms.

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18.4 Experimental Result

In order to verify our analysis and calculation, a test rig with the same components was constructed:

I = 1 A, V_1 = 30 V, $L_{10} = L_{20}$ = 20 mH, R_{eq} = 10 $\Omega_1 = C_2 = C$ = 0.22 μF, and $L_1 = L_2 = L$ = 100 μH

Therefore, ω_0 = 213 krad/s, f_0 = 33.93 kHz, and Q = 2. The MOSFET device is IRF640 (R_{ds} = 0.15 ohm, C_{ds} = 140 pF). Since the junction capacitance of C_{ds} is much smaller than the resonance capacitance C = 0.22 μF (C/C_{ds} = 1429), it does not affect the experimental results. The output current waveform is a perfect sine function. A set of tested output voltage waveforms that correspond to the output current with β = 1, 1.4142, and 1.59 is shown in Figures 18.11, 18.12 and 18.13. The particular applied frequencies for the figures are f = 33.9, 48.0, and 54.0 kHz and peak-to-peak voltage V_{pp} = 28.1, 40.3, 71.9, and 65.5 V, which are very close to the values in Figures 18.8, 18.9 and 18.10.

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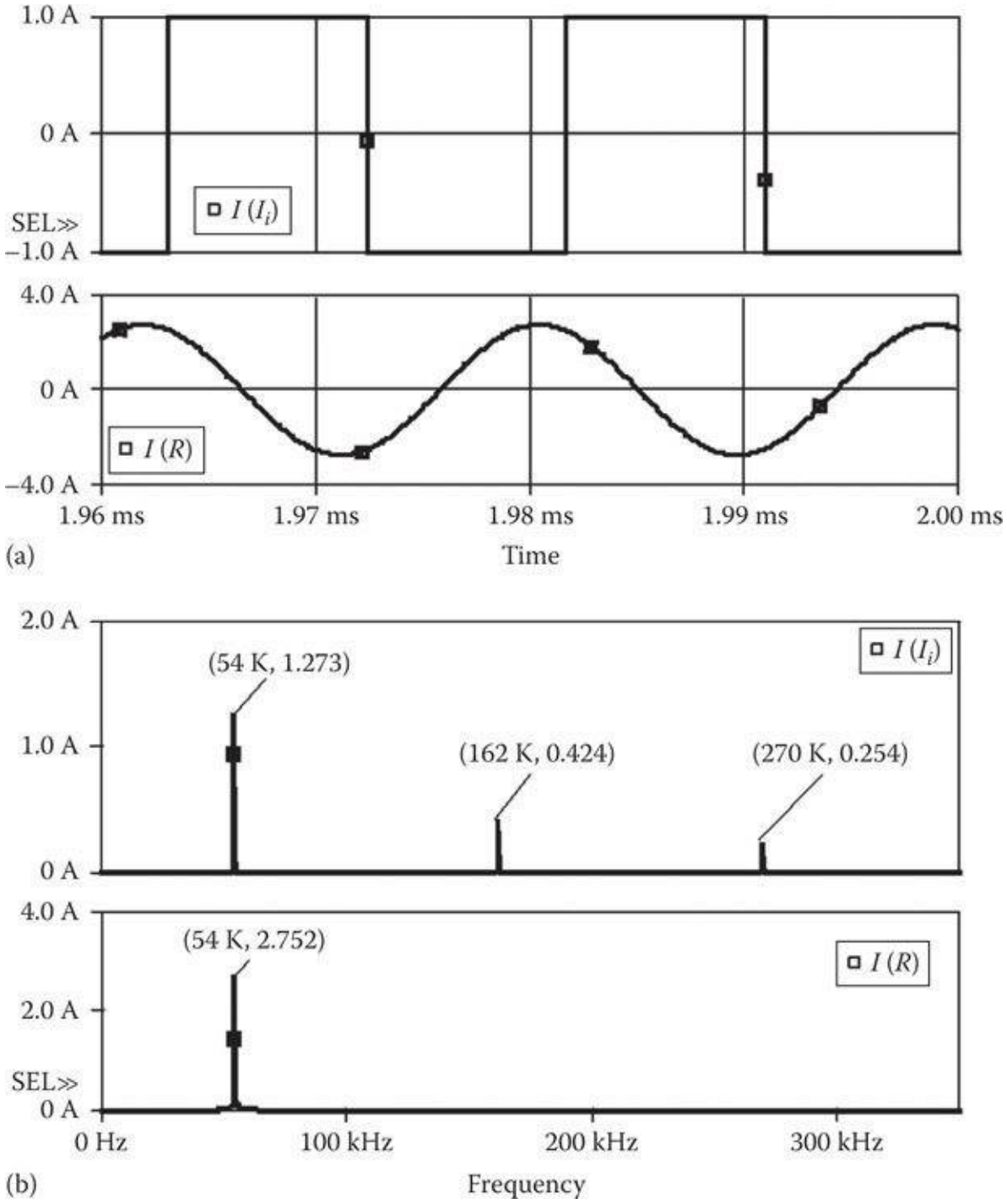


FIGURE 18.10
Input and output current waveforms at f = 54 kHz. (a) Input and output current waveforms. (b) The corresponding fast Fourier transform spectra of input and output current waveforms.

18.5 Discussion

18.5.1 Function of the Double Γ-CL Circuit

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Single Γ-CL filter is a well-known circuit. As a ∏-CLC filter, it is a typical low-pass filter. All harmonics with frequency $\omega > \omega_0$ will be blocked. Cascade double Γ-CL filter circuit has thoroughly different characteristics from that of low-pass filters. It allows the signal with higher frequency $\omega > \omega_0$ (it means $\beta > 1$ in Section 18.2) passing it and enlarging the energy.

18.5.2 Applying Frequency to This Double Γ-CL CSRI

From analysis and verifications, it can be found that the effective applying frequency to this double Γ-CL CSRI is $(0.6 - 2.0)f_0$. Outside this region, both current transfer gain and efficiency are falling fast.

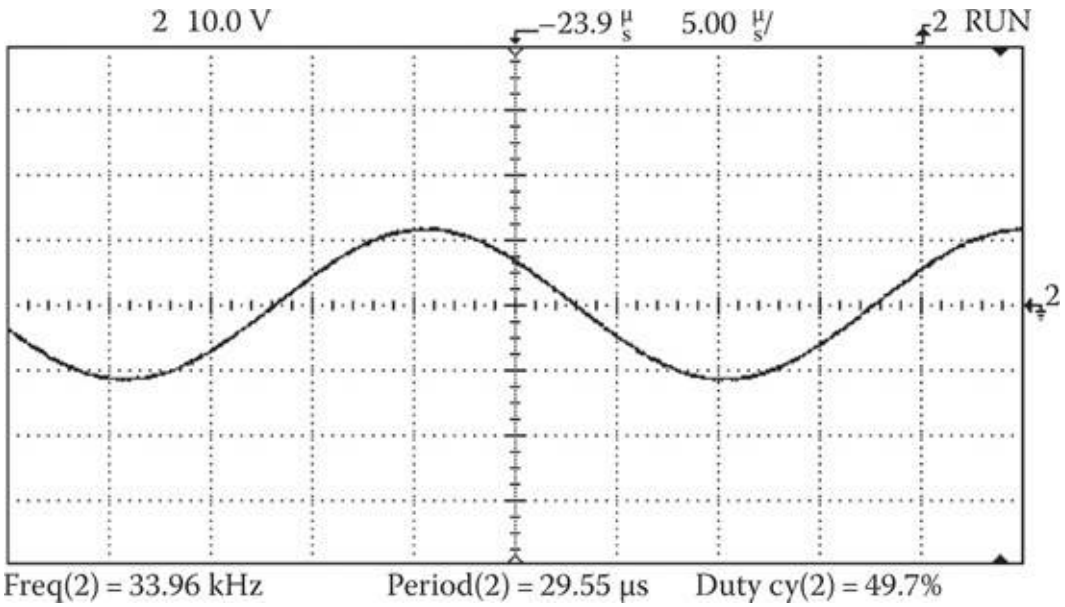


FIGURE 18.11
Testing waveform of the output voltage at $\beta = 1$.

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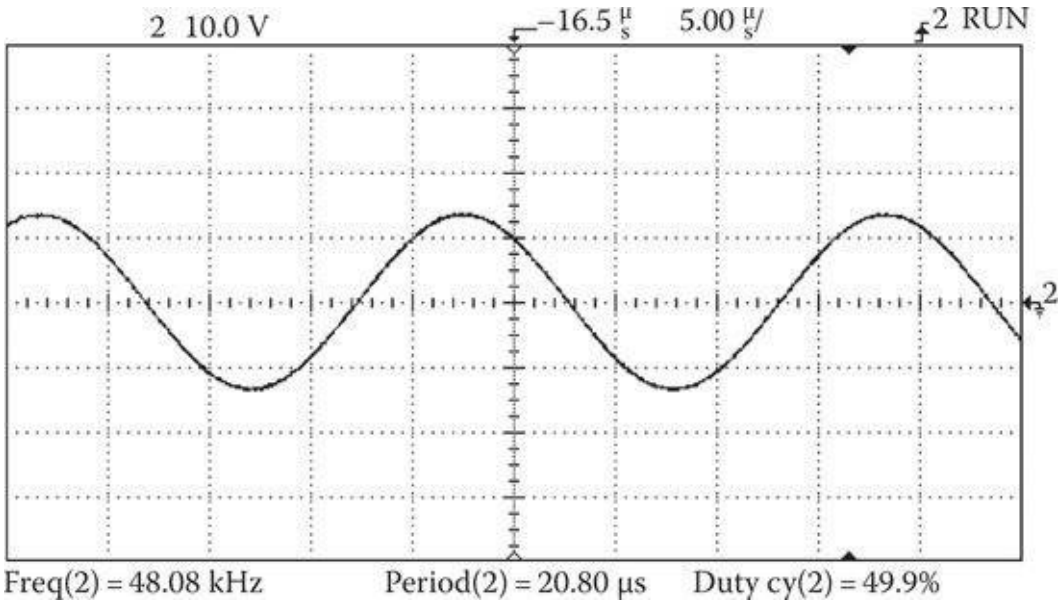


FIGURE 18.12
Testing waveform of the output voltage at β = 1.414.

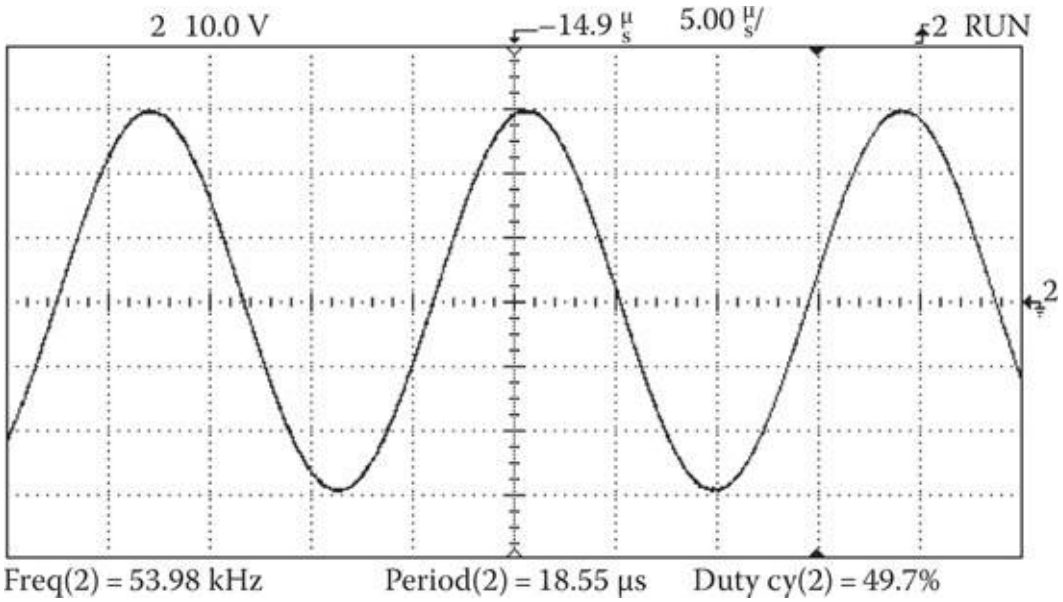


FIGURE 18.13
Testing waveform of the output voltage at β = 1.59.

18.5.3 Explanation of $g > 1$

We recognized the fact that current transfer gain is greater than unity from mathematical analysis and simulation and experimental results. The reason to enlarge the fundamental current is that the resonant circuit transfers the energy of other higher-order harmonics to the fundamental component. Therefore, the gain of the fundamental current can be greater than unity.

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19

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Cascade Reverse Double Γ-LC Resonant Power Converter

A four-element resonant power converter (RPC)—cascaded reverse double Γ-LC RPC—will be discussed in this chapter. Since the first element is an inductor, the power supply should be a bipolar voltage source. Do remember that the first element of current source resonant inverters in the previous chapters is a capacitor; therefore, a bipolar current source was employed. The major work is concentrated on the analysis of steady-state operation, dynamic behavior, and control specialties of the novel resonant converter. The simulation and experimental results show that this resonant converter has many distinct advantages over the existing two- or three-element RPCs and overcomes their drawbacks.

19.1 Introduction

In general, a switched-mode power converter is often required to meet all or most of the following specifications:

- High switching frequency
- High power density for reduction of size and weight
- High conversion efficiency
- Low total harmonic distortion (THD)
- Controlled power factor if the source is an AC voltage
- Low electromagnetic interference

A review of the commonly used pulse-width-modulated (PWM) converter and new generated resonant converter is presented in order to fully understand the two major branches of the high-frequency switching converter. Although PWM technique is widely used in power electronic applications, it encounters serious problems when the switching converter operates at high frequencies. Due to the hard-switching transitions caused by PWM technique, switching losses possess large proportion in total power dissipations. In other words, when the switch is turned on, the current through it rises very fast, while the voltage across it cannot descend immediately due to the parasitic output capacitance. Similarly, when the switch is turned off, the voltage across it rises rapidly, while the current through it cannot drop at once because of the recombination of carriers.

In general, a resonant power converter (RPC) is defined as a converter in which one or more switching waveforms are resonant waveforms. It is reasonable to say that an RPC

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usually contains a resonant circuit. In fact, there are many topologies of the RPC, which are many more than zero-current-switching and zero-voltage-switching quasi-resonant converters in Chapter 14.

19.2 Steady-State Analysis of Cascade Reverse Double Γ-LC RPC

In this chapter, a cascade reverse double Γ-LC RPC is introduced. Under some assumptions and simplifications, the steady-state AC analysis is undertaken to study the two most interesting topics: the voltage transfer gain and the input impedance.

19.2.1 Topology and Circuit Description

The circuit diagram of a half-bridge cascade reverse double Γ-LC RPC is shown in Figure 19.1. Like other resonant converters, this topology consists of a bipolar voltage source, resonant network (the cascade reverse double Γ-LC), the rectifier plus filter, and the load (i.e., a resistive load R). The power MOSFETs S_1 and S_2 and their antiparalleled diodes D_1 and D_2 act together as a bipolar voltage source. To operate this circuit, S_1 is turned on and off 180° out of phase with respect to the turn-off and turn-on of S_2 at same frequency $\omega = 2\pi f$. After the switching circuit, the input voltage can be considered as a bipolar square-wave voltage alternating in value between +V and $-V$, which is then input to the resonant circuit section. L_1, L_2 and C_1, C_2 represent the resonant inductors and capacitors, respectively. The output DC voltage is obtained by rectifying the voltage across the second resonant capacitor C_2. L_f and C_f comprise a low-pass filter to smooth out the output voltage and current, and R denotes either an actual or an equivalent load resistance.

The following assumptions should be made:

1. All the switches and diodes used in the converter are ideal components.
2. All the inductors and capacitors are passive, linear, and time invariant.
3. The output inductor is large enough to assume that the load current does not vary significantly during the switching period.
4. The converter operates above resonance.

19.2.2 Classical Analysis on AC Side

This analysis is available on the AC side before the rectifier bridge.

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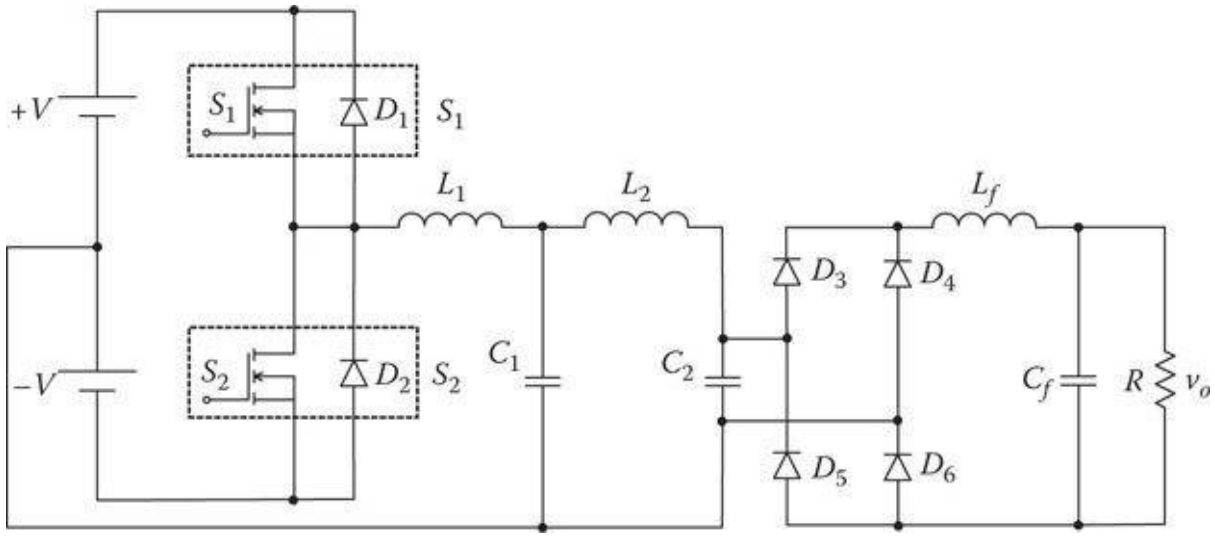


FIGURE 19.1
Circuit diagram of cascade reverse double Γ-LC resonant power converter.

19.2.2.1 Basic Operating Principles

For the cascade reverse double Γ-LC RPC considered here, the half-bridge converter applies a square wave of voltage to a resonant network. Since the resonant network has the effect of filtering the higher-order harmonic voltages, a sine wave of current will appear at the input to the resonant circuit (this is true over most of the load range of interest). This fact allows classical AC analysis techniques to be used. The analysis proceeds as follows. The fundamental component of the square-wave input voltage is applied to the resonant network, and the resulting sine waves of current and voltage in the resonant circuit are computed using classical AC analysis. For a rectifier with an inductor output filter, the sine-wave voltage at the input to the rectifier is rectified, and the average value is taken to arrive at the resulting output DC voltage. For a capacitive output filter, a square wave of voltage appears at the input to the rectifier, while a sine wave of current is injected into the rectifier. For this case, the fundamental component of the square-wave voltage is used in the AC analysis.

19.2.2.2 Equivalent Load Resistance

It is necessary that the rectifier with its filter should be expressed as an equivalent load resistance before the analysis is carried out, which illustrates the derivation of the equivalent resistance to use in loading the resonant circuit. The resonant converter uses an inductor output filter and drives the rectifier with an equivalent voltage source, that is, a low-impedance source provided by the resonant capacitor. A square wave of current is drawn by the rectifier, and its fundamental component must be used in arriving at an equivalent AC resistance. For this case, the root-mean-square values of the voltage and current before the rectifier are given as

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$$v_{ac}(\text{rms}) = \frac{\pi}{2\sqrt{2}} V_o$$

$$i_{ac}(\text{rms}) = \frac{2\sqrt{2}}{\pi} I_{L_f}$$

$$R_{eq} = \frac{v_{ac}(\text{rms})}{i_{ac}(\text{rms})} = \frac{\pi^2}{8} \frac{V_o}{I_{L_f}} = \frac{\pi^2}{8} R$$

The equivalent resistance R_{eq} is shown in Figure 19.2.

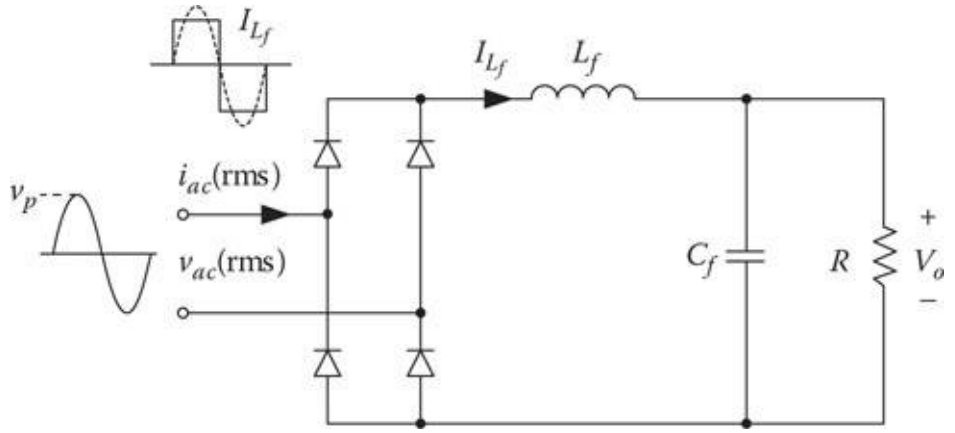


FIGURE 19.2
Equivalent load resistance R_{eq}.

19.2.2.3 Equivalent AC Circuit and Transfer Functions

The equivalent AC circuit diagram of the cascade reverse double Γ-LC RPC is shown in Figure 19.3. Note that all the parameters and variables are transferred to the *s*-domain. Using the Laplace operator $s = j\omega_s$, it is a simple matter to write down the voltage transfer gain of the cascade reverse double Γ-LC RPC:

$$g(s) = \frac{V_o(s)}{V_i(s)} = \frac{R_{eq}}{\left[s^4 L_1 L_2 R_{eq} C_1 C_2 + s^3 L_1 L_2 C_1 + s^2 (L_1 R_{eq} C_1 + L_1 R_{eq} C_2 + L_2 R_{eq} C_2) + s(L_1 + L_2) + R_{eq}\right]}$$

or

$$g(s) = \frac{R_{eq}}{B(s)} \tag{19.1}$$

where

$$B(s) = s^4 L_1 L_2 R_{eq} C_1 C_2 + s^3 L_1 L_2 C_1 + s^2 (L_1 R_{eq} C_1 + L_1 R_{eq} C_2 + L_2 R_{eq} C_2) + s(L_1 + L_2) + R_{eq} \tag{19.2}$$

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The voltage and current stresses on different reactive resonant components are obtained with respect to the input fundamental voltage V_i.

The voltage and current on inductor L_1 are

$$\frac{V_{L_1}(s)}{V_i(s)} = \frac{sL_1[s^3L_2R_{eq}C_1C_2 + s^2L_2C_1 + sR_{eq}(C_1 + C_2) + 1]}{B(s)} \tag{19.3}$$

$$\frac{I_{L_1}(s)}{V_i(s)} = \frac{s^3L_2R_{eq}C_1C_2 + s^2L_2C_1 + sR_{eq}(C_1 + C_2) + 1}{B(s)} \tag{19.4}$$

The voltage and current on capacitor C_1 are

$$\frac{V_{C_1}(s)}{V_i(s)} = \frac{s^2L_2R_{eq}C_2 + sL_2 + R_{eq}}{B(s)} \tag{19.5}$$

$$\frac{I_{C_1}(s)}{V_i(s)} = \frac{sC_1(s^2L_2R_{eq}C_2 + sL_2 + R_{eq})}{B(s)} \tag{19.6}$$

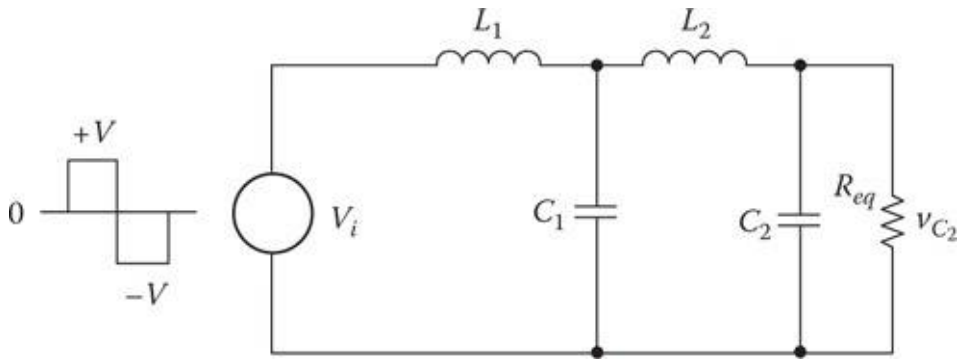


FIGURE 19.3
Equivalent circuit of the cascade reverse double Γ-LC resonant power converter.

The voltage and current on inductor L_2 are

$$\frac{V_{L_2}(s)}{V_i(s)} = \frac{sL_2(sR_{eq}C_2 + 1)}{B(s)} \tag{19.7}$$

$$\frac{I_{L_2}(s)}{V_i(s)} = \frac{sR_{eq}C_2 + 1}{B(s)} \tag{19.8}$$

The voltage and current on capacitor C_2 are

$$G(s) = \frac{V_{C_2}(s)}{V_i(s)} = \frac{R_{eq}}{sC_2 \cdot B(s)} \tag{19.9}$$

$$\frac{I_{C_2}(s)}{V_i(s)} = \frac{sR_{eq}C_2}{B(s)} \tag{19.10}$$

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The input impedance is given by

$$Z_{in} = \frac{B(s)}{s^3 L_2 R_{eq} C_1 C_2 + s^2 L_2 C_1 + s R_{eq}(C_1 + C_2) + 1} \tag{19.11}$$

19.2.2.4 Analysis of Voltage Transfer Gain and the Input Impedance

In general, the voltage gain and the input impedance have more attractions to the designer rather than other transfer functions listed earlier. To simplify the mathematical analysis, the resonant components are chosen as follows:

$$L_1 = L_2 = L \quad C_1 = C_2 = C \quad \omega_0 = \sqrt{\frac{1}{LC}}$$

The quality factor Q is defined as

$$Q = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 C R_{eq}} = \frac{Z_0}{R_{eq}} \tag{19.12}$$

where the characteristic impedance Z_0 is

$$Z_0 = \sqrt{\frac{L}{C}} \tag{19.13}$$

The relative switching frequency is defined as

$$\beta = \frac{\omega}{\omega_0} \tag{19.14}$$

where

ω is the switching frequency

ω_0 is the natural resonance frequency

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{19.15}$$

Under the previously simplified conditions, the voltage gain $g(s)$ given in the previous section can be rewritten as

$$B(\beta) = R_{eq}[1 - 3\beta^2 + \beta^4 + j(2 - \beta^2)\beta Q] \tag{19.16}$$

$$g(\beta) = \frac{1}{(1 - 3\beta^2 + \beta^4) + j(2 - \beta^2)\beta Q} = |g(\beta)| \angle \theta \tag{19.17}$$

The determinant and phase of $g(\beta)$ are given by

$$|g(\beta)| = \frac{1}{\sqrt{(1 - 3\beta^2 + \beta^4)^2 + (2 - \beta^2)^2 \beta^2 Q^2}}$$

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and

$$\theta = -\tan^{-1}\frac{(2-\beta^2)\beta Q}{1-3\beta^2+\beta^4} \tag{19.18}$$

Analogously, the input impedance $Z_{in}(s)$ can also be simplified as

$$Z_{in}(\beta) = \frac{R_{eq}[1-3\beta^2+\beta^4+j(2-\beta^2)\beta Q]}{1-\beta^2+j(2-\beta^2)\beta/Q} = |Z_{in}(\beta)|\angle\phi \tag{19.19}$$

where

$$|Z_{in}(\beta)| = \frac{R_{eq}\sqrt{(1-3\beta^2+\beta^4)^2+(2-\beta^2)^2\beta^2Q^2}}{\sqrt{(1-\beta^2)^2+(2-\beta^2)^2\beta^2/Q^2}}$$

and

$$\phi = \tan^{-1}\frac{(2-\beta^2)\beta Q}{1-3\beta^2+\beta^4} - \tan^{-1}\frac{(2-\beta^2)\beta}{(1-\beta^2)Q} \tag{19.20}$$

The characteristics of the voltage gain $|g(\beta)|$ and phase angle θ versus relative frequency β referring to various Q are shown in Figures 19.4 and 19.5, respectively. Note that for lower Q value, the voltage gain $|g(\beta)|$ is higher than unity at some certain switching frequencies. It means the output voltage can be larger than the fundamental harmonic of the input voltage. The result could be explained thusly: the resonant network consisting of inductors and capacitors has the function of filtering the higher-order harmonic components in the input quasi-square voltage. The energy of higher-order harmonics is then transferred to the fundamental component, thus enlarging the output voltage.

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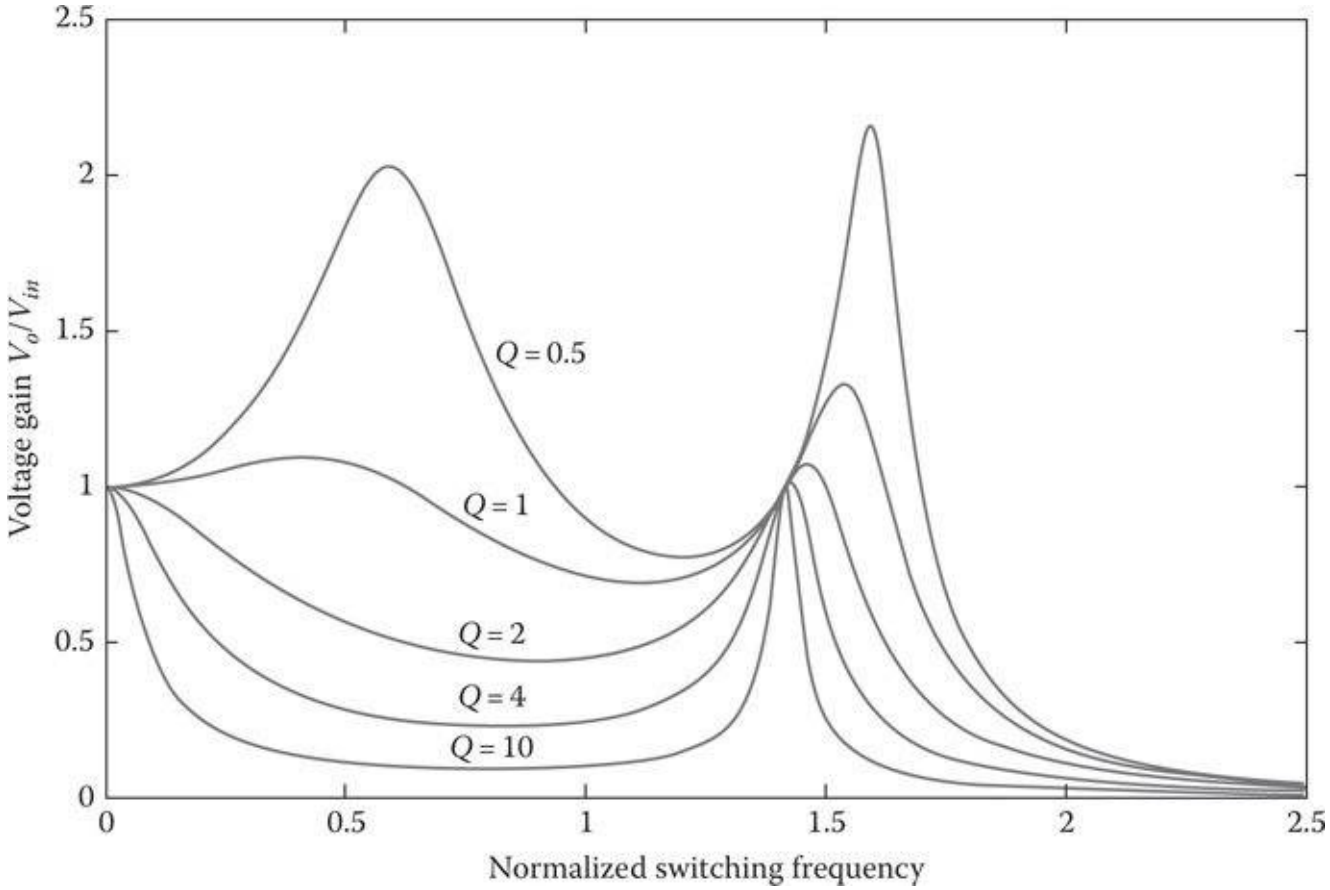


FIGURE 19.4
Voltage gain $|g(\beta)|$ versus β referring to Q.

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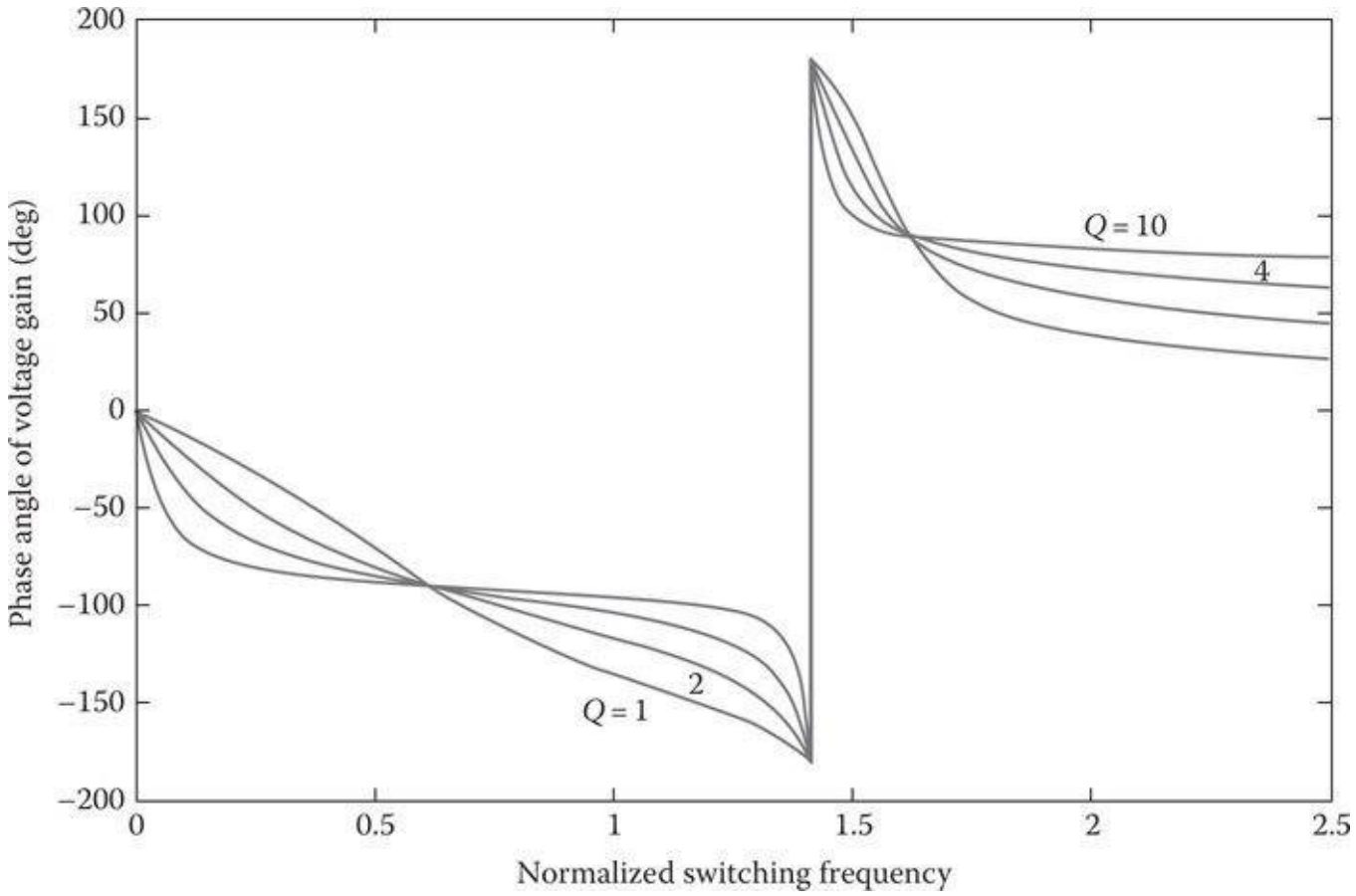


FIGURE 19.5
Phase angle θ versus β referring to *Q*.

This explanation is reasonable when fast Fourier transform is applied to the comparison to waveforms of the input voltage and the second capacitor voltage, respectively. The resonant circuit in cascade reverse double Γ-LC RPC allows the signal with higher frequency ($\beta > 1$) passing it and enlarging the energy. In other words, the bandwidth of this novel converter is wider, as it provides more options for the designer to choose the appropriate operating frequency in different applications.

The maximum voltage gain $|g(\beta)|$ can be obtained from

$$\frac{d}{d\beta^2}\left|g(\beta)\right| = 0$$

or

$$4\beta^6 + (3Q^2 - 18)\beta^4 + (22 - 8Q^2)\beta^2 + 4Q^2 - 6 = 0 \tag{19.21}$$

when

$$Q = 1, \quad 4\beta^6 - 15\beta^4 + 14\beta^2 - 2 = 0 \tag{19.22}$$

yields $\beta_1 = 0.42$, $\beta_2 = 1.11$, $\beta_3 = 1.53$.

It means the local maximum or minimum values on the gain curve are achieved at these roots, respectively. In general, the voltage gain decreases with the increase of the *Q* value. For

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instance, when Q = 1, 2, and 4 with $\beta^2 = 2$, the gain $|g(\beta)|$ = 1, 0.5, and 0.25, respectively. At certain switching frequencies, the smaller the value of Q, the higher the gain.

Specifically, when $Q \ll 1$, Equation 19.21 can be simplified as

$$2\beta^6 - 9\beta^4 + 11\beta^2 - 3 = 0 \tag{19.23}$$

It yields two positive real roots as $\beta_1 = 0.618$ and $\beta_2 = 1.618$.

These roots indicate the existence of two peaks in the voltage gain curve, which is the main characteristics of the four-energy-storage element resonant converters and rarely stated in most conventional two- or three-element counterparts.

The voltage gain $|g(\beta)|$ at these two roots is then given by

$$|g(\beta)| = \left.\frac{1}{\sqrt{(1-3\beta^2+\beta^4)^2 + (2-\beta^2)^2\beta^2Q^2}}\right|_{\beta_1,\beta_2} = \frac{1}{Q} \tag{19.24}$$

This result is derived under the condition $Q \ll 1$ but is applicable for all Q values.

Furthermore, when $Q \gg 1$, Equation 19.21 can be rearranged as

$$3\beta^4 - 8\beta^2 + 4 = 0 \tag{19.25}$$

It gives other two positive real roots as $\beta_3 = 0.816$ and $\beta_4 = 1.414$.

The former represents the switching frequency at which the local minimum gain is achieved, while at the latter, the maximum voltage gain can be obtained.

From Equation 19.24, it can be noted that when β =1.414 ($\beta^2 = 2$), the voltage gain $|g(\beta)|$ constantly keeps unity with any value of Q, as shown in Figure 19.4.

The absolute value of the input impedance $|Z_{in}(\beta)|$ and phase angle ϕ versus β referring to various Q is shown in Figures 19.6 and 19.7, respectively. The input impedance has its maximum value when the switching frequency is equal to natural resonant frequency (i.e., β = 1) and its minimum value when the β = 1.414. The phase angle ϕ keeps zero when β = 1.414, with any Q value, which means the resonant converter can be regarded as a pure resistive load.

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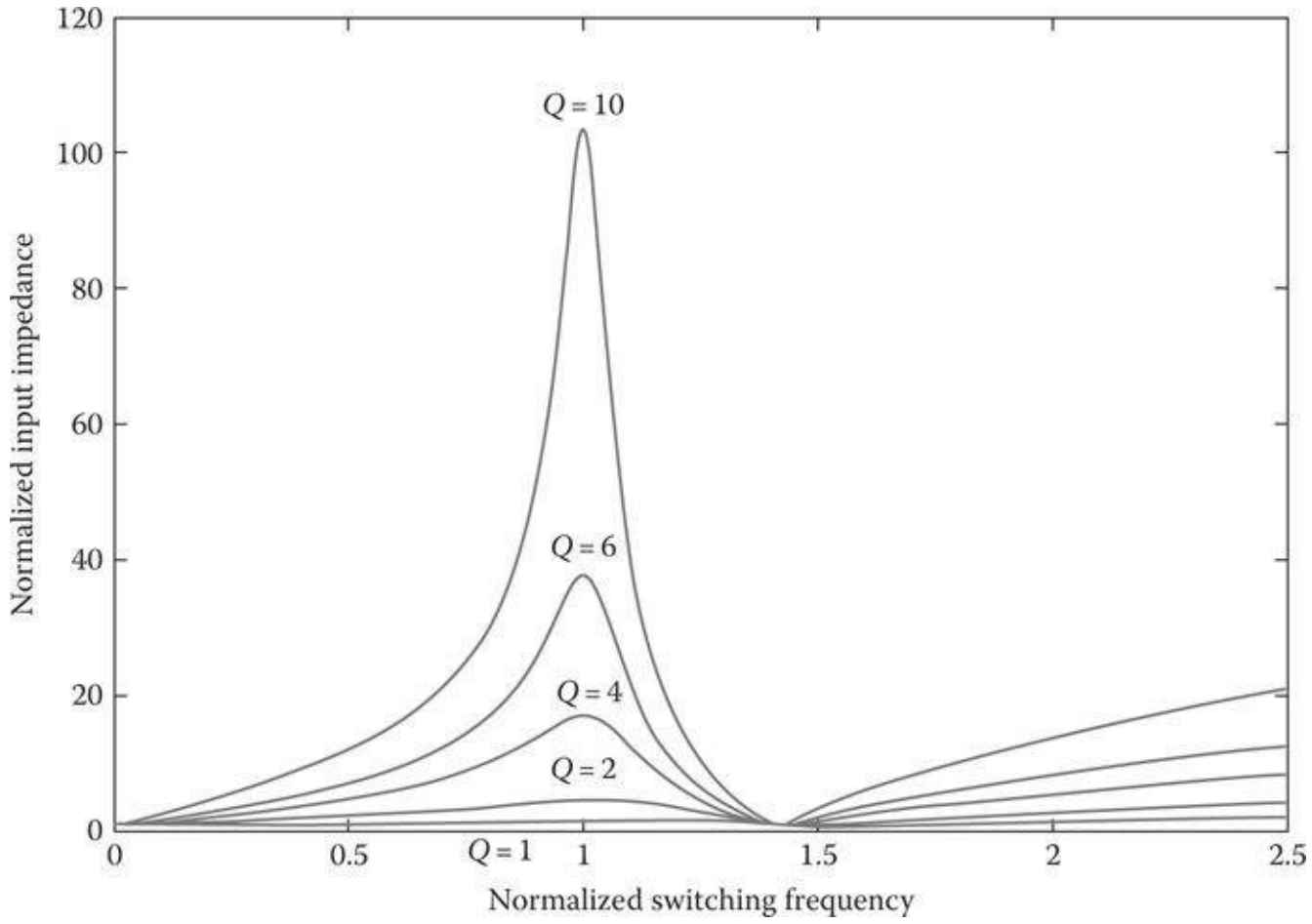


FIGURE 19.6
Input impedance $|Z_{in}(\beta)|$ versus β referring to Q.

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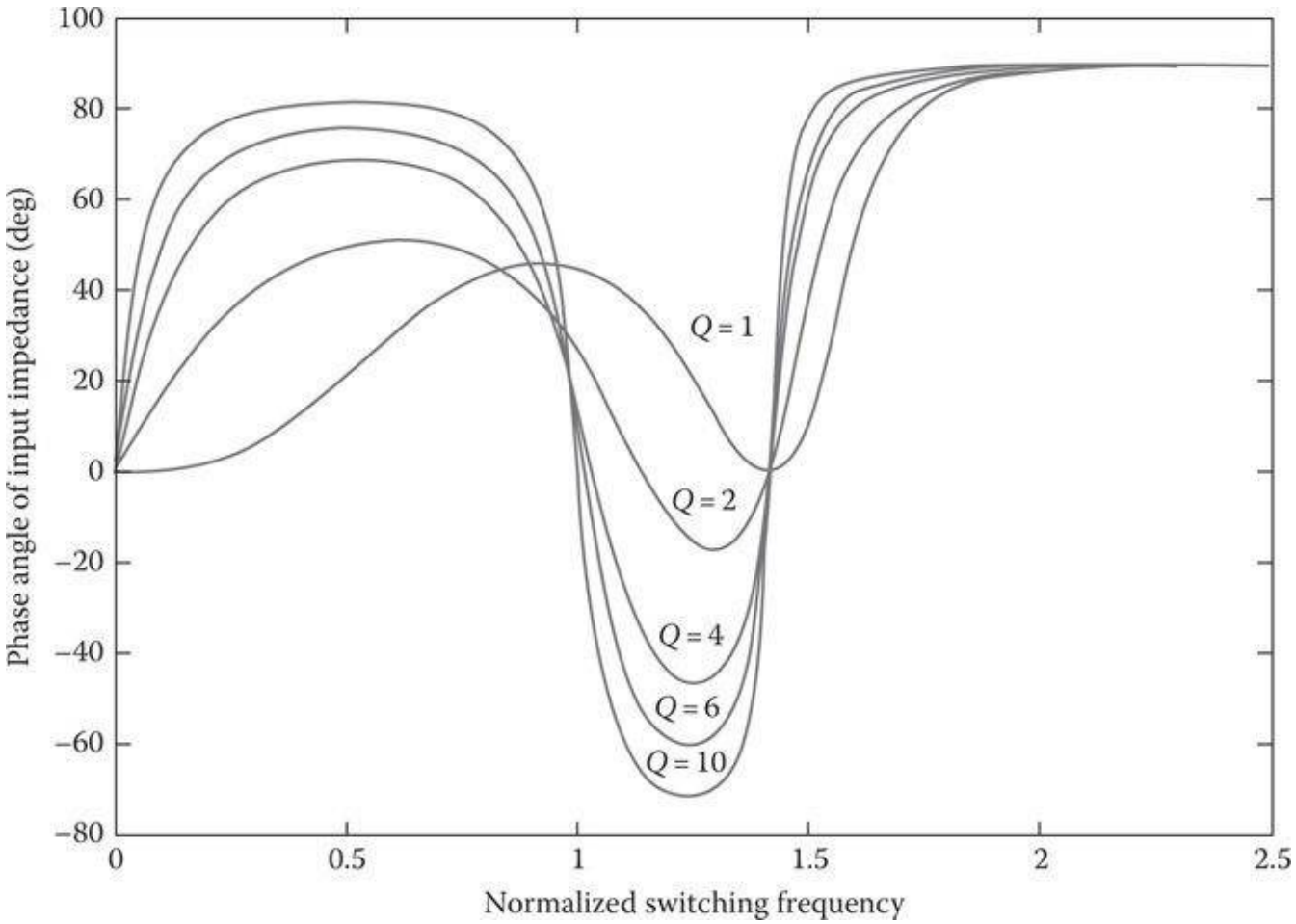


FIGURE 19.7
Phase angle ϕ versus β referring to *Q*.

19.2.3 Simulation and Experiment Results

Some simulation and experimental results shown in this section are helpful to understand the design and analysis. The chosen technical data are good examples to implement a particular RPC for reader's reference.

19.2.3.1 Simulation Studies

In order to verify the mathematical analyses, a four-element cascade reverse double Γ-LC RPC is simulated using PSpice. The parameters used are V_i = ±15 V, $L_1 = L_2$ = 100 μH, $C_1 = C_2$ = 0.22 μF, and R = 22 Ω. The natural resonant frequency is $f_0 = 1/2\pi\sqrt{LC} = 34$ kHz. The applying frequency is f = 50 kHz, corresponding to the β = 1.42. The simulation results are shown in Figure 19.8. The input signal V_i is a square waveform and the voltage across C_2 is a very smooth sinusoidal waveform.

19.2.3.2 Experimental Results

To verify the simulation results of the proposed cascade reverse double Γ-LC RPC, a test rig was constructed with the same conditions: V_i = ±15 V, $L_1 = L_2$ = 100 μH, $C_1 = C_2$ = 0.22 μF,

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and $R = 22\ \Omega$. The natural resonant frequency is $f_0 = 34$ kHz. For high-frequency operation, the main power switch selected is IRF640 with its inner parasitic diode used as the anti-paralleled diode. A high-speed integrated chip IR2104 is utilized to drive the half-bridge circuit. The switching frequency is chosen to be 50.38 kHz, corresponding to the $\beta = 1.42$. The experimental results are shown in Figure 19.9. The input signal V_i is a square waveform and the voltage across C_2 is a very smooth sinusoidal waveform.

Select the switching frequency to be 42.19 kHz, corresponding to the $\beta = 1.24$. The experimental results are shown in Figure 19.10. The input signal V_i is a square waveform and the voltage across C_2 is also a smooth sinusoidal waveform.

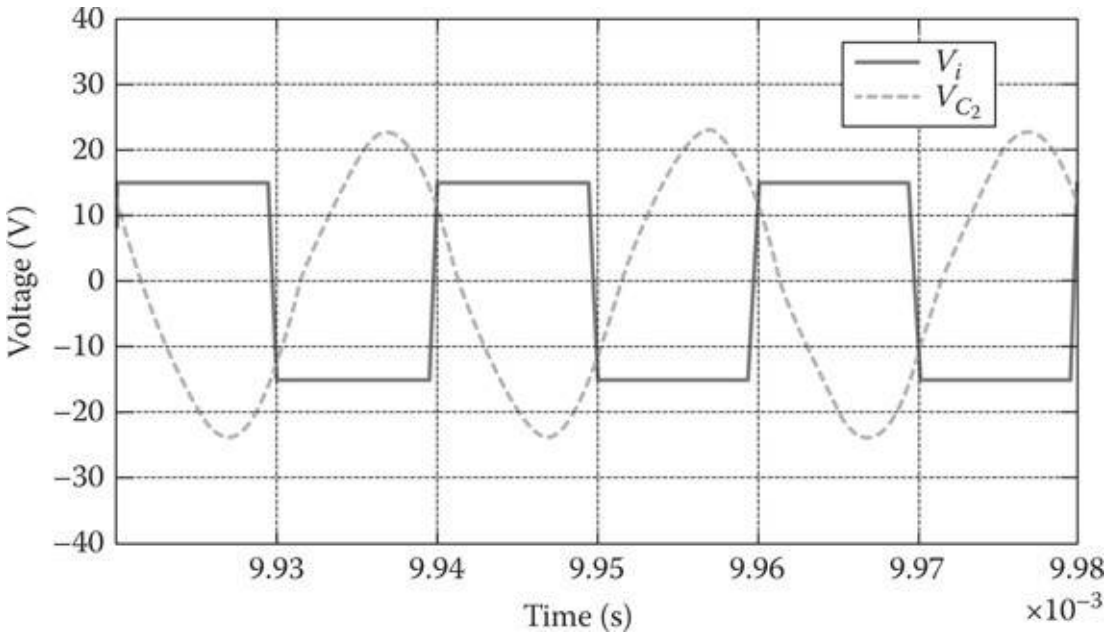


FIGURE 19.8
Simulation results at frequency $f = 50$ kHz.

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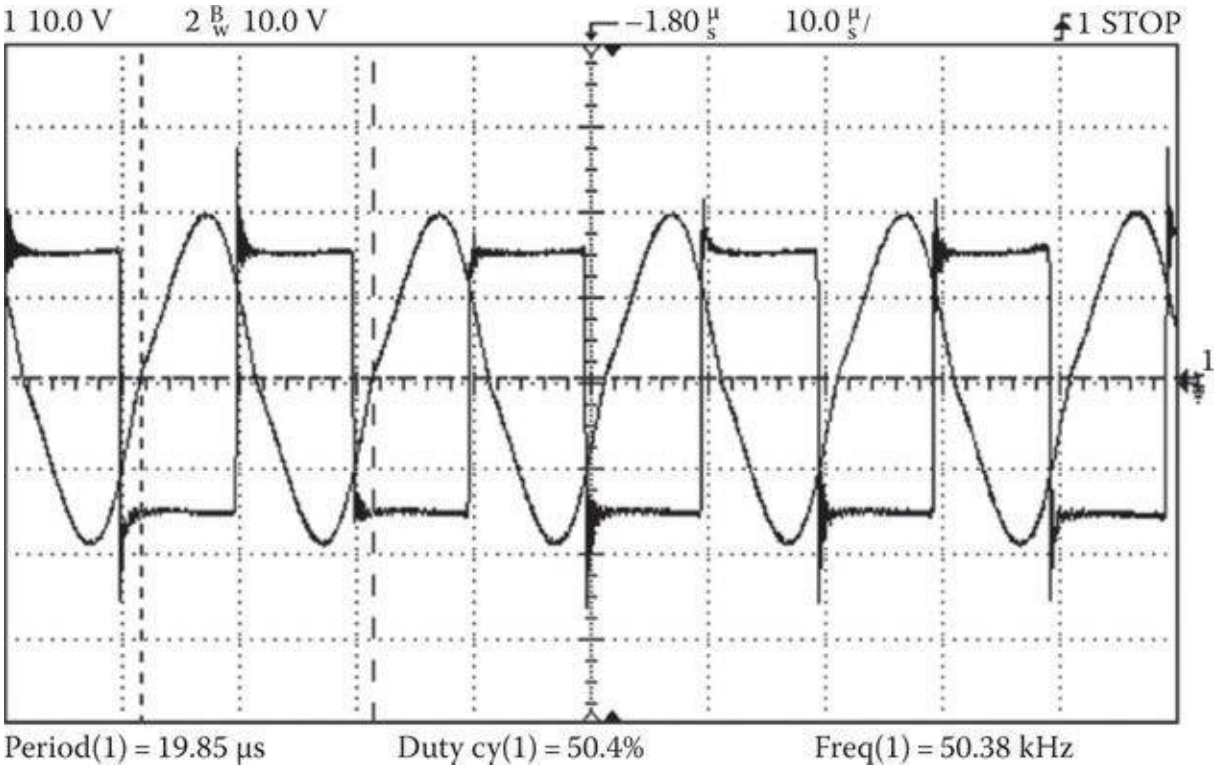


FIGURE 19.9
Experimental waveforms (f = 50.38 kHz).

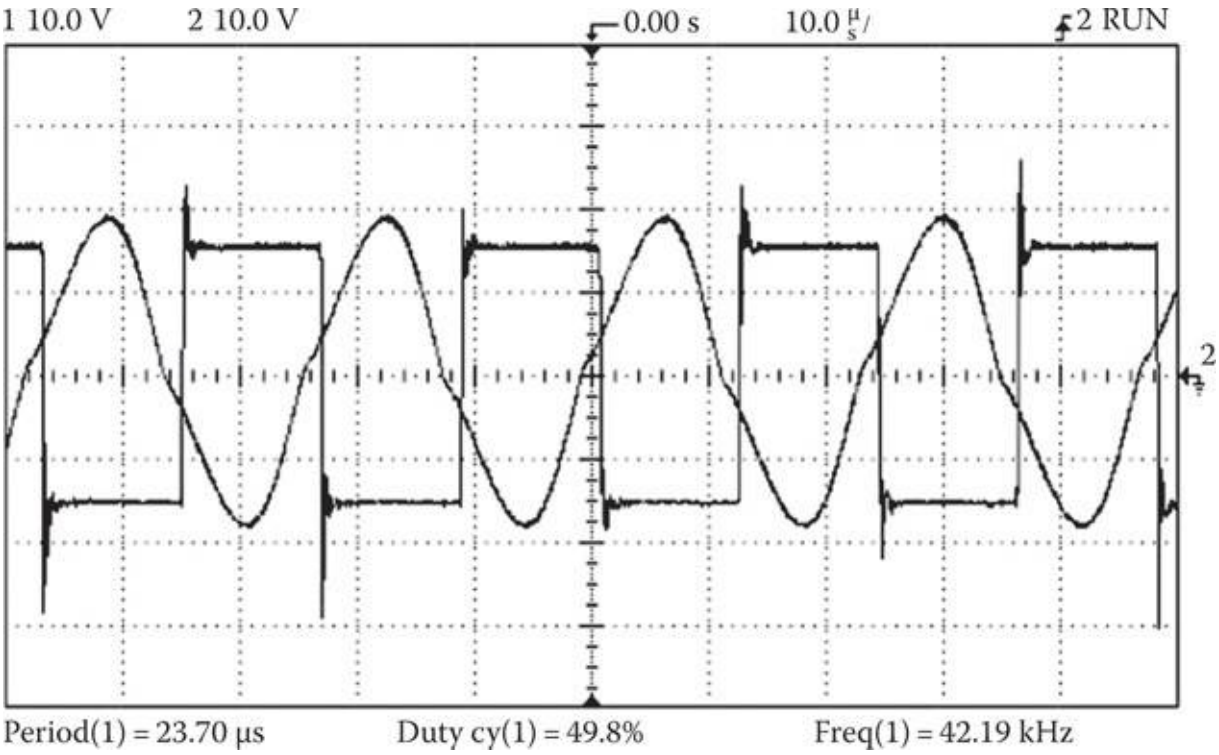


FIGURE 19.10
Experimental waveforms (f = 42.19 kHz).

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19.3 Resonance Operation and Modeling

From the circuit diagram in Figure 19.1, the steady-state operation of the circuit is characterized by four operating modes within one switching period, when the resonant converter operates under continuous conduction mode (CCM). The equivalent circuits corresponding to each operating mode are depicted in Figure 19.11. Note that for a large inductor output filter, the bridge rectifier and the load can be represented as an alternating current sink with constant amplitude I_0, synchronous with the polarity of the second resonant capacitor voltage v_{C_2}.

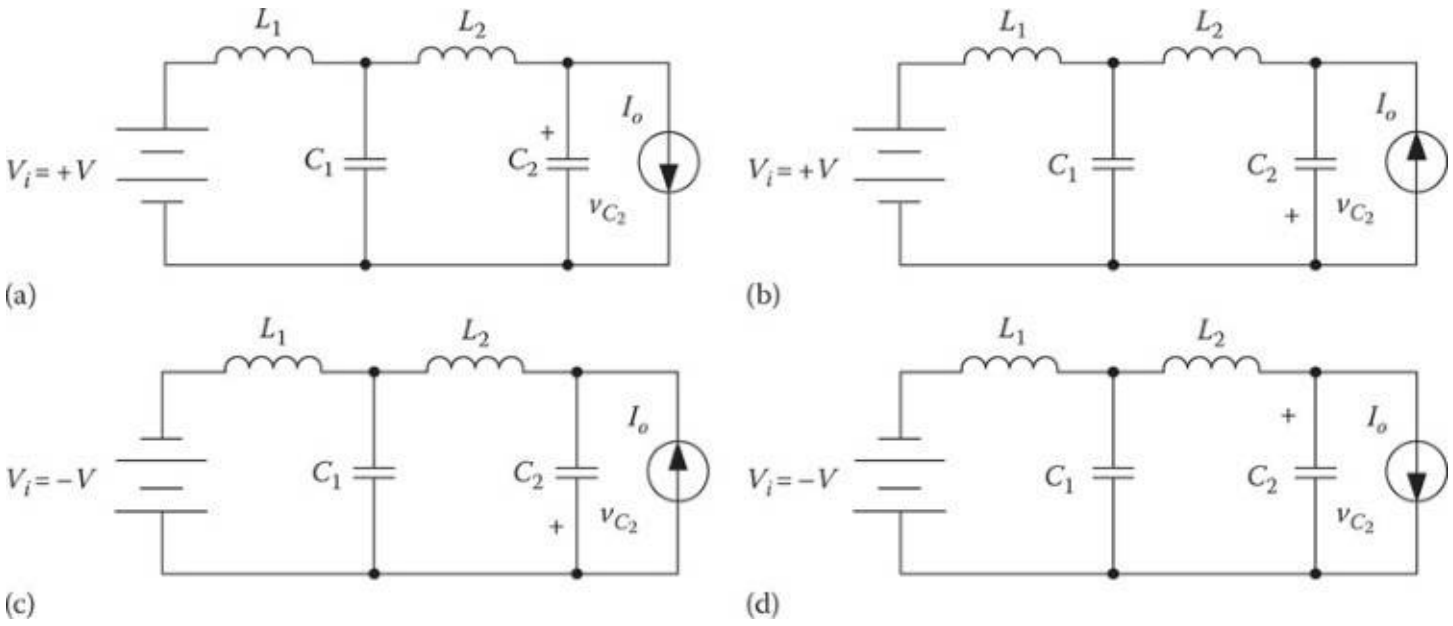


FIGURE 19.11
Different operating resonance modes. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

19.3.1 Operating Principle, Operating Modes, and Equivalent Circuits

The operating modes of cascade reverse double Γ-LC RPC are very difficult to distinguish by analytic calculations, even under CCM condition. However, the state of the converter should not exceed four modes when it operates above resonant frequency. The sequence among different modes is dependent on the phase angle to the voltage gain $V_{C_2}(s)/V_i(s)$. In other words, when this angle is between 0° and +180°, the voltage across the second capacitor v_{C_2} leads the input quasi-wave voltage V_i in Figure 19.12; thus, the sequence from Mode 1 to Mode 4 should be

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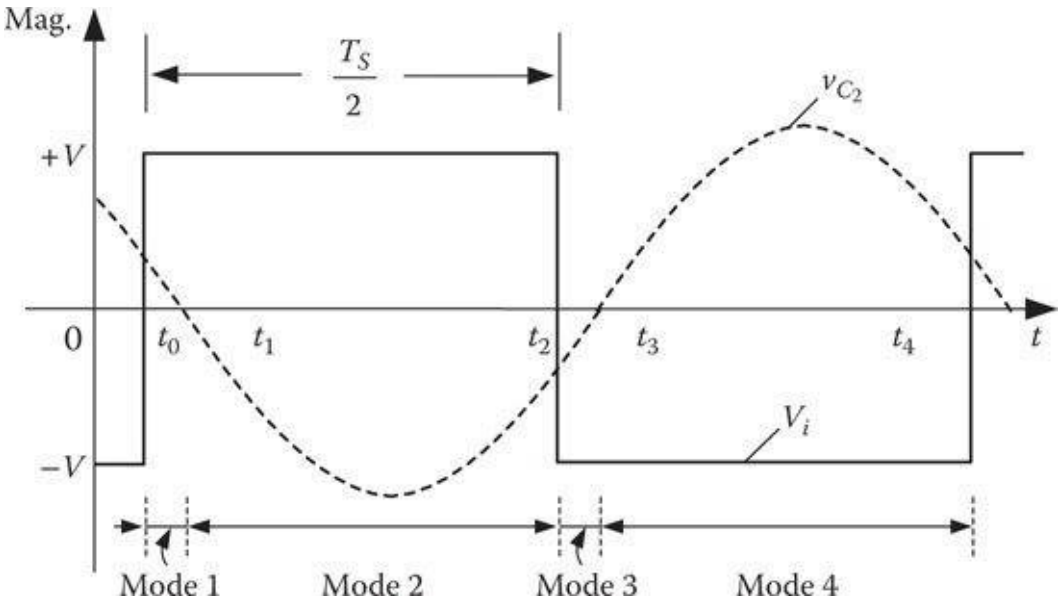


FIGURE 19.12
Voltage waveforms when v_{C_2} leads V_i.

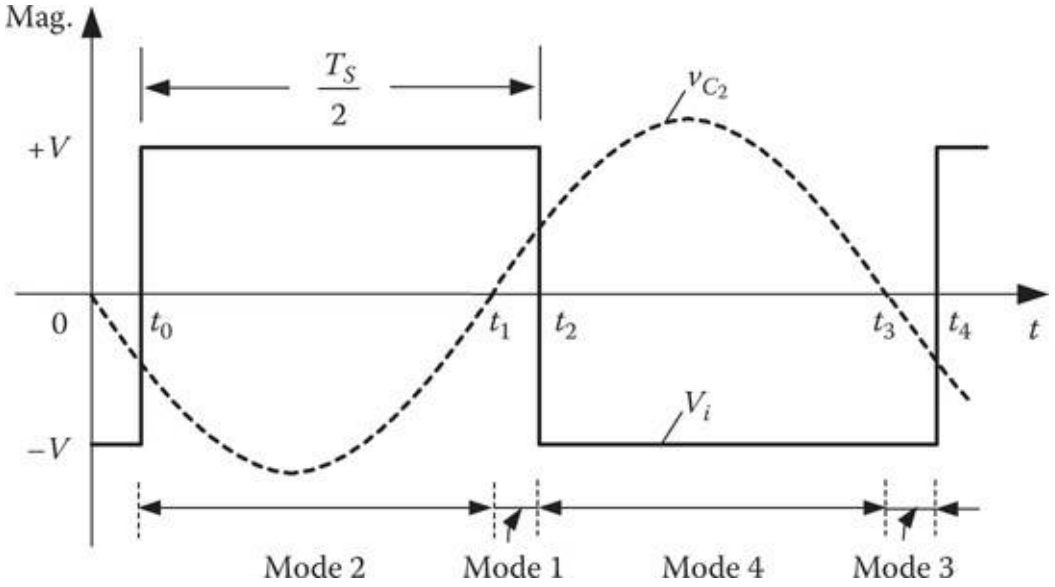


FIGURE 19.13
Voltage waveforms when v_{C_2} lags behind V_i.

- Mode 1 $(t_0 < t < t_1)$: $V_i > 0, v_{C_2} > 0$ (Figure 19.11a)
- Mode 2 $(t_1 < t < t_2)$: $V_i > 0, v_{C_2} < 0$ (Figure 19.11b)
- Mode 3 $(t_2 < t < t_3)$: $V_i < 0, v_{C_2} < 0$ (Figure 19.11c)
- Mode 4 $(t_3 < t < t_4)$: $V_i < 0, v_{C_2} > 0$ (Figure 19.11d)

Similarly, when the angle is between −180° and 0°, v_{C_2} will lag behind the input voltage V_i in Figure 19.13, causing the sequence to change to

- Mode 2 $(t_0 < t < t_1)$: $V_i > 0, v_{C_2} < 0$ (Figure 19.11b)

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- Mode 1 ($t_1 < t < t_2$): $V_i > 0, v_{C_2} > 0$ (Figure 19.11a)
- Mode 4 ($t_2 < t < t_3$): $V_i < 0, v_{C_2} > 0$ (Figure 19.11d)
- Mode 3 ($t_3 < t < t_4$): $V_i < 0, v_{C_2} < 0$ (Figure 19.11c)

In practice, when simulation is in progress, it is up to the algorithm that determines the shifting instant between different operating modes, by means of judging the switching period and the polarity of the second capacitor voltage.

19.3.2 State-Space Analysis

On the basis of the fact that the steady-state operation of resonant converter is periodic and composed of multiple operating modes, each mode stands for one state dependent on the different input voltage and rectifier current; thus, the state equation for each mode is given by

$$\dot{x}_i = A_i x_i + B_i \tag{19.26}$$

where

x_i is the state vector of the converter

A_i is the state coefficient matrix

B_i is the input vector of the converter in the ith operating mode, respectively

For ith mode, Equation 19.26 can be solved analytically:

$$x_i(t) = e^{A_i t} x_i(t_0) + \int_0^t e^{A_i(t-\tau)} B_i d\tau = \Phi_i x_i(t_0) + \Gamma_i \tag{19.27}$$

Here,

$\Phi_i = \Phi(t, t_0) = e^{A_i t}$ is the state transition matrix

$$\Gamma_i = \int_0^t e^{A_i(t-\tau)} B_i d\tau$$

$x_i(t_0)$ are the initial conditions for the ith mode

For the continuous operation, each state solved in ith mode will be employed as the initial conditions for the next $(i + 1)$th mode.

In fact, the solving process of Equation 19.27 is very tedious and time consuming by the requirement for evaluating the integral. However, by combining A_i and B_i to form an augmented dynamic matrix, the integration overhead can be eliminated at the expense of obtaining only the cyclic steady-state description:

$$\frac{d}{dt}\begin{pmatrix} x_i(t) \\ \cdots \\ 1 \end{pmatrix} = \left(\begin{array}{c:c} A_i & B_i \\ \cdots & \cdots \\ 0 & 0 \end{array}\right)\begin{pmatrix} x_i(t) \\ \cdots \\ 1 \end{pmatrix} \tag{19.28}$$

or

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$$\frac{d}{dt}\hat{x}_i(t) = \hat{A}_i\hat{x}_i(t) \tag{19.29}$$

By means of the concept of state transition matrix, the solution for the state vector in different operating modes can be expressed as

$$\hat{x}(t_1) = \hat{\Phi}_1\hat{x}_1(t_0)$$

$$\hat{x}(t_2) = \hat{\Phi}_2\hat{\Phi}_1\hat{x}_1(t_0)$$

For *i*th mode,

$$\hat{x}(t_i) = \hat{\Phi}_i\hat{\Phi}_{i-1}\cdots\hat{\Phi}_1\hat{x}(t_0) = \hat{\Phi}_{tot}\hat{x}(t_0) \tag{19.30}$$

where

$$\hat{\Phi}_i = \begin{pmatrix} \Phi_i & \Gamma_i \\ 0 & 1 \end{pmatrix}$$

and $\hat{x}(t_i)$ is the state vector at time t_i.

Due to periodic nature of the system, the state vector at initial time t_0 should be equal to the one at final time t_i in one cycle, that is,

$$x(t_i) = \Phi_{tot}x(t_0) + \Gamma_{tot} = x(t_0) \tag{19.31}$$

yields

$$x_{init}(t_0) = (I^n - \Phi_{tot})^{-1}\Gamma_{tot} \tag{19.32}$$

Thus, the state variables at any subsequent time are solved from Equation 19.30.

To obtain the average steady-state output voltage, the average values of the state variables over a complete cycle are found from

$$x_{av} = \frac{1}{T}\int_{t_0}^{t_0+T} x(t)dt \tag{19.33}$$

Again, the expression includes the integral process, which can be simplified by augmenting the state vector with

$$\dot{x}_{av}(t) = \frac{1}{T}x(t) \tag{19.34}$$

Then, consider the total dynamics of the converter during the *i*th mode; the simultaneous equations are given by

$$\dot{x}_i = A_ix_i + B_i \tag{19.35}$$

$$\dot{x}_{i-av} = \frac{d_i}{T}x_i \tag{19.36}$$

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where d_i is the duty cycle for ith mode in one cycle.

Substituting Equation 19.36 into Equation 19.28, the resulting dynamic equation is

$$\frac{d}{dt}\begin{pmatrix} x_i(t) \\ \hdashline 1 \\ \hdashline x_{i-av}(t) \end{pmatrix} = \left(\begin{array}{c:c:c} A_i & B_i & 0 \\ \hdashline 0 & 0 & 0 \\ \hdashline \dfrac{d_i}{T} I^n & 0 & 0 \end{array}\right)\begin{pmatrix} x_i(t) \\ \hdashline 1 \\ \hdashline x_{i-av}(t) \end{pmatrix} \tag{19.37}$$

or

$$\dot{z}_i(t) = \tilde{A}_i z_i(t) \tag{19.38}$$

Again, as discussed in the previous section, the state equation can be expressed as the function of state transition matrices in different modes:

$$z(t_i) = \tilde{\Phi}_i \tilde{\Phi}_{i-1} \cdots \tilde{\Phi}_1 z(t_0) \tag{19.39}$$

with the initial conditions

$$z(t_0) = \begin{pmatrix} x_{init}(t_0) \\ \hdashline 1 \\ \hdashline 0 \end{pmatrix} \tag{19.40}$$

From the state variables, that is, the voltage across the capacitors and current through the inductors, their average values can be gained directly.

The state coefficient matrix and the input source vector are determined in terms of different operating modes of the resonant converter. Considering the operating conditions described in Figure 19.12, for *Mode 1*, suppose $V_i > 0$ and $v_{C_2} > 0$, it can be obtained that

$$A_1 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 & -1/C_2 & 0 \\ 0 & 0 & 0 & 1/L_f & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/RC_f \end{bmatrix}$$

and

$$B_1 = \begin{bmatrix} V/L_1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

where

$$x = (i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}, i_{L_f}, v_{C_f})^T$$

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For *Mode 2*, $V_i > 0$, $v_{C_2} < 0$, the structure of the topology is changed due to the alteration of the polarity of the second capacitor voltage, giving

$$A_2 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & -1/L_2 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & 0 & 0 & 1/C_2 & 0 \\ 0 & 0 & 0 & -1/L_f & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/(RC_f) \end{bmatrix}$$

and

$$B_2 = B_1.$$

For *Mode 3*, $V_i < 0$, $v_{C_2} < 0$. Because only the input source is changed, the topology of the system remains invariant. Thus, the state coefficient matrix A_3 is identical with A_2, that is,

$$A_3 = A_2 \quad \text{and} \quad B_3 = \begin{bmatrix} -V/L_1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

Similarly, for

Mode 4, $V_i < 0$, $v_{C_2} > 0$, when operating the above resonance, it yields

$$A_4 = A_1 \quad \text{and} \quad B_4 = B_3$$

By employing the earlier coefficient matrices and vectors with the initial conditions, the values of all state variables in different operating modes can be obtained following Equation 19.39. Thus, the dynamic operating behavior of the resonant converter can be described by these state variables as well.

19.4 Small-Signal Modeling of Cascade Reverse Double Γ-LC RPC

In the previous section, state-space averaging technique has been applied to investigate the dynamic behavior and successfully simulated the waveforms at different time intervals; however, the numerical results cannot reveal the relations of various control specialties, for example, frequency response and closed-loop control system stability. In order to study these characteristics more deeply, a number of mathematical methods were presented, and among them, the small-signal modeling is implemented.

19.4.1 Small-Signal Modeling Analysis

19.4.1.1 Model Diagram

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The block diagram of the small-signal model is depicted in Figure 19.14, where $\hat{v}$ and $\hat{f}_{sN}$ represent small-signal perturbation of the line voltage and the frequency control signal. The output variable is the perturbed output voltage, $\hat{v}_o$. With the model, it is easy to obtain the commonly used small-signal transfer functions, such as control-to-output transfer function, line-to-output transfer function, input impedance, and output impedance.

19.4.1.2 Nonlinear State Equation

The equivalent circuit of the resonant converter is shown in Figure 19.15. As can be seen, the half-bridge circuit employing two diodes applies a square-wave voltage, v_{ab}, to the resonant

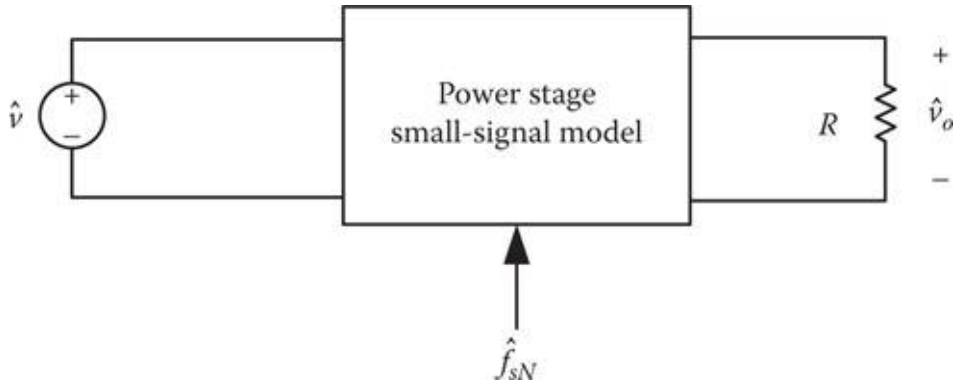


FIGURE 19.14
Small-signal perturbations in input voltage and switching frequency.

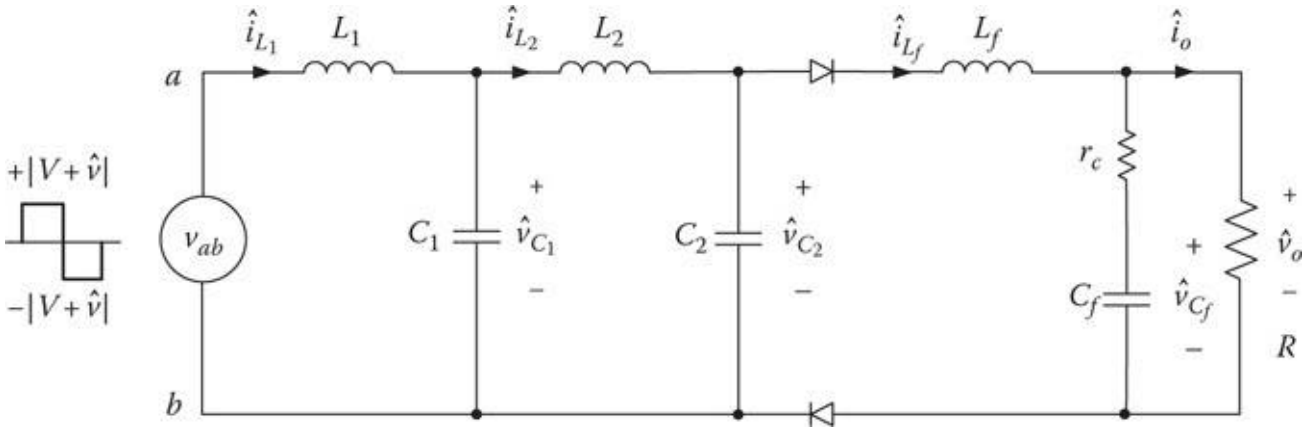


FIGURE 19.15
Equivalent circuit of cascade reverse double Γ-LC resonant power converter.

network. Suppose the converter operates above resonance, the state equations of the resonant converter can be obtained, where the nonlinear terms are in boldface:

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$$
\begin{aligned}
L_1 \frac{di_{L_1}}{dt} + v_{C_1} &= v_{ab} \\
C_1 \frac{dv_{C_1}}{dt} + i_{L_2} &= i_{L_1} \\
L_2 \frac{di_{L_2}}{dt} + v_{C_2} &= v_{C_1} \\
C_2 \frac{dv_{C_2}}{dt} + sgn(v_{C_2}) i_{L_f} &= i_{L_2} \\
L_f \frac{di_{L_f}}{dt} + (i_{L_f} - i_o) r_c + v_{C_f} &= |v_{C_2}| \\
C_f \frac{dv_{C_f}}{dt} &= i_{L_f} - i_o
\end{aligned}
\tag{19.41}
$$

The output variable is the output voltage, v_o, which gives

$$
v_o = (i_{L_f} - i_o) r_c + v_{C_f} \tag{19.42}
$$

In this circuit, the output voltage is regulated either by the input line voltage, v, or by the applying switching frequency, ω. Thus, the operating point p can be expressed as the function of these variables $p = \{v, R, \omega\}$.

19.4.1.3 Harmonic Approximation

Under the assumption that both the voltage and current inside the resonant network are quasi-sinusoidal, the so-called fundamental approximation method is applied to the derivation of the small-signal models. In other words, the variables in the resonant network are assumed as

$$
\begin{aligned}
i_{L_1} &= i_{1s}(t) \sin \omega t + i_{1c}(t) \cos \omega t \\
i_{L_2} &= i_{2s}(t) \sin \omega t + i_{2c}(t) \cos \omega t \\
v_{C_1} &= v_{1s}(t) \sin \omega t + v_{1c}(t) \cos \omega t \\
v_{C_2} &= v_{2s}(t) \sin \omega t + v_{2c}(t) \cos \omega t
\end{aligned}
\tag{19.43}
$$

Note that the envelope terms $\{i_{1s}, i_{1c}, i_{2s}, i_{2c}, v_{1s}, v_{1c}, v_{2s}, v_{2c}\}$ are slowly time varying; thus, the dynamic behavior of these terms can be investigated. The derivatives of i_{L_1}, i_{L_2}, v_{C_1}, and v_{C_2} are found to be

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$$\frac{di_{L_1}}{dt}=\left[\frac{di_{1s}}{dt}-\omega i_{1c}\right]\sin\omega t+\left[\frac{di_{1c}}{dt}+\omega i_{1s}\right]\cos\omega t$$

$$\frac{di_{L_2}}{dt}=\left[\frac{di_{2s}}{dt}-\omega i_{2c}\right]\sin\omega t+\left[\frac{di_{2c}}{dt}+\omega i_{2s}\right]\cos\omega t$$

$$\frac{dv_{C_1}}{dt}=\left[\frac{dv_{1s}}{dt}-\omega v_{1c}\right]\sin\omega t+\left[\frac{dv_{1c}}{dt}+\omega v_{1s}\right]\cos\omega t \quad (19.44)$$

$$\frac{dv_{C_2}}{dt}=\left[\frac{dv_{2s}}{dt}-\omega v_{2c}\right]\sin\omega t+\left[\frac{dv_{2c}}{dt}+\omega v_{2s}\right]\cos\omega t$$

19.4.1.4 Extended Describing Function

By employing the extended describing function (EDF) modeling technique stated in the literature, the nonlinear terms in Equation 19.41 can be approximated either by the fundamental harmonic terms or by the DC terms, to yield

$$v_{ab}(t)\approx f_1(v)\sin\omega_s t$$

$$\operatorname{sgn}(v_2)i_{L_f}\approx f_2(v_{2s},v_{2c},i_{L_f})\sin\omega_s t+f_3(v_{2s},v_{2c},i_{L_f})\cos\omega_s t \quad (19.45)$$

$$\left|v_{C_2}\right|\approx f_4(v_{2s},v_{2c})$$

These functions are called EDFs. They are dependent on the operating conditions and the harmonic coefficients of the state variables. The EDF terms can be calculated by making Fourier expansions of the nonlinear terms, to give

$$f_1(v)=\frac{4}{\pi}v$$

$$f_2(v_{2s},v_{2c},i_{L_f})=\frac{4}{\pi}\frac{v_{2s}}{A_p}i_{L_f} \quad (19.46)$$

$$f_3(v_{2s},v_{2c},i_{L_f})=\frac{4}{\pi}\frac{v_{2c}}{A_p}i_{L_f}$$

$$f_4(v_{2s},v_{2c})=\frac{2}{\pi}A_p$$

where $A_p=\sqrt{v_{2s}^2+v_{2c}^2}$ is the peak voltage of the second capacitor voltage v_{C_2}.

19.4.1.5 Harmonic Balance

Substituting Equations 19.43, 19.44, 19.45 and 19.46 into Equation 19.41, the nonlinear large-signal model of cascade reverse double Γ-LC RPC is obtained as follows:

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$$
\begin{aligned}
L_1\left(\frac{di_{1s}}{dt}-\omega_s i_{1c}\right)+v_{1s} &= \frac{4}{\pi}v \\
L_1\left(\frac{di_{1c}}{dt}+\omega_s i_{1s}\right)+v_{1c} &= 0 \\
C_1\left(\frac{dv_{1s}}{dt}-\omega_s v_{1c}\right) &= i_{1s}-i_{2s} \\
C_1\left(\frac{dv_{1c}}{dt}+\omega_s v_{1s}\right) &= i_{1c}-i_{2c} \\
L_2\left(\frac{di_{2s}}{dt}-\omega_s i_{2c}\right) &= v_{1s}-v_{2s} \\
L_2\left(\frac{di_{2c}}{dt}+\omega_s i_{2s}\right) &= v_{1c}-v_{2c} \\
C_2\left(\frac{dv_{2s}}{dt}-\omega_s v_{2c}\right)+\frac{4}{\pi}\frac{v_{2s}}{A_p}i_{L_f} &= i_{2s} \\
C_2\left(\frac{dv_{2c}}{dt}+\omega_s v_{2s}\right)+\frac{4}{\pi}\frac{v_{2c}}{A_p}i_{L_f} &= i_{2c} \\
L_f\frac{di_{L_f}}{dt}+(i_{L_f}-i_o)r_c &= \frac{2}{\pi}A_p-v_{C_f} \\
C_f\frac{dv_{C_f}}{dt} &= i_{L_f}-i_o
\end{aligned}
\tag{19.47}
$$

The corresponding output equation is

$$
v_o=(i_{L_f}-i_o)r_c+v_{C_f} \tag{19.48}
$$

It should be noted that the small-signal modulation frequency is lower than the switching frequency; thus, the nonlinear model can be linearized by perturbing the system around the operating point *p*. The perturbed variables are the inputs, the state variables, and the outputs. Each one has the form of

$$
x(t)=X+\hat{x}(t)
$$

where

X is the steady state at the operating point

$\hat{x}(t)$ is a small-amplitude perturbation

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Similarly, in this circuit, the input variables are found to be

$$v = V + \hat{v} \quad \omega_s = \Omega_s + \hat{\omega}_s$$

19.4.1.6 Perturbation and Linearization

Under the small-amplitude perturbation assumptions, the complete linearized small-signal models can be established by applying the perturbation to Equation 19.47 and only considering the first partial derivatives, to give

$$\begin{aligned}
L_1 \frac{d\hat{i}_{1s}}{dt} &= Z_{L_1}\hat{i}_{1c} + E_{1s}\hat{f}_{sN} - \hat{v}_{1s} + k_v\hat{v} \\
L_1 \frac{d\hat{i}_{1c}}{dt} &= -Z_{L_1}\hat{i}_{1s} - E_{1c}\hat{f}_{sN} - \hat{v}_{1c} \\
C_1 \frac{d\hat{v}_{1s}}{dt} &= \hat{i}_{1s} - \hat{i}_{2s} + G_s\hat{v}_{1c} + J_{1s}\hat{f}_{sN} \\
C_1 \frac{d\hat{v}_{1c}}{dt} &= \hat{i}_{1c} - \hat{i}_{2c} - G_s\hat{v}_{1s} - J_{1c}\hat{f}_{sN} \\
L_2 \frac{d\hat{i}_{2s}}{dt} &= \hat{v}_{1s} - \hat{v}_{2s} + Z_{L_2}\hat{i}_{2c} + E_{2s}\hat{f}_{sN} \\
L_2 \frac{d\hat{i}_{2c}}{dt} &= \hat{v}_{1c} - \hat{v}_{2c} - Z_{L_2}\hat{i}_{2s} - E_{2c}\hat{f}_{sN} \\
C_2 \frac{d\hat{v}_{2s}}{dt} &= \hat{i}_{2s} - g_{ss}\hat{v}_{2s} + g_{sc}\hat{v}_{2c} - 2k_s\hat{i}_{L_f} + J_{2s}\hat{f}_{sN} \\
C_2 \frac{d\hat{v}_{2c}}{dt} &= \hat{i}_{2c} - g_{cc}\hat{v}_{2c} + g_{cs}\hat{v}_{2s} - 2k_c\hat{i}_{L_f} + J_{2c}\hat{f}_{sN} \\
L_f \frac{d\hat{i}_{L_f}}{dt} &= (\hat{i}_o - \hat{i}_{L_f})r_c - \hat{v}_{C_f} + k_s\hat{v}_{2s} + k_c\hat{v}_{2c} \\
C_f \frac{d\hat{v}_{C_f}}{dt} &= \hat{i}_{L_f} - \hat{i}_o
\end{aligned} \tag{19.49}$$

where the input variables are $\hat{v}$ and $\hat{f}_{sN}$, standing for the perturbed line voltage and normalized switching frequency, respectively.

The output part of the small-signal model is given by

$$\hat{v}_o = \left(\hat{i}_{L_f} - \hat{i}_o\right)r_c + \hat{v}_{C_f} \tag{19.50}$$

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All the parameters used in the earlier models are given in Appendix 19.A.

19.4.1.7 Equivalent Circuit Model

This linearized small-signal model makes it possible to describe the operating characteristics of the resonant converter using equivalent circuit model, as shown in Figure 19.16.

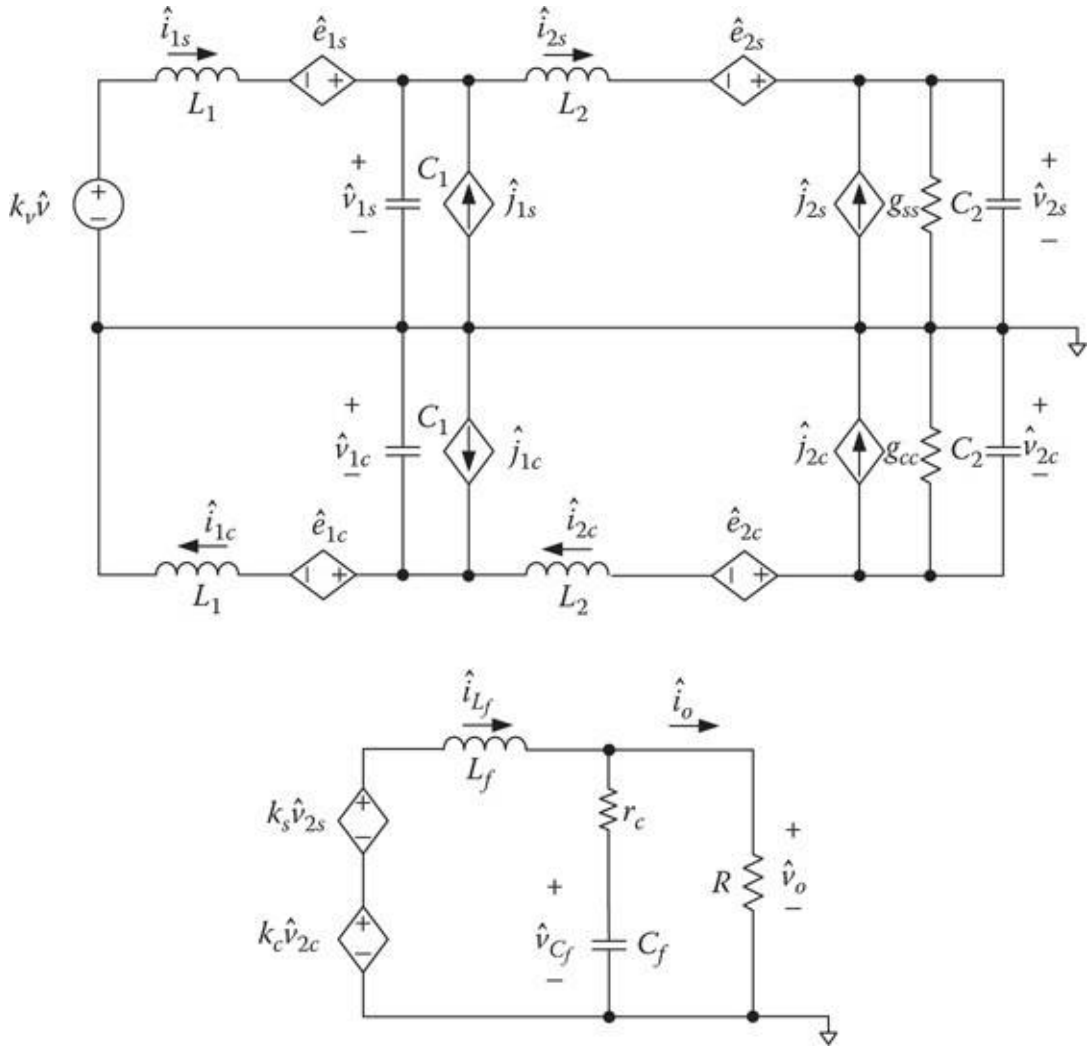


FIGURE 19.16
Equivalent small-signal circuit of cascade reverse double Γ-LC resonant power converter.

In this model, the circuit is divided into two parts: the resonant network and the output part. To simplify the drawing, some dependent sources are defined as

$$\hat{e}_{1s} = Z_{L_1}\hat{i}_{1c} + E_{1s}\hat{f}_{sN} \qquad \hat{e}_{1c} = Z_{L_1}\hat{i}_{1s} + E_{1c}\hat{f}_{sN}$$

$$\hat{e}_{2s} = Z_{L_2}\hat{i}_{2c} + E_{2s}\hat{f}_{sN} \qquad \hat{e}_{2c} = Z_{L_2}\hat{i}_{2s} + E_{2c}\hat{f}_{sN}$$

$$\hat{j}_{1s} = G_s\hat{v}_{1c} + J_{1s}\hat{f}_{sN} \qquad \hat{j}_{1c} = G_s\hat{v}_{1s} + J_{1c}\hat{f}_{sN}$$

$$\hat{j}_{2s} = g_{sc}\hat{v}_{2c} - 2k_s\hat{i}_{L_f} + J_{2s}\hat{f}_{sN} \qquad \hat{j}_{2c} = g_{cs}\hat{v}_{2s} - 2k_c\hat{i}_{L_f} + J_{2c}\hat{f}_{sN}$$

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By employing the Kirchhoff's current law and voltage law, the equivalent circuit can be drawn following the state equations 19.49. Note that in the output part, the voltage across the second capacitor $|\hat{v}_{C_2}|$ is replaced by two voltage-controlled sources $\{k_s\hat{v}_{2s}, k_c\hat{v}_{2c}\}$. This circuit model can be implemented in general-purpose simulation software, such as PSpice or MATLAB®, to obtain the frequency response of the system.

19.4.2 Closed-Loop Control System Design

The closed-loop control system diagram of the half-bridge cascade reverse double Γ-LC RPC is illustrated in Figure 19.17, where the feedback loop is composed of the sampling network, the compensator, and the voltage-controlled oscillator (VCO). The sampling network, R_1 and R_2, contributes attenuation according to its sampling ratio of $R_1/(R_1 + R_2)$.

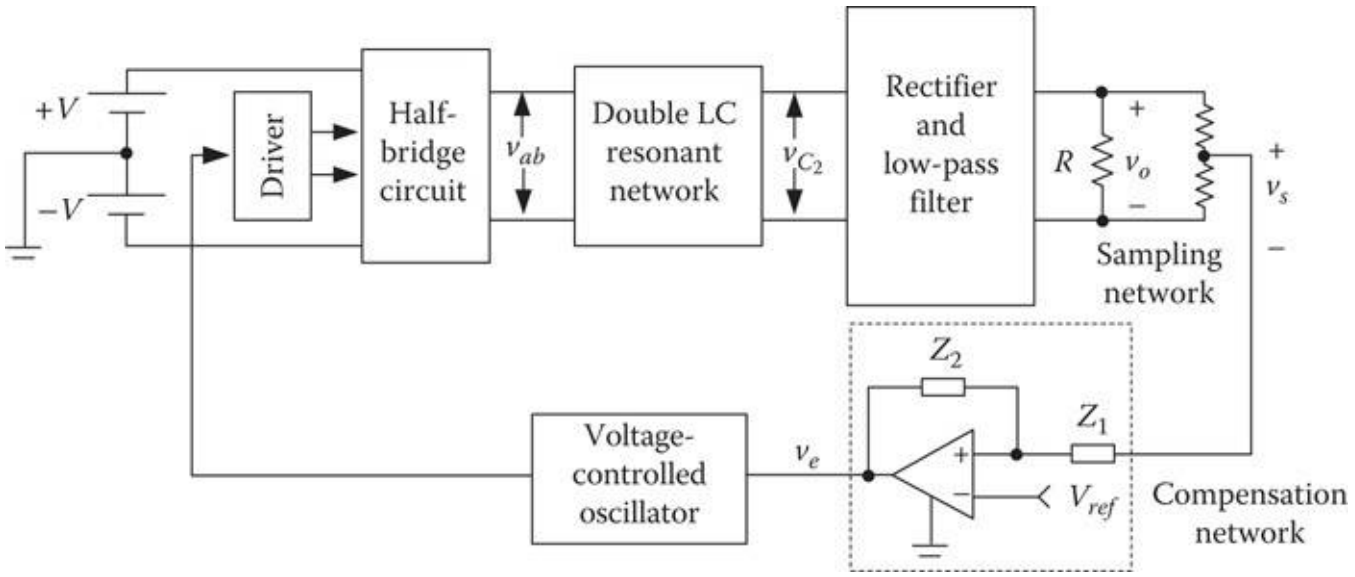


FIGURE 19.17
The closed-loop system of cascade reverse double Γ-LC resonant power converter.

Since the two resistors are chosen to be equal, the gain attenuation of the network is $20 \times \log(v_s/v_o) = -6$ dB. The sampled voltage, v_s, is then sent to the inverting input side of the error amplifier, where it is compared with a fixed reference voltage v_{ref} and generates an error voltage, v_e. This voltage determines the frequency output of a VCO, whose gain can be obtained either in datasheet or by experiment. The Bode plot, considering all the voltage gains of the main circuit, the sampling network, and VCO, is shown in Figure 19.18.

It should be noted that the slope of the magnitude response at the unity-gain crossover frequency is −40 dB/decade. Both the gain margin and the phase margin of the small-signal model are not able to meet the requirements of the stability. Thus, the alleged feedback compensation is often used to shape the frequency response such that it remains stable under all operating conditions, especially in the presence of noise or disturbance injected at any point in the loop. In order to yield a −20 dB/decade slope at the unity-gain crossover frequency, the magnitude response of the compensation network must have a slope of +20

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dB/decade slope at the unity-gain crossover frequency. Hence, a three-pole and double-zero compensation network is employed, whose circuit implementation and Bode diagram are shown in Figures 19.19 and 19.20, respectively.

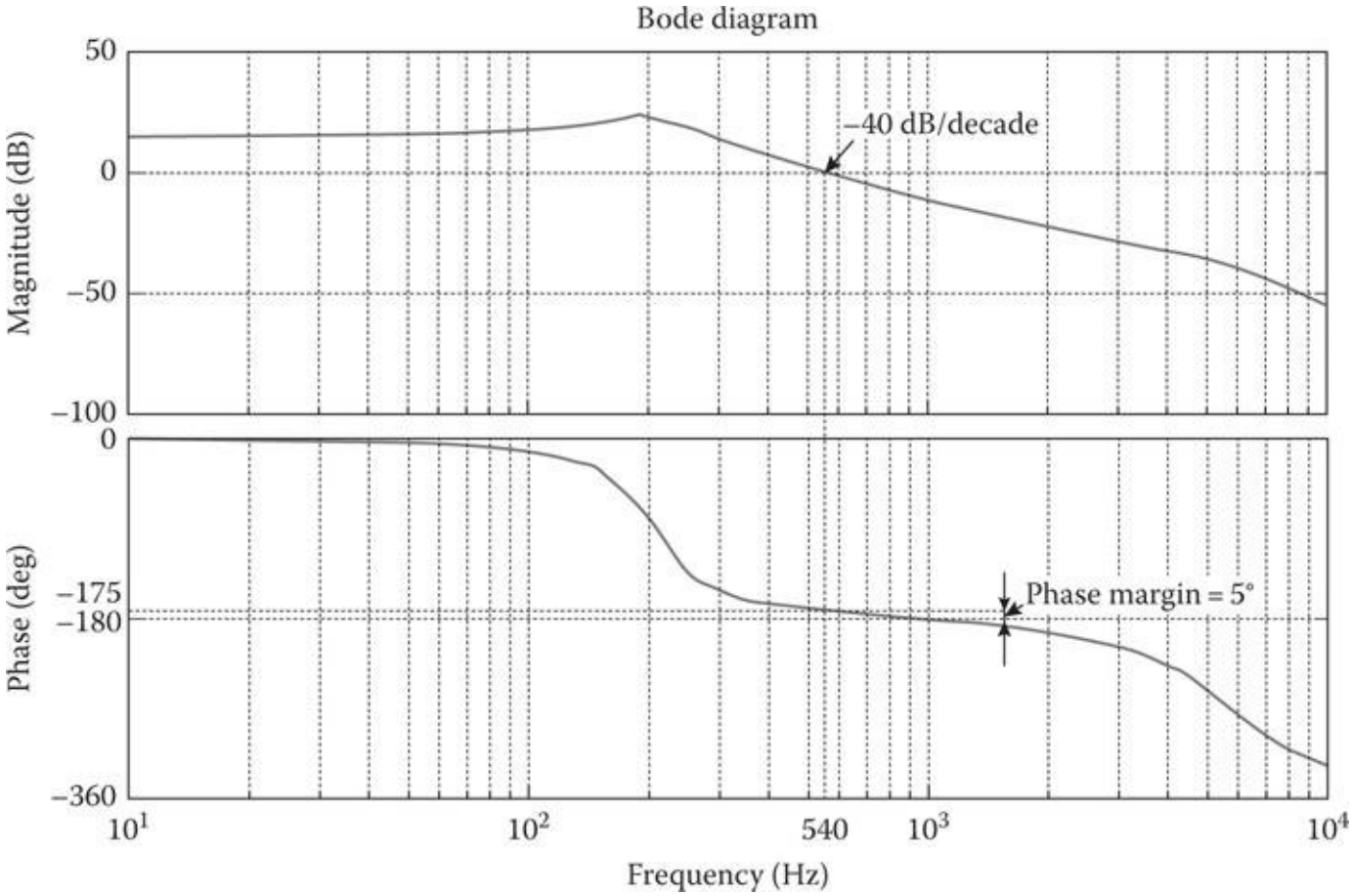


FIGURE 19.18
Bode diagram of the small-signal equivalent circuit.

The transfer function for this compensation network is

$$H(j\omega) = \frac{1 + j\omega R_2 C_1}{-\omega^2 R_2 C_1 C_2 + j\omega(C_1 + C_2)} \frac{1 + j\omega(R_1 + R_3)C_3}{R_1 + j\omega R_1 R_3 C_3} \tag{19.51}$$

As can be seen from this equation, it has two high-frequency poles, one at $f_{p1} = 1/2\pi R_3 C_3$ and the other at $f_{p2} = (C_1 + C_2)/2\pi R_2 C_1 C_2$. The zeros are at $f_{z1} = 1/2\pi R_2 C_1$ and

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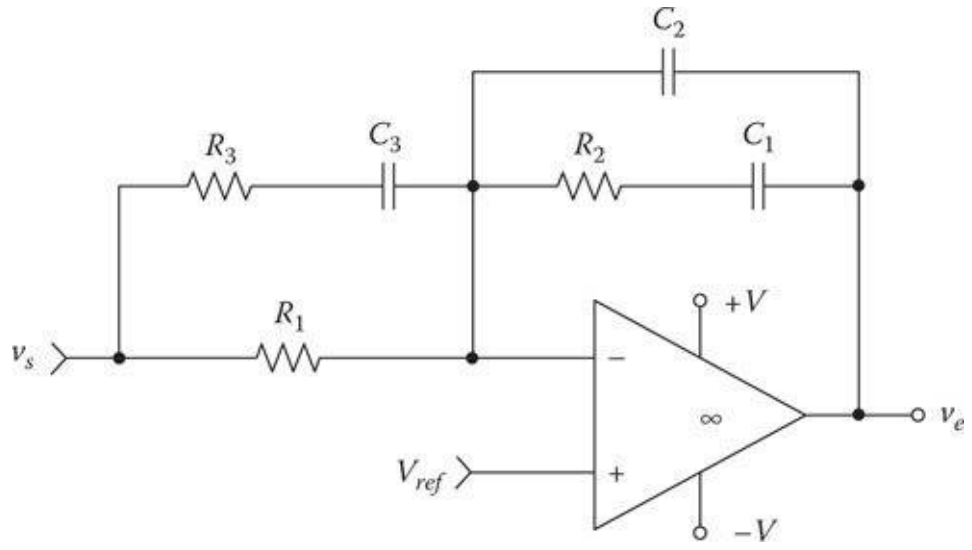


FIGURE 19.19
Compensation network.

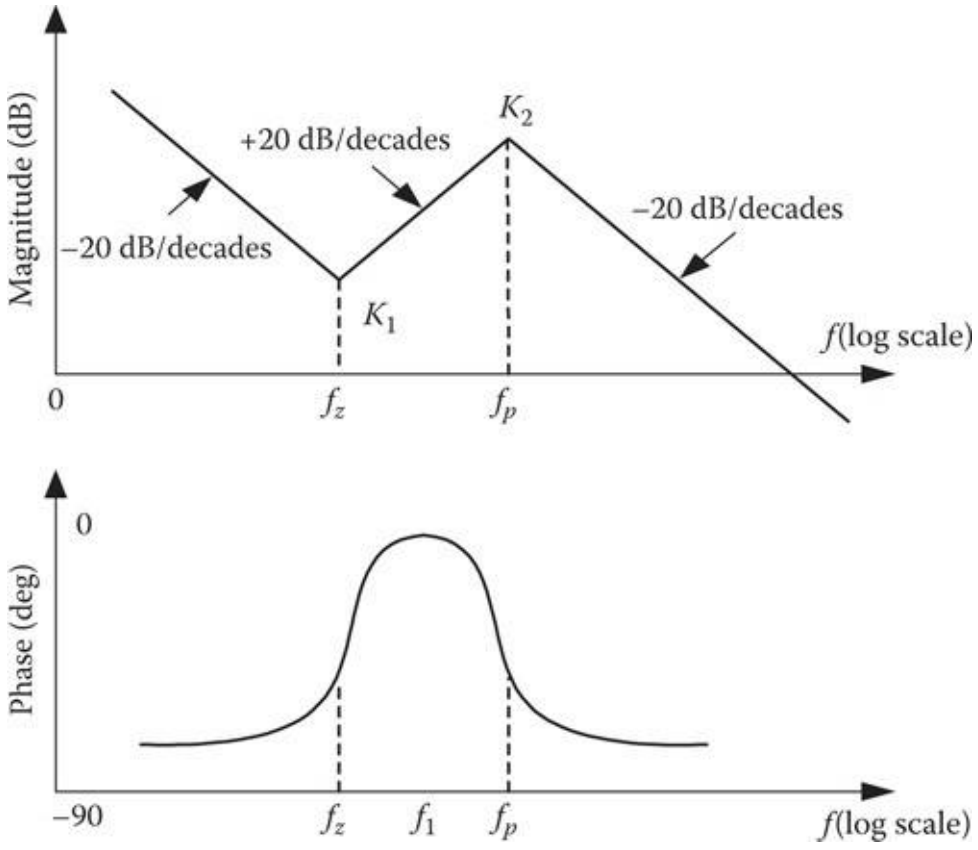


FIGURE 19.20
Bode schematic diagram of the compensation network.

$f_{z2} = 1/2\pi(R_1 + R_3)C_3$ respectively. The two gains of the compensation network are $K_1 = R_2/R_1$ and $K_2 = R_2(R_1 + R_3)/R_1R_3$, respectively. To simplify the design process, the two high-frequency poles are usually chosen to be equal to each other (i.e., $f_{p1} = f_{p2} = f_p$) such that

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$$\frac{1}{2\pi R_3 C_3} = \frac{C_1 + C_2}{2\pi R_2 C_1 C_2} \tag{19.52}$$

The phase lag due to the double poles, θ_p, is

$$\theta_p = 2\tan^{-1}\left(\frac{f_p}{f_1}\right) \tag{19.53}$$

where f_1 is the unity-gain crossover frequency.

Similarly, the two zeros are also chosen to be equal, such that

$$\frac{1}{2\pi R_2 C_1} = \frac{1}{2\pi(R_1 + R_3)C_3} \tag{19.54}$$

The phase boost at the double zeros, θ_z, is

$$\theta_z = 2\tan^{-1}\left(\frac{f_1}{f_z}\right) \tag{19.55}$$

Hence, the total phase lag introduced by the compensation network and the error amplifier at the unity-gain crossover frequency is

$$\theta_c = 270° - 2\tan^{-1}\left(\frac{f_1}{f_z}\right) + 2\tan^{-1}\left(\frac{f_p}{f_1}\right) \tag{19.56}$$

where the 270° phase lag is due to the phase inversion introduced by the inverting amplifier and the pole at the origin of the compensation network.

Consider the real system described in Figure 19.21; the unity-gain crossover frequency is chosen to be 900 Hz, where the attenuation is −16 dB. Hence, the gain of the error amplifier at the unity-gain crossover frequency is chosen to be +16 dB in order to yield 0 dB at the unity-gain crossover frequency.

The locations of the double poles and double zeros of the compensation network are chosen to yield the desired phase margin of 45°. The total phase shift at the unity-gain crossover frequency is 360° −45° or 315°. Taking into account the effect of equivalent series resistor (ESR) in the output capacitor, the phase lag of the output filter with an output capacitor ESR is

$$\theta_{LC} = 180° - \tan^{-1}\left(\frac{f_1}{f_{ESR}}\right) \tag{19.57}$$

where f_{ESR} is the ESR break frequency

$$f_{ESR} = \frac{1}{2\pi r_c C_f} \tag{19.58}$$

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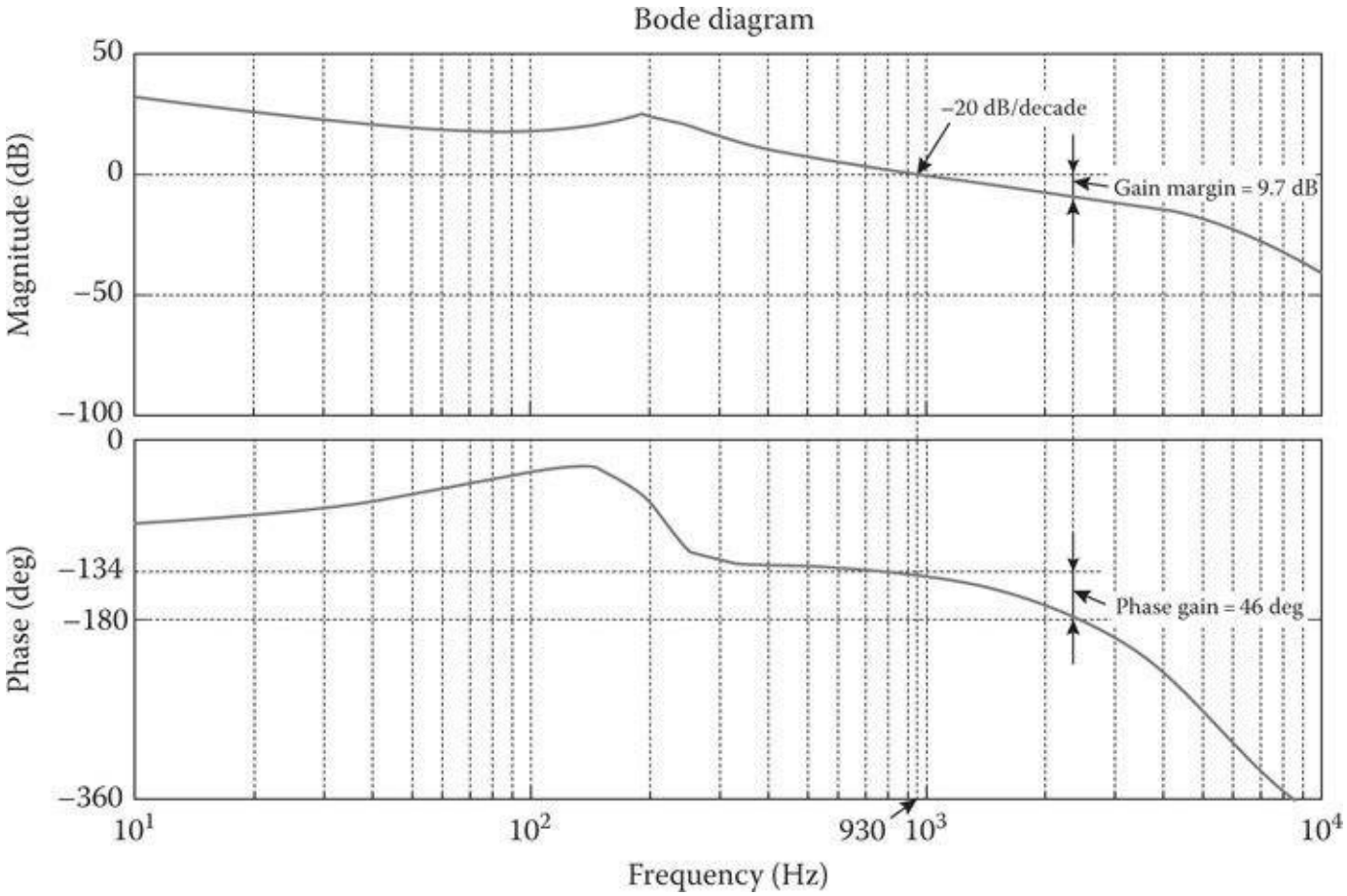


FIGURE 19.21
Bode diagram of the open-loop system.

Then, the phase lag contribution from the compensation network and the error amplifier is

$$\theta_{ea} = 315° - \theta_{LC} \tag{19.59}$$

Hence, from Equation 19.58, the phase lag contribution from the compensation network is

$$2\tan^{-1}\left(\frac{3}{f_z}\right) - 2\tan^{-1}\left(\frac{f_p}{3}\right) = 270° - \theta_{ea} \tag{19.60}$$

Solving this equation yields a value of 4.64 to achieve a phase lag of 65.67°. Hence, the high-frequency pole should be located at 4.64 times the unity-gain crossover frequency, or 4.2 kHz, while the low-frequency zero should be located at one-fourth of the unity-gain crossover frequency, or 190 Hz. There are six components to be selected for the compensation network. As described previously, the gain at the double zero, K_1, is 0 dB, or 1. Assuming an R_1 value of 1 $k\Omega$, R_2 is 1 $k\Omega$ too. The gain at the double poles, K_2, is selected to be 20 dB, or 10. Thus, R_3 is given by

$$R_3 = \frac{R_1 R_2}{K_2 R_1 - R_2} \tag{19.61}$$

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The capacitance value for C_3 is

$$C_3 = \frac{1}{2\pi f_p R_3} \tag{19.62}$$

Hence, the capacitance values of C_1 and C_2 can be calculated, respectively, from Equations 19.52 and 19.54.

The Bode diagram of the open-loop system is given in Figure 19.21. Note that the gain at the unity-gain crossover frequency in the overall magnitude response of the feedback-compensated resonant converter is 0 dB with a slope of −20 dB/decade. The unity-gain crossover frequency is enhanced from 540 to 930 kHz, at which point the phase lag is reduced from −175° to −134°. The values of gain margin and phase margin are 9.7 dB and 46°, respectively. Both of them have fit the specified requirements of the stability.

In most cases, the stability plays an important role in various performance indexes of a closed-loop system. For this resonant converter, the stability can be studied by analyzing the characteristics of the poles and zeros of the closed-loop system. Since the small-signal model has been found in the previous section, the state-space equations can be established from Equation 19.49, to give

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u}$$

and

$$\hat{y} = C\hat{x} + D\hat{u}$$

where

$$\hat{x} = \left(\hat{i}_{1s}, \hat{i}_{1c}, \hat{v}_{1s}, \hat{v}_{1c}, \hat{i}_{2s}, \hat{i}_{2c}, \hat{v}_{2s}, \hat{v}_{2c}, \hat{i}_{L_f}, \hat{v}_{C_f}\right)^T$$

$$\hat{u} = \left(\hat{v}, \hat{f}_{sN}, \hat{i}_o\right)^T \quad \hat{y} = \hat{v}_o$$

Based on the relationship between the state-space equation and transfer function, these equations of the open-loop system can be transformed to the transfer function $G_1(s)$, to give

$$G_1(s) = \frac{\hat{Y}(s)}{\hat{U}(s)} = C[sI - A]^{-1}B + D \tag{19.63}$$

By considering both the expression in Equation 19.51 and $G_1(s)$, the closed-loop control system transfer function can be obtained. Hence, the poles of the closed-loop control system are found to be

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$$p_{1,2} = -0.3138 \pm 19.3296i \qquad p_{3,4} = -0.8750 \pm 12.9716i$$
$$p_{5,6} = -0.8809 \pm 5.2819i \qquad p_{7,8} = -0.3914 \pm 0.9492i$$
$$p_{9,10} = -0.0071 \pm 0.0377i \qquad p_{11,12} = -0.7777 \pm 0.0000i$$
$$p_{13} = 0$$

Note that all the real parts of the poles are nonnegative; thus, the whole system is found stable. The root loci of the closed-loop system are given in Figure 19.22.

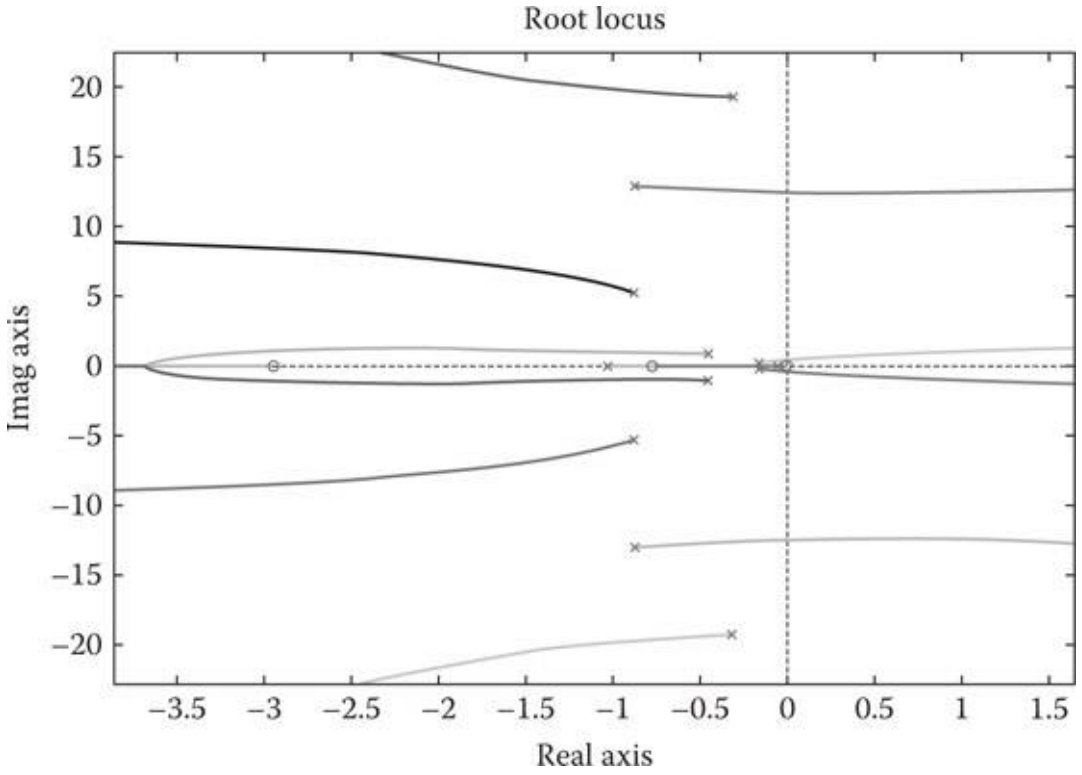


FIGURE 19.22
Root loci of the closed-loop system.

19.5 Discussion

In all the previous sections, the analyses are undertaken on the basis of the assumption that two resonant inductors are identical, as well as two resonant capacitors. The following discussion will be focused on the condition that the resonant components have different values, that is, variable parameters. In addition, the discontinuous operation, always occurring when switching frequency is lower than the natural resonant frequency, will also be taken into consideration.

19.5.1 Characteristics of Variable-Parameter Resonant Converter

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In fact, most of the derivation results and general conclusions in Sections 19.3 and 19.4 are still valid for the variable-parameter condition, except that the curves of the voltage transfer gain are a little bit different. For instance, if the ratios of two inductors and two capacitors are defined as

$$p = \frac{L_1}{L_2} \quad \text{and} \quad q = \frac{C_1}{C_2}$$

then the Equation 19.1 can be rewritten as

$$g(\omega) = \frac{R_{eq}}{\omega^4 p\beta L^2 C^2 R_{eq} - \omega^2 (pq + p + 1) LCR_{eq} + R_{eq} + j[\omega L(p+1) - \omega^3 L^2 Cpq]} \tag{19.64}$$

Following the same definitions of the natural resonant frequency ω_0, Q value, and relative frequency β, the voltage transfer gain $g(\beta)$ is given by

$$g(\beta) = \frac{1}{1 - \beta^2 (pq + p + 1) + \beta^4 pq + j[(p+1) - pq\beta^2]\beta Q} \tag{19.65}$$

and its determinant is

$$|g(\beta)| = \frac{1}{\sqrt{[1 - \beta^2 (pq + p + 1) + \beta^4 pq]^2 + [(p+1) - pq\beta^2]^2 \beta^2 Q^2}} \tag{19.66}$$

The local maximum and minimum values of the voltage gain $g(\beta)$ can be gained by solving the resulting equation after setting the derivatives of the determinant to zero:

$$\frac{d}{d\beta^2} |g(\beta)| = 0 \tag{19.67}$$

$$\begin{aligned} &4p^2 q^2 \beta^6 + [3p^2 q^2 Q^2 - 6pq(pq + p + 1)]\beta^4 \\ &+ [4pq + 2(pq + p + 1)^2 - 4pq(p+1)Q^2]\beta^2 \\ &+ Q^2 (p+1)^2 - 2(pq + p + 1) = 0 \end{aligned} \tag{19.68}$$

When $p = q = 1$, this equation is simplified to be

$$4\beta^6 + (3Q^2 - 18)\beta^4 + (22 - 8Q^2)\beta^2 + 4Q^2 - 6 = 0$$

which is the same as Equation 19.21.

Figure 19.23a, b, c and d depicts the voltage gain $|g(\beta)|$ with different parameter ratios referring to various Q values. One can find that all the curves have the similar shapes in Figure 19.4, which begins with unity at low switching frequency and displays two peaks with lower Q values. However, the different parameter ratio results in a different bandwidth. Thus, the designer will have more choices to find the most appropriate bandwidth to meet the requirements of various applications. Besides this, with certain parameter ratios (e.g., $p = 2$, $q = 1$), all the curves intersect at one point, which is independent of the Q values. The

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corresponding switching frequency can be calculated by setting the imaginary part of the denominator in Equation 19.65 to zero, which gives

$$p+1=pq\tilde{\beta}^2$$

or

$$\tilde{\beta}^2=\frac{p+1}{pq} \tag{19.69}$$

Substituting Equation 19.69 into Equation 19.65, the voltage gain at this frequency is obtained as

$$\left|g(\tilde{\beta})\right|=\frac{1}{p} \tag{19.70}$$

Hence, the voltage transfer gain is only dependent on the inductors ratio a and it determines the rough shape of the gain curve over a wide frequency range [$0\sim\tilde{\beta}$], which is useful for the designer to estimate the needed operating point.

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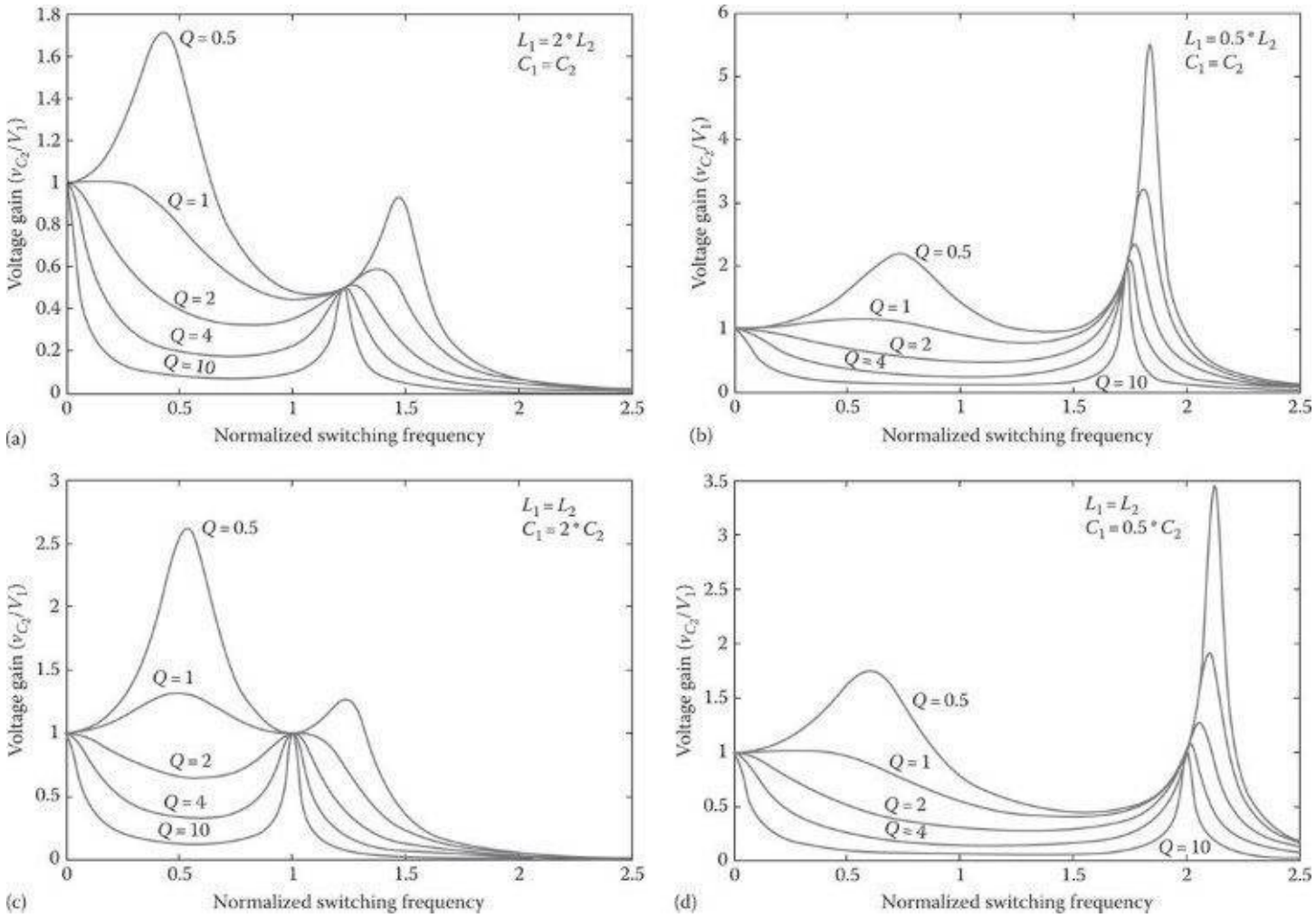


FIGURE 19.23
Voltage gain $|g(\beta)|$ with different parameter ratios referring to various Q. (a) $L_1 = 2L_2$ and $C_1 = C_2$. (b) $L_1 = 0.5L_2$ and $C_1 = C_2$. (c) $L_1 = L_2$ and $C_1 = 2C_2$. (d) $L_1 = L_2$ and $C_1 = 0.5C_2$.

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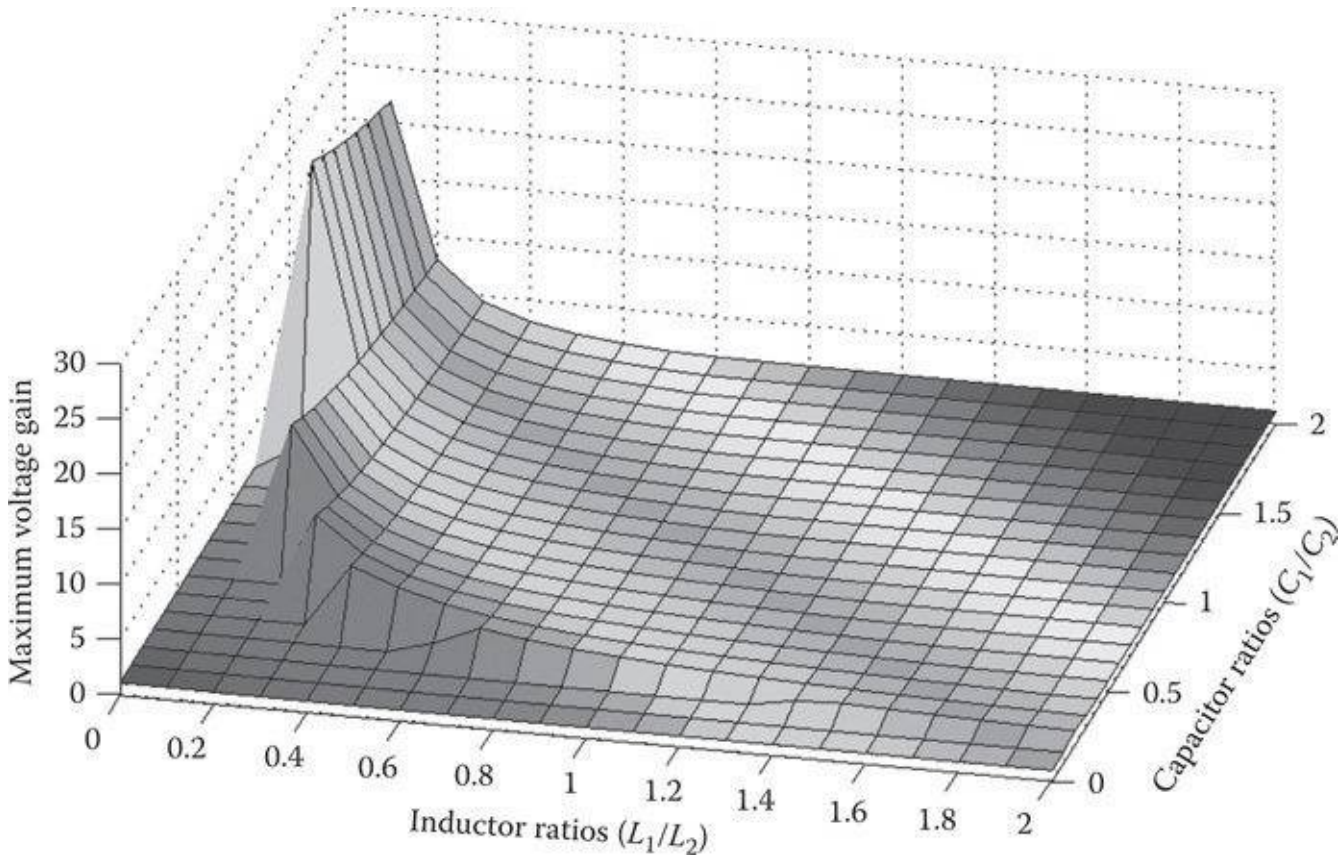


FIGURE 19.24
Maximum voltage gain versus different parameter ratios of p and q.

Figure 19.24 gives the maximum voltage transfer gain versus different parameter ratios of p and q, corresponding to the peak value in Figure 19.23a, b, c and d. Note that the maximum gain is obtained with small p and large q. This is true because when L_1 is much smaller than L_2, while C_1 is larger than C_2, the cascade reverse double Γ-LC RPC will be degraded to the conventional parallel resonant converter, which voltage gain is prominent near the natural resonant frequency. Figure 19.24 shows the three-dimensional relations.

The dynamic analysis of the variable-parameter resonant converter is similar to that in the previous section, except that some relevant matrices need to be amended. The waveforms of the input and the resonant voltage are shown in Figure 19.25a, where some distortions can be found in the second capacitor voltage v_{C_2}. Figure 19.25b is the probe output of the commonly used circuit simulation software PSpice. From this, one can find a good accordance between the two figures.

The comparison of the resonant output voltage and THD of the variable-parameter resonant converter is given in Table 19.1. The comparison of output voltage and THD among different resonant converters is given in Table 19.2. Compared to other conditions, the second capacitor voltage obtains the highest amplitude when $L_1 = L_2$, $C_1 = C_2$, while it keeps the lowest THD value. Thus, it is reasonable to implement the practical cascade reverse double Γ-LC RPC with dual symmetric resonant network.

19.5.2 DCM

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When the switching frequency is lower than half of the natural resonant frequency, the current through the inductors and the voltage across the capacitors will become discontinuous. For the cascade reverse double Γ-LC PRC, in discontinuous conduction mode (DCM) operation, the energy in the resonant capacitor is consumed before the new half of a switching cycle. There are six stages of operation in one switching cycle, as shown in Figure 19.26. Suppose before the beginning of a switching cycle, the second inductor current i_{L_2} is zero.

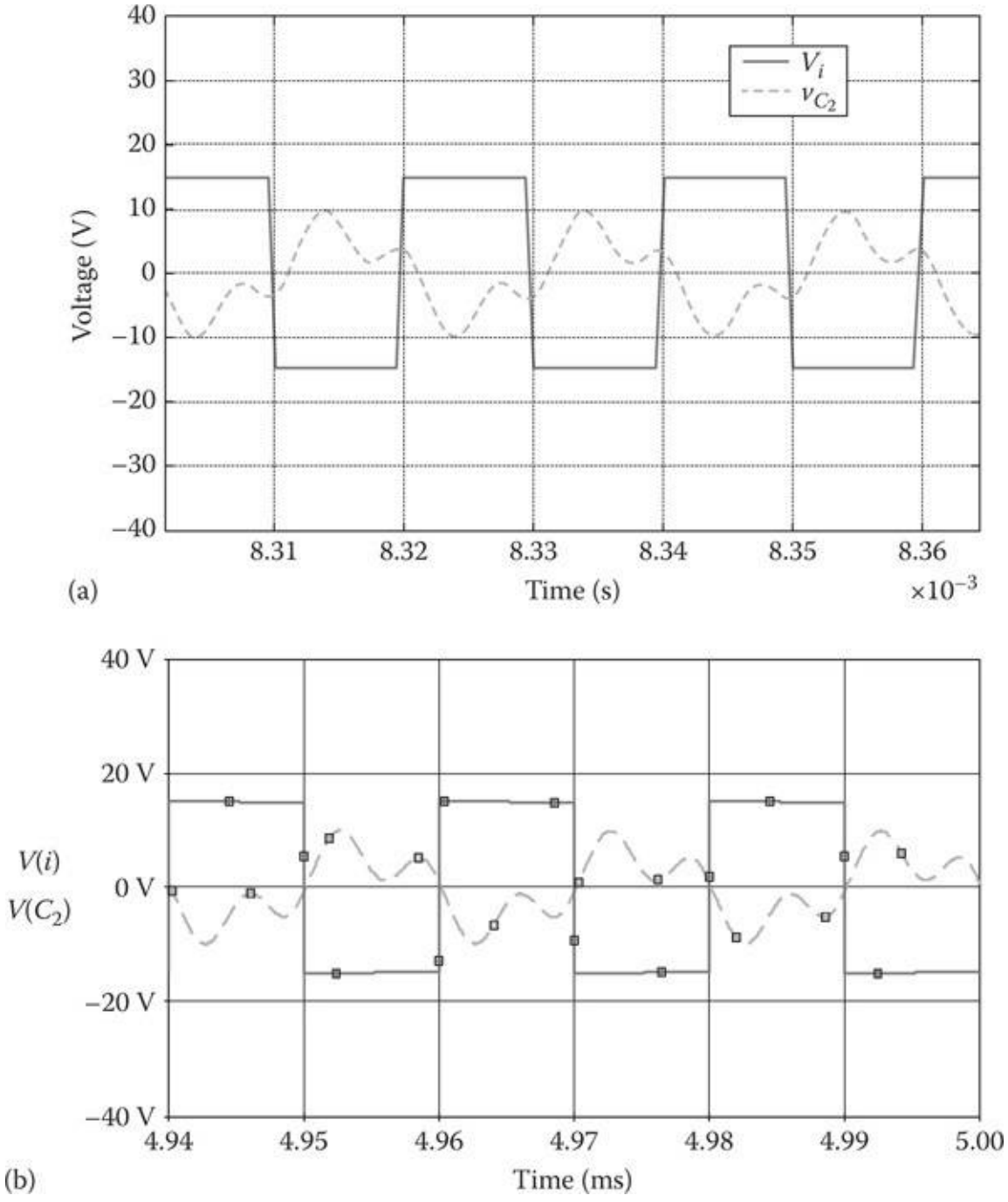


FIGURE 19.25
Simulation waveforms using MATLAB® (a) and PSpice (b) when $L_1 = 10L_2$.

TABLE 19.1
Comparison of Output Resonant Voltage and Total Harmonic Distortion Values under Different Parameter Ratios

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		Switching Frequency f_s = 50 kHz	
$\alpha(L_1/L_2)$	$\beta(C_1/C_2)$	V_{C_2} Amplitude (V)	THD (%)
1	1	23.5	2.41
2	1	11.0	7.90
0.5	1	17.0	6.84
1	2	6.0	5.82
1	0.5	8.0	5.93
2	2	3.5	2.72
0.5	0.5	10.0	7.14
0.5	2	19.0	8.55
2	0.5	6.0	3.91

Note: With L_2 = 100 μH, C_2 = 0.22 μF, R = 22 Ω, L_f = 2.4 mH, and C_f = 220 μF.

TABLE 19.2
Comparison of Output Voltage and Total Harmonic Distortion among Different Resonant Converters

			Harmonic Statistics			Harmonic Proportion (%)		
Converter	THD (%)	V_o (V)	First	Third	Fifth	First	Third	Fifth
SRC	3.355	7.88	16.50	3.042	3.663	100	18.4	22.2
RPC	4.254	6.09	12.18	0.419	0.261	100	3.44	2.14
SRPC	4.341	15.9	59.87	2.485	0.625	100	4.15	1.04
CRD Γ-LC	2.407	12.0	23.29	0.517	0.179	100	2.22	0.77
V_i	—	—	18.83	6.366	3.820	100	33.8	18.5

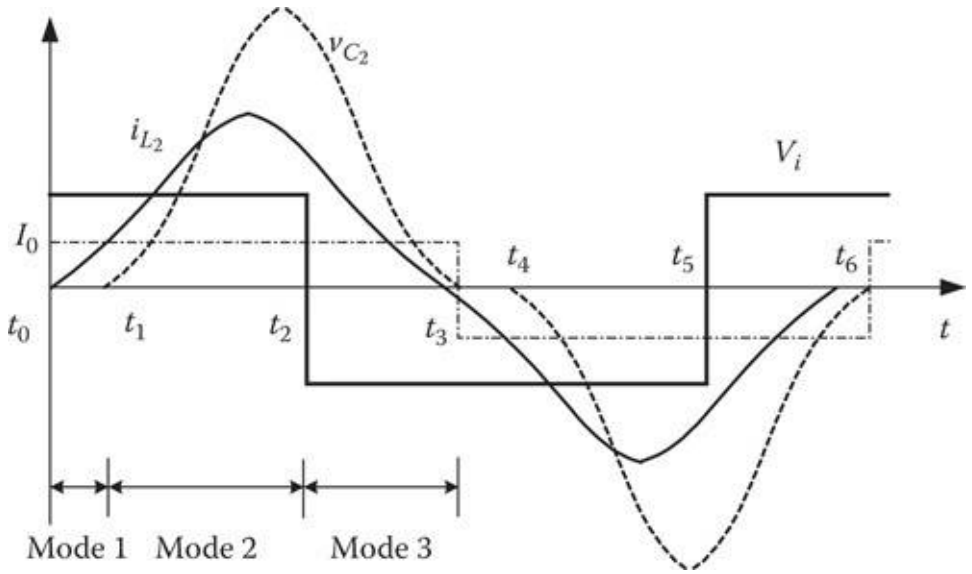


FIGURE 19.26
Switching waveforms for the discontinuous-mode cascade reverse double Γ-LC resonant power converter.

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When stage 1 begins at time t_0, since i_{L_2} is lower than the constant-current-sink I_o, all the rectifier diodes become forward biased and conduct. The second capacitor C_2 is clamped to zero volts by the freewheeling action, which is shown in Figure 19.27a. Thus, the second inductor L_2 is charged and the current though it is increased. Stage 2 commences when the current i_{L_2} reaches the magnitude of the current-sink I_0, at time t_1. The topology at this moment is the same as that in CCM operation. Stage 3 starts when the input voltage source V_i changes its polarity at time t_2, as depicted in Figure 19.27c. This completes the first half-cycle of operation. The next half-cycle operation repeats the same way as the first half-cycle, except that the direction of the inductor current i_{L_2} and the polarity of the capacitor voltage v_{C_2} are reversed.

The state coefficient matrix and input source vector corresponding to two additional operating modes are given by

$$A_5 = \begin{bmatrix} 0 & 0 & -1/L_1 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 & 0 & 0 \\ 1/C_1 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1/L_f \\ 0 & 0 & 0 & 0 & 1/C_f & -1/RC_f \end{bmatrix}$$

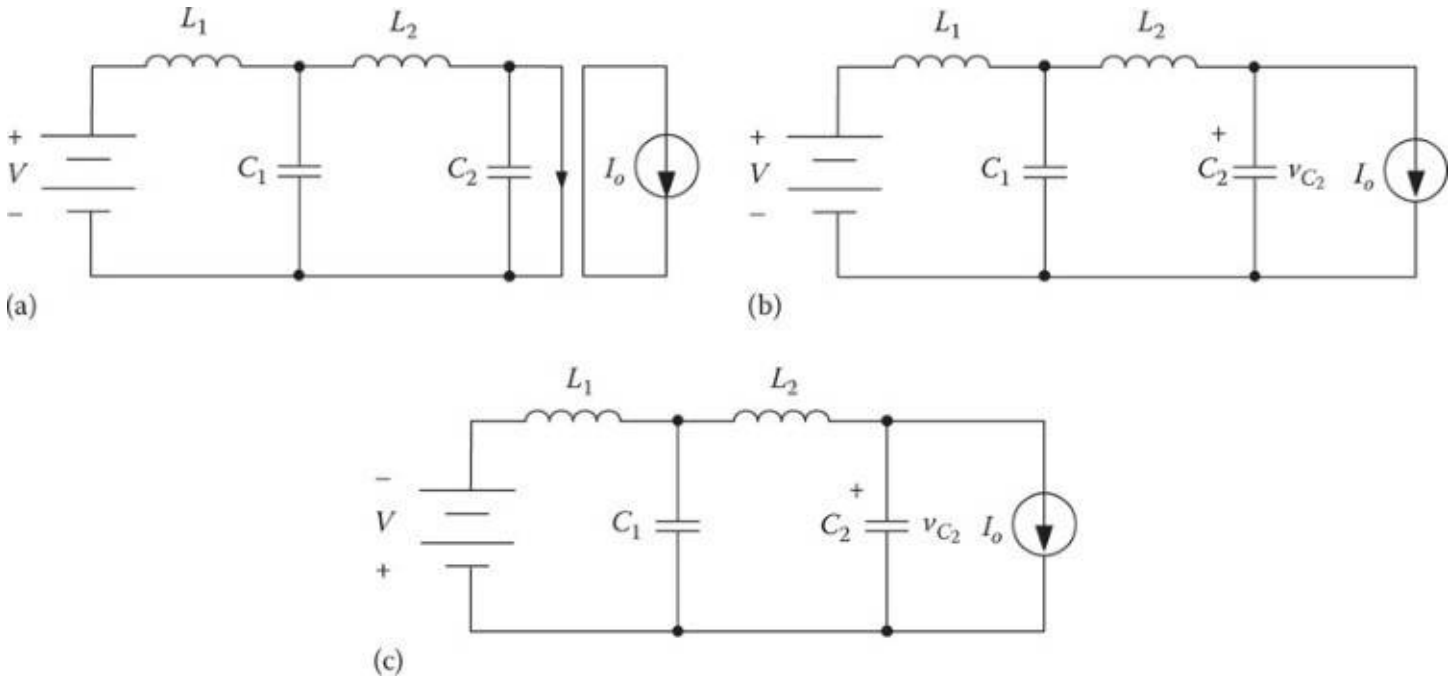


FIGURE 19.27
Discontinuous-mode equivalent circuits in half-cycle. (a) General equivalent circuit. (b) Positive half-cycle equivalent circuit. (c) Negative half-cycle equivalent circuit.

$$B_5 = \begin{bmatrix} V/L_1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

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and

$$A_6 = A_5, \quad B_6 = \begin{bmatrix} -V/L_1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T$$

The augmented state-space equation in Section 19.4 is still valid besides that the state transition matrices describing two additional operating modes should be considered as well. The waveforms of simulation and experimental results under DCM operation are shown in Figure 19.28. Note that the second capacitor voltage is discontinuous at some intervals, which verifies the description of the theoretical analysis.

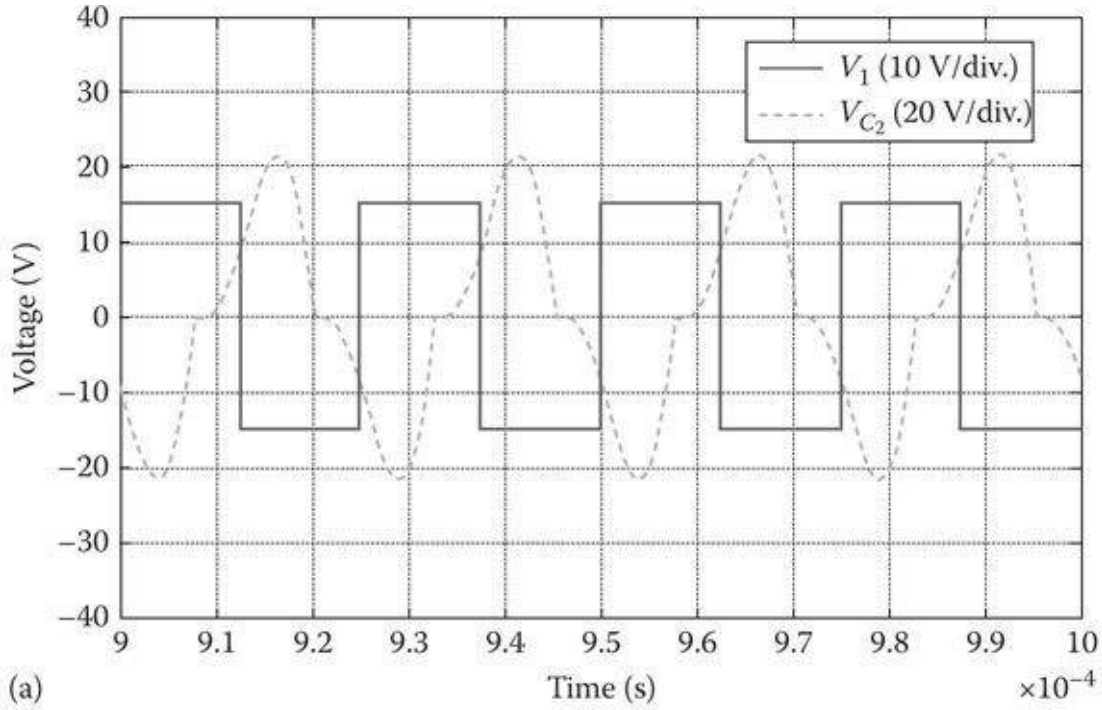
In practice, the DCM is often dependent on the switching frequency and the equivalent load current I_0. Namely, under a certain load current, when the switching frequency is increased, the operating state of the resonant converter will transfer from DCM to CCM. Conversely, if the switching frequency is invariant, the increase of the load current will lead to the occurrence of DCM. Thus, it is very significant to find the relationship between the load current and the switching frequency, in other words, to find the critical load current J_{cr} under a certain frequency.

In many open literatures, the critical load current is always obtained by solving the differential equations and identifying the respective duration of various subintervals. For instance, the normalized critical load current of RPC is given as

$$J_{cr} = \sqrt{\sin^2\left(\frac{\gamma}{2}\right) + \sin^2\left(\frac{\gamma}{4}\right)} - \sin\left(\frac{\gamma}{2}\right) \tag{19.71}$$

This conclusion is very simple and straightforward to describe the relationship between f_s and I_0. However, it is acquired at the cost of very complicated calculations and derivations. For sinusoidal resonant power converter (SRPC), there is no similar analytical expression given in the literature. In fact, with the increase of the quantity of the resonant components, the order of the differential equations becomes very large so that it seems impossible to solve them by pen and paper. Once again, the numerical calculation offers a very useful solution to overcome such a problem.

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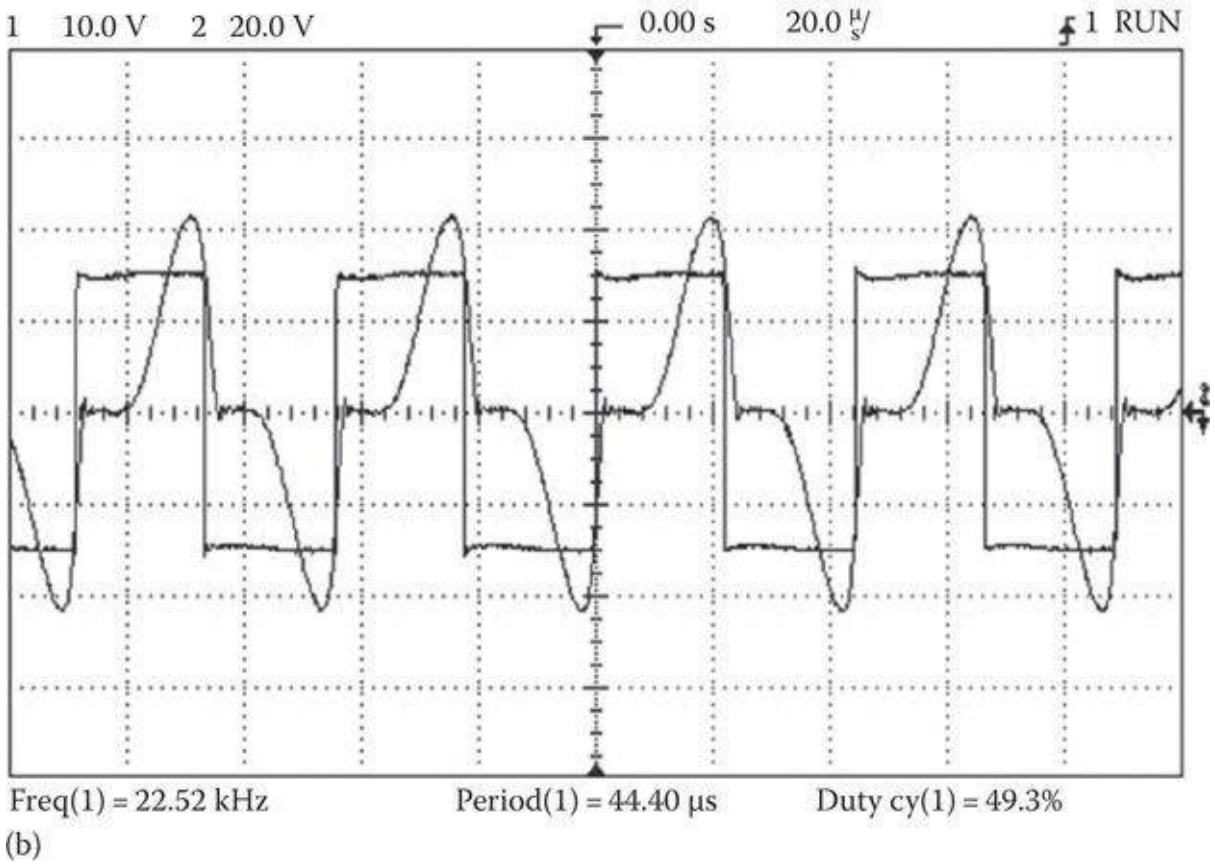


FIGURE 19.28
(a) Simulation and (b) experimental switching waveforms for discontinuous conduction mode operation.

The numerical analysis method starts at solving the higher-order state equations using recursion algorithm. Once the steady state is achieved, the algorithm judges whether the

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critical load current is found correctly. The drawbacks of this method are in two aspects: one is the discrete result; the other is time consuming. However, the obtained results are proved to be precise and useful so long as the step of the loop is small enough. The critical load resistor and critical load current versus the switching frequency are shown in Figures 19.29 and 19.30, respectively.

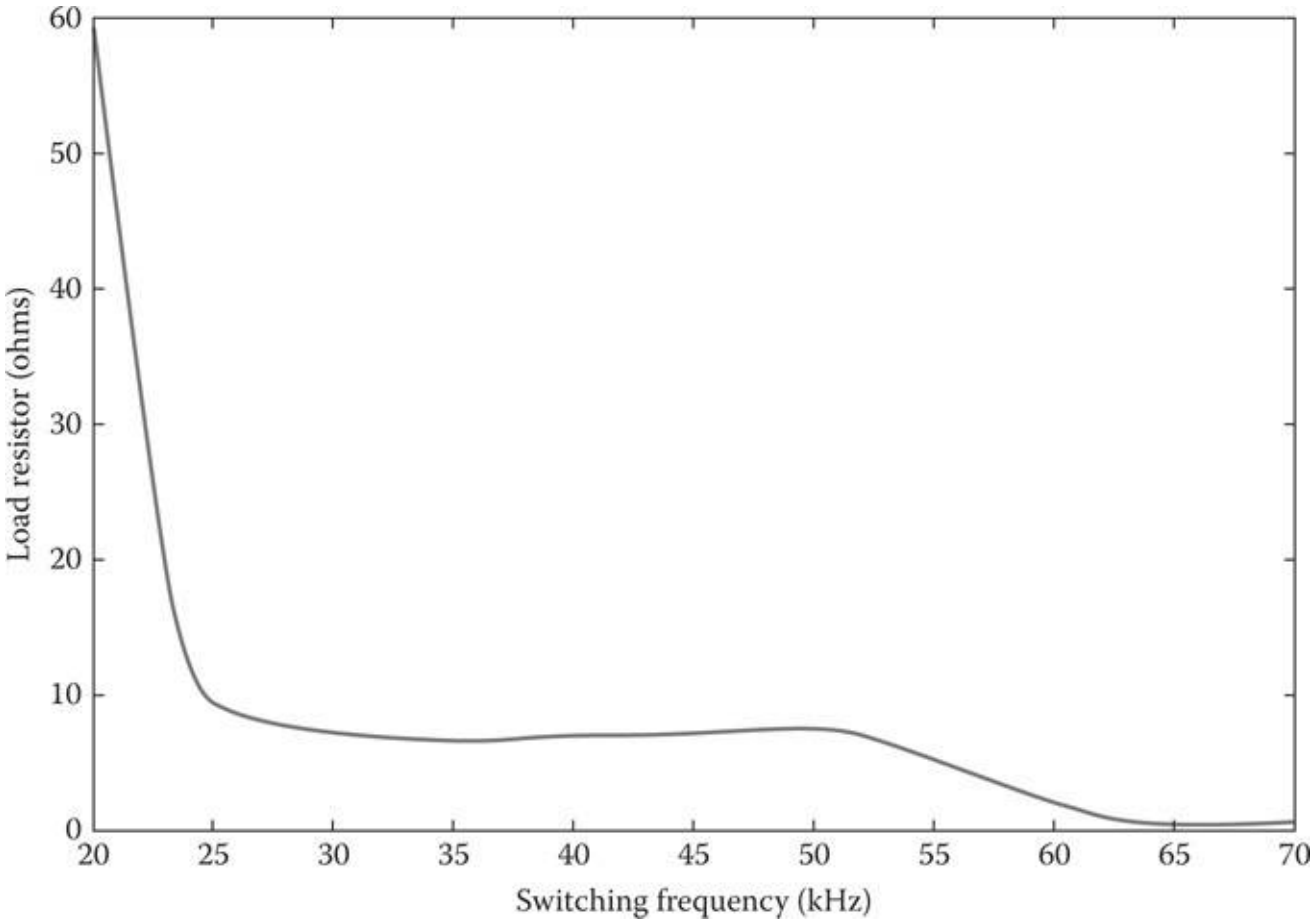


FIGURE 19.29
Critical load resistor versus frequency.

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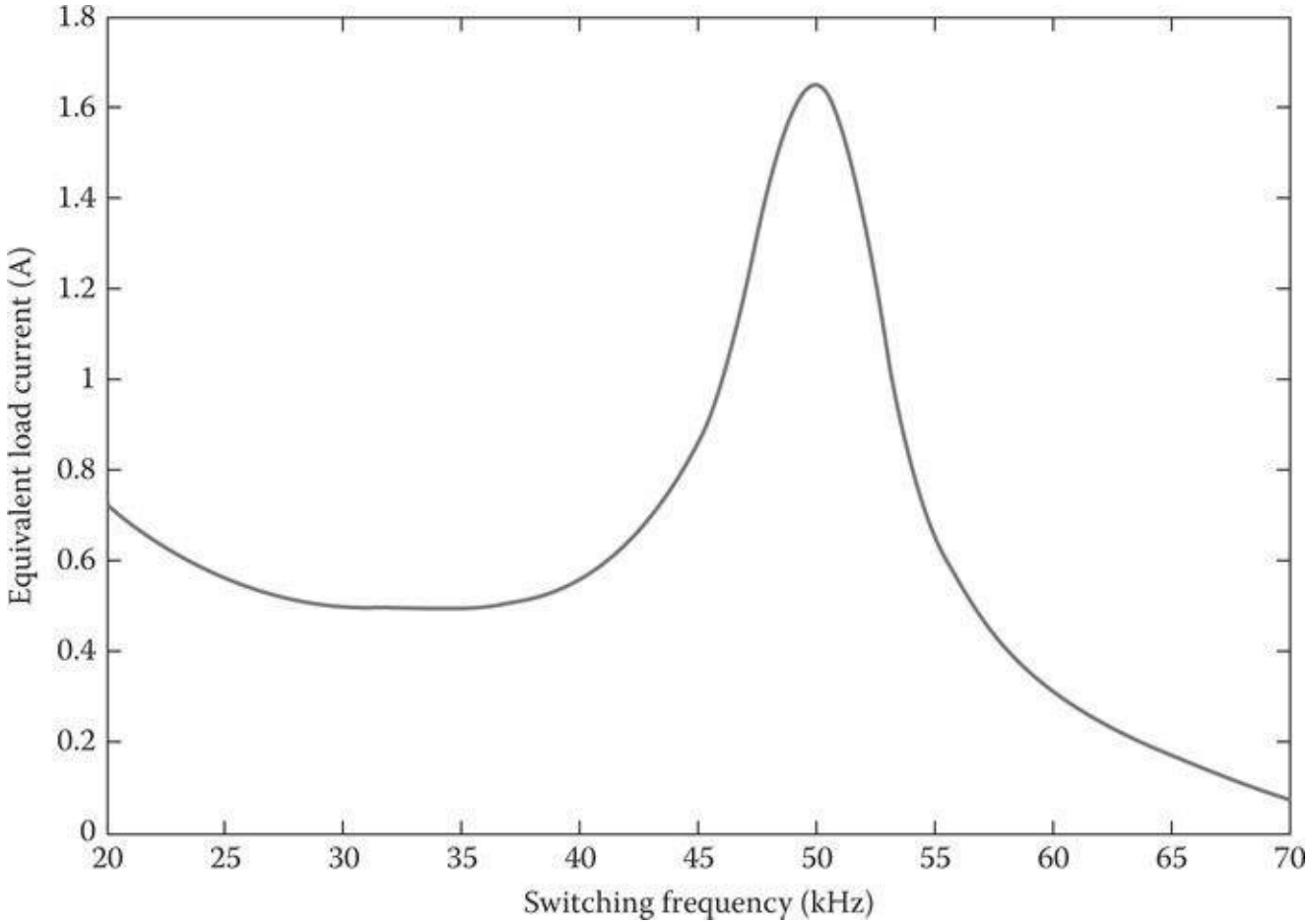


FIGURE 19.30
Critical load current versus frequency.

Appendix: Parameters Used in Small-Signal Modeling

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$$k_v = \frac{4}{\pi}$$

$$k_s = \frac{2}{\pi}\frac{V_{2s}}{A_p}$$

$$k_c = \frac{2}{\pi}\frac{V_{2c}}{A_p}$$

$$Z_{L_1} = \Omega_s L_1$$

$$Z_{L_2} = \Omega_s L_2$$

$$G_s = \Omega_s C_1$$

$$E_{1s} = \omega_0 L_1 I_{1c}$$

$$E_{1c} = \omega_0 L_1 I_{1s}$$

$$E_{2s} = \omega_0 L_2 I_{2c}$$

$$E_{2c} = \omega_0 L_2 I_{2s}$$

$$J_{1s} = \omega_0 C_1 V_{1c}$$

$$J_{1c} = \omega_0 C_1 V_{1s}$$

$$J_{2s} = \omega_0 C_2 V_{2c}$$

$$J_{2c} = -\omega_0 C_2 V_{2s}$$

$$g_{ss} = \frac{g_e \alpha^2}{\alpha^2 + \beta^2}$$

$$g_{cc} = \frac{g_e \beta^2}{\alpha^2 + \beta^2}$$

$$g_{sc} = \Omega_s C_2 + \frac{\alpha\beta}{\alpha^2 + \beta^2}$$

$$g_{cs} = -\Omega_s C_2 + \frac{\alpha\beta}{\alpha^2 + \beta^2}$$

$$V_e = \frac{4}{\pi} V_g$$

$$g_e = \frac{8}{\pi^2 R}$$

$$A_p = \frac{1}{\sqrt{\alpha^2 + \beta^2}} V_e$$

$$\alpha = g_e \Omega_s L \left(\Omega_s^2 LC - 2 \right)$$

$$\beta = \Omega_s^4 L^2 C^2 - 3\Omega_s^2 LC + 1$$

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DC Energy Sources for DC/DC Converters

The DC/DC converter is used to convert a DC source voltage to another DC voltage actuator (user). In a DC/DC converter system, the main parts are the DC voltage source, switches, diodes, inductors/capacitors, and load. This chapter introduces the various DC energy sources that are usually employed in DC/DC converters.

20.1 Introduction

In a DC/DC converter system, the initial energy source is a DC voltage source with certain voltage and very low internal impedance, which can be usually omitted. This means the used DC voltage source is ideal. The DC voltage source can be a battery, a DC bus (usually equipped in factories and laboratories), a DC generator, and an AC/DC rectifier. As is well known, the battery, DC bus, and DC generator can be considered an ideal voltage source. They will be not discussed in this book. AC/DC rectifiers are widely applied in industrial applications and research centers since it is easily constructed and less costly. In this chapter, the AC/DC rectifiers will be discussed in detail. AC/DC rectifiers can be grouped as follows:

- Single-phase half-wave diode rectifier
- Single-phase full-wave bridge diode rectifier
- Three-phase bridge diode rectifier
- Single-phase half-wave thyristor rectifier
- Single-phase full-wave bridge thyristor rectifier
- Three-phase bridge thyristor rectifier
- Other device rectifiers

20.2 Single-Phase Half-Wave Diode Rectifier

The single-phase half-wave diode rectifier is shown in Figure 20.1; it is the simplest rectifier circuit. The load Z in the figure can be any type such as resistor, inductor, capacitor, back electromotive force (EMF), and/or a combination of these. This rectifier can rectify the AC input voltage into DC output voltage. The analysis of the circuit is based on the assumption that a diode as an ideal component is used for the rectification. A diode forward biased will conduct without forward voltage drop and resistance. A diode reverse biased will be blocked, and likely an open circuit. Since the used diode is not continuously conducted, the output current is always discontinuous in some part of negative half-cycle.

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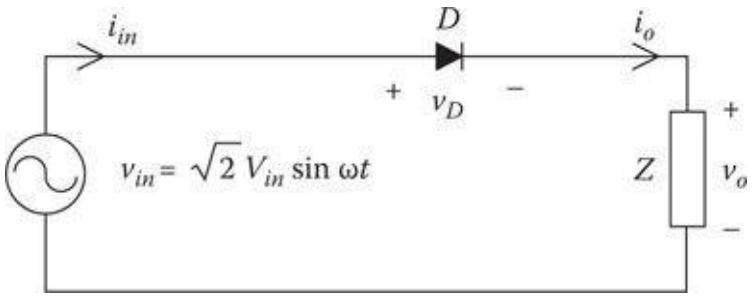


FIGURE 20.1
Half-wave diode rectifier.

20.2.1 Resistive Load

A single-phase half-wave rectifier with a purely resistive load (R) is shown in Figure 20.2a, and its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.2b and c.

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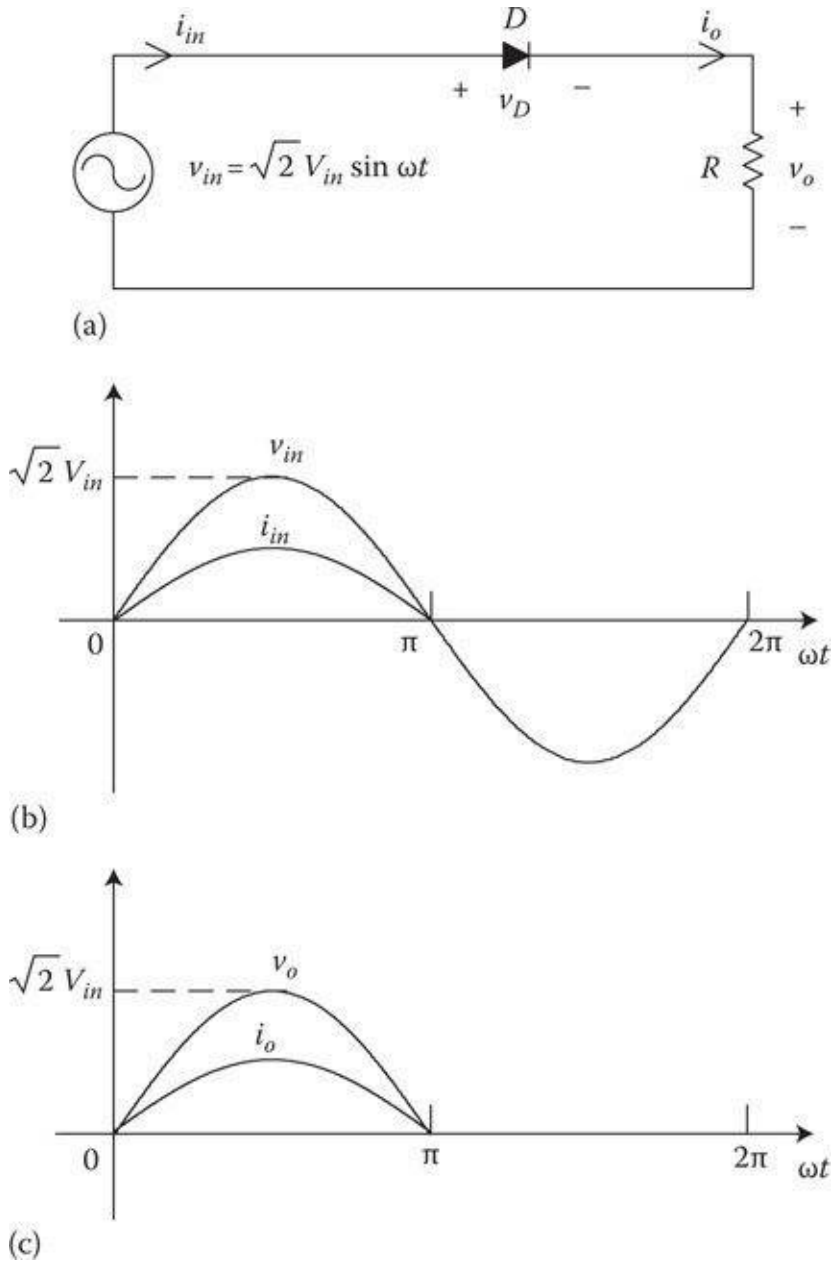


FIGURE 20.2
A single-phase half-wave rectifier with a purely resistive load (R). (a) Circuit diagram. (b) Input voltage and current. (c) Output voltage and current.

The AC supply voltage v_{in} is sinusoidal; the output voltage and current obey Ohm's law. Therefore, the output voltage and current are sinusoidal half-waveforms:

$$v_{in}(t) = \sqrt{2} V_{in} \sin \omega t \tag{20.1}$$

$$v_o(t) = \begin{cases} \sqrt{2} V_{in} \sin \omega t & 0 \le \omega t \le \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \tag{20.2}$$

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$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{R}\sin\omega t & 0 \le \omega t \le \pi \\ 0 & \pi < \omega t < 2\pi \end{cases} \tag{20.3}$$

where V_{in} is the root-mean-square (rms) value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a half-wave of a sinusoidal waveform for both voltage and current without angle shift between the voltage and the current. The output DC average voltage and current are

$$V_{o-av} = \frac{\sqrt{2}}{\pi}V_{in} = 0.45V_{in} \tag{20.4}$$

$$I_{o-av} = 0.45\frac{V_{in}}{R} \tag{20.5}$$

20.2.2 Single-Phase Half-Wave Rectifier with a Capacitive Filter

The single-phase half-wave rectifier in Figure 20.3 has a parallel *R-C* load. The purpose of the capacitor is to reduce the variation in the output voltage, making it more like a pure DC voltage.

Assuming the rectifier works in the steady state, the capacitor is initially charged to a certain DC voltage and the circuit is energized at $\omega t = 0$; the diode becomes forward biased at the angle $\omega t = \alpha$ as the source becomes positive. When the source decreases after $\omega t = \pi/2$, the capacitor discharges from the discharging angle θ into the load resistor. From this point, the voltage of the source becomes less than the output voltage, reversely biasing the diode and isolating the load from the source. The output voltage is a decaying exponential with time constant *RC* while the diode is switched off.

The output voltage is described by

$$v_d(\omega t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \textit{diode on} \\ V_\theta e^{-(\omega t-\theta)/\omega RC} & \textit{diode off} \end{cases} \tag{20.6}$$

where

$$V_\theta = \sqrt{2}V_{in}\sin\theta \tag{20.7}$$

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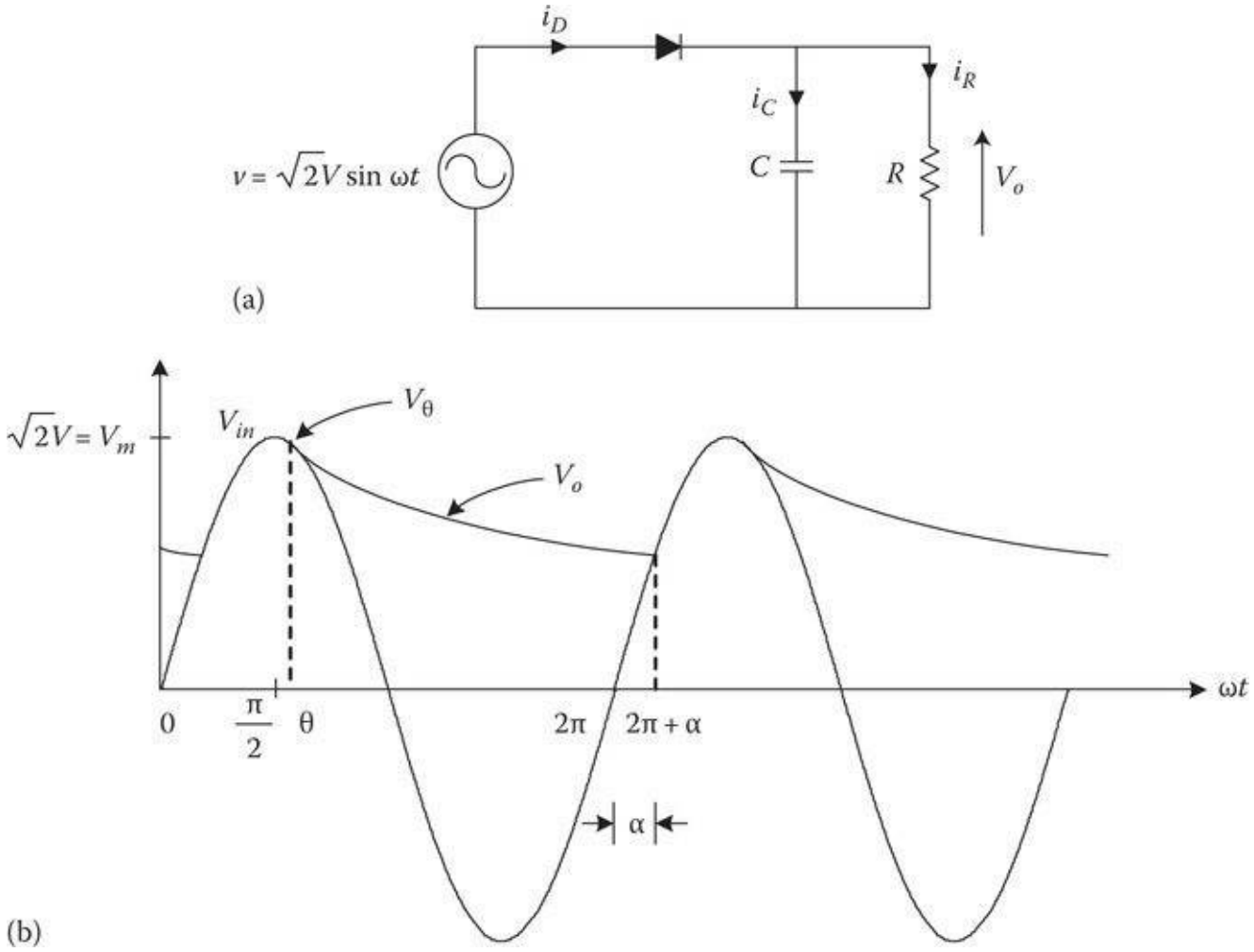


FIGURE 20.3
A single-phase half-wave rectifier with a purely resistive load ($R + C$). (a) Circuit diagram. (b) Input and output voltages.

At $\omega t = \theta$, the slopes of the voltage functions are equal to

$$\sqrt{2}V_{in}\cos\theta = \frac{\sqrt{2}V_{in}\sin\theta}{-\omega RC}e^{-(\theta-\theta)/\omega RC}$$

$$\text{Hence,} \quad \frac{1}{\tan\theta} = \frac{-1}{\omega RC} \tag{20.8}$$

$$\text{Thus,} \quad \theta = \pi - \tan^{-1}(\omega RC)$$

Note: The discharging angle θ must be > π/2. (*Historic mistake in the literature:* θ = π/2.)

The angle at which the diode turns on in the second period, $\omega t = 2\pi + \alpha$, is the point at which the sinusoidal source reaches the same value as the decaying exponential output.

$$\sqrt{2}V_{in}\sin(2\pi+\alpha) = (\sqrt{2}V_{in}\sin\theta)e^{-(2\pi+\alpha-\theta)/\omega RC}$$

or

$$\sin\alpha - (\sin\theta)e^{-(2\pi+\alpha-\theta)/\omega RC} = 0 \tag{20.9}$$

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The preceding equation must be solved numerically as follows.

Peak capacitor current occurs when the diode turns on at $\omega t = 2\pi + \alpha$:

$$i_{C-peak} = \omega C\sqrt{2}V_{in}\cos(2\pi+\alpha) = \omega C\sqrt{2}V_{in}\cos\alpha \tag{20.10}$$

Note: The capacitor peak current locates at $\omega t = \alpha$, which is usually much smaller than $\pi/2$. (*Historic mistake in literature:* $\alpha \approx \pi/2$.)

The resistor current $i_R(t)$ is

$$i_R(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{R}\sin\omega t & \textit{diode on} \\ \dfrac{V_\theta}{R}e^{-(\omega t-\theta)/\omega RC} & \textit{diode off} \end{cases}$$

where

$$V_\theta = \sqrt{2}V_{in}\sin\theta$$

Its peak current at $\omega t = \pi/2$ is

$$i_{R-peak} = \frac{\sqrt{2}V_{in}}{R} \quad \omega t = \frac{\pi}{2}$$

Its current at $\omega t = 2\pi + \alpha$ (and $\omega t = \alpha$) is

$$i_R(2\pi+\alpha) = \frac{\sqrt{2}V_{in}}{R}\sin(2\pi+\alpha) = \frac{\sqrt{2}V_{in}}{R}\sin\alpha \tag{20.11}$$

Usually, the capacitive reactance is smaller than the resistance R; the main component of the source current is capacitor current. Therefore, the peak diode (source) current is

$$i_{D-peak} = \omega C\sqrt{2}V_{in}\cos\alpha + \frac{\sqrt{2}V_{in}}{R}\sin\alpha \tag{20.12}$$

Advice: The source peak current locates at $\omega t = \alpha$, which is usually much smaller than $\pi/2$. (*Historic mistake in literature:* The source peak current locates at $\omega t = \pi/2$.)

The peak-to-peak ripple of the output voltage is given by

$$\Delta V_d = \sqrt{2}V - \sqrt{2}V\sin\alpha = \sqrt{2}V(1-\sin\alpha) \tag{20.13}$$

Example

A single-phase half-wave diode rectifier shown in Figure 20.3a operates from a supply of V_{in} = 240 V, 50 Hz, to a load of R = 100 Ω. and C = 100μF in parallel. If α = 12.63°, determine the peak capacitor current and peak source current.

Solution:

From Equation 20.10, the peak capacitor current at $\omega t = \alpha$ is

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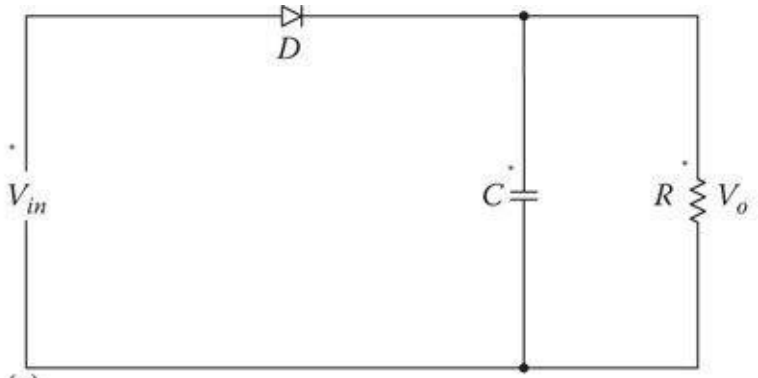
$$i_{C-peak} = \omega C\sqrt{2}V\cos\alpha = 100\pi * 0.0001 * 240 * \sqrt{2} * \cos 12.63^{\circ} = 10.4 \text{ A}$$

From Equation 20.12, the peak source current at $\omega t = \alpha$ is

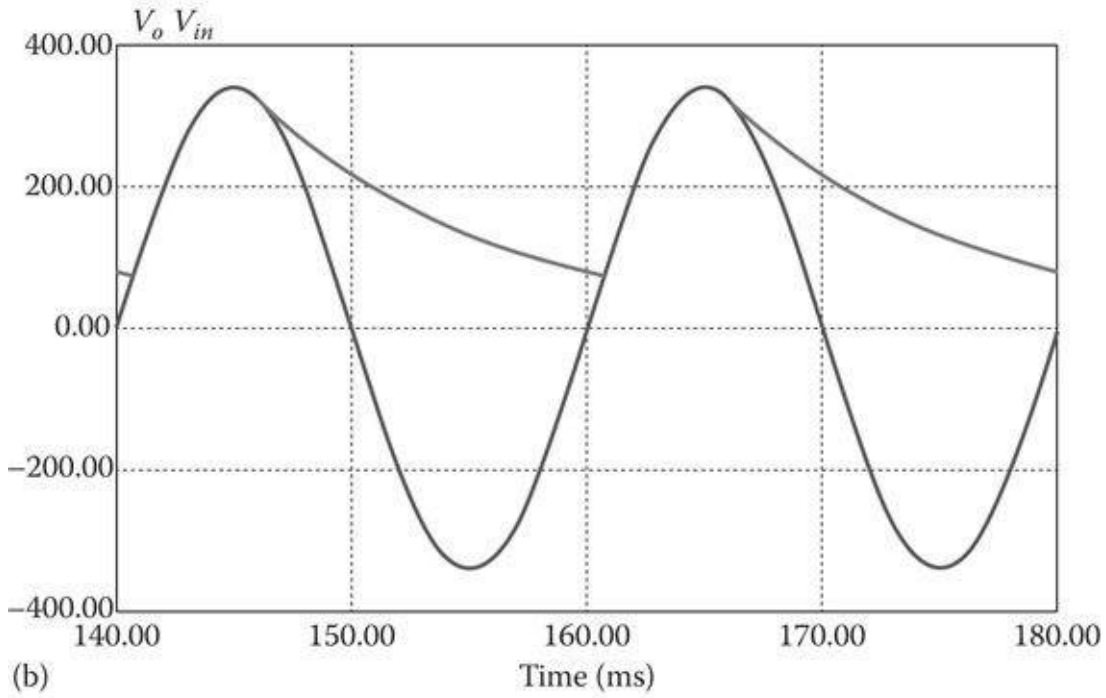
$$i_{D-peak} = \omega C\sqrt{2}V\cos\alpha + \frac{\sqrt{2}V}{R}\sin\alpha = 10.4 + \frac{240\sqrt{2}}{100}\sin 12.63^{\circ} = 11.14 \text{ A}$$

In order to help readers understand the current waveforms, the simulation results are presented in Figure 20.4 for reference: V_{in} = 340 V/50 Hz, C = 100 μF, and R = 100 Ω.

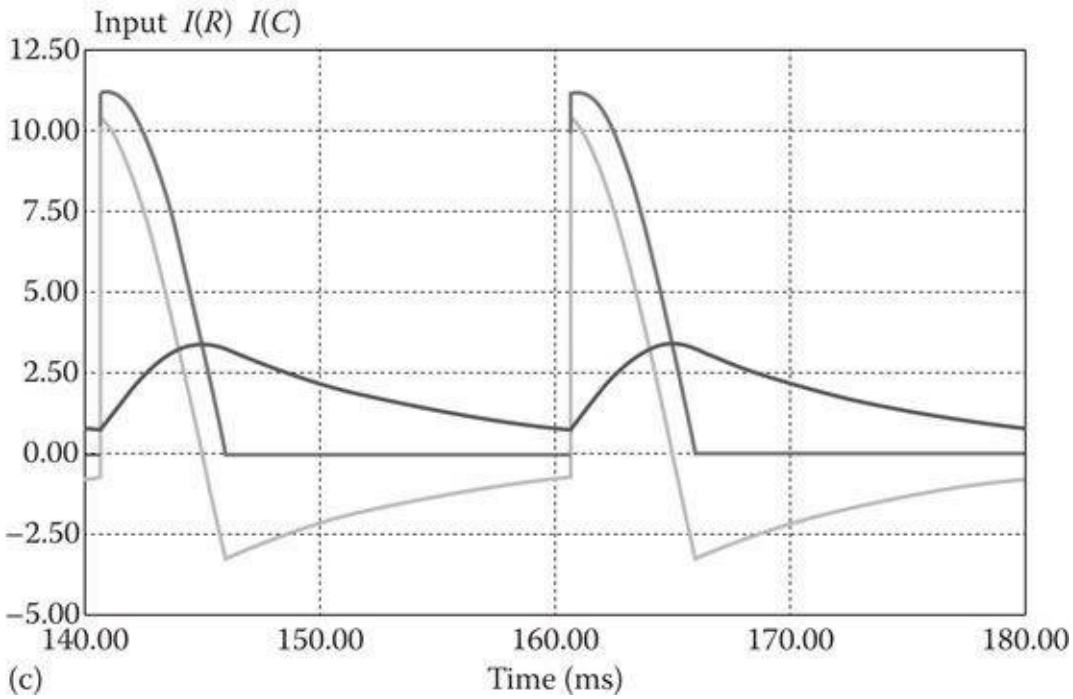
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(a)



(b)



(c)

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FIGURE 20.4
Simulation results: (a) Circuit diagram. (b) Input and output voltages. (c) Input, capacitor, and resistor current.

20.2.3 Inductive Load

A single-phase half-wave rectifier with an inductive load (a resistor R plus an inductor L) is shown in Figure 20.5a.

The input voltage and current v_{in} and i_{in} waveforms are shown in Figure 20.5b, the output voltage v_o in Figure 20.5c, and the output current i_o in Figure 20.5d. The AC supply voltage is sinusoidal; the output voltage and current obey Ohm's law. The impedance of the load is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & 0 \le \omega t \le (\pi + \phi) \\ 0 & (\pi + \phi) < \omega t < 2\pi \end{cases} \tag{20.14}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform more than a half-cycle. Since it is a negative value in the negative half-cycle, the output DC average voltage is

$$V_{o-av} = \frac{\sqrt{2}}{\pi}(1 - \cos\phi)V_{in} = 0.45(1 - \cos\phi)V_{in} \tag{20.15}$$

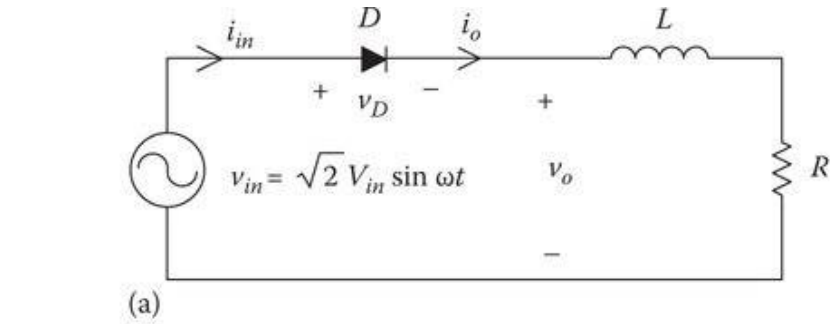
The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{|Z|}[\sin(\omega t - \phi) + \sin\phi \cdot e^{-t/\tau}] & 0 \le \omega t \le (\pi + \phi) \\ 0 & (\pi + \phi) < \omega t < 2\pi \end{cases} \tag{20.16}$$

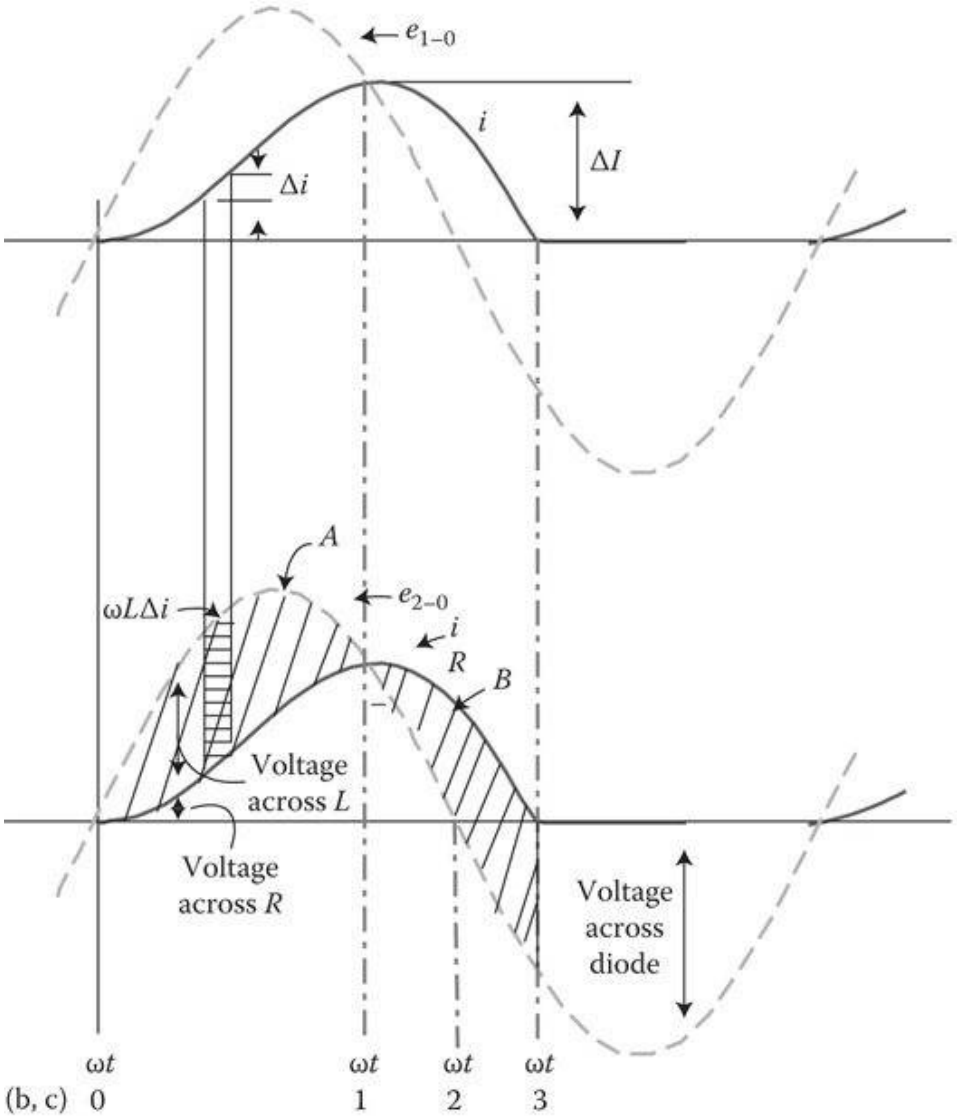
where the load time constant is $\tau = L/R$. The input and output current average value is

$$I_{o-av} = 0.45\frac{V_{in}}{R}(1 - \cos\phi) \tag{20.17}$$

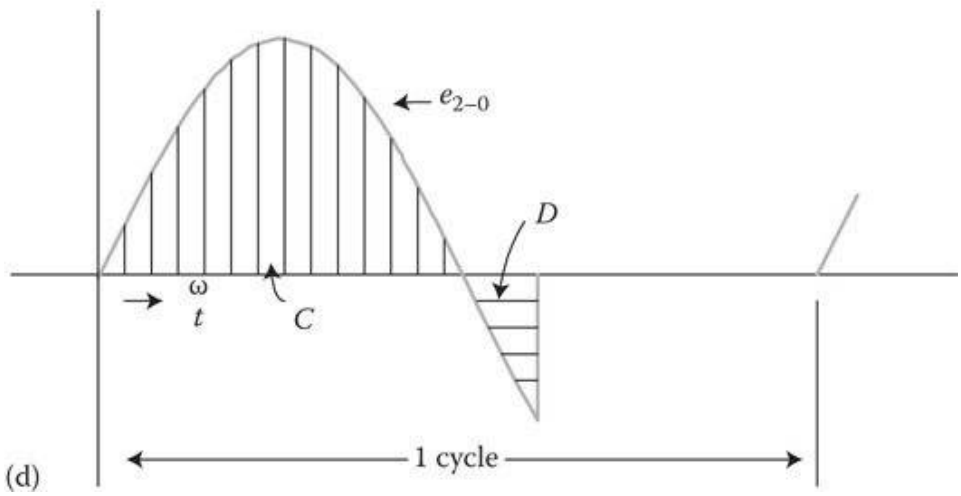
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(a)



(b, c)



(d)

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FIGURE 20.5
A single-phase half-wave rectifier with an inductive load ($R + L$). (a) Circuit diagram. (b) Input voltage and current. (c) Analysis of input voltage and current. (d) Output voltage.

20.2.4 Pure Inductive Load

A single-phase half-wave rectifier with a pure inductive load (an inductor L only) is shown in Figure 20.6a.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.6b and c. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal. The output voltage can follow it in all time. The impedance of the load is

$$Z = j\omega L = \omega L \angle \pi/2$$

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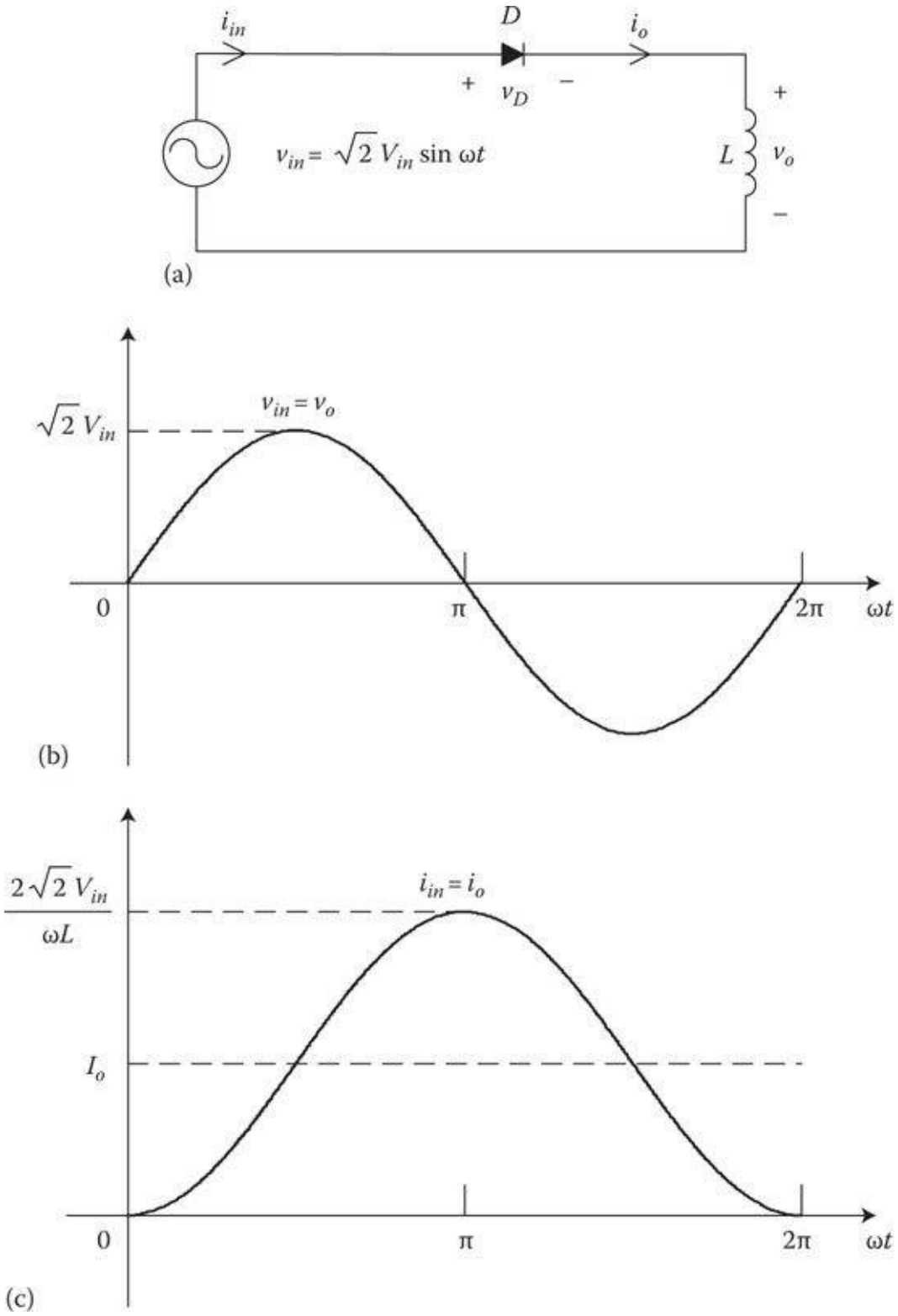


FIGURE 20.6
A single-phase half-wave rectifier with a pure inductive load (L). (a) Circuit diagram. (b) Input and output voltages. (c) Input and output currents.

The input and output voltages are

$$v_{in}(t) = v_o(t) = \sqrt{2} V_{in} \sin \omega t$$

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where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output can be a full sinusoidal waveform too. Since it is a negative value in full negative half-cycle, the output DC average voltage is 0.

The input and output current waveform is a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \frac{\sqrt{2}V_{in}}{\omega L}(1 - \cos \omega t) \tag{20.18}$$

20.2.5 Back EMF plus Resistor Load

A single-phase half-wave rectifier with a resistor plus an EMF load (a resistor *R* plus an EMF) is shown in Figure 20.7a.

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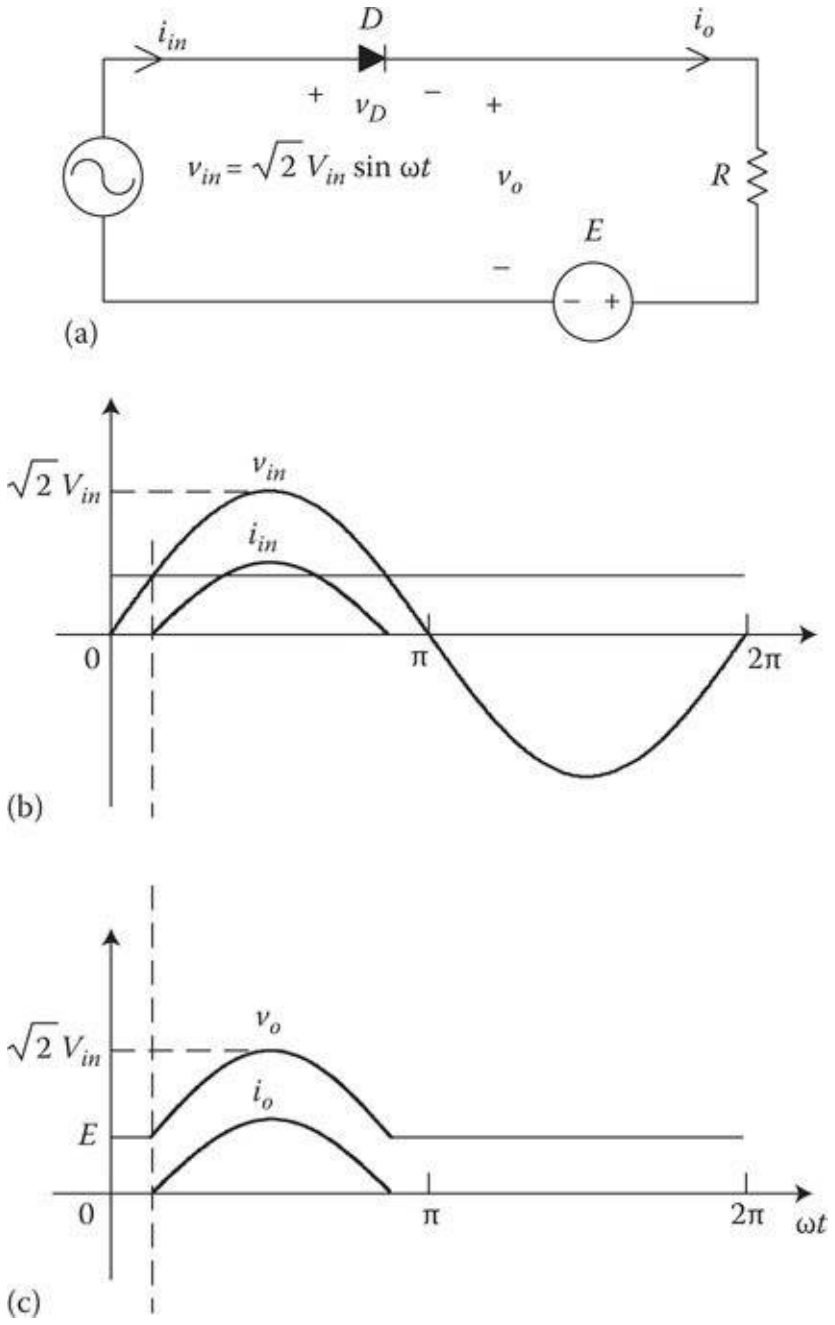


FIGURE 20.7
Single-phase half-wave rectifier with an EMF plus a resistor (R + EMF). (a) Circuit diagram. (b) Input voltage and current. (c) Output voltage and current.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.7b and c. The EMF value is E, which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m is

$$m = \frac{E}{\sqrt{2}V_{in}} < 1$$

and

$$\alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

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The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal, and the output voltage and current obey Ohm's law. The impedance of the load is *R*.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le (\pi - \alpha) \\ E & (\pi - \alpha) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.19}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle. The output DC average voltage is

$$V_{o-av} = \frac{\sqrt{2}V_{in}}{\pi}\cos\alpha + E\left(\frac{1}{2} + \frac{\alpha}{\pi}\right) > E \tag{20.20}$$

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in}\sin\omega t - E) & \alpha \le \omega t \le (\pi - \alpha) \\ 0 & (\pi - \alpha) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.21}$$

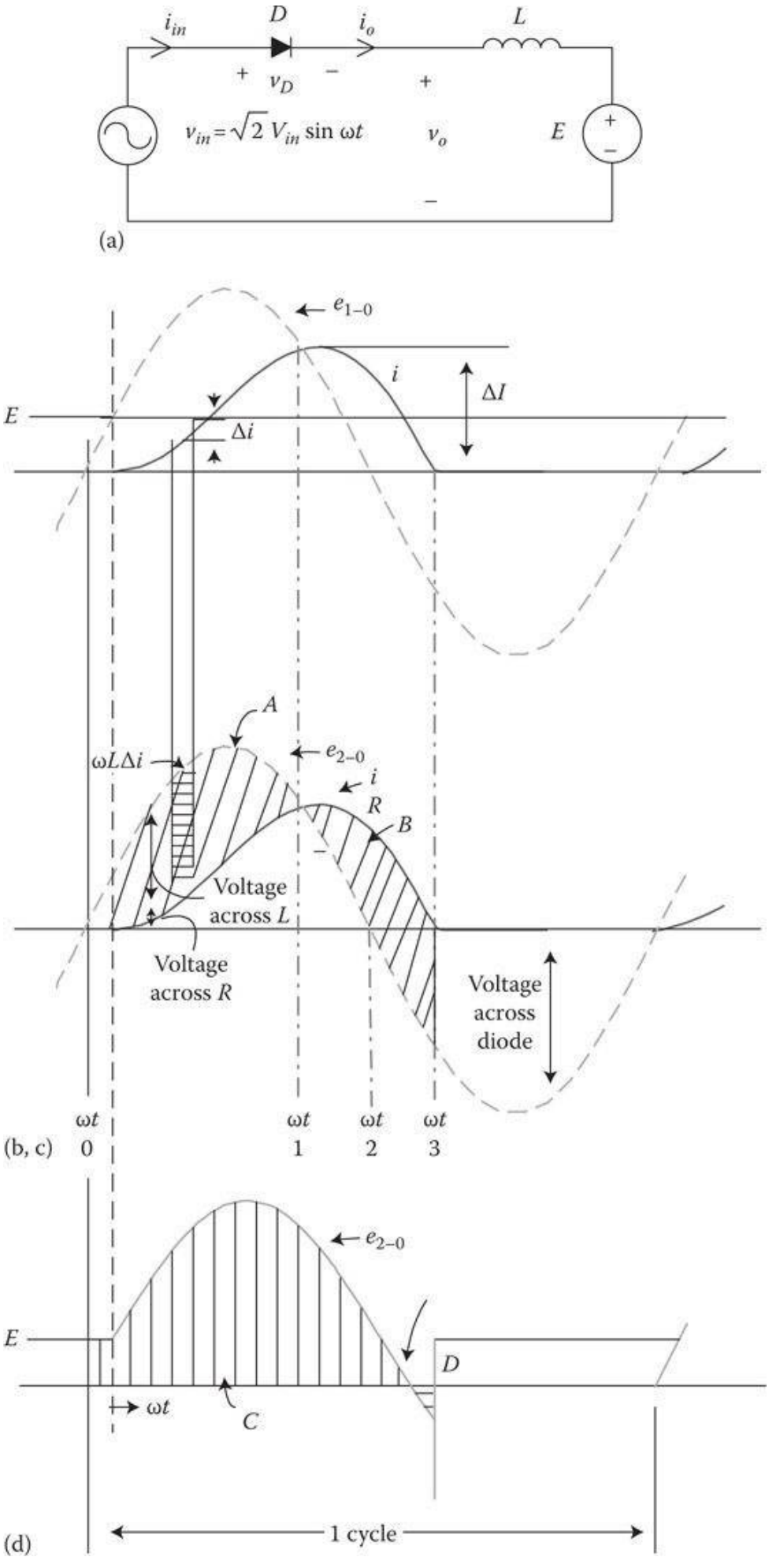
The input and output current average value is

$$I_{o-av} = \frac{0.45V_{in}}{2R}[2\cos\alpha - m(\pi - 2\alpha)] \tag{20.22}$$

20.2.6 Back EMF plus Inductor Load

A single-phase half-wave rectifier with an EMF and inductive load (an EMF plus an inductor *L*) is shown in Figure 20.8a.

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FIGURE 20.8
Single-phase half-wave rectifier with an EMF plus an inductor (EMF + *L*). (a) Circuit diagram. (b) Input voltage and current. (c) Analysis of input voltage and current. (d) Output voltage.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.8b and c. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is a sinusoidal waveform:

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le (\pi+\gamma) \\ E & (\pi+\gamma) < \omega t < (2\pi+\alpha) \end{cases} \tag{20.23}$$

where

$$\int_{\alpha}^{\pi-\alpha} (\sqrt{2}V_{in}\sin\omega t - E)d(\omega t) = \int_{\pi-\alpha}^{\pi-\alpha+\gamma} (E - \sqrt{2}V_{in}\sin\omega t)d(\omega t)$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform. The output DC average voltage is *E*.

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{\omega L}[(\cos\alpha - \cos\omega t) - m(\omega t - \alpha)] & \alpha \le \omega t \le (\pi+\alpha+\gamma) \\ 0 & (\pi+\alpha+\gamma) < \omega t < (2\pi+\alpha) \end{cases} \tag{20.24}$$

The input and output current average value is

$$I_{o-av} = \frac{0.45V_{in}}{2\omega L}\left[\gamma\cos\gamma - \sin(\alpha+\gamma) + \sin\alpha - \frac{m}{2}\alpha^2\right] \tag{20.25}$$

20.3 Single-Phase Bridge Diode Rectifier

Single-phase full-wave diode rectifier has two circuits:

1. Bridge (Graetz) circuit
2. Center-tap (midpoint) circuit

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These are shown in Figure 20.9a and b. The input and output waveforms are the same in both circuits. We use the Graetz circuit for the description in the following sections.

20.3.1 Resistive Load

A single-phase full-wave diode rectifier with a purely resistive load (R) is shown in Figure 20.10a.

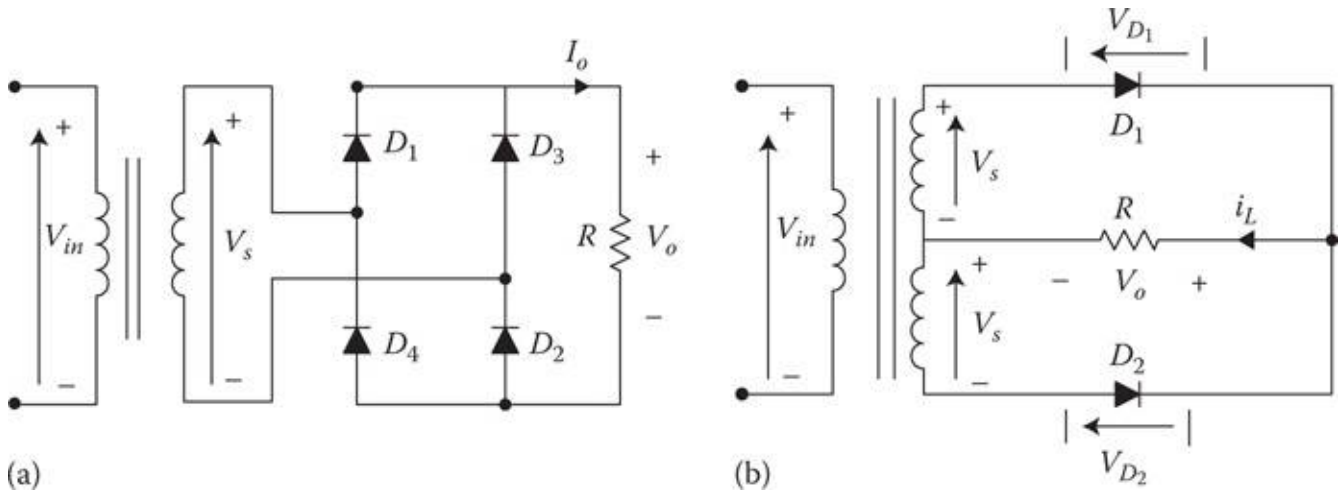


FIGURE 20.9
Single-phase full-wave diode rectifier. (a) Bridge (Graetz) circuit. (b) Center-tap (midpoint) circuit.

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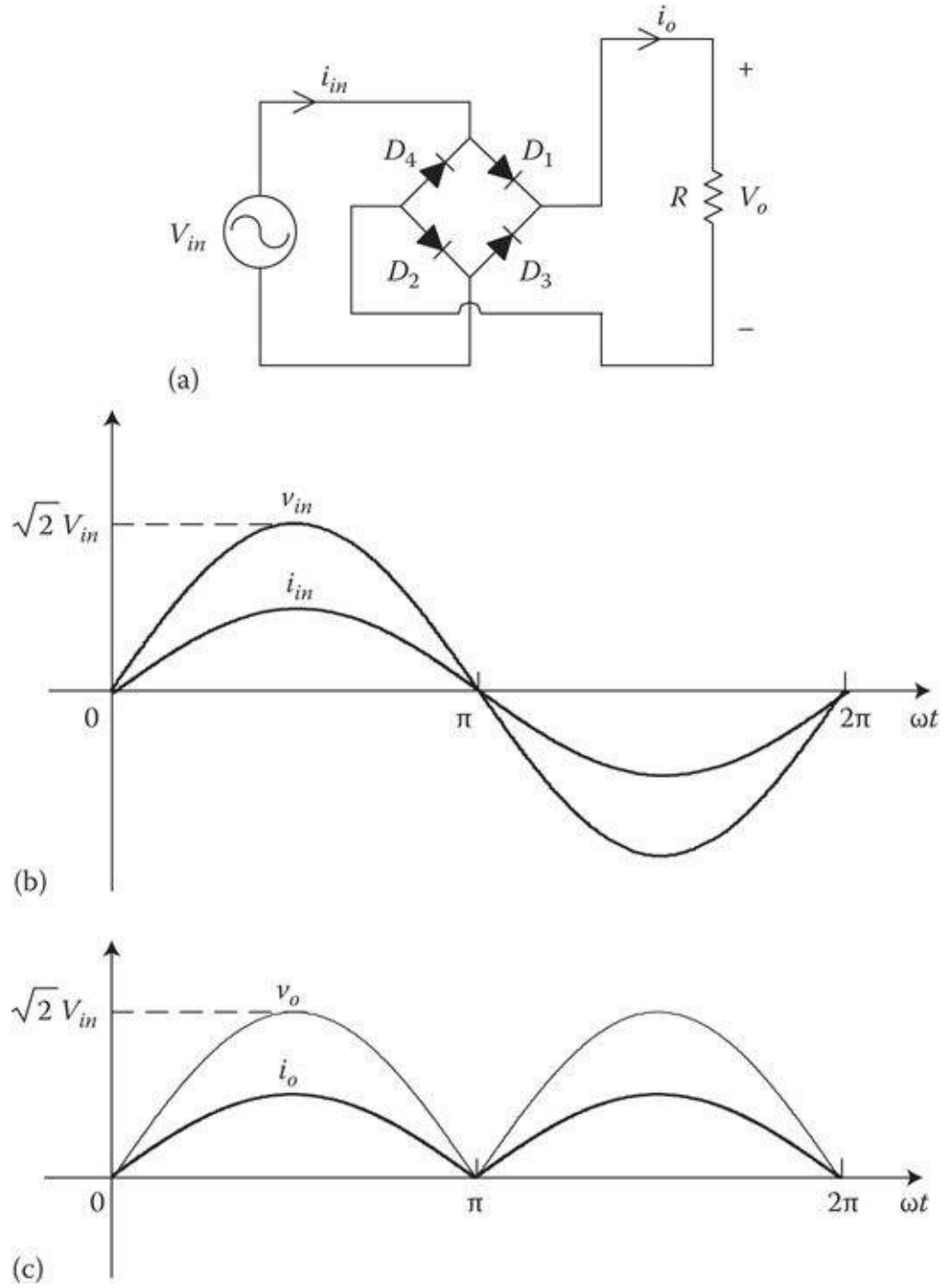


FIGURE 20.10
Single-phase full-wave diode rectifier with a purely resistive load (R). (a) Circuit diagram. (b) Input voltage and current. (c) Output voltage and current.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.10b and c. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal; the output voltage and current obey Ohm's law. Therefore, the output voltage and current are sinusoidal half-waveforms:

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.26}$$

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$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & 0 \le \omega t \le \pi \\ \sqrt{2}V_{in}\sin(\omega t - \pi) & \pi < \omega t < 2\pi \end{cases} \tag{20.27}$$

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{R}\sin\omega t & 0 \le \omega t \le \pi \\ \dfrac{\sqrt{2}V_{in}}{R}\sin(\omega t - \pi) & \pi < \omega t < 2\pi \end{cases} \tag{20.28}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a repeating half-wave sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 2ω. After fast Fourier transform (FFT) analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only *n*th ($n = 2k$) harmonics existing. The parameter ripple factor (*RF*) is defined as

$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n}}{V_{dc}} \tag{20.29}$$

where

V_{dc} is the DC component of the output voltage, which is the average value

V_n is the *n*th-order harmonic component of the output voltage

The output DC average voltage and current are

$$V_{o-av} = \frac{2\sqrt{2}}{\pi}V_{in} = 0.9V_{in} \tag{20.30}$$

$$I_{o-av} = 0.9\frac{V_{in}}{R} \tag{20.31}$$

20.3.2 Back EMF Load

A single-phase full-wave diode rectifier with an EMF plus resistor load (a resistor *R* plus an EMF) is shown in Figure 20.11a.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.11b and c. The EMF value is *E*, which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter *m*:

$$m = \frac{E}{\sqrt{2}V_{in}} < 1$$

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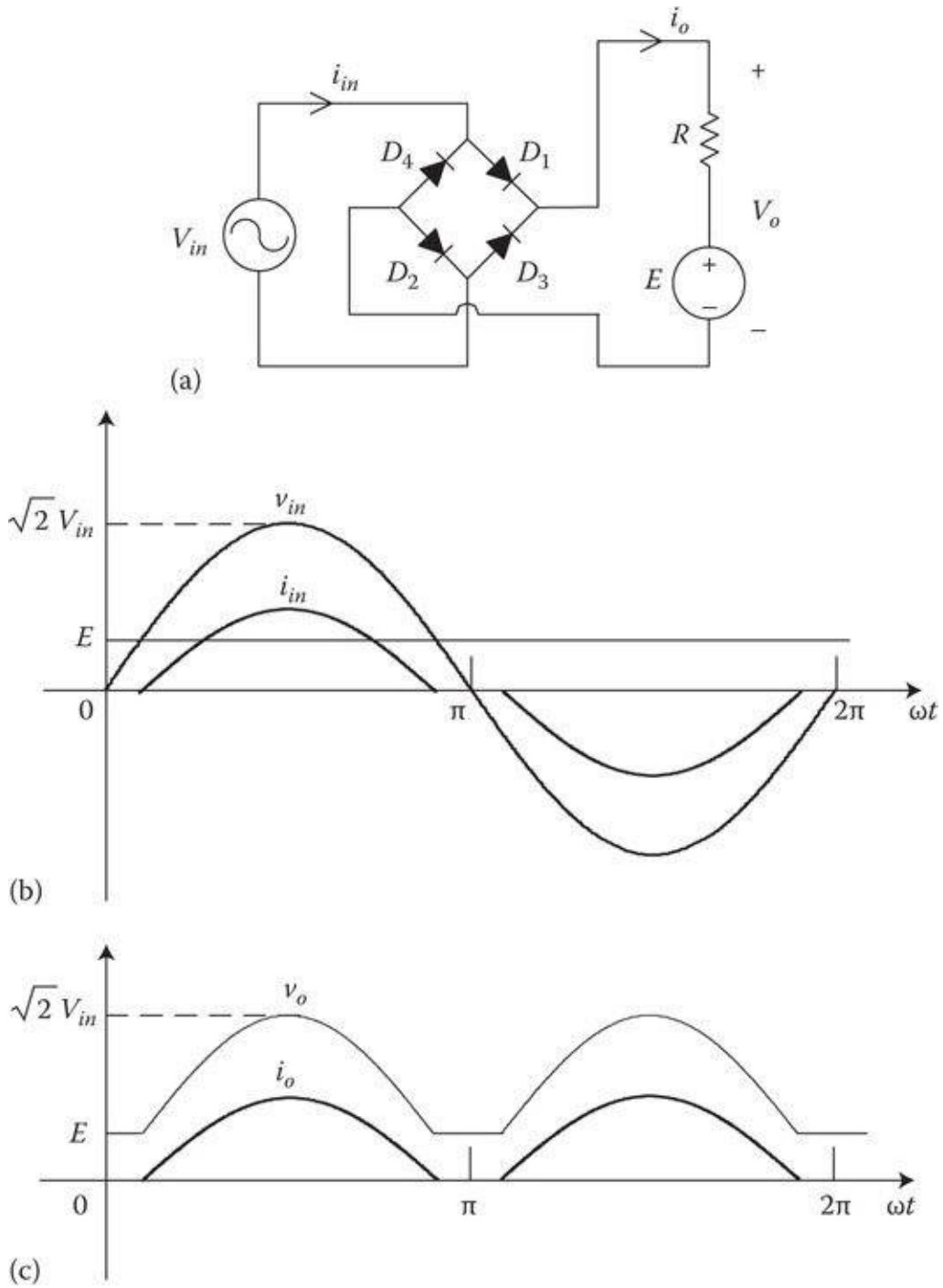


FIGURE 20.11
Single-phase full-wave D-rectifier with an EMF plus a resistor (*R* + EMF). (a) Circuit diagram. (b) Input voltage and current. (c) Output voltage and current.

and

$$\alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal; the output voltage and current obey Ohm's law. The impedance of the load is *R*.

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The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le (\pi - \alpha) \\ E & (\pi - \alpha) < \omega t < (\pi + \alpha) \end{cases} \tag{20.32}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle with the repeating frequency of 2ω. The output DC average voltage is

$$V_{o-av} = \frac{2\sqrt{2}V_{in}}{\pi}\cos\alpha + \frac{2\alpha}{\pi}E > E \tag{20.33}$$

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in}\sin\omega t - E) & \alpha \le \omega t \le (\pi - \alpha) \\ 0 & (\pi - \alpha) < \omega t < (\pi + \alpha) \end{cases} \tag{20.34}$$

The input and output current average value is

$$I_{o-av} = \frac{0.45V_{in}}{R}[\cos\alpha - m(\pi - 2\alpha)] \tag{20.35}$$

20.3.3 *R-C* Load

Linear and switch-mode DC power supplies require AC/DC rectification. To obtain a "smooth" output, capacitor *C* is connected as shown in Figure 20.12.

Neglecting diode forward voltage drop, the peak of the output voltage is $\sqrt{2}V$. During *each half-cycle* the capacitor undergoes cyclic changes from $v_{d(\min)}$ to $\sqrt{2}V$ in the period between $\omega t = \alpha$ and $\omega t = \pi/2$ and discharges from $\sqrt{2}V$ to $v_{d(\min)}$ in the period between $\omega t = \theta$ and $\omega t = \pi + \alpha$. The resultant output of the diode bridge is unipolar but time-dependent:

$$v_d(\omega t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \textit{diode on} \\ V_\theta e^{-(\omega t - \theta)/\omega RC} & \textit{diode off} \end{cases} \tag{20.36}$$

where

$$V_\theta = \sqrt{2}V_{in}\sin\theta \tag{20.37}$$

At $\omega t = \theta$, the slopes of the voltage functions are equal to

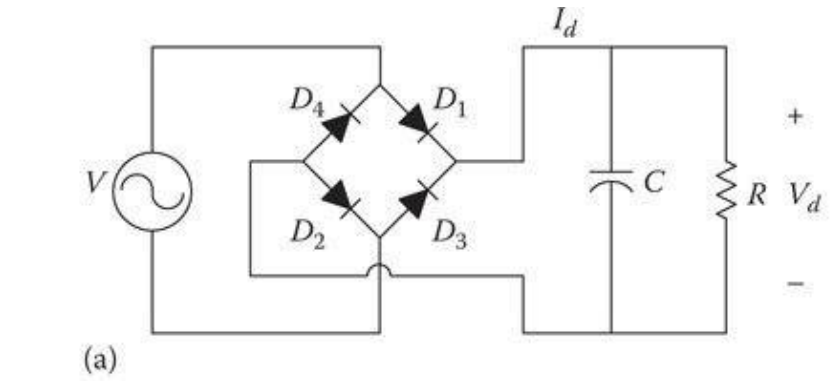
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$$\sqrt{2}V_{in}\cos\theta = \frac{\sqrt{2}V_{in}\sin\theta}{-\omega RC}e^{-(\theta-\theta)/\omega RC}$$

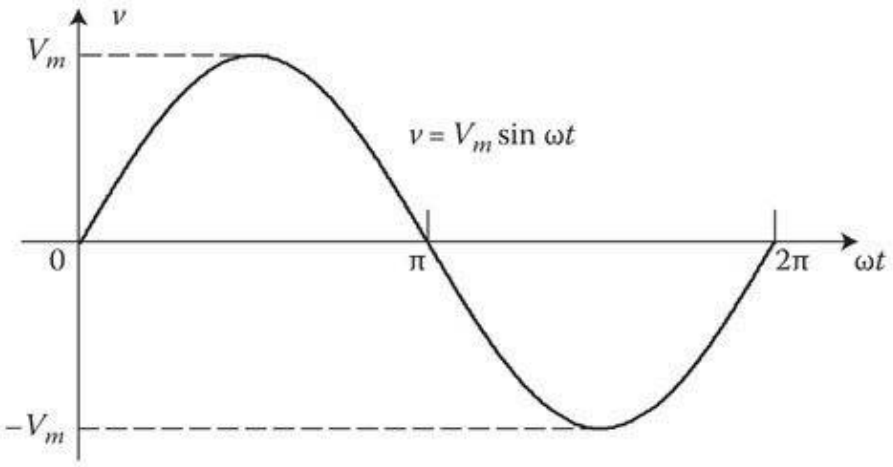
$$\therefore \frac{1}{\tan\theta} = \frac{-1}{\omega RC} \tag{20.38}$$

Thus, $\theta = \pi - \tan^{-1}(\omega RC)$

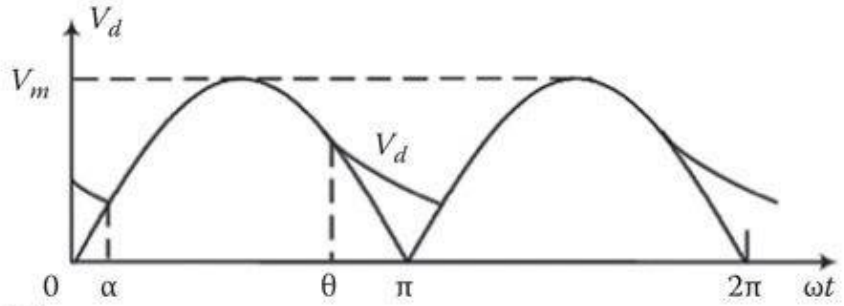
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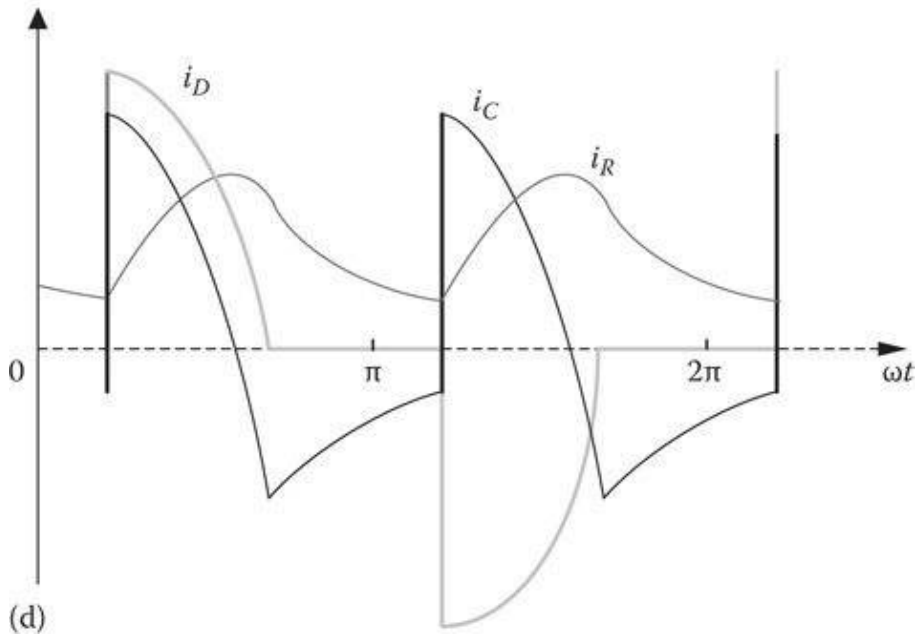
(a)



(b)



(c)



(d)

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FIGURE 20.12
Single-phase full-wave *D*-rectifier with an capacitive load (*R* + *C*). (a) Circuit. (b) Input voltage. (c) Output voltage. (d) Current waveforms.

The angle at which the diode turns on in the second period, $\omega t = \pi + \alpha$, is the point at which the sinusoidal source reaches the same value as the decaying exponential output:

$$\sqrt{2}V\sin(\pi+\alpha) = (\sqrt{2}V\sin\theta)e^{-(\pi+\alpha-\theta)/\omega RC}$$

or

$$\sin\alpha - (\sin\theta)e^{-(\pi+\alpha-\theta)/\omega RC} = 0 \tag{20.39}$$

The preceding equation must be solved numerically.

The output average voltage is

$$V_d = \frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} v_d d(\omega t) = \frac{\sqrt{2}V_{in}}{\pi}\left[\int_{\alpha}^{\theta}\sin\omega t d(\omega t) + \int_{\theta}^{\pi+\alpha}\sin\theta e^{-\frac{t-\theta/\omega}{RC}} d(\omega t)\right]$$

$$= \frac{\sqrt{2}V_{in}}{\pi}\left[(\cos\alpha-\cos\theta) + \omega RC\sin\theta\int_{0}^{(\pi+\alpha-\theta)/\omega} e^{-\frac{t}{RC}} d\left(\frac{t}{RC}\right)\right]$$

$$= \frac{\sqrt{2}V_{in}}{\pi}\left[(\cos\alpha-\cos\theta) + \omega RC\sin\theta\left(1-e^{-\frac{\pi+\alpha-\theta}{\omega RC}}\right)\right] \tag{20.40}$$

The output rms voltage is

$$V_{d-rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\pi+\alpha} v_d^2 d(\omega t)} = \sqrt{\frac{2V_{in}^2}{\pi}\left[\int_{\alpha}^{\theta}(\sin\omega t)^2 d(\omega t) + \int_{\theta}^{\pi+\alpha}\sin^2\theta e^{-2\frac{t-\theta/\omega}{RC}} d(\omega t)\right]}$$

$$= \sqrt{2}V_{in}\sqrt{\frac{1}{\pi}\left[\left(\frac{\theta-\alpha}{2} - \frac{\cos 2\alpha - \cos 2\theta}{4}\right) + \omega RC\sin^2\theta\left(1-\frac{e^{-2(\pi+\alpha-\theta)/\omega RC}}{2}\right)\right]} \tag{20.41}$$

Since the average capacitor current is zero, the output average current is

$$I_d = \frac{V_d}{R} = \frac{\sqrt{2}V_{in}}{\pi R}\left[(\cos\alpha-\cos\theta) + \omega RC\sin\theta\left(1-e^{-\frac{\pi+\alpha-\theta}{\omega RC}}\right)\right] \tag{20.42}$$

The FF and RF of the output voltage are

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$$FF = \frac{V_{d-rms}}{V_d} = \frac{\sqrt{2}V_{in}\sqrt{1/\pi\left[((\theta-\alpha)/2)-((\cos 2\alpha-\cos 2\theta)/4)\right]+\omega RC\sin^2\theta(1-(e^{-2(\pi+\alpha-\theta)/\omega RC})/2)]}}{\sqrt{2}V_{in}/\pi[(\cos\alpha-\cos\theta)+\omega RC\sin\theta(1-e^{-(\pi+\alpha-\theta)/\omega RC})]}$$

$$= \frac{\sqrt{\pi}\sqrt{[(\theta-\alpha)/2]-(\cos 2\alpha-\cos 2\theta)/4+\omega RC\sin^2\theta(1-(e^{-2(\pi+\alpha-\theta)/\omega RC})/2)}}{\cos\alpha-\cos\theta+\omega RC\sin\theta(1-e^{-(\pi+\alpha-\theta)/\omega RC})}$$

$$RF = \sqrt{FF^2-1} \tag{20.43}$$

20.4 Three-Phase Half-Bridge Diode Rectifier

A three-phase half-bridge diode rectifier is shown in Figure 20.13. The three-phase AC suppliers have the same rms value V_{in} with amplitude $\sqrt{2}V_{in}$ and frequency ω, and the phase angle shift is 120°.

20.4.1 Resistive Load

A three-phase half-bridge diode rectifier with a purely resistive load (R) is shown in Figure 20.13a.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.13b and c. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal. Therefore, the output voltage and current are sinusoidal half-waveforms:

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

$$v_o(t) = \sqrt{2}V_{in}\sin\omega t \quad \left(\frac{2n\pi}{3}+\frac{\pi}{6}\right) \le \omega t \le \left(\frac{2n\pi}{3}+\frac{5\pi}{6}\right) \tag{20.44}$$

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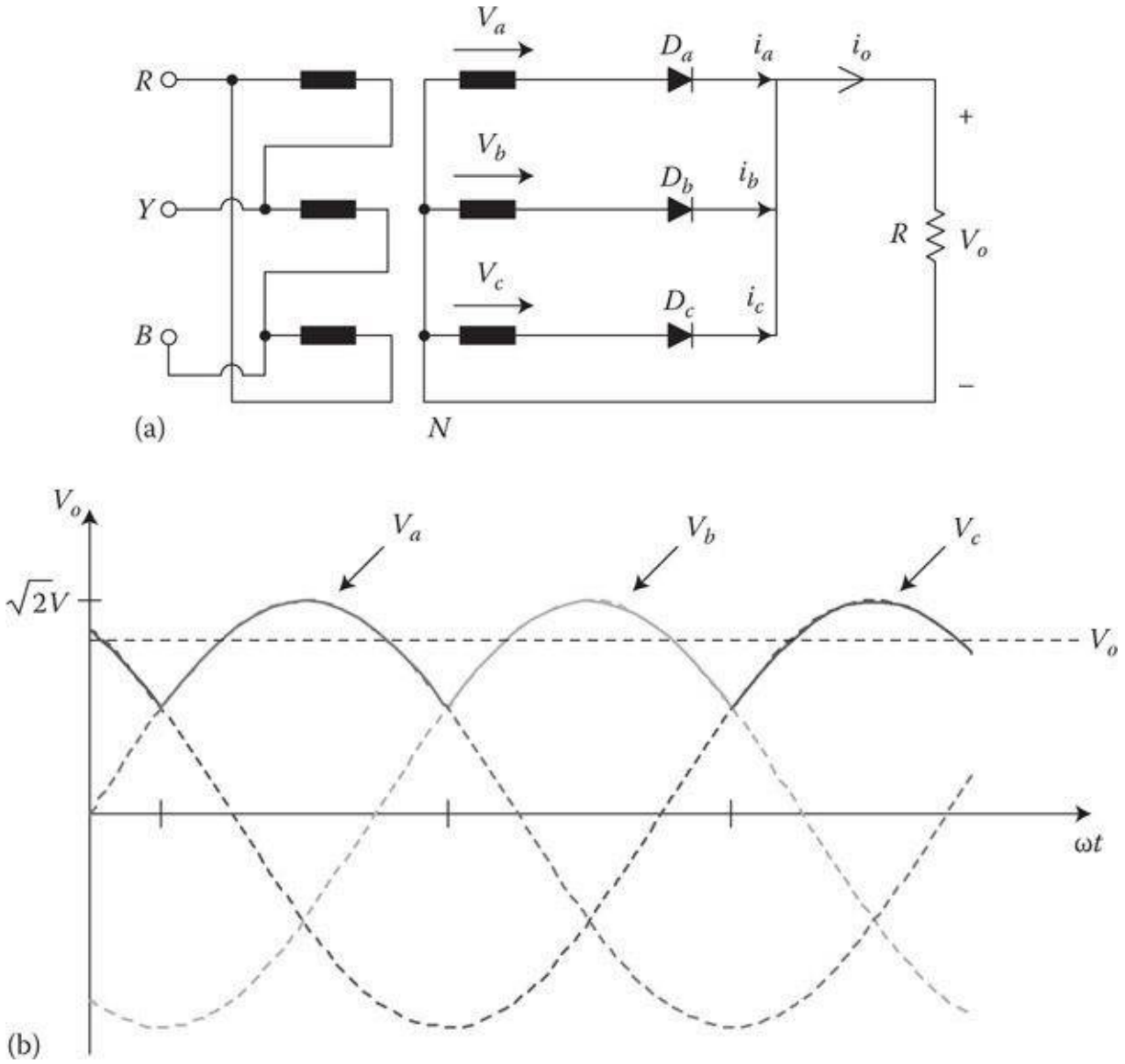


FIGURE 20.13
A three-phase half-bridge diode rectifier with a resistor (R). (a) Circuit diagram. (b) Input voltage waveform.

where $n = 1, 2, 3, \ldots$

$$i_{in}(t) = i_o(t) = \frac{\sqrt{2}V_{in}}{R}\sin\omega t \qquad \left(\frac{2n\pi}{3} + \frac{\pi}{6}\right) \le \omega t \le \left(\frac{2n\pi}{3} + \frac{5\pi}{6}\right) \tag{20.45}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a repeating partial sinusoidal waveform for both voltage and current without angle shift between voltage and current. The output is a DC voltage with ripple in the repeating frequency 3ω. After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only *n*th ($n = 3k$) harmonics existing. The parameter *RF* is defined as

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$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n}}{V_{dc}} \tag{20.46}$$

where

V_{dc} is the DC component of the output voltage, which is the average value

V_n is the nth-order harmonic component of the output voltage

The output DC average voltage and current are

$$V_{o-av} = \frac{3\sqrt{6}}{2\pi} V_{in} = 1.17 V_{in} \tag{20.47}$$

$$I_{o-av} = 1.17 \frac{V_{in}}{R} \tag{20.48}$$

20.4.2 Back EMF Load ($0.5\sqrt{2}V_{in} < E < \sqrt{2}V_{in}$)

A three-phase half-wave diode rectifier with an EMF plus a resistor load (a resistor R plus an EMF) is shown in Figure 20.14. This section discusses the case that the EMF value E is in condition: $0.5\sqrt{2}V_{in} < E < \sqrt{2}V_{in}$. Suppose an auxiliary parameter m:

$$0.5 < m = \frac{E}{\sqrt{2}V_{in}} < 1$$

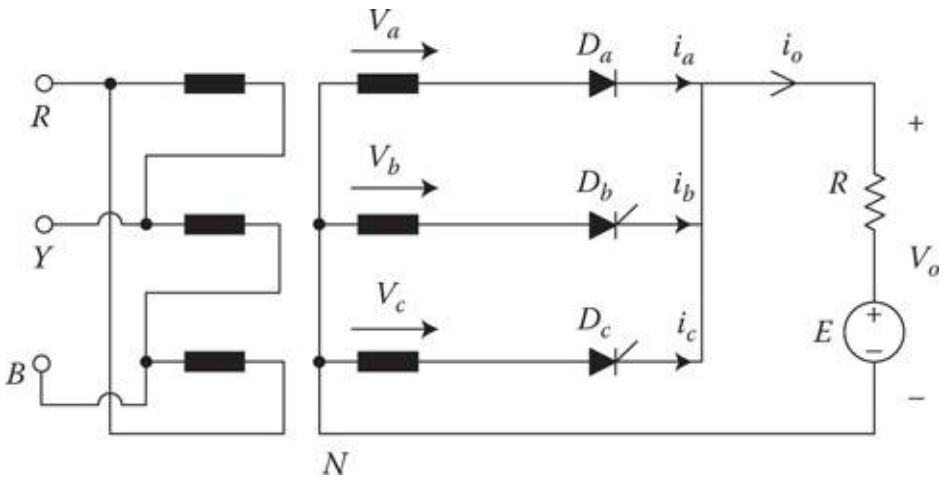


FIGURE 20.14
Three-phase half-wave diode rectifier with an EMF plus a resistor (R + EMF).

and

$$30^\circ < \alpha = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}} < 90^\circ$$

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal; the output voltage and current obey Ohm's law. The impedance of the

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load is *R*.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \left(\frac{2n\pi}{3}+\alpha\right) \le \omega t \le \left(\frac{2n\pi}{3}+\pi-\alpha\right) \\ E & \text{other} \end{cases} \tag{20.49}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle with the repeating frequency 3ω. The output DC average voltage is

$$V_{o-av} = \frac{3\sqrt{2}V_{in}}{\pi}\cos\alpha + \left(\frac{3\alpha}{\pi}-\frac{1}{2}\right)E > E \tag{20.50}$$

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in}\sin\omega t - E) & \alpha \le \omega t \le (\pi-\alpha) \\ 0 & (\pi-\alpha) < \omega t < (\pi+\alpha) \end{cases} \tag{20.51}$$

20.4.3 Back EMF Load ($E < 0.5\sqrt{2}V_{in}$)

A three-phase half-wave diode rectifier with an EMF plus a resistor load (a resistor *R* plus an EMF) is also shown in Figure 20.14. The EMF value *E* is in the condition $E < 0.5\sqrt{2}V_{in}$. Suppose an auxiliary parameter *m:*

$$m = \frac{E}{\sqrt{2}V_{in}} < 0.5$$

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

$$v_o(t) = \sqrt{2}V_{in}\sin\omega t \quad \left(\frac{2n\pi}{3}+\frac{\pi}{6}\right) \le \omega t \le \left(\frac{2n\pi}{3}+\frac{5\pi}{6}\right) \tag{20.44}$$

where $n = 1, 2, 3, \ldots$

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in}\sin\omega t - E) & \left(\frac{2n\pi}{3}+\frac{\pi}{6}\right) \le \omega t \le \left(\frac{2n\pi}{3}+\frac{5\pi}{6}\right) \\ 0 & \text{other} \end{cases} \tag{20.52}$$

where V_{in} is the rms value of the input voltage. The input wave is a sinusoidal waveform; the corresponding output voltage is a repeating partial sinusoidal waveform. There is no shift angle between the input voltage and current. The output voltage is a DC voltage with ripple in

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the repeating frequency 3ω. After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only *n*th ($n = 3k$) harmonics existing.

Where V_{dc} is the DC component of the output voltage, which is the average value of V_{o-av}, and V_n is the nth-order harmonic of the output voltage. The output DC average voltage is

$$V_{o-av} = \frac{3\sqrt{6}}{2\pi} V_{in} = 1.17 V_{in} \tag{20.53}$$

20.5 Three-Phase Full-Bridge Diode Rectifier with Resistive Load

A three-phase full-bridge diode rectifier with a purely resistive load (R) is shown in Figure 20.15a.

Its input/output voltage v_{in} and v_o and input/output current i_{in} and i_o waveforms are shown in Figure 20.15b. The three-phase AC suppliers have the same rms value V_{in} with amplitude $\sqrt{2}V_{in}$ and frequency ω and phase angle shift 120°. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal. Therefore, the output voltage and current are sinusoidal half-waveforms:

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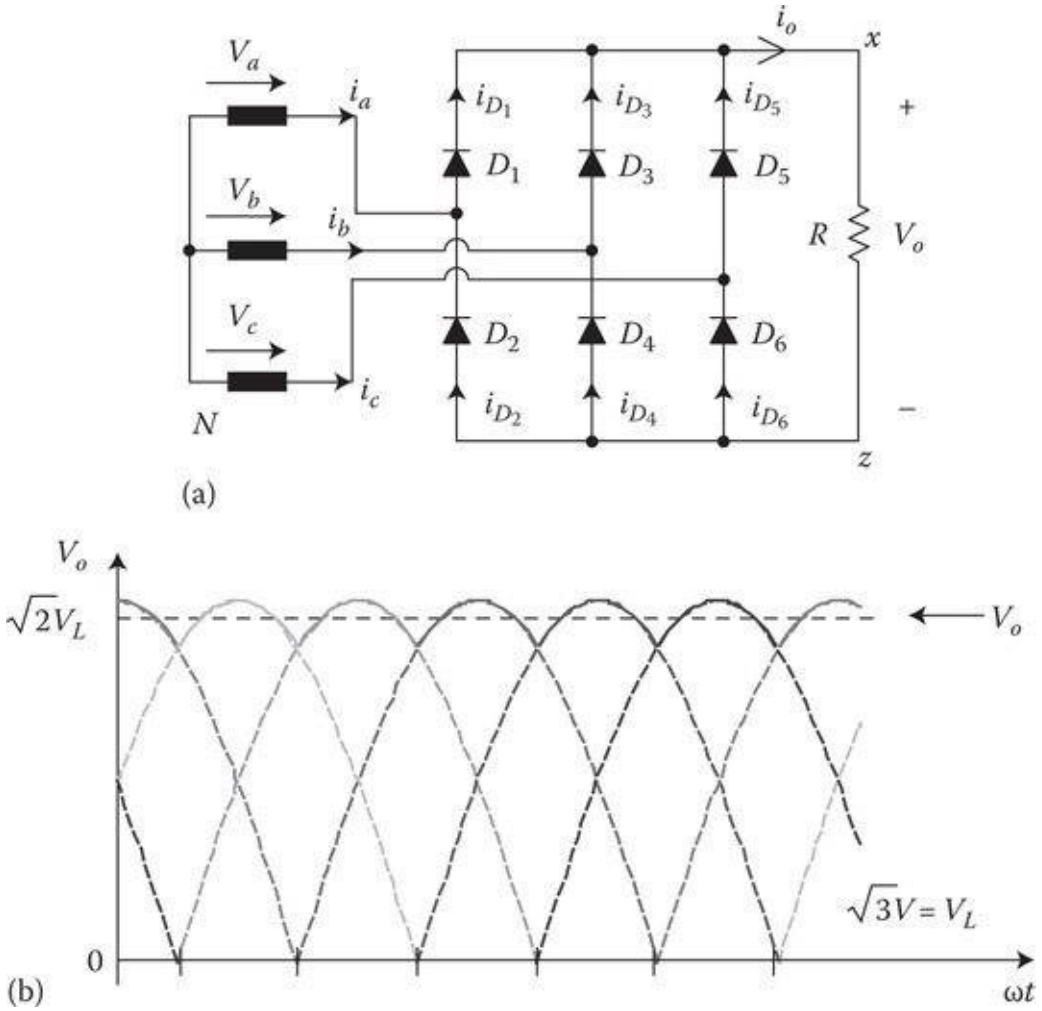


FIGURE 20.15
Three-phase full-bridge diode rectifier with a resistor (*R*). (a) Circuit diagram. (b) Input voltage waveform.

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

$$v_o(t) = \sqrt{6}V_{in}\sin\omega t \qquad \frac{n\pi}{3} \le \omega t \le \frac{(n+1)\pi}{3} \tag{20.54}$$

where $n = 1, 2, 3, \ldots$

$$i_{in}(t) = i_o(t) = \frac{\sqrt{6}V_{in}}{R}\sin\omega t \qquad \frac{n\pi}{3} \le \omega t \le \frac{(n+1)\pi}{3} \tag{20.55}$$

where V_{in} is the rms value of the input voltage. The input voltage wave is a sinusoidal waveform; the corresponding output is a repeating partial sinusoidal waveform for both voltage and current without angle shift between the voltage and current. The output is a DC voltage with ripple in the repeating frequency 6ω. After FFT analysis of the rectified waveform, harmonic components are shown in the frequency spectrum. From the spectrum, there are only *n*th ($n = 6k$) harmonics existing. The parameter *RF* is defined as

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$$RF = \frac{V_{ac}}{V_{dc}} = \frac{\sqrt{\sum_{n=1}^{\infty} V_n}}{V_{dc}} = 0.054 \tag{20.56}$$

where

V_{dc} is the DC component of the output voltage

V_n is the *n*th-order harmonic component of the output voltage

The input voltage is an AC voltage with distortion in the repeating frequency 6ω. After FFT analysis of the supplying waveform, the harmonic components are shown in the frequency spectrum. From the spectrum, there are only *n*th (n = 6k ± 1) harmonics existing. The parameter total harmonic distortion (*THD*) is defined as

$$THD = \frac{V_{ac}}{V_{fund}} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n}}{V_{fund}} = 0.046 \tag{20.57}$$

where

V_{fund} is the fundamental component of the input voltage

V_n is the *n*th-order harmonic component of the input voltage

The output DC average voltage and current are

$$V_{o-av} = \frac{3\sqrt{6}}{\pi} V_{in} = 2.34 V_{in} \tag{20.58}$$

$$I_{o-av} = 2.34 \frac{V_{in}}{R} \tag{20.59}$$

Since the output DC voltage ripple is very small (*RF* = 0.054), the EMF load usually has the condition $E < \sqrt{6}V_{in}$. No need to spend time discussing this case.

20.6 Thyristor Rectifiers

A thyristor is a silicon-controlled rectifier. It is a four-layer $p-n-p-n$ semiconductor device forming three junctions $J_1-J_2-J_3$, as shown in Figure 20.16a.

It has three external electrodes: anode, cathode, and gate. This structure can be considered as two-type transistors in cascade connection shown in Figure 20.16b and c. Its characteristics will be discussed in the next section. It is controlled by a firing pulse with shifting firing angle (α). When α = 0°, the characteristics of a thyristor is the same to those of a diode.

20.6.1 Single-Phase Half-Wave Rectifier with Resistive Load

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A single-phase half-wave thyristor rectifier with resistive load (R) is shown in Figure 20.17. The firing angle a can be set in the following range:

$$0 < \alpha < \pi$$

As before, the input voltage is a sinusoidal wave:

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \tag{20.1}$$

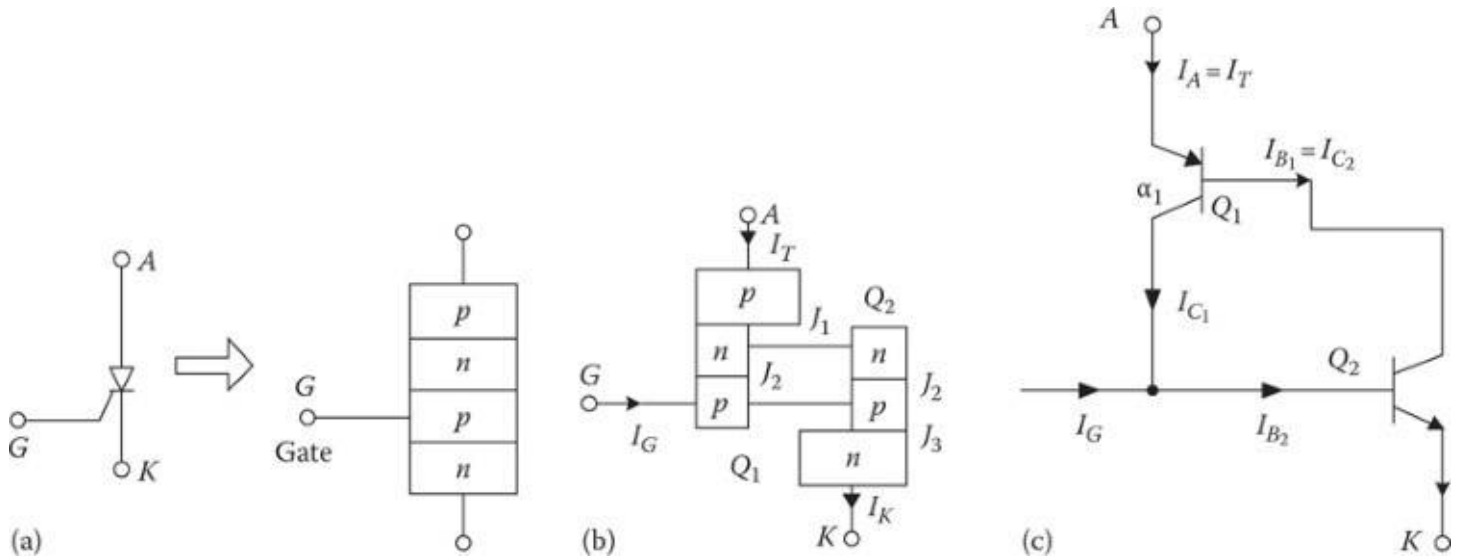


FIGURE 20.16
Thyristor. (a) Thyristor symbol and structure. (b) Combination by two transistors. (c) Equivalent circuit.

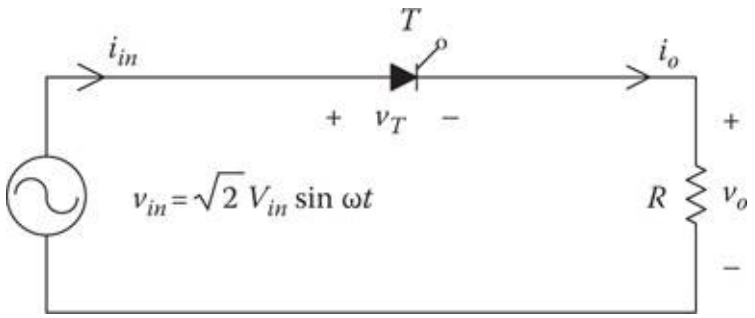


FIGURE 20.17
Single-phase half-wave thyristor rectifier with a resistor (R).

The output voltage and current are

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \le \omega t \le \pi \\ 0 & \pi < \omega t < 2\pi + \alpha \end{cases} \tag{20.60}$$

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{R} \sin \omega t & \alpha \le \omega t \le \pi \\ 0 & \pi < \omega t < 2\pi + \alpha \end{cases} \tag{20.61}$$

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Their average values are

$$V_{o-av} = 0.225V_{in}(1+\cos\alpha) \tag{20.62}$$

$$I_{o-av} = 0.225\frac{V_{in}}{R}(1+\cos\alpha) \tag{20.63}$$

20.6.2 Single-Phase Half-Wave Thyristor Rectifier with Inductive Load

A single-phase half-wave thyristor rectifier with inductive load (R + L) is shown in Figure 20.18. The load time constant is $\tau = L/R$. Hence, the load impedance Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi \tag{20.64}$$

where

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

The output voltage and current are

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le \beta \\ 0 & \beta < \omega t < 2\pi + \alpha \end{cases} \tag{20.65}$$

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{|Z|}\sin(\omega t - \phi) + \sin(\alpha - \phi)e^{-\frac{(\beta-\alpha)/\omega}{L/R}} & \alpha \le \omega t \le \beta \\ 0 & \beta < \omega t < 2\pi + \alpha \end{cases} \tag{20.66}$$

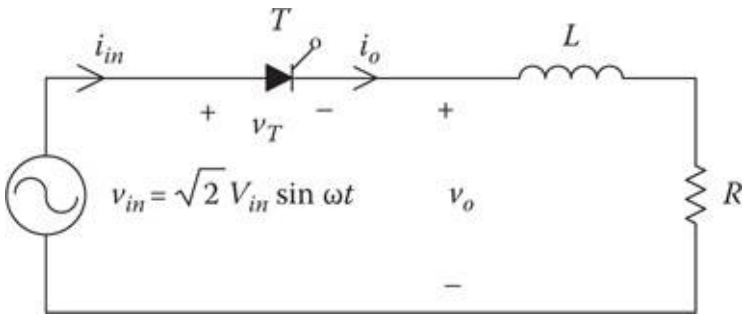


FIGURE 20.18
Single-phase half-wave thyristor rectifier with inductive load (R + L).

where β is the extinction angle and is determined by

$$\sin(\beta - \phi) = \sin(\alpha - \phi)e^{-\frac{\beta-\alpha}{\omega\tau}} \qquad \tau = \frac{L}{R} \tag{20.67}$$

Their average values are

$$V_{o-av} = 0.225V_{in}(\cos\alpha - \cos\beta) \tag{20.68}$$

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$$I_{o-av} = 0.225 \frac{V_{in}}{R}(\cos\alpha - \cos\beta) \tag{20.69}$$

20.6.3 Single-Phase Half-Wave Thyristor Rectifier with Pure Inductive Load

A single-phase half-wave thyristor rectifier with pure inductive load (L) is shown in Figure 20.19. The load is an inductor L only. Therefore,

$$Z = j\omega L = \omega L \angle \phi \tag{20.70}$$

where

$$\phi = \frac{\pi}{2}$$

The output voltage and current are

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le 2\pi - \alpha \\ 0 & 2\pi - \alpha < \omega t < 2\pi + \alpha \end{cases} \tag{20.71}$$

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{|Z|}(\cos\alpha - \cos\omega t) & \alpha \le \omega t \le 2\pi - \alpha \\ 0 & 2\pi - \alpha < \omega t < 2\pi + \alpha \end{cases} \tag{20.72}$$

Their average values are

$$V_{o-av} = 0 \tag{20.73}$$

$$I_{o-av} = \frac{\sqrt{2}V_{in}}{\omega L \pi}[(\pi - \alpha) + \sin\alpha] \tag{20.74}$$

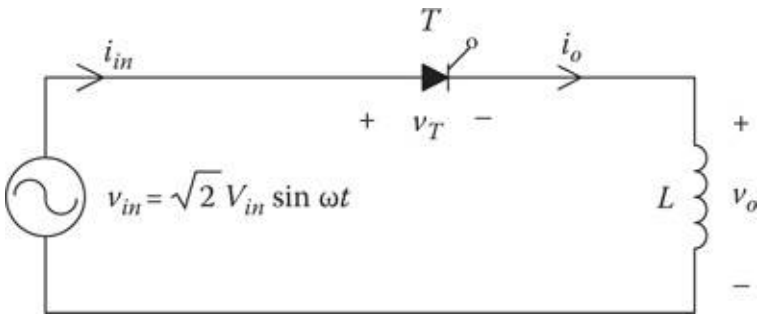


FIGURE 20.19
Single-phase half-wave thyristor rectifier with pure inductive load (L).

20.6.4 Single-Phase Half-Wave Rectifier with Back EMF plus Resistive Load

A single-phase half-wave thyristor rectifier with an EMF plus a resistor load (a resistor R plus an EMF) is shown in Figure 20.20. The EMF value is E, which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m:

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$$m = \frac{E}{\sqrt{2}V_{in}} < 1$$

and

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \tag{20.1}$$

The thyristor conduction condition requires firing angle $\alpha \geq \eta$.

Hence, The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\pi - \eta) \\ E & (\pi - \eta) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.75}$$

The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle. The output DC average voltage is

$$V_{o-av} = \frac{\sqrt{2}V_{in}}{2\pi}(\cos \eta + \cos \alpha) + \frac{E}{2\pi}(\alpha + \pi + \eta) > E \tag{20.76}$$

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \frac{1}{R}(\sqrt{2}V_{in} \sin \omega t - E) & \alpha \leq \omega t \leq (\pi - \eta) \\ 0 & (\pi - \eta) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.77}$$

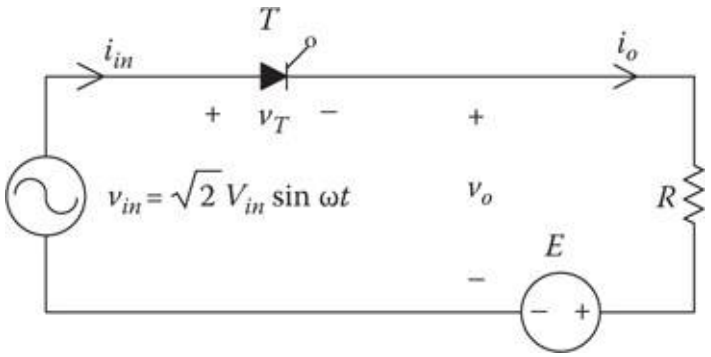


FIGURE 20.20
Single-phase half-wave thyristor rectifier with an EMF plus a resistor (*R* + EMF).

The input and output current average value is

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$$I_{o-av} = \frac{\sqrt{2}V_{in}}{2\pi R}[\cos\eta + \cos\alpha - m(\pi - \eta - \alpha)] \tag{20.78}$$

20.6.5 Single-Phase Half-Wave Rectifier with Back EMF plus Inductive Load

A single-phase half-wave thyristor rectifier with an EMF plus an inductive load (an EMF plus a resistor R and an inductor L) is shown in Figure 20.21. The EMF value is E, which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter m:

$$m = \frac{E}{\sqrt{2}V_{in}} < 1$$

and

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

As before, the load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1} \frac{\omega L}{R}$$

and the load time constant is $\tau = L/R$.

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in} \sin\omega t \tag{20.1}$$

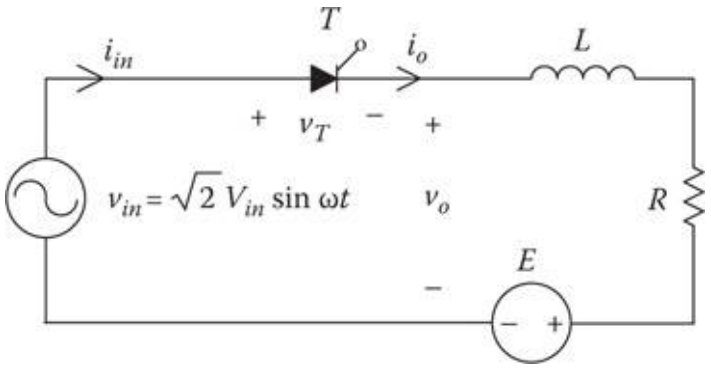


FIGURE 20.21
Single-phase half-wave thyristor rectifier with an EMF plus a resistor and inductor (EMF + R + L).

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Since the inductor causes the current continuity, the thyristor conduction angular length is y, which usually $\alpha + \gamma \geq \pi$. The thyristor conduction condition requires firing angle $\alpha \geq \eta$. Hence, the output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\alpha + \gamma) \\ E & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.79}$$

where γ is determined by

$$e^{-\frac{\gamma}{\omega L/R}} = \frac{(m/\cos\phi) - \sin(\alpha + \gamma - \phi)}{(m/\cos\phi) - \sin(\alpha - \phi)} \tag{20.80}$$

The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle. The output DC average voltage is

$$V_{o-av} = E \tag{20.81}$$

The input and output current waveform is no longer a sinusoidal waveform:

$$i_{in}(t) = i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{|Z|}\left[\sin(\omega t - \phi) - \left\{\dfrac{m}{con\phi} - \left[\dfrac{m}{con\phi} - \sin(\alpha - \phi)\right]e^{-\frac{\gamma}{\omega L/R}}\right\}\right] & \alpha \leq \omega t \leq (\alpha + \gamma) \\ 0 & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.82}$$

The input and output current average value is

$$I_{o-av} = \frac{\sqrt{2}V_{in}}{2\pi R}[\cos\alpha - \cos(\alpha + \gamma) - m\gamma] \tag{20.83}$$

20.6.6 Single-Phase Half-Wave Rectifier with Back EMF Plus Pure Inductor

A single-phase half-wave thyristor rectifier with an EMF plus a pure inductor *L* is shown in Figure 20.22. The EMF value is *E*, which is smaller than the input peak voltage $\sqrt{2}V_{in}$. Suppose an auxiliary parameter *m:*

$$m = \frac{E}{\sqrt{2}V_{in}} < 1$$

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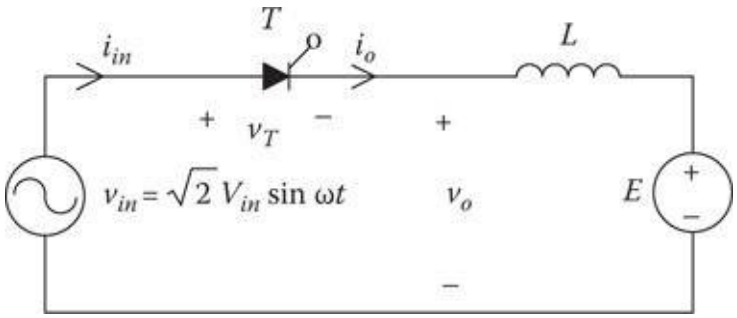


FIGURE 20.22
Single-phase half-wave thyristor rectifier with an EMF plus a inductor (EMF + *L*).

and

$$\eta = \sin^{-1} m = \sin^{-1} \frac{E}{\sqrt{2}V_{in}}$$

The load *Z* is

$$Z = j\omega L = \omega L \angle \phi$$

where

$$\phi = \frac{\pi}{2}$$

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \tag{20.1}$$

Since the inductor causes the current continuity, the thyristor conduction angular length is γ, which usually $\alpha + \gamma \geq \pi$. The thyristor conduction condition requires firing angle $\alpha \geq \eta$.

Hence, the output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in} \sin \omega t & \alpha \leq \omega t \leq (\alpha + \gamma) \\ E & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.84}$$

where γ is determined by

$$\gamma = \frac{con\alpha - \cos(\alpha + \gamma)}{m} \tag{20.85}$$

The input wave is a sinusoidal waveform; the corresponding output is a partial sinusoidal waveform less than a half-cycle. The output DC average voltage is

$$V_{o-av} = E \tag{20.86}$$

The input and output current waveform is no longer a sinusoidal waveform:

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$$i_{in}(t) = i_o(t) = \begin{cases} \frac{\sqrt{2}V_{in}}{\omega L}[\cos\alpha - \cos\omega t - m(\omega t - \alpha)] & \alpha \le \omega t \le (\alpha + \gamma) \\ 0 & (\alpha + \gamma) < \omega t < (2\pi + \alpha) \end{cases} \tag{20.87}$$

The input and output current average value is

$$I_{o-av} = \frac{\sqrt{2}V_{in}}{2\pi\omega L}\left[\gamma\cos\alpha + \sin\alpha - \sin(\alpha + \gamma) - \frac{m\gamma^2}{2} + m\alpha\gamma\right] \tag{20.88}$$

20.6.7 Single-Phase Full-Wave Semicontrolled Rectifier with Inductive Load

A single-phase full-wave semicontrolled rectifier with an inductive load (an inductor *L* and a resister *R*) plus a freewheeling diode *D* is shown in Figure 20.23. This rectifier is operating in quadrant I only because of the freewheeling diode *D*. The rectified output waveform is repeating in the frequency 2ω. The load *Z* is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

and the load time constant is $\tau = L/R$.

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in}\sin\omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le \pi \\ 0 & \pi < \omega t < (\pi + \alpha) \end{cases} \tag{20.89}$$

The output DC average voltage is

$$V_{o-av} = \frac{\sqrt{2}V_{in}}{\pi}(1 + \cos\alpha) \tag{20.90}$$

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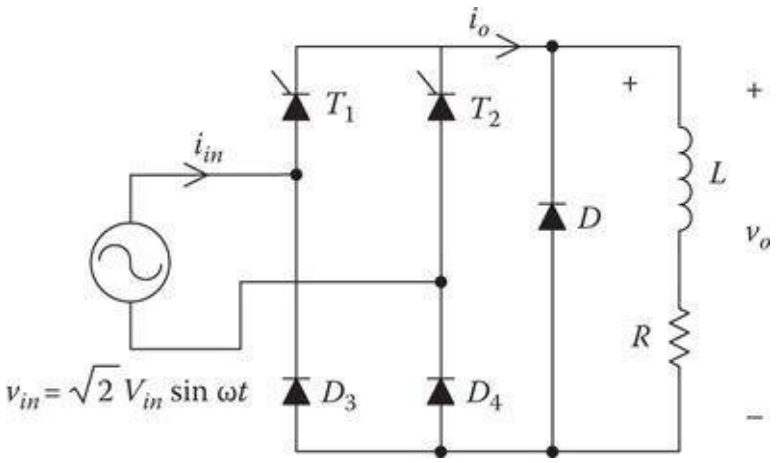


FIGURE 20.23
Single-phase full-wave semicontrolled thyristor rectifier with an inductive load ($L + R$) plus a freewheeling diode D.

If the inductance is large enough and the load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, the input and output current waveform can be considered constant:

$$i_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{(\pi - \alpha)R}(1 + \cos\alpha) & \alpha \le \omega t \le \pi \\ 0 & \pi < \omega t < (\pi + \alpha) \end{cases} \tag{20.91}$$

The input and output current average value is

$$I_{o-av} = \frac{\sqrt{2}V_{in}}{\pi R}(1 + \cos\alpha) \tag{20.92}$$

20.6.8 Single-Phase Full-Controlled Rectifier with Inductive Load

A single-phase full-wave semicontrolled thyristor rectifier with an inductive load (an inductor L and a resister R) is shown in Figure 20.24. This rectifier is operating in quadrants I and IV. The rectified output waveform is repeating in the frequency 2ω. If the inductance is large enough, the output current can be constant. The load Z is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

and the load time constant is $\tau = L/R \gg T/2 = 1/2f$

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

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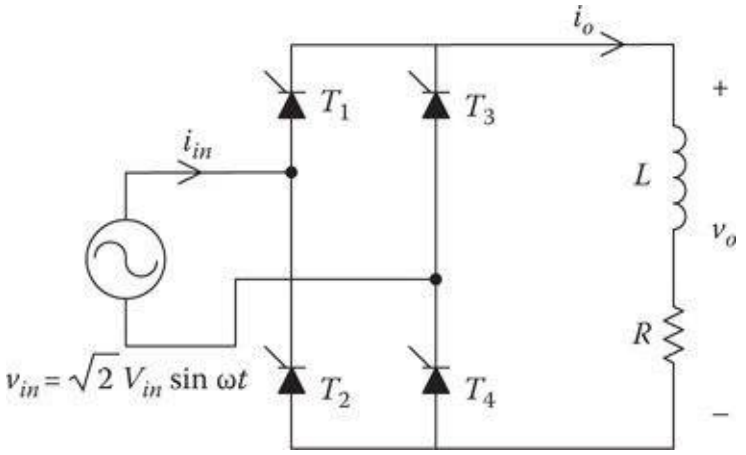


FIGURE 20.24
Single-phase full-wave semicontrolled thyristor rectifier with inductive load ($L + R$).

The input voltage is

$$v_{in}(t) = \sqrt{2}V_{in} \sin \omega t \tag{20.1}$$

The output voltage is

$$v_o(t) = \sqrt{2}V_{in} \sin \omega t \qquad \alpha \le \omega t \le (\pi + \alpha) \tag{20.93}$$

The output DC average voltage is

$$V_{o-av} = \frac{2\sqrt{2}V_{in}}{\pi} \cos \alpha \tag{20.94}$$

If the inductance is large enough and the load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, the input and output current waveform can be considered constant:

$$i_o(t) = \frac{2\sqrt{2}V_{in}}{\pi R} \cos \alpha \tag{20.95}$$

The input and output current average value is

$$I_{o-av} = \frac{\sqrt{2}V_{in}}{\pi R}(1 + \cos \alpha) \tag{20.96}$$

20.6.9 Three-Phase Half-Wave Rectifier with Resistive Load

A three-phase half-wave thyristor rectifier with a resister R is shown in Figure 20.25. This rectifier is operating in quadrant I only. The rectified output waveform is repeating in the frequency 3ω. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input line-to-neutral (between phase a and N) voltage is

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$$v_{aN}(t) = \sqrt{2}V_{in}\sin\left(\omega t - \frac{\pi}{6}\right) \tag{20.97}$$

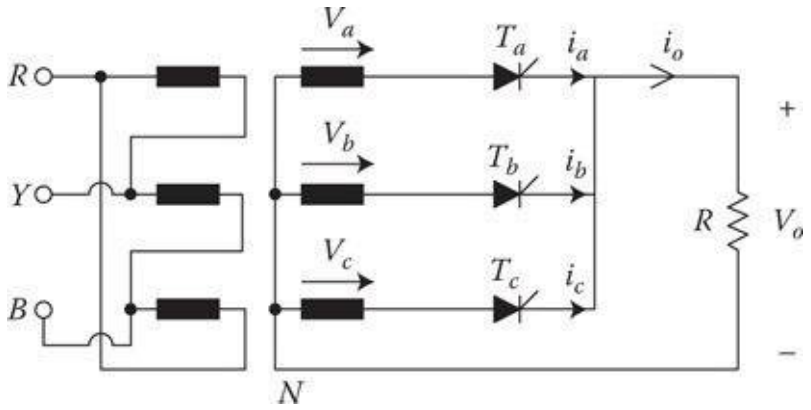


FIGURE 20.25
Three-phase half-wave semicontrolled thyristor rectifier with resister.

The output voltage is

$$v_o(t) = \begin{cases} \sqrt{2}V_{in}\sin\omega t & \alpha \le \omega t \le \dfrac{2\pi}{3} \\ 0 & \omega t > \dfrac{2\pi}{3} \end{cases} \tag{20.98}$$

The firing angle α starts from the phase cross point $\omega t = 30°$. Each thyristor's conduction period is 120°. The possible firing angle range is $0 \le a \le 150°$.

The output DC average voltage is a partial sinusoidal wave:

$$V_{o-av} = \begin{cases} \dfrac{3\sqrt{6}V_{in}}{2\pi}\cos\alpha & \alpha \le \dfrac{\pi}{6} \\ \sqrt{6}V_{in}\sqrt{\dfrac{1}{6} + \dfrac{\sqrt{3}}{8\pi}\cos 2\alpha} & \alpha > \dfrac{\pi}{6} \end{cases} \tag{20.99}$$

The output current waveform is a partial sinusoidal wave:

$$v_o(t) = \begin{cases} \dfrac{\sqrt{2}V_{in}}{R}\sin\omega t & \alpha \le \omega t \le \dfrac{2\pi}{3} \\ 0 & \omega t > \dfrac{2\pi}{3} \end{cases} \tag{20.100}$$

The output current average value is

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$$V_{o-av} = \begin{cases} \dfrac{3\sqrt{6}V_{in}}{2\pi R}\cos\alpha & \alpha \le \dfrac{\pi}{6} \\ \dfrac{\sqrt{6}V_{in}}{R}\sqrt{\dfrac{1}{6}+\dfrac{\sqrt{3}}{8\pi}\cos 2\alpha} & \alpha > \dfrac{\pi}{6} \end{cases} \tag{20.101}$$

20.6.10 Three-Phase Half-Wave Thyristor Rectifier with Inductive Load

A three-phase half-wave thyristor rectifier with an inductive load (an inductor *L* and a resister *R*) is shown in Figure 20.26. This rectifier is operating in quadrants I and IV.

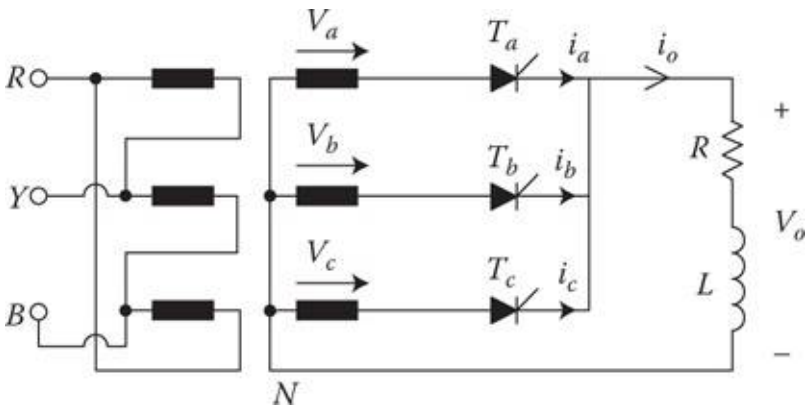


FIGURE 20.26
Three-phase half-wave semicontrolled thyristor rectifier with inductive load (*L* + *R*).

The rectified output waveform is repeating in the frequency 3ω. If the inductance is large enough, the output current can be constant. The load *Z* is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

and the load time constant is $\tau = L/R \gg T/3 = 1/3f$.

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input line-to-neutral (between phases a and *N*) voltage is

$$v_{aN}(t) = \sqrt{2}V_{in}\sin\left(\omega t - \frac{\pi}{6}\right) \tag{20.97}$$

The output voltage is

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$$v_o(t) = \sqrt{2}V_{in}\sin\omega t \qquad \alpha \le \omega t \le \left(\frac{2\pi}{3} + \alpha\right) \tag{20.102}$$

The firing angle α starts from the phase cross point $\omega t = 30°$. The possible firing angle range is $0 \le \alpha \le 180°$.

The output DC average voltage is

$$V_{o-av} = \frac{3\sqrt{6}V_{in}}{2\pi}\cos\alpha \tag{20.103}$$

If the inductance is large enough and the load time constant $\tau = L/R$ is larger than the half-cycle $T/2 = 1/2f$, the output current waveform can be considered constant:

$$i_o(t) = \frac{3\sqrt{6}V_{in}}{2\pi R}\cos\alpha \tag{20.104}$$

The output current average value is

$$I_{o-av} = \frac{3\sqrt{6}V_{in}}{2\pi R}\cos\alpha \tag{20.105}$$

20.6.11 Three-Phase Full-Wave Thyristor Rectifier with Resistive Load

A three-phase full-wave thyristor rectifier with a resister R is shown in Figure 20.27. This rectifier is operating in quadrant I only. The rectified output waveform is repeating in the frequency 6ω. The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

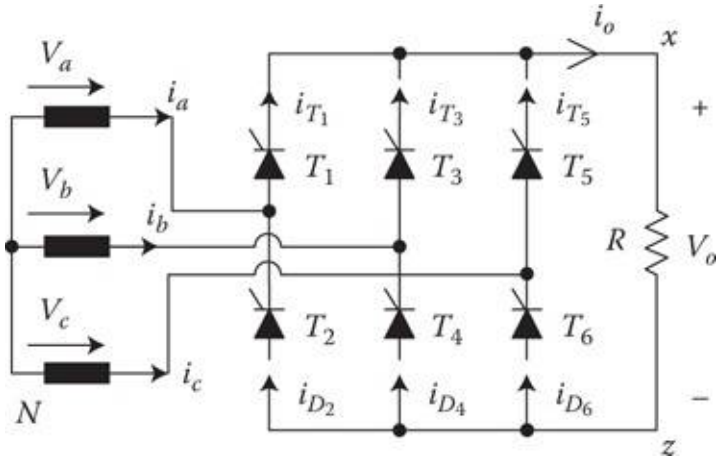


FIGURE 20.27
Three-phase full-wave thyristor rectifier with resister (R).

The input line-to-line (between phase a and phase c) voltage is

$$v_{ac}(t) = \sqrt{6}V_{in}\sin\left(\omega t - \frac{\pi}{6}\right) \tag{20.97}$$

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The output voltage is

$$v_o(t) = \begin{cases} \sqrt{6}V_{in}\sin\omega t & \alpha \le \omega t \le \dfrac{2\pi}{3} \\ 0 & \omega t > \dfrac{2\pi}{3} \end{cases} \tag{20.106}$$

The firing angle α starts from the phase cross point ωt = 30°. Each thyristor maximum conduction period is 120°. The possible firing angle range is $0 \le \alpha \le 150°$.

The output DC average voltage is

$$V_{o-av} = \begin{cases} \dfrac{3\sqrt{6}V_{in}}{\pi}\cos\alpha & \alpha \le \dfrac{\pi}{6} \\ 2\sqrt{6}V_{in}\sqrt{\dfrac{1}{6}+\dfrac{\sqrt{3}}{8\pi}\cos 2\alpha} & \alpha > \dfrac{\pi}{6} \end{cases} \tag{20.107}$$

The output current waveform is a partial sinusoidal wave:

$$v_o(t) = \begin{cases} \dfrac{\sqrt{6}V_{in}}{R}\sin\omega t & \alpha \le \omega t \le \dfrac{2\pi}{3} \\ 0 & \omega t > \dfrac{2\pi}{3} \end{cases} \tag{20.108}$$

The output current average value is

$$I_{o-av} = \begin{cases} \dfrac{3\sqrt{6}V_{in}}{2\pi R}\cos\alpha & \alpha \le \dfrac{\pi}{6} \\ \dfrac{\sqrt{6}V_{in}}{R}\sqrt{\dfrac{1}{6}+\dfrac{\sqrt{3}}{8\pi}\cos 2\alpha} & \alpha > \dfrac{\pi}{6} \end{cases} \tag{20.109}$$

20.6.12 Three-Phase Full-Wave Thyristor Rectifier with Inductive Load

A three-phase full-wave thyristor rectifier with inductive load (an inductor *L* and a resister *R*) is shown in Figure 20.28. This rectifier is operating in quadrants I and II. The rectified output waveform is repeating in the frequency 6ω. If the inductance is large enough, the output current can be constant. The load *Z* is

$$Z = R + j\omega L = \sqrt{R^2 + (\omega L)^2}\angle\phi$$

where

$$|Z| = \sqrt{R^2 + (\omega L)^2}$$

$$\phi = \tan^{-1}\frac{\omega L}{R}$$

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and the load time constant is $\tau = L/R \gg T/3 = 1/3f$.

The circuit will be analyzed for the relationship of the output to the input. The AC supply voltage is sinusoidal.

The input line-to-line (between phases a and c) voltage is

$$v_{ac}(t) = \sqrt{6}V_{in}\sin\left(\omega t - \frac{\pi}{6}\right) \tag{20.97}$$

The output voltage is

$$v_o(t) = \sqrt{6}V_{in}\sin\omega t \qquad \alpha \le \omega t \le \left(\frac{2\pi}{3} + \alpha\right) \tag{20.110}$$

The firing angle a starts from the phase cross point $\omega t = 30°$. The possible firing angle range is $0 \le a \le 180°$.

The output DC average voltage is

$$V_{o-av} = \frac{3\sqrt{6}V_{in}}{\pi}\cos\alpha \tag{20.111}$$

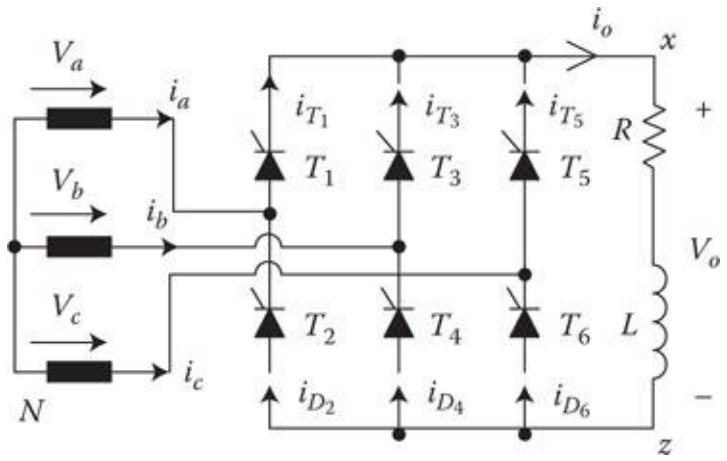


FIGURE 20.28
Three-phase full-wave thyristor rectifier with inductive load ($L + R$).

If the inductance is large enough and the load time constant $\tau = L/R$ is larger than the half-cycle $T/6 = 1/6f$, the output current waveform can be considered constant:

$$i_o(t) = \frac{3\sqrt{6}V_{in}}{\pi R}\cos\alpha \tag{20.112}$$

The output current average value is

$$I_{o-av} = \frac{3\sqrt{6}V_{in}}{\pi R}\cos\alpha \tag{20.113}$$

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21

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Control Circuit: EMI and Application Examples of DC/DC Converters

21.1 Introduction

During investigation of DC/DC prototypes and their characteristics, much attention is paid to the circuitry components of the converters. Actually, control components as auxiliary apparatus play important roles in DC/DC converter operation. For example, the pulse-width-modulated (PWM) pulse-train generator is used to yield the switching signal to all switches of DC/DC converters.

Electromagnetic interference (EMI), electromagnetic susceptibility (EMS), and electromagnetic compatibility (EMC) have to be considered during DC/DC converter design because they affect the converter and other equipment working operation heavily.

Some particular examples of DC/DC converters are presented in this chapter to demonstrate DC/DC converter application.

21.2 Luo-Resonator

The Luo-resonator is a pulse-width-modulated (PWM) generator, which produces the PWM pulse-train switching signal used for DC/DC converters. This resonator consists of only three *operational amplifiers* (OAs) and provides a pulse train of the switching signal to control static switch-*on* or switch-*off* with adjustable frequency *f* and conduction duty *k*. Luo-resonator can be reintegrated into an application-specific integrated circuit to produce portable DC/DC converters.

The Luo-resonator is a high efficiency and simple circuit with easily adjusting frequency *f* and conduction duty *k*. Its circuit diagram is shown in Figure 21.1. It consists of three *OA*s named OA1−OA3 and auxiliary. These three Type 741 OAs are integrated in a chip TL074 (which contains four OAs). Two potentiometers are applied to adjust the frequency *f* and conduction duty *k*.

The analysis of the Luo-resonator is performed under the assumption that the OA is ideal:

1. Its open-loop gain is infinity.
2. Its input impedance is infinity and output impedance is zero.
3. Its output voltage positive and negative maximum values are equal to the power supply voltages.

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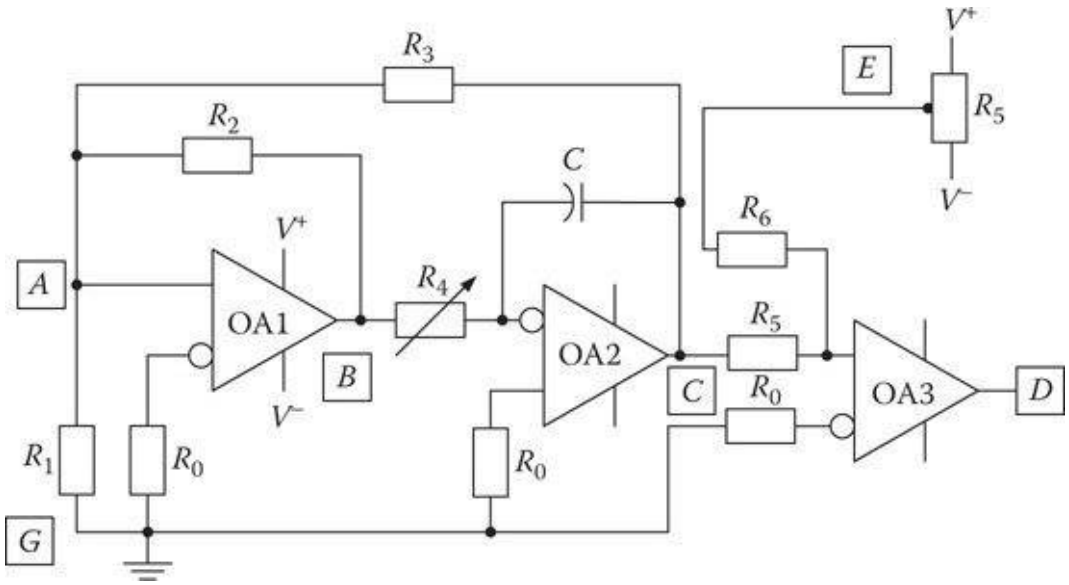


FIGURE 21.1
Luo-resonator.

21.2.1 Circuit Explanation

Type 741 OA can work with a ±3 to ±18 V power supplies, which are marked V^+, G, and V^- with $|V^-| = V^+$. OA2 in Figure 21.1 acts as the integration operation; its output V_C is a triangle waveform with regulated frequency $f = 1/T$ controlled by potentiometer R_4. OA1 acts as a resonant operation; its output V_B is a square waveform with the frequency f. OA3 acts as a comparator; its output V_D is a square waveform pulse train with regulated conduction duty k controlled by R_7.

First, the output voltage of OA1 maintained as $V_B = V^+$. In the mean time, V_B inputs to OA2 via R_4. Because of the capacitor C, the output voltage V_C of OA2 decreases toward V^- with the slope $-1/R_4C$. Voltage V_C feeds back to OA1 negatively via R_3. Voltage V_A at Point A changes from $2mV^+/(1 + m)$ downward to 0 in the period of $0 \sim 2mR_4C$. It then intends toward negative. It causes the OA1's output voltage $V_B = V^-$ at $t = 4mR_4C$ and voltage V_A jumps to

$$\frac{2mV^-}{1+m} \tag{21.1}$$

Therefore, the output voltage of OA1 jumps to $V_B = V^-$. In the mean time, V_B inputs to OA2 via R_4. Because of the capacitor C, the output voltage V_C of OA2 increases toward V^+ with the slope $1/R_4C$. Voltage V_C feeds back to OA1 negatively via R_3. Voltage V_A at Point A changes from $2mV^-/(1 + m)$ upward to 0 in the period of $0-2mR_4C$. It then intends toward positive. It causes the OA1's output voltage $V_B = V^+$ at $t = 4mR_4C$ and voltage V_A jumps to

$$\frac{2mV^+}{1+m} \tag{21.2}$$

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Voltage V_B takes the two values either V^+ or V^-.

Voltage V_C is a triangle waveform and inputs to OA3. It compares with shift signal $V_{off\text{-}set}$ regulated by the potentiometer R_7 via R_6. When $V_{off\text{-}set} = 0$, OA3 yields its output voltage V_D as a pulse train with conduction duty $k = 0.5$. Positive $V_{off\text{-}set}$ shifts the zero-cross point of voltage V_C downward; hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k > 0.5$. Vice versa, negative $V_{off\text{-}set}$ shifts the zero-cross point of voltage V_C upward; hence, OA3 yields its output voltage V_D as a pulse train with conduction duty $k < 0.5$ as shown in Figure 21.2. Conduction duty k is controlled by $V_{off\text{-}set}$ via the potentiometer R_7.

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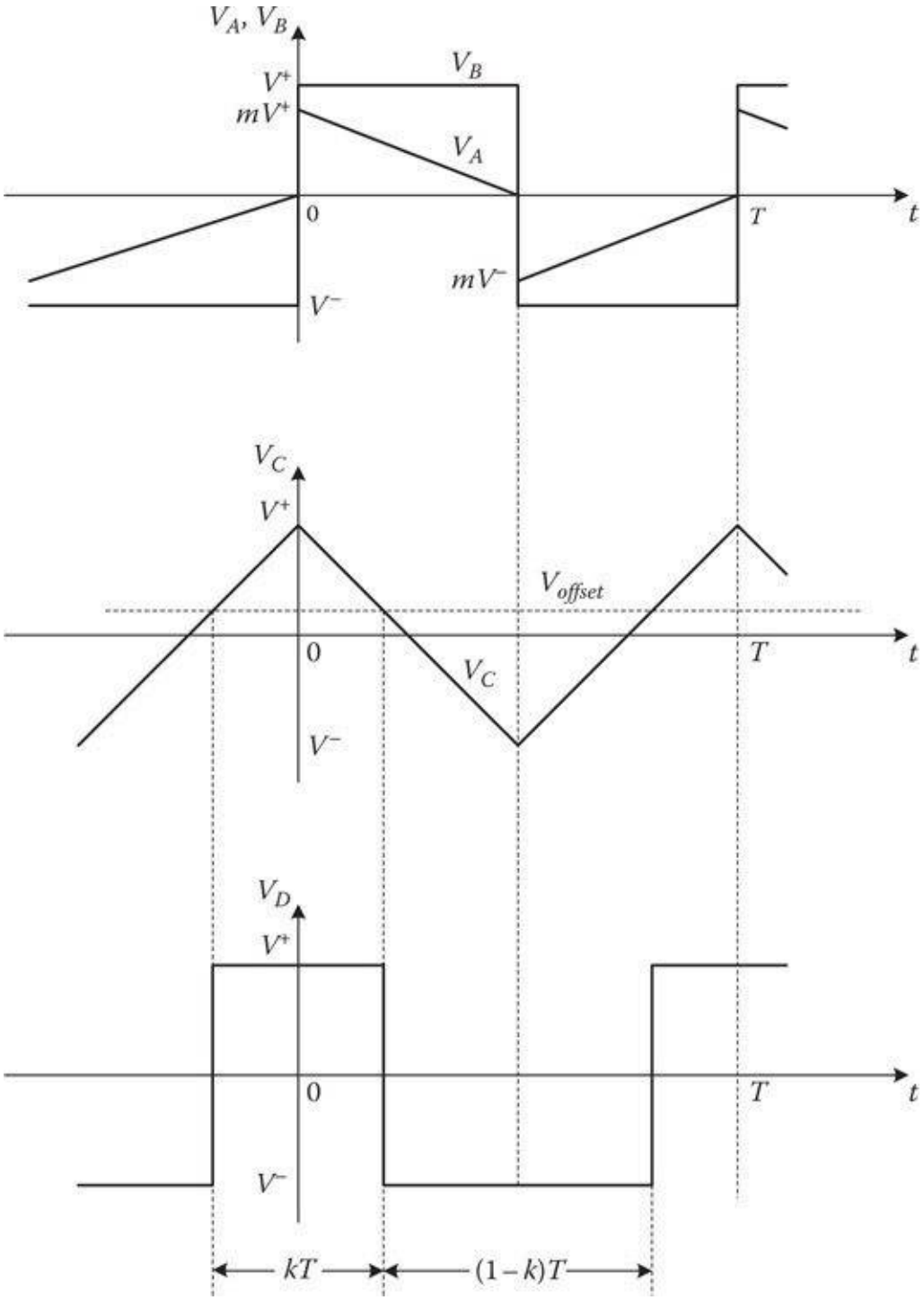


FIGURE 21.2
Voltage waveforms of Luo-resonator.

21.2.2 Calculation Formulae

The calculation formulae are obtained as follows:
Setting

$$m = \frac{R_3}{R_2} \tag{21.3}$$

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we obtain

$$f = \frac{1}{T} = \frac{1}{4mR_4C} \tag{21.4}$$

and

$$k = 0.5 + \frac{R_5 V_{offset}}{2R_6 V^+} \tag{21.5}$$

If the positive and negative maximum values of the shift voltage $V_{off\text{-}set}$ are V^+ and V^- and $R_5 = R_6$, the value of the conduction duty k is in the range between 0 and 1.0. Considering the resistance tolerance is 5%, we usually choose that resistance R_6 is slightly smaller than resistance R_5.

This PWM pulse train V_D is applied to the DC/DC converter switch such as a transistor, MOSFET or IGBT via a coupling circuit. The voltage waveforms of $V_A - V_D$ are shown in Figure 21.2.

21.2.3 Design Example

A Luo-resonator was designed as shown in Figure 21.2 with the following component values: R_0 = 10 kΩ, $R_1 = R_2 = R_5$ = 100 kΩ, $R_3 = R_6$ = 95 kΩ, R_4 = 510 Ω−5.1 kΩ, R_7 = 20 kΩ, and C = 5.1 nF.

The results are m = 0.95, frequency f = 10−100 kHz, and conduction duty k = 0−1.0.

21.2.4 Discussion

Type 741 OA of chip TL074 has the frequency bandwidth of 2 MHz. Its open-loop gain is only about 20 when this Luo-resonator works at f = 100 kHz. The waveform of V_C may be deformed slightly. It increases or decreases as an exponential curve, but linearly. However, the frequency f and conduction duty k of the output PWM pulse train are still adjustable.

Although real maximum positive- and negative-output voltages of all OA are slightly smaller than the power supply voltages V^+ and V^-, experimental results verified that Luo-resonator still works well. When power supply voltages change from ±5 to ±18 V, the variations of the frequency f and conduction duty k are less than 2%.

21.3 EMI, EMS, and EMC

EMI generally exists in all electrical and electronic equipment, especially in all DC/DC converters. Since the switching frequency applied in DC/DC converter is high, it causes significant EMI if carelessly designed. For the sake of providing the power quality, two objectives must be achieved. First, limit the high-frequency emissions that can be imposed on

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the power mains. Second, elaborate the current EMS test methods with the goal of reducing the EMS of devices on the consumer end of the power grid.

EMC has come a long way from the “black magic” approach in the early 1960s to an almost exact science today with its analytical methods, measurement techniques, and simulation software. Four decades ago, all existing handbooks on EMC could be counted on the fingers of one hand, but today they could occupy several shelves in a respectable library. This fact is caused by the significant reason that the applied frequency in 200 kHz to 5 MHz is much higher than those (5−100 kHz) of 50 years ago. EMI is a serious problem in power electronic circuits because of their fast switching characteristics. Many countries have imposed EMC regulations that must be met before electronic products can be sold legally. Because of this fact, the vital importance of this problem in all equipment including DC/DC converters is recognized.

21.3.1 EMI/EMC Analysis

The recent investigation of international regulations on EMC has prompted active research in the study of EMI emission from switched-mode power converters, which are now indispensable components in modern electronic equipment such as computers. EMI study can be focused on the following three major elements:

1. The EMI source (EMI emission)
2. The coupling path (EMI transmission)
3. The victim (EMI effect)

It is important to minimize the coupling path and to improve the EMI immunity. An effective solution for EMI suppression is to attack the problem at the EMI source. By studying power electronics circuits, the high *dv/dt* and *di/dt* involved in the switching operation of traditional hard-switched power electronics devices are the major source of *EMI emission.* Effectively reducing *dv/dt* and *di/dt* in DC/DC converters will largely attenuate the EMI emission in radio-frequency radiation.

In order to improve the energy efficiency and reliability of power converters, soft-switching techniques created in the 1980s have been proposed to reduce the following:

- The switching power losses across the power devices
- The switching stress of switched-mode power electronics circuits

Essentially, soft-switching techniques create a zero-voltage-switching (ZVS) and/or zero-current-switching (ZCS) conversion process for the power switched to turn-on and turnoff. Therefore, the instantaneous power losses across the main switches can be reduced or eliminated. Results published recently have confirmed the feasibility of such soft-switched operation.

Coupling path is a complex problem. EMI emission is created by the EMI source and radiated out by certain manner; then EMI reaches the receiver or victim. The EMI transferring process from the source to victim is called coupling path. It relies on the following factors:

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- The physical structure in both EMI source and victim
- The location and direction between EMI source and victim
- The transmission media (shielded or unshielded) between EMI source and victim
- The difference of the frequency bandwidths between EMI source and victim

Successfully cut, the coupling path can effectively reduce the EMI to other equipment (victim). Unfortunately, no matter how carefully it is done, EMI still affects all victims.

Victim is the equipment to be harmed by the EMI. In order to reduce the interference, some effective measures can be taken:

- Neat physical structure
- Distance from source
- Shielding equipment
- Large different frequency band from EMI source

We concentrate to reduce the EMI emission that may be created by DC/DC converters in further sections.

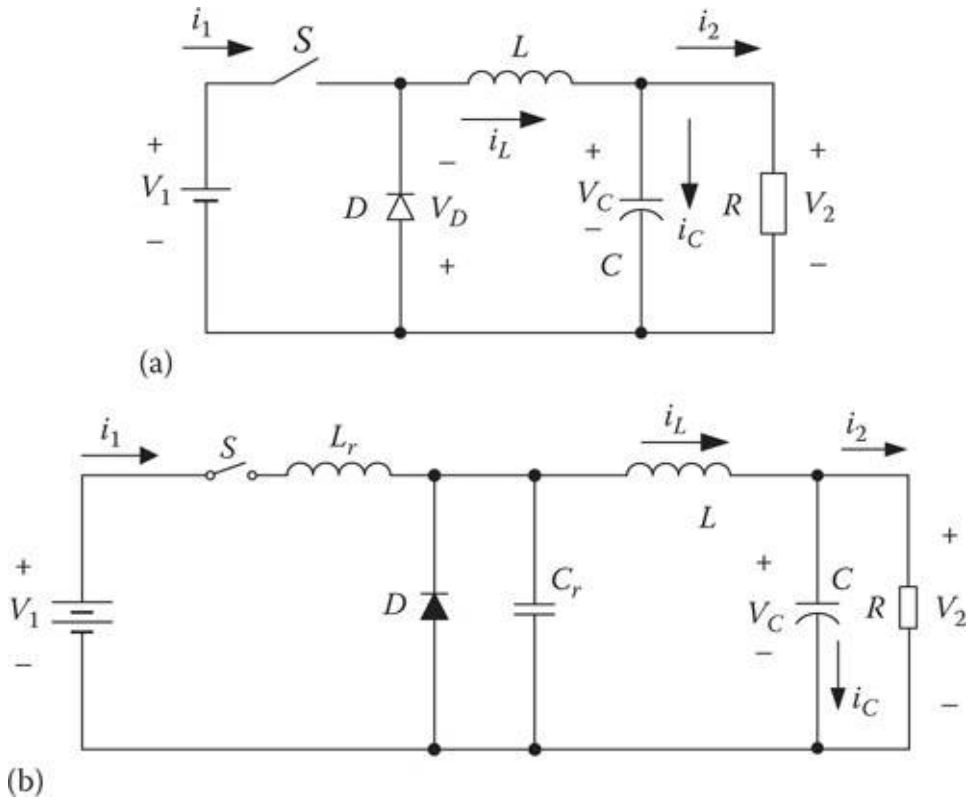


FIGURE 21.3
(a) Hard-switching and (b) soft-switching (ZCS-QR) buck converters.

21.3.2 Comparison with Hard Switching and Soft Switching

Hard-switching converters usually have large rates of *dv/dt* and *di/dt*. For example, a hard-switching buck converter in Figure 1.23a can be redrawn in Figure 21.3a. Its corresponding

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soft-switching buck converter is shown in Figure 21.3b. The soft-switching buck converter is similar to its hard-switching circuit, except that it consists of the extra resonant components L_r and C_r. Since the values of the extra resonant components L_r and C_r are usually small, they can be carefully combined in the power devices (switch S and diode D) such as snubbers. Although a snubber circuit can reduce the EMI, it generally causes additional energy loss. Thus, resonant converters not only produce less EMI but also exhibit lower energy loss than hard-switching converters with snubber circuit.

The resonant inductor L_r limits the initial current of the main switch S to provide zero-current condition during switch-on. The resonant process can provide another zero-current condition for switch-off operation. The resonant capacitor C_r can discharge through the antiparallel diode of the main switch S (it usually exists in the device), thus clamping the voltage across S to about 1 V for near-zero voltage turn-off of the main switch S.

21.3.3 Measuring Method and Results

An EMC analyzer is usually used to measure the EMI emission conducted and radiated. For example, an EMC analyzer HP 8591EM is widely applied in experiments to measure both conducted and radiated emissions. During the tests, the detector function was set to the *Comité International Special des Perturbations Radioelectriques* quasi-peak function. With the converter off, the frequency range of interest is swept to survey ambient environmental level. With the converter on, the signals measured are the ambient and the converter emission signals. The actual emission from the converter can be obtained by subtracting the ambient signal from the measured signals.

The basic converter components (L and C) in each set of hard-switched and soft-switched converters are identical and the two converters are tested under same load conditions. The magnitude of the inductor current and load current in the two converters of each type are essentially identical. The converters have no EMI filters and are not shielded. In addition, none of the converters has any enclosure. The background EMI was measured just before turning on each converter. Both the conducted EMI (from 50 kHz) and radiated EMI (from 50 kHz to 5 MHz) of the converters were recorded. In the radiated EMI measurement, the results have been corrected with the antenna. All converters were tested with an output power of about 55 W.

For both of the hard-switched and soft-switched buck converters, V_{in} = 55 V, V_o = 20 V, the switching frequency f = 50 kHz and duty cycle k = 0.4, L = 2.5 mH, C = 20 μF, and R = 7.5 Ω. For the soft-switched buck converter, L_r = 4 μH and C_r = 1 μF. Figure 21.4 shows the voltage and current waveforms of the main switch S in the hard-switched buck converter. The corresponding current FFT spectrum is shown in Figure 21.5. The switching trajectory in this case is illustrated in Figure 21.6. Figure 21.7 shows the voltage and current waveforms of the main switch S in the soft-switched buck converter. The corresponding current FFT spectrum is shown in Figure 21.8. The switching trajectory in this case is illustrated in Figure 21.9. The L-shape of the trajectory confirms the main switch S in soft-switching state.

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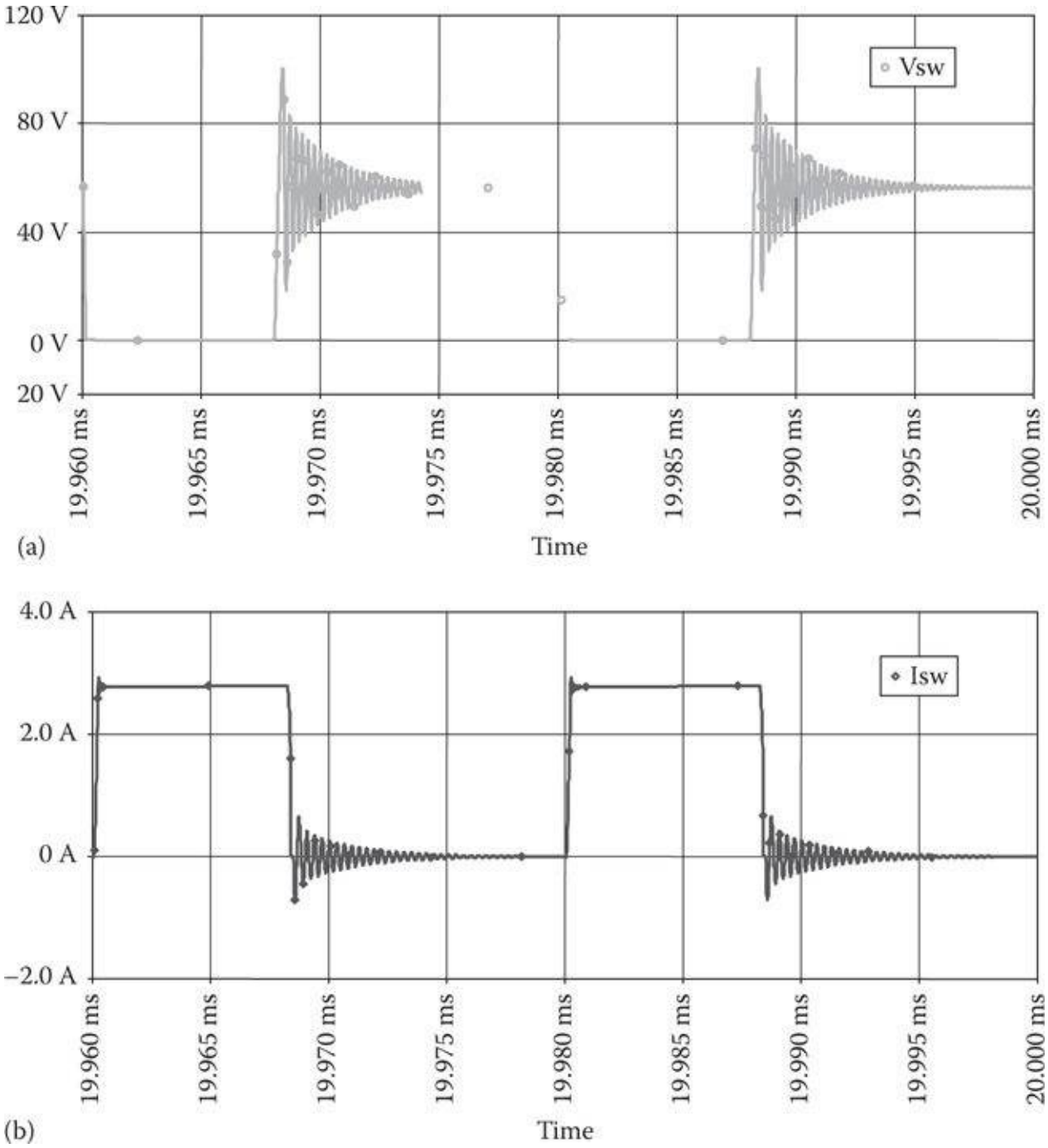


FIGURE 21.4
(a) Voltage and (b) current waveforms of hard-switching buck converter.

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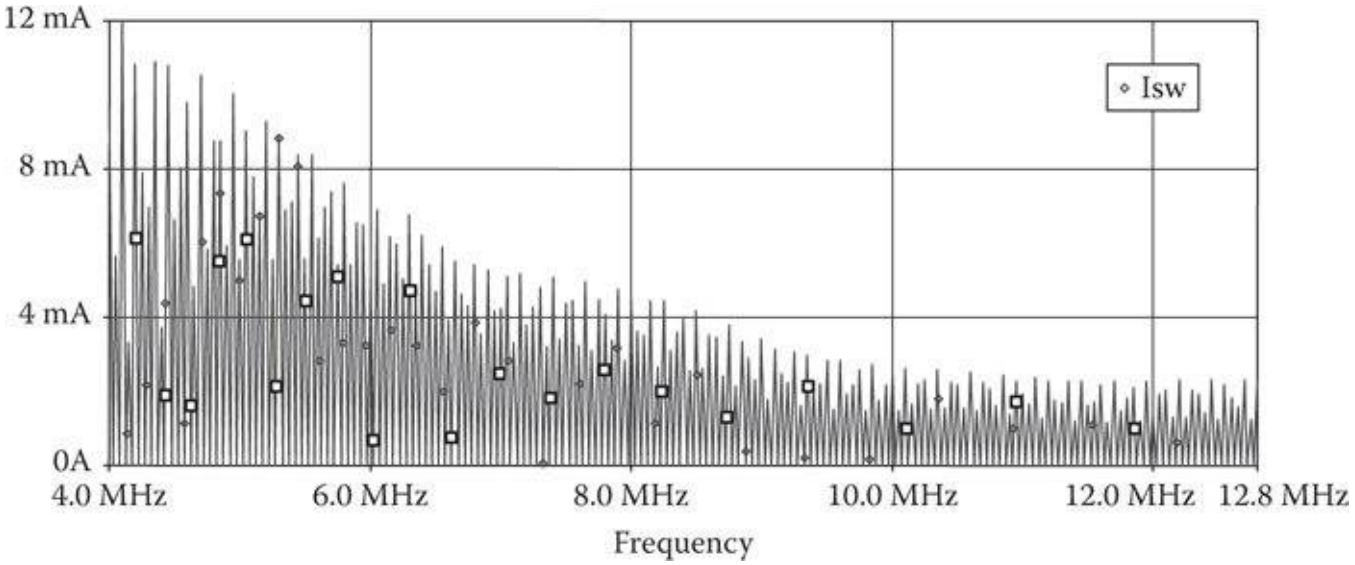


FIGURE 21.5
Current fast Fourier transform spectrum of hard-switching buck converter.

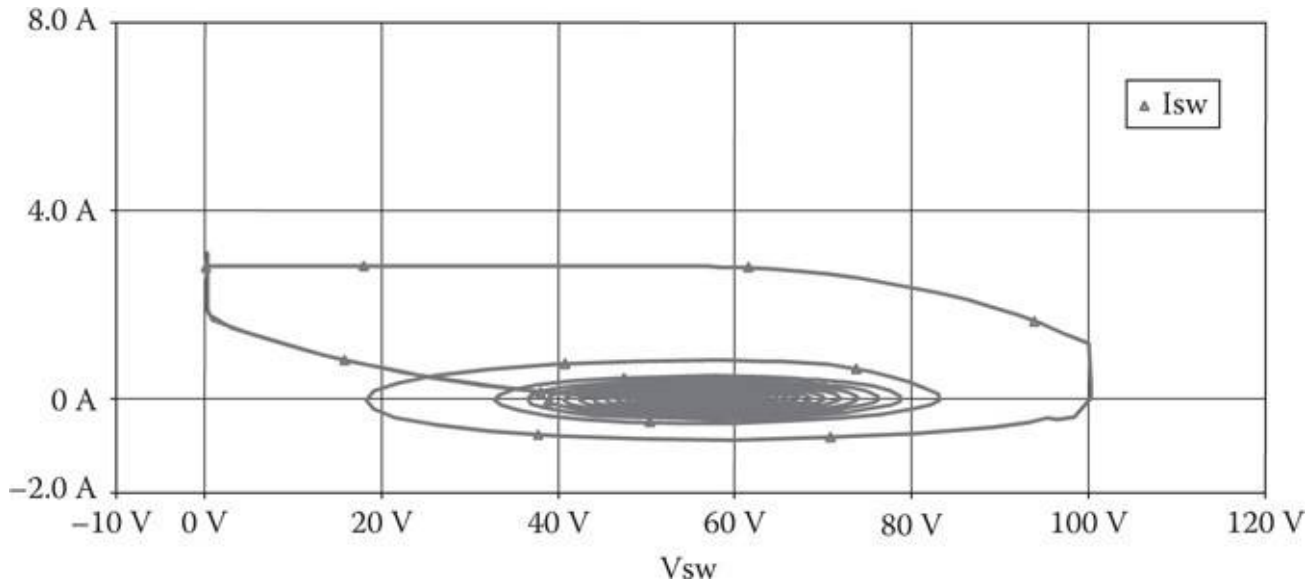


FIGURE 21.6
Switching trajectory of hard-switching buck converter.

The comparison of Figures 21.4 and 21.7 shows that the soft-switched voltage and current waveforms have very little transient ringing. The reverse recovery current of the diode in the soft-switched converter is also much less than in the hard-switched converter. The significant reduction of the transient ringing in the soft-switched converter results in much reduced *dv/dt* and *di/dt*.

The comparison of the FFT spectrums in Figures 21.5 and 21.8 shows that the soft-switched current has much lower total harmonic distortion than hard-switched current. The FFT spectrum in Figure 21.8 shows the frequency bands are lower than that in Figure 21.5. Otherwise, amplitudes of all harmonics in Figure 21.8 are lower than those in Figure 21.5.

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From this fact, EMI emission is much lower than that of the corresponding soft-switching converter.

The FFT spectrums in Figures 21.5 and 21.8 show that harmonics of the soft-switching converter are much smaller than that of the hard-switching converter. The switching trajectories in Figures 21.6 and 21.9 show that the conducted and radiated EMI emission from the hard-switching buck converter (together with the background noise) is larger than that from the soft-switching buck converter. It can be seen that the soft-switching technique effectively limits the conducted and radiated EMI emission.

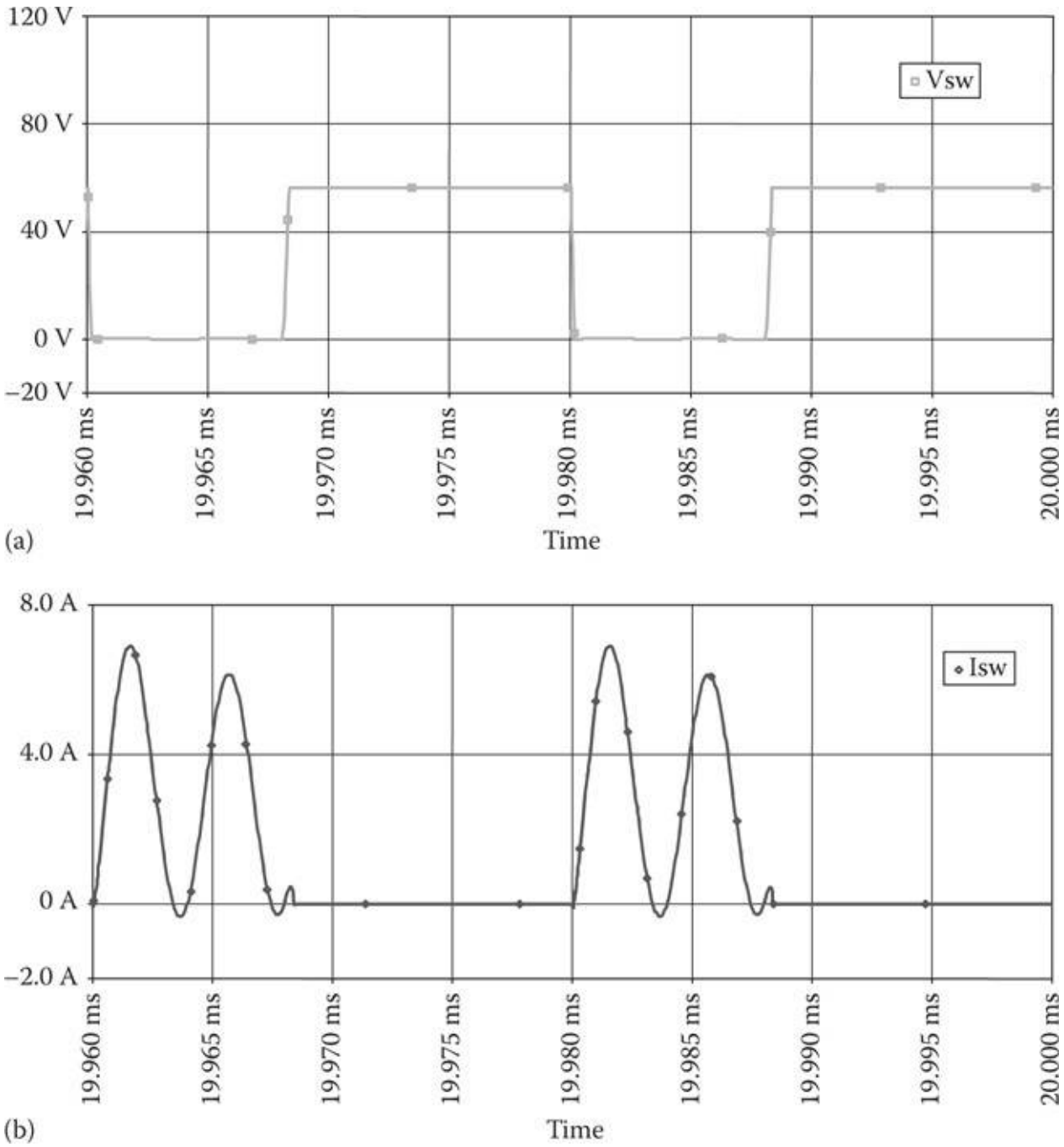


FIGURE 21.7
(a) Voltage and (b) current waveforms of soft-switching buck converter.

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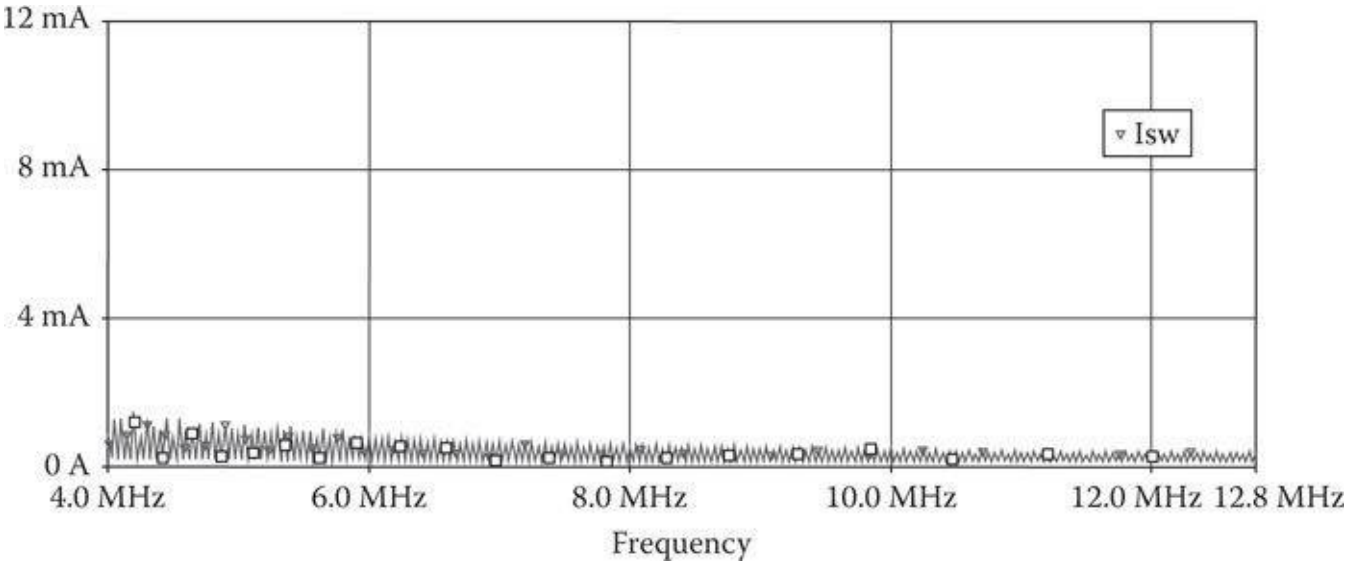


FIGURE 21.8
Current fast Fourier transform spectrum of soft-switching buck converter.

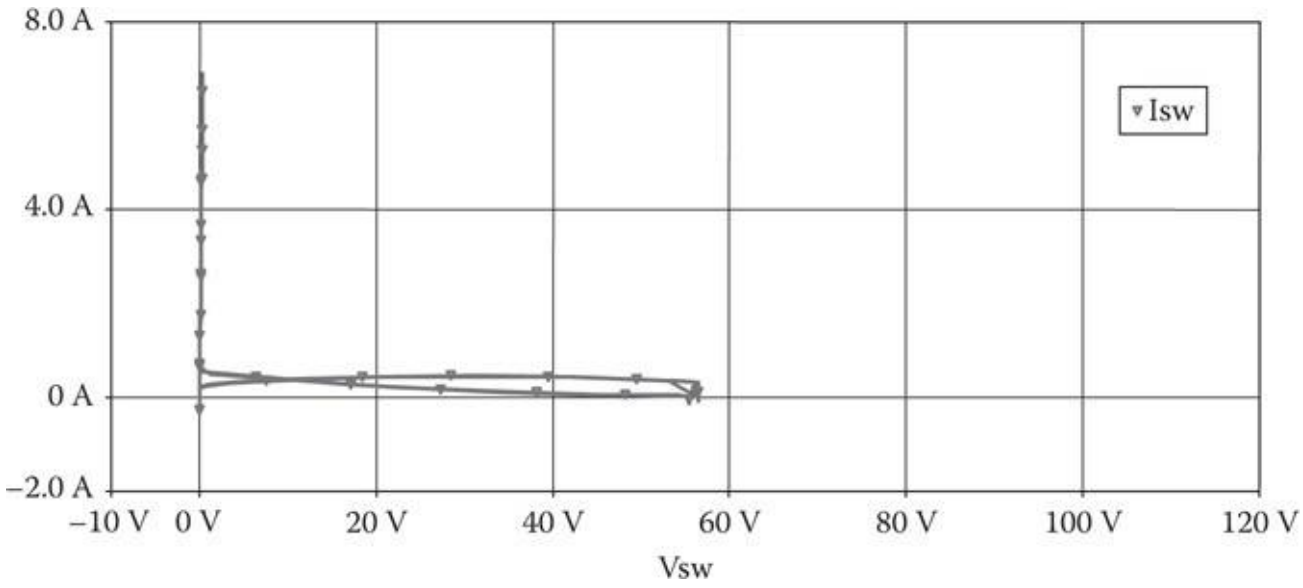


FIGURE 21.9
Switching trajectory of soft-switching buck converter.

21.3.4 Designing Rule to Minimize EMI/EMC

In order to reduce the EMI in certain stage and keep the reasonable EMC, the following rules have to be considered during designing a DC/DC converter:

- Take soft-switching techniques ZCS, ZVS, and ZT.
- Reduce the switching frequency as low as possible.
- Reduce the working power.
- Use fewer inductors.
- House DC/DC converter in a shielded enclosure.

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21.4 Some DC/DC Converter Applications

DC/DC conversion technique has been rapidly developed and has been widely applied in industrial applications and communication equipment. Some particular examples of DC/DC converters are presented here to demonstrate DC/DC converter application:

- A 5000 V insulation test bench
- MIT 42 V/14 V 3 kW dual direction DC/DC converter
- IBM 1.8 V/200 A power supply

21.4.1 5000 V Insulation Test Bench

Insulation test bench is the necessary equipment for semiconductor manufacturing organizations. An adjustable DC voltage power supply is the heart of this equipment. Traditional method to obtain the adjustable high DC voltage is a diode rectifier via a setting-up transformer. It is costly and large size with poor efficiency.

Using a positive-output Luo-converter quadruple-lift circuit, plus a general IC chip TL494, can easily implement the high output voltage (say, 36−1000 V) from a 24 V source,

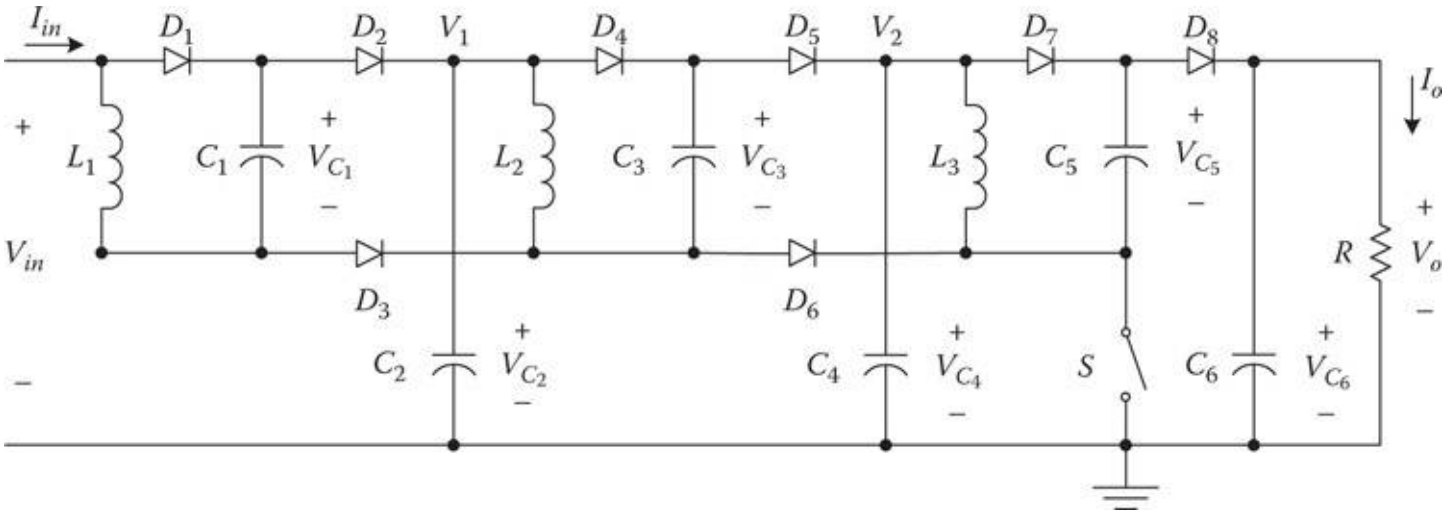


FIGURE 21.10
The 5000 V insulation test bench.

TABLE 21.1
Experimental Results of the 5000 V Test Bench

Experimental Results of the 5000 V Test Bench

Conduction duty, k	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.82
Output voltage, V_o (V)	192	226	273	244	455	648	1029	1953	5184	6760

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which is shown in Figure 2.57. If higher voltage is required, it is available to implement 192–5184 V, via a positive-output super-lift Luo-converter triple-lift circuit; this diagram is shown in Figure 21.10. This circuit is small, effective, and low cost. The output voltage can be determined by

$$V_o = \left(\frac{2-k}{1-k}\right)^3 V_{in} \tag{21.6}$$

The conduction duty cycle k is only adjusted in the range 0–0.8 to carry out the output voltage in the range of 192–5184 V. The experimental results are listed in Table 21.1. The measured data verified the advantage of this power supply.

21.4.2 MIT 42/14 V 3 kW DC/DC Converter

MIT 42/14 V 3 kW DC/DC converter was required to transfer 3 kW energy between two battery sources with 42 and 14 V. The circuit diagram is shown in Figure 21.11. This is a two-quadrant ZVS quasi-resonant converter (QRC). The current in the low-voltage side can be up to 250 A. This is a typical low-voltage strong-current converter. It is easier to carry out by ZVS-QRC.

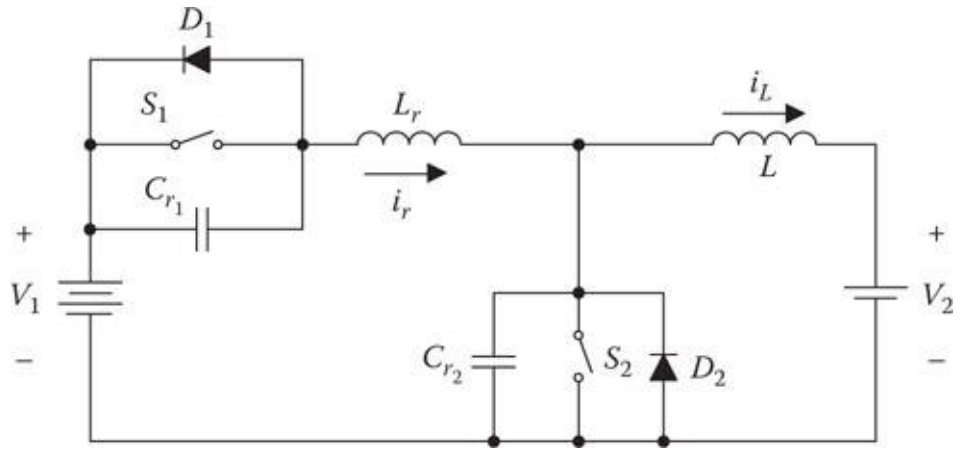


FIGURE 21.11
The MIT 42 V/14 V 3 kW dual direction DC/DC converter.

This converter consists of two sources V_1 and V_2, one main inductor L, two main switches S_1 and S_2, two reverse-paralleled diodes D_1 and D_2, one resonant inductor L_r, and two resonant capacitors C_η and C_{r2}. The working conditions are selected:

V_1 = 42 V
V_2 = 14 V
L = 470 μH
$C_\eta = C_{r2} = C_r = 1\mu F$

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$$L_r = \begin{cases} 1\ \mu\text{H} & \text{(normal operation)} \\ 9\ \mu\text{H} & \text{(low-current operation)} \end{cases}$$

Therefore,

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} = 10^6\ \text{rad/s} \tag{21.7}$$

$$Z_o = \sqrt{\frac{L_r}{C_r}} = 1\,\Omega \quad \text{(normal operation)} \tag{21.8}$$

$$\alpha = \sin^{-1}\frac{V_1}{Z_o I_2} \tag{21.9}$$

It is easy to keep the quasi-resonance when the working current $I_2 > 50$ A. If the working current is too low, the resonant inductor will take a large value to guarantee the quasi-resonance state. This converter performs two-quadrant operation:

1. *Mode A* (*quadrant I*)*:* Energy transferred from V_1 side to V_2 side
2. *Mode B* (*quadrant II*)*:* Energy transferred from V_2 side to V_1 side

Assuming the working current is I_2 = 100 A and the converter works in Mode A, the following calculations are obtained:

$$\omega_o = \frac{1}{\sqrt{L_r C_r}} = 10^6\ \text{rad/s} \tag{21.10}$$

$$Z_o = \sqrt{\frac{L_r}{C_r}} = 1\,\Omega \tag{21.11}$$

$$\alpha = \sin^{-1}\frac{V_1}{Z_o I_2} = 24.83^\circ \tag{21.12}$$

$$t_1 = \frac{V_1 C_r}{I_2} = 0.42\ \mu\text{s} \tag{21.13}$$

TABLE 21.2
Experimental Test Results of the MIT 42 V/14 Converter (with the Condition L_r = 1 μH, C_r = 1 μH, $C_{r1} = C_{r2} = 1$ μF)

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Experimental Test Results of the MIT 42 V/14 Converter (with the Condition $L_r = 1$ μH, $C_{r1} = C_{r2} = 1$ μF)

Mode	F (KHz)	I_1 (A)	I_2 (A)	I_L (A)	P_1 (W)	P_2 (W)	η (%)	PD (W/in.^{3})
A	78	77.1	220	220	3239	3080	95.1	23.40
A	80	78.3	220	220	3287	3080	93.7	23.58
A	82	81	220	220	3403	3080	90.5	24.01
B	68	220	69.9	220	3080	2939	95.3	22.28
B	70	220	68.3	220	3080	2871	93.2	22.04
B	72	220	66.6	220	3080	2797	90.8	21.77

$$t_2 = \frac{\pi + \alpha}{\omega_0} = 3.58\ \mu s \tag{21.14}$$

$$t_3 = \frac{1+\cos\alpha}{V_1} I_2 L_r = \frac{1+0.908}{42} 100 * 10^{-6} = 4.54\ \mu s \tag{21.15}$$

$$t_4 = \frac{t_1 + t_2 + t_3}{V_1/V_2 - 1} = \frac{0.42 + 3.58 + 4.54}{2} = 4.27\ \mu s \tag{21.16}$$

$$T = t_1 + t_2 + t_3 + t_4 = 0.42 + 3.58 + 4.54 + 4.27 = 12.81\ \mu s \tag{21.17}$$

$$f = \frac{1}{T} = \frac{1}{12.81} = 78.06\ \text{kHz} \tag{21.18}$$

$$k = \frac{t_3 + t_4}{T} = \frac{4.54 + 4.27}{12.81} = 0.688 \tag{21.19}$$

The volume of this converter is 270 in.^{3}. The experimental test results in full power 3 kW are listed in Table 21.2. From the tested data, a high power density 22.85 W/in.^{3} and a high efficiency 93% are obtained. Because of soft-switching operation, the EMI is low and EMS and EMC are reasonable.

21.4.3 IBM 1.8 V/200 A Power Supply

This equipment is suitable for IBM next-generation computers with power supply 1.8 V/200 A. This is a ZCS SR DC/DC Luo-converter and is shown in Figure 21.12. This converter is based on the double-current synchronous rectifier DC/DC converter plus ZCS technique. It employs a hexaploid-core flat transformer with the turn ratio N = 1/12. It has a six-unit ZCS synchronous rectifier double-current DC/DC converter. The six primary coils are connected in series, and six secondary circuits are connected in parallel. Each unit has particular input voltage V_{in} to be about 33 V and can offer 1.8 V/35 A, individually. The total output current is 210 A. The equivalent primary full current is I_1 = 17.5 A and the equivalent primary load voltage is V_2 = 130 V. The ZCS natural resonant frequency is

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$$\omega_o = \frac{1}{\sqrt{L_r C_r}} \tag{21.20}$$

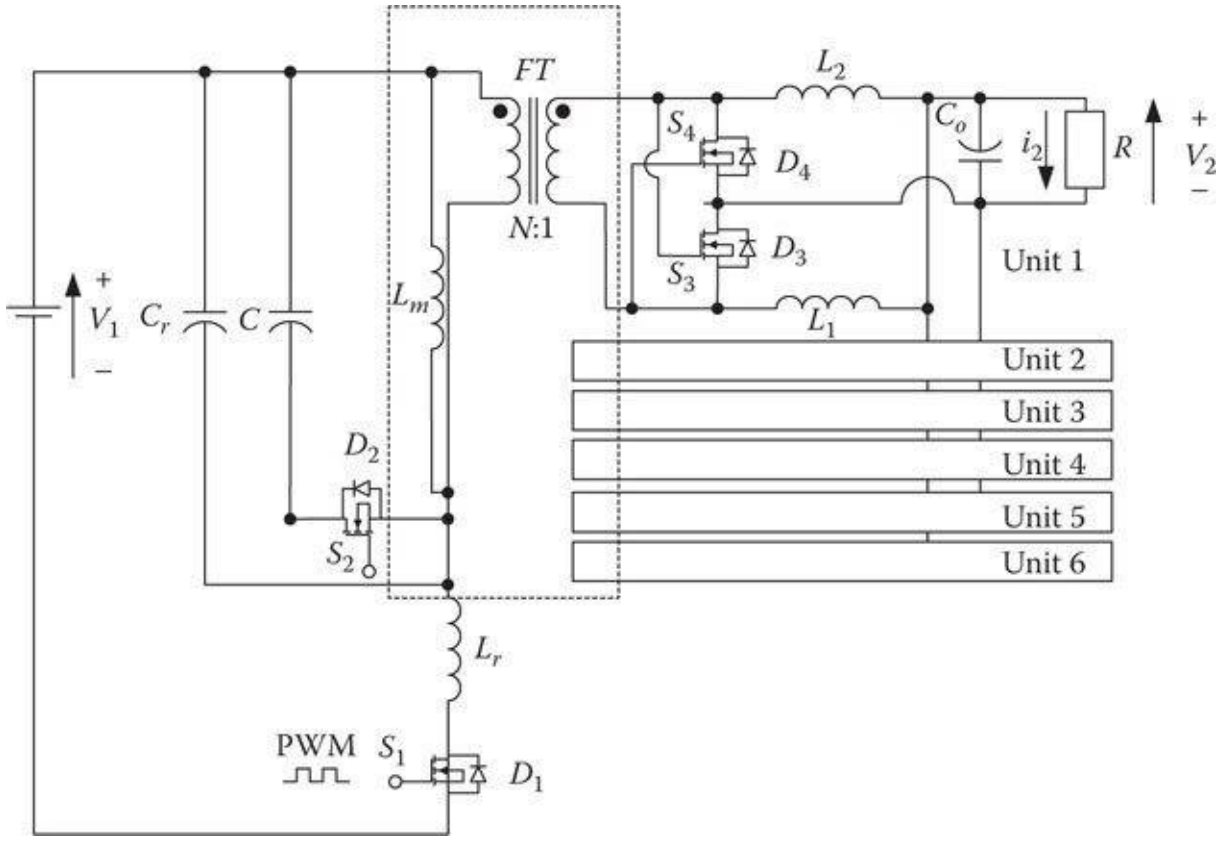


FIGURE 21.12
The IBM 1.8 V/200 A power supply.

$$Z_o = \sqrt{\frac{L_r}{C_r}} \tag{21.21}$$

$$\alpha = \sin^{-1} \frac{Z_o I_1}{V_1} \tag{21.22}$$

The main power supply is from public utility board via a diode rectifier. Therefore, V_1 is nearly 200 V, and each unit input voltage V_{in} is about 33 V. Other calculation formulae are

$$t_1 = \frac{I_1 L_r}{V_1} \tag{21.23}$$

$$t_2 = \frac{\pi + \alpha}{\omega_0} \tag{21.24}$$

$$t_3 = \frac{1 + \cos\alpha}{I_1} V_1 C_r \tag{21.25}$$

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$$t_4 = \frac{V_1(t_1+t_2)}{I_1 V_2}\left(I_1 + \frac{V}{Z_0}\frac{\cos\alpha}{\pi/2+\alpha}\right) - (t_1+t_2+t_3) \tag{21.26}$$

$$T = t_1 + t_2 + t_3 + t_4 \tag{21.27}$$

$$f = \frac{1}{T} \tag{21.28}$$

$$k = \frac{t_1+t_2}{T} \tag{21.29}$$

Real output voltage and input current are

$$V_o = kNV_1 - \left(R_L + R_S + \frac{L_m}{T}N^2\right)I_o \tag{21.30}$$

$$I_{in} = kNI_o \tag{21.31}$$

The power transfer efficiency is

$$\eta = \frac{V_o I_o}{V_{in} I_{in}} = 1 - \frac{R_L + R_S + (L_m/T)N^2}{kNV_{in}} I_o \tag{21.32}$$

The commercial unit of this power supply works in voltage closed-loop control with inner current closed loop to keep the output voltage constant. Applying frequency is arranged in the band of 200−250 kHz. The volume of the power supply is 14 in.^{3}. The transfer efficiency is about 88%–92%, and the power density is about 25.7 W/in.^{3}.

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Index

A

Absolute value, 4, 7
AC component, 529, 532, 534, 537, 542, 544, 547, 549
AC/DC converters, 32
AC/DC rectifiers, 674
Active-clamped SR Luo-converter
  demagnetizing process, 574
  equivalent circuit, 572–573
  magnetizing process, 573
  switching-off period, 574
  switching-on period, 573
Amplifier
  error, 657, 659–660
  inverting, 659
  operational, 713–714
Angular frequency, 74, 85, 96, 595, 597
Angular length, 702–703
Angular position, 529, 532, 534, 537, 542, 545, 547, 550
Angular shift-angular distance, 577, 580
Application specific integrated circuit (ASIC), 713
Arithmetic progression, 28, 30, 193
A-type chopper, 2–4, 19
Average
  charge, 195, 236
  current, 38–39, 63, 70, 78, 88, 99, 102, 109–110, 112, 119–120, 127–128, 136, 140, 145, 147, 150–152, 155, 157, 164, 171, 177–178, 182, 184, 196, 201, 214, 223, 237, 279, 313, 348, 391, 421, 424, 437, 439, 530, 533, 535, 538, 545, 550, 691
  inductor current, 459, 462, 466, 469, 473
  inductor voltages, 40, 45, 49, 52, 55, 146, 148
  input current, 196, 437–441, 448, 450–455, 460, 462, 464, 466, 468, 470–471, 473, 543, 548
  output current, 110, 119, 127, 437–441, 448, 450, 452–455, 460, 462, 464, 466, 468, 470–471, 473
  power density, 441, 451, 474, 539, 552, 559
  power transfer efficiency, 441, 539, 552, 559, 572, 574, 576, 579, 581

www.EngineeringEBooksPdf.com

source current, 67, 78, 112, 413, 417
value(s), 38, 66, 110, 230, 273–274, 308, 341, 376, 413, 416, 420, 424, 637, 649–650, 687, 693, 695, 698–699
voltage, 58, 68, 99, 102, 110, 112, 119–120, 127–129, 136, 140, 145, 147, 150–152, 156, 177–178, 182, 184, 392, 415, 418, 422, 425, 463, 467, 471, 675, 678, 682–683, 685, 687, 689, 691, 693–696, 700, 702–704, 706–710

B

Back EMF, 408, 434, 673, 682–685, 687–689, 694–695, 700–703
Bipolar current source, 593–594, 605, 619
Bipolar voltage source, 592–593, 636
Bode plot, 74, 657
Boost converters, 2
circuit diagram, 19–20
Cúk converter, 26
negative-output cascaded, 311–342
positive-output cascaded, 277–310
SEPIC, 26
voltage transfer gains, 228–230, 272–273
Boost converters, negative-output cascaded
additional series, 311
elementary circuit, 317–319
higher-stage circuit, 322
three-stage circuit, 319, 321–322
two-stage circuit, 318–320
double series, 311
elementary circuit, 317, 323
higher-stage circuit, 327
three-stage circuit, 324–327
two-stage circuit, 323–325
experimental results, 341–342
family tree, 338–339
main series, 311
elementary circuit, 311–314
higher-stage circuit, 316
three-stage circuit, 313, 315–316
two-stage circuit, 312, 314–315
multiple series, 311
elementary circuit, 333–334
higher-stage circuit, 337

www.EngineeringEBooksPdf.com

three-stage circuit, 336–337
two-stage circuit, 334–336
output voltage, 338
simulation results, 341–342
transient process, 342
triple series, 311
elementary circuit, 328–329
higher-stage circuit, 333
three-stage circuit, 330–332
two-stage circuit, 329, 331
voltage transfer gain, 338–340
Boost converters, positive-output cascaded
additional series, 277
elementary circuit, 283–285
higher-stage circuit, 288–289
three-stage circuit, 286–288
two-stage circuit, 285–287
double series, 277
elementary circuit, 284, 289
higher-stage circuit, 293–294
three-stage circuit, 291–293
two-stage circuit, 289–290, 292
experimental results, 309–310
family tree, 305–306
main series, 277
elementary circuit, 278–279
high-stage circuit, 282–283
three-stage circuit, 280–282
two-stage circuit, 279–281
multiple series, 277
elementary circuit, 300–301
higher-stage circuit, 305
three-stage circuit, 303–305
two-stage circuit, 301–302, 304
output voltage, 305
simulation results, 308–309
transient process, 310
triple series, 277
elementary circuit, 294–295
higher-stage circuit, 299–300
three-stage circuit, 297–299

www.EngineeringEBooksPdf.com

two-stage circuit, 295–296, 298
voltage transfer gain, 306–308
Boost pumps, 9, 605
Boundary
CCM/DCM, 43–44, 48, 51, 54, 57, 61, 73, 82, 94, 100, 103–104, 117, 125, 134, 137, 140, 149, 159–160, 166–167, 174–175, 179–180, 186, 350–351, 416, 419–420, 423, 426–427, 461, 464, 468, 472
condition, 47, 51, 54, 57, 60
curve, 73, 82, 93, 100, 103, 116, 124, 133, 137, 140, 160, 167, 174, 180, 186
elementary circuit, 117, 144, 160, 190
state, 43, 48, 51, 54, 57, 61
Bridge converter, 22, 24, 29
B-type chopper, 2, 4–5, 29, 407
Buck–boost converter, 2
circuit diagram, 20
mode A, 409
mode C, 411
ZCS, 533, 536
ZVS, 546, 549
Buck–boost pump, 9, 10
Buck converter, 2
circuit diagram, 19
mathematical modeling
CCM, 400
impulse interference response, 381–382, 385–389, 401
power losses, 381
unit-step function response, 381, 384–389, 401
voltage transfer gains, 228–230, 271–273, 307–308, 338, 340
ZCS, 528
ZVS, 541
Buck pump, 8

C

Capacitor–inductor (CL) filter, 594
Cascade boost converters
negative-output cascaded boost converters, 311–342
positive-output cascaded boost converters, 277–310
Cascade double Γ-CL CSRI
circuit diagram, 619–620
component voltages and currents, 620–621

www.EngineeringEBooksPdf.com

current transfer gain, 623–627
equivalent circuit, 620
experimental results, 631, 633
function analysis, 619
input impedance, 620–623
power transfer efficiency, 627–629
simulation method, 629–632
Cascade reverse double Γ-LC RPC
AC analysis
equivalent AC circuit diagram, 638–639
equivalent load resistance, 637
experimental results, 644–645
input impedance, 640, 642–644
operating principles, 637
simulation results, 644
topology and circuit diagram, 636
transfer functions, 638–639
voltage gain, 639–642
DCM, 665, 667–670
definition, 635
PWM, 635
resonance operation
CCM, 645
equivalent circuits, 646–647
modes, 645–647
principle, 646–647
state-space analysis, 647–651
small-signal model
block diagram, 651
closed-loop control system, 656–662
EDF, 653
equivalent circuit model, 655–656
harmonic approximation, 652–653
harmonic balance, 654
nonlinear state equation, 651–652
perturbation and linearization, 655, 671
specifications, 635
variable-parameter resonant converter
inductors and capacitors, 662
maximum voltage gain vs. parameter ratios, 665
resonant output voltage and THD, 665–667

www.EngineeringEBooksPdf.com

voltage transfer gain, 662–664
waveforms, 665–666
Charge
average, 195, 236
capacitor, 66, 76, 85, 110, 119, 127, 410–411, 413, 420
decrease of, 441
gate, 569
increase of, 441
variation, 70, 313
Choppers
A-type chopper, 2–4, 19
B-type chopper, 2, 4–5, 29, 407
E-type choppers, 29
first-quadrant chopper, 3–7
fourth-quadrant chopper, 4, 6–7
second-quadrant chopper, 4–7
third-quadrant chopper, 4–7
Circuit network, 74, 95
Clamp
active, 32, 570, 574, 576, 578, 580
capacitor, 572, 574
dynamic, 567–568
CL filter, *see* Capacitor–inductor filter
Closed-loop control system
block diagram, 656–657
capacitance value, 660
compensation network, 658–660
ESR, 659
open-loop system, 660–661
resistors, 657
root loci, 661–662
transfer function, 661
unity-gain crossover frequency, 658–660
VCO, 657
Comparator, 714
Conduction duty cycle, 3, 19, 22, 41, 107–108, 345–346, 348, 350, 356–357, 380, 389, 427, 430, 477, 528, 531, 533, 536, 541, 543, 546, 549, 559, 592–594, 723
Constant time-delay method, 560–562, 564
CSRI, *see* Current source resonant inverterCúk
converter, 26, 39–45
Cúk pump, 10, 12

www.EngineeringEBooksPdf.com

Current source resonant inverter (CSRI)
cascade double Γ-CL
circuit diagram, 619–620
component voltages and currents, 620–621
current transfer gain, 623–627
equivalent circuit, 620
experimental results, 631, 633
function analysis, 619
input impedance, 620–623
power transfer efficiency, 627–629
simulation method, 629–632
Π-CLL
component voltages and currents, 607–608
current source, 605
current transfer gain, 610–615
DC current component, 618
equivalent circuit, 605–606
frequency, 618
function analysis, 607
input impedance, 607, 609–611
load, 606
power transfer efficiency, 616
pump circuits, 605
resonant circuit, 605–606
simulation method, 616–617

D

DC/AC inverters, 1
DC component, 529, 532, 534, 537, 542, 544, 547, 549
DEC, *see* Double/enhanced circuit
Diode rectifiers
single-phase full-wave rectifier
back EMF load, 687–689
center-tap circuit, 685–686
Graetz circuit, 685–686
R-C load, 689–691
resistive load, 685–687
single-phase half-wave rectifier
back EMF plus inductive load, 683–685
back EMF plus resistor load, 682–683

www.EngineeringEBooksPdf.com

capacitive filter, 675–679
forward bias, 673
inductive load, 678, 680
pure inductive load, 681–682
resistive load, 674–675
reverse bias, 673–674
three-phase full-bridge rectifier, 695–696
three-phase half-bridge rectifier
back EMF load, 693–695
resistive load, 692–693
Domain, 597
Double-current SR Luo-converter
demagnetizing process, 576
equivalent circuit, 574–575
magnetizing process, 575
switching-off period, 576
switching-on period, 575
Double/enhanced circuit (DEC), 16, 18, 200
Double-output (D/O) Luo-converters, 25–26, 431
boundaries, 189–190
current variation ratio, 154
elementary circuit, 191
DCM, 156, 158–161
equivalent circuit, 155
negative conversion path, 157–159, 188
positive conversion path, 155–157, 187–188
filling efficiency, 190
freewheeling diode current variation, 189
negative path, 154, 188
output voltages, 189–190
positive path, 153–154, 187–188
quadruple-lift circuit, 191
DCM, 185–187
equivalent circuit, 182
negative conversion path, 183–185, 188
positive conversion path, 181–183, 188
re-lift circuit, 191
DCM, 169, 171, 174–175
equivalent circuit, 168
negative conversion path, 171–174, 188
positive conversion path, 169–171, 188

www.EngineeringEBooksPdf.com

self-lift circuit, 191
DCM, 163–164, 166–168
equivalent circuit, 162
negative conversion path, 164–166, 188
positive conversion path, 162–164, 188
triple-lift circuit, 191
DCM, 179–181
equivalent circuit, 176
negative conversion path, 177–179, 188
positive conversion path, 176–177, 188
voltage transfer gain, 154, 189
voltage variation ratio, 154–155

E

EDF, *see* Extended describing function
Efficiency, 616, 618
Electromagnetic compatibility (EMC), 716–718
Electromagnetic interference (EMI)
EMC, 716–718
5000 V insulation test bench, 722–723
hard-switching, 718–722
IBM 1.8 V/200 A power supply, 725–727
Luo-resonator
analysis, 713
calculation formulae, 715–716
design, 716
open-loop gain, 716
operational amplifier, 713–715
MIT 42/14 V 3 kW DC/DC converter, 723–725
soft-switching, 718–722
Electromagnetic susceptibility (EMS), 713
EMC, *see* Electromagnetic compatibility
EMI, *see* Electromagnetic interference
EMS, *see* Electromagnetic susceptibility
Energy factor (EF), power DC/DC converters
average current, 391
capacitor–inductor stored energy ratio (CIR), 390
discontinuous capacitor voltage, 391–392
discontinuous inductor current, 391
filling coefficients, 391–392

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inductor stored energy/energy losses ratio (ILR), 390
pumping energy (PE), 389
stored energy (SE), 390
total variation of stored energy, 392
variation energy factor (EF_v), 392
variation of stored energy in capacitor, 391
variation of stored energy in inductor, 390
VR, 390
Equivalent load resistance, 637
Equivalent series resistor (ESR), 659
E-type choppers, 29
Exponential function, 75, 85, 98, 102, 117, 127, 135, 138, 176, 178, 181, 183, 437, 439
Extended describing function (EDF), 653

F

Family tree, 1, 33
negative-output cascaded boost converters, 338–339
negative-output multiple-lift push–pull switched-capacitor Luo-converters, 521–522
negative-output super-lift Luo-converters, 270–271
positive-output cascaded boost converters, 305–306
positive-output multiple-lift push-pull switched-capacitor Luo-converters, 497–498
positive-output super-lift Luo-converters, 227
split capacitors, positive-output super-lift Luo-converters, 371–372
split inductors, positive-output super-lift Luo-converters, 371–372
Fast Fourier transform (FFT), 601–602, 627, 629–632, 720–721
Fifth-generation DC/DC converters, 31–32; *see also* Synchronous rectifier DC/DC converters
Filters
band-pass, 592, 615, 627
capacitor-inductor, 694
inductor current, 154
low-pass filter, 24–25, 41, 47, 50, 53, 56, 60, 65, 67, 110, 120, 129, 165, 172, 413, 417, 568, 584–585, 592, 594, 605, 617, 632, 636
network, 32
output, 58, 659
Π-type, 108, 153–154, 161, 169, 176, 181
two-element, 595
Firing
angle, 697, 700, 702–703, 707–710
pulse, 697
First-generation DC/DC converters

www.EngineeringEBooksPdf.com

developed, 25–28
fundamental, 19–22
SL converters, 28
transformer-type, 22–24
VL converters, 28
First-quadrant chopper, 3–7
5000 V insulation test bench, 722–723
Flat transformer SR Luo-converter
demagnetizing process, 571–572
equivalent circuit, 570
magnetizing process, 571
switching-off period, 572
switching-on period, 571
Flyback converter, 23–24
Flyback pump, 12–13
Forward braking process, 2
Forward converter, 22–23
dynamic clamp circuit, 567–568
efficiencies, 567–568
Forward motoring operation, 2, 29, 442–447, 456
Forward pump, 12–13
Forward regenerating operation, 2–3
Forward running, 2, 29
Forward starting process, 2
Forward synchronous rectifier (FSR), 569
Four-element resonant power converter (RPC), 584–585, 587–591
Four-quadrant SC DC/DC converter
mode A (forward motoring)
circuit description, 443–444
experimental results, 451
mode A1, 447–449
mode A2, 449–451
mode B (forward regenerative braking)
circuit description, 444–445
mode B1, 452–453
mode B2, 454–456
mode C (reverse motoring), 445–446, 456
mode D (reverse regenerative braking), 446–447, 456
Four-quadrant SI DC/DC Luo-converter
experimental results, 474
mode A (forward motoring)

www.EngineeringEBooksPdf.com

circuit description, 457–458
continuous mode, 459–461
discontinuous mode, 461–463
switch status, 457
mode B (forward regenerative braking)
circuit description, 457–458
continuous mode, 463–464
discontinuous mode, 464–466
switch status, 457
mode C (reverse motoring)
circuit description, 458
continuous mode, 467–468
discontinuous mode, 468–470
switch status, 457
mode D (reverse regenerative braking)
circuit description, 458–459
continuous mode, 470–472
discontinuous mode, 472–474
switch status, 457
Four-quadrant ZCS quasi-resonant Luo-converters
experimental results, 538–539
mode A, 526–531
mode B, 526–527, 531–533
mode C, 526–527, 533–536
mode D, 526–527, 536–538
switch status, 526, 528
Four-quadrant ZT quasi-resonant Luo-converters
design considerations, 560–562, 564
experimental results, 559, 563
mode A, 552–555
mode B, 552–553, 555–556
mode C, 552–553, 557–558
mode D, 552–553, 558–559
simulation results, 558–563
switch/diode status, 553
Four-quadrant ZVS quasi-resonant Luo-converters
experimental results, 551–552
mode A, 539–543
mode B, 539–540, 543–546
mode C, 539–540, 546–548
mode D, 539–540, 549–551

www.EngineeringEBooksPdf.com

switch status, 539, 541
Fourth-generation DC/DC converters
high-frequency-link integral-half-cycle converters, 30
load-resonant converters, 30
resonant-DC-link converters, 30
resonant-switch converters, 30
ZCS-QRCs, 31
ZT converters, 31
ZVS-QRCs, 31
Fourth-quadrant chopper, 4, 6–7
Frequency
chopping, 3, 19
domain (ω-domain), 607
fundamental, 615–616, 627
mono-resonance, 539, 552
normal angular, 74, 85, 96
operation, 496
relevant, 595–596, 610, 612, 622, 624, 628
repeating, 65, 108, 153, 407, 427, 431, 526, 569, 592–594, 687, 689, 693–696
resonance, 528, 531, 533, 536, 539, 541, 544, 547, 549, 639
switch, 43, 107–108, 193, 235, 277, 311, 346, 359, 380, 389, 391, 430–431, 433, 441–442, 447, 449, 451–452, 454, 461, 474, 526, 539, 552, 559, 605, 607, 619, 635, 639–640, 642, 644, 651–652, 654–655, 662–663, 665, 668–669, 716, 719, 722
unity-gain crossover, 657–661
variable, 38, 145
ZCS resonant, 577
ZVS resonant, 579
FSR, *see* Forward synchronous rectifier

G

Gain
current transfer, 596, 602, 608, 610, 612, 618, 621, 623–626, 629–630, 632, 634
voltage transfer, 28, 229–230, 272–273, 307–308, 340, 639–644
Gauss theorem, 74, 84, 95, 97
Graetz bridge, 685–686

H

Half-bridge converter, 24
Half-bridge diode rectifier, 692–695
Half-wave rectifier

www.EngineeringEBooksPdf.com

single-phase, 697–703
three-phase, 706–708
Hard-switching, 718
Harmonic approximation, 652–653
Harmonic balance, 654
Higher-order harmonics, 627, 640
High-voltage-regulated power supply (HVRPS), 152–153
Hong function, 106, 143, 190, 206, 212, 219, 226, 252, 345

I

IBM 1.8 V/200 A power supply, 725–727
IGBT, *see* Insulated-gate bipolar transistor
Imaginary axis, 95, 97
Imaginary poles, 74, 84, 95–97
Impedance
infinite, 605
input, 595–596, 607, 620, 639–644
normalized, 350, 352, 529, 531, 533, 537, 542, 544, 547, 549, 577, 580
output, 651, 713
simplified, 609–615, 621–627
Instantaneous values, 71–72, 80–82, 91–93, 115–116, 123–124, 131–133
Insulated-gate bipolar transistor (IGBT), 3, 38, 393, 716

J

Junction
capacitor, 554, 561, 564
n-p, 697
n-p-n, 697
p-n, 697
p-n-p, 697

L

Laplace operator, 74, 83, 95, 380, 382, 394, 638
Laplace transforms, 74, 83, 95, 379, 597
Large-scale integrated chip (LSIC), 32
Left hand half plane/left-hand half-plane, 83, 97, 380, 397
Luo-converters, multiple-quadrant operation
application, 407
conduction duty, 431

www.EngineeringEBooksPdf.com

DCM, 430
vs. double-output Luo-converter, 431
experimental results, 429–430
general description, 407–408
mode A
circuit explanation, 409–410, 413–414
discontinuous region, 416
switch status, 412
variations of currents and voltages, 415–416
mode B
circuit explanation, 410, 416–418
discontinuous region, 419–420
switch status, 412
variations of currents and voltages, 418–419
mode C
circuit explanation, 411, 420–422
discontinuous region, 423
switch status, 412
variations of currents and voltages, 422–423
mode D
circuit explanation, 411–412, 424–425
discontinuous region, 427
switch status, 412
variations of currents and voltages, 425–426
simulation results, 427–429
switching frequency, 431
Luo-converters, negative-output multiple-lift push-pull switched-capacitor
additional series
elementary circuit, 507
higher-order lift circuit, 510
re-lift circuit, 508
triple-lift circuit, 509
enhanced series
elementary circuit, 507, 510
higher-order lift circuit, 512
re-lift circuit, 510–511
triple-lift circuit, 511–512
experimental results, 523
family tree, 521–522
main series
elementary circuit, 504

www.EngineeringEBooksPdf.com

higher-order lift circuit, 506
re-lift circuit, 504–505
triple-lift circuit, 505–506
multiple-enhanced series
elementary circuit, 517, 520
higher–order lift circuit, 521
re-lift circuit, 518, 520
triple-lift circuit, 519–520
output voltage, 521
re-enhanced series
elementary circuit, 513, 516
higher-order lift circuit, 516
re-lift circuit, 514, 516
triple-lift circuit, 515–516
simulation results, 521–522
Luo-converters, negative-output super-lift
additional series, 235
elementary circuit, 243–247
higher-order lift circuit, 251–252
re-lift circuit, 245, 247–249
triple-lift circuit, 246, 249–251
enhanced series, 235
elementary circuit, 244, 252–253
higher-order lift circuit, 259
re-lift circuit, 253–256
triple-lift circuit, 254, 256–259
experimental results, 274–276
family tree, 270–271
main series, 235
elementary circuit, 236–239
higher-order lift circuits, 243
re-lift circuit, 237, 239–240
triple-lift circuit, 238, 240–242
multiple-enhanced series, 235
elementary circuit, 265–266
higher-order lift circuit, 270
re-lift circuit, 267, 269
triple-lift circuit, 268–270
output voltage, 270
re-enhanced series, 235
elementary circuit, 259–260, 263

www.EngineeringEBooksPdf.com

higher-order lift circuit, 264–265
re-lift circuit, 261, 263
triple-lift circuit, 262, 264
simulation results, 273–276
voltage transfer gain, 271–273
Luo-converters, positive-output multiple-lift push-pull switched-capacitor
additional series
elementary circuit, 481
higher-order lift circuit, 483
re-lift circuit, 481–482
triple-lift circuit, 482–483
enhanced series
elementary circuit, 481, 484, 486
higher-order lift circuit, 486
re-lift circuit, 484, 486
triple-lift circuit, 485–486
experimental result, 498, 500
family tree, 497–498
main series
elementary circuit, 478
higher-order lift circuit, 480
re-lift circuit, 478–479
triple-lift circuit, 479–480
multiple-enhanced series
elementary circuit, 491, 494
higher-order lift circuit, 494
re-lift circuit, 492, 494
triple-lift circuit, 493–494
output voltage, 497
re-enhanced series
elementary circuit, 487–488
higher-order lift circuit, 490
re-lift circuit, 488, 490
triple-lift circuit, 489–490
simulation results, 497, 499
theoretical analysis, 495–496
Luo-converters, positive-output super-lift
additional series, 193
elementary circuit, 200–203
higher-order lift circuit, 206–207
re-lift circuit, 202–204

www.EngineeringEBooksPdf.com

triple-lift circuit, 203, 205–206
enhanced series, 193
elementary circuit, 201, 208–209
higher-order lift circuit, 211–212
re-lift circuit, 207, 209–210
triple-lift circuit, 208, 210–211
experimental results, 230, 232–233
family tree, 227
main series, 193
elementary circuit, 194–197
higher-order lift circuit, 199
re-lift circuit, 195, 197–198
triple-lift circuit, 196, 198–199
multiple-enhanced series, 193
elementary circuit, 220, 223
higher-order lift circuit, 226
re-lift circuit, 221, 224
triple-lift circuit, 222, 225–226
output voltage, 227
re-enhanced series, 193
elementary circuit, 212–214, 216
higher-order lift circuit, 219
re-lift circuit, 214, 216–217
triple-lift circuit, 215, 217–218
simulation results, 230–233
voltage transfer gain, 228–230
Luo-converter, ultra-lift
CCM
circuit diagram, 346–347
instantaneous values, 352–353
operation, 347–350
DCM
circuit diagram, 346–347
instantaneous values, 354–355
operation, 350–352
experimental results, 357
simulation results, 356–357
voltage transfer gains, 355
Luo-pump
negative, 10–11
negative super, 15–16, 18

www.EngineeringEBooksPdf.com

positive, 10–11
positive super, 14–15
Luo-resonator
analysis, 713
calculation formulae, 715–716
design, 716
open-loop gain, 716
operational amplifier, 713–715
LSIC, *see* Large-scale integrated chip

M

Mathematical modeling, power DC/DC converters
buck converter
CCM, 400
impulse interference response, 381–382, 385–389, 401
power losses, 381
unit-step function response, 381, 384–389, 401
impulse interference response, 381–382, 385–389
super-lift Luo-converter, 402–404
transfer function, 379
critical variation of storage energy, 397
large variation of storage energy, 397–399
small variation of storage energy, 395–397
very small variation of storage energy, 394–396
Metal-oxide-semiconductor-field-effect transistor (MOSFET)
n-channel (N-MOSFET), 65
p-channel (P-MOSFET), 65, 108, 145, 153
Mirror-symmetrical, 26, 153, 159, 174, 179, 185
MIT 42/14 V 3 kW DC/DC converter, 723–725
Modified positive output Luo-converters
application, 152–153
elementary circuit, 145–146
quadruple-lift circuit, 151–153
re-lift circuit, 147–150
self-lift circuit, 146–147
triple-lift circuit, 150–151
Multiple energy-storage element resonant power converters (x-element RPCs)
bipolar current source, 593–594
bipolar voltage source, 592–593
four-element, 584–585, 587–591

www.EngineeringEBooksPdf.com

three-element, 584–586
two-element, 583–584, 594–602
Multiple-lift push-pull switched-capacitor converters, 30
Multiple-quadrant operating Luo-converters
application, 407
conduction duty, 431
DCM, 430
vs. double-output Luo-converter, 431
experimental results, 429–430
general description, 407–408
mode A
circuit explanation, 409–410, 413–414
discontinuous region, 416
switch status, 412
variations of currents and voltages, 415–416
mode B
circuit explanation, 410, 416–418
discontinuous region, 419–420
switch status, 412
variations of currents and voltages, 418–419
mode C
circuit explanation, 411, 420–422
discontinuous region, 423
switch status, 412
variations of currents and voltages, 422–423
mode D
circuit explanation, 411–412, 424–425
discontinuous region, 427
switch status, 412
variations of currents and voltages, 425–426
simulation results, 427–429
switching frequency, 431
Multiple-quadrant soft-switching converters
ZCS quasi-resonant Luo-converters
experimental results, 538–539
mode A, 526–531
mode B, 526–527, 531–533
mode C, 526–527, 533–536
mode D, 526–527, 536–538
switch status, 526, 528
ZT quasi-resonant Luo-converters

www.EngineeringEBooksPdf.com

design considerations, 560–562, 564
experimental results, 559, 563
mode A, 552–555
mode B, 552–553, 555–556
mode C, 552–553, 557–558
mode D, 552–553, 558–559
simulation results, 558–563
switch/diode status, 553
ZVS quasi-resonant Luo-converters
experimental results, 551–552
mode A, 539–543
mode B, 539–540, 543–546
mode C, 539–540, 546–548
mode D, 539–540, 549–551
switch status, 539, 541
Multiple-quadrant switched-capacitor Luo-converters, 29–30
Multiple-quadrant ZCS quasi-resonant Luo-converters
experimental results, 538–539
mode A, 526–531
mode B, 526–527, 531–533
mode C, 526–527, 533–536
mode D, 526–527, 536–538
switch status, 526, 528
Multiple-quadrant ZT quasi-resonant Luo-converters
design considerations, 560–562, 564
experimental results, 559, 563
mode A, 552–555
mode B, 552–553, 555–556
mode C, 552–553, 557–558
mode D, 552–553, 558–559
simulation results, 558–563
switch/diode status, 553
Multiple-quadrant ZVS quasi-resonant Luo-converters
experimental results, 551–552
mode A, 539–543
mode B, 539–540, 543–546
mode C, 539–540, 546–548
mode D, 539–540, 549–551
switch status, 539, 541

N

www.EngineeringEBooksPdf.com

Natural resonant frequency, 571, 573, 575, 584–585, 644, 662, 665
Negative Luo-pump, 10–11
Negative-output (N/O) cascaded boost converters
  additional series, 311
    elementary circuit, 317–319
    higher-stage circuit, 322
    three-stage circuit, 319, 321–322
    two-stage circuit, 318–320
  double series, 311
    elementary circuit, 317, 323
    higher-stage circuit, 327
    three-stage circuit, 324–327
    two-stage circuit, 323–325
  experimental results, 341–342
  family tree, 338–339
  main series, 311
    elementary circuit, 311–314
    higher-stage circuit, 316
    three-stage circuit, 313, 315–316
    two-stage circuit, 312, 314–315
  multiple series, 311
    elementary circuit, 333–334
    higher-stage circuit, 337
    three-stage circuit, 336–337
    two-stage circuit, 334–336
  output voltage, 338
  simulation results, 341–342
  transient process, 342
  triple series, 311
    elementary circuit, 328–329
    higher-stage circuit, 333
    three-stage circuit, 330–332
    two-stage circuit, 329, 331
  voltage transfer gain, 338–340
Negative-output (N/O) Luo-converters, 25
  boundaries, 142–144
  common formulae, 142
  current variation ratio, 109, 142
  elementary circuit, 144
    average voltages and currents, 110, 112–113
    circuit description, 110–111

www.EngineeringEBooksPdf.com

DCM, 111, 116–117
equivalent circuits, 110–111
instantaneous current and voltage values, 115–116
variations of currents and voltages, 113–115
filling efficiency, 143
freewheeling diode current, 142
output voltage, 143
quadruple-lift circuit, 138–141, 144
re-lift circuit, 144
average voltages and currents, 127–129
circuit description, 126–127
DCM, 126, 133–134
equivalent circuits, 125–126
instantaneous current and voltage values, 131–133
variations of currents and voltages, 129–131
self-lift circuit, 144
average voltages and currents, 119–120
circuit description, 117–119
DCM, 118, 124–125
equivalent circuits, 117–118
instantaneous current and voltage values, 123–124
variations of currents and voltages, 121–123
triple-lift circuit, 135–138, 144
voltage transfer gain, 109, 142
voltage variation ratio, 109–110, 142
Negative-output (N/O) multiple-lift push-pull switched-capacitor Luo-converters
additional series
elementary circuit, 507
higher-order lift circuit, 510
re-lift circuit, 508
triple-lift circuit, 509
enhanced series
elementary circuit, 507, 510
higher-order lift circuit, 512
re-lift circuit, 510–511
triple-lift circuit, 511–512
experimental results, 523
family tree, 521–522
main series
elementary circuit, 504
higher-order lift circuit, 506

www.EngineeringEBooksPdf.com

re-lift circuit, 504–505
triple-lift circuit, 505–506
multiple-enhanced series
elementary circuit, 517, 520
higher-order lift circuit, 521
re-lift circuit, 581, 520
triple-lift circuit, 519–520
output voltage, 521
re-enhanced series
elementary circuit, 513, 516
higher-order lift circuit, 516
re-lift circuit, 514, 516
triple-lift circuit, 515–516
simulation results, 521–522
Negative-output (N/O) super-lift Luo-converters
additional series, 235
elementary circuit, 243–247
higher-order lift circuit, 251–252
re-lift circuit, 245, 247–249
triple-lift circuit, 246, 249–251
enhanced series, 235
elementary circuit, 244, 252–253
higher-order lift circuit, 259
re-lift circuit, 253–256
triple-lift circuit, 254, 256–259
experimental results, 274–276
family tree, 270–271
main series, 235
elementary circuit, 236–239
higher-order lift circuits, 243
re-lift circuit, 237, 239–240
triple-lift circuit, 238, 240–242
multiple-enhanced series, 235
elementary circuit, 265–266
higher-order lift circuit, 270
re-lift circuit, 267, 269
triple-lift circuit, 268–270
output voltage, 270
re-enhanced series, 235
elementary circuit, 259–260, 263
higher-order lift circuit, 264–265

www.EngineeringEBooksPdf.com

re-lift circuit, 261, 263
triple-lift circuit, 262, 264
simulation results, 273–276
voltage transfer gain, 271–273
Negative push-pull pump, 15–17
Negative super Luo-pump, 15–16, 18
N-MOSFET, *see* Metal-oxide-semiconductor field-effect-transistor, n-channel
Nonlinear state equation, 651–652
Normalized load, 38, 43–45, 48, 51, 54, 57, 61, 65, 73–74, 82–83, 93–95, 100, 104, 108, 116–117, 124–125, 133–134, 137–138, 141, 153, 160, 167, 175, 180, 186

O

OAs, *see* Operational amplifiers
Ohm's law, 675, 678, 683, 687–688, 694
Open-loop system, 660–661
Operational amplifiers (OAs), 713–714
Original point, 74

P

Π-CLL CSRI
component voltages and currents, 607–608
current source, 605
current transfer gain, 610–615
DC current component, 618
equivalent circuit, 605–606
frequency, 618
function analysis, 607
input impedance, 607, 609–611
load, 606
power transfer efficiency, 616
pump circuits, 605
resonant circuit, 605–606
simulation method, 616–617
Period
repeating, 3, 19, 31, 65, 71, 108, 112, 119, 127, 153, 346, 407, 531, 533, 536, 538, 543, 546, 548, 551, 571, 575
switching, 38, 47, 50, 56–57, 60, 277, 311, 359, 389, 434, 436–437, 439, 443, 456, 636, 645, 647
switch-off, 31, 39, 45–47, 49, 52, 55–58, 62, 64–65, 70, 77–78, 80, 86–88, 91, 108–109, 146, 149, 153, 194, 197, 237, 241, 244, 278, 280, 285, 289, 295, 302, 312, 314–315, 317,

www.EngineeringEBooksPdf.com

319, 324, 346, 361–362, 364, 367, 407, 437, 439, 448, 450, 452, 454, 477–478, 503, 528, 531
switch-on, 39–40, 45–46, 48–49, 52, 55, 58, 62, 65, 67, 77–78, 86–88, 91, 108, 112, 146, 149, 153, 194, 197–198, 200, 204–205, 209, 236, 239, 241, 244, 249, 257, 278, 283, 285, 287, 292, 294–295, 298, 300, 312, 314–315, 317, 319, 321, 326, 346, 361–362, 364, 367, 407, 437, 439, 448, 450, 452, 454, 477, 503, 541, 543, 546, 549
P-MOSFET, *see* Metal-oxide-semiconductor field-effect-transistor, p-channel
Poles
conjugate complex, 74, 84, 95, 97
imaginary, 74, 84, 95–97
negative real, 74, 84, 95, 97
pair of conjugate complex poles, 74, 84, 95, 97
real, 74, 84, 95, 97, 395–397
Positive buck-boost converter, 21–22
Positive Luo-pump, 10–11
Positive-output (P/O) buck–boost converter, 2
Positive-output (P/O) cascaded boost converters
additional series, 277
elementary circuit, 283–285
higher-stage circuit, 288–289
three-stage circuit, 286–288
two-stage circuit, 285–287
double series, 277
elementary circuit, 284, 289
higher-stage circuit, 293–294
three-stage circuit, 291–293
two-stage circuit, 289–290, 292
experimental results, 309–310
family tree, 305–306
main series, 277
elementary circuit, 278–279
high-stage circuit, 282–283
three-stage circuit, 280–282
two-stage circuit, 279–281
multiple series, 277
elementary circuit, 300–301
higher-stage circuit, 305
three-stage circuit, 303–305
two-stage circuit, 301–302, 304
output voltage, 305
simulation results, 308–309

www.EngineeringEBooksPdf.com

transient process, 310
triple series, 277
elementary circuit, 294–295
higher-stage circuit, 299–300
three-stage circuit, 297–299
two-stage circuit, 295–296, 298
voltage transfer gain, 306–308
Positive-output (P/O) Luo-converters, 25
boundaries, 105–107
common formulae, 104
conduction duty cycle, 108
current variation ratio, 65, 105
elementary circuit, 107
circuit description, 66–68
DCM, 67, 72–74
equivalent circuits, 66–67
instantaneous current and voltage values, 71–72
stability analysis, 74–75
variations of currents and voltages, 68–71
filling efficiency, 105
freewheeling diode current, 105
output voltages, 106, 108
quadruple-lift circuit, 101–104, 106
re-lift circuit, 106
average currents, 88
circuit description, 85–87
DCM, 86, 93–95
equivalent circuits, 85–86
instantaneous current and voltage values, 91–93
stability analysis, 95–97
variations of currents and voltages, 88–91
self-lift circuit, 106
average current, 78
circuit description, 76–77
DCM, 76, 82–83
equivalent circuits, 75–76
instantaneous current and voltage values, 80–82
source current, 78
stability analysis, 83–85
variations of currents and voltages, 78–80
switching frequency, 108

www.EngineeringEBooksPdf.com

triple-lift circuit, 98–101, 106
voltage transfer gain, 105
voltage variation ratio, 66, 105
Positive-output (P/O) multiple-lift push-pull switched-capacitor Luo-converters
additional series
elementary circuit, 481
higher-order lift circuit, 483
re-lift circuit, 481–482
triple-lift circuit, 482–483
enhanced series
elementary circuit, 481, 484, 486
higher-order lift circuit, 486
re-lift circuit, 484, 486
triple-lift circuit, 485–486
experimental result, 498, 500
family tree, 497–498
main series
elementary circuit, 478
higher-order lift circuit, 480
re-lift circuit, 478–479
triple-lift circuit, 479–480
multiple-enhanced series
elementary circuit, 491, 494
higher-order lift circuit, 494
re-lift circuit, 492, 494
triple-lift circuit, 493–494
output voltage, 497
re-enhanced series
elementary circuit, 487–488
higher-order lift circuit, 490
re-lift circuit, 488, 490
triple-lift circuit, 489–490
simulation results, 497, 499
theoretical analysis, 495–496
Positive-output (P/O) super-lift Luo-converters
additional series, 193
elementary circuit, 200–203
higher-order lift circuit, 206–207
re-lift circuit, 202–204
triple-lift circuit, 203, 205–206
enhanced series, 193

www.EngineeringEBooksPdf.com

elementary circuit, 201, 208–209
higher-order lift circuit, 211–212
re-lift circuit, 207, 209–210
triple-lift circuit, 208, 210–211
experimental results, 230, 232–233
family tree, 227
main series, 193
elementary circuit, 194–197
higher-order lift circuit, 199
re-lift circuit, 195, 197–198
triple-lift circuit, 196, 198–199
multiple-enhanced series, 193
elementary circuit, 220, 223
higher-order lift circuit, 226
re-lift circuit, 221, 224
triple-lift circuit, 222, 225–226
output voltage, 227
re-enhanced series, 193
elementary circuit, 212–214, 216
higher-order lift circuit, 219
re-lift circuit, 214, 216–217
triple-lift circuit, 215, 217–218
simulation results, 230–233
split capacitors
additional series, 368–371
double/enhanced circuit, 367
elementary circuit, 362–365
experimental results, 373–375
family tree, 371–372
main series, 365–366
multiple/enhanced circuit, 367
α split capacitors, 360
three capacitors, 360
transient process waveforms, 375–376
two capacitors, 360
split inductors
additional series, 368–371
elementary circuit, 362–365
experimental results, 373–375
family tree, 371–372
main series, 365–366

www.EngineeringEBooksPdf.com

simulation results, 372–374
α split capacitors, 361
three capacitors, 361
transient process waveforms, 375–376
two capacitors, 361
voltage transfer gain, 228–230
Positive push-pull pump, 15, 17
Positive super Luo-pump, 14–15
Potentiometers, 713–714
Power DC/DC converters
damping time constant, 394
energy factor
average current, 391
CIR, 390
discontinuous capacitor voltage, 391–392
discontinuous inductor current, 391
EF_v, 392
filling coefficients, 391–392
ILR, 390
PE, 389
SE, 390
total variation of stored energy, 392
variation of stored energy in capacitor, 391
variation of stored energy in inductor, 390
VR, 390
mathematical modeling
design examples, 399–404
impulse interference response, 381–382, 385–389
transfer function, 379, 394–399
unit-step function response, 381, 384–389
power efficiency, 393
system stability, 393
time constant, 393
Power transfer efficiency, 627–629
cascade double Γ-CL, 627–629
Π-CLL, 616
PSpice, 230, 273–274, 308–309, 341, 356, 427, 497–498, 521, 558, 600, 616, 629, 644, 656, 665–666
Pulse-width modulation (PWM), 38
Pump circuits

www.EngineeringEBooksPdf.com

developed
Cúk pump, 10, 12
negative Luo-pump, 10–11
positive Luo-pump, 10–11
fundamental
boost, 9
buck, 8
buck–boost, 9, 10
SL pumps
DEC, 16, 18
negative push-pull pump, 15–17
negative super Luo-pump, 15–16, 18
positive push-pull pump, 15, 17
positive super Luo-pump, 14–15
transformer-type
flyback pump, 12–13
forward pump, 12–13
ZETA pump, 14
Push-pull
converter, 23–24
pump, 15–18
PWM, *see* Pulse-width modulation

Q

QF, *see* Quality factor
QRC, *see* Quasi-resonant converter
Quadrant I operation, 3
Quadrant II operation, 3
Quadrant III operation, 3
Quadrant IV operation, 3
Quality factor (QF), 639
Quasi-resonant converter (QRC), 525

R

Resonance
circuit, 528, 531, 533, 536, 541, 543, 546, 549
frequency, 531, 533, 536, 541, 544, 547, 549
state, 526
Resonant
capacitor, 529, 532, 534–535, 537, 616, 636–637, 662, 665, 718

www.EngineeringEBooksPdf.com

circuit, 31, 525, 605–606, 615, 618, 627, 634–637, 642
converter, 525, 635, 637, 644–645, 647, 650–652, 655, 661, 667–668, 718
critical/optimum-resonant state, 525
current, 529–530, 532, 534–535, 537–538
inductor, 554, 636, 662, 718, 724
operation, 714
overresonant state, 525
quasi-resonant state, 525
switch, 525
voltage, 542–545, 547–550, 598–601, 665–666
Reverse braking process, 3
Reverse motoring operation, 2–3, 442, 456, 467–470
Reverse regenerating operation, 3
Reverse running, 2, 29, 407
Reverse starting process, 2
Ripple
current, 431
factor, 379, 388, 687
small, 37, 43, 71, 80, 91, 107, 115–116, 123–124, 131, 133, 144, 153, 157, 159, 164, 166, 171, 174
voltage, 19, 24–25, 38, 100, 103, 137, 140, 185, 197, 203–204, 206, 209–211, 216–218, 223–224, 226, 239–240, 242, 247–248, 251, 256, 258, 263–264, 266, 269, 279, 284, 287–288, 292–293, 298–299, 304–305, 313, 318, 320, 322, 325, 327, 331–332, 336–337, 696
waveform, 115
RMS, *see* Root-mean-square
Root-locus method, 74, 83
Root-mean-square (RMS), 675

S

SC converters, *see* Switched-capacitor converters
Schottky diode, 495, 567–568
s-domain, 638
Second-generation DC/DC converters, 28–29
Second-quadrant chopper, 4–7
Self-lift DC/DC converters
enhanced self-lift P/O Luo-converters, 62–64
normalized load, 38
output voltage, 38
reverse self-lift N/O Luo-converter
CCM, 55–57

www.EngineeringEBooksPdf.com

DCM, 57–58
equivalent circuits, 55
reverse self-lift P/O Luo-converter
CCM, 49–51
DCM, 51–52
equivalent circuits, 49
self-lift Cúk converter
CCM, 40–43
DCM, 43–45
equivalent circuits, 39–40
self-lift N/O Luo-converter
CCM, 52–54
DCM, 54–55
equivalent circuits, 52–53
self-lift P/O Luo-converter
CCM, 45–48
DCM, 48–49
equivalent circuits, 45–46
SEPIC
CCM, 58–61
DCM, 61–62
equivalent circuits, 58–59
voltage transfer gain, 38
SEPIC, *see* Single-ended primary inductance converter
SI converters, *see* Switched-inductor converters
Silicon-controlled rectifier, 697
Single-ended primary inductance converter (SEPIC), 26, 58–62
Single-phase full-wave diode rectifier
back EMF load, 687–689
center-tap circuit, 685–686
Graetz circuit, 685–686
R-C load, 689–691
resistive load, 685–687
Single-phase half-wave diode rectifier
back EMF plus inductive load, 683–685
back EMF plus resistor load, 682–683
capacitive filter, 675–679
forward bias, 673
inductive load, 678, 680
pure inductive load, 681–682
resistive load, 674–675

www.EngineeringEBooksPdf.com

reverse bias, 673–674
Sinusoidal resonant power converter (SRPC), 668–669
Sixth-generation DC/DC converters
four-energy-storage-element, 32
three-energy-storage-element, 32
two-energy-storage-element, 32
SL Luo-converters, *see* Super-lift Luo-converters
SL pumps, *see* Super-lift pumps
Small-signal modelling
block diagram, 651
closed-loop control system
block diagram, 656–657
capacitance value, 660
compensation network, 658–660
ESR, 659
open-loop system, 660–661
resistors, 657
root loci, 661–662
transfer function, 661
unity-gain crossover frequency, 658–660
VCO, 657
EDF, 653
equivalent circuit model, 655–656
harmonic approximation, 652–653
harmonic balance, 654
nonlinear state equation, 651–652
perturbation and linearization, 655, 671
Snubbers, 564, 718
Soft-switching converters, *see* Fourth-generation DC/DC converters
s-plane, 74, 83
Split capacitors, positive-output super-lift Luo-converters
additional series
elementary circuit, 368–370
higher-order lift circuit, 371
re-lift circuit, 369–370
triple-lift circuit, 369–371
double/enhanced circuit, 367
elementary circuit
α split capacitors, 364–365
two split capacitors, 362–363
experimental results, 373–375

www.EngineeringEBooksPdf.com

family tree, 371–372
main series, 365–366
multiple/enhanced circuit, 367
split stages, 360
transient process waveforms, 375–376
Split inductors, positive-output super-lift Luo-converters
additional series
elementary circuit, 368–370
higher-order lift circuit, 371
re-lift circuit, 369–370
triple-lift circuit, 369–371
elementary circuit
β split inductors, 364–365
two split inductors, 362–364
experimental results, 373–375
family tree, 371–372
main series, 365–366
simulation results, 372–374
α split capacitors, 361
three capacitors, 361
transient process waveforms, 375–376
two capacitors, 361
SRPC, *see* Sinusoidal resonant power converter
State-space analysis
average values, 649
coefficient matrix, 650–651
dynamic equation, 649
*i*th mode, 647–648
state transition matrix, 648–650
state vector, 648–649
Super-lift (SL) Luo-converters
mathematical modeling, 402–404
negative-output cascaded boost converters, 311–342
negative-output super-lift Luo-converters, 235–276
positive-output cascaded boost converters, 277–310
positive-output super-lift Luo-converters, 193–233, 359–376
ultra-lift Luo-converter, 345–358
Super-lift (SL) pumps
DEC, 16, 18
negative push-pull pump, 15–17
negative super Luo-pump, 15–16, 18

www.EngineeringEBooksPdf.com

positive push-pull pump, 15, 17
positive super Luo-pump, 14–15
Switch
auxiliary switch, 526, 552, 554, 559–562, 564
changeover, 408, 526, 539
switch-off, 31, 39, 45–47, 49, 52, 55–58, 62, 64–65, 70, 77–78, 80, 86–88, 91, 108–109, 146, 149, 153, 194, 197, 237, 241, 244, 278, 280, 285, 289, 295, 302, 312, 314–315, 317, 319, 324, 346, 361–362, 364, 367, 407, 437, 439, 448, 450, 452, 454, 477–478, 503, 528, 531
switch-on, 39–40, 45–46, 48–49, 52, 55, 58, 62, 65, 67, 77–78, 86–88, 91, 108, 112, 146, 149, 153, 194, 197–198, 200, 204–205, 209, 236, 239, 241, 244, 249, 257, 278, 283, 285, 287, 292, 294–295, 298, 300, 312, 314–315, 317, 319, 321, 326, 346, 361–362, 364, 367, 407, 437, 439, 448, 450, 452, 454, 477, 503, 541, 543, 546, 549
Switched-capacitor (SC) converters, 29
Switched-capacitor (SC) multiple-quadrant converters
four-quadrant converter
circuit description, 442
mode A, 443–444, 447–451
mode B, 444–445, 452–456
mode C, 445–446, 456
mode D, 446–447, 456
two-quadrant converter
circuit description, 434–436
conduction duty, 441
efficiency, 441
experimental results, 441
mode A, 436–438
mode B, 439–441
switching frequency, 442
Switched-inductor (SI) converters, 30
Switched-inductor (SI) four-quadrant DC/DC Luo-converter
experimental results, 474
mode A (forward motoring)
circuit description, 457–458
continuous mode, 459–461
discontinuous mode, 461–463
switch status, 457
mode B (forward regenerative braking)
circuit description, 457–458
continuous mode, 463–464
discontinuous mode, 464–466

www.EngineeringEBooksPdf.com

switch status, 457
mode C (reverse motoring)
circuit description, 458
continuous mode, 467–468
discontinuous mode, 468–470
switch status, 457
mode D (reverse regenerative braking)
circuit description, 458–459
continuous mode, 470–472
discontinuous mode, 472–474
switch status, 457
Switching frequency, 69–70, 639–640
Synchronous rectifier (SR) DC/DC converters; *see also* Fifth-generation DC/DC converters
active-clamped SR Luo-converter, 572–574
double-current SR Luo-converter, 574–576
flat transformer SR Luo-converter, 570–572
with low-resistance MOSFET, 568–569
ZCS SR Luo-converter, 576–579
ZVS SR Luo-converter, 579–581

T

Tapped inductor converter, 26–28
Third-generation DC/DC converters
multiple-lift push-pull switched-capacitor converters, 30
multiple-quadrant switched-capacitor Luo-converters, 29–30
switched-capacitor converters, 29
switched-inductor converters, 30
Third-quadrant chopper, 4–7
Three-element resonant power converter (RPC), 584–586
Three-phase full-bridge diode rectifier, 695–696
Three-phase half-bridge diode rectifier
back EMF load, 693–695
resistive load, 692–693
Thyristor
single-phase full-wave semicontrolled rectifier, 704–706
single-phase half-wave rectifier, 697–703
three-phase full-wave rectifier, 708–711
three-phase half-wave rectifier, 706–708
Total harmonic distortion (THD), 388, 539, 552, 584–585, 602, 617, 629–630, 665–667, 696
Transfer functions, 638–639

www.EngineeringEBooksPdf.com

Transformer-type converters, 22–24
Transformer-type pumps
flyback pump, 12–13
forward pump, 12–13
ZETA pump, 14
Turns ratio, 12, 22, 571, 575
Two-element resonant power converter (RPC)
circuit diagram, 594–595
current transfer gain, 596
experimental results, 601–602
input impedance, 595–596
operation analysis, 597–600
simulation results, 600–602
topologies of, 583–584
Two-quadrant SC DC/DC converter
circuit description, 434–436
conduction duty, 441
efficiency, 441
experimental results, 441
mode A, 436–438
mode B, 439–441
switching frequency, 442

U

Ultra-lift (UL) Luo-converter
CCM
circuit diagram, 346–347
instantaneous values, 352–353
operation, 347–350
DCM
circuit diagram, 346–347
instantaneous values, 354–355
operation, 350–352
experimental results, 357
simulation results, 356–357
voltage transfer gains, 355
Uninterruptible power supply (UPS), 32
Unipolar current source, 592
Unipolar voltage source, 592
Unit-step function, 206, 212, 219, 226, 252, 381, 384, 386–388, 395–399, 401, 403

www.EngineeringEBooksPdf.com

Unity-gain crossover frequency, 658–660
UPS, *see* Uninterruptible power supply

V

Variation
current, 41, 47, 51, 54, 57, 61, 99, 103, 105, 136, 140, 142, 177, 179, 182, 184, 188, 369–370
peak-to-peak, 41–42, 68, 70–71, 78, 80, 85, 88, 90–91, 113, 115, 121, 129–130, 415, 418–419, 422–423, 425–426, 459, 462–463, 465, 467, 469, 471, 473
voltage, 47–48, 51, 54, 57, 60–61, 100, 103, 105, 137, 140, 142, 177, 179, 183, 185, 188, 350
voltage ratio
variation ratio of the current, 42–43, 48, 51, 54, 57, 61, 70, 113, 121, 129, 164, 173
variation ratio of the voltage, 42, 66, 80, 109–110, 113, 121, 129, 131, 408
Voltage-controlled oscillator (VCO), 656–657
Voltage-lift (VL) converters, 28
double-output Luo-converters
boundaries, 189–190
current variation ratio, 154
elementary circuit, 153, 155–161, 191
filling efficiency, 190
freewheeling diode current variation, 189
negative path, 154, 188
output voltages, 189–190
positive path, 153–154, 187–188
quadruple-lift circuit, 181–187, 191
re-lift circuit, 168–175, 191
self-lift circuit, 161–168, 191
triple-lift circuit, 176–181, 191
voltage transfer gain, 154, 189
voltage variation ratio, 154–155
modified P/O Luo-converters
application, 152–153
elementary circuit, 145–146
quadruple-lift circuit, 151–153
re-lift circuit, 147–150
self-lift circuit, 146–147
triple-lift circuit, 150–151
N/O Luo-converters
boundaries, 142–144

www.EngineeringEBooksPdf.com

common formulae, 142
current variation ratio, 109, 142
elementary circuit, 108, 110–117, 144
filling efficiency, 143
freewheeling diode current, 142
output voltage, 143
quadruple-lift circuit, 138–141, 144
re-lift circuit, 125–134, 144
self-lift circuit, 117–125, 144
triple-lift circuit, 135–138, 144
voltage transfer gain, 109, 142
voltage variation ratio, 109–110, 142
P/O Luo-converters
boundaries, 105–107
common formulae, 104
conduction duty cycle, 108
current variations, 105
elementary circuit, 65–75
filling efficiency, 105
freewheeling diode current, 105
output voltages, 106, 108
quadruple-lift circuit, 101–104
re-lift circuit, 85–97
self-lift circuit, 75–85
switching frequency, 108
triple-lift circuit, 98–101
variation ratio of current, 65
variation ratio of voltage, 66
voltage transfer gain, 105
voltage variations, 105
self-lift converters
enhanced self-lift P/O Luo-converters, 62–64
normalized load, 38
output voltage, 38
reverse self-lift N/O Luo-converter, 55–58
reverse self-lift P/O Luo-converter, 49–52
self-lift Cúk converter, 39–45
self-lift N/O Luo-converter, 52–55
self-lift P/O Luo-converter, 45–49
SEPIC, 58–62
voltage transfer gain, 38

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W

Waveform(s)
- current, 8, 12, 14–16, 68–69, 78–79, 88–89, 113, 114, 121–122, 128, 130, 230, 273–274, 308, 341, 350, 435–436, 497–498, 521, 523, 529, 532, 535, 537, 600, 617, 629–632, 678, 682–683, 685, 689–690, 694, 700, 702–703, 705–709, 711, 719–721
- pulse-train, 616, 627, 629, 714
- sinusoidal, 615, 627–628, 644, 675, 678, 682–683, 685, 687, 689, 693–697, 700, 702–703, 707, 709
- square, 616, 627, 629, 644, 714
- voltage, 4–6, 10, 435, 443–447, 528, 531, 533, 536, 541–543, 545–547, 549–550, 631, 646–647, 692, 695–696, 715–716

Working point, 584–585

X

x-element RPCs, *see* Multiple energy-storage element resonant power converters

Z

Zero, 40, 43, 45, 48–49, 51–52, 54–55, 57–58, 61, 65, 72–74, 82–84, 93–97, 101, 104, 107, 109, 116, 124, 133–134, 138, 141, 146, 148, 154, 159–160, 174, 179–180, 186–187

Zero-current-switching quasi-resonant converters (ZCS-QRCs), 31
- experimental results, 538–539
- mode A, 526–531
- mode B, 526–527, 531–533
- mode C, 526–527, 533–536
- mode D, 526–527, 536–538
- switch status, 526, 528

Zero-current-switching (ZCS) SR Luo-converter
- demagnetizing process, 578
- equivalent circuit, 576–577
- magnetizing process, 577–578
- resonant period, 578
- switching-off period, 578

Zero-transition (ZT) converters, 31

Zero-transition (ZT) quasi-resonant Luo-converters
- design considerations, 560–562, 564
- experimental results, 559, 563
- mode A, 552–555
- mode B, 552–553, 555–556
- mode C, 552–553, 557–558
- mode D, 552–553, 558–559

www.EngineeringEBooksPdf.com

simulation results, 558–563
switch/diode status, 553
Zero-voltage-switching quasi-resonant converters (ZVS-QRCs), 31
experimental results, 551–552
mode A, 539–543
mode B, 539–540, 543–546
mode C, 539–540, 546–548
mode D, 539–540, 549–551
switch status, 539, 541
Zero-voltage-switching (ZVS) SR Luo-converter
demagnetizing process, 580
equivalent circuit, 579
magnetizing process, 579–580
resonant period, 580
switching-off period, 580
ZETA converter, 24
ZETA pump, 14

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