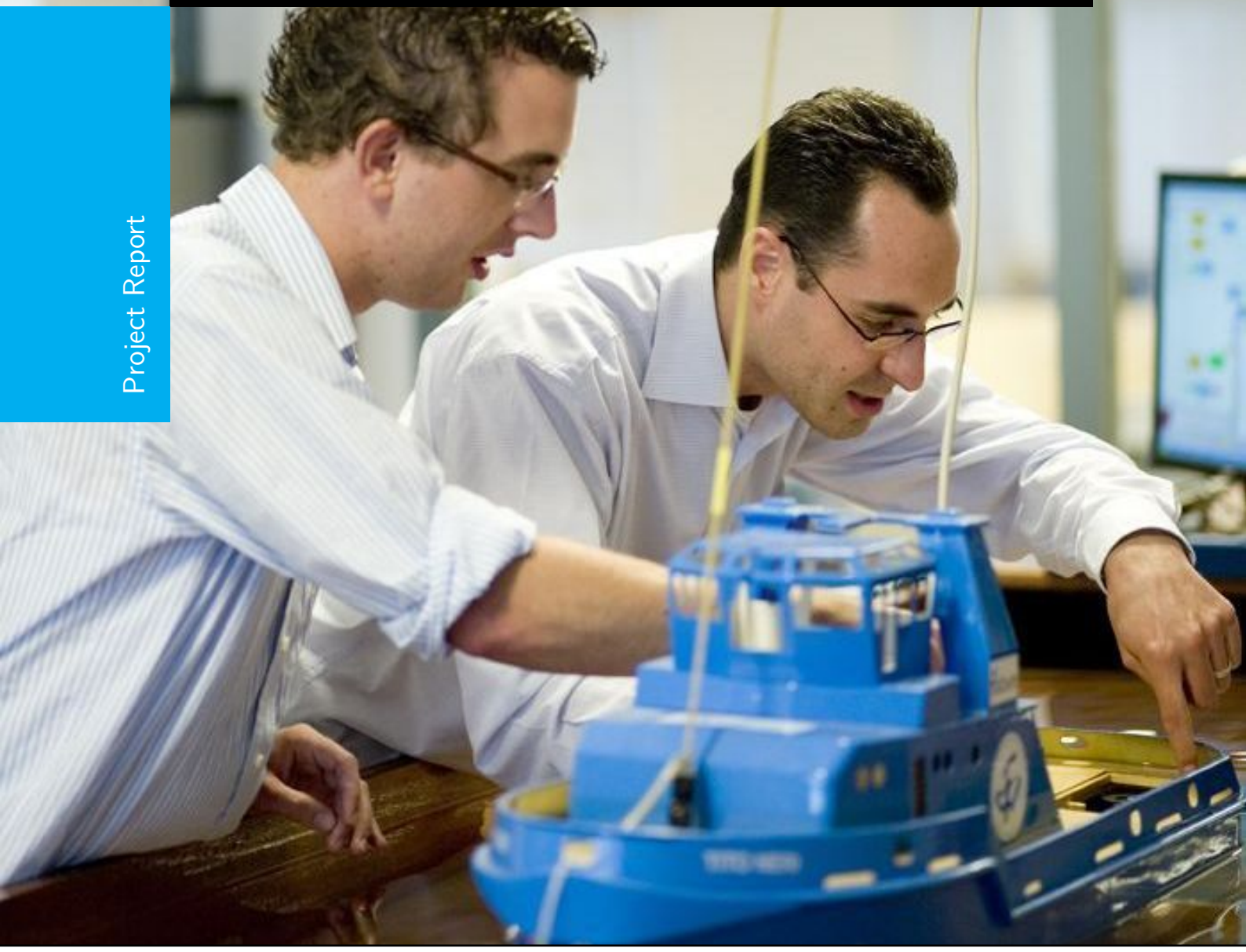
Modeling and analysis of high frequency high voltage multiplier circuit for high voltage power supply

Weijun Qian

Project Report



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Abstract

High frequency high voltage power supply has been widely applied in many industrial applications such as the medical X-ray machine and eletrostatic precipitators. As a part of the high frequency high voltage power supply, the electrical performances of the voltage multiplier circuit will influence the behaviors of applications like the X-ray machine such as the imaging quality. The electrical performances include the output voltage drop and voltage ripple, rise time and decay time of output voltage and power losses. In order to get high imaging quality of the X-ray machine and reduce damage to patients, the multiplier circuit is required to be designed with low output voltage drop and voltage ripple as well as fast respond time.

This thesis concentrates on the investigation of the electrical performances of the Half-wave series Cockcroft-Walton(HWCW) voltage multiplier circuit. The operations in start-up process and steady state are explained in details and methods to evaluate the electrical performances are introduced. Significant parameters of the multiplier circuit that play a role in determining the electrical performances are investigated. Analysis of impact of the parasitic components on the electrical performances are carried out together with simulations. An analytical power loss model is developed in the thesis by deriviations of currents in the HWCW voltage multiplier circuit. At last, optimization of capacitance distributions are discussed and compared to provide methods when selecting the capacitance values in the circuit. The analyses in the thesis are verified by the simulation results in LTspice.

Thesis committee members:
Prof.dr.ir.Pavol Bauer
Dr.ir.Zian Qin
Dr.ir.Jose Rueda Torres

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Chapter 1

Introduction

1-1 Problem Statement

High voltage power supplies have been widely used in many industrial applications such as laser, spectral analysis, medical x-ray imaging, electrostatic precipitators and so on[1][2]. Moreover, high voltage power supply operated under high frequency has the advantage of reducing its volume and cost as well as leading to higher power density design[3]. Therefore, the demands for high frequency high voltage power supplies have been increased.

The traditional use of a high voltage turns ratio step-up transformer in high frequency high voltage power supply is limited by its parasitic components such as leakage inductance and winding capacitance. The low efficiency and large output voltage drop and voltage ripple will lead to bad behaviors of industrial applications like the medical X-ray machine as is introduced in section 1-1-1. In order to produce large output voltage with small ripple, a common high frequency high voltage power supply is composed of an ac input source, DC-Bus, a high frequency inverter, a high voltage transformer and a high voltage multiplier circuit as is shown in Figure 1-1.

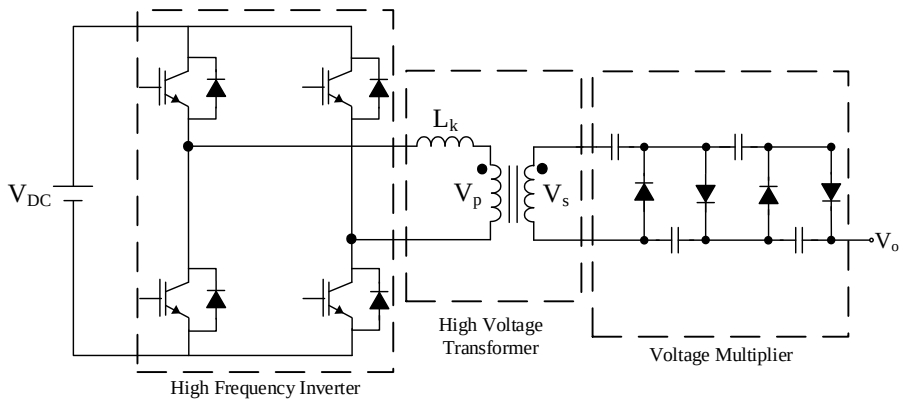

Figure 1-1: High frequency high voltage power supply circuit

The voltage multiplier circuit is applied at the output of the high voltage transformer. The output of the voltage multiplier circuit is the output of the high voltage power supply as well. The multiplier circuit plays an important role in converting the AC input to DC output and stepping up the output voltage value with small voltage ripple. Therefore, the behavior of the voltage multiplier circuit determines the behavior of the high voltage power supply. The voltage multiplier circuit are further introduced in section 1-1-2.

1-1-1 Medical X-ray/CT machine

An impontant industrial utilization for high frequency high voltage power supply is the medical X-ray machine[1]. For a high-quality modern medical X-ray machine, the clarity of X-ray imaging is required to be high and the damage to patients must be kept as small as possible. The behaviors of medical X-ray machines are dependent on the electrical performances of the high voltage power supply including the voltage regulation(voltage drop and voltage ripple) and respond time(rise time and decay time) of output voltage[4]. Bad voltage regulation and slow respond time will result in poor X-ray imaging quality as is shown in Figure 1-2 and more damage to patients[5].

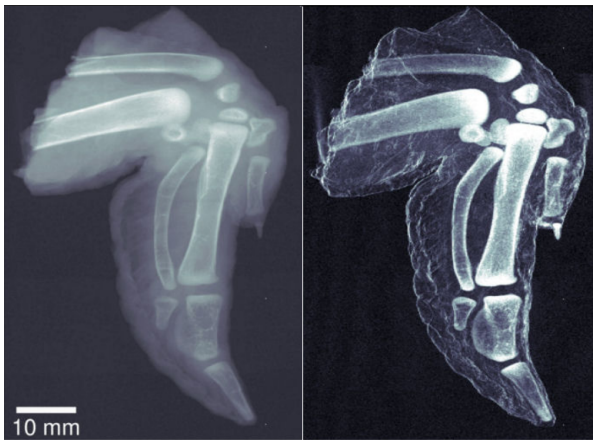

Figure 1-2: Comparison of X-ray imaging quality

First, the input voltage value of the X-ray machine is important in order to reduce the damage to patients as well as to improve the imaging quality[6]. When the voltage value is raised, the penetration of X-rays is enhanced and clear image can be obtained with few X-rays. When the voltage value is decreased, the penetration of X-rays is decreased and more X-rays are required to obtain clear image. The number of X-rays absorbed by patients will also increase and result in more damage to patients.

Second, the voltage ripple of output voltage is related with the clarity of X-ray imaging because the difference among energy spectrum distribution of X-ray will be large if the output voltage ripple is large[6]. If the voltage fluctuates seriously in steady state, the penetration abilities of phontons will also fluctuate and result in bad quality of X-ray imaging. Therefore, the voltage value is required to be DC with large value and small ripple.

Moreover, the power supply is used as a pulse power supply and the respond time in one high voltage pulsation cycle is required to be kept within tens of microseconds. When the voltage

value is far smaller than its steady state value during the rising process and decay process, soft X-rays which are not effective for imaging are produced[7] and the noise will be produced as well.

At last,the power loss in the power supply circuit is another important criteria in order to reduce heating and prolong the service life of the circuit.

1-1-2 Voltage multiplier circuit

The voltage multiplier circuit is an AC-to-DC voltage conversion circuit consisting of n stages. The voltage multiplier circuit is able to produce any output voltage in principle by increasing the number of stages[8] The effective use of voltage multiplier circuits can realize the high voltage conversion up to 100's kV range and are cost efficient[9]. There are several different topologies for voltage multiplier circuits and the most commonly used one is the series half-wave Cockcroft-Walton (HWCW) voltage multiplier circuit shown in Figure 1-3 which is applied in this project[10]. Each stage of the HWCW voltage multiplier circuit comprises 2 legs and each leg is the series connection of one diode and one capacitor.

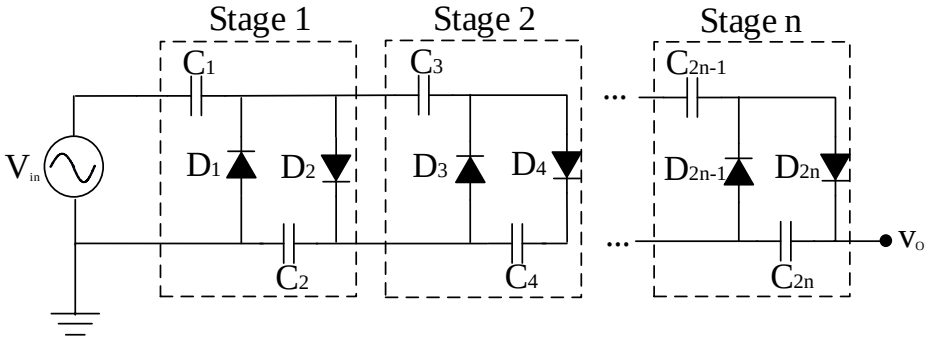

Figure 1-3: Series half-wave Cockcroft-Walton voltage multiplier circuit

When the voltage multiplier circuit is loaded, there are several important electrical performance of the voltage multiplier circuit: the voltage drop&voltage ripple, the rise time&decay time and power losses. The electrical performance will influence the behavior of industrial applications as is introduced in section 1-1-1. Most of the completed research on the voltage multiplier circuits are focusing on the choice of capacitance distribution value[11][12] and the improvement of circuit topology for better output voltage regulation[13][4]. Research on the detailed analysis of electrical performance of the voltage multiplier circuit and power loss calculation are not in-depth. Therefore, this project is focusing on the analysis and modeling of electrical performance of the HWCW voltage multiplier circuit in order to obtain better performance.

1-2 Thesis objectives

This master thesis project is carried out to improve the behavior of the medical X-ray machine by optimizing the high frequency high voltage power supply with the voltage multiplier circuit.

The main objective of this master thesis project is to investigate the electrical performance(voltage drop&voltage ripple and rise time&decay time) and to prolong the serive life of the voltage multiplier circuit.

In order to achieve the objective, there are several research questions that have to be answered:

- What are the factors that will influence the voltage drop&voltage ripple and the rise time&decay time of the HWCW voltage multiplier circuit?
- Where are the power losses in the voltage multiplier circuit coming from and how to estimate them?
- What are the criterion when selecting the operating frequency and capacitance value of the multiplier circuit?

1-3 Thesis approach and layout

The project is carried on based on the case study of a 2-stage series HWCW voltage multiplier circuit. All the theoretical analysis are verified with simulations in LTspice. In order to explain the research questions above, the thesis is organized as follows:

- In chapter 2, operations in start-up process and steady state are explained in details. The causes of voltage drop and voltage ripple are explained by derivation of formulas. The introduction and analysis of rise time and decay time are illustrated as well. At last, different topologies are compared to explain why the HWCW multiplier circuit is chosen in this project.
- In chapter 3, the impact of different parameters on the electrical performance of the multiplier circuit are studied respectively. Simulations are made to verify the analysis. Optimal stage number are also given by calculations.
- In chapter 4, the impact of parasitics of the electrical components on the electrical performance of the multiplier circuit are studied. The parasitic components include the junction capacitance of diodes, ESR,ESL and parallel capacitance of capacitors, leakage inductance and winding capacitance of the transformer. Simulations are made in LTspice to verify the analysis.
- In chapter 5, the reverse recovery analysis for rectifier are analyzed and the equations for the diode current are derived. Power loss model is built up to evaluate the loss distribution of the converter.
- In chapter 6, capacitance distribution is optimized. 5 optimization methods and their influence to the electrical performance of the multiplier circuit are discussed respectively.
- In chapter 7, important conclusions of the analysis from chapter 2 to 6 are summarized. At last, recommendations for setting the parameters of the HWCW voltage multiplier circuit are given.

Chapter 2

Operation Analysis of Voltage Multiplier Circuit

The commonly used series HWCW voltage multiplier circuit is composed of n stages. In each stage, there are two pairs of diodes and capacitors. In the start-up process, the voltage across the capacitors are boosted step by step until steady state is reached. In steady state, voltage drop and voltage ripple will occur when the circuit is loaded. There are some important electrical performances when evaluating the voltage multiplier circuit such as voltage drop&voltage ripple and rise time&decay time. The electrical performances determine the behavior of the high voltage power supply.

In section 2.1, how the HWCW voltage multiplier circuit works in start-up process and boosts the voltage value are explained. In section 2.2, operations of the HWCW voltage multiplier in steady state are analyzed. Section 2.3 introduces the output voltage drop and voltage ripple. Different rectifier circuits are compared in section 2.4. In section 2.5, the rise time and decay time of the multiplier circuit are introduced and analyzed. At last, comparison between different voltage multiplier topologies are made in section 2.6 to explain why the HWCW voltage multiplier circuit is chosen.

2-1 Start-up process analysis

The operations in the 2-stage voltage multiplier circuit (voltage quadrupler) shown in Figure 2-1 are analyzed as a case study in this thesis.

The voltage quadrupler circuit is made up of two stages and each stage includes two legs which is composed of the series connection of one capacitor and one rectifier. The output load is the resistive load R_{Load} representing the X-ray machine. In the voltage multiplier circuit shown in Figure 2-1, C_2 and C_4 are the output capacitors that charge R_{Load}. The output voltage of the voltage multiplier circuit is the voltage across R_{Load} which equals to the summation of voltage across all the output capacitors.

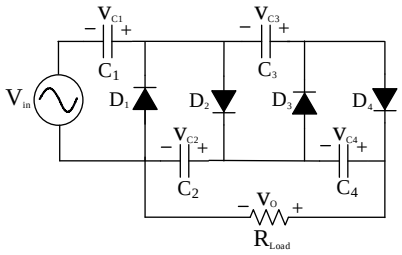

Figure 2-1: 2-stage series HWCW voltage multiplier

2-1-1 Operations in start-up process

In the start-up process, the voltage across capacitors are boosted from 0 to the steady state value step by step. Charges can be regarded as transferring from the voltage source to C_1 and from capacitors in low stages to capacitors in high stages. For a typical series HWCW voltage multiplier circuit with stage number n, in the k^{th} switching cycle of the voltage source, D_{2k} and D_{2k+1} starts to conduct in the circuit (k<n). From the n^{th} switching cycle, all the diodes will conduct once in one switching cycle. The sequence of the conducting diodes is: D_{2n-1},D_{2n-3},$\cdots$,D_3,D_1,D_{2n},$D_{2(n-1)}$,$\cdots$,D_4,D_2. The operations of voltage quadrupler circuit in start-up process are explained in this section . The waveform of voltage across capacitors in the start-up process is shown in Figure 2-2:

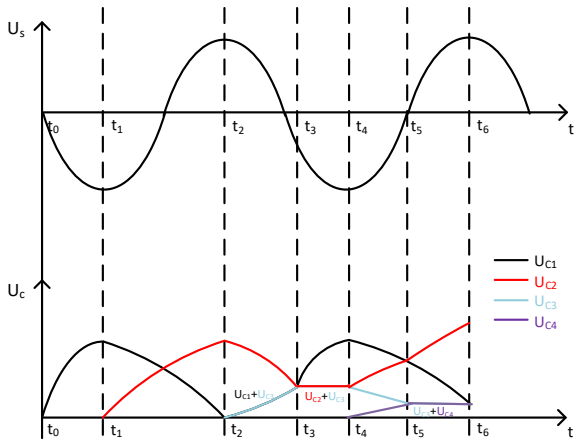

Figure 2-2: Capacitor voltage waveform in start-up process

The operations in the start-up process can be splitted into 6 steps. The behavior in each step is clarified below.

- t_0-t_1
  From t_0 to t_1, the voltage source is in the negative switching cycle and its value is decreasing from 0 to -V_m where V_m represents the maximum voltage of the voltage source. During this time period, V_{in}>V_{C1} and D_1 starts to conduct. The equivalent circuit is shown in Figure 2-3(a). C_1 is charged to V_m by the voltage source. Charges move from the voltage source to C_1.
  At t_1, V_{C1}=V_m , D_1 is blocked and the charging of C_1 stops.

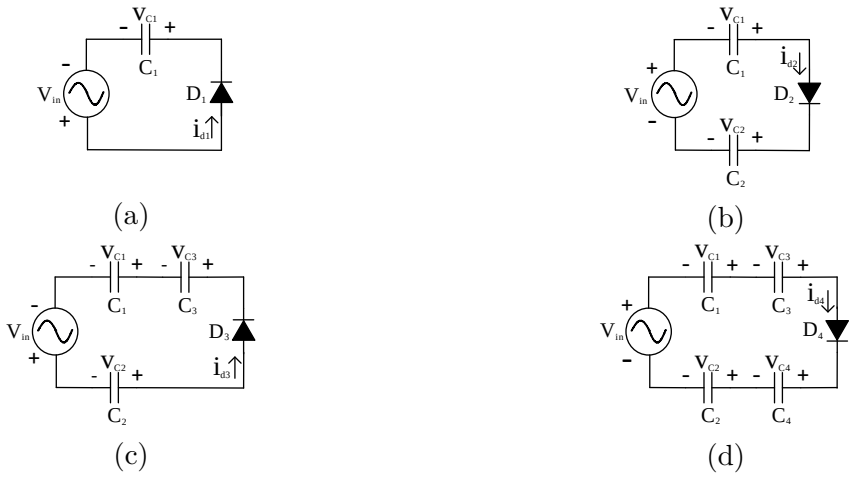

Figure 2-3: Equivalent circuits in start-up process

- t_1-t_2
  At t_1, V_{C1}=V_m and V_{C2}=0.
  From t_1 to t_2, the voltage source is increasing from -V_m to V_m and V_{C1}+V_{in}>V_{C2}. D_2 starts to conduct and the equivalent is shown in Figure 2-3(b). During this time period, C_1 is discharged while C_2 is charged by C_1. Charges can be regarded as moving from C_1 to C_2.
  At t_2, V_{C1}=0, V_{C2}=V_m and D_2 is blocked.

- t_2-t_3
  At t_2, V_{C1}=V_{C3}=0, V_{C2}=V_m.
  From t_2 to t_3, the value of voltage source is decreasing from Vm and the relationship V_{C2}>V_{C1}+V_{C3}+V_{in} is valid. Therefore D_3 starts to conduct and all other diodes are blocked.The equivalent circuit is shown in Figure 2-3(c). C_1 and C_3 are charged at the same rate, C_2 is discharged.
  At t_3, V_{C1}=V_{C2}=V_{C3}=$\frac{V_m}{2}$, both the charging of C_3 and the discharging of C_2 stop, D_3 is blocked.

- t_3-t_4
  From t_3 to t_4, the value of voltage source keeps decreasing in the negative switching cycle. Since D_3 is blocked at t_3 and V_{C2}=V_{C3}, the relationship V_{in}>V_{C1} is valid during this time period. Therefore, D_1 starts to conduct immediately after D_3 and the equivalent circuit is shown in Figure 2-3(a).Operations in this step are the same as that from t_0 to t_1. C_1 continues to be charged by the voltage source to V_m again until t_4. Charges move from the voltage source to C_1.
  At t_4, V_{C1}=V_m, D_1 is blocked again.

- t_4-t_5
  From t_4 to t_5,the voltage source value is increasing from -V_m to 0. Since V_{C1}=V_m and V_{C2}=V_{C3}=$\frac{V_m}{2}$ at t_4, the relationship that V_{C1}+V_{C3}+V_{in} > V_{C2}+V_{C4} is valid.Therefore, D_4 starts to conduct and the equivalent circuit is shown in Figure 2-3(d). During this time period, C_1 and C_3 are discharged while C_2 and C_4 are charged until t_5.

At t_5,V_{C3}=V_{C4} and D_4 is blocked, both the discharging of C_3 and the charging of C_4 stop.

- t_5-t_6
  From t_5 to t_6, the value of voltage source keeps increasing from 0 to V_m and the relationship V_{C1}+V_{in}>V_{C2} is valid. Therefore, D_2 starts to conduct immediately after D_4. The equivalent circuit is shown in Figure 2-3(b) and the operations are the same as that from t_1 to t_2, C_1 continues to be discharged and C_2 continues to be charged until the voltage source reaches its maximum value at t_6.
  At t_6, V_{C1}=V_{C3}=V_{C4} and D_2 stops conducting.

In the following steps of the start-up process, the similar operations as explained above are repeated until the steady state is reached. Since the voltage source is always decreasing from 0 to -Vm at the beginning of one switching cycle, diodes with odd numbers conduct prior to diode with even numbers.Moreover,diodes in higher stages always conduct prior to diode in lower stages in one switching cycle which can be concluded by applying Kirchhoff's law. Therefore,the conducting sequence of diodes in one switching cycle can be drawn: D_{2n-1},D_{2n-3},$\cdots$,D_3,D_1,D_{2n},$D_{2(n-1)}$,$\cdots$,D_4,D_2. One diode conducts only once in one switching cycle.

2-1-2 Conditions for the conduction of diodes

From the analysis above, the conditions for the conductions of diodes in the quadrupler circuit can be concluded.

- Condition for conduction of D_3
  Before D_3 starts to conduct, the value of V_{in} can be either decreasing in the positive switching cycle or increasing in the negative switching cycle. When the input voltage reaches the value that fulfills the condition V_{C2}=V_{in}+V_{C1}+V_{C3}, D_3 starts to conduct.The equivalent circuit is shown in Figure 2-3(c).
  C_1,C_3 are charged and C_2 is discharged during the conduction of D_3. D_3 is blocked when V_{C2}=V_3. Following relationships are valid during the conduction of D_3, where $V(D_{3-})$ represents voltage at the time point before D_3 is blocked and $V(D_{3+})$ represents voltage at the time point after D_3 is blocked:

$$\begin{cases} V_{C2}(D_{3-}) = V_{in}(D_{3-}) + V_{C1}(D_{3-}) + V_{C3}(D_{3-}) \\ V_{C2}(D_{3+}) = V_{C3}(D_{3+}) \end{cases} \tag{2-1}$$

- Condition for conduction of D_1
  D_1 starts to conduct immediately when the conduction of D_3 stops. The equivalent circuit is shown in Figure 2-3(a). After D_3 is blocked, V_{C2}=V_{C3} and V_{in} continues to decrease in the negative switching cycle. Therefore, V_{in}>V_{C1} and D_1 starts to conduct in the circuit. C_1 continues to be charged to V_m until V_{in} reaches -V_m. Following relationships are valid during the conduction of D_1, where $V(D_{1-})$ represents voltage at the time point before D_1 is blocked and $V(D_{1+})$ represents voltage at the time point after D_1 is blocked:

$$\begin{cases} V_{C1}(D_{1-}) = V_{in}(D_{1-}) \\ V_{C1}(D_{1+}) = V_m \end{cases} \tag{2-2}$$

- Condition for conduction of D_4
  After D_1 is blocked, the voltage source starts to increase from -V_m to V_m. During some time period , $V_{C1}+V_{C3}+V_{in}<V_{C2}+V_{C4}$, $V_{C1}=V_m$, $V_{C2}=V_{C3}$. Therefore, $V_{C4}>V_{in}+V_m$ holds and no diodes are conducting in the circuit. When V_{in} increases to the value that $V_{C1}+V_{C3}+V_{in}=V_{C2}+V_{C4}$, D_4 starts to conduct. The equivalent circuit is shown in Figure 2-3(d). During the conduction of D_4, C_1 and C_3 are discharged while C_2 and C_4 are charged. When the condition that $V_{C3}=V_{C4}$ is fulfilled, D_4 is blocked and D_2 is ready to conduct.

  Following relationships are valid during the conduction of D_4, where $V(D_{4-})$ represents voltage at the time point before D_4 is blocked and $V(D_{4+})$ represents voltage at the time point after D_4 is blocked :

$$\begin{cases} V_{C2}(D_{4-}) + V_{C4}(D_{4-}) = V_{in}(D_{4-}) + V_{C1}(D_{4-}) + V_{C3}(D_{4-}) \\ V_{C3}(D_{4+}) = V_{C4}(D_{4+}) \end{cases} \tag{2-3}$$

- Condition for conduction of D_2
  D_2 starts to conduct immediately after D_4 because V_{in} keeps increasing so that $V_{C1}+V_{in}>V_{C2}$ and $V_{C3}=V_{C4}$.The equivalent circuit is shown in Figure 2-3(b). During the conduction of D_2, C_1 keeps to be discharged and C_2 keeps to be charged in the circuit. D_2 is blocked when V_{in} reaches V_m. V_{C2} reaches its maximum value in the switching cycle. Afterwards, the conduction of diodes with odd numbers start.

  Following relationships are valid during the conduction of D_2, where $V(D_{2-})$ represents voltage at the time point before D_2 is blocked and $V(D_{2+})$ represents voltage at the time point after D_2 is blocked :

$$\begin{cases} V_{C2}(D_{2-}) = V_{in}(D_{2-}) + V_{C1}(D_{2-}) \\ V_{C2}(D_{2+}) = V_{in}(D_{2+}) + V_{C1}(D_{2-}) \end{cases} \tag{2-4}$$

If all the components in the multiplier circuit are ideal and the multiplier circuit is not loaded, in steady state $V_{C1}=V_m$, $V_{C2}=V_{C3}=V_{C4}=2V_m$, $V_{out}= 4V_m$.

2-1-3 Simulations and Discussions

The simulations are made to verify the analysis of operations in the start-up process in LTspice. The electrical components used in the simulation are ideal.The parameters are indicated in Table 2-1. The simulation circuit is shown in Figure 2-4.

Table 2-1: Simulation parameters for voltage quadrupler circuit

V_{in}	5kV
Frequency	500kHz
Capacitance value	10nF
Output power	2kW

The waveform of voltage across capacitors are shown in Figure 2-5.
Compare the waveform of capacitor voltage in Figure 2-2 and Figure 2-5, the simulation

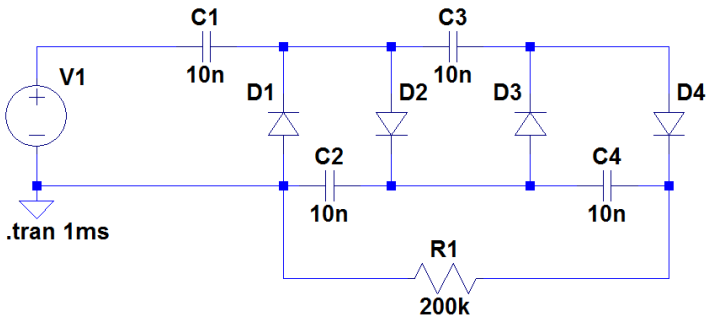

Figure 2-4: Simulation circuit of voltage quadrupler in LTspice

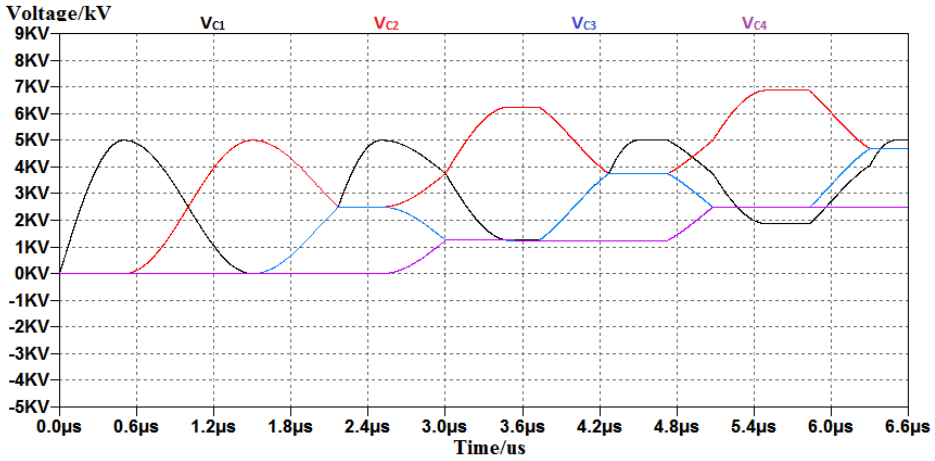

Figure 2-5: Results of simulation in start-up process

results correspond with the theoretical analysis.
Discussions:
1.Each capacitor keeps being charged and discharged during the start-up process except for C_{2n} which only has the process of being charged. Since C_{2n} does not have the discharging process and according to the voltage relationships in section 2-1-2,the initial values of capacitor voltage increase as the switching cycle of input voltage source increases. Therefore, voltage across capacitors are boosted to steady state values step by step. Charges can be regarded as transfering from voltage source to C_1 and from capacitors in low stages to capacitors in high stages in the start-up process. After the start-up process is finished, the steady state is reached.
2.One diode conducts only once in one switching cycle of the voltage source and odd diodes conduct prior to even diodes. Moreover, the diode in the last stage conducts at first and the diode in one stage lower conducts immediately after it. There will be some time periods during which all the diodes are blocked between the conduction of odd and even groups of diodes. The conducting time of diode is related with the voltage difference between two adjacent capacitors.

2-2 Steady state analysis

The steady state is reached when the values of capacitor voltage are not increased. For a n-stage no-load series HWCW voltage multiplier circuit, the steady state values of capacitor voltage are: $V_{C1}=V_m$, $V_{C2}=V_{C3}=\cdots=V_{C2n}=2*V_m$, $V_o=n*V_{in}$. When the multiplier circuit is loaded, charging and discharging of capacitors occur in steady state because of the voltage drop of output capacitors which are resulted from the charging process of R_{Load}. As a result, voltage drop and voltage ripple arise in steady state, which are further explained in section 2-3.

2-2-1 Operations in steady state

For the voltage quadrupler circuit, the waveform of diode current and capacitor voltage are shown in Figure 2-6. Even diodes are conducting in the positive switching cycles of the voltage

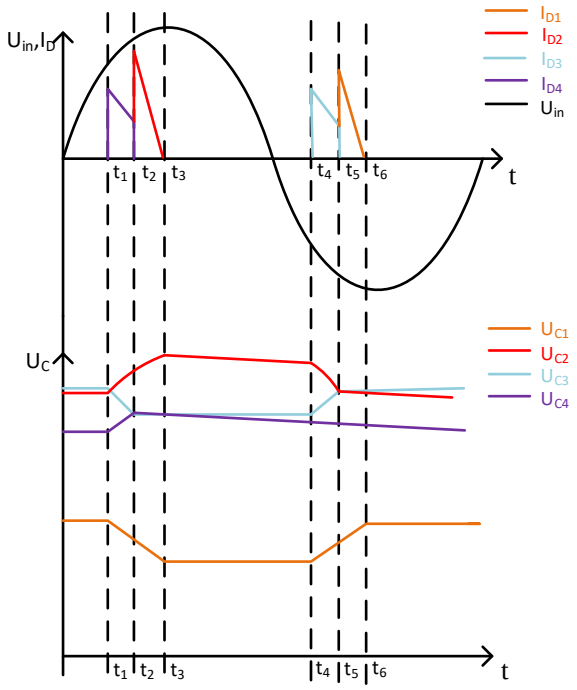

Figure 2-6: Diode current and Capacitor voltage waveform in steady state

source while odd diodes are conducing in the negative switching cycles. As is discussed in section 2-1, diodes in higher stages always conduct prior to diodes in lower stages in one switching cycle. The operations in the positive and negative switching cycle are similar.

- Before t_1
  Before t_1, the voltage source is increasing from 0 in the positive switching cycle. The relationship that $V_{C1}+V_{C3}+V_{in}<V_{C2}+V_{C4}$ is valid during this time period. As a result, all the diodes are blocked. The equivalent circuit is shown in Figure 2-7(e).
  C_2 and C_4 are charging the output load. Therefore, voltage across C_1 and C_3 remain

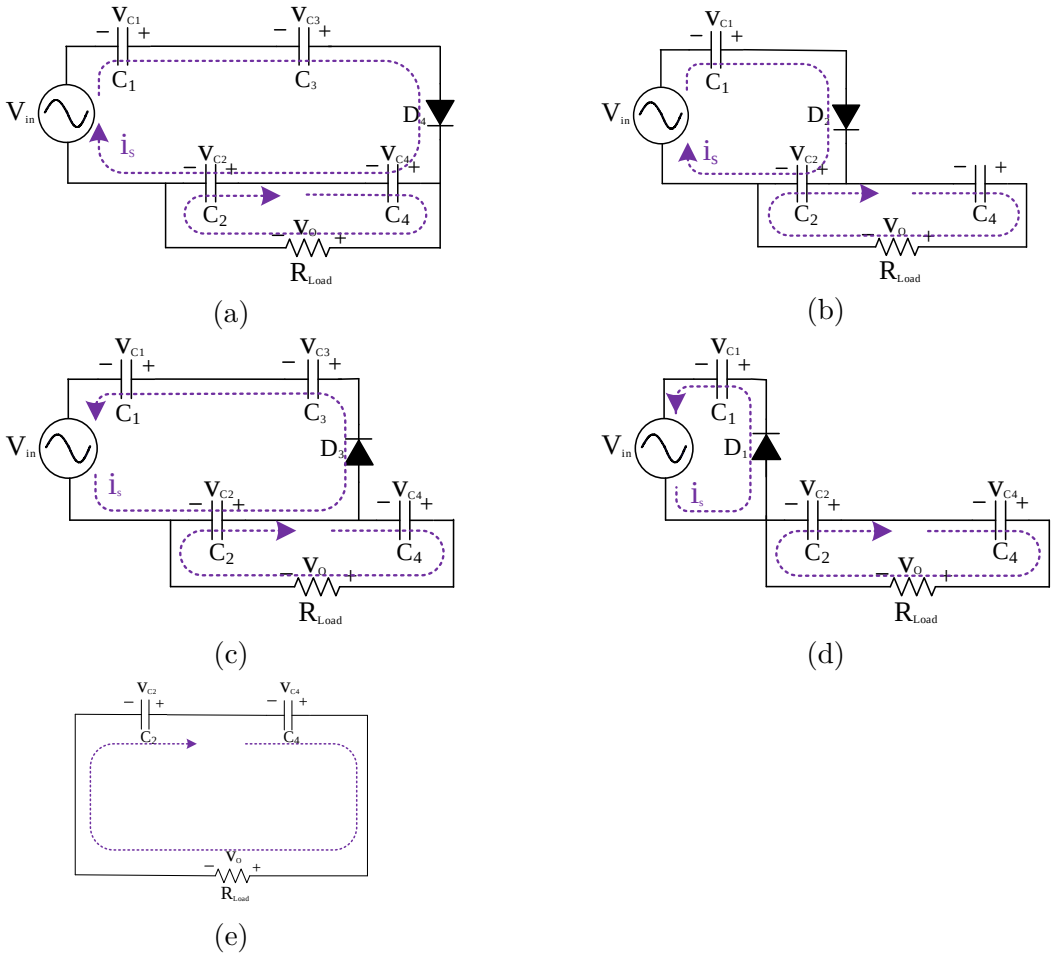

Figure 2-7: Equivalent circuits in steady state

the same while voltage across C_2 and C_4 keep decreasing at the same rate. As a result,voltage across the even capacitor is lower than that of the odd capacitor in the same stage except for the first stage.

- t_1-t_2
  At t_1, the input voltage increases to a certain value that fulfills the condition $V_{C1}+V_{C3}+V_{in} = V_{C2}+V_{C4}$. After t_1, the voltage source value keeps increasing, therefore D_4 starts to conduct first due to $V_{C4}<V_{C3}$ and other diodes are still blocked. Therefore, there are two conduction loops in the circuit during this time period as is shown in Figure 2-7(a). In the diode conducting loop, C_2 and C_4 are charged while C_1 and C3 are discharged. In the output loop, C_2 and C_4 are charging the load. Voltage across C_2 and C_4 are increased because the charging rate is much higher than the discharging rate while voltage across C_1 and C_3 are decreased. At t_2, $V_{C3}=V_{C4}$ and D_4 stops conducting. V_{C4} reaches its maximum value in steady state.

- t_2-t_3
  At t_2, $V_{C3}=V_{C4}$ and $V_{C1}+V_{in}>V_{C2}$ are valid. Therefore, D_2 starts to conduct immediately after D_4. There are also two loops in the circuit during this time interval as is

shown in Figure 2-7(b).
In the diode conducting loop, C_1 is discharged while C_2 is charged. In the output loop, C_2 and C_4 continue to charge the load. As a result, from t_2 to t_3, V_{C1} keeps decreasing and V_{C2} keeps increasing. V_{C3} remains the same value as what it is at t_3, which is also the minimum value of V_{C3} in steady state. V_{C4} also decreases due to the existence of output load. The voltage source reaches its maximum value V_m at t_3 and D_2 stops conducting. At t_3, V_{C1} reaches its minimum value and V_{C2} reaches its maximum value in steady state.

- t_3-t_4
  From t_3 to t_4, the voltage source value keeps decreasing and the relationship $V_{C2}< V_{C1}+V_{C3}+V_{in} < V_{C2}+V_{C4}$ is valid. All the diodes are blocked in the circuit. The equivalent circuit is shown in Figure 2-7(e).The operations in the circuit are the same as the operations before t_1. There is only one output loop in the circuit. C_2 and C_4 are charging the output load. V_{C2} and V_{C4} are decreasing at the same rate.

- t_4-t_5
  At t_4, the voltage source is in the negative switching cycle and its value is decreased to a certain value that fulfills the condition $V_{C1}+V_{C3}+V_{in}=V_{C2}$ which lets D_3 to start conducting in the circuit. There are again two loops in the circuit as is shown in Figure 2-7(c).
  In the diode conducting loop, C_1 and C_3 are charged while C_2 is discharged. In the output loop, C_2 and C_4 are charging the output load. As a result, V_{C1} and V_{C3} are increased , V_{C2} is decreased and V_{C4} keeps decreasing at the output discharging rate. At t_5, $V_{C2}=V_{C3}$ and the conduction of D_3 stops. V_{C3} reaches its maximum value in steady state.

- t_5-t_6
  From t_5 to t_6, the voltage source keeps decreasing to $-V_m$. Therefore, D_1 starts to conduct immediately after D_3. There are two loops in the circuit as shown in Figure 2-7(d).
  In the multiplier loop, C_1 is charged by the voltage source. In the output loop, C_2 and C_4 are charging the output load. As a result, V_{C1} keeps increasing while V_{C2} and V_{C4} keep decreasing. At t_6, the value of voltage source reaches $-V_m$ and the conduction of D_1 stops. V_{C1} reaches its maximum value in steady state at t_6.

2-2-2 Simulations and discussions

Simulations are made to verify the analysis of operations in steady state in LTspice. The simulation parameters and circuit are shown in Table 2-1 and Figure 2-4 respectively.
The simulation results of capacitor voltage are shown in Figure 2-8 and results of diode currents are shown in Figure 2-9.
Discussions:
The simulation results correspond with the theoretical analysis.
1.The steady state is reached when values of capacitor voltage are not increased any more. In steady state of a typical n-stage no-loaded HWCW voltage multiplier circuit, $V_{C1}=V_m$, $V_{Ck}=2V_m(1<k\leqslant n)$, $V_{out}=2n*V_m$.

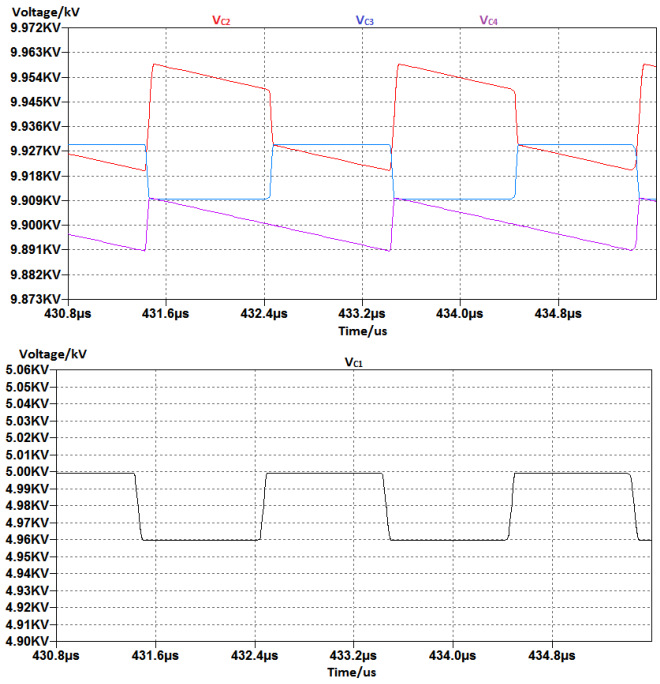

Figure 2-8: Simulation waveform of voltage capacitor in steady state

2.When the absolute value of input voltage source is relatively low that the inequation:

$$\sum_{k=1}^{n-1} V_{C_{2k}} < \sum_{k=1}^{n} V_{C_{2k-1}} + V_{in} < \sum_{k=1}^{n} V_{C_{2k}}$$

is valid, there will be no diode conducting in the multiplier circuit.
When the voltage source is in the positive switching cycle and rises to the value that fulfills the condition:

$$\sum_{k=1}^{n} V_{C_{2k-1}} + V_{in} = \sum_{k=1}^{n} V_{C_{2k}}$$

D_{2n} starts to conduct. After the conduction of D_{2k}, D_{2k-2} starts to conduction immediately until the value of input voltage source reaches V_m and D_2 stops conducting. When the voltage source is in the negative switching cycle and decreases to the value that fulfills the condition:

$$\sum_{k=1}^{n-1} V_{C_{2k}} = \sum_{k=1}^{n} V_{C_{2k-1}} + V_{in}$$

D_{2n-1} starts to conduct. D_1 stops conducting when the voltage source value reaches $-V_m$. Therefore, one diode only conduct once in one switching cycle and there will only be one diode conducting in the circuit during a time.
3.When any diode is conducting in the circuit, there will be two loops-the diode conducting loop and the output loop. The output loop exists in the circuit any time which means that the output capacitors are always charging the output load. When even diodes are conducting in the circuit, even capacitors are charged while odd capacitors are discharged. When odd diodes are conducting in the circuit, odd capacitors are charged while even capacitors are

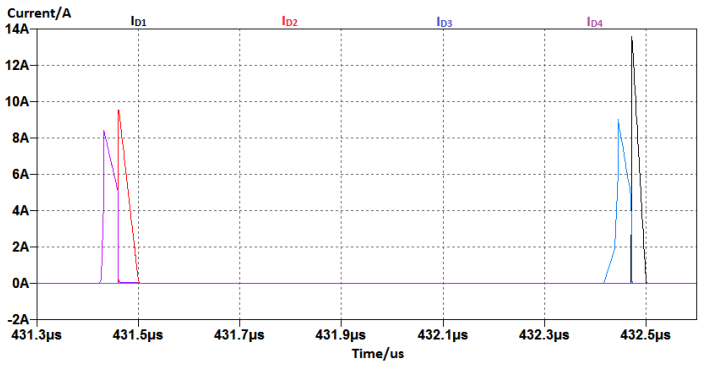

Figure 2-9: Simulation waveform of diode current in steady state

discharged. The exception is that C_{2n} only has the charging process in the multiplier loop.
4.Each capacitor has its maximum and minimum voltage value in steady state. For odd capacitor C_{2k-1}, the maximum value is reached when the D_{2k-1} finishes conducting and the minimum value is reached when D_{2k} finishes conducting. For capacitor C_{2k}, the maximum value is reached when D_{2k} finishes conducting and the minimum value is reached when D_{2n} starts conducting. When no diodes are conducting in the circuit, V_{C2k-1} keeps constant while V_{C2k} keeps decreasing due to the influence of the output load. Moreover, the maximum value of C_{2k} equals to the minimum value of C_{2k-1} when k>1.

2-3 Voltage drop and voltage ripple

As can be inferred from the discussions in section 2-2, due to the existence of output load, voltage drop and voltage ripple across capacitors exist in steady state in voltage multiplier circuit. The voltage drop and voltage ripple are discussed in this section. The voltage drop and voltage ripple of a n-stage HWCW voltage multiplier circuit is[14]:

$$\Delta V_o = \frac{4n^3 + 3n^2 - n}{6} \frac{I_o}{fC} \tag{2-5}$$

$$\delta V_o = \frac{n(n+1)}{2} \frac{I_o}{fC} \tag{2-6}$$

2-3-1 Derivations of voltage drop and voltage ripple

For the derivations of equation 2-1 and 2-2, some assumptions have to be made:
1.All the electrical components in the voltage multiplier circuit are ideal.
2.The charging and discharging time of capacitors are much smaller than the period of input voltage source.
3.The influence of the output load is ignored.
4.The total charge flowing in the first stage is N times the total charge flowing in the k^{th} stage. The assumption is also valid when the capacitance distribution is not equal in each stage. This assumption was assumed by Cockcroft and Walton and is in approximate agreement

with the experimental results[15].
Capacitors are being charged and discharged continuously in steady state due to the existence of the output load, which results in voltage fluctuation. Charge through capacitors in the same stage are equal Q_{C2k-1}=Q_{C2k} because the charging/discharging rate and time are the same.
The charge dissipates in the load resistance and charge through capacitors in the last stage equals to Q_o[15]:

$$Q_{C2n-1} = Q_{C2n} = Q_o = \frac{I_o}{f} \tag{2-7}$$

Therefore, charge through capacitors in the k^{th} stage can be derived based on Assumption 4:

$$Q_{C2k-1} = Q_{C2k} = (n-k+1)\frac{I_o}{f} \tag{2-8}$$

The voltage ripple of capacitors in the k^{th} stage is:

$$\delta V_{C2k-1} = \delta V_{C2k} = (n-k+1)\frac{I_o}{fC} \tag{2-9}$$

The output voltage ripple is the summation of voltage ripple of output capacitors:

$$\delta V_o = \sum_{k=1}^{n} \delta V_{C2k} = \frac{n(n+1)}{2}\frac{I_o}{fC} \tag{2-10}$$

From Figure 2-6, voltage drop of C_i is the summation of voltage ripples of C_1 to C_{i-1}($1<i\leqslant 2n$).

$$\Delta V_i = \sum_{j=1}^{i-1} \delta V_j \tag{2-11}$$

Therefore, the expressions for voltage drop of odd/even capacitors can be derived respecitvely:

$$\Delta V_{2k-1} = \sum_{i=1}^{k-1} \delta V_{2i-1} + \sum_{i=1}^{k-1} \delta V_{2i} = 2\sum_{i=1}^{k-1}(n-k+1) * \frac{I_o}{fC} = (2n-k+2)(k-1)\frac{I_o}{fC} \tag{2-12}$$

$$\Delta V_{2k} = \sum_{i=1}^{k} \delta V_{2i-1} + \sum_{i=1}^{k-1} \delta V_{2i} = [(2k-1)(n+1) - k^2]\frac{I_o}{fC} \tag{2-13}$$

The output voltage drop is the summation of voltage drop across output capacitors:

$$\Delta V_o = \sum_{k=1}^{n} \delta V_{2k} = \sum_{k=1}^{n}(2k-1)(n+1)\frac{I_o}{fC} - \sum_{k=1}^{n} k^2 \frac{I_o}{fC} = \frac{4n^3+3n^2-n}{6}\frac{I_o}{fC} \tag{2-14}$$

What should be noticed is that the calculated voltage drop in (2-16) is the difference between the maximum capacitor voltage value in steady state and the ideal no-load capacitor value.

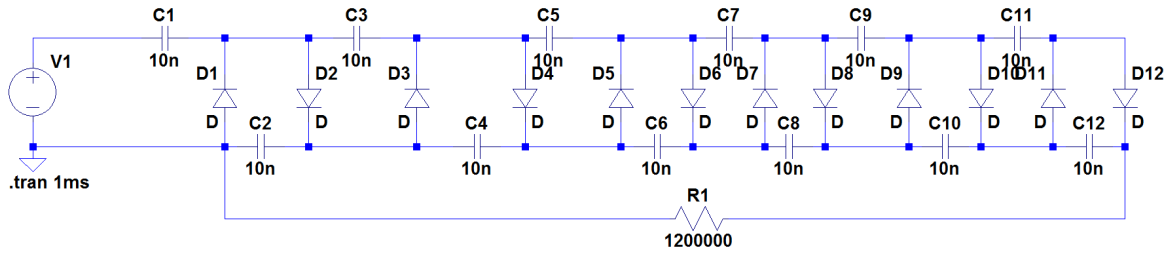

Figure 2-10: Simulation of 6-stage HWCW voltage multiplier circuit

Table 2-2: Parameters of 6-stage HWCW voltage multiplier circuit

V_{in}	5kV
Frequency	500kHz
Capacitance value	10nF
Output power	3kW

2-3-2 Simulations and Discussions

Simulations are made in LTspice to compare calculation and simulation results of voltage drop and voltage ripple.
The simulation is based on a 6-stage HWCW voltage multiplier circuit shown in Figure 2-10. The parameters are shown in Table 2-2.
The comparison between calculation and simulation results of voltage drop and voltage ripple is shown in Table 2-3.

The main reason for the errors between the calculation and simulation results is that the output voltage is assumed to $2nV_m$ when calculating the voltage drop and voltage ripple using equation (2-10) and (2-14). In reality, the output voltage is smaller than $2nV_m$ because of the existence of voltage drop and voltage ripple.Therefore, the actual output current in (2-10) and (2-14) is smaller as well. As a result, the simulated voltage drop and voltage ripple will be smaller than the calculation values.

As can be observed from the simulation results, the errors between the calculation and simulation results become larger as the stage number gets larger. This is due to the fact that the voltage drop of k^{th} capacitor is the summation of voltage ripples of capacitors in lower stages as is indicated in Equation (2-11), the errors are accumulated as the stage number gets larger.

The simulated voltage ripple of the even capacitor is smaller than that of the odd capacitor in the same stage. This is because of the influence of output load. The even capacitors are charging the output load at the same time they are being charged in the multiplier, which will decrease the voltage ripple of even capacitors.

Discussions:

1.Voltage drop and voltage ripple exist in the capacitor voltage when the multiplier circuit is loaded. The voltage ripple values of capacitors in the same stage are the same as is shown in Equation (2-9). The voltage drop of C_i is accumulation of voltage drops from C_1 to $C_{i-1}(1<i\leqslant 2n)$ as is shown in Equation (2-12) and (2-13). For a typical n-stage series

Table 2-3: Comparison of calculation and simulation results of voltage drop and voltage ripple

	$\Delta V_{cal}/V$	$\Delta V_{sim}/V$	Errors	$\delta V_{cal}/V$	$\delta V_{sim}/V$	Errors
V_{C1}	0	0	0	60	59.1	1.5%
V_{C2}	60	59.7	0.5%	60	58.2	3%
V_{C3}	120	112.4	6.7%	50	53.5	6.5%
V_{C4}	170	158.9	6.9%	50	52.7	5.1%
V_{C5}	220	204.7	7.5%	40	38.5	3.9%
V_{C6}	260	243	7%	40	37.8	5.8%
V_{C7}	300	276.3	8.6%	30	30.9	2.9%
V_{C8}	330	303.7	8.7%	30	30.4	1.3%
V_{C9}	360	326.6	10.2%	20	20.5	2.4%
V_{C10}	380	346.2	9.8%	20	19.5	2.5%
V_{C11}	400	354.8	12.7%	10	11.6	13.8%
V_{C12}	410	366.4	11.9%	10	11.4	12.3%
V_{out}	1610	1480	8.8%	210	208.7	0.6%

HWCW voltage multiplier circuit, the output voltage ripple and voltage drop are expressed in Equations (2-10) and (2-14) respectively.

2.The calculation values of voltage ripple and voltage drop are larger than the actual values. The errors become larger when the stage number increases. The voltage drop and voltage ripple are related with stage number, output power, frequency and capacitance value which will be further discussed in Chapter 3.

2-4 Comparative analysis of bridge diode rectifier and voltage doubler

2-4-1 Full-wave bridge diode rectifier

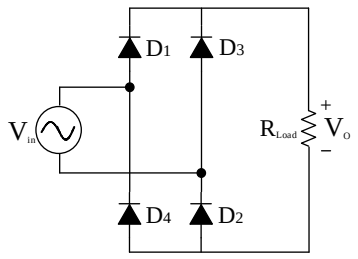

Figure 2-11: Full-wave bridge diode rectifier

The full-wave bridge diode rectifier shown in Figure 2-11 is used in many DC power supplies. It provides full-wave rectification to convert the AC input to DC output by connecting 4 individual diodes in a closed loop. The main advantage of full wave bridge rectifier is that no center-tapped transformer is needed so that the cost and size are reduced.

The current always flows continuously through one of the top diodes D_1,D_3 and one of the bottom diodes D_2,D_4. The waveform of the current and voltage at input and output are shown in Figure 2-12.

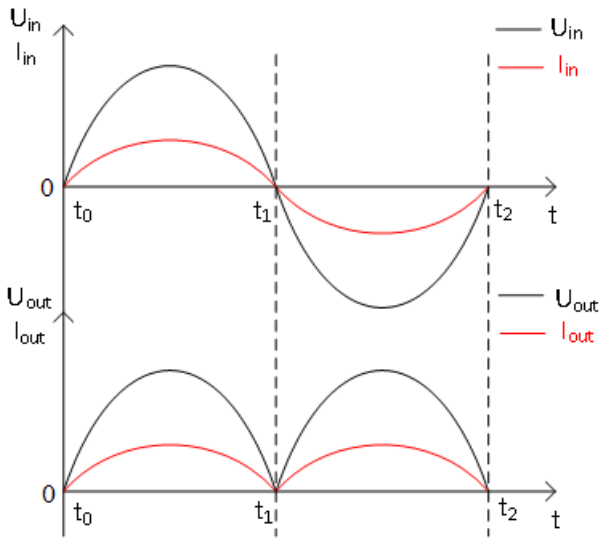

Figure 2-12: Waveform of output voltage of Full-wave bridge diode rectifier

- t_0 to t_1

  The input voltage is in the positive switching cycle, as a result D_1 and D_2 are conducting and V_{out}=V_{in}, I_{out}=I_{in}. The equivalent circuit during this time period is shown in Figure 2-13(a).

- t_1 to t_2

  The input voltage is in the negative switching cycle, as a result D_3 and D_4 are conducting and V_{out}=-V_{in}, I_{out}=-I_{in}. The equivalent circuit during this time period is shown in Figure 2-13(b).

The dc-side output voltage of the full-wave bridge diode rectifier can be expressed as $V_{out}(t)$= $|V_{in}|$. The AC input voltage is rectified to DC output with the same amplitude.

The full-wave bridge diode rectifier is also simulated in LTspice. The simulation waveform are shown in Figure 2-14.

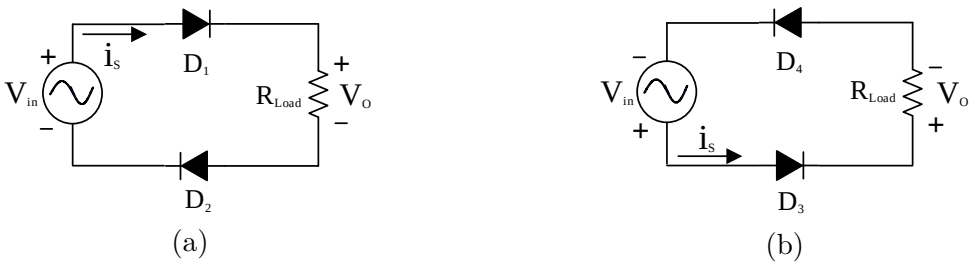

Figure 2-13: Equivalent circuits of full-wave bridge diode rectifier

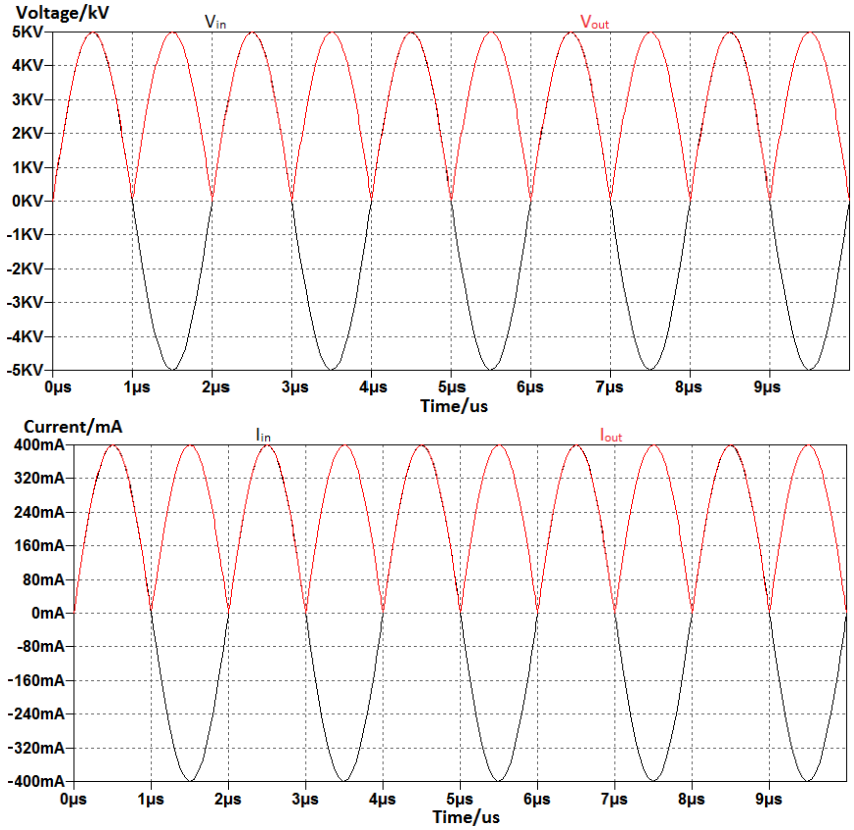

Figure 2-14: Simulation waveform of full-wave diode bridge rectifier

2-4-2 Voltage doubler

Although the full wave bridge diode rectifier is able to convert the AC input voltage to DC output, the voltage amplitude is not changed. The common input voltage value may be insufficient to meet the requirements for many industrial applications. Therefore, a voltage doubler circuit shown in Figure 2-15 may be applied to double the input voltage value at output.

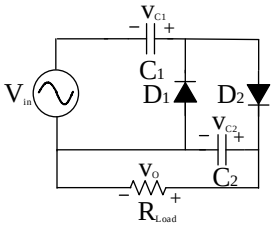

Figure 2-15: Voltage doubler

The voltage doubler is one-stage series HWCW voltage multiplier circuit consisting of voltage source, two pairs of diodes and capacitors and output load. The output voltage V_{out}=V_{C2}=$2V_m$.

The waveforms of capacitor voltage in the start-up process and steady state are shown in Figure 2-16(a) and Figure 2-16(b) respectively.

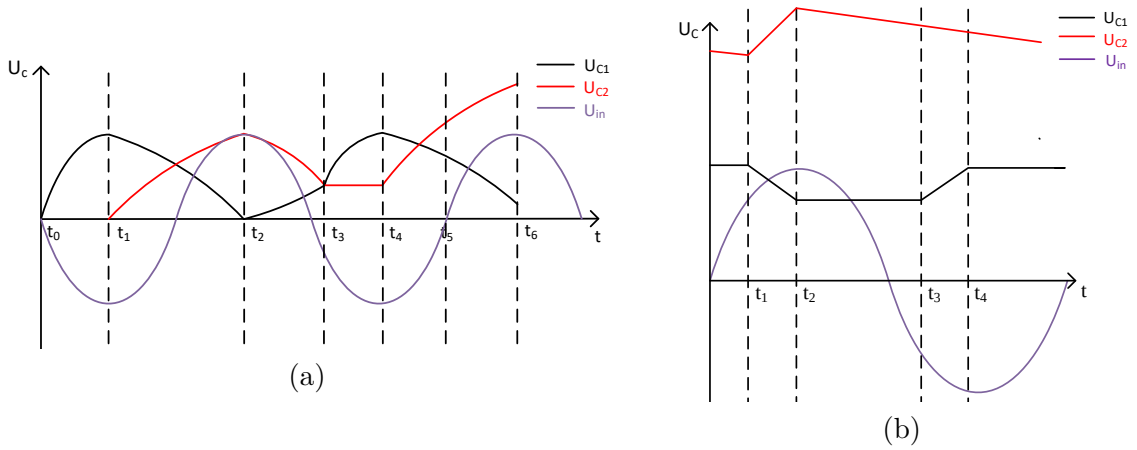

Figure 2-16: Waveform of voltage doubler

The operations in the start-up process are similar with what has been analyzed in section 2-1-1. In steady state, V_{C1}=V_m and V_{C2}=2V_m when the multiplier circuit is not loaded. The voltage drop and voltage ripple will appear if the circuit is loaded with output load.

At t_1 in Figure 2-16(b), the voltage source is in the positive switching cycle and rises to the certain value that fulfills the relationship V_{C1}+V_{in}=V_{C2}. As a result, D_2 is conducting from t_1 to t_2. C_2 is charged and C_1 is discharged until V_{in} increases to V_m at t_2.

At t_3, the voltage source is in the negative switching cycle and decreases to the certain value that fulfills the relationship V_{in}=-V_{C1}. As a result, D_1 is conducting from t_3 to t_4. C_1 is charged by the voltage source. C_1 and C_2 are charged and discharged continuously in steady state.

2-4-3 Discussions

The comparisons of the full-wave bridge diode rectifier circuit, voltage doubler and voltage quadrupler circuit are shown Table 2-4.

Table 2-4: Comparison of AC-DC voltage conversion circuits

	Diode bridge rectifier	Voltage doubler	Voltage quadrupler
AC-DC voltage conversion	Yes	Yes	Yes
Center-tapped transformer	No	No	No
Ratio of $\frac{V_{out}}{V_m}$	1	2	4
Voltage drop	0	$\frac{I_o}{fC}$	$7\frac{I_o}{fC}$
Voltage ripple	V_m	$\frac{I_o}{fC}$	$3\frac{I_o}{fC}$

All the three circuits compared in this section are voltage rectifier circuits and center-tapped transformers are not required. For the full-wave diode bridge rectifier,only the polarities of voltage and current are rectified while the amplitudes are not changed. For different kinds of load at dc side such as inductive load, capacitive load, dc current source and so on, the

current waveform is different. The voltage doubler circuit and voltage quadrupler circuit are not only able to convert the polarities but also to increase the voltage value from input to output.

The voltage quadrupler has the biggest magnification factor of 4 at output voltage as well as large voltage drop and voltage ripple. The voltage doubler has the magnification factor of 2 and moderate voltage drop and voltage ripple. The full-wave bridge diode rectifier has no voltage drop but the voltage ripple is the biggest among three circuits. In order to meet the requirements for output voltage value, voltage drop and voltage ripple of the medical X-ray machine, the voltage doubler circuit is selected in this project.

2-5 Rise time and Decay time

Besides the voltage drop and voltage ripple discussed in section 2-3, the rise time and decay time of output votlage are also important electrical parameters when evaluating the voltage multiplier circuit especially when the multiplier circuit is used as a part of pulse power supply, which requires fast respond time of output voltage for the generation of nearly rectangular pulse shapes.

The key factors influencing the rise time and decay time are the stage number, the operating frequency, capacitance value and output power. The rise time is defined as the time duration when the output voltage rise from 10% to 90% of its steady state value and the decay time is defined as the time duration when the output voltage falls from 100% to 10% of its steady state value. The definition of rise time and decay time is shown in Figure 2-17 where t_r represents rise time and t_f represents decay time.

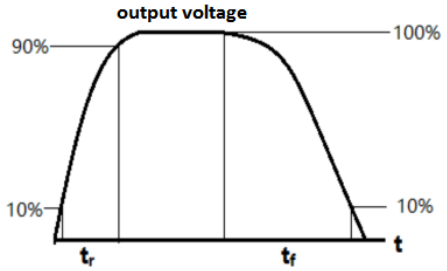

Figure 2-17: Definition of rise time and decay time

2-5-1 Analysis of rise time

The analysis of output rise time is based on operations and voltage relationships in the start-up process in section 2-1. The rise time is the time duration when the output voltage rises from $0.1V_{out}$ to $0.9V_{out}$. The ideal output voltage of voltage multiplier circuit in Table 2-1 can be calculated taking voltage drop and voltage ripple into consideration:

$$V_{out} = V_{noload} - \Delta V_o - \frac{1}{2}\delta V_o = 2nV_m - (\frac{2}{3}n^3 + \frac{3}{4}n^2 + \frac{1}{12}n)\frac{I_o}{fC} \tag{2-15}$$

By using the voltage relationships concluded in section 2-1-2, the voltage value across capacitors in each half switching cycle during the start-up process can be estimated theoretically. The results of rise time of the voltage quadrupler circuit are indicated in Table 2-5 where C represents the number of switching cycle, A represents the amplitude of input voltage V_m, N represents negative switching cyle and P represents positive switching cycle.

Table 2-5: Rise time calculation for voltage quadrupler

C	V_{C1}		V_{C2}		V_{C3}		V_{C4}		V_{out}	
	N	P	N	P	N	P	N	P	N	P
1	A	0	0	A	0	0	0	0	0	0
2	A	$\frac{A}{4}$	$\frac{A}{2}$	$\frac{5A}{4}$	$\frac{A}{2}$	$\frac{A}{4}$	0	$\frac{A}{4}$	$\frac{A}{2}$	$\frac{3A}{2}$
3	A	$\frac{3A}{8}$	$\frac{3A}{4}$	$\frac{11A}{8}$	$\frac{3A}{4}$	$\frac{A}{2}$	$\frac{A}{4}$	$\frac{A}{2}$	A	$\frac{15A}{8}$
4	A	$\frac{15A}{32}$	$\frac{15A}{16}$	$\frac{47A}{32}$	$\frac{15A}{16}$	$\frac{23A}{32}$	$\frac{A}{2}$	$\frac{A}{2}$	$\frac{23A}{16}$	$\frac{35A}{16}$
5	A	$\frac{35A}{64}$	$\frac{35A}{32}$	$\frac{99A}{64}$	$\frac{35A}{32}$	$\frac{29A}{32}$	$\frac{23A}{32}$	$\frac{29A}{32}$	$\frac{29A}{16}$	$\frac{157A}{64}$
6	A	$\frac{157A}{256}$	$\frac{157A}{128}$	$\frac{413A}{256}$	$\frac{157A}{128}$	$\frac{273A}{256}$	$\frac{29A}{32}$	$\frac{273A}{256}$	$\frac{273A}{128}$	$\frac{343A}{128}$
7	A	$\frac{343A}{512}$	$\frac{343A}{256}$	$\frac{855A}{512}$	$\frac{343A}{256}$	$\frac{308A}{256}$	$\frac{273A}{256}$	$\frac{308A}{256}$	$\frac{77A}{32}$	2.873A
8	A	0.718A	1.437A	1.718A	1.437A	1.32A	$\frac{77A}{64}$	1.32A	2.756A	2.92A
9	A	0.76A	1.519A	1.759A	1.519A	1.419A	1.32A	1.419A	2.839A	3.179A
10	A	0.795A	1.589A	1.795A	1.589A	1.504A	1.419A	1.504A	3.009A	3.299A
11	A	0.825A	1.65A	1.825A	1.65A	1.577A	1.504A	1.577A	3.154A	3.402A
12	A	0.851A	1.701A	1.851A	1.701A	1.639A	1.577A	1.639A	3.278A	3.49A
13	A	0.872A	1.745A	1.872A	1.745A	1.692A	1.639A	1.692A	3.384A	3.564A
14	A	0.891A	1.782A	1.891A	1.782A	1.737A	1.692A	1.737A	3.474A	3.628A

The expression of the input voltage source is V_{in}=-5sin(2π*500000*t)kV. According to Equation(2.17), V_{out}=19.83kV, 0.1V_{out}=1.983kV=0.3966E, 0.9V_{out}=17.847kV=3.57E. When output voltage reaches to 10% of its maximum value, the voltage source is in its first period and D2 is conducting in the circuit. At this time point, V_{C2}=V_{out}=1.983kV, V_{C1}=V_m-V_{C2}=3.017kV. Therefore, the equation can be obtained:

$$-5sin(2\pi ft_1) + 3.017 = 1.983$$

$$t_1 = 0.934\mu s$$

When output voltage reaches to 90% of its maximum value, Table 2-5 shows that this situation happens in the 14^{th} switching period when D2 is conducting in the circuit. At this time, V_{C2}=V_{out}-V_{C4}=9.162kV, V_{C1} can be regarded as V_{C1}=0.891E=4.455kV.

$$5sin(2\pi ft_2) + 4.455 = 9.162$$

$$t_2 = 27.39\mu s$$

Therefore, the calculated rise time t_r=t_2-t_1=26.456μs.

2-5-2 Analysis of decay time

The decay process starts when the input voltage source is blocked. After the voltage source is blocked, the multiplier circuit is composed of capacitors and output load and the charged capacitors will charge the output load. Therefore, the decay process of output voltage can be regarded as the combination of several stages of RC discharging process. The RC discharging expression is $V_t = V_{om} * e^{-t/RC}$, where V_{om} is the maximum value of output voltage in steady state. τ is defined as time constant which equals to RC.

The decay process of the voltage quadrupler circuit with equal capacitance value per stage includes three stages.

In the first stage, only C_2 and C_4 are charging the output load while V_{C1} and V_{C3} keep unchanged because $V_{C2}+V_{C4}>V_{C1}+V_{C3}$. The discharging rates of C_2 and C_4 are the same. This stage finishes when V_{C2} and V_{C4} fall to such values that the relationship $V_{C2}+V_{C4}=V_{C1}+V_{C3}$ is fulfilled, which means that $V_{C2}=V_{C4}=7.5$kV, $V_{C1}=5$kV and $V_{C3}=10$kV at the end of first stage in this case. $V_{out}=15\text{kV}=0.75V_{om}$. In this stage, C_2 and C_4 are connected in series and the time constant $\tau_1=0.5R_LC$. The decay time in the first stage can be calculated:

$$0.75V_{om} = V_{om} * exp(-\frac{t_1}{\tau_1})$$

$$t_1 = -\tau_1 * ln(0.75) = 0.144R_LC$$

In the second stage, all the capacitors are charging the output load together with the same rate. This stage ends when V_{C1} discharges to 0. At the end of the second stage, $V_{C1}=0$, $V_{C2}=V_{C4}=2.5$kV, $V_{C3}=5$kV and $V_{out}=5\text{kV}=0.25V_{om}$. In this stage, C_1 and C_3 are connected in series, C_2 and C_4 are connected in series and the two series connections are connected in parallel. Therefore, the equivalent capacitance is $C_{eq}=10\text{nF}=C$. The time constant is $\tau_2=R_LC$. The decay time in the second stage can be calculated:

$$0.25V_{om} = 0.75V_{om} * exp(-\frac{t_2}{\tau_2})$$

$$t_2 = -\tau_2 * ln(\frac{1}{3}) = 1.1R_LC$$

In the third stage, C_2 , C_3 and C_4 are charging the output load together with the same rate. This stage finishes when the output voltage falls to $0.1V_{om}$. In this stage, C_2 and C_4 are connected in series and they are connected in parallel with C_3. Therefore, the equivalent capacitance is $C_{eq}=15\text{nF}=1.5C$. The time constant is $\tau_3=1.5R_LC$. The decay time in the third stage can be calculated:

$$0.1V_{om} = 0.25V_{om} * exp(-\frac{t_3}{\tau_3})$$

$$t_3 = -\tau_3 * ln(0.4) = 1.37R_LC$$

Therefore, the total decay time of the output voltage is $t_f=t_1+t_2+t_3=2.614R_LC$.

The calculation results of decay time are shown in Table 2-6.

Table 2-6: Calcultion results of decay time

Decay Stage	t_1	t_2	t_3
$t_{f,cal}/\mu s$	288	2200	2740

2-5-3 Simulations and discussions

Simulations are made in LTspice to verify the theoretical analysis of rise time and decay time. The simulation parameters and circuit are shown in Table 2-1 and Figure 2-4 respectively.

The simulation waveform of rise time is shown in Figure 2-18(a) and that of decay time is shown in Figure 2-18(b). The simulation results are shown in Table 2-7.

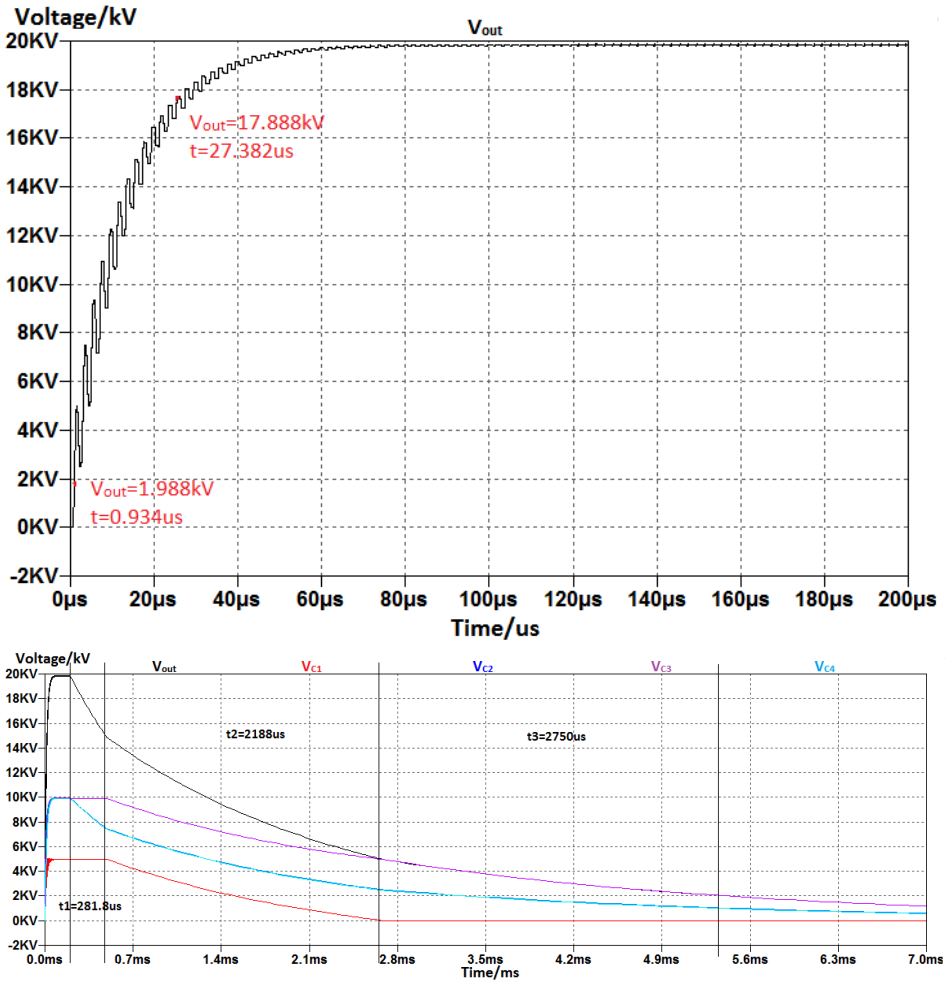

Figure 2-18: Simulation waveform of rise time and decay time

Discussions:

1.The simulation results correspond with the theoretical analysis in section 2-5-1 and 2-5-2. When the stage number is varied, similar analyses like methods in section 2-5-1 and 2-5-2 can be applied to calculate the rise time and decay time of output voltage theoretically.

Table 2-7: Simulation results of rise time and decay time

	Rise time	Decay time			
		t_1	t_2	t_3	t_f
$t_{cal}/\mu s$	26.456	288	2200	2740	5228
$t_{sim}/\mu s$	26.448	281.8	2188	2750	5219.8
Errors	0.03%	2.2%	0.5%	0.36%	0.15%

The rise time is related with the operations in start-up process. When the capacitance distribution is equal in the circuit, the rise time is directly determined by the operating frequency. When unequal capacitance distribution is applied in the circuit, the rise time will be influenced by the capacitance value, which will be further discussed in the Chapter 6.

The decay process is the combination of several stages of RC discharging processes made up of capacitors and output load. The decay time is determined by the values of capacitance and output load. The influence of circuit parameters to rise time and decay time are futher discussed in Chapter 3.

2-6 Other voltage multiplier topologies

The multiplier circuit applied in this project is the commonly used series HWCW voltage multiplier circuit. However, the voltage multiplier circuit has many other common topologies such as half-wave parallel voltage multiplier and full-wave series voltage multiplier. In this section, the other topologies of Cockcroft walton voltage multiplier circuit are introduced to compare with the series HWCW voltage multiplier. The stage numbers of all the multiplier circuits introduced in this section are two.

2-6-1 Full-wave Cockcroft-Walton voltage multiplier circuit

The full-wave C.W. voltage multiplier circuit(FWCW) is also known as symmetrical C.W. voltage multiplier circuit as is shown in Figure 2-19. A center-tapped transformer is needed for the full-wave voltage multiplier to supply the two symmetrical parts of the circuit. Compared with the half-wave C.W voltage multiplier, the full-wave multiplier has better voltage regulation which is shown in Table 2-8[15][16]. However, the number of passive components in FWCW multiplier circuit is obviously increased. The frequency of output ripple in full-wave voltage multiplier is twice the frequency of input voltage, therefore, it is easier to filter high frequency ripples.

Table 2-8: Voltage drop and Voltage ripple comparison

	Voltage drop	Voltage ripple
HWCW VM	$(\frac{2}{3}n^3+\frac{1}{2}n^2-\frac{1}{6}n)\frac{I_o}{fC}$	$\frac{n(n+1)}{2}\frac{I_o}{fC}$
FWCW VM	$(\frac{1}{6}n^3+\frac{1}{4}n^2+\frac{1}{3}n)\frac{I_o}{fC}$	$\frac{n}{2}\frac{I_o}{fC}$

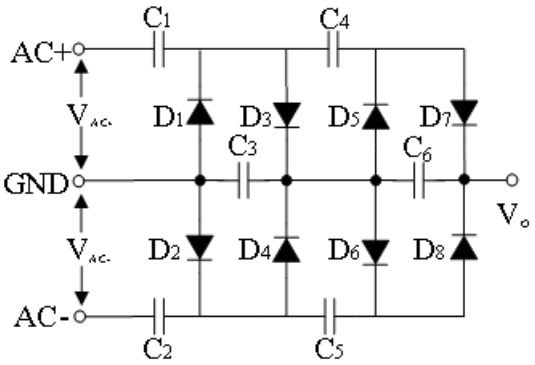

Figure 2-19: 2-stage Full-wave Cockcroft-Walton voltage multiplier

The principle of operations in FWCW Voltage multiplier is similar with the HWCW voltage multiplier. The steady state capacitor voltage values in the first stage (C_1 and C_2 in Figure 2-19) are V_m and other steady state capacitor voltage values are $2V_m$.

The anti-phase sinusoidal input voltage V_{AC+} and V_{AC-} are provided by the center-tapped transformer. V_{AC+} and V_{AC-} have the same amplitude with phase difference of 180°. In the two-stage full-wave multiplier circuit, C_3 and C_6 are two output capacitors which feed the output load if existed. The output voltage V_{out}=V_{C3}+V_{C6}. The full-wave C.W. voltage multiplier can be seen as two HWCW voltage multiplier connected in parallel. Therefore, the operations in the start-up process of the full-wave multiplier circuit are similar with those of the HWCW multiplier circuit.

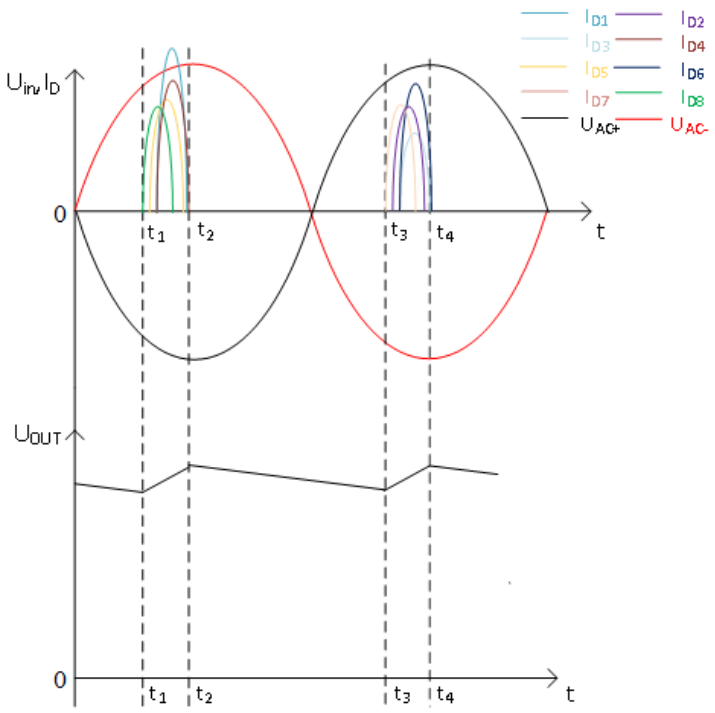

Figure 2-20: Waveform in steady state for FWCW multiplier circuit

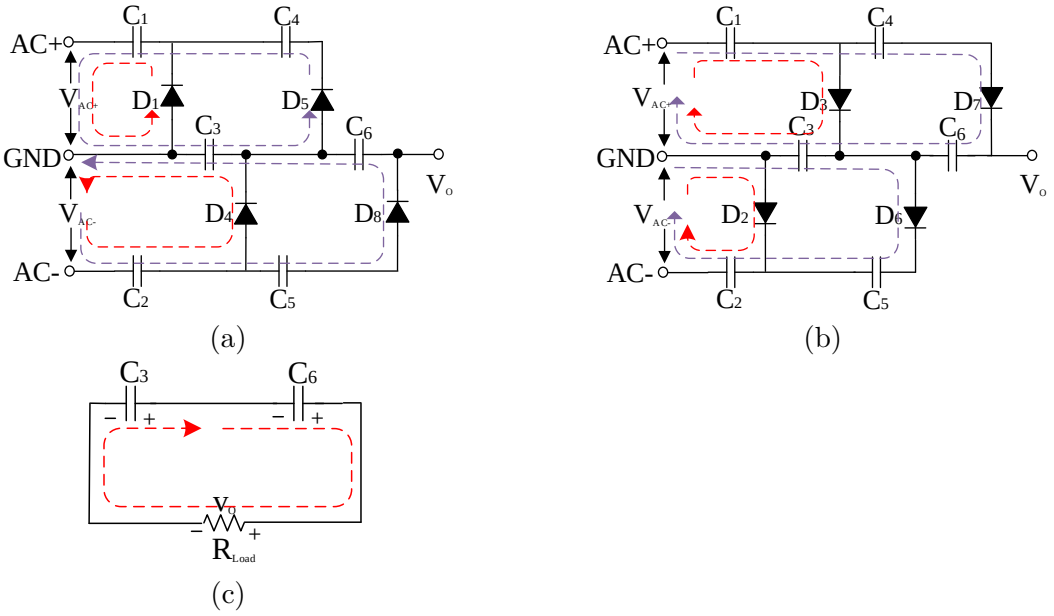

Figure 2-21: Equivalent circuits in steady state for FWCW circuit

In steady state, V_{C1}=V_{C2}=V_m, voltage across other capacitors are $2V_m$, the output voltage equals to 2n*V_m. The voltage and diode waveform in steady state is shown in Figure 2-20.

- t_1 to t_2

  U_{AC+} is in the negative switching cycle and U_{AC-} is in the positive switching cycle. Therefore, D_1, D_4, D_5 and D_8 are conducting while D_2, D_3, D_6 and D_7 are blocked. The equivalent circuit is shown in Figure 2-21(a). Rectifiers in higher stages conduct prior to rectifiers in low stages.

  During this time interval, C_1 and C_4 are charged by the voltage source while the output capacitors C_3 and C_6 are charged by C_2 and C_5. Therefore, the output voltage increases during this time period.

- t_2 to t_3

  From t_2 to t_3, all the diodes are blocked and the output capacitors C_3 and C_3 are charging the load, which makes the output voltage decrease during this time interval. The equivalent circuit is shown in Figure 2-21(c).

- t_3 to t_4

  From t_3 to t_4, U_{AC+} is in the positive switching cycle and U_{AC-} is in the negative switching cycle. Therefore, D_2, D_3, D_6 and D_7 are conducting while D_1, D_4, D_5 and D_8 are blocked. The equivalent circuit is shown in Figure 2-21(b).

  During this time interval, C_2 and C_5 are charged by the voltage source while the output capacitors C_3 and C_6 are charged by C_1 and C_4. The output voltage increases as a result.

Simulations of the FWCW voltage multiplier circuit are made in comparison with HWCW multiplier circuit in LTspice. The model for the FWCW voltage multiplier circuit is shown Figure 2-22 and the parameters are shown in Table 2-1.

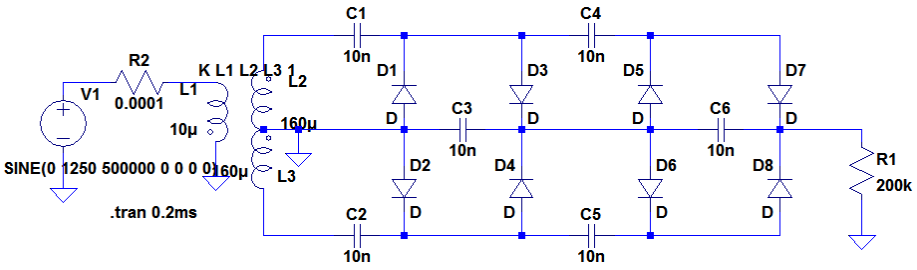

Figure 2-22: Simulation circuit for FWCW multiplier circuit

The simulation results are shown in Figure 2-23.

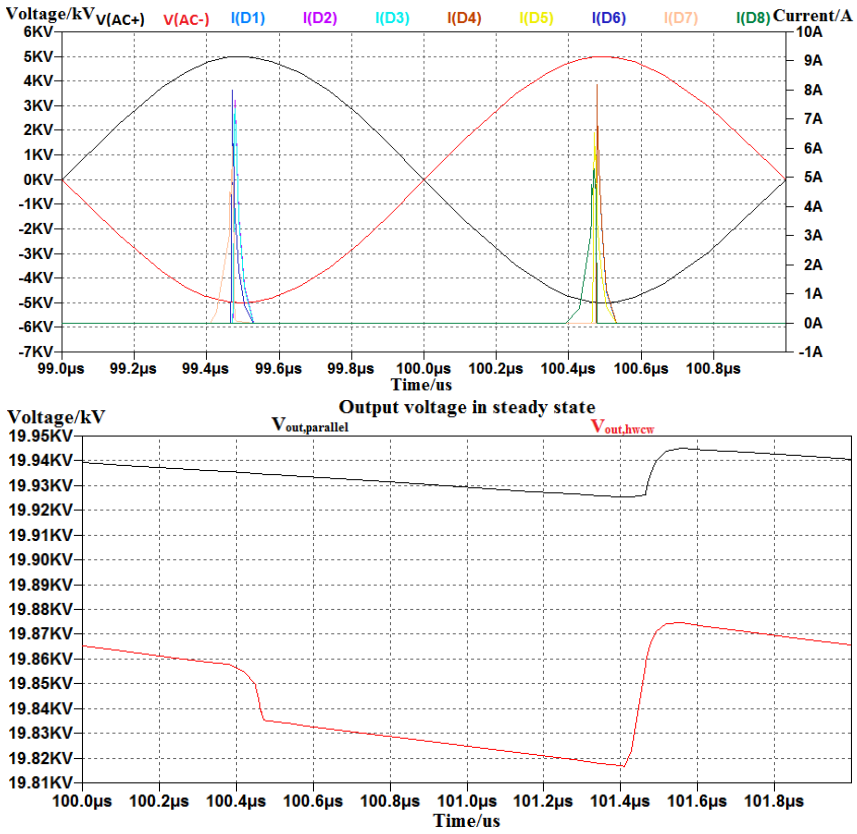

Figure 2-23: Simulation waveform of FWCW multiplier circuit

The simulation results correspond with the theoretical analysis. From Figure 2-23(b), voltage drop and voltage ripple of the FWCW voltage multiplier circuit are smaller than those of the HWCW voltage multiplier circuit which can be calculated using the equations shown in Table 2-8. the full-wave multiplier has better voltage regulation than the HWCW voltage multiplier.

FWCW voltage multiplier is developed due to the relatively high voltage drop and voltage ripple of the HWCW voltage multiplier. The output voltage ripple of the two parallel half-wave multiplier are almost the same with 180 phase difference. Since the output voltage of the full-wave multiplier is the summation of the output voltage of two half-wave multipliers, the magnitude of output voltage ripple of full-wave multiplier circuit is much smaller than that of the half-wave multiplier circuit. However, since the center-tapped transformer is needed and the number of capacitors increases in the FWCW voltage multiplier circuit, the size and cost also increase as a result.

2-6-2 Half-wave parallel voltage multiplier circuit

The half-wave parallel voltage multiplier shown in Figure 2-24 has the advantage of small size, high efficiency and uniform stress on diodes. Compared with the series voltage multiplier, the parallel voltage multiplier requires higher voltage ratings for capacitors per stage.

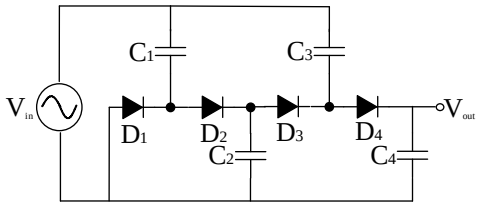

Figure 2-24: 2-stage half-wave parallel voltage multiplier

The waveform of capacitor voltage in the start-up process is shown in Figure 2-25.

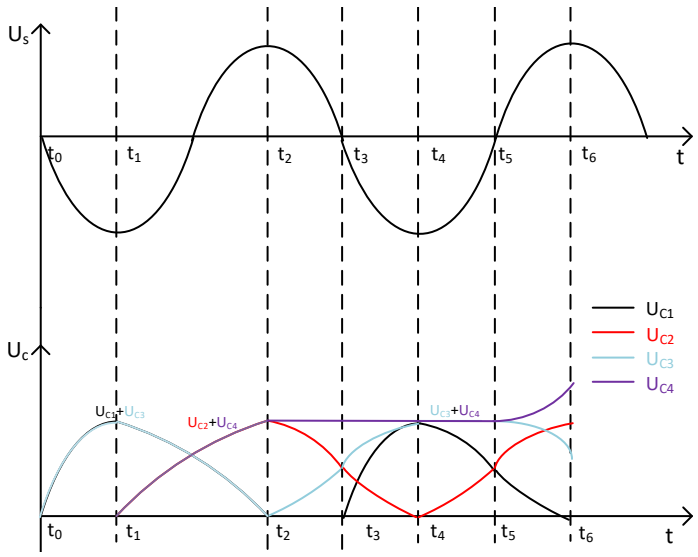

Figure 2-25: Waveform in start-up process of parallel voltage multiplier

- t_0 to t_1
  From t_0 to t_1, the voltage source is decreasing in the negative cycle. Therefore D_1,D_2

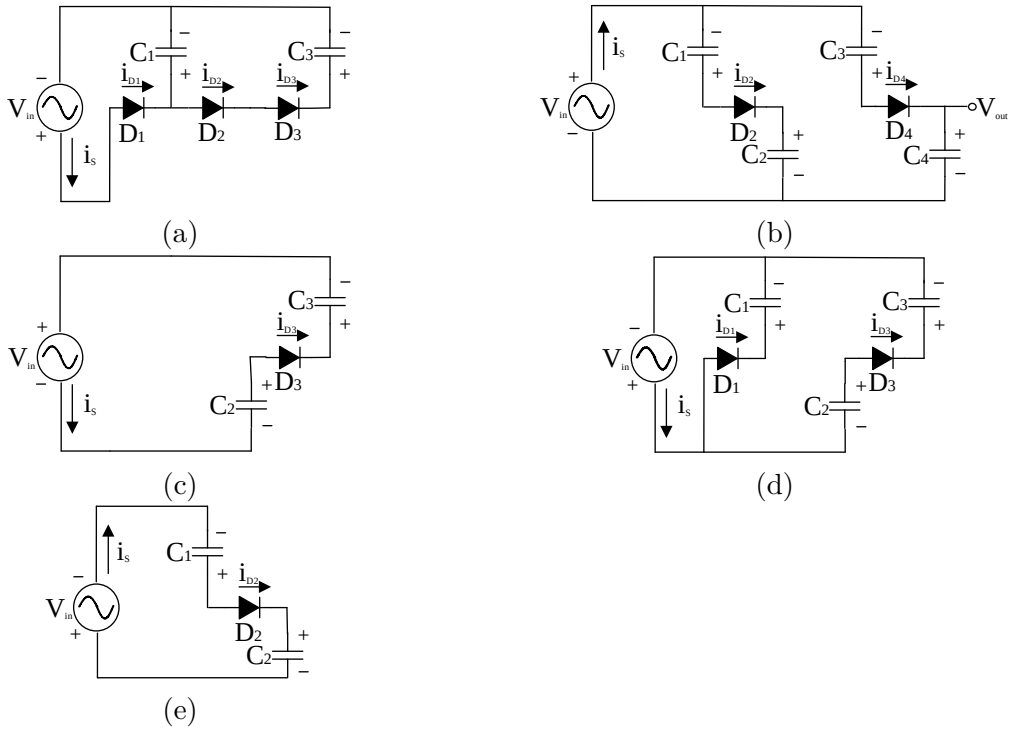

Figure 2-26: Equivalent circuits in start-up process of parallel voltage multiplier

and D_3 are conducting while D_4 is blocked. The equivalent circuit is shown in Figure 2-26(a). As a result, C_1 and C_3 are connected in parallel and they are charged to V_m at t_1 by voltage source.

- t_1 to t_2
  From t_1 to t_2, the voltage source is increasing from -V_m to V_m. Since C_1 and C_3 are charged to V_m at t_1, D_2 and D_4 are conducting while D_1 and D_3 are blocked in this stage.The equivalent circuit is shown in Figure 2-26(b). Therefore, C_1 and C_2 are connected in parallel with C_3 and C_4, C_1 and C_3 are discharged to 0 while C_2 and C_4 are charged to V_m at t_2. The charges can be seen as moving from C_1 to C_2 and from C_3 to C_4.

- t_2 to t_3
  From t_2 to t_3, the voltage source is in the positive switching cycle and its value is decreasing. Since V_{C2}=V_{C4}=V_m and V_{C1}=V_{C3}=0 at t_2, D_1,D_2 and D_4 are all blocked and only D_3 is conducting.The equivalent circuit is shown in Figure 2-26(c). Therefore, C_2 and C_3 are connected to the voltage source in series, C_2 is discharged to $\frac{V_m}{2}$ and C_3 is charged to $\frac{V_m}{2}$ at t_3.

- t_3 to t_4
  From t_3 to t_4, the voltage source is decreasing in the negative cycle. Since V_{C1}=0, V_{C2}=V_{C3}=$\frac{V_m}{2}$ and V_{C4}=V_m at t_3, D_1 and D_3 are conducting while D_2 and D_4 are blocked. The equivalent circuit is shown in Figure 2-26(d). In this stage, C_2 continues to discharge to 0 and C_3 continues to be charged to V_m, C_1 is charged to V_m again by the voltage source at t_4.

- t_4 to t_5
  From t_4 to t_5, the voltage source increases from -V_m to 0. Since V_{C1}=V_{C3}=V_{C4}=V_m and V_{C2}=0, D_1, D_3 and D_4 are blocked while only D_2 is conducting. The equivalent circuit is shown in Figure 2-26(e). C_1 and C_2 are connected in series, C_1 is discharged and C_2 is charged. V_{C1}=V_{C2}=$\frac{V_m}{2}$ at t_5.

- t_5 to t_6
  From t_5 to t_6, the voltage source increases in the positive switching cycle. Therefore D_4 starts to conduct together with D_2. The equivalent circuit is also shown in Figure 2-26(b). C_1 and C_3 are discharged while C_2 and C_4 are charged in this stage.

Same operations are repeated in the following periods until the steady state is reached. Charges move from C_1 to C_2, C_2 to C_3 and C_3 to C_4 and the values of V_{C2}, V_{C3} and V_{C4} keep increasing before steady state. In steady state, the V_{C1}=V_m, V_{C2}=2V_m, V_{C3}=3V_m and V_{C4}=4V_m.

The waveform in steady state is shown in Figure 2-27.

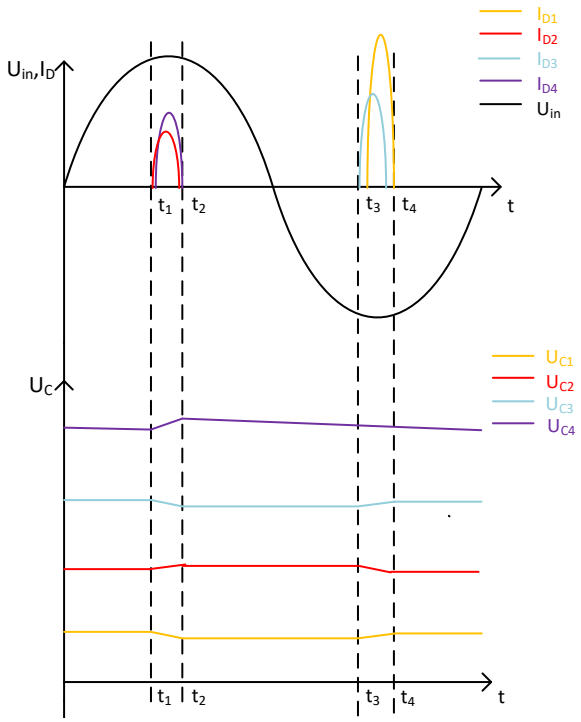

Figure 2-27: Waveform in steady state of parallel voltage multiplier

- t_1 to t_2
  From t_1 to t_2, D_2 and D_4 are conducting while D_1 and D_3 are blocked. The equivalent circuit is shown in Figure 2-26(b). Therefore C_1 and C_3 are discharged while C_2 and C_4 are charged.

- t_3 to t_4
  From t_3 to t_4, D_1 and D_3 are conducting while D_2 and D_4 are blocked. The equivalent

circuit is shown in Figure 2-26(d). Therefore, C_1 and C_3 are charged while C_2 are discharged. C_4 is also discharged because C_4 is charging the output load.

The simulation of the parallel voltage multiplier is also made in comparison with the series HWCW voltage multiplier in LTspice. The simulation circuit is shown in Figure 2-28 and the parameters are shown in Table 2-1.

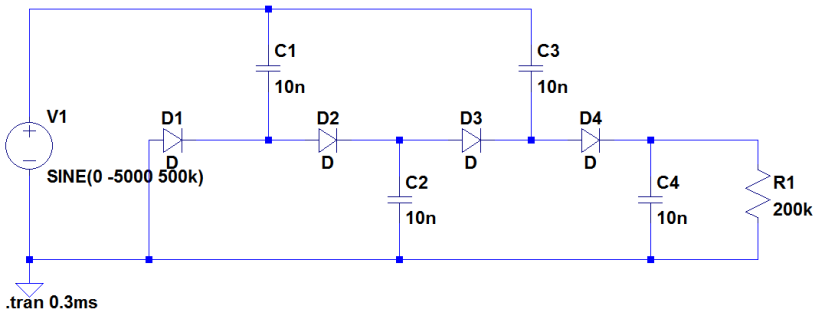

Figure 2-28: Simulation circuit for HW parallel multiplier circuit

The simulation results are shown in Figure 2-29. The waveform of capacitor voltage in start-up process is in Figure 2-29(a), the waveform of diode current in steady state is in Figure 2-29(b) and the comparison of capacitor voltage of series and parallel multiplier circuit in steady state is in Figure 2-29(c).

The simulation results correspond with the theoretical analysis. The voltage drop and voltage ripple is decreased in parallel voltage multiplier due to the fact that the output voltage is provided only by the last capacitor in the parallel multiplier circuit while the output voltage is summation of voltage across output capacitors in the series multiplier circuit.

2-6-3 Discussions

The output voltage drop and voltage ripple of the three multiplier circuits discussed in this section are compared in Table 2-9. Both the full-wave series C.W. voltage multiplier and the

Table 2-9: Comparison of voltage drop and voltage ripple of different topologies

	Voltage drop/V	Voltage ripple/V
Half-wave series CW VM	163	58
Full-wave series CW VM	59	18
Half-wave parallel CW VM	69	20

half-wave parallel C.W. voltage multiplier have better voltage regulation behavior. However, the center-tapped transformer and more passive components are needed in the full-wave series C.W. voltage multiplier circuit which results in the increase in size and cost of the power supply circuit. The voltage stress across capacitors in the half-wave parallel C.W. voltage multiplier circuit are inequal. Capacitors in high stages have to stand higher voltage stress than capacitors in low stages and the selections of capacitors in high stages have to be made

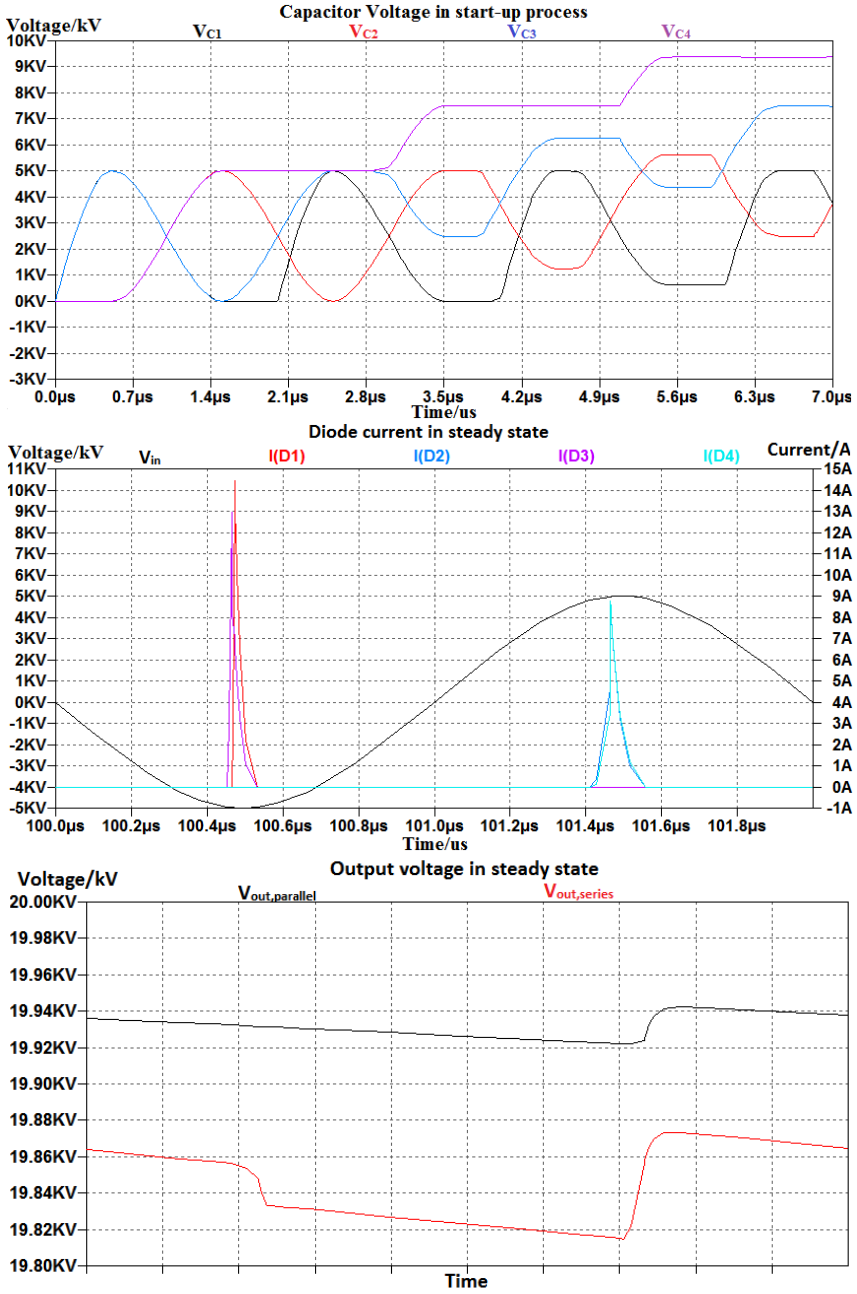

Figure 2-29: Simulation waveform of HW parallel multiplier circuit

sure that the capacitors will not be broken down. The parallel multiplier circuit is not suitable for high voltage power supplies.

Taking the requirements for output voltage value, physical size and cost into consideration, the series half-wave Cockcroft-Walton voltage multiplier circuit is selected as a part of the power supply in this project.

2-7 Summary

In this chapter, the operating principles of the voltage quadrupler circuit in start-up process and steady state are explained explicitly in section 2-1 and section 2-2. The operations in different time intervals are analyzed and simulations are made in LTspice to verify the theoretical analyses.

Important electrical performances of the voltage multiplier circuit including voltage regulation parameters(voltage drop and voltage ripple) and respond time(rise time and decay time) of output voltage are introduced in section 2-3 and section 2-5 respectively. Formulas to calculate the voltage drop and voltage ripple are derived in section 2-3-1. Methods to calculate the respond time theoretically are introducted in section 2-5. The rise time is related with the operations in start-up process and the decay time is combination of several stages of RC discharging process.

Different rectifier circuit are compared in section 2-4 to explain why the voltage quadrupler circuit is selected as a case study in this project. At last, the HWCW voltage multiplier circuit is compared with other topologies such as full-wave series CW voltage multiplier and half-wave parallel CW voltage multiplier to clarify the reason of choosing the HWCW voltage multiplier circuit in the project in section 2-6. The advantages and drawbacks of different circuits are shown in Table 2-10. The choice of the rectifier circuit topology should base on the specific requirements for voltage value, voltage drop, voltage ripple, physical size and cost.

The analyses in the following chapters are based on the results in this chapter.

Table 2-10: Advantages and Drawbacks of different rectifier circuits

	Advantages	Drawbacks
HWCW VM	1.AC-DC voltage conversion 2.Moderate voltage drop and ripple 3.No center-tapped transformer 4.Moderate physical size and cost	1.Bad voltage regulation with large stage number
Bridge rectifier	1.AC-DC voltage conversion 2.Small physical size and cost 3.No center-tapped transformer 4.No voltage drop	1.Large voltage ripple 2.unable to boost voltage value
FWCW VM	1.AC-DC voltage conversion 2.Small voltage drop and ripple	1.Center-tapped tranformer needed 2.Large physical size and cost 3.Doubled output rippler frequency
Parallel VM	1.AC-DC voltage conversion 2.Small voltage drop and ripple 3.No center-tapped tranformer	1.Large voltage stress across capacitors in high stages

Chapter 3

Impact of Circuit Parameters on Electrical Performances

As is discussed in the section 2-3 and 2-5, the electrical performances of the multiplier circuit(voltage drop&voltage ripple and rise time&decay time) are influenced by the circuit parameters such as operating frequency, capacitance value, output power and stage number. In this chapter, the impact of circuit parameters on electrical performance are discussed separately.

Several assumptions are valid in this chapter:

- All the components in the circuit are considered to be ideal.
- The capacitance distribution is equal in each stage.
- The influence of the output load is neglected.
- The charging and discharging time of capacitors are much smaller than the period of input voltage source.

The influence of operating frequency, capacitance value and output power are discussed in section 3-1,3-2 and 3-3 respectively. Optimal stage number for the HWCW multiplier circuit is derived in section 3-4.

3-1 Influence of frequency to electrical performance

3-1-1 Influence of frequency to voltage drop and voltage ripple

From equation (2-5) and (2-6), it can be inferred that the voltage drop and voltage ripple are in inverse proportion to frequency when other parameters are constant. In order to

investigate the influence of frequency, the operating frequency is set to be 3 different values: 100kHz,500kHz and 1MHz while other parameters shown in Table 2-1 keep unchanged.

The calculation results of voltage drop and voltage ripple with different values of operating frequency are shown in Talbe 3-1.

Table 3-1: Calculation results of voltage regulation with different frequency values

Frequency	100kHz	500kHz	1MHz
Voltage drop/V	700	140	70
Voltage ripple/V	300	60	30

Simulations are made in LTspice to compare with the calculations. The simulation waveform is shown in Figure 3-1 and the simulation results are shown in Table 3-2.

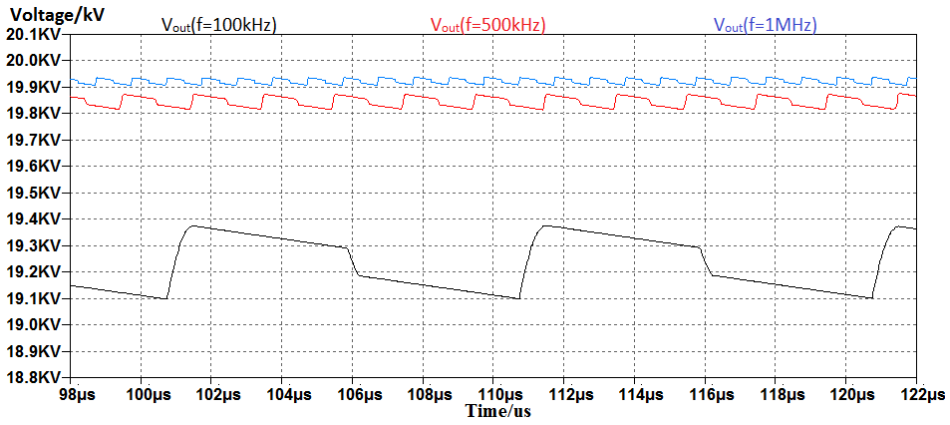

Figure 3-1: Simulation waveform of voltage regulation with different frequency values

Table 3-2: Simulation results of voltage regulation with different frequency values

	ΔV_{sim}/V	ΔV_{cal}/V	Errors	δV_{sim}/V	δV_{cal}/V	Errors
100kHz	637	700	9.9%	278	300	7.9%
500kHz	130.7	140	7.1%	58.1	60	3.2%
1MHz	65.3	70	6.7%	29.1	30	3%

The errors between the calculation results and the simulation results come from the fact that the output current is assumed to be ideal during calculation, which means that the voltage drop and voltage ripple are not considered in calculation. Therefore, the value of output current used in calculation is larger than its real value and the calculated voltage drop and voltage ripple values are larger than the real values as well.

From both calculation and simulation results, it can be verified that voltage drop and voltage ripple are in inverse proportion to frequency. In this case, only the operating frequency is changed while other parameters are the same. The charge Q_o through the output load also changes in inverse proportion to frequency due to $Q_o = \frac{I_o}{f}$. The charge through capacitors change in inverse proportional to frequency as well as is explained in section 2-3. Since the capacitance value keeps constant, the voltage across capacitors are also in inverse proportion

to frequency due to $V_C = \frac{Q_C}{C}$. Due to the fact that the output voltage drop and voltage ripple are the summation of those of output capacitors, the output voltage drop and voltage ripple are in inverse proportion to frequency.

3-1-2 Influence of frequency to rise time

The analysis of rise time is explained in section 2-5-1 in details. For the voltage quadrupler circuit with equal capacitance distribution per stage, the rise time of output voltage takes around 13.5 switching periods. Therefore, the rise time is directly determined by frequency and they are in inverse proportion.

The rise time of output voltage under different operating frequencies can be calculated using the methods introduced in section 2-5-1. The calculation results are shown in Table 3-3.

Table 3-3: Calculation results of rise time with different frequency values

Frequency	100kHz	500kHz	1MHz
Rise time/μs	132.34	26.456	13.232

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-2 and the simulation results are shown in Table 3-4.

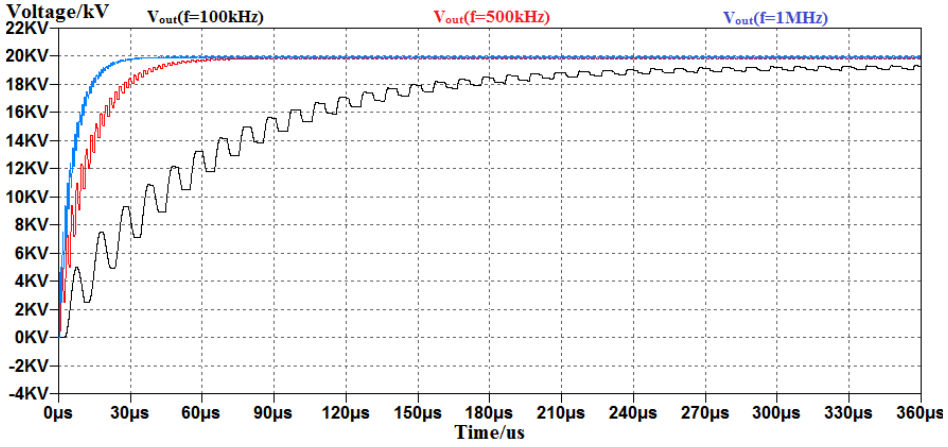

Figure 3-2: Simulation waveform of rise time with different frequency values

Table 3-4: Simulation results of rise time with different frequency values

Frequency	$t_{r,sim}/\mu$s	$t_{r,cal}/\mu$s	Errors
100kHz	132.25	132.34	0.07%
500kHz	26.448	26.456	0.03%
1MHz	13.224	13.232	0.07%

The simulation results correspond with the theoretical calculations. The rise time of the output voltage is in inverse proportion to frequency because the rise time is related with the periods of the input voltage source when the topology of the multiplier circuit is determined. In order to get fast rise time , the voltage multiplier circuit should work under high frequency.

3-1-3 Influence of frequency to decay time

As is discussed in section 2-5-2, the decay process the combination of several stages of RC discharging processes. The decay time is only related with the value of capacitance and output load. Therefore, it can be inferred that frequency has nothing to do with the decay time.

The calculation results of the decay time with different frequencies are the same as is shown in Table 3-5.

Table 3-5: Calculation results of decay time with different frequency values

Frequency	100kHz	500kHz	1MHz
Decay time/μs	5228	5228	5228

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-3 and the simulation results are shown in Table 3-6.

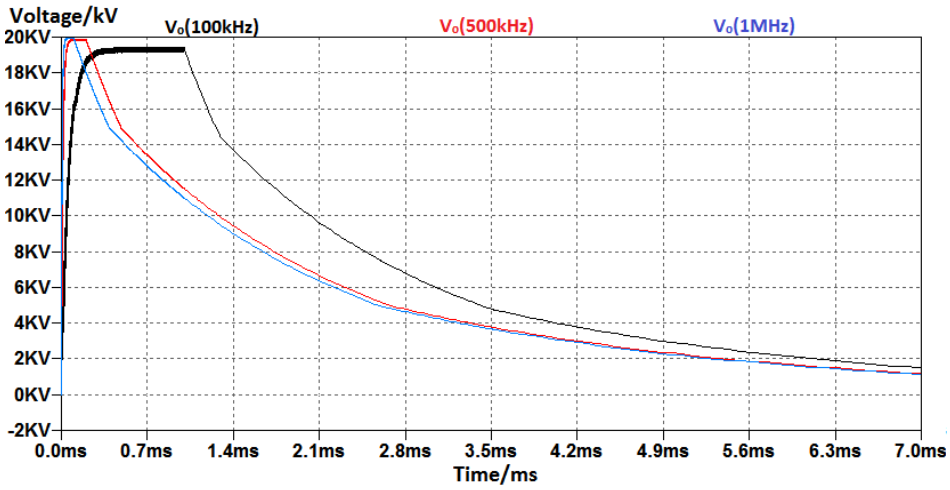

Figure 3-3: Simulation waveform of rise time with different frequency values

Table 3-6: Simulation results of rise time with different frequency values

Frequency	$t_{f,sim}/\mu s$	$t_{f,cal}/\mu s$	Errors
100kHz	5220	5228	0.15%
500kHz	5219.8	5228	0.15%
1MHz	5221	5228	0.13%

Discussions:

1.The frequency is in inverse proportion to charge flowing through output load and then the voltage across capacitors are in inverse proportion to frequency as well. As a result, the output voltage drop and voltage ripple are in inverse proportion to frequency as well.

2.The rise time is related with the periods of the input voltage source, therefore, the rise time is in inverse proportion to frequency.

3.The decay process has nothing to do with frequency since the decay process is the RC discharging process which is only related with the values of capacitance and load resistance.

3-2 Influence of capacitance value to the electrical performance

3-2-1 Influence of capacitance value to voltage drop and voltage ripple

From equation (2-5) and (2-6), it can be inferred that the voltage drop and voltage ripple are in inverse proportion to the capacitance value when other parameters are constant. In order to investigate the influence of capacitance value, the capacitance value is set to be 3 different values: 1nF,10nF and 50nF while other parameters shown in Table 2-1 are kept unchanged.

The calculation results of voltage drop and voltage ripple with different capacitance values are shown in Talbe 3-7.

Table 3-7: Calculation results of voltage regulation with different capacitance values

Capcitance	1nF	10nF	50nF
Voltage drop/V	1400	140	28
Voltage ripple/V	600	60	12

Simulations are made in LTspice to compare with the calculations. The simulation waveform is shown in Figure 3-4 and the simulation results are shown in Table 3-8.

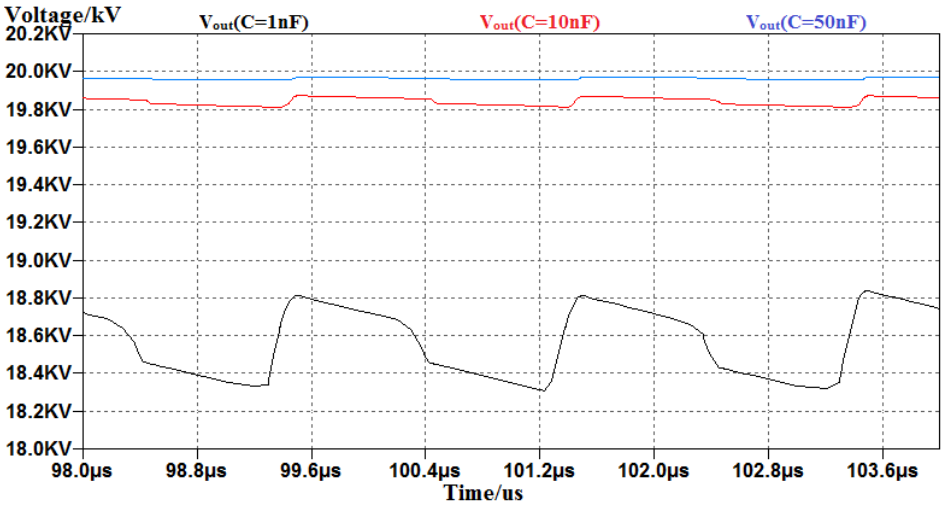

Figure 3-4: Simulation waveform of voltage regulation with different capacitance values

The errors between the calculation results and the simulation results come from the fact that the output current is assumed to be ideal during calculation. When the real voltage drop and voltage ripple are relatively large, the errors between calculation and simulation results are large as well.

From both calculation and simulation results, it can be verified that voltage drop and voltage ripple are in inverse proportion to capacitance value. In this case, only the capacitance value

Table 3-8: Simulation results of voltage regulation with different capacitance values

	$\Delta V_{sim}/V$	$\Delta V_{cal}/V$	Errors	$\delta V_{sim}/V$	$\delta V_{cal}/V$	Errors
1nF	1199	1400	16.8%	495	600	21.2%
10nF	130.7	140	7.1%	58.1	60	3.2%
50nF	27.7	28	1.1%	11.6	12	3.4%

is changed. The charge Q_o through the output load keeps unchanged due to $Q_o=\frac{I_o}{f}$ and the charge through capacitors keep unchanged as well. Therefore, the voltage across capacitors are in inverse proportion to the capacitance value due to $V_C=\frac{Q_C}{C}$. Since the output voltage drop and voltage ripple are the summation of those of output capacitors, the output voltage drop and voltage ripple are in inverse proportion to capacitance value.

3-2-2 Influence of capacitance value to rise time

Even though the rise time is not directly determined by the capacitance value, it will still be influenced in some cases because the capacitance value will influence the steady state value of output voltage.

For example, when C=1nF, V_{out}=18.3kV and $0.9V_{out}$=16.27kV=3.294E. Therefore, the output voltage rises to $0.9V_{out}$ in the 10^{th} switching period of the input voltage when D_2 is conducting in the circuit. The calculation results of rise time are shown in Table 3-9.

Table 3-9: Calculation results of rise time with different capacitance values

Capacitance	1nF	10nF	50nF
Rise time/μs	20.546	26.456	26.454

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-5 and the simulation results are shown in Table 3-10.

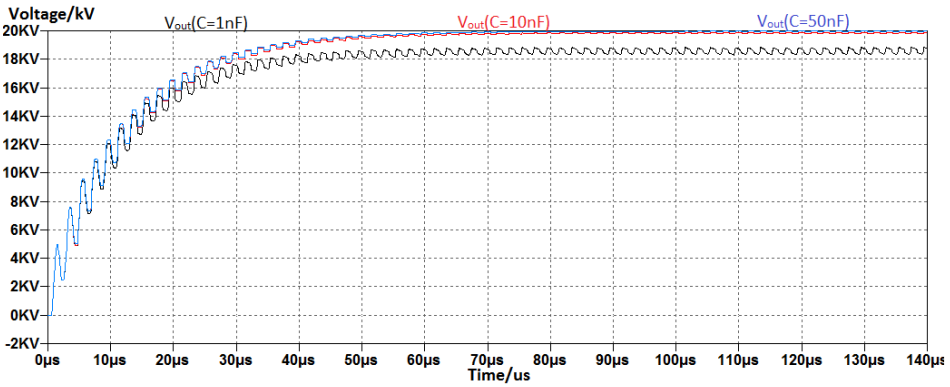

Figure 3-5: Simulation waveform of rise time with different capacitance values

The simulation results correspond with the theoretical calculations. The rise time is not determined by capacitance value but it will be influenced by capacitance value in some cases.

Table 3-10: Simulation results of rise time with different capacitance values

Capacitance	$t_{r,sim}/\mu s$	$t_{r,cal}/\mu s$	Errors
1nF	20.607	20.546	0.3%
10nF	26.448	26.456	0.03%
50nF	26.443	26.454	0.08%

3-2-3 Influence of capacitance value to decay time

As is discussed in section 2-5-2, the decay process is the combination of several stages of RC charging processes. The decay time is proportional to the capacitance value.

The calculation results of the decay time with different capacitance values are shown in Table 3-11.

Table 3-11: Calculation results of decay time with different capacitance values

Capacitance	1nF	10nF	50nF
Decay time/ms	0.523	5.228	26.14

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-6 and the simulation results are shown in Table 3-12.

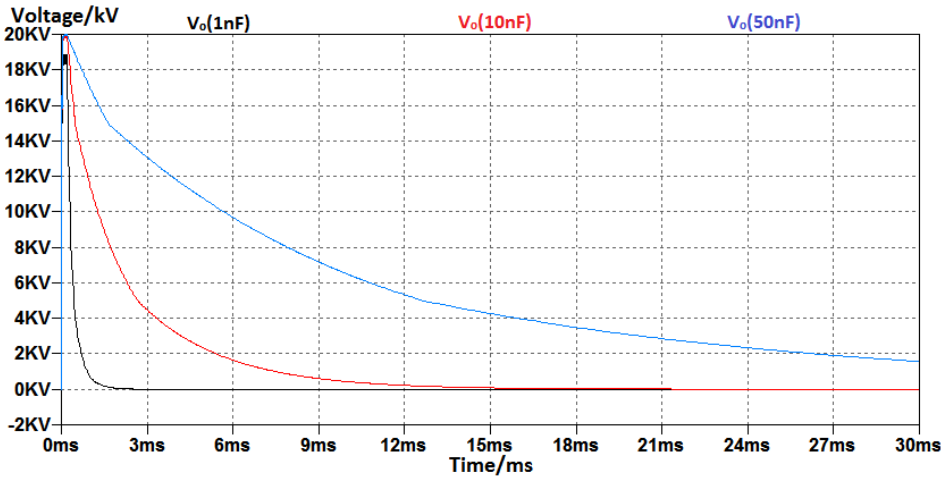

Figure 3-6: Simulation waveform of rise time with different capacitance values

The simulation results correspond with the theoretical analysis. From both the theoretical analysis and the simulation results, the decay time is proportional to the capacitance value. In order to obtain fast decay time, the capacitance in the multiplier circuit should be chosen as small as possible.

Discussions:

1. The voltage drop and voltage ripple are in inverse proportion to the capacitance value because the voltage across capacitors are in inverse proportion to the capacitance value when the charge are not changed.

Table 3-12: Simulation results of rise time with different capacitance values

Capacitance	$t_{f,sim}$/ms	$t_{f,cal}$/ms	Errors
1nF	0.522	0.523	0.19%
10nF	5.22	5.228	0.15%
50nF	26.16	26.14	0.08%

2.The rise time is not directly determined by the capacitance value. However, the capacitance value will influence the voltage drop and voltage ripple and as a result the steady state value of output voltage is changed. Due to the changed output voltage, the number of switching cycles for the output voltage to rise from 10% to 90% of its steady state value will be influenced.The smaller the capacitance value is, the smaller the rise time is. The relationship between the capacitance value and rise time is nonlinear.

3.The decay process is the RC discharging process and the decay time is proportional to the capacitance value. In order to achieve fast respond time, the capacitance should be chosen as small as possible.

3-3 Influence of output power to the electrical performance

3-3-1 Influence of output power to voltage drop and voltage ripple

In the multiplier circuit, the output power is controlled by setting different values of the output load P_{out}=U_o*I_o=$\frac{U_o^2}{R_L}$. From equation (2-5) and (2-6), it can be inferred that the voltage drop and voltage ripple are proportional to output power when other parameters are constant.

In order to investigate the influence of output power, the output power is set to be 3 different values: 1kW,2kW and 4kW by controlling the output load to be 400kΩ, 200kΩ and 100kΩ respectively. Other parameters are shown in Table 2-1 and kept unchanged.

The calculation results of voltage drop and voltage ripple with different output power are shown in Talbe 3-13.

Table 3-13: Calculation results of voltage regulation with different output power

Output power	1kW	2kW	4kW
Voltage drop/V	70	140	280
Voltage ripple/V	30	60	120

Simulations are made in LTspice to compare with the calculations. The simulation waveform is shown in Figure 3-7 and the simulation results are shown in Table 3-14.

The errors between the calculation results and the simulation results come from the fact that the output current is assumed to be ideal during calculation.

From both calculation and simulation results, it can be verified that voltage drop and voltage ripple are proportional to output power. In this case, only the output power is changed. The

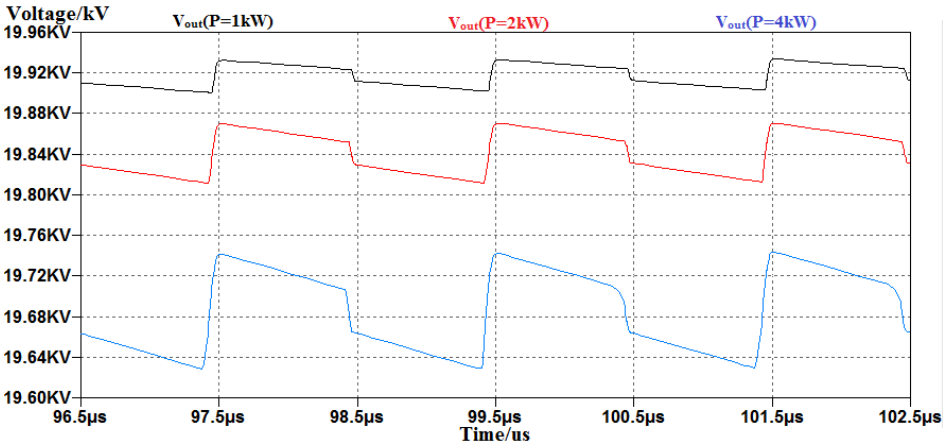

Figure 3-7: Simulation waveform of voltage regulation with different output power

Table 3-14: Simulation results of voltage regulation with different output power

	ΔV_{sim}/V	ΔV_{cal}/V	Errors	δV_{sim}/V	δV_{cal}/V	Errors
1kW	67.3	70	4%	29.8	30	0.6%
2kW	130.7	140	7.1%	58.7	60	2.2%
4kW	257	280	8.9%	113.8	120	5.4%

charge Q_o through the output load are proportional to output power due to $Q_o=\frac{I_o}{f}$ and the charge through capacitors are proportional to output power as well. Therefore, the voltage across capacitors are in proportion to the output power due to $V_C=\frac{Q_C}{C}$. Since the output voltage drop and voltage ripple are the summation of those of output capacitors, the output voltage drop and voltage ripple are proportional to output power.

3-3-2 Influence of output power to rise time

Even though the rise time is not directly determined by output power, it will still be influenced in some cases because the output power will influence the steady state value of output voltage.

For example, when P_{out}==4kW, V_{out}=19.66kV and $0.9V_{out}$=17.694kV=3.5388E. Therefore, the output voltage rises to $0.9V_{out}$ in the 13^{th} switching period of the input voltage when D_2 is conducting in the circuit. The calculation results of rise time are shown in Table 3-15.

Table 3-15: Calculation results of rise time with different output power

Output power	1kW	2kW	4kW
Rise time/μs	26.471	26.456	24.497

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-8 and the simulation results are shown in Table 3-16.

The simulation results correspond with the theoretical calculations. The rise time is not determined by output power but it will be influenced by output power in some cases.

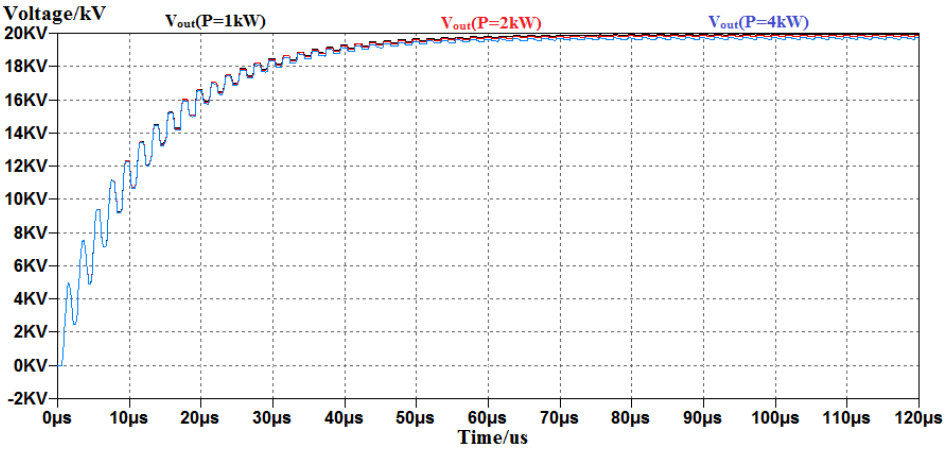

Figure 3-8: Simulation waveform of rise time with different output power

Table 3-16: Simulation results of rise time with different output power

Output power	$t_{r,sim}/\mu s$	$t_{r,cal}/\mu s$	Errors
1kW	26.428	26.471	0.16%
2kW	26.448	26.456	0.03%
4kW	24.448	24.497	0.2%

3-3-3 Influence of output power to decay time

As is discussed in section 2-5-2, the decay process is the combination of several stages of RC discharging process. The decay time is proportional to R_{Load} and therefore it is in inverse proportion to output power.

The calculation results of the decay time with different output power are shown in Table 3-17.

Table 3-17: Calculation results of decay time with different output power

Output power	1kW	2kW	4kW
Decay time/ms	10.456	5.228	2.614

Simulations are made in LTspice to verify the calculations. The simulation waveform is shown in Figure 3-9 and the simulation results are shown in Table 3-18.

The simulation results correspond with the theoretical analysis. From both the theoretical analysis and the simulation results, the decay time is in inverse proportion to output power. In order to obtain fast decay time, the voltage multiplier circuit should work under high power levels.

Discussions:

1. The voltage drop and voltage ripple are proportional to output power because the charge through capacitors are proportional to output power. The output power is controlled by the value of output load.

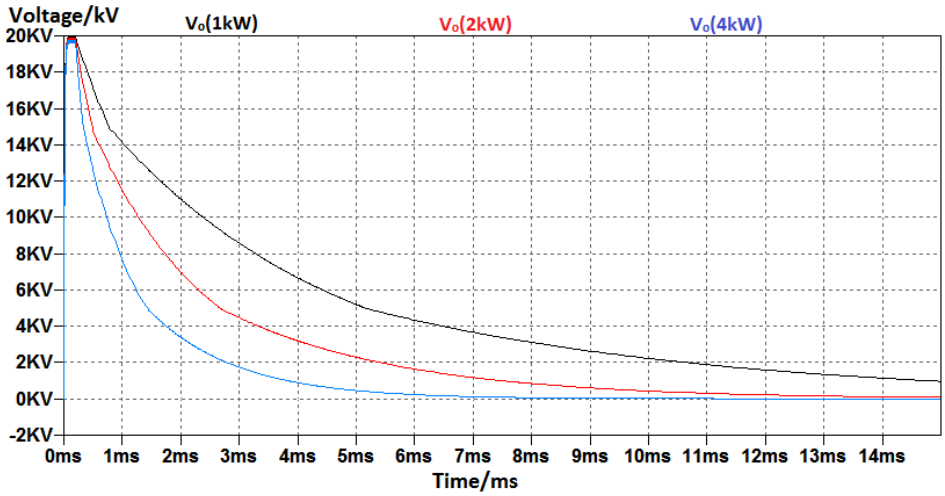

Figure 3-9: Simulation waveform of rise time with different output power

Table 3-18: Simulation results of rise time with different output power

Output power	$t_{f,sim}$/ms	$t_{f,cal}$/ms	Errors
1kW	10.468	10.456	0.11%
2kW	5.22	5.228	0.15%
4kW	2.616	2.614	0.08%

2.The rise time is not directly determined by output power. However, the output power will influence the voltage drop and voltage ripple and as a result the steady state value of output voltage is changed. Due to the changed output voltage, the number of switching cycles for the output voltage to rise from 10% to 90% of its steady state value will be influenced.The larger the output power is, the smaller the rise time is. The relationship between output power and rise time is nonlinear.

3.The decay process is the RC discharging process and the decay time is proportional to the output load. As a result, the decay time is in inverse proportion to output power. In order to achieve fast respond time, the power level of the voltage multiplier circuit should be as high as possible.

3-4 Optimal stage number

In this section, the optimal stage number for the HWCW voltage multiplier circuit in principle is derived. In principle, the voltage multiplier circuit is able to produce any output voltage as the stage number increases. However, it is not the truth if the voltage drop and voltage ripple are taken into consideration. When all the circuit parameters except for the stage number have been determined for the HWCW voltage multiplier circuit, there will be an optimal stage number N_{opt} which provides the largest output voltage. When the stage number increases than N_{opt}, the output voltage will start to decrease.

The output voltage value considering voltage drop and voltage ripple of a n-stage HWCW

voltage multiplier circuit is:

$$V_{out} = V_{o,noload} - \Delta V_o - \frac{1}{2}\delta V_o = 2nV_m - \frac{8n^3 + 9n^2 + n}{12}\frac{I_o}{fC} \tag{3-1}$$

Since I_o is a function of n as well I_o=$\frac{2nV_m}{R_L}$, equation (3-1) can be rewritten as:

$$V_{out} = 2nV_m - \frac{8n^3 + 9n^2 + n}{12}\frac{2nV_m}{fCR_L} \tag{3-2}$$

From Equation(3-2), if the stage number n is the only variable in the circuit, when n increases from zero, the output voltage increases as well at first. Due to the fast increase of the negative term n^4 and n^3 in the formula, the output voltage will reach a largest value at a optimal stage number N_{opt} and then start to decrease. Therefore, for a voltage multiplier circuit, if the stage number is the only variable quantity in the circuit, there is an optimal stage number N_{opt} existing.

N_{opt} can be calculated by differentiating V_{out} with respect to n and let the $V_{out}^{'}$ to be 0.

$$V_{out}^{'}(n) = 2V_m - \frac{32n^3 + 27n^2 + 2n}{6}\frac{V_m}{fCR_L} = 0 \tag{3-3}$$

By solving the equation(3-3), since the stage number is only possible to be a positive real number, the optimal stage number is obtained:

$$N_{opt} = -\frac{9}{32} + \sqrt[3]{-\frac{a}{2} + \sqrt{\frac{a^2}{4} + \frac{b^3}{27}}} + \sqrt[3]{-\frac{a}{2} - \sqrt{\frac{a^2}{4} + \frac{b^3}{27}}} \tag{3-4}$$

where a=$\frac{441}{16384}$-$\frac{3}{8}$fCR_L and b=-$\frac{179}{1024}$.

When all the parameters of the HWCW voltage multiplier circuit have been determined, the optimal stage number can be obtained with Equation (3-4). The HWCW voltage multiplier circuit provides the largest output voltage at N_{opt}. When the stage number increases larger than N_{opt}, the output voltage value starts to decrease.

3-5 Summary

In this chapter, the influence of circuit parameters including frequency, capacitance value, output power and stage number to electrical performances of the voltage multiplier circuit are discussed.

For voltage drop and voltage ripple, they are proportional to output power and in inverse proportion to frequency and capacitance value. The rise time of output voltage is in inverse proportion to frequency and it is not directly determined by capacitance value and output power. However, the capacitance value and output power will influence the steady-state output voltage value and as a result they will also influence the rise time in some cases. Moreover, when different capacitance values are used per stage, the rise time will be affected which will be discussed in Chapter 6. The rise time has nothing to do with the operating frequency but it is proportional to the values of capacitance and output load. At last, optimal stage number is given in section 3-4.

Chapter 4

Impact of parasitic components in the circuit

In chapter 2 and chapter 3, all the components in the multiplier circuit are asuumed to be ideal, which is not the truth in reality.

In this chapter, the influence of important parasitic components of the diodes, capacitors and transformer to the electrical performance of the voltage multiplier circuit are studied. The parasitic components include the junction capacitance of diodes(C_j), the equivalent series resistor(ESR), equivalent series inductance(ESL) and equivalent parallel capacitance(C_{pp}) of capacitors and the winding capacitance and leakage inductance of the transformer. The voltage multiplier circuit including the parasitic components is shown in Figure 4-1.

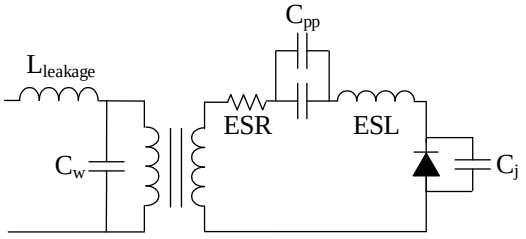

Figure 4-1: Parasitic components in voltage multiplier circuit

In section 4-1, the influence of junction capacitance of diodes is introduced. The effect of ESR,ESL and C_{pp} of capacitors are discussed in section 4-2. At last, the impact of parasitic components of the transformer are explained in section 4-3.

4-1 Junction capacitance of diodes

The effect of junction capacitance becomes significant when the operating frequency is high. The existence of junction capacitance will influence the voltage regulation of the multiplier

circuit. In this section, the influence of junction capacitance C_j of diodes to the voltage multiplier circuit is discussed. Operations in the negative switching cycles are explained as an example when D_1 and D_3 are forward biased while D_2 and D_4 are reverse biased. Operations in the positive switching cycles are the same.

The following assumption is valid:

The junction capacitances are much smaller than the capacitors and the multiplier circuit is working as normal. The voltage across capacitors are large enough to have constant values when no diodes are conducting in the circuit.

The waveform of V_{Cj1}, V_{Cj3}, I_{D1}, I_{D3} are shown in Figure 4-2.

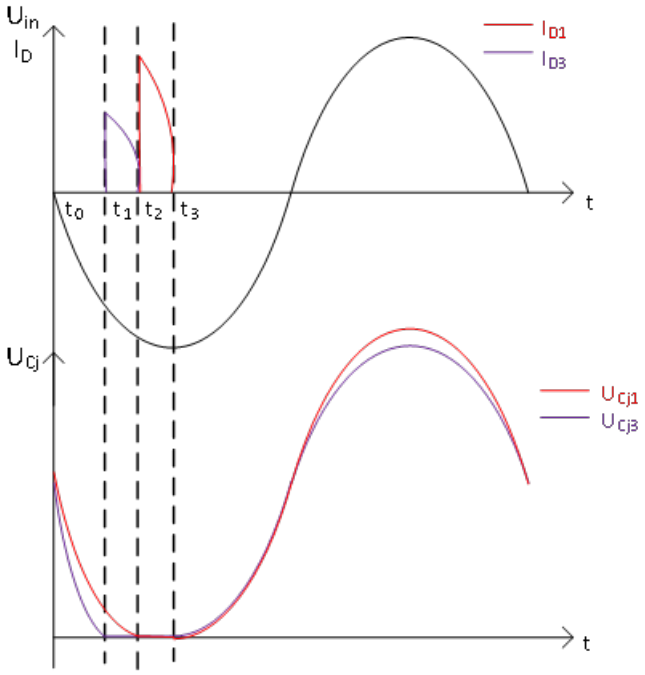

Figure 4-2: Waveform of voltage across junction capacitance

- t_0 to t_1
  From t_0 to t_1, the voltage source is decreasing in the negative switching cycle, D_2 and D_4 are blocked. Since $V_{C1}>V_{in}$ and $V_{C3}+V_{C1}>V_{in}+V_{C2}$, D_1 and D_3 are blocked as well. The equivalent circuit is shown in Figure 4-3(a).

  The relationship $V_{C1}+V_{in}=V_{Cj1}$ and $V_{C1}+V_{C3}+V_{in}=V_{C2}+V_{Cj3}$ can be obtained by using Kirchhoff's law. Since the voltage source is decreasing in the negative switching cycle, V_{Cj1} and V_{Cj3} are decreasing as well.

- t_1 to t_2
  At t_1, V_{in} is decreased to a certain value that $V_{C1}+V_{C3}+V_{in}=V_{C2}$ and D_3 starts to conduct. C_{j3} is shorted by D_3 and V_{Cj3} decreases to 0. The equivalent circuit is shown in Figure 4-3(b). V_{Cj1} continues to be discharged. V_{Cj4} increases to the maximum value.

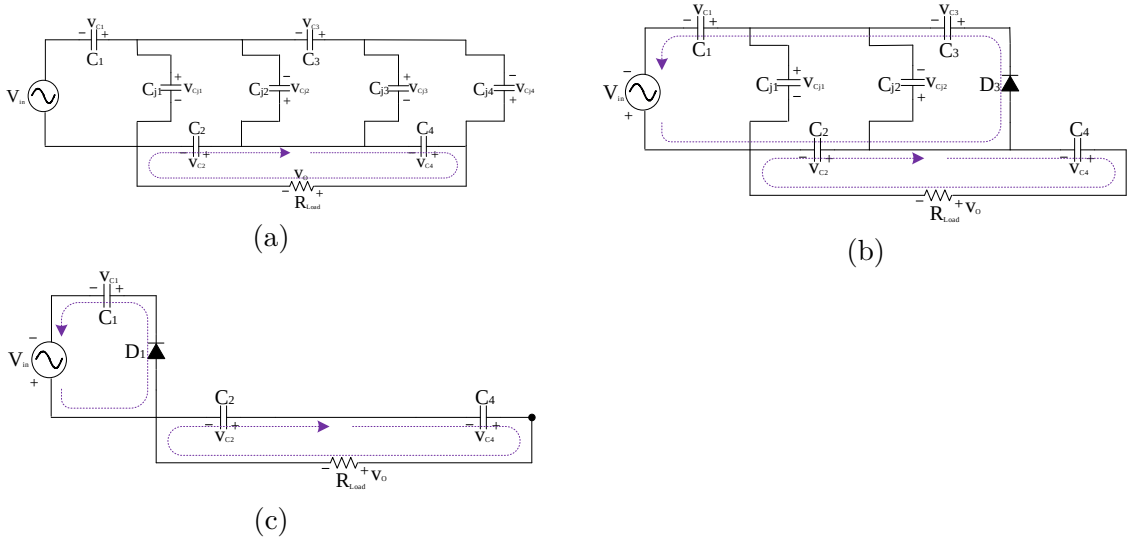

Figure 4-3: Equivalent circuits in steady state with junction capacitance

- t_2 to t_3
  At t_2, V_{C1}=V_{in}, D_3 is blocked and D_1 starts to conduct. C_{j1} is shorted by D_1 and V_{Cj1} decreases to 0. The equivalent circuit is shown in Figure 4-3(c). V_{Cj2} increases to its maximum value.

- After t_3
  After t_3, all the diodes are blocked again and the equivalent circuit is shown in Figure 4-3(a). Currents flow into the multiplier circuit and charge the junction capacitance. As a result, V_{Cj1} and V_{Cj3} increase from 0.

From the analysis above, the differences of the operations in steady state when junction capacitances are considered can be concluded:

In the conductive intervals of diodes, the junction capacitance are shorted by the conducting diode and they have no impact on the behaviors of the circuit. The operations during the conductive intervals are the same as what is discussed in section 2-2.

In the intervals when no diode is conducting in the circuit, due to the existence of junction capacitance, current provided by the voltage source flow into the multiplier circuit. As a result, the capacitors will be charged and discharged as well as the junction capacitance. Therefore, voltage across capacitor cannot keep constant anymore as is discussed in section 2-2 in non-conductive intervals of diodes.

The comparsion of waveform of V_{C1} and V_{C3} with or without junction capacitance is shown in Figure 4-4 where V_{C10} and V_{C30} represent waveform with ideal diodes while V_{C1j} and V_{C3j} represent waveform with junction capacitance.

From Figure 4-4, capacitors will be charged and discharged during the non-conductive intervals of diodes, which results in the increase in the voltage drop and voltage ripple. The charging and discharging rates are related with the value of junction capacitance. When the junction capacitance become larger, the voltage drop and voltage ripple will become larger as well.

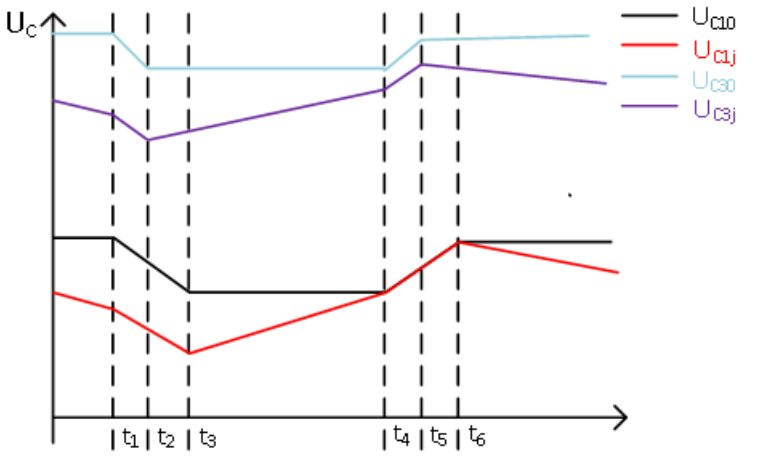

Figure 4-4: Waveform of capacitor voltage with junction capacitance

Simulations are made in LTspice with the existence of the junction capacitances of diodes to verify the theoretical analysis. The junction capacitances are set to be 0, 50pF and 200pF to have a comparison. The other circuit parameters keep unchanged.

The simulation waveform is shown in Figure 4-5.

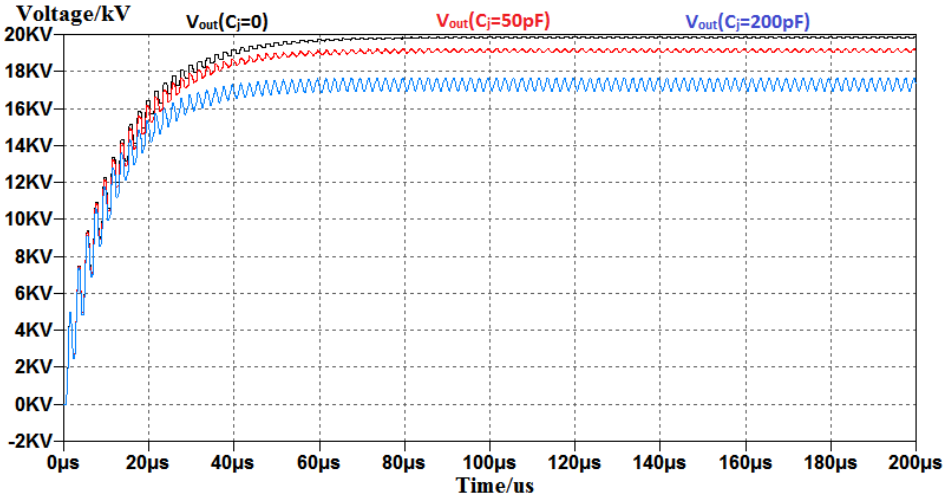

Figure 4-5: Simulation waveform with junction capacitance

The values of voltage drop and voltage ripple are shown in Table 4-1.

Due to the existence of junction capacitances, currents will flow into the mutliplier circuit during non-conductive intervals of diodes and capacitors are charged and discharged as a result. Therefore, the voltage ripple and voltage drop of capacitors are increased. When the values of junction capacitances are larger, the values of voltage drop and voltage ripple get larger as well. Diodes with low junction capacitance should be chosen to improve the voltage regualtion of the multiplier circuit.

Table 4-1: Voltage drop and voltage ripple with junction capacitance

C_j	Voltage drop/V	Voltage ripple/V
0	130.7	58.7
50pF	747.8	228.2
200pF	2339.3	705.9

4-2 Parasitic components of capacitors

The parasitic components of capacitors include equivalent series resistor(ESR), equivalent series inductance(ESL) and equivalent parallel capacitance(C_{pp}) as is shown in Figure 4-6.

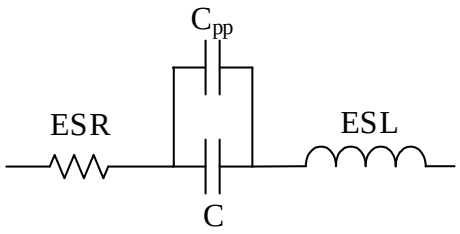

Figure 4-6: Parasitic components of capacitor

The studies are based on the actual capacitor that is used in the 2-stage voltage multiplier circuit, which is MLCC - SMD/SMT 4kV 2200pF 10% X7R from Syfer.

Based on the dissipation factor of the capacitor and the operating frequency, the ESR of each individual capacitor can be calculated:

$$ESR = tan\delta * \frac{1}{2\pi fC} = 0.025 * \frac{1}{2\pi * 500000 * 2200 * 10^{-12}} = 3.62\Omega$$

Therefore,the value of the parasitic components for each individual capacitor applied is shown in Table 4-2.

Table 4-2: Parasitic components for each individual capacitor

Capacitor Type	ESR	ESL	C_{pp}
MLCC - SMD/SMT 4kV 2200pF 10% X7R,Syfer	3.62Ω	3nH	1pF

In order to meet the requirements for the capacitance value as well as the voltage rating of each individual capacitors, 14 capacitors are connected in parallel as a group and three such groups are connected in series in each stage. Therefore, in each stage, 42 capacitors are used in total. The equivalent values of capacitance, ESR, ESL and C_{pp} per stage are shown in Table 4-3.

Table 4-3: Equivalent values of parasitic components of capacitors per stage

Capacitance	ESR	ESL	C_{pp}
10.267nF	0.775Ω	0.643nH	4.67pF

4-2-1 Equivalent Series Resistance

In this section, the influence of ESR is discussed. ESR is the electrical resistance in series with the capacitor plate and ESR is made up of the metal leads and plates and the connections between them.

There are three effects resulted from ESR in the steady state operations of the voltage multiplier circuit. The first one is that the current in the circuit is decreased due to the increased impedance Z=R-$\frac{j}{\omega C}$ compared with the ideal capacitor. The second effect is that when the voltage source has reached ± V_m, the diode will not stop conducting immediately because of the voltage across ESR V_{ESR}. The diode continues to conduct in the circuit before V_{ESR} is discharged to 0. The last effect is that ESR will bring additional voltage drop across capacitorsr. The additional voltage drop caused by ESR can be calculated by Δ (Δ V)=ESR*I_{av}[17].

The simulations are made by setting the value of ESR in the simulation model. The voltage drop caused by ESR is shown in Figure 4-7.

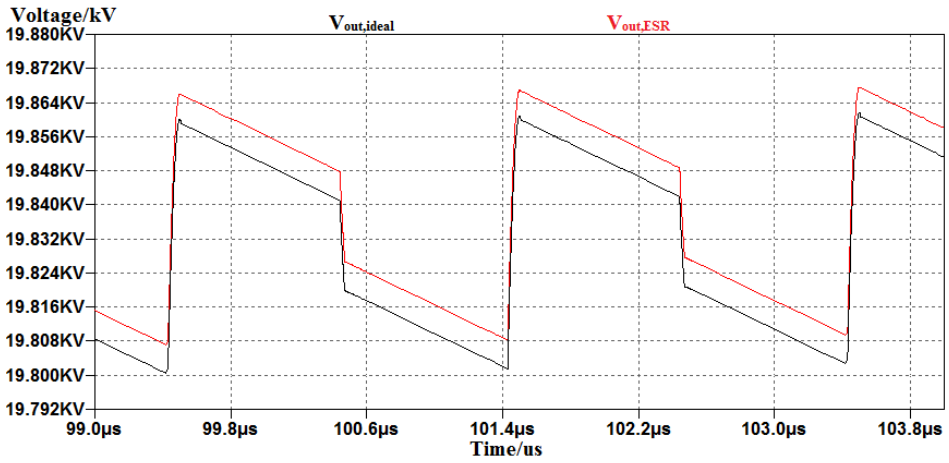

Figure 4-7: Simulation waveform with ESR

Due to fact that V_{ESR} will decrease to 0 rapidly when the voltage source reaches its maximum value in one switching cycle, phenomena called 'ESR jump' are present in capacitor voltage as is shown in Figure 4-8.

The existence of ESR has little to do with the voltage ripple. The voltage ripple is caused due to the existence of the output load. The output capacitors charge the output load and therefore the voltage ripple exists. Since the ESR of output capacitors are in series with R_{Load} in the output circuit, the output current is decreased. As a result, the voltage ripple of output capacitors decrease. However, since the value of ESR is so small compared with R_{Load}, the influence of ESR to voltage ripple is so small that can be neglected.

Discussions:

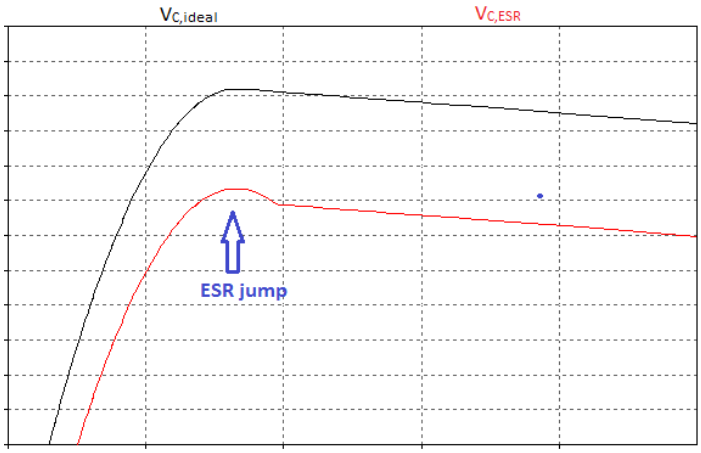

Figure 4-8: ESR jump

1.The existence of ESR increases the output voltage drop. The additional voltage drop of the k^{th} capacitor is related with ESR and I_C:

$$\Delta(\Delta V_{Ck}) = ESR_{Ck} * (\sum_{i=1}^{k} I_{Ci})$$

The additional output voltage drop is the summation of the additional voltage drop across all the output capacitors:

$$\Delta(\Delta V_o) = \sum_{i=1}^{k} \Delta(\Delta V_{2i})$$

2.The influence of ESR to voltage ripple is very slight compared with the voltage drop. The increase in voltage ripple can be ignored especially with a small ESR value.

3.The existence of ESR causes the phenomena of 'ESR jump' in capacitor voltage.

4.The existence of ESR causes extra power losses in the circuit which will be further discussed in chapter 5.

4-2-2 Equivalent Series Inductance

The equivalent series inductance(ESL) is another important parasitic component in a regular electrolytic capacitor. It represents the inductive property of the capacitor construction. The existence of ESL will influence the voltage drop, voltage ripple and circuit stability.

Taking ESL into consideration, the resonance occurs due to the combination of L and C. The resonance frequency is :

$$f = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{3 * 10^{-9} * 2.2 * 10^{-9}}} = 62MHz$$

The capacitor behaves like an inductor when the operating frequency is over the resonance frequency 62MHz, which means that the voltage multiplier must be operated at the frequency under the resonance frequency. For the selection of capacitors, the ESL must be considered.

Assume the rectifiers are ideal and ESL is not considered, the total reactance per stage is provided only by the capacitor:

$$X = X_C = -\frac{j}{2\pi fC}$$

If the parasitic series inductance of capacitor is taken into consideration, the reactance per stage is decreases:

$$X = X_C + X_L = -\frac{j}{2\pi fC} + j2\pi fL = j(-\frac{1}{2\pi fC} + 2\pi fL)$$

The current value in the voltage multiplier circuit is increased. Voltage across capacitors are calculated by $U_C = \frac{1}{C}\int Idt$, therefore the increase in the current will result in the increase in capacitor voltage. The voltage drop is smaller and the deduction of the voltage drop is related with the ESL value. ESL has little to do with voltage ripple as well.

Simulations are made in LTspice. The simulation waveform of output voltage with and without ESL in steady state are shown in Figure 4-9.

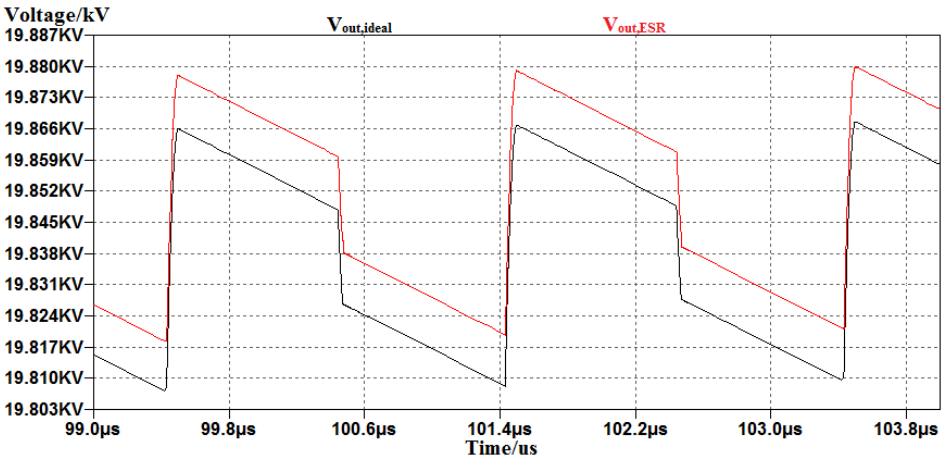

Figure 4-9: Simulation waveform with ESL

The simulation results of voltage drop and voltage ripple are shown in Table 4-4.

Table 4-4: Simulation results with ESL

	Voltage drop/V	Voltage ripple/V
Ideal capacitors	130.7	58.7
Capacitors with ESL	114.9	58.7

The simulation results correspond with the theoretical analysis. The ESL will decrease the value of voltage drop and has little to do with voltage ripple.

There are some other interesting phenomena to be paid attention to with the existence of ESL:

1.The existence of ESL results in LC oscillation as is shown in Figure 4-10.

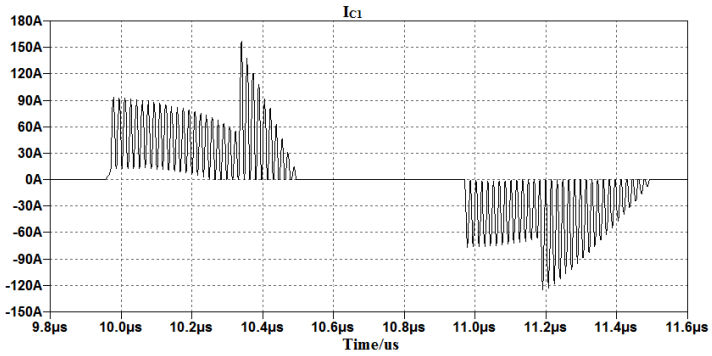

Figure 4-10: LC oscillation due to ESL

The frequency of LC oscillation is the resonance frequency 62MHz calculated above, which means each individual oscillation takes around 15.9ns. In the simulation results, during 0.342us, 21 LC oscillations take place in total. Therefore, each individual LC oscillation take 16.2ns, which is correspond with the calculated value of 15.9ns.

The LC oscillation will also influence the stability of the voltage multiplier circuit.

2.When the diodes are conducting in the circuit, current will flow through ESL and there will be voltage across ESL u(t)=L$\frac{di}{dt}$. The voltage induced across ESL is not large, but it will cause voltage spikes in capacitor voltage as is shown in Figure 4-11.

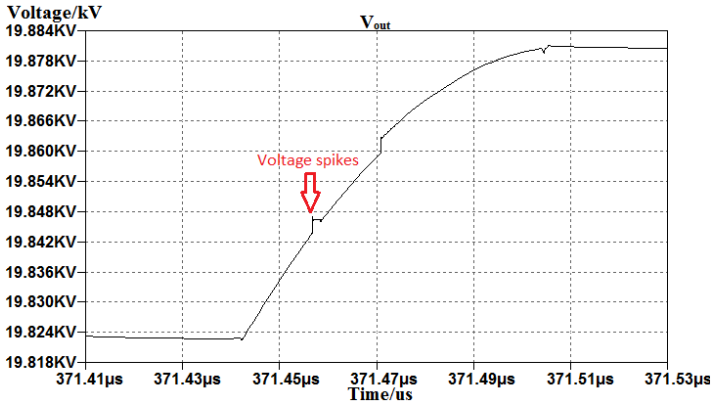

Figure 4-11: Voltage spikes due to ESL

Discussions:

1.The existence of ESL will decrease the voltage drop and has little to do with voltage ripple. ESL are in series with capacitor and will decrease the reactance per stage, which results in larger current and therefore larger voltage across capacitors.

2.The combination of ESL and capacitor will cause LC oscillations in the multiplier circuit which may influence the stability of the circuit. The oscillation frequency is related with the values of ESL and capacitor.

3.The voltage across ESL will cause the phenomena of voltage spikes in capacitor voltage. However, due to the relatively low values of ESL and $\frac{di}{dt}$, the influence of voltage spikes are not important.

4-2-3 Equivalent parallel capacitance

Besides ESR and ESL, there is another kind of parasitic component for the capacitor which is not discussed commonly - parasitic parallel capacitance (C_{pp}). The parasitic parallel capacitance represents the structural capacitance between the capacitance and the ground.

The existence of parasitic parallel capacitance will influence the equivalent value of the capacitance in each stage. Due to the change of the capacitor value, voltage drop and voltage ripple will also be impacted by C_{pp}. The value of the real C_{pp} is often very small compared with the real capacitor value, in order to study the influence of C_{pp}, the value of C_{pp} is assumed to be 0.5nF per stage in this section. Therefore, the equivalent capacitor value considering C_{pp} is 10.767nF.

According to equation (2-12) and (2-16), the existence of Cpp will decrease voltage drop and voltage ripple in the multiplier circuit. The calculation result are shown in Table 4-5.

Table 4-5: Calculation results of voltage regulation with C_{pp}

	Voltage drop/V	Voltage ripple/V
Ideal capacitors	136.36	58.44
Capacitors with C_{pp}	130.3	55.73

Therefore, the values of voltage drop and voltage ripple considering Cpp is 95.4% of the values when ideal capacitors are used.

Simulations are made in LTspice. The simulation waveform of output voltage with and without C_{pp} in steady state are shown in Figure 4-12.

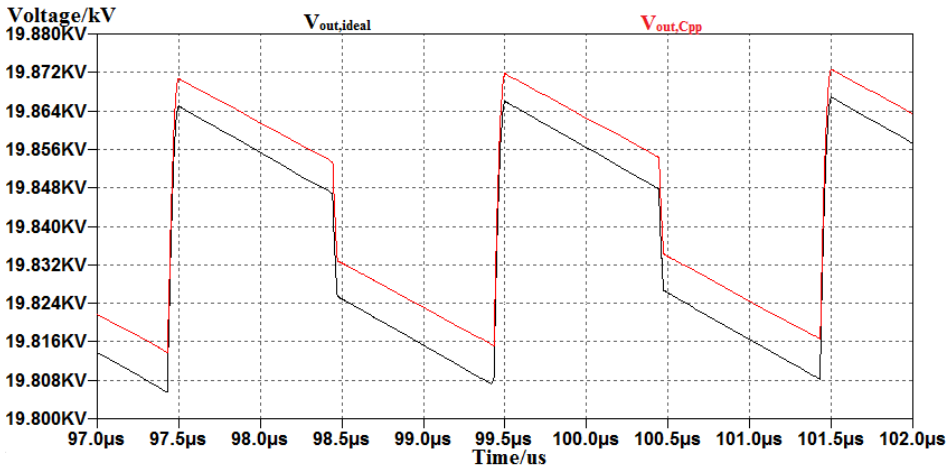

Figure 4-12: Simulation waveform of output voltage with C_{pp}

The simulation results are shown in Table 4-6.

The ratio between the simulated value is :

$$\frac{\Delta V_{o,Cpp}}{\Delta V_{o,ideal}} = \frac{122.48}{128.17} = 95.5\%$$

Table 4-6: Simulation results of voltage regulation with C_{pp}

	Voltage drop/V	Voltage ripple/V
Ideal capacitors	128.17	56.66
Capacitors with C_{pp}	122.48	54.04

$$\frac{\delta V_{o,Cpp}}{\delta V_{o,ideal}} = \frac{54.04}{56.66} = 95.4\%$$

The simulation results correspond with the theoretical analysis. The existence of C_{pp} decreases the values of voltage drop and voltage ripple.

4-3 Parasitic components of transformer

4-3-1 Influence of parasitic components to the transformer

In the high frequency high voltage power supply circuit, the output of the transformer is the input of the voltage multiplier circuit. Therefore, the parasitic components of the transformer will influence the behavior of the voltage multiplier circuit as well. The equivalent circuit of parasitic components of the transformer is shown in Figure 4-13[18].

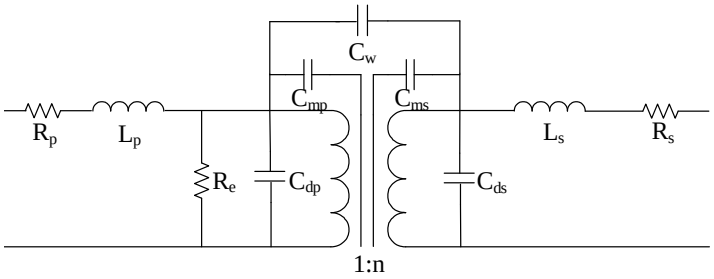

Figure 4-13: Parasitic components of transformer

In the equivalent circuit, L_p and L_s represent the leakage inductance at primary side and secondary side of the transformer respectively. R_p and R_{s2} represent the dc winding resistance for the primary and secondary windings while R_e is the equivalent core-loss shunt resistance. C_{dp} and C_{ds} are the winding capacitance at the primary and secondary side, C_{mp} and C_{ms} represent the distributed capacitance between the core and windings. C_w is the distributed capacitance between primary winding and secondary winding.

The parasitic components of the transformer especially the leakage inductance and winding capacitance have great influence on the performance of the voltage multiplier circuit that can not be ignored. The existence of leakage inductance may cause the delay of the conduction of input current and the stored energy in the leakage inductance will cause voltage spikes. The existence of winding capacitance will result in the current spikes. Leakage inductance and winding capacitance will also lead to oscillation in the circuit. The input voltage at the voltage multiplier side will be smaller than estimated and the voltage regulation of the multiplier circuit will be affected as a result.

The definition of the coupling coefficient of a transformer is K=$\frac{M}{\sqrt{L_1 L_2}}$, where L_1,L_2 represent primary winding inductance and secondary winding inductance respectively, M is the mutual inductance between the primary and secondary windings. For ideal transformers, the value of coupling coefficient equals to 1, which means perfect coupling between the primary and secondary winding that no leakage inductance exists. However, in reality , due to the physical distance between primary and secondary windings, part of the windings behave like an inductor in series with the transformer and therefore the coupling coefficient is smaller than 1. The coupling coefficient can also be realized in LTspice by changing the K-statement for transformer.

There are three main effects caused by the parasitic components to the transformer circuit.

The first effect is the delay of conduction of current and voltage as is shown in Figure 4-14. The current and voltage at the primary side of the tranformer are I_p and U_p respectively. The current and voltage at the secondary side of the tranformer are I_s and U_s respectively, which are also the input of the voltage multiplier circuit.

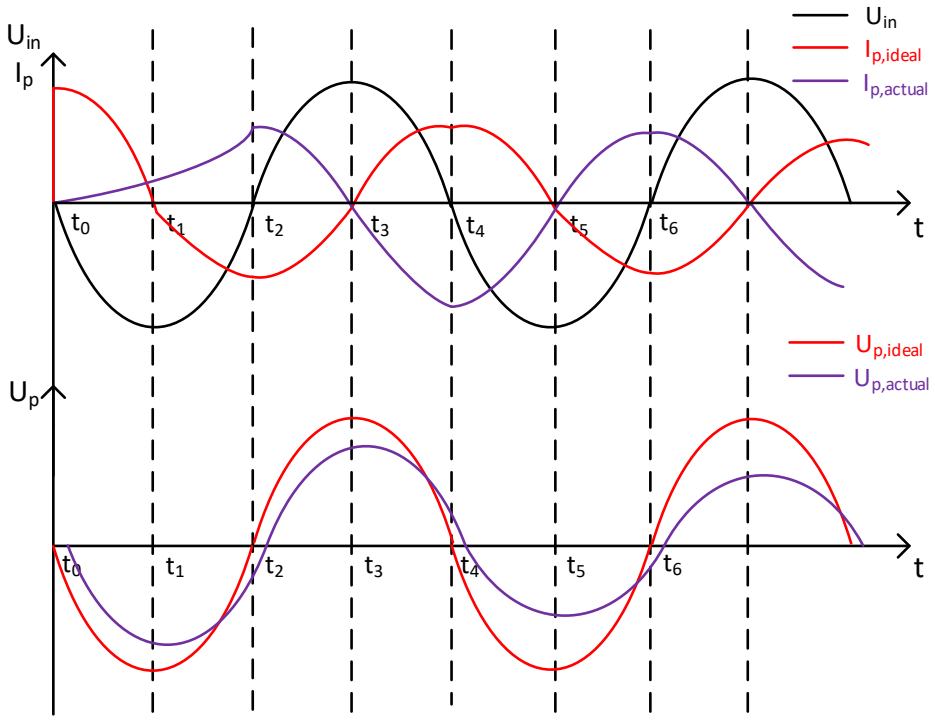

Figure 4-14: Waveform at primary side of the transformer

In the voltage multiplier circuit with the ideal transformer,I_p increases rapidly at beginning and U_p is in phase with the input voltage for the transformer. When the parasitic components of the transformer are considered,the conduction of I_p is delayed due to the effect of leakage inductance as is shown in Figure 4-14. The currents flow through the leakage inductance and establish a magnetic field. When the currents change, the flux change and the changing flux induce EMF. The induced EMF causes a current that opposes I_p. Therefore, the built-up of I_p is slower than the ideal transformer circuit and no current spikes occur at the beginning. As a result, the built up of U_p lags the input voltage source when parasitic components of the transformer are considered.

The second effect is that the errors of the voltage turn ratio from primary side to secondary side occur because of the winding resisitances, leakage flux and displacement currents, which are presented by leakage inductance and winding capacitance[19]. The comparison of waveform for U_s is shown in Figure 4-15.

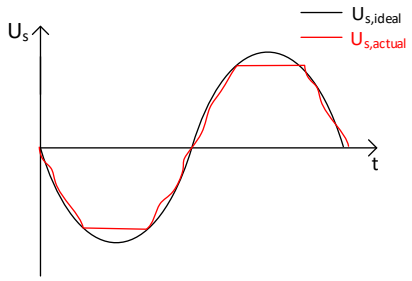

Figure 4-15: Comparsion of waveform for U_s

The third effect is that the leakage inductance and distribution capacitance will lead to LC oscillation in the circuit as well, which may result in the electromagnetic interference.

4-3-2 Influence to the electrical performance of multiplier circuit

As is discussed in section 2-1, D_4 starts to conduct when V_{in} increases to the value that fulfills the condition $V_{C1}+V_{C3}+V_{in} = V_{C2}+V_{C4}$. Due to the fact that the maximum value of V_{in} is decreased as is shown in Figure 4-15, it can be inferred that the boost of voltages across capacitors will end earlier in start-up process with actual transformer models than with the ideal models. Therefore, the steady state is reached earlier.

Based on the fact that the start-up process is forced to end earlier, it can be inferred that the voltage drop of the multiplier circuit is increased while the voltage ripple is decreased. However, it is difficult to calculate the voltage drop and voltage ripple caused by parasitic components of the transformer theoretically.

Simulations are made in LTspice to verify the theoretical analysis. The leakage inductance is set as μH, the winding capacitance is set as 3nF and the coupling coefficient is set as 0.98. The simulation waveform of output voltage with and without parasitic components of the transformer are shown in Figure 4-16.

The voltage drop and voltage ripple are shown in Table 4-7.

Table 4-7: Simulation results of voltage regulation with actual transformer

	Voltage drop	Voltage ripple
Ideal transformer	120.9V	55.7V
Actual transformer	1.902kV	45.2V

Due to the sudden stop of the start-up process caused by the decreased input voltage, the steady state is reached earlier and therefore the rise time will be shorter than the ideal case. The decay process has little to do with the parasitic components of the transformer. The

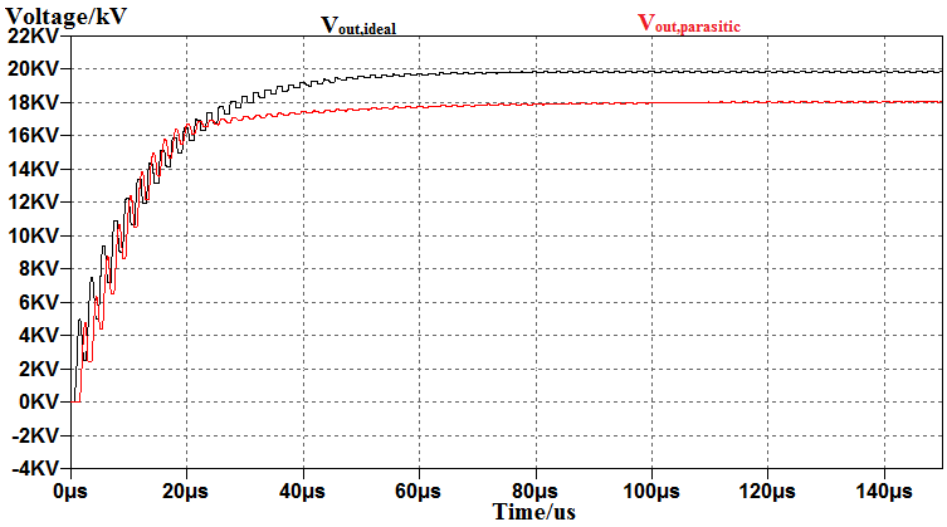

Figure 4-16: Simulation waveform of output voltage with actual transformer

reduced steady state output voltage value may decrease the decay time but the influence is not obvious.

The simulation waveform of rise time and decay time with and without parasitic components of the transformer are shown in Figure 4-16 and Figure 4-17 respectively.

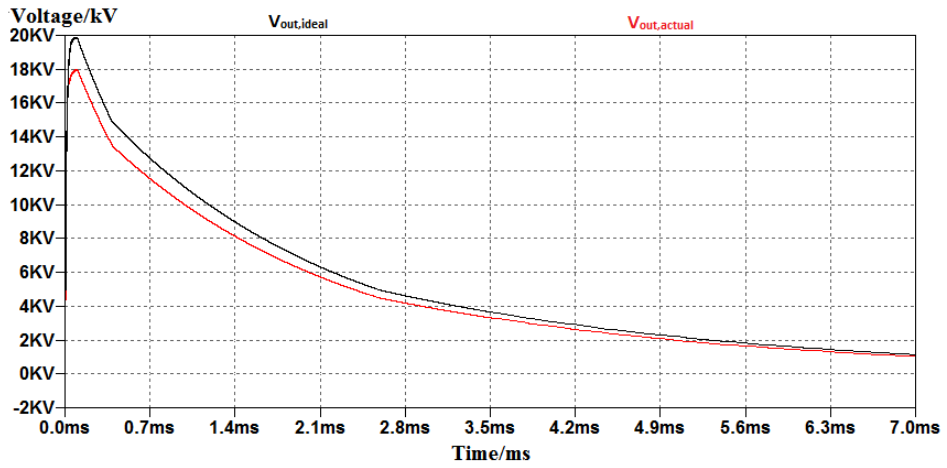

Figure 4-17: Simulation waveform of decay process with actual transformer

The simulation results of rise time and decay time are shown in Table 4-8.

The simulation results correpsond with theoretical analysis. The parasitic components of transformer will decrease the value of input voltage for the multiplier circuit. As a result, the voltage drop is increased and the voltage ripple is decreased. The rise time is decreased as well. The parasitic components of transformer has little to do with the decay time.

Table 4-8: Simulation results for respond time with actual transformer

	Rise time	Decay time
Ideal transformer	26.37μs	5.23ms
Actual transformer	16.06μs	5.22ms

4-4 Summary

In this chapter, the impact of important parasitic components of diodes, capacitors and transformer are considered.

The junction capacitance of diodes will increase voltage drop and voltage ripple as is analyzed in section 4-1. The influence of ESR, ESL and C_{pp} of capacitors are discussed in section 4-2. The existence of ESR will increase voltage drop and cause 'ESR jump'. The existence of ESL will decrease voltage drop and cause LC oscillations and voltage spikes in the circuit. The existence of C_{pp} will increase the equivalent capacitance value per stage and decrease voltage drop and voltage ripple. The parasitics of the transformer will force the start-up process to end earlier than expected. As a result, the voltage drop is increased, the voltage ripple is decreased and the rise time is decreased as well.

In the next chapter, power losses in the multiplier circuit are discussed, which is another important criteria to evaluate the voltage multiplier circuit.

Chapter 5

Power Loss Analysis of the Multiplier Circuit

Besides the electrical performance of the voltage multiplier circuit, the power loss analysis is also significant in order to reduce heating and prolong the service life of the power supply circuit. Therefore, the power losses in the multiplier circuit are discussed in this chapter.

The power losses mainly come from the conduction loss and reverse recovery loss of diodes and ESR of capacitors. In section 5-1, detailed switching process of diodes is analyzed. The formulas to calculate the currents in the multiplier circuit are derived in section 5-2. The power losses caused by diodes and capacitors are calculated respectively in section 5-3 and 5-4.

5-1 Detailed switching process of diodes in HWCW voltage multiplier

In the real voltage multiplier circuit, reverse recovery will take place during the switching process of diodes, which results in the diode switching losses and therefore cannot be neglected. In this section, the reverse recovery problems are taken into consideration and the detailed analysis of the switching process of diodes in the HWCW voltage multiplier circuit are discussed.

The waveform of current through ideal diodes without reverse recovery in steady state is shown in Figure 2-6. The waveform of the diode currents in steady state taking reverse recovery problems into consideration are shown in Figure 5-1. The operations in the positive switching cycles of the input voltage source when even diodes are conducting in the circuit are explained as an example. The operations of the odd diodes in the negative switching cycles are the same. The reverse recovery procedure of diodes in the first stage and diodes in the other stages are very different[20].

1. Reverse recovery of diodes in the first stage:

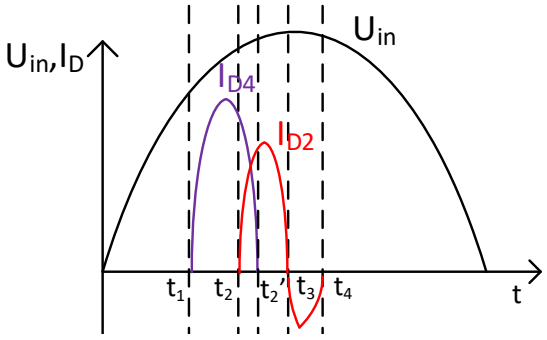

Figure 5-1: Reverse recovery of diodes in steady state

- t_2 to t_3
  From t_2 to t_3, the operations are the same as is discussed in section 2-2-1. D_2 starts to conduct at t_2. I_{D2} decreases to 0 at t_3 when U_{in} increases to V_m.

- t_3 to t_4
  From t_3 to t_4, the reverse recovery procudure of D_2 occurs. The equivalent circuit is shown in Figure 5-2(a). In order to eliminate the minor carrier stored in D_2, the reverse recovery procedure of D_2 begins. I_{D2} will turn negative and increase to the maximum reverse recovery current I_{D2rrm} at first. Then I_{D2} will decrease to 0 at t_4. The voltage across D_2 is zero since V_{D2}=$V_{C1ss,min}$+V_m-$V_{C2ss,max}$. Therefore, the zero voltage switching(ZVS) is realized.

2. Reverse recovery of diodes in the other stages

- t_1 to $t_2^{'}$
  From t_1 to $t_2^{'}$, the operations are the same as is discussed in section 2-2-1. I_{D4} decreases to zero and V_{C4}=V_{C3} at t_2.

- $t_2^{'}$ to t_3
  From $t_2^{'}$ to t_3, D_2 is conducting in the circuit. The equivalent circuit is shown in Figure 5-2(b), V_{D4} equals to the forward voltage drop of D_2 as V_{C4} and V_{C3} stop to change. Therefore, D_4 is not blocked and I_{D4}=0.

  After t_3, D_4 is blocked. Since I_{D4} has been zero, zero current switch is realized and no reverse recovery takes place.

Therefore, the reverse recovery process only occurs in the diodes in the first stage(D_2 and D_2). However, even though the reverse recovery occurs, the reverse recovery loss is zero due to the zero voltage switching. Diodes in other stages have no reverse recovery losses.

The simulation are made in LTspice with the actual model of power rectifier Byg23m. The simulation waveform is shown in Figure 5-3.

Discussions:

In the simulation waveform shown in Figure 5-3, D_4 still shows reverse recovery process. This is because of the commutation of diode currents as is shown in the time interval from t_2

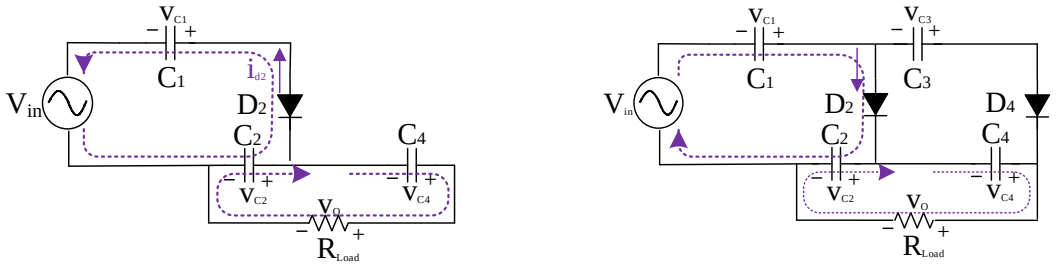

Figure 5-2: Equivalent circuits of reverse recovery procedures

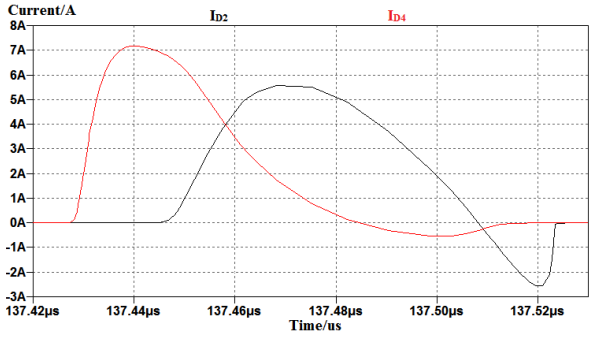

Figure 5-3: Simulation results of actual diode models

to $t_2^{'}$ in Figure 5-1. In the theoretical analysis, the commutations of diode currents are not taken into consideration , V_{C3} and V_{C4} are assumed to keep constant after they have reached the same value. When the actual diode models are applied, D_2 starts to conduct before I_{D4} decreases to 0. As a result, V_{C3} continues to decrease and V_{C4} continues to increase until $t_2^{'}$ after they have reached the same value. Therefore, V_{C4}>V_{C3} when I_{D4} decreases to 0. As a result, negative voltage is applied across D_4 and I_{D4} turns to a small negative value. The reverse recovery of D_4 can be ignored compared with that of D_2.

5-2 Derivations of diode currents

In order for further research on power losses, the method to calculate currents in the HWCW voltage multiplier circuit is derived in this section.

From the analysis above, diodes with odd numbers and diodes with even numbers conduct in different half switching cycles of the input voltage source. Moreover, diodes with higher stage numbers conduct at first and diodes with lower stage numbers conduct at last. When the k^{th} diode is conducting in the circuit, all the capacitors with number$leqslant$k are charging or discharging in the multiplier circuit. Therefore, the total charging and discharging time of diodes in low stages are longer than diodes in high stages. From the equation of the voltage ripple of each capacitor shown in equation (2-9) , it can be obtained the difference of the voltage ripple of two adjacent odd/even capacitors is $\frac{I_o}{fC}$ assuming the capacitance distribution is equal in each stage.

The voltage drop across capacitors are:

$$\Delta V_{2k-1} = (2n-k+2)(k-1) * \frac{I_o}{fC} \tag{5-1}$$

$$\Delta V_{2k} = [(2n-1)(n+1) - k^2] * \frac{I_o}{fC} \tag{5-2}$$

The input voltage source of the multiplier circuit is Asin2πft, where A is the maximum input voltage value V_m.

- Derivation of I_{D1}
  When D_1 is conducting in the circuit, I_{D1}=I_s=I_{C1}.

  The maximum value of V_{C1} in steady state is A. According to the regulations concluded in section 2-1-2, the equation can be obtained:

$$Asin2\pi ft = A - (\delta V_{C1} - \delta V_{C3}) = A - \frac{I_o}{fC} \tag{5-3}$$

$$t = \frac{arcsin(1 - \frac{I_o}{AfC})}{2\pi f} \tag{5-4}$$

  Equation (5-4) is the time point when D_1 starts to conduct. The conduction of D_1 stops at the time point when V_{in} reaches -V_m. Therefore, the conducting time for D_1 is:

$$t_{D1} = \frac{1}{4f} - \frac{arcsin(1 - \frac{I_o}{AfC})}{2\pi f} \tag{5-5}$$

  This is also the charging time of C_1 during the conduction of D_1. Therefore, I_{D1} can be calculated:

$$I_{D1} = I_{C1} = C_1 \frac{dV}{dt} = C_1 \frac{\frac{I_o}{fC}}{t_{D1}} = \frac{I_o}{ft_{D1}} = \frac{I_o}{\frac{1}{4} - \frac{arcsin(1-\frac{I_o}{AfC})}{2\pi}} \tag{5-6}$$

  This is the average value of I_{D1} during t_{D1}, the average value and rms value in one switching period can be calculated based on I_{D1}, t_{D1} and frequency.

- Derivation of I_{D2k-1}
  D_{2k-1} starts to conduct at the time point when the voltage source reaches the value at which fulfills the condition:

$$V_{in} + \sum_{i=1}^{k-1} V_{C2i} = \sum_{i=1}^{k} V_{C2i-1} \tag{5-7}$$

  The equation can be rewritten:

$$V_{in} = \sum_{i=1}^{k} V_{C2i-1} - \sum_{i=1}^{k-1} V_{C2i} = V_{C2k-1} + \sum_{i=1}^{k-1} (V_{C2i-1} - V_{C2i}) \tag{5-8}$$

$$V_{in} = V_{C2k-1} + V_{C1} - V_{C2} + \sum_{i=2}^{k-1}(V_{C2i-1} - V_{C2i}) \tag{5-9}$$

The difference of the odd and even number capacitor in the ith stage (i<k) is:$\frac{2i*I_o}{fC}$

At the time point when D_{2k-1} starts to conduct, the value of V_{C1},V_{C2} and V_{C2k-1} are:

$$V_{C1} = A - \frac{kI_o}{fC} \tag{5-10}$$

$$V_{C2} = 2A - \Delta V_{C2} - \frac{(n-k)I_o}{fC} = 2A - \frac{(2n-k)I_o}{fC} \tag{5-11}$$

$$V_{C2k-1} = 2A - \Delta V_{C2k-1} - \frac{I_o}{fC} = 2A - (2n-k+2)(k-1) * \frac{I_o}{fC} - \frac{I_o}{fC} \tag{5-12}$$

Therefore, the equation can be obtained:

$$Asin2\pi ft = A - (2nk - 4n - 2k^2 + 8k - 3)\frac{I_o}{fC} \tag{5-13}$$

Let the corfficient to be α_{2k-1}=2nk-4n-2k^2+8k-3

$$t = \frac{arcsin(1 - \frac{\alpha_{2k-1}I_o}{fCA})}{2\pi f} \tag{5-14}$$

This is the time from the time point at which D_{2k-1} starts to conduct to the time point when V_{in} reaches -V_m. The conduction of D_{2k-1} stops at the time point when V_{C2k-1} reaches its maximum value in steady state. Then, odd diode in one stage lower starts to conduct. Therefore, the conducting time of D_{2k-1} should be:

$$t_{D2k-1} = \frac{1}{4f} - \frac{arcsin(1 - \frac{\alpha_{2k-1}I_o}{fCA})}{2\pi f} - \sum_{i=1}^{k-1} t_{D2k-1} \tag{5-15}$$

The current during the conduction of D_{2k-1} is:

$$I_{D2k-1} = I_{C2k-1} = C_{2k-1}\frac{dV}{dt} = C\frac{\frac{I_o}{fC}}{t_{D2k-1}} = \frac{I_o}{ft_{D2k-1}}$$

$$= \frac{I_o}{f * (\frac{1}{4f} - \frac{arcsin(1-\frac{\alpha_{2k-1}I_o}{fCA})}{2\pi f} - \sum_{i=1}^{k-1} t_{D2k-1})} \tag{5-16}$$

This is the average value of I_{D2k-1} during the conduction of D_{2k-1}, the average value and rms value of I_{D2k-1} in one switching period can be calculated based on I_{D2k-1}, t_{D2k-1} and frequency.

In order to calculate the diode currents in the circuit, the calculation should start from rectifiers in the lower stages at first.

- Derivation of I_{D2k}
  D_{2k} starts to conduct at the time point when the voltage source reaches the value at which fulfills the condition:

$$V_{in} + \sum_{i=1}^{k} V_{C2i-1} = \sum_{i=1}^{k} V_{C2i} \tag{5-17}$$

The equation can be rewritten:

$$V_{in} = \sum_{i=1}^{k} V_{C2i} - \sum_{i=1}^{k} V_{C2i-1} = V_{C2} - V_{C1} + \sum_{i=2}^{k} (V_{C2i} - V_{C2i-1}) \tag{5-18}$$

At the time point when D_{2k} starts to conduct, the value of V_{C1},V_{C2} are:

$$V_{C1} = A - \frac{(n-k)I_o}{fC} \tag{5-19}$$

$$V_{C2} = 2A - \Delta V_{C2} - \frac{kI_o}{fC} = 2A - \frac{(n+k)I_o}{fC} \tag{5-20}$$

In the same stage, $V_{C2i-1} > V_{C2i}$

$$\sum_{i=2}^{k} (V_{C2i} - V_{C2i-1}) = \sum_{i=1}^{k-1} 2i \frac{I_o}{fC} = -\frac{k(k-1)I_o}{fC} \tag{5-21}$$

Therefore, the equation can be obtained:

$$Asin2\pi ft = A - \frac{k(k+1)I_o}{fC} \tag{5-22}$$

$$t = \frac{arcsin(1 - \frac{k(k+1)I_o}{fCA})}{2\pi f} \tag{5-23}$$

This is the time from the time point at which D_{2k} starts to conduct to the time point when V_{in} reaches V_m. The conduction of D_{2k} stops at the time point when V_{C2k} reaches its maximum value in steady state. Then, even diode in one stage lower starts to conduct. Therefore, the conducting time of D_{2k} should be:

$$t_{D2k} = \frac{1}{4f} - \frac{arcsin(1 - \frac{k(k+1)I_o}{fCA})}{2\pi f} - \sum_{i=1}^{k-1} t_{D2k} \tag{5-24}$$

The current during the conduction of D_{2k-1} is:

$$I_{D2k} = I_{C2k} = C_{2k} \frac{dV}{dt} = C \frac{\frac{I_o}{fC}}{t_{D2k}} = \frac{I_o}{f t_{D2k}}$$

$$= \frac{I_o}{f * (\frac{1}{4f} - \frac{arcsin(1 - \frac{k(k+1)I_o}{fCA})}{2\pi f} - \sum_{i=1}^{k-1} t_{D2k})} \tag{5-25}$$

This is the average value of I_{D2k} during the conduction of D_{2k}, the average value and rms value of I_{D2k} in one switching period can be calculated based on I_{D2k}, t_{D2k} and frequency.

In order to calculate the diode currents in the circuit, the calculation should start from rectifiers in the lower stages at first.

Using the equation (5-6),(5-16) and (5-25), the diode currents can be calculated. In case of ideal diode models, the model shown in Figure 5-4 can be used when calculating the RMS value of currents taking I_{D1} and I_{D3} as an example. The commutations between the currents and the rise time of currents are ignored.

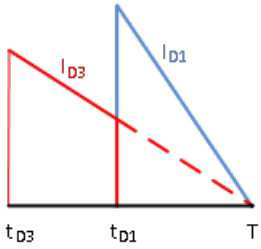

Figure 5-4: RMS calculation model

In the RMS current model, t_{D3} and t_{D1} represent the time when D_3 and D_1 start to conduct in the circuit in steady state, T is the time when the voltage source reaches -Vm.

The calculation results of t_D and I_D are shown in Table 5-1.

Table 5-1: Calculation results of t_D and I_D

	D_1	D_2	D_3	D_4
$t_D/\mu s$	0.028	0.04	0.035	0.03
I_D/A	7.022	4.964	5.667	6.759

The calculation values of average and RMS values of currents are shown in Table 5-2.

Table 5-2: Calculation results of avetage and rms values of diode currents

	D_1	D_2	D_3	D_4
$I_{D,av}$/mA	98.3	99.28	95.39	101.38
$I_{D,rms}$/mA	968.23	815.8	745.24	838.7

Simulations are made in LTspice to verify the calculations. The comparison of the calculation and simulation results of diode currents are shown in Table 5-3.

From the comparison between the simulation and calculation results of diode currents shown in Table 5-3, the calculation results of I_{D1} and the even diodes correspond with the simulation results. However, the calculation of I_{D3} has errors of around 10%. This is because of the influence of the output loop that even capacitors are always charging the output load in the whole switching cycle. As a result, when the odd diodes start to conduct, the voltage

Table 5-3: Comparison of simulation and calculation results of diode currents

	$I_{D,av,sim}$/mA	$I_{D,av,cal}$/mA	Errors	$I_{D,rms,sim}$/mA	$I_{D,rms,cal}$/mA	Errors
D_1	99.08	98.3	0.8%	951.5	968.23	1.76%
D_2	99.3	99.28	0.02%	804.37	815.8	1.42%
D_3	101.54	95.39	6.01%	845.69	745.24	11.88%
D_4	101.9	101.38	0.51%	826.52	838.7	1.47%

across even capacitors will be smaller than the maximum steady state value and the voltage across odd capacitors will be larger than the minimum steady state value. Therefore, some optimizations can be applied to improve the accuracy of the calculation of odd diode currents by considering the effect of the output loop.

The output loop is the RC discharging circuit. The time constant is $\tau=\frac{CR_L}{n}=1000\mu$s. Due to the conduction time of diodes is much smaller than the switching cycle $t_D \ll T$, the voltage drop of C_2 between the end of conduction of even diodes and beginning of conduction of odd diodes can be seen as the voltage drop of C_2 in half of a switching cycle.

$$\Delta V_{C3} = (1 - exp(-\frac{t}{\tau})V_{ss}) = (1 - exp(-0.001)) * 9960 = 9.955V$$

$$Asin2\pi ft + 2A - \frac{2I_o}{fC} - 9.955 = A - \frac{2I_o}{fC} + 2A - \frac{4I_o}{fC} - \frac{kI_o}{fC} + 9.955$$

$$Asin2\pi ft = A - \frac{5I_o}{fC} + 19.91$$

As a result, $t_{D3}=0.029\mu$s,$I_{D3}=6.897$A and $I_{D3,av}=100$mA, $I_{D3,rms}=847.6$mA after optimization.

The comparison between calculation and simulation results after optimization is shown in Table 5-4.

Table 5-4: Comparison of simulation and calculation results of diode currents after optimization

	$I_{D,av,sim}$/mA	$I_{D,av,cal}$/mA	Errors	$I_{D,rms,sim}$/mA	$I_{D,rms,cal}$/mA	Errors
D_1	99.08	98.3	0.8%	951.5	968.23	1.76%
D_2	99.3	99.28	0.02%	804.37	815.8	1.42%
D_3	101.54	100	1.5%	845.69	847.6	0.23%
D_4	101.9	101.38	0.51%	826.52	838.7	1.47%

Discussions:

Formulas to calculate the diode currents in the HWCW voltage multiplier circuit are derived in equation (5-6),(5-16) and (5-25). The optimization method of odd diode currents considering the influence of the output load is introduced as well. Based on the diode currents, the average and rms values of currents through diodes and capacitors can be calculated.

The errors between the simulation and calculation results may come from the fact that the output current used in the formula is not accurate due to the existence of output load. When calculating the average values and rms values , the current is assumed to be discrete but actually it is continuous which will also result in the errors.

5-3 Conduction losses of diodes

In this section, the power losses of the diodes in the voltage multiplier circuit are calculated and the influence of frequency to power losses is compared. The power losses of diodes consist of conduction losses and switching losses. The conduction losses are losses produced by diodes during conduction and the switching losses of diodes are caused by reverse recovery as is discussed in section 5-1.

The conduction loss is calculated by[21]:

$$P_{con} = U_{D0} * I_{F,av} + R_D * I_{F,rms}^2 \tag{5-26}$$

Where U_{D0} is the on-state zero-current voltage and R_D is the on-state resistance of the diode.

The diodes used in the real multiplier circuit are GB01SLT12_25C. From datasheet, U_{D0} and R_D can be calculated: U_{D0}=0.97V,R_D=0.6Ω. The parameters of the voltage multiplier circuit are shown in Table 2-1, the power losses are calculated under three different frequencies of 100kHz, 250kHz and 500kHz.

Using Equation (5-6),(5-16) and (5-25), the calculation results of diode currents are shown in Figure 5-5.

Table 5-5: Diode currents under different frequencies

Frequency	Current	D_1	D_2	D_3	D_4
100kHz	$I_{D,av,cal}$/mA	100.35	99.63	99.18	98.18
	$I_{D,rms,cal}$/mA	652.97	539.97	521.03	547.28
250kHz	$I_{D,av,cal}$/mA	99.28	99.98	99.13	99.96
	$I_{D,rms,cal}$/mA	815.8	686.88	675.6	690.47
500kHz	$I_{D,av,cal}$/mA	98.3	99.28	100	101.38
	$I_{D,rms,cal}$/mA	968.23	815.8	847.6	838.7

Based on the current values, the conduction losses can be estimated under different frequencies. In order to satisfy the maximum peak reverse voltage of the diodes, 10 diodes are connected in series in each stage to avoid the diodes from breaking down. The conduction losses are shown in Table 5-6.

Table 5-6: Calculation results of conduction losses

Frequency	$P_{D1,cal}$/W	$P_{D2,cal}$/W	$P_{D3,cal}$/W	$P_{D4,cal}$/W	$P_{Dtotal,cal}$/W
100kHz	3.53	2.71	2.59	2.75	11.58
250kHz	4.96	3.8	3.7	3.83	16.29
500kHz	6.58	4.96	5.28	5.2	22.02

Simuations are made in LTspice. The simulation results of diode currents and power losses based on the simulation values are shown in Table 5-7 and Table 5-8.

The errors between the calculation results and the simulation results of conduction losses are shown in Table 5-9.

Table 5-7: Simulation results of diode currents under different frequencies

Frequency	Current	D_1	D_2	D_3	D_4
100kHz	$I_{D,av,sim}$/mA	109.14	103.66	107.5	102.72
	$I_{D,rms,sim}$/mA	620.22	532.63	527.26	527.03
250kHz	$I_{D,av,sim}$/mA	120.79	118	124.43	119.38
	$I_{D,rms,sim}$/mA	747.77	643.27	648.6	607.81
500kHz	$I_{D,av,sim}$/mA	99.08	99.3	101.54	101.9
	$I_{D,rms,sim}$/mA	951.5	804.37	845.69	826.52

Table 5-8: Simulation results of conduction losses under different frequencies

Frequency	$P_{D1,sim}$/W	$P_{D2,sim}$/W	$P_{D3,sim}$/W	$P_{D4,sim}$/W	$P_{Dtotal,sim}$/W
100kHz	3.37	2.65	2.71	2.66	11.39
250kHz	4.53	3.63	3.73	3.38	15.27
500kHz	6.39	4.85	5.28	5.09	21.61

The conduction losses are related with the selection of diodes and the current values in the multiplier circuit. Diodes with lower U_{D0} and R_D will result in fewer conduction losses. When the diodes and the topology of the multiplier circuit are determined, the conduction losses are increased with the increased operating frequency since the current is increased.

Table 5-9: Comparison of simulation and calculation results of conduction losses

Frequency	$P_{con,cal}$/W	$P_{con,sim}$/W	Errors
100kHz	11.58	11.39	1.7%
250kHz	16.29	15.27	6.7%
500kHz	22.02	21.61	1.9%

5-4 Power losses of capacitors

The power losses of capacitors are provided by the ESR of capacitors. The ESR is related with the operating frequency in the circuit. Capacitor losses are calculated by:

$$P_C = ESR * I_{C,rms}^2 \tag{5-27}$$

The ESR values under different frequencies per stage are shown in Table 5-10.

Capacitor losses are calculated under three different frequencies: 100kHz, 250kHz and 500kHz as well in order to find the influence of frequency to power losses of capacitors. The currents through capacitors are the sum of the diode currents. The capacitor with lower number has larger charging and discharging time and larger current. The calculation results of capacitor currents and power losses are shown in Table 5-11.

Simuations are made in LTspice. The simulation results of capacitor currents and losses based on the simulation values are shown in Table 5-12.

Discussions:

Table 5-10: ESR values under different frequencies

Frequency	100kHz	250kHz	500kHz
ESR/Ω	3.875	1.55	0.775

Table 5-11: Calculation results of capacitor currents and losses with different frequencies

		100kHz	250kHz	500kHz
C_1	$I_{C1,cal}$/A	1.13	1.43	1.75
	$P_{C1,cal}$/W	4.94	3.16	2.37
C_2	$I_{C2,cal}$/A	0.93	1.18	1.45
	$P_{C2,cal}$/W	3.35	2.15	1.62
C_3	$I_{C3,cal}$/A	0.75	0.96	1.17
	$P_{C3,cal}$/W	2.17	1.42	1.06
C_4	$I_{C4,cal}$/A	0.54	0.69	0.83
	$P_{C4,cal}$/W	1.12	0.73	0.53
$P_{Ctotal,cal}$/W		11.58	7.46	5.58

1.From both the calculation and simulation results, the increase in frequency will result in the decrease in capacitor losses. When the operating frequency is increased, although the rms values of the capacitor current are also increased, the frequency-related ESR values are decreased and they are in inverse proportion to frequency. As a result, the capacitor losses are decreased as the frequency is increased.

2.When the frequency is relatively low, the ratio of diode losses is low and the ratio of capacitor losses is high. When the frequency is relatively high, the ratio of diode losses is high and the ratio of capacitor losses is low. The comparison between the diode losses and capacitor losses are shown in Figure 5-5.

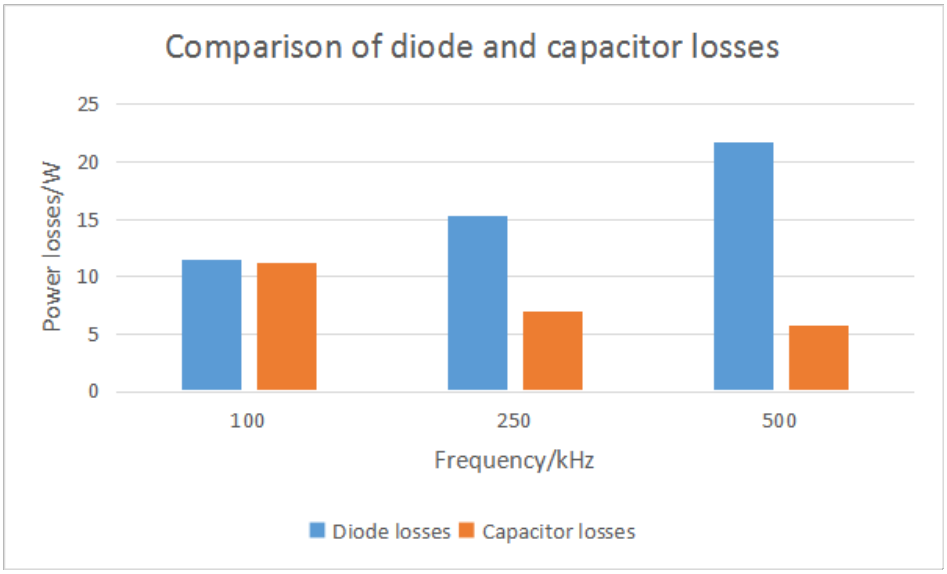

Figure 5-5: Power losses of diodes and capacitors with different frequencies

Table 5-12: Simulation results of capacitor currents and losses with different frequencies

		100kHz	250kHz	500kHz
C_1	$I_{C1,sim}$/A	1.13	1.42	1.75
	$P_{C1,sim}$/W	4.94	3.13	2.37
C_2	$I_{C2,sim}$/A	0.91	1.14	1.46
	$P_{C2,sim}$/W	3.21	2.01	1.65
C_3	$I_{C3,sim}$/A	0.72	0.89	1.22
	$P_{C3,sim}$/W	2.01	1.23	1.15
C_4	$I_{C4,sim}$/A	0.51	0.6	0.83
	$P_{C4,sim}$/W	1.01	0.56	0.53
$P_{Ctotal,sim}$/W		11.17	6.93	5.7
Errors		3.7%	7.1%	2.1%

Therefore, when the multiplier circuit is operating at low frequencies, the capacitor losses should be considered first. On the contrary, when the operating frequency of the circuit is high, the diode losses should be considered first. The choice of frequency should be determined by taking both the capacitor losses and diode losses into consideration.

5-5 Summary

In this chapter, the main power losses in the voltage multiplier circuit are analyzed. The service life of the voltage multiplier circuit can be predicted by considering the power loss analyses when designing a voltage multiplier circuit.

The detailed switching process of diodes is explained in section 5-1. Reverse recovery only occurs in the diodes in the first stage. Even though the reverse recovery process occurs, due to the zero voltage switching, the reverse recovery losses of diodes do not exist. Equations for diode currents are derived and a new RMS value calculation model is proposed in section 5-2. Based on the derivations of diode currents, the conduction losses of diodes and ESR losses of capacitors can be calculated in section 5-3 and section 5-4 respectively. As the operating frequency increases, the conduction losses increase while the ESR losses decrease.

Chapter 6

Optimization of Capacitance Network

6-1 Introduction

The analyses in the previous chapters are based on the assumption of equal capacitance distribution per stage in the HWCW voltage multiplier circuit. However, according to [11][12], the performance of voltage drop and voltage ripple will be different when different capacitances are used per stage. The formulas of output voltage ripple and output voltage drop are shown in equation (6-1) and (6-2) when capacitances are unequal[14]:

$$\delta V_o = \frac{I_o}{f} \sum_{k=1}^{n} \frac{n-k+1}{C_{2k}} \tag{6-1}$$

$$\Delta V_o = \frac{I_o}{f} \left(\sum_{k=1}^{n} \frac{(n-k+1)^2}{C_{2k-1}} + \sum_{k=1}^{n-1} \frac{(n-k+1)(n-k)}{C_{2k}} \right) \tag{6-2}$$

Table 6-1: Optimization methods for unequal capacitance distribution

Method 1	C_{2k-1}=C_{2k}=C (k>0)
Method 2	C_1=2C; C_k=C (k>1)
Method 3	C_{2k-1}=C_{2k}=(n-k+1)C (k>0)
Method 4	C_{2k-1}=$(n-k+1)^2$C; C_{2k}=(n-k+1)C (k>0)
Method 5	C_{2k-1}=$(n-k+1)^2$C; C_{2k}=(n-k+1)(n-k)C; C_2=C_1=C (k>1)

In this section, the electrical performances of the HWCW voltage multiplier circuit including the voltage regulation, respond time and power losses are studied based on unequal capacitance distribution per stage. In order to compare the effects of unequal capacitance distributions, five optimization methods shown in Table 6-1 are discussed. In Table 6-1, C represents the base capacitance and C=10nF in this project.

Method 1 to Method 4 in Table 6-1 are proposed by [11] and Method 5 is proposed in this thesis. The aims of the optimization methods are to decrease the contributions of the terms

in equation(6-1) and (6-2) to voltage drop and voltage ripple. Moreover, by the proposing of Method 5, the terms in equation (6-1) and (6-2) are minimized to the minimum degree as is shown in equation (6-3) and (6-4) below. The values of output voltage drop and voltage ripple are decreased by applying the capacitance distribution methods indicated in Table 6-1.

$$\delta V_o = \frac{I_o}{fC} \sum_{k=1}^{n} \frac{1}{(n-k)} \tag{6-3}$$

$$\Delta V_o = \frac{I_o}{f}(\sum_{k=1}^{n} \frac{1}{C} + \sum_{k=1}^{n-1} \frac{1}{C}) = (2n-1)\frac{I_o}{fC} \tag{6-4}$$

When the stage number of the HWCW voltage multiplier circuit equals to two, the capacitance distributions of Case 4 and Case 5 are totally the same in each stage. Therefore, the analyses are based on the 3-stage HWCW voltage multiplier shown in Figure 6-1 in this chapter.

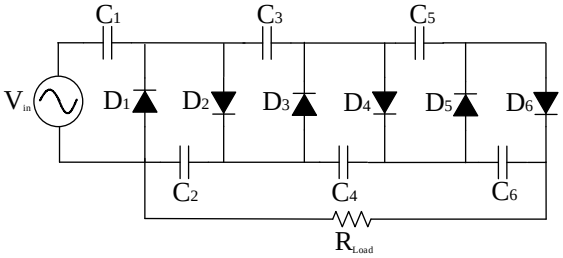

Figure 6-1: 3-stage HWCW voltage multiplier circuit

The capacitance value in each stage for the five optimization methods are shown in Table 6-2. The capacitance values are selected based on the fact that the total numbers of capacitors used in each method are kept the same. As a result, the capacitance distrubtion methods are compared under same size and cost of the multiplier circuit.

Table 6-2: Capacitance distribution values in five optimization methods

	C_1/nF	C_2/nF	C_3/nF	C_4/nF	C_5/nF	C_6/nF
Method 1	35.2	35.2	35.2	35.2	35.2	35.2
Method 2	66	33	33	33	33	33
Method 3	52.8	52.8	35.2	35.2	17.6	17.6
Method 4	118.8	39.6	52.8	26.4	13.2	13.2
Method 5	99	66	44	22	11	11

The influence of the optimization methods to voltage drop&voltage ripple, rise time&decay time and power losses are discussed in section 6-2,6-3 and 6-4 respectively.

6-2 Influence of capacitance optimization to voltage drop and voltage ripple

As is mentioned in section 2-3-1, the assumptions during the derivations of voltage drop and voltage ripple are still valid. Therefore, the output voltage drop and voltage ripple of five

optimization methods can be derived according to equation (6-1) and (6-2). The formulas of output voltage drop ΔV_o, output voltage ripple δV_o, the total voltage deduction compared with no-load output voltage value $\Delta V_{o,tot}$ and total capacitance value C_{tot} are indicated in Table 6-3, where $\Delta V_{o,tot}=\Delta V_o+\frac{1}{2}\delta V_o$.

Table 6-3: Voltage drop and voltage ripple for five optimization methods

	δV_o	ΔV_o	$\Delta V_{o,total}$	C_{tot}
Method 1	$\frac{n(n+1)}{2}\frac{I_o}{fC}$	$\frac{4n^3+3n^2-n}{6}\frac{I_o}{fC}$	$\frac{8n^3+9n^2+n}{12}\frac{I_o}{fC}$	2nC
Method 2	$\frac{n(n+1)}{2}\frac{I_o}{fC}$	$\frac{4n^3-n}{6}\frac{I_o}{fC}$	$\frac{8n^3+3n^2+n}{12}\frac{I_o}{fC}$	(2n+1)C
Method 3	$\frac{nI_o}{fC}$	$\frac{n^2I_o}{fC}$	$\frac{2n^2+n}{2}\frac{I_o}{fC}$	n(n+1)C
Method 4	$\frac{nI_o}{fC}$	$\frac{n(n+1)}{2}\frac{I_o}{fC}$	$\frac{n^2+2n}{2}\frac{I_o}{fC}$	$\frac{n(n+1)(n+2)}{3}$C
Method 5	$(\sum_{k=1}^{n-1}\frac{1}{n-k}+1)\frac{I_o}{fC}$	$\frac{(2n-1)I_o}{fC}$	$(2n-\frac{1}{2}+\frac{1}{2}\sum_{k=1}^{n-1}\frac{1}{n-k})\frac{I_o}{fC}$	$\frac{4n^3+3n^2-n+6}{6}$C

If we define the output voltage deduction ratio M as the ratio of total output voltage deduction $\Delta V_{o,tot}$ to no-load steady state output voltage value($M=\frac{\Delta V_{o,tot}}{2nV_m}$), M represents the ability of voltage conversion from input to output for multiplier circuits with different stage numbers. The ability of voltage conversion becomes worse as M increases.

For methods from Method 1 to Method 4, the formulas of $\Delta V_{o,tot}$ include terms of n^3 and n^2 which result in the existence of n^2 and n in M. As a result, M is an increasing function of the stage number n and the voltage conversion ratio becomes smaller as the stage number increases. Therefore, for Method 1 to Method 4, the output voltage value will reach its largest value at an optimal stage number N_{opt}. The output voltage value starts to decrease when the stage number is larger than N_{opt} because the increase in voltage drop and voltage ripple is larger than the increase in output voltage.

For Method 5, if $\frac{I_o}{fC}$ is assumed to be constant, the terms of $\Delta V_{o,tot}$ can be rewritten as:

$$\Delta V_{o5,tot} = 2n + \sum_{k=1}^{n-2}\frac{1}{n-k} = 2n + \sum_{k=2}^{n-1}\frac{1}{k} \approx 2n + ln(n-1) - 1 + C \tag{6-5}$$

C is the Euler's constant and C≈0.57722.

Therefore, M_5 can be expressed as a function of n:

$$M_5(n) = \frac{2n + ln(n-1) - 0.42278}{2n} = 1 + \frac{1}{2} * \frac{ln(n-1) - 0.42278}{n} \tag{6-6}$$

The derivative of M_5 is:

$$M_5'(n) = \frac{1}{2n^2} * (\frac{n}{n-1} - ln(n-1) + 0.42278) \tag{6-7}$$

From equation (6-5), it can be obtained that M_5 has its largest value when n=6 that $M_5(n=6)=1.05\frac{I_o}{fC}$. When the stage number keeps increasing larger than 6, the voltage conversion ratio of Method 5 is not decreasing like ratios of Method 1 to Method 4. Therefore, the voltage conversion ability is steady as the stage number increases. In other words, with Method 5, the

voltage multiplier circuit is able to provide any output voltage in principle even the voltage drop and voltage ripple are taken into consideration.

The voltage conversion ratio $\frac{V_o}{V_m}$ is calculated for the five optimization methods when the stage number increases from 1 to 15. The results of the voltage conversion ratio are shown in Figure 6-2.

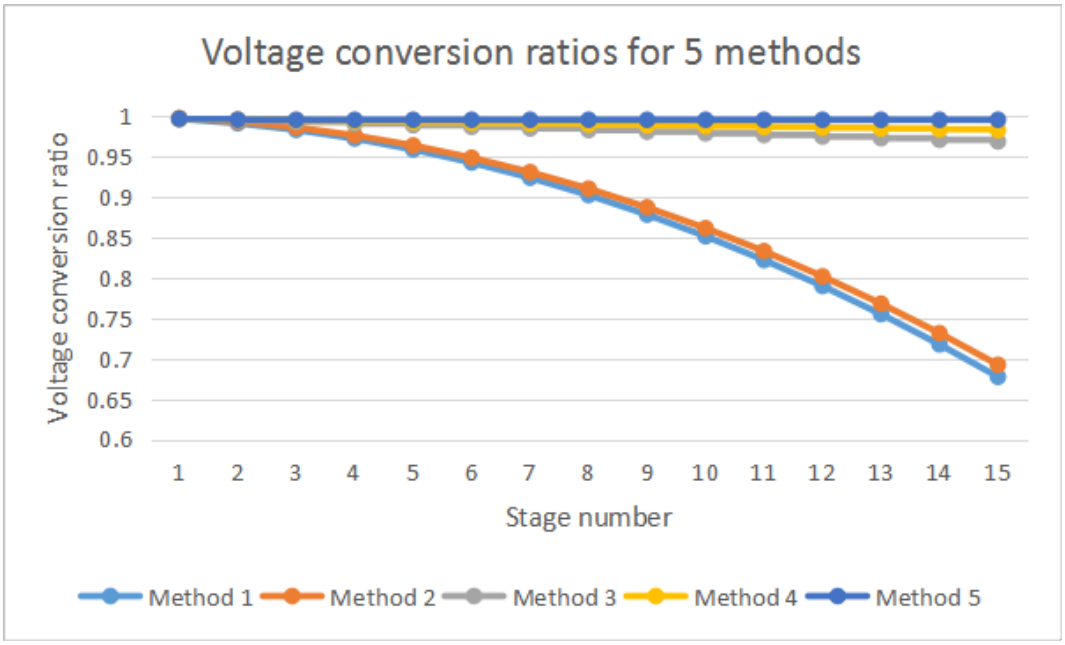

Figure 6-2: Voltage conversion ratio with stage number in 5 methods

From Figure 6-2, it is verified that the voltage conversion ratio of Method 5 can be regarded as constant while the ratios of other methods decrease as the stage number increases. Method 5 provides the best performance in voltage drop and votlage ripple whatever the stage number is. Compared with Method 1 and Method 2, the variations in voltage conversion ratios of Method 3,4 are smaller. However, the improvement in voltage drop and voltage ripple will lead to larger total capacitance as a result.

The 3-stage HWCW voltage multiplier in Figure 6-1 is used as a case study in this chapter. The values of voltage drop and voltage ripple are calculated with the five optimization methods as shown in Table 6-4. The base capacitance is C=10nF and other parameters keep unchanged as shown in Table 2-1.

Table 6-4: Calculation results of voltage regulation in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$\delta V_{o,cal}/V$	22.73	24.24	22.73	30.3	30.3
$\Delta V_{o,cal}/V$	83.33	70.71	68.18	60.61	60.61

The simulations are made in LTspice. The simulation waveforms of voltage drop and voltage ripple in steady state for 5 methods are shown in Figure 6-3.

The simulation results of voltage drop and voltage ripple are shown in Table 6-5.

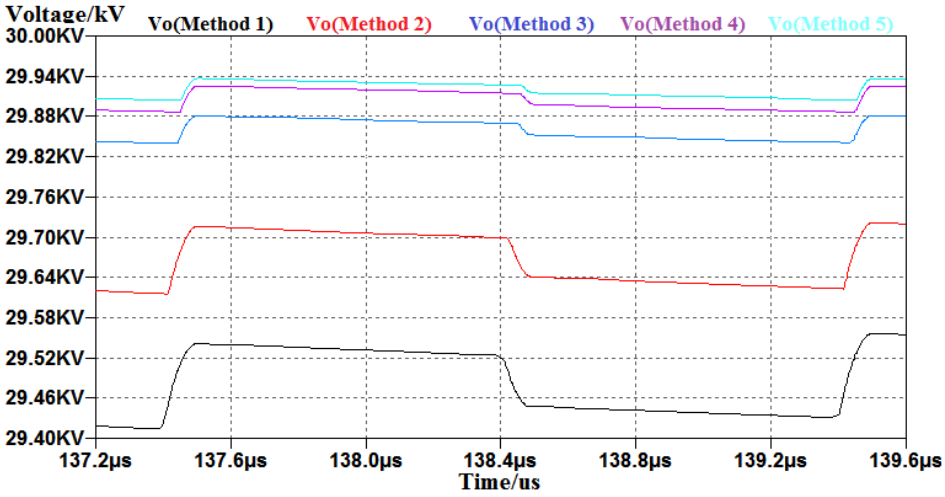

Figure 6-3: Simulation waveform of voltage regulation in 5 methods

Table 6-5: Simulation results of voltage regulation in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$\delta V_o/V$	22.41	23.81	22.3	29.68	29.26
$\Delta V_o/V$	78.9	66.79	66.6	57.66	58.56

The simulation results correspond with the theoretical analysis. Method 4 and Method 5 have the smallest voltage drop while Method 1 and Method 3 have the smallest voltage ripple. For the total output voltage, Method 4 and Method 5 have the best performance. The unequal capacitance distribution will lead to improvement in voltage drop and voltage ripple. The voltage drop and voltage ripple can be theoretically calculated using the formulas in Table 6-3.

6-3 Influence of capacitance distribution to respond time

6-3-1 Rise time with capacitance optimization

For Method 1 with the equal capacitance distribution per stage, the rise time can be estimated from Table 6-6. In order to simplify the table, only the voltage values of output capacitors and output voltage are indicated in Table 6-6. V_{out}=5.93A where A is the maximum voltage of inout voltage source V_m, the rise time is the time period when the output voltage rises from 0.593A to 5.34A.

From Table 6-6, when V_o=0.1V_{om}=0.593A, the circuit is in the first switching cycle. When V_o=0.9V_{om}=5.34A, the circuit is in the 30^{th} switching cycle. Therefore, the rise time takes around 29 switching periods which is approximately 59μs.

When the capacitance distribution in the circuit is unequal such as from Method 2 to Method 5, the voltage relationships listed in section 2-1-2 are not valid anymore because the voltage variations of the adjacent capacitors will be different. For example, when D_2 is conducting in the circuit as is shown in Figure 2-3(b) and $C_1 \neq C_2$, the voltage drop of C_1 does not equal to

Table 6-6: Rise time calculation for 3-stage HWCW multiplier

Period	V_{C2}		V_{C4}		V_{C6}		V_{out}	
	N	P	N	P	N	P	N	P
1	0	A	0	O	0	0	0	A
2	0.5A	1.25A	0	0.25A	0	0	0.5A	1.5A
3	0.75A	1.375A	0.125A	0.438A	0	0.063A	0.875A	1.863A
4	0.906A	1.453A	0.25A	0.578A	0.063A	0.156A	1.219A	2.187A
5	1.016A	1.508A	0.367A	0.691A	0.156A	0.262A	1.539A	2.461A
6	1.099A	1.55A	0.478A	0.788A	0.262A	0.369A	1.839A	2.707A
7	1.169A	1.584A	0.579A	0.874A	0.369A	0.474A	2.117A	2.932A
8	1.229A	1.615A	0.674A	0.951A	0.474A	0.574A	2.377A	3.14A
9	1.283A	1.642A	0.749A	1.016A	0.574A	0.662A	2.606A	3.32A
10	1.329A	1.664A	0.839A	1.084A	0.662A	0.75A	2.83A	3.498A
11	1.374A	1.687A	0.917A	1.146A	0.75A	0.834A	3.041A	3.667A
12	1.416A	1.708A	0.99A	1.203A	0.834A	0.912A	3.24A	3.823A
13	1.456A	1.728A	1.057A	1.256A	0.912A	0.985A	3.425A	3.969A
14	1.492A	1.746A	1.121A	1.306A	0.985A	1.053A	3.598A	4.105A
15	1.526A	1.763A	1.179A	1.353A	1.053A	1.116A	3.758A	4.232A
16	1.558A	1.779A	1.234A	1.396A	1.116A	1.175A	3.908A	4.35A
17	1.588A	1.794A	1.286A	1.437A	1.175A	1.23A	4.049A	4.461A
18	1.615A	1.808A	1.334A	1.474A	1.23A	1.282A	4.179A	4.564A
19	1.641A	1.821A	1.378A	1.51A	1.282A	1.33A	4.301A	4.661A
20	1.665A	1.833A	1.42EA	1.542A	1.33A	1.375A	4.415A	4.75A
21	1.687A	1.844A	1.459A	1.573A	1.375A	1.417A	4.521A	4.834A
22	1.708A	1.854A	1.495A	1.602A	1.417A	1.456A	4.62A	4.912A
23	1.728A	1.864A	1.529A	1.628A	1.456A	1.492A	4.713A	4.984A
24	1.746A	1.873A	1.56A	1.653A	1.492A	1.526A	4.798A	5.052A
25	1.763A	1.882A	1.59A	1.677A	1.526A	1.558A	4.879A	5.117A
26	1.779A	1.89A	1.617A	1.698A	1.558A	1.588A	4.954A	5.176A
27	1.794A	1.897A	1.643A	1.718A	1.588A	1.615A	5.025A	5.23A
28	1.808A	1.904A	1.667A	1.737A	1.615A	1.641A	5.09A	5.282A
29	1.821A	1.91A	1.689A	1.755A	1.641A	1.665A	5.151A	5.33A
30	1.833A	1.916A	1.71A	1.771A	1.665A	1.688A	5.208A	5.375A

the voltage increase of C_2 as well. If C_1:C_2=n:1, ΔV_{C1}:ΔV_{C2}=1:n. As a result, the increase in voltage across capacitors will be faster, which means that the start-up process requires fewer swtiching periods to reach steady state when unequal capacitance distribution methods are used.

For methods from Method 2 to Method 5, since the base capacitance is the same as Method 1(C=10nF) and C_1 always has the largest capacitance value, the increase in total capacitance represents the increase in ratios of adjacent capacitor values. Therefore, the rise time of the output voltage decreases as the total capacitance increases.

Simulations are made in LTspice to verify the analysis. The simulation waveform is shown in Figure 6-4 and the simulation results are shown in Table 6-7.

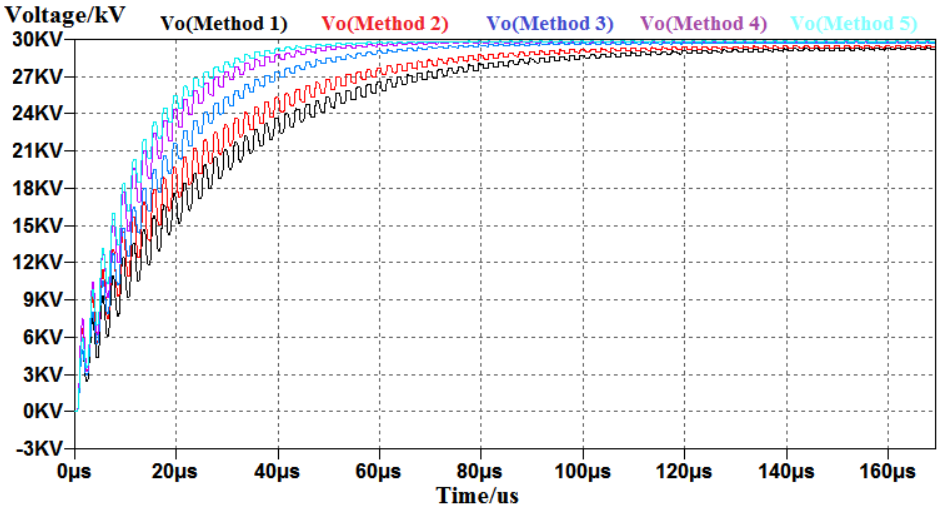

Figure 6-4: Simulation waveform of rise time in 5 methods

Table 6-7: Simulation results of rise time in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$T_r/\mu s$	58.37	48.43	36.29	26.49	24.32

The simulation results correspond with the theoretical analysis. Method 5 has the fastest rise time while Method 1 has the slowest rise time.

6-3-2 Decay time with capacitance optimization

The decay process is the combination of several stages of RC discharging processes. Therefore, the decay process is influenced by the change of capacitance value per stage. The decay process of five capacitance optimization methods are discussed seperately in this section.

- Decay process of Method 1
  The decay process of Method 1 includes three stages.

In the first stage, the output capacitors C_2, C_4 and C_6 are charging the load, this stage ends when $V_{C2}+V_{C4}+V_{C6}=V_{C1}+V_{C3}+V_{C5}$=25kV. At the end of this stage, $V_{C2}=V_{C4}=V_{C6}$=8.33kV, V_o=0.83V_{om}. Therefore, τ_1=0.33RC, t_1=0.06RC.

In the second stage, all the capacitors are charging the load together until V_{C1} decreases to 0. At the end of this stage, $V_{C2}=V_{C4}=V_{C6}$=3.33kV, V_o=0.33V_{om}. Therefore, τ_2=0.67RC, t_2=0.61RC.

In the third stage, C_2 to C_6 are charging the load together until V_o=0.1V_{om}. τ_3=0.83RC, t_3=RC.

The total decay time of output voltage in Method 1 is t_{d1}=1.67RC.

- Decay process of Method 2
  The decay process of Method 2 includes two stages.

  In the first stage, the output capacitors C_2, C_4 and C_6 are charging the load, this stage ends when $V_{C2}+V_{C4}+V_{C6}=V_{C1}+V_{C3}+V_{C5}$=25kV. At the end of this stage, $V_{C2}=V_{C4}=V_{C6}$=8.33kV, V_o=0.83V_{om}. Therefore, τ_1=0.33RC, t_1=0.06RC.

  In the second stage, all the capacitors are charging the load together until V_o=0.1V_{om}. τ_2=0.73RC, t_2=1.55RC.

  The total decay time of output voltage in Method 2 is t_{d2}=1.61RC.

- Decay process of Method 3
  The decay process of Method 3 includes 5 stages.

  In the first stage, the output capacitors C_2, C_4 and C_6 are charging the load. At the end of this stage, V_{C2}=9.09kV, V_{C4}=8.64kV,V_{C6}=7.27kV, V_o=0.83V_{om}. Therefore, τ_1=0.55RC, t_1=0.1RC.

  In the second stage, all the capacitors are charging the load together until V_{C6} decreases to 0. At the end of this stage, V_{C2}=6.67kV,V_{C4}=5kV, V_o=0.39V_{om}. Therefore, τ_2=1.09RC, t_2=0.83RC.

  In the third stage, V_{C1} to V_{C5} are charging the load until V_{C5} decreases to 0. At the end of this stage, V_{C2}=4.67kV,V_{C4}=2kV, V_o=0.22V_{om}. Therefore, τ_3=1.75RC, t_3=0.98RC.

  In the fourth stage, V_{C1} to V_{C4} are charging the load until V_{C4} decreases to 0. At the end of this stage, V_{C2}=3.33kV, V_o=0.11V_{om}. Therefore, τ_4=2.4RC, t_4=1.66RC.

  In the fifth stage, V_{C1} to V_{C3} are charging the load until V_o=0.1V_{om}. Therefore, τ_5=4.2RC, t_5=0.44RC.

  The total decay time of output voltage in Method 3 is t_{d3}=4.01RC.

- Decay process of Method 4
  The decay process of Method 4 includes 5 stages.

  In the first stage, the output capacitors C_2, C_4 and C_6 are charging the load. At the end of this stage, V_{C2}=9.09kV, V_{C4}=8.64kV,V_{C6}=7.27kV, V_o=0.83V_{om}. Therefore, τ_1=0.55RC, t_1=0.1RC.

  In the second stage, all the capacitors are charging the load together until V_{C6} decreases to 0. At the end of this stage, V_{C2}=6.67kV,V_{C4}=5kV, V_o=0.39V_{om}. Therefore, τ_2=1.28RC, t_2=0.98RC.

In the third stage, V_{C1} to V_{C5} are charging the load until V_{C5} decreases to 0. At the end of this stage, V_{C2}=6.56kV,V_{C4}=4.83kV, V_o=0.38V_{om}. Therefore, τ_3=1.93RC, t_3=0.05RC.

In the fourth stage, V_{C1} to V_{C4} are charging the load until V_{C4} decreases to 0. At the end of this stage, V_{C2}=3.33kV, V_o=0.11V_{om}. Therefore, τ_4=3.97RC, t_4=4.88RC.

In the fifth stage, V_{C1} to V_{C3} are charging the load until V_o=0.1V_{om}. Therefore, τ_5=5.77RC, t_5=0.61RC.

The total decay time of output voltage in Method 4 is t_{d4}=6.62RC.

- Decay process of Method 5
  The decay process of Method 5 includes 5 stages.

  In the first stage, the output capacitors C_2, C_4 and C_6 are charging the load. At the end of this stage, V_{C2}=9.5kV, V_{C4}=8.5kV,V_{C6}=7kV, V_o=0.83V_{om}. Therefore, τ_1=0.6RC, t_1=0.11RC.

  In the second stage, all the capacitors are charging the load together until V_{C6} decreases to 0. At the end of this stage, V_{C2}=8.33kV,V_{C4}=5kV, V_o=0.44V_{om}. Therefore, τ_2=1.33RC, t_2=0.84RC.

  In the third stage, V_{C1} to V_{C5} are charging the load until V_{C5} decreases to 0. At the end of this stage, V_{C2}=7.85kV,V_{C4}=3.54kV, V_o=0.38V_{om}. Therefore, τ_3=2.23RC, t_3=0.35RC.

  In the fourth stage, V_{C1} to V_{C4} are charging the load until V_{C4} decreases to 0. At the end of this stage, V_{C2}=6.67kV, V_o=0.22V_{om}. Therefore, τ_4=4.23RC, t_4=2.29RC.

  In the fifth stage, V_{C1} to V_{C3} are charging the load until V_o=0.1V_{om}. Therefore, τ_5=8.77RC, t_5=7RC.

  The total decay time of output voltage in Method 4 is t_{d4}=10.59RC.

The decay time of output voltage in each method is calculated in Table 6-8.

Table 6-8: Calculation results of decay time in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$t_{d,cal}$/ms	11.76	10.63	14.12	17.48	23.3

Simulations are made in LTspice to verify the theoretical analysis above. The simulation waveform is shown in Figure 6-5 and the simulation results are shown in Table 6-9.

Table 6-9: Simulation results of decay time in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$t_{d,sim}$/ms	11.66	10.63	14.16	17.52	23.29

Discussion:

The simulation results correspond with the theoretical analysis. Among the five capacitance distribution methods, Method 2 has the fastest decay time while Method 5 has the slowest

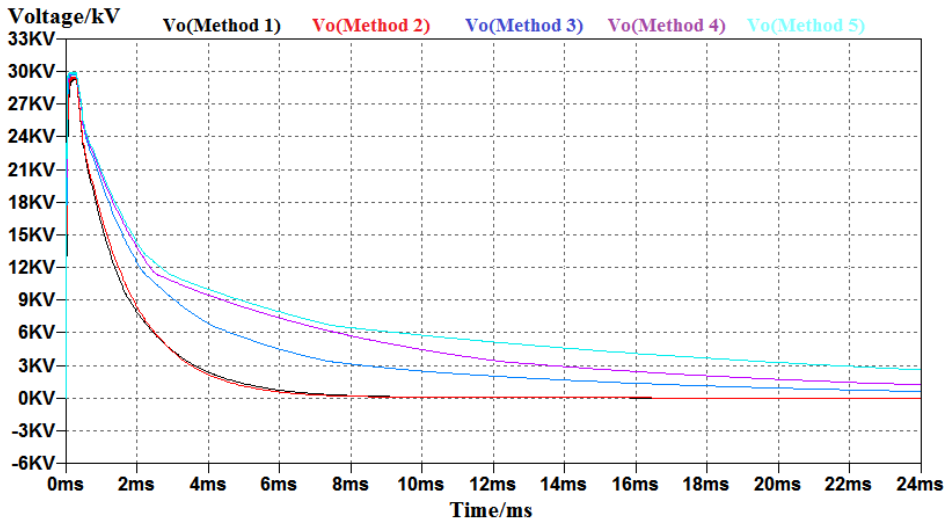

Figure 6-5: Simulation waveform of decay time in 5 methods

decay time. However, the decay time of Method 5 is still controlled within tens of microseconds which is acceptable for the power supply circuit. Moreover, when the power supply is used as a common supply instead of pulse power supple, the decay time is not as important as rise time.

6-4 Influence of capacitance distribution to power loss

6-4-1 Diode losses with capacitance optimization

The derivations in section 5-2 are still valid with unequal capacitance value per stage. Therefore, the power losses produced by diodes and capacitors can be estimated based on the conclusions in section 5-2. The formulas in section 5-2 should be modified in case of unequal capacitance distribution.

- Calculation of I_{D1}
  When D_1 is conducting in the circuit, the voltage drop across C_1 during the conduction of D_1 is $\frac{I_o}{fC_1}$. The conduction time of D_1 t_{D1} and average current value during the conduction of D_1 I_{D1} can be calculated.

$$t_{D1} = \frac{1}{4f} - \frac{arcsin(1 - \frac{I_o}{AfC_1})}{2\pi f}$$

$$I_{D1} = \frac{I_o}{ft_{D1}}$$

- Calculation of I_{D2}
  When D_2 is conducting in the circuit, $Asin2\pi ft = V_{C2} - V_{C1}$.

$$V_{C1} = A - \frac{(n-k)I_o}{fC_1} = A - \frac{2I_o}{fC_1}$$

$$V_{C2} = 2A - \delta V_{C1} - \frac{kI_o}{fC_2} = 2A - \frac{3I_o}{fC_1} - \frac{I_o}{fC_2}$$

Therefore,t_{D2} and I_{D2} can be calculated.

$$t_{D2} = \frac{1}{4f} - \frac{arcsin(1 - \frac{I_o}{AfC_1} - \frac{I_o}{AfC_2})}{2\pi f}$$

$$I_{D2} = \frac{I_o}{ft_{D2}}$$

- Calculation of I_{D3}
  When D_3 is conducting in the circuit, $Asin2\pi ft = V_{C3} + V_{C1} - V_{C2}$.

$$V_{C1} = A - \frac{kI_o}{fC_1} = A - \frac{2I_o}{fC_1}$$

$$V_{C2} = 2A - \delta V_{C1} - \frac{(n-k)I_o}{fC_2} - X_{C2} = 2A - \frac{3I_o}{fC_1} - \frac{I_o}{fC_2} - X_{C2}$$

$$V_{C3} = 2A - \delta V_{C1} - \delta V_{C2} - \frac{I_o}{fC_3} + X_{C2} = 2A - \frac{3I_o}{fC_1} - \frac{3I_o}{fC_2} - \frac{I_o}{fC_3} + X_{C2}$$

  X_{C2} represents the voltage drop of C_2 within half of the swithing period due to the existence of output load.

  Therefore,t_{D3} and I_{D3} can be calculated.

$$t_{D3} = \frac{1}{4f} - \frac{arcsin(1 - \frac{2I_o}{AfC_1} - \frac{2I_o}{AfC_2} - \frac{I_o}{AfC_3} + \frac{2X_{C2}}{A})}{2\pi f} - t_{D1}$$

$$I_{D3} = \frac{I_o}{ft_{D3}}$$

- Calculation of I_{D4}
  When D_4 is conducting in the circuit, $Asin2\pi ft = V_{C4} + V_{C2} - V_{C3} - V_{C1}$.

$$V_{C1} = A - \frac{(n-k)I_o}{fC_1} = A - \frac{I_o}{fC_1}$$

$$V_{C2} = 2A - \delta V_{C1} - \frac{kI_o}{fC_2} = 2A - \frac{3I_o}{fC_1} - \frac{2I_o}{fC_2}$$

$$V_{C3} = 2A - \Delta V_{C3} - \frac{I_o}{fC_3} + X_{C2} = 2A - \Delta V_{C3} - \frac{I_o}{fC_3} + X_{C2}$$

$$V_{C4} = 2A - \Delta V_{C3} + X_{C2} - \delta V_{C3} - \frac{I_o}{fC_4}$$

  Therefore,t_{D4} and I_{D4} can be calculated.

$$t_{D4} = \frac{1}{4f} - \frac{arcsin(1 - \frac{2I_o}{AfC_1} - \frac{2I_o}{AfC_2} - \frac{I_o}{AfC_3} - \frac{I_o}{AfC_4})}{2\pi f} - t_{D2}$$

$$I_{D4} = \frac{I_o}{ft_{D4}}$$

- Calculation of I_{D5}
  When D_5 is conducting in the circuit, Asin2πft=V_{C5}+V_{C3}+V_{C1}-V_{C4}-V_{C2}. D_5 is in the last stage, when D_5 starts to conduct, voltage across odd capacitors are at the minimum steady state value while voltage across even capacitors are at the maximum steady state value minus X_C.

$$V_{C1} = A - \delta V_{C1}$$
$$V_{C2} = 2A - \delta V_{C1} - X_{C2}$$
$$V_{C3} = 2A - \Delta V_{C3} - \delta V_{C3} + X_{C2}$$
$$V_{C4} = 2A - \Delta V_{C4} - X_{C4}$$
$$V_{C5} = 2A - \Delta V_{C5} - \delta V_{C5} + X_{C2} + X_{C4}$$

  t_{D5} and I_{D5} can be calculated.

$$t_{D3} = \frac{1}{4f} - \frac{arcsin(1 - \frac{\Delta V_{C5}+\delta V_{C5}}{A} + \frac{2X_{C2}+2X_{C4}}{A})}{2\pi f} - t_{D1} - t_{D3}$$

$$I_{D5} = \frac{I_o}{f t_{D5}}$$

- Calculation of I_{D6}
  When D_6 is conducting in the circuit, Asin2πft=V_{C6}+V_{C4}+V_{C2}-V_{C5}-V_{C3}-V_{C1}. D_6 is in the last stage, when D_6 starts to conduct, voltage across odd capacitors are at the maximum steady state value while voltage across even capacitors are at the minimum steady state value.

  t_{D6} and I_{D6} can be calculated.

$$t_{D6} = \frac{1}{4f} - \frac{arcsin(1 - \frac{\Delta V_{C6}+\delta V_{C6}}{A})}{2\pi f} - t_{D2} - t_{D4}$$

$$I_{D6} = \frac{I_o}{f t_{D6}}$$

When unequal capacitance per stage are applied in the circuit, the currents can be calculated according to the formulas above. It is notable that when calculating the currents through odd diodes, the influence of output load should be taken into consideration in order to get accurate results.

The RMS model shown in Figure 5-4 is still valid. The average and rms values of diode currents in steady state can be calculated with the RMS model. The results are shown in Table 6-10.

Based on the current values in Table 6-10, the conduction losses can be estimated. In order to satisfy the maximum peak reverse voltage of the diodes, 10 diodes are connected in series in each stage to avoid the diodes from breaking down. The conduction losses are shown in Table 6-11.

Simulations are made in LTspice. The parameters are kept the same with the theoretical calculations which is indicated in Table 2-1. The simulation results of diode currents are shown in Table 6-12.

Table 6-10: Steady state diode current values in 5 methods

		Method 1	Method 2	Method 3	Method 4	Method 5
D_1	$I_{Dav,cal}$/mA	64.56	66.31	65.9	69.19	67.68
	$I_{Drms,cal}$/mA	984.08	1176.49	1105.56	1350	1288
D_2	$I_{Dav,cal}$/mA	64.67	63.8	65.23	64.25	62.77
	$I_{Drms,cal}$/mA	822.53	865.72	917.42	939.13	998.89
D_3	$I_{Dav,cal}$/mA	64.5	66.06	65.11	67.08	63.96
	$I_{Drms,cal}$/mA	850.74	847	920.69	930.51	859.29
D_4	$I_{Dav,cal}$/mA	67.49	66.91	64.19	64.42	68.37
	$I_{Drms,cal}$/mA	848.75	843.54	843.52	847.72	838.25
D_5	$I_{Dav,cal}$/mA	64.46	66.06	68	66.63	64.75
	$I_{Drms,cal}$/mA	838.75	827.38	796.48	720.98	661.17
D_6	$I_{Dav,cal}$/mA	68.82	66.91	65.91	68.07	67.15
	$I_{Drms,cal}$/mA	858.47	835.28	744.36	707.35	665.44

Table 6-11: Calculation results of conduction loss in 5 methods

	P_{D1}/W	P_{D2}/W	P_{D3}/W	P_{D4}/W	P_{D5}/W	P_{D6}/W	P_{Dtot}/W
Method 1	6.44	4.69	4.97	4.98	4.85	5.09	31.02
Method 2	8.95	5.11	4.94	4.92	4.75	4.83	33.5
Method 3	7.97	5.68	5.72	4.89	4.46	3.96	32.68
Method 4	11.61	5.91	5.84	4.94	3.76	3.66	35.72
Method 5	10.61	6.59	5.05	4.88	3.25	3.31	33.69

The conduction losses can be calculated from the results in Table 6-12. The simulation results of conduction losses in five methods are shown in Table 6-13.

The unequal capacitance distribution per stage results in larger currents flowing in the circuit, which leads to larger conduction losses of diodes. The total conduction losses in the multiplier circuit increase as a result. Method 1 has the smallest conduction losses while Method 4 and Method 5 have the largest conduction losses. The conduction loss of D_1 increases obviously compared with the conduction losses of other diodes.

6-4-2 Capacitor losses with capacitance optimization

The capacitor losses due to the existence of ESR are discussed in this section. Based on the results in Table 6-10, the capacitor currents can be calculated which is shown in Table 6-14.

The relationship of capacitance value and corresponding ESR value is shown in Table 6-15. The capacitor is MLCC - SMD/SMT 4kV 2200pF 10% X7R from Syfer. Capacitors are connected in combination of series and parallel connections to meet the requirement for both the capacitance value and voltage rating.

Based on results in Table 6-14 and Table 6-15, the capacitor losses due to ESR can be calculated. The calculation results are shown in Table 6-16.

Simulations are made in LTspice. The simulation results of capacitor currents are shown in Table 6-17.

Table 6-12: Simulation results of diode currents in 5 methods

		Method 1	Method 2	Method 3	Method 4	Method 5
D_1	$I_{Dav,sim}$/mA	66.82	66.81	67.18	66.88	66.96
	$I_{Drms,sim}$/mA	950.64	1096	1043	1245	1192
D_2	$I_{Dav,sim}$/mA	66.95	66.58	67.61	66.43	67.82
	$I_{Drms,sim}$/mA	802.22	834.53	874.18	878.76	957.22
D_3	$I_{Dav,sim}$/mA	67.12	66.37	67.35	67.43	67.54
	$I_{Drms,sim}$/mA	835.74	817.69	876.89	880.43	921.84
D_4	$I_{Dav,sim}$/mA	66.85	67.95	67.88	66.69	66.36
	$I_{Drms,sim}$/mA	810.1	816.93	845	835.41	802.47
D_5	$I_{Dav,sim}$/mA	68.03	68.16	68.64	67.05	67.02
	$I_{Drms,sim}$/mA	841.26	825.79	791.63	723.21	695.41
D_6	$I_{Dav,sim}$/mA	68.4	67.62	67.95	67.51	67.18
	$I_{Drms,sim}$/mA	831.17	817.85	742.89	692.36	655.4

Table 6-13: Simulation results of conduction losses in 5 methods

	P_{D1}/W	P_{D2}/W	P_{D3}/W	P_{D4}/W	P_{D5}/W	P_{D6}/W	P_{Dtot}/W
Method 1	6.07	4.51	4.84	4.59	4.91	4.81	29.73
Method 2	7.86	4.82	4.66	4.66	4.75	4.67	31.42
Method 3	7.18	5.24	5.27	4.94	4.43	3.97	31.03
Method 4	9.95	5.28	5.31	4.83	3.79	3.53	32.69
Method 5	9.17	6.16	5.75	4.51	3.55	3.23	32.37

The capacitor losses can be calculated based on the results in Table 6-17. The simulation results of capacitor losses are shown in Table 6-18.

The simulation results correspond with the theoretical calculations. Even though the capacitor currents increase with increased capacitance values, the ESR values of capacitors decrease as well. As a result, the total capacitor losses in the multiplier circuit decrease when the unequal capacitance distribution are applied in the multiplier circuit.

The total power losses including the diode losses and capacitor losses in five optimization methods are shown in Table 6-19. The distributions of conduction losses and capacitor losses are shown in Figure 6-6.

6-5 Summary

In this chapter, the optimization of unequal capacitance value per stage is applied in the voltage multiplier circuit. Five optimization methods indicated in Table 6-1 are discussed and compared including four methods from reference and one newly proposed method 'Method 5' in this thesis. With Method 5, the output voltage conversion ratio will not decrease like other four methods as the stage number increases. Therefore, the voltage multiplier with Method 5 is able to produce large output voltage in principle even the voltage drop and voltage ripple are taken into consideration.

Table 6-14: Calculation results of capacitor currents in 5 methods

	$I_{C1,cal}$/A	$I_{C2,cal}$/A	$I_{C3,cal}$/A	$I_{C4,cal}$/A	$I_{C5,cal}$/A	$I_{C6,cal}$/A
Method 1	2.13	1.89	1.7	1.47	1.2	0.86
Method 2	2.22	1.89	1.68	1.45	1.18	0.84
Method 3	2.19	1.89	1.66	1.38	1.09	0.74
Method 4	2.3	1.87	1.61	1.32	1.01	0.71
Method 5	2.23	1.82	1.52	1.26	0.94	0.67

Table 6-15: Relationsip of capacitance and ESR values

	ESR_{C1}/Ω	ESR_{C2}/Ω	ESR_{C3}/Ω	ESR_{C4}/Ω	ESR_{C5}/Ω	ESR_{C6}/Ω
Method 1	0.23	0.23	0.23	0.23	0.23	0.23
Method 2	0.12	0.24	0.24	0.24	0.24	0.24
Method 3	0.15	0.15	0.23	0.23	0.45	0.45
Method 4	0.07	0.2	0.15	0.3	0.6	0.6
Method 5	0.08	0.12	0.18	0.36	0.72	0.72

The comparisons are made with the condition that the numbers of total capacitors used in each method are kept the same. Therefore, the size and cost of the power supply circuit are the same for each method. With unequal capacitance distributions, electrical performances such as voltage drop, voltage ripple and output voltage rise time are improved. The decay time is increased but it is still controlled within acceptable ranges. Moreover, when the circuit is used as a regular power supply instead of a pulse power supply, the decay time is not as important as rise time. With unequal capacitance distributions, the power losses in the circuit increase as well due to the increased current. The distribution method should be chosen by taking the specific requirements for the multiplier circuit into consideration.

Table 6-16: Calculation results of capacitor losses in 5 methods

	P_{C1}/W	P_{C2}/W	P_{C3}/W	P_{C4}/W	P_{C5}/W	P_{C6}/W	P_{Ctot}/W
Method 1	1.03	0.81	0.65	0.49	0.33	0.17	3.48
Method 2	0.59	0.86	0.68	0.51	0.34	0.17	3.15
Method 3	0.72	0.54	0.62	0.43	0.54	0.25	3.1
Method 4	0.35	0.7	0.39	0.53	0.62	0.3	2.89
Method 5	0.4	0.4	0.42	0.57	0.64	0.33	2.76

Table 6-17: Simulation results of capacitor currents in 5 methods

	$I_{C1,sim}$/A	$I_{C2,sim}$/A	$I_{C3,sim}$/A	$I_{C4,sim}$/A	$I_{C5,sim}$/A	$I_{C6,sim}$/A
Method 1	2.19	1.96	1.76	1.52	1.23	0.85
Method 2	2.19	1.88	1.67	1.44	1.16	0.81
Method 3	2.16	1.87	1.64	1.37	1.08	0.74
Method 4	2.24	1.84	1.59	1.31	1	0.69
Method 5	2.23	1.86	1.57	1.25	0.96	0.65

Table 6-18: Simulation results of capacitor losses in 5 methods

	P_{C1}/W	P_{C2}/W	P_{C3}/W	P_{C4}/W	P_{C5}/W	P_{C6}/W	P_{Ctot}/W
Method 1	1.09	0.87	0.7	0.52	0.34	0.16	3.68
Method 2	0.58	0.85	0.67	0.5	0.32	0.16	3.08
Method 3	0.7	0.53	0.61	0.42	0.53	0.25	3.04
Method 4	0.37	0.68	0.38	0.52	0.6	0.29	2.84
Method 5	0.4	0.42	0.45	0.57	0.67	0.31	2.82

Table 6-19: Total power losses in 5 methods

	Method 1	Method 2	Method 3	Method 4	Method 5
$P_{con,tot}$/W	29.73	31.42	31.03	32.69	32.37
$P_{ESR,tot}$/W	3.68	3.08	3.04	2.84	2.82
P_{total}/W	33.41	34.5	34.07	35.53	35.19

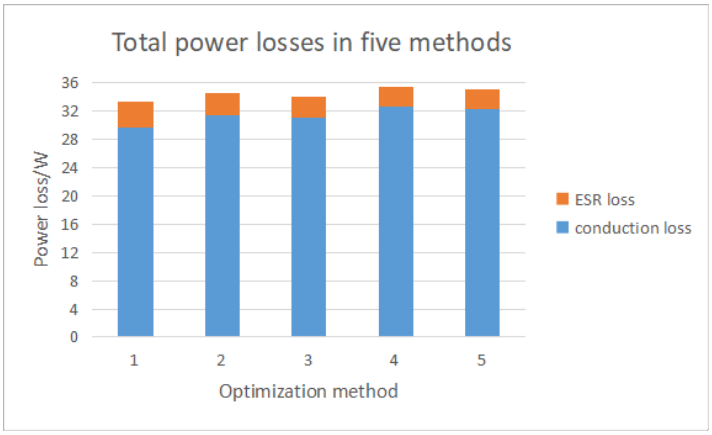

Figure 6-6: Distributions of conduction loss and capacitor loss in 5 methods

Chapter 7

Conclusion

This master thesis project is carried out in order to investigate and improve the electrical performance of the voltage multiplier circuit including the voltage drop&voltage ripple, rise time&decay time of output voltage and power losses. So as to achieve the primary objective, many efforts have been made towards the goal including the analysis and modeling of influence of circuit parameters and parasitic components, the establishment of power loss model and optimization methods of unequal capacitance value per stage. Based on the theoretical analysis and simulation verification presented in this thesis report from Chapter 2 to 6, the most important conclusions are summarized below:

- The voltage drop and voltage ripple are proportional to output power and in inverse proportion to frequency and capacitance value. The rise time is in inverse proportion to frequency and the decay time is proportional to output power and capacitance value. Therefore, when determining the circuit parameters, lower output power and higher frequency will improve the electrical performances of the circuit. The capacitance value should be determined by considering the trade-offs between the voltage regulation and decay time.

  The junction capacitance of diodes and ESR of capacitors will cause additional voltage drop and voltage ripple in the circuit. Although the existence of ESL and C_{pp} of capacitros will improve the voltage regulation, they will also cause LC oscillations and voltage spikes in the circuit. The parasitics of the transformer will force the start-up process to end ealier than expected. As a result, the voltage drop is increased while the voltage ripple and rise time are decreased.

- The power loss model of the voltage multiplier circuit is established in the thesis. The reverse recovery process only exists in the diodes in the first stage. However, the reverse recovery happens with zero voltage switching which results in no reverse recovery losses. The calculation methods of conduction losses of diodes and capacitor losses due to ESR are introduced by the deriviations of currents and a RMS calculation model. When the frequency is relatively low, the ESR losses are in majority. When the frequency is high

,the conduction losses are in majority. The conduction losses increase and the capacitor losses decrease as the frequency increases.

- Five optimization methods of unequal capacitance value distributions are compared in this thesis. Among the five optimization methods, one newly proposed method that is able to keep the output voltage turn ratio in steady as the stage number increases is introduced. With the newly proposed method, the voltage drop, voltage ripple and rise time are optimized. Although the decay time is increased, it is still kept under a reasonable range.

  For voltage multiplier circuits with different specific requirements, there will always be one best capacitance distribution method out of five.

7-1 Recommedation for choice of parameters

For the capacitance value, unequal capacitance distribution per stage will improve the electrical behavior. Five capacitance distribution methods are compared in this thesis. Although the performance of voltage drop, voltage ripple and rise time can be improved by applying unequal capacitances, the decay time and total capacitances are increased. Due to different requirements for different voltage multiplier circuits, the base capacitance value and capacitance distribution method should be selected by considering the trade-offs between the electrical performances and the physical size and cost of the voltage multiplier circuit.

For the frequency value, higher operating frequency will lead to better voltage regulation and faster rise time. Higher frequency will also decrease the physical size of the multiplier circuit. Therefore, it is better to set the frequency as high as possible in principle. However, the upper limit of operating frequency exists in the practical due to some constraints. The bottle necks for further switching frequency increase are indicated below:

1.The increase in frequency will result in the deduction of the reactance of capacitors and increase in currents flowing in the voltage multiplier circuit. As a result, higher operating frequency will lead to more power losses in the circuit as is analyzed in this thesis. The service life of the voltage multiplier circuit will therefore be decreased due to heating under high operating frequency.

2.Real capacitors have the equivalent series inductance , which result in the self resonance of capacitors due to the combination of L and C. The capacitors behave like inductors when the operating frequency is over the self resonanct frequency, which means that the voltage multiplier may not work anymore. Therefore, the operating frequency must be controlled under the resonant frequency of capacitors.

3.The diode reverse recovery time will also influence the upper limit of the operating frequency of the multiplier circuit. When the operating frequency is so large that the reverse recovery time of diodes are larger than the switching period, the multiplier circuit will not work any longer.

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