Printed Circuits Handbook

50th Anniversary Edition!

SEVENTH EDITION

- Printed Circuit Supply Chain Management
- Lead-Free Materials and Processes
- Printed Circuit Reliability
- Printed Circuit Design and Layout Processes

Clyde F. Coombs, Jr., and Happy T. Holden

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ABOUT THE EDITORS-IN-CHIEF

Clyde F. Coombs, Jr., joined Hewlett-Packard in 1959, where he developed the plated-through-hole process that became the basis for printed circuit production for the next 40+ years. He was the editor-in-chief of all six previous editions of *Printed Circuits Handbook*.

Happy T. Holden is the retired director of electronics engineering and innovations at Gentex Corporation, and has worked with printed circuits in various capacities since 1970. Previously, he was the CTO for Foxconn's MIP Business Group (supplier of mechanical components, flexible circuits, and rigid PCBs), a senior PCB technologist for Mentor Graphics' System Design Division, and an advanced technology manager at Westwood Associates (Nan Ya PCB) and Merix Corporation, and he worked for Hewlett-Packard for 28 years in various engineering and marketing roles.

PRINTED CIRCUITS HANDBOOK

Clyde F. Coombs, Jr. Co-Editor-in-Chief

Happy T. Holden Co-Editor-in-Chief

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CONTRIBUTORS

Mudasir Ahmad *Cisco Systems, San Jose, California* (Chaps. 62, 64)

Mark Brillhart *Palo Alto, California* (Chaps. 62, 64)

Antonio Caputo *Isola Group, Chandler, Arizona* (Chap. 59)

Michael Carano *Technologist and Chemical Consultant, Maple Plain, Minnesota* (Chap. 32)

Marc Carter *IPC—Association Connecting Electronics Industries, Bannockburn, Illinois* (Appendix)

Jean-Paul Clech *EPSI Inc., Montclair, New Jersey* (Chap. 63)

Clyde F. Coombs, Jr. *Co-Editor-in-Chief*, Printed Circuits Handbook, *Los Altos, California* (Chap. 1)

C. D. (Don) Dupriest *Lockheed Martin Missiles and Fire Control, Dallas, Texas* (Chap. 31)

Sylvia Ehrler *Feinmetall GmbH, Herrenberg, Germany* (Chap. 15)

Joseph Fjelstad *Verdant Electronics, Seattle, Washington* (Chaps. 67, 68, 69, 71)

Gary M. Freedman *Colab Engineering LLC, Stow, Massachusetts* (Chaps. 46, 47, 48, 49, 50, 51, 52)

Reza Ghaffarian *Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California* (Chaps. 60, 61)

Bill Hargin *Z-zero, Redmond, Washington* (Chap. 20)

Happy T. Holden *Co-Editor-in-Chief*, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan* (Chaps. 1, 5, 16, 25, 26, 27, 31, 43, 58, 65, 66)

Stacy Kalisz Johnson *Agilent Technologies, Gilbert, Arizona* (Chap. 55)

Mike Jouppi *Thermal Management Inc., Centennial, Colorado* (Chaps. 22, 23)

Jason Keeping *Celestica, Toronto, Ontario, Canada* (Chap. 44)

Edward Kelley *Isola Group, Chandler, Arizona* (Chaps. 9, 10, 11, 12, 13, 14)

George Milad *Uyemura International Corporation, Southington, Connecticut* (Chaps. 33, 35)

Mark I. Montrose *Montrose Compliance Services, Inc., Santa Clara, California* (Chap. 20)

Gregory C. Munie *IPC—Association Connecting Electronics Industries, Bannockburn, Illinois* (Chap. 45)

Hayao Nakahara *N.T. Information Ltd., Huntington, New York* (Chaps. 2, 34)

Robert (Bob) Neves *Microtek Laboratories, Changzhou, China* (Chap. 53)

Dominique K. Numakura *DKN Research, Haverhill, Massachusetts* (Chap. 70)

Stig Oresjo *Agilent Technologies, Loveland, Colorado* (Chap. 55)

Kenneth P. Parker *Agilent Technologies, Loveland, Colorado* (Chaps. 56, 57)

Mel Parrish *STI Electronics, Inc., Madison, Alabama* (Chap. 54)

Gareth Parry *Draig Technologies Inc., Stouffville, Ontario, Canada* (Chaps. 30, 37)

Lee W. Ritchey *Speeding Edge, Glen Ellen, California* (Chaps. 17, 19)

Tim Rodgers *University of Colorado, Boulder, Colorado* (Chaps. 3, 4, 6, 7, 8)

Michael Roesch *Hewlett-Packard Company, Palo Alto, California* (Chap. 15)

Andy Shaughnessy *Managing Editor*, The PCB Design Magazine *and* PCB Design 007, *Seaside, Oregon* (Chap. 18)

Vern Solberg *Solberg Technical Consulting, Saratoga, California* (Chap. 24)

Matthias Stickel *KSG Leiterplatten GmbH, Gornsdorf, Germany* (Chaps. 28, 29, 38)

Douglas Trobough *Isola Group, Chandler, Arizona* (Chaps. 9, 10, 11, 12, 13, 14)

Laura J. Turbini *International Reliability Consultant, Waltham, Massachusetts* (Chaps. 45, 59)

David A. Vaughan *Taiyo America, Inc., Carson City, Nevada* (Chap. 36)

Susy Webb *Design Science, Sugar Land, Texas* (Chap. 21)

David J. Wilkie *Everett Charles Technologies, Pomona, California* (Chaps. 39, 40, 41, 42)

PREFACE

This book provides the reader with the tools to be successful in the printed circuit world of today, and of the foreseeable future. A world where, increasingly, the designer/user organizations are not only different from the manufacturing organizations, they are separated by geography and language, and, perhaps most importantly, one where there is great opportunity for serious disconnect between the understanding of what is required by the user and what can be accomplished by the manufacturer. The term “supply chain” has been used to define these issues in general for non-vertically integrated organizations, but here, for the first time, we have focused specifically on those supply chain elements that relate to printed circuits. This includes design, specification, supplier identification and qualification, and process understanding and control, as well as quality and reliability specification and assurance. When a user organization entrusts its present, as well as its future, success to an outside manufacturing organization, the need for care and clarity cannot be overstated. Chapters, written by authors with experience in these issues, have been specifically developed to provide the reader with usable information on dealing with them, and will help guide the development of these relationships, for the benefit of all.

In addition, with the continued, and increasing, importance of printed circuits as the basic building block of all electronic devices, issues associated with them can be found throughout the engineering and manufacturing organizations, rather than in just design and layout in engineering and purchasing and product assembly in manufacturing. Knowledge of printed circuits, at some level, is needed by many staff members who find they have a need to understand the issues of a technology and industry that did not previously concern them. This book provides a reference, for those who are not printed circuit professionals, to find information on, and answers to, questions on process issues. It also helps define the appropriate questions to pose to either members of their own organization or the potential supplier, while developing the entire range of relationships.

From its beginning, the printed circuit has not only been one of the most important technology developments ever made, but one of the least understood and appreciated. It has often been mistakenly considered a “commodity” and purchased on the basis of board, or assembly, initial cost. In fact, there is no such thing as a “standard” or “generic” printed circuit. Every board is actually an “application-specific interconnection system” that can have immense impact on the performance, quality, reliability, and cost of the final product in which it is used. A problem that could have been resolved in the early design and acquisition processes may not be evident until the product is in use, when it is the most difficult and expensive to resolve. This book helps the reader deal with these issues at each step of the supply chain, which includes those inside the user organization as well as the supplier organizations. Specifically, these have brought about a new part entirely devoted to the understanding of, and working with, the printed circuit supply chain itself. The generic issues of

supply chain management have been well documented; however, applying them to the specific problems created by printed circuits requires specialized understanding and is addressed only in this book.

While introducing new tools to address the supply chain issues, the book remains committed to its historical role of providing detailed descriptions of the technology and processes of printed circuits that have evolved over the years, and brought up to date in this edition. It remains the only single reference on all aspects of printed circuit technology. At the same time, when revising process chapters, we have included, where possible, a discussion of issues that the reader should consider when dealing with suppliers that are involved in making boards using these processes by addressing such questions as: What are the things that help the reader know if a supplier, in fact, has the capabilities to provide what is needed? What is unreasonable to expect? How can the desired result be demonstrated initially, and maintained over time?

In using contract manufacturing to fabricate and assemble boards, the user gives up the ability to define the design rules. Success will come by having a partnership with the supplier that reconciles the needs of the user with the capabilities of the manufacturing organization. To make the communications on printed circuit issues between the designer/user and the manufacturer clearer and more efficient, the book also contains new chapters, and expanded revisions of existing chapters on design and layout of boards and assemblies. These include additional information on design and layout basics, high-performance boards, CAD tools, design for manufacturing, and information exchange systems and standards.

As electronic products have become more complex, with higher levels of performance expected, volumes never seen before, and new process and material challenges, such as

“lead-free” soldering, the using organization has had to delegate more responsibility for much of the quality and reliability of the product to the supplier organization. In response, this book also contains critical new material on the reliability of boards and assemblies, with consideration for new base materials, and assembly processes. These chapters were developed specifically for this book, and much of their contents is not available anywhere else, and will allow the user to reach reasonable agreements on process controls and acceptance criteria that ensure the needs are met.

With the continuing concern over the impact on the global environment of printed circuit wet and fabrication processes, as well as assembled boards at the end of their useful life, the issue of RoHS (Restriction of Hazardous Substances), and specifically “lead free” has caused a revolution in the industry unprecedented in its history. Specific information on the impact of the resulting changes in materials and processes is documented and described. For example, for lead-free solders, we start with the Periodic Table and define what is even possible for an alternate alloy. Thus physics and material science are used to describe alternatives available.

The end result of these additions is essentially the creation of a new book, not just a new edition. Twenty-five percent of the chapters are new to this edition, while only 16 percent are reprinted from previous editions.

The publication of this book coincides with the 50th anniversary of the publication of the first edition. That book had 16 chapters, contributed by 11 authors. This edition, the seventh, has 71 chapters contributed by 38 authors. This clearly reflects the development of the level of the technology, as well as the expansion of the user base for printed circuits over time. The fact that this book has maintained a high position of usefulness and importance to

those in the printed circuit field for this length of time must really be attributed to the skills of the authors who have contributed chapters developed from their considerable knowledge and expertise in their respective areas and at considerable time expense. It has been said that the author list for this book reads like a “who’s who” in the printed circuit industry. This has resulted in information the reader can actually use to solve problems.

We also thank the IPC—Association Connecting Electronics Industries, which has given this book total cooperation and support for every edition. We would especially like to acknowledge the active help and encouragement of IPC managers Anne Marie Mulvihill, David Bergman, and Greg Munie (who also authored a chapter). Their efforts were a great contribution to our ability to accomplish the development of a project of this size and complexity.

Clyde F. Coombs, Jr.
Happy T. Holden
Co-Editors-in-Chief

PART 1

PRINTED CIRCUIT TECHNOLOGY DRIVERS

CHAPTER 1

ELECTRONIC PACKAGING AND HIGH-DENSITY INTERCONNECTIVITY[a]

Clyde F. Coombs, Jr.

Co-Editor-in-Chief, Printed Circuits Handbook, *Los Altos, California*

Happy T. Holden

Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

1.1 INTRODUCTION

All electronic components must be interconnected and assembled to form a functional and operating system. The design and the manufacture of these interconnections have evolved into a separate discipline called *electronic packaging*. Since the early 1950s, the basic building block of electronic packaging is the printed wiring board (PWB), and it will remain that into the foreseeable future. This book

outlines the basic design approaches and manufacturing processes needed to produce these PWBs.

This chapter outlines the basic considerations, the main choices, and the potential trade-offs that must be accounted for in the selection of the interconnection methods for electronic systems. Its main emphasis is on the analysis of potential effects that the selection of various printed wiring board types and design alternatives could have on the cost and performance of the complete electronic product.

1.2 MEASURING THE INTERCONNECTIVITY REVOLUTION

The continuing increase in component performance and lead density, along with the reduction in package sizes, has required that PWB technology find corresponding ways to increase the interconnection density of the substrate. With the introduction and continued refinement of such packaging techniques as the ball grid array (BGA), chip-scale packaging (CSP), and chip-on-board (COB), traditional PWB technology has approached a point where alternative ways of providing high-density interconnection have had to be developed.

This has been called at times high-density interconnects (HDI), the interconnection revolution, or the density revolution, because doing the same things in the same way, only smaller, was no longer sufficient.

1.2.1 Interconnect Density Elements

The extent of these interconnect density issues is not always observable, but the chart[1] in Figs. 1.1 and 1.2 can help one define and understand it. The chart portrays the interrelationship between component packaging, surface-

mount technology (SMT) assembly, and PWB density. As can be seen, these three elements are interlinked. A change in one has a significant effect on the overall interconnection density. The metrics are as follows:

- *Assembly complexity*. The measure of the difficulty of assembling surface-mounted components in parts per square inch and leads per square inch.
- *Component packaging complexity*. The degree of sophistication of a component, measured by its average leads (I/Os) per part.
- *Printed wiring board density*. The amount of wiring a PWB has as measured by the average length of traces per square inch or the area of that board, including all signal layers. The metric is inches per square inch.

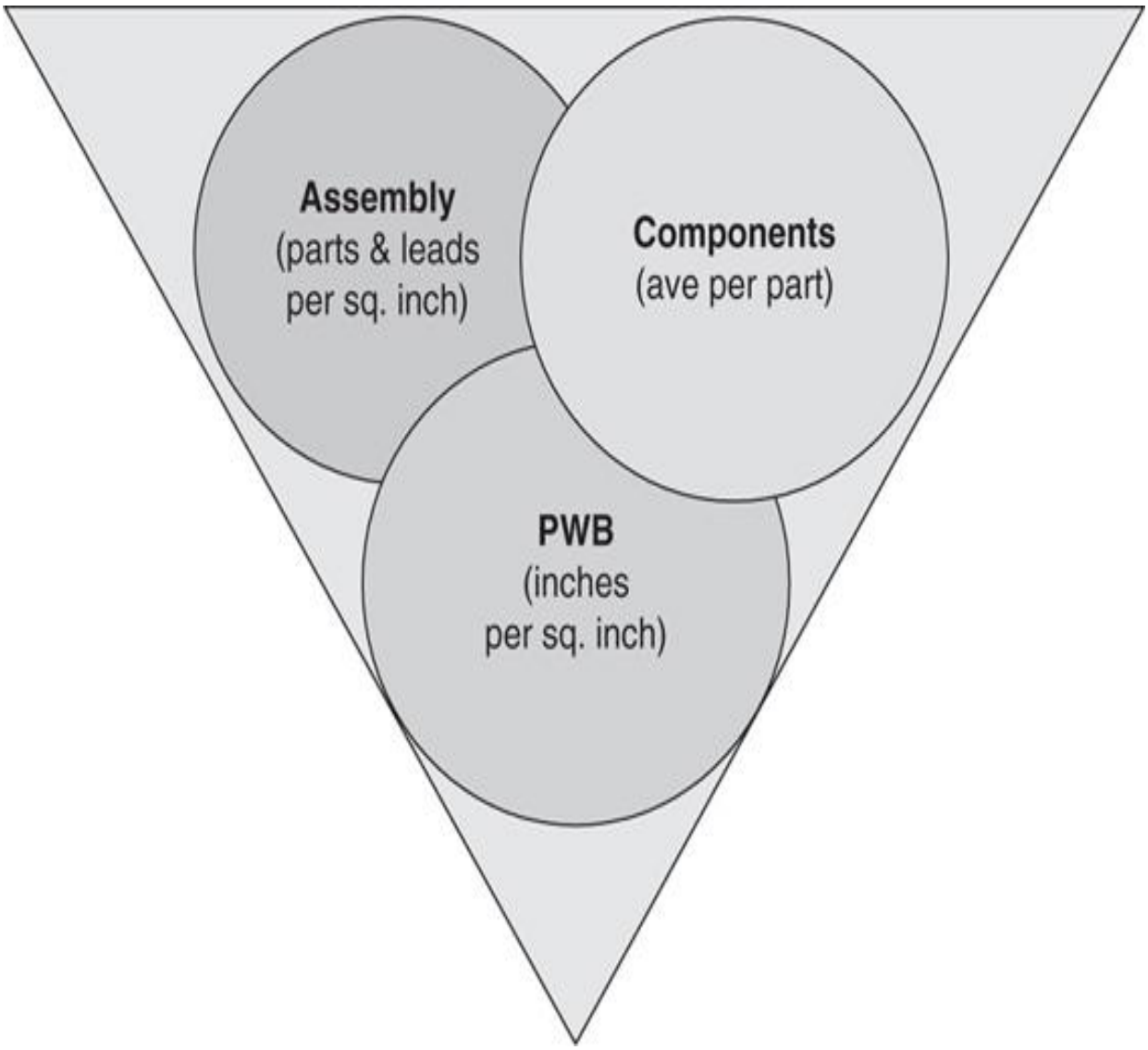

FIGURE 1.1 Representation of the metrics of assembly, component, and PWB technologies and their general relationship to each other.

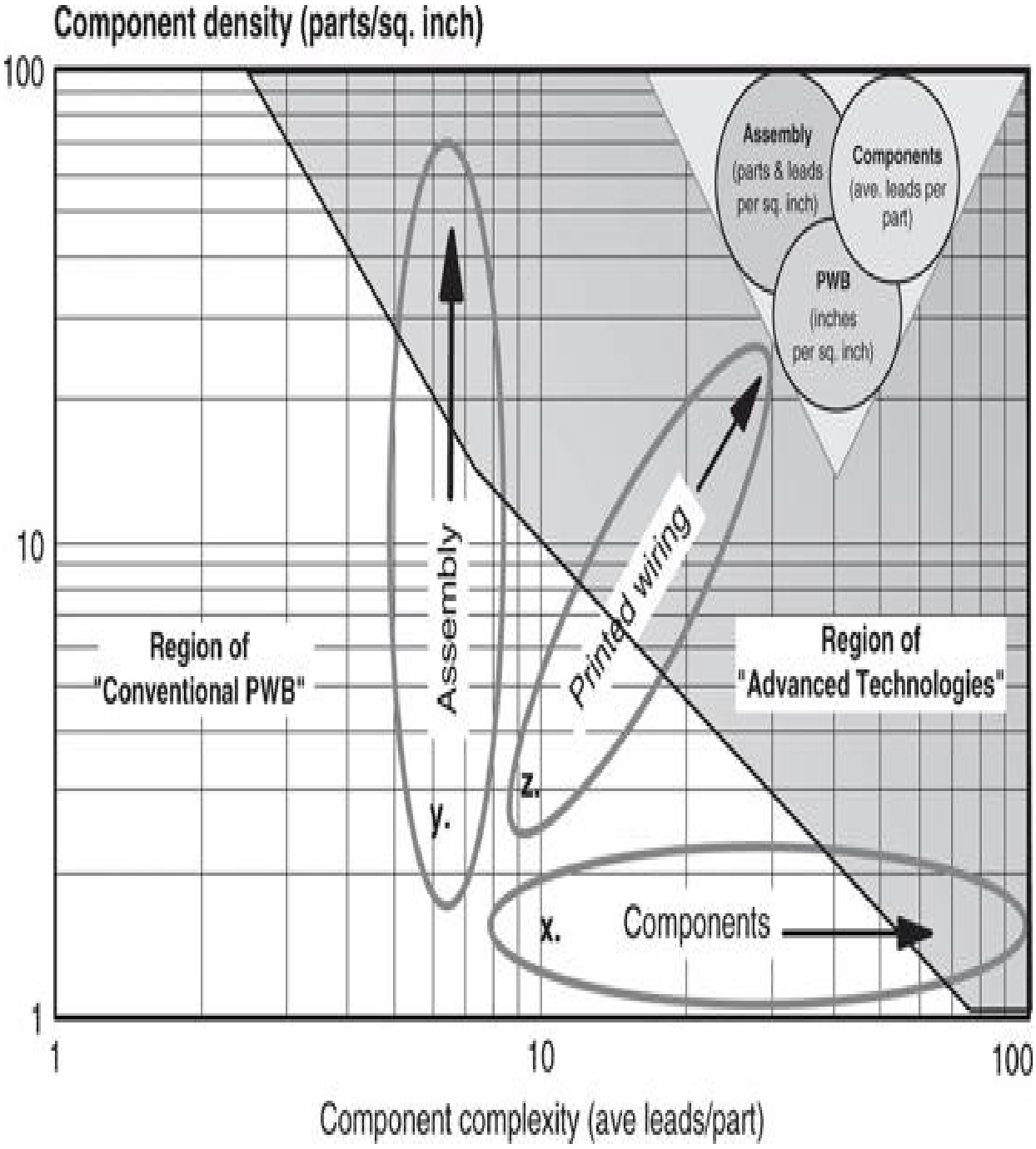

FIGURE 1.2 Component technology map, showing the relationship of assembly, PWB, and component technologies on overall package density and technology.

1.2.2 Interconnect Technology Map

To visualize the interrelationships of the three elements, see Fig. 1.2.[1] It shows these elements as axes of a three-dimensional technology map that defines the passage from conventional PWB structures to advanced technologies and shows how changes in just one of the elements can increase or decrease the total density of the entire electronic package.

To describe the component complexity of an assembly, the total component connections (I/Os) include both sides of an assembly, as well as edge fingers, or contacts, which are divided by the total number of components on the assembly. The resulting average leads (I/Os) per part provides the *x* axis of Fig. 1.1. The horizontal oval shape shows how the component complexity can vary from two leads per part in discrete circuit elements to the very large numbers seen on BGA and application-specific integrated circuits.

When Fig. 1.2 is used to describe surface-mount assemblies, the vertical (*y* axis) dimension (shown as a vertical oval) indicates how complex it is to assemble the board by number of components per square inch or square centimeter for the surface area of the PWB. This vertical oval can vary from 1 to over 100 parts per square inch. As the parts become smaller and closer together, this number naturally goes up. A second assembly measure is average leads (I/Os) per square inch or square centimeter. This is the *x*-axis value multiplied by the *y*-axis value. (For a further description of these issues, and equations for quantifying them, see Chap. 16.)

The *z*-axis oval in Fig. 1.2 describes the printed wiring board's density. This is the wiring required to connect all the I/Os of the components at the size of the assembly specified, assuming three nodes per net. This axis has the units inches per square inch, or centimeters per square centimeter. A further description of this metric is provided in this chapter and in more detail in Chap. 16.

1.2.3 An Example of the Interconnect Revolution

By charting products of a particular type over time, an analysis will show how the interconnect technology has changed and continues to change, its rate of change, and the direction of these changes. An example is given in Fig. 1.3. This shows how component technology, assembly technology, and PWB technology have led to the evolution of the same computer CPU from:

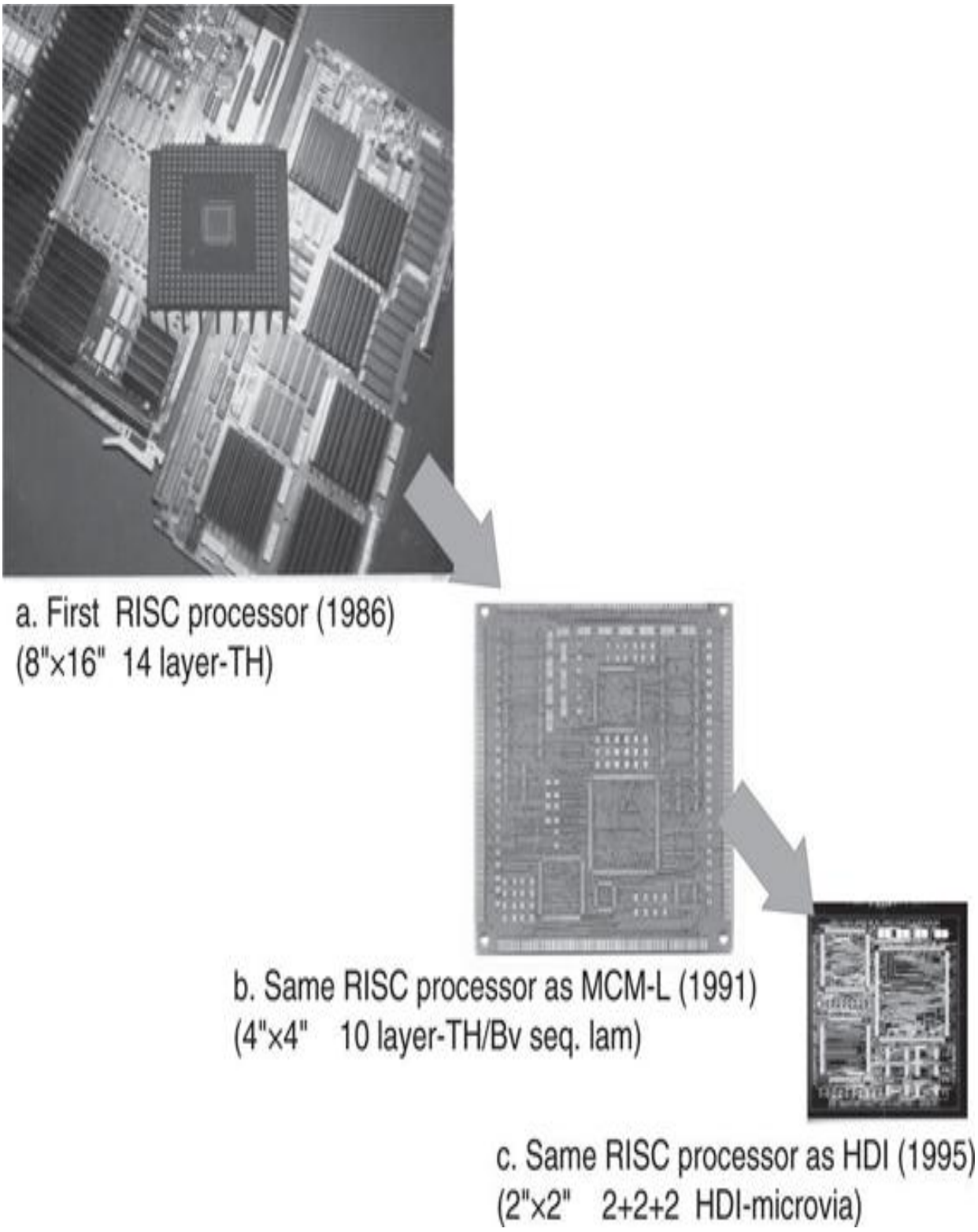

FIGURE 1.3 Example of the same computer CPU board as it used alternative component, assembly, and PWB technologies. (*a*) Size and appearance of each generation. (*b*) Movement of total board density from traditional to HDI. (*c*) HDI.

A 14-layer board through-hole with a surface area of 128 in^2 in 1986 (Fig. 1.3*a*) to a 10-layer surface-mount technology board with a surface area of 16 in^2 in 1991 (Fig. 1.3*b*) to a high-density interconnect board with sequential build-up microvias, buried and blind vias, and a surface area of 4 in^2 in 1995 (Fig. 1.3*c*).

1.2.4 Region of Advanced Technologies

A second valuable feature of the chart in Fig. 1.2 is the area identified as the region of advanced technologies. This is where calculations and data have shown that it is necessary to have an HDI structure. Therefore, this is the barrier, or wall of HDI: on one side it is most cost effective to use traditional PWB technologies; on the other side it becomes cost effective to use HDI technologies. Continuing beyond this point, HDI becomes necessary.

1.3 HIERARCHY OF INTERCONNECTIONS

To have the proper perspective on where PWBs fit into electronic systems, it will be helpful to describe briefly the packaging hierarchy of electronic systems. Some time ago, the Institute for Interconnecting and Packaging Electronic Circuits (IPC)[2] proposed eight categories of system elements in ascending order of size and complexity, which will be used here to illustrate typical electronic packaging structures. These are as follows:

Category A consists of fully processed active and passive devices. Bare or uncased chips and discrete capacitors,

resistors, or their networks are typical examples of this category.

Category B comprises all packaged devices (active and passive) in plastic packages, such as DIPs, TSOPs, QFPs, and BGAs, as well as those in ceramic packages, such as PGAs, and connectors, sockets, and switches. All are ready to be connected to an interconnecting structure.

Category C is substrates that interconnect uncased or bare chips (i.e., the components of category A) into a separable package. Included here are all types of multichip modules (MCMs), chip-on-boards (COBs), and hybrids.

Category D covers all kinds of substrates that interconnect and form assemblies of already packaged components, that is, those from categories B and C. This category includes all types of rigid PWBs, flexible and rigid-flexible, and discrete-wiring boards.

Category E covers the back planes made by printed wiring and discrete-wiring methods or with flexible circuits, which interconnect PWBs, but not components, from the preceding groups.

Category F covers all intraenclosure connections. Included in this category are harnesses, ground and power distribution buses, RF plumbing, and coax or fiberoptic wiring.

Category G includes the system assembly hardware, card racks, mechanical structures, and thermal control components.

Category H encompasses the entire integrated system with all its bays, racks, boxes, and enclosures and all auxiliary and support subsystems.

As seen from the preceding list, PWBs are exactly in the center of the hierarchy and are the most important and universally used element of electronic packaging.

The packaging categories F, G, and H are used mainly in large mainframes, supercomputers, central office switching, and some military systems. Since there is a strong trend toward the use of miniaturized and portable electronic products for the majority of electronic packaging designs, trade-offs are made in the judicious application and selection among the elements of the first five categories. These are discussed in this chapter.

1.4 FACTORS AFFECTING SELECTION OF INTERCONNECTIONS

Selection of the packaging approaches among the various aforementioned elements is dictated not only by the system function, but also by the component types selected and by the operating parameters of the system, such as the clock speeds, power consumption, and heat management methods, and the environment in which the system will operate. This section provides a brief overview of these basic constraints that must be considered for proper packaging design of the electronic system.

1.4.1 Speed of Operation

The speed at which the electronic system operates is a very important technical factor in the design of interconnections. Many digital systems operate at close to 100 MHz and are already reaching beyond that level. The increasing system speed is placing great demands on the ingenuity of packaging engineers and on the properties of materials used for PWB substrates.

The speed of signal propagation is inversely proportional to the square root of the dielectric constant of the substrate

materials, requiring designers to be aware of the dielectric properties of the substrate materials they intend to use. The signal propagation on the substrate between chips, the so-called *time of flight*, is directly proportional to the length of the conductors and must be kept short to ensure the optimal electrical performance of a system operating at high speeds.

For systems operating at speeds above 25 MHz, the interconnections must have transmission line characteristics to minimize signal losses and distortion. Proper design of such transmission lines requires careful calculation of the conductor and dielectric separation dimensions and their precise manufacture to ensure the expected accuracy of performance. For PWBs, there are two basic transmission line types:

1. Stripline
2. Microstrip (for details, see Chap. 20)

1.4.2 Power Consumption

As the clock rates of the chips increase and as the number of gates per chip grows, there is a corresponding increase in their power consumption. Some chips require up to 30 W of power for their operation. With that, more and more terminals are required to bring power in and to accommodate the return flow on the ground planes. About 20 to 30 percent of chip terminals are used for power and ground connections. With the need for electrical isolation of signals in high-speed systems operation, the count may go to 50 percent.

Design engineers must provide adequate power and ground distribution planes within the multilayer boards (MLBs) to ensure efficient, low-resistance flow of currents, which may be substantial in boards interconnecting high-speed chips consuming tens of watts and operating at 5 V,

3.3 V, or lower. Proper power and ground distribution in the system is essential for reducing *di/dt* switching interference in high-speed systems, as well as for reducing undesirable heat concentrations. In some cases, separate bus-bar structures have been required to meet such high power demands.

1.4.3 Thermal Management

All the energy that has been delivered to power integrated circuits (ICs) must be efficiently removed from the system to ensure its proper operation and long life. The removal of the heat from a system is one of the most difficult tasks of electronic packaging. In large systems, huge heat-sink structures, dwarfing the individual ICs, are required to air-cool them, and some computer companies have built giant superstructures for liquid cooling of their computer modules. Some computer designs use liquid immersion cooling. Still, the cooling needs of large systems tax the capabilities of existing cooling methods.

The situation is not that severe in smaller, tabletop or portable electronic equipment, but it still requires packaging engineers to ameliorate the hot spots and ensure longevity of operation. Since PWBs are notoriously poor heat conductors, designers must carefully evaluate the method of heat conduction through the board, using such techniques as heat vias, embedded metal slugs, and conductive planes.

1.4.4 Electronic Interference

As the frequency of operation of electronic equipment increases, many ICs, modules, or assemblies can act as generators of radio frequency (RF) signals. Such electromagnetic interference (EMI) emanations can seriously

jeopardize the operation of neighboring electronics or even of other elements of the same equipment, causing failures, mistakes, and errors, and must be prevented. There are specific EMI standards defining the permissible levels of such radiation, and these levels are very low.

Packaging engineers, and especially PWB designers, must be familiar with the methods of reducing or canceling this EMI radiation to ensure that their equipment will not exceed the permissible limits of this interference.

1.4.5 System Operating Environment

The selection of a particular packaging approach for an electronic product is also dictated by its end use and by the market segment for which that product is designed. The packaging designer has to understand the major driving force behind the product use. Is it cost driven, performance driven, or somewhere in between? Where will it be used—for instance, under the hood of a car, where environmental conditions are severe, or in the office, where the operating conditions are benign? The IPC[2] has established a set of equipment operating conditions classified by the degree of severity, which are listed in Table 1.1.

TABLE 1.1 Realistic Representative-Use Environments, Service Lives, and Acceptable Cumulative-Failure Probabilities for Surface-Mounted Electronics by Use Categories

Use category	Worst-case use environment					Years of service	Acceptable failure risk, %
	T_{min}, °C	T_{max}, °C	ΔT,* °C	t_D, h	Cycles/year		
1—Consumer	0	+60	35	12	365	1–3	~1
2—Computers	+15	+60	20	2	1460	~5	~0.1
3—Telecomm	–40	+85	35	12	365	7–20	~0.01
4—Commercial aircraft	–55	+95	20	12	365	~20	~0.001
5—Industrial & automotive	–55	+95	20	12	185		
(passenger compartment)			&40	12	100	~10	~0.1
			&60	12	60		
			&80	12	20		
6—Military	–55	+95	40	12	100		
ground & ship			&60	12	265	~5	~0.1
7—LEO	–40	+85	35	1	8760	5–20	~0.001
Space GEO				12	365		
8—Military *b*	*a*			40	2	365	
avionics *c*	–55	+95	60	2	365	~10	~0.01
			80	2	365		
			&20	1	365		
9—Automotive			60	1	1000		
(under hood)	–55	+125	&100	1	300	~5	~0.1
			&140	2	40		

& = in addition.

*ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation, calculate ΔT_c.

1.4.5.1 Cost. The universal digitization of most electronic functions led to the merger of consumer, computer, and communication technologies. This development resulted in the increased appeal of electronics and the need for mass production of many electronic products. Thus, product cost has become the most important criterion in any design of electronic systems. While complying with all the aforementioned design and operation conditions, the design engineer must keep cost as the dominant criterion, and must analyze all potential trade-offs in light of the best cost/performance solution for the product.

The importance of the rigorous cost trade-off analysis during the design of electronic products is underscored by the fact that about 60 percent of the manufacturing costs are determined in the first stages of the design process, when only 35 percent of the total design effort has been expended.

Attention to manufacturing and assembly requirements and capabilities [so-called design for manufacturability and assembly (DFM/A)] during product design can reduce assembly costs by up to 35 percent and PWB costs by up to 25 percent.

The elements that must be considered for the most cost-effective electronic packaging designs are

- Optimization of the PWB design and layout to reduce its manufacturing cost
- Optimization of the PWB design to reduce its assembly cost
- Optimization of the PWB design to reduce testing and repair costs

The following sections provide some guidelines on how to approach such optimization of PWB designs. Basically, the costs of the electronic assemblies are directly related to their complexity and there are a number of measurements

relating the effects of various PWB design elements to their costs to guide the design engineer in selection of the most cost-effective approach.

1.5 ICs AND PACKAGES

The most important factors influencing PWB design and layout are the component terminal patterns and their pitches, especially those of ICs and their packages, since these dictate the density of the interconnecting substrates. Thus, this element will be considered first.

Driven by the need for improved cost and performance, the complexity of ICs is constantly increasing. Due to relentless progress in IC technology, the gate density on a chip is increasing by about 75 percent per year, resulting in the growth of IC chip I/O terminals by 40 percent per year, which places ever increasing demands on the methods of their packaging and interconnection.

As a result, the physical size of electronic gears keeps shrinking by 10 to 20 percent per year, while the surface area of substrates is being reduced by about 7 percent per year. This is accomplished by continuously increasing wiring densities and reducing line widths, which has severely stressed PWB manufacturing methods, reduced processing yields, and increased the costs of the boards.

1.5.1 IC Packages

Since their inception, IC chips have been placed within ceramic or plastic packages. Until about 1980, all IC packages had terminal leads that were soldered into plated through-holes (PTHs) of the PWBs. Since then, an increasing number of IC packages have their terminals made in a form

suitable for surface-mounting technology (SMT), which has become the prevailing method of component mounting.

There has been a proliferation of IC package types, both for through-hole assembly as well as for surface mounting, varying in their lead configurations, placement, and pitches. Also, IPC-SM-782[3] provides a good catalog of the available SMT packages and of the PWB footprint formats they require for their assembly.

Basic I/O termination methods of IC packages include the following:

- *Peripheral*, where the terminations are located around the edges of the chip or package
- *Grid-array*, where the terminations are located on the bottom surface of the chip or package

1.6 DENSITY EVALUATIONS

1.6.1 Component Density Analysis

Because the components and their terminations exert a major effect on the design of the PWB, a number of metrics have been developed to establish the relationships between component density and PWB density. A major analysis of these relationships has been made by H. Holden[4] and some of his charts and derivations are provided here to guide the design engineers during the development of a rational PWB design.

This information is very useful in determining where the designed product will fit in the component density spectrum and what, therefore, is to be expected for PWB density.

Figure 1.4 provides a generalized view of the relationships among the component density, their terminal density, and the necessary wiring density that will be required to

accommodate the selected degree of component complexity. The definition of the wiring connectivity W_f is provided.

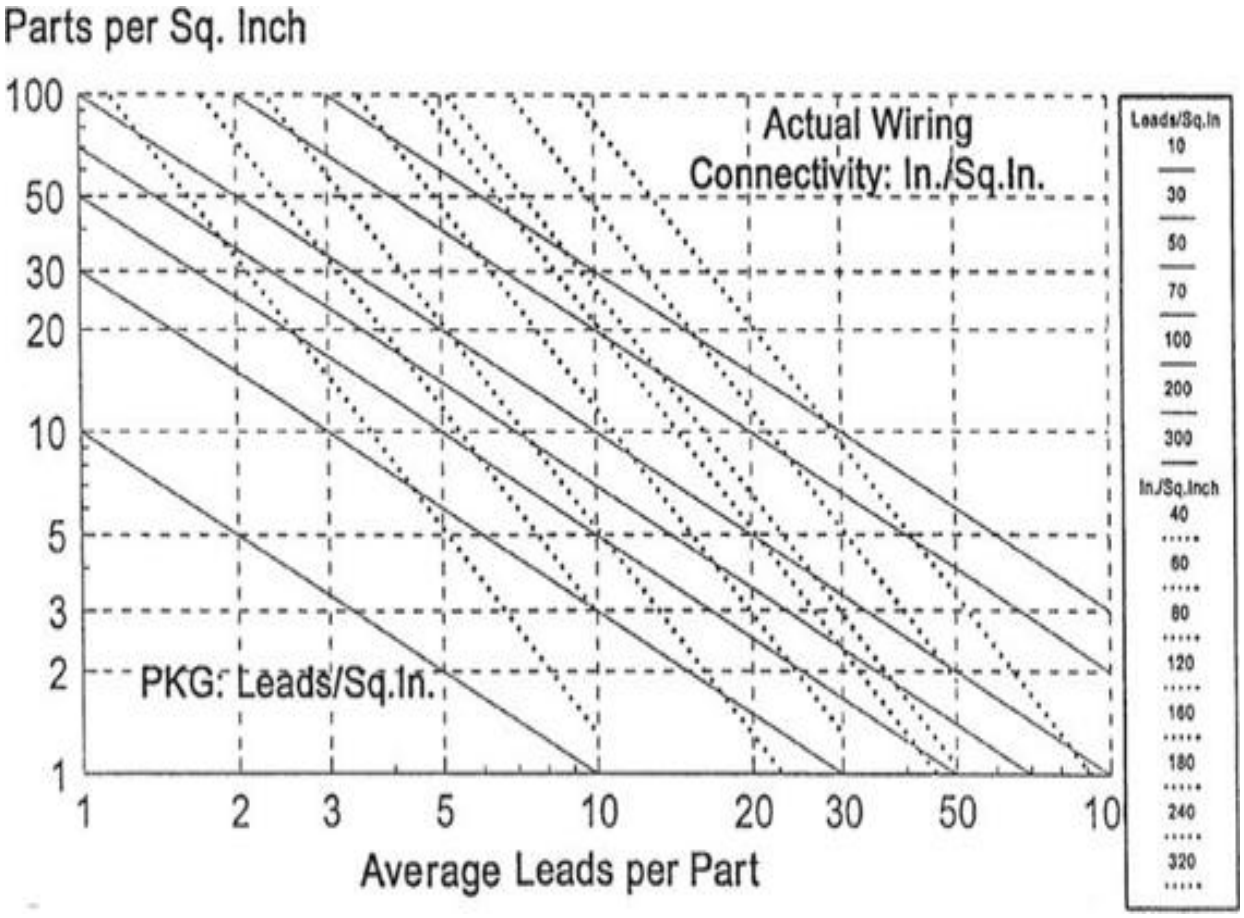

FIGURE 1.4 Plot of general relations between component and wiring density.

1.6.2 PWB Density Metrics

It is essential for the proper design of PWBs to determine the density requirements and then analyze alternative methods of board construction for the most cost-effective design. There are a number of basic terms and equations used for the calculation and analysis of PWB wiring density.

$$W_c = \frac{T * L}{G} \text{ in/in}^2 \qquad (1.1)$$

where W_c = wiring capacity
T = tracks per channel
L = number of signal layers
G = channel width

But it is more important to determine the required wiring density that will be sufficient to interconnect all the components on the desired board size. There have been a number of empirically developed equations that permit the calculation of such a wiring demand. The simplest has been developed by Dr. D. Seraphim[5]:

$$W_d = 1.25\, N_t * P \tag{1.2}$$

where W_d = wiring demand
N_t = number of I/Os
P = pitch between packages

1.6.3 Special Metrics for Direct Chip Attach

The assembly of uncased or bare chips on substrates has become popular mostly due to the ability of such assemblies to reduce the area of interconnections. The ideal limit for such assembly would be to place all the chips tightly together, without any space in between. This would result in 100 percent packaging efficiency, a metric measuring the ratio of silicon area to the substrate area. Naturally, such 100 percent efficiency is not achievable, but this metric is still useful in ranking various substrate construction or bare chip attachment methods, as shown in Fig. 1.5.

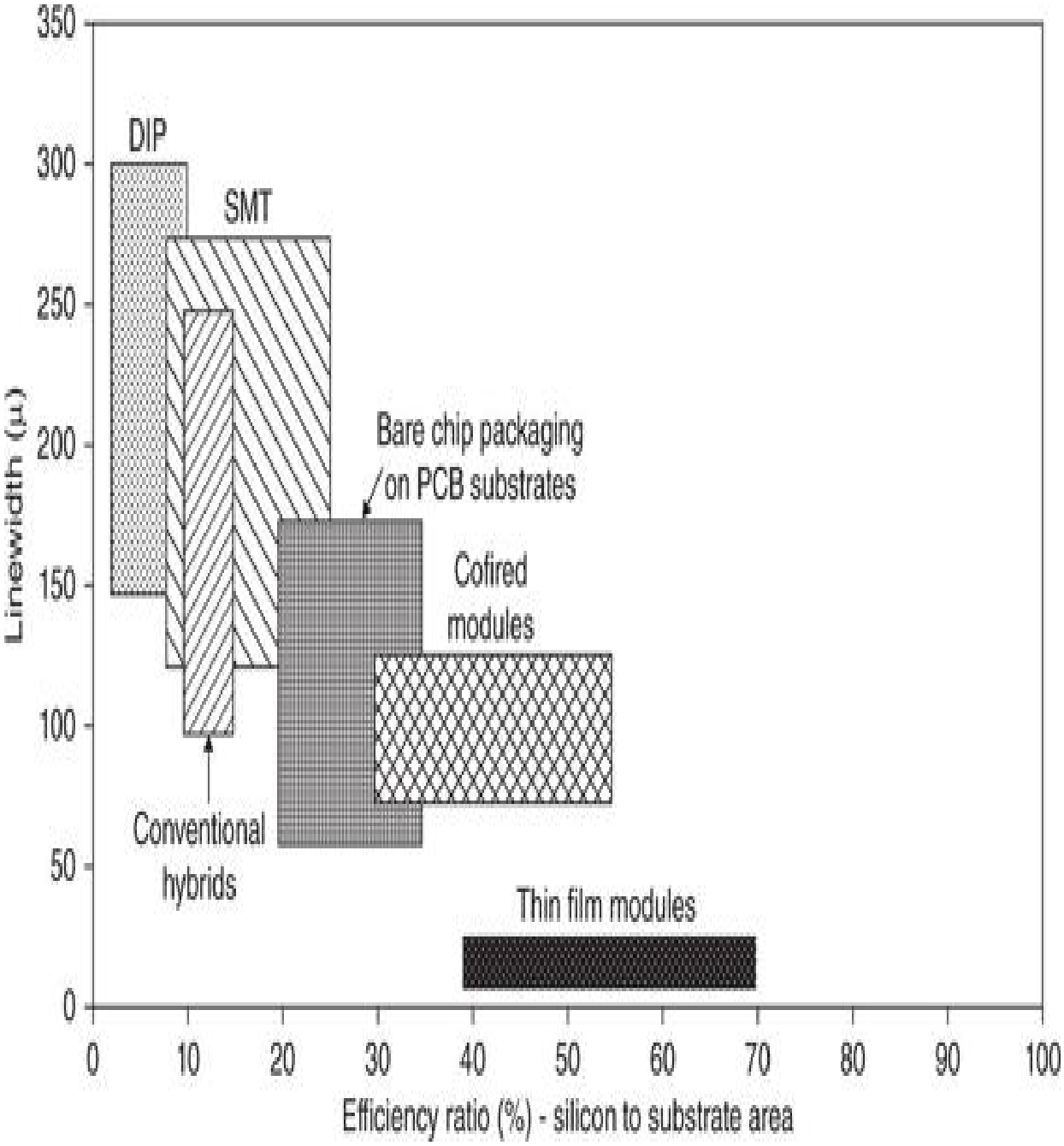

FIGURE 1.5 Packaging efficiency. (*Courtesy of BPA, used with permission*.)

Packaging efficiency of 100 percent is impossible to achieve because all chip-mounting methods require some space around the chips. Even with flip-chips, there must be a distance left between the chips to permit room for the placement tool.

Dr. H. Charles[6] of Johns Hopkins University has listed the dimensions in Table 1.2 for the necessary spacing between the chips (or the total width of the frame around the chips) for various chip attachment methods. These or very similar distances have also been cited by a number of other sources.

TABLE 1.2 Spacing Required between Chips

Attachment Method	Chip Spacing, mils
Flip-chip	15–20
Wire-bonding	70–80
Flip TAB	100–120
Regular TAB	150–400

Even with the flip-chip mounting, packaging efficiency must be derated to about 90 percent, for wire-bonding to 70 percent and for TABs to about 50 percent, and in some cases much more. A very similar situation is shown graphically in Fig. 1.6. The packaging efficiency deratings, shown in Fig. 1.6, are required to accommodate only the wiring bond pads on the substrates. But the mounting of bare chips on PWBs requires additional signal redistribution area to permit placement of larger-diameter PTHs farther out for communication with internal layers. It is evident that the packaging efficiencies on PWBs could be reduced to the range of only 20 to 30 percent, unless special surface signal redistribution layers (as previously mentioned) are used, which are made of unreinforced dielectric material. In such cases, packaging efficiency and the chip-to-chip distances will again be similar to the values cited in Table 1.2.

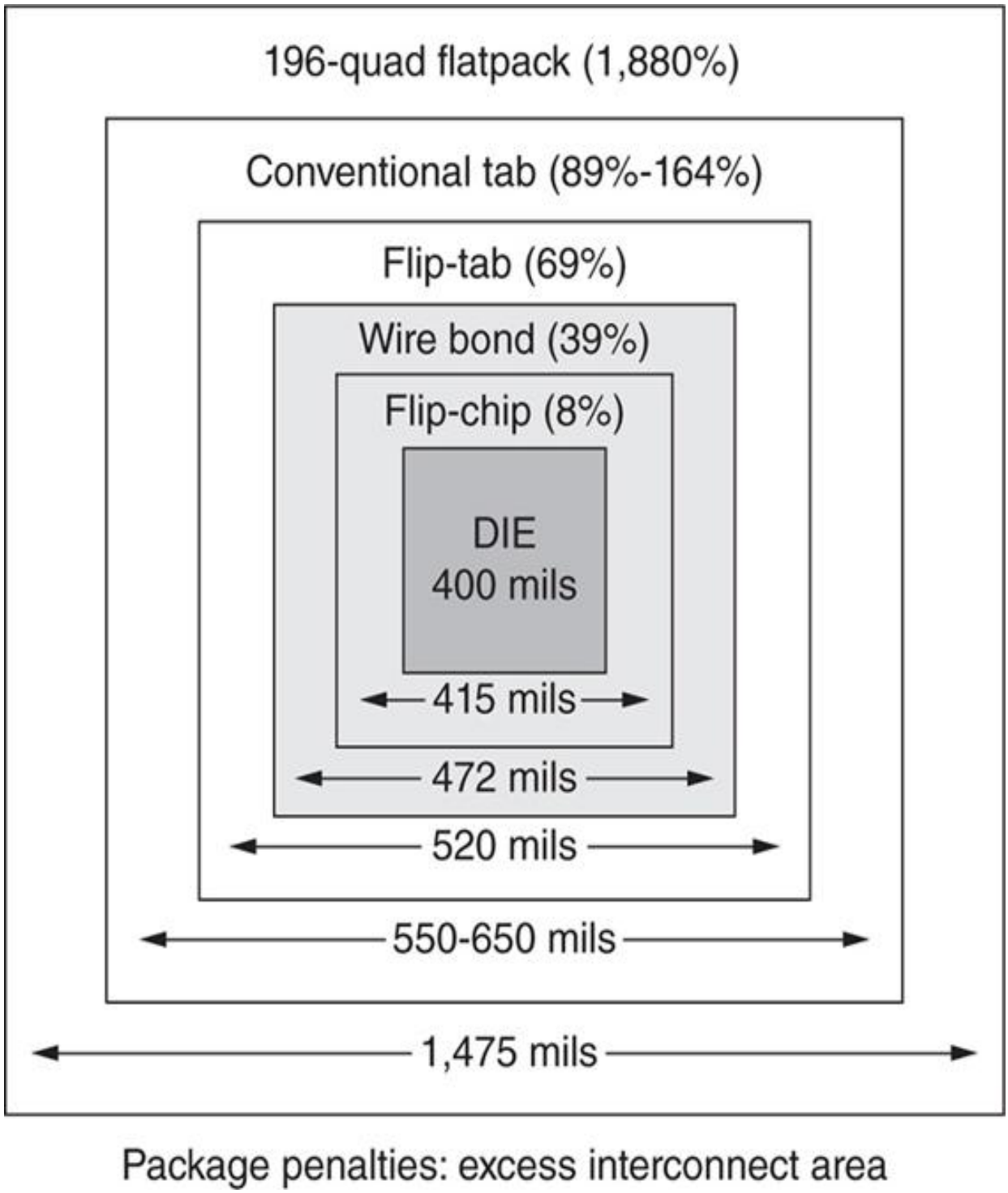

FIGURE 1.6 Chip area required to accommodate bonding methods.

It is apparent that direct chip attach on PWBs will result in the significant reduction of the packaging efficiency of such assemblies, except for the fact that components can be

mounted on both sides of the PWB substrate. It has been shown that wire-bonding can be done on both sides of a PWB with some special fixturing; also, outer lead bonding (OLB) of TABs can be done on both sides of the PWB substrate. Thus, while single-sided bare chip assembly on PWBs reduces its packaging efficiency to about half that of other types of substrate constructions, the ability to place components on both sides of PWBs brings it back to the same packaging efficiency level as others.

1.7 METHODS TO INCREASE PWB DENSITY

There are four basic ways to increase the connectivity or available conductor capacity of PWBs[7]:

- Reduce hole and pad diameters
- Increase the number of conductive channels between pads by reducing the widths of the conductors
- Increase the number of signal planes
- Add blind or buried via structures

The effect of each approach on manufacturing yields, and thus on board costs, will be discussed in sequence. It should be noted that the last option is the simplest but the most costly solution, and thus should be used only after the methods suitable for resolving the first two conditions have been proven inadequate for achieving the desirable board density.

1.7.1 Effect of Pads on Wiring Density

The major obstacles preventing increase of conductor channel capacity are large pad diameters around the plated through-holes (PTHs), since, at the present state of technology, PWBs still require pads wider than the conductors at their location. These pads reduce the obtainable connectivity of PWB boards and must be accounted for in a proper analysis of interconnection density I_d. For instance, in one design, the reduction of pad diameters from 55 to 25 mils (by 55 percent) doubled the interconnection density, while the reduction in conductor pitch C_p from 18 to 7 mils (by 61 percent) increased it only by 50 percent. It is obvious that the reduction of pad diameters, or their total elimination, could be a more efficient way to increase the wiring capacity of complex PWBs.

The purpose of copper pads surrounding the drilled holes in PWBs is to accommodate any potential layer-to-layer or pattern-to-hole misregistrations and thus prevent any hole breakout outside the copper area of the pads. This misregistration is caused mainly by the instability and movement of the base laminate during its processing through the PWB or multilayer board (MLB) manufacturing steps.

The base material standards specify that such movement be limited to a maximum of 300 ppm, but the actual base material excursions are closer to 500 ppm, producing 10 mils of layer movement within a 20-in distance. For many applications this tolerance is too wide, as it requires at least a 10-mil-wide annular ring around drilled holes, resulting in considerable conductor channel blockage.

Another cause of material instability in MLBs is the excessive material movement that occurs if the laminating temperature exceeds the glass transition temperature T_g of the laminate resin. On the other hand, if the laminating temperature remains below the T_g of the resin, there is

minimal dimensional variation of the base material, as the resin is still in its linear expansion phase. This explains the need for use of high-T_g resins in the PWB industry.

The data obtained from the performance of new, more stable unidirectional laminates indicate that the base material movement is reduced, for instance to 200 from 500 ppm, and the requirements for the annular ring width will be reduced to 4 from 10 mils.

Table 1.4 illustrates the connectivity gains made possible when a more stable laminate material is used, permitting a reduction in the initial diameters of the pads (as given in the first column) spaced at 1.5 mm (0.100 in) while keeping the conductor pitches constant. The most effective use of the signal plane area is achieved when the pads are eliminated and the *z*-axis interconnects are confined within the width of the conductors forming the invisible vias.

This derivation is based on actual data obtained from the performance of new, more stable, unidirectional laminates. While MLBs using these new, more dimensionally stable, unidirectional laminates with reduced pad diameters could be manufactured by conventional manufacturing methods, the production of MLBs with invisible vias requires the use of a sequential manufacturing process similar to the SLC process previously described.

PWB manufacturers are reasonably comfortable with the production of boards with 4- or 5-mil-wide conductors, but they still require large pads around plated holes to ensure against hole breakout. This limits the currently available wiring density to about 40 to 60 in/in^2 per plane, as seen from Table 1.3. A technology that will permit PWB manufacturers to fabricate invisible vias could increase the connectivity per PWB signal plane from this current range to the level of 100 to 140 in/in^2. Conductor widths of 0.002 in will offer a PWB of 200 to 250 in/in^2 per signal plane.

TABLE 1.3 Effect of Pad Diameters on Interconnectivity Density

Pad dia, in	Cond Pitch, in	I_d @ 500 ppm, in/in^2	I_d @ 200 ppm, in/in^2	I_d @ Invisible via, in/in^2
0.055	0.010	20	37	55
0.036	0.018	30	48	55
0.025	0.009	40	96	100
0.025	0.007	60	130	143

Table 1.4 illustrates the most important result of increased connectivity per layer: a reduction in the number of signal layers needed to provide the same wiring density W_d. Table 1.4 was constructed by applying connectivity data from Table 1.3 to a 50-in^2 MLB with total wiring length of 10,000 in. Note also that the layer count in Table 1.3 has been brought up to the next higher full-layer value, that is, the calculated 1.4 layers have been recorded as 2 layers.

TABLE 1.4 Effect of Increased Connectivity on Reduction of Layers

Pad dia, in	Cond Pitch, in	I_d @ 500 ppm, layers	I_d @ 200 ppm, layers	I_d @ Invisible via, layers
0.055	0.010	10	6	4
0.036	0.018	7	4	4
0.025	0.009	5	2	2
0.025	0.007	4	2	2

The major benefit of such a reduction in the layer count is that it can result in a significant reduction of the manufacturing cost while providing the same total interconnection length.

1.7.2 Reduction of Conductor Width

An obvious method of increasing the connectivity of PWBs is to reduce the widths of conductors and spaces and thus increase the number of available wiring channels on each signal plane, as described previously. This is the direction that has been used in the IC and PWB industries for many years. However, it is impossible to decrease conductor widths or spaces indefinitely. The reduction of the conductor width is limited by the current-carrying capacity of thin, small conductors, especially when these conductors are long, as they frequently are on PWBs. There are processing limits to this conductor reduction, since manufacturing yields may plummet if the reduction stretches the process capabilities beyond their normal limits.

There is also a limit to the reduction of the spaces between the conductors, governed mainly by electrical considerations, that is, by the need to prevent excessive cross talk, to minimize noise, and to provide proper signal propagation conditions and characteristic impedance.

Still, such conductor reductions, if achieved within the described limits, can be an effective path for increasing the PWB density and the reduction of PWB manufacturing costs. As seen from Table 1.5, constructed from cost data derived from the Columbus program of BPA, the reduction of conductor widths from 6 to 3 mils halves the number of signal layers necessary to ensure the same connectivity (while their yields, interconnection density, and board area were kept constant). This reduction in the number of layers

can significantly reduce the manufacturing costs of PWB boards.

TABLE 1.5 Effect of Conductor Widths on Number of Layers and Board Cost for a 6-in × 8-in MLB, with I_d = 450 in/in^2, 65 to 68 Percent Yields

Line-Space	Total No. of Layers	No. of Signal Layers	Board Cost, %
3–3	8	4	55
4–4	10	6	64
5–6	12	7	77
5–7	14	8	87
6–6	16	8	90
7–8	20	10	100

1.7.3 Effect of Conductor Widths on Board Yields

It is obvious that any successful increase of conductor density I_d in PWBs would be effective only if the processes exist that permit manufacture with reasonable yields. Unfortunately, the yields of thin conductors in PWBs fall rapidly as their widths are reduced below 5 mils, as shown in Fig. 1.7. Therefore, the understanding of manufacturing yields is very important for analysis of the most cost-effective manufacturing process, because the process yields have a major effect on the cost of interconnection substrates.

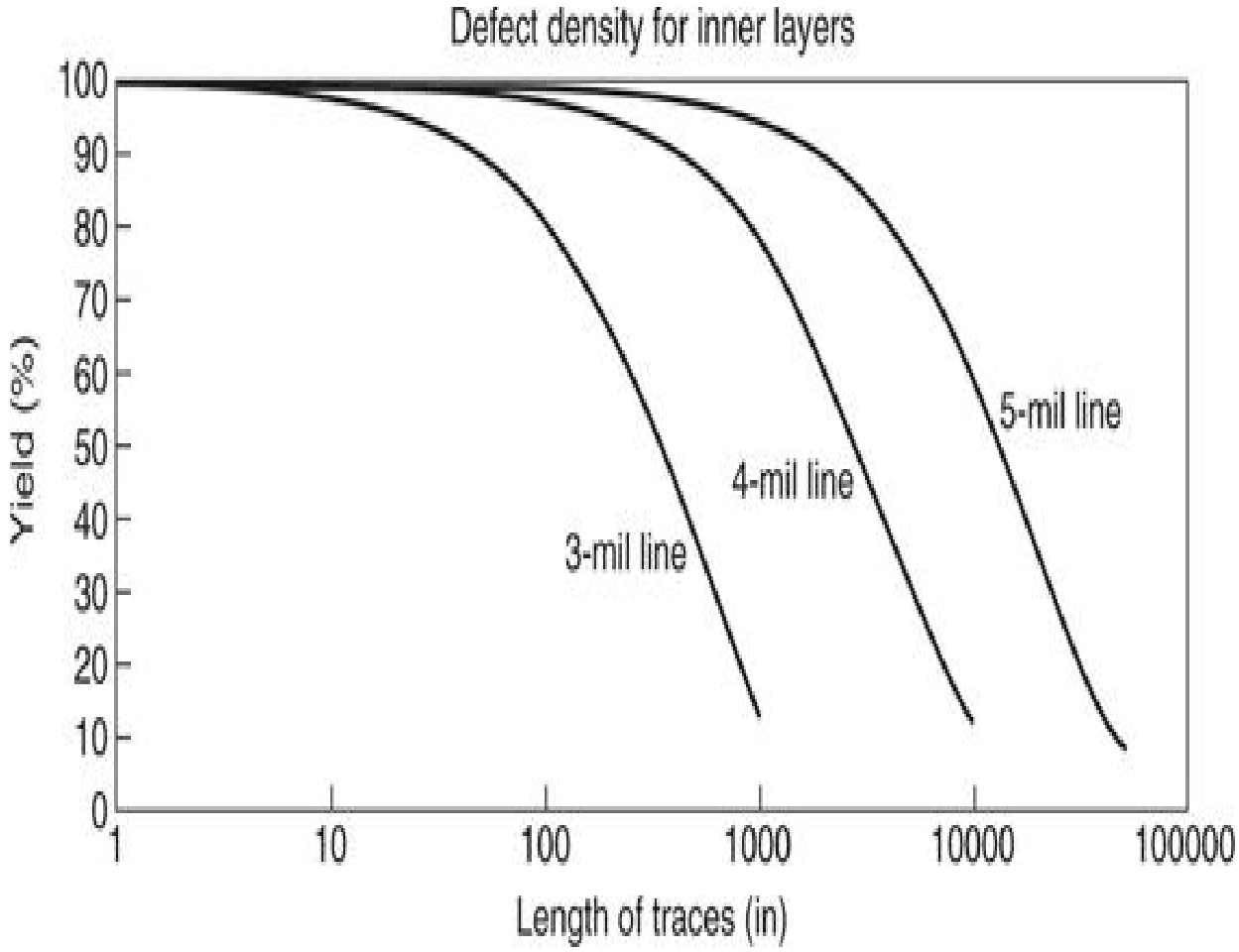

FIGURE 1.7 Board yields versus conductor width.

A useful empirical equation for calculating the manufacturing cost is

$$\text{Cost } C = \frac{(\text{material} + \text{process cost})}{\text{yield } Y} \tag{1.3}$$

To establish the effect of the interconnection density I_d on the final yield of substrates, the total processing yield can be split into two components: one that depends on the conductor density, that is, Y_{Id}, and the second, which is a function of the combined yields of the rest of the manufacturing processes:

$$Y_{\text{total}} = Y_{ld} * Y_{\text{proc}} \tag{1.4}$$

In a well-controlled manufacturing operation, the process-dependent yields (such as plating) remain fairly constant for a given technology, permitting the yield function to be based solely on the changes in the conductor widths.

As seen from Fig. 1.8, the defects that affect this density-dependent yield function Y_{ld} are conductor opens and shorts between them. It would be reasonable to assume that such defects have a Poisson distribution over the total length TL of conductors of a substrate, with an average defect frequency of v. The yield is the probability of zero defects ($n = 0$) in the total conductor length TL. Thus,

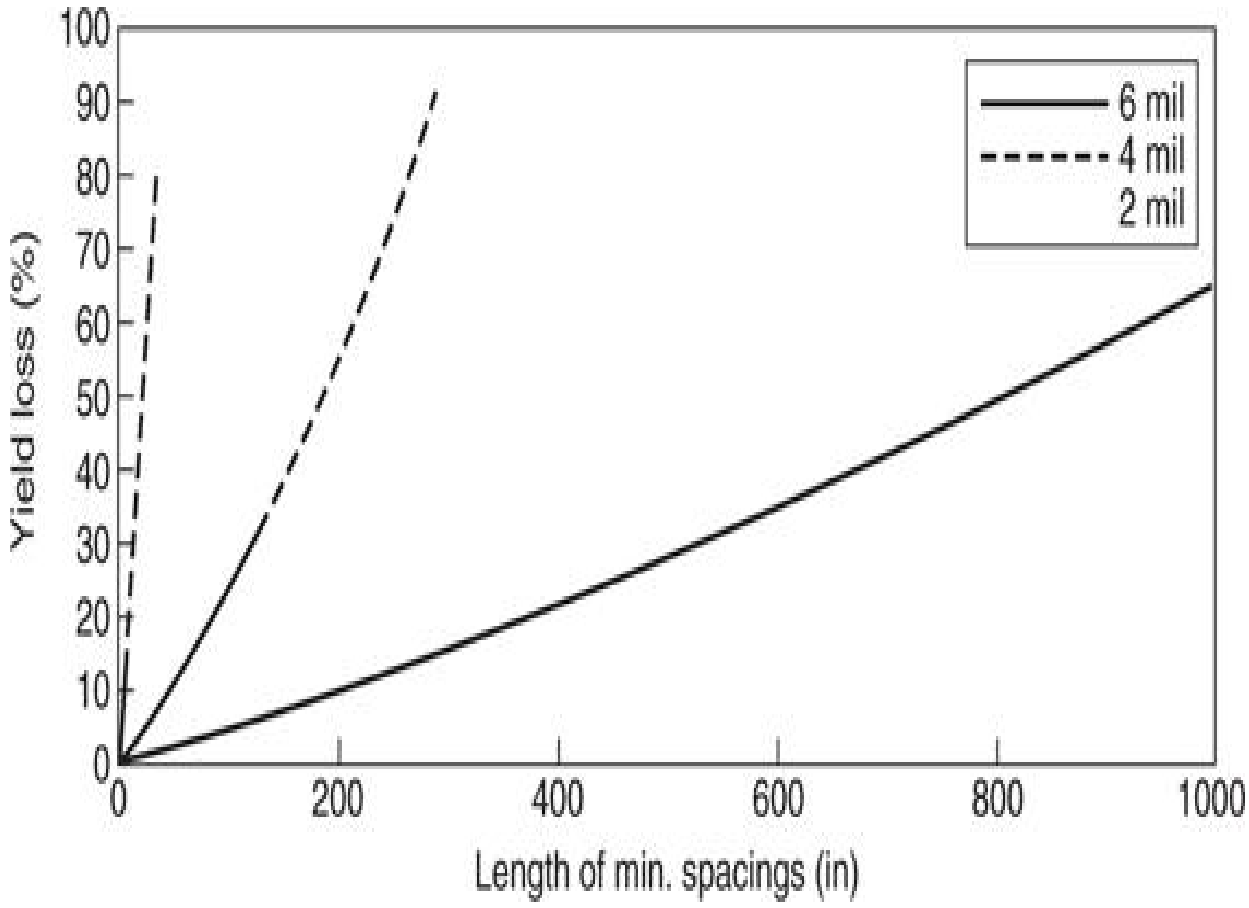

FIGURE 1.8 Yield loss from shorts.

$$Y = (\text{at } n = 0) = e^{(-\nu * \text{TL})} \text{ (Poisson distribution)} \quad (1.5)$$

As seen from Figs. 1.7 and 1.8, the defect frequency ν depends also on the widths of lines and spaces, that is, on the conductor pitch C_p. With a decrease of C_p, ν will increase, but for very large C_p, ν should be 0, since Y_{ld} will be 100 percent.

For instance, in the case of a design using invisible pads, where $C_p = 2w$, the interconnection density I_d can be expressed as I_d = TL/A, and I_d is proportional to C_p, that is, $I_d * C_p = 1$, and TL = A/C_p. Therefore, ν in this equation can be empirically expressed as:

$$\nu = -\ln \frac{Y_0}{\text{TL}_0} * \left(\frac{C_{p0}}{C_p} \right)^b \quad (1.6)$$

where b is an exponent dependent on the technology or process used to form the conductors. This exponent b varies considerably from facility to facility and among various pattern formation methods, and must be empirically determined for each case.

1.7.4 Increase in Number of Conductor Layers

This is the simplest and most straightforward solution: when there is insufficient room on existing layers to place all the necessary interconnecting paths, add a layer. This approach has been widely practiced in the past, but when cost effectiveness of the substrates is of paramount importance, a very careful design analysis must be made to minimize layer counts in MLBs, because there is a significant cost

increase with every additional layer in the board. As seen from Table 1.5, calculated for 6-in × 8-in MLBs produced in large quantity with yields and conductor density kept constant, there is almost a linear relationship between board costs and layer count.

Table 1.5 also shows that any increase in the number of signal layers in boards operating at frequencies requiring transmission line characteristics will double the total number of layers, due to the need to interleave ground or DC power planes between signal planes.

A typical example of the effect of layer count on the finished MLB yield can be seen from Fig. 1.9, prepared some years ago by BPA. We can see that there is a definite decrease in the manufacturing yields with an increased number of layers in any of the line width categories. This is rather a typical situation in board manufacturing because increased complexity and thickness of MLB with a higher number of layers usually leads to a larger number of problems on the production floor.

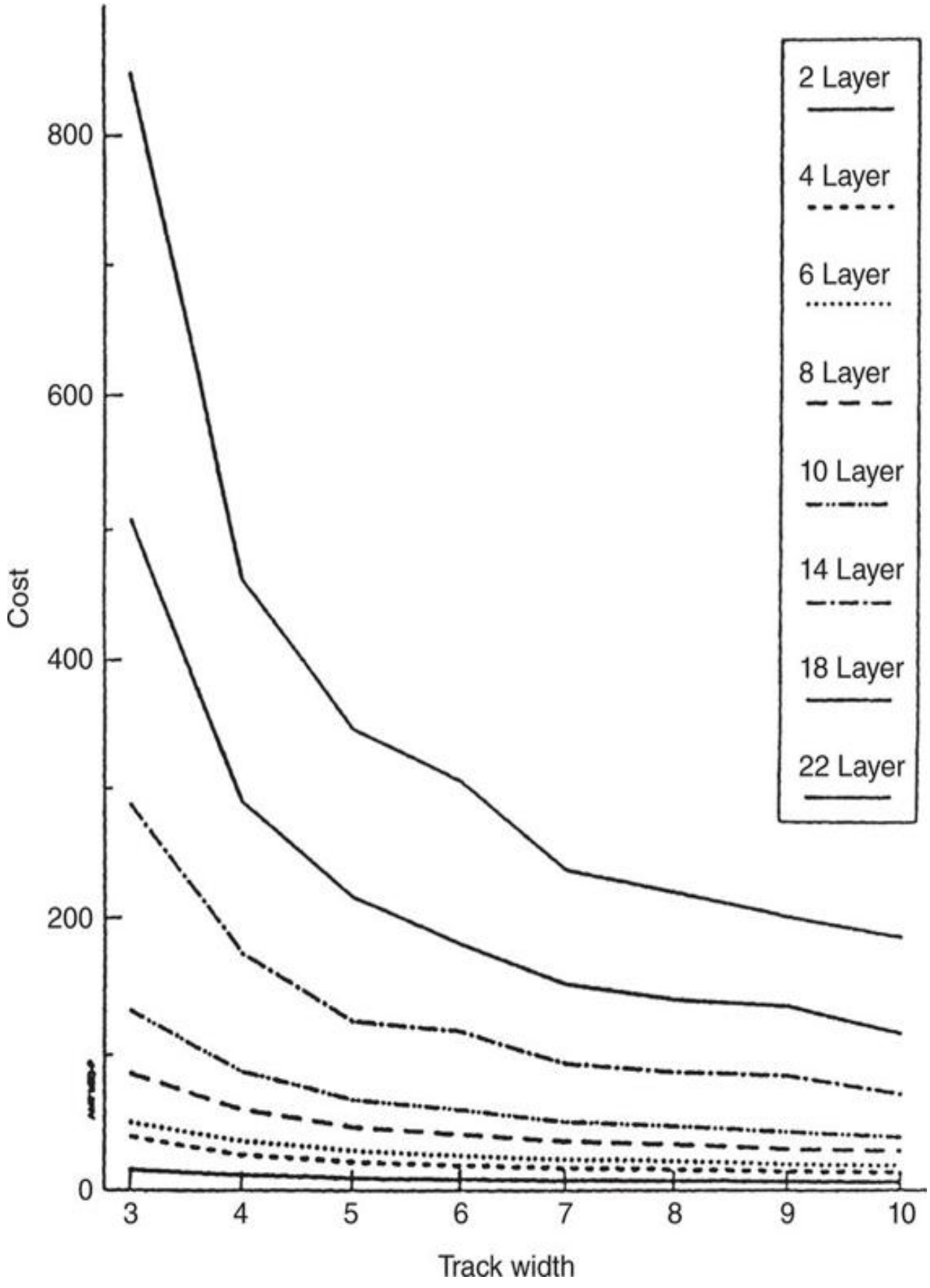
2 Layer
4 Layer
6 Layer
8 Layer
10 Layer
14 Layer
18 Layer
22 Layer
800
600
400
200
0
Cost
3
4
5
6
7
8
9
10
Track width

FIGURE 1.9 Cost relationships between number of layers and conductor widths.

1.7.5 Add Blind or Buried via Structures

By adding blind or buried vias to a board, additional routing channels and routing space can be achieved. Later chapters will detail more on blind and buried vias, especially the small vias called "*microvias*" or HDI technologies[8].

1.8 REFERENCES

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7. G. Messner, "Analysis of the Density and Yield Relationships Leading Toward the Optimal Interconnection Methods," *Proceedings of Printed Circuits World Conference VI*, San Francisco, CA, May 1993, pp. M 19 1–20.
8. Y. Tsukada et al., "A Novel Solution for MCM-L Utilizing Surface Laminar Circuit and Flip Chip Attach Technology," *Proceedings of the 2d International Conference on Multichip Modules*, Denver, CO, April 1993, pp. 252–259.

[a] Adapted from “Electronic Packaging and Interconnectivity,” by Clyde F. Coombs, Jr., Chap. 1 in *Printed Circuits Handbook*, 4th ed. (McGraw-Hill, New York, 1996).

CHAPTER 2

TYPES OF PRINTED WIRING BOARDS

Hayao Nakahara
N.T. Information Ltd., Huntington, New York

2.1 INTRODUCTION

Since the invention of printed wiring technology by Dr. Paul Eisner in 1936, several methods and processes have been developed for manufacturing printed wiring board (PWBs) of various types. Most of these have not changed significantly over the years; however, some specific trends continue to exert major influences on the types of PWBs required and the processes that create them:

1. Computers and portable telecommunications equipment require higher-frequency circuits, boards, and materials, and also use more functional components that generate considerable amounts of heat that need to be extracted.
2. Consumer products have incorporated digital products into their design, requiring more functionality at ever-lower total cost.

3. Products for all uses continue to get smaller and more functional, driving the total circuit package itself to become more dense, causing the PWBs to evolve to meet these needs.

These trends have led to the larger use of nonorganic base substrates, such as aluminum and soft iron. In addition, alternate ways to create boards have been developed. These will be discussed in this chapter, along with the traditional board structures and processes. The terms *printed wiring board, PWB*, and *board* will be used synonymously. Also, the words *laminate, substrate*, and *panel* will be used interchangeably.

2.2 CLASSIFICATION OF PRINTED WIRING BOARDS

PWBs may be classified in many different ways according to their various attributes. One fundamental structure common to all of them is that they must provide electrical conductor paths which interconnect components to be mounted on them.

2.2.1 Basic PWB Classifications

There are two basic ways to form these conductors:

1. *Subtractive:* In the subtractive process, the unwanted portion of the copper foil on the base substrate is etched away, leaving the desired conductor pattern in place.
2. *Additive:* In the additive process, formation of the conductor pattern is accomplished by adding copper to a bare (no copper foil) substrate in the pattern and places desired. This can be done by plating copper, screening

conductive paste, or laying down insulating wire onto the substrate on the predetermined conductor paths.

The PWB classifications given in Fig. 2.1 take into consideration all these factors, i.e., fabrication processes as well as substrate material. The use of this figure is as follows:

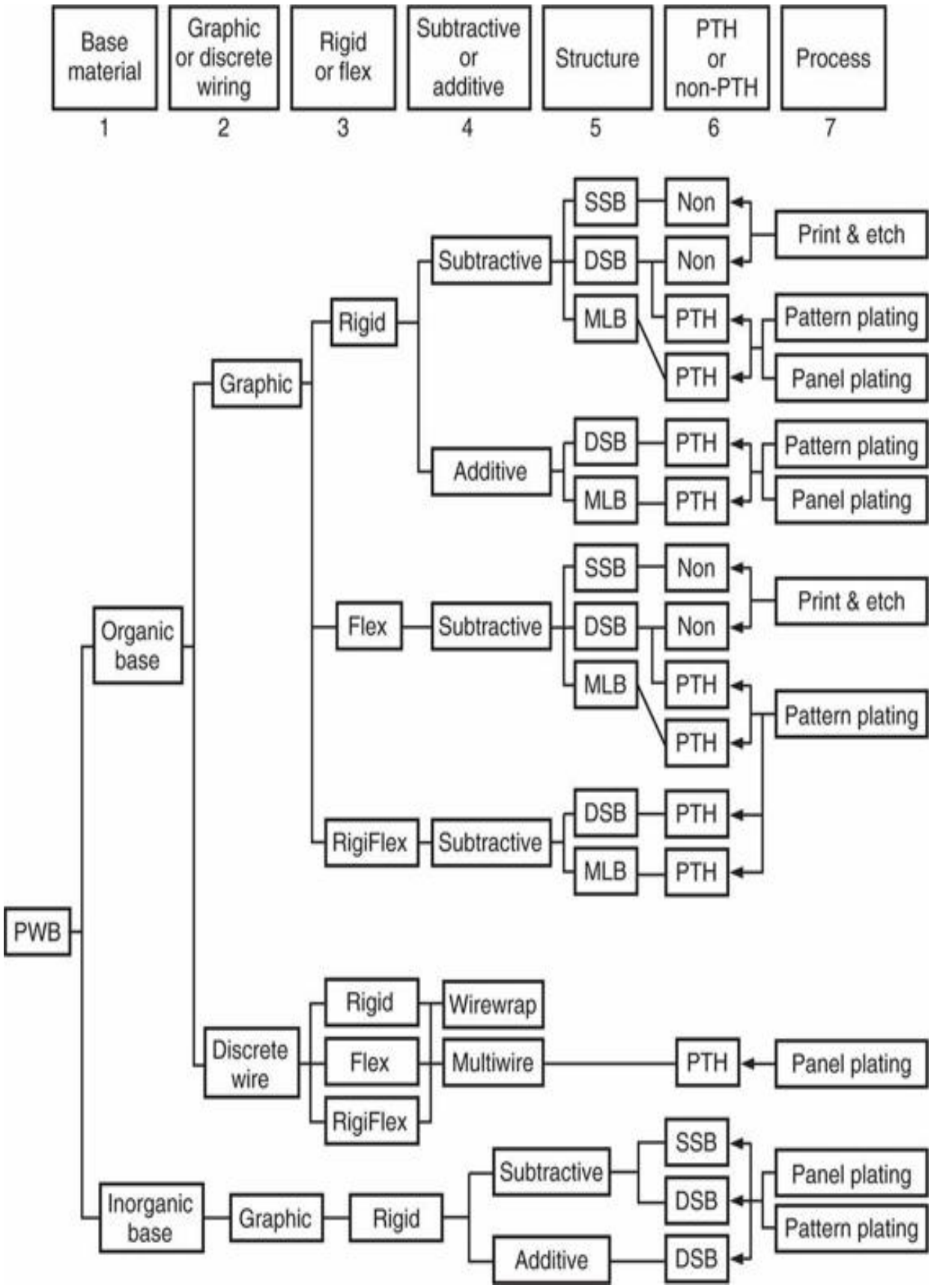

Base material
1
Graphic or discrete wiring
2
Rigid or flex
3
Subtractive or additive
4
Structure
5
PTH or non-PTH
6
Process
7
PWB
Organic base
Graphic
Rigid
Subtractive
SSB
Non
DSB
Non
MLB
PTH
PTH
Print & etch
Pattern plating
Panel plating
Additive
DSB
PTH
MLB
PTH
Pattern plating
Panel plating
Flex
Subtractive
SSB
Non
DSB
Non
MLB
PTH
PTH
Print & etch
Pattern plating
RigiFlex
Subtractive
DSB
PTH
MLB
PTH
Discrete wire
Rigid
Flex
RigiFlex
Wirewrap
Multiwire
PTH
Panel plating
Inorganic base
Graphic
Rigid
Subtractive
SSB
DSB
Additive
DSB
Panel plating
Pattern plating

FIGURE 2.1 Classification of printed wiring boards.

- Column 1 shows the classification of PWBs by the nature of their substrate.
- Column 2 shows the classification of PWBs by the way the conductor pattern is imaged.
- Column 3 shows the classification of PWBs by their physical nature.
- Column 4 shows the classification of PWBs by the method of actual conductor formation.
- Column 5 shows the classification of PWBs by the number of conductor layers.
- Column 6 shows the classification of PWBs by the existence or absence of plated-through-holes (PTHs).
- Column 7 shows the classification of PWBs by production method.

2.3 ORGANIC AND NONORGANIC SUBSTRATES

One of the major issues that has arisen with the ever-higher speed and functionality of components used in computers and telecommunications is the availability of materials for the PWB substrate that are compatible with these product and process needs. This includes the stresses on substrate material created by more and longer exposure to soldering temperatures during the assembly process, as well as the need to match the coefficient of thermal expansion for components and substrate. The resultant search has found new materials, both organic and nonorganic based. The details of these materials are explained in Chaps. 6 through 11, but this outlines the basic character of the two types of substrate.

2.3.1 Organic Substrates

Organic substrates consist of layers of paper impregnated with phenolic resin or layers of woven or nonwoven glass cloth impregnated with epoxy resin, polyimide, cyanate ester, BT resin, etc. The usage of these substrates depends on the physical characteristics required by the application of the PWB, such as operating temperature, frequency, or mechanical strength.

2.3.2 Nonorganic Substrates

Nonorganic substrates consist mainly of ceramic and metallic materials such as aluminum, soft iron, and copper-invar-copper. The usage of these substrates is usually dictated by the need of heat dissipation, except for the case of soft iron, which provides the flux path for flexible disk motor drives.

2.4 GRAPHICAL AND DISCRETE-WIRE BOARDS

Printed wiring boards may be classified into two basic categories, based on the way they are manufactured:

1. Graphical
2. Discrete-wire

2.4.1 Graphical Interconnection Board

A *graphical PWB* is the standard PWB and the type that is usually thought of when PWBs are discussed. In this case, the image of the master circuit pattern is formed photographically on a photosensitive material, such as treated glass plate or plastic film. The image is then transferred to the circuit board by screening or photoprinting the artwork generated from the master. Due to the speed and economy of making master artwork by laser plotters, this master can also be the working artwork.

Direct laser imaging of the resist on the PWB can also be used. In this case, the conductor image is made by the laser plotter, on the photoresistive material, which is laminated to the board, without going through the intermediate step of creating a phototool. This tends to be somewhat slower than using working artwork as the tool and is not generally applied to mass production. Work continues on faster resists, as well as exposure systems, and this method will undoubtedly continue to emerge.

2.4.2 Discrete-Wire Boards

Discrete-wire boards do not involve an imaging process for the formation of signal conductors. Rather, conductors are formed directly onto the wiring board with insulated copper wire. Wire-wrap® and Multiwire® are the best known discrete-wire interconnection technologies. Because of the allowance of wire crossings, a single layer of wiring can match multiple conductor layers in the graphically produced boards, thus offering very high wiring density. However, the wiring process is sequential in nature and the productivity of discrete-wiring technology is not suitable for mass production. Despite this weakness, discrete-wiring boards are in use for some very high density packaging applications. See Fig. 2.2 for an example of a discrete-wiring board.

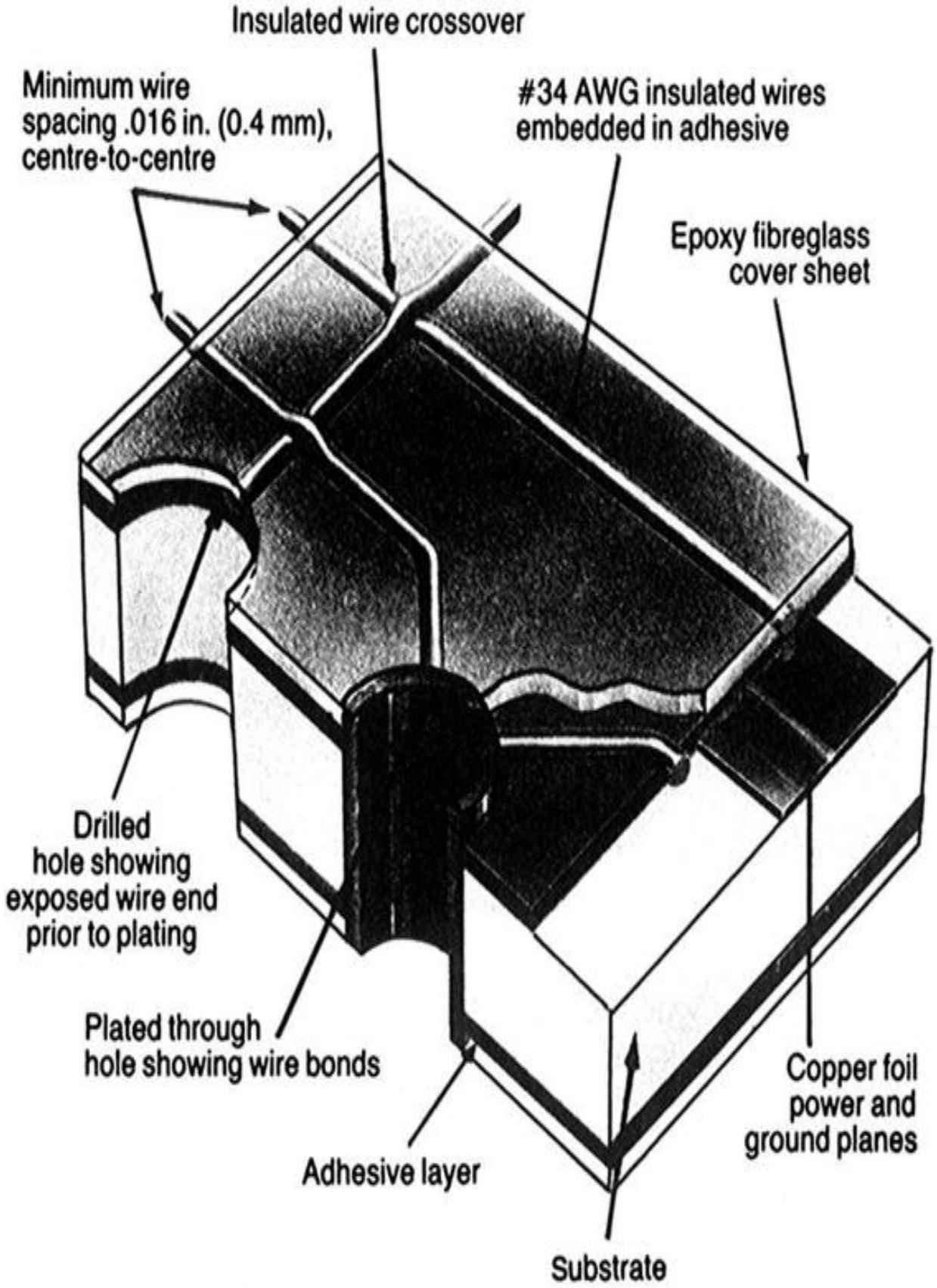

Insulated wire crossover
Minimum wire spacing .016 in. (0.4 mm), centre-to-centre
#34 AWG insulated wires embedded in adhesive
Epoxy fibreglass cover sheet
Drilled hole showing exposed wire end prior to plating
Plated through hole showing wire bonds
Adhesive layer
Substrate
Copper foil power and ground planes

FIGURE 2.2 Example of discrete-wiring board.

2.5 RIGID AND FLEXIBLE BOARDS

Another class of boards is made up of the *rigid* and *flexible* PWBs. Whereas boards are made of a variety of materials, flexible boards generally are made of polyester and polyimide bases. *Rigi-flex boards*, a combination of rigid and flexible boards usually bonded together, have gained wide use in electronic packaging (see Fig. 2.3). Most rigi-flex boards are three-dimensional structures that have flexible parts connecting the rigid boards, which usually support components; this packaging is thus volumetrically efficient.

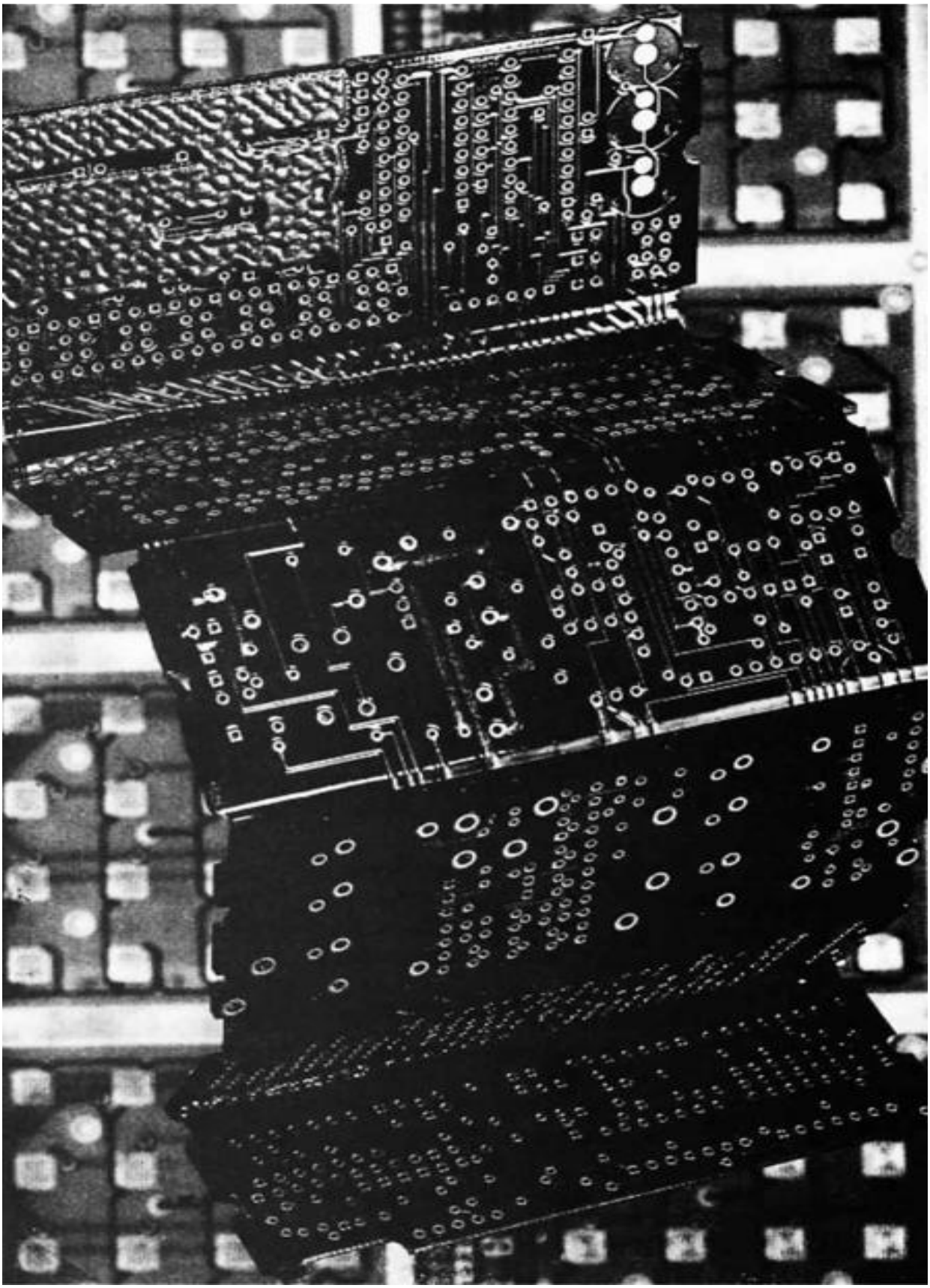


FIGURE 2.3 Rigi-flex printed wiring board.

2.6 GRAPHICALLY PRODUCED BOARDS

The majority of boards produced in the world are graphically produced. There are three alternative types:

1. Single-sided boards
2. Double-sided boards
3. Multilayer boards

2.6.1 Single-Sided Boards

Single-sided boards (SSBs) have circuitry on only one side of the board and are often referred to as print-and-etch boards because the etch resist is usually printed on by screen-printing techniques and the conductor pattern is them formed by chemically etching the exposed, and unwanted, copper foil.

2.6.1.1 Typical Single-Sided Board Materials. This method of board fabrication is generally used for low-cost, high-volume, and relatively low functionality boards. In the Far East, for example, the majority of SSBs are made of paper-based substrates for lowest cost, with the most popular grade of paper-based laminate being XPC-FR, which is a flame-retardant phenolic material that is also highly punchable. In Europe, FR-2 grade paper laminate is the most popular substrate for SSBs because it emits less odor than XPC-FR when placed in high-voltage, high-temperature environments, such as inside a television set chassis. In the United States, CEM-1 material, which is a composite of paper and glass impregnated with epoxy resin, is the most popular

substrate for SSBs. While not as low cost as XPC-FR or FR-2, CEM-1 has gained popularity because of its mechanical strength and also because of the relative unavailability of paper phenolic laminates.

2.6.1.2 Single-Sided Board Fabrication Process.

Given the emphasis on cost and low complexity, SSBs are generally produced in highly automated, conveyorized print-and-etch lines, using the following basic process flow.

Step 1: Cut substrate into appropriate panel size by either sawing or shearing.

Step 2: Place panel in loader which feeds them into the line.

Step 3: Clean panels.

Step 4: Screen panel with ultraviolet curable etch-resist ink.

Step 5: Cure the etch-resist ink.

Step 6: Etch exposed copper.

Step 7: Strip the resist.

Step 8: Apply solder resist.

Step 9: Screen legend.

Step 10: Form holes by drilling or punching.

Step 11: Test for shorts and opens.

The conveyor speed of automated print-and-etch lines ranges from 30 to 45 ft/min. Some lines are equipped with an online optical inspection which enables the elimination of the final electrical open/short test.

As previously noted, after the conductor pattern is generated in the print-and-etch line, holes for component insertion are formed on the panel by punching when the

panel is made of paper-based substrate, but must be formed by drilling when the panel is made of glass-based substrate.

2.6.1.3 Process Variations. In some variations, the conductor surface of the PWB gets insulated, exposing only pads, and then conductive paste is screened to form additional conductors on the same side of the board, thus forming double conductive layers on a single side.

Most metal-core PWB consumer applications are made of aluminum substrate, which comes as a copper-clad material. PWBs made of such material do not have through-holes, and components are usually surface-mount types. These circuits are frequently formed into three-dimensional shapes.

2.6.2 Double-Sided Boards

By definition, double-sided boards (DBs) have circuitry on both sides of the boards. They can be classified into two categories:

1. Without through-hole metallization
2. With through-hole metallization

The category of through-hole metallization can be further broken into two types:

1. Plated-through-hole (PTH)
2. Silver-through-hole (STH)

2.6.2.1 Plated-Through-Hole Technology. PTH technology is discussed in some detail in Sec. 2.7; however, some comments are appropriate here.

Metallization of holes by copper plating has been practiced since the mid-1950s. Since PWB substrate is an insulating material, and therefore nonconductive, holes must be metallized first before subsequent copper plating can take

place. The usual metallization procedure is to catalyze the holes with palladium catalyst followed by electroless copper plating. Then, thicker plating is done by galvanic plating. Alternately, electroless plating can be used to plate all the way to the desired thickness, which is called *additive plating*.

The biggest change in the manufacturing process of double-sided PTH boards, and also of multilayer boards (MLBs), is the use of *direct metallization* technologies. (See Chap. 34 for full discussion of electroless and direct metallization for through-hole boards.) Here, simply, it eliminates the electroless copper process. The hole wall is made conductive by palladium catalyst, carbon, or polymer conductive film, then copper is deposited by galvanic plating. The elimination of electroless copper, in turn, allows the elimination of environmentally hazardous chemicals, such as formaldehyde, and EDTA, which are two main components of electroless copper-plating solutions.

2.6.2.2 Silver-Through-Hole Technology. STH boards are usually made of paper phenolic materials or composite epoxy paper and glass materials, such as CE-1 or CE-3. After double-sided copper-clad materials are etched to form conductor patterns on both sides of the panel, holes are formed by drilling. Then the panel is screened with silver-filled conductive paste. Instead of silver, copper paste can also be used.

Since STHs have a relatively high electrical resistance compared with PTHs, the application of STH boards is limited. However, because of their economic advantage (the cost of STH boards is usually one-half to two-thirds that of functionally equivalent PTH boards), their application has spread to high-volume, low-cost products such as audio equipment, floppy disk controllers, car radios, remote controls, etc.

2.6.3 Multilayer Boards

By definition, multilayer boards (MLBs) have three or more circuit layers (see Fig. 2.4). Main applications of MLBs used to be confined to sophisticated industrial electronic products. Now, however, they are the mainstream of all electronic devices, including consumer products such as portable video cameras, cellular phones, and audio discs.

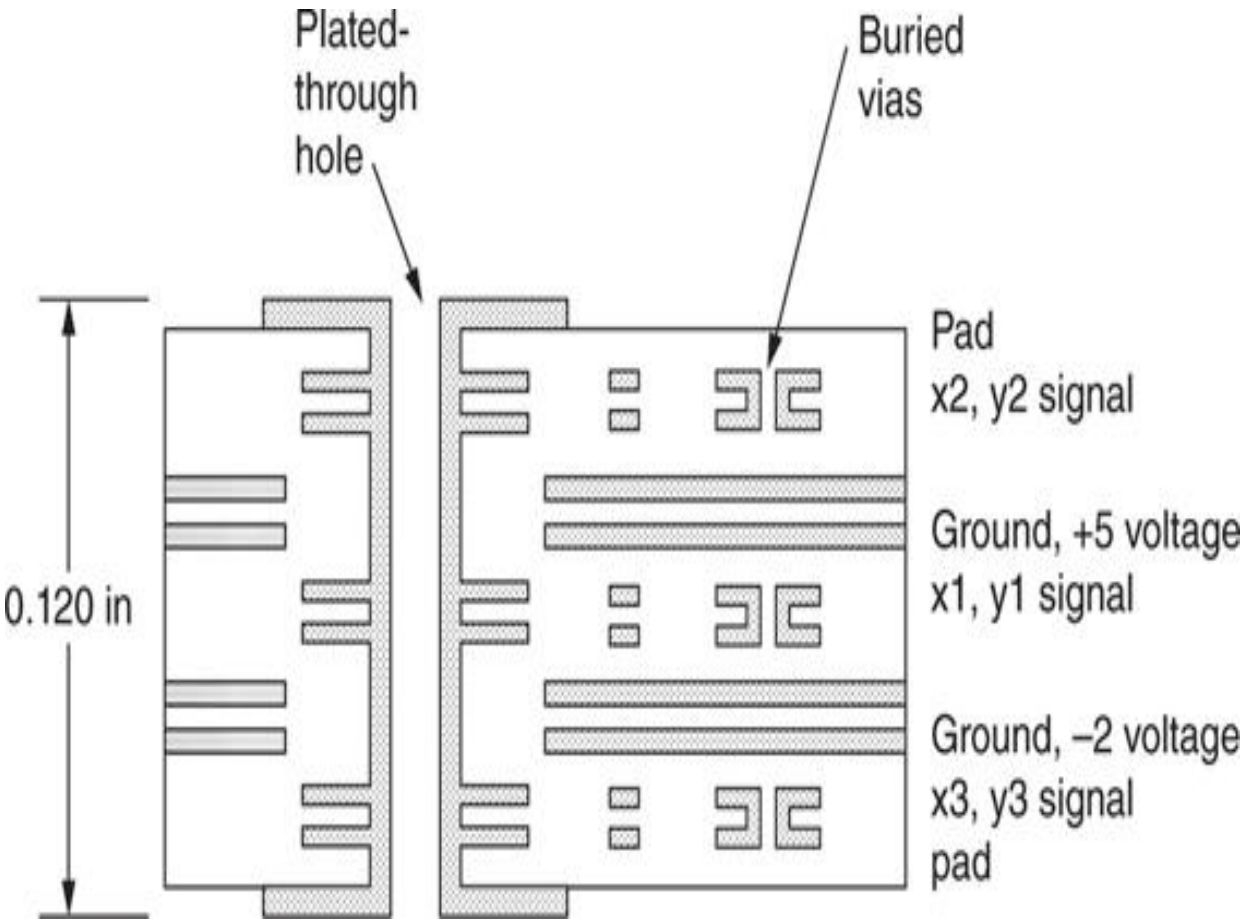


FIGURE 2.4 Cross-section multilayer board with buried via holes. Buried vias are built into each of the double-sided boards that make up the final multilayer structure.

2.6.3.1 Layer Count. As personal computers and workstations become more powerful, mainframe computers and supercomputers are being replaced in many applications by these smaller machines. As a result, the use of highly

sophisticated MLBs, which have layer counts over 70, are being reduced, but the technology to produce them is proven. At the other end of the layer-count spectrum, thin and high-density MLBs with layer counts between 4 and 8 are mainstream. The drive toward thinner MLBs will continue and is made possible by the continuing concurrent advancement of materials and equipment to handle thin core materials.

2.6.3.2 Via and Via Production Technologies. As PWBs have had to address the issues of higher speed, higher density, and the rise of surface-mount components that use both sides, the need to communicate between layers has increased dramatically. At the same time, the space available for vias has decreased, causing a continuing trend toward smaller holes, more holes on the board, and the decline of the use of holes that penetrate the entire board, which use space on all layers. As a result, the use of buried and blind vias has become a standard part of multilayer board technology, driven by the need for this increased package density (Fig. 2.4).

One of the immediate issues that arise from these trends is the problems of drilling and the associated cost of this fabrication step. Printed wiring boards, which once were stacked three high on a drilling machine, must be drilled individually, and the number of holes per board has risen, to accommodate the need for vias. This has caused a major problem for fabricators, who find that a lack of drilling capacity is creating a big demand on funds for additional machines, while the cost of drilling continues to increase dramatically. Therefore, alternate methods for creating vias are being developed. These pressures will be ongoing, and therefore the process listed here, or some equivalent, will undoubtedly become more important as the drive to miniaturization continues and drilling individual holes becomes less and less practical.

These processes have been developed to mass-produce vias without drills.

2.6.3.2.1 Surface Laminar Circuits (SLCs). The most notable MLB technology developed to form vias is the *sequential* fabrication of multilayers without press operations. This is particularly important for surface blind via holes.

The process for fabricating a board using surface laminar circuits is as follows (see Fig. 2.5):

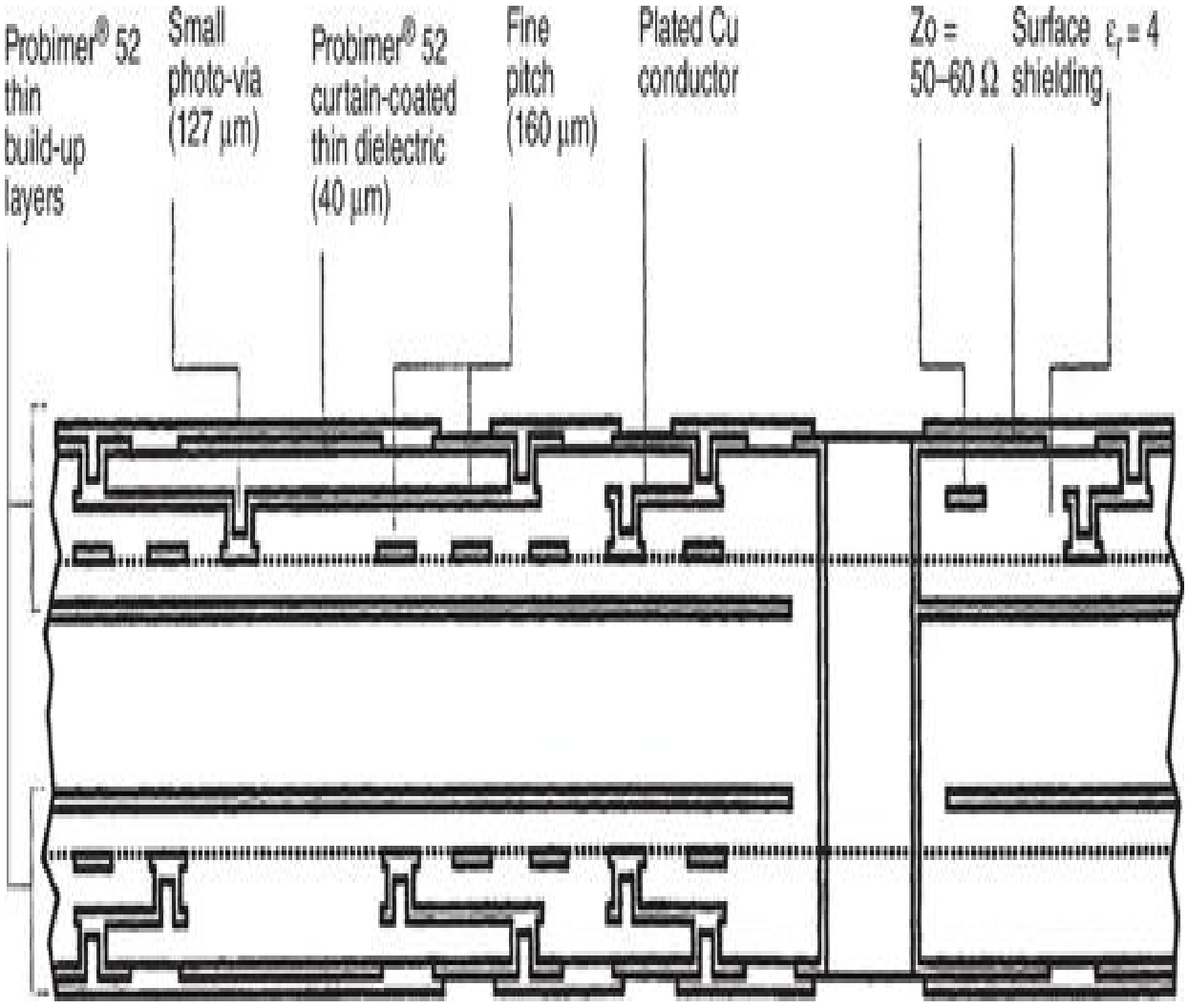


FIGURE 2.5 Example of surface laminar circuit (SLC) board cross section. (*Courtesy IBM Yasu and Ciba-Geigy Limited*.)

1. Innerlayer ground and power distribution patterns are formed.
2. Panel receives an oxide treatment.
3. Insulating photosensitive resin is coated over the panel by curtain or screen-coating methods.
4. Holes are formed by photoexposure and development.
5. Panel is metallized by usual copper reduction process (consisting of catalyzing and electroless copper plating or by direct metallization process).
6. Thicker deposition of copper is made by continuation of electroless copper plating or galvanic plating.
7. Circuit patterns are formed by dry film tenting process.

2.6.3.2.2 DYCOstrate®. A different approach to small via creation has been taken by Dyconex AG of Switzerland. After ground and power patterns are formed on the panel, and the panel is oxide-treated, polyimide-backed copper foil is laminated on the panel. Holes in the copper are formed by a chemical etching process, and the insulating polyimide material underneath the holes is removed by plasma etching. PWBs made in such a way are called DYCOstrate. In other, similar technologies, different dielectric materials are used, and they are removed by alkaline solutions. The rest of the process is similar to that for SLC; that is, holes are metallized and a thick copper deposition is made by electroless or galvanic plating, and the circuit pattern is formed by a tent-and-etch process (see Fig. 2.5).

2.6.3.2.3 Drilled Vias. In both SLC and DYCOstrate cases, through-holes can also be made by conventional drilling and plating processes, in addition to the surface blind via holes.

2.6.3.2.4 Cost Impact. The manufacturing cost of these sequential technologies is not necessarily directly cheaper than conventional MLB technology, which depends on a laminating press operation. However, since the cost of making standard holes in a board can be as high as 30

percent of the total manufacturing cost, and the creation of holes in these processes is comparatively inexpensive, the overall cost for equivalent functionality can be less. In addition, the fine pattern capability for this process is excellent. For example, an eight-layer conventional structure can often be reduced to a four-layer structure, reducing the total cost for the same packaging density.

2.7 MOLDED INTERCONNECTION DEVICES

Three-dimensional circuit technology was of great interest in the early to mid-1980s. The proponents for this technology, however, realized the mistake of trying to make it directly competitive with conventional flat circuits and have developed a niche where the substrate also offers other functional uses, such as structural support for the product.

Manufacturers of three-dimensional circuits prefer to call them *molded interconnection devices* (MIDs). In many applications of MIDs, the number of components to interconnect the electronic and electrical components can be reduced, thus making the total assembly cost cheaper and the final structure more reliable.

2.8 PLATED-THROUGH-HOLE TECHNOLOGIES

In 1953, the Motorola Corporation developed a plated-through-hole (PTH) process called the *Placir* method,[1] in which the entire surface and hole walls of an unclad panel are sensitized with $SnCl_2$ and metallized by spraying on silver with a two-gun spray. Next, the panel is screened with

a reverse conductor pattern, using a plating resist ink, leaving metallized conductor traces uncovered. The panel is then plated with copper by an electroplating method. Finally, the resist ink is stripped and the base silver removed to complete the PTH board. One problem associated with the use of silver is the migration caused by silver traces underneath the copper conductors.

The Placir method was the forerunner of the semiadditive process, which is discussed in Chap. 32.

In 1955, Fred Pearlstein[2] published a process involving electroless nickel plating for metallizing nonconductive materials. This catalyzer consists of two steps. First, the panel is sensitized in $SnCl_2$ solution, and then it is activated in $PdCl_2$ solution. This process presented no problem for metallizing nonconductive materials.

At the same time that Pearlstein's paper was published, copper-clad laminates were starting to become popular. Manufacturers of PWBs applied this two-step catalyzing process to making PTHs using copper-clad laminates. This process, however, turned out to be incompatible with the copper surface. A myriad of black palladium particles called *smads* were generated between copper foil and electrolessly deposited copper, resulting in poor adhesion between the electroless copper and the copper foil. These smads and electroless copper had to be brushed off with strong abrasive action before the secondary electroplating process could begin. To overcome this smad problem, around 1960 researchers began attempting to develop better catalysts; the products of their research were the predecessors of modern palladium catalysts.[3]

The mid-1950s was a busy time in the area of electroless copper-plating solutions. Electrolessly deposited nickel is difficult to etch. But since it adheres somewhat better to the base than does electroless copper, research for the development of stable electroless copper-plating solutions

was quite natural. Many patent applications for these solutions were filled in the mid-1950s. Among the applicants were P. B. Atkinson, Sam Wein, and a team of General Electric engineers, Luke, Cahill, and Agens. Atkinson won the case, and a patent[4] teaching the use of Cu-EDTA as a complexing agent was issued in January 1964 (the application had been filed in September 1956).

2.8.1 Subtractive and Additive Processes

Photocircuits Corporation was another company engaged throughout the 1950s in the development of chemicals for PTH processes. Copper-clad laminates were expensive, and a major portion of expensive copper foil had to be etched (*subtracted*) to form the desired conductor pattern. The engineers at Photocircuits, therefore, concerned themselves with plating (*adding*) copper conductors wherever necessary on unclad materials for the sake of economy. Their efforts paid off. They were successful in developing not only the essential chemicals for reliable PTH processes but also the fully additive PWB manufacturing technology known as the CC-4[a] process.

With the use of $SnCl_2$-$PdCl_2$ catalysts and EDTA-base electroless copper-plating solutions, the modern PTH processes became firmly established in the 1960s. The process of metallizing hole walls with these chemicals for the subsequent formation of PTHs is commonly called the *copper reduction process*. In the subtractive method, which begins with copper-clad laminates, pattern plating and panel plating are the two most widely practiced methods of making PTH boards. These methods are discussed in the following subsections.

2.8.2 Pattern Plating

In the pattern-plating method, after the copper reduction process, plating resist layers of the reverse conductor image are formed on both sides of the panel by screening resist inks. In most fineline boards, photosensitive dry film is used instead. There are some minor variations in the pattern-plating method (see Fig. 2.6):

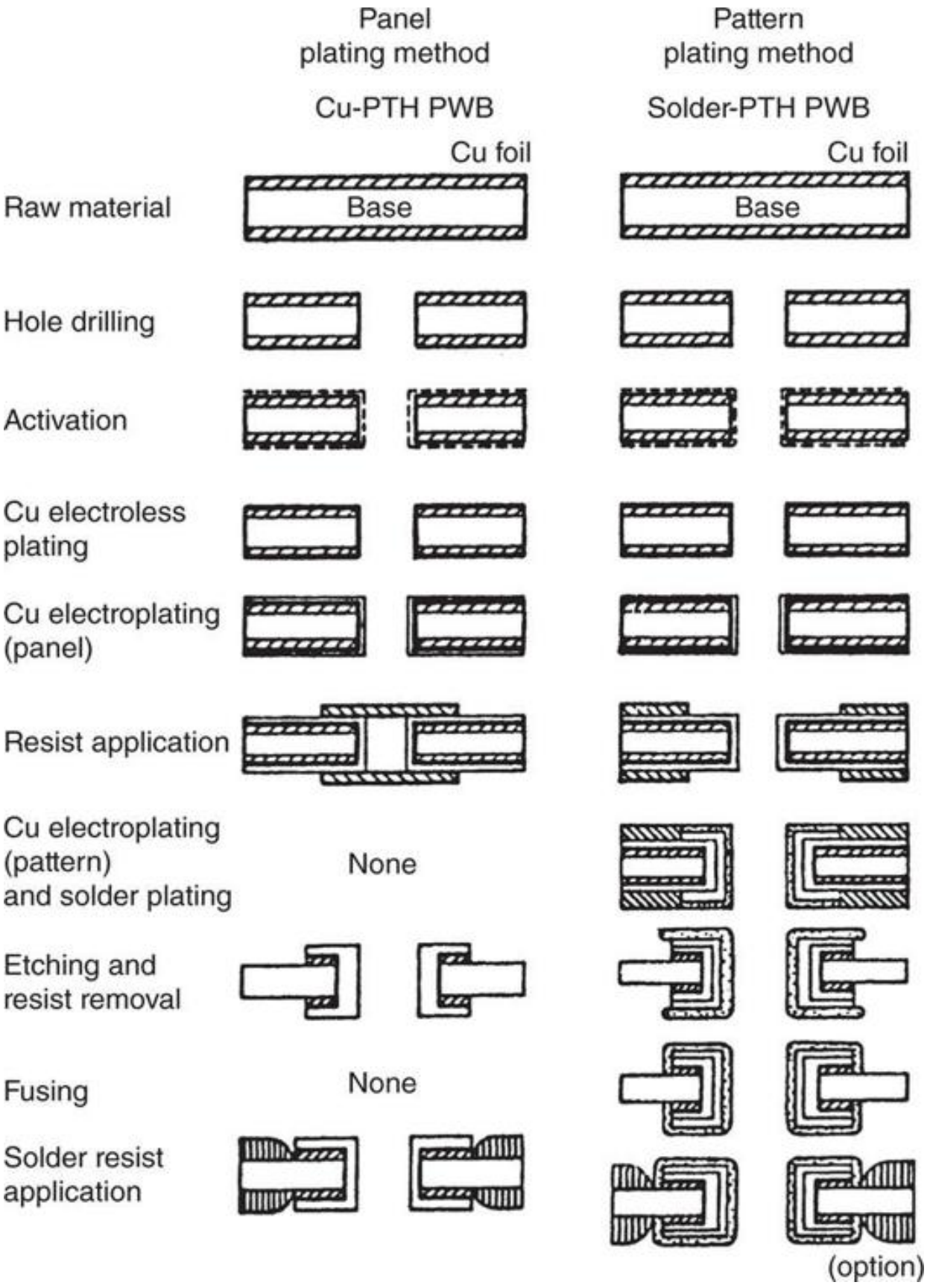

Panel plating method
Pattern plating method
Cu-PTH PWB
Solder-PTH PWB
Cu foil
Cu foil
Raw material
Base
Base
Hole drilling
Activation
Cu electroless plating
Cu electroplating (panel)
Resist application
Cu electroplating (pattern) and solder plating
None
Etching and resist removal
Fusing
None
Solder resist application
(option)

FIGURE 2.6 Key manufacturing steps in panel plating and pattern-plating methods.

1. Catalyzing (preparing the nonconductive surface to cause copper to come out of solution onto that surface)
2. Thin electroless copper (0.00001 in) followed by primary copper electroplating; thick electroless copper (0.0001 in)
3. Imaging (application of a plating resist in the negative of the desired finished circuit)
4. Final electroplating copper
5. Solder plating (as etching resist) 0.0002 or 0.0006 in
6. Stripping plating resist
7. Etching of base copper
8. Solder etching (0.0002-in case); solder reflow (0.0006-in case)
9. Solder mask followed by hot-air solder coater leveler if solder etching is used
10. Final fabrication and inspection

Most manufacturers of DSBs with relatively wide conductors employ thick electroless copper plating. However, thin electroless copper followed by primary electroplating is preferred for boards having fine-line conductors, because a considerable amount of surface is brushed off for better adhesion of dry film. This provides a higher reliability for PTHs. Solder reflow boards had been preferred by many customers, particularly in military and telecommunications applications, until the emergence of hot-air solder coater levelers. Although the solder-over-copper conductors protect the copper from oxidization, solder reflow boards have some limitations. Solder mask is hard to apply over reflowed solder, and it tends to wrinkle and peel off in some areas when the boards go through component soldering. A more serious problem is the solder bridging that occurs when the conductor width and clearance become very small.

In step 9, the entire surface of the board except for the pads is covered by solder mask, and then the board is immersed into the hot-air solder coater leveler, resulting in a thin coating of solder over the pads and the hole walls. The operation sounds simple, but it requires constant fine-tuning and maintenance of the hot-air solder coater leveler; otherwise, some holes may become heavily clogged with solder and are then useless for component insertion.

One advantage of the pattern-plating method over the panel-plating method is in etching. The pattern-plating method needs to etch only the base copper. The use of ultrathin copper foil (UTC), which is usually ⅛ or ¼ oz thick, offers a real advantage. However, as long as electroplating is used, the pattern-plating method cannot escape from a current distribution problem, regardless of the thickness of the base foils. The panel-plating method by electroplating suffers from the same problem but to a lesser degree. Good current distribution is very difficult to achieve when the boards are not of the same size or type, and particularly if some have large ground planes on the outer faces being plated. When the board has a few holes in an isolated area remote from the bulk of the circuitry, these tend to become overplated, making component lead insertion difficult during assembly. To minimize this current distribution problem, various countermeasures are practiced, such as special anode position, anode masking, agitation, and plating thieves. But none of these offers a decisive solution to the distribution problem, and they are extremely difficult to implement flexibly and effectively in a large plating operation, where a large number of product mixes have to be handled all the time.

Another advantage of the pattern-plating method is its ability to form padless micro-via holes of a diameter ranging from 0.012 to 0.016 in. Micro-via holes enable better usage of conductor channels, thereby increasing the connective capacity of the board.

2.8.3 Panel Plating

In the panel-plating method, there are two variations for finishing the board after the panel is plated with electrolytic copper to the desired thickness. In the *hole-plugging* method, the holes are filled with alkaline-etchable ink to protect the hole walls from being etched; this is used in conjunction with screened etch resist. In the other method, called *tent-and-etch* or simply *tenting*, the copper in the hole is protected from etching by covering the hole or tenting with dry film, which is also used as an etch resist for conductors on the panel surface. The simplified sequence of the panel-plating method is as follows (see Fig. 2.6):

1. Catalyzing
2. Thin electroless copper deposition (0.0001 in)
3. Electroplating copper (0.001 to 0.0012 in)
4. Hole plugging with alkaline-resolvable ink; tenting (dry film lamination)
5. Screen-print etching resist (conductor pattern); photoexpose the panel for conductor pattern
6. Etching copper
7. Stripping etching resist
8. Solder mask
9. Solder coater leveler (optional)
10. Final fabrication and inspection

The panel-plating method is ideal for bare copper board. However, it is a difficult way to make padless via holes, which are becoming more popular. Generally, the conductor width of 0.004 in is considered to be the minimum realizable by this method for mass production.

Although the use of the panel-plating method in the United States and western Europe is limited, nearly 60 percent of the PTH boards in Japan are manufactured by this method.

2.8.4 Additive Plating

Plated-through holes can be formed by additive (electroless) copper deposition, of which there are three basic methods: fully additive, semiadditive, and partially additive. Of these, semiadditive involves pattern electroplating for PTHs with very thin surface copper, but the other two form PTHs solely by electroless copper deposition. The additive process has various advantages over the subtractive process in forming fineline conductors and PTHs of high aspect ratio.

2.9 SUMMARY

Modern electronic packaging has become very complex. Interconnections are pushed more into lower levels of packaging. The choice of which packaging technology to use is governed by many factors: cost, electrical requirements, thermal requirements, density requirements, and so on. Material also plays a very important role. All things considered, PWBs still play important roles in electronic packaging.

2.10 REFERENCES

1. Robert L. Swiggett, *Introduction to Printed Circuits*, John F. Rider Publisher, Inc., New York, 1956.
2. Private communication with John McCormack, PCK Technology, Division of Kollmorgen Corporation.
3. C. R. Shipley, Jr., U.S. Patent 3,011,920, Dec. 5, 1961.
4. R. J. Zebliski, U.S. Patent 3,672,938, June 27, 1972.

[a] CC-4 is a registered trademark of Kollmorgen Corporation.

PART 2

MANAGING THE PRINTED CIRCUIT SUPPLY CHAIN

CHAPTER 3

BASICS OF PRINTED CIRCUIT SUPPLY CHAIN MANAGEMENT

Tim Rodgers
University of Colorado, Boulder, Colorado

3.1 INTRODUCTION

Printed circuit boards (PCBs) and printed circuit assemblies (PCAs) are often the most technically complex components that are purchased for electronic assemblies and products. This complexity leads to a number of challenges for a supply chain management (SCM) team that may be significantly different when compared with the other parts and commodities that the team manages.

3.1.1 Examples of Printed Circuit Supply Chain Issues

- PCBs and PCAs are custom-designed and therefore cannot simply be purchased from a catalog. There are many suppliers, but their capabilities and performance varies

widely, requiring more attention to supplier selection and qualification.

- A wide variety of manufacturing processes are used to create PCBs and PCAs, ranging from precise photoimaging and component placement, mechanical presses for lamination and ovens for solder reflow, wet chemical plating and etching, and high-speed drilling and routing. Buyers don't have to become expert in these processes; however, they can be intimidating.
- PCBs and PCAs are required to perform as part of an electrical circuit and that performance is critical to the success of the final product. The PCB obviously provides electrical interconnections between components attached to the board, but in some cases it operates as an active component in its own right. It may not be possible to determine whether the PCA works correctly until your design team has evaluated its performance as part of the final product.
- Although components on a PCA can be replaced, traces cut, and jumpers added, PCBs and PCAs cannot be easily reworked, returned, or recycled if the product requirements change. This can lead to additional cost and unwanted inventory.

The next several chapters are intended to guide experienced or new SCM professionals who may be unfamiliar with PCBs and PCAs and are looking for help. Figure 3.1 gives an overview of Part 2 of *Printed Circuits Handbook*.

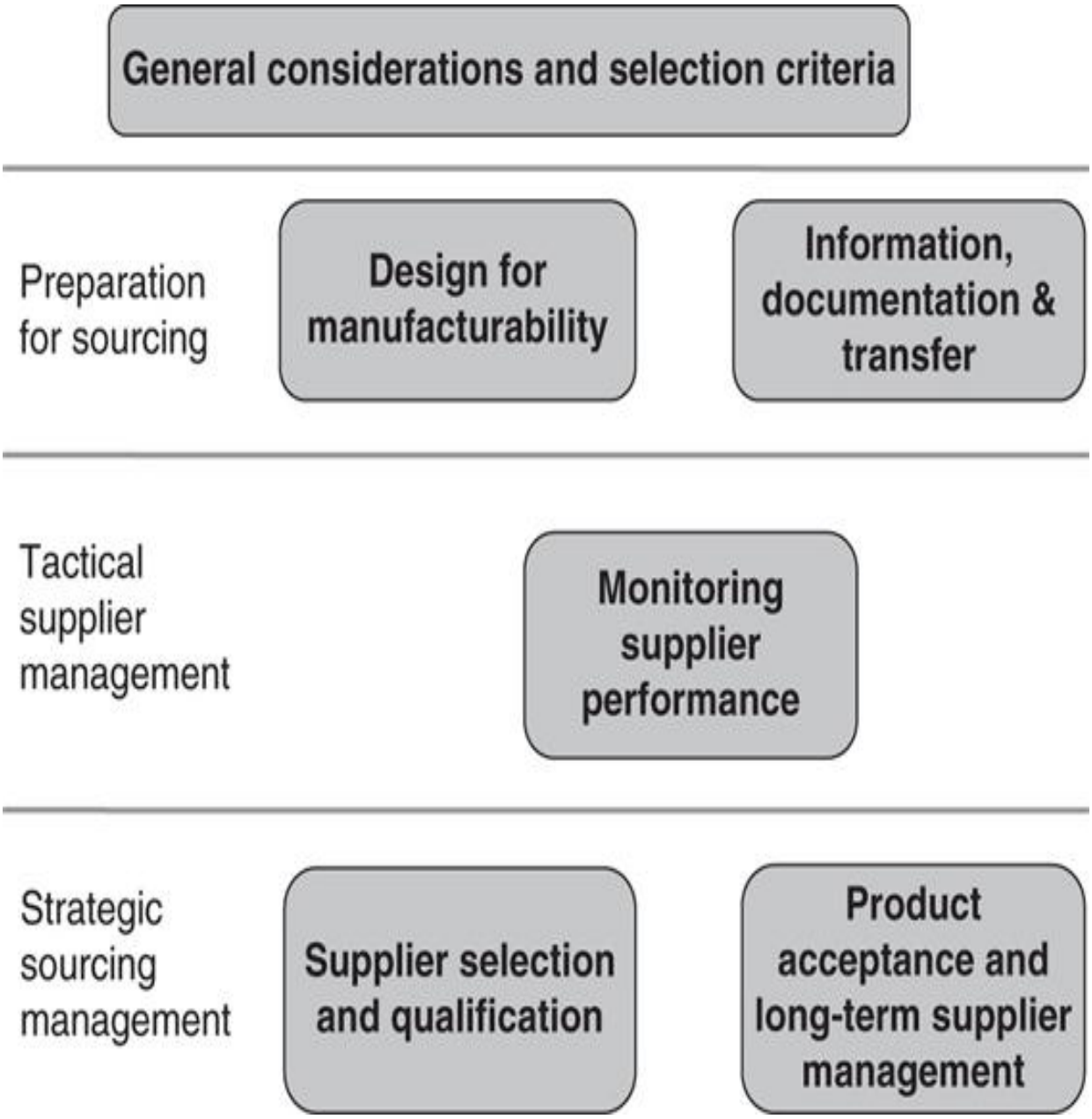


FIGURE 3.1 Supply chain management focus.

3.1.2 Overall Printed Circuit Supply Chain Management Chapters

- *Basics of Printed Circuit Supply Chain Management (Chap. 3)*. This chapter includes some general considerations for

PCB and PCA sourcing decisions, and the criteria that should be used to evaluate and select suppliers.

- *Design for Manufacturability (Chap. 4)*. This chapter explains the importance of DFM as a way of optimizing performance and cost, reviews the major contributors to cost and manufacturability, and provides some practical examples.
- *Managing Information, Documentation, Formatting, and Exchange (Chap. 5)*. This chapter outlines the recommended steps for creating documentation and drawings in order to specify the design requirements and other expectations for the suppliers.
- *Supplier Selection and Qualification (Chap. 6)*. This chapter applies the business considerations and selection criteria described in Chap. 3 to evaluate and qualify suppliers, including processes to perform technical assessments of samples provided by the supplier.
- *Process Control, Monitoring, and Incoming Inspection (Chap. 7)*. This chapter gives a brief introduction to quality assurance methodology based on six sigma principles, with specific recommendations for process control, testing, and inspection of PCBs and PCAs at the supplier.
- *Product Acceptance and Feedback (Chap. 8)*. The final chapter in Part 2 provides guidelines for design qualification, lot acceptance, and ongoing inspection of received PCBs and PCAs. It also includes recommendations for long-term supplier management that minimize the internal management cost while maintaining a high level of performance.

3.2 GENERAL BUSINESS CONSIDERATIONS

Before choosing a supplier it is important to understand where the PCBs and PCAs fit in the overall value delivery system for an electronic assembly (see Fig. 3.2). This is because the incoming requirements for the next, downstream step in the value chain, whether component assembly or top-level assembly, will dictate many of the requirements for the upstream suppliers. The key questions are

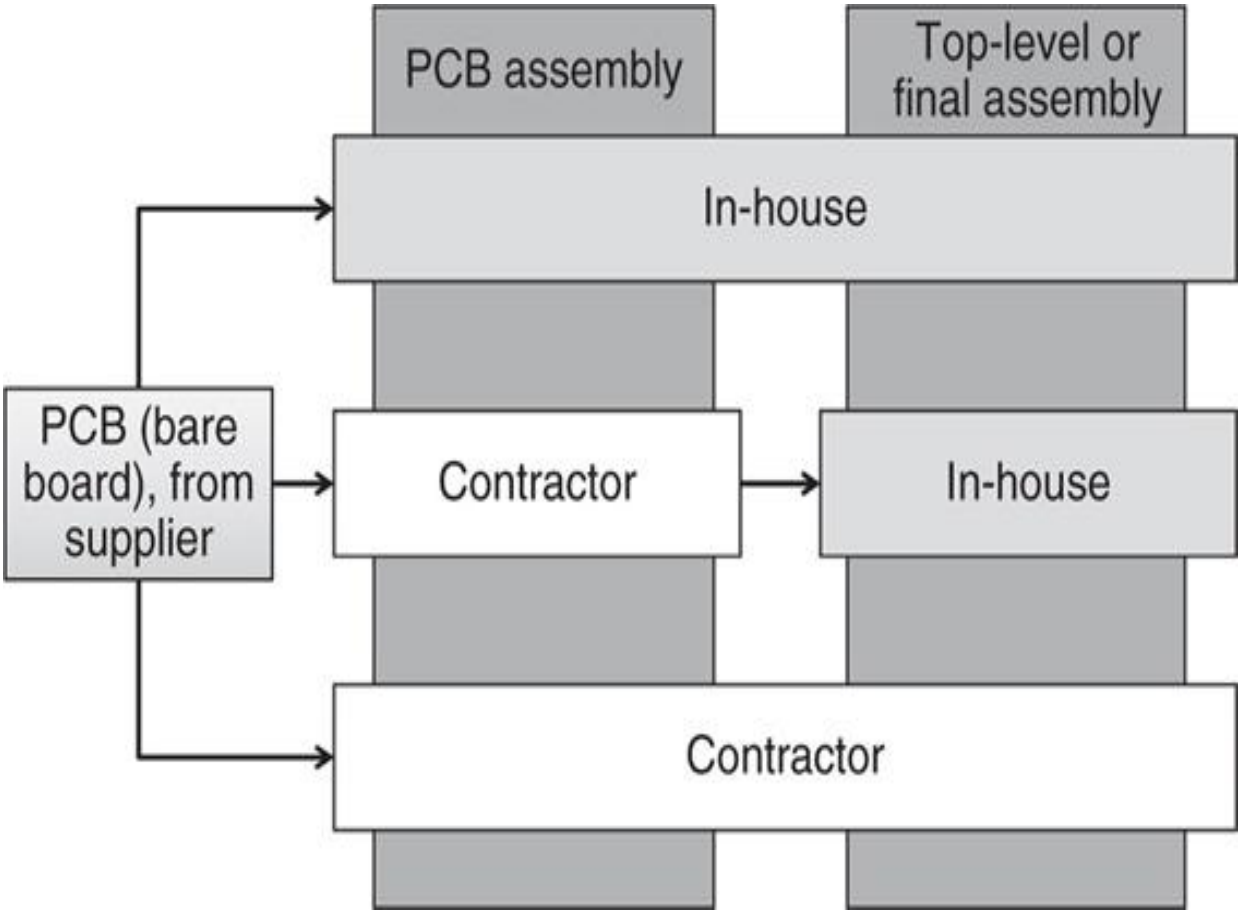


FIGURE 3.2 PCB and PCA value delivery system.

- Where are the PCBs or PCAs going after they are obtained from the supplier?
- Will they be assembled on-site at an in-house, captive factory?

- Or, will they be sent to another contractor for component assembly, and possibly final assembly as well?

3.3 CONTRACT MANUFACTURERS

Contract manufacturers who provide assembly services often have their own preferred list of qualified suppliers that can be used to greatly simplify the sourcing decision. Regardless of whether the PCBs/PCAs go next, whether to an internal or external factory, that facility must be included in sourcing decisions to ensure that manufacturability is taken into account. The supplier evaluation team will be discussed in more detail later in this chapter.

If the firm has its own internal capability to assemble PCBs and create PCAs, the sourcing strategy must include a discussion of whether it is better to make or buy the PCAs.

3.3.1 Sourcing Factors That Should Be Considered

- Are there special technology requirements? The internal factory may not currently have the capabilities that are required to support the design. If that is the case, then the design must be outsourced.
- What is the capacity of the internal factory? Outsourcing may be the only option if the internal factory cannot meet the required delivery time. The internal “make” option may be expected to be more responsive; however, this is not always the case.
- What is the cost of internal assembly versus outsourcing? Note that it may be possible to find an external supplier that can provide lower unit cost, but unused internal capacity is also a cost to the business.

3.4 CRITERIA FOR EVALUATING SUPPLIERS

The choice of a specific supplier depends on the relative importance of several different dimensions of supplier performance (see Table 3.1). Suppliers have inherent capabilities and strengths that are based on their own strategic decisions about how they choose to compete. Those capabilities will determine how well they fit the sourcing strategy and how they are likely to perform as an ongoing business partner. Understanding what is most important to the business will guide initial supplier selection and determine whether the supplier's performance continues to meet your requirements.

TABLE 3.1 PCB Supplier Performance Criteria

Category	Examples
Technology	Electrical (thick copper, dielectric) Thermal (low TCE) Dimensional (flexible or molded circuit) Assembly (surface finish, tolerances)
Responsiveness	On-time delivery Rapid prototyping Lead time
Quality	Conformance to industry standards Conformance to internal specifications Order completeness Accuracy of required documentation
Cost and price	Price per unit Supplier management costs
Other services	Design support Locally-based sales or technical staff

3.4.1 Supplier Performance Requirements

- *Technology*. The PCB or PCA is expected to perform in the final service environment, both as a mechanical platform for other components, and as an element in the electrical circuit. Suppliers must be able to provide the chosen combination of design elements (e.g., conductors, layers), surface finishes, dielectric materials, dimensions, and other technical specifications as required.

- *Responsiveness*. This category includes the supplier's ability to achieve on-time delivery, and the lead time that the supplier requires for orders and design changes, both of which must be consistent with the requirements of the downstream assembly and production processes.
- *Quality*. The PCB or PCA must conform consistently to industry standard, and also any unique internal specifications and requirements for the design. This category also includes order completeness and the accuracy of any required documentation provided by the supplier.
- *Cost and price*. Obviously the price paid to the supplier per unit is an important factor. However, there are other cost elements that should be considered, including any internal staff and other expenses required for ongoing supplier management, and inventory holding costs due to fixed order quantities or slow response to design changes.
- *Other services*. PCB and PCA suppliers may offer other services that may be valuable to the business, including design support, or locally based sales or technical staff to help address issues.

Each of these categories will be described in more detail later in this chapter.

3.4.2 The Sourcing Strategy Team

Because PCBs and PCAs are a custom-designed component with significant implications for a successful product, a cross-functional sourcing team is strongly recommended to review the business requirements, determine how to prioritize and assign weighting factors to these requirements, and subsequently evaluate and qualify potential suppliers.

The sourcing strategy team should be led by a commodity manager or senior buyer in the SCM organization, and at

minimum the team should include representatives from design engineering and the manufacturing group that will use the PCB or PCA, whether internal or outsourced. Representatives from the quality and finance functional groups may also be added to the team, if available.

The team's initial responsibility is to develop a sourcing strategy that is aligned with the needs and priorities of the business. It is possible that a single supplier can meet all of these needs, but it is more likely that compromises and trade-offs will have to be made. The sourcing strategy team needs to determine which performance characteristics are "musts" or "wants," and what can be traded for higher performance in a different area. Note that over time the needs and priorities of the business may change, and this requires a reevaluation of the sourcing strategy.

3.4.3 Technology

At a fundamental level, suppliers must be able to provide a PCB or PCA that meets certain performance requirements, and their inability to do so will typically eliminate them from further consideration. For PCBs these include electrical, thermal, dimensional, and assembly requirements.

The most common materials used to fabricate rigid PCBs are FR-4 laminate with ½-oz copper conductors. SCM professionals should consult with the electrical engineers on the design team to understand whether the PCB is required to provide specific performance characteristics as part of the circuit. Examples include thicker copper for current carrying capacity, or a material with a different dielectric constant between conductive layers.

Other applications may require laminate materials with a low coefficient of thermal expansion to reduce strain on solder joints and improve reliability. The physical dimensions and size constraints of the finished product can limit the use

of a rigid board, making it necessary to opt for a flexible or molded circuit. Non-standard technical requirements such as these may significantly limit the supply base; however, there are still many suppliers who can meet the need.

Suppliers who can offer narrow conductor widths, small-diameter through vias, blind or buried vias, and high layer counts give designers more options for circuit layout, although these options can add significant cost due to the special processing required and lower production yields. Chapter 4, “Design for Manufacturability,” describes some of the more common technology trade-offs and their relative costs.

Printed circuit assembly operations have standard requirements for surface finishes, and location and dimensional tolerances for holes, pads, and fiducials. The electronics manufacturing industry generally follows IPC standards and specifications, and any reputable PCB supplier will be familiar with IPC-A-600 Acceptance of Printed Wiring Boards. Other standards may be specified by the assembly operation and these should be clearly communicated to the supplier, and ideally the supplier’s performance should be verified independently before selection.

Table 3.2 summarizes the key questions for determining the technology requirements for PCBs.

TABLE 3.2 PCB Technology Considerations

Technology	Consideration
What is the laminate material?	Dielectric constant Low thermal expansion
What are the required characteristics of the conductors?	Conductor width and spacing Through via diameter Copper thickness
Any constraints on the physical dimensions of the board	Overall board thickness, length, width and tolerances Flexible or molded substrate
What are the requirements for the assembly operation?	Surface finish Dimensional and location tolerances Other requirements

The technology considerations for suppliers of PCAs include the following:

- Single- versus double-sided assembly
- Restrictions on back-side active components
- The ability to accurately place fine pitch components (e.g., QFP, BGA, COB)
- The ability to handle non-standard components requiring manual placement
- Support of non-lead soldering

PCB and PCA suppliers will provide a detailed list of their capabilities, materials, and processes on request. However, for most applications, it is important to verify those capabilities with samples, prototypes, or first articles. Chapter 6, “Supplier Selection and Qualification,” provides a

review of the common methods used to evaluate samples for supplier qualification.

3.4.4 Responsiveness

Supplier responsiveness considerations should be familiar to any experienced SCM team, regardless of the commodity:

- On-time delivery
- Rapid prototyping capability
- Lead time for production orders
- Minimum order quantity

PCB and PCA suppliers obviously must be able to meet your technology requirements, but it is also important that the boards or assemblies arrive when they are needed. You can measure a supplier's on-time delivery performance over time; however, this is difficult to assess before placing the initial order with a new supplier. The sourcing strategy team should determine the business requirements for rapid and reliable on-time delivery and ask potential suppliers how they can support those needs.

Despite the availability of simulation tools, PCB and PCA design performance typically cannot be verified without the actual hardware. Electrical engineers and board designers value rapid turn-around time for prototype boards to test performance, and suppliers who can provide this service have an advantage.

Many businesses use different suppliers for prototype and production boards, with the prototype supplier located geographically close to the design team to reduce the delivery time and facilitate communication. A single supplier who can offer a local quick-turn prototype facility that is associated with a higher-volume production facility (typically in a region with lower labor and production costs) offers the

best of both worlds. (See Fig. 3.3.) This model also reduces the need to communicate design and manufacturability information from the prototype supplier to the production supplier.

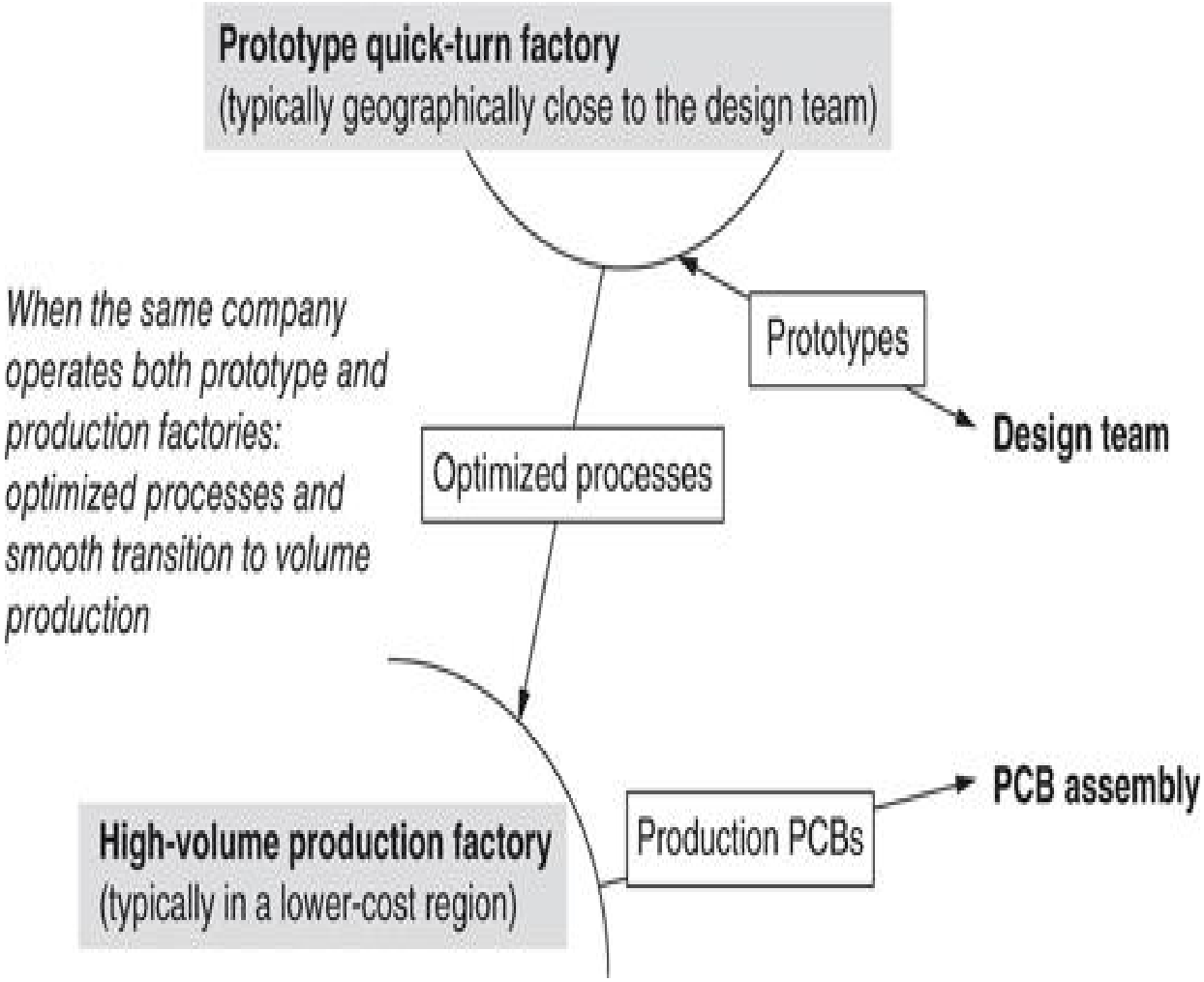


FIGURE 3.3 Prototype and production factories.

Suppliers will typically advertise a standard lead time for order completion and delivery of production boards, but most will also usually offer a faster turn-around time option to expedite the order at a higher price. The sourcing strategy team should consider the likelihood of design changes or other engineering change orders that require a quick change from one PCB or PCA version to another. A slow response

here could mean a large quantity of obsolete inventory in-house or in-transit, particularly for a large minimum order quantity. If changes are likely and frequent, a supplier who can provide expedited orders at a manageable cost will be valuable.

Inventory buffer and safety stock management also depends on the likelihood of late deliveries and the supplier's minimum order quantity. Supply chain professionals should audit a supplier's fulfillment and shipping processes, and estimate the business's sensitivity to delays in order to optimize buffers.

Table 3.3 summarizes the key questions for determining the responsiveness requirements for PCBs or PCAs.

TABLE 3.3 PCB/PCA Responsiveness Considerations

What is the acceptable range of delivery time vs. plan?
Is late delivery acceptable?
How early?
What is the expected quantity of parts per order?
What is the expected frequency of orders?
What is the standard lead time for production orders?
Is shorter lead time valuable to the business?
Does the engineering team need rapid prototyping capability?

3.4.5 Quality

As with delivery performance and responsiveness, it is very difficult to assess a supplier's quality performance in advance. All reputable suppliers should be familiar with the IPC standards for PCBs and PCAs (see summary in Table 3.4). These define the minimum specifications; however, downstream assembly and production sites may have

additional and more-stringent requirements, for example, for dimensional tolerances or more-detailed inspection reports.

TABLE 3.4 Subset of IPC Standards for PCBs and PCAs

Standard	Title
IPC-2615	Printed Board Dimensions and Tolerance
IPC-D-325	Documentation Requirements for Printed Boards
IPC-ET-652	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-7351B	Generic Requirements for Surface Mount Design and Land Pattern Standards
IPC-4652	Metal Foil for Printed Wiring Applications
IPC-4101	Laminate Prepreg Materials Standard for Printed Boards
IPC-A-600	Acceptance of Printed Wiring Boards
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6013	Specification for Printed Wiring, Flexible and Rigid-Flex
IPC-TF-870	Qualification and Performance of Polymer Thick Film Printed Boards
IPC-FA-251	Assembly Guidelines for Single and Double Sided Flexible Printed Circuits

All PCB suppliers should have the capability to perform visual inspection and simple electrical continuity testing for opens and shorts, and the sourcing strategy team should consider whether this should be done on all boards or an audit sample. For PCAs, in-circuit testing is typically performed on 100 percent of all assemblies. Customers can also request functional testing of the PCAs; however, this will require a dedicated test fixture that must be designed and provided by the customer, or designed and purchased separately from the supplier.

Suppliers can ensure that all shipped PCBs pass required testing and inspection; however, a supplier with a high-production yield will operate at lower costs. A low production yield is often an indicator of manufacturing process problems that can lead to low reliability of the final product in the field. The sourcing strategy team should consider a site audit to assess the effectiveness of the supplier's internal quality processes to meet specifications on a consistent basis. Chapter 7, "Process Control, Monitoring, and Incoming Inspection," provides specific guidelines and recommendations for process monitoring and inspection.

It is important to determine the response and level of engagement that is expected from the supplier when there is a quality issue with received PCBs. The supplier should actively participate in troubleshooting and root cause analysis, and may be asked to inspect and sort boards in any suspect lot received. SCM commodity managers should also clearly communicate their warranty expectations in their contract terms and conditions, including processes for returning defective boards to the supplier for rework or scrap.

Table 3.5 summarizes the key questions for determining the quality requirements for PCBs or PCAs.

TABLE 3.5 PCB/PCA Quality Considerations

Does downstream assembly have special quality needs beyond IPC standards?	
What are the production testing and inspection requirements?	Additional testing Sampling and audit frequency Reports
Do PCAs require functional testing?	
What is the expected supplier response to quality issues?	Returns, rework and scrap On-site lot inspection Warranty for field failures due to bad parts

3.4.6 Cost and Price

Obviously the supplier who offers the lowest quoted price per unit will get the attention of the SCM team. However, the profit margins at the average PCB or PCA supplier are typically very small. The lowest-cost supplier will not make much profit on your business and they are unlikely to freely offer other capabilities and services that may be needed or desired. It is important to understand the impact of PCB or PCA price on the total material cost of the final product to determine the overall sensitivity to price changes.

Also, as mentioned above, price is something that may be traded for other considerations, such as expedited delivery or rapid prototyping. Poor supplier performance in these other areas can lead to additional costs that may not be immediately apparent. For example, a long delivery pipeline from the supplier will contribute to inventory costs, which can be particularly expensive following a design change.

Note that the supplier’s cost to produce the PCB or PCA is the most important factor in determining the price that is quoted to a customer, and that cost is almost entirely due to

decisions made by the PCB or PCA designer. Chapter 4 provides details about the most common cost models and drivers used by suppliers. Understanding these models will help designers make decisions that optimize performance and cost. Actual pricing may vary according to market conditions.

Table 3.6 summarizes the key questions for determining the cost and price requirements for PCBs or PCAs.

TABLE 3.6 PCB/PCA Cost and Price Considerations

Is there a material cost budget that limits the maximum price per unit?
What is the overall sensitivity to PCB/PCA price?
Is the business willing to pay more to receive other services?
Shorter lead time or smaller lot sizes for production orders
Faster prototype turn-around time

3.4.7 Other Supplier Services

The availability of other engineering, design, and sales support services may be an additional consideration in choosing a supplier. As mentioned above, many major PCB and PCA suppliers offer local prototyping services that are associated with a separate high-volume production facility. This capability enables the supplier to quickly transfer knowledge about the PCB or PCA design from the early prototypes, which should mean a smoother ramp to higher production quantities. Suppliers may also be able to provide support to assist designers and electrical engineers, including board layout, schematic capture, and performance simulation tools.

The sourcing strategy team should also consider the value of having a locally based sales and technical staff that can quickly respond to questions, quality and delivery issues,

and other routine communication needs. All of these services certainly add to the supplier's operating costs; however, the value of the services can greatly outweigh any incremental increase in board or assembly price.

3.4.8 Other Supplier Management Considerations

PCBs and PCAs may be different than other commodities in some ways, but in many other ways standard supplier management principles apply. Here are a few additional considerations when formulating a sourcing strategy:

- *Supplier management costs*. It may be possible or even necessary to assign dedicated staff to manage PCB or PCA suppliers, but typically this is a shared responsibility within the SCM team. There is an incremental cost associated with each supplier, including time and travel, and businesses should take that into account when deciding on the number and geographic location of their PCB or PCA suppliers.
- *Sole sourcing versus multiple suppliers*. One way to minimize supplier management costs is to choose a single supplier to meet all of your needs. However, sole sourcing significantly increases supply risk. The supplier strategy team should consider the cost and benefit of maintaining multiple suppliers who actively compete against each other and reduce the risk of supply interruptions.
- *Managing poor performance*. Poor supplier performance over a period of time may ultimately lead to a discussion about changing suppliers. However, there is a switching cost associated with starting a new business relationship with a supplier, or ending a relationship with an existing supplier. Working to improve an underperforming supplier also has a cost, and there is no assurance of success. At

some point it may be better to end the relationship. Chapter 8, “Product Acceptance and Feedback,” includes additional guidelines regarding long-term supplier performance management and options for correcting poor performance.

- *Intellectual property protections*. Because PCBs and PCAs are custom-designed, drawings, schematics, and other documents are confidential information that must be kept secret and secure at the supplier. Chapter 5, “Manufacturing Information, Documentation, Formating, and Exchange,” provides more details about protecting sensitive and confidential information. All suppliers should be regularly audited to ensure that the appropriate protections are in-place and effective, and a supplier who cannot provide these protections with confidence should not be selected.
- *Business stability and environmental stewardship*. As with any commodity, buyers should consider whether or not the supplier has the financial stability to remain a long-term business partner. Suppliers should also maintain processes and business records that support the buyer’s goals for environmental stewardship and sustainability.

3.5 SUPPLIER SELECTION CRITERIA EXAMPLE

The specific needs of each business will determine the relative importance of all the performance characteristics of suppliers, and what trade-offs can be made to optimize the mix of suppliers and capabilities. Before investigating and evaluating suppliers, the sourcing strategy team should review the business needs for technology, responsiveness, quality, cost and price, and other service requirements. Note that it is unlikely that each of these requirements will be

equally important. Some requirements may be “musts,” meaning the team will not consider a supplier who cannot provide that requirement. Other requirements are “wants” that are desired but would not eliminate a supplier from consideration.

A common approach is to assign weighting factors to indicate the relative importance of each requirement. This makes it possible to evaluate suppliers based on their ability to meet those requirements using a weighted criteria analysis. Table 3.7 shows an example of how one sourcing strategy team might prioritize their needs for a PCB supplier. This decision-making methodology will be revisited in Chap. 6.

TABLE 3.7 Supplier Selection Criteria Weighting Example

Selection Criteria	"Must" Requirement?	Relative Weight (1 to 5)
Technology		
• Standard FR-4 laminate	Yes	
• Minimum conductors 4 mils	No	2
• Minimum via diameter 12 mils	No	4
• Pb-free surface finish	Yes	
Responsiveness		
• 6 week lead time for production	No	3
• 0 days late, no more than 3 days early	Yes	
Quality		
• 100% opens/shorts testing	Yes	
• Defective boards returned to supplier	Yes	
Cost and Price		
• No more than $X per square inch	No	5
Other Services		
• Prototypes within one week	No	2
• Local sales and technical support	No	4

CHAPTER 4

DESIGN FOR MANUFACTURABILITY

Tim Rodgers
University of Colorado, Boulder, Colorado

4.1 GENERAL PRINCIPLES

The design process for an electronic system requires decisions that will influence the cost and performance of the printed circuit assembly (PCA).

4.1.1 Examples That Influence Cost and Performance

- Product architecture and circuit design assigns the partitioning of functions between component-level and board-level, and this determines the approximate size and number of PCAs that are required.
- In many cases, a previously defined standard card cage or other form factor constraint leads to a maximum board

length and width requirement.

- Electrical performance characteristics such as timing requirements, controlled impedance, and maximum current or voltage determine allowable combinations of trace width, trace length, and dielectric thickness.
- High I/O components will dictate local connectivity requirements for successful circuit routing.
- The board layout designer may be given some flexibility in determining component placement, conductor width, and layer count during schematic capture and routing.

Not surprisingly, it is usually possible to create more than one PCB or PCA design that meets the specified performance requirements. Figure 4.1 gives three possible design solutions for a single circuit schematic and set of components. When faced with equivalent design alternatives, how does one decide which is “best”? Most people would agree that it is the one that results in the lowest overall cost. If the number of design alternatives is small, it may be possible to obtain a price quote for each one. However, price quotes from suppliers can be misleading. Price is often based on prevailing market conditions or the desire of a supplier to attract or discourage business.

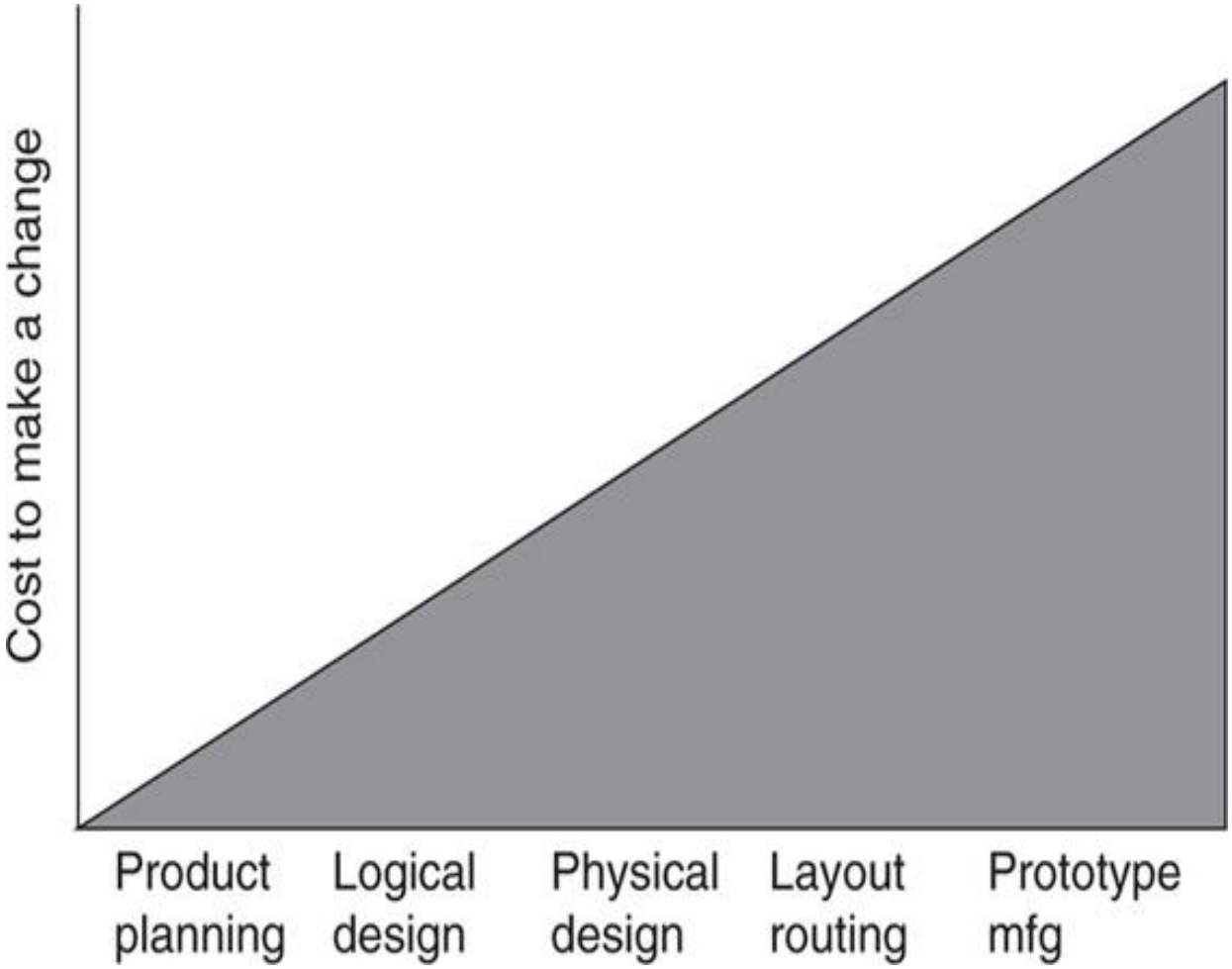


FIGURE 4.1 Cost opportunity at different design stages.

There is also value in being able to quickly estimate the impact of design on cost. Because of the increasing pressure to shorten time-to-market, design engineers may not have the luxury of using trial-and-error and price quotes to fine tune a new design. In addition, the farther down the development cycle for a new product, the greater the difficulty in introducing a design change for any reason. Decisions made during the early phases of product planning and logical design have a greater impact on final cost than is often realized (see Fig. 4.2).

56 gates
50 devices,59 equivalent IC's
182 signal lines
290 non-supply connections
24.56 sq inches board area

	Design 1	Design 2	Design 3
Layers	6	4	4
Vias	130	270	234
Line length	411.726"	466.512"	411.644"
Minimum trace width / space width	12/12 mils	8/7 mils	6/6 mils
Totalholes	791	931	895

FIGURE 4.2 Alternative PCB design for a single schematic.

When engineers and designers understand what contributes to the cost of the printed circuit board (PCB) or PCA, and how their decisions can optimize both performance and cost, they not only save money for the immediate purchase order, but also over the entire life of the product.

4.2 PCB/PCA PRICING MODELS

PCB fabricators and PCA assemblers are in business to make money, and they expect to recover their expenses of doing business with at least some profit. While many elements

contribute to those expenses, designers, engineers, and supply chain management professionals are most interested in the things they can directly control through their own design choices.

The operating cost of any manufacturing facility will include overhead for such things as administration and sales and marketing. However, these are usually considered design-independent and outside the control of the customer. Similarly, the mark-up for profit depends less on the design, and more on how badly the supplier wants to win this business, the competitive environment, and other strategic considerations.

Design-dependent costs can be estimated by looking at the cost of the materials used in production plus the allocated cost of any processes that are used, adjusted for any yield losses that are incurred due to failures at inspection or test. Figure 4.3 illustrates this relationship.

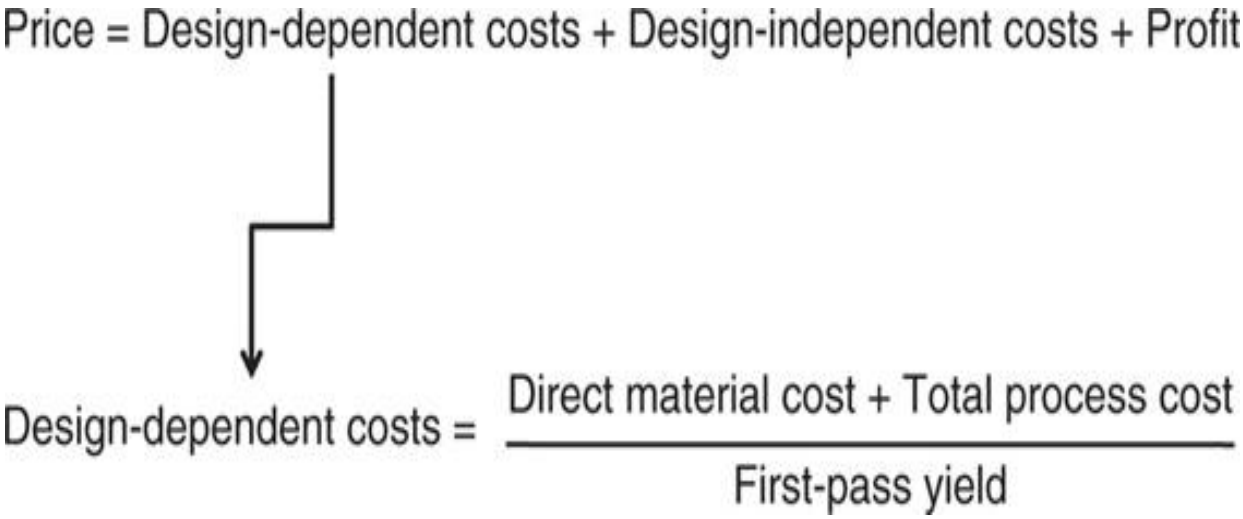


FIGURE 4.3 Contributions to design-dependent costs.

The materials used to construct a PCB are the source of the *direct material cost*. This includes copper foil, prepreg, copper clad core laminate, and soldermask. The material cost can be easily determined from board area and details about the board construction, such as laminate type, number

of layers, and number of prepreg plies. It also includes any deposited metal layer, although with the exception of gold this cost is negligible. For a PCA this would certainly include any attached components in the bill of materials.

Manufacturing processes are characterized by variable costs that depend on the number of units that are produced, and fixed costs that do not. Variable costs include indirect consumables, labor, and maintenance. Fixed costs are incurred regardless of whether the process is used, such as depreciation on capital equipment. From the standpoint of design-dependent costs these can be lumped together as the *total process cost*.

The specific cost model for PCB or PCA suppliers can vary; however, many operations use the concept of a cost center with a specific allocation applied to each unit that passes through the center. For example, if it costs a total of $100,000 per year to operate and maintain a process (or, cost center), and recent history indicates that 10,000 units per year will be processed, then the allocation for the process is $10 per unit. Note that in this model a process that is rarely used will have a smaller basis for cost allocation and therefore a higher rate. This will become important when we look at nonstandard PCB and PCA production.

The internal, *first-pass yield* at a supplier must also be factored into the cost for several reasons. PCBs are difficult to rework, and because of the risk to long-term reliability many customers prefer to have suppliers scrap any boards that fail testing. Production scheduling must compensate for yield loss by increasing the number of panels launched for a given purchase order. PCAs can be reworked by replacing components, but this adds both labor and component cost. Note that the cost of rework is usually passed to customers as an additional process cost, or appears as a yield variance.

Rather than calculate a bottoms-up cost for each new design, PCB fabricators typically create a standard pricing

matrix that provides a basis for quoting. This matrix assumes a standard set of design characteristics that includes laminate material, outerlayer surface finish, minimum conductor width, and minimum hole size, and estimates the cost for a given board size and layer count. Any characteristics of the board design that deviate from standard materials and processing adds cost and is accounted for as either a price adder, or its own pricing model. PCA assemblers use the component bill-of-materials and a similar matrix for quoting purposes.

While each factory or supplier may have their own internal and confidential cost model, we can infer the relative cost contributions of different design features from average market price data. Figure 4.4 shows the results of a survey of Chinese PCB suppliers taken in July 2012 with a range of prices (in cents per square inch) for PCBs with different layer counts. Where absolute price data are unavailable, it is still possible to compare design options using a ratio, or relative price compared to a standard. See, for example, Fig. 4.5 for a price comparison of different types of FR-4 laminate.

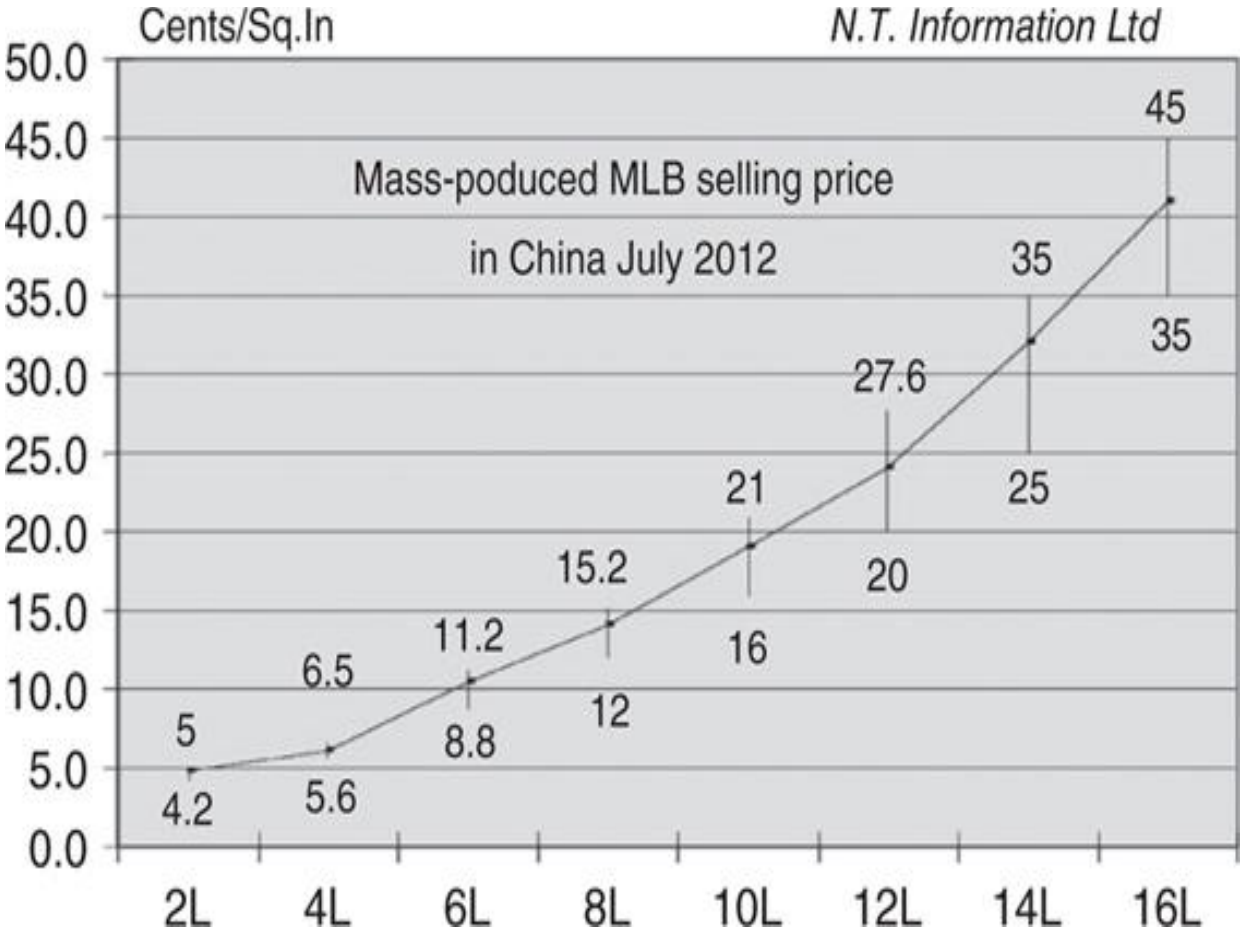


FIGURE 4.4 Market price survey data for PCBs.

4.2.1 Material Cost Drivers

For PCBs the predominant driver of material cost is the dielectric laminate, including copper-clad core and prepreg. Design decisions that relate to laminate cost include the type of material itself, the board size, and the number of layers.

4.2.1.1 Material Type. Glass-reinforced FR-4 certainly remains the default choice for PCBs, and DiCY-free or halogen-free varieties are currently available with a variety of thermal characteristics (see Fig. 4.5). There are cheaper materials such as paper phenolic, but their performance may not meet the electrical and thermal requirements for the finished PCA. At the other end of the spectrum are more

expensive and exotic materials using different resins and reinforcements for high speed or low thermal expansion applications. Figure 4.6 shows some of these materials and their associated permittivity and dissipation factor. The effect of laminate type on board cost for a double sided and a multilayer board is illustrated in Figs. 4.7 and 4.8.

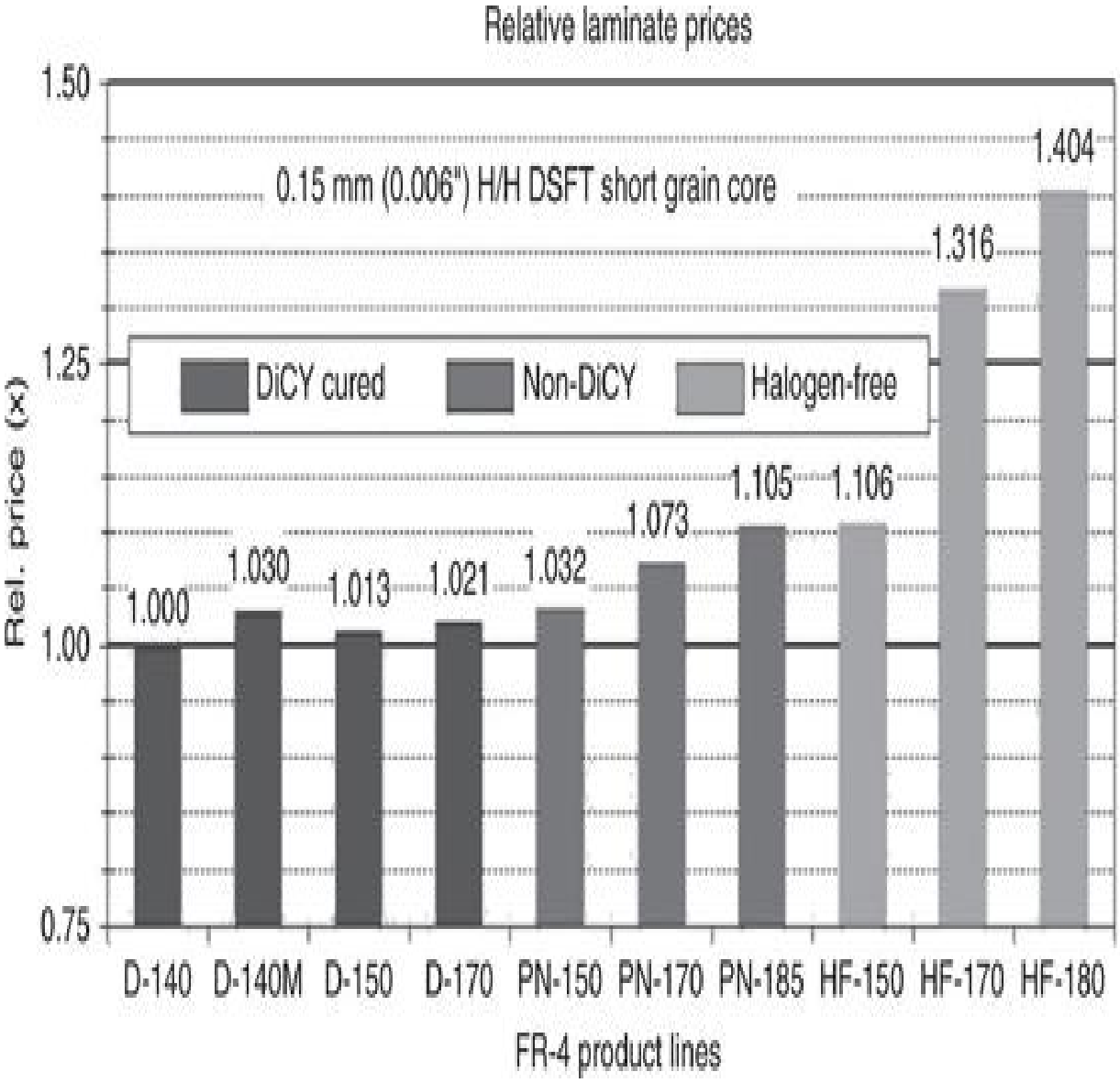


FIGURE 4.5 Relative price for different types of FR-4.

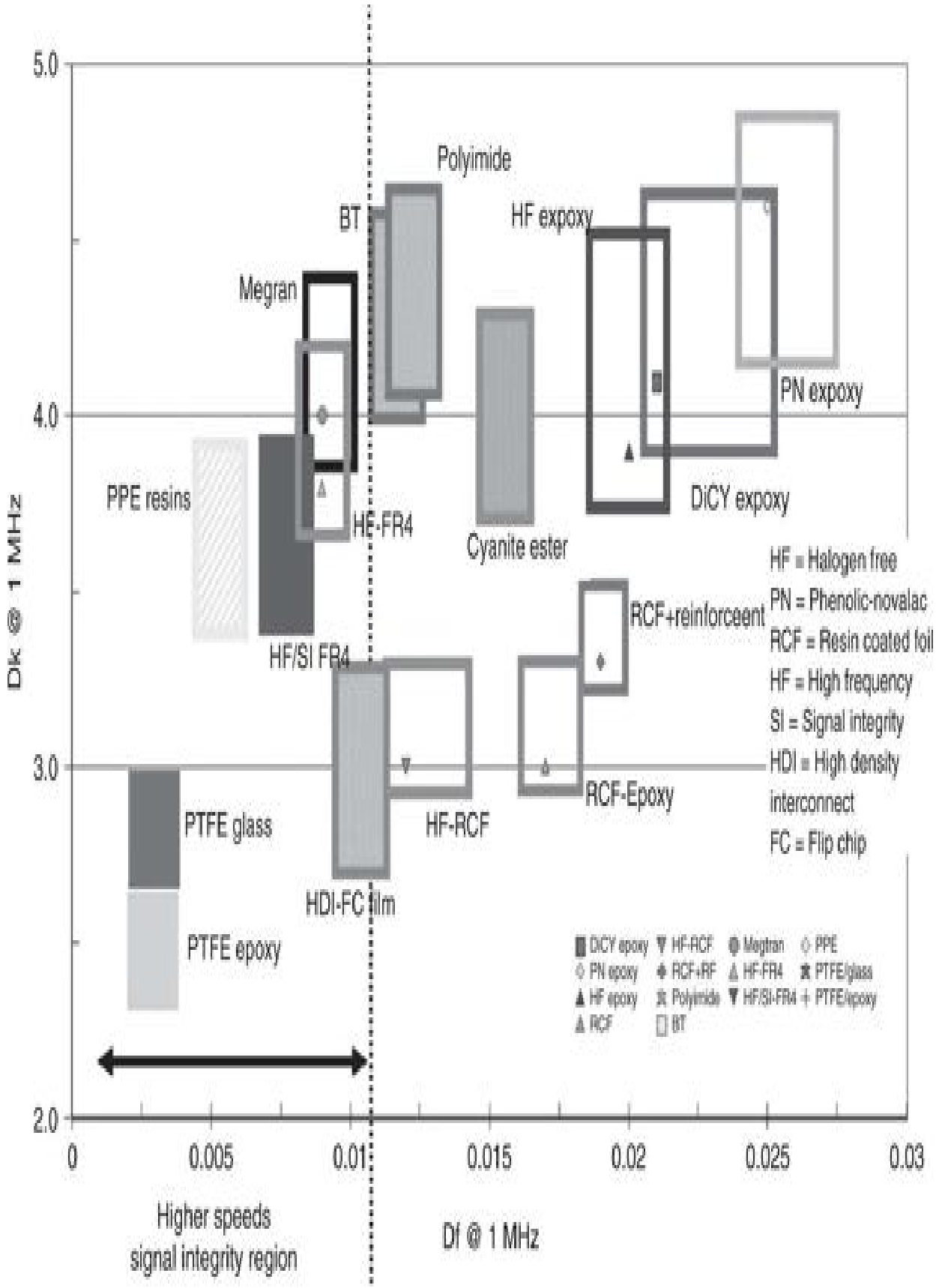

5.0
4.0
3.0
2.0
Dk @ 1 MHz
0
0.005
0.01
0.015
0.02
0.025
0.03
Df @ 1 MHz
Higher speeds
signal integrity region
Polyimide
BT
HF expoxy
Megran
PN expoxy
PPE resins
HF-FR4
Cyanite ester
DiCY expoxy
RCF+reinforceent
HF/SI FR4
HF-RCF
RCF-Epoxy
PTFE glass
HDI-FC film
PTFE epoxy
HF = Halogen free
PN = Phenolic-novalac
RCF = Resin coated foil
HF = High frequency
SI = Signal integrity
HDI = High density
interconnect
FC = Flip chip
DiCY epoxy
HF-RCF
Megtron
PPE
PN epoxy
RCF+RF
HF-FR4
PTFE/glass
HF epoxy
Polyimide
HF/SI-FR4
PTFE/epoxy
RCF
BT

FIGURE 4.6 Electrical characteristics of alternative PCB materials.

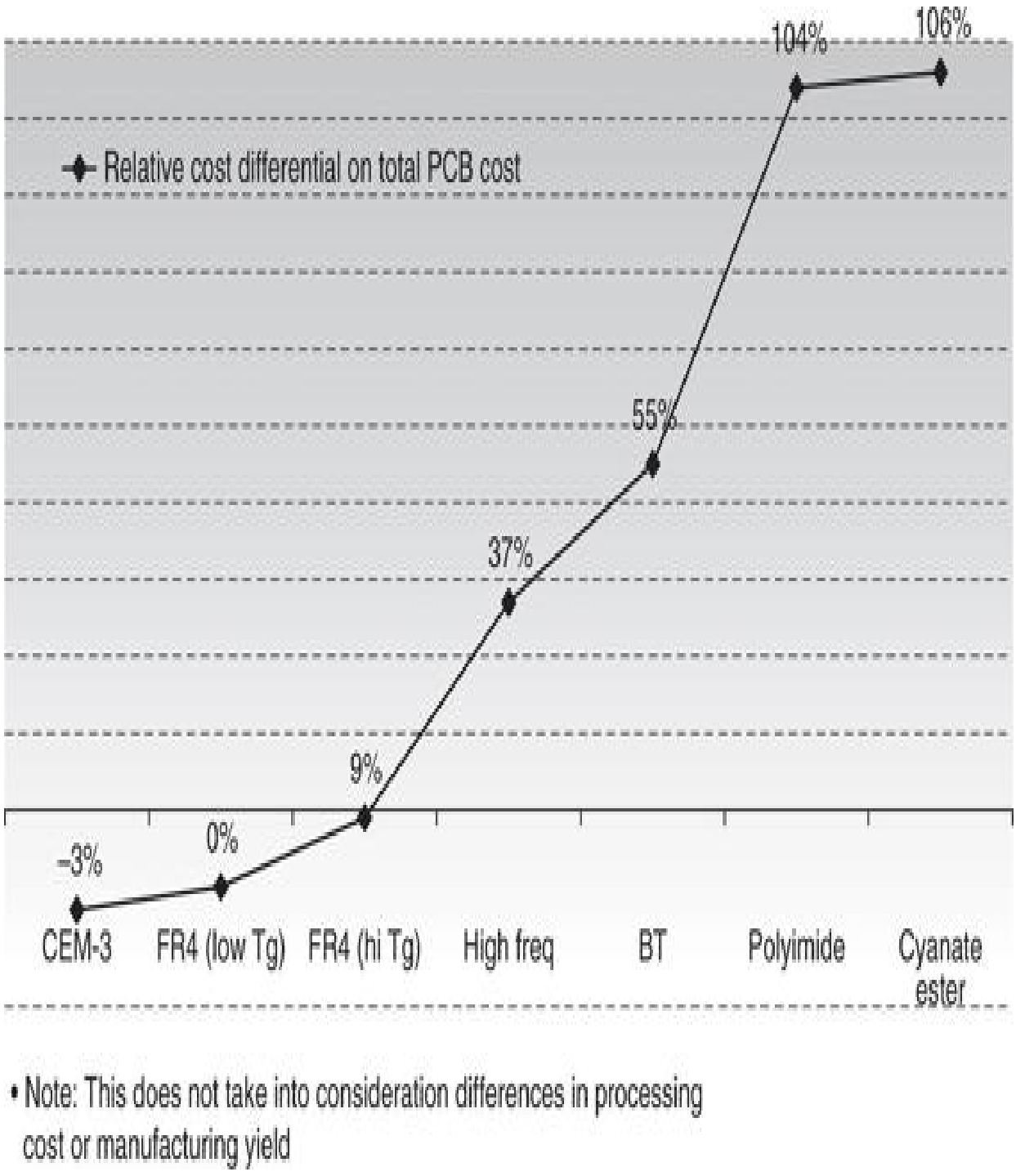


FIGURE 4.7 Effect of laminate type on double-sided PCB cost.

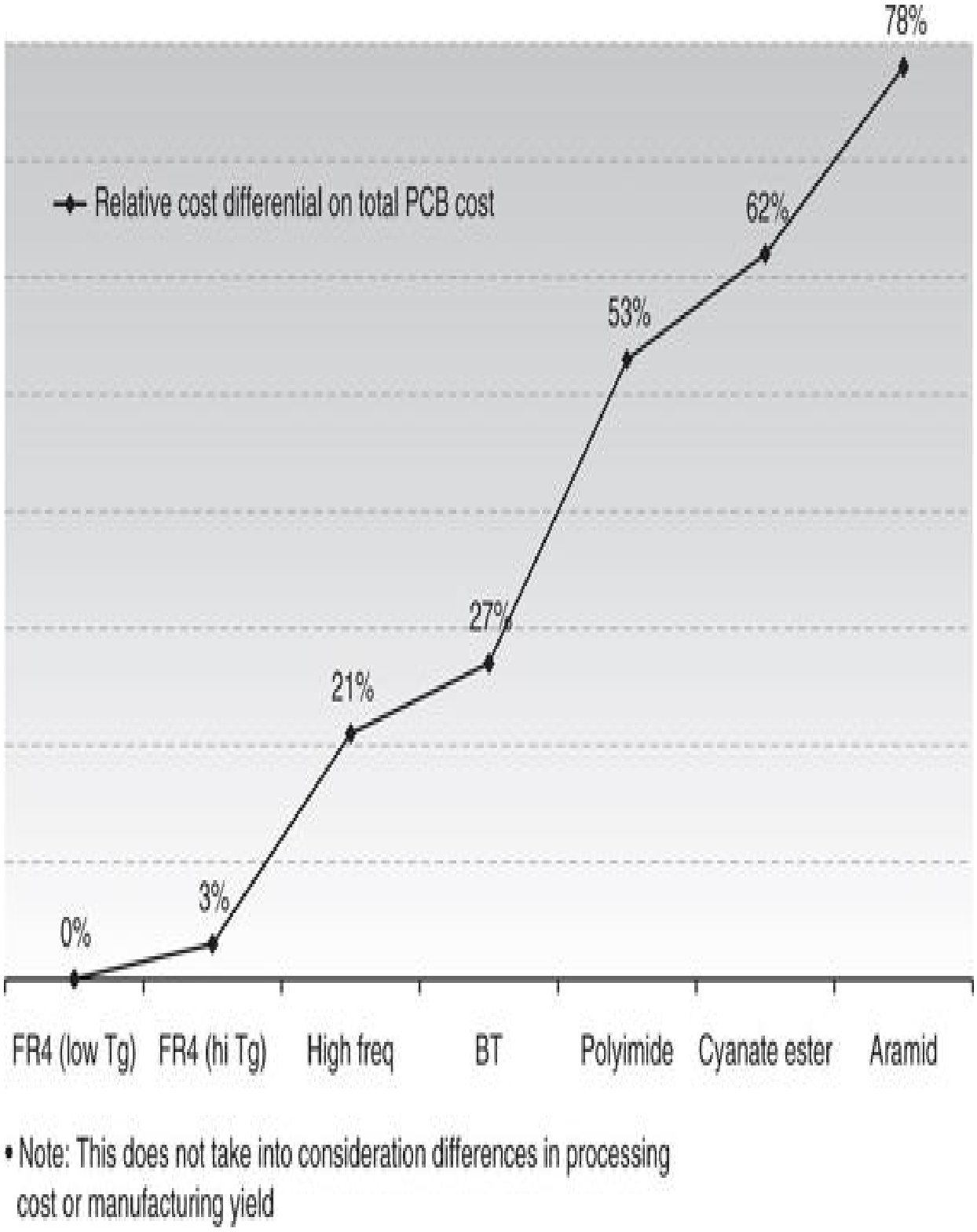


FIGURE 4.8 Effect of laminate type on multilayer PCB cost.

4.2.1.2 Board Size and Layer Count. These design elements determine how much material is used, and suppliers use these as the starting point for any price quote. PCB fabricators build panels and then cut them (depanelize) into individual boards, so there is an obvious advantage to maximize panel utilization since the customer is paying for the entire panel (see Fig. 4.9). Suppliers will work with their customers to optimize board dimensions, spacing between boards, and panel layouts using nesting and rotation to minimize unused space.

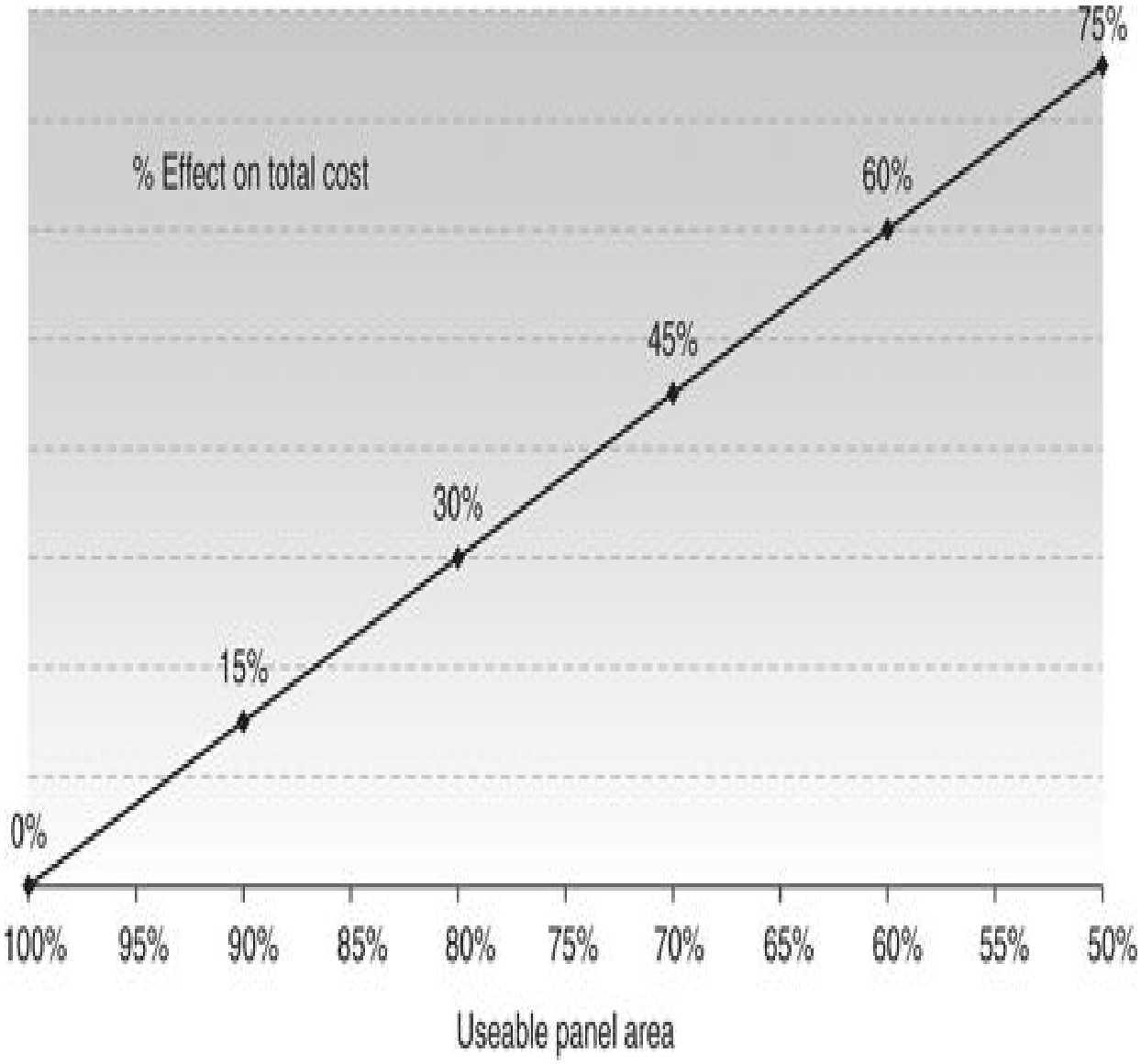


FIGURE 4.9 Effect of panel utilization on relative PCB cost.

Designers add layers to provide more area for signal routing, especially when overall board size is constrained.

Figures 4.4, 4.10, and 4.11 show the effect of layer count on price and the differential cost of adding two more layers.

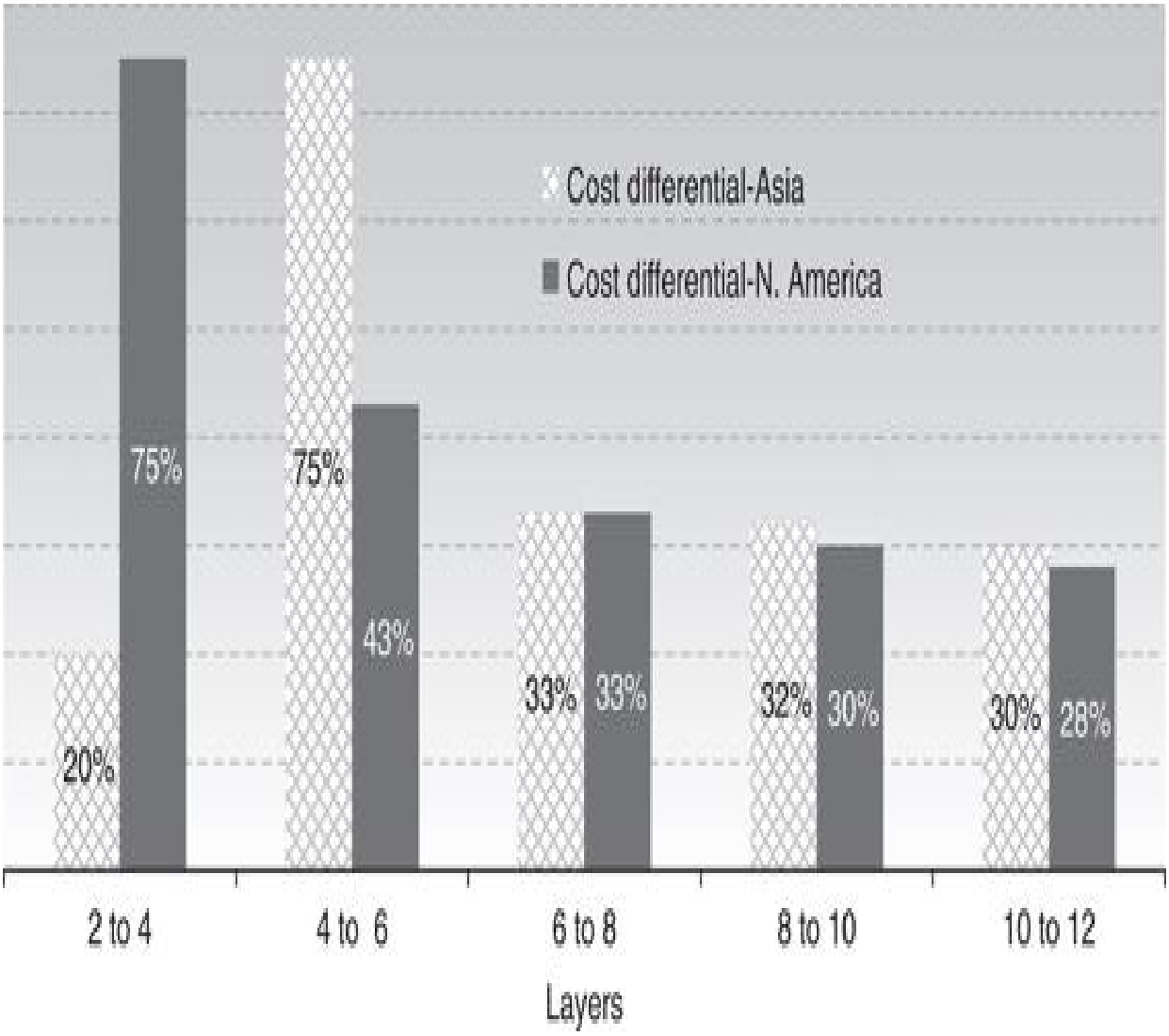


FIGURE 4.10 Cost differential for two additional layers.

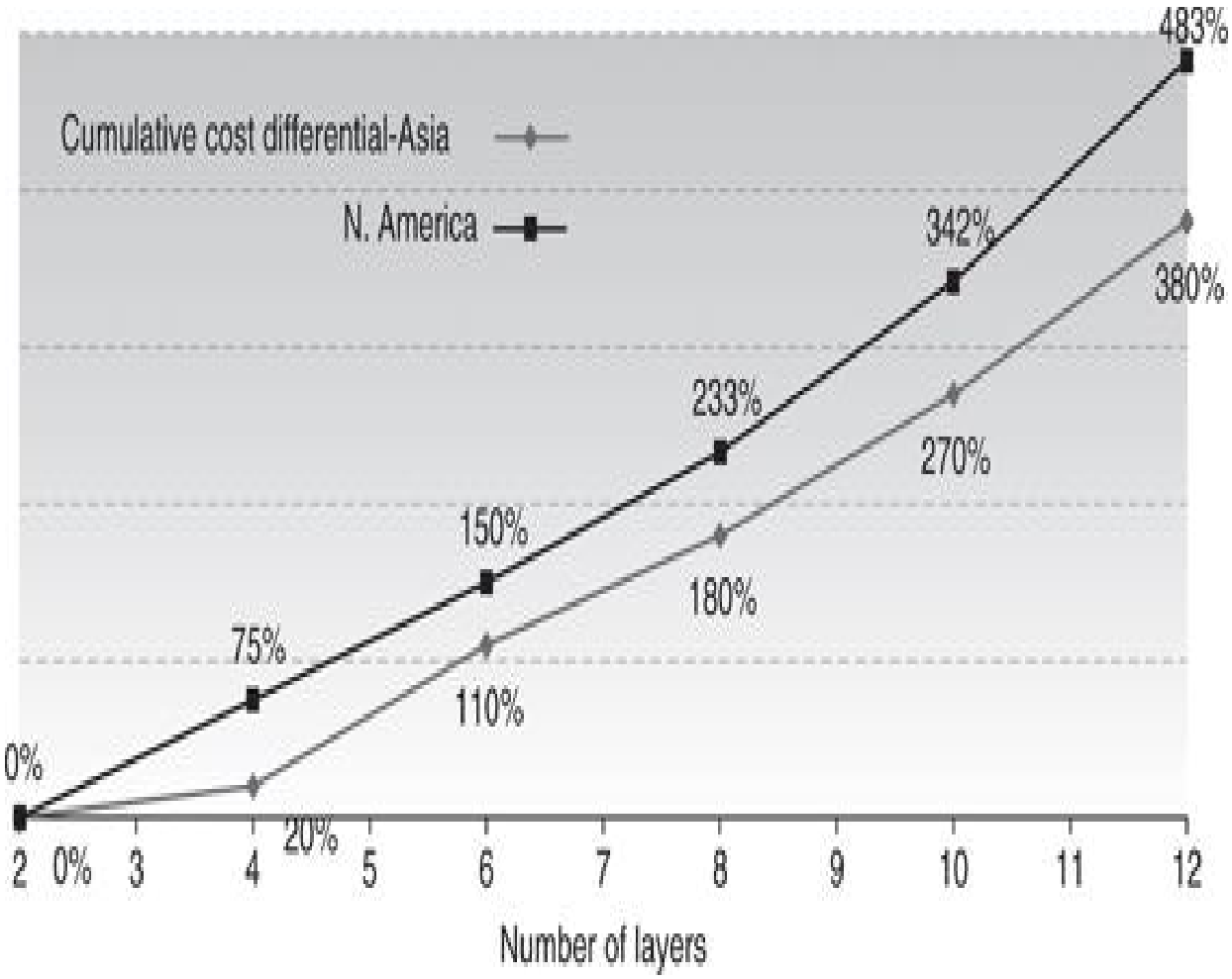


FIGURE 4.11 Cumulative cost differential compared to two-sided board.

Higher *board thickness* can contribute to higher PCB cost, in part because of the slightly greater amount of laminate required, but also because of the requirement of nonstandard thicknesses of copper-clad core material. See Fig. 4.12.

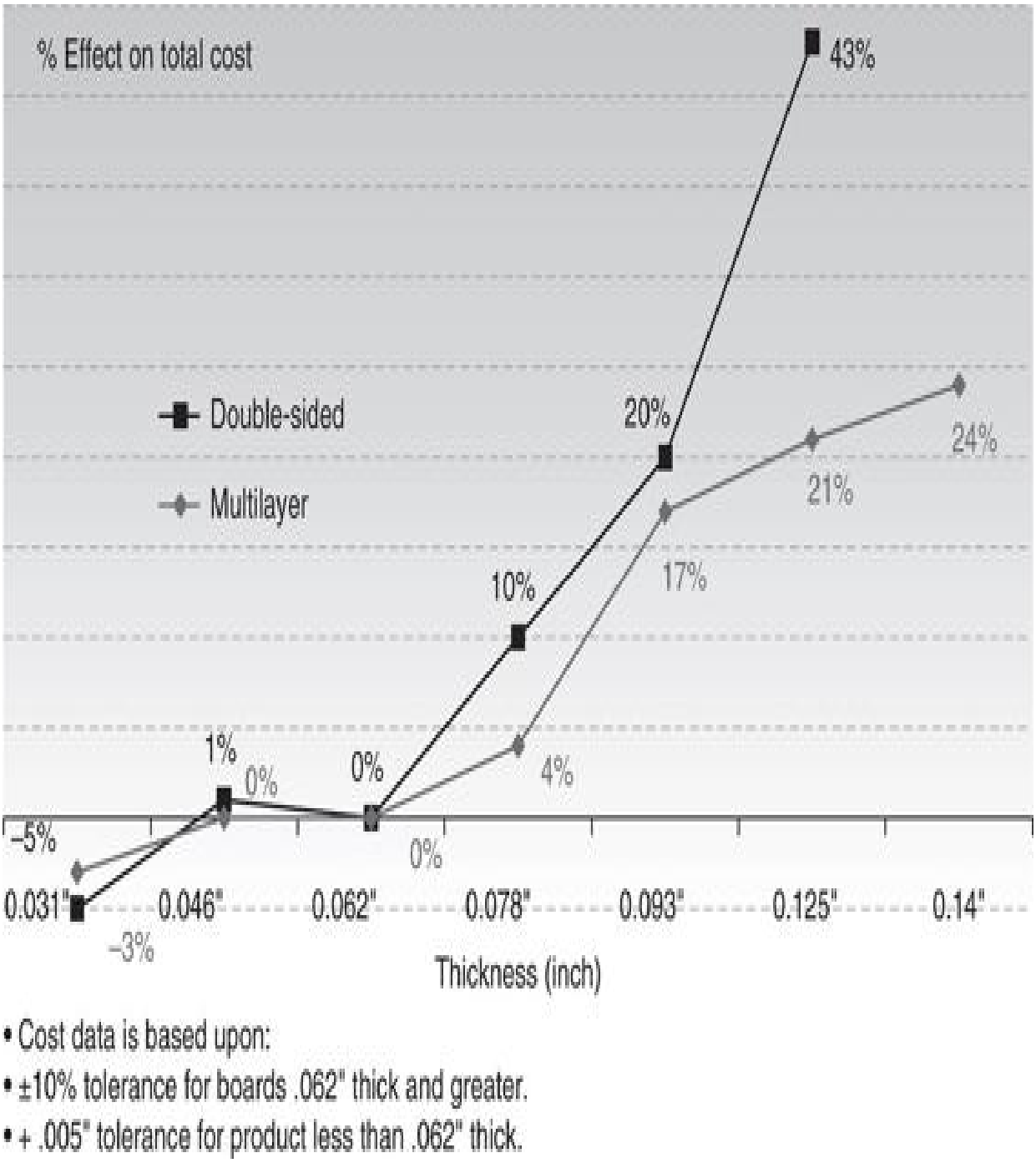


FIGURE 4.12 Effect of PCB thickness on relative cost.

Standard PCBs use copper as the primary conductive medium, but copper is relatively cheap and is rarely a material cost consideration, even for the thicker copper-clad materials used for high-current applications. The bigger impact of thick copper is to etching tolerance for smaller

features (see the discussion of production yield in Sec. 4.4). Common *surface finishes* have a slight impact on board cost compared with tin/lead solder applied by HASL, with the notable exception of gold (Figs. 4.13 and 4.14).

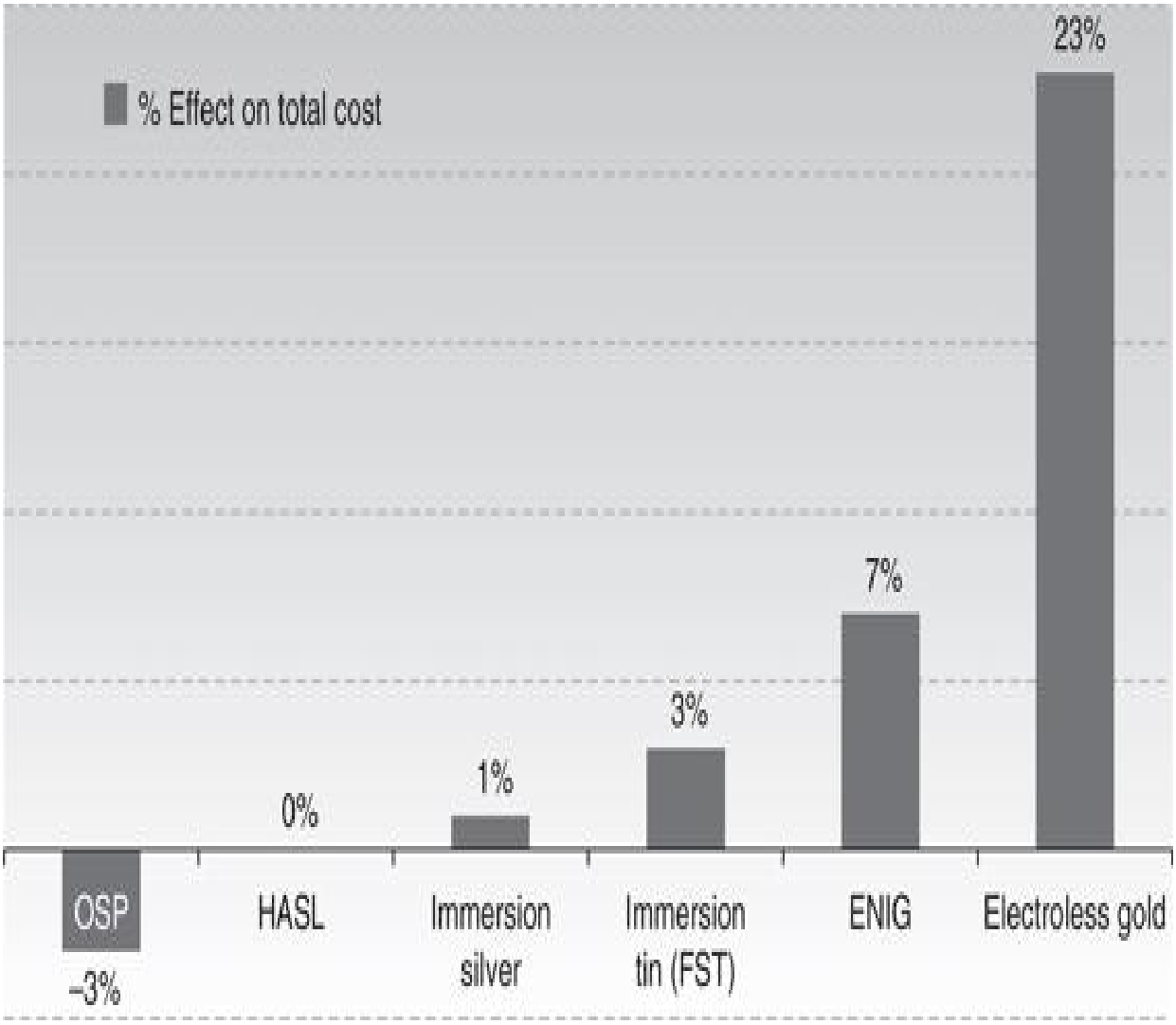


FIGURE 4.13 Effect of surface finish on relative PCB cost.

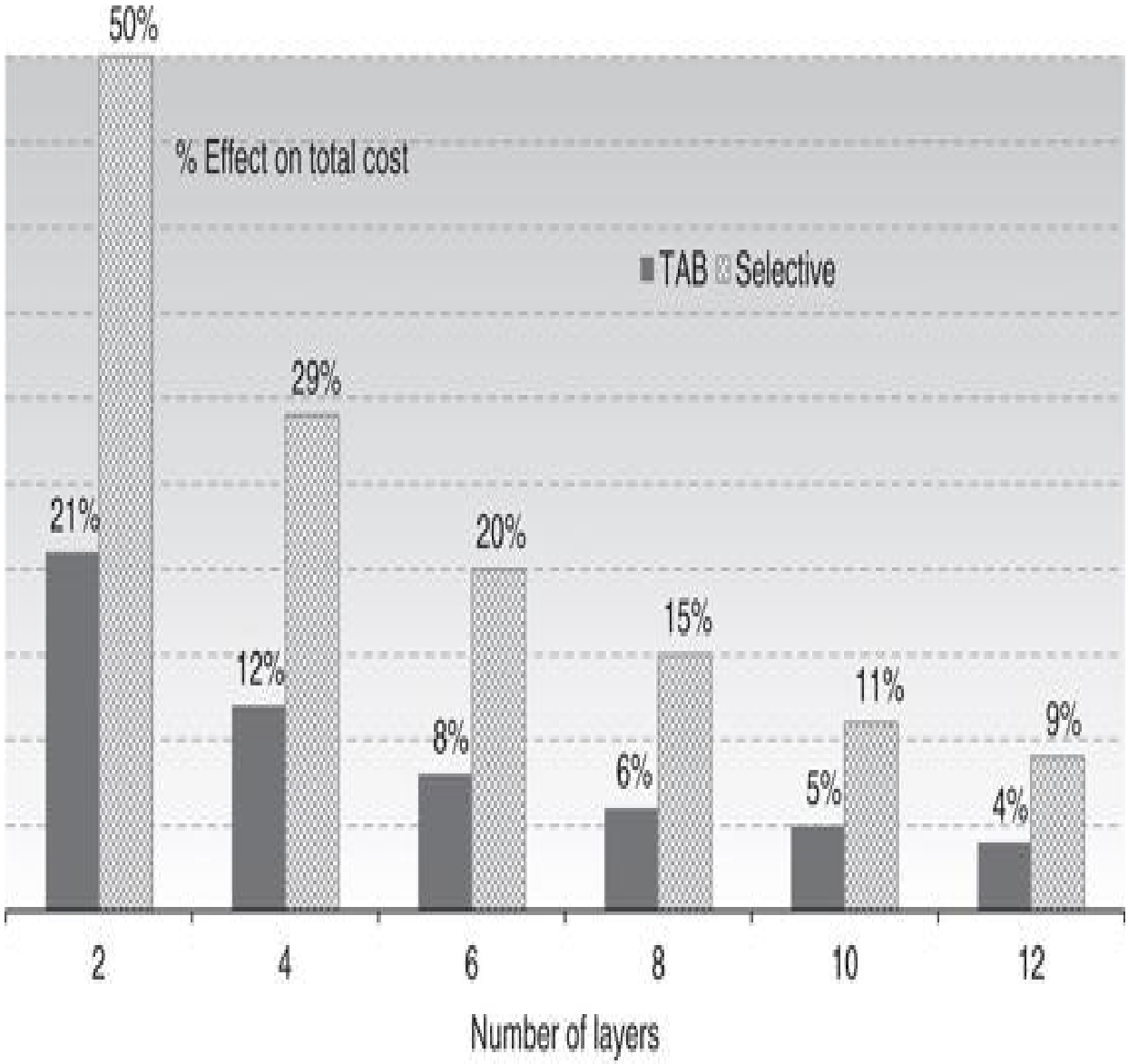


FIGURE 4.14 Effect of gold-plated fingers on relative PCB cost.

4.3 PROCESS COST DRIVERS

For a PCB factory, the logical production cost centers include

- Innerlayer processing (imaging, etching, inspection)
- Lamination
- Drilling
- Outerlayer processing (plating, etching, final surface finish)
- Soldermask
- Graphics printing
- Depanelization
- Final inspection and electrical test
- Other special processes (e.g., gold connector fingers)

For a PCA factory these are

- Solder paste printing
- Surface mount component placement
- Thermal reflow
- Through-hole component placement
- Wave solder
- Manual component placement
- Final inspection and electrical test

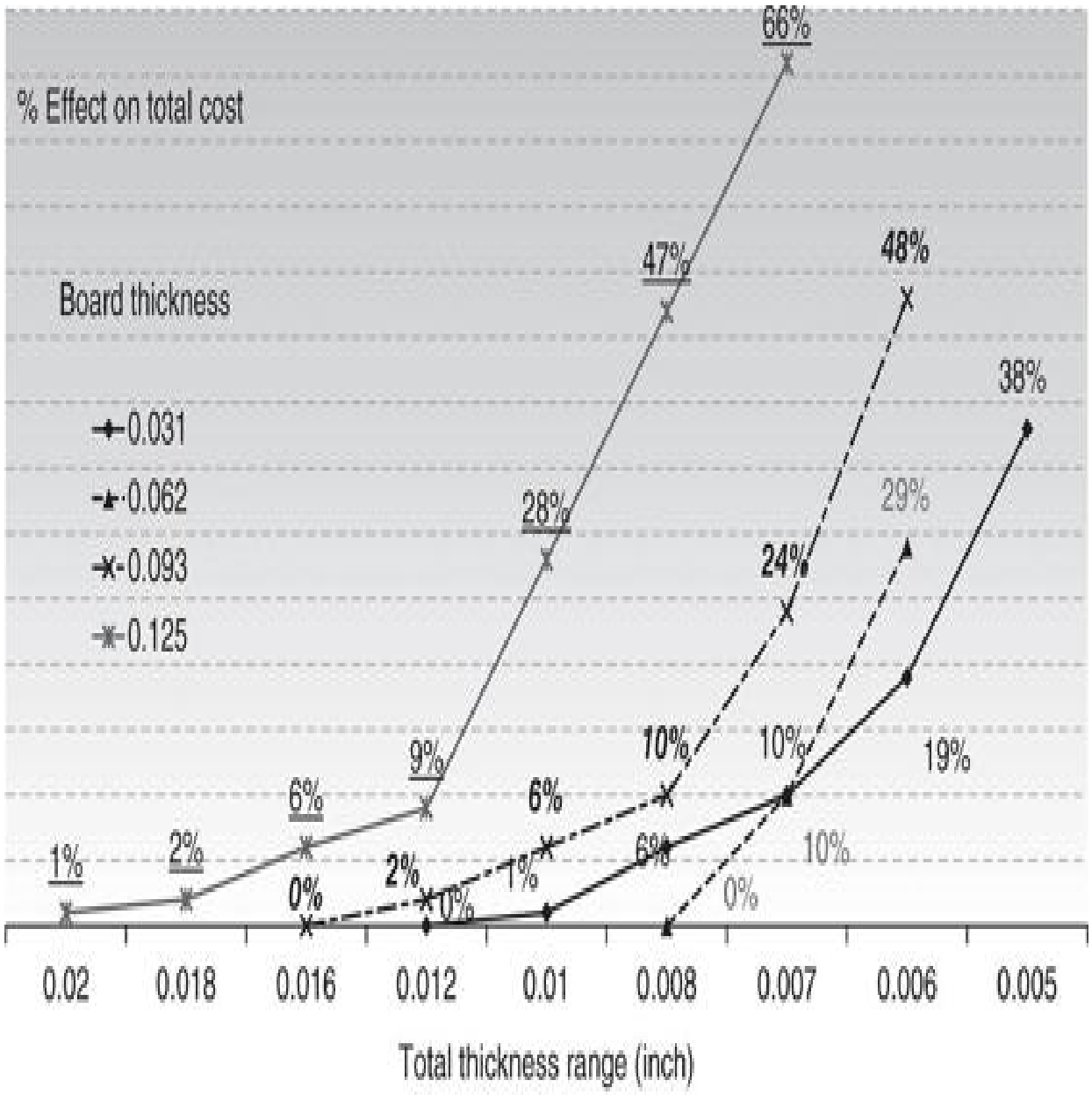
Standard processing defines a baseline for board pricing and is automatically accounted for in quoting models that use board area and layer count. Here are some examples of how the design contributes to total process cost for a PCB or PCA:

- Some board designs have to go through processes more than once. In the simplest case, the number of layers will determine how many times the innerlayer processing rate is applied. Double-sided surface mount assembly will require at least two passes through component placement and reflow. Buried or blind vias typically require sequential lamination.

- Since the drilling process cost is often expressed per hole, this cost will depend on the stack height, or the number of panels that can be drilled at one time, which in turn is based on the board thickness and minimum hole diameter.
- Most cost centers process full panels, so the more images or boards that can be designed on a single panel, the smaller the per-board process cost.

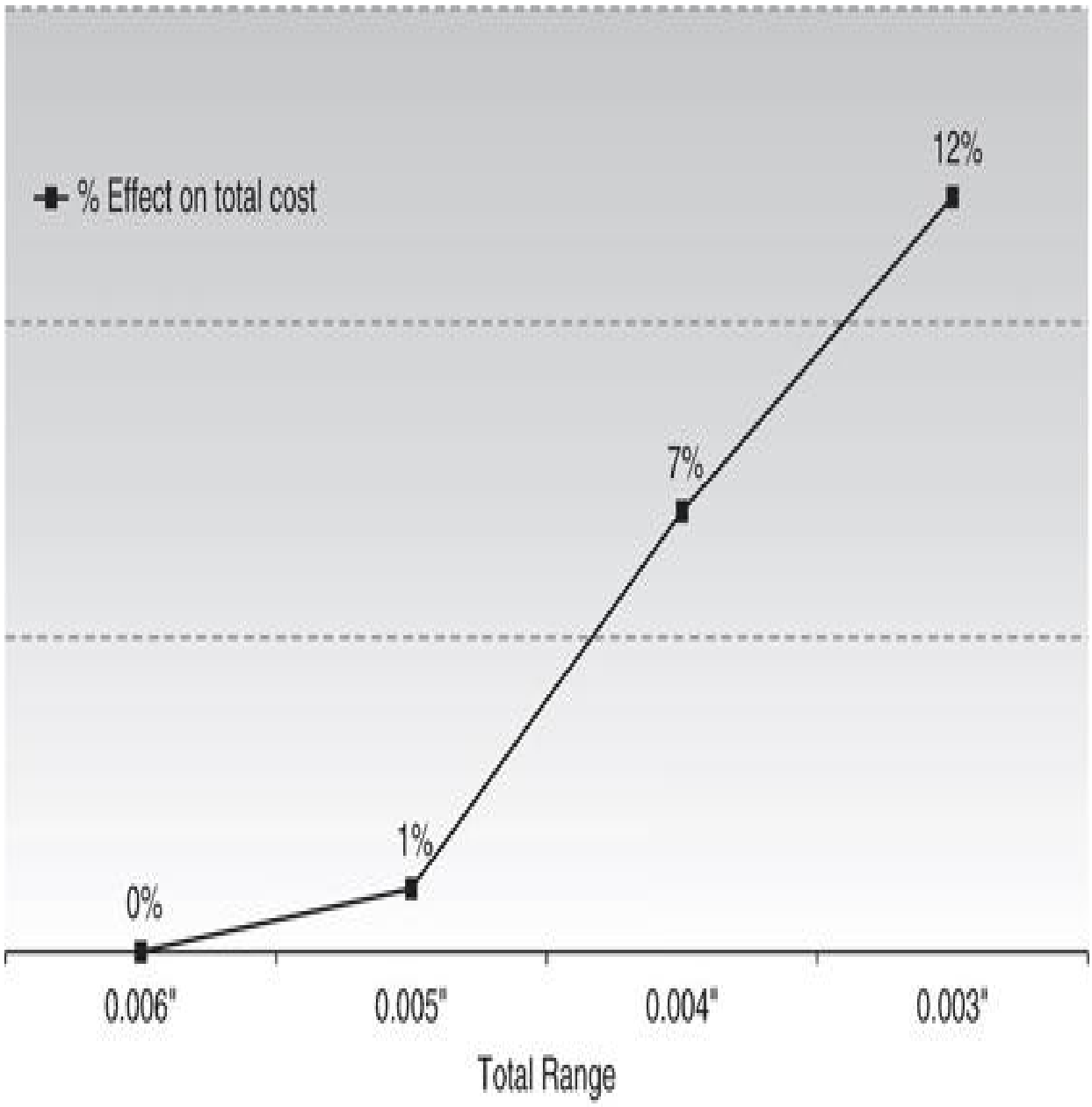
Note that one-time processes such as initial set-up and prints for soft tooling may be added as a charge to the first purchase order, or distributed over several orders.

Any additional PCB or PCA process steps that are not included in the standard pricing model will add to the cost, such as hole plugging, beveling, or plated edges or slots. This includes special processes that require greater control in order to achieve the required tolerances, such as board thickness, hole size, and controlled impedance applications (see Figs. 4.15, 4.16, and 4.17). Manual processes are obviously more expensive than automated ones because of the labor required. This includes manual taping or masking, manual depanelization, and manual placement of components that cannot be loaded into a pick-and-place machine.



- Thickness tolerance is based on the sum of the plus and minus tolerances.
- Ex: + .004/–.003 has a total thickness range of .004. "This data is derived from 4 layer product. The cost impact is more dramatic as the layer count increases.

FIGURE 4.15 Effect of board thickness tolerance on relative PCB cost.



• Total range is the sum of the plus and minus tolerances. Ex: +.002"/-.003" has a total range of .005". A .004" range and less require panel plating to ensure compliance to the tight finished hole size requirements. Cost data is based on a final board thickness of .062" and a maximum aspect ratio of 3:1.

FIGURE 4.16 Effect of finished hole size tolerance on relative PCB cost.

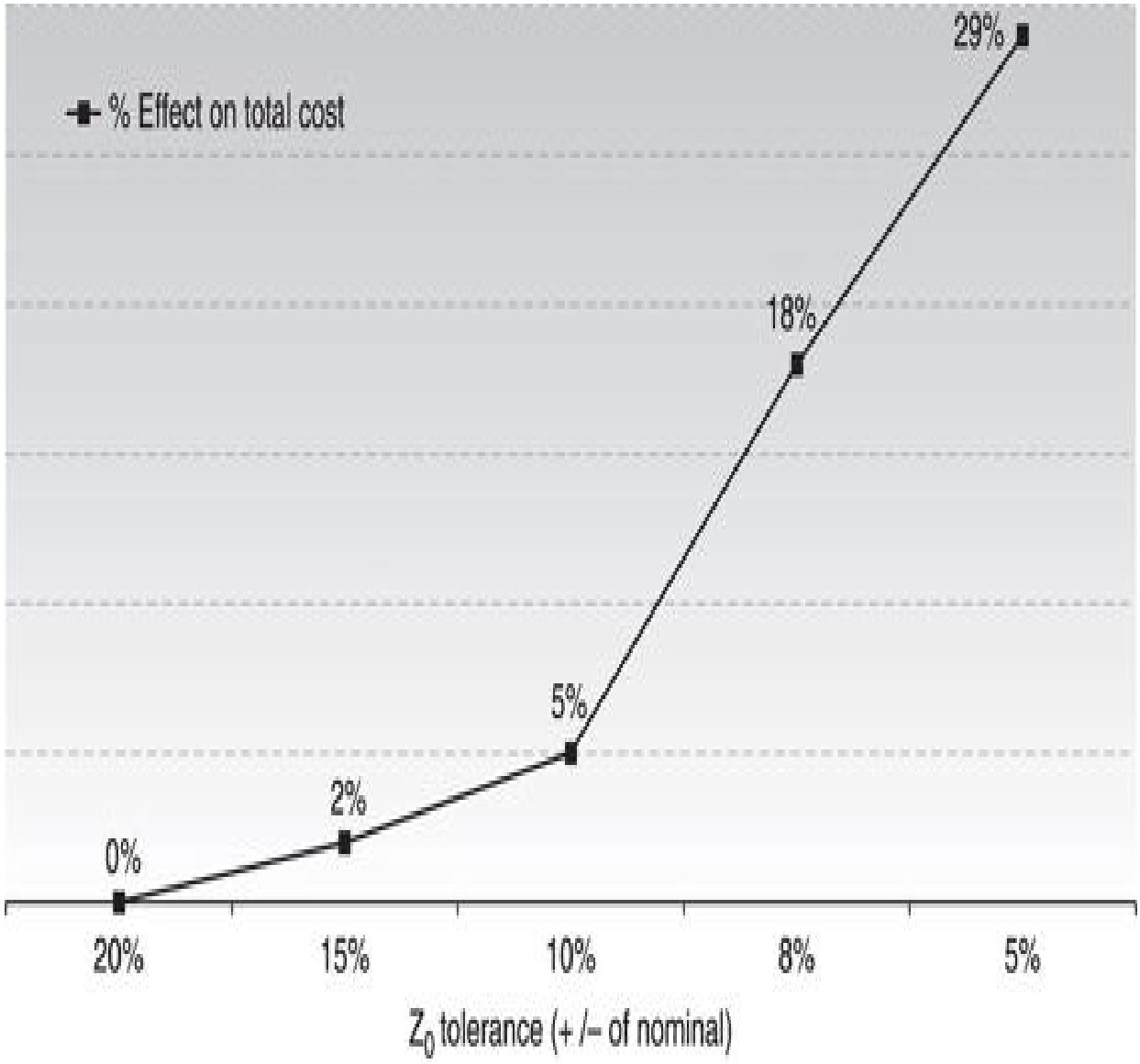


FIGURE 4.17 Effect of impedance tolerance on relative PCB cost.

4.4 PRODUCTION YIELD AND DESIGN FOR MANUFACTURABILITY

The concept of design for high-production yield or design for manufacturability (DFM) is not new, but early programs consisted of a collection of recommendations or best practices based on the experience of senior experts. The beginning of a more systematic approach to DFM can be traced to the pioneering work in the early 1980s by Geoffrey Boothroyd from the University of Rhode Island and Peter Dewhurst from the University of Massachusetts.[a,b] Their system analyzed each part in a mechanical assembly from the standpoint of

1. The necessity of its existence as a separate part (fewer parts are better)
2. Ease of handling, feeding, and orienting the part
3. Ease of securing the part to the base assembly

The results of this analysis were an estimate of assembly time and a rating for overall design efficiency, with the implication that higher design efficiency provides not just higher productivity, but also higher production yield.

Based on Boothroyd's seminars and studies on the cost of motions and joining methods, Hitachi's Production Engineering Research Laboratory (PERL) developed an Assemblability Evaluation Method (AEM) that rates the ease of assembly to get a quantitative score. General Electric obtained a license from Hitachi and added improvements.

The Hitachi/GE studies led to an assembly model that examines the manufacturing processes as a series of individual steps. The probability of introducing a fatal defect at each step is determined by the nature of the process and specific design elements. Penalty points are assessed to processes and elements that introduce difficulty, such as an operation that requires registration and alignment of several parts at once. A high final score suggests a low assembly yield, and multiple design options can be objectively compared.

Without DFM models, design engineers work independently to create specifications and requirements without regard for the capabilities of the intended manufacturing site. By the time problems are discovered it is often too late in the launch schedule to make changes, leaving the production team to struggle to meet yield, quality, cost, or delivery targets, and possibly risking field failures and long-term reliability issues.

With DFM, the design can be optimized for manufacturing without sacrificing performance, which leads to higher production yields, lower cost for the supplier (which usually means lower price to the customer), and a lower probability of defect escapes.

Unfortunately, while the Hitachi/GE models work well with mechanical assemblies and even PCAs, they are not very applicable to PCB fabrication. Summed algorithms are inappropriate for PCBs because of the statistical uncertainty associated with the individual process steps. Each step has a probability of introducing a fatal defect that depends on not only the design elements but also the result of previous steps.

Also, interactions and trade-offs between PCB design elements are difficult to characterize. For example, the diameter of drilled holes should be large to avoid the mass transfer limits of electroplating and the higher cost of reduced drill stack height. On the other hand, for a fixed pad size, a smaller via results in a larger hole-to-pad annular ring, which provides a margin for drilled hole breakout or reduced conductor width that can result from extreme misregistration (see Fig. 4.18).

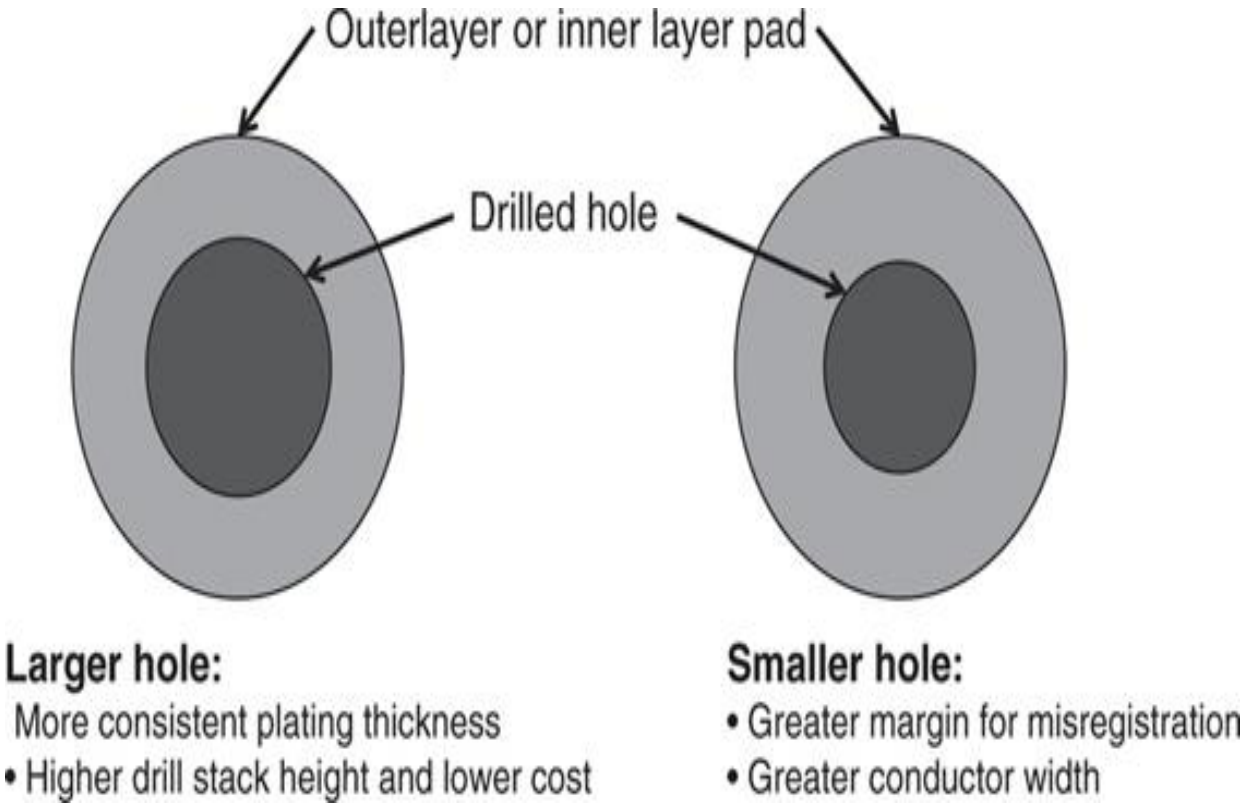


FIGURE 4.18 Bigger holes or smaller holes?

In this environment PCB designers and manufacturers use their intuition and judgment based on experience with similar boards, usually provided as best practices. These may take the form of a company-wide design standard, but most designers rely on IPC Standards to guide their decisions. See Fig. 4.7 for a list of some of the more common IPC Standards.

4.4.1 Design for Manufacturability Guidelines

Manufacturing yield depends entirely on the performance of the PCB or PCA supplier, which in turn depends both on both (1) the inherent capability of the production processes, and (2) the ability of the supplier to monitor and control those processes. Chapter 7, “Process Control, Monitoring, and

Incoming Inspection," provides details about what suppliers should be expected to do to manage their processes. However, because the predominant majority of PCB and PCA suppliers use the same basic manufacturing processes, it's possible to create a general set of guidelines that will maximize yield and thereby reduce cost, regardless of the supplier's quality management system.

PCBs and PCAs are typically inspected for cosmetic defects and rejected at the factory, but the most common reason for yield loss is failure at electrical test due to opens or shorts.

4.4.2 Design Decisions That Contribute to Manufacturing Yield Loss

- *Conductors*. A design with narrow lines and spaces requires better control over imaging and etching processes to maintain the required conductor cross section and remove all copper between conductors. This is a bigger problem with thick copper layers because the etching process may not be able to guarantee both (Figs. 4.19, 4.20, and 4.21). The probability of an open or short increases with the length of the minimum width conductor, so designers are advised to use narrow conductors only where necessary, and increase conductor width in areas of lower wiring density. (See Figs. 4.22, 4.23, and 4.24.)

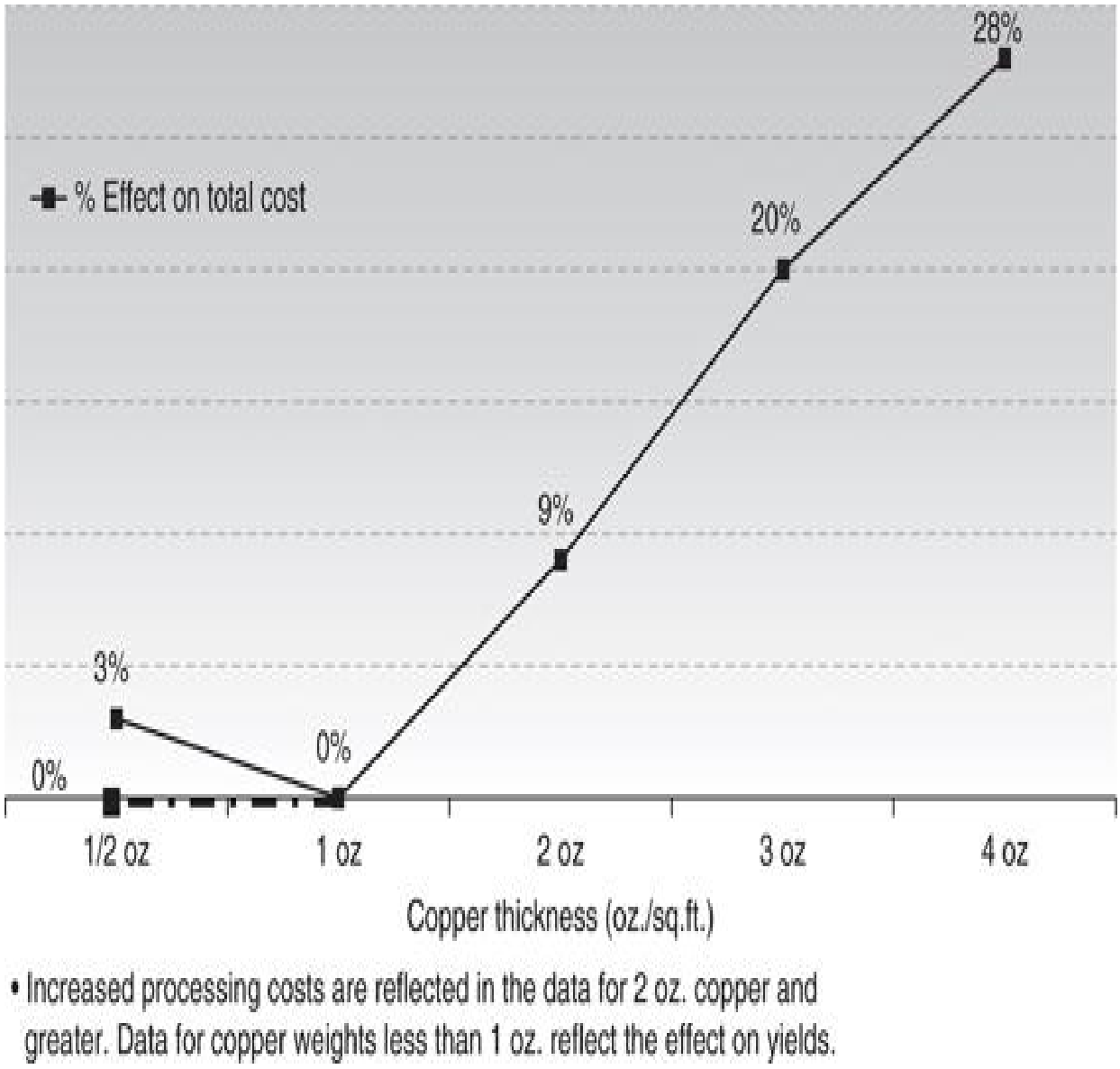


FIGURE 4.19 Effect of innerlayer copper thickness on relative PCB cost.

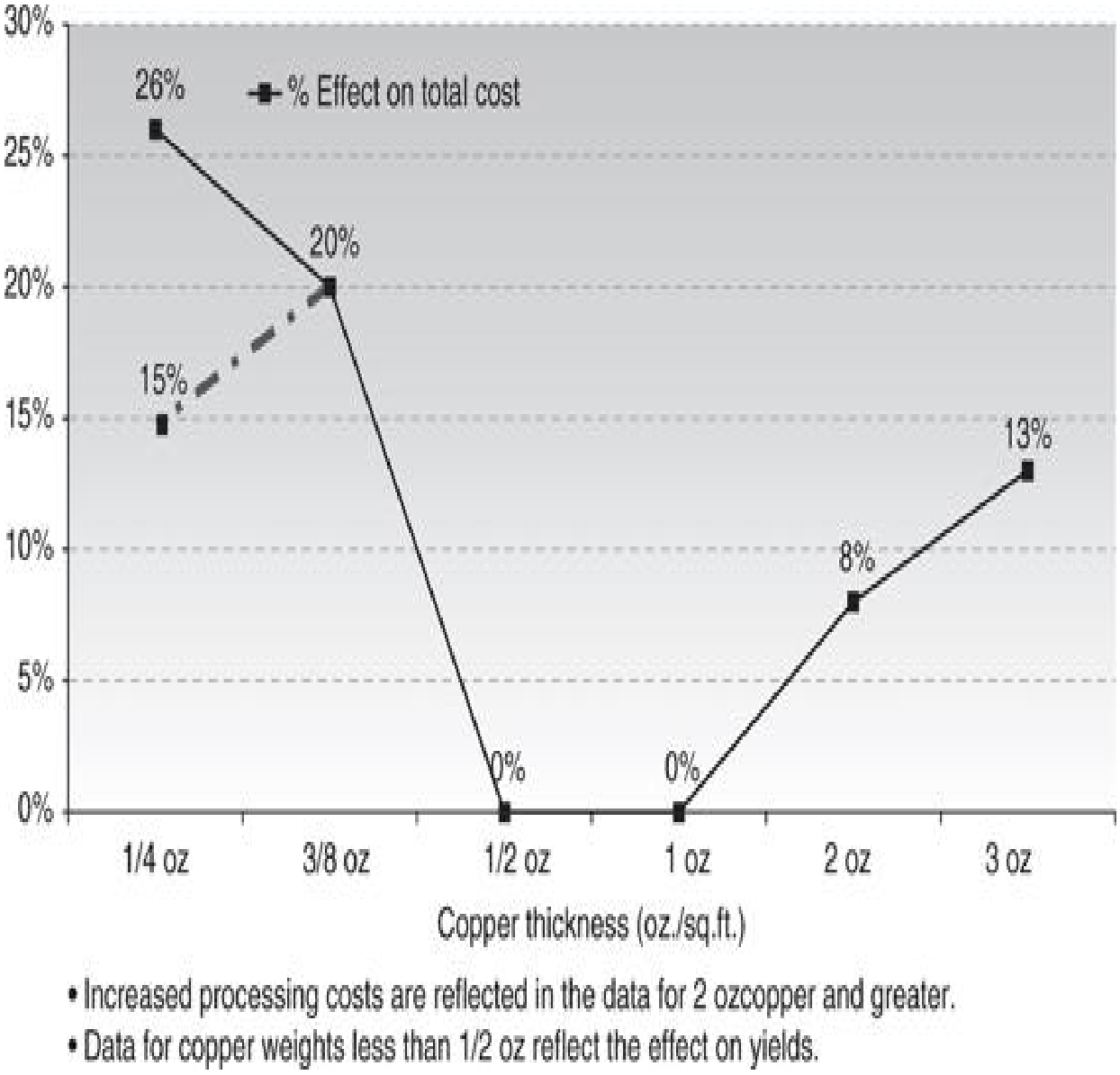


FIGURE 4.20 Effect of outerlayer copper thickness on relative 2-S PCB cost.

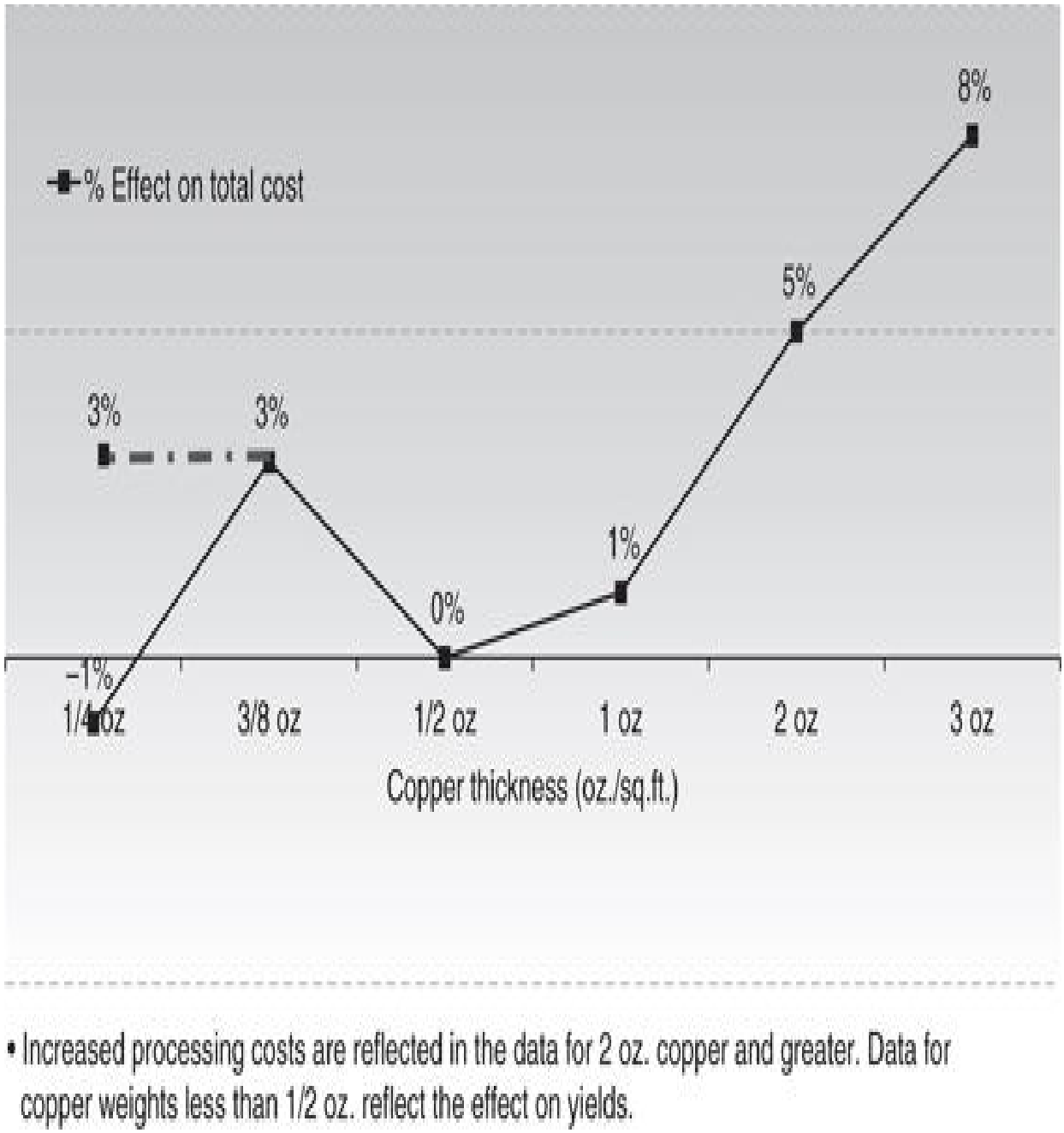


FIGURE 4.21 Effect of outerlayer copper thickness on relative PCB cost for multilayer board.

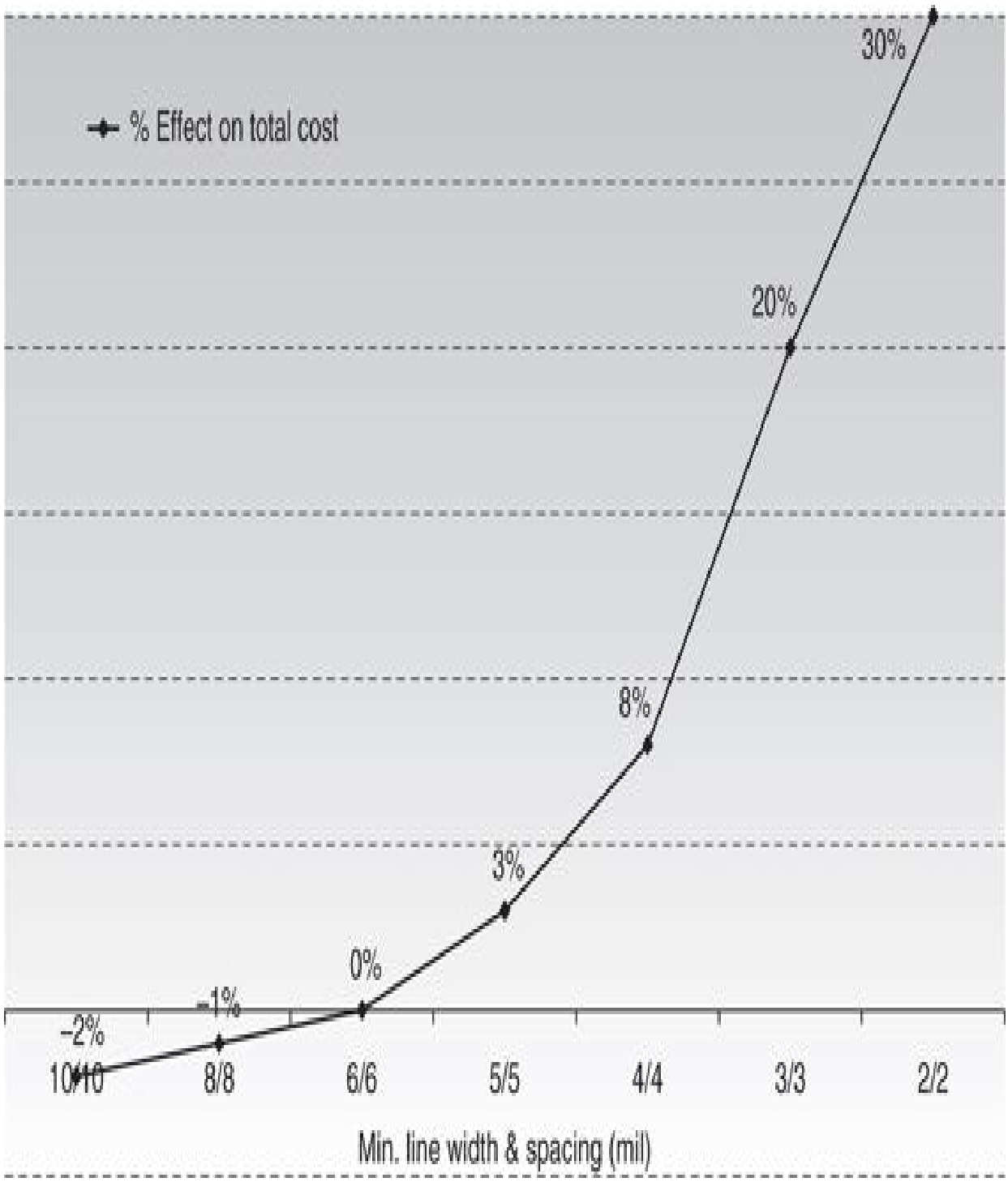


FIGURE 4.22 Effect of innerlayer line width on relative PCB cost for multilayer board.

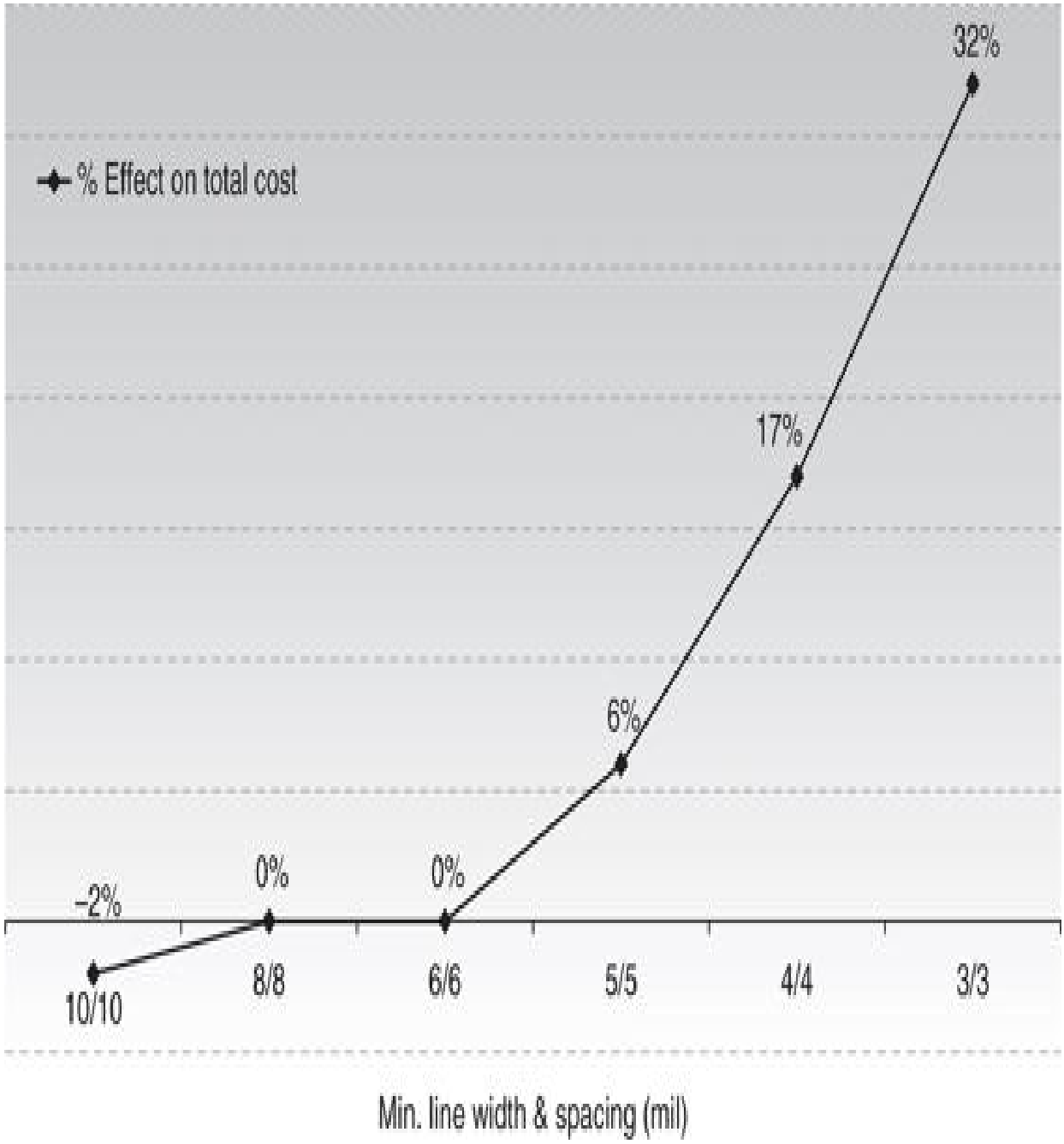
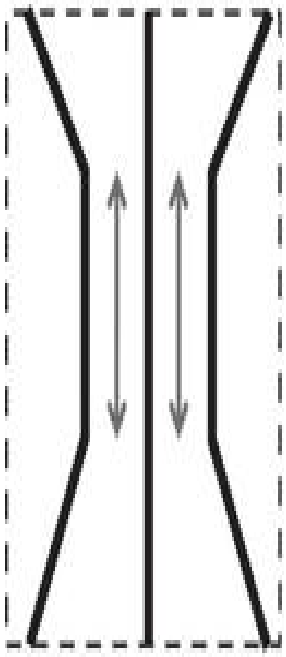
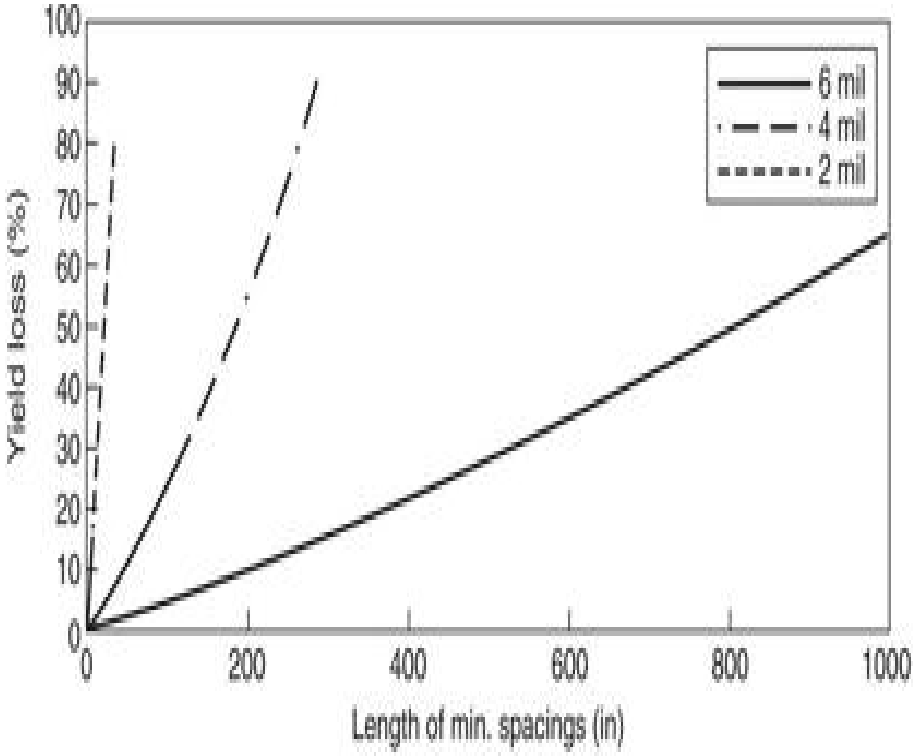


FIGURE 4.23 Effect of outerlayer line width on relative PCB cost for multilayer board.

Finer traces and spaces will be a cost driver



Length of minimum spacing



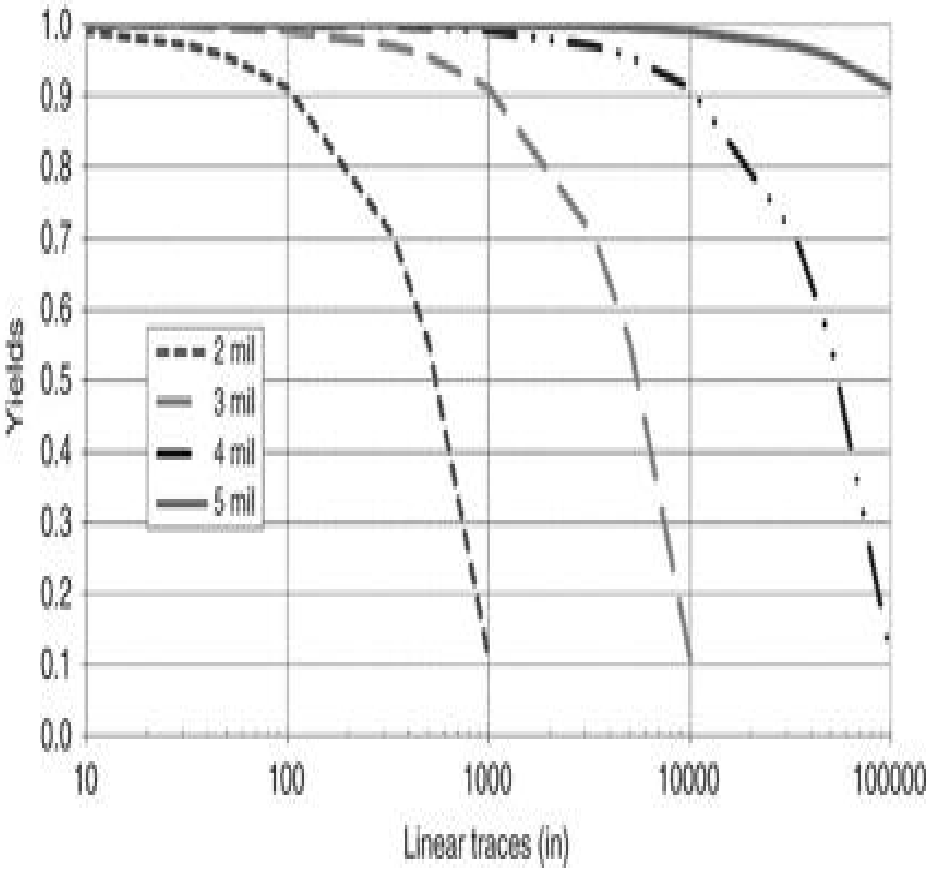
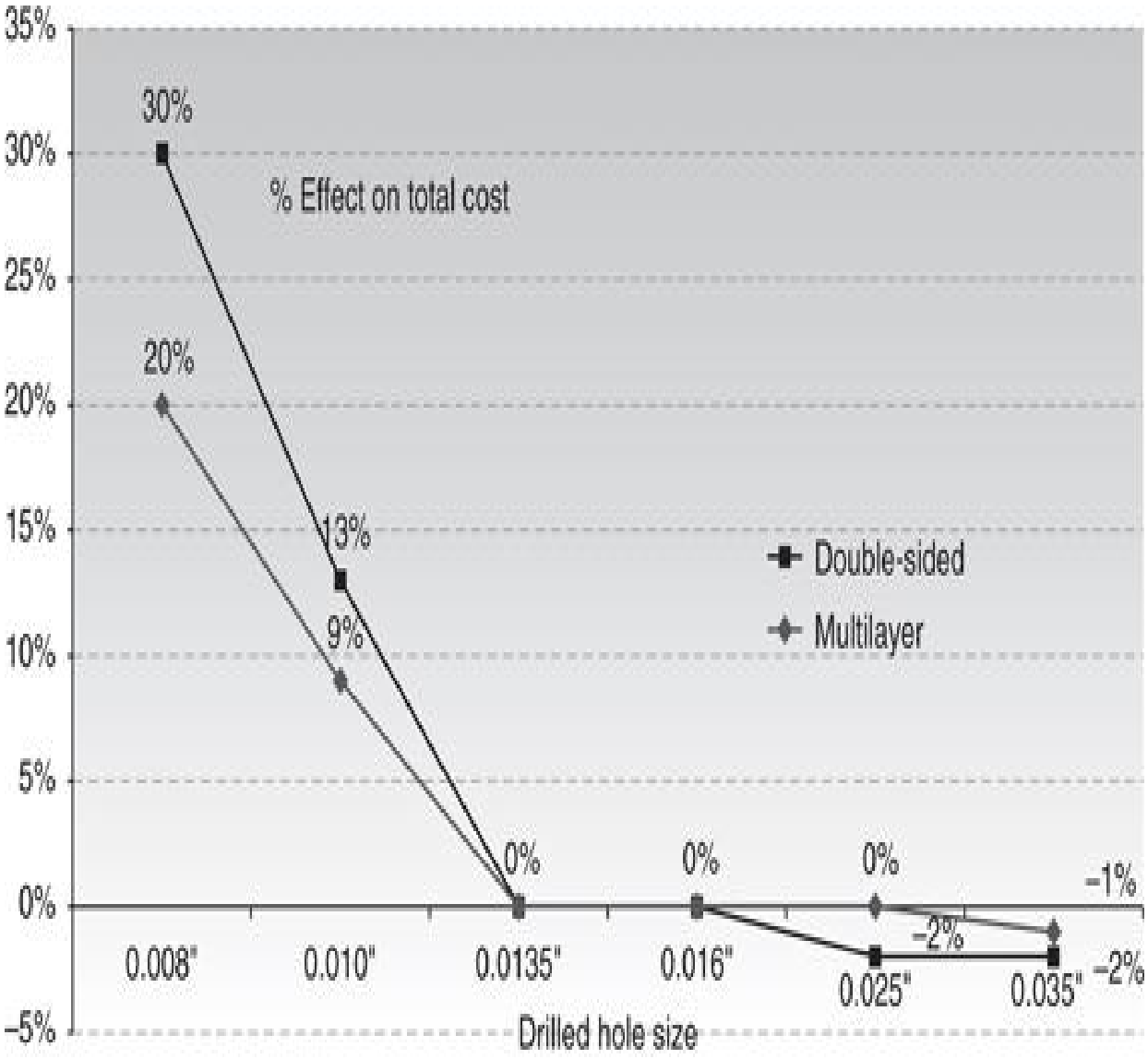


FIGURE 4.24 Effect of minimum trace length on relative PCB cost.

- *Vias and through holes*. Every drilled hole is a potential open or short, so designers are often cautioned to minimize total hole count. Smaller-diameter vias can provide more wiring density; however, it is more difficult to achieve the required plating thickness due to mass transfer limitations, especially for thicker boards (high aspect ratio). Drill bits for smaller holes are fragile and broken bits can damage the PCB. (See Figs. 4.25 and 4.26.)



• This data reflects the minimum drilled hole size in boards .062" thick.

FIGURE 4.25 Effect of minimum drilled hole size on relative PCB cost.

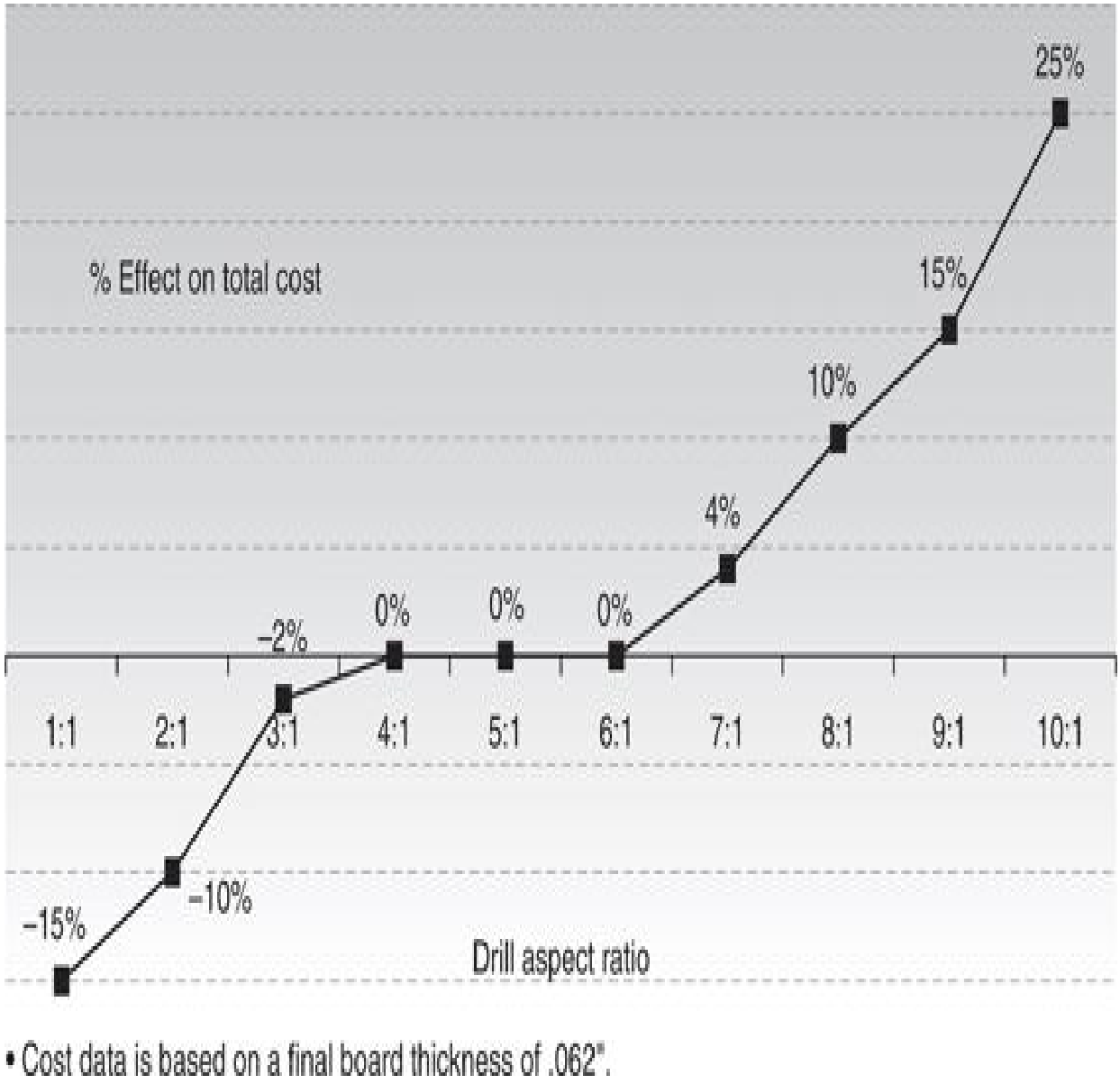


FIGURE 4.26 Effect of hole aspect ratio on relative PCB cost.

- *Via and through hole annular ring*. The pad surrounding a via or through hole needs to be big enough to maintain sufficient conductor width and allow some variation in positional tolerance for drilling and imaging. However, pads also take up valuable space on the PCB so there is a desire to minimize the annular ring around the drilled hole (Fig. 4.27).

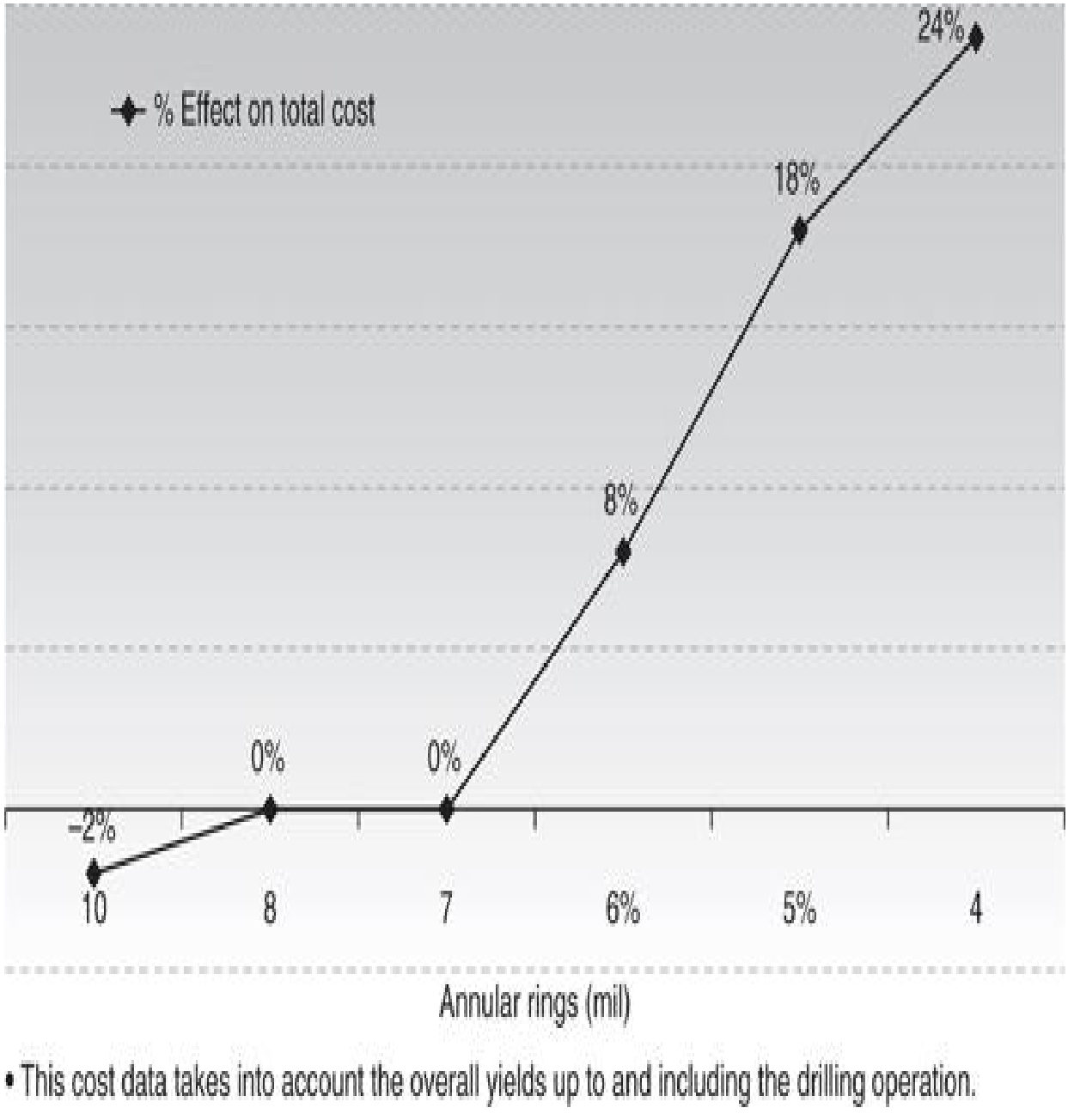


FIGURE 4.27 Effect of hole annular rings on relative PCB cost.

- *Fine pitch surface mount components*. Automated pick and place relies on fiducials to optimize location, but the narrower pads for fine pitch components means higher risk for misplacement and lead offset, which can lead to yield loss at the PCA assembler, or a less reliable solder joint in the field.

4.4.3 Common Examples of the Use of DFM and Cost Models to Optimize Designs

There are many scenarios that illustrate the use of DFM and cost models to optimize design for performance and cost. These include:

- *More layers versus larger PCB*. If the board size is not constrained by a standard card cage or other physical limitation, then the designer can provide more real estate for circuit routing either by adding more signal layers or increasing the size of the PCB. In most cases the added material and processing cost per layer is greater than the cost of the larger board area. This is particularly true if the PCB fabricator can offer multiple panel sizes to optimize material utilization.
- *Double-sided assembly versus larger PCB*. Board size can be significantly reduced if double-sided assembly is an option. In this case the cost of the larger PCB is compared with the additional processing cost for a second pass through the solder paste printing and reflow processes. These processes are generally highly automated with low operating costs, so double-sided assembly is usually the right choice here, assuming that the selected components are amenable to backside attachment on the PCA assembly line.
- *More layers versus higher wiring density per layer*. This is a trade-off between the higher material and processing cost per layer and the probability of higher scrap at the supplier due to failures at electrical test. The answer depends on the PCB supplier's process capability to deliver small features and narrow conductors at high yield. Production yield for a given minimum conductor width falls off sharply beyond the limit of the supplier's capability. If

the designer can stay within that “sweet spot,” it is better to increase wiring density than to add more layers.

- *Dedicated signal layers versus mixed signal/power/ground layers*. The standard for PCBs is ½ oz copper for outerlayers and 1 oz copper for innerlayers, but engineers and designers typically choose thicker copper for power and ground layers in high current applications. To minimize the total layer count, designers may use power/ground layers for signal routing, but production yields are lower when trying to etch small features with thick copper. Once again, the best solution is determined by the supplier’s optimum range of conductor width that matches their process capability.

4.5 DFM COMPLEXITY MODELS

In the late 1980s, Happy Holden, then with Hewlett-Packard, led a research study to create a model for predicting PCB first-pass production yield based on a set of design characteristics, including board area, layer count, minimum conductor width, and minimum via diameter. Rather than an additive model such as the ones based on the Hitachi/GE assembly studies, the PCB yield model recognized the cumulative and weighted interactions between design elements, expressed as a single “Complexity Index” metric. Designs with higher complexity would be expected to have a lower production yield. However, the yield for any given lot or order quantity could vary widely depending on factors such as handling, operator training, equipment maintenance, or other special causes of variability. *Complexity Index* will be defined in Chap. 16, “Planning for Design, Fabrication, and Assembly.”

The HP team measured actual first-pass production yields for a variety of PCB designs and developed a best-fit

regression model using the complexity index metric (see Fig. 4.28). The model predicts the highest-probability value of the production yield at a given manufacturing site that has a specific set of process capabilities. A different PCB fabricator with different capabilities would have its own regression model to predict yield for a given complexity index (see Fig. 4.29), which could be determined from actual yield data or parametric test coupons. Chapter 6, “Supplier Selection and Qualification,” describes some of these techniques in more detail.

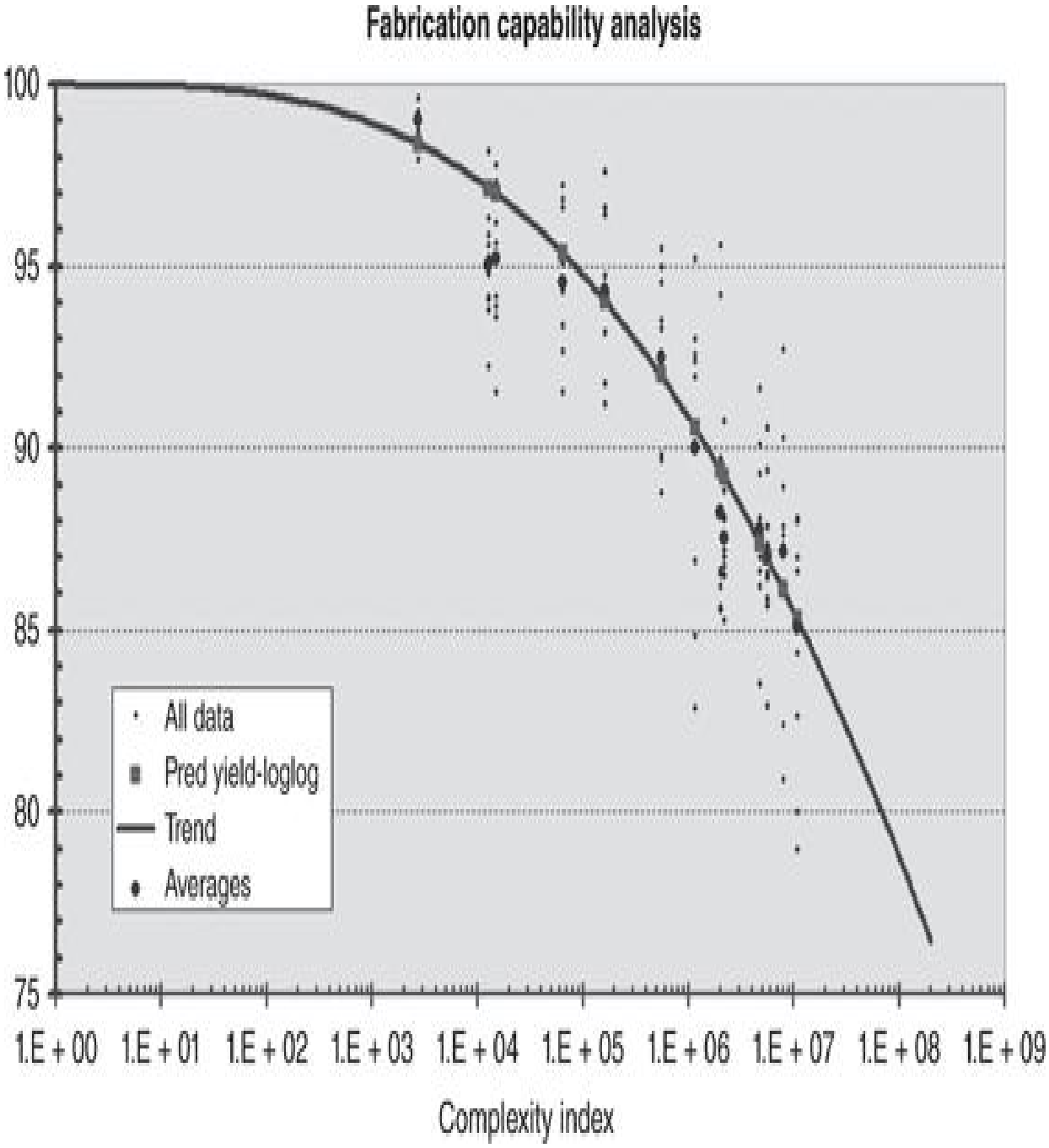


FIGURE 4.28 Example of predicted yield versus complexity index.

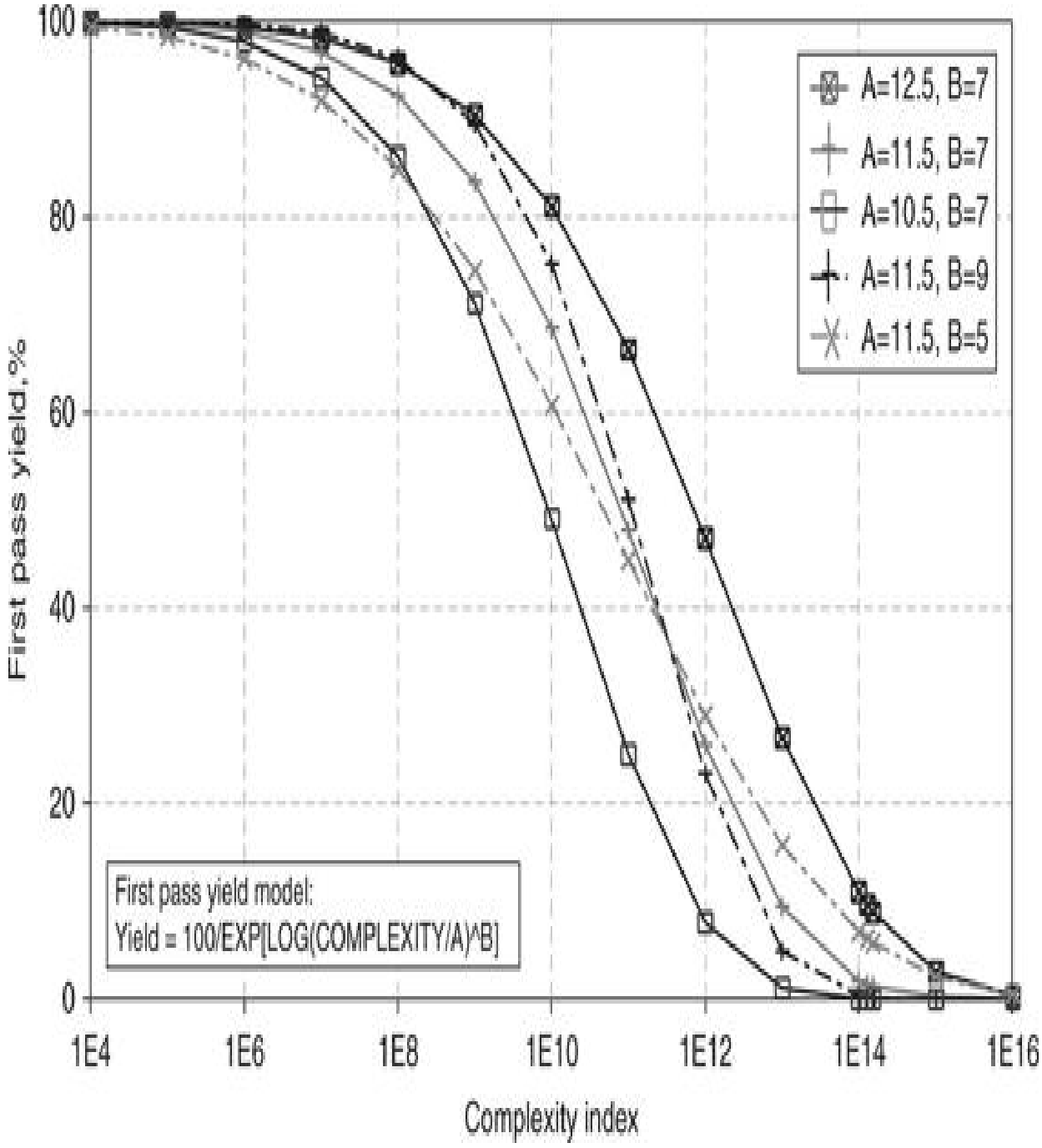


FIGURE 4.29 Yield-complexity models for different PCB fabricators.

4.5.1 Technology and Assurance of Supply

Some suppliers may be able to offer uncommon materials or manufacturing processes that provide desirable performance. However, optimizing the PCB or PCA design for a single supplier or a small subset of suppliers is potentially dangerous and places the sourcing strategy at risk. A more robust strategy includes an “open source” design with generally available materials and processes. This makes it easier to transfer to an alternate supplier if necessary.

At the same time, it is important for sourcing teams to follow the development and growth of new PCB/PCA technology. What is uncommon and exotic today may become mainstream tomorrow. Those who can successfully anticipate the broader availability of advanced interconnect technology will be able to give design teams high-performance options while protecting assurance of supply.

a Boothroyd, G., “Design for Assembly—A Designer’s Handbook,” Department of Mechanical Engineering, University of Massachusetts, Amherst, November 1980.

b Boothroyd, G., Dewhurst, P. and Knight, W., “Product Design for Manufacture and Assembly, 2nd Edition,” Marcel Dekker, New York, 2002.

CHAPTER 5

MANUFACTURING INFORMATION, DOCUMENTATION, FORMATTING, AND EXCHANGE[a]

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

5.1 INTRODUCTION

This chapter presents the elements of needed manufacturing information, documentation, data exchange, the data exchange process, its pitfalls and best practices, the most widely used data exchange formats and their main characteristics, and evolution drivers in data exchange.

The electronics manufacturing marketplace is a dynamic domain where supply chains of trading partners compete in a global economy in which time to market and efficiency are key factors for success. Data communication is a vital key to supply chain management. Efficient and accurate data exchange is an extremely important factor in customer supply networks.

The challenge of more efficient and accurate data exchange has only recently begun to be addressed and the future for data exchange improvements holds much potential.

The manufacturing of printed circuit boards (PCBs) and assemblies (PCAs) begins with the soft PCB information process. This process is the transformation of customer computer-aided design (CAD) data and specifications into the necessary tools required for manufacturing the bare PCB and populating the assembly. The typical tools required for manufacturing PCBs include artwork for photo printing of inner conductive layers, outer conductive layers, and solder mask patterns. Artwork is also created for screen-printing patterns for nomenclature and via plugging layers. Additional tools required include drill and routing numerical controlled (NC) programs, electrical testing netlists and fixtures, and CAD reference soft tools.

The PCB Information process for assembly requires assembly drawings, bills of materials (BOM), and schematic or logic diagrams, and includes the solder-paste stencil design, assembly array layout, and the resulting computer numeric control (CNC) programs for component placement, in-circuit test program creations, and possibly the creation of a functional test program. Many of these procedures will be covered in subsequent chapters in Part 8 “Assembly, Soldering Materials, and Processes” of this handbook.

During the PCB information process, the customer part numbers are analyzed to determine the compatibility of the design features with the manufacturing process capabilities. Additionally, attempts to optimize the manufacturing of the product at the lowest cost are a primary goal. However, the majority of the costs have been defined before the design is transmitted to the manufacturing site by the PCB designer. An early investment in time by the PCB design team and the manufacturing PCB information team can result in the most significant savings in overall product cost.

This chapter describes the PCB information exchange process, as defined in Fig. 5.1, including the transfer of information, design reviews, optimization of materials, definition of BOM and routings, tool creation, and additional processes that are required.

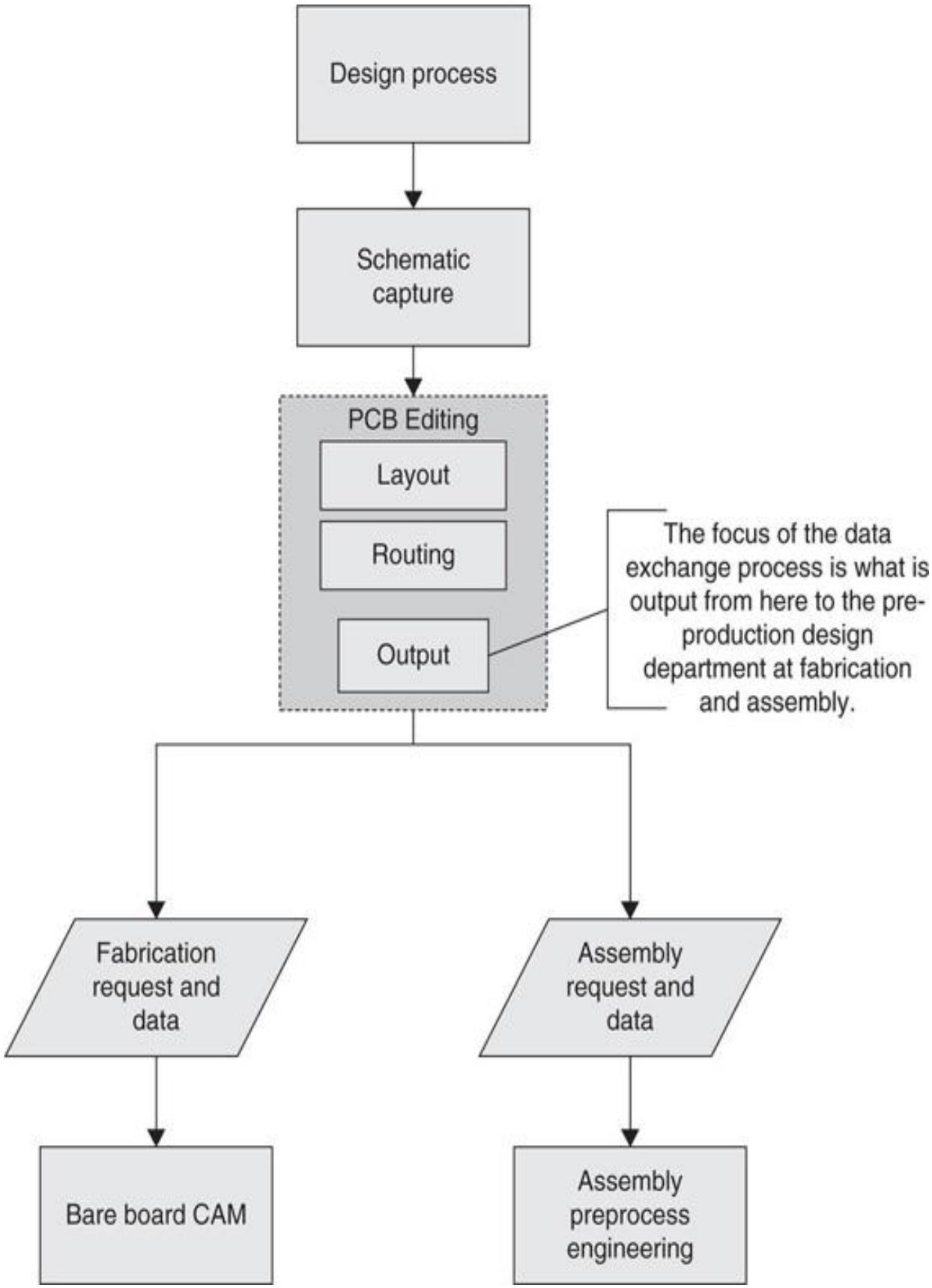

Design process
Schematic capture
PCB Editing
Layout
Routing
Output
The focus of the data exchange process is what is output from here to the pre-production design department at fabrication and assembly.
Fabrication request and data
Assembly request and data
Bare board CAM
Assembly preprocess engineering

FIGURE 5.1 The soft-PCB information process (computer-aided manufacturing [CAM]) for PCB fabrication and assembly).

5.2 MANUFACTURING INFORMATION

The information process begins with the receipt of information from the design department. Unfortunately, although the time required to send information to the manufacturer has decreased to minutes or hours from day(s), a significant issue with the provision of packages to manufacturers is the completeness of the information provided.

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has a new document, IPC-2610, that defines a complete documentation package, including the following:

- IPC-2611, “Generic Requirements for Electronic Product Documentation”
- IPC-2612, “Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)”
- IPC-2613, “Sectional Requirements for Assembly Documentation (Electronic Printed Board and Module Assembly)
- IPC-2614, “Sectional Requirements for Board Fabrication Documentation (Printed Circuit Board Description Including Embedded Passives)”
- IPC-2615, “Sectional Requirements for Dimensions and Tolerances”
- IPC-2616, “Sectional Requirements for Electrical and Mechanical Part Descriptions (Specification and Source Control Part Descriptions)”
- IPC-2617, “Sectional Requirements for Discrete Wiring Documentation (Wire Harness, Point to Point and Flexible

Cable Descriptions)”

IPC-2618, “Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, and Procurement Documents)”

Timely PCB Information of a part number depends on having the correct information. All features required to exist on the PCB must be defined for the manufacturer. The information is defined via design data, drawings, and textual information. Automated data are encouraged whenever possible.

5.2.1 Required Information

In addition to PCB design data, copious information pertinent to board manufacture is exchanged between partners in the manufacturing and assembly process. Such information can include standard compliance requirements (e.g., UL) statements of workmanship (SOW), and delivery and packaging instructions. Modern data exchange formats address some of these comprehensive data exchange issues. The design-to-manufacturing data exchange process should ideally progress to become online collaboration. The drivers of this progression are globalization, the supply chain, and time-to-market pressure.

Historically, the PCB design-to-manufacturing flow began with manually laid-out artworks whose images were printed on copper-clad laminates and developed, etched, and stripped within the same vertically integrated organization. Advances in miniaturization and multilayer board technology led to the need for specialization, and outsourcing of bare board fabrication became the norm. Together with advances in PCB fabrication tools and digital communication, the outsourcing supplier communication advanced from courier delivered artwork to data tapes and disks and later to

electronic transfer over modems and finally over the Internet. Globalization and outsourcing continue to push the envelope of electronic business communication in the PCB industry as well as everywhere around us.

The PCB fabrication tools driving the history of data exchange are mostly imaging tools and placement machines. PCB lithography began with hand-routed artworks and continued with photo plotters, aperture wheels, and computerized numerical control (CNC). Gerber Scientific was the most successful of the early photo-plotter vendors, and hence the Gerber 274D format caught on.[1] Later these were replaced with laser plotters without aperture wheels, but the Gerber data format remained the "lowest common denominator" format. In the PCB assembly arena, robotic assembly machines of varying complexities succeeded hand assembly. This trend led to the need for electronic assembly data, just as the artwork-to-laserplotter development in board fabrication led to the need for electronic fabrication data.

Bare board fabrication and board assembly share some common data elements but also have distinct data needs. Examples of common elements are the outer circuit and mask layers and through-drill information. Unique data elements are, for example, inner layers for board fabricators and component placement locations and functional component descriptions for assembly houses. All these data elements are described in the next section.

The information and common data formats required to permit the PCB information of the PCB include the following:

- *Part number information*

  Information: This information defines the part number to be built, including revision number, releases, dates, etc.

  Format: This information is typically provided in the part drawing or may be provided as an additional text file.

- *Fabrication drawing*
  Information: This drawing describes the unpopulated printed board and all features that become part of the board. It may contain specific design requirements such as material requirements, multilayer stack-up diagram, dielectric separation between layers, controlled impedance requirements, solder mask type, nomenclature color, location, size requirements for the fabricator's ID, Underwriter's Laboratories (UL), electrostatic discharge (ESD), country of origin, and dimensional tolerances, as well as testing and electrical performance expectations. The dimensional datum (see Fig. 5.2) should be clearly identified.

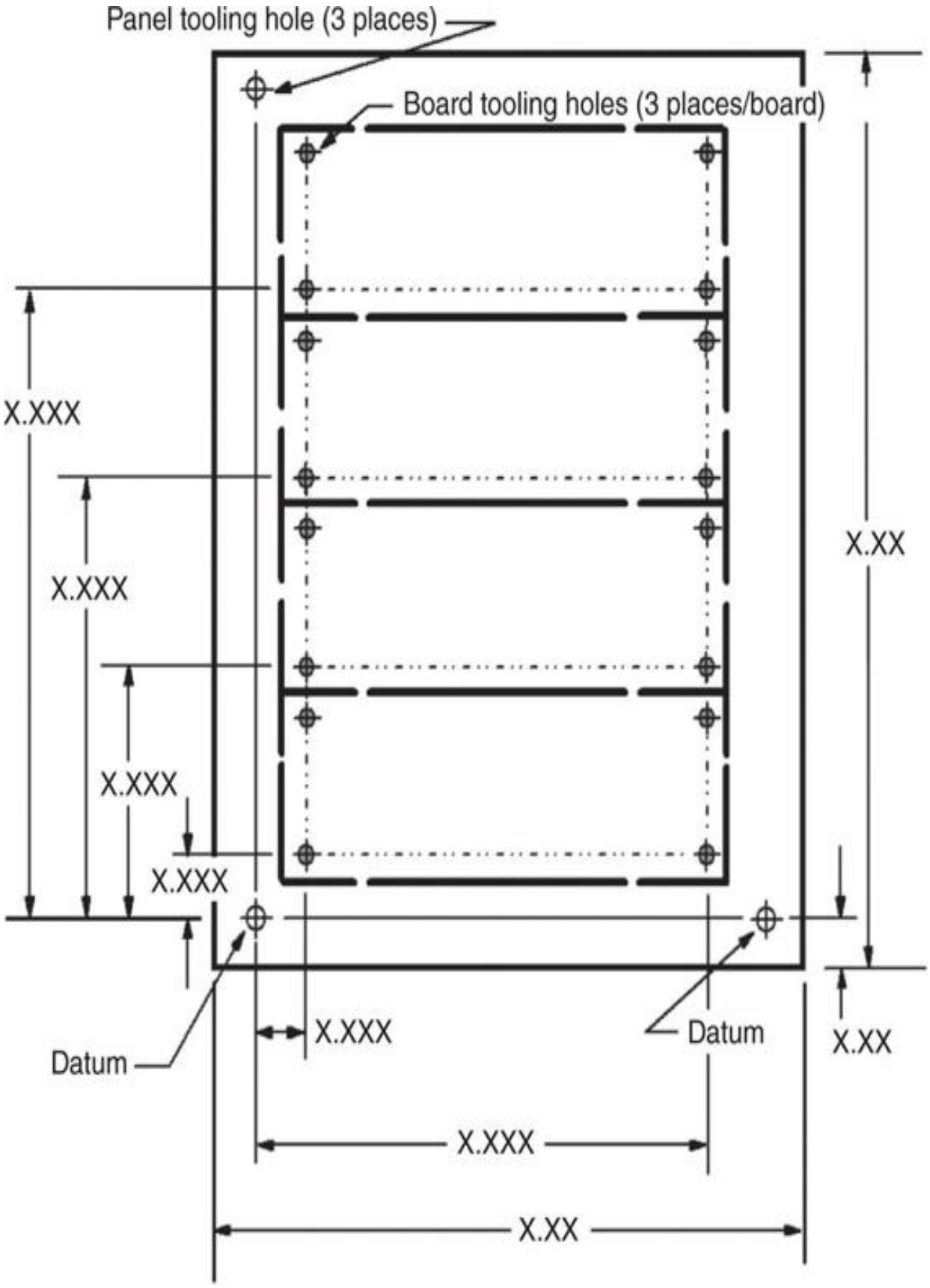

Panel tooling hole (3 places)
Board tooling holes (3 places/board)
X.XXX
X.XXX
X.XXX
X.XXX
X.XX
X.XXX
X.XX
Datum
Datum
X.XXX
X.XX

FIGURE 5.2 Datum identification examples.

Format: Common formats for drawings are Adobe PDF, HP-GL, HP-GL-II, and PostScript.

- *Drill drawing*
  Information: Although the drill data are provided via data files, this information typically contains only the location of holes and the tool number. The drill drawing identifies the location of the datum reference planes and the coordinate dimensioning system of the board (see Fig. 5.2). The tool number is referenced against the drill drawings to determine the required sizes, plating status, size tolerances, and the total count for verification. This is for plated (TH), nonplated (NPTH), blind/buried vias, and countersink holes.

  Format: Common formats for drawings are Adobe PDF, HP-GL, HP-GL-II, and PostScript.
- *Subpanel drawing*
  Information: Many assembly operations require boards to be provided in a subpanel form (many parts on one shippable unit). The drawing defines the orientation and position of each part, the subpanel dimensions, PCB information hole information, special markings, and specific manufacturing processes and tolerances.

  Format: Common formats for drawings are Adobe PDF, HP-GL, HP-GL-II, and PostScript.
- *Manufacturing notes*
  Information: Manufacturing information is usually included on the fabrication drawing or attached documents. This document details the following:
  - Board details: The type, size and shape of the printed board, bow and twist allowances, overall board thickness requirements including tolerances, PCB information hole information, special markings, and specific manufacturing processes and tolerances.

- Materials: Type class and grade of materials, including color if applicable. Plating and coating material(s), type, thickness, and tolerances. Solder mask and marking inks type, minimum thickness, and permanency.
- Conductors: Shape and arrangement of both conductors and nonconductor patterns, thickness, dimensions, and tolerances, including conductor width and spacing allowances.
- Acceptability: Location of quality conformance coupons or circuitry, control documents for acceptability, X-OUTs accepted and assembly-panel concerns.

Format: Common formats for drawings are Adobe PDF, HP-GL, HP-GL-II, and PostScript.

- *Artwork data*

  Information: These data consist of files for each circuit layer, coating (e.g., solder mask), marking (i.e., nomenclature), solder paste, hole plugging, and possible test-probing layer.

  Format: The data required are usually RS-274X, commonly called Gerber data or ODB++ (Orbitech Data Base). Gerber and ODB++ data are provided as a standard output from most PCB CAD systems. Other possible formats include GenCAM and the new IPC2581 (see Sec. 5.4.5 “Modern Data Exchange Formats” for more details).

- *Aperture list files*

  Information: The definitions of the shapes used for drawing are required for each layer provided of artwork data. Special shapes such as thermal pads should specifically define their method of construction.

  Format: This information is usually provided as a text file, although the information may also be defined in the beginning of the individual artwork files, including constructions of complex apertures.

- *Drill data*

Information: This information may consist of a single or multiple file(s), and defines the location and tool number used for each hole in the PCB. The files required should define all plated, unplated (which can be combined with plated if fully defined), buried via, and blind via layers.

Format: Common data files provided are in Excellon format.

- *Drill tool files*

  Information: This information describes the size, plating status, layer-from, and layer-to (in the case of buried and blind vias) drill-data format and filenames. This information is referenced against the drill drawing.

  Format: This information is usually provided as a text file, although the information may also be defined in the beginning of the individual drill files.

- *Special requirements information*

  Information: The drawing or a file should describe any special requirements not defined in other information. Typical of such requirements would be the details and image enlargement of “break-away” tabs on a subpanel or details of “hole-plugging” requirements. It is important for the PCB designer not to assume that requirements are understood, but to refer to specifications or clearly define the requirements.

  Format: This information is typically provided in the part drawing or may be provided as an additional text or drawing file.

- *Netlist data*

  Information: Netlist data define the connectivity of the circuitry.

  Format: This information can be provided from the CAD systems in various formats, or it can be extracted from the drill and artwork data. Contact the PCB manufacturer for compatible formats if the netlist data are to be provided

directly. The IPC has defined a neutral format, IPC356, that provides all the information necessary for netlist and electrical test fixture creation.

In addition, the IPC has defined an alternative neutral standard format for most of the previously defined data. These formats provide simpler processing at the manufacturer. They include IPC-D-350, IPC-2511 (GenCAM), and IPC-2581 (the offspring of ODB++ and GenCam). These formats can be generated by most PCB CAD systems and processed by most PCB CAM/PCB Information systems. The PCB customer should review the compatibility of these formats with the PCB manufacturer prior to sending data formatted with them.

5.3 FABRICATION INFORMATION EXCHANGE

When a printed circuit assembly (PCA) design (layout, routing, and verification) is complete, the board data must be sent to the PCB manufacturer. An output format is chosen to export the data from the computer-aided design (CAD) system. Historically, the output to bare board manufacturing was in Gerber data format and drill information was accompanied by some textual “readme” files. (These files did not contain precise definition of layer stack-up, drill span, or component outlines). These files would be sent—or rather, “thrown over the wall”—to the fabricator, sometimes without even being checked. When the board reached the assembly stage, the board assembler would receive Gerber images of the outer layers, *x, y* locations of the components and a BOM file. These methods were recognized as troublesome because errors and lack of communication necessitated

many clarification calls, faxes, and e-mails, and slowed down the process.

5.3.1 Assessing Quality of Data Exchange Formats

Designers and editors, forced to verify the data after output for correctness and manufacturability, began to work with CAD and computer-aided manufacturing (CAM) tool vendors and industry consortia to develop better formats and methods for data exchange. They sought a data exchange format that was explicit, intelligent, optimized, and bidirectional:

Explicit. There should be no need for guesswork or reverse engineering of design and no need for external files (see Fig. 5.3).

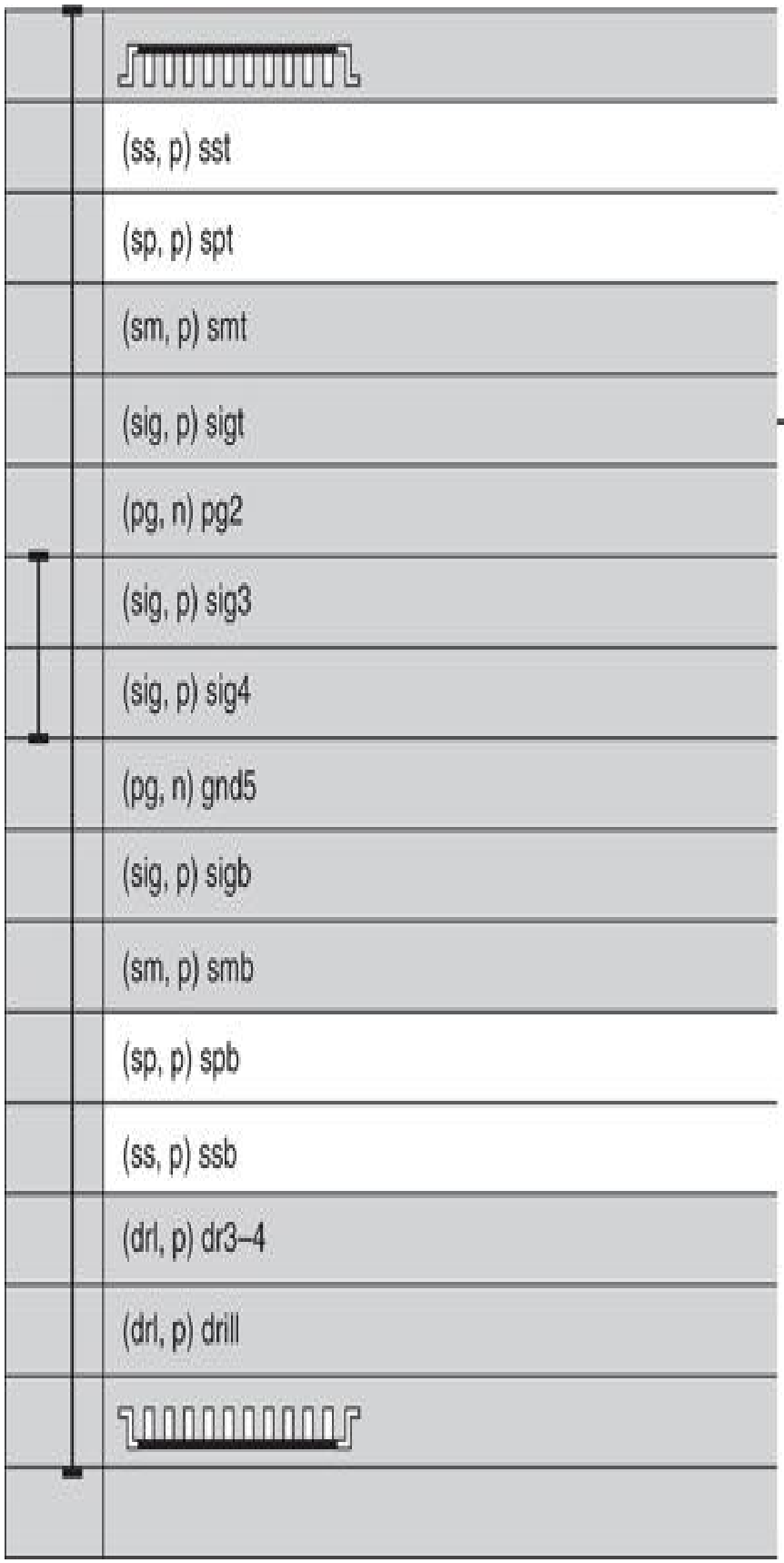

(ss, p) sst
(sp, p) spt
(sm, p) smt
(sig, p) sigt
(pg, n) pg2
(sig, p) sig3
(sig, p) sig4
(pg, n) gnd5
(sig, p) sigb
(sm, p) smb
(sp, p) spb
(ss, p) ssb
(drl, p) dr3–4
(drl, p) drill
Top Cu. Layer is a positive signal layer named "sigt"

FIGURE 5.3 A CAM system view of a typical six-layer PCA after input from an "intelligent" format that defines the layers' order and characteristics explicitly and unambiguously. If Gerber files were used it would take some time to arrange the layers' order and characteristics manually. The example includes the following:

Silk screen legend files: sst (for top) and ssb (for bottom)
Solder paste stencil aperture layers: spt and spb
Solder mask images: smt and smb
Outer copper layers: sigt and sigb
Second layer: pg2 (power layer, which is negative)
Fifth layer: gnd5 (ground layer, which is also negative)
Inner circuit layers: sig3 and sig4
Drill layers: drill (through drill layer) and dr3-4 (buried via connecting sig3 and sig4)

Intelligent. The format retains CAD information that may help the manufacturer (see Fig. 5.4).

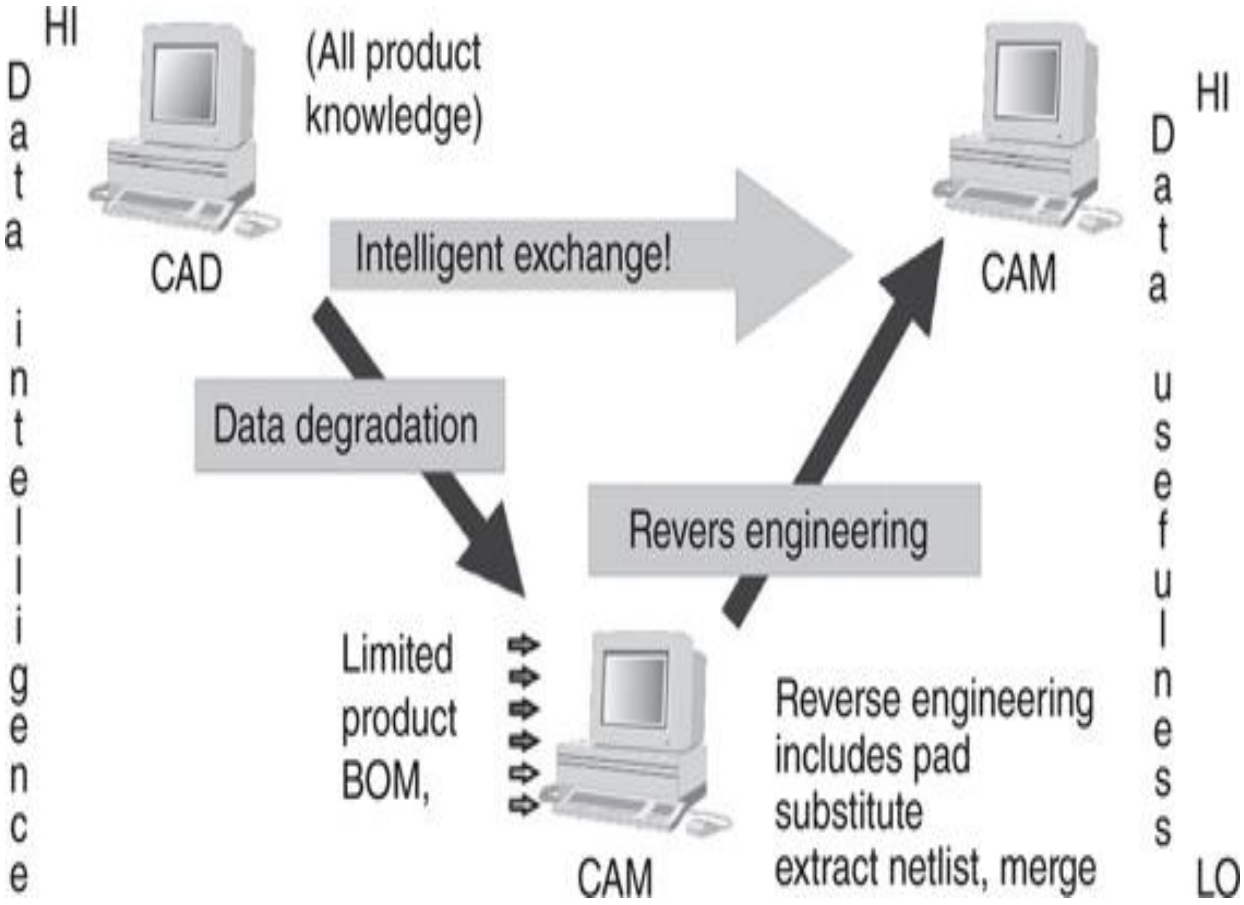


FIGURE 5.4 OEM, CEM, and Fab communication levels. In this figure the *y* axis denotes the level of intelligence and the *x* axis denotes the data exchange process progression over time. When the formats used carry less design intelligence, it is lost (data degradation). Non-value-added reverse engineering (such as manually rebuilding the board stack-up) is required to rebuild intelligence that is required for manufacturing. If an intelligent exchange format is used, no design data are lost and no reverse engineering is required, resulting in a faster, more accurate, and more efficient process.

Optimized. A surface should be represented by a clear outline and not drawn with overlapping vectors (see Fig. 5.5).

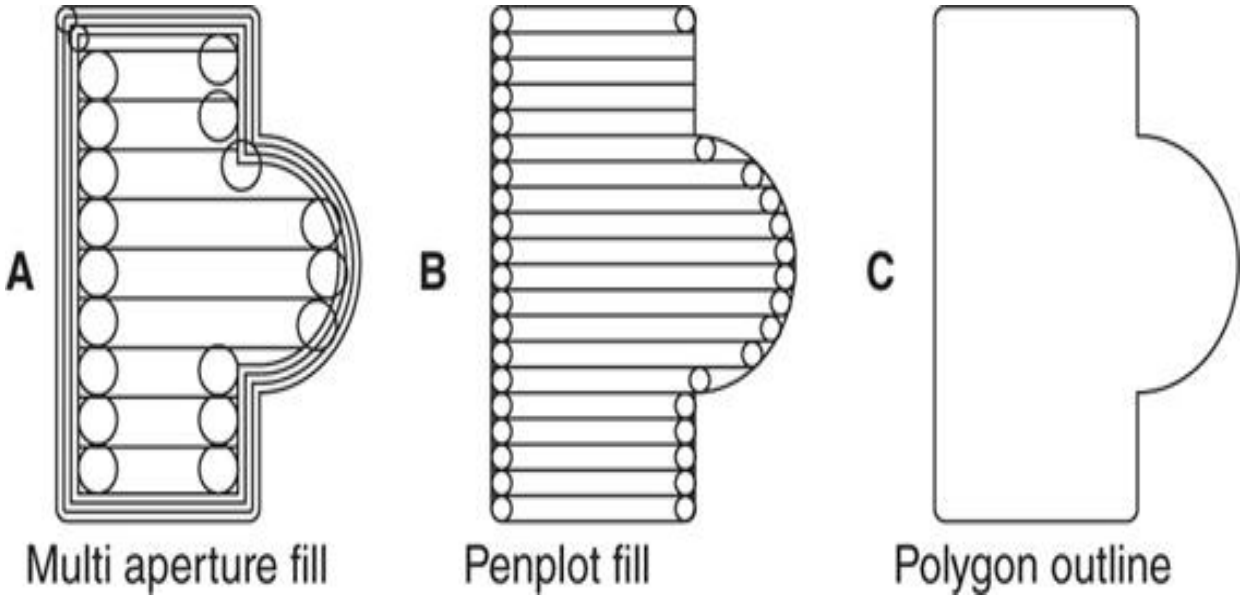


FIGURE 5.5 Optimizing surfaces: (*a*) a polygon filled by different vector widths; (*b*) the same polygon as drawn by a pen plotter; (*c*) the polygon as defined by its external outline. Option *c* is clearly much more efficient and economical. The outline in (*c*) is the actual outline of the polygon, whereas (*a*) and (*b*) represent approximations.

Bidirectional. The format should be inherently capable of passing data back and forth, not just passing them one way. This can be achieved through free viewers, annotations tools, and so on.

Other important issues to consider in the context of data exchange are the following:

Accountability. Who is responsible if something is misunderstood? If the exchange always succeeds, it is easier to differentiate between design and manufacturing errors.

Data ownership. Who can authorize changes? If reverse engineering is performed, subtle design changes may be introduced without OEM authorization.

Trust. Is the supplier an ally to whom all available data are provided, or are some design details withheld to protect intellectual property rights?

The next section details all the data elements that designers and manufacturers need to pass among each other.

5.3.2 Elements of Data Exchange: Intelligent Design Data

The goal of a supply chain is short time to market, high quality, and lowest cost, and achieving this goal requires high clarity, efficient communication, and not just a bare-bones data hand-over.

Although a PCB can be manufactured from supplied artworks and drill tapes alone, it is much more efficient to send accurate and verifiable electronic data. The data can include information elements beyond the graphic image and component location information that form the minimum "pure" design data required for improved manufacturing. Among these elements are

- Mechanical specifications
- Component geometry
- Component tolerances and vendor information
- Standards that the product has to meet

Some of the information belongs in an SOW and need not be repeated in the case of an established partnership. Included may be marking instructions, packaging instructions, and information needed to ensure conformance to standards.

This section lists the information required for data exchange for fabrication.

5.3.2.1 Minimum Requirements. These are the minimum required elements of data needed for fabrication:

- Layer graphics (see Fig. 5.6)

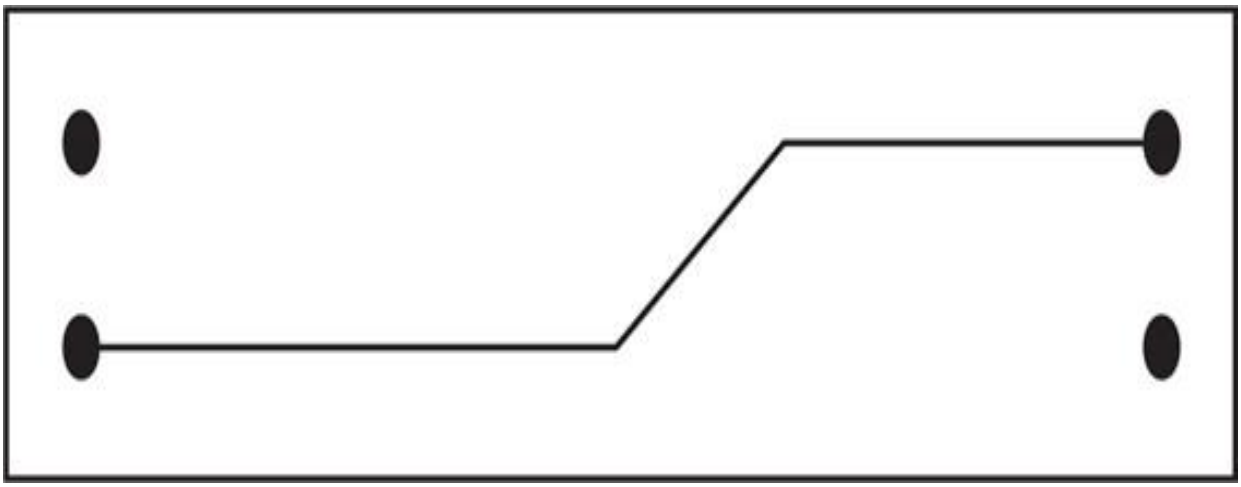


FIGURE 5.6 A layer graphic represents—board outline and rout informing the features of a circuit (or a document) layer represented by computer-readable geometric entities involving *x* and *y* coordinates and geometric objects—lines, arcs, circles, and so on.

- Drill data: locations, spans (for blind and buried vias), tolerances, and plating thickness
- Board outline and rout information
- Stack-up requirements (layer order)

5.3.2.1.1 Important Additional Information. These elements are important but not absolutely required for fabrication:

- Netlist information is required to verify that the graphic and drill data truly represent the design. It is highly advisable always to include netlist data so that the graphics can be verified.
- Assembly panelization definition is required to deliver multiple PCBs in a ready-to-assemble array form (four or more cell phone boards can be assembled together due their small dimensions).

5.3.2.1.2 Extra Information. This extra information is not covered by computerized formats, but is useful in fabrication:

- Electrical (impedance) and material requirements (solder mask, legend, etc.). (Impedance requirements refer not only to line width and tight tolerances thereof but also the actual impedance value, in ohms, and the frequency and impedance model to use.) Fabrication drawing (extra instructions, dimensions)
- Type of finish and quality requirements [hot air solder leveling (HASL) versus organic solderability preservative (OSP), solder mask]
- Packaging and delivery instructions
- Testing coupon requirements
- These additional information elements can be provided as well:
- Design for manufacturing (DFM) analysis results and criteria (e.g., spacing criteria and violations thereof)
- Component placement information, which can help the manufacturer create solder mask clearances that provide a good fit for soldering

5.3.3 Elements of Data Exchange for Assembly

This section lists the data elements to consider for assembly processes.

***5.3.3.1 Common to Fabrication and Assembly*.** These elements are common to fabrication and assembly:

- Outer layer graphics (for circuit, solder mask, and legend images)

- Drill information (especially through drills and mechanical drills)
- Board dimensions and outline

5.3.3.2 Required for Assembly. These elements are required specifically for assembly:

- Component placement information, including rotations.
- BOM and approved vendor list (AVL) information (AVL is not required if parts are supplied by consignment).
- Mechanical assemblies and their locations (screws, shields and heat sinks, etc.).
- Board electrical schematics for testing (see Fig. 5.7). This information is usually transferred either as an element of a CAD database or as a human- and machine-readable drawing format [usually as a Hewlett Packard Pen Plotter (HPGL) or Data eXchange Format (DXF) file]. [Machine-readable in this context means identification of textual labels for nets (signals) and pin and component names. The computer programs cannot understand the connectivity symbolism of the line drawings within schematic drawings.]

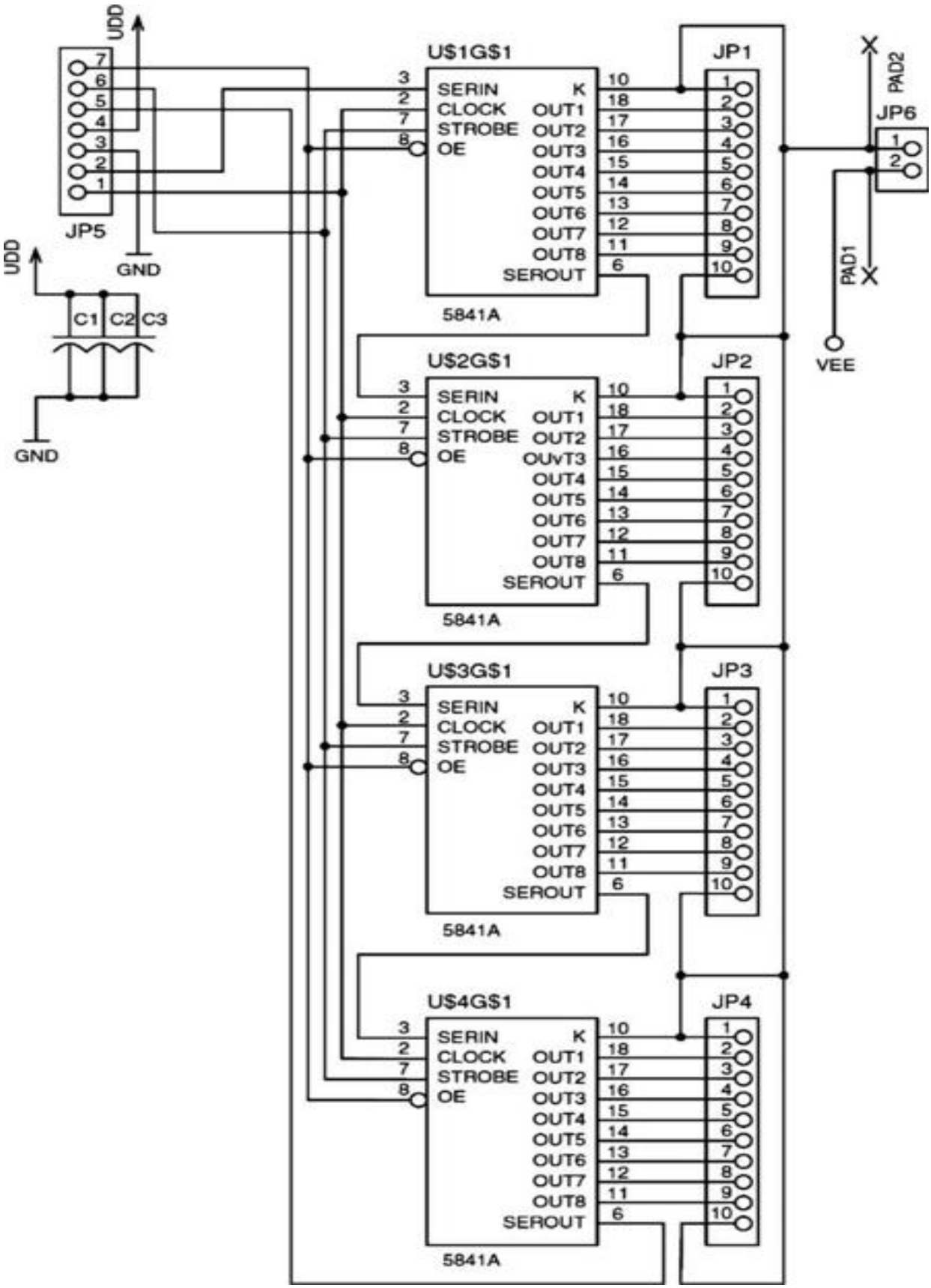

UDD
JP5
GND
UDD
C1
C2
C3
GND
U$1G$1
SERIN
CLOCK
STROBE
OE
K
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
SEROUT
5841A
JP1
U$2G$1
OUvT3
JP2
U$3G$1
JP3
U$4G$1
JP4
PAD2
JP6
PAD1
VEE

FIGURE 5.7 Product schematic drawing (for components, signals, and interconnections) as sent by the product electrical designer to the PCB editor. There are four 18-pin logical components having SERIN (serial in) and eight output (out1-out8) pins each connected to output connectors (JP1-JP4) and to an input connector JP5 and a ground connection with three capacitors.

5.3.3.3 Extra Information. This extra information, not currently covered by electronic formats, must be read and understood:

- Test requirements
- Material instructions
- Delivery and packaging instructions

5.4 DATA EXCHANGE FORMATS

This section describes the most widely used data exchange formats in the electronics industry according to a common list of characteristics. Advantages and disadvantages of each format are discussed.

5.4.1 Format Types and Their Characteristics

There are several format families differentiated by their origins, properties, and usage. They fall into four categories:

1. Historical file collections
2. Full-design databases
3. Component information (BOM and AVL)
4. Formats that support full design to manufacturing

5.4.1.1 Historical File Collections. The historical file collection that is used to transfer design data is composed of

three file types:

5.4.1.1.1 Graphic Image Formats. Gerber 274D and 274X[2] belong to this group (see Sec. 5.3.2.1). (There are other formats in this group, most of which are used internally within CAM systems and as archive formats within bare-board fabrication facilities. Pentax format, DaiNippon Screen, and MDA Autoplot belong to this group.) Most of these formats originated as a photo-plotter machine language; they describe single-graphic (drill, drawing), two-dimensional layers. They are usually accompanied by drill files indicating drill locations and diameters. The main drawbacks to graphic image formats are that they represent single layers rather than whole PCBs and that they cannot be verified unless accompanied by a netlist file.

5.4.1.1.2 Netlist. A netlist presents a list of net numbers, and for each net a list of points by their x and y coordinates, and the surface upon which they can be found (see Fig. 5.8). This is the basic information representing PCB connectivity against which PCB graphics can be verified and from which a test program for an electrical test machine can be constructed. One type of netlist identifies the locations of the nets that the PCB is designed to implement. Another type of netlist is a CAD software design package schematic netlist that identifies connectivity between components [by component and pin number as an input/output (I/O) pin identifier], but does not identify their physical location.

```
327LDIN_47          IC52  -U5        A01X+110078Y+030997X0200Y    R180
317LDIN_47          VIA   -    MD0100PA00X+110274Y+031194X0230Y    R180
327LDIN_47          IC10  -J2        A01X+134371Y+039414X0200Y
317LDIN_47          VIA   -    MD0100PA00X+134174Y+039217X0230Y
```

(a)

```
Signal LDIN_47
IC52 U5
IC10 J2
```

(b)

FIGURE 5.8 Example of a netlist: (*a*) this part represents a physical netlist with *x* and *y* coordinates [the first line translates as “Pin U5 of component IC52 is connected to net LDIN_47 and is at location (11.0078, 3.0997)”]; (*b*) this part represents the same netlist but at schematic stage with only component and pin names; the electric signal identified as LDIN_47 connects IC52 pin V5 to IC10 pin J2 through two vias.

5.4.1.1.3 Component Information. In addition to being part of the historical file collection, BOM and AVL files are also part of an independent file class that is required even when the more advanced formats are used (see Sec. 5.3.5).

***5.4.1.2 Full-Design Database: CAD Formats*.** Full-design databases, which are formatted using either the CAD system database format or American Standard Code for Information Interchange (ASCII)[b] extracts thereof, represent information for the component and their connectivity through the board as hierarchical arrangements of nets and subnets broken into traces, vias, and planes. They are transferred for board assembly and test but not for board fabrication. Because OEMs consider these formats to present

a proprietary information security risk, they often prefer to convey inferior quality information using other formats in order to preserve privacy.

5.4.1.3 Explicit Design for Manufacturing Formats.

Formats for full design for manufacturing were explic itly built for design-to-manufacturing data exchange and contain nearly all of the required computer-readable data elements in a well-designed, explicit, intelligent layout. Some of these formats originated as DFM/CAM vendor formats whereas others were designed by an industry association committee.

5.4.1.4 Component Information: BOM and AVL.

A PCA may be designed for more than one product variant and to support future functionality. Therefore, for almost all designs, some of the reference designators (or actual bare board footprints on which components can be placed) will not be populated for all assembled board orders. BOM files are used to tell the assembler which reference designators should actually be placed on a given board for a specific order.

The separation between electrical functionality of components and their actual procurement leads to the need for an AVL file. CAD databases usually contain part numbers that represent functionality and are internal to the design organization rather than part numbers (including the vendor and catalog number) that customers can order. Component engineers are charged with finding true part numbers to implement the internal ones, and this information is usually organized in spreadsheets or text files called AVLs or approved component lists (ACLs).

5.4.2 Historical File Formats Descriptions

Each format description that follows includes its domain (the elements that are covered), its history and expected future path, distinctive characteristics, and a short example. Format description references can be found at the end of the chapter.

5.4.2.1 Gerber (274D and 274X), Drill and "Readme." Gerber formats are the "lowest common denominator" for passing bare-board fabrication information. They are composed of one file per graphic layer, one file for each drill layer, text files that list the PCB stack-up, and optional drawing files that list critical dimensions and requirements. Inclusion of a netlist file with each Gerber transfer is imperative to ensure correct board fabrication.

A common problem with both Gerber 274D and drill formats (usually Excellon I and II) is the lack of definition of both units and scale factor of numbers (Excellon is a precision drill machines manufacturer). Each coordinate is given as a collection of digits, and the translator, or user, must define the units (in in. or mm) and the location of the decimal points in the format. Another problem stems from the use of arbitrary numbers ("Dcodes" for aperture numbers on an aperture wheel) to describe the width of lines and size of pads. Accurate translation of these files depends on the correct definition of an aperture wheel, which is described separately. Figure 5.9 shows a photo-plotter schematic that explains the source of the terminology.

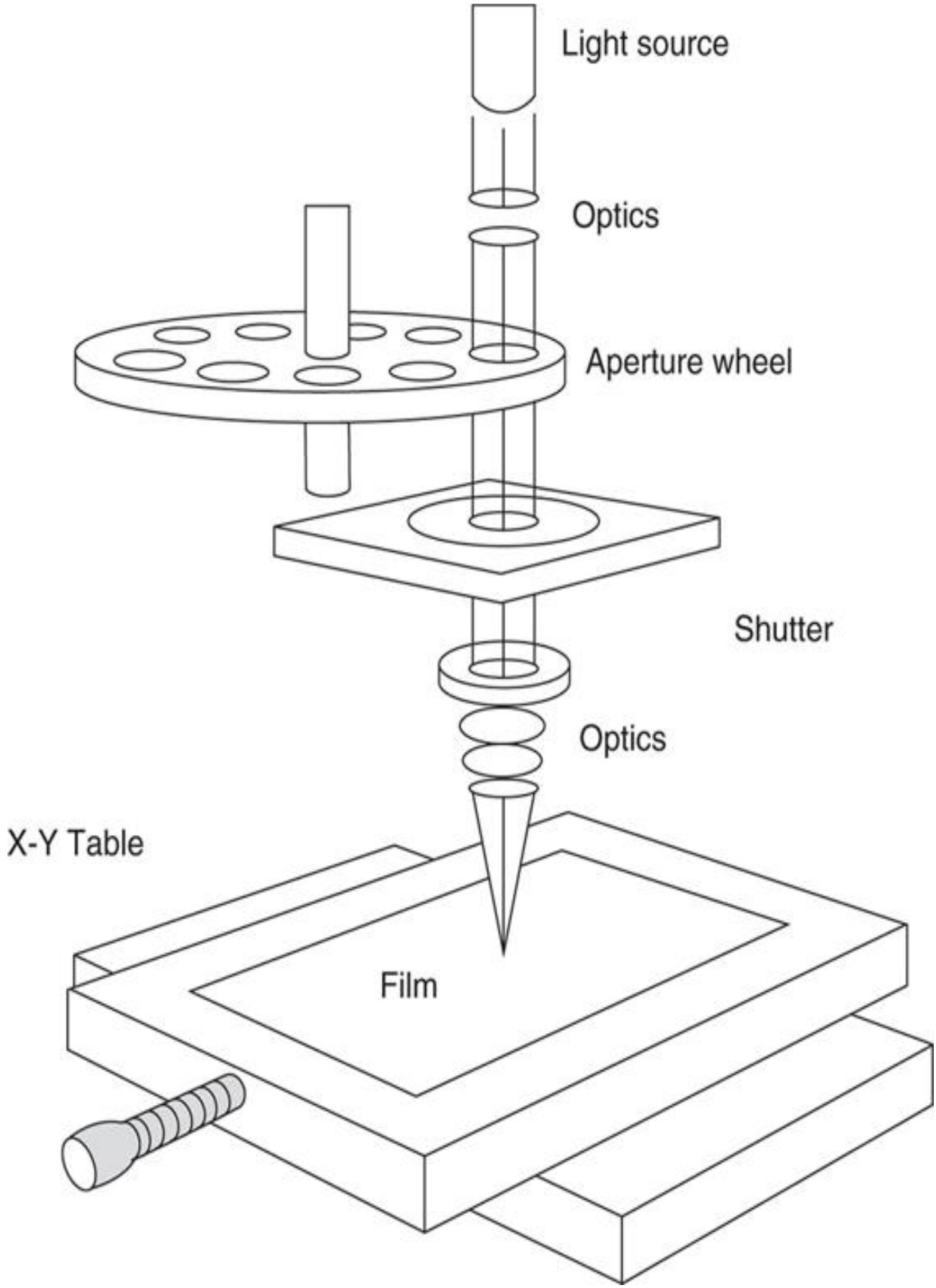

Light source
Optics
Aperture wheel
Shutter
Optics
X-Y Table
Film

FIGURE 5.9 A photo plotter uses a stationary light source to deliver light through a rotating variable size aperture wheel (which determines the size of the light spot on the table) onto a table that can move in the *x* and *y* directions. A shutter shuts or allows light passage as required. Precision optics control the focus of the light spot.

The commands that drive this mechanism are *x* and *y* coordinate movement commands to position the table, those that turn the shutter on and off, and Dcode commands that rotate the aperture wheel to the required position.

Gerber 274X was designed in the early 1970s (by a team of two engineers—one from Gerber Scientific and another from what used to be the biggest PCB factory in the United States, the AT&T plant in Richmond, Virginia) to overcome some Gerber 274D problems. Gerber 274X permeated slowly at first, but its adoption accelerated and Gerber 274D is now used less frequently.

Both 274D and 274X are used to transfer graphic images of circuit and mask layers and images of documentation layers used for instructions. Other graphic drawing formats are occasionally used to transfer board and drawing data. The most common formats are HPGL (the format of HP pen plotters) and DXF (the AutoCAD exchange format).

Several drill formats originating from drill machine makers other than Excellon (Sieb and Mayer, Posalux, etc.) are sometimes used to transfer drill data or to archive old drill data. They suffer from the same problems of Dcode (explained in Fig. 5.9) and unit definition.

5.4.2.1.1 Gerber 274D. Gerber RS-274-D has been the most common format for describing PCB plot data. This format was originally intended to drive vector photo plotters (see Fig. 5.8), produced by Gerber Systems Corporation (see Fig. 5.10 for an annotated snapshot section of a Gerber file).

Example	
G90*	G90 indicates absolute coordinates.This means that that each set of coordinates is referenced to the table's origin (0,0).The converse to absolute is incremental;each coordinate is measured relative the previous coordinate value and is set by issuing the G91 command.
G70*	G70 indicates inch units.
G54D10*	G54,tool select (line 3),is the most commonly encountered Gcode and instructs the plotter to rotate the aperture wheel to the position described by Dxx immediately following the G54 command. If this code is omitted,the the photo plotter then identifies the next Dxx command as telling it to select a tool.
G01X0Y0D02*	Dcodes are instructions to the photo plotter that, naturally, include the letter *D*. The first three Dcodes control the movement of the x,y table.D02 (D2) tells the plotter to move to the x,y location specified with the shutter closed.
X450Y330D01*	D01 (D1):This command tells the plotter to move with the shutter open to the x,y location specified.
.X455Y300D03*	D03 (D3):This command tells the plotter to move with the shutter closed to the x,y location specified, then open and close the shutter—known as flashing the exposure.
G54D11*	
Y250D03*	
Y200D03*	
Y150D03*	
X0Y0D02*	
M02*	The *M* in Mcommands stands for miscellaneous; in this case, M02 means stop or end of file.

FIGURE 5.10 An annotated section of a Gerber file.

The basic commands of this format include the following:

- Selecting the aperture
- Opening and closing the aperture shutter
- Moving the head to a given *x, y* coordinate

Typically, commands are separated by the asterisk character (*).[3]

5.4.2.1.2 Gerber 274X. Gerber RS-274-X is a common format in use today for describing PCB plot data. The format can be divided into two parts:

1. The Gerber part
2. The extended part, which includes commands for the following:
   - Standard aperture definition
   - Aperture Macro definition (special symbols)
   - Layer polarity selection

Typically, extended commands begin with % and end with *%.

Unlike Gerber 274D format, Gerber 274X includes definition of coordinates using the FS command (see Fig. 5.11). Reading software uses this information when reading Gerber parts.

Example

%FSLAX23Y23*%	This command indicates (L)eading zero suppression,(A)bsolute, 2.3, or xx.xxx and yy.yyy decimal point location
%MOIN*%	This command specifies inches
%SFA1.000B1.000*%	
%ADD11C,0.00500*%	These are aperture definition commands defining various diameter circles (5, 8, 10, 20, and 25 mil, respectively)
%ADD13C,0.00800*%	
%ADD14C,0.01000*%	
%ADD70C,0.02000*%	
%ADD71C,0.02500*%	
G54D11*	Here the Gerber part begins.
%LPD*%	This command indicates that digitized data is dark. However, when the entire film is reversed, the digitized data will be clear.

```
G11*G70*G01*D02*G54D10*X-0020000Y-0250000D02*X-0020000Y-0265200D01*
X0010000Y-0255000D02*X0010000Y-0250000D01*X0025200Y-0344800D02*
X0025200Y-0285000D01*X0022800Y-0265200D02*X0022800Y-0270000D01*
```

This is straight Gerber code with multiple commands on a line.

FIGURE 5.11 An annotated Gerber 274X section.

The most serious limitation of Gerber 274X is polygon representation. No solution was provided for describing internal cutouts or clearances. Each implementation of Gerber 274X-based CAD output deals with these in its own way. The most problematic way is to use self-intersecting polygons (SIPs) where the “pen” does not leave the board

while drawing the internal cutouts, but “swerves” to the inside of the external outline to draw the internal cutout and then returns (see Fig. 5.11).

An SIP is a polygon with two nonconsecutive edges (segments or curves) touching each other. SIPs are illegal in CAM systems that define legal polygons as those whose edges intersect only at endpoints of consecutive edges.

Translation of 274X data into a CAM system might fail with a “Self Intersecting Polygon” error because some CAD systems create surfaces using self-intersecting polygons.

SIPs are not mathematically robust, and the following SIP operations are problematic:

- Resizing (enlarge, shrink, scale—especially with differing *x* and *y* values)
- Accurate copper calculations (these require unambiguous definition of the copper location)

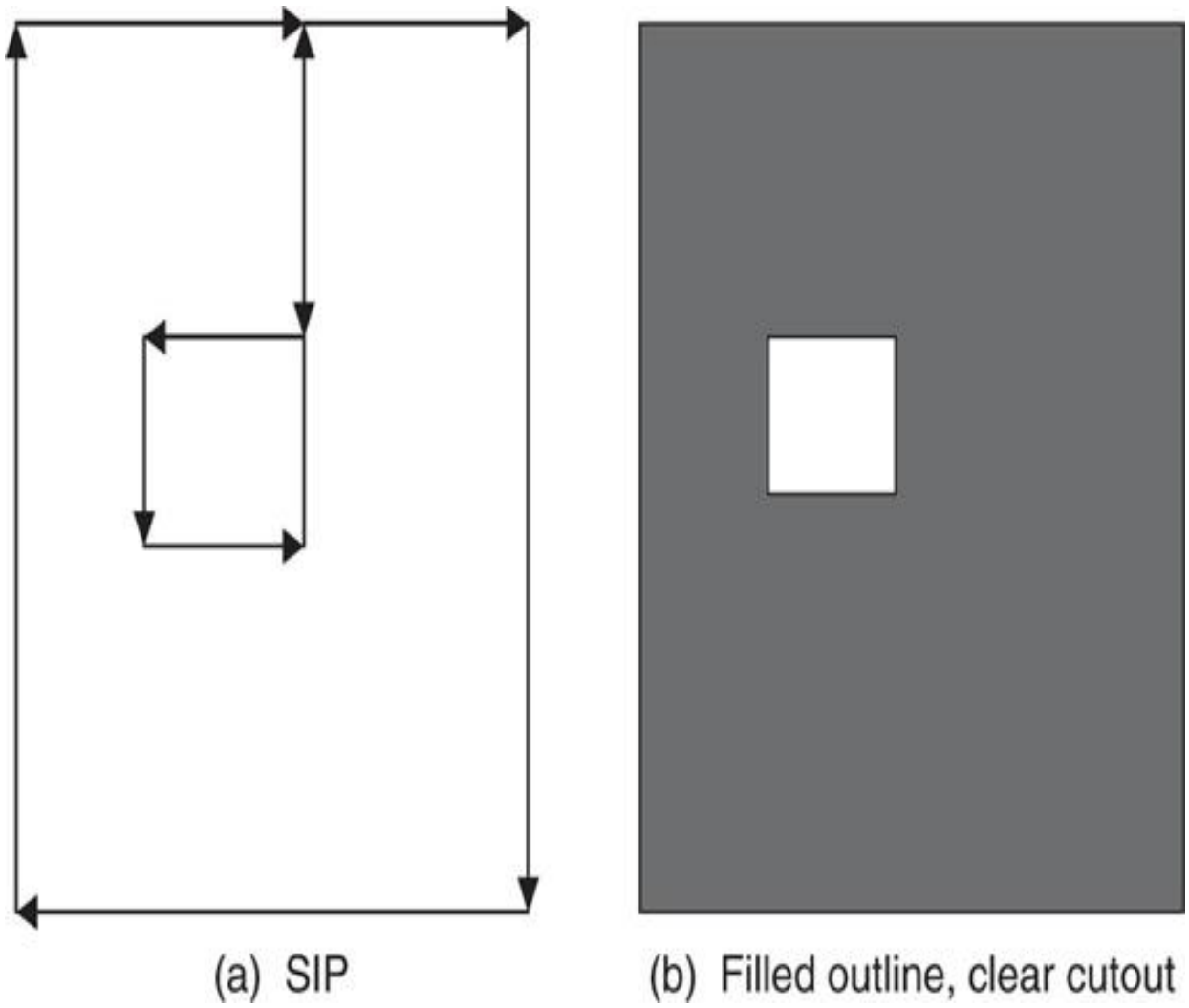


FIGURE 5.12 An SIP: (*a*) as drawn by self-intersection, with a single path and the pen not removed from the paper; (*b*) with a filled rectangle as an outline and a clear rectangle as the cutout.

In most CAM systems, a surface is a mathematical entity that describes planes. It can contain islands (positive polygons) and holes (negative polygons). If the layer is positive, islands represent copper, whereas holes represent non-copper (see Fig. 5.13). Copper planes usually implement power or ground connections, where the clearances provide spacing for data signal vias that pass through the plane but must be electrically disconnected from it.

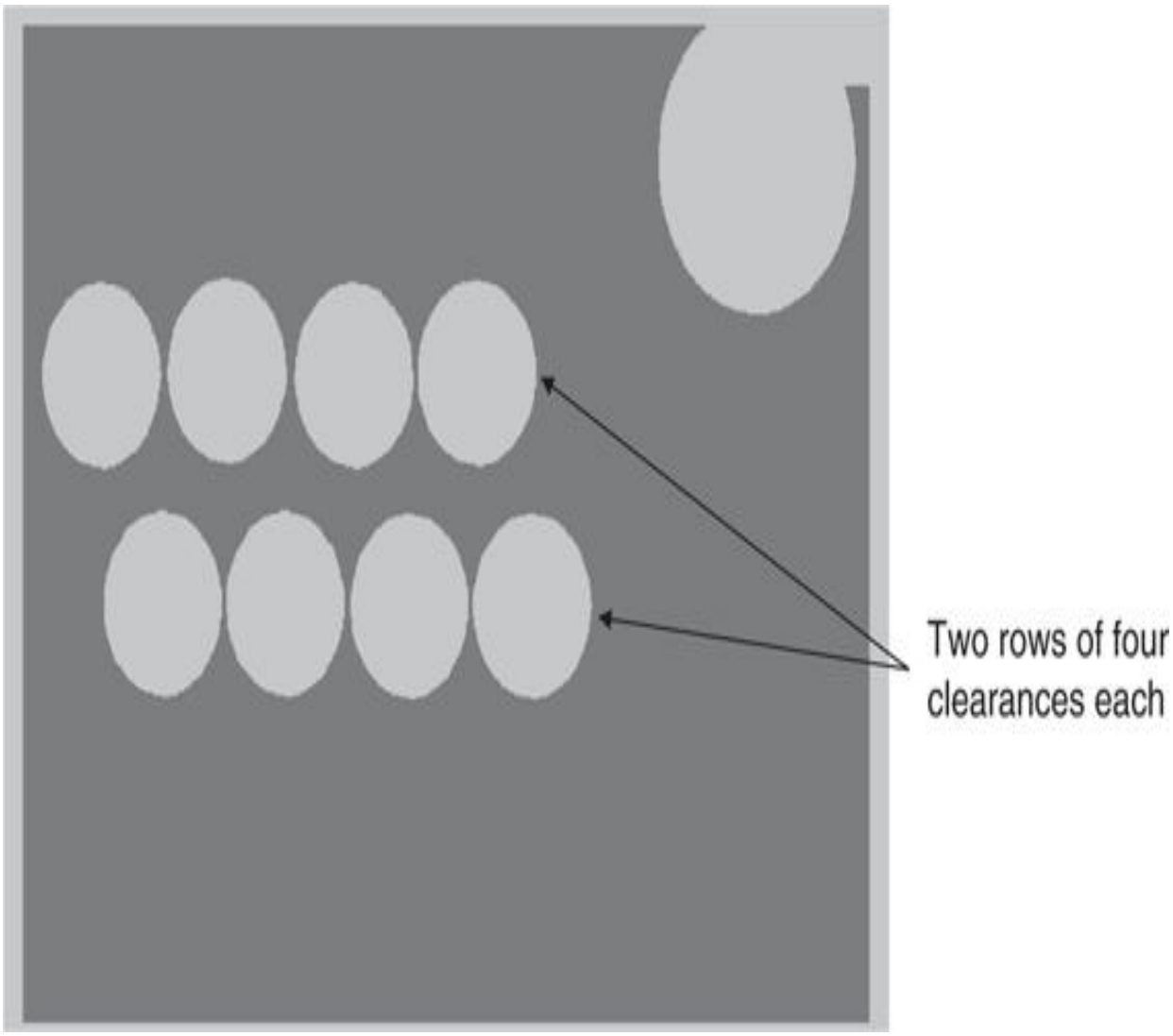


FIGURE 5.13 This surface is composed of one rectangular island, with a circular cutout in the top-right corner representing copper and eight round holes representing clearances.

There are two non-ambiguous ways of drawing planes with cutouts in 274X. The first is to use positive polarity for the islands and negative polarity for the holes. The second is to decompose the plane into positive surfaces that, when combined, yield the outline with the holes.

5.4.2.2 Netlist Formats. A netlist is a set of connection points joined together to form networks. Each point represents a contact point on the surface of a bare board. A

connection point can be either a drilled hole or a surface mount pad. All points belonging to one network should be connected to each other through PCB layer circuitry and/or power and ground planes.

5.4.2.2.1 Gerber Data. Gerber data format is the oldest artwork format. It was developed with the first NC photo plotters in the early 1970s. It is the "least complete" of data formats in that it consists of an aperture wheel definition, an x-y starting coordinate, an "open shutter" command, an x-y ending coordinate, and a "close shutter" command. The aperture wheel must also be defined. Figure 5.14 shows a typical Gerber format program.

```
*                (Always a good idea to start a plot with an asterisk)
04 *             (Comment; Date: Sun Feb 26 16:48:19 2006)
G04 *            (Comment; Layer 1: Layer_1.gbr )
G54D12*          (G54, tool select Aperture number D12)
D2*              (D02: move to the x-y location specified with the shutter closed.)
X40000Y30000D03* (Go to X-4.0000", Y-3.0000, D03 (D3): move to the x-y location specified
                 with the shutter closed; then open and close the shutter-known as flashing
                 the exposure.)
G54D10*          (Select Aperture number D10)
X10000Y10000D02* (Go to X-1.0000", Y-1.0000, not drawing a line)
G01X50000D01*    (Go to X-5.0000", Y-1.0000, drawing the base of the triangle)
Y60000*          (Go to X-5.0000", Y-5.0000, still drawing)
X10000Y10000*    (Go to X-1.0000", Y-1.0000, drawing the hypotenuse)
M02*             (End of plot)
```

FIGURE 5.14 Example of a Gerber format program.

The Gerber 274-X is the preferred version today, as the apertures are embedded in the format. Figure 5.15 shows the RS-274X 2.5 leading absolute format.

```
GERBER RS-274 X          FIRE 9xxx
                         BARCO BDP
G04 Date:  Sun Feb       G04 Date:  Sun Feb 26      ;
26 16:57:09 2006 *       16:57:39 2006 *            ;       Sun Feb 26 16:57:58 2006
G04 Layer_1:             G04 Layer 1:               ;        Layer 1: Layer_1.gbr
Layer_1.gbr *            Layer_1.gbr *              ;
%FSLAX25Y25*%            G04%FILE="Layer_1.gbr";
%MOIN*%                  %*                         U=MIL
%SFA1.000B1.000*%        G04%PAR.%*                 X90.0,510.0 Y90.0,610.0
%MIA0B0*%                G04%MODE=A;%*              A10=C,20.00
%IPPOS*%                 G04%UNIT=I;%*              A12=C,100.00
%ADD10C,0.02000*%        G04%ZERO=L;%*              A12
                         G04%FORM=2.5;%*            F400.00,300.00
%ADD12C,0.10000*%        G04%IMTP=POSITIVE;%*       A10
%LNLayer_1'.gbr*%        G04%ADRS=Q;%*            M100.00,100.00D500.00,D,600.00D100.00,100.00
%SRX1Y1I0J0*%            G04%MIRR=N;%*
G54D10*                  G04%CROS=X;%*
%LPD*%                   G04%EMUL=UP;%*
G54D12*                  G04%XSCL=1.000000;%*
X40000Y30000D03*         G04%YSCL=1.000000;%*
G54D10*                  G04%POEX=11,13;%*
X10000Y10000D02*         G04%POIN=14,15;%*
G01X50000D01*            G04%MRGE=PAINT;%*
Y60000*                  G04%NEXT=="-";%*
X10000Y10000*            G04%NFLG=P;%*
M02*                     G04%EOP.%*
                         G04%APR,100000.%*
                         G04%A10:CIR,2000,X0,Y0.
                         %*
                         G04%A12:CIR,10000,X0,Y0
                         .%*
                         G04%EOA.%*
                         G54D10*
                         G54D12*
                         X40000Y30000D03*
                         G54D10*
                         X10000Y10000D02*
                         G01X50000D01*
                         Y60000*
                         X10000Y10000*
                         M02*
IPC D-350
C    Date:  Sun  Feb  26  16:58:20  2006
C    Database:   (Untitled)
C
P    UNITS   CUST
P    IMAGE   NCON POS
P    IMAGE   NCON POS
322D1000L01S          NULL                                  GO    X 00004000Y 00003000
112D0200L01S          NULL                                  GO    X 00001000Y 00001000X
00005000Y     00001000
000                                                        X
00005000Y   00006000X   00001000Y   00001000
999
```

FIGURE 5.15 Example showing RS-274D 2.5, the leading absolute format.

5.4.2.2.2 GenCAM. Developed by IPC to improve data transfer for manufacturing in the 1980s, GenCAM is an ASCII-based, English-readable, and universal vendor-independent data exchange format. IPC-D-350 was the first such format in the 1970s, followed by IPC2511/GenCAM in the 1990s, and in the new millennium IPC-2581 evolved.

5.4.2.2.3 IPC-D-356.[c] IPC-D-356 is an ANSI-accepted standard that has become the most widely used standard for transferring netlist information. The IPC-D-356 format is used to transfer netlist information within the PCB design and fabrication community. This information can be used to verify the integrity of the design by netlist extraction from the Gerber graphics and comparison with the IPC-D-356 CAD reference. The information is also used within both the bare board and the assembled board test domains.

Most data in the IPC-D-356 file (see Fig. 5.16) consist of electrical test records of two types:

```
C This is a comment field
P UNITS CUST
317A01AUXNEG A10 -1 D0380PA00X+068250Y+002250X0620Y0620
317UN2CAP62PCA0 A10 -2 D0380PA00X+068250Y+001250X0620Y0000
327UN2CAP62PCA0 A9 -1 A01X+066330Y+001500X0800Y0250
327A01AUXPOS A9 -2 A01X+066330Y+002000X0800Y0250
327N/C A9 -3 A01X+066330Y+002500X0800Y0250
327N/C A9 -4 A01X+066330Y+003000X0800Y0250
327N/C A9 -5 A01X+064170Y+003000X0800Y0250
327N/C A9 -6 A01X+064170Y+002500X0800Y0250
```

FIGURE 5.16 A section of an IPC-D-356 file. It contains two drill records (“317”) and six surface mount records (“327”). The four bottom solder mask (SMT) points

should not be connected, hence their “net name” fields contain “N/C,” indicating “Not connected.”

1. Drill records (starting with “317”)
2. Surface mount pad records (starting with “327”)

There are also other general parameter records.

Each IPC-D-356 record consists of one line and (for historic reasons) is of a fixed length with a maximum of 80 characters.

The information extracted from translation of IPC-D-356 files to an internal netlist might include solder mask coverage and midpoint flags, along with the dimensions and location of connection points and their groupings into networks. Information in component and pin identification fields is not necessarily extracted for comparison purposes.

There are two amendments to IPC-D-356: IPC-D-356A and IPC-D-356B. Most of the extra information included in these formats is important for bare-board electrical testing and, unless buried passives are used, the information is generally not needed for CAD-to-CAM data consistency verification. If buried passives are used, it is better to transfer IPC-D-356A after verifying readability by the supplier.

5.4.3 Mentor Graphics Neutral File[4]

Several nonstandard netlist formats can be output by various CAD software suites. All such formats contain connection point records and their grouping into nets. American designers and fabricators occasionally used a stripped-down version of the Mentor CAD format Neutral File to transfer netlist information, and thus it is described here.

The Mentor Graphics Board Station Fablink application produced the Mentor Graphics Neutral File format. It has

several sections, each describing one aspect of a board (components, netlist, holes, etc.).

A full neutral file contains these information sections:

- BOARD: board attributes
- NET: net points
- GEOM: packages and pins
- COMP: components and “toeprints”—another name for a pad pattern outline
- HOLE: drilled holes
- PAD: approximate shape of pads

The BOARD and NET sections contain sufficient information to derive a netlist. If the file includes all sections, it is possible to derive components and drills but not full routing (trace) information.

The Fablink user can control which sections are included in the file (see Fig. 5.17).

```
# file: /tmp_mnt/disk/ed8/mj/demo/1/pcb/mfg/neutral_file
# date: Monday June 2, 2005; 18:46:15
#
##############################################
###Panel Added Part Information
##############################################
##############################################
###Board Information
##############################################
BOARD SYSTEST_BOARD OFFSET x:0.0 y:0.0 ORIENTATION 0
B_UNITS Inches
##############################################
###Attribute Information
##############################################
B_ATTR 'MILLING_ORIGIN' 'MILLING 0 0.0 0' -0.4 -4.0
B_ATTR 'DRILL_ORIGIN' '' 0.0 0.0
B_ATTR 'BOARD_DEFINITION_IDENTIFIER' '' 0 0
....
###Nets Information
##############################################
NET /+8VTO10V
N_PIN J1-1 0.5 -3.2 term_1 0
N_PIN CR1-1 -0.2 -2.7 term_1 0
N_PIN W2-3 0.3 -2.5 term_1 0
NET /DATA_BIT_1
N_PIN J2-1 0.8 -1.7 term_1 0
N_PIN U2-3 1.1 -3.1 term_1 0
....
##############################################
###Geometry Information
##############################################
GEOM DIP20
G_PIN 1 0.0 0.0 term_1 Thru 0.033
G_PIN 2 0.0 -0.1 term_1 Thru 0.033
G_PIN 3 0.0 -0.2 term_1 Thru 0.033
G_PIN 4 0.0 -0.3 term_1 Thru 0.033
....
##############################################
###Component Information
```

Comments that denote file section boundaries

FIGURE 5.17 An excerpt from a Mentor Neutral File. Section names and records roles are pretty obvious, because clear key words are used. The number sign, #, denotes a comment.

5.4.3.1 Component Placement List.

Component placement lists (CPL) are ASCII or spreadsheet files used to transfer component *x, y* locations if CAD data files are not sent. CPL files are usually minimally formatted into columns. Required columns are the reference designator, *x, y* locations, and component rotation. In Fig. 5.15, the example CPL file also includes CAD package information.

```
!
! SIDE 1 !
R101        0   R0805          10467C    5065000    880000     90    SMT
R141        0   R0805          10467C    6670000    585000     270   SMT
R127        0   R0805          10467C    6595000    585000     270   SMT
R182        0   R0805          10467C    3850000    1260000    0     SMT
R199        0   R0805          10467C    4015000    1020000    0     SMT
R62         0   R0805          10467C    7885000    810000     180   SMT
R512        0   R0805          10467C    -45000     1065000    90    SMT
R6          0   R0805          10467C    3475000    140000     180   SMT
R214        0   R0805          10467C    3000000    1580000    0     SMT
R76         0   R0805          10467C    7940000    505000     90    SMT
R128        0   R0805          10488C    4275000    895000     0     SMT
R44         0   R0805          10488C    3850000    1415000    0     SMT
R59         0   R0805          10512C    8495000    1035000    90    SMT
M9          0   M_74F153_SO16  105328C   4835000    1305000    270   SMT
```

FIGURE 5.18 An example of a typical simple text tabulated CPL file. The first line translates as “Place resistor R101 at $x = 5.065$, $y = 0.88$ at 90°. Use part number 10467C. For information, see CAD package R0805. The mounting process is SMT.” This example is just a text file listing.

5.4.4 CAD Formats

The leading CAD system vendors have created several formats. When there is a high level of cooperation between customer and supplier, the design customer can send the whole design database from the CAD system on which it was created (and achieve the goal of intelligent exchange as depicted in Fig. 5.3). CAD formats are excellent for testing assembled boards because they include the schematic information. In addition, they include component locations and packages, as well as enough data to derive the graphics of any board layer. They must be accompanied by BOM information and also AVL information (unless parts are consigned) to define which components to place for each board variant and which components to procure.

CAD formats are less suitable for board fabrication, because they lack a flattened WYSIWYG ("what you see is what you get") representation of the circuit layers. Examples of CAD formats include Mentor's Board Station Neutral and Geoms files [4], as well as Cadence or ORCAD layout files.

When CAD formats are used for data exchange, their format is, by definition, the format of the specific CAD system that was used for layout and routing. The designer must therefore verify that the supplier can read it or use some translation tool to convert the data to a format readable by the supplier, risking conversion errors.

5.4.5 Modern Data Exchange Formats

5.4.5.1 ODB Format. Orbitech developed ODB++ as a "complete" data description format used for design to manufacturing (DFM) and CAD/CAM data exchange. It contains all the relevant design data for manufacturing and assembly. Section 5.4.1 provides details.

ODB++ and IPC-2581 are examples of formats that were explicitly designed for the purpose of CAD to CAM data exchange. ODB++ is the internal format for Valor's[5] tools and was developed early as an exchange format. IPC-2581 is a vendor-independent format developed as a joint effort by Valor and an IPC-sponsored committee to correct the historical problems associated with data exchange.

ODB++ and IPC-2581 are the only formats that can include all the data needed for manufacturing, including BOM and AVL information. They come closest to the idea of intelligent exchange depicted in Fig. 5.3.

5.4.5.2 ODB++. The ODB++ data format is a common language used for DFM and CAD/CAM data exchange. It overcomes many data communication obstacles within design/manufacturing supply chains. Data in this powerful open database impart an integrated and accurate physical model of all bare-board, component, and test-related information. It is designed as a simple yet comprehensive description of all entities used in the manufacture and assembly of a PCB.

The Valor Universal Viewer (VUV) is free software that enables ODB++ design data to be viewed graphically on Windows, Sun, or HP-UX workstations.

ODB++ uses a standard file system structure.[5] ODB++ denotes a job using a simple directory tree that can be transferred between systems with no loss of data (see Fig. 5.19).

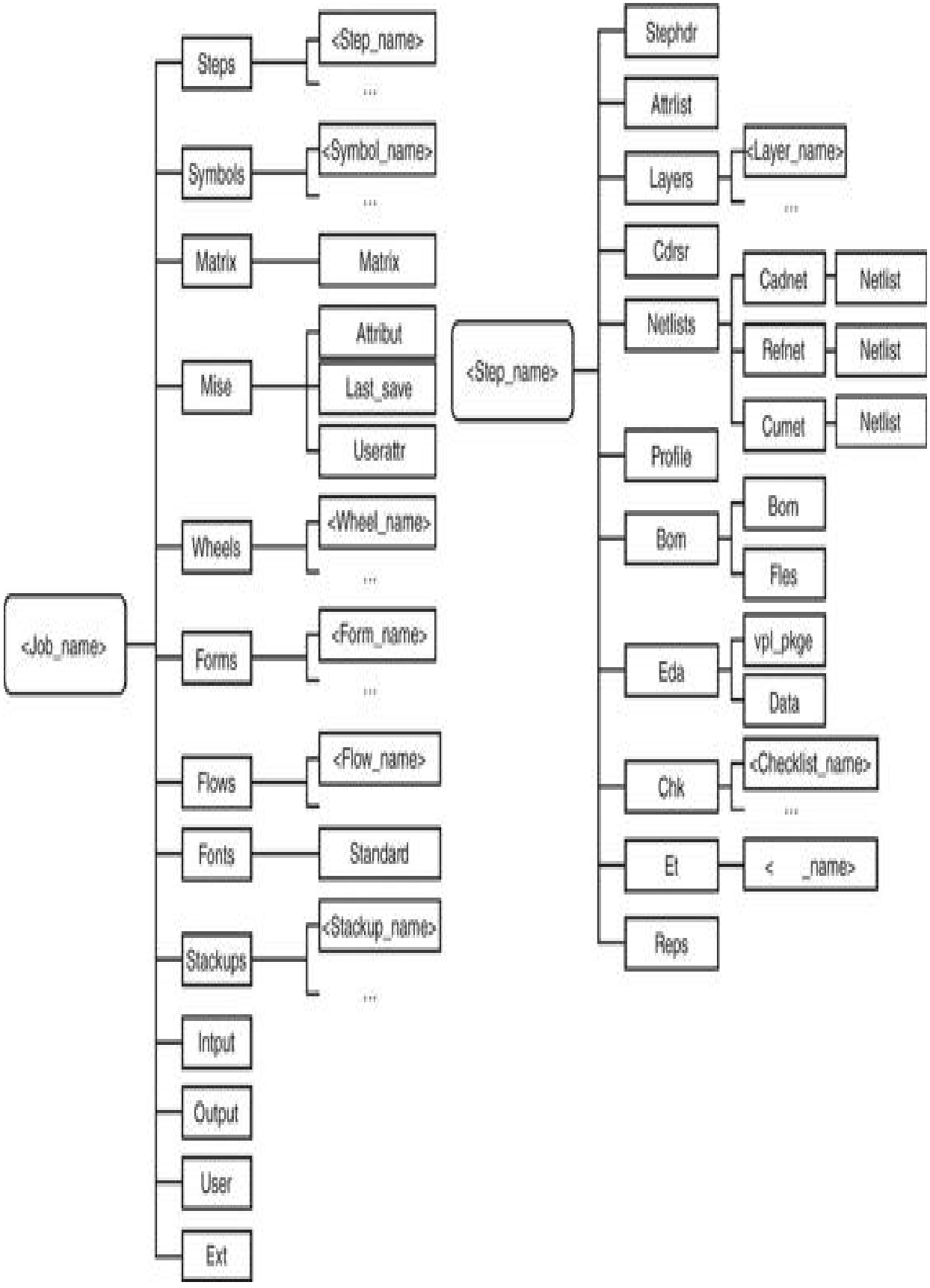

<Job_name>
Steps
<Step_name>
...
Symbols
<Symbol_name>
...
Matrix
Matrix
Misc
Attribut
Last_save
Userattr
Wheels
<Wheel_name>
...
Forms
<Form_name>
...
Flows
<Flow_name>
Fonts
Standard
Stackups
<Stackup_name>
...
Intput
Output
User
Ext
<Step_name>
Stephdr
Attrlist
Layers
<Layer_name>
...
Cdrsr
Netlists
Cadnet
Netlist
Refnet
Netlist
Cumet
Netlist
Profile
Born
Born
Flies
Eda
vpl_pkge
Data
Chk
<Checklist_name>
...
Et
< _name>
Reps

FIGURE 5.19 ODB++ job tree—the left-hand side of the figure describes the top-most elements under the job level and the right-hand side describes the top-most elements under the step level.

The advantages of a directory tree compared to one large file are apparent when a job is being read or saved. The flexible tree structure allows only selected parts of the job to be read or saved, avoiding the overhead of reading and writing a large file.

When a job must be transferred, standard compression utilities can be used to convert a directory tree into a single file.

ODB++ is widely used in the PCB industry and many vendor tools support it, including some CAD systems that offer output to ODB++ format. Description of all ODB++ format elements is beyond the scope of this chapter, but a small excerpt from a layer features file, shown in Fig. 5.20, can exemplify its explicitness and its clarity.

```
#
#Feature symbol names
#
$0 r3.937
$1 r5
$2 r5.118
$3 r5.906
$4 r9.843
$5 r13.779
$6 r19.685
$7 r23.622
$8 r27.559
$9 r30.315
$10 r39.37
$11 r53.15
$12 r55.118

#
#Feature attribute names
#
@0 .nomenclature
@1 .geometry
@2 .string
@3 .pad_usage
@4 .string_angle

#
#Layer features
#
P 5.3145669 3.215 0 P 0 0
P 5.1909449 3.1756299 12 P 0 2;1=0,3=0
L -0.3374074 1.5350394 -0.2950992 1.5249055 2 P 0 ;0,2=270.000000
L -0.2950992 1.5249055 -0.2598425 1.5249055 2 P 0 ;0,2=270.000000
```

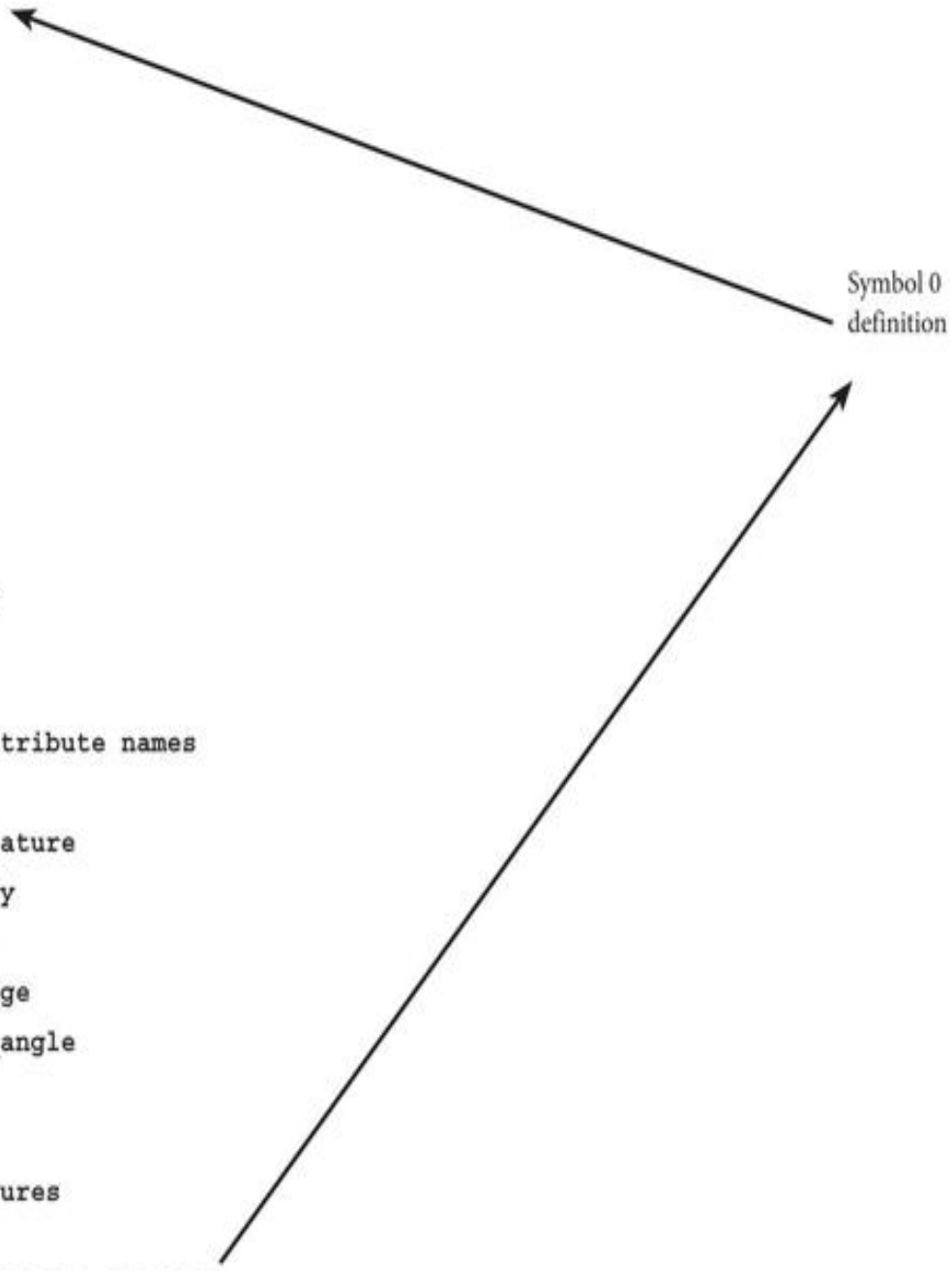


FIGURE 5.20 An ODB++ feature file with annotations. “P 5.3145669 3.215 0 P 0 0” indicates a pad at (5.314, 3.215) with a 3.937 mil diameter. (The first 0 points to symbol 0, clearly represented by “$0 r3.937” in the symbols section. “P 0 0” indicates that the pad has “P” (positive polarity), is not rotated 0°, and has zero attribute values.

5.4.5.3 IPC-2581. IPC-2581, on the part of the IPC and the electronics industry, is a universal vendor-independent data exchange format.[6] IPC-D-350 was the first such format in the 1970s, followed by IPC-2511 GenCAM in the 1990s; in the new millennium, IPC-2581 evolved.

IPC-2581 (nicknamed “Offspring”) is based on ODB++ and is the culmination of the ODB++ and GenCAM convergence project sponsored by the National Electronics Manufacturing Initiative (NEMI). IPC-2581 has inherited some of IPC-2511 GenCAM characteristics.

IPC-2581 is actually a series of IPC-258*x* documents, where *x* represents 1–9; IPC-2581 consists of the generic requirements (or, in this case, the full format description), whereas IPC-2582 and above are sectional requirements. IPC-2584, for example, contains the sectional requirements for fabrication and explains which generic IPC-2581 elements are required for bare-board fabrication and which elements are optional.

IPC-2581 is an all-inclusive, explicit, accurate, and intelligent format containing all data needed for both manufacturing and assembly. The following data elements can be described in a full-mode IPC-2581 file:

- Original schematic capture files
- Original layer/stack instance files
- Original conductor routing files
- BOM and AVL
- Component packages and logical Nets
- Outerlayer copper lands
- Solder mask, solder paste, and legend layers

- Drilling and routing layers
- Documentation layers
- Physical nets
- Outer copper layers (nonlands)
- Innerlayers
- Nondocument miscellaneous layers
- Instructions and specifications
- Component tuning and programming instructions, program files, and/or references thereof

This format contains information not available in the earlier formats (including details about personnel and the enterprise, material requirements, and component tuning and programming). Most industry tools lack these items in their internal formats, so at this point these sections are usable primarily in human-readable form.

Future evolution and market acceptance of IPC-2581 depend on committee work and vendor implementation and could well take several more years.

5.4.5.4 Component Information. BOM and AVL files do not usually follow any global standard, but rather conform to the internal standards of each organization. Their format may be simple ASCII or a spreadsheet (see Fig. 5.21). Interpretation of BOM and AVL files requires either manual or semi-automatic parsing followed by conversion into a known supported format. This process might entail creation of templates that recognize various types of BOM and AVL files and translate them semi-automatically.

ITEM	CPN	GEOM	COUNT	DESCRIPTION	REFERENCE		
1	1016975		1	SPROM_ASSY			
2	13r010c0	smd0402	6	cap, 1.0pF, sheet5	C502	C503	
					C504		
					C519	C587	
					C618		
3	13r030c0	smd0402	2	cap, 3.0pF, sheet6	C517 C545		
4	13r040c0	smd0402	1	cap, 4.0pF, sheet6	C531		
5	13r0r5c0	smd0402	1	cap, 0.5pF, sheet5	C591		
6	13r101j0	smd0402	3	cap, 100pF, sheet6	C500	C533	
					C536		
7	13r102k1	smd0402	5	cap, 1000pF, sheet5	C518	C571	
					C573		
							C581 C617

FIGURE 5.21 A typical spreadsheet-style BOM file containing the customer part number, part information, and reference designators.

BOM and AVL files are sometimes combined in a single BOM/AVL file that lists reference designators to be placed and part-ordering information.

Figure 5.22 is a typical AVL file sample as seen in already-tabulated format.

```
1    COMPONENT                  DESCRIPTION
2
3    VENDOR NAME                VENDOR ID     VENDOR PART ID 4
-------------------------------------------------------------------
5
6    XYZ00001                   CAP CHIP 1PF 0.25PF 50V COG 0402
7
8    KEMET ELECTRONICS CORPORA  KEMET         C0402C109C5GACTU
9    MURATA ELECTRONICS         MURATA        GRM36COG010C050AQ
10   TEXAS INSTRUMENTS          TI            GRM36COG010C050AQ
11
12   XYZ00002                   CAP CHIP 3PF 0.25PF 50V COG 0402
13
14   MURATA ELECTRONICS         MURATA        GRM36COG030C050AQ
15   TEXAS INSTRUMENTS          TI            GRM36C0G030C050AQ
```

FIGURE 5.22 Typical simple text tabulated AVL file excerpt.

The line numbers are not part of the file. Lines 1 through 5 are header lines and lines 6 through 15 are data lines. There are two types of data lines; line 1 contains column headers for the first line type, and line 3 contains column headers for the second line type. Lines 6 and 12 are lines of the first type, representing functional devices [usually referred to as customer part numbers (CPNs)]. Lines 8 through 10 and 14 and 15 are of the second type and represent alternative orderable part numbers [usually referred to as manufacturer part numbers (MPNs)].

Line 6 translates as “Part number XYZ00001 is a 1 Pico Farad chip capacitor of description ‘CAP CHIP 1PF 0.25PF 50V COG 0402,’” whereas line 8 translates as “to get the XYZ00001 functionality from Kemet Electronics Corporation, specify catalog number C0402C109C5GACTU.”

5.5 INITIAL DESIGN REVIEW

The purpose of the initial design review is to determine the potential fit of the product to the manufacturing facility, determine general cost information, and prepare for PCB information. Proper upfront analysis of a product prior to manufacturing or PCB information saves time and materials.

It is the responsibility of the manufacturing site to determine the fit of a given product to its capabilities. PCB manufacturing sites should monitor and maintain a list of manufacturing capabilities and a technology roadmap of where the facility is developing additional process capabilities. This list of capabilities defines the acceptability of a product for manufacturing or whether the product is a research and development project.

5.5.1 Design Review

Reviewing the incoming package for design and performance requirements (e.g., line width and spacing, impedance) versus the PCB manufacturing capabilities will define the capability for manufacturing and provide a prediction of the resulting yield. Among the design characteristics that should be reviewed against process capabilities are the following:

Item	Issue
Maximum number of layers	Higher-layer-count products require greater control of processes and PCB information tolerances.
Board thickness	Some process or handling equipment may have limitations on board thickness (either too thin or too thick).
Minimum feature width	Finer line widths require better control of artwork and process tolerances. In addition, the relationship of line width to copper weight is significant in providing a well-defined line. Fine lines with lower copper weights are easier to manufacture than fine lines with higher copper weights. For normal impedances, like 50 ohm, thinner lines will require thinner dielectrics.
Minimum feature spacing	Finer feature spacing requires better control of artwork and process tolerances. In addition, the relationship of feature spacing to copper weight is significant. Fine spaces with lower copper weights are easier to manufacture than fine spaces with higher copper weights.
	Minimum feature spacings affect electrical cross-talk. Closer spacing to reference ground will minimize this cross-talk.
Minimum finished hole size	Smaller holes require higher manufacturing process capabilities and imply (due to design characteristics) finer tolerances on PCB Information and internal registration systems. The aspect ratio (AR) of diameter to board thickness is a major process concern.
Maximum aspect ratio	Small holes and thick boards result in difficulty during the plating processes and can result in defective products that may or may not pass electrical testing. Plating high-AR holes requires chemistry and process parameter enhancements.
PCB dimensional tolerances	Fine PCB profile or cutout tolerances may result in punching/blanking requirements versus routing, or changes in the routing parameters or programming.
Feature-to-feature tolerances	The location of features on the PCB relative to other features may require alternative materials or process changes to reduce the tolerances.
Hole size tolerances	Consistency in the plating process versus selected drilling hole size and plating densities has significant impact on the capability to control hole tolerances. Adjustments to the PCB design, drill hole size selection, or process parameters may be required to produce an acceptable product with tighter tolerances.
Impedance requirements	The multilayer stack-up thicknesses and tolerances, along with the copper thickness and line widths, must match the nominal impedance and the upper- and lower-acceptability limit. Often, various impedances cannot be fabricated on the same layer.

5.5.2 Material Requirements

Determination of the bill of materials is required during the initial analysis of the design. The determination of the BOM and other material-processing requirements will define the manufacturing facility's capability to produce and its material cost structure. In addition, the definition of the material requirements will be the basis for the generation of the process traveler requirements.

The primary materials requiring definition are those included in the BOM, including laminates, prepregs, copper foil, solder mask, and gold. The materials may be explicitly defined by the PCB customer (e.g., usage of a specific solder mask), or may be implied in the drawings or specifications provided with the PCB Information package.

Several factors impact the selection of the raw materials, including the following:

- Customer-defined physical constraints, for example, the definition of the physical dimensions between conductive layers
- Customer specification of electrical properties, for example, the definition of the impedance requirements on certain layers
- Manufacturing process capabilities related to lamination thicknesses and tolerances
- Specification of material dielectric requirements, for example, the usage of FR-4 or polyimide
- Specifications of physical operating parameters, for example, the minimum requirements of the glass transition temperature

The determination of the laminates, prepregs, and copper foils are based on the following:

- Standard constructions for the PCB manufacturer of a defined PCB layer count, final thickness, copper weight, and dielectric spacing.
- Custom constructions based on defined physical constraints (e.g., minimum dielectric spacing). These custom constructions are defined through knowledge of the lamination pressing thickness of materials versus copper circuitry densities and the availability of materials from suppliers.
- Custom constructions based on defined electrical property constraints, such as controlled impedances, crosstalk, or capacitance. These custom constructions are typically defined via equations or software models provided with certain product parameters.

The determination of solder mask is based on the customer specifications and drawings. Once the acceptability of the solder masks is defined, the PCB manufacturer selects the acceptable masks based on either preferred process (due to volume or cost) or the design characteristics' interaction with the solder mask. These design characteristics include the following:

- *Tenting or plugging of vias*. A hole plugging epoxy may be preferred over liquid photoimageable solder mask with a secondary via plugging process.
- *Platable area densities/higher external copper weights*. Thin solder masks may not be able to ensure coverage of high plating.
- *Secondary processes*. Post-solder-mask processes may chemically or mechanically alter the appearance of certain solder masks.

The determination of gold requirements is based on the thickness and area of the gold. These factors can be used to calculate the requirement of gold per PCB product.

5.5.3 Process Requirements

The selection of the proper product routing (or traveler) is critical to the upfront analysis of the product acceptability to manufacturing. Considering a typical multilayer PCB product, the product routings can be broken into two parts: the innerlayer pieces and the outerlayer piece.

The product routings of the innerlayer pieces are fairly standard, and are typically as follows:

Step	Typical process requirements
Layer cleaning	Cleaning of the laminate surface via either mechanical or chemical cleaning processes
Imaging	Coating of the laminate with photoresist material and the exposure of the photoresist with artwork defining the innerlayer pattern
Develop-etch-strip (DES)	Developing of the photoresist, etching of the exposed copper, and stripping of the remaining photoresist
Innerlayer inspection	Inspection of the innerlayer piece to the PCB design intent
Oxide	Coating of the innerlayer piece with an oxide layer prior to lamination

One of the few decision points in innerlayer manufacturing is whether the product will require inspection. This decision can be based on the manufacturing facility's process capabilities and the design of the specific innerlayer piece. For example, if the process capability for innerlayer manufacturing of designs at 0.008 in lines and spaces is 100 percent yield, and the product has been designed at or above 0.008 in lines and spaces, then the product may not require inspection. Typically, the design package will identify the design technologies (e.g., line width and spacing);

however, these should be confirmed during the design analysis and review stage.

The product routings of the outerlayer pieces define the finished product appearance and, as a result, are more complex. Assuming a pattern plating process, the typical outerlayer process routings for a solder-mask-over-bare-copper (SMOBC)/hot-air-solder-level (HASL) product is as follows:

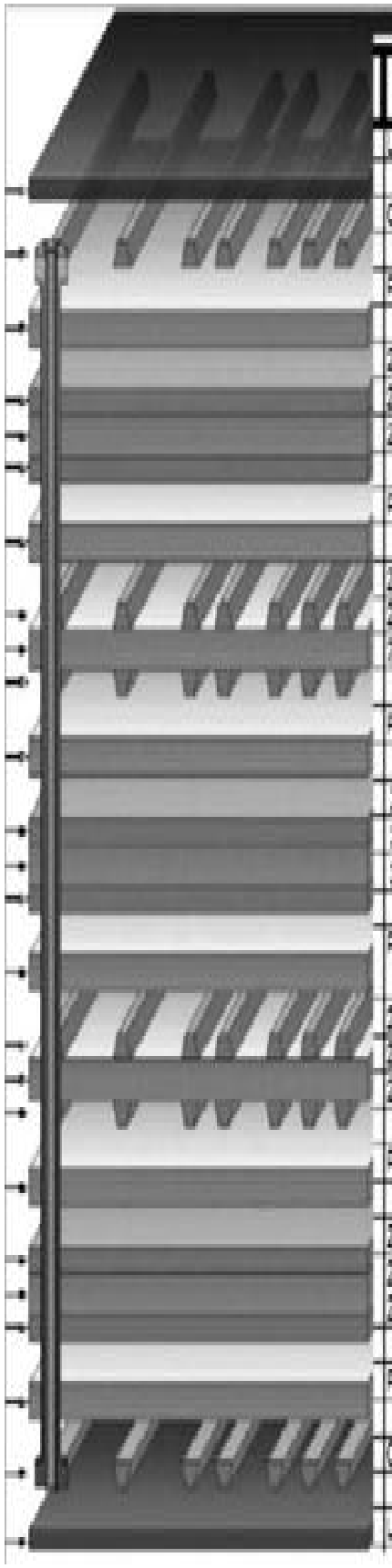
Step	Typical process requirements
Lamination	Lamination of innerlayer pieces with prepreg and copper foils to create the outerlayer piece
Drilling	Addition of the holes providing pathways for electrical conductivity between outer layer and innerlayer pieces and for other PCB design purposes
Electroless copper plating	Deposition of copper on the surface and in the holes of the product, providing the conductivity necessary for electroplating
Imaging	Coating of the panel with photoresist material, the exposure of the photoresist with artwork defining the outerlayer pattern, and the developing of the outerlayer pattern
Electroplate copper	The plating of the final circuitry of the product
tin plating	Sacrificial plating over the final circuitry of the product
Strip-etch-strip (SES)	Stripping of the remaining photoresist, etching of the exposed copper, and stripping of the sacrificial plating
Solder mask	Coating of the bare copper product with either dry film or liquid photoimageable solder mask, exposing of the panel with the PCB customer-supplied artwork pattern, developing of the pattern (exposing the sites requiring solder), and curing of the solder mask
Nomenclature	Screening of the nomenclature onto the panel and curing
HASL	Coating of the exposed copper sites with solder, leveling to the customer's requirements of thickness
Depanelization	NC routing of the PCB products from the manufacturing panel
Electrical testing	Electrical testing of the product for conformance to the PCB design
Inspection	Verification of product conformance to specifications prior to shipment to the PCB customer

After the electroplate copper operation, the process may change to meet the surface finish requirements. Some of the alternative steps affecting the outerlayer product routing include the following:

Item	Typical process requirements
Selective gold plating	Before the SES process, the panel is coated with additional resist and the selective sites are exposed. These exposed sites are then plated with nickel and gold. The panel will then proceed through the SES process. The HASL step would be omitted.
NPTH in planes without annular ring	A secondary drilling operation will be required to drill the holes, if the hole is to be located through the copper or the hole/feature size is beyond the process capabilities of tenting. This step may occur at the depanelization step.
Scoring	Additional PCB Information holes may be required to register the panel to the scoring machine blades. Programming of the scoring machine will be required to set the locations and depth of the cuts. This step may occur prior to NC routing of the product.
Countersink holes	The countersinking process is normally performed prior to depanelization.
Gold finger plating	Nickel and gold are plated over the finger area on connectors. This process typically requires shearing/NC routing separation of the panel to place the fingers at the edge of the remaining pieces, taping the product to expose only the fingers, stripping the solder, plating nickel, plating gold, and removing the tape. These operations occur prior to the depanelization process. Finger-plated products usually require chamfering of the fingers.
Via plugging	Plugging of vias may occur prior to solder mask or after the HASL operations.
Chamfer	After depanelization of the products from the manufacturing panel, the PCB products are processed through a machine to add an angle to the edge of the part or fingers.
Organic coating	Products requiring organic coating would omit the HASL step and be coated prior to inspection.

5.5.4 Multilayer Stack-Up

Multilayer stack-up, defined in Sec. 17.2.2 and Chap. 31, must be carefully specified. This is the function of the stack-up definition (see Fig. 31.2), which is usually part of the fabrication drawing. Impedance specifications (from the electrical performance data block) should be compatible with the materials stack-up. Figure 5.23 shows a cross-sectional view of the finished multilayer. Figure 5.24 shows the stack-up code.



Description	Stock No	Usage	Base	Finish	Er
Liquid Photoimageable Mask	PSR-4000 BL-3	Mask	0.600		4.100
Copper Foil	H oz	Copper	0.000	2.000	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
2116 Core	NP-170TL	Copper	1.300	1.300	
2116 Core	NP-170TL	Dielectric	4.000	4.000	4.270
2116 Core	NP-170TL	Copper	1.300	1.300	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
2-1080 Core	NP-170TL	Copper	0.600	0.600	
2-1080 Core	NP-170TL	Dielectric	4.000	4.000	3.900
2-1080 Core	NP-170TL	Copper	0.600	0.600	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
2-2116	NP-170TL	Copper	1.300	1.300	
2-2116	NP-170TL	Dielectric	10.000	10.000	3.990
2-2116	NP-170TL	Copper	1.300	1.300	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
2116 Core	NP-170TL	Copper	0.600	0.600	
2116 Core	NP-170TL	Dielectric	4.000	4.000	4.270
2116 Core	NP-170TL	Copper	0.600	0.600	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
2116 Core	NP-170TL	Copper	1.300	1.300	
2116 Core	NP-170TL	Dielectric	4.000	4.000	4.270
2116 Core	NP-170TL	Copper	1.300	1.300	
Prepreg 2313	NP-170B	Dielectric	3.700	3.700	3.840
Copper Foil	H oz	Copper	0.600	2.000	
Liquid Photoimageable Mask	PSR-4000 BL-3	Mask	0.600		4.100

FIGURE 5.23 Stack-up drawing to define thickness, layer order, and tolerances for a multilayer.

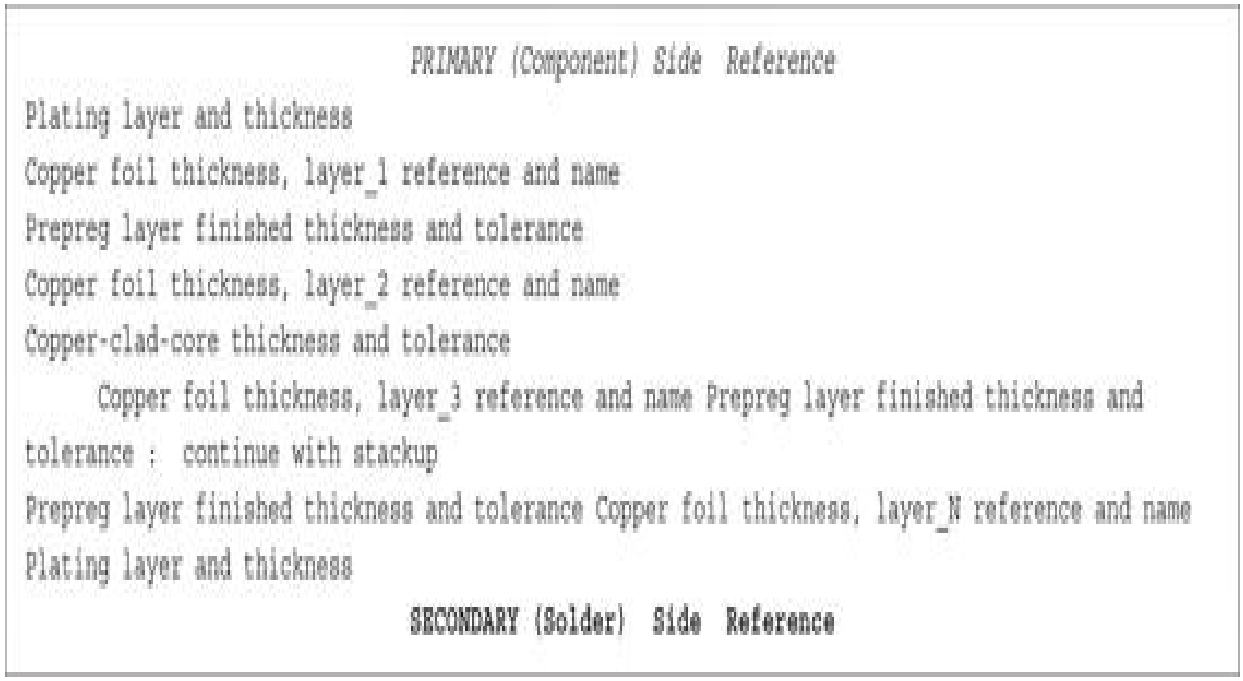


FIGURE 5.24 Stack-up code listing.

5.5.5 Panelization

The selection of the manufacturing panel is one of the most important steps in achieving product profitability. Several factors affect the selection of panel sizes to produce a specific product. These include

- Material utilization
- Process-specific constraints
- Process limitations

All of these factors impact the selection of the manufacturing panel size and the profitability of the product.

5.5.5.1 Material Utilization. The material manufacturing costs, which correspond to 30 to 40 percent

of total costs, are directly related to the square inches of material processed. The material costs can include the following: laminate, prepreg, copper foil, solder mask, photoresists, drill bits, chemicals, and so on. Generally, these materials are consumed relative to the panel area manufactured.

The appropriate manufacturing panel size (see Fig. 5.25) should be selected such that the shippable product consumes the highest percentage of the manufactured panel as possible, thus reducing waste material and product costs.

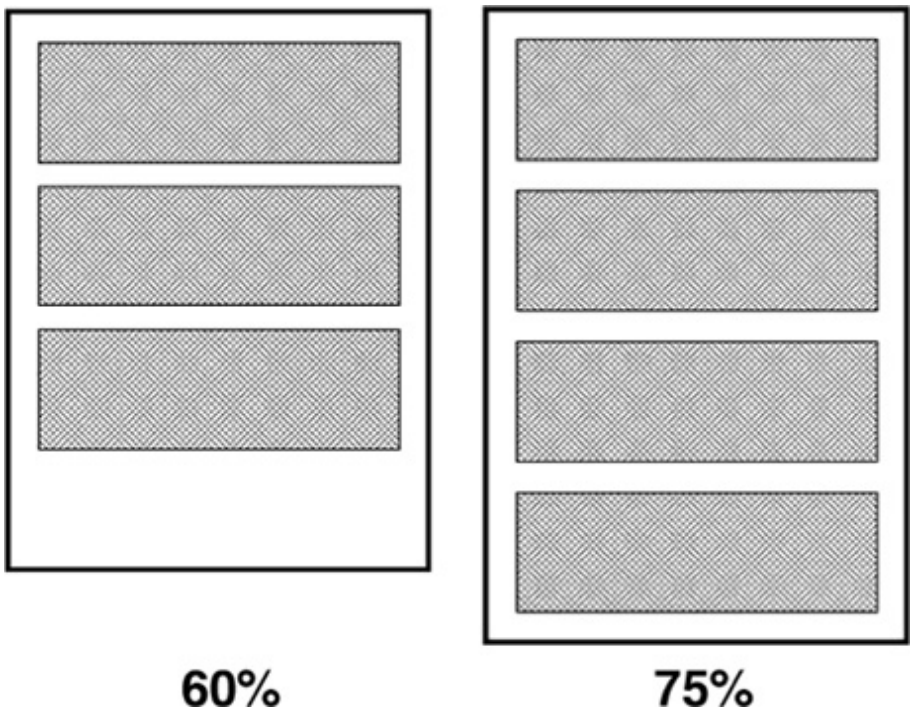


FIGURE 5.25 Selection of the best panel to increase the material utilization of the shippable product.

During the design phase of the PCB, the board profile is defined. If the profile's design results in poor manufacturing panel utilization, it will significantly impact the cost of the product. When defining the PCB board profile, the PCB designer should ask the manufacturing site to provide DFM feedback. Oddly shaped PCB profiles can still result in good material utilization, through nesting of the PCB on the panel.

General limitations in the selection of appropriate panel sizes include the following: minimum spacing between products for depanelization processes (typically 0.100 in) and minimum panel border-to-product spacing to permit PCB information and registration systems (typically 1.0 in).

In Asia, minimizing materials to minimize costs plays a much more important role than in North America or Europe, where rapid turnaround time may be the singular focus. Table 5.1 shows a typical set of multilayer panel sizes for a large Asian PCB manufacturer.

TABLE 5.1 Typical Multilayer Panel Sizes for a PCB

Type	Panel Size (in)	Useable Area (with soldermask)
Standard	12 × 14	10.2" × 12.2"
Standard	12 × 16	10.2" × 14.2"
Standard	12 × 20	10.2" × 5.2"
Standard	13 × 16	11.2" × 14.2"
Standard	13 × 20	11.2" × 5.2"
Standard	14 × 16	12.2" × 14.2"
Standard	14 × 20	12.2" × 5.2"
Standard	14 × 21	12.2" × 19.2"
Standard	14 × 22	12.2" × 5.2"
Standard	14 × 23	12.2" × 21.2"
Standard	14 × 24	12.2" × 22.2"
Standard	16 × 20	14.2" × 5.2"
Standard	16 × 21	14.2" × 19.2"
Standard	16 × 22	14.2" × 5.2"
Standard	16 × 23	14.2" × 21.2"
Standard	16 × 24	14.2" × 22.2"
Standard	17 × 14	15.2" × 12.2"
Standard	18 × 14	15.2" × 12.2"
Standard	18 × 16	15.2" × 14.2"
Standard	18 × 20	15.2" × 5.2"
Standard	18 × 22	15.2" × 5.2"
Standard	18 × 23	15.2" × 21.2"
Standard	18 × 24	15.2" × 22.2"
Chip packaging	12 × 18	10.0" × 15.0"
HDI-microvia Optional	16 × 18	14.0" × 15.0"

5.5.5.2 Product Process-Specific Constraints. In the selection of manufacturing panel sizes, there may be processing constraints that restrict the usage of specific panels or limit the method of placing the shippable product on the panel. For example, the manufacturing of products with gold tab plating may require additional spacing between products and restrictions on the rotation and nesting of products. These constraints may force the usage of panel sizes below the optimal material utilization.

5.5.5.3 Process Limitations. Process limitations may require the usage of nonoptimal panel sizes. For example, due to a product's registration requirements, additional PCB Information may be required, thus reducing the available area for shippable product and reducing the material utilization. Another example is the limitations of some processes to permit larger panel sizes due to the physical processing constraints of the equipment.

The panelization process results in the placement of the PCB single images in the locations defined in the panelization definition step during the initial design review. In addition to the placement of the PCB single images and rotated/nested images (Fig. 5.26), the following features may be added to the panel for manufacturing.

FIGURE 5.26 Nesting and rotation of a multi-image panel.

5.5.6 Initial Design Analysis

After the initial design review, the basics of the design are known and a decision on whether to manufacture the design has to be made. If it is decided to proceed with manufacturing, the cost of the product must be determined. Once the cost has been determined, the product price can be provided to the PCB customer.

The material and process requirements with the manufacturing panel selection, combined with the prediction of yield based on the design review, define the basics of the product costs.

5.5.6.1 Automated Design Analysis. Many automated design analysis software systems exist. You can find them on the Internet by searching on key words such as “Automated Design Analysis,” “Computer Aided Manufacturing,” or “Design Validation.” Figure 5.27 shows a report resulting

from a CAM macro executed on an ODB++ design file, “8-Layer.”

Date Sun Mar 12 17:48:51 2006	Agent file used

Quote Report

Operator:	H Holden	Job#.	8–Layer	Rev:	1st.

No Logo	PCB fabricator 612 Wheelers Farms Road Milford CT 06461 USA 203–283–3000
Customer:	XYZ Corporation Holden Cust Street Address Anywhere CT 00000 USA
Phone: Cust phone	**Fax:** Cust for
E-mail Cust Email	

Board information

Board size: 9.050" x 5.377"	**Thickness:** 0.062 mil	**Border layer present?**	No
Panel size 22,000" x 16.000"	**Core size** 4.000 mil	**# of nets**	562
Laminate type	NP–170	**Copper weight**	0.50 oz.

Total (Elec.) layers: 8	# of internal layers: 2	# of plane layers: 6	POS 2	NEG 0

Drill information

# of drill tools/total count	10	1768	**Blind buried vias?** Yes
Smallest drill/total count	13.000 mil	1484	**# of drill Files.** 1
Tightest drill to trace:	0.064 mil		

Design analysis

	Internals	Other (user defined):
Smallest trace:	6.000 mil	6.000 mil
Smallest airgap	5.000 mil	5.000 mil
Smallest annular ring:	N/A	0.000 mil
Smallest thermal annular ring:	N/A	0.000 mil
Smallest pad:	20.000 mil	20.000 mil

SMT pads:

# of pads.	Top	Bottom	Total
	912	1288	2200

Smallest pitch	Top	Bottom
	19.680 mil	2.000 mil

Gold tabs:

# of fingers: Top	# of fingers: Bottom	Finger size: Length	Finger size: Width
0	22	600 0 mil	250.0 mil

Gold thickness 0.0000 15 mil

Soldermask info:

Top: Yes **Bottom:** Yes

Vias tented/plugged Yes

Silkscreen info:

Top: Yes **Bottom:** Yes

Color: White

FIGURE 5.27 Automated design analysis report performed on an ODB++ file.

5.5.6.2 Design Analysis Checksheet. Figure 5.28 shows a design analysis checksheet for determining whether a PCB design is ready for manufacturing.

Checklist

CAD netlist compare
Annular ring error
Padstack checklist
Plane clearence error
Manufacturability analysis,DRC
Thermal leg count violation
Circuit checklist
Unterminated lines
Resist slivers
Copper islands
Solder mask checklist
Sholder short violation
Mask coverage
Mask to via check
Sloder paste check
Silkscreen clipping
Teardrop pad addition
Part to part clearence/automation
Quality parts
Hole audit/lead diameter
Part density
Height clearence
Allowable machine span
Part spacing
Drill optimization
Automatic solder mask generator
Bare board test points
In-circuit test point analysis
In-circuit test checklist
Boundary scan audit
Test point management
Design profile
Registration generator
Keepout audit

FIGURE 5.28 A design analysis checksheet.

5.6 DESIGN INPUT

The input of the design into the CAM system is primarily performed by defining the apertures and shapes to be used and then loading Gerber data into the PCB CAM system. Alternatively, most PCB CAM systems accept the IPC-350 format.

The information loaded into the PCB CAM systems includes all artwork layers (e.g., circuitry layers and solder mask layers) and the drill files. Although some PCB CAM systems can accept NC routing files (i.e., board profiling), these files are normally not part of the PCB design system's capabilities to create, and therefore are not provided to the PCB manufacturer.

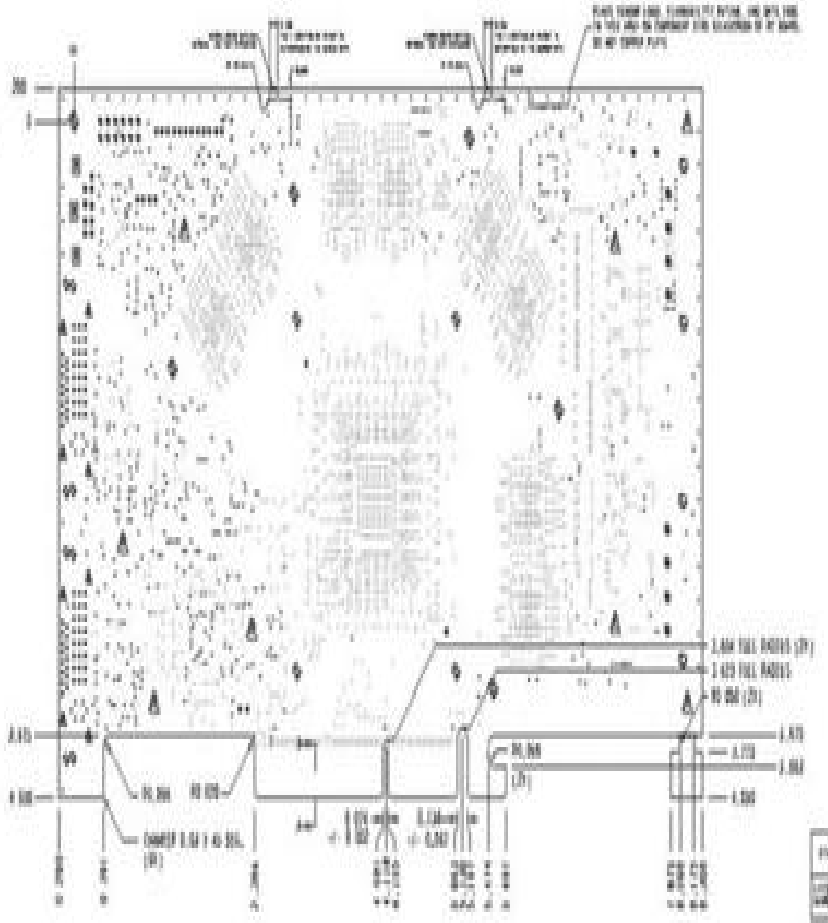
Before loading the PCB design files, the PCB CAM operator must relate the aperture codes within the design file to physical shapes within the PCB CAM system. These shapes are usually round, square, and rectangular, but may also include complex shapes (e.g., thermal relief pads for innerlayer planes). The complex shapes may need to be created on the CAM system from information provided by the PCB designer. The complete definition of these complex shapes by the PCB designer is critical to the success of the resulting design. Incomplete descriptions could result in nonfunctional designs.

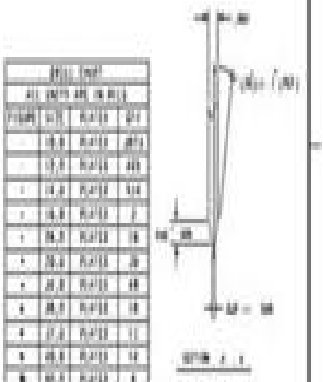
During the loading process of the design files, it is important to review any log files and screen messages for missing aperture definitions or damaged design files. After loading the files, the PCB CAM operator should review the design for any problems with the interpretation of the data or apertures while aligning the data for further processing. The PCB CAM operator also must ensure that the apertures

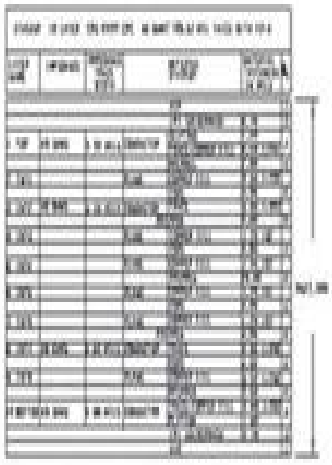
match those defined by the PCB designer and that the design input process has proceeded without failure, since subtle errors may not be discovered within the manufacturing site but only at the PCB customer site, and such errors could result in nonfunctional designs.

5.6.1 Documentation

5.6.1.1 Drill Drawing Example. Figure 5.29 shows an example of a drill drawing.







NOTES: UNLESS OTHERWISE SPECIFIED:

1. MATERIAL : GLASS-EPOXY RESIN SHEET, MEETING REQUIREMENTS OF NEMA GRADE FR-4 OR EQUIVALENT.
2. FINISH: COPPER, MACROETCH 120 MICROINCHES MINIMUM. SOLDER MASK OVER BARE COPPER, BLACK, MATTE FINISH.
3. EDGE FINGERS: ELECTROPLATING: 50 MICROINCHES GOLD OVER 100 MICROINCHES NICKEL.
4. FINISH: SOLDERMASK OVER BARE COPPER (ALSO ON UNUSED AREAS) THICKNESS: 1000 MIN. SOLD MASK THICKNESS COLOR - GREEN.
5. CONNECTOR HOLES: TOLERANCE: .002 MIN UNLESS OTHERWISE STATED. CONNECTOR HOLES: SMOOTH, BREAK ALL SHARP EDGES AND CORNERS.
6. SILKSCREEN LEGEND TO BOARD USING WHITE, NON-CONDUCTIVE, EPOXY BASED. REMOVE SILKSCREEN FROM PADS.
7. TOLERANCES: MACHINING: .010 / INCH MIN ALONG CONNECTOR EDGE. ETCHING: +/- 20% OF MASTER PATTERN. HOLE DIAMETER: + .003 +/-.002, -.003 +/-.002 HOLE DIAMETER + .004 - .002 - (HOLE DIAMETER)
8. ACCEPTABILITY BASED ON [illegible] SPEC 6012-0010 (LATEST REV.) AND IPC-A-600 CLASS 2, (LATEST REV.) REFER TO [illegible] SPEC FOR ORDER OF PRECEDENCE.
9. TEST ALL BOARDS FOR OPENS AND SHORTS.
10. DO NOT SOLDER MASK OVER BY-PASS PAD.
11. NO SOLDERMASK ON FIDUCIALS.
12. NO SOLDERMASK MAY COVER ANY GOLD FINGERS.
13. DO NOT USE TOP-TO-BOTTOM PAD ALIGNMENT VIA ALIGNMENT IS RECOMMENDED.
14. NO HEATSINK MODIFICATIONS ALLOWED WITHOUT PRIOR WRITTEN APPROVAL FROM [illegible]. EXCEPT FOR TOLERANCE TRACK MINIMAL MODIFICATIONS TO MEET REQUIREMENTS AND THE ADDITION OF SLAB GROOVES WHERE REQUIRED.
15. DCM SHOWS CCP TO PROVIDE FINAL ARTICLE PRIOR TO [illegible].
16. ANNULAR RING CLEARANCES ON THIS BY DESIGN IS PLATED
17. THIS BOARD HAS BLIND VIA ON TOP TO INT2 SEE SHEET 2

DO NOT SCALE DRAWING

REVISIONS				
ITEM	REV	DESCRIPTION	DATE	APPROVED

FIGURE 5.29 Example of a drill drawing.

5.6.1.2 Fabrication Drawings. See Fig. 5.30 for an example of a fabrication drawing.

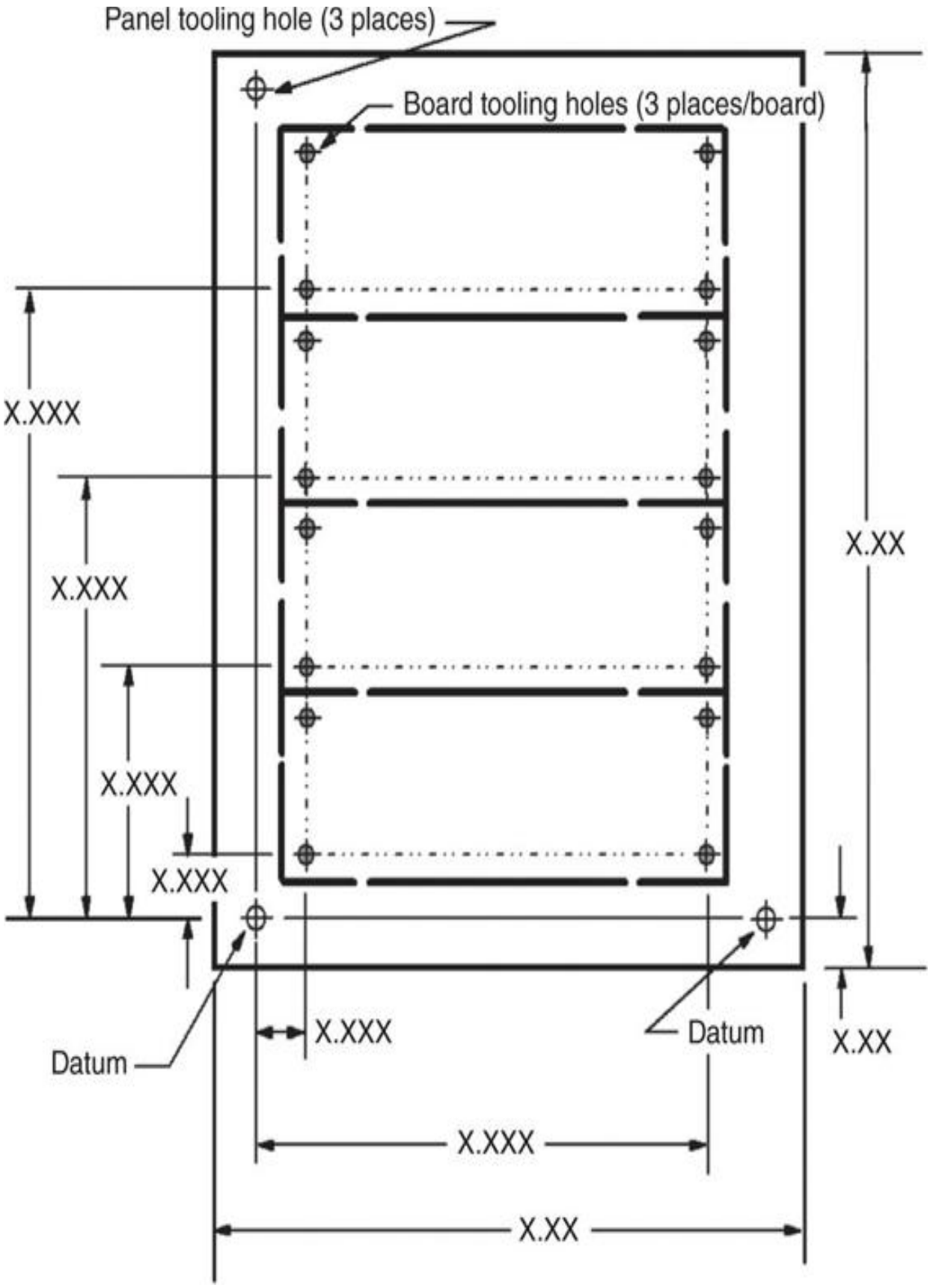

Panel tooling hole (3 places)
Board tooling holes (3 places/board)
X.XXX
X.XXX
X.XXX
X.XXX
X.XX
Datum
X.XXX
Datum
X.XX
X.XXX
X.XX

FIGURE 5.30 Example of a fabrication drawing

5.6.1.3 Stack-Up Drawing.

Figure 5.31 shows a stack-up drawing.

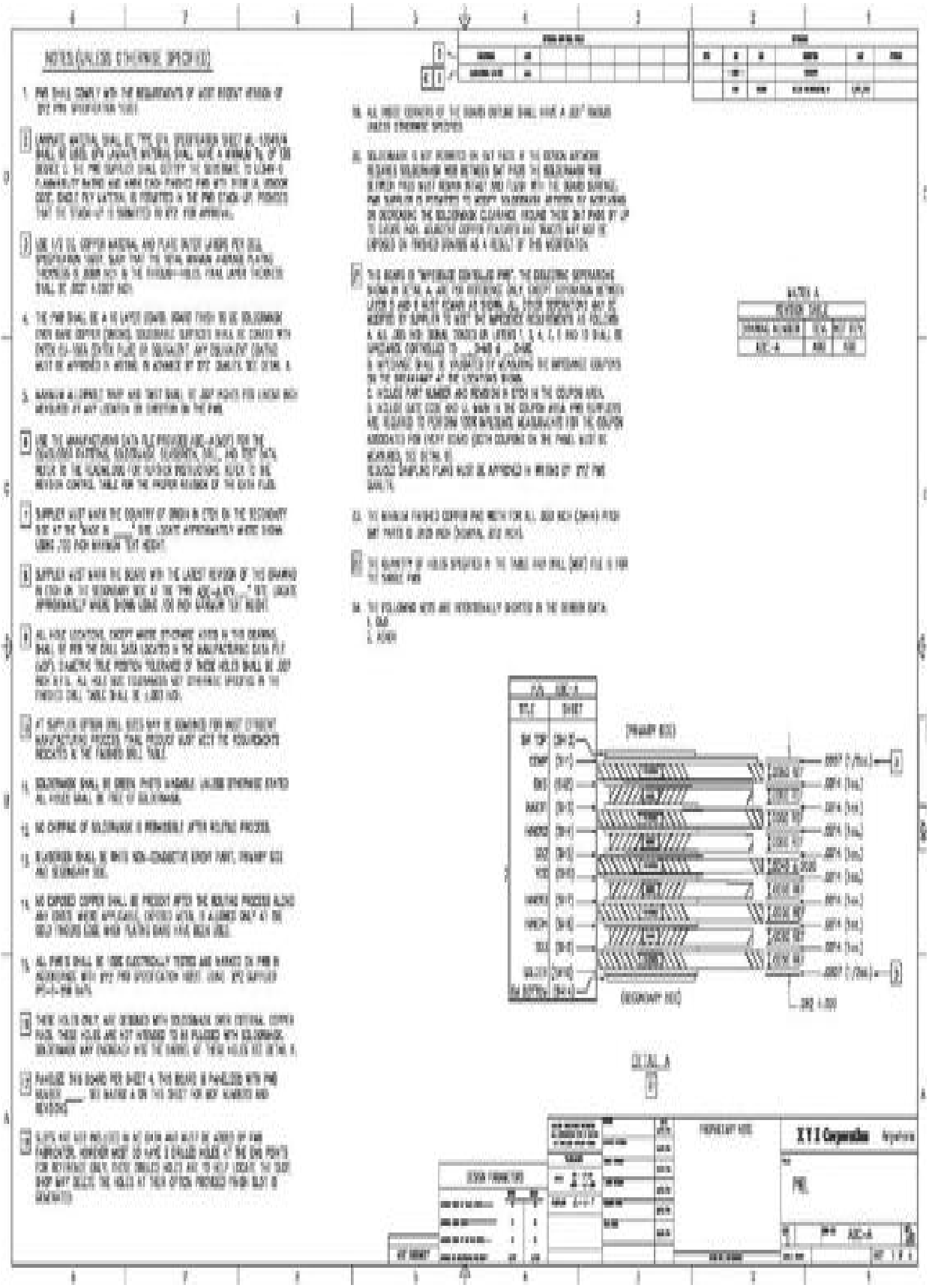


FIGURE 5.31 Example of a stack-up drawing.

5.6.1.4 Stack-Up Data Block. Table 5.2 shows an example of a stack-up data block.

TABLE 5.2 Example of a Stack-Up Data Block

P/N	ABC-d
Title	Sheet
S/M top	(SH14)
Component	L1-(SH 1)
Ground	L2-(SH 2)
Power	L3-(SH 3)
Signal_1	L4-(SH 4)
Signal_2	L5-(SH 5)
Power	L6-(SH 6)
Power	L7-(SH 7)
Signal_3	L8-(SH 8)
Signal_4	L9-(SH 9)
Power	L10-(SH 10)
Ground	L11-(SH 11)
Solder	L12-(SH 12)
S/M	(SH 13)
Bottom	

5.6.1.5 Manufacturing Notes. Figures 5.29 and 5.30 show examples of manufacturing notes.

5.6.2 Electrical Performance Data Block

Table 5.3 shows an example of an electrical performance data block.

TABLE 5.3 Example of an Electrical Performance Data Block

Bus	Data	Agp 8x	PCI	DDR2/3 clocks
Type	Single	Single	Differential	Differential
Tolerance	50 ohms ± 10%	55 ohms ± 10%	100 ohms ± 10%	120 ohms ± 10%
Geometry (mils)	Trace/space	Trace/space	Trace/space Space to other pair	Trace/space Space to other pair
Top (Layer 1)	9.5/10 (Ref L2)	7.75/10 (Ref L2)	5.0/6 (Ref L2)	4.0/10 (Ref L2)
PWR (Layer 2)	VCC	VCC	VCC	VCC
GND (Layer 3)	GND	GND	GND	GND
Signal 1 (Layer 4)	4.5/4.5 (Ref L3 & L6)	3.725./4.25 (Ref L3 & L6)	4/10/4/10 (Ref L3 & L6)	3/10/3/10 (Ref L3 & L6)
Signal 2 (Layer 5)	4.5/4.5 (Ref L3 & L6)	3.725./4.25 (Ref L3 & L6)	Not allowed	Not allowed
PWR (Layer 6)	VCC2	VCC2	VCC2	VCC2
PWR (Layer 7)	VDD	VDD	VDD	VDD
Signal 3 (Layer 8)	4.5/4.5 (Ref L7 & L10)	3.725/4.25 (Ref L7 & L10)	Not allowed	Not allowed
Signal 4 (Layer 9)	4.5/4.5 (Ref L7 & L10)	3.725/4.25 (Ref L7 & L10)	4/10/4/10 (Ref L7 & L10)	3/10/3/10 (Ref L7 & L10)
GND (Layer 10)	GND	GND	GND	GND
PWR (Layer 11)	VCC1	VCC1	VCC1	VCC1
Bottom (Layer 12)	9.5/10 (Ref L11)	7.75/10 (Ref L11)	5.0/6 (Ref L11)	4.0/10 (Ref L11)
Measurement requirement	Measure on coupon	Measure on coupon	Measure on coupon	Measure on coupon

5.7 DESIGN ANALYSIS AND REVIEW

Design analysis and review is a refinement of the initial design review performed earlier but is the first step in the CAM (soft-PCB Information) process. This step focuses on the actual design data submitted for fabrication and assembly. The design analysis and review step consists of the following tasks:

- Design rule checking
- Manufacturability analysis
- Single-image edits
- DFM enhancements
- Panelization
- Fabrication parameters extraction

These tasks provide the final checking of the PCB design requirements against the capabilities of the PCB manufacturer and preparation of the design for manufacturing.

Most fabrication problems occur or are discovered during the initial PCB Information (CAM) phase. The following are among the causes of such problems:

- Poorly documented designs
- Improperly formatted drill files
- Use of 274-D Gerber with separate aperture tables
- Lack of proper clearance on solder mask openings
- Inadequate drill-to-copper clearance
- Misaligned layers
- Inadequate manufacturing clearances
- Lack of an IPC-D-356 netlist
- Use of positive plane layers instead of negative ones

- Minimal communication between the designer and the fabricator

The best advice for these problems is to fix them during the design phase. Consider the following precautions and considerations:

- Try not to use 274-D with separate aperture tables.
- Because there are no standards for aperture tables, the fabricator must do extra work to accommodate the tables, with increased opportunity for error.
- Use 274-X whenever possible. The apertures are embedded and files are easier for the fabricator to work with. This provides better support for special aperture shapes.
- Better yet, if possible, use “intelligent” formats like GenCAM, DirectCAM, or ODB++. These formats should enable the fabricator to better understand your design. Also, such formats have the netlist information embedded.
- Design rules can be embedded in some formats.

5.8 ACKNOWLEDGMENTS

Portions of this chapter were taken from Chap. 18, “Information Formating and Exchange,” written by Bini Elhanan for the *Printed Circuits Handbook*, 6th ed. (Coombs), 2008.

I would like to thank Jeff Miller, WISE Software Solutions (www.wssi.com); DownStream Technologies (www.downstreamtech.com); and Julian Coates of Valor, Inc. (www.valor.com) for their invaluable contributions to this chapter.

5.9 REFERENCES

1. Dean, Graham, “A Review of Modern Photoplotting Formats,” Electronics Manufacturing Technology, http://www.everythingpcb.com/p13447.htm.
2. Document 40101-S00-066A, Mania Barco Corporation. (http://members.optusnet.com.au/~eseychell/rs274xrevd_e.pdf)
3. http://www.artwork.com/gerber/appl2.htm.
4. Mentor Graphics Fablink User’s Manual. (www.mentor.com/)
5. Valor ODB++ manual, available upon request from Paul Barrow at Paul.Barrow@valor.com; Tel, +972-8-9432430 (ext. 165); Fax, +972-8 – 9432429; Valor Computerized Systems, Ltd., P.O. Box 152, Yavne 70600, Israel.
6. IPC-2581, “Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology”; IPC-258x and sectional requirements thereof, Institute for Interconnecting and Packaging Electronic Circuits, 3000 Lakeside Drive, Bannockburn, IL, USA.

[a] Some of the material in this chapter was written by Bibi Elhanan-Valor.

[b] See http://www.lookuptable.com/

[c] References ANSI/IPC-D-356 published by the Institute for Interconnecting and Packaging Electronic Circuits (IPC).

CHAPTER 6

SUPPLIER SELECTION AND QUALIFICATION

Tim Rodgers
University of Colorado, Boulder, Colorado

6.1 INTRODUCTION

In this chapter the business considerations and selection criteria initially described in Chap. 3, “Basics of Printed Circuit Supply Chain Management,” will be applied to evaluate and select printed circuit board (PCB)/printed circuit assembly (PCA) suppliers. The chapter also includes recommendations and benefits for creating a formal supplier qualification program and approved vendor list (AVL).

Whether a business is looking for a supplier that will only be used for a single purchase order, or a long-term partner that will become a key element in the value delivery system, it’s important to have a methodology for assessing supplier capabilities and performance. It is very likely that there will be multiple suppliers who can meet the needs of the business, some possibly better than others. It’s not a good idea to choose any random supplier for such an important

component, especially if the customer expects to place multiple purchase orders over the life of a single product. The time and cost required to change suppliers because of poor performance can be significant.

Chapter 3 provided a framework for considering how PCBs and PCAs fit into the overall new product design and development process, and how they ultimately support the business's supply chain strategy. The cross-functional sourcing strategy team must understand the needs of the business and the relative importance of supplier performance characteristics, including technology, responsiveness, quality, cost, and the availability of other services. See Table 6.1 for a summary of the common considerations for evaluating PCB/PCA suppliers:

TABLE 6.1 PCB Supplier Performance Criteria

Category	Examples
Technology	Electrical (thick copper, dielectric) Thermal (low TCE) Dimensional (flexible or molded circuit) Assembly (surface finish, tolerances)
Responsiveness	On-time delivery Rapid prototyping Lead time
Quality	Conformance to industry standards Conformance to internal specifications Order completeness Accuracy of required documentation
Cost and Price	Price per unit Supplier management costs
Other Services	Design support Locally-based sales or technical staff

- Technology
- Responsiveness
- Quality
- Price and cost

While it’s easy to ask suppliers about their capabilities, it can be difficult to objectively determine whether a supplier can sustain the required performance and meet the needs of the business over the long term. This chapter provides a review of some of the more common methods used to

evaluate supplier processes and work products that will give the sourcing team more confidence in selecting a supplier.

Finally, many companies use a formal supplier qualification program that includes an AVL. Suppliers on the AVL are favored for new purchase orders, and teams may require special approval to use a supplier that is not on the AVL. This chapter describes some of the benefits that can be realized by both the supplier and the customer with such a program.

6.2 EVALUATING SUPPLIERS

It has become quite easy to find suppliers today by using standard Internet search methods. The Institute of Printed Circuits (IPC) maintains a database of member manufacturers and suppliers for both PCBs and PCAs with links to their respective websites. Suppliers will typically advertise their standard capabilities, and they often include their target markets and a list of some of their major, current customers. If the supplier is already working with customers in your market segment, then they should be familiar with the technology and quality requirements.

A supplier capability matrix is very commonly used to present the standard product and service offerings, and this can also make it convenient to quickly compare the standard offerings from different suppliers. Table 6.2 is an example of a capability matrix that uses readily available information from supplier websites, sales brochures, and other sources.

TABLE 6.2 Example of a Supplier Capability Matrix

Inner Layer Feature	Standard	Special/Premium
Minimum conductor width		
• 0.5 oz or 1 oz copper	0.1 mm (0.004")	0.075 mm (0.003")
• 2 oz copper	0.15 mm (0.006")	0.125 mm (0.005")
Minimum spacing width		
• 0.5 oz or 1oz copper	0.125 mm (0.005")	0.1 mm (0.004")
• 2 oz copper	0.15 mm (0.006")	0.125 mm (0.005")
Tolerances		
• 0.5 oz copper	±0.01 mm (0.0004")	
• 1 oz copper	±0.015 mm (0.0006")	
• 2 oz copper	±0.035 mm (0.0014")	
Copper foil thickness, 2-sided core	0.5/0.5 oz	2/2 oz with less than
	1/1 oz	0.15 mm conductor width
	2/2 oz	1/2 oz with less than
	1/2 oz	0.15 mm conductor width
Minimum pad size	Finished hole size +0.013"	Finished hole size +0.010"
Minimum plane clearance	Finished hole size +0.030"	Finished hole size +0.022"

A capability matrix may provide a quick way of determining whether a supplier should be considered further, but a supplier's advertising does not necessarily give a complete picture of how they will perform on a consistent basis. Wherever possible, sourcing teams should measure actual performance or audit processes to evaluate suppliers and substantiate marketing claims.

The following sections include recommended methods that can be used by sourcing teams to assess the capabilities of suppliers and ultimately select the ones that can best meet their requirements.

6.2.1 Technology

The simplest way to determine whether a supplier can provide a given set of technology requirements is by checking their advertised capabilities or sending a formal request for information (RFI) to the supplier. For a PCB the RFI should describe the dielectric material, surface finish, minimum conductor widths and spacings, minimum via diameter, essential tolerances, specific workmanship requirements or quality standards, and any other characteristics that are critical to the performance of the board. Similarly, for a PCA the RFI should specify single- or double-sided assembly, minimum component lead pitch, unusual components requiring manual placement, and lead-free requirements.

Note that for unusual, non-standard laminate materials and manufacturing processes it’s important to know how much experience the supplier has. If the supplier has limited or infrequent experience, there’s a greater risk of delay and quality issues. When the volume of work is low, a supplier will typically subcontract nonstandard technology to a nearby facility with specialized capabilities. In this case, the sourcing team should consider both *how long* the supplier has built production orders with the nonstandard technology, and *how often* they run these processes.

However, a match between the business’s technology requirements and a supplier’s advertised offerings does not guarantee a good long-term fit. This is especially true for requirements such as minimum conductor width that are dependent on a supplier’s ability to manage and control their

production processes. While it's standard for suppliers to perform 100 percent electrical test on all production units, a supplier with high first-pass yield will have lower costs due to less scrap and rework, and their boards will have higher reliability in the field.

Sourcing teams should consider whether to perform an objective, independent assessment of the supplier's ability to meet technology requirements over time, particularly for repeat orders of the same part number, or additional part numbers with similar requirements.

6.2.1.1 Two Common Techniques to Assess Suppliers' Technologies

1. Ask the supplier that's being considered to build a small quantity of boards using a new design. These "first articles" can be inspected, tested, and subjected to destructive analysis by the buyer's engineering team. Note, however, that it's very risky to add supplier evaluation to the development schedule for a new product.
2. Use a design that is already in production at a different supplier. This removes the schedule risk from new product development, and provides an opportunity to compare performance with a "known good" standard.

Unfortunately, both of these approaches have limited effectiveness because of the very small sample size. It's hard to draw general conclusions about long-term process capability from selective visual inspection or destructive analysis of a few boards.

The recommended alternative for evaluating PCB suppliers is the program described in the document IPC-9151D (May 2012) Process Capability and Relative Reliability ($PCQR^2$) Benchmark Test Standard and Database and at www.pcbquality.com. This methodology is based on test modules and procedures developed by Conductor Analysis

Technology, Inc. (CAT) and sponsored by the IPD-D-36 PCQR^2 Subcommittee. CAT has created 1- × 1-in test patterns that are arranged on a standard PCB panel (see Figs. 6.1 and 6.2) and are provided under license to IPC. These patterns include a range of conductor widths and spacings, via and pad diameters, soldermask clearances, and other design features.

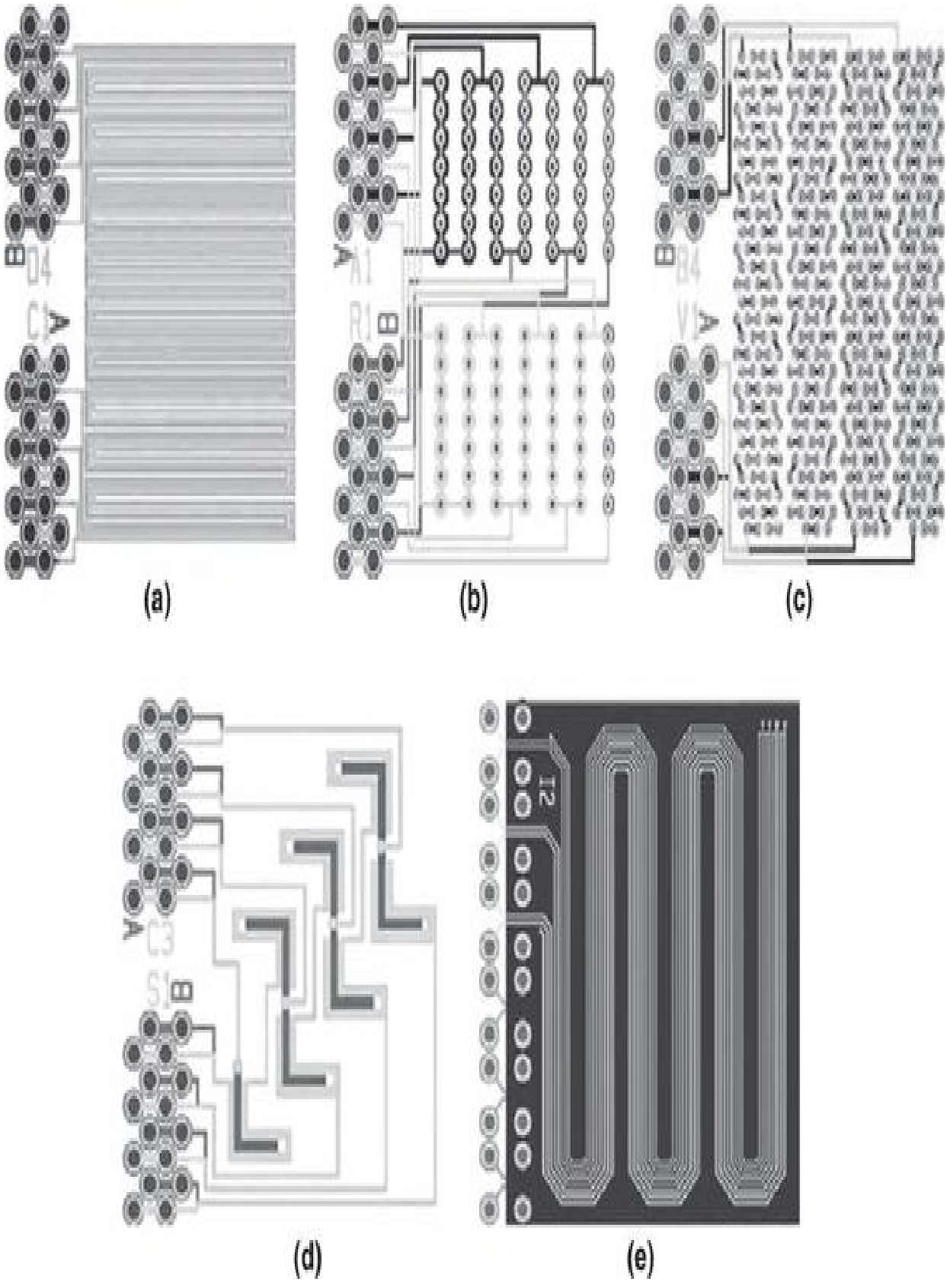

(a)
(b)
(c)
(d)
(e)

FIGURE 6.1 PCQR2 test patterns: (*a*) conductor/space module; (*b*) via registration module; (*c*) via formation and registration module; (*d*) soldermask registration module; (*e*) controlled impedance module. (*Courtesy of Conductor Analysis Technologies, Inc*.)

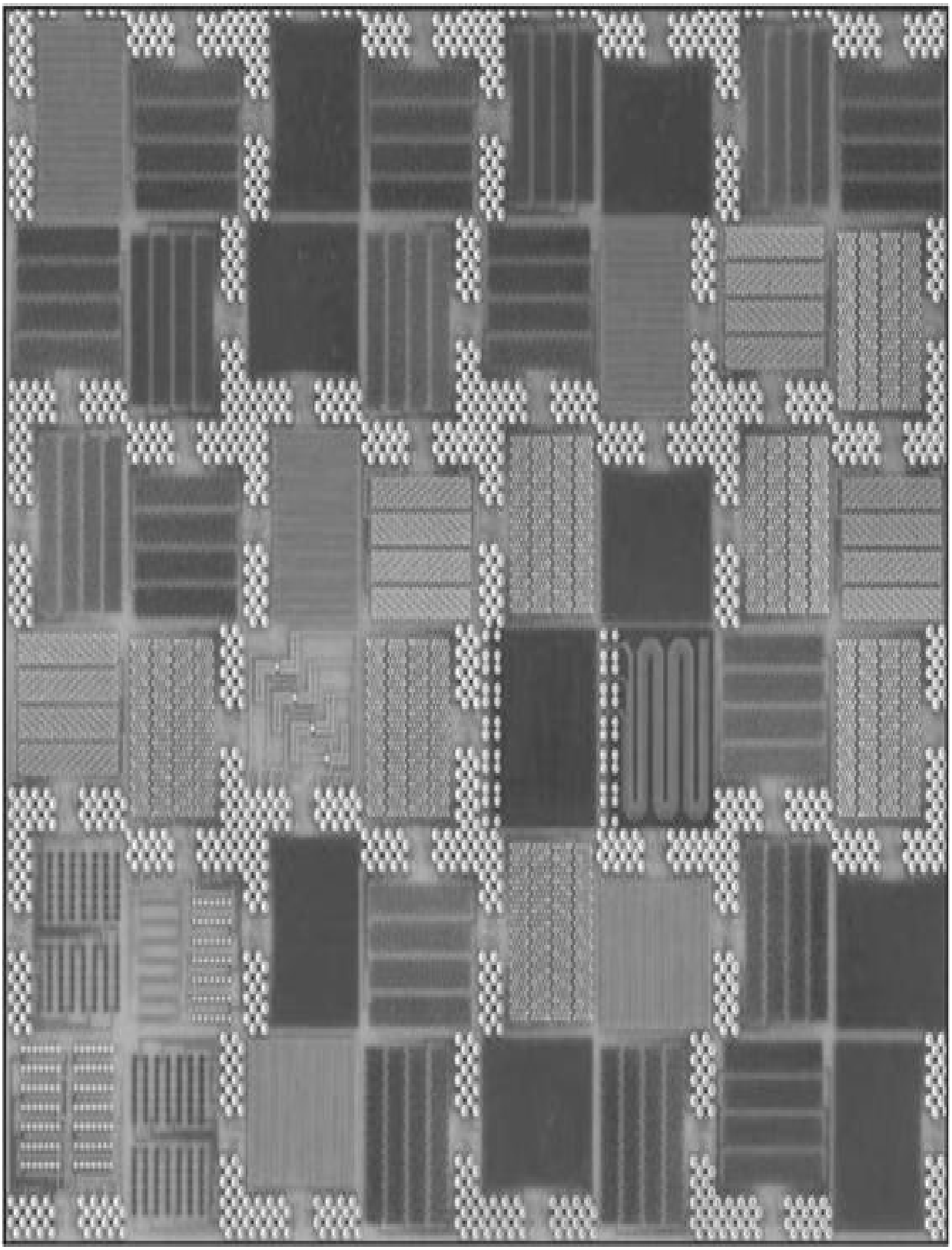


FIGURE 6.2 IPC-9151D PCQR2 benchmark design, full panel layout.

In this program, the supplier fabricates panels with the test patterns using artwork provided by CAT, and the panels are then submitted directly to CAT for testing using electrical measurements, optical analysis (including x-ray and cross-sections) and other techniques. CAT performs additional data analysis and adds the results to a shared database of supplier capabilities. The database, which includes the identity of the participating PCB suppliers, is available through an annual subscription from IPC.

The CAT analysis uses panel measurements to estimate defect density, predicted yields, and process capability. Figures 6.3 through 6.10 illustrate the range and detail of information that is available in the database.

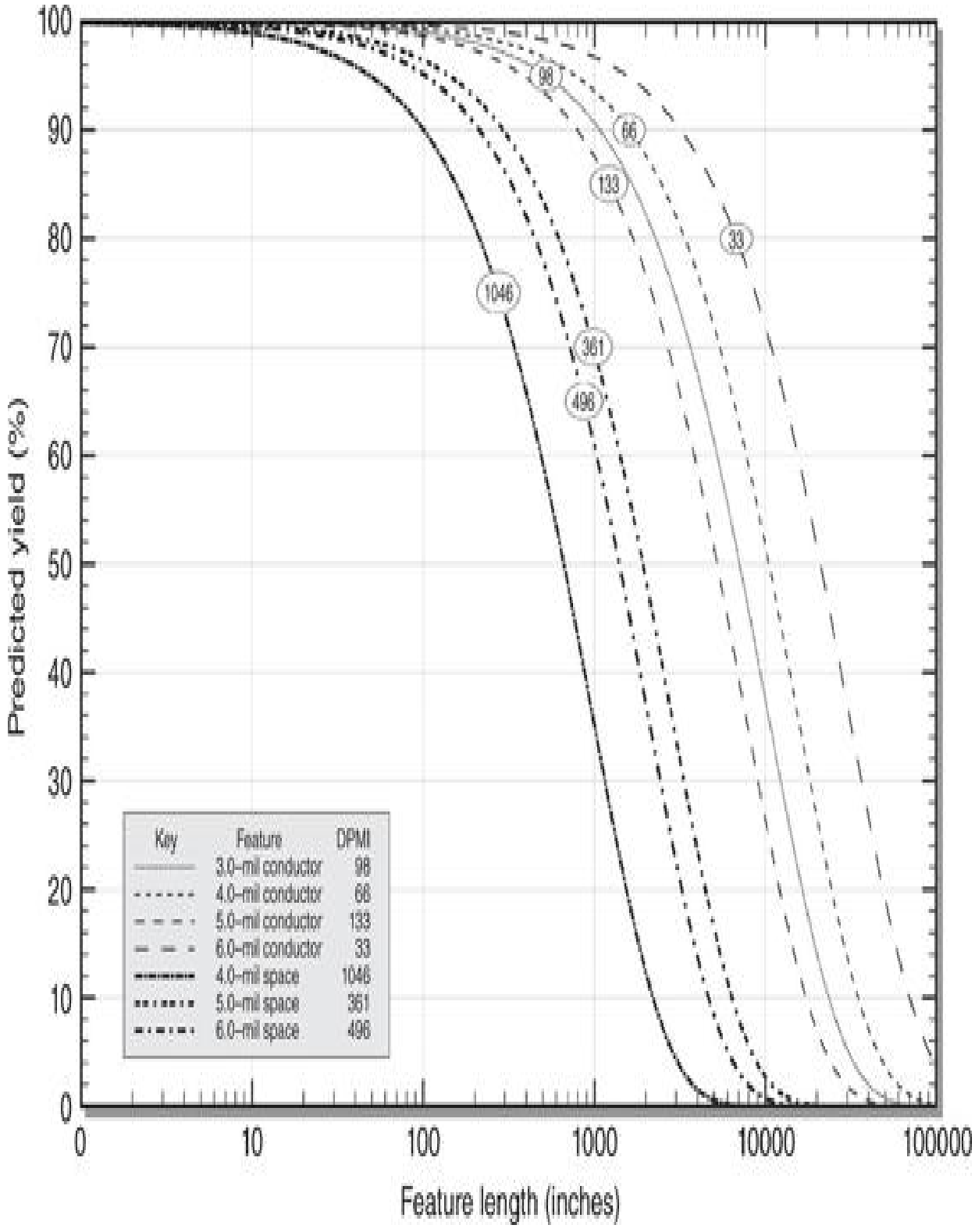


FIGURE 6.3 Predicted product yield versus conductor length.

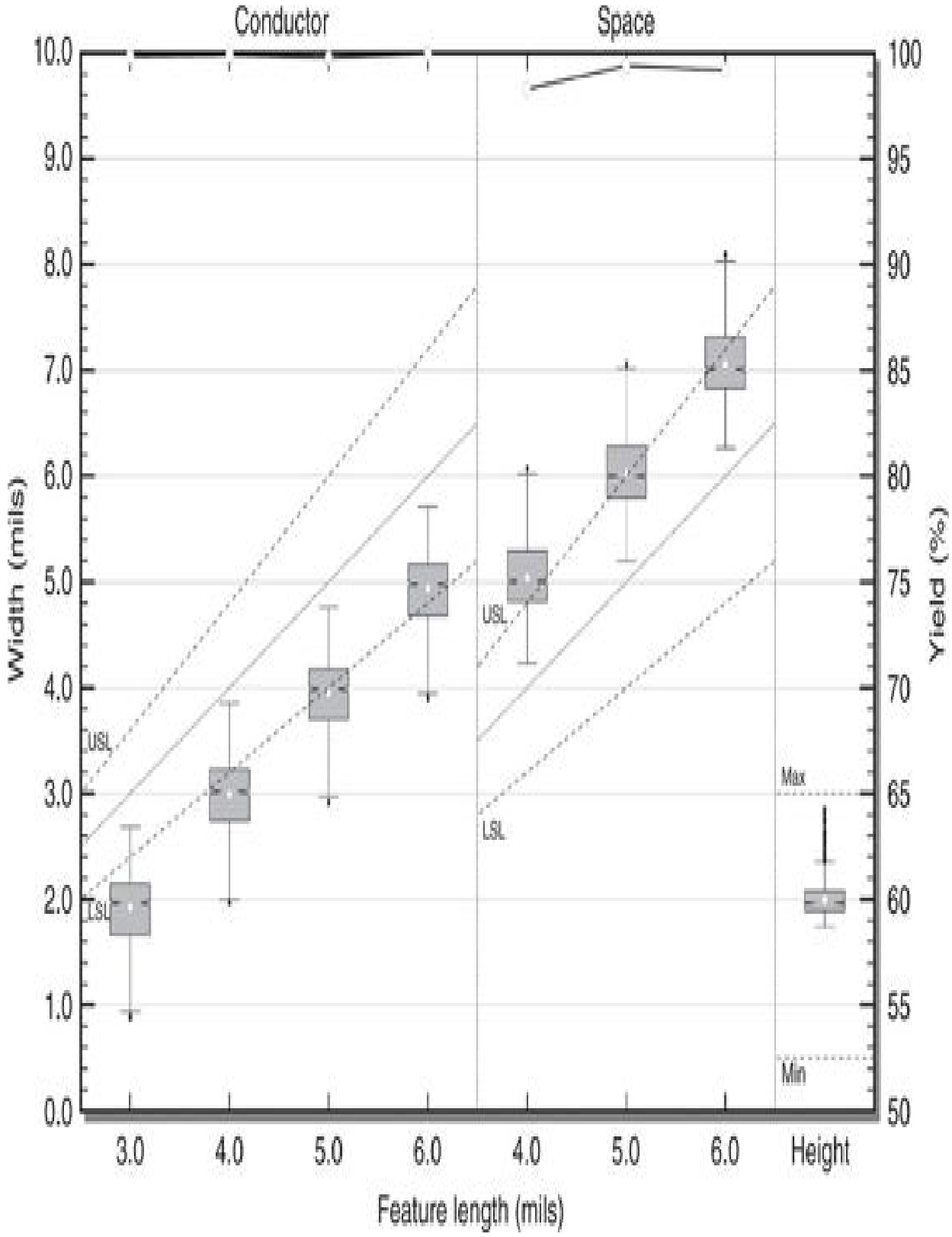


FIGURE 6.4 Measured conductor and space width versus target values.

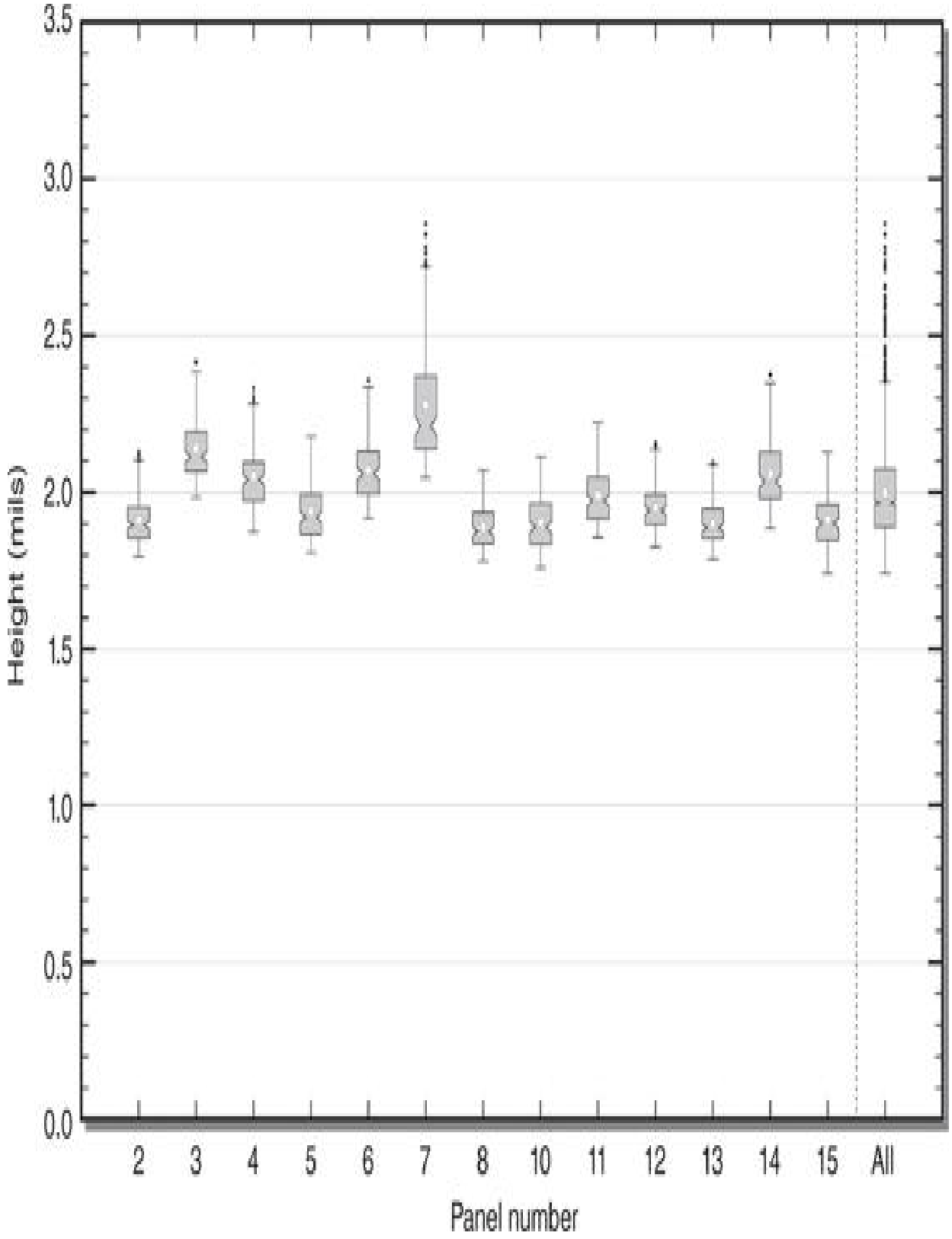


FIGURE 6.5 Conductor height versus panel number.

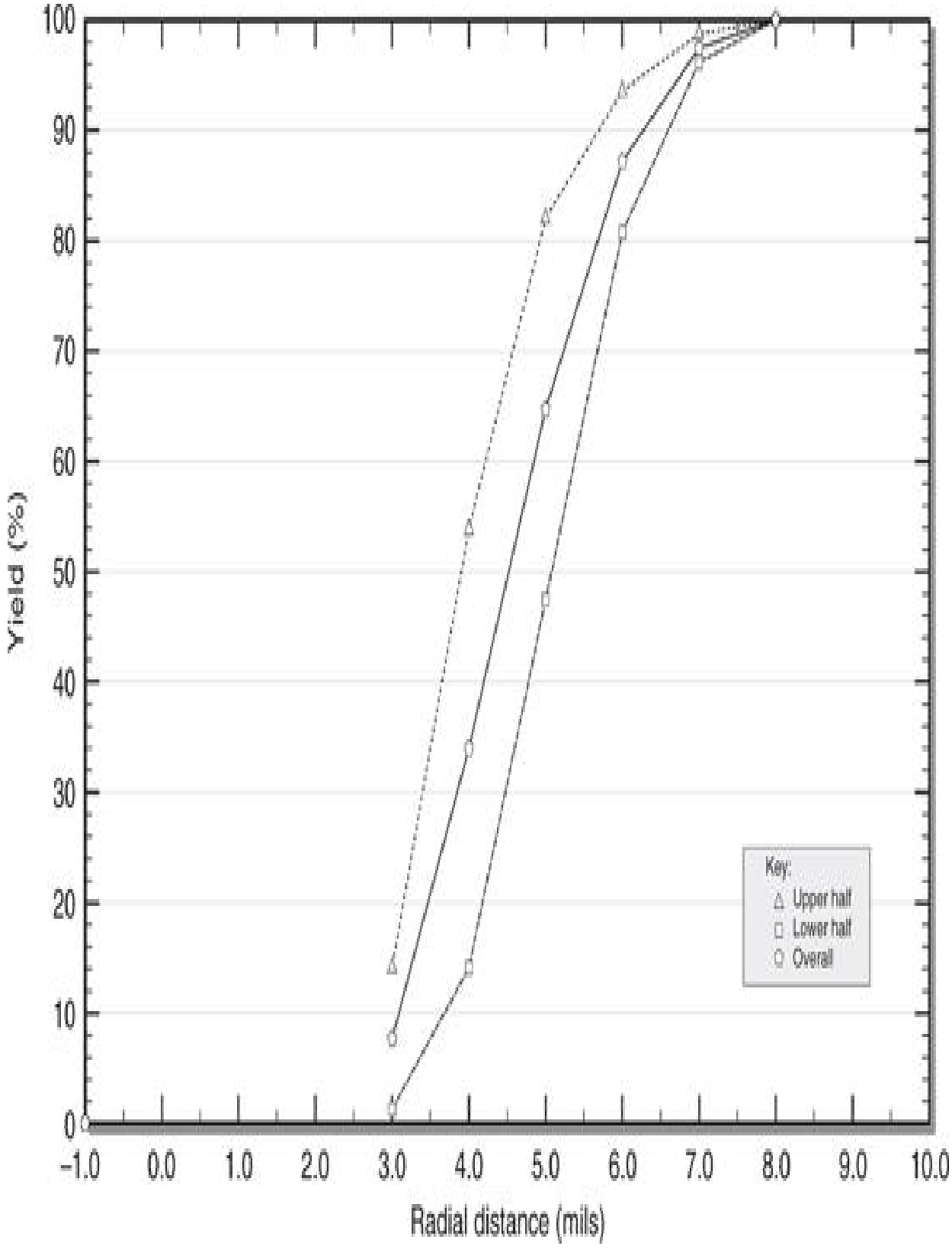


FIGURE 6.6 Via registration versus radial distance.

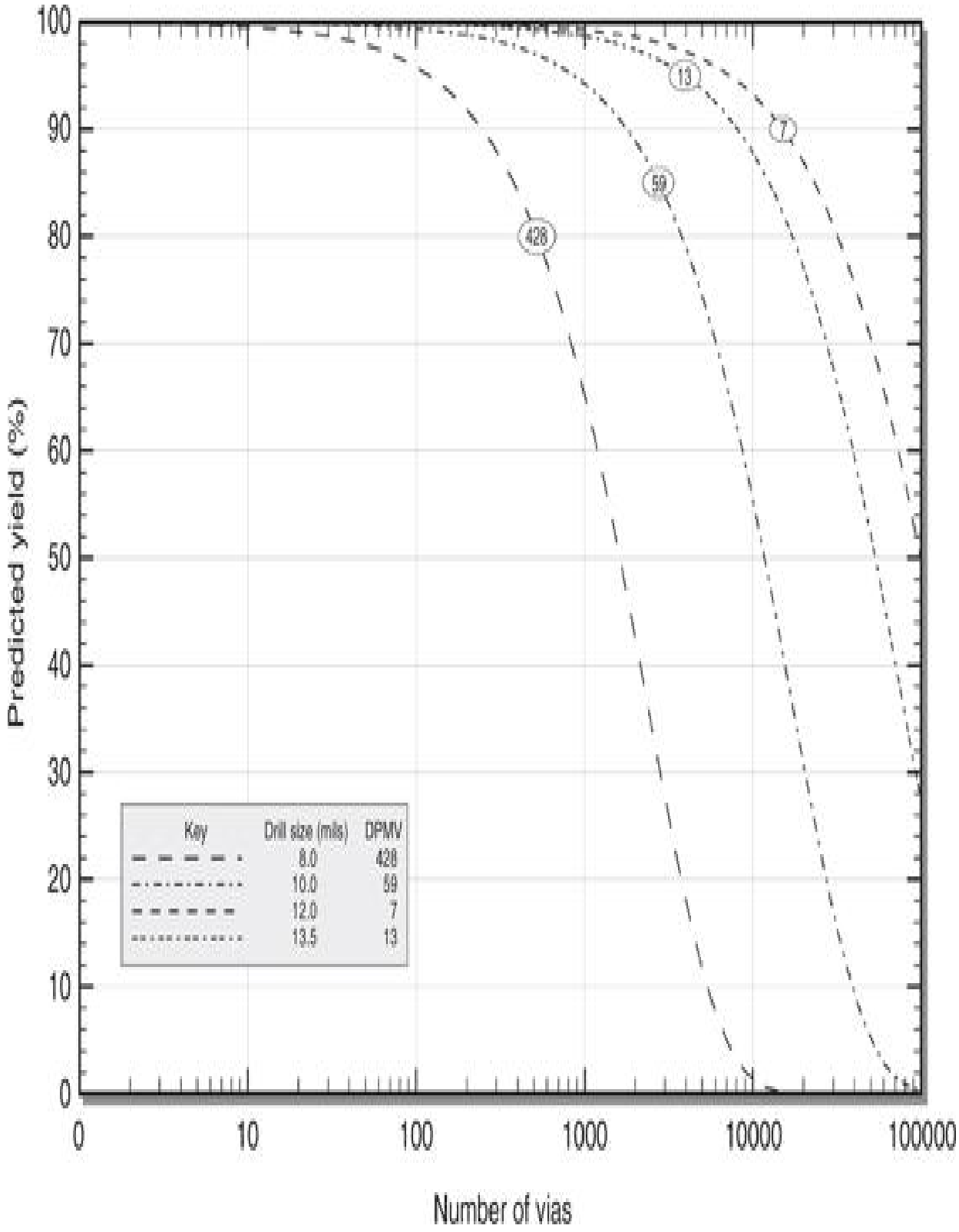


FIGURE 6.7 Conductor height versus panel number.

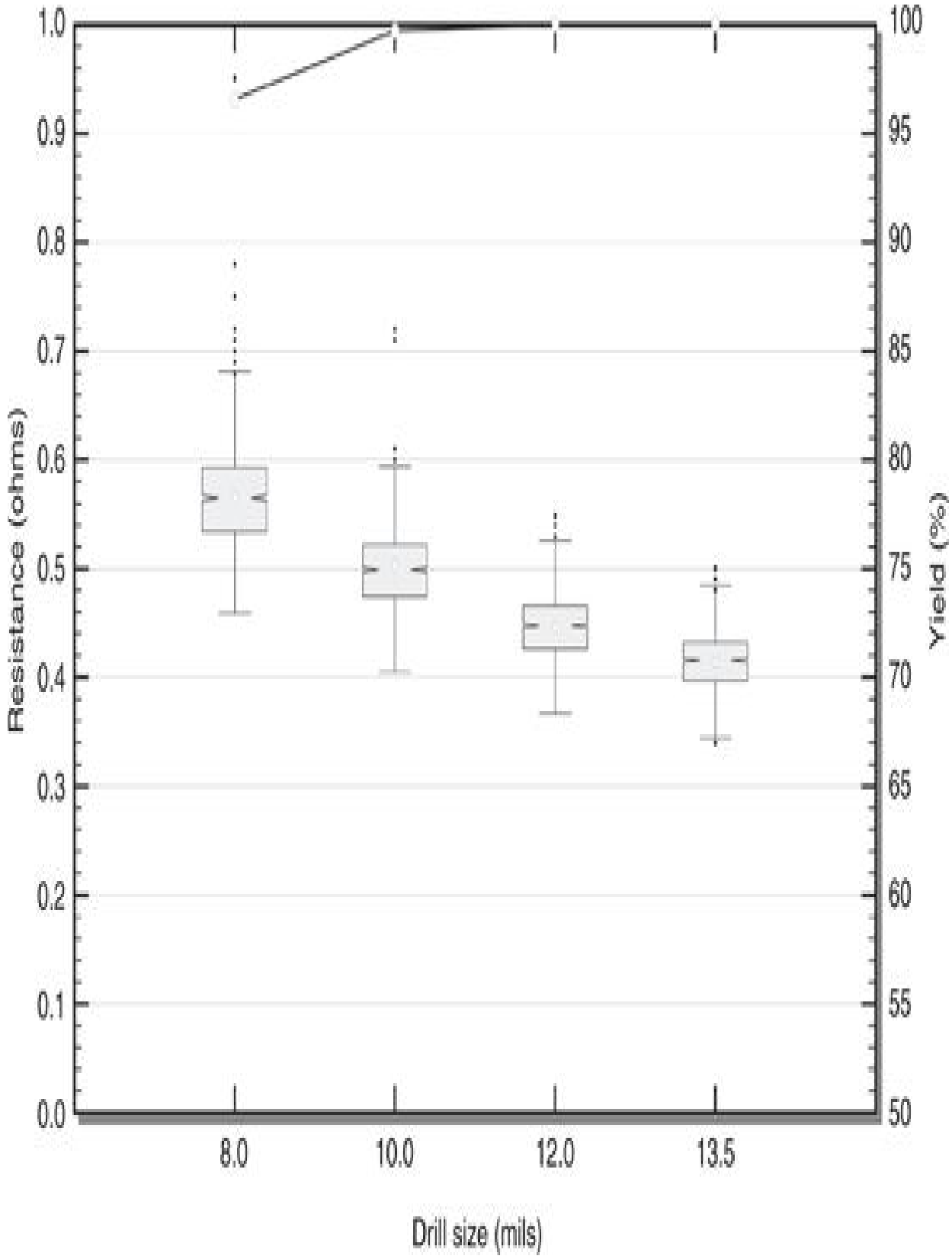


FIGURE 6.8 Conductor height versus panel number.

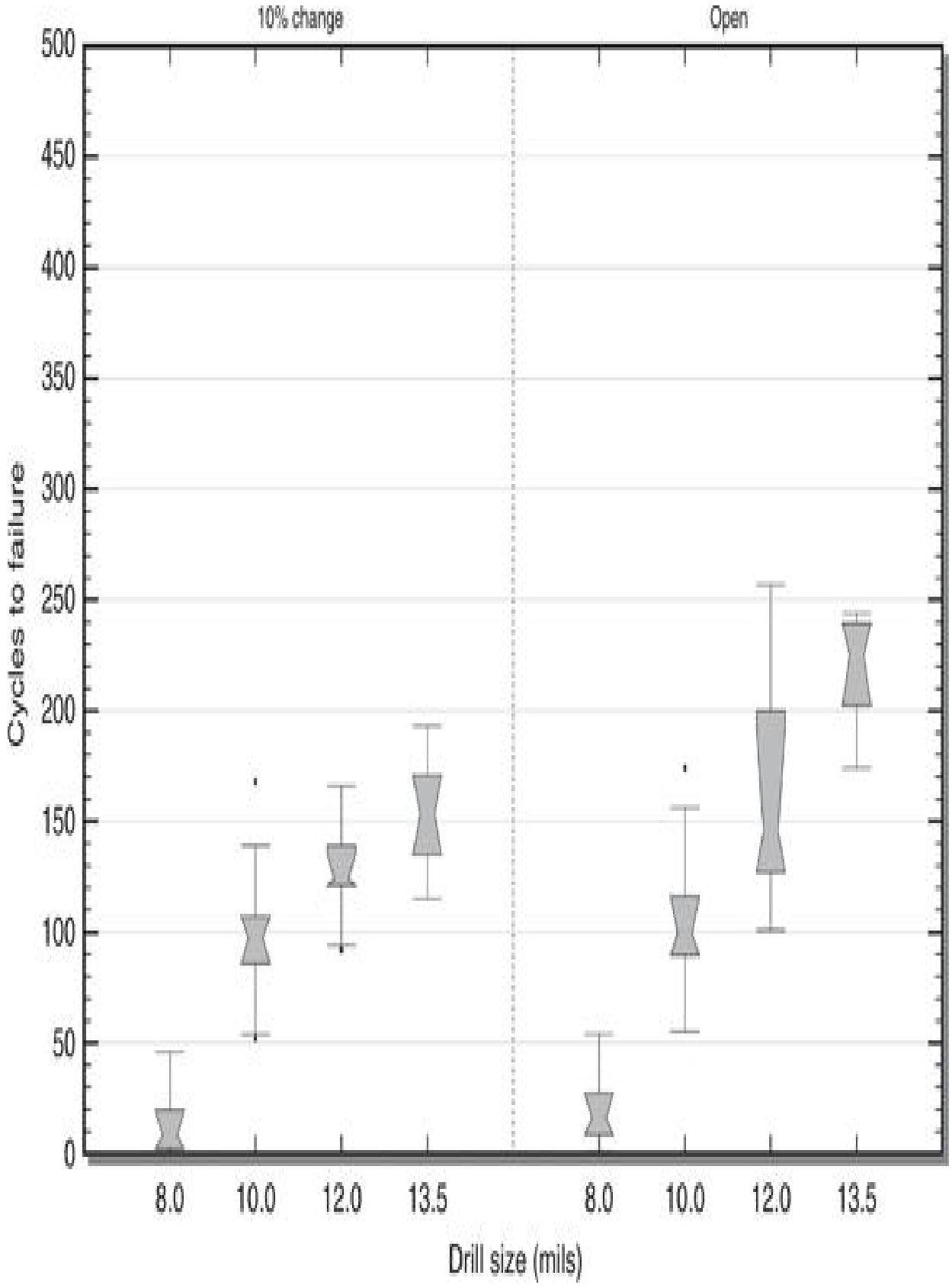

10% change
Open
500
450
400
350
300
250
200
150
100
50
0
Cycles to failure
8.0
10.0
12.0
13.5
8.0
10.0
12.0
13.5
Drill size (mils)

FIGURE 6.9 Conductor height versus panel number.

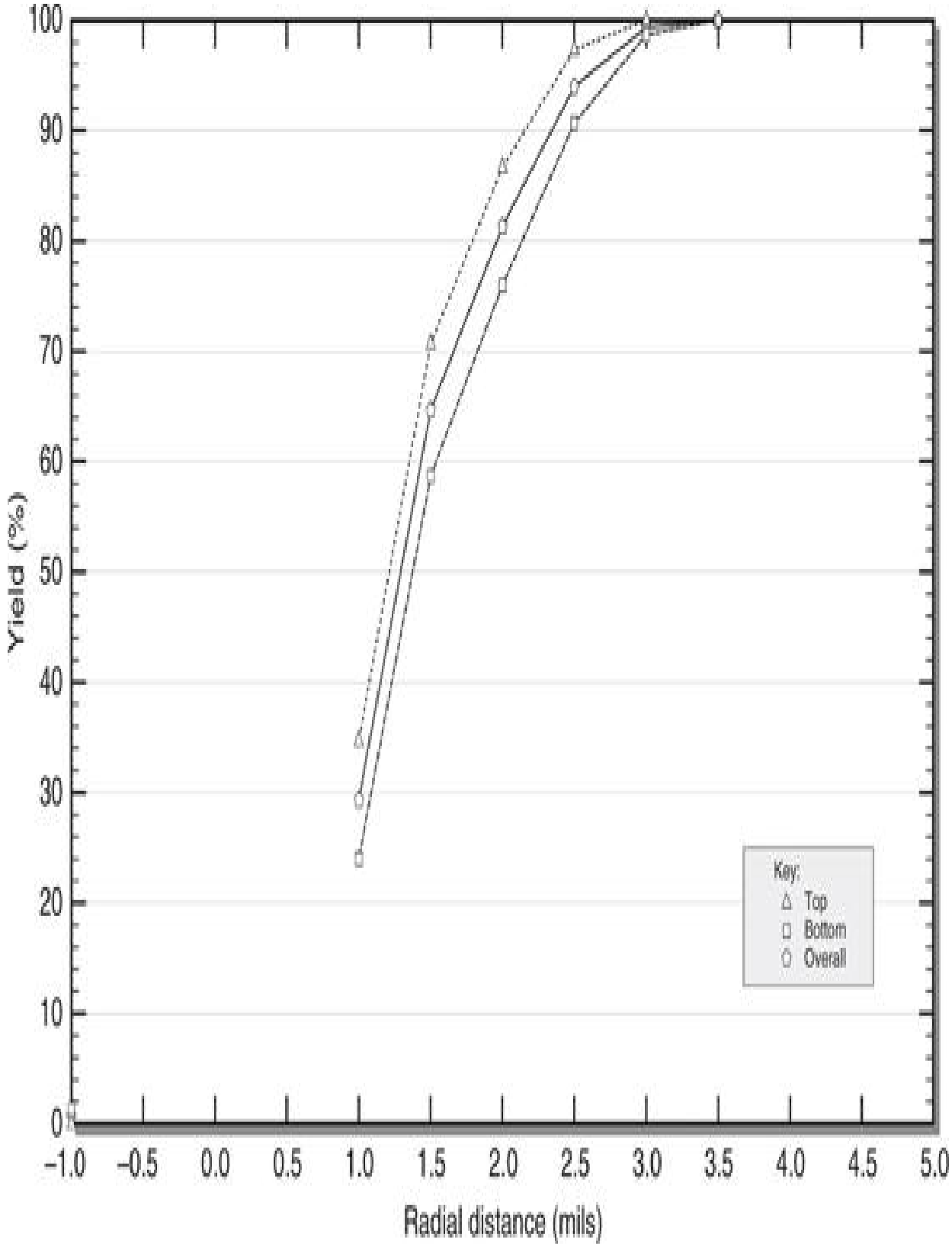


FIGURE 6.10 Conductor height versus panel number.

While it is possible for a company to create unique test patterns and conduct their own analysis, there’s tremendous value in participating in the IPC and CAT program. Database subscribers have the ability to review detailed results from individual suppliers and compare their capabilities across the industry. As of July 2014, a total of 72 PCB production facilities are included in the database, including suppliers in the US, China, Taiwan, South Korea, Canada, France, and Austria. Program subscribers include Dell, GE, Honeywell, Intel, Lockheed-Martin, Raytheon, and Sandia National Laboratories.

Because the test patterns are repeated over an entire panel, it is possible to collect a lot of data from a small number of panels (as few as 10) and produce statistically significant results. Subscribers can use the database not only to benchmark supplier capabilities, but also to establish design rules and guidelines for their board designers. The information provided by CAT can also be used to measure supplier performance improvement over time, and isolate specific production processes that need attention.

6.2.2 Responsiveness

It’s difficult to independently verify supplier claims about responsiveness characteristics such as percent on-time delivery and production order lead time. Generally speaking, however, the greater the geographic distance between the supplier and the customer, the greater the probability of transportation and logistics issues that will increase the variability of delivery time. Or, to put it a different way, delays are more likely when there are more hand-offs in the delivery chain, and these potential delays make it harder for anyone to accurately predict when a shipment will actually arrive.

Rather than simply accept the assurances provided by a supplier, sourcing teams can audit production and fulfillment processes to help determine whether the supplier can consistently meet the business's responsiveness requirements. Listed below are some questions that can be included in a supplier request for information (RFI) and verified during an on-site audit.

6.2.2.1 Responsiveness Questions for a Supplier

- Does the supplier have a dedicated outbound shipping department that handles bills of lading, customs, and other required documentation?
- Does the supplier have long-standing relationships with shipping and logistics service providers with experience delivering in your region?
- What contingency plans has the supplier used to help guarantee on-time delivery in case of shipment interruptions or delays?
- Does the supplier have a local or regional office that can monitor shipments from the factory and expedite as necessary? Can customers track shipments as well?
- What processes does the supplier use to facilitate fast turn production orders in the factory? How are expedited orders prioritized, tracked, and managed?
- How does the supplier manage design changes requested by the customer, including version control processes and disposition of work-in-progress?

The answers to these questions will lead to either greater confidence or greater concern regarding a supplier's responsiveness, and provide a basis to compare the likely performance of different suppliers.

6.2.3 Quality

Sourcing teams should only consider PCB and PCA suppliers whose quality management systems (QMS) have received an ISO 9001:2008 compliance certificate from an accredited external auditor. The certificate must be renewed at regular intervals, generally once every 3 years. The supplier should also be able to show evidence of recent internal audits of the quality management system. See Fig. 6.11.

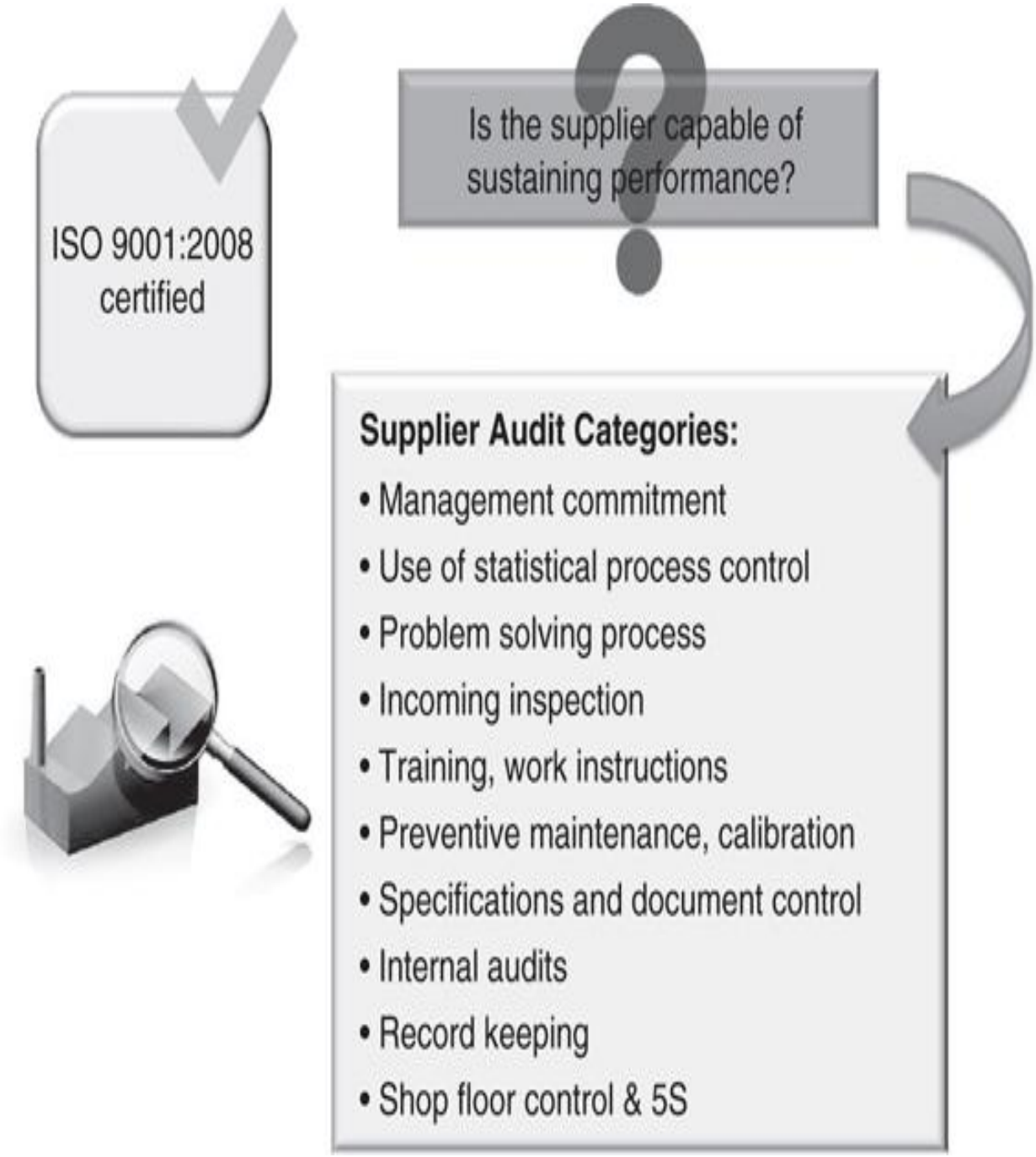


FIGURE 6.11 Supplier quality audit.

Potential customers can request a review of a supplier's QMS. It should include clear statements of commitment from the management team, and processes for traceability, communicating with customers, testing to confirm that a product meets customer requirements, control and

disposition of nonconforming product, and reviewing past results to support continuous improvement. The sourcing team should also inquire about the results and corrective actions from the most recent external audit, including nonconformities, observations, and opportunities for improvement.

The ISO 9001 certificate indicates that the supplier has a documented QMS that met the standard's requirements with no major nonconformities at the time of an external audit. However, because a company is unlikely to win business or contracts without the certificate, there is a risk that a supplier may be putting more emphasis on passing the audit than on sustaining quality performance over time. Also, the auditor only certifies that the processes in the QMS are being followed, but not whether following those processes actually ensures product quality.

While it is reassuring that PCB and PCA suppliers perform 100 percent electrical test on their finished products, and nothing should be shipped that does not pass, customers should nevertheless insist on sound operating processes that reduce the likelihood of nonconforming product. A higher first-pass yield means lower production costs for the supplier, which should in turn lead to lower price per unit. When the supplier's processes are capable and in-control, the PCBs and PCAs that do pass final test and inspection are better suited for downstream production and more reliable in the field. Chapter 7, "Process Control, Monitoring, and Incoming Inspection," provides recommendations for both customers and suppliers.

Sourcing teams should consider performing their own on-site audit to assess a supplier's internal processes and how they contribute to product quality (see Fig. 6.11). Some teams may prefer sending the supplier a request for information (RFI) with audit questions, but there is no substitute for a site visit and tour of the production facility, and the cost of the trip is a small price to pay for greater

confidence. Figure 6.12 is a sample agenda for a 2-day quality audit of a PCB supplier, and Table 6.3 shows some specific questions that might be asked during an inspection of the drilling operation.

FIGURE 6.12 Sample quality audit for PCB supplier.

TABLE 6.3 Sample Audit Questions: Drilling Process

- What is the inspection process for drill bits (incoming, repainted, and during use)?
- What is the frequency for repainting? When is the drill discarded?
- How is drill use and wear measured?
- What is the drill entry and back-up material?
- How are panels kept clean in the drill room?
- What are the temperature and humidity controls in the drill room?
- Are the drill machines isolated from vibration?
- Do the drill machines have isolated power and grounding?
- Is the actual rpm and feed rate independently determined?
- What is the inspection process for drilled holes? Test pattern? Cross-sections?
- How are accuracy and precision determined?
- Check the drill machine maintenance log
- X-ray verification after drill?

In addition to the audit, the sourcing team should ask the supplier to provide examples of their commitment to customer quality objectives. Figure 6.13 shows different levels of supplier quality maturity from the standpoint of the customer. A supplier who works on behalf of their customer is a valuable partner who helps reduce overall cost. This includes providing DFM feedback to the customer's design, proactively warning the customer of potential quality issues, preventive action to eliminate the root cause of problems, and a focus on process management and control instead of testing and inspection.

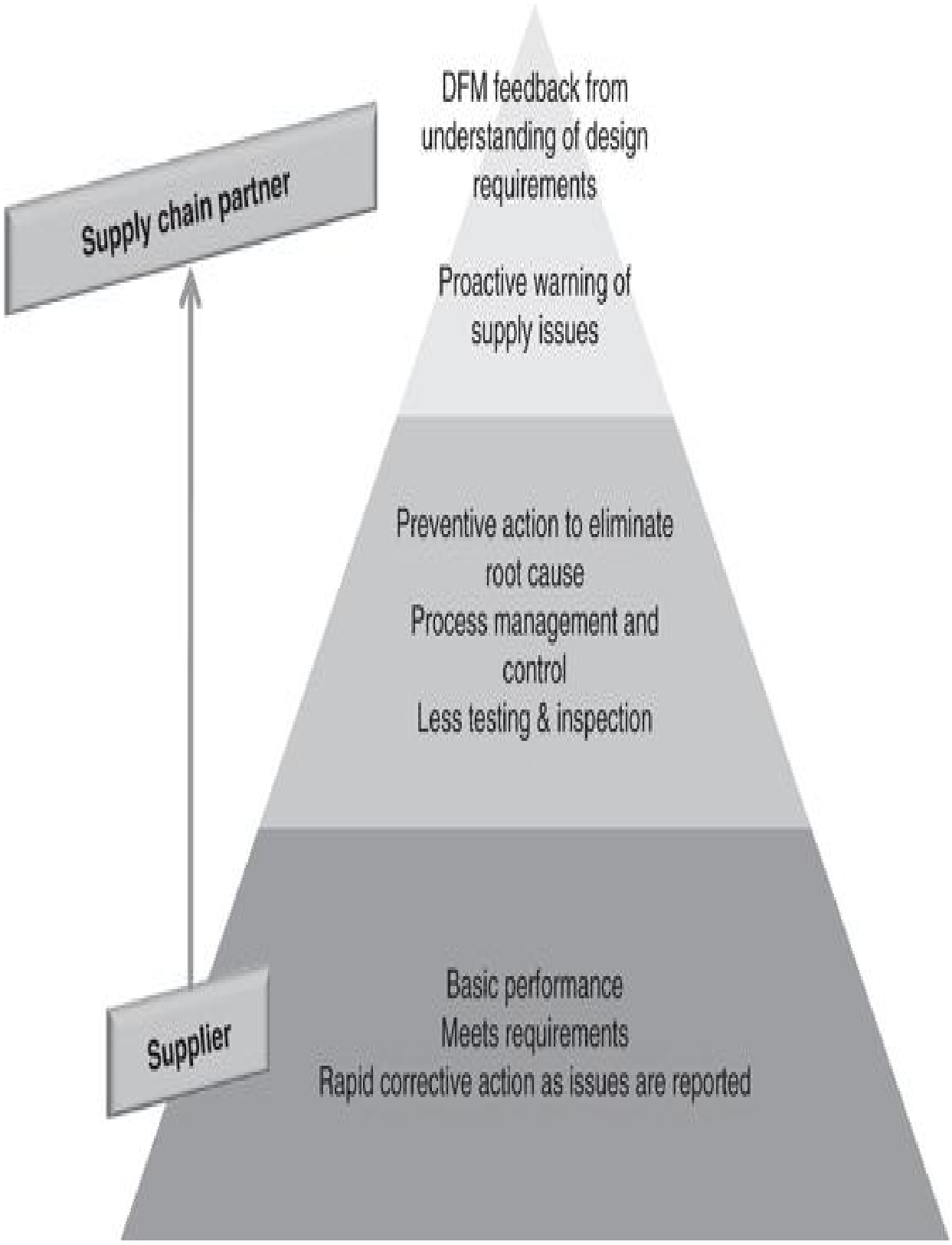


FIGURE 6.13 Supplier quality maturity model.

Depending on the final service environment for the finished PCA, the engineering design team may require that PCB and PCA suppliers routinely submit test results from coupons subjected to accelerated service life conditions and destructive analysis. Of course this can also be used to evaluate the processes of a new supplier. There are many coupon systems that can be used for reliability testing of PCBs. Most of these designs use daisy-chained vias since these sites usually provide the greatest risk of failure. The coupons can be arranged on test panels that are fabricated at the supplier and later subjected to conditioning and thermal stress before they are evaluated using destructive or nondestructive methods.

6.2.3.1 Typical Test Procedures for Coupons

- Normal and accelerated thermal cycling
- Thermal shock
- Surface insulation resistance
- Resistance at high humidity
- Solderability
- Peel strength
- Glass transition temperature
- High pot testing

Note that many suppliers can provide reliability test results from their own in-house testing or from independent laboratories.

6.2.4 Cost and Price

Unlike the other dimensions of supplier performance, PCB/PCA price is an objective and measurable characteristic that is relatively easy to obtain and easy to compare from one supplier to another. Sourcing teams can send a request-

for-quote document, or RFQ, that includes details about the board design, order quantity, standard or rush delivery options, quality expectations, documentation requirements, and any other information that the supplier may need to prepare an estimated price, or bid. If multiple suppliers are presented with an RFQ at the same time, their replies provide a useful basis for comparison.

Unfortunately there are caveats and limitations to RFQ responses:

- A price quote from a supplier is usually only valid for a specific period of time, typically 30 days or less. The actual board price when the production order is placed may be higher than the earlier RFQ response, and may in fact change from one order to the next over the life of the design, unless the supplier has agreed to a contracted price.
- While PCB/PCA price is based on the supplier's internal cost, it can vary depending on how badly the supplier wants the business. A supplier may quote more aggressively in order to help fill their factory and improve asset utilization, or attract a high-profile customer.
- The overwhelming majority of PCB and PCA suppliers use basically the same manufacturing processes for production orders, and it's unlikely that price differences between suppliers for the same design are due to some underlying breakthrough in process cost or yield, particularly for suppliers in the same labor market.

Note that although it's tempting to always choose the supplier that offers the lowest price, "leaving some money on the table" makes it much more likely that a supplier will be cooperative and responsive. PCB and PCA suppliers typically operate with very small profit margins and may not be very accommodating or flexible with a customer who has already won significant price concessions.

The sourcing strategy team should also consider the total cost of supplier management when comparing prices. A supplier who offers the lowest price per unit may require a disproportionate amount of attention from internal purchasing and engineering departments due to documentation errors, quality problems, or inconsistent delivery performance. This added cost-of-management is often overlooked and can be hard to measure, but it effectively increases the price per unit and is a very common reason for switching suppliers. While these costs are difficult to anticipate at the beginning of a new relationship with a supplier, they should be included in routine supplier performance reviews (see Chap. 8, “Product Acceptance and Feedback”).

6.3 SUPPLIER SELECTION

The results from the testing of sample boards, site audits, RFIs, and RFQs are all important inputs for comparing suppliers and determining how likely they are to perform consistently over time. Figure 6.14 shows a suggested sequence of steps for collecting and evaluating these inputs.

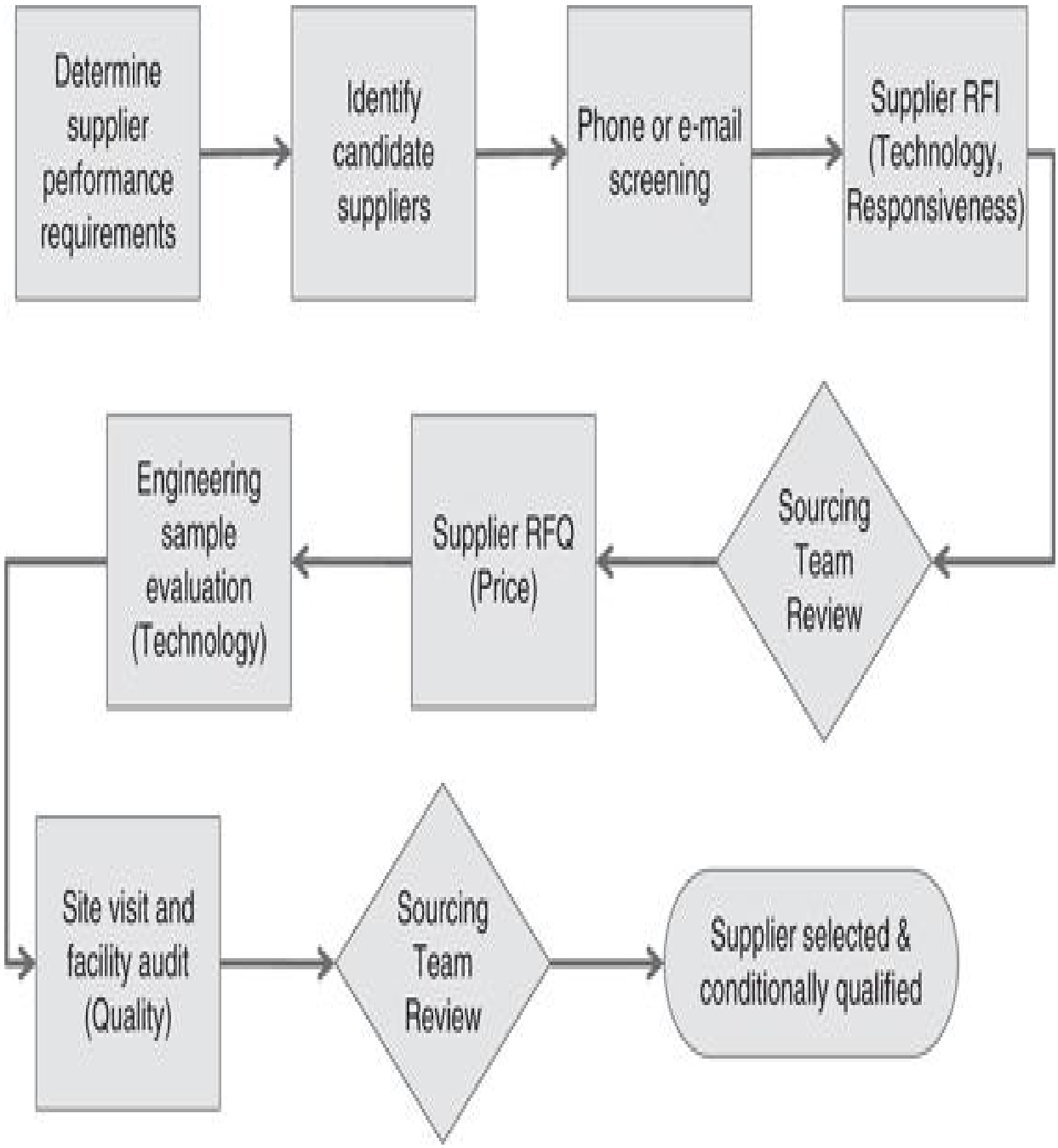


FIGURE 6.14 New supplier selection and qualification process.

It may seem that the best supplier is the one that provides the best overall combination of performance across all categories. However, the sourcing team should base their recommendation on the specific needs of the business that have been weighted to indicate relative importance. See Fig.

3.10 for an example. The more information that the sourcing team can obtain from stakeholders regarding what the business requires and the relative importance of each factor, the more likely that the best supplier will be chosen.

Some suppliers may be eliminated from further consideration because they cannot provide a “must” requirement. The remaining suppliers can be evaluated using a weighted criteria or similar decision-making process that applies factors to a qualitative ranking of each supplier’s assessment. Table 6.4 illustrates this technique.

TABLE 6.4 Supplier Selection Criteria Weighting Example

Selection Criteria	Must Requirement?	Relative Weight	Supplier A Rating	Supplier A Weighted	Supplier B Rating	Supplier B Weighted
Technology						
• Standard FR-4 laminate	Yes		Yes		Yes	
• Minimum conductors 4 mils	No	2	3	6	5	10
• Minimum via diameter 12 mils	No	4	3	12	5	20
• Pb-free surface finish	Yes		Yes		Yes	
Responsiveness						
• 6 week lead time for production	No	3	4	12	3	9
• 0 days late, no more than 3 days early	Yes		Yes		Yes	
Quality						
• 100% opens/shorts testing	Yes		Yes		Yes	
• Defective boards returned to supplier	Yes		Yes		Yes	
Cast and Price						
• No more than $X per square inch	No	5	2	10	1	5
Other Services						
• Prototypes within one week	No	2	2	4	4	8
• Local sales and technical support	No	4	5	20	4	16
TOTAL WEIGHTED SCORE				64		68

6.3.1 Techniques for Evaluating Suppliers

- In this case both Supplier A and Supplier B meet all of the "must" requirements and will be evaluated further.

- The sourcing team has used information gathered from their technical evaluations, RFIs, RFQs and on-site audits to give the two suppliers a qualitative rating for each of the remaining selection criteria.
- The weighted score for each supplier is obtained by multiplying the qualitative rating by the relative weight previously determined (based on the importance to the business).
- The total weighted score is the sum of the individual weighted scores for each selection criteria. Supplier B has a slightly higher score because it provides a better fit to the business requirements.

6.4 SUPPLIER QUALIFICATION

A supplier who has been selected for a specific purchase order is typically placed on a company's approved vendor list (AVL). Because the sourcing team has already evaluated the suppliers on the AVL, they are generally preferred for future business. Companies often have policies that restrict the use of non-AVL suppliers without explicit management approval. AVL suppliers are easier to do business with because they are already familiar with the customer's requirements and documentation. This means they are less likely to have quality issues because of errors or misunderstandings. Since they have more experience with the customer's designs, AVL suppliers are also better able to offer DFM feedback that will reduce cost and increase first-pass yield.

6.4.1 Additional Considerations

- Supplier selection is usually determined by the capabilities and performance of a factory at a single

location. If the supplier proposes to transfer production to a different location with different physical processes, operators, and management team, the sourcing team should reevaluate.

- The steps described in this chapter can be used by the sourcing team to choose suppliers that are likely to perform well and meet the needs of the business. However, additional steps should be taken to qualify and approve production of a **specific part number** by an approved supplier. Chapter 8 provides guidelines for design qualification, lot acceptance and ongoing inspection.

In addition to the AVL, some companies have a more formal qualification program that provides additional benefits for preferred suppliers. Because of their consistently high performance, these suppliers are identified as strategic partners who have an important role to play in the overall value delivery system.

A preferred supplier may receive better pricing and payment terms, participate in long-range capacity planning, and collaborate with the customer's design and engineering teams. Other benefits for a preferred supplier include an advertised relationship with a well-known customer (especially valuable for smaller suppliers), and predictable and consistent demand for better asset utilization. For the customer, a preferred supplier can help reduce inventory and testing costs, and enable faster time-to-market by rapid qualification of new part numbers.

Finally, it should be remembered that supplier capabilities and performance can change over time, as can the technology and business needs of the customer. Sourcing teams should routinely audit and assess qualified suppliers to ensure that they are still able to meet the technology, responsiveness, quality and cost requirements. Suppliers should also be given regular feedback on their performance,

and encouraged to address areas of concern and proactively implement improvements. Chapter 8 includes recommendations for long-term supplier management.

CHAPTER 7

PROCESS CONTROL, MONITORING, AND INCOMING INSPECTION

Tim Rodgers
University of Colorado, Boulder, Colorado

7.1 INTRODUCTION

Chapter 6, “Supplier Selection and Qualification,” provided detailed recommendations for a printed circuit board (PCB) or printed circuit assembly (PCA) sourcing team to evaluate alternate suppliers and choose those that best meet their business needs. If the supplier is only required for a single purchase order or transaction, then the team can immediately shift their focus to design qualification and lot acceptance, which is described in Chap. 8, “Product Acceptance and Feedback.”

However, if the relationship with the supplier is expected to continue over an extended period of time that includes multiple purchase orders and part numbers, the sourcing team should understand whether the supplier has the

production processes and management systems to *sustain* the required performance with a minimum of oversight. This chapter includes information that can help a sourcing team assess a supplier's processes and determine the likelihood of consistently receiving PCBs or PCAs that conform to the design requirements.

There may be several testing or inspection steps in the overall supply chain for a product that contains electronic assemblies (see Fig. 7.1). PCBs are typically visually inspected before they are loaded with components, and the PCAs may be inspected again before being assembled into the final product. Functional testing of the final product before shipping often detects defective PCAs. Some production designs may include accelerated reliability testing for a sample of the finished products. However, it's important to find defective or nonconforming parts as early as possible, and ideally prevent them from being produced in the first place.

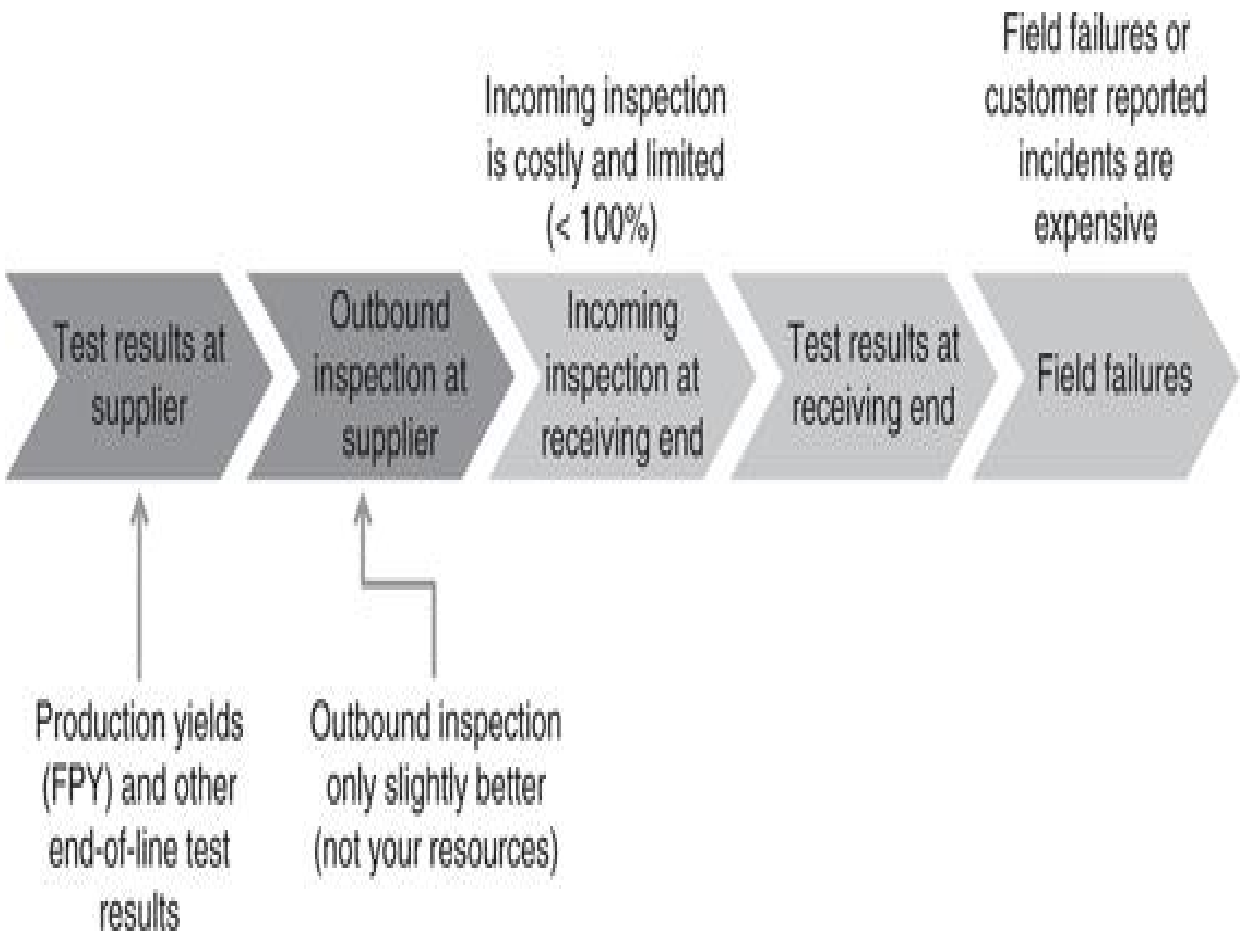


FIGURE 7.1 Quality checks at supplier and receiving end.

Figure 7.2 illustrates the relative cost of finding defects through the PCA supply chain. When defective PCAs are found during final assembly, the engineering, manufacturing, and quality teams must consider whether to scrap or rework by replacing components, which adds significant cost and possibly delays production. Defective PCBs that are found before component loading are somewhat less costly, but manual rework by cutting traces or adding jumpers adds a reliability risk, and scrap PCBs have become a major worldwide environmental concern.

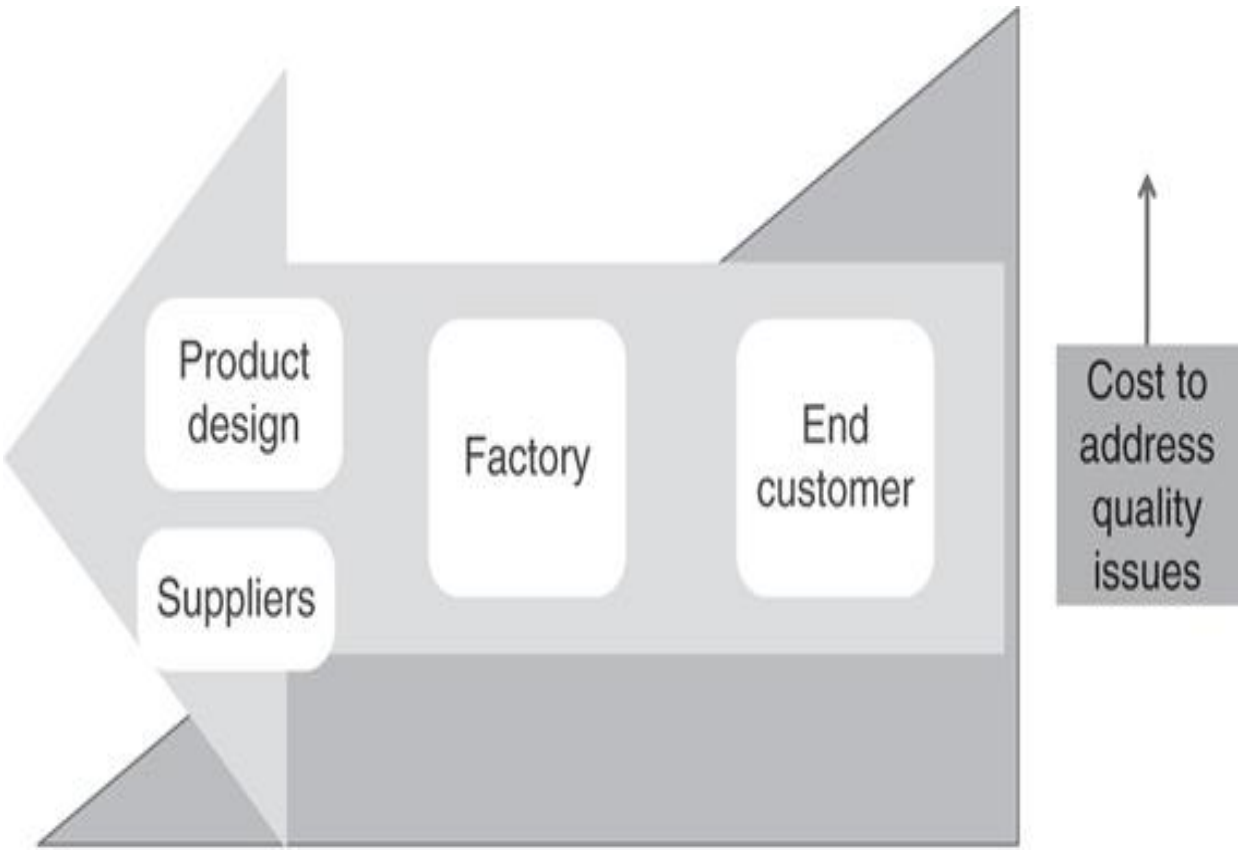


FIGURE 7.2 Improving quality at the supplier.

Because of these added expenses, and the risks to production schedules, long-term reliability, and environmental stewardship, businesses should insist that their suppliers do everything possible to prevent shipping nonconforming parts. Sourcing teams should routinely monitor their suppliers' ability to manage and control their production processes.

7.2 PROCESS CAPABILITY AND PROCESS CONTROL

A supplier will routinely subject 100 percent of their PCBs or PCAs to continuity testing ("opens and shorts"), and PCAs may also have to pass functional testing before shipment.

Any PCB or PCA that fails this testing may be scrapped or reworked, depending on the authorization given by the customer. Suppliers typically report first-pass yield (FPY) before rework as an indicator of the overall performance of their production processes.

A supplier with a low FPY can correctly claim that all of their shipped boards pass testing; however, this is an indicator that the supplier's processes are fundamentally less able to deliver conforming product. This requires the supplier to start more panels in order to complete their order, and figure out what to do with the boards that failed, both increasing their costs. Low FPY also suggests the possibility of lower long-term reliability for boards that pass continuity testing before leaving the factory, but are susceptible to failure after field use or environmental exposure, especially for narrow conductor widths and spacings.

In addition to passing continuity testing or functional testing, there may be other characteristics of the PCB or PCA that are critical to the performance of the final product.

7.2.1 Characteristic Performance for the Product

- Board width and length
- Pad height
- Plating thickness
- Through hole diameter and location relative to a datum
- Fiducial location relative a datum
- Trace impedance

The sourcing team should consult with electrical engineers, PCB/PCA designers, and downstream production engineers to identify the critical performance parameters (CPPs) for the

finished board or assembly. Often critical-to-function or critical-to-assembly dimensional requirements and tolerances are explicitly called out on CAD drawings that accompany the design. The performance of a supplier is determined by how well they can consistently deliver boards or assemblies that not only pass continuity or functional testing, but also meet the CPP requirements.

To understand the role that suppliers play in meeting the CPP requirements, it's necessary to review some of the basic concepts behind statistical process control, process capability, and the six sigma methodology for process improvement.

If a physical process is repeated many times and the output of the process is measured, the results are often found to follow a normal distribution, commonly referred to as a bell curve (see Fig. 7.3). This distribution of the process outputs can be described by the mean, or average of the measured values, and the standard deviation, which characterizes the variability of the distribution. The mean and standard deviation are usually taken to be fundamental characteristics of the process, also known as statistics of the *population* of an infinite number of outputs. The mean and standard deviation of a subset of measured outputs are statistics of a *sample* from that population, and are used to approximate the population statistics. The more samples are taken, the better the approximation.

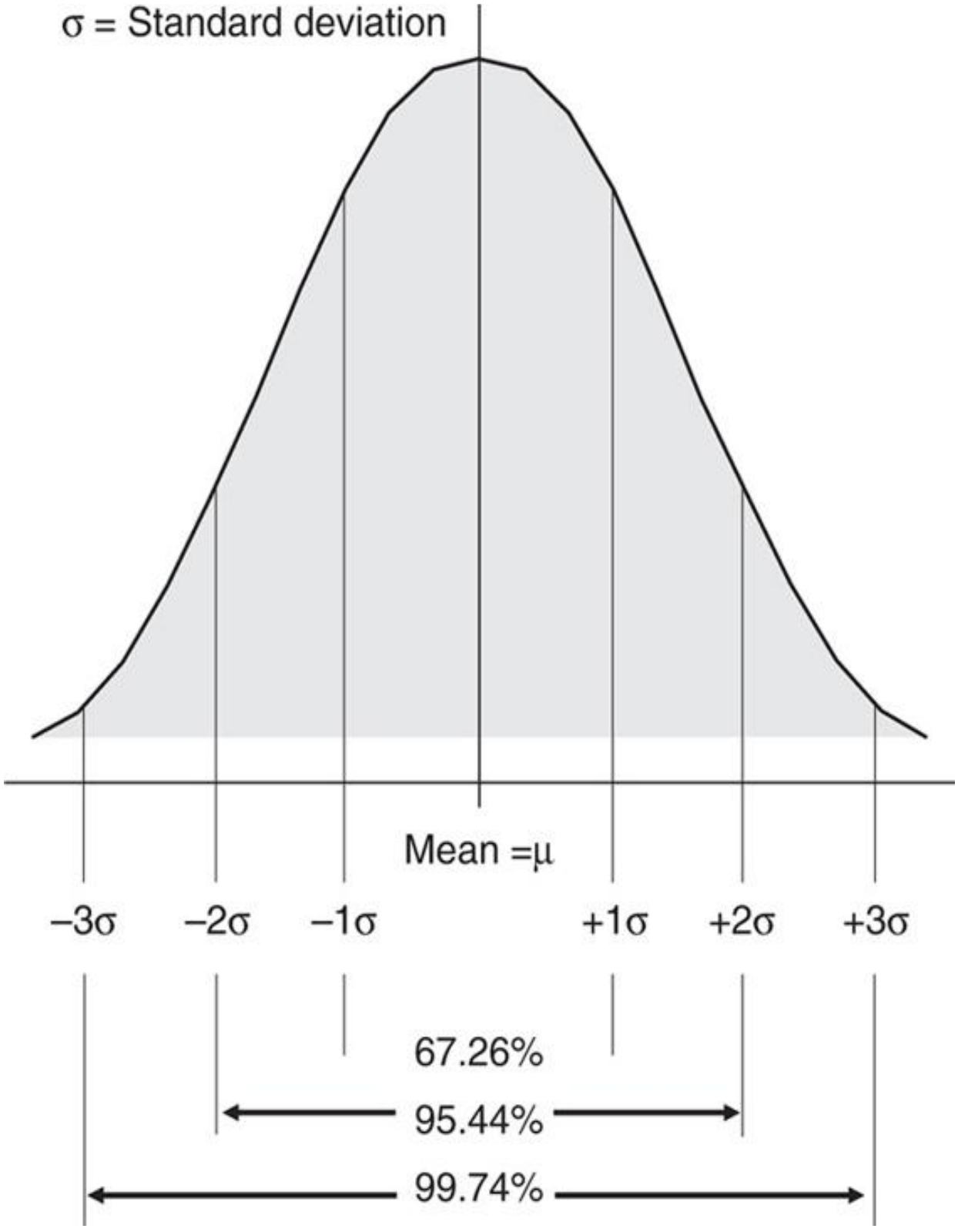


FIGURE 7.3 Normal distribution.

The distribution is valuable because it shows the probability of a particular output occurring. For example, there's a 67.26 percent probability that the output will occur within 1 standard deviation above and below the mean, and a 99.74 percent probability that the output will occur within 3 standard deviations from the mean.

The normal distribution model assumes that the output is determined only by the inherent randomness of the process itself, which is referred to as the *common causes* of variability. *Special causes* are events that are external to the usual, expected functioning of the process. When special causes are present, the process output may not follow any expected pattern or distribution and are unpredictable. A process that is governed only by common causes is said to be "in control" and provides outputs that can be predicted using the process mean and standard deviation. A process with special causes is "out of control."

Some suppliers may use a monitoring tool called a *control chart* to determine whether a process is in control (see Fig. 7.4). A control chart plots the average of a sample of measured outputs collected over a period of time. If only common causes are present, these data points will be randomly distributed on either side of the process mean. A data point that falls outside the control limits is considered to be an unexpected and very low-probability event for a process that is governed only by common causes. This indicates the presence of special causes that must be identified and eliminated in order to bring the process under control. Note that there are other low-probability events and patterns in the control chart that indicate special causes. Figure 7.5 shows several examples of special causes that may be present in a typical factory environment.

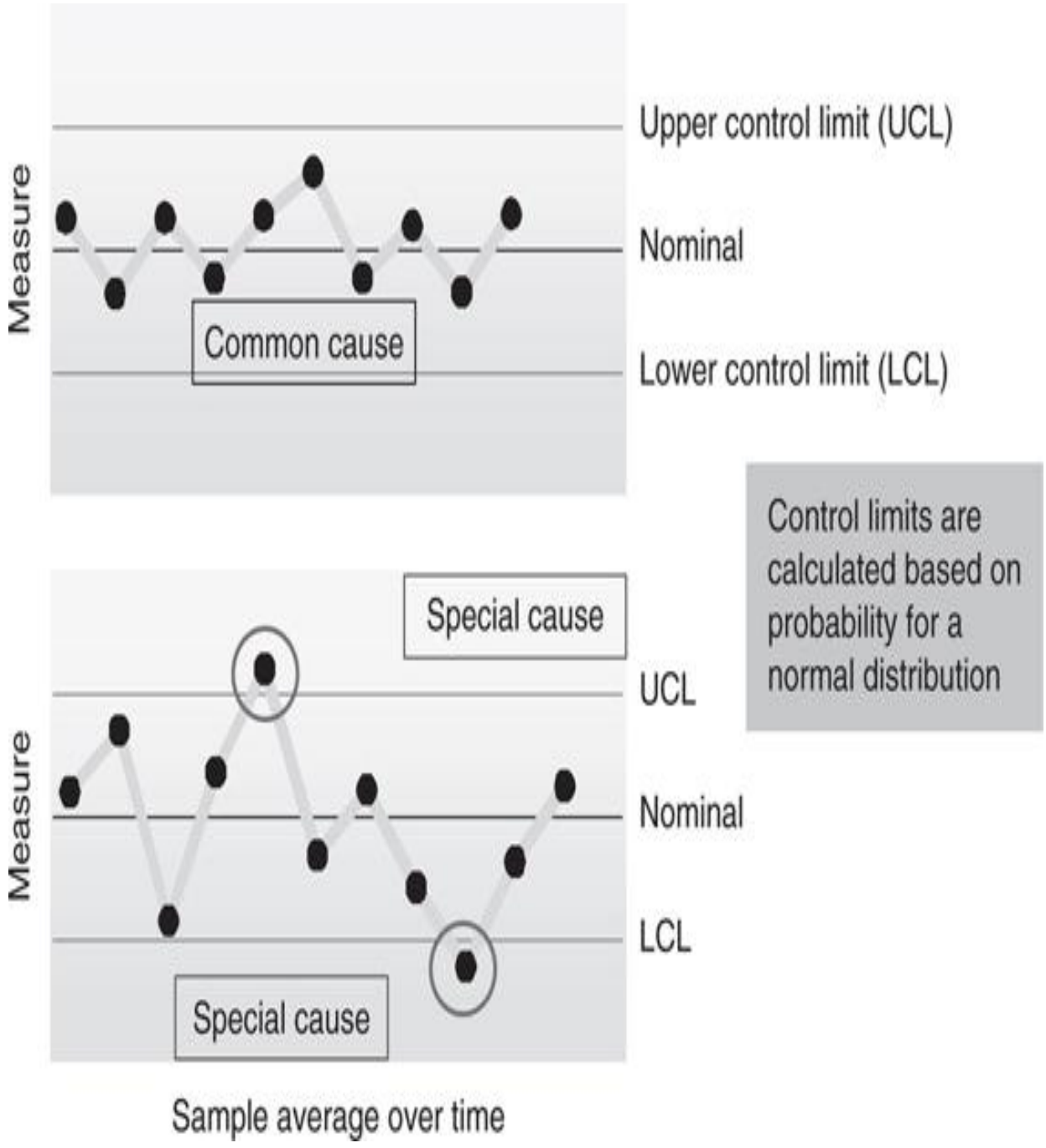


FIGURE 7.4 Process control chart example.

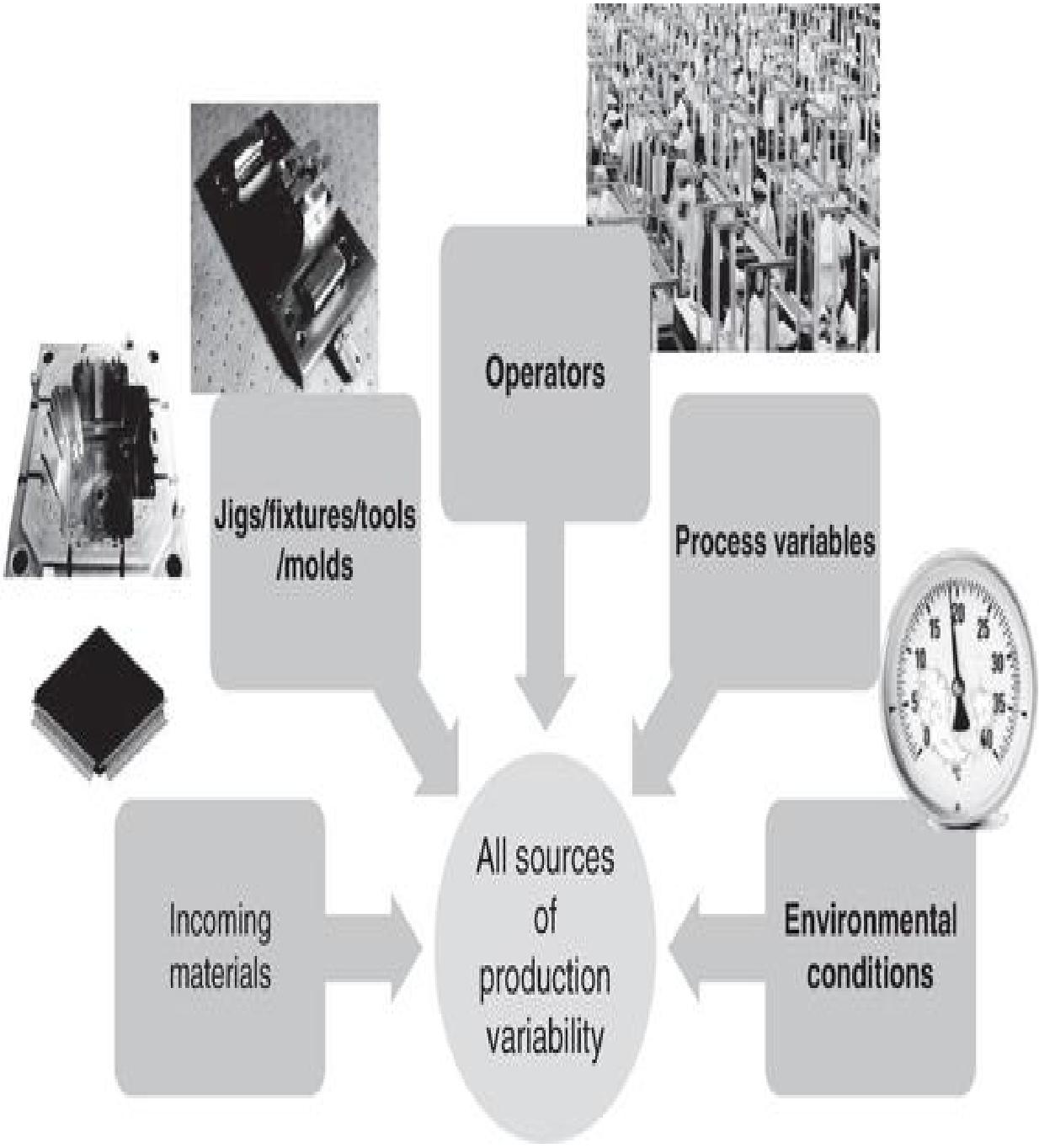


FIGURE 7.5 Special causes in a factory environment.

Obviously both the customer and the supplier benefit from manufacturing processes that are in control and provide predictable outputs. However, a process that is in control does not necessarily produce outputs that meet the customer's requirements. Suppliers often use *process*

capability studies to determine the probability of producing nonconforming parts. These studies use a sample of process outputs to create an estimated distribution, then compares that distribution to the specification limits defined by the customer (see Fig. 7.6). The most common process capability metric is C_{pk}. If the C_{pk} is 1.0 or greater, this means that there is a 99.73 percent probability that a process output will be within the defined specification limits. Or, to say it a different way, there is a 0.27 percent chance that the output will be outside the specification limits. Note that a six sigma process has a C_{pk} of 2.0 or greater, which corresponds to only two nonconforming parts per billion.

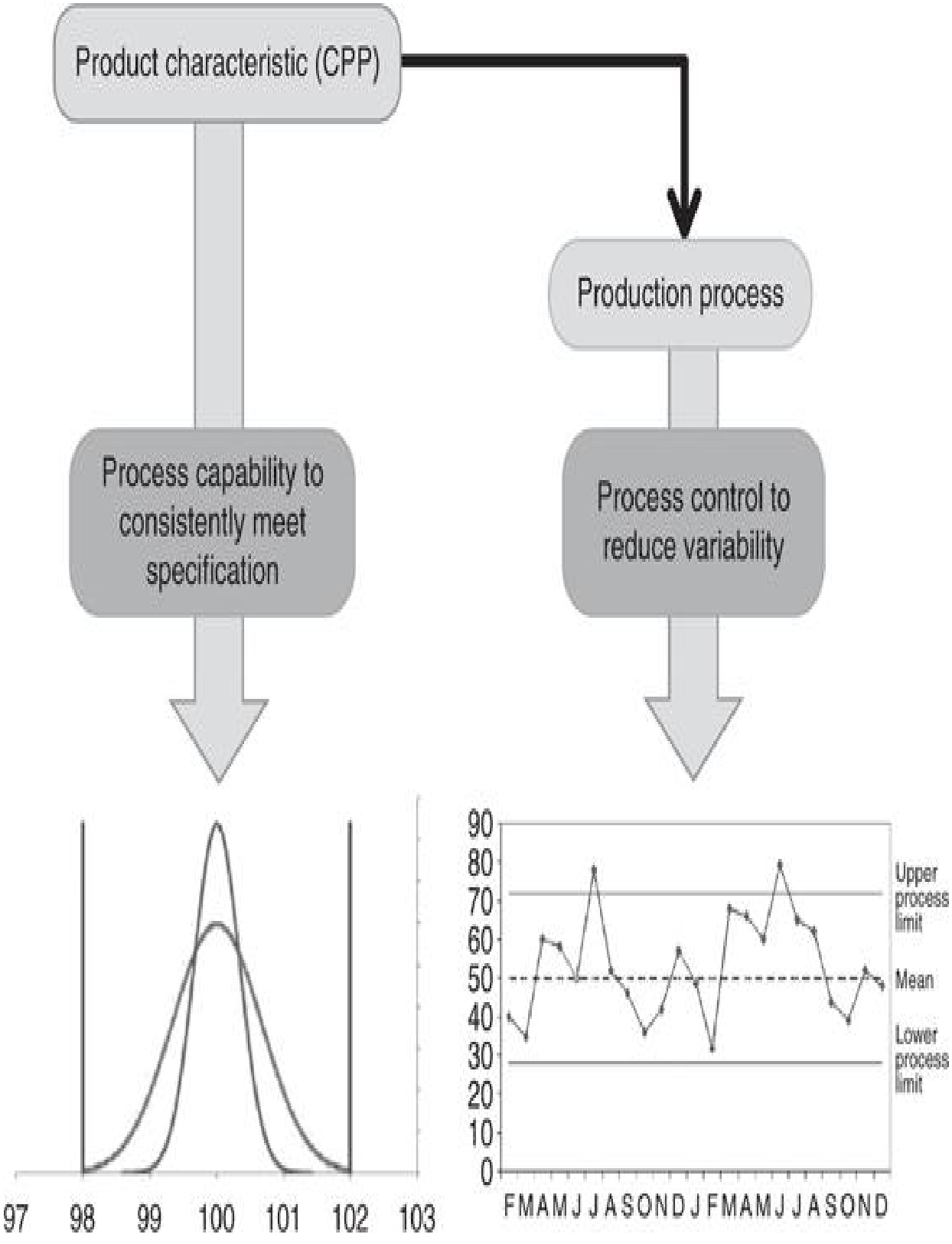


FIGURE 7.6 Process capability index.

After the sourcing team has identified the CPPs and their specification limits, they should ask the supplier to perform a process capability study to determine how well the production facility can meet those requirements, and how many nonconforming parts are predicted for a given lot size. Depending on the result, it may be necessary to implement short-term testing or inspection until the supplier can improve the process capability and reduce the probability of nonconformance.

A supplier may be able to improve process capability by either shifting or “centering” the process mean, or reducing the variability of the process. However, before making any change to the process to improve its performance, the supplier should verify that the process is in control, and eliminate any special causes (see Fig. 7.7).

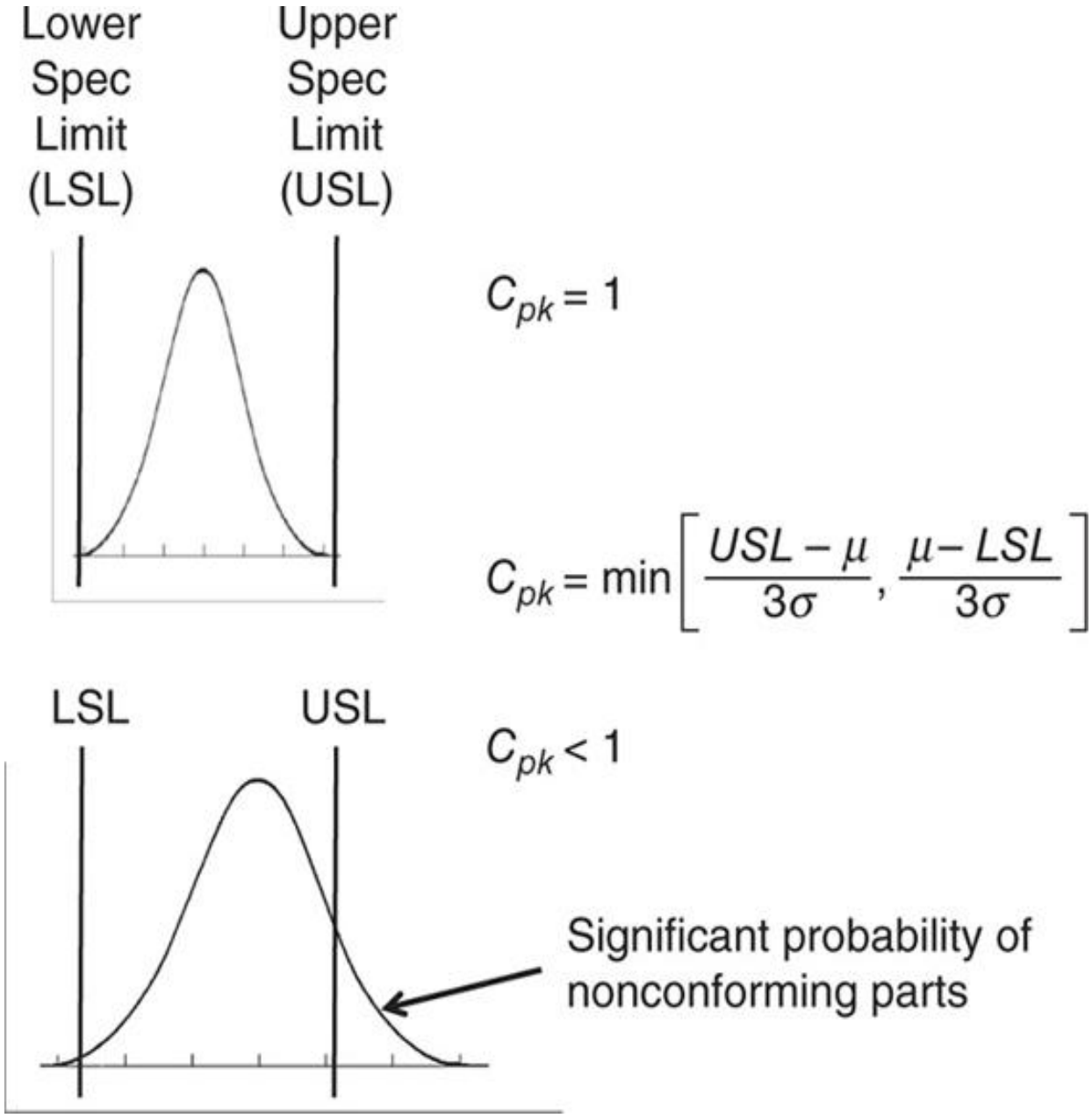


FIGURE 7.7 Process capability and process control.

7.3 PROCESS MONITORING AND TROUBLESHOOTING

A supplier and the sourcing team can use process control and process capability reports to measure the output of a

process. Control charts help determine whether special causes of variability are present that could lead to unpredictable output.

Process capability studies determine the likelihood that the output of the process will be outside the specification limits defined by the customer. However, the goal of a supplier should not only be to prevent nonconforming parts from being sent to the customer, *it should also be to prevent nonconforming parts from being built in the first place*.

The most effective and lowest cost way to assure quality is to define and implement a process that enables a high probability of conforming parts, and then manage the process to identify and systematically eliminate special causes of variability. Active process management leads to higher first pass yields at the factory and higher reliability product in the field.

Once a process is established, it's important to be able to monitor the inputs and operations of the process to determine whether it is being managed effectively. A supplier with an experienced engineering and management team will perform regular internal audits and checks to monitor their processes. However, when a process is not performing well it may be difficult and time consuming to troubleshoot and identify the source of the problem.

7.4 ASSESSING A PCB FABRICATORS CAPABILITY

Chapter 6, "Supplier Selection and Qualification," provides a brief introduction to supplier quality audits and a framework for inspection of production processes to help the sourcing team assess the quality system of a supplier. A more detailed methodology for assessing and troubleshooting PCB

fabrication processes is presented in Tables 7.1 through 7.21. This includes the following focus areas:

1. Engineering and artwork generation
2. Receiving and incoming inspection
3. Innerlayer processing
4. Innerlayer automated optical inspection (AOI)
5. Lamination
6. Drilling
7. Deburr and electroless
8. Outerlayer processing
9. Outerlayer AOI
10. Plating
11. Soldermask and via plugging
12. Hot air leveling
13. Organic surface protection (OSP)
14. Final fabrication and routing
15. Electrical test
16. Final inspection and impedance test
17. Laboratory processes
18. Waste treatment and chemical storage processes
19. Packaging and outgoing quality assurance (OQA)
20. Electroless nickel and immersion gold
21. Maintenance processes

TABLE 7.1 Engineering Process Audit

Item	Audit Criteria
1.00	Are the front-end engineering processes documented, and are the latest revision work instructions, PM, calibration & inspection procedures for all front-end processes in place for operators to follow?
1.01	Does evidence exist that process capability studies have been performed for the artwork generation, i.e., processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp and Cpk reporting?
1.02	Is the overall appearance of the area and equipment condition adequate?
1.03	Does traceability exist that permits tracking the artwork and tool generation to the PCB manufacturing lot numbers and process equipment (CAD station, plotters, exposure machines, etc.)?
1.04	Is there a continuous improvement team in place for the front-end engineering with documented action plans?
1.05	Are the laboratory records for artwork processes complete and up-to-date?
1.06	Are the operator and maintenance PMs documented and objective evidence exists that they are performed?
1.07	Are the calibration labels on critical equipment current?
1.08	Do training records exist for front end personnel and are they current?
1.09	Do health and safety procedures exist and are they being followed?
1.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling artwork?
	Product Engineering
1.11	Is there a formal pre-production design review of product designs with Quality, Engineering, Materials, and Manufacturing involvement for each new part number?
1.12	Is there a procedure in place and objective evidence that pre-production design review is compared to the current volume manufacturing capability matrix before accepting an order?

1.13 Is there objective evidence that a formal review of the customer specification has been performed and that necessary information has been included in all required documentation (traveler, inspection documents, etc.)?

1.14 Is it understood that subcontracting on the product is not allowed without written permission?

1.15 Does the PCB manufacturing site have a current valid ISO certification?

1.16 Is a checklist used to determine all items required for product engineering and tool planning? If so, is there objective evidence that they are used 100% of the time?

1.17 Is there a closed loop system to ensure that all items on the tooling checklist were performed before the tooling is released to production?

1.18 Are the design packages checked and reviewed by authorized personnel prior to being released to production?

1.19 Are there comprehensive design rules for creating tools based on process requirements and customer acceptance criteria?

1.20 Is there an electronic ECO process for all changes made to tooling?

1.21 Is there a process to ensure written approval from the customer prior to making manufacturing, inspection, or test process changes?

1.22 Is there objective evidence that a pre-production lot was run for all new part numbers and revisions before production lots were issued?

1.23 Is the DFM review report signed off by Quality, Production, ME, and TE?

1.24 Is there a log for DFM non-compliance found in pilot run and mass production?

1.25 Is there evidence that Engineering has taken action to all the DFM non-compliance?

1.26 Is there evidence that Engineering has enhanced its design guidelines based on experience?

1.27 Is there a procedure in place and objective evidence for revision controls for traveler, tooling, etc.?

1.28 Is there a procedure in place for the addition of fileting/teardrop to outerlayer trace to pad for PTH, BGA's and SMD's for immersion silver product?

1.29 Is it documented to perform a DRC after the fileting/teardrop addition for spacing violations and other design concerns?

1.30 Does impedance modeling capability exist with a continuous feedback loop from production lots?

1.31 Is there a revision control system in place for all tooling?

	Artwork Generation
1.32	Is the artwork generated in a controlled temperature ± 2.0° C and humidity environment ± 5%?
1.33	Does the temperature and relative humidity in AW generation equivalent to the imaging areas where the film will be used?
1.34	Is the artwork 100% AOI inspected and the data used for continuous improvement?
1.35	Are the artwork dimensions verified and used for SPC and improvement plans?
1.36	Is the artwork Dmin and Dmax measured?
1.37	Has a gage R&R been performed on the artwork dimensional measurement system?
1.38	Does a formalized artwork compensation feedback loop exist with objective evidence?
1.39	Is there an established hold time after the application of artwork protective film coating before artwork dimensional measurements?
1.40	Is a photoplotter registration lines & spacing accuracy check performed every two days and monitored via SPC?
1.41	Is there a separate storage area for artwork not currently in production use? Is it temperature and humidity controlled?
1.42	Is there a documented artwork inventory system that controls artwork revision, film hit count, etc.?
1.43	Is the compare method used to make sure no pattern is missing?
	Drill & Rout Tooling
1.44	Are the drill programs verified against customer data prior to releasing to production?
1.45	Is there a procedure/system in place to verify items not in the drill program supplied: i.e., tooling holes in arrays, slots, etc.?
1.46	Are the rout programs verified against customer data prior to releasing to production?
	Electrical Test Fixtures
1.47	Are electrical test fixtures and programs designed and fabricated in-house?
1.48	Are the electrical test fixtures set-up and verification performed by engineers or engineering technicians?

TABLE 7.2 Receiving and Incoming Process Audit

Item	Audit Criteria
2.00	Are the Receiving & Incoming Inspection processes documented and are the latest revision work instructions, PM, calibration, and inspection procedures in place for operators to follow?
2.01	Does evidence exist for process capability for the incoming processes, i.e., processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp and Cpk reporting?
2.02	Is the overall appearance of the area and equipment condition adequate?
2.03	Does lot traceability exit that permits tracking the raw material lot numbers to the manufacturing lot number?
2.04	Is there a continuous improvement team in place for the Receiving & Incoming Inspection with documented action plans?
2.05	Are the laboratory records for Receiving & Incoming Inspection (bulk chemicals, laminates & prepregs, etc.) processes complete an up to date?
2.06	Are the operator and maintenance PMs documented and objective evidence exist that they are performed?
2.07	Are the calibration labels on critical equipment current?
2.08	Do training records exist for Receiving & Incoming personnel and are they correct?
2.09	Do health and safety procedures exist and are they being followed?
2.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Incoming Inspection
2.11	Are general storage conditions acceptable, with appropriate temperature and humidity control with automatic alarms or notification systems for out of control excursions?
2.12	Are the storage conditions (temperature, humidity, etc.) based on the raw material suppliers recommendations and do they meet those requirements?
2.13	Is the incoming inspection procedure in place which provides the accept criteria for raw material?
2.14	Is incoming inspection performed with actual physical verification of material? If not, do you have a documented ship-to-stock vendor program that includes Certificate of Compliance, periodic inspection plan, documented vendor audit program, vendor process capability program, vendor scorecard, and quarterly vendor review?
2.15	For non-inspection materials or ship-to-stock, is there any evidence of supplier inspection/control plan, and results shown except for collecting C of C, documented vendor audit program, vendor scorecard and quarterly vendor review?
2.16	Are inspected materials and waiting for inspection materials properly labeled, easily identified, and segregated to insure that waiting for inspection materials are not mistakenly used before the inspections have been completed?
2.17	Are all chemical and raw material containers/cartons, etc. properly identified with accept (pass) or reject (fail) labels, with traceability information?
2.18	Are all chemical and raw material containers/cartons, etc. that are identified as received/passed/rejected properly segregated to avoid missing incoming inspection or mistakenly used for production?
2.19	Are all passed lots transferred from the inspection area to parts warehouse within 2 working days?
2.20	Is the shelf like properly defined and identified on material/chemical containers?
2.21	Is there a documented procedure to verify that the material expirations date (shelf life) of all critical materials/chemicals are within the expiration dates in all warehouses and storage areas? Is it audited on a weekly basis?
2.22	Is there a documented procedure for first-in/first-out for materials and chemicals?
2.23	Is there evidence that only passed lots are in the warehouse and production lines?
2.24	Do all failed lots go through the MRB process?
2.25	Do all rework/screen/waive disposition require Engineering and Quality approval?
2.26	Are all material sorts, reworks, and screens performed in a designated area to insure defective materials are not mistakenly mixed with production material?
2.27	Is there a documented Supplier Quality Management system and are the individual suppliers' performance monitored internally on a weekly basis?
2.28	Is there objective evidence that each supplier's quality, cost, and delivery performance is reviewed with the supplier on at least a quarterly basis?

2.29	Are there written procedures which require material and chemical supplier audits? Are they up to date?
2.30	Is there a documented SCAR procedure for material and chemical suppliers?
2.31	Is there objective evidence that SCARs have been issued for rejected lots and parts found?
2.32	Is there a SCAR closure tracking procedure and is it current?
2.33	Are the material suppliers' corrective action responses checked and verified for effectiveness?
2.34	Is the incoming/line/feed quality of major suppliers tracked and feedback to procurement and the suppliers?
2.35	Is there objective evidence that the incoming inspection information is used to rate and disqualify suppliers?
2.36	Is all in-process WIP and materials properly identified and controlled in designated areas?

TABLE 7.3 Innerlayer Fabrication Process Audit

Item	Audit Criteria
3.00	Are the Innerlayer processes documented and are the latest revision work instructions, PM, calibration & inspection procedures for all innerlayer processes in place for operators to follow?
3.01	Does evidence exist that process capability have been performed for the innerlayer processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
3.02	Is the overall appearance of the area and equipment condition adequate?
3.03	Does lot traceability exist that permits tracking the I/L lot number to all major equipment, laminate material, artwork and resist lot used to fabricate the product?
3.04	Is there a continuous improvement team in place for the Innerlayer process area with documented actions plans?
3.05	Are the laboratory records for Innerlayer processes complete and up to date?
3.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
3.07	Are the calibration labels on critical equipment current?
3.08	Do training records exist for front end personnel and are they current?
3.09	Do health and safety procedures exist and are they being followed?
3.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	CCL Shearing
3.11	Is there an evidence that CCL feed speed and cutting direction are well listed in WI?
3.12	Is there a system in place to insure the material grain direction is maintained during the shearing routing operation
	Pre-Clean
3.13	Is the innerlayer preclean process being run per the current documentation?
3.14	Is there a pre-startup checklist for the preclean line? Is it current (completely filled in)?
3.15	Is there a system to identify uneven copper weights on a core and a method to insure that the uneven copper weight cores are imaged correctly?
3.16	Is there objective evidence that the scrub/preclean chemistries are being analyzed by the laboratory on the documented frequency?
3.17	Is the microetch rate monitored? Is it under SPC control with calculated control limits and are the charts & actions current?
3.18	Are dump and remake schedules documented for the preclean line and objective evidence exist that they are being adhered too?

3.19	Are there documented maximum final rinse water contamination levels, rinse flow rates and are these verified by conductivity measurements?
3.20	Is there an evidence to demonstrate that all chemicals are monitored and controlled as listed in WI?
3.21	Is all in-process WIP and materials properly identified and controlled in designate area?
3.22	Is a water break test performed every shift to ensure quality of pre-clean?
3.23	Is there positive air pressure from the cleanroom at the preclean line entrance into the cleanroom?

Imaging

3.24	Is the cleanroom positive pressure monitored on a regular basis with alarms for out of control notification?
3.25	Is the cleanroom well controlled by temperature, humidity and particles which meet 10K Max. requirement and out of control notification? Review objective evidence.
3.26	Are the resist lamination and exposure areas in the cleanroom utilizing yellow lighting and do all exterior windows have UV blocking film?
3.27	Is there a defined specification for the rubber durometer hardness for the lamination rollers and is it checked?
3.28	Is there a documented maintenance replacement schedule for the laminator resist cutter?
3.28	Is there objective evidence to demonstrate that all dry films and/or liquid resist are stored in temperature and humidity control environment? Also, inventoried under FIFO with expired date control?
3.29	Are there tacky roller clean machines in front of the laminator?
3.30	For dry film lamination, is the temperature of the lamination roller checked and verified using an infrared meter?
3.31	Is there a documented resist inspection criteria with pass/fail guidelines?
3.32	Is there an evidence to demonstrate that all chemicals are monitored and controlled as listed in WI?
3.33	Is all in-process WIP and materials properly identified and controlled in designate area? Including expiration date on age sensitive material?

3.34 Is there a documented resist strip/rework procedure with the maximum number of reworks identified?

3.35 Are resist defective cores due to the lamination or coating process fully exposed before resist removal i.e. stripped?

3.36 Is there evidence to demonstrate that exposure energy and vacuum are well controlled? Step tabs/wedges for exposure.

3.37 Is the exposure uniformity monitored across the exposure area with a radiometer and are exposure uniformity limits established and adhered too?

3.38 Is there a latest revision control on working film?

3.39 Is there appropriate verification of artworks before use to check for damage, eg AOI? Is there a stablization process in place before film is used?

3.40 Is there an evidence that working film and T/C are well controlled at cleanning room?

3.41 Is there an evidence that a maximum number of exposures has been established and the number of exposure times of working film is monitored?

3.42 Is the artwork cleaned after defined exposure times using tacky roller? Review the condition of the tacky rollers.

3.43 Are there tools and procedures with tolerance limits in place for front-to-back registration verification during the artwork setup?

3.44 Are first articles processed through DES & AOI prior to exposing the remainder of the lot? Is the front to back verified during this process?

3.45 Is process capability for front-to-back registration on layers measured and controlled? Is it identified as a critical SPC parameter?

3.46 Is the maximum number of permissible exposures documented with a system to track the number of exposures?

3.47 Is the artwork segregated and destroyed after the maximum number of exposures have been reached?

3.48	Is there an evidence that the number of exposure times of working film is monitored and the artwork is not being used beyond documented useful life?
3.49	Is the artwork stored appropriately to prevent damage and ensure the consistent scaling?
3.50	Is the max holding time between expose and develop documented and followed?

Develop-Etch-Strip

3.51	Is there a pre-startup checklist for the DES line? Is it current (completely filled in)?
3.52	Is there an evidence to demonstrate that all chemicals are monitored and controlled as listed in WI?
3.53	Are all in-process WIP and materials properly identified and controlled in designate area?
3.52	Are dump and remake schedules documented for the DES line and objective evidence exist that they are being adhered too?
3.53	Is the developer chemistry analyzed by the laboratory and is it on a feed & bleed pH controller?
3.54	Is "break point " testing performed on the developer for both top and bottom of the core with documented frequency, percent limits & test records?
3.55	Is a first article run prior to etching the lot to confirm etcher settings and linewidths?
3.56	Is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters?
3.57	Is there a manifold nozzle layout & conveyor schedule available and is it used to validate correct equipment setup?
3.58	Is the etch unifomity checked at least monthly and records maintained as a quality document?

3.59	Are the etcher conveyor speeds defined and documented by copper weight/thickness?
3.60	Is "break point" testing performed on the stripper for both top and bottom of the core with documented frequency, percent limits & test records?
3.61	Is the filtration system adequate? What's the clean frequency and renew frequency?
3.62	Is the stripper chemistry analyzed by the laboratory and is it on a feed & bleed controller?
3.63	Are there documented maximum final rinse water contamination levels, rinse flow rates and are these verified by conductivity measurements?
3.64	Are the cores observed coming off the DES line clean, dry and stain free?
3.65	Is there a documented I/L strip/rework procedure with proper quality controls and traceability?
3.66	Are slip sheets used to separate each core (signals & power/grounds) to prevent scratches?
3.67	Is there a system in place to identify the linewidths to be measured on a core?
3.68	Are gage R&R's performed on a routine basis for the linewidth measurement system? Is it current?
3.69	Are the linewidths measured after develop/etch/strip in each lot using equipment of adequate accuracy (eg. Scope has graduations $\leq$0.001"?
3.70	Are linewidth measurement frequency documented and is the frequency at a minimum of the first core, middle and last core off the line in the lot?

TABLE 7.4 Innerlayer AOI Inspection Process Audit

Item	Audit Criteria
4.00	Are the Innerlayer AOI processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all AOI & PEP processes in place for operators to follow?
4.01	Does evidence exist that process capability studies have been performed for the innerlayer AOI processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
4.02	Is the overall appearance of the area and equipment condition adequate?
4.03	Does lot traceability exist that permits tracking the I/L lot number to AOI machine/verification station and rework/repair used in inspection or repair?
4.04	Is there a continuous improvement team in place for the Innerlayer AOI Process Area with documented actions plans?
4.05	Are the laboratory records for Innerlayer processes complete and up to date?
4.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
4.07	Are the laboratory records for Innerlayer processes complete and up to date?
4.08	Do training records exist for Front End personnel and are they current?
4.09	Do health and safety procedures exist and are they being followed?
4.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?
	AOI
4.11	Is 100% AOI performed on signal layers? Are all AOIs operated under a controlled environment? (Humidity, Temperature,...etc)
4.12	Are all in process WIP and materials properly identified and controlled in designate area?
4.13	Are the power and ground layers either AOI inspected or electrical tested based on a statistically valid sampling plan?
4.14	Are the AOI programs data driven using the customer's data and are all the critical AOI settings and programs established by Engineering?
4.15	Does the AOI program have appropriate parameters programed to cover minimum linewidths, minimum spacing, dishdowns, etc?

4.16	Is a standard defect board used to verify each AOI machine is catching all defects at the beginning of each shift?
4.17	Is there a system in place to notify the Image Area for first articles with repeat defects?
4.18	If excess random defects are detected on a lot is this information immediately fed back to the DES operation for review and action? i.e. excess copper, nicks, shorts, opens?
4.19	Is the AOI defect verification performed on separate verification stations and defect data collected and reported in a meaningful manner?
4.20	Is there a limit established for the maximum number of false hits before a lot is reviewed by a MRB/DRB team?
4.21	Are repaired panels re-AOI'd to confirm all defects were found and repaired?
4.22	Are yields tracked daily at AOI and feedback loop to I/L process improvement team established? Are first pass yield and final yield targets defined?
4.23	Are corrective actions taken if yields fall below target?
4.24	Is Pareto analysis used to determine the top defects? Is effective continuous improvement used to eliminate top defects?
	Post-Etch Punch
4.25	Is rivet or pin lamination used?
4.26	Are all in process WIP and materials properly identified and controlled in designate area?
4.27	Is the imaged feature to tooling hole location verified on each lot? Have tolerance limits been established to insure registration for this technology level?
4.28	Is the front to back registration verified based on a sampling plan for each lot?
4.29	For post-etch-punch, Is the offset measured each shift and plotted on SPC? Are there established SPC actions for offset adjustments?
4.30	Does post-etch-punch tooling pattern have non-symmetrical holes to prevent panel being laminated upside down?
4.31	Is the post etch punch calibration and punch sharpening set-up on a routine maintenace schedule and is it current?
4.32	Is there a comprehensive PEP Preventative Maintenance plan with current updated records?

TABLE 7.5 Lamination Process Audit

Item	Audit Criteria
5.00	Are the Oxide, Layup & Lamination processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
5.01	Does evidence exist that process capability studies have been performed for the Oxide, Layup & Lamination processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
5.02	Is the overall appearance of the area and equipment condition adequate?
5.03	Does lot traceability exist that permits tracking the I/L lot numbers to the O/L lot number and to all major equipment and materials i.e. prepreg, laminate, copper foil used to fabricate the product?
5.04	Is there a continuous improvement team in place for the Oxide & Lamination Process Area with documented actions plans?
5.05	Are the laboratory records for Oxide process complete and up to date?
5.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
5.07	Are the calibration labels on critical equipment current?
5.08	Do training records exist for Front End personnel and are they current?
5.09	Do health and safety procedures exist and are they being followed?
5.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?
	Pre-Lamination
5.11	Does evidence exist that the Oxide Chemistry supplier has audited the line in the previous three months? If so, were actions taken?
5.12	Have DOEs been conducted to verify the optimum oxide thickness to ensure no delamination after thermal stress test?
5.13	Are all in-process WIP and materials properly identified and controlled in designate area?
5.14	Is the microetch rate monitored? Is it under SPC control with calculated control limits and are the charts & actions current?
5.15	For horizontal oxide lines, is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters? How are nozzles checked for plugs and proper spray pattern

5.16	Are oxide bond strength test performed for all material types for each oxide line used on the product on a weekly basis?
5.17	Are the oxide chemistries on a auto-dosing system?
5.18	Is DI water used for rinses?
5.19	Are the cores exiting the machine dry and stain free?
5.20	Is the 5% HCL or 10% Sulfuric acid spot test performed and are the results greater than 10 minutes?
5.21	Is the Weight gain test performed for Black Oxide and Weight Loss test for Brown Oxide process? SPC Chart
5.22	Is there an evidence that black oxide thickness is well controlled?
5.23	Are the oxided panels uniform in color, appearance and free of scratches/handling damage?
5.24	Are cores reworked at oxide? If so, is there a documented rework procedure with the maximum number of reworks established?

Lamination

5.25	Is the lay-up done in a clean room with adequate temperature and humidity control?
5.26	Are there established hold-times for oxide cores in the layup operation?
5.27	Are all in-process WIP and materials properly identified and controlled in designate area?
5.28	Are prepreg types and MFG date identified during lay-up? Are material types tracable to incoming and is recorded on work order?
5.29	Has adequate testing and DOE's been performed insure the dielectric and board press out thickness for all copper weights, signal, P/G layers and degree of cure have been optimized?
5.30	Are the lamination programs defined depending on the different stack ups? How to select the lamination program?
5.31	Are Rivet process or Pin-lamination used to hold stacks to ensure the registration?

5.32	Is the material profile done regularly to ensure the actual cooldown rate not exceed 5 deg C/minute? What is the heat rise and cool down rate?
5.33	Are steel plates cleaned for each cycle and polished periodically? Is the thickness of the steel plate checked regularly?
5.34	Is there an evidence that lamination press platen flatness/parallelism is checked minimum once per six months ?
5.35	Is the temperature uniformity for each press opening monitored using thermocouples each shift?
5.36	Are the laminated panels inspected for resin spots?
5.37	Is board thickness measured after lamination on all panels or on appropriate sample size at a min 5 points on each panel?
5.38	Is SPC used to track the board thickness by part number and does a action plan exist for out of control points?
5.39	Does a feedback loop exist for dielectric and PCB thickness to Front-End Engineering for continuous improvement and out of control situations?
5.40	Is there X-ray punch with accuracy compensation design for registration control?
5.41	Is there a documented quality conformance procedure with accept/reject criteria for lamination press malfuctions (temperature, pressure, etc. interuptions) to insure the quality of the product in the press?
5.42	Is there a lamination repair document that prevents re-lamination and abrasive techniques for the removal of epoxy spots or board thickness violations?
5.43	Are procedures in place for inspecting and testing lamination integrity?
	Pre-Drill X-ray
5.44	Does there exist a documented accept/reject criteria at pre-drill x-ray for misregistration?
5.45	Are all in-process WIP and materials properly identified and controlled in designate area?
5.46	Is there a documented routine dimensional measurement confirmation performed on the x-ray pre-drill measurement system?
5.47	Is there on-going feedback mechanism to use X-ray drill measurements to optimize artwork scaling factor?

TABLE 7.6 Drilling Process Audit

Item	Audit Criteria
6.00	Are the Drill & Resharpening processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
6.01	Does evidence exist that process capability studies have been performed for the Drill & Resharpening processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
6.02	Is the overall appearance of the area and equipment condition adequate?
6.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. drill machine, drill bits, etc. used to fabricate the product?
6.04	Is there a continuous improvement team in place for the Drill Process Area with documented actions plans?
6.05	Are the laboratory records (i.e. Cross-sections for hole roughness, etc.) for Drill process complete and up to date?
6.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
6.07	Are the calibration labels on critical equipment current?
6.08	Do training records exist for the Drill & Resharpening operators and are they current?
6.09	Do health and safety procedures exist and are they being followed?
6.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

6.11 Does the traveller clearly define all the drilling parameters including stack height?

6.12 Is the stack height, maximum hit per drill bit, and feeds and speeds as a function of laminate type, board thickness, layer count and hole size controlled properly?

6.13 Is the drilling program checked prior to being released for production?

6.14 Is there evidence to demonstrate that spindle run-out is well controlled?

6.15 Does the drilling machine have broken bit and wrong bit size detection capability?

6.16 Is drilled hole registration checked by cross-section or X-ray? What is the frequency?

6.17 Is true position monitored monthly for each spindle and controlled to +/–3 mils?

6.18 Do action plans exist for investigating and reducing broken bits? Does objective evidence exist that this is in control?

6.19 Is there a documented drill rework/repair procedure with quality checks?

6.20 Are PCB's with missing holes placed back on the drill machine and drilled?

6.21 Are resharpened drill bit inspected and identified prior to use?

6.22 Are the maximum number of re-sharpens documented & controlled?

6.23 Is the inspection of new or resharpened drill bits flute length, diameter performed with non-contact method?

6.24 Are Aluminum plates inspected for dents and scratches before use?

6.25 Are output boards at the bottom of each spindle inspected on the hole size & location, hole registration and hole quantity etc?

6.26 Is there an effective process for removing surface debris after drilling?

6.27	Are collets PM(ed) periodically?
6.28	Is there a general inspection procedure with drilling positional accuracy, hole size, hole quantity, hole location and copper surface appearance defined?
6.29	Are drill machines capability data for hole position accuracy traceable for each machine and spindle?
6.30	Are drill machines capability data for runout traceable for each machine and spindle?
6.31	Is the stroke height checked & pressure foot inspected weekly?
6.32	Is the depth into the back-up material checked for each spindle weekly?
6.33	Is there a documented quality conformance procedure with accept/reject criteria for drill machine malfuctions (vacuum, air pressure, etc. interuptions) to insure the quality of the product in the press?
6.34	Is registration monitored by Perfect Test machine or X-ray check after Drilling?
6.35	Is the hole roughness monitored as part of the cross-section evaluations and is this information feedback to the drill process and quality engineer?
6.36	Is SPC used in Drilling process?
6.37	Are all passed/rejected boards properly labeled and segregated to avoid mixing or missing?
6.38	Does all in process WIP and materials be properly identified and controlled?
6.39	Is there a SPC control implemented and control chart updated for critical parameters?
6.40	Are relevant corrective actions taken toward all the out of control points?

TABLE 7.7 Deburr & Electroless Process Audit

Item	Audit Criteria
7.00	Are the Deburr & Electroless Copper Plating processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
7.01	Does evidence exist that process capability studies have been performed for the Electroless Copper Plating process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
7.02	Is the overall appearance of the area and equipment condition adequate?
7.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. deburr machine, plating line, plating tanks, etc. used to fabricate the product?
7.04	Is there a continuous improvement team in place for the Electroless Process Area with documented actions plans?
7.05	Are the laboratory records (i.e. Chemical Analysis, Backlight, X-sections, etc.) for Deburr & Electroless Copper Plating process complete and up to date?
7.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
7.07	Are the calibration labels on critical equipment current?
7.08	Do training records exist for the Deburr & Electroless Copper Plating operators and are they current?
7.09	Do health and safety procedures exist and are they being followed?
7.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Deburring
7.11	Is there a pre-startup checklist for the Deburr line? Is it current(completely filled in)?
7.12	Are there air knives, fluid heads & ultrasonics on the deburr machine?
7.13	Is there a wet course-grit scrubber ~180-330grit in the deburr line?
7.14	Are all in-process WIP and materials properly identified and controlled in designate area?
7.15	Is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters?
7.16	Is a hole inspection/checker used after deburr for plugged holes? If so, are the data used for continuous improvement activities.
7.17	Is there evidence to demonstrate that good control of scrubbing rollers - bristle check?
7.18	Is the Ultrasonic vibration check with a meter each shift and data included in the shift check list?
7.19	Does the process documentation cover the procedures to be used for different technology PCBs i.e. standard lower technology versus high aspect ratio, thick PCB's? Are they passed through multiple times?
7.20	Is the uniformity of the pressure checked as part of startup checklist?
7.21	After the deburr operation are the exterior of the boards and holes completely dry?
7.22	Are footprints performed as part of the startup procedure and when board thickness changes?

	Desmear
7.23	Is there a pre-startup checklist for the Desmear line? Is it current?
7.24	Were the pre-startup checklist, process documentation, rework and inspection procedures based on the chemisry suppliers recommendations?
7.25	Are Dump and Remake schedules documented for the Desmear line and objective evidence exist that they are being adhered too?
7.26	Are all in-process WIP and materials properly identified and controlled in designate area?
7.27	Is the permanganate electrolytically regenerated?
7.28	Are the temperatures, pumps, bath condition, tanks/sumps and process times on the line within the process specifications?
7.29	Is the weight loss checked regularly to verify the effective of the desmear?
7.30	Is there an evidence that chemical analysis is performed periodically?

	Electroless
7.31	Is a standard electroless copper process utilized for the product?
7.32	Is there a pre-startup checklist for the electroless line? Is it current (completely filled in)?
7.33	Are the pre-startup checklist, process documentation, rework and inspection procedures based on the chemistry suppliers recommendations?
7.34	Are all in-process WIP and materials properly identified and controlled in designate area?
7.35	Does the chemical area have negative pressure or a ventilization design that provide adequate ventilation in the process area?
7.36	Is the incoming process water tested for pH, ionic and organic contaminants?
7.37	Is all process chemistries utilizing deionized (DI) or reverse osmosis (RO) water?
7.38	Is the microetch rate monitored? Is it under SPC control with calculated control limits and are the charts & actions current?
7.39	Is the deposition rate (weight gain) of electroless copper tank performed regularly?
7.40	Is backlight inspection performed to check the coverage of the electroless copper including both sides of the hole?
7.41	Is dummy-plating performed as part of the start-up procedure before electroless copper plating product?
7.42	Is auto-dosing utilized on the electroless copper bath?
7.43	For vertical electroless copper lines, is the overall basket conditions good and panel spacing greater than 0.5 inches?
7.44	Do the elecroless copper tanks have vibration? Are they in good condition and on a preventative maintenance schedule?
7.45	For horizontal electroless copper platers, is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters? How are nozzles checked for plugs and proper spray pattern?
7.46	Are the panels as observed coming off the plating line clean, dry and stain free?
7.47	Is there chemical filtration used in support tanks?
7.48	Are the temperatures, pumps, bath condition, tanks/sumps and process times on the line within the process specifications?
7.49	Is there a documented allowable rework procedure with appropriate quality checks?
7.50	Are Dump and Remake schedules documented for the electroless line and objective evidence exist that they are being adhered too?
7.51	Is there a documented line down procedure that clearly identifies the appropriate steps for the product in the line?
7.52	Is there a documented quality conformance procedure with accept/reject criteria for electroless plating line malfuctions (hoist, time, temperature, etc. interuptions) to insure the quality of the product in the line at the time of malfunction?
7.53	Is there an active continuous improvement team for plating voids in the electroless copper operation?
7.54	Is there a documented clearly defined cleaning procedure for the electroless tanks?
7.55	Is SPC used for Desmear and Electroless process ? Is the corrective action taken for the out of control status?

TABLE 7.8 Outerlayer Process Audit

Item	Audit Criteria
8.00	Are the Outerlayer Preclean & Imaging processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
8.01	Does evidence exist that process capability studies have been performed for the Outerlayer Preclean & Imaging process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
8.02	Is the overall appearance of the area and equipment condition adequate?
8.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. process lines, resist lot number, etc. used to fabricate the product?
8.04	Is there a continuous improvement team in place for the Outerlayer Process Area with documented actions plans?
8.05	Are the laboratory records (i.e. Chemical Analysis, etc.) for Outerlayer Preclean & Imaging process complete and up to date?
8.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
8.07	Are the calibration labels on critical equipment current?
8.08	Do training records exist for the Outerlayer Preclean & Imaging operators and are they current?
8.09	Do health and safety procedures exist and are they being followed?
8.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Pre-Clean	
8.11	Is there a pre-startup checklist for the preclean line? Is it current(completely filled in)?
8.12	If the preclean line is a scrub, is the footprint inspection procedure documented and performed for different thickness product?
8.13	If the outerlayer preclean inludes a microetch, is the microetch rate monitored and is the electroless copper thickness compensated for the copper removal?
8.14	Is there objective evidence that the scrub/preclean chemistries are being analyzed by the laboratory on the documented frequency?
8.15	If a scrub preclean is used, is there an established brush - bristle maintenance schedule?
8.16	Are all in-process WIP and materials properly identified and controlled in designate area?
8.17	Are Dump and Remake schedules documented for the preclean line and objective evidence exist that they are being adhered too?
8.18	Are the final rinses deionized or RO water?
8.19	Are the panels as observed coming off the preclean line clean, dry and stain free?

	Imaging
8.20	Is the cleanroom well controlled by temperature, humidity and particles which meet 10K Max. requirement and out of control notification? Review objective evidence.
8.21	Is the cleanroom positive pressure monitored on a regular basis with alarms for out of control notification?
8.22	Are the process documentation, rework and inspection procedures based on the resist suppliers recommendations?
8.23	Are all in-process WIP and materials properly identified and controlled in designate area?
8.24	Are the resist lamination and exposure areas in the cleanroom utilizing yellow lighting and do all exterior windows have UV blocking film?
8.25	Is there objective evidence to demonstrate that all dry films and/or liquid resist are stored in temperature and humidity control environment? Also, inventoried under FIFO with expired date control?
8.26	Is there a defined specification for the rubber durometer hardness for the lamination rollers and is it checked?
8.27	Is there a documented maintenance replacement schedule for the laminator resist cutter?
8.26	Are tack roller clean machines used in front of the laminator?
8.27	Is the temperature of the lamination roller checked and verified using the infrared meter?

8.28 Is there inspection criteria applied for dry film lamination with documented pass/fail criteria? (eg, bubble, tension force)

8.29 Is there a documented resist strip/rework procedure with the maximum number of reworks identified?

8.30 Are resist defective panels due to the lamination or coating process fully exposed before resist removal i.e. stripped?

8.31 Is there a latest revision control on working film?

8.32 Is there appropriate verification of artworks before use to check for damage, eg AOI? Is there a stablization process in place before film is used?

8.33 Is the artwork cleaned after defined exposure times using tacky roller? Review the condition of the tacky rollers.

8.34 Is there evidence to demonstrate that exposure energy and vacuum are well controlled? Step tabs/wedges for exposure.

8.35 Is the exposure uniformity monitored across the exposure area with a radiometer and are exposure uniformity limits established and adhered too?

8.36 Are first articles processed through Outerlayer Develop & AOI prior to exposing the remainder of the lot? Is the front to back verified during this process?

8.37 Is process capability for front-to-back registration on layers measured an controlled?

8.38 Is the maximum number of permissible exposures documented with a system to track the number of exposures?

8.39 Is the artwork segregated and destroyed after the maximum number of exposures have been reached?

8.40 Are artworks stored appropriately to prevent damage and ensure the consistent scaling?

8.41 Is the max holding time between expose and develop documented and followed?

Outerlayer Develop–Panel Plating Process–DES Line	
8.42	Is there a pre-startup checklist for the develop line? Is it current(completely filled in)?
8.43	Are Dump and Remake schedules documented for the developer and objective evidence exist that they are being adhered too?
8.44	Are all in-process WIP and materials properly identified and controlled in designate area?
8.45	Is the developer chemistry analyzed by the laboratory and is it on a feed & bleed pH controller?
8.46	Is "break point" testing performed on the developer for both top and bottom of the core with documented frequency, percent limits & test records?
8.47	Is a first article run prior to developing the lot to confirm developer settings and linewidths?
8.48	Is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters?
8.49	Is there a manifold nozzle layout & conveyor schedule available and is it used to validate correct equipment setup?
8.50	Are there documented maximum final rinse water contamination levels, rinse flow rates and are these verified by conductivity measurements?
8.51	Are the panels observed coming off the developer line clean, dry and stain free?
8.52	Is there a documented allowable rework procedure with appropriate quality checks?
8.53	Is there a documented O/L strip/rework procedure with proper quality controls and traceability?
8.54	Is there a system in place to identify the linewidths to be measured on a panel?
8.55	Are Gage R&R's performed on a routine basis for the linewidth measurement system? Is it current?
8.56	Are all repaired boards identified for traceability?
8.57	Is there a documented maximum hold time for panels with laminated photoresist before copper plating?

TABLE 7.9 Outerlayer AOI Inspection Process Audit

Item	Audit Criteria
9.00	Are the Outerlayer AOI & Repair processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
9.01	Does evidence exist that process capability studies have been performed for the Outerlayer AOI & Repair process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
9.02	Is the overall appearance of the area and equipment condition adequate?
9.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. AOI machine, verification station, operator, welder, etc. used to fabricate the product?
9.04	Is there a continuous improvement team in place for the Outerlayer AOI & Repair Process Area with documented actions plans?
9.05	Are the laboratory records for Outer Layer AOI processes complete and up to date?
9.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
9.07	Are the calibration labels on critical equipment current?
9.08	Do training records exist for the Outerlayer AOI & Repair operators and are they current?
9.09	Do health and safety procedures exist and are they being followed?
9.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Outerlayer AOI	
9.11	Is 100% AOI performed on outlayer? If No, what's the sample size?
9.12	Are the AOI programs data driven using the customer's data and are all the critical AOI settings and programs established by Engineering?
9.13	Are all in-process WIP and materials properly identified and controlled in designate area?
9.14	Does the AOI program have appropriate parameters programed to cover minimum linewidths, minimum spacing, dishdowns, etc?
9.15	Is there a system in place to notify the Image Area for first articles with repeat defects?
9.16	If excess defects are detected on a lot is this information immediately fed back to the previous operation for review and action? i.e. excess copper, nicks, shorts, opens?
9.17	Is the AOI defect verification performed on separate verification stations and defect data collected and reported in a meaningful manner?
9.18	Is there a documented procedure identifing the maximum number of repairs allowed, including but not limited too welding opens, cutting out shorts and excess copper spots, etc?
9.19	Is there a limit established for the maximum number of false hits before a lot is reviewed by a MRB/DRB team?
9.20	Are repaired panels re-AOI'd to confirm all defects were found and repaired?
9.21	Are all repaired boards identified for traceability?
9.22	Are yields tracked daily at AOI and feedback loop to O/L process improvement team established? Are first pass yield and final yield targets defined?
9.23	Does the In-process Inspection check the boards after AOI/verification on sampling basis? Is the loss rated of AOI monitored?
9.24	Are corrective actions taken if yields fall below target?
9.25	Is golden boards used to check the AOI machine before the inspection of each shift?
9.26	Is Pareto analysis used to determine the top defects? Is effective continuous improvement used to eliminate top defects?

TABLE 7.10 Plating Process Audit

Item	Audit Criteria
10.00	Are the Electrolytic Copper Plating processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
10.01	Does evidence exist that process capability studies have been performed for the Electrolytic Copper Plating process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
10.02	Is the overall appearance of the area and equipment condition adequate?
10.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. Plating chemistry, plating line, plating tank, etc. used to fabricate the product?
10.04	Is there a continuous improvement team in place for the Electrolytic Copper Plating Process Area with documented actions plans?
10.05	Are the laboratory records (i.e. Chemical Analysis, Cross-sections, etc.) for Electrolytic Copper Plating process complete and up to date?
10.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
10.07	Are the calibration labels on critical equipment current?
10.08	Do training records exist for the Electrolytic Copper Plating operators and are they current?
10.09	Do health and safety procedures exist and are they being followed?
10.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Copper Plating	
10.11	Is there a pre-startup checklist for the electrolytic copper plating line? Is it current (completely filled in)?
10.12	Are the pre-startup checklist, process documentation, rework and inspection procedures based on the chemistry suppliers recommendations?
10.13	Do the plating current and program used match the design and traveler? What is the ASF range used during plating? Who determines ASF? How?
10.14	Is the copper plating process an electrolytic acid copper plating system?
10.15	Is dummy-plating performed as part of the start-up procedure before plating product?
10.16	Is all in-process WIP and materials properly identified and controlled in designate area?
10.17	Is chemical area with good ventilization design for operation enviroment control?
10.18	Is incoming water tested with PH and organics?
10.19	Is all chemistry utilizing (DI) water?
10.20	Is the operation conducted in a enclosed and controlled environment?
10.21	Are organic & inorganic contaminants in the plating tank analyzed and monitored?
10.22	Is vibration used? How often is the vibration checked?
10.23	Is a CVS used for additive analysis?
10.24	Are Hull Cells performed on a routine frequency?
10.25	Is there an established schedule for the anode, buss bars, and cables maintenance? Is it current?
10.26	Are the anodes at a satisfactory level in the anode baskets based on the date of the last anode maintenance?
10.27	Are the buss bars clean, insulation on the cables in good condition, and are the cables connections free of corrosion?
10.28	Is the resistance of the of the buss bars and cables checked as part of the weekly maintenace?
10.29	Is there an documented rectifier calibration procedure and is it current?
10.30	Is the filter bag cleaned and checked periodically to ensure no plugging and broken?
10.31	Are filters managed properly? Clean frequency, renew frequency?
10.32	Is there an established carbon treatment schedule with a maximum frequency of treating each plating tank every six months?
10.33	Is PTH and small via hole wall quality checked by cross-section and followed by a closed loop corrective action?
10.34	Are cross-sections frequency performed per GNTX-7000?

10.35 Is the customer specification for copper thickness documented on the traveler and other quality documents?

10.36 Is a Caviderm used for copper thickness process control? If so, has a copper thickness coorelation to cross-sections been performed and smallest via on the panel?

10.37 Is there a documented procedure to verify hole size for press-fit and other tight toleranced plated through holes at the electroplating operation using pin gages?

10.38 Is there a feedback loop to pre-production engineering to provide hole size data to insure the hole sizes are centered on nominal and have a good Cpk?

10.39 Is there a documented quality conformance procedure with accept/reject criteria for electrolytic plating line malfuctions(hoist, time, temperature, etc. interuptions) to insure the quality of the product in the plating line?

10.40 Is there an evidence that the elongation and tensile strength test is conducted on a frequency of once per month per copper plating tank?

10.41 Are plating distributions performed each plating tank on a monthly basis?

10.42 Is the tin thickness and uniformity monitored regularly to ensure the quality?

10.43 Are thermal stressed cross-sections performed as an in-process plating control?

10.44 Is there an evidence that expiration date of all wet materials are well controlled?

10.45 Is pure tin used as etch resist in plating ?

10.46 Is there a documented allowable rework procedure with appropriate quality checks?

10.47 If product is reworked, is the rework documented on the traveler, and does the reworked product receive appropriate re-inspection and testing?

Strip-Etch-Strip	
10.48	Is there a pre-startup checklist for the strip-etch-strip line? Is it current(completely filled in)?
10.49	Are Dump and Remake schedules documented for the strip-etch-strip and objective evidence exist that they are being adhered too?
10.50	Is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters?
10.51	Is there a manifold nozzle layout & conveyor schedule available and is it used to validate correct equipment setup?
10.52	Are all in-process WIP and materials properly identified and controlled in designate area?
10.53	Is "break point " testing performed on the stripper for both top and bottom of the panel with documented frequency, percent limits & test records?
10.54	Is the filtration system adequate? What's the clean frequency and renew frequency?
10.55	Are the etchant, stripper and tin strip chemistries analyzed by the laboratory and are they on a feed & bleed controller?
10.56	Is a first article run prior to etching the lot to confirm etcher settings and linewidths?
10.57	Are the etcher conveyor speeds defined and documented by external copper weight/thickness?
10.58	Is the etch unifomity checked at least monthly and records maintained as a quality document?
10.59	Are there documented maximum final rinse water contamination levels, rinse flow rates and are these verified by conductivity measurements?
10.60	Are slip sheets used to separate each panel to prevent scratches?
10.61	Is there a system in place to identify the linewidths to be measured on a panel?
10.62	Are fine pitch SMT pad size measured and SPC utilized?
10.63	Are Gage R&R's performed on a routine basis for the linewidth measurement system? Is it current?
10.64	Is there evidence that the impedance is being monitored/checked as part of the SES first article on controlled impedance product?
10.65	Is "break point " testing performed on the strip tin for both top and bottom of the panel with documented frequency, percent limits & test records?
10.66	Are the panels observed coming off the SES line clean, dry and stain free?

TABLE 7.11 Soldermask & Via Plugging Process Audit

Item	Audit Criteria
11.00	Are the Soldermask, Legend & Via Plugging processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
11.01	Does evidence exist that process capability studies have been performed for the S/M process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
11.02	Is the overall appearance of the area and equipment condition adequate?
11.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. Soldermask coaters, developers, Imaging equipment etc. used to fabricate the product?
11.04	Is there a continuous improvement team in place for the Soldermask Process Area with documented actions plans?
11.05	Are the laboratory records (i.e. Chemical Analysis, S/M Thickness, etc.) for Soldermask process complete and up to date?
11.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
11.07	Are the calibration labels on critical equipment current?
11.08	Do training records exist for the Soldermask operators and are they current?
11.09	Do health and safety procedures exist and are they being followed?
11.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Pre-Clean
11.11	Is there a pre-startup checklist for the preclean lines? Is it current (completely filled in)?
11.12	Is there objective evidence that the scrub/preclean chemistries are being analyzed by the laboratory on the documented frequency?
11.13	If the preclean is a scrub, are footprints performed and is this requirement documented?
11.14	If the preclean is a microetch, is the microetch rate monitored and is this requirement documented?
11.15	Is the soldermask preclean/scrub process being run per the current documentation?
11.16	If a scrub preclean is used, is there an established brush—bristle maintenance schedule?
11.17	Is all in-process WIP and materials properly identified and controlled in designate area?
11.18	Are Dump and Remake schedules documented for the preclean line and objective evidence exist that they are being adhered too?
11.19	Are the final rinses deionized or RO water?
11.20	Is there positive air pressure from the cleanroom at the preclean line entrance into the cleanroom?
11.21	Are the panels completely dry (esp. in the holes) upon exit?

Soldermask Printing

11.22 Is there a pre-startup checklist for the soldermask coaters? Is it current (completely filled in)?

11.23 Are the panels racked or stacked before coat?

11.24 Is all in-process WIP and materials properly identified and controlled in designate area?

11.25 Is the viscosity of the solder mask after preparation checked to ensure the quality?

11.26 Is the date and time that the soldermask expires after preparation specified on its container?

11.27 Is there objective evidence to demonstrate that all soldermasks are stored in temperature and humidity control environment? Also, inventoried under FIFO with expired date control?

11.28 Is there evidence to demonstrate that the cleaness is well controlled of solder mask coating room?

11.29 Are the soldermask coaters cleaned and maintained to a documented procedure?

11.30 If soldermask screen printers are used, is the silk-screen stencil life cycle controlled?

11.31 If soldermask screen printers are used, are the silk-screen stencils identified with labels or plates which as visible when the stencil is in its racks or mounted in the printer?

11.32 Is there a documented requirement to inspect a stencil once cleaned?

11.33 Is the screen tension checked before each use?

11.34 Are the squeegees controlled properly, such as the width, angle, resharpen freq?

11.35 Is there a system in place to determine the S/M coated weight or coated thickness and tack dry weight loss? Is it under SPC control?

11.36 Is there a documented allowable rework procedure with appropriate quality checks?

11.37 Are thermal profiles performed on the tack dry ovens on a documented schedule? Is there objective evidence that it is being performed?

11.38 Are thermal profiles performed on the tack dry ovens when fully loaded?

Soldermask Exposure	
11.39	Is there a pre-startup checklist for the exposure units? Is it current(completely filled in)?
11.40	Is imaging done in a clean room with the parameters tracked effectively (temperature, humidity, particulate counts)?
11.41	Are the working films clearly defined the P/N REV and No. of exposure?
11.42	Are all in-process WIP and materials properly identified and controlled in designate area?
11.43	Is the cleanroom positive pressure monitored on a regular basis with alarms for out of control notification?
11.44	Are the soldermask coating and exposure areas in the cleanroom utilizing yellow lighting and do all exterior windows have UV blocking film?
11.45	Is there appropriate verification of the artwork before use to check for damage, eg AOI?
11.46	Is there inspection criteria applied for S/M with documented pass/fail criteria?
11.47	Is there a documented S/M strip/rework procedure after coat or expose with the maximum number of reworks identified?
11.48	Are defective S/M coated panels due to S/M misregistration or other coating problems fully exposed before S/M removal i.e. stripped?
11.49	Is there appropriate verification of artworks before use to check for damage? Is there a stablization process in place before film is used?
11.50	Is there a documented process for requesting compensated S/M artwork for registration problems?
11.51	Are artworks cleaned after defined exposure times using tacky roller? Review the condition of the tacky rollers.
11.52	Is there evidence to demonstrate that exposure energy and vacuum are well controlled? Step tabs/wedges for exposure.
11.53	Is the exposure uniformity monitored across the exposure area with a radiometer and are exposure uniformity limits established and adhered too?
11.54	Is there a documented procedure to monitor exposure machine lamp life based on power output measurements (i.e. mW/cm^2)?
11.55	Are first articles processed through S/M Develop & Inspection prior to exposing the remainder of the lot? Is the registration verified during this process?
11.56	Is process capability for registration measured and controlled?
11.57	Is the maximum number of permissible exposures documented with a system to track the number of exposures? Also, are the artworks segregated and destroyed after the maximum number has been reached?
11.58	Is the artwork segregated and destroyed after the maximum number of exposures have been reached?
11.59	Is there a documented allowable rework procedure with appropriate quality checks?
11.60	Is the artwork stored appropriately to prevent damage and ensure the consistent scaling?
11.61	Is the max holding time between expose and develop documented and followed?

Developing

11.62 Is there a pre-startup checklist for the Develop line? Is it current (completely filled in)?

11.63 Is development tank filtration checked before each shift operation?

11.64 Are all in-process WIP and materials properly identified and controlled in designate area?

11.65 Are Dump and Remake schedules documented for the developer and objective evidence exist that they are being adhered too?

11.66 Is the developer chemistry analyzed by the laboratory and is it on a feed & bleed pH controller?

11.67 Is "break point" testing performed on the developer for both top and bottom of the core with documented frequency, percent limits & test records?

11.68 Is a first article run prior to developing the lot to confirm developer settings, registration and soldermask clearances?

11.69 Is there an established frequency that the operator inspects the line for plugged nozzles, conveyor problems and adherences to process parameters?

11.70 Is there a manifold nozzle layout & conveyor schedule available and is it used to validate correct equipment setup?

11.71 Are there documented maximum final rinse water contamination levels, rinse flow rates and are these verified by conductivity measurements?

11.72 Are the panels observed coming off the developer line clean, dry and stain free?

11.73 Is there a documented S/M strip/rework procedure with proper quality controls and traceability?

11.74 Are Gage R&R's performed on a routine basis for the S/M defined pad size measurement system? Is it current?

11.75 Are S/M defined pads & registration measured after develop on min first, middle, and last panel in each lot using equipment of adequate accuracy (eg. Scope has graduations <0.005"

11.76 Are Panels inspected after developing?

	Soldermask Cure
11.77	Are all in-process WIP and materials properly identified and controlled in designate area?
11.78	Is there a pre-startup checklist for the S/M cure ovens/line? Is it current(completely filled in)?
11.79	Is the solder mask thickness effectively monitored?
11.80	Is a S/M cure monitored on a routine/documented procedure? Does objective evidence exist?
11.81	Is the same S/M material used for touch-up & repair as was originally coated on the PCB?
11.82	Is there a S/M strip operation after final cure? Is it a documented & controlled process?
11.83	Does the first pass yields for soldermask include the soldermask strip data/quantity?
11.84	Are cross-sections taken to monitor the S/M sidewall for undercut, etc. Are these reviewed by Engineering?
11.85	Is there a documented allowable rework procedure with appropriate quality checks?
11.86	Are tack dry/final cure ovens cleaned & calibrated as part of the routine maintenance?
11.87	Are thermal profiles performed on the final cure ovens on a documented schedule? Is there objective evidence that it is being performed?
11.88	Are thermal profiles performed on the final cure ovens when fully loaded?

Via Plugging/Cap & Legend

11.89 Are all in-process WIP and materials properly identified and controlled in designate area?

11.90 Does the current process documentation cover screen preparation, screen cleaning, emulsion coating/application, exposure, development and baking conditions?

11.91 Is the screen exposure performed in an environmentally controlled area with the relative humdity controlled to with +/−5% and temperature control of +/−2 degrees C?

11.92 Has the via plugging and legend process capabilities i.e. DOE's, etc been performed to optimize the screen mesh used, ink viscosity, blotting frequency (absorption paper), registration to prevent via plug or legend ink on SMT pads for the tightest tolerance designs?

11.93 Are there sufficient controls for ensuring via fill requirements are met?

11.94 Is the viscosity of the via plug ink checked after preparation to ensure that it mets documented requirements?

11.95 Is there objective evidence to demonstrate that all via plug ink are stored in temperature and humidity control environment? Also, inventoried under FIFO with expired date control?

11.96 Is the date and time that the via plug ink expires after preparation specified on its container?

11.97 Are the screen printers cleaned and maintained to a documented procedure?

11.98 Is blotter paper (screen cleaning absorption paper) used to remove excess ink on the legend & via plugging screens on a 10-20 panel frequency while screening product? Was this frequency based on engineering tests?

11.99	Has the via plug ink curing parameters been established and are they re-verified on a quarterly basis?
11.A0	Is the screen developing performed in a clean area with adequate ventilation?
11.A1	Are the squeegees controlled properly, such as the width, angle, resharpen freq?
11.A2	Are the screen frames routinely inspected for squareness, twisted rails, broken corners and other similar defects that would interfere with properly tensioned screens?
11.A3	Is there a documented closed loop system to verify the silk-screen stencil life cycle is controlled?
11.A4	Are silk-screen stencils identified with labels or plates which are visible when the stencil is in its racks or mounted in the printer
11.A5	Is there a documented requirement to inspect a stencil after it is cleaned?
11.A6	Is the screen tension checked during screen stretching, after develop & prior to use in manufacturing?
11.A7	Are the screens cleaned on a defined frequency?
11.A8	Is there a documented allowable via plugging & legend rework procedure with appropriate quality checks?

TABLE 7.12 Hot Air Leveling Process Audit

Item	Audit Criteria
12.00	Are the Hot Air Leveling processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
12.01	Does evidence exist that process capability studies have been performed for the Hot Air Leveling process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
12.02	Is the overall appearance of the area and equipment condition adequate?
12.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. HAL line, XRF, etc. used to fabricate the product?
12.04	Is there a continuous improvement team in place for the Hot Air Leveling Process Area with documented actions plans?
12.05	Are the laboratory records (i.e. Chemical Analysis, Solder Impurities etc.) for Hot Air Leveling process complete and up to date?
12.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
12.07	Are the calibration labels on critical equipment current?
12.08	Do training records exist for the Hot Air Leveling operators and are they current?
12.09	Do health and safety procedures exist and are they being followed?
12.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Pre-Clean	
12.11	Is there a pre-startup checklist for the preclean lines? Is it current?
12.12	Is there objective evidence that the preclean chemistries are being analyzed by the laboratory on the documented frequency?
12.13	Is the microetch rate monitored? Is it under SPC control with calculated control limits and are the charts & actions current?
12.14	Are Dump and Remake schedules documented for the preclean line and objective evidence exist that they are being adhered too?
12.15	Are the final rinses deionized or RO water?
12.16	Is there evidence to demonstrate that all chemicals are monitored and controlled as listed in WI?
12.17	Are all in-process WIP and materials properly identified and controlled in designate area?
12.18	Is the specific gravity of the flux controlled?
12.19	Is there an evidence to demonstrate that the PCB surface cleanliness is monitored and controlled?

Hot Air Solder Leveling

12.20 Is there a pre-startup checklist for the HASL lines? Is it current(completely filled in)?

12.21 Are all in-process WIP and materials properly identified and controlled in designate area?

12.22 Is a pilot run to set HASL conditions such as Dip-in speed, dwell, withdraw speed, Hot air Temperature and pressure, Knife angle and gap to ensure the required solder thickness for each P/N to fine tune the setting to get uniform tin thickness and minimum plugged vias?

12.23 Is the angle and Gap of air knife verified regularly?

12.24 Is air knife distance checked with V-block as part of start-up checklist?

12.25 Did the supplier perform measurement verification and GR&R for air knife angle and air knife distance?

12.26 Is the Temperature and Pressure of Hot air verified regularly?

12.27 Are panels washed right after HASL to prevent flux drying?

12.28 Did the supplier ilnclude specific gravity and viscosity as flux process control parameters?

12.29 Does the supplier analyze the nickel and copper concentration in tin pot twice per week and establish SPC charts for each element?

12.30 When the nickel conc or copper conc out of spec, does the supplier do alloy adjustment to make sure the nickel and copper conc are within the spec? Do they reanalyze the nickel conc and copper conc after adjustment? Documented procedure and proof of training with sign-off by manufacturing manager?

12.31 Did the supplier document adjusting the alloy to maintain the nickel & copper concentrations within the Nihon specfication? Is there any proof of training with sign-off by manufacturing manager?

12.32 Does the supplier standardize the copper removal frequency? Is the carbonization removed thouroughly? What's the frequency?

12.33 Does the supplier document the air knife replacement frequency based on the production panels? Is the air knife blade smooth and will not impact the tin uniformity after HASL?

12.34 Are panels placed in slotted racks after HASL?

12.35 Did the supplier implement 20-40X stereo microscope inspection methodology for visual inspection for solder uniformity and solder plugged holes?

12.36 Is the lighting at LF HASL inspection area adequate?

12.37 Are the inspectors provided the visual aids for determining preferred and unacceptable uniformity conditions?

12.38 On-site check the LF HASL boards using 20~40X microscope, are the uniformity of tin is acceptable and solder plugged via hole less than 5%?

12.39 Does the supplier monitor one and two pass LF-HASL trends and set one pass 30-day goal of 95%.

12.40 Does the supplier have the log sheet to record the LF HASL parameters setting for each Lot according to the customer's requirement?

12.41 Is solder thickness & composition checked on sampling basis after HASL?

12.42 Does the supplier measure the tin thickness on BGAs, QFP, SMT & 3mm X 3mm pad sizes? Sample size is 5 panels/lot min?

12.43 Does the traveler or other process documentation specify the solder thickness that meets HOLDEN CONSULTING PCB Specification GNTX-7000 criteria?

12.44 Is the solder purity checked and monitored? Is this requirement documented in the standard operating procedure?

12.45 Does the supplier send the solder sample to 3rd party for analysis for the nickel concentration and copper concentration in the solder pot, did they do correlation study with internal analysis? Did the supplier document this? Is there any proof of training with sign-off by manufacturing manager?

12.46 Is the X-ray used for solder thickness measurement? What's the frequency?

12.47 Is there a documented procedure to verify hole size for press-fit and other tight toleranced plated through holes at the HASL operation using pin gages?

12.48 Is there a feedback loop to pre-production engineering to provide hole size data to insure the hole sizes are centered on nominal and have a good Cpk?

12.49 Does the supplier perform 6X thermal stress test and do horizontal & vertical cross-section to verify the hole wall quality?

12.50 Does the supplier check the intermetallic thickness 1/week?

12.51 Have the supplier establish computer system for the LF HASL setting for each P/N?

12.52 Is there objective evidence to demonstrate that the PM's are being performed?

12.53 Are the panels in-time/on line inspected to prevent the volume defect

12.54 Is there a procedure to define the Rework of the defective boards after HASL?

12.55 Does the rework procedure defines the allowed maximum number of passes at 2 or less (first HASL & one re-HASL)?

12.56 Are the customer's fab print requirements for LF HASL copper thickness documented in the traveler and verified by cross section analysis?

12.57 For LF HASL applications, are analysis performed verifying LF HASL deposits are free of lead?

12.58 Are waste treatment manifests filed demonstrating HASL preclean, HASL/LFHASL and post clean chemistries/materials are properly disposed?

Post-Clean

12.59 Is there a pre-startup checklist for the postclean lines? Is it current?

12.60 Is the horizontal cooling system well maintained and set up and the boards can be held up (no scratch on solder surface will be caused)

12.61 Does the supplier add conductivity measurements to final DI rinse water on LF-HASL post treatment line?

12.62 Are the boards rinsed by warm water?

12.63 Are the boards rinsed by High pressure water/scrubbing?

12.64 Are Dump and Remake schedules documented for the postclean line and objective evidence exist that they are being adhered too?

12.65 Are the final rinses deionized or RO water?

12.66 Is there an evidence to demonstrate that the PCB surface cleanliness is monitored and controlled?

TABLE 7.13 OSP Process Audit

Item	Audit Criteria
13.00	Are the OSP processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
13.01	Does evidence exist that process capability studies have been performed for the OSP process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
13.02	Is the overall appearance of the area and equipment condition adequate?
13.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. OSP line used to fabricate the product?
13.04	Is there a continuous improvement team in place for the OSP Process Area with documented actions plans?
13.05	Are the laboratory records (i.e. Chemical analysis, etc.) for OSP process complete and up to date?
13.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
13.07	Are the calibration labels on critical equipment current?
13.08	Do training records exist for the OSP operators and are they current?
13.09	Do health and safety procedures exist and are they being followed?
13.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

OSP

13.11 Does the traveler or other process documentation specify the OSP coating thickness?

13.12 Is the OSP thickness specification per the suppliers recommendation?

13.13 Is the OSP thickness determined per the OSP suppliers recommended procedure?

13.14 Is the OSP thickness verified at start-up and checked twice per shift while processing PCB's?

13.15 Are all in-process WIP and materials properly identified and controlled in designate area?

13.16 Are the chemicals analyzed per supplier recommendation and is SPC implemented where applicable?

13.17 Is there objective evidence that the microetch (microinches of copper) is being performed per the suppliers recommendation? Is it under SPC control?

13.18 What is the max. allowable Cu limit in the microetch?

13.19 Is there objective evidence to demonstrate that the PM's are being performed?

13.20 Is the OSP line free of crystallization build-up?

13.21 Is there an documented squeegee (squeezing) roller inspection and cleaning procedure?

13.22 Is there a documented process to insure that there is no OSP residue present on the gold fingers for all PCB's with G/F connectors?

	Ionic Contamination
13.23	Is ionic contamination testing performed prior to OSP application on the product per the customer's specification?
13.24	Is the ionic contamination test frequency being performed at a minimum of once per lot?
	Quality Inspections
13.25	Are the latest visual inspection work instructions with defect photos posted for operator use?
13.26	Are visual inspections being performed using 1.75× magnification per IPC-A-600 and verifications being performed at 30× magnification?
13.27	Is 100% visual inspection being performed?
13.28	Is the plated copper thickness verified after the OSP operation?
13.29	Are random samples pulled to verify the presence of OSP before they are packaged?
	Rework
13.30	Is there a documented allowable rework procedure based on the OSP process supplier recommendations?
13.31	Are the OSP re-coats limited to only one complete cycle through the OSP line?
13.32	Are all repaired boards identified for traceability?
13.33	Is testing performed after all rework to validate conformance to HOLDEN CONSULTING PCB Specification requirements?
13.34	Is the Cu thickness in PTHs validated as part of the testing after rework to ensure no issues due to additional exposure to microetch chemistries?

	Handling
13.35	Have standard handling procedures been established based on OSP supplier handling requirements and put on-site for operator use?
13.36	After OSP coating, are all output boards protected by sulfur free slit paper?
13.37	Are the boards kept in a non-corrosive environment after the application of OSP while still in the manufacturing facility?
13.38	Is there a documented maximum hold time for unpackaged OSP boards?
13.39	Are the operators wearing gloves to help prevent tarnish when handling boards after ImAg has been applied?
13.40	Are the PCBs handled by the edges?
	OSP Packaging
13.41	Does the OSP finished PCBs packaging conform to the standards and procedures provided by the OSP process supplier?
13.42	Is the OSP finished PCBs using vacuum packaging?
13.43	Have all packaging materials (including slip sheets if used) been verified sulfur-free?
13.44	Are the sealed packages stored below 86°F (30°C)?
13.45	Since dessicants can contain sulfur, are they not used in packing the OSP PCBs?
13.46	Since rubber bands, adhesive tapes, labels, stamps can contain sulfur, are they not used on packing materials or boards?

TABLE 7.14 Final Fabrication Process Audit

Item	Audit Criteria
14.00	Are the FAB processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
14.01	Does evidence exist that process capability studies have been performed for the FAB process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
14.02	Is the overall appearance of the area and equipment condition adequate?
14.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. rout & scoring machines, etc. used to fabricate the product?
14.04	Is there a continuous improvement team in place for the FAB Process Area with documented actions plans?
14.05	Are the laboratory records (i.e. Chemical analysis, etc.) for the process complete and up to date?
14.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
14.07	Are the calibration labels on critical equipment current?
14.08	Do training records exist for the FAB operators and are they current?
14.09	Do health and safety procedures exist and are they being followed?
14.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Routing
14.11	Is the routing program checked prior to being released to production?
14.12	Are panels fixtured with locked pins during routing?
14.13	Are all in-process WIP and materials properly identified and controlled in designate area?
14.14	Is first article dimension checked on the bottom panel from each spindle before production start-up and on each subsequent rout machine setup?
14.15	Is stack height controlled properly based on pinning and abrasive used?
14.16	Is there evidence to demonstrate that all routing bits, V-cut/Beveller knives are well controlled? Such as the life control?
14.17	Is mechanical dimension PCB specification available at inspection station under document control?
14.18	Is there evidence to demonstrate that V-cut depth and board dimension are well controlled?
14.19	Is there process documentation in place to identify the customer's V-groove requirements? Is it verified during setup and lot inspection?
14.20	Are output boards at the bottom of each spindle inspected the dimension?

TABLE 7.15 Electrical Test Process Audit

Item	Audit Criteria
15.00	Are the Electrical Test processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
15.01	Does evidence exist that process capability studies have been performed for the Electrical Test process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
15.02	Is the overall appearance of the area and equipment condition adequate?
15.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. Test Fixture, Tester, Operator, etc. used to fabricate the product?
15.04	Is there a continuous improvement team in place for the Electrical Test Process Area with documented actions plans?
15.05	Are the laboratory records (i.e., etc.) for the process complete and up to date?
15.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
15.07	Are the calibration labels on critical equipment current?
15.08	Do training records exist for the Electrical Test operators and are they current?
15.09	Do health and safety procedures exist and are they being followed?
15.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Electrical Test
15.11	Are boards separated in a fool proof manner after test to avoid mixing passed and failed boards?
15.12	Are temperature and humidity monitored to optimized test conditions?
15.13	Are all in-process WIP and materials properly identified and controlled in designate area?
15.14	Does the test fixture passed the incoming inspection before they are used?
15.15	Are the tools and fixtures associated with P/N and REV clearly identified?
15.16	Is full open and full short test by Aluminum foils and back up routinely before testing every shift?
15.17	Are all open/short test machine grounded?
15.18	Is testing machine having self-check function before each shift machine start-up?
15.19	Is there procedure in place that clearly defines the ET fixture set up? Is there objective evidence that it is followed?
15.20	Are the test fixtures for the product capable of simultaneously contacting all assigned points? No flip testing allowed.
15.21	Are the tools and fixture checked at the start of each shift?
15.22	Is Debug performed in an isolated area to avoid mixing passed and failed boards?
15.23	Are boards re-tested after verification?
15.24	Are repaired PCB's subjected to a complete electrical test after repair?
15.25	Are false defect rate tracked with defined target?
15.26	Are the PCBs properly identified by their P/N, status, and traceability information?
15.27	Are all passed/rejected boards properly labeled and segregated to avoid mixing or missing?
15.28	Is the 100% electrical test requirement documented and performed per customer specification?
15.29	Are the electrical testers capable of testing open circuit resistance threshold of 10 ohms as described in the customer specification?
15.30	Are the electrical testers capable of testing isolation resistance threshold of at least 10 Megaohms with a voltage of at least 100 volts as described in the customer specification?
15.31	Do the electrical testers have a means of limiting the energy delivered to failing (shorted) networks so that tested products are not damaged?
15.32	Is the open and short repair procedures documented and operators trained and certified?
15.33	Is the same S/M material used for touch-up & repair as was originally coated on the PCB?
15.34	Are the soldermask touch-ups tape tested?
15.35	Is there documentation that identifies traces that can and cannot be repaired?
15.36	Is the baking oven well calibrated?
15.37	Are the passed boards marked properly with an electrical test stamp?
15.38	Are the electrical test equipment capabilities evaluated regularly?
15.39	Is the Dielectric Withstanding voltage 500V AD/DC +0.15/−0 for spacing over .003 in and 250V AC/DC +0.15/-0 for spacing under .003 in?

TABLE 7.16 Final Inspection/Impedance Process Audit

Item	Audit Criteria
16.00	Are the Final Inspection processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
16.01	Does evidence exist that process capability studies have been performed for the Final Inspection process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
16.02	Is the overall appearance of the area and equipment condition adequate?
16.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and inspectors?
16.04	Is there a continuous improvement team in place for the Final Inspection Area with documented actions plans?
16.05	Are the laboratory records for Final Inspection Certificates of Conformance & FAI's complete and up to date?
16.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
16.07	Are the calibration labels on critical equipment current?
16.08	Do training records exist for the Final Inspection operators and are they current?
16.09	Do health and safety procedures exist and are they being followed?
16.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Final Inspection	
16.11	Are customer specifications readily accessible, clearly legible, and understood in the inspection area?
16.12	Are inspection stations equipped with magnified ring lights or stereo microscopes (10× min)?
16.13	Is there adequate lighting in the inspection area and at inspection stations?
16.14	Do the final QC inspectors have access to 40× magnification or greater for defect verification?
16.15	Are all in-process WIP and materials properly identified and controlled in designate area?
16.16	Is there a workmanship standard for touch up of final QC?
16.17	Is there the standard handling work instruction put on site? Are the inspectors handling the board properly to avoid damage or mixing?
16.18	Is there a nonconforming procedure that clearly define the disposition of nonconforming boards?
16.19	Are all of the nonconforming boards sufficiently segregated and identified?
16.20	Is there a documented system to track the performance i.e. number of inspection escapes to the customer for each inspector? If the inspectors performance is poor, is there any re-training or job transition?
16.21	Are previous quality issues and customer complaints highlighted in inspection records for a given part number?
16.22	Is there a feedback loop to pre-production engineering to provide hole size data to insure the hole sizes are centered on nominal and have a good Cpk?
16.23	Are inspection tools/gages (pin gages, calipers, etc) and test equipment on a defined calibration frequency? Does objective evidence exist that it is being performed?
16.24	Are the rejected PCB properly identified by their P/N, reject status, and reject information?
16.25	Does the final QC documentation have inspection guidelines for soldermask interface attack (SMIA) and have the operators been trained to identify this defect?
16.26	Are requirements documented, procedures established and methods adhered too for soldermask repairs?
16.27	Is the same S/M material used for touch-up & repair as was originally coated on the PCB?
16.28	Are all in-process and final inspection reworks and touch-ups cross checked by final QC inspectors?
16.29	Are soldermask touchups adhesion tape tested per IPC (IPC-TM-650, Method 2.4.28.1)?

	Impedance Test
16.30	Are controlled impedance boards/coupons tested in accordance with customer's spec and drawing?
16.31	Is there a documented system in place to convey the customer's impedance measurement requirements on the PCB fab drawing?
16.32	Is the impedance equipment separated in ESD room so that there is no influence on test?
16.33	Are all in-process WIP and materials properly identified and controlled in designate area?
16.34	Is there a work instruction for impedance test?
16.35	Are TDR probes inspected regularly for wear and replaced as needed? Are the machines calibrated periodically?
16.36	Is the impedance equipment utilized have accuracy, repeatability and reproducibility of 10% or less of the impedance range being verified?
16.37	Are impedance measurement records maintained for a minimum of two years?
16.38	Is the impedance test using automated fixture?

TABLE 7.17 Laboratory Process Audit

Item	Audit Criteria
17.00	Are the Laboratory Procedures documented and are the latest revision Work Instructions, PM, Calibration, Inspection procedures and all wet and dry lab procedures in place for the laboratory technicians to follow?
17.01	Does evidence exist for process capability for the Packaging & OBE processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
17.02	Is the overall appearance of the area and laboratory equipment condition adequate?
17.03	Does lot traceability exist that permits tracking the O/L lot and to all major equipment and materials i.e., etc. used to fabricate the product?
17.04	Is there a continuous improvement team in place for the Laboratory Area with documented actions plans?
17.05	Are the laboratory records (i.e. Cross-sections for hole roughness, etc.) for the process complete and up to date?
17.06	Are the technician and Maintenance PM's documented and objective evidence exist that they are performed?
17.07	Are the calibration labels on critical equipment current and current?
17.08	Do training records exist for the Laboratory Technicians and are they current?
17.09	Do health and safety procedures exist and are they being followed?
17.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?
	Cross-Section Laboratory
17.11	Are the requirements documented, procedures established and methods adhered too for microsection evaluations?
17.12	Is there a documented system for customer fab drawing requirements (dielectric thickness, copper weights, surface copper, plating thickness, etc.) for microsection verification?
17.13	Is there a formal system to provide feedback to Product Engineering, Process Engineering and Operations for microsection failures?
17.14	Are structural integrity microsection coupons prepared per IPC-TM-650, Method 2.1.1 or 2.1.1.2 with acceptability verified per IPC-6012, Class 2?
17.15	Are thermal stressed samples prepared for microsection coupon per IPC-TM-650, Method 2.6.8 and microsectioned per IPC-TM-650, Method 2.1.1.2 with acceptability verified per IPC-6012, Class 2?
17.16	Is the structural integrity verified at 1X and 3X thermal shocks?

17.17	Are thermal stressed microsection performed at the rate of at least one coupon per 100 customer panels produced?
17.18	Is the temperature verified on the solder pot before coupons are thermal stressed?
17.19	Is the microscope measurement system validated against a standard daily before microsection measurements?
17.20	Has a Gage R & R been performed on the microsection measurement system?
17.21	Are microsection coupons retained for six months with an adequate index system for locating archived microsections?
17.22	Are the archived microsection coupons and documents traceable to manufacturing lots and shipping lots?
17.23	Is there a system in place to archive microsection results and coupons for six months?
17.24	Are plating adhesion tests performed per IPC-6012, Class 2 Section 3.3.7 at the customer's prescribed frequency?
17.25	Are solderability test performed per IPC-6012, Class 2 and method D of J-STD-003, Category 2?
17.26	Are solderability test samples archived for six months?

Reliability & Wet Laboratory

17.27	Is there a documented analytical sampling plan with a closed loop system to insure that all chemical analysis are performed per either the laboratory procedure or manufacturing SOP?
17.28	Is there a documented traceable closed loop system to insure that identified adds to wet processes are made?
17.29	Have guard band limits been established for all critical process chemistries to insure chemical processes stay in control between analysis?
17.30	Is there a documented procedure to make chemical adds based on action limits to prevent chemistries from going outside the specification limits between analysis?
17.31	Are chemical process Cpk reports for critical chemistries generated, monitored and have continuous improvement plans for any Cpk less than 1.5?
17.32	Is there a system in place to monitor chemical reagent expiration date?
17.33	Is there an archived traceable system to find historical analytical results for all chemical laboratory analysis?
17.34	Are the analytical reagents certified standards or are they verified against known standards?
17.35	Are the analytical instruments standardized against know standards prior to performing chemical analysis?
17.36	Are all tests performed in a safe manner with proper protective gloves, face shield, clothing and ventilation?
17.37	Is S.I.R testing performed at least once per quarter on inner layers after oxide, prior to soldermask and after finishing (each soldermask type)?

TABLE 7.18 Waste Treatment & Chemical Storage Process Audit

Item	Audit Criteria
18.00	Are the waste treatment procedures, purified water (deionized or reverse osmosis) and chemical storage procedures documented and are the latest revision Work Instructions, PM, Calibration, Inspection procedures & all wet lab procedures in place for the laboratory technicians to follow?
18.01	Does evidence exist that the Waste Treatment processes have been characterized and the capabilities and treatment capacities are fully understood and documented?
18.02	Is the overall appearance of the area and waste treatment equipment condition adequate?
18.03	Are the waste treatment discharge records traceable to dates treated and treatment equipment?
18.04	Is there a continuous improvement team in place for the Waste Treatment operation with documented actions plans?
18.05	Are the laboratory records for waste treatment process complete and up to date?
18.06	Are the waste treatment technician/operators and maintenance PM's documented and objective evidence exist that they are performed?

18.07 Are the calibration labels on critical equipment current and current?

18.08 Do training records exist for the Waste Treatment Technicians/Operators and are they current?

18.09 Do health and safety procedures exist and are they being followed?

18.10 Have standard chemical handling procedures been established and put on-site for the operators to follow? Are the operators wearing appropriate safety equipment while handling chemicals or waste?

Chemical Storage

18.11 Are bulk storage tanks located in area that has adequate containment for spills?

18.12 Are bulk storage tanks connected to segregated waste streams to avoid cross contamination, noncompatible chemicals from coming into contact with each other and contamination of the environment?

18.13 Is there a system in place to monitor the level (quantity) in the bulk tanks to insure additional chemistry is ordered to prevent running out?

18.14 Are bulk chemicals analyzed or certifications verified before pumping from the delivery tanker into the bulk storage tank?

18.15 Are drummed chemicals stored in a warehouse with temperature control and stored per the chemical suppliers recommendation?

18.16 Are drummed chemicals labeled with a legible label with adequate information to insure that the appropriate chemical is issued to the floor when a request is submitted?

18.17 Are drummed chemicals stored in a warehouse utilizing a first-in first-out system?

18.18 Are drummed chemicals managed under inventory control to insure that additional chemistries are ordered in time to prevent running out?

18.19 Are there documented water quality levels established for the deionized water and/or reverse osmosis water systems?

18.20 Are there established maintenace schedules for the deionized or reverse osmosis systems based on water quality (purification) levels?

18.21 Is there a documented system for the deionized water and/or reverse osmosis water systems to insure water quality levels are maintained?

18.22 Are drummed chemicals managed under inventory control to insure that additional chemistries are ordered in time to prevent running out?

	Waste Treatment
18.23	Are all hazardous chemical manufacturing process waste streams segregated (i.e. chelated metals, etc.) and processed through the waste treatment operation before discharging to the environment?
18.24	Do the hazardous chemical process equipment equipped with containment vessels to help control/manage spills and are they piped to the appropriate waste stream for the waste treatment operation?
18.25	Are there documented reaction plans in place for spills in the manufacturing areas to insure the waste treatment treating capacity is not exceeded and resulting in an discharge excursion?
18.26	Are the waste streams analyzed to confirm conformance to governmental treated waste regulatory requirements?
18.27	Are waste treatment discharge levels reviewed by upper management during operation reviews?
18.28	Is there a documented reaction plan for waste treatment excursions that exceed internal and external (governmental) regulatory requirements?
18.29	Are hazardous waste and spent solids removed from the premises by government approved agencies or licensed companies?
18.30	Is waste water treatment in accordance with government standards?
18.31	Are records of compliance to government standards for waste water current?
18.32	How often is the waste water tested? Does the company check this regularly or wait for the government agency to test the waste water?
18.33	Are all manifests and transactions records of hazardous waste and spent solids removal current?
18.34	Are hazardous waste and spent solids picked up on a scheduled basis or an "on-call" basis?
18.35	Have any of the waste streams exceeded governmental regulatory requirements in the past twelve months?
18.36	Is there a waste minimization project team in place with active actions?

TABLE 7.19 Packaging & OQA Process Audit

Item	Audit Criteria
19.00	Are the Packaging & OBE processes documented and are the latest revision Work Instructions, Calibration & Inspection procedures for all processes in place for operators to follow?
19.01	Does evidence exist for process capability for the Packaging & OBE processes i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
19.02	Is the overall appearance of the area and equipment condition adequate?
19.03	Does lot traceability exist that permits tracking the O/L lot and to all major equipment and materials i.e., etc. used to fabricate the product?
19.04	Is there a continuous improvement team in place for the Packaging & OBE Process Area with documented actions plans?
19.05	Are the laboratory records (i.e. Cross-sections for hole roughness, etc.) for Packaging & OBE process complete and up to date?
19.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
19.07	Are the calibration labels on critical equipment current?
19.08	Do training records exist for the Packaging & OBE operators and are they current?
19.09	Do health and safety procedures exist and are they being followed?
19.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

	Packaging
19.11	Is the work instruction for packaging in place and under document control?
19.12	Are lots properly separately part number to avoid mixing parts during packaging?
19.13	Are parts vacuum packaged?
19.14	Are proper methods used to prevent moisture absorption?
19.15	Are weight restriction defined for boxes?
19.16	Are customers requirements for packaging accessible?
19.17	Does the suppliers have bar code capability?
19.18	Are boxes properly labeled on outside with date code, qty, x-out, inspection reports?
	Outgoing Quality Audit (OQA)
19.19	Is there an inspection Instruction for the specific product being audited?
19.20	Is the sampling plan set with consideration of existing outgoing quality level and target?
19.21	Is the OQA defective level tracked as an index to predicted the outgoing quality level?
19.22	Does the OQA test and inspection has good coverage? Such as check the packaging, labeling, quality of PCB and the attachments etc?
19.23	Do all units of the reject lot go through all the final test and inspection, and not just for the failed test and inspection?
19.24	Are the rejected PCB properly identified by their P/N, reject status, and reject information?
19.25	Is CAR issue for the failure found?

TABLE 7.20 Electroless Nickel/Immersion Gold Process Audit

Item	Audit Criteria
20.00	Are the Electroless Nickel—Immersion Gold processes documented and are the latest revision Work Instructions, PM, Calibration & Inspection procedures for all processes in place for operators to follow?
20.01	Does evidence exist that process capability studies have been performed for the Electroless Nickel—Immersion process i.e. processes characterized, critical parameters identified, FMEA, SPC, gage R&R, and Cp & Cpk reporting?
20.02	Is the overall appearance of the area and equipment condition adequate?
20.03	Does lot traceability exist that permits tracking the O/L lot number to all major equipment and materials i.e. Plating line, XRF, etc. used to fabricate the product?
20.04	Is there a continuous improvement team in place for the Electroless Nickel—Immersion Gold Process Area with documented actions plans?
20.05	Are the laboratory records (i.e. Chemical analysis, cross-sections, etc.) for Electroless Nickel—Immersion Gold process complete and up to date?
20.06	Are the operator and maintenance PM's documented and objective evidence exist that they are performed?
20.07	Are the calibration labels on critical equipment current?
20.08	Do training records exist for the Electroless Nickel—Immersion Gold operators and are they current?
20.09	Do health and safety procedures exist and are they being followed?
20.10	Have standard handling procedures been established and put on-site for the operators to follow? Are the operators wearing gloves when handling product?

Electroless Nickel/Immersion Gold (ENIG)

20.11 Has the ENIG chemical supplier audited and approved process. Provide date of last audit?

20.12 Is there a pre-startup checklist for the plating line(s)? Is it current (completely filled in)?

20.13 Is the line an automated with an established timeway?

20.14 Is there objective evidence that the chemistries are being analyzed by the laboratory on the documented frequency?

20.15 Are all in-process WIP and materials properly identified and controlled in designate area?

20.16 During production runs, are additional checks of controllers, pumps, bath levels, temperatures, agitation, and rinses performed every two hours?

20.17 Are the chemical controls based on the process chemistry suppliers TDS?

20.18 Are the rinses DI water? Clean and algae free?

20.19 Are the maximum nickel and gold bath turnover before dump documented? Does objective evidence exist?

20.20 Is a first article checked performed on the first basket or rack to confirm process parameter to insure meeting nickel and gold thickness and other quality parameters?

20.21 Are liners, or anodic protection used in the nickel & gold bath?

20.22 Is the maximum idle time at temperature established for the plating line?

20.23 Is air agitation used in critical tanks i.e. microetch, rinses, nickel bath?

20.24 Is the microetch rate monitored on a daily basis?

20.25 Is the nickel tank on an automatic controller and do controller calibration records exist?

20.26 Is the stabilizer added separately to the electroless nickel bath?

20.27 Are the process rack/baskets coating in good condition, free of plate-up and on an documented recoating schedule?

20.28 Is there a documented quality conformance procedure with accept/reject criteria for gold finger plating line malfuctions(chemistries out of spec. time, temperature, etc. interuptions) to insure the quality of the product in the plating line?

20.29 Does the traveler or other process documentation specify the Nickel/Gold thickness?

20.30 Is the nickel and gold plating rates documented and objective evidence exist that they are being monitored?

20.31 Is rework performed for ENIG? If so, what type of rework?

20.32 Is the IPC tape test performed on each lot for plating adhesion?

20.33 Are the customer specific ENIG thickness requirements documented on the traveler?

20.34 Are the XRF calibration records current and are appropriate XRF standards used to verify calibration?

20.35	Is X-ray measurement for Au/Ni/thickness performed on every production rack?
20.36	Are the deposition rates microinches/minute for the nickel & gold plating calculated and confirmed to meet the chemical supplier's recommended deposition rate each shift?
20.37	Is the solderability test being performed per J-STD-003, Category 2 to evaluate surface and hole solderability per IPC 6012 class 2 requirements?
20.38	Is the solderability test frequency being performed at a minimum of once per lot?
20.39	Have interactive influences for corrosion of nickel & gold peel been studied and findings implemented? Identify black pad precautions taken.
20.40	Have critical process parameter been identified on SPC and Cpk values monitored?
20.41	Is there a documented shutdown procedure for the entire plating line(s) that includes the critical steps for the nickel plating bath (temperature & nickel controller flushing)?

TABLE 7.21 Maintenance Process Audit

Item	Audit Criteria
	Equipment Maintenance
21.00	Is there a documented maintenance schedule for all critical equipment?
21.01	Do the maintenance records indicte the maintenance is being performed at the documented frequency?
21.02	Is there a closed-loop system to verify the maintenance occurs on the prescibed frequency?
21.03	Is there a valid spare parts inventory control system?
21.04	Are key spare part components identified and replenishment min/max. levels established?
21.05	Are worn/used parts disposed of properly to ensure they are not re-used?
	D.I. Water Maintenance
21.06	Are sand bed pre-filters used before Activated Carbon, RO and/or Ion-Exchange filters?
21.07	Is there a scheduled frequency to replace the media?
21.08	Is there an Activated Carbon prefiltration to block bacteria from entering the main filtration system?
21.09	Is an RO system or ion-exchanger used to prefilter the water before mixed bed or resin polishers?
21.10	Is there a scheduled frequency to service the RO or ion-exchange units?
21.11	Is the DI water resistivity electronically monitored? M ohms or u-Siemens?
21.12	Is D.I. Water process rating acceptability at (4)18 to 15 meg, (3)15 to 10 meg, (2)10 to 5 meg or (1-0)less? Or in micro Siemens: (4).055 to .065 uS, (3).065 to .100 uS, (2).100 to .200 uS, greater?
21.13	At what resistance is an emergency filter change required? Less than 5Meg? Greater than .200uS?
21.14	Is there an Ultra-Violet final filtration to kill bacteria, which may be growing in the DI filter system, and prevent live bacteria from entering the factory DI water plumbing system?
21.15	How often is the factory plumbing (DI water pipes) cleaned to remove/purge algae? Is this maintenance on a scheduled basis? Semi-Annual or Annual?
21.16	Is the status of DI water plumbing cleanliness (bacteria & algae level) verified by TSS (total suspended solids) testing? Is this test performed on a monthly or semi-annual basis? Most TDS (total disolved solids) can be detected by resistivity meter, but is TDS tester also utilized to detect PPM?
21.17	At what TSS level is an emergency Plumbing System Cleaning required?
21.18	Is the Plumbing System Cleaned with H_2O_2 and peracitic acid? Other?
21.19	Are all water pipes throughout the factory labeled DI (for de-ionized water) and CITY or CW (for city water)?
21.20	Do all DI water rinse processes have resistivity meters at the input to the equipment?

Sourcing teams or suppliers can use the in-depth audit questions provided in each focus area to

- Troubleshoot PCB fabrication processes
- Eliminate special causes of variability
- Quickly identify areas for process improvement that will significantly reduce the likelihood of nonconforming product

The questions can be submitted as a written questionnaire, but it's generally much more effective to conduct an on-site audit of the suspect processes, ideally by a senior process engineer with expertise in PCB fabrication.

7.5 TESTING AND INSPECTION

Sound processes that are well managed are more likely to consistently produce good parts and minimize nonconformance, but testing nevertheless plays an important role in electronics manufacturing. Generally, it's better to insist that suppliers perform this testing on behalf of the customer rather than ship PCBs or PCAs for incoming inspection and disposition at the customer's site.

Suppliers are able to conduct testing and visual inspection at different stages of production. The sourcing team needs to consider *what specific testing is necessary* to support the overall quality strategy, and *how many parts should be tested* (the sampling frequency).

7.5.1 Testing and Inspection Commonly Performed at Suppliers

7.5.1.1 Incoming

- Lot check and inspection of incoming materials, chemicals, and components to verify what was ordered from their own suppliers
- Visual inspection of copper-clad laminate for physical damage, such as dents, scratches, or discoloration
- Inspection and verification of electrical test fixtures

7.5.1.2 In-process

- Automated optical inspection (AOI) for imaging artwork, finished innerlayers, and finished laminate after outerlayer processing to verify dimensions of etched features
- Visual inspection of laminated panels for physical damage, dents, scratches and other imperfections
- Visual inspection of hole positional accuracy, hole size, hole quantity, hole location, and surface appearance after drilling
- Backlight inspection of electroless copper coverage
- Visual inspection of soldermask coverage
- Visual inspection of solder uniformity and solder plugged holes after hot air leveling
- Visual inspection of solder joints after reflow and wave soldering

7.5.1.3 Outbound

- Coordinate measuring machine—measurements of critical dimensions and locations relative to datum
- Continuity testing (“opens and shorts”)
- Functional testing of PCAs using dedicated test fixtures
- Visual inspection versus workmanship standards, such as IPC-A-600 Acceptance of Printed Wiring Boards
- Controlled impedance measurements using time-domain reflectometry
- Inspection of cross-sections to check dielectric thickness or plating thickness

- Other destructive analysis and reliability testing, following procedures in IPC-TM-650, Test Methods Manual
- Cross-sections and x-ray analysis of solder joints

The sourcing team should review the standard test and inspection processes that are routinely conducted at the supplier, and review with internal engineering and quality teams to decide whether those processes will provide adequate coverage, particularly for the CPPs. The customer can certainly specify additional product-specific testing and inspection, either on finished boards or test coupons. If requested, inspection reports should be available from the supplier for each lot or work order.

The other decision that the sourcing team needs to make is the sampling frequency for supplier PCB/PCA testing or inspection. The team can insist on 100 percent inspection for in-process panels and boards; however, outbound audits that require destructive analysis of boards can add significant cost without improving quality. A common approach is to randomly select a small sample of boards for audit testing, based on acceptable quality level (AQL) tables (see Table 7.22). These tables provide the size of a random sample for a given lot size and desired quality level, and the maximum number of defects permitted in that sample in order to accept the lot.

TABLE 7.22 AQL Table Example

Lot size			Inspection Level		
			I	II	III
2	To	8	A	A	B
9	To	15	A	B	C
16	To	25	B	C	D
26	To	50	C	D	E
51	To	90	C	E	F
91	To	150	D	F	G
151	To	280	E	G	H
281	To	500	F	H	J
501	To	1200	G	J	K
1201	To	3200	H	K	L
3201	To	10000	J	L	M
10001	To	35000	K	M	N
35001	To	15000	L	N	P
		0			
150001	To	50000	M	P	Q
		0			
500001	and	over	N	Q	R

Code letter	Sample size	Acceptable quality level: 1.0%	1.5%	2.5%	4.0%	6.5%
A	2	0	0	0	0	0
B	3	0	0	0	0	0
C	5	0	0	0	0	1
D	8	0	0	0	1	1
E	13	0	0	1	1	2
F	20	0	1	1	2	3
G	32	1	1	2	3	5
H	50	1	2	3	5	7
J	80	2	3	5	7	10
K	125	3	5	7	10	14
L	200	5	7	10	14	21
M	315	7	10	14	21	21
N	500	10	14	21	21	21
P	800	14	21	21	21	21
Q	1250	21	21	21	21	21
R	2000	21	21	21	21	21

Maximum number of defects allowed

Inspection Levels:

- Level I: High confidence in supplier
- Level II: Default
- Level III: Low confidence in supplier

Lot size = 400, Inspection Level II -> Code H
Sample size = 50, Maximum of 3 defects for AQL of 2.5%

7.6 INCOMING INSPECTION

As mentioned above, it's better to identify nonconforming PCBs or PCAs at the supplier rather than at the receiving end. This means that only boards that pass testing and inspection are shipped to the customer, and any nonconforming boards can be immediately analyzed for root cause and dispositioned at the supplier. Note that there may be exceptions where specialized testing can only be performed at the customer site, for example if other elements of the final product are required to verify system functionality.

Chapter 8 describes the recommended procedures for qualifying a supplier for a specific part number and authorizing production. After the supplier has been approved for the part number, incoming inspection at the customer site can be reduced to a low-frequency audit as a confidence check of the supplier's overall quality system. If failures are found at incoming inspection, the sourcing team can recommend the following actions:

- Increase the frequency of incoming inspection at the receiving end until the supplier has demonstrated quality improvement. Use Inspection Level III in Table 7.22 as a guide.
- Meet with the supplier to review the defective boards, and return the boards to the supplier for root cause analysis and corrective action.
- Conduct a follow-up audit of the supplier's quality system, focusing on process management in the production areas that are implicated in the root cause analysis.
- Add more testing or increase the frequency of testing at the supplier, but only as a temporary measure. Improved quality comes from improved processes, not more testing.

- Consider passing the cost of the additional incoming inspection back to the supplier, if this is permitted in the terms and conditions of the supplier contract.

A decline in the quality performance from an approved supplier should also be addressed at regular business reviews with supplier management. Chapter 8 provides more details on this topic.

CHAPTER 8

PRODUCT ACCEPTANCE AND FEEDBACK

Tim Rodgers
University of Colorado, Boulder, Colorado

8.1 INTRODUCTION

The previous chapters in this part include processes and recommendations for determining the criteria that should be used to evaluate and select printed circuit board (PCB) or printed circuit assembly (PCA) suppliers, qualifying these suppliers, and monitoring their performance. This final chapter provides guidelines for design qualification, lot acceptance, and ongoing inspection of received boards and assemblies. It also gives some suggestions for long-term supplier management that minimizes the customer's internal expenses while maintaining a high level of supplier performance.

8.2 DESIGN QUALIFICATION

Chapter 6, “Supplier Selection and Qualification,” describes a general process for selecting a PCB or PCA supplier and adding them to an approved vendor list (AVL). Most companies establish guidelines for purchasing that favor AVL suppliers, including special approvals that are required in order to use a supplier that is not on the AVL. Some customers may consider a supplier on the AVL to be automatically qualified to build any design ordered by the customer. This general or “blanket” qualification would be based on the information and performance data collected during the initial supplier evaluation and selection process.

However, if the technology or quality requirements for a new design are significantly different or more challenging, the sourcing team should consider a design qualification process to verify that the approved supplier can meet the new requirements. Design-specific qualification is less risky, but it requires fabricating and inspecting additional boards, usually referred to as first articles, before authorizing full production at the supplier. Note that a customer can decide to accept first articles as incoming material if they pass inspection. The sourcing team can require design qualification for each new design, but if the new design is not significantly different they may choose to waive this requirement. Table 8.1 compares the pros and cons of general versus design qualification.

TABLE 8.1 Comparison of Product Qualification Strategies

	Pros	Cons
General Qualification (applies to all boards and assemblies)	• Based on information already collected during supplier assessment and selection processes • Eliminates delays and costs due to additional qualification testing and inspection	Risk of supplier using non-standard processes and special handling that does not represent actual production conditions
Part Qualification only for new technology	Focuses qualification activities on higher risk technology not previously used (e.g., new materials and processes)	Additional time and expense for qualification testing and inspection
Part Qualification for each new part number or design	Lowest risk	Additional time and expense for qualification testing and inspection

	Pros	Cons
First article inspection (FAI) as a separate order before authorizing production	Higher confidence that subsequent production will meet customer requirements	• Additional expense for separate order, although boards that pass may be approved for use • Risk of supplier using non-standard processes and special handling that does not represent actual production conditions
FAI using a sample of boards from the first production lot	• Boards that pass FAI can be immediately used in production • Standard production conditions at the supplier	If the lot is rejected at inspection, significant delays until corrective action is implemented

The benefit of first article inspection (FAI) before approving production is based on the assumption that the samples provided by the supplier are representative of the fabrication processes that will be used for later purchase orders. It’s important that the sourcing team makes this clear to the supplier. Any special handling of the FAI order or nonstandard processing can render the results meaningless because any subsequent production orders may not follow these same processes.

The number of boards in the FAI order depends on the level of confidence required to proceed. The AQL table in Table 8.2 provides a useful guide for selecting a sample size given the quality level and maximum number of defective boards permitted.

TABLE 8.2 AQL Table Example

Lot size			Inspection Level		
			I	II	III
2	To	8	A	A	B
9	To	15	A	B	C
16	To	25	B	C	D
26	To	50	C	D	E
51	To	90	C	E	F
91	To	150	D	F	G
151	To	280	E	G	H
281	To	500	F	H	J
501	To	1200	G	J	K
1201	To	3200	H	K	L
3201	To	10000	J	L	M
10001	To	35000	K	M	N
35001	To	15000	L	N	P
		0			
150001	To	50000	M	P	Q
		0			
500001	and	over	N	Q	R

Code letter	Sample size	1.0%	1.5%	2.5%	4.0%	6.5%
A	2	0	0	0	0	0
B	3	0	0	0	0	0
C	5	0	0	0	0	1
D	8	0	0	0	1	1
E	13	0	0	1	1	2
F	20	0	1	1	2	3
G	32	1	1	2	3	5
H	50	1	2	3	5	7
J	80	2	3	5	7	10
K	125	3	5	7	10	14
L	200	5	7	10	14	21
M	315	7	10	14	21	21
N	500	10	14	21	21	21
P	800	14	21	21	21	21
Q	1250	21	21	21	21	21
R	2000	21	21	21	21	21

Acceptable quality level

Maximum number of defects allowed

Inspection Levels:

- Level I: High confidence in supplier
- Level II: Default
- Level III: Low confidence in supplier

Lot size = 400, Inspection Level II -> Code H

Sample size = 50, Maximum of 3 defects for AQL of 2.5%

A popular alternative to inspecting a separate order of first articles is to take a sample of boards from the first lot received, again using Table 8.2. This ensures that the boards used to approve production came from the same fabrication processes. However, this is a risky approach. If defects are found during inspection, this could mean discarding or reworking the entire order, and delaying subsequent production until corrective action is taken and a new shipment is received.

8.3 INCOMING INSPECTION AND LOT ACCEPTANCE

Chapter 7, “Process Control, Monitoring, and Incoming Inspection,” explains how to assess a supplier’s production processes and identify opportunities for improvement that will help reduce or possibly eliminate the need for incoming inspection. While it may be a useful check of quality performance when the customer has little experience with a new supplier, incoming inspection adds time and expense on the customer side. It also creates a lengthy feedback loop for any failures or discrepancies. It’s much better to “drive quality upstream” and insist on defect prevention through stable and robust processes, and early defect detection through in-process checks.

If the sourcing team decides to conduct incoming inspection on a short-term basis to determine whether to accept a lot of boards, the sampling plan provided in Table 8.2 is recommended. The table on the right shows the maximum number of defects that are permitted in the sample in order to achieve the required quality level. If more than that number of defects is found, then the entire lot should be rejected, and the supplier should be notified immediately to initiate a corrective action plan (see below).

Note that incoming inspection should be focused on the critical performance parameters (CPPs) previously identified by the engineering and production teams.

Boards that are rejected at incoming inspection, or elsewhere in subsequent processing or testing at the customer site should be immediately segregated from other boards in a separate physical location so they cannot be used in production. The recommended procedure is to use a cross-functional *material review board (MRB)* to regularly inspect segregated boards to determine an appropriate disposition. Figure 8.1 provides an overview of a typical MRB process.

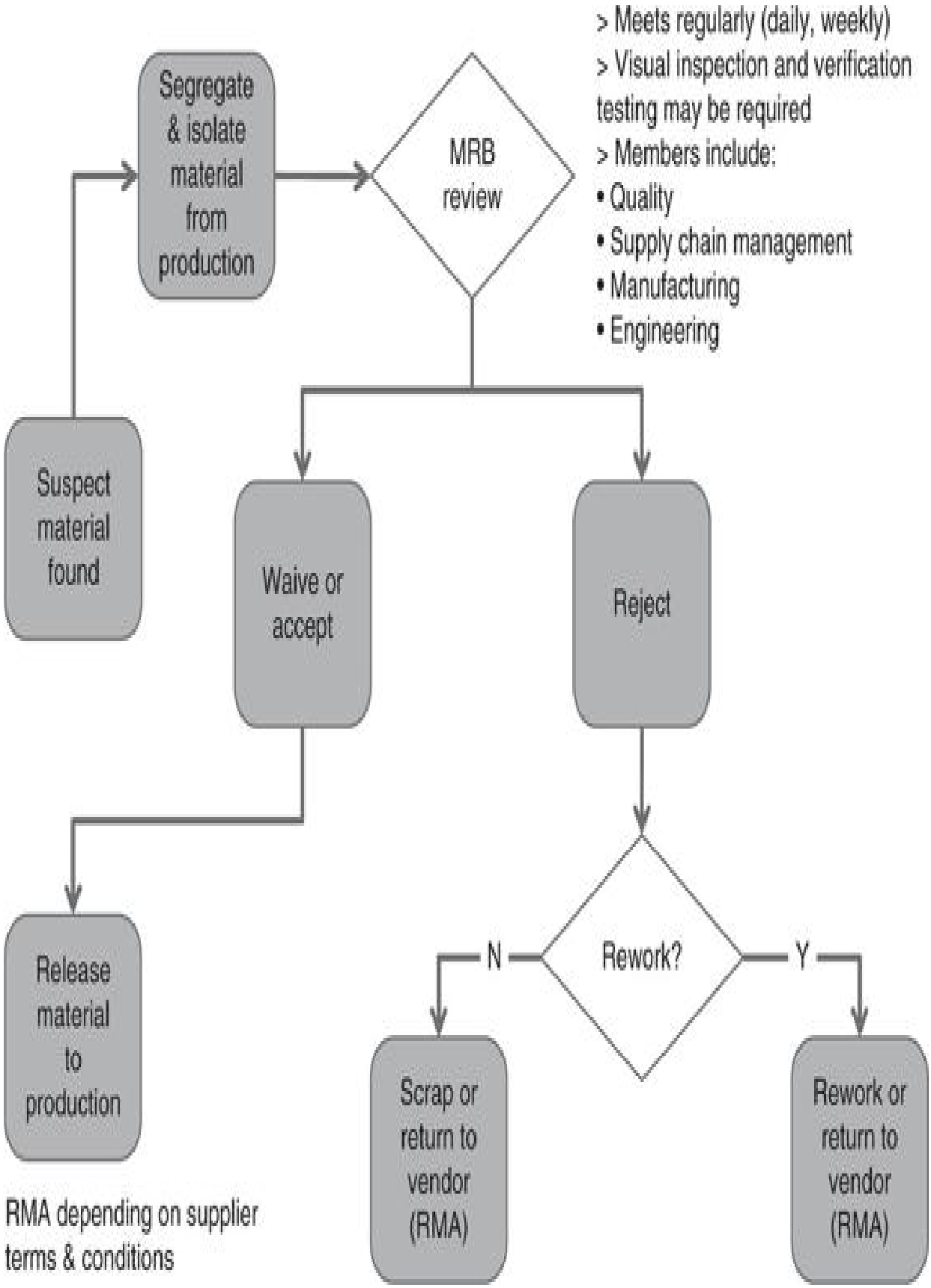

> Meets regularly (daily, weekly)
> Visual inspection and verification testing may be required
> Members include:
• Quality
• Supply chain management
• Manufacturing
• Engineering
Segregate & isolate material from production
MRB review
Suspect material found
Waive or accept
Reject
Release material to production
Rework?
N
Y
Scrap or return to vendor (RMA)
Rework or return to vendor (RMA)
RMA depending on supplier terms & conditions

FIGURE 8.1 Basic material review board (MRB) process.

8.3.1 Possible Actions by the MRB

- Recommend the board for *rework*, followed by testing and inspection. Rework for a PCB may include manually cutting a trace or soldering a jumper wire, or replacing a component for a PCA. Reworked boards are less reliable than a good board and the decision to use reworked boards in the final product should be discussed with the appropriate engineering teams. The supplier must also be consulted to determine whether the rework should be done at the customer or at the supplier. In some cases a supplier may send authorized personnel to perform the rework at the customer's location. Regardless of where the rework occurs, the terms and conditions of the supplier contract should be consulted to determine who bears the expense of rework.
- Recommend the board for *scrap*. This may be appropriate if any attempted rework would create an unacceptable risk to product reliability, or is not economically feasible. Note that suppliers are typically reluctant to declare a board to be a bad candidate for rework. Scrapped boards are usually returned to the supplier for root cause analysis and replacement using a return merchandise authorization (RMA) process. As before, the terms and conditions of the supplier contract will determine any financial adjustments.
- Recommend the board for *use as-is*. This action essentially waives or overrules the finding of the previous test or inspection, determining after closer examination that the board can be accepted for subsequent production. This may be appropriate if there is some confusion or disagreement about acceptance criteria. It may also be taken as a calculated risk if the nonconformance is not critical to the function or reliability of the final product, or

if the factory needs the boards to avoid a more serious disruption in production.

If any nonconforming boards are discovered at incoming inspection or during later assembly or test operations, the sourcing team should discuss whether to increase the sample size and/or increase the scope of testing. To increase the sample size, refer to Table 8.2 and Inspection Level III. Additional testing or inspection may also be appropriate in order to check for similar dimensional or workmanship defects elsewhere on the same board.

8.4 SUPPLIER PERFORMANCE MANAGEMENT

It is important to notify suppliers promptly regarding any performance issue, specifically for quality or delivery problems discovered at the customer:

- For high-volume production, the supplier may have work-in-progress (WIP) that requires immediate intervention to address quality or delivery issues and prevent shipping more boards with the same defects or nonconformances.
- For new suppliers on the AVL, early feedback will enable the supplier to quickly address any misunderstandings or confusion regarding customer expectations before starting work on the next purchase order.

The timing of this communication depends on how quickly the supplier is expected to correct the issue. Feedback should be specific and detailed, including part number, lot number, invoice, date received, and supporting evidence such as photographs and test results if available. The supplier will need this information to conduct an

investigation of root cause and develop an appropriate corrective action plan.

For serious quality problems that require scrap or rework, customers should insist that the supplier submit a written document that describes the investigation and corrective actions, or a corrective action report (CAR). The purpose of the document is to provide a record of the problem solving activities, and establish confidence that the supplier has successfully addressed the issue and that the issue will not recur. A common methodology used by many suppliers is *Eight Disciplines Problem Solving (8D)* created by the U.S. Department of Defense and popularized by Ford (see Table 8.3), and the CAR based on this process is sometimes referred to as an *8D report*.

TABLE 8.3 8D Problem Solving and Report Elements

	Discipline	Description
D1	Use a team approach	Identify a team with technical expertise, product and process knowledge, and decision making authority; and provide their names
D2	Describe the problem	Use specific terms, photographs, and test or inspection results to explain the nature of the problem, including who, what, where, when, why, how, and how many.
D3	Develop interim containment plan	Define the plan that will be used to isolate the problem from the customer
D4	Determine, identify and verify root causes	Brainstorm possible causes, verify that they could be the cause of the problem, and identify the most likely root cause
D5	Choose and verify permanent corrections for the problem	Verify that the correction will actually solve the problem, using quantitative evidence
D6	Implement and validate corrective actions	Implement process changes and present evidence that those changes have eliminated the root cause
D7	Take preventive measures	Modify systems, practices, and procedures to prevent reoccurrence of this problem and any similar problems
D8	Congratulate the team	Recognize the efforts of the team

Another popular methodology is the *7-Step Problem Resolution Process*, attributed to Toyota and described in Table 8.4. Both 8D and the 7-Step Process emphasize the need to understand why the issue is occurring under one set of circumstances but not another, and to consider more than one possible root cause. Regardless of which process is used,

the customer should require a systematic approach to problem solving at the supplier that avoids these pitfalls:

TABLE 8.4 7-Step Problem Resolution Process

Step	Purpose	Output	Key Questions
1. Define Problem	Identify the problem and the importance of working on it. Usually a short title that best describes the problem	• Problem statement • Project owner • Business priority • Stakeholders (customers, suppliers, team members)	• What is the problem or gap to be addressed? • Why is this a customer / business priority? • Who are the key players associated with the project?
2. Current Situation	Clarify the problem area(s) as the situation exists today. Describe what is known about the problem	• Identification of where the problem is and is-not • Supporting information to help focus the root cause analysis	• What data do you have about the problem? • Are there trends in this data? • Is there other data that you need? • What key areas does the data tell you to focus on?
3. Cause Analysis	Identify and verify the root causes of the problem	• Causes of the the problem • Data and analysis verifying root causes	• Why is the problem occurring? • What are possible root causes based on data collected and analyzed in Step 2? • What causes have the greatest impact on the problem?
4. Solutions	Develop plans to eliminate the root causes of the problem	• Documentation of proposed solutions • Plan for implementing and monitoring results	• What possible solutions would eliminate the causes identified in Step 3? • What are the recommended solutions? • Who is impacted by the solutions? • What is the implementation plan? • What monitors have been established to measure improvements?
5. Check Results	Implement plans, confirm they have impacted the root causes and that goals for improvement have been met	• Data confirming that the solutions eliminated the root causes • Decision on whether to standardize the improvement	• To what extent have the solutions eliminated the root causes? • Have the desired goals been achieved? • Were there deviations from the planned improvement? • Should the improvements be standardized?
6. Standardization	Modify process/system to ensure that the improvements are sustained over time	• Documented plan for communicating, integrating and monitoring the change • Implementation of the plan	• What does the new process look like? • How will you integrate changes into the organization?
7. Future Plans	Evaluate	• Data and documentation showing the effect of the improvement effort • Summary of remaining problems and a plan for addressing them	• To what extend did the solution improve the problem? • Does the problem require further investigation? • What issues were uncovered during the problem solving? • What other areas should the process changes be applied to? • What did the team learn during the problem solving?

- Problem poorly defined and characterized
- Rapid convergence on a single root cause without considering others
- Unclear ownership for problem resolution
- Failure to segregate suspect material
- Poor verification of root cause or solution
- No schedule to track deliverables for verification
- No leverage of knowledge, defects discovered on similar products

There is often some urgency to find and resolve the issue, and the sourcing team should be wary of quick solutions proposed by the supplier without thorough analysis. The supplier may propose additional testing and inspection on their side to check for defects and prevent future escapes, but the sourcing team should push for permanent process changes to prevent defects from occurring in the first place. Finally, the corrective action request should not be considered closed until improvement has actually been measured and noted by the customer. A corrective action plan is not the same thing as the successful implementation of that plan.

Failure to promptly or successfully resolve an issue is a serious matter that could jeopardize the relationship between a supplier and a customer, particularly for repeat occurrences of the same issue. The sourcing team should closely monitor supplier investigations and their implementation of corrective action plans. Although any failure to meet customer requirements is a concern, issues will happen from time to time, and a supplier who takes swift and effective action on behalf of the customer can still be considered a valued partner.

8.5 BUSINESS REVIEWS

In addition to real-time notification about issues discovered by the customer, the sourcing team should also schedule periodic, formal reviews of supplier performance, including AVL suppliers who are well established. These meetings are often combined with on-site supplier factory audits and customer demand forecasts. The frequency of these business reviews may depend on the volume of shipments and the timeliness of the information that will be shared with the supplier, but should be at least once per year. A sample agenda for a supplier business review is shown in Table 8.5.

TABLE 8.5 Supplier Business Review Sample Agenda

Presentation from the customer's sourcing team:
➢ Review of supplier performance requirements and targets
➢ Production and delivery metrics
➢ Quality metrics and corrective action results
➢ Comparison of supplier performance vs. competitive benchmarks
➢ Future technology requirements
➢ Projected demand
Presentation from the supplier:
➢ Update on corrective action plans and open CARs
➢ Cost reduction plans, including yield improvement
➢ Other process improvements underway

8.5.1 Agenda Items for a Supplier Business Review Meeting

- General customer performance requirements and business priorities, emphasizing the elements of technology, responsiveness, quality, and cost (or price)

previously established by the sourcing team (see Chap. 3, “Basics of Printed Circuit Supply Chain Management”)

- Quantitative data based on the supplier’s performance during the previous review period, focused on the critical needs of the customer
- Supplier performance goals for the upcoming review period
- A look ahead to upcoming technology and demand requirements
- Any changes in the customer’s business that could impact the supplier relationship

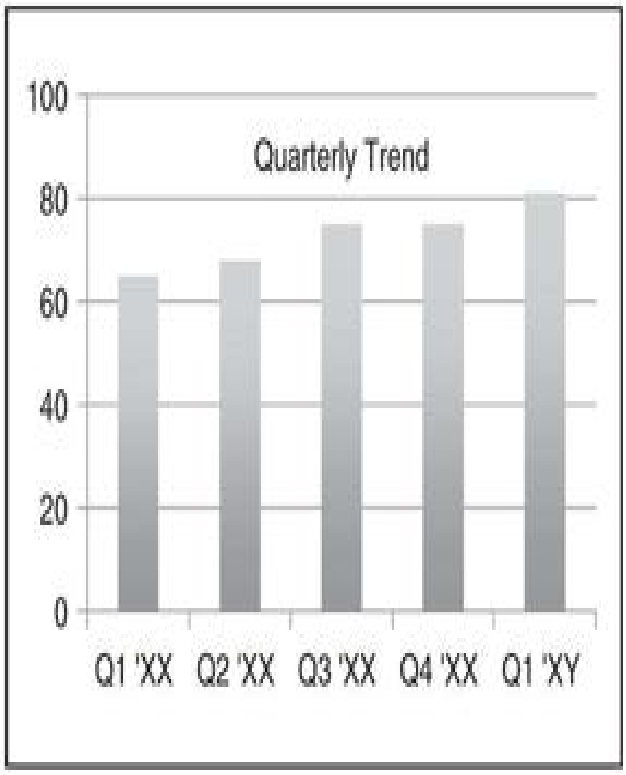
The specific supplier performance metrics will vary depending on the customer’s business priorities, but here are some examples used by sourcing teams:

- Percent of on-time deliveries (typically within a range of the commit date, such as from 3 days early to 0 days late)
- Lots rejected due to nonconforming or defective boards
- Score from a factory quality audit conducted by the customer
- Number and status of CARs
- Board price versus price reduction goals

A recommended way of presenting this information is a *supplier scorecard* or dashboard that includes a high-level summary of performance and trends over time. The sourcing team can assign a numerical score for each performance category, depending on how well the supplier meets the needs of the business, with the number of possible points in each category based on the importance of that category to the business. Figure 8.2 shows an example of a supplier scorecard and a plot of the supplier’s quarterly performance over time.

Category	Target	Max score	Supplier score
Minimum conductor width	4 mil	10	5 (8 mil)
On-time deliveries	95%	20	18 (90%)
Lead time for design changes	1 week	5	2 (2.5 weeks)
Rejected lots	0 lots	20	15 (1 lot)
Quality audit score	90	10	8 (75)
Open CARs	None > 1 month	15	15
First-pass yield	85%	10	10
Price reduction	5%	10	8 (4%)
TOTAL		100	81

Scorecard



Spider Diagram vs. Competition

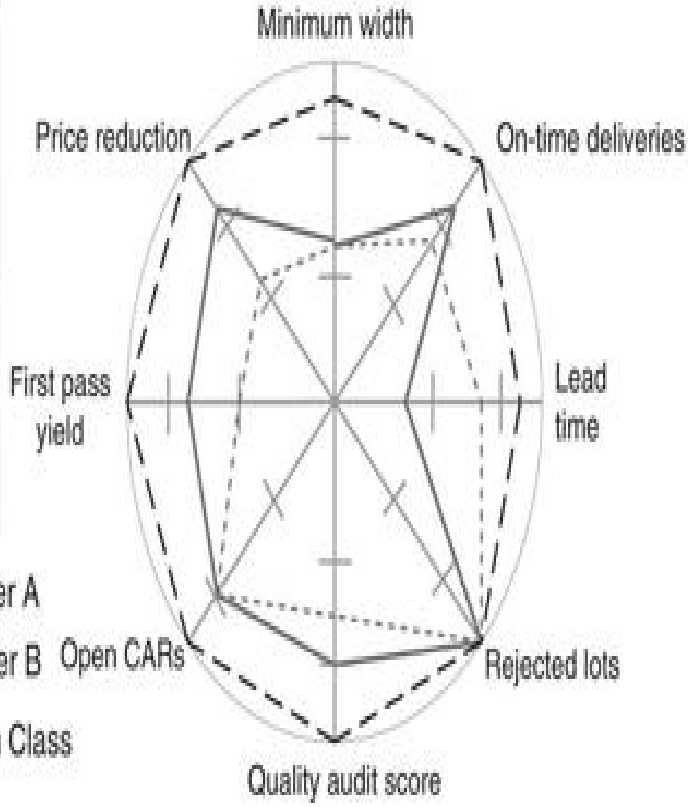


FIGURE 8.2 Supplier performance scorecard.

Also, if the customer uses more than one supplier for PCBs or PCAs, it can be useful to compare a supplier's performance against its competitors and identify gaps that can inspire improvement. A popular way of comparing suppliers is a *spider diagram*, shown in Fig. 8.2. Each supplier's performance level or score is plotted on axes radiating from the center and the points connected by a series of lines. Each axis represents a category in the scorecard. The resulting polygon provides a visual representation of overall performance and how that compares with other suppliers. Generally, the sourcing team should make sure their suppliers understand the need to improve over time in order to remain competitive and support the changing needs of the customer. The team should also regularly review supplier performance goals to determine if it's appropriate to raise the bar and demand higher performance.

The supplier should be invited to present at the business review as well. Possible topics of interest to the sourcing team include updates on new technology development, cost reductions and yield improvements, status reports on unresolved CARs, and any other planned process changes that could impact the customer.

If a supplier's performance consistently fails to meet expectations, or the sourcing team believes that the supplier is not making a good faith effort to improve, it may be necessary to switch suppliers for future production. Some companies will designate an under-performing supplier as "on probation" and restrict their use until improvement plans are successfully implemented within a designated period (see Fig. 8.3). The loss of future business needs to be a credible threat to be effective, and the sourcing team must weigh the switching cost and supply disruption against the

confidence level of better performance from a different supplier.

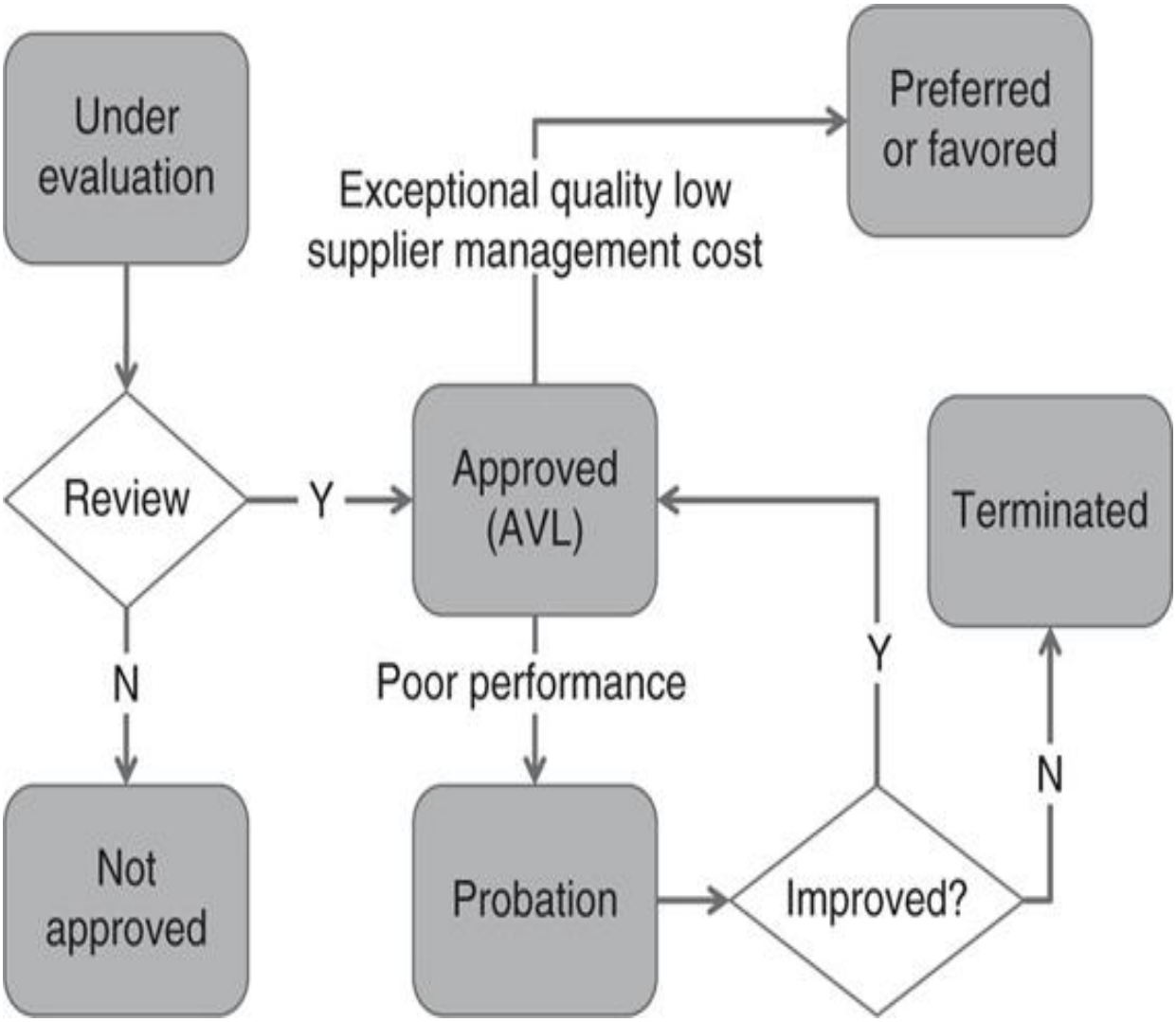


FIGURE 8.3 Supplier categories and transitions.

8.6 STRATEGIC SUPPLIER MANAGEMENT

In the case of a single transaction between a supplier and a customer there's little incentive for the supplier to provide exceptional performance that exceeds expectations. Most

suppliers operate with very small profit margins, and higher levels of service do not necessarily command a higher price. However, when a supplier believes there is a high probability of repeated transactions over an extended period, there are opportunities for mutual collaboration and partnership that supports strategic business objectives on both sides of the relationship.

From the standpoint of the customer, a supplier requires less time and cost to manage if they consistently provide high quality boards and deliver within the expected window. For example, high quality means the customer can consider a ship-to-stock program that eliminates incoming inspection or reduces it to a low-frequency audit. New designs can be rapidly qualified, which could translate into faster time-to-market. Similarly, a supplier can reduce or avoid cost when they are given the opportunity to provide design feedback to improve manufacturability, quality, and reliability.

Many companies have established a *preferred or favored supplier program* that recognizes the contribution of these suppliers to expense management and customer satisfaction (see Fig. 8.3). Preferred suppliers may receive a plaque, certificate, or other award from their customer that they can display in their lobby or promote on their website, but more importantly they may be eligible for considerations such as favorable pricing and payment terms. A customer might also agree to commit to pay for a fixed level of manufacturing capacity at a preferred or favored supplier, thereby providing predictable demand for better asset utilization.

The sourcing team should consider inviting a preferred supplier to participate in long-term planning discussions. Sharing this information helps the supplier understand the customer's future technology requirements and decide whether to add these capabilities. This works the other way as well: the customer's design team can capitalize on the supplier's technology that is currently available or in development. The customer can also provide insights about

other changes in the business that could have an impact on the supplier, such as emerging markets and the optimum geographic location of the supply chain. Generally, the better a supplier understands the customer’s business, the better they can represent the customer’s interests. Figure 8.4 summarizes the potential benefits of a closer partnership.

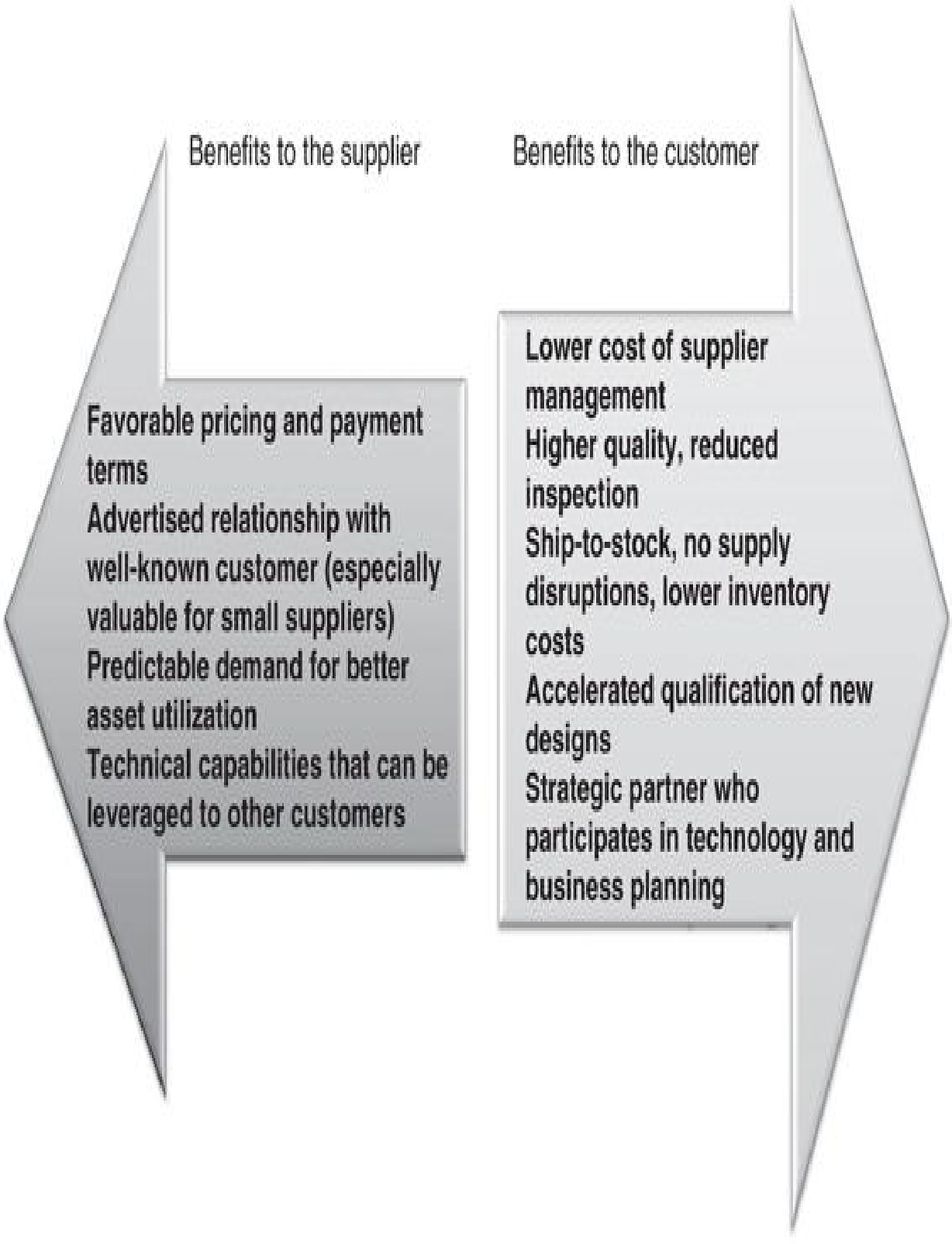


FIGURE 8.4 Advantage of a preferred supplier program.

8.6.1 Circumstances That Make It Necessary to Terminate a Supplier Relationship

- Persistent quality or responsiveness problems, and failure to successfully manage corrective actions
- Customer's cost to manage the supplier is excessive (e.g., number of resources and time required, including additional inspection or other quality incidents)
- Lower pricing from an alternate supplier
- Changing technology requirements that cannot be met by the supplier, such as high density interconnect technology or advanced materials and processes
- Changing business requirements that cannot be met by the supplier, such as shorter lead time or more consistent delivery time

Note that there is a cost for switching suppliers, particularly if this means starting a new relationship with a supplier that has no previous experience with the customer. The sourcing team should not overreact to supplier performance problems. It's important to assess these problems to determine whether the supplier is actually at fault, and assess whether a different supplier would be a net improvement. The timing of switching suppliers is also a consideration. Moving production of an active part number can create confusion in ordering and inventory management. It may be better to start production at the new supplier for the next new design or design revision.

If the decision is made to terminate the relationship, the sourcing team should give early notice to the supplier to prevent incurring additional cost for incoming materials. The customer is certainly not required to give a reason, but it is good business practice. A transition plan is necessary to determine the schedule for ramping down production,

managing remaining inventory and work-in-process, and returning all intellectual property that is owned by the customer.

PART 3

MATERIALS

CHAPTER 9

INTRODUCTION TO BASE MATERIALS

Edward Kelley
Douglas Trobough
Isola Group, Chandler, Arizona

9.1 INTRODUCTION

Just as printed circuits are a basic building block of electronic devices, base materials are a fundamental building block of printed circuits. But while the field of base materials can appear simple, variants in the building blocks used to make the base materials add significant complexity when deciding what material to use. In simple terms, base materials consist of just three components: the resin system (including any fillers used), the reinforcement, and the conductive foil. However, combinations of the available materials in each of these component categories require the user to make several important decisions. The best decision often depends on the end use application, which drives decisions on electrical performance, reliability and of course cost.

Also, because base materials are the most fundamental component of the printed circuit, they interact with critical printed circuit manufacturing processes. Therefore, not only are the physical and electrical properties of the material critical, but their compatibility with manufacturing processes used is also of great importance.

The advent of the European Union's Restriction of Hazardous Substances (RoHS) directive and the lead-free assembly processes that resulted, redefined the requirements for base materials. The impact of lead-free assembly on base materials and a method of selecting materials for lead-free assembly are discussed in Chap. 14 Requirements to support circuit densification, reliability, and electrical performance are also critical and will be discussed in Chap. 12. This chapter discusses grades and specifications of base materials, as well as the manufacturing processes used to make them.

9.2 GRADES AND SPECIFICATIONS

The various types of base materials can be classified by the reinforcement type, the resin system used, the glass transition temperature (T_g) of the resin system, as well as many other properties of the material. With the advent of lead-free assembly processes, properties other than T_g have become as important, if not more important when selecting a base material. The decomposition temperature (T_d) is one of these properties and will be defined shortly.

The most commonly referenced specification for base materials is IPC-4101, "Specification for Base Materials for Rigid and Multilayer Printed Boards." In the past, the National Electrical Manufacturers Association (NEMA) has also been used in specifying base materials.

9.2.1 NEMA Industrial Laminating Thermosetting Products

One of the first classifications of base materials for printed circuits (and other electrical components) was completed by the NEMA. NEMA's industrial laminating thermosetting products standard documents many of the materials used in printed circuits as well as specifications for some of their properties. Historical NEMA grades are outlined in Table 9.1 and cross-referenced with IPC-4101 in Table 9.2. Some of the commonly used materials have been FR-2, CEM-1, CEM-3, and, of course, FR-4.

TABLE 9.1 NEMA Base Material Grades

Grade	Resin	Reinforcement	Flame Retardant
XXXPC	Phenolic	Cotton paper	No
FR-2	Phenolic	Cotton paper	Yes
FR-3	Epoxy	Cotton paper	Yes
FR-4	Epoxy	Woven glass	Yes
FR-5	Epoxy	Woven glass	Yes
FR-6	Polyester	Mat glass	Yes
G-10	Epoxy	Woven glass	No
CEM-1	Epoxy	Cotton paper/woven glass	Yes
CEM-2	Epoxy	Cotton paper/woven glass	No
CEM-3	Epoxy	Woven glass/mat glass	Yes
CEM-4	Epoxy	Woven glass/mat glass	No
CRM-5	Polyester	Woven glass/mat glass	Yes
CRM-6	Polyester	Woven glass/mat glass	No
CRM-7	Polyester	Mat glass/glass veil	Yes
CRM-8	Polyester	Mat glass/glass veil	No

TABLE 9.2 IPC-4101 Base Material Summary

Spec. Sheet #	Reinforcement Type	Resin System	ID Reference*	T_g Range	Other Properties
00	Cellulose paper	Phenolic	XPC	None	UL94 HB
01	Cellulose paper	Phenolic	XXXPC	None	UL94 HB
02	Cellulose paper	Phenolic	FR-1	None	UL94 V-1
03	Cellulose paper	Phenolic	FR-2	None	UL94 V-1
04	Cellulose paper	Epoxy	FR-3	None	UL94 V-1
05	Cellulose paper	Phenolic, phosphorus flame retardant	FR-2	None	UL94 V-1, limits on Br and Cl content
10	Woven E-glass surface/ cellulose paper core	Epoxy/phenolic	CEM-1	100°C min.	UL94 V-0, with or without inorganic fillers
11	Woven E-glass surface/ nonwoven E-glass core	Polyester/vinyl ester	CRM-5/11	None	UL94 V-1, inorganic fillers
12	Woven E-glass surface/ nonwoven E-glass core	Epoxy	CEM-3	None	UL94 V-0, with or without inorganic fillers
13	Woven E-glass	Polyester/vinyl ester	None	None	UL94 V-1, Inorganic fillers
14	Woven E-glass surface/ nonwoven E-glass core	Epoxy, phosphorous flame Retardant	CEM-3	None	UL94 V-0, limits on Br and Cl content
15	Woven E-glass surface/ cellulose paper core	Epoxy/phenolic, phosphorous Flame retardant	CEM-1	100°C min.	UL94 V-0, limits on Br and Cl content
16	Woven E-glass surface/ nonwoven E-glass core	Epoxy/phenolic	CEM-3	100°C min.	UL94 V-0, contains inorganic fillers
20	Woven E-glass fabric	Epoxy	G-10, MIL-S-13949/03-GE, GEN	None	UL94 HB
21	Woven E-glass	Difunctional and multifunctional epoxy	FR-4, MIL-S-13949/04-GF, GFN, GFK, GFP, GFM	110°C min.	UL94 V-0
22	Woven E-glass	Epoxy, hot strength retention, nonflame resistant	G-11 MIL-S-13949/02-GB, GBN, GBP	135–175°C	UL 94 HB
23	Woven E-glass	Epoxy, hot strength retention, flame resistant	FR-5, MIL-S-13949/05-GH, GHN, GHP	135–185°C	UL94 V-1
24	Woven E-glass	Epoxy/multifunctional epoxy	FR-4, MIL-S-13949/04-GF, GFG, GFN	150°C min.	UL94 V-0

25	Woven E-glass	Epoxy/PPO	MIL-S-13949/04-GF, GFG, GFN	150–200°C	UL94 V-1
26	Woven E-glass	Epoxy/multifunctional epoxy	FR-4, MIL-S-13949/04-GF, GFT	170°C min.	UL94 V-0
27	Unidirectional E-glass, cross-plied	Epoxy/multifunctional epoxy	N/A	110°C Min.	UL94 V-1
29	Woven E-glass	Epoxy/cyanate ester	MIL-S-13949/ 04-GFN, GFT	170–220°C	UL94 V-1
30	Woven E-glass	Bismaleimide/triazine (BT)/epoxy	GPY, MIL-S-13949/26-GIT, GMT	170–220°C	UL94 HB
31	None	Epoxy/multifunctional epoxy	N/A	90°C min.	Non-reinforced film, inorganic fillers, thermally conductive
32	Woven E-glass	Epoxy/multifunctional epoxy	N/A	90°C min.	Inorganic fillers, thermally conductive
33	None	Epoxy/multifunctional epoxy	N/A	150°C min.	Nonreinforced film, inorganic fillers, thermally conductive
34	None	Epoxy/multifunctional epoxy	N/A	150°C min.	Nonreinforced film, inorganic fillers, thermally conductive
35	Woven E-glass	Epoxy/phenolic, phosphorous flame retardant	CEM-3	110°C min.	Inorganic fillers, thermally conductive
40	Woven E-glass	Polyimide	GPY MIL-S-13949/10-GI, GIN, GII, GIP, GIL	200°C min.	UL94 HB, with or without inorganic fillers
41	Woven E-glass	Polyimide	GPY MIL-S-13949/10-GI, GIP	250°C min.	UL94 HB with or without inorganic fillers
42	Woven E-glass	Polyimide/epoxy	GPY MIL-S-13949/10-GII	200°C min.	UL94 HB with or without inorganic fillers
43	Woven E-glass	Polyimide	MIL-S-13949/10 – GI, GIN, GIL, GIP	250°C min.	UL94 HB, with inorganic fillers
44	Woven E-glass	Polyimide, modified polyimide nitrogen/inorganic compound for flame retardants	N/A GIL, GIP	250°C min.	UL94 V-0, with inorganic fillers and limits on Br and Cl
50	Woven aramid	Epoxy/multifunctional epoxy	MIL-S-13949/15-AF, AFN, AFG	150–200°C	UL94 V-1

53	Nonwoven aramid paper	Polyimide	MIL-S-13949/31-BIN, BIJ	220°C min.	UL94 HB
55	Nonwoven aramid paper	Epoxy/multifunctional epoxy	MIL-S-13949/22-BF, BFN, BFG	150–200°C	UL94 V-1
58	Nonwoven aramid paper	Multifunctional epoxy, nonepoxy, phosphorus flame retardant	N/A	135–185°C	UL94 V-0, limits on Br and Cl content
60	Woven quartz	Polyimide	MIL-S-13949/19-QIL	250°C min.	UL94 HB
61	Woven quartz	Cyanate ester	MIL-S-13949/19-QIL	220°C min.	UL94 V-0
70	Woven S-2 glass	Cyanate ester	N/A	230°C min.	UL94 V-1
71	Woven E-glass	Cyanate ester	MIL-S-13949/29-GCN	230°C min.	UL94 V-1
72	Woven E-glass	Epoxy/cyanate ester/nonepoxy	FR-4	170°C min.	UL94 V-0, contains fillers
73	Woven E-glass	Epoxy/cyanate ester/modified Epoxy or nonepoxy	FR-4	170°C min.	UL 94-V-0, contains fillers
80	Woven E-glass surface/cellulose paper core	Epoxy/phenolic (catalyzed for additive process), flame resistant (bromine or antimony)	CEM-1	100°C min.	UL94 V-0, Kaolin or inorganic catalyst
81	Woven E-glass surface/ nonwoven E-glass core	Epoxy (catalyzed for additive process)	CEM-3	None	UL94 V-0, Kaolin or inorganic catalyst
90	Woven E-gass	Polyphenylene ether, bromine/ antimony flame retardant	N/A	175°C min.	UL94 V-1
91	Woven E-glass	Polyphenylene ether	N/A	175°C min.	UL94 V-1
96	Woven E-glass	Polyphenylene ether, phosphorous flame retardant	N/A	175°C min.	UL94 V-1, limits on Br and Cl content
97	Woven E-glass	Difunctional epoxy, multifunctional epoxy	FR-4, MIL-S-13949/04 - GF, GFN, GFK, GFP, GFM	110°C min.	UL94 V-0, inorganic fillers
98	Woven E-glass	Epoxy/multifunctional epoxy	FR-4, MIL-S-13949/04 - GF, GFG, GFN	150°C min.	UL94 V-0, inorganic fillers
99	Woven E-glass	Epoxy/multifunctional Epoxy/ modified or nonepoxy	FR-4	150°C min.	UL94 V-0, inorganic fillers
101	Woven E-glass	Epoxy/multifunctional epoxy/ modified or nonepoxy	FR-4	110°C min.	UL94 V-0, inorganic fillers
102	Woven E-glass	Modified polyphenylene ether	N/A	185°C min.	UL94 V-0, inorganic fillers

103	Woven E-glass	Epoxy/polyphenylene oxide	N/A	150°C min.	UL94 V-1, inorganic fillers
121	Woven E-glass	Difunctional epoxy, multifunctional epoxy, modified or nonepoxy	FR-4	110°C min.	UL94 V-0
122	Woven E-glass	Difunctional epoxy, multifunctional epoxy, modified or nonepoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	110°C min.	UL94 V-0
124	Woven E-glass	Epoxy, multifunctional epoxy/ modified or nonepoxy	FR-4	150°C min.	UL94 V-0
125	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or nonepoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	150°C min.	UL94 V-0, limits on Br and Cl content
126	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or nonepoxy	FR-4	170°C min.	UL94 V-0, inorganic fillers
127	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or noneoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	110°C min.	UL94 V-0, inorganic fillers, limits on Br and Cl content
128	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or nonepoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	150°C min.	UL94 V-0, inorganic fillers, limits on Br and Cl content
129	Woven E-glass	Epoxy, multifunctional epoxy, modified or nonepoxy	FR-4	170°C min.	UL94 V-0
130	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or nonepoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	170°C min.	UL94 V-0, inorganic fillers, limits on Br and Cl content
131	Woven E-glass	Epoxy, multifunctional epoxy, modified epoxy or nonepoxy, phosphorous, nitrogen and/or inorganic flame retardants	FR-4	170°C min.	UL94 V-0, limits on Br and Cl content

*ANSI, NEMA, and/or MIL-S-13949 grade. Note that MIL-S-13949 is not an active specification.

FR-2 is comprised of multiple plies of paper impregnated with a flame-resistant phenolic resin. It possesses good punching characteristics and is relatively low in cost. It has typically been used in simple applications such as radios, calculators, and toys, where dimensional stability and high performance are not required. FR-3 is also paper based, but uses an epoxy resin system.

CEM-1 uses a paper-based core with woven glass cloth on the surfaces, both impregnated with an epoxy resin. This enables the material to be punched while realizing improved electrical and physical properties. CEM-1 has been used in both consumer and industrial electronics.

CEM-3, a composite of dissimilar core materials, uses an epoxy resin impregnated, nonwoven fiberglass core with epoxy resin impregnated, woven fiberglass cloth surface sheets. It is higher in cost than CEM-1, but is more suitable for plated through holes. CEM-3 had been used in early home computers, automobiles, and home entertainment products.

FR-4, by far the most commonly used material for printed circuits, is constructed of woven fiberglass cloths impregnated with an epoxy resin or epoxy resin blend. The outstanding electrical, mechanical, and thermal properties of FR-4 have made it an excellent material for a wide range of applications including computers and peripherals, servers and storage networks, telecommunications, aerospace, industrial controls, and automotive applications. FR-4 will be discussed in more detail later.

9.2.2 IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

The most commonly used specification for base materials is IPC-4101. This specification presents a classification scheme and specification sheets for the various materials in use. Table

9.2 summarizes the various materials by specification sheet number. Each specification sheet in IPC-4101[1] includes property requirements for that particular material type. It is recommended that the latest revision of this document be reviewed, although it is possible to specify materials based on past revisions of this document. Table 9.2 is presented for reference only and may not be all-inclusive as new specification sheets can be added periodically, so the user should consult this document when reviewing requirements. UL94 comments in Table 9.2 reference the minimum flammability requirements for that material. Materials may be more flame retardant than these minimum ratings. Also note that materials with halogen-free flame retardants are noted as such in the resin system column. Definitions of the UL flammability ratings are given in Chap. 11.

Some of the properties documented in the specification sheets of IPC-4101 include T_g, copper peel strengths at different conditions, volume resistivity, surface resistivity, moisture absorption, dielectric breakdown voltage, permittivity, loss tangent, flexural strengths and arc resistance. These properties will be discussed further in Chap. 11. In some cases the specification is listed as AABUS. AABUS is an acronym for "as agreed between user and supplier," meaning there is not currently an agreed upon industry specification value for that property.

It is also important to understand that the specification sheets may be used as a general starting point, and that the user and supplier are free to agree upon exceptions to certain values when sourcing the material. For example, there is a growing desire for lower and lower copper roughness profiles for signal integrity reasons. As the copper roughness decreases, the copper peel strength will generally decrease as well, and may fall below the values in the specification sheet. In this case, the user and supplier could reference a particular specification sheet and make an exception for the peel strength value. This could be done for other properties as well.

It should also be noted that the properties covered by these specification sheets refer to copper clad laminate and prepreg as noted on these sheets. Base material suppliers generally develop corresponding data sheets with typical material properties for the laminate and prepreg. Properties of actual printed circuits may vary from the values listed on the laminate and prepreg specification and data sheets. There can be multiple reasons for this, including property variation based on the actual construction and resin content of the materials used, as well as the influence of the printed circuit manufacturing process.

9.2.3 IPC-4103 Specification for Base Materials for High-Speed/High-Frequency Applications

There are additional specifications related to materials depending on the application. One of these is IPC-4103, which is for high-speed/high-frequency applications. As stated in the scope of this specification, it is for high-speed/high-frequency materials used for fabrication of printed circuits for microstrip, stripline, high-speed digital and RF/microwave electrical and electronic circuits. In general, laminates controlled by this specification usually have a dissipation factor of less than 0.005.

IPC-4103 parallels IPC-4101 in many ways, with the obvious increased emphasis on electrical properties. Like IPC-4101, IPC-4103 maintains specification sheets for different materials. Tables 9.3 and 9.4 are the summaries of specification sheets contained in IPC-4103. Note that there can be differences in the designations for metal cladding, as well as the overall designation scheme used in IPC-4103 compared to IPC-4101. The latest revisions of these specifications should be referenced when using these designations.

TABLE 9.3 Summary of Legacy Specification Sheets in IPC-4103

Specification Sheet #	Reinforcement	Resin System	Filter	Permittivity Range	ID Reference
IPC-4103/01	Woven E-Glass	PTFE	None	2.45-2.65	MIL-13949/8, Type GT
IPC-4103/02	Woven E-Glass	PTFE	None	2.40-2.60	MIL-13949/9, Type GX
IPC-4103/03	Non-Woven E-Glass	PTFE	None	2.15-2.35	MIL-13949/6, Type GP
IPC-4103/04	Non-Woven E-Glass	PTFE	None	2.15-2.35	MIL-13949/7, Type GR
IPC-4103/05	Woven E-Glass	PTFE	None	2.15-2.35	MIL-13949/14, Type GY
IPC-4103/06	With or Without Woven or Non-Woven E-Glass	PTFE	Ceramic	3.00 Maximum	N/A
IPC-4103/07	With or Without Woven or Non-Woven E-Glass	PTFE	Ceramic	5.0-7.0	N/A
IPC-4103/08	With or Without Woven or Non-Woven E-Glass	PTFE	Ceramic	7.5-11.0	N/A
IPC-4103/09	Woven E-Glass	PTFE	None	2.70-3.60	N/A
IPC-4103/10	Woven E-Glass	Hydrocarbon	Ceramic	3.25-3.45	N/A
IPC-4103/11	Woven E-Glass	Hydrocarbon	Ceramic	3.40-3.60	N/A
IPC-4103/12	Woven E-Glass Face Sheets, Non-Woven E-Glass Core	Polyester	Kaolin	3.00-4.50	CRM-5
IPC-4103/13	Woven E-Glass Face Sheets, Non-Woven E-Glass Core	Polyester	Kaolin	3.00-3.50	CRM-5
IPC-4103/14	Woven E-Glass	Polyester	None	3.00-4.00	N/A
IPC-4103/15	None	Thermoplastic	None	1.98-2.35	N/A
IPC-4103/16	Woven or None Woven E-Glass	PTFE	Ceramic	3.00-4.90	N/A
IPC-4103/17	Woven E-Glass	Hydrocarbon	None	2.50-3.60	N/A

TABLE 9.4 Summary of IPC-4103A Specification Sheets

Material	Specification Sheet Number	Dk Range	Df Low to High Performance Cutoff
Laminate	IPC-4103/200	<2.20	0.0015
	IPC-41 03/210	2.21 to 2.33	0.0020
	IPC-4103/220	2.34 to 2.65	0.0025
	IPC-4103/230	2.66 to 3.05	0.0025
	IPC-4103/240	3.06 to 3.58	0.0025
	IPC-4103/250	3.59 to 4.50	0.0025
	IPC-4103/260	4.51 to 5.99	0.0025
	IPC-4103/270	6.00 to 8.99	0.0025
	IPC-4103/280	9.00 to 11.00	0.0025
	IPC-4103/290	>11.01	0.0025
Bonding Layer	IPC-4103/500	<2.20	0.0015
	IPC-41 03/510	2.21 to 2.33	0.0020
	IPC-4103/520	2.34 to 2.65	0.0025
	IPC-4103/530	2.66 to 3.05	0.0025
	IPC-4103/540	3.06 to 3.58	0.0025
	IPC-4103/550	3.59 to 4.50	0.0025
	IPC-4103/560	4.51 to 5.99	0.0025
	IPC-4103/570	6.00 to 8.99	0.0025
	IPC-4103/580	9.00 to 11.00	0.0025
	IPC-4103/590	>11.01	0.0025

9.2.4 IPC/JPCA-4104 Specification for High-Density Interconnect and Microvia Materials

In addition to IPC4101 and IPC-4103, IPC/JPCA-4104[3] is also used, and pertains to additional materials used for high-density interconnect (HDI) and microvia designs, particularly for thin multilayer PCBs used in such applications as mobile phones, smartphones and tablet computers. It contains information on the general classification and characteristics of HDI materials. Like the other specifications, it provides a designation scheme specific to the HDI materials as well as conformance and quality assurance requirements. The designation system for IPC-4104 is also different than for materials covered by IPC-4101, so it is recommended to refer to IPC-4104 when it is desired to use this system.

Figure 9.1 provides a very simple illustration of HDI with microvias, and Fig. 9.2 provides an illustration of various methods that can be used to manufacture HDI circuits with microvias. Currently, laser drilled microvias are the most common method used to make microvias, although there are specific applications and design types that use other methods. For many of the printed circuits manufactured today with microvias, conventional glass reinforced materials are used, albeit mostly with thin fiberglass cloth styles. These materials will be discussed further in Chap. 11, covering base material components. In addition, Chaps. 25 and 26 focus specifically on HDI.

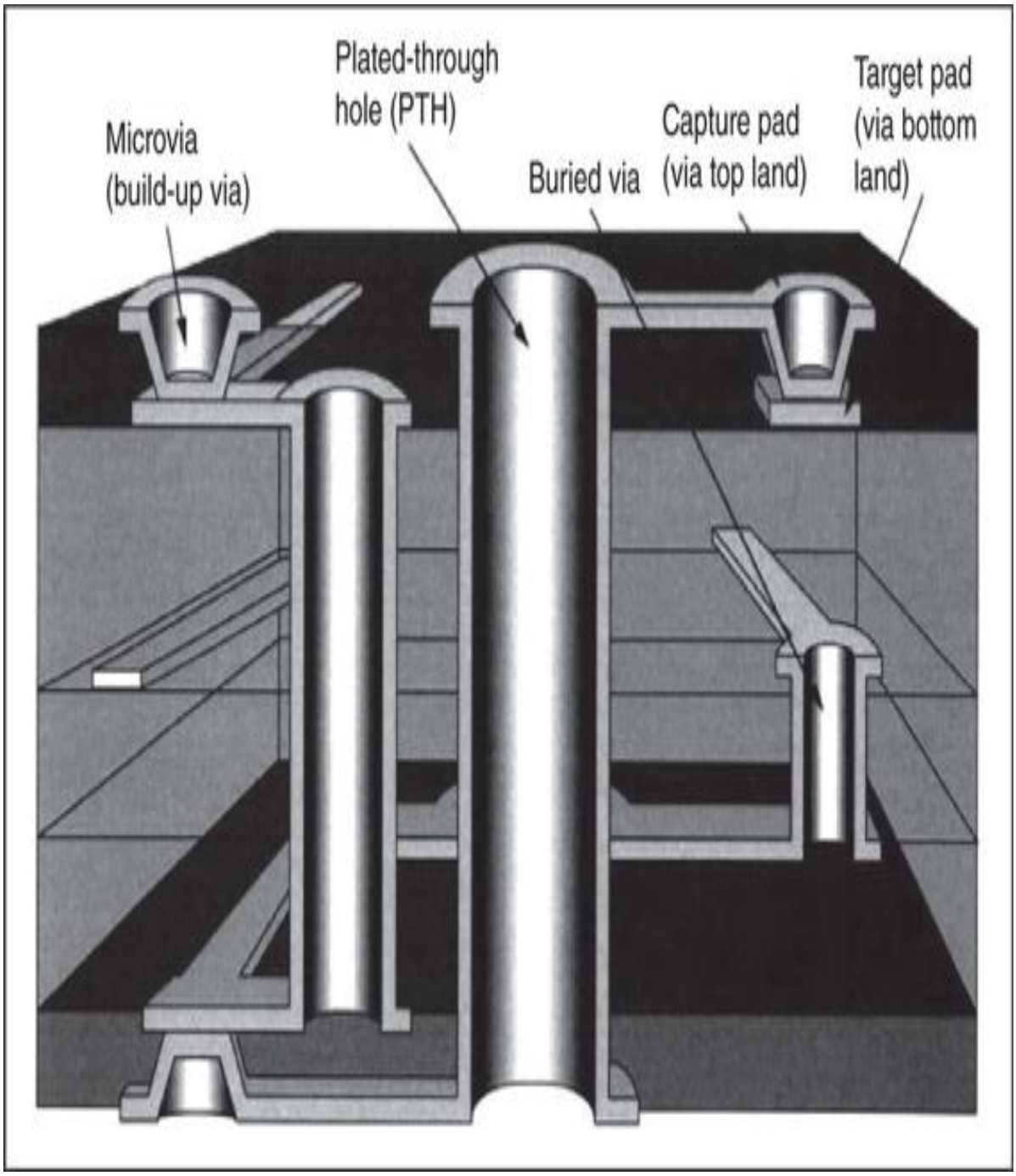


FIGURE 9.1 General illustration of HDI with microvias. (*From IPC-4104*.)

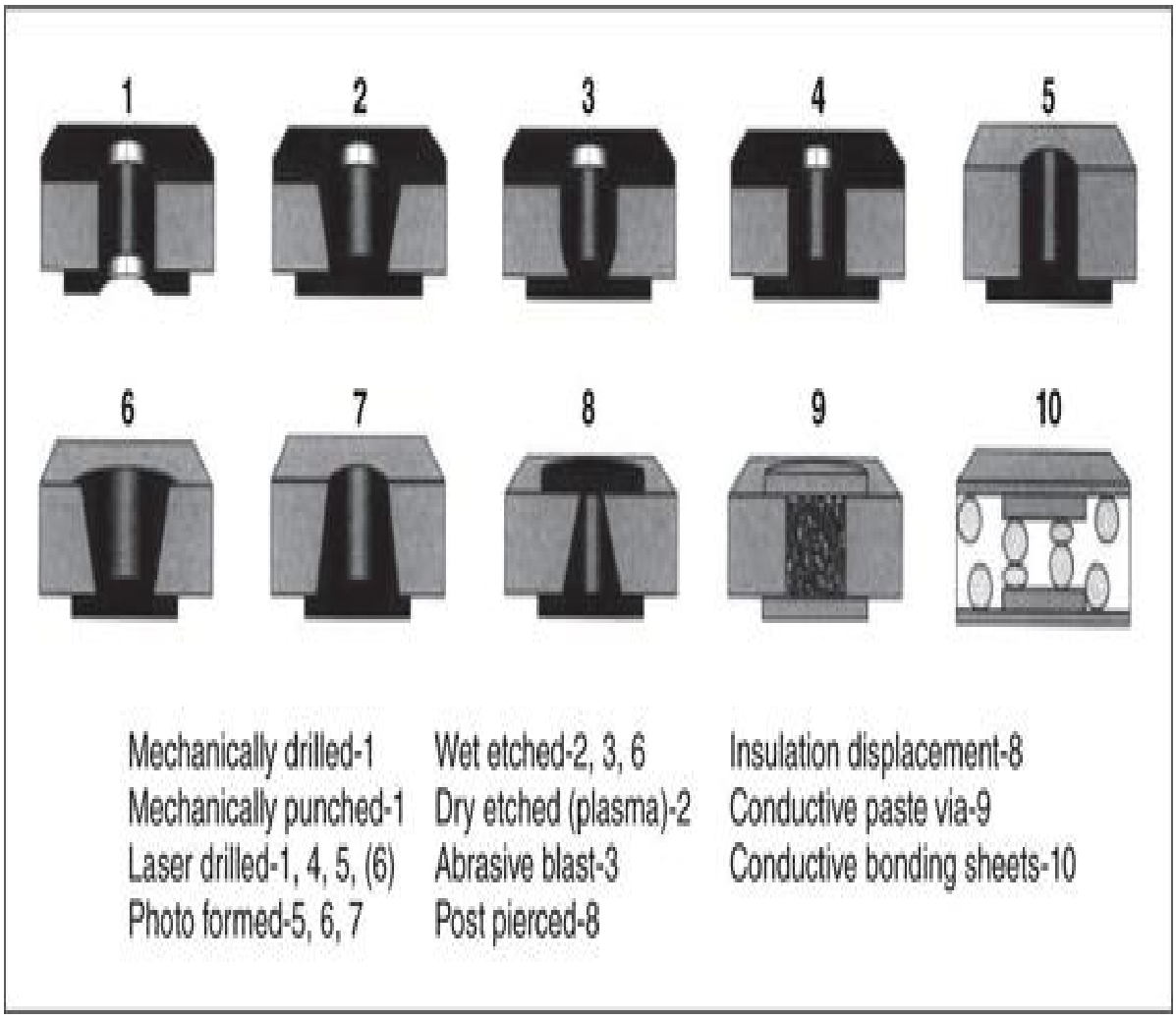


FIGURE 9.2 Methods used to form microvias. (*From IPC-4104*.)

9.3 PROPERTIES USED TO CLASSIFY BASE MATERIALS

Historically, the T_g had been the most common property used to classify FR-4 base materials, and this is one of the primary properties documented in IPC-4101. Materials with high T_g values were generally viewed as being more reliable. While this question was never as simple as specifying only the T_g, the move toward lead-free assembly has caused a fundamental redefinition of what properties are needed to ensure a given

level of reliability. The reason is that the alloys used in lead-free assembly require higher peak temperatures than those used in tin-lead assembly. These higher peak temperatures can approach the point where many base materials begin to decompose. For this reason, the decomposition temperature has become important, along with thermal expansion properties, modulus, moisture absorption as well as adhesion characteristics often measured by using time-to-delamination tests such as the T260 test.

The T_g and its impact on *z*-axis expansion are summarized below along with the decomposition temperature. The other properties will be discussed in Chaps. 11 and 12.

9.3.1 Glass Transition Temperature, T_g

The T_g of a resin system is the temperature at which the material transforms from a relatively rigid or "glassy" state, to a more deformable state with a significant drop in modulus. This is a thermodynamic change in the material which is reversible as long as the resin system has not been degraded. This is to say that when a material that has been heated above its T_g is cooled back below the T_g, it returns to a more rigid state with essentially the same properties as before. However, if the material is heated to too high a temperature beyond T_g, irreversible changes in properties may result. The temperature at which this will happen varies by material type and is related to resin decomposition, discussed later.

A material is not in a liquid state when it is above the T_g. It is a temperature at which physical changes take place due to the weakening of molecular bonds within the material. It is important to understand T_g since the properties of base materials are different above T_g than below T_g. While the T_g is typically described as being a very precise temperature, this is somewhat misleading, because the physical properties of the

material can begin to change as the T_g is approached and some of the molecular bonds are affected. As the temperature increases, more of the bonds become weakened until the material reaches a steady state with new properties. This explains the curved line in Fig. 9.3, which is discussed in the following text.

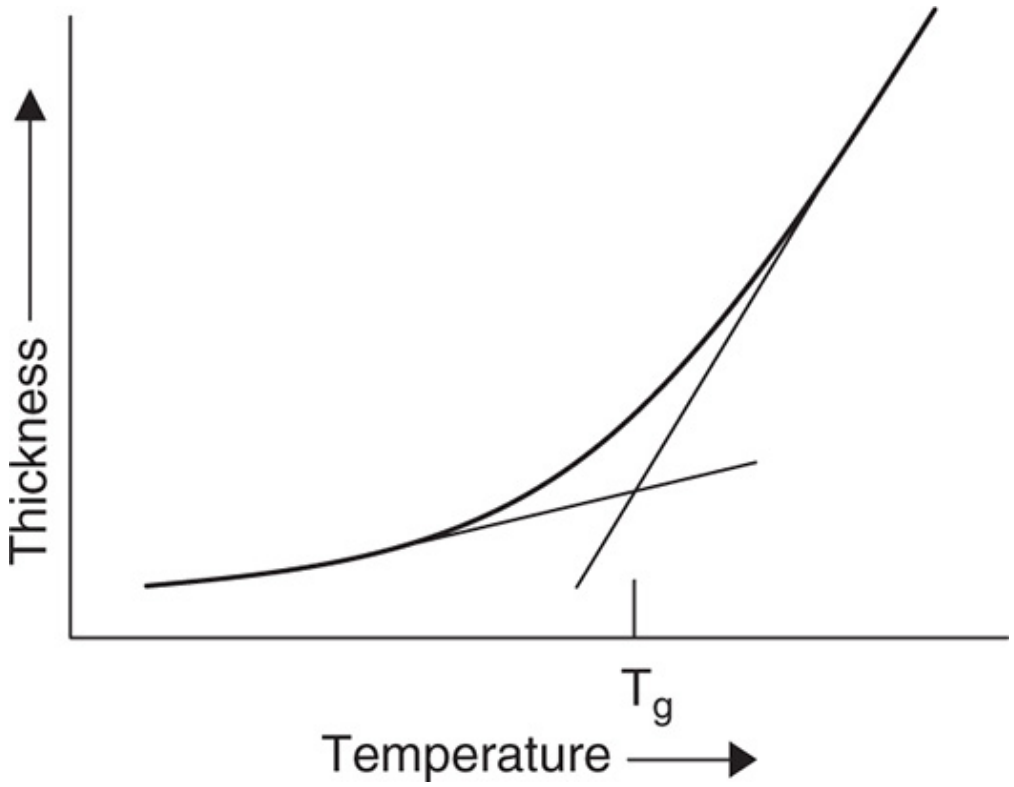


FIGURE 9.3 Glass transition temperature by TMA.

The T_g of a resin system has several important implications. These include

- The impact on thermal expansion.
- The temperature at which the materials' modulus properties decrease.
- A measure of the degree of cure of the resin system.

9.3.1.1 Thermal Expansion. All materials will undergo changes in physical dimensions in response to changes in

temperature. The rate at which the material expands is much lower below the T_g than above. Thermomechanical analysis (TMA) is a procedure used to measure dimensional changes versus temperature. Extrapolating the linear portions of the curve to the point at which they intersect provides a measure of the T_g (see Fig. 9.3). The slopes of the linear portions of the curve above and below the T_g represent the respective rates of thermal expansion, or as they are typically called, the coefficients of thermal expansion (CTEs). CTE values are important since they influence the reliability of the finished circuit. Other things being equal, less total thermal expansion will result in greater circuit reliability as less stress is applied to plated holes. With a higher T_g value, the onset of more rapid thermal expansion is delayed.

9.3.1.2 Modulus Decrease. Modulus can be defined as the ratio of stress-to-strain in a material. A high modulus material would exhibit little strain even at high levels of stress. In the discussion of T_g, a materials' modulus is relatively high below T_g, and decreases rapidly as it is heated above the T_g. Differences in modulus properties between material types can influence thermal reliability performance, but it should also be noted that for conventional materials for PCBs, the actual modulus values in a PCB will also be affected by the glass fabric type and copper foil, in addition to the resin system.

9.3.1.3 Degree of Cure. The resin systems used in base materials begin with subcomponents that contain reactive sites on their molecular structures. The application of heat to the resin system and curing agents causes the reactive sites to *cross-link* or bond together. This process of curing the resin system brings about physical changes in the material in proportion to the degree to which the cross-linking occurs, including increases in the T_g. When most of the reactive sites have cross-linked, the material is said to be fully cured and its ultimate physical properties will be established.

Besides TMA, two other thermal analysis techniques are also commonly used for measuring T_g: differential scanning calorimetry (DSC) and dynamic mechanical analysis (DMA), with DSC one of the most common methods used today.

- DSC measures heat flow versus temperature rather than the dimensional changes measured by TMA. The heat absorbed or given off will also change as the temperature increases through the T_g of the resin system. T_g measured by DSC is often somewhat higher than measurements by TMA.
- DMA measures the modulus of the material versus changes in temperature, and also will give somewhat higher values for T_g.

Materials that are not fully cured can cause problems in circuit manufacturing processes and with finished circuit reliability. For example, an undercured multilayer circuit can exhibit greater amounts of total *z*-axis thermal expansion. This adversely affects circuit board reliability due to the increased stress on the plated through holes as the circuit expands.

Because increased cross-linking will require greater amounts of energy (heat) to weaken the bonds in the molecular structure of the resin system, measurements of T_g can sometimes be used to determine the degree of cure of the resin system. For some resin system types, especially the "dicy-cured" FR-4 materials widely used before the advent of lead-free assembly, a measure of the degree of cure can be obtained by performing two thermal analyses on the same sample. After the first analysis, the sample is subjected to a thermal cycle designed to promote additional cross-linking within the resin system, and then a second thermal analysis is performed. The degree of cure is measured by comparing the difference in measured T_g between the two analyses (see Fig. 9.4). If the material is fully cured, the difference between T_{g2} and T_{g1} will be small. It should also be noted that internal stress and sample composition can affect the degree of cure

measurements, particularly on nondicy cured higher T_g materials.

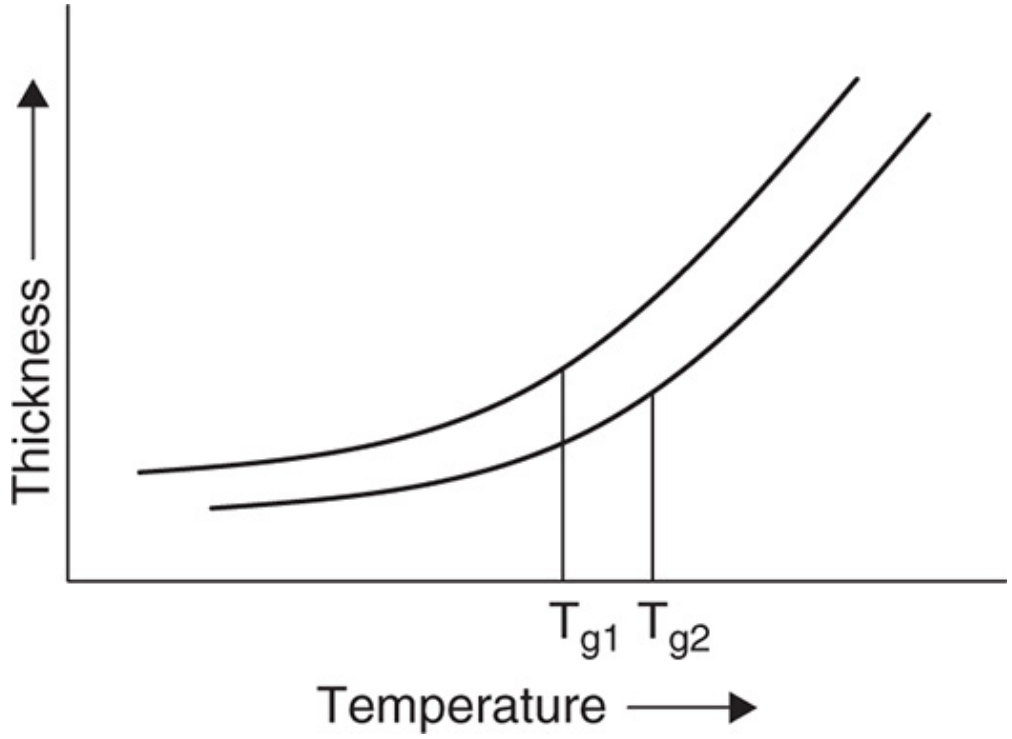


FIGURE 9.4 Measuring degree of cure.

However, great care must be exercised when using these methods to assess degree of cure. An understanding of the resin system is important because not all resins will behave the same way when performing sequential tests such as this. The "phenolic-cured" FR-4 resin systems that grew in volume with the advent of lead-free assembly will generally advance in cure somewhat with additional thermal cycles. With the dicy-cured FR-4s, it was common to use this difference in T_g as an assessment of cure, with a requirement of ± 5°C between measurements. With phenolic-cured FR-4 resins, as well as most new resin systems, this method is not always appropriate. It is recommended to discuss the feasibility of this assessment for a given material type with the supplier of that material.

The terminology used to discuss the degree of cure can also be important. Below are some common terms that can assist in

discussions related to the state of cure of a material.

- *Undercured*. Refers to material that will readily continue to cross-link when exposed to curing temperatures. The T_g and other properties can change significantly after exposure to curing temperature.
- *Poorly cured*. Refers to material that has a low T_g or low cross-link density compared to its potential cure level. In this case the material does not continue to cross-link or cure significantly when exposed to curing temperatures. T_g and other properties remain little changed with additional exposure to curing temperatures. This usually occurs due to the action of a contaminant or substance that interferes with curing. In many resin systems, moisture can cause this.
- *Well cured*. Refers to material cured to the point where it achieves its targeted T_g level and level of cross-linking. Note that a well cured material may or may not continue to form some additional cross-link bonds when exposed to curing temperatures, depending on the polymer and catalyst system.
- *Fully cured*. A fully cured material will not form significant new cross-link bonds when exposed to curing temperatures. Note that a poorly cured material as just defined is also fully cured in the sense that additional exposure to curing temperatures will not promote additional cross-linking.

9.3.1.4 Advantages and Disadvantages of High T_g Values. Implicit in many discussions of T_g is the assumption that higher values of T_g are always better. This is not always the case. While it is certainly true that higher values of T_g will delay the onset of high rates of thermal expansion for a given resin system, total expansion can differ from material to material. A material with a lower T_g could exhibit less total expansion than a material with a higher T_g, due to differing resin CTE values or by incorporating fillers into the resin

system that lower the CTE of the composite material. This is illustrated in Fig. 9.5. Material C exhibits a higher T_g than material A, but material C exhibits more total thermal expansion because its CTE value above T_g is much higher. On the other hand, with the same CTE values above and below the T_g, the higher-T_g material B exhibits less total thermal expansion than material A. Finally, although the T_g values are the same, material B exhibits less total expansion than material C due to a lower CTE value above T_g. This will be discussed further in Chap. 11 in the context of the impact of lead-free assembly temperatures on base materials.

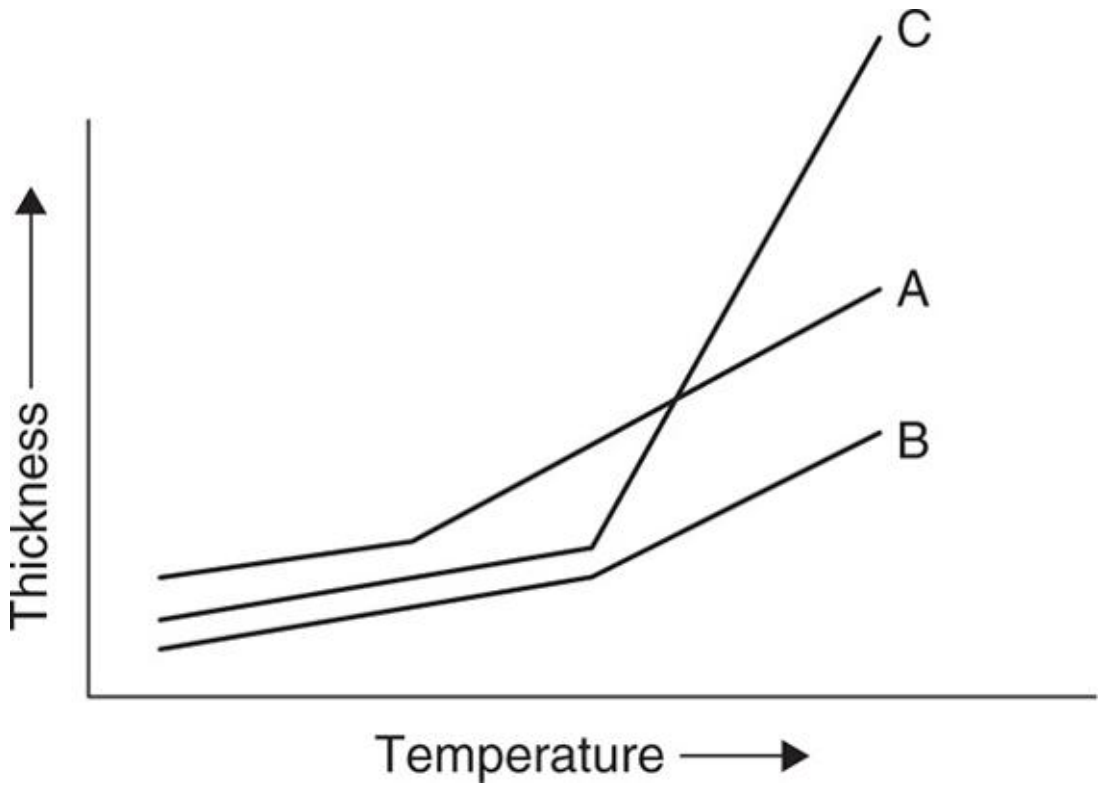


FIGURE 9.5 T_g versus thermal expansion.

Finally, there are other properties to consider when selecting a material. T_g is just one property and very often it is really the expansion properties that are most relevant rather than the actual value of T_g.

T_d is an important property for lead-free assembly, with higher values generally preferred, although once at a certain level, higher T_d's do not offer any further benefit. Advanced FR-4 resin systems can combine both high T_g and high T_d. This will be discussed in detail in Chap. 11.

In addition, higher T_g resin systems can be harder and more brittle than lower T_g systems. This can adversely affect productivity in the printed circuit manufacturing process. In particular, the drilling process can be affected as slower drilling, reduced drill bit life or reduced stack heights can be required for high-T_g materials.

Lower copper peel strength values and shorter times to delamination can also be correlated with higher T_g values, though other factors influence these properties as well. The time to delamination is a measure of the time it takes for the resin and copper, or resin and reinforcement, to separate or delaminate, and can be correlated to T_d. This will also be discussed in Chaps. 10 and 11. This time-to-delamination test utilizes TMA equipment to bring a sample to a specified temperature and then measures the time it takes for failure to occur. Failure is typically delamination between the resin and copper foil, or resin and glass within the laminate. Temperatures of 260°C (T260) and 288°C (T288) are commonly used for this testing.

9.3.2 Decomposition Temperature, T_d

As a material is heated to higher temperatures, a point is reached where the resin system will begin to decompose. The chemical bonds within the resin system will begin to break down and volatile components will be driven off, reducing the mass of the sample. The decomposition temperature, T_d, is a property which describes the point at which this process occurs. The traditional definition of T_d is the point where 5

percent of the original mass is lost to decomposition. However, 5 percent is a very large number when multilayer PCB reliability is considered, and temperatures where lower levels of decomposition occur are very important to understand, particularly with respect to lead-free assembly. To illustrate this, consider Fig. 9.9.

In Fig. 9.6, you can see curves for two FR-4 materials. The "traditional FR-4," a 140°C T_g material in this case, has a decomposition temperature of 320°C by the 5 percent weight loss definition. The "enhanced FR-4" has a decomposition temperature of 350°C by the 5 percent weight loss definition. Most of the dicy-cured high-T_g FR-4 materials used in the past actually have decomposition temperatures in the range of 290 to 310°C, while the 140°C T_{gd} FR-4 materials cured with dicy generally have slightly higher T_d values. The shaded regions indicate the peak temperature ranges for standard tin-lead assembly and lead-free assembly. A very common question is, if a PCB will be assembled at 260°C, and the material has a decomposition temperature of 310–320°C, then why wouldn't it be compatible with lead-free assembly?

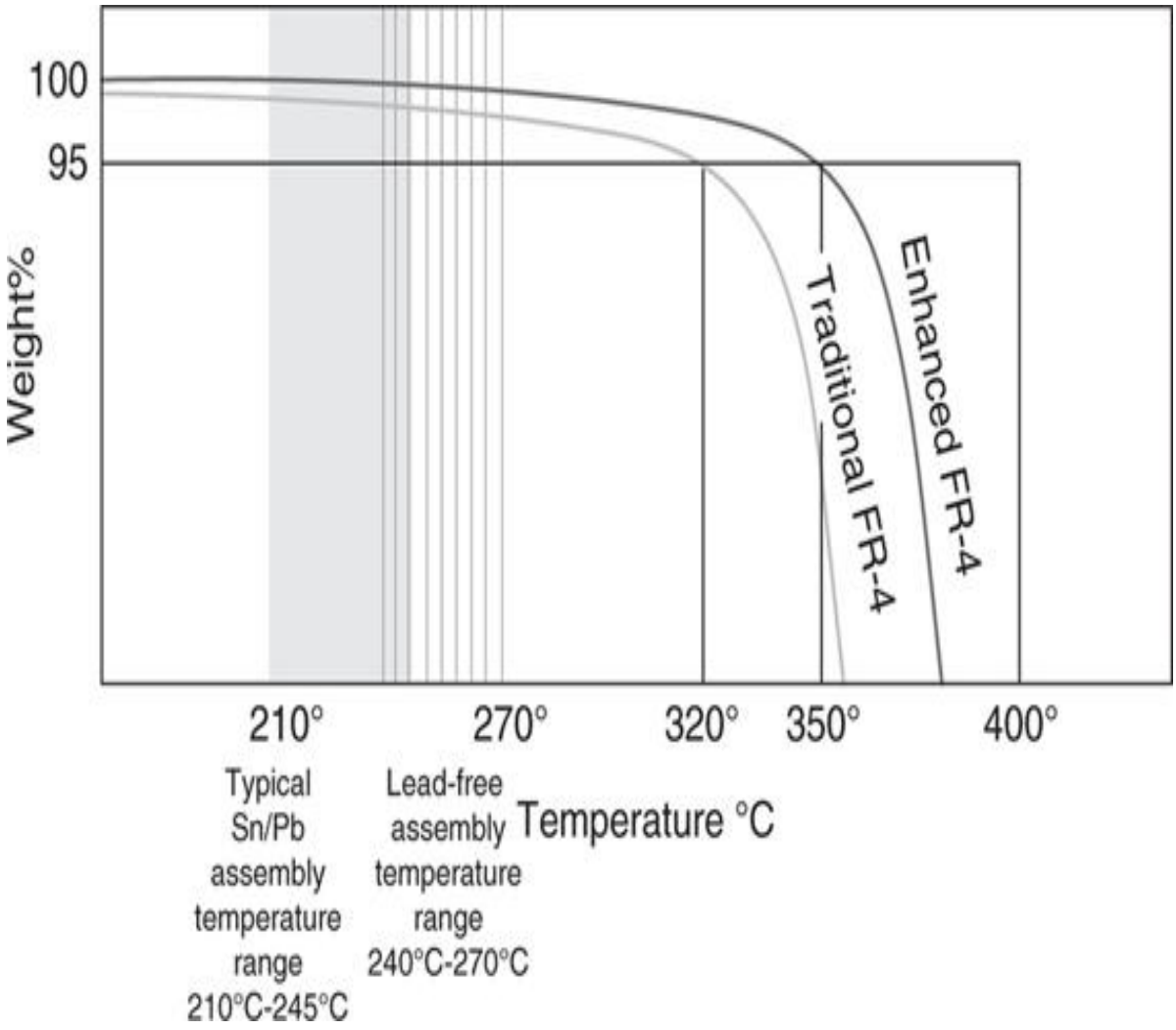


FIGURE 9.6 Illustration of decomposition curves.

The answer lies in the level of decomposition in the temperature ranges where assembly will take place. In the tin-lead temperature range, neither material exhibits a significant level of decomposition. However, in the lead-free assembly temperature range, the traditional FR-4 begins to exhibit 1.5 to 3 percent weight loss. This level of decomposition can compromise long-term reliability or result in defects such as delamination during assembly, particularly if multiple assembly cycles or rework cycles are performed. On the other hand, beyond a certain value, higher levels of T_d do not offer any further benefit. If the peak temperatures a PCB will be subjected to do not approach or exceed the critical range of

decomposition, then specifying a higher value does not provide any value, and may result in the exclusion of materials with good cost-performance value.

9.4 TYPES OF FR-4

As can be seen in Table 9.2, several materials listed are considered FR-4. This begs the question: What is FR-4? In Table 9.2, it can be seen that each material considered FR-4 is flame-resistant, uses a woven fiberglass reinforcement and is primarily an epoxy-based resin system.

9.4.1 Differences between FR-4s

So what can be different about these materials? The most obvious difference between the commercially available FR-4 materials is in T_g values. Specification sheet 21 refers to an FR-4 with a minimum T_g of 110°C. More common are FR-4 materials with T_g values between 130 to 140°C and 170 to 180°C. Therefore, it is obvious that FR-4 materials can consist of different types of epoxy resins. Indeed, there are many types of epoxy resins that will provide differing T_g values, as well as differences in other properties.

Specification sheets 92-95 list FR-4 materials with non-halogen-based flame retardants, as well as different T_g ranges. Sheets 92 and 94 indicate the use of a phosphorus-based flame retardant, whereas sheets 93 and 95 show the use of aluminum hydroxide. So FR-4 may include different types of flame retardants. In addition, several FR-4 materials, such as those shown in sheets 99, 101, and 126, show that these materials contain inorganic fillers. These fillers are often used to reduce the amount of *z*-axis expansion.

9.4.2 The Longevity of FR-4

FR-4 materials have been the most successful, most commonly used materials in printed circuit manufacturing for many years. Why? Well, as we just discussed above, FR-4 actually encompasses a range of material types, even though they share certain properties and are primarily epoxy based. The result is that there is often an FR-4 material readily available for the most common end-use applications. For relatively simple applications, the 130 to 140°C T_g FR-4s have become the material of choice. In higher layer count multilayer circuits, in very thick circuits, as well as those requiring improved thermal properties, the 170 to 180°C T_g FR-4s have become the material of choice, although properties beside the T_g must also be considered in these applications.

In addition, the components used in FR-4 materials, particularly woven fiberglass cloth and epoxy resins, provide a very good combination of performance, processability, and cost. The range of woven fiberglass cloth styles available makes it easy to control dielectric and overall circuit thicknesses. As noted earlier, the range of epoxy resin types also makes it relatively simple to tailor material properties to end-use applications. The combination of good electrical, thermal, and mechanical properties of epoxies also explains why they have become the primary type of resin used in printed circuits. Epoxy-based materials are also relatively easy to process through conventional printed circuit manufacturing processes, at least in comparison to some of the other types of materials available.

9.4.3 UL Reclassification of FR-4: FR-4.0 and FR-4.1

Originally, FR-4 materials were brominated epoxy resins with fiberglass cloth reinforcement. As just noted, as the range of applications with varying performance criteria increased, many

variants of these components were introduced in order to meet the needs of the different applications. The result was a range of materials with somewhat different compositions and differing levels of performance, even though all were called FR-4. As a result, Underwriters Laboratories (UL) initiated a reclassification of FR-4 into FR-4.0 and FR-4.1.

FR-4.0 is the category for the original brominated epoxy based materials while FR-4.1 consists of resin systems with a non-halogen-based flame retardant. For FR-4.1, there are limits on bromine, chlorine and total bromine plus chlorine contents. The limit is 900 parts per million (ppm) each for bromine and chlorine, with the total not to exceed 1500 ppm. For the resin system, both categories must contain at least 50 percent epoxy resin, and a maximum inorganic filler content of 45 percent. Inorganic fillers would include silica, talc, clay, aluminum hydroxide, ceramics and other types of inorganic particles. Woven fiberglass cloth is still the reinforcement type for both categories.

9.5 LAMINATE IDENTIFICATION SCHEME

As IPC specifications are regularly reviewed and updated, it is recommended that the latest IPC specification be used for actual applications. However, an example of a laminate designation in IPC-4101 is

L	25	1500	C1/C1	A	A
Material Designator	Specification Sheet Number	Nominal Laminate Thickness	Metal Cladding Type and Nominal	Thickness Tolerance Weight/Thickness	Surface Quality Class

Material designator. "L" refers to laminate.

Specification sheet number. This designation references the specification sheet number as in Table 9.2.

Nominal laminate thickness. Four digits identify this variable. It may be specified either over the cladding or over the dielectric. For metric specification, the first digit represents whole millimeters, the second represents tenths of millimeters, and so on. For orders requiring Imperial units, the four digits indicate the thickness in ten-thousandths of an inch (tenths of mils). In the example shown, 1500 is designated for a thickness of 1.5 mm, which would be specified as 0591 when using Imperial units.

Metal cladding type and nominal weight/thickness. Five designators are used to specify cladding type and thickness. The first and fourth indicate the type, the second and fifth indicate thickness, and the third is a slash to differentiate sides of the base material. Table 9.5 lists the types of metal cladding. Table 9.6 lists copper foil weights and thicknesses.

TABLE 9.5 Metal Cladding Types Summarized in IPC-4101 (see also IPC-4562, Metal Foil for Printed Wiring Applications)[2]

Designation	Metal Cladding Type
A	Copper, wrought, rolled (IPC-4562, grade 5)
B	Copper, rolled (treated)
C	Copper, electrodeposited (IPC-4562, grade 1)
D	Copper, electrodeposited, double treat (IPC-4562, grade 1)
G	Copper, electrodeposited, high ductility (IPC-4562, grade 2)
H	Copper, electrodeposited, high temperature elongation (IPC-4562, grade 3)
J	Copper, electrodeposited, annealed (IPC-4562, grade 4)
K	Copper, wrought, light cold rolled (IPC-4562, grade 6)
L	Copper, wrought, annealed (IPC-4562, grade 7)
M	Copper, wrought, rolled, low temperature annealable (IPC-4562, grade 8)
N	Nickel
O	Unclad
P	Copper, electrodeposited, high temperature elongation, double treat (IPC-4562, grade 3)
R	Copper, reverse treated electrodeposited (IPC-4562, grade 1)
S	Copper, reverse treated electrodeposited, high temperature elongation (IPC-4562, grade 3)
T	Copper, copper foil parameters as dictated by contract or purchase order
U	Aluminum
X	As agreed between user and supplier
Y	Copper Invar Copper
Z	Copper, electrodeposited, high temperature elongation, double-treat (IPC-4562, grade 3) for buried capacitance applications

TABLE 9.6 Foil Weights and Thicknesses from IPC-4101 (see also IPC-4562, Metal Foil for Printed Wiring Applications)[4]

		Metric		English		
Foil Designator	Common Industry Terminology	Area Weight (g/m^2)	Nominal Thickness (mm)	Area Weight (oz/ft^2)	Area Weight ($g/254\ in.^2$)	Nominal Thickness (10^{-3} in)
E	5 µm	45.1	5.1	0.148	7.4	0.20
Q	9 µm	75.9	8.5	0.249	12.5	0.34
T	12 µm	106.8	12.0	0.350	17.5	0.47
H	1/2 oz	152.5	17.1	0.500	25.0	0.68
M	3/4 oz	228.8	25.7	0.750	37.5	1.01
1	1 oz	305.0	34.3	1	50.0	1.35
2	2 oz	610.0	68.6	2	100.0	2.70
3	3 oz	915.0	102.9	3	150.0	4.05
4	4 oz	1220.0	137.2	4	200.0	5.40
5	5 oz	1525.0	171.5	5	250.0	6.75
6	6 oz	1830.0	205.7	6	300.0	8.10
7	7 oz	2135.0	240.0	7	350.0	9.45
10	10 oz	3050.0	342.9	10	500.0	13.50
14	14 oz	4270.0	480.1	14	700.0	18.90

Thickness tolerance class. This variable references the thickness tolerance as agreed between user and supplier (see Table 9.7). Classes A, B, and C refer to measurement by micrometer of the base material without cladding. Class D requires measurement by microsection (see Fig. 9.7). Classes K, L, and M refer to measurement by micrometer of the base material with the metal cladding.

TABLE 9.7 Base Laminate Thickness Tolerances from IPC-4101

Nominal Thickness of Laminate, mm [in.]	Class A/K mm [in.]	Class B/L mm [in.]	Class C/M mm [in.]	Class D mm [in.]
0.025 to 0.119 [0.0009 to 0.0047]	±0.025 [±0.000984]	±0.018 [±0.000709]	±0.013 [±0.000512]	−0.013 [−0.000512] +0.025 [+0.000984]
0.120 to 0.164 [0.0047 to 0.0065]	±0.038 [±0.00150]	±0.025 [±0.000984]	±0.018 [±0.000709]	−0.018 [−0.000709] +0.030 [+0.00118]
0.165 to 0.299 [0.0065 to 0.0118]	±0.050 [±0.00197]	±0.038 [±0.000150]	±0.025 [±0.000984]	−0.025 [−0.000984] +0.038 [+0.00150]
0.300 to 0.499 [0.0118 to 0.0196]	±0.064 [±0.00252]	±0.050 [±0.00197]	±0.038 [±0.00150]	−0.038 [−0.00150] +0.050 [+0.00197]
0.500 to 0.785 [0.0197 to 0.0309]	±0.075 [±0.00295]	±0.064 [±0.00252]	±0.050 [±0.00197]	−0.050 [−0.00197] +0.064 [+0.00252]
0.786 to 1.039 [0.0309 to 0.04091]	±0.165 [±0.006496]	±0.10 [±0.00394]	±0.075 [±0.00295]	—
1.040 to 1.674 [0.04091 to 0.06594]	±0.190 [±0.007480]	±0.13 [±0.00512]	±0.075 [±0.00295]	—
1.675 to 2.564 [0.06594 to 0.10094]	±0.23 [±0.00906]	±0.18 [±0.00709]	±0.10 [±0.00394]	—
2.565 to 3.579 [0.10094 to 0.14091]	±0.30 [±0.0118]	±0.23 [±0.00906]	±0.13 [±0.00512]	—
3.580 to 6.35 [0.14094 to 0.250]	±0.56 [±0.0220]	±0.30 [±0.0118]	±0.15 [±0.00591]	—

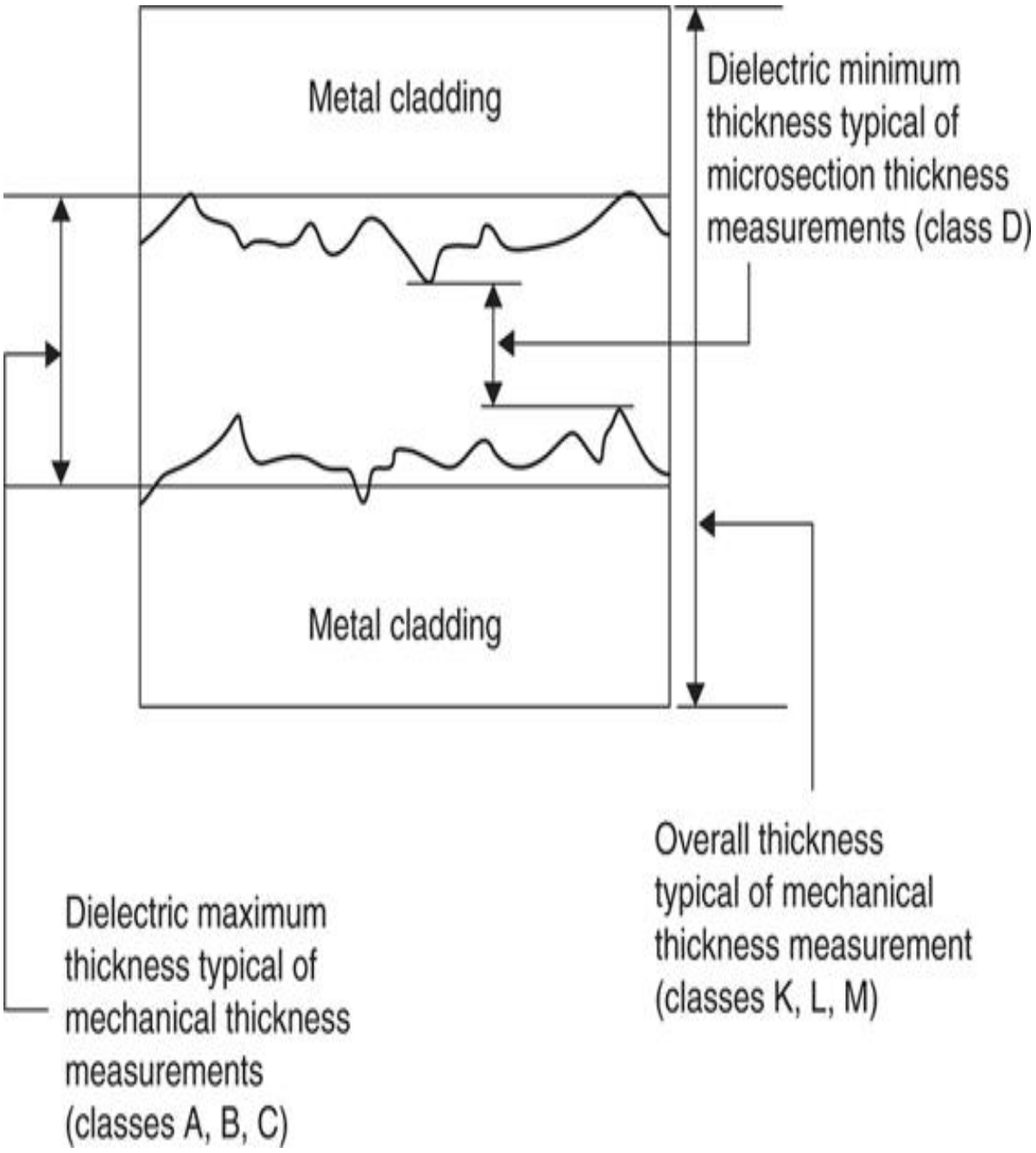


FIGURE 9.7 Dielectric minimum thickness measurements by microsection. (*From IPC-4101*.)

Surface quality class. This class is identified by either A, B, C, D, or X (as agreed upon between user and supplier). Specimens are examined with normal or corrected 20/20 vision. The worst 50 mm × 50 mm (1.97 in. × 1.97 in.) is examined at 10× magnification. Indentations are located

visually using normal or corrected 20/20 vision. The longest dimension of each foil indentation in a specimen is measured with a suitable reticule on a minimum 4× magnifier, with referee inspections at 10×. A point value is allocated according to the longest dimension, as shown in Table 9.8. Surface quality class is determined by the total point count of foil indentations within 300 mm × 300 mm (11.81 in. × 11.81 in.), as shown in Table 9.9.

TABLE 9.8 Pit and Dent Point Values from IPC-4101

Longest Dimension, mm (in)	Point Value
0.13–0.25 mm (0.005–0.009)	1
0.26–0.50 mm (0.009–0.019)	2
0.51–0.75 mm (0.019–0.029)	4
0.76–1.00 mm (0.029–0.039)	7
>1.00 mm (0.039)	30

TABLE 9.9 Surface Quality Grades from IPC-4101

Surface Quality Class	Maximum Point Count	Other Requirements
Class A	29	
Class B	17	
Class C	5	Longest dimensions </=380 µm (14.96 mil)
Class D	0	Longest dimensions <125 µm (4.92 mil) Resin spots = 0
Class X	As agreed between user and supplier (AABUS)	

9.6 PREPREG IDENTIFICATION SCHEME

An example of a prepreg identification in IPC-4101 is

P	25	E7628	TW	RE	VC
Material Designator	Specification Sheet	Reinforcement Style Number	Resin Content Method	Flow Parameter Method	Optional Prepreg Method

Material designator. P refers to prepreg.

Specification sheet number. This designation references the specification sheet number as in Table 9.2.

Reinforcement style. The reinforcement type and style of prepreg is indicated by five digits based on the chemical type and style. In the example, E refers to E-glass and 7628 is the glass fabric style.

Resin content method. This variable refers to the method used to specify resin content of a prepreg. The two methods are RC, which refers to percent resin content of the prepreg, and TW, which refers to the treated weight of the prepreg. A 00 designator would indicate that no method is specified.

Flow parameter method. This variable indicates how much the resin in the prepreg will flow under specified conditions—a critical property. The options are

MF: resin flow percent
SC: scaled flow thickness
NF: no flow
RE: rheological flow
DH: delta H
PC: percent cure
00: no method specified

Optional prepreg method. Other test methods may also be designated here. These include

VC: volatile content
DY: dicy inspection
GT: gel time
00: none specified

The choice of test methods and their required nominal values and tolerances are normally agreed upon between user and supplier.

In addition to properties on the specification sheets, IPC-4101 includes class specifications for other properties as well. These include length and width, bow and twist, and thermal conductivity, among others.

9.7 LAMINATE AND PREPREG MANUFACTURING PROCESSES

While there are a few different processes that can be used to integrate the components that make up printed circuit base materials, the overwhelming majority of materials are manufactured using a common process. In recent years, however, new techniques have been developed and continue to be developed. These new processes have been designed to either lower the cost of manufacturing or to improve material performance, or both. Common to all processes is the need to manufacture a copper clad laminate and the bonding sheets or *prepregs* used to manufacture multilayer circuits.

9.7.1 Conventional Manufacturing Processes

The overall conventional manufacturing process is illustrated in Fig. 9.8. This process can be subdivided into two processes: prepreg manufacturing and laminate manufacturing. Prepreg is also called *B-stage* or bonding sheets, while laminate is sometimes called *C-stage*. The terms B-stage and C-stage refer to the degree to which the resin system is polymerized or cured. B-stage refers to a state of partial cure. B-stage is designed to melt and continue polymerizing when it is exposed to sufficient temperatures. C-stage refers to a state of “full” cure (typically we never realize *full* cure, in the sense that not all reactive sites on the resin molecules have cross-linked; however, we use the term *full cure* to mean that the overwhelming majority of such sites have reacted and additional exposure to temperature will do little to advance the state of cure).

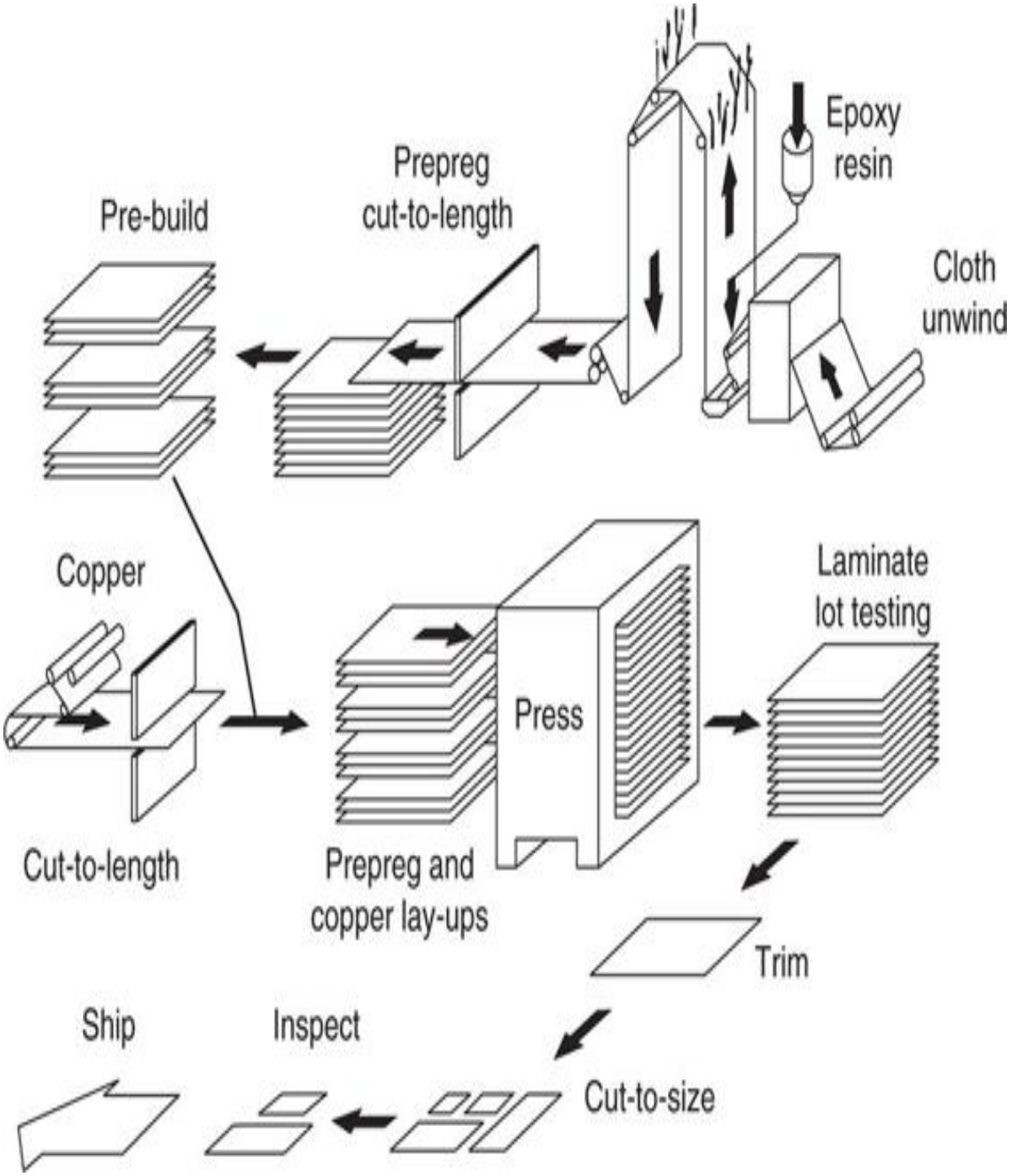


FIGURE 9.8 The conventional manufacturing process.

9.7.2 Prepreg Manufacturing

The first step in most of these processes involves coating a resin system onto the chosen reinforcement, most commonly a

woven fiberglass cloth. Rolls of fiberglass cloth or alternative reinforcement type are run through equipment called *treaters*. Figure 9.9 shows some of the resin system components that are mixed and aged prior to application to the fiberglass cloth. Figure 9.10 illustrates the overall treating process. The fiberglass cloth is drawn through a pan containing the resin system and then precise metering rolls help control thickness and also push resin into the yarns of the glass cloth (see Fig. 9.11).

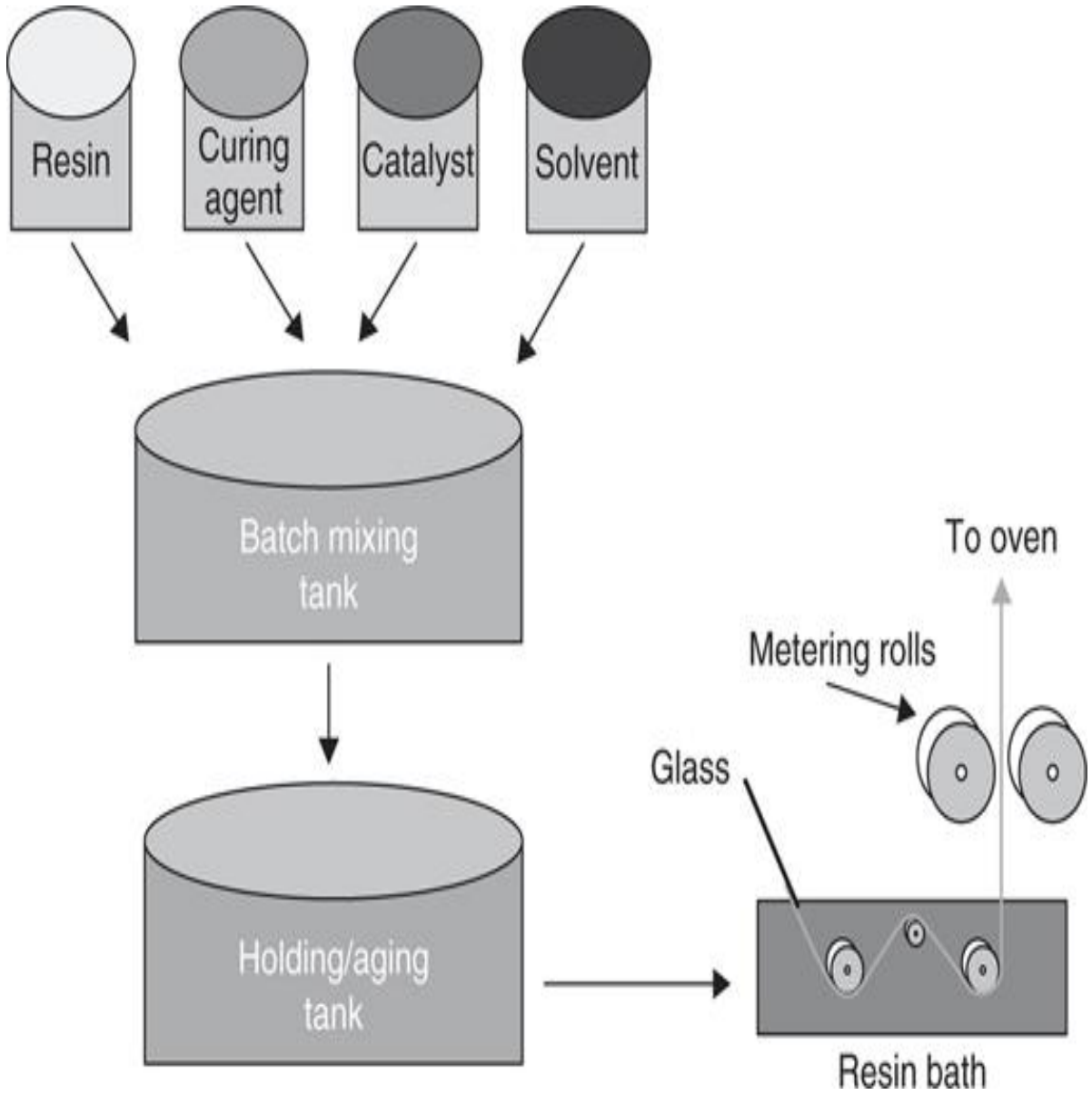


FIGURE 9.9 Resin mixing, aging, and treating.

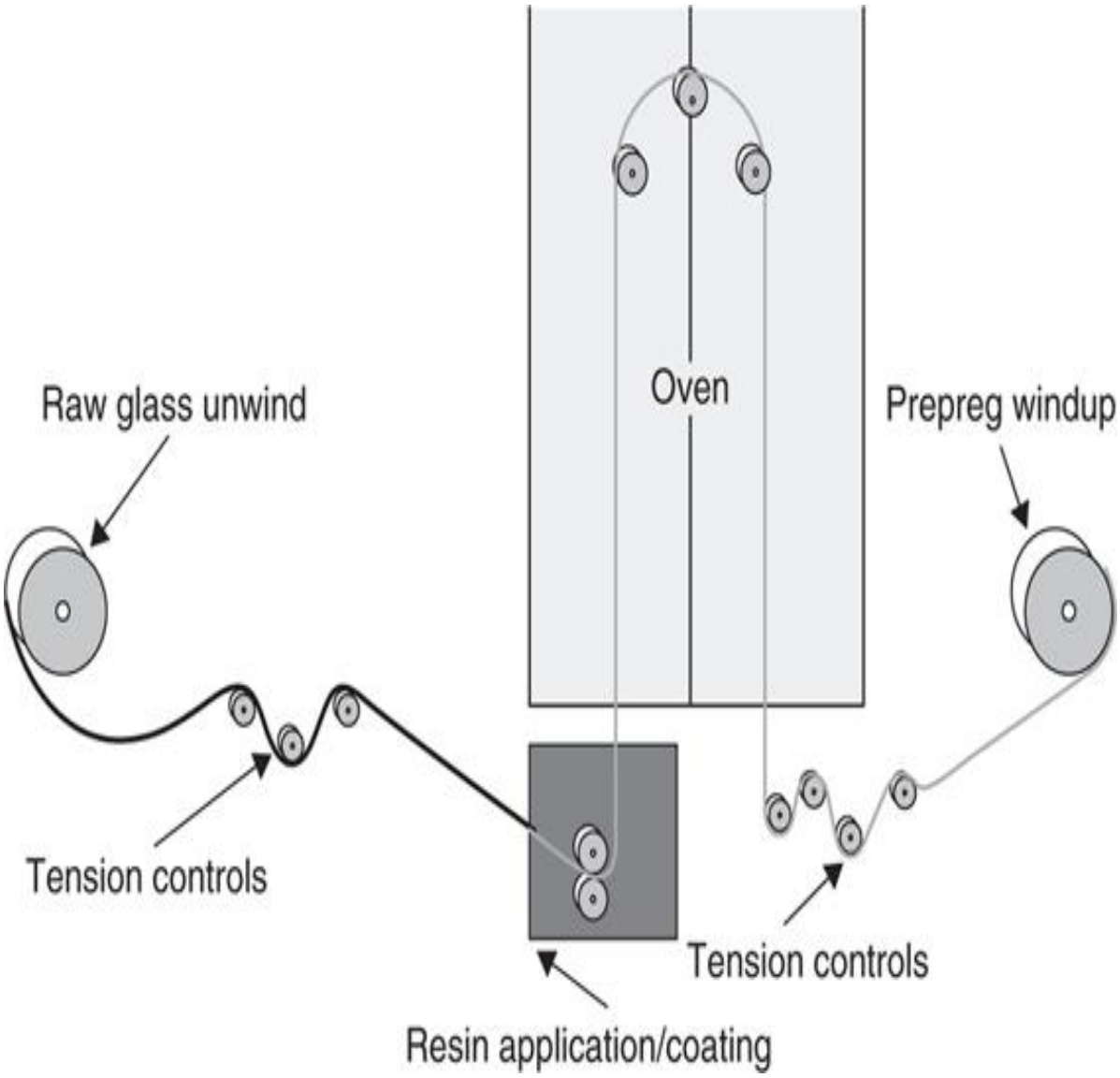


FIGURE 9.10 “Treating” fiberglass cloth with resin.

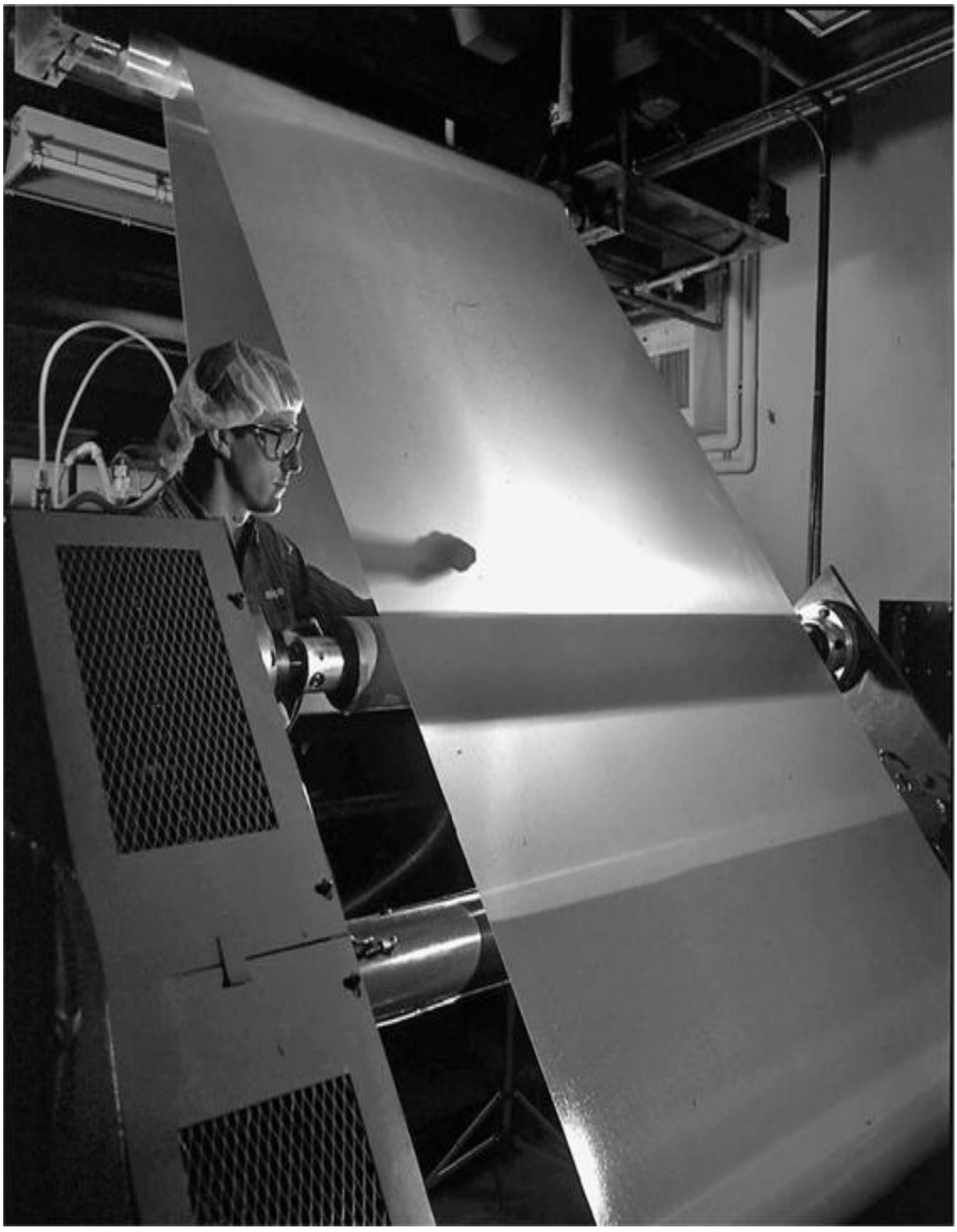


FIGURE 9.11 Prepreg after treating with resin.

Next the cloth is pulled through a series of heating zones. These heating zones commonly utilize forced air convection,

infrared heating, or a combination of the two. In the first set of zones, solvent used to carry the resin system components is evaporated off. Subsequent zones are dedicated to partially curing the resin system, or B-staging the resin. Finally, the prepreg is then rewound into rolls or cut into sheets.

A number of process controls are required in this operation. The concentrations of the resin system components must be controlled and the viscosity of the resin system maintained within acceptable limits. Tension on the cloth as it is pulled through the treater is also important, for among other reasons, it is vital not to distort the weave pattern of the cloth. Control of the resin-to-glass ratio or resin content, the degree of cure of the resin and cleanliness are also critical.

Because the resin system at this point is only partially cured, prepregs must typically be stored in temperature- and humidity-controlled environments. Temperature, for obvious reasons, could affect the degree of cure of the resin and therefore its performance in laminate or multilayer circuit pressing. Since moisture can affect the performance of many curing agents and accelerators, not to mention the performance of the resin system during lamination or press cycles, humidity is also important to control during prepreg storage. Absorbed moisture that becomes trapped during lamination cycles can also lead to blisters or delaminations within the laminate or multilayer circuit.

9.7.3 Laminate Manufacturing

The process of copper clad laminate manufacturing begins with the prepreg material. Prepregs of certain fiberglass cloth styles and specific resin contents are combined with the desired copper foils to make the finished laminate. First, the prepregs and copper foils are sheeted to the desired size. Figure 9.12 shows an automated copper-sheeting process.

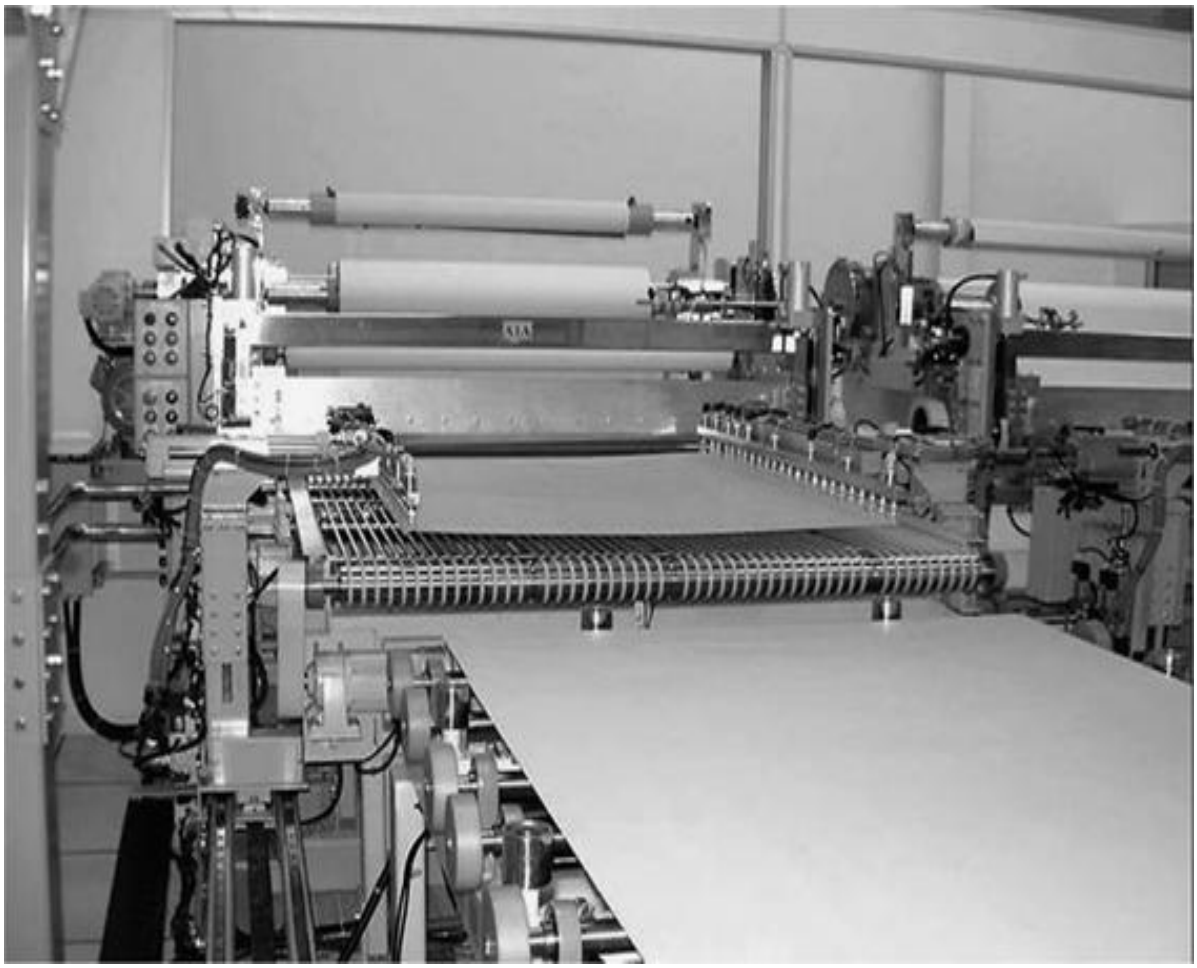


FIGURE 9.12 Sheeting of rolls of copper foil.

These materials are then laid up in the proper sequence to produce the desired copper clad laminate. Figures 9.13 and 9.14 are examples of an automated build-up process where the prepreg and copper foil materials are combined prior to being pressed together. Several of these individual sandwiches of prepreg and copper foil are stacked on top of each other, typically separated by stainless steel plates, although other separator materials, including aluminum, can also be used. These stacks are then loaded into multi-opening lamination presses (see Figs. 9.15 and 9.16), where pressure, temperature, and vacuum are applied. The specific press cycle used will vary depending upon the particular resin system, the degree of cure of the prepregs and other factors. The presses themselves have many platens that can be heated by steam or

hot oil that flows through the platens, or they can also be heated electrically.

FIGURE 9.13 Automated build-up of copper and prepreg.

FIGURE 9.14 Automated build-up of copper and prepreg.

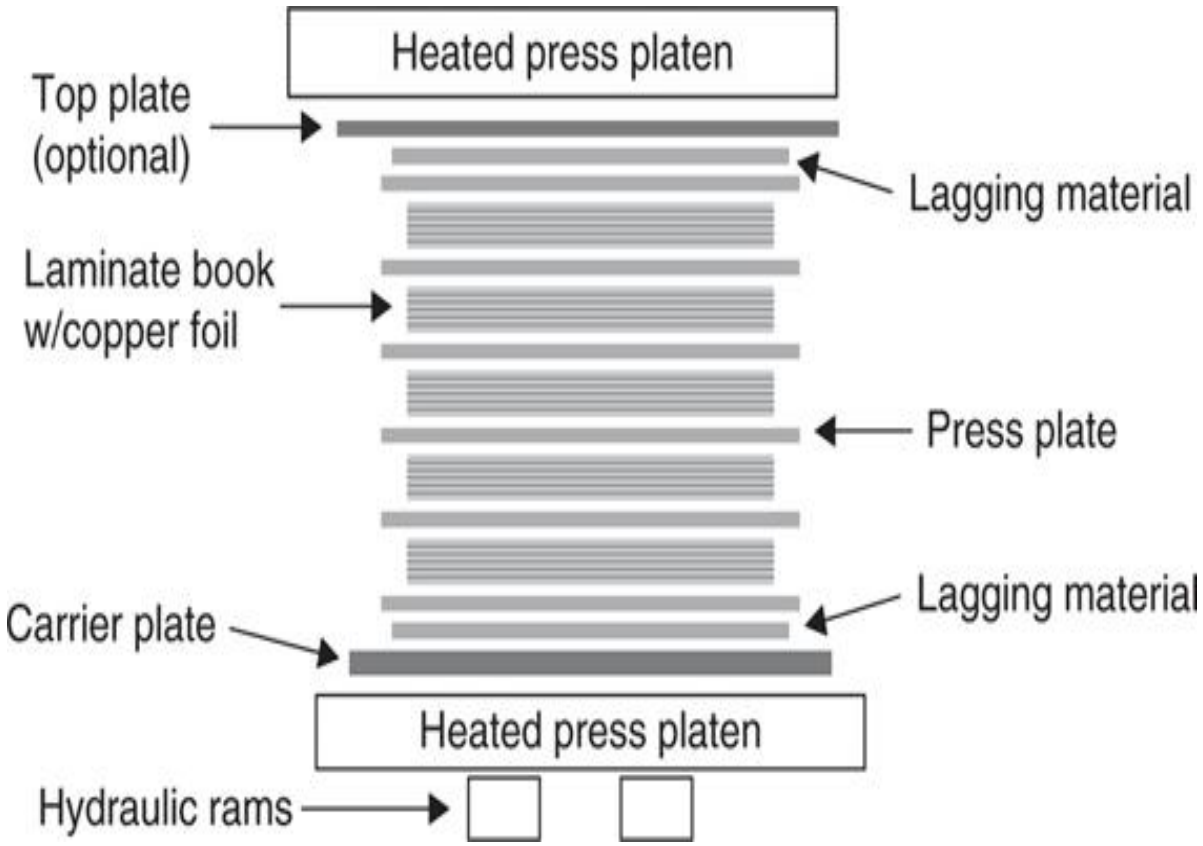


FIGURE 9.15 Laminate pressing.

FIGURE 9.16 Lamination press with multiple openings.

Process controls in the lamination/pressing process are also critical. Cleanliness in the manufacturing environment and cleanliness of the steel separator plates are critical in achieving

good surface quality and in avoiding embedded foreign material within the laminate. Control of the temperature rise during lamination will provide the desired amount of resin flow, while control of the cooldown rate can impact warp and twist. The length of time that the laminate is above the temperature required to initiate the curing reaction will determine the degree of cure, as will the degree to which the actual temperature exceeds this temperature.

While these descriptions of prepreg and laminate manufacturing give a simple description of the processes used, it is important to understand that there are many variables that influence the quality and performance of the finished products. In addition, many of these variables interact with each other, meaning that a change in one may influence others and may require adjustments to these other process variables. In summary, prepreg and laminate manufacturing is much more complex than it appears at first glance.

9.7.4 Direct Current or Continuous Foil Manufacturing

Continuous foil or direct current manufacturing is an alternative method used to manufacture copper clad laminates (see Fig. 9.17). Prepregs are still used in this process, however, the lay-up and pressing operations are somewhat different. In this process, the copper foils are not sheeted, but kept in rolls. To start, copper foil with the side to be bonded to the prepreg facing up, is laid down, while still part of a continuous roll. The prepregs are laid up in the proper sequence, and then the roll of copper foil is passed over the prepregs so that it is applied to the top of what will become the finished laminate. Typically, two rolls of foil are used to allow dissimilar copper weights or types to be bonded to either side of the laminate. A separator plate, typically anodized aluminum, is then placed on top of this sandwich, and the process is repeated so that several laminates are stacked up.

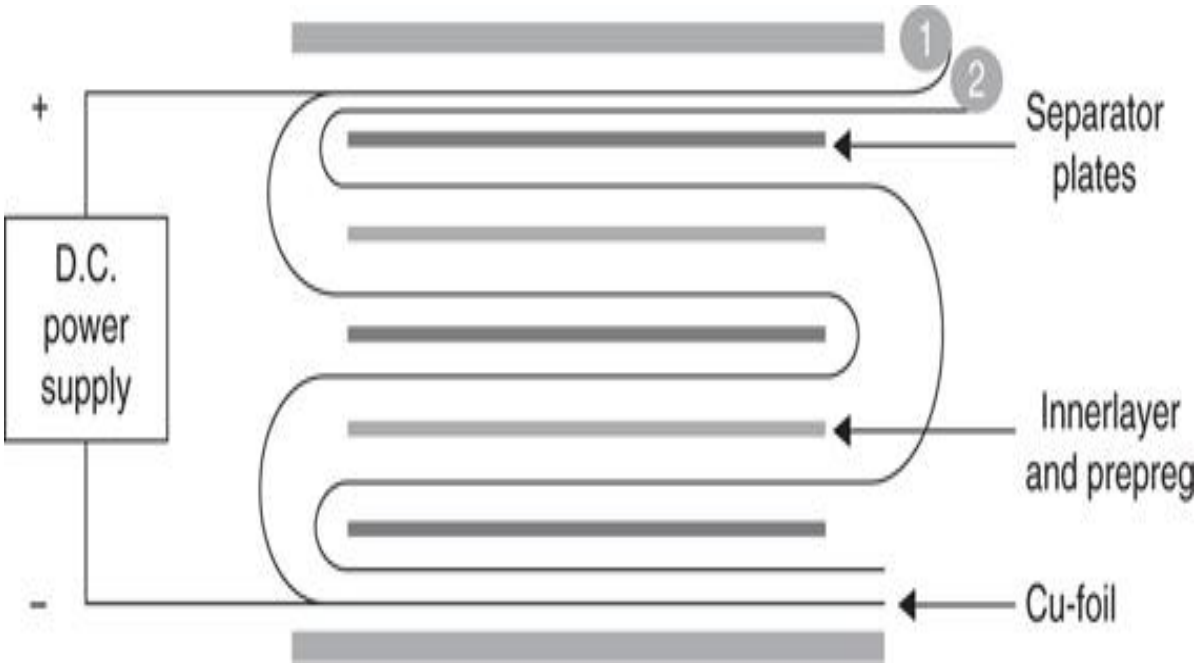


FIGURE 9.17 Laminate pressing with continuous copper foil and direct current heating.

At this point, the stack of laminates is loaded into a press and subjected to heat, pressure, and vacuum. However, as opposed to the conventional process, this technique involves applying direct current to the copper foil that runs throughout the stack. The current heats the foil and therefore the prepregs are adjacent to the foils. By controlling the amount of current, you control the temperature of the materials in the stack.

9.7.5 Continuous Manufacturing Processes

Over the years, continuous lamination processes have also been designed. Rather than cut the prepregs and foils into sheets, lay them up and press them as individual laminates, these processes use rolls of prepreg or bare fiberglass cloth and rolls of copper foil that are continuously unwound and fed together into a continuous horizontal press. One process starts with rolls of prepreg. Another starts with the bare, untreated fiberglass cloth, applies a resin to the cloth and is sandwiched

with the copper foil as it is fed continuously into a horizontal press. At the back end of the press, sections of the continuous laminate can be cut into sheets, or with thin laminates, rolls of copper clad laminate can be manufactured.

9.8 REFERENCES

1. IPC-4101, “Specification for Base Materials for Rigid and Multilayer Printed Boards.”
2. IPC-4103A, “Specification for Base Materials for High Speed/High Frequency Applications.”
3. IPC-4104, “Specification for High Density Interconnect (HDI) and Microvia Materials.”
4. IPC-4562, “Metal Foil for Printed Wiring Applications.”

CHAPTER 10
BASE MATERIAL COMPONENTS

Edward Kelley
Douglas Trobough
Isola Group, Chandler, Arizona

10.1 INTRODUCTION

While there are many types of base materials, there are three basic components:

1. The resin system, including additives and fillers
2. The reinforcement(s)
3. The conductor

Each of these components is important in its own right, and in combination determines the properties of the base material as well as the relative cost of the material. Environmental legislation such as the European Union's Restriction of Hazardous Substances (RoHS) directive has had a profound impact on all levels of the electronics supply chain, including these components. RoHS restricts the use of lead, which is an element in the solder used for component

assembly onto printed circuits. The impact on the base materials and components is primarily the result of higher assembly temperatures that are associated with lead-free assembly. Table 10.1 summarizes the key issues for base material components. The impact of RoHS will be discussed further in Chap. 13.

TABLE 10.1 Lead-Free Assembly Impact on Base Material Components

Component	Lead-Free Assembly Impact	Potential Solutions	Related Considerations
Resin system	1. Peak assembly temperatures can reach point where resin decomposition begins. 2. Higher temperatures result in increased thermal expansion, delamination and stress on plated holes as a result. 3. Vapor pressure of absorbed moisture much higher at lead-free assembly temperatures; can lead to blistering/ delamination. 4. "Phenolic" lead-free compatible materials often not as good for electrical performance, especially Df.	1. Formulate resin system with higher decomposition temperatures. 2. Formulate for lower coefficients of thermal expansion. 3. Evaluate materials for moisture absorption/release characteristics; drying processes in PCB fabrication and/or assembly. 4. Evaluate nondicy/ nonphenolic laminate materials with lower Df.	1. Reformulation can adversely affect electrical properties and manufacturability. 2. Can also impact mechanical properties and manufacturability. 3. PCB storage conditions during manufacturing and prior to assembly are much more important, especially humidity conditions. 4. Cost/performance trade-off. New materials now in high volume use that offer more choices.
Fiberglass cloth	Thermal and mechanical stress on resin-to-glass bond. Volatilized components can also stress this bond.	Cleanliness, moisture resistance and choice of proper coupling agent for resin adhesion more important.	Loss of resin-to-glass adhesion through thermal cycling could impact CAF resistance. Use of spread glass cloth may be beneficial.
Copper foil	Thermal and mechanical stress on resin-to-copper bond.	Improved copper surface treatments for improved adhesion, i.e., coupling agents.	Roughness will impact signal attenuation, especially at high frequencies.

The RoHS directive also restricts specific halogen-containing flame retardants. However, most base materials for printed circuits do not contain the restricted flame retardants. Nevertheless, there is growing interest in halogen-free materials, and this will be discussed further in this chapter.

10.1.1 Epoxy Resin Systems

The most successful and widely used resin systems for printed circuit applications are epoxy resin systems. There are many types of epoxy resins, and this class of resin system continues to be the workhorse among printed circuit board materials. This is a result of the combination of good mechanical, electrical, and physical properties and the relatively low cost of epoxies in comparison to the higher-performance resins. In addition, epoxy systems are relatively easy to process, which aids in keeping manufacturing costs down.

10.1.2 Definition of Epoxy

One of the most common versions of epoxy resin for printed circuit applications is manufactured from reacting epichlorohydrin and bisphenol-A. This reaction is shown in Fig. 10.1. The bromination of the bisphenol-A provides flame retardancy to the finished resin system. Figure 10.2 shows the structure of tetrabromobisphenol-A, or TBBPA. Figure 10.3 shows a reaction used to manufacture brominated epoxy resins. Brominated epoxy resins such as this are the most common component used to incorporate flame retardancy to the finished product, although non-halogen-based flame retardants can also be used, and are discussed in Sec. 10.3.7. The triangular rings on either end of the difunctional epoxy are the epoxide functional groups. In

subsequent resin polymerization, these groups react and result in the curing of the resin system. The –OH groups present on the epoxy molecule also react with the epoxide groups, providing crosslinking among the epoxy molecules (Fig. 10.4).

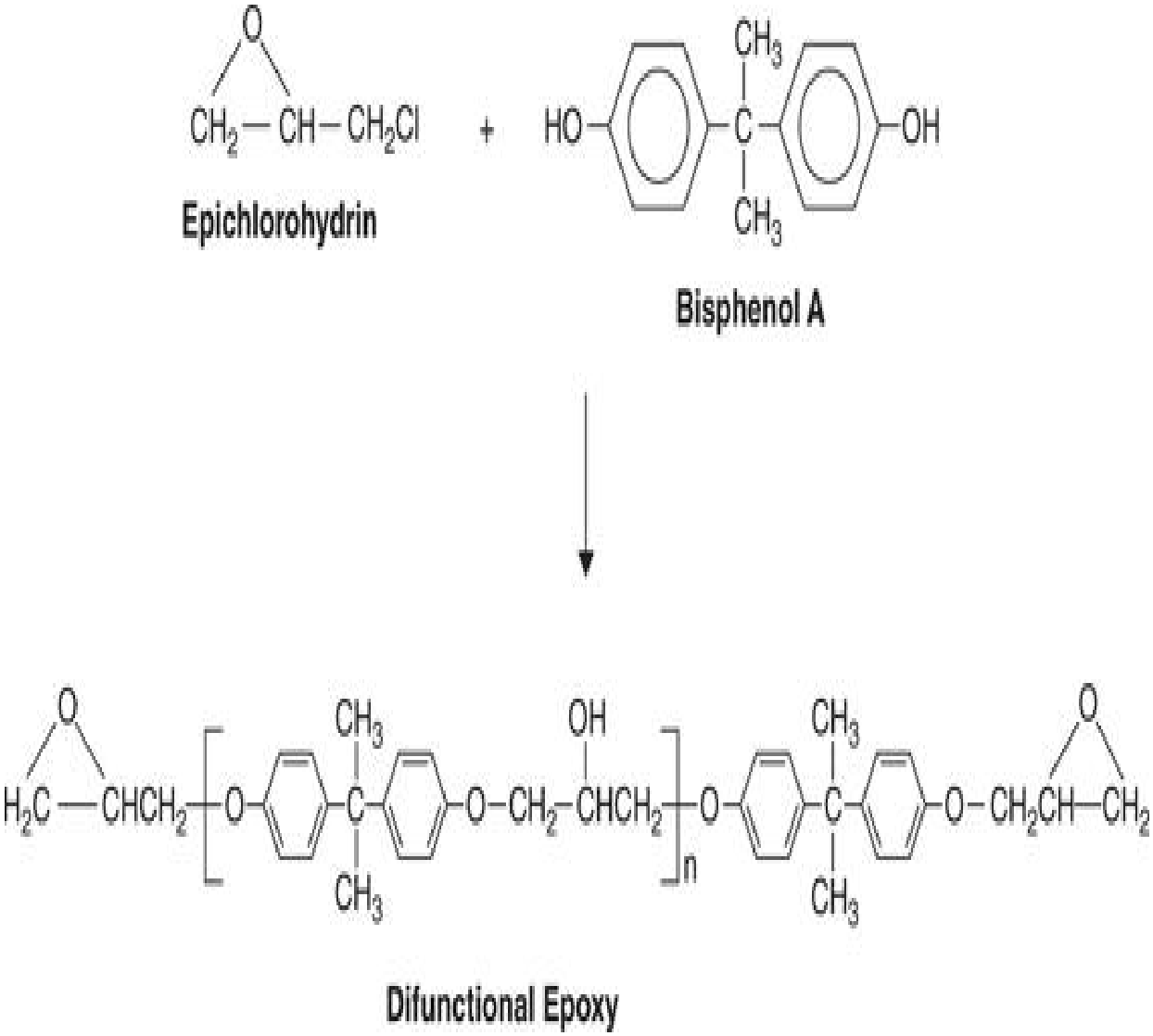


FIGURE 10.1 Reaction to form difunctional epoxy resin.

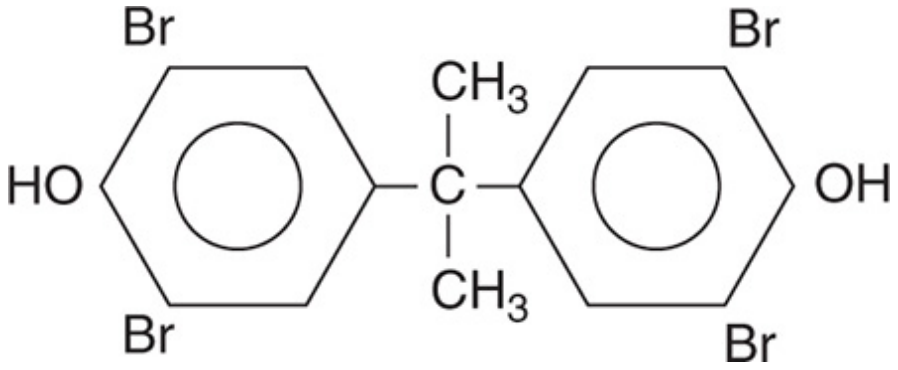
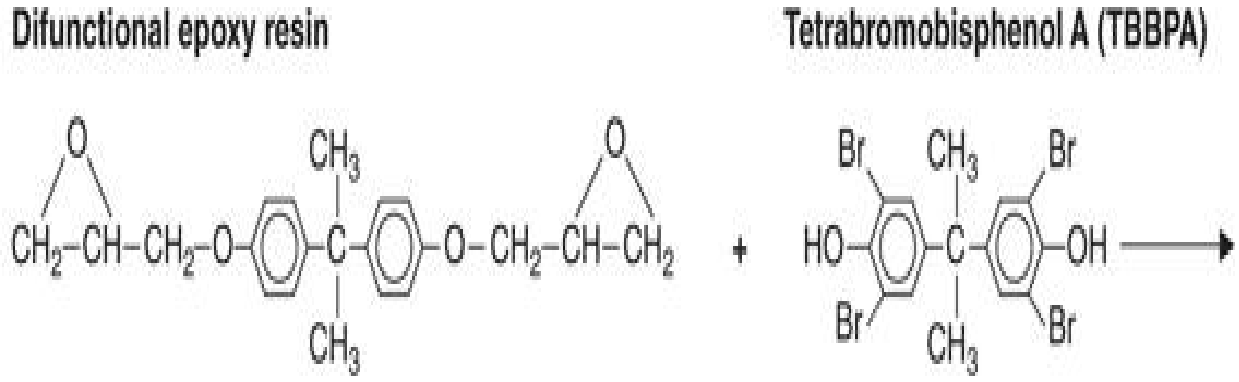


FIGURE 10.2 Tetrabromobisphenol-A (TBBPA).



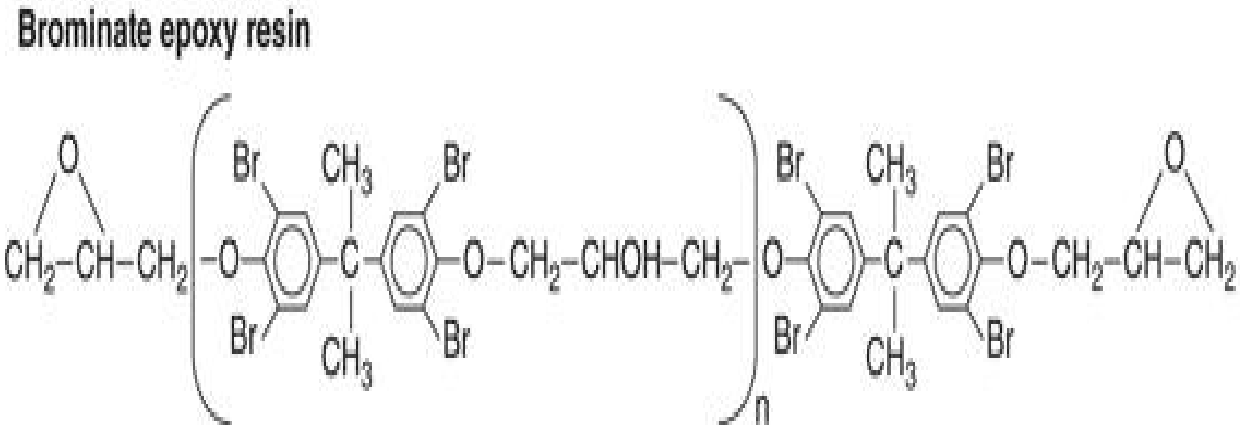


FIGURE 10.3 Brominated difunctional epoxy resin.

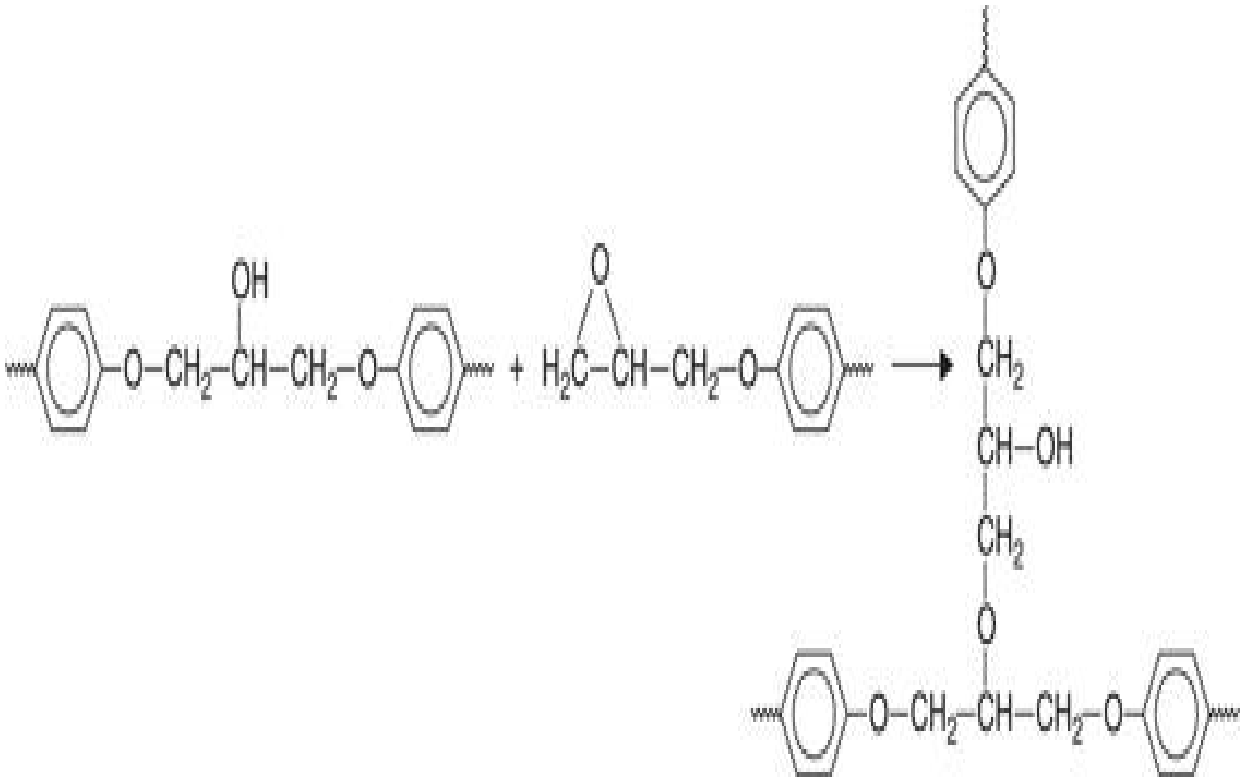


FIGURE 10.4 Crosslinking of –OH and epoxide functional groups.

10.1.3 Difunctional Epoxies

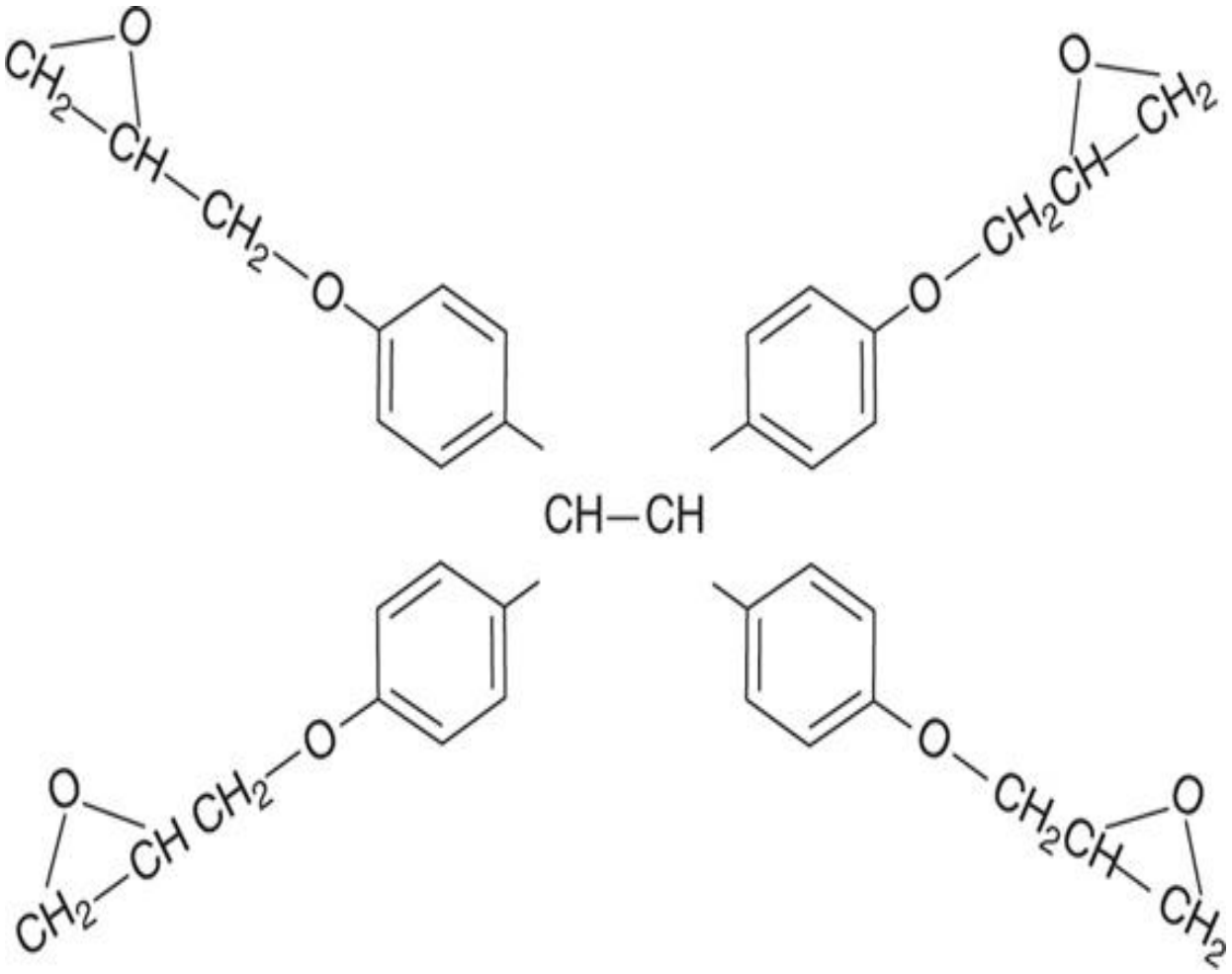
The epoxy resins in Figs. 10.1 and 10.3 are difunctional epoxies. The molecular weight of the epoxy can be varied based on the number of repeating groups shown in the center of the molecule. On either end of the molecule you see the epoxide functional groups. The name *difunctional epoxy* is derived from the fact that there are two epoxide groups, one on either end of the molecule. The molecular weight, the curing agents used to react the resin, and other factors will affect the finished properties of the resin system, including T_g and T_d. The T_g is the temperature at which the resin turns from a rigid or glassy state to a softer, more deformable state. The T_g is important because it affects the thermal and physical properties of the base material and finished circuit board, especially thermal expansion

properties. The T_d is the decomposition temperature and will influence thermal reliability of the printed circuit. These properties are discussed in more detail in Chaps. 11 and 12, and again in Chap. 13 as they relate to compatibility with lead-free assembly processes.

Difunctional epoxies can have a range of T_g's, but are typically below 120°C. These epoxies are sometimes used in relatively unsophisticated products such as simple double-sided printed circuits, but are more commonly blended with other epoxies in higher performance systems.

10.1.4 Tetrafunctional and Multifunctional Epoxies[1]

The use of epoxy compounds with more than two epoxide functional groups per molecule results in greater cross-linking when the resin is cured. Among other things, this results in higher T_g levels. Resin systems with these types of epoxies can exhibit improved thermal and physical properties. However, the curing chemistry will also have an impact on these properties, and often the higher-T_g materials can be harder and more brittle, requiring process adjustments in the printed circuit manufacturing process. Common commercially available laminate materials based on epoxy resin systems can be segmented into a few T_g ranges, 125 to 145°C, 150 to 165°C, and greater than 170°C. There are epoxy systems, or epoxies blended with other resins that have T_g's above 190°C as well. These resin systems may be blends of difunctional, tetrafunctional and multifunctional epoxy resins. Figures 10.5 and 10.6 are examples of tetrafunctional and multifunctional epoxies.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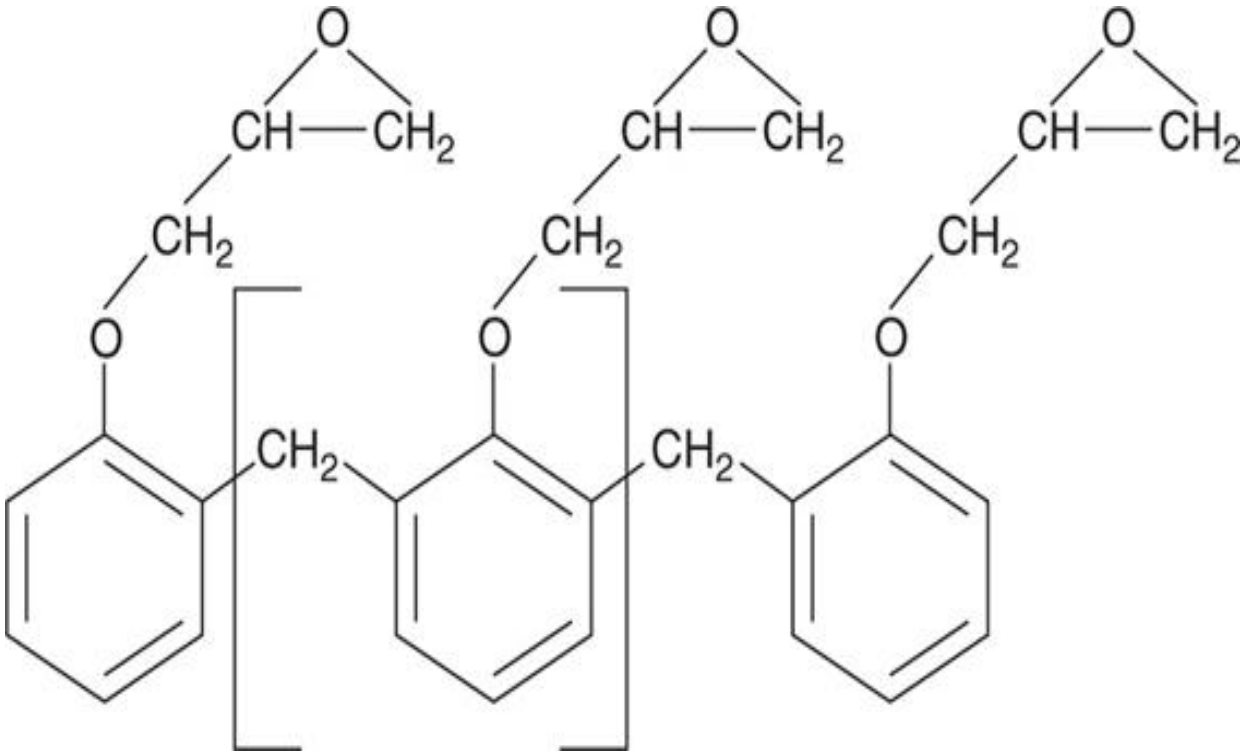


FIGURE 10.6 A multifunctional epoxy phenol novolac resin.

A cost-performance trade-off exists among the commonly used epoxy resin systems. In general, resin systems offering higher levels of T_g and T_d will cost more. In addition, the higher-T_g systems can incur increased circuit manufacturing costs, due primarily to increased multilayer lamination cycle times and decreases in drilling productivity. However, the improvement in performance is often required to meet design and reliability requirements.

10.2 OTHER RESIN SYSTEMS

Many other resin systems are also available. In choosing a resin system, the circuit board designer and fabricator will have to consider what level of performance is needed, as there is typically a strong cost-performance relationship. This cost-performance relationship is driven not only by the base

price of the material itself, but also by the impact the material has on processing costs, both during laminate and prepreg manufacturing, and during printed circuit manufacturing processes.

10.2.1 Epoxy Blends

Blends of epoxy resins with other types of resins have become common in order to tailor material properties, especially for improvements in electrical performance. These are used when performance demands exceed the capabilities of even the high-T_g/T_d epoxies, but where the costs of the highest performance materials cannot be justified. In many cases, the driving force behind these materials is the need for improved electrical properties versus the standard epoxy offerings. Specifically, improvements in the dielectric constant (permittivity) and dissipation factor (loss tangent) are the properties of interest. Materials with lower values for these properties are needed for circuits that operate at high frequencies. A variety of polymers have been used to make these materials; however, many of them are proprietary to a specific material supplier.

Historically, these blends included epoxy-polyphenylene oxide (PPO) (see Fig. 10.7) and epoxy-cyanate ester, as well as epoxy isocyanurate (see Fig. 10.8). However, these materials have become less widely used as new polymers have been adopted. Styrene maleic anhydride (SMA) (Fig. 10.9) is one of these polymers. Besides the improvement in electrical properties, SMA has high heat resistance and high dimensional stability.

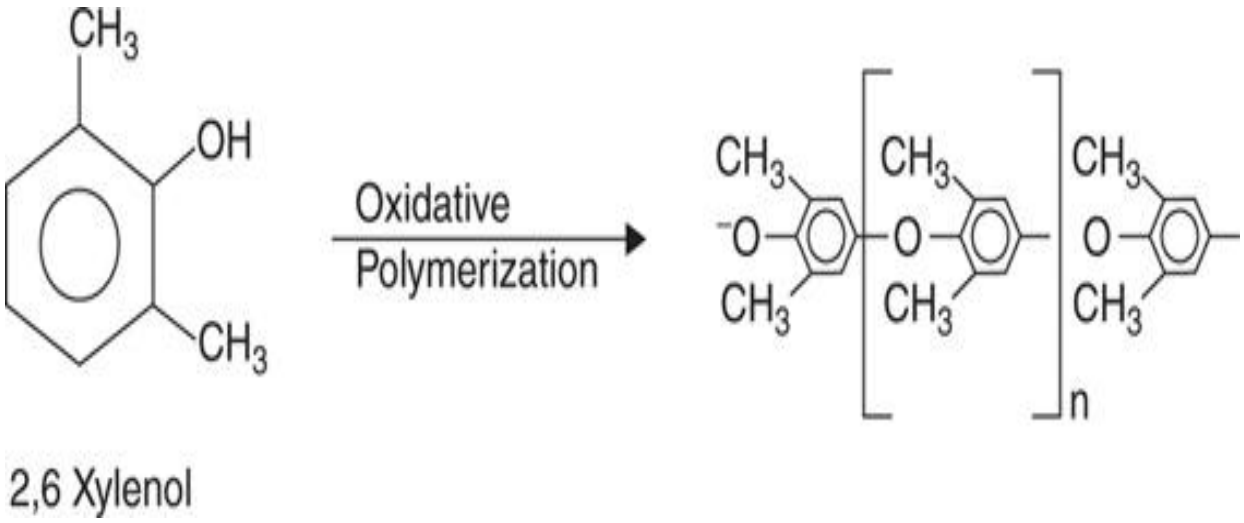


FIGURE 10.7 Polyphenylene oxide (PPO).

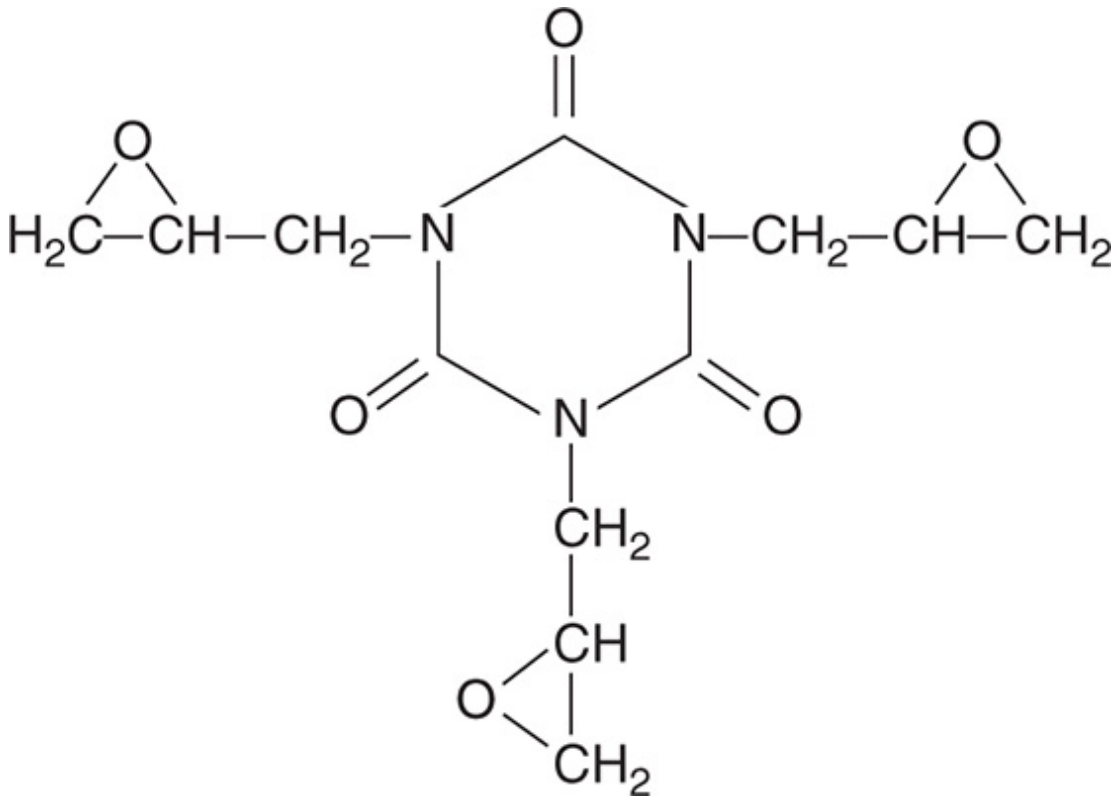


FIGURE 10.8 Epoxy isocyanurate.

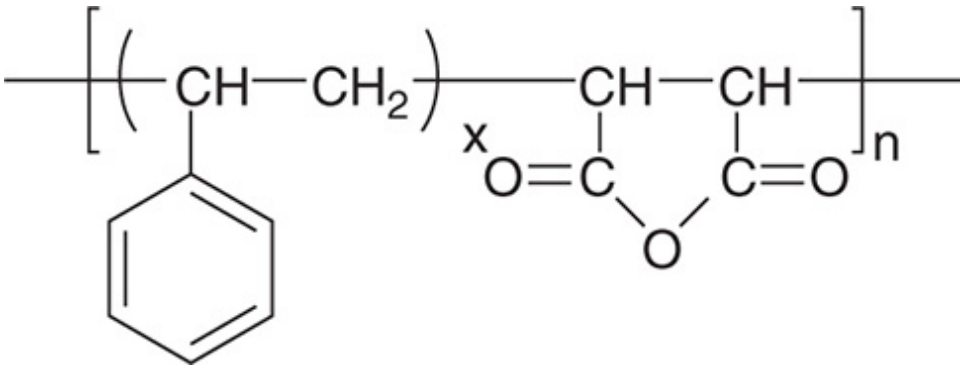


FIGURE 10.9 Styrene maleic anhydride.

While these various resin blends have been developed to minimize impacts to common printed circuit manufacturing processes, they can impact productivity in multilayer lamination and drilling and can require special desmear and hole wall conditioning processes, depending on the design of the printed circuit and fabrication process used. On the other hand, they may have less of an impact to these processes when compared to the even higher performance materials.

These epoxy blends are often used in high frequency applications including communications equipment, servers, storage devices and high speed computing applications.

10.2.2 Bismaleimide Triazine/Epoxy

Typically, epoxy is added to Bismaleimide Triazine (BT) resins in order to modify the properties of pure BT. Therefore these materials are also considered epoxy blends. BT/epoxies normally have T_g values in the range of 180 to 220°C and exhibit a good combination of electrical, thermal, and chemical resistance properties. BT/epoxy is commonly used in BGA substrates and chip scale packages since it can meet the requirements of specifications for use in semiconductor chip packaging. It can also be used in high-density multilayers requiring good thermal, electrical, and chemical performance.

The primary disadvantage of BT based materials is cost. The greater the amount of BT, the higher the cost. BT can also be more brittle than pure epoxy systems, and moisture absorption can also be higher.

10.2.3 Cyanate Ester

Cyanate ester systems possess very high T_g values, typically in the neighborhood of 250°C, and exhibit good electrical performance. Thermal stability is also good. However, cyanate esters are relatively expensive and require special processing which can add additional cost to the finished circuit. They can also be very sensitive to moisture. For these reasons, cyanate ester materials are used only in niche applications, and alternate resin systems have been introduced with more desirable properties. Blends with epoxies have also been used to modify processability, electrical performance, and cost.

10.2.4 Polyimide

When extreme heat resistance is required, polyimide resins offer outstanding performance. With a T_g of 260°C for the purest systems to 220°C for modified or toughened systems, and very high decomposition temperatures, circuits manufactured with polyimide materials exhibit very high levels of thermal reliability. The high T_g of these resin systems also helps to minimize thermal expansion, as most of the thermal expansion occurs pre-T_g, where expansion rates are relatively low. These materials have commonly been used in burn-in boards, aerospace and avionics, down-well oil drilling, and military applications where thermal performance is vital. Again, however, these resin systems

are relatively expensive and more difficult to process, generally limiting them to niche applications.

10.2.5 Polytetrafluoroethylene (Teflon®)

A variety of Polytetrafluoroethylene (PTFE) based products are also available for applications where extremely good electrical properties are required. These materials often require very specialized processing and are relatively expensive. Hybrids of PTFE-based materials and other material types are often used to gain the performance benefits of the PTFE-based materials where needed, while controlling the total circuit cost by using other less costly materials in other layers of the multilayer circuit. PTFE-based materials are commonly used in RF/microwave applications.

10.2.6 Polyphenylene Ether

Polyphenylene Ether (PPE) -based products offer superior electrical properties compared to the epoxy blends discussed above, and also offer excellent thermal performance. This resin system can be used in RF and wireless communications as well as high-speed computing applications. Early versions of these resin systems were difficult to process, but improvements have been made to enable the manufacture of PCBs using conventional PCB manufacturing methods.

10.2.7 Halogen-Free Resin Systems

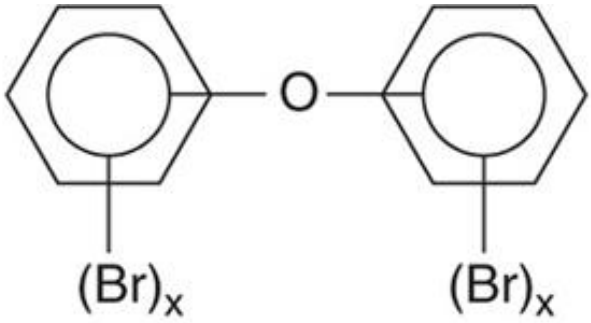
The use of halogen-free resin systems has been increasing. While there has been much discussion about the potential environmental impact of halogenated flame retardants, it

should be noted that the typical halogenated flame retardant used in printed circuits, TBBPA, which is commonly incorporated into a reactive polymer, has been the subject of many toxicology studies and is considered quite safe. In contrast, some other halogenated flame retardants have been restricted, and this will be discussed shortly. But as a result of concerns about halogenated flame retardants generally, some companies have promoted halogen-free alternatives as being better for the environment, so called “green” marketing. The issue to be aware of is that there is a long history of safety in products based on TBBPA chemistry, with less of a history with some of the alternatives. On the other hand, in some cases, using halogen-free chemistry can result in an improvement in electrical performance, specifically a lower dissipation factor. Research and development in this area has increased in recent years, so it is recommended to search the current literature when making decisions about what products to use.

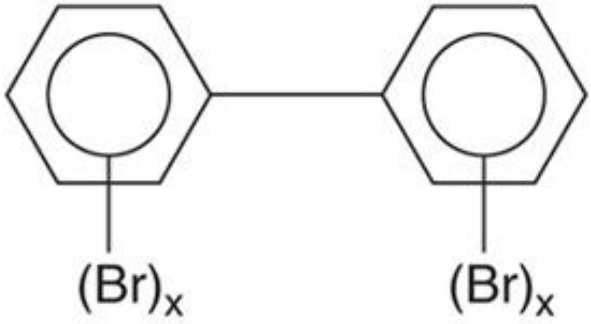
10.3 LEGISLATIVE ISSUES

The European Union’s RoHS and WEEE directives (the WEEE directive addresses waste electronic equipment and recycling requirements) affect not only the lead used in printed circuits, but the flame retardants used in the resin system as well. The RoHS directive restricts the use of specific types of brominated flame retardants. The restricted class of compounds are polybrominated biphenyls (PBBs) and polybrominated biphenyl oxides (PBBOs), also called polybrominated diphenyl ethers (PBDEs). The generic structure of these compounds are shown in Fig. 10.10. Specific compounds within these classes of flame retardants can vary in their toxicity, and given the dynamic nature of legislative initiatives, it is important to check the current

status of these compounds when making decisions on what materials to use.



Polybrominated Biphenyl Oxide (PBBO or PBDE)



Polybrominated Biphenyl (PBB)

FIGURE 10.10 Restricted brominated flame retardants.

In the case of standard epoxy materials used in printed circuits, flame retardancy has commonly been achieved by brominating the epoxy resin. This normally involves manufacturing the epoxy resins with tetrabromobisphenol A (TBBPA), which contains bromine within the chemical backbone (see Fig. 10.2). TBBPA is not restricted by the RoHS directive. Because TBBPA is reacted into the epoxy resin itself, it is not available for release into the environment. Under excessive exposure to heat, the bromine is released and retards burning. TBBPA has been used successfully for

many years as a flame retardant and is still used in the majority of materials. However, while the RoHS directive applies only to specific brominated flame retardants, the WEEE directive may require separation and special handling of materials containing any brominated flame retardant. The separation and special handling relate to concerns about the by-products of incineration, especially if incineration is done at too low a temperature. Furthermore, individual countries continue to look at introducing their own legislative initiatives in regards to these flame retardants, and as such, it is always important to check the status of these efforts.

10.3.1 Flame Retardant Chemistry

Polymer combustion occurs in a continuous cycle, as highlighted in Fig. 10.11. Heat generated in the flame is transferred back to the polymer surface, producing volatile polymer fragments that constitute fuel for further burning. These fragments diffuse into the flame zone where they react with oxygen by free-radical chain reactions. This in turn produces more heat and continues the cycle. Flame retardancy is achieved by interrupting this cycle.

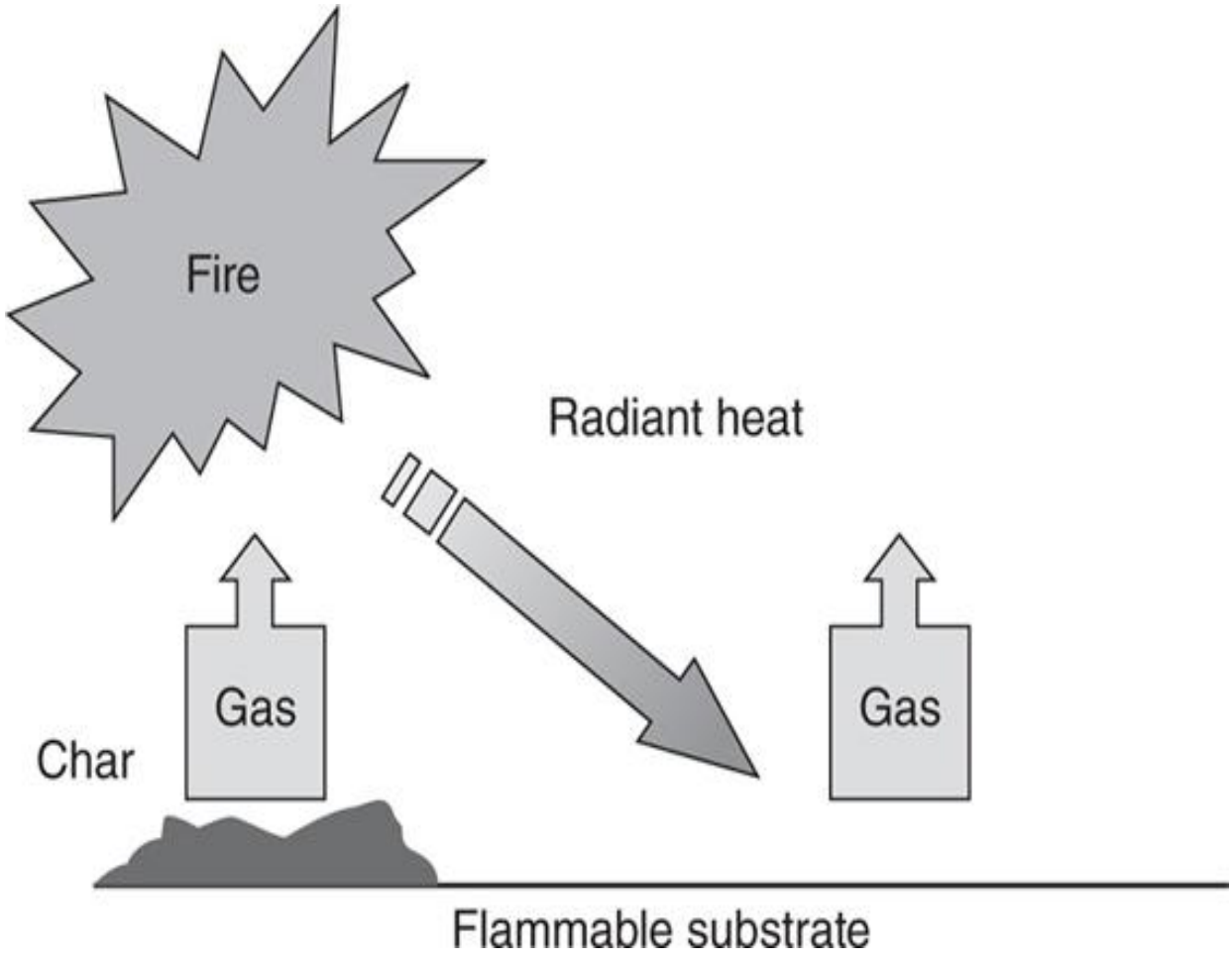


FIGURE 10.11 Polymer combustion.

There are two basic ways to interrupt this cycle. One method is called solid phase inhibition and involves changes in the polymer substrate. Systems that promote extensive polymer crosslinking at the surface form a carbonaceous char upon heating. The char then insulates the underlying polymer from the heat of the flame, preventing production of new fuel and further burning. Other systems evolve water during heating, cooling the surface and increasing the amount of energy needed to maintain the flame.

The second method is called vapor phase inhibition and involves changes in the flame chemistry. Reactive species are built into the polymers, which are transformed into volatile free-radical inhibitors during burning. These materials diffuse into the flame and inhibit the branching

radical reactions. As a result, increased energy is required to maintain the flame and the cycle is interrupted. For many materials, both solid and vapor phase inhibition occur.

Polymers, including the various types of epoxy resins, differ in their inherent flammability. The types of resins and curing agents selected can impact the fundamental flammability of the resin system, and determine how much additional flame retardant components are needed to achieve the desired flammability rating. For example, polymers with a high concentration of aromatic groups will generally have higher thermal stability as well as the ability to form char on burning. Additives such as TBBPA, or epoxy resins built from TBBPA contain bromine on the molecular backbone. Most organic halogenated compounds such as these retard burning by vapor phase inhibition. They typically decompose to yield HBr or HCl (HBr in the case of TBBPA-based materials) which quench chain-branching free radical reactions in the flame. Some halogen acids also catalyze char formation.

10.3.2 Halogen-Free Alternatives

Halogen-free alternatives include phosphorus-based compounds, nitrogen-based flame retardants, inorganic flame retardants and hydrated fillers. These can be subdivided into reactive components and additives. A reactive component is one that becomes directly incorporated into the resin system itself, like TBBPA. As with TBBPA, reacted components have the advantage of not being available for release to the environment through leaching or solvent extraction. An example of a reactive, nonhalogen flame retardant would be epoxidized phosphorus compounds. The epoxide groups of these compounds make them reactive and result in chemical bonding into the polymer backbone. In contrast, red phosphorus is an

inorganic solid that can be dispersed into an epoxy formulation. Hydrates, such as aluminum hydroxide or magnesium hydroxide, decompose and liberate water, which then suppresses the burning process. In some cases, organic flame retardants may be dispersed into the bulk resin system as an additive, in the way inorganic fillers can be dispersed within the resin system to alter other properties.

In choosing a flame retardant, consideration must be given to the impact on the performance of the resin system and the finished base material. These materials, at the levels required for flame retardancy, can affect the physical properties of the laminate, change rheological properties and alter cure kinetics of the resin system. Generally, the reactive compounds are preferred since they are bound to the polymer backbone, which prevents release into the environment, and they seem to facilitate obtaining the desired material properties in comparison to additives or fillers. But combinations of reactive compounds and additives to the resin system can work synergistically and still meet other performance requirements. Table 10.2 summarizes some of the available halogen-free flame retardants.

TABLE 10.2 Halogen-Free Flame Retardants

Type	Primary Mechanism	Examples	Considerations
Phosphorus	Char former	Red phosphorus, ammonium polyphosphate, organic phosphorus compounds	Red phosphorus difficult to process, toxic. Organic phosphorus compounds are a common alternative, but generally more costly and can lower T_g.
Inorganic/ hydrated fillers	Evolve water, endothermic, may promote char	Alumina trihydrate, magnesium hydroxide, zinc borate, antimony oxides	Inexpensive, but generally require high loadings and can degrade mechanical and other properties. Toxicity of antimony-based retardants a concern. Can be used with other flame retardants synergistically.
Nitrogen	Intumescent System, generates gas that foams char	Melamine, melamine Cyanurate	Impact on material properties, other environmental impact concerns.

Organic phosphorus-based flame retardants have become a common alternative flame retardant used in printed circuit base materials. However, others are also being used and combinations of two or more types of halogen-free flame retardants can also be used synergistically to achieve adequate flammability levels while minimizing adverse impacts on material properties. Some of the impacts that must be evaluated are moisture absorption, copper peel strength, T_g reduction, changes in resin flow, change in mechanical or electrical performance, and the impact on CAF resistance. Some of the currently used alternatives include the following:

- *Alumina trihydrate (ATH)*. ATH works by generating water vapor to reduce the flammable gas concentration and also

forms a char. It is relatively inexpensive and easy to drill, but lowers the decomposition temperature, T_d, and typically requires a fairly high loading to pass UL94 V-0 flammability rating.(see Fig. 10.12).

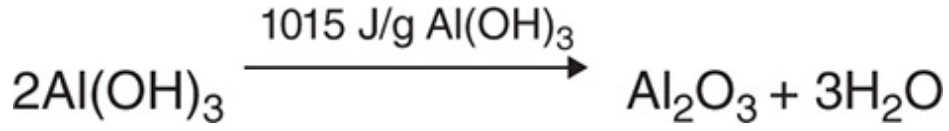


FIGURE 10.12 Decomposition of ATH.

- *Melamine derivatives*. Melamine polyphosphate (MPP) (Fig. 10.13) is one example of this category of flame retardant. Such nitrogen containing compounds decompose to generate an inflammable gas and the phosphorous compounds create a char. These flame retardants are widely available and inexpensive, but may result in higher moisture absorption and are nonreactive.

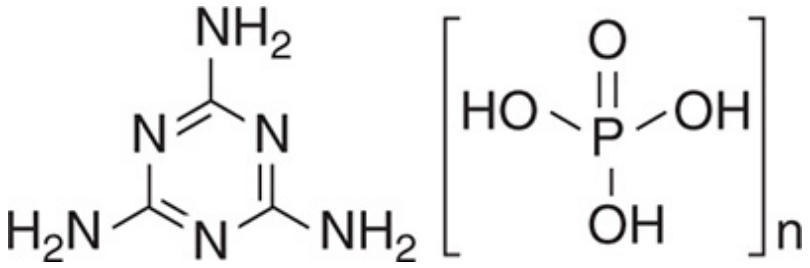
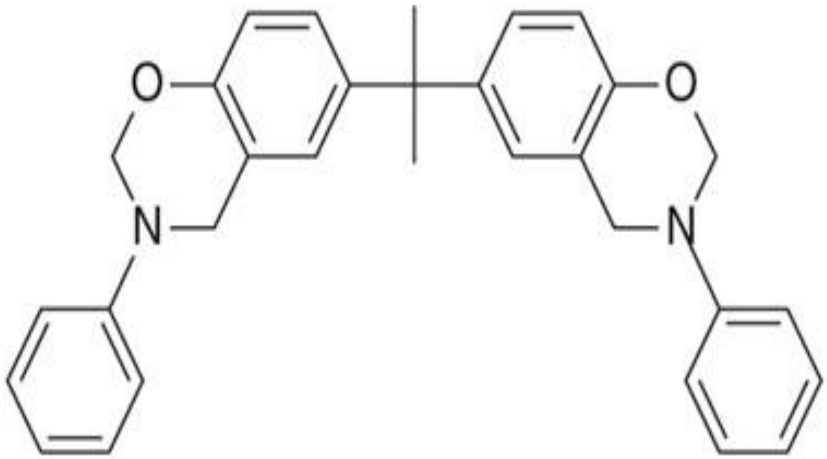
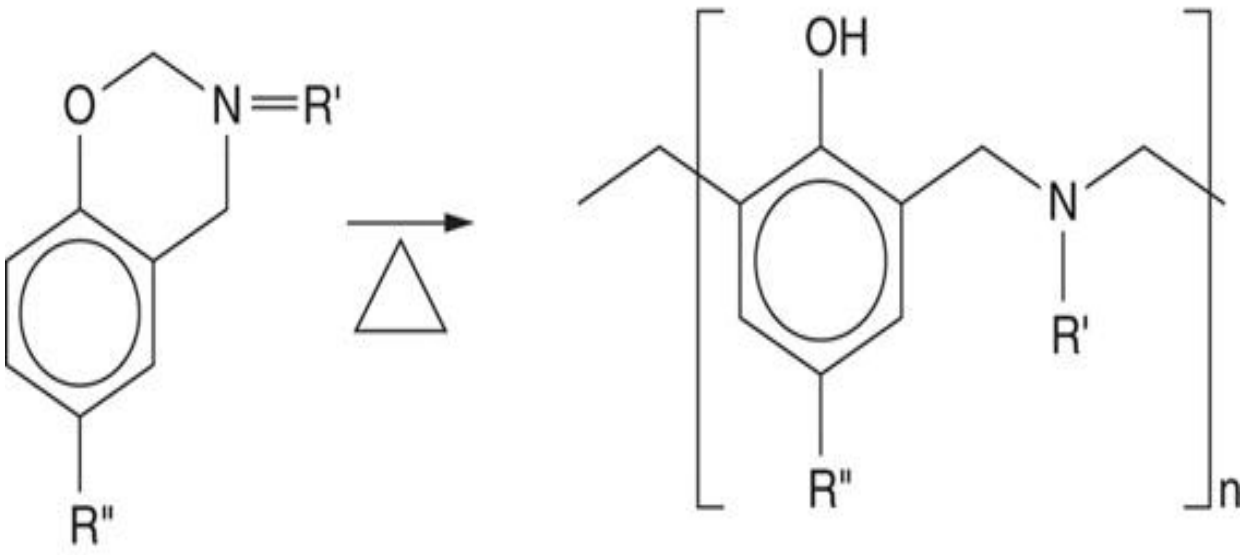


FIGURE 10.13 Melamine polyphosphate (MPP).

- *Nitrogen containing resins*. Examples include benzoxazine and melamine phenolic formaldehyde novolac as shown in Figs. 10.14 and 10.15. The advantage of these compounds is that they are reactive and support a high T_g. On the other hand, they are generally not as effective as reactive phosphorous compounds, can be difficult to fully cure, and are often not as thermally stable. They can also be relatively brittle.



Benzoxazine



Benzoxazine reaction schematic

FIGURE 10.14 Benzoxazine.

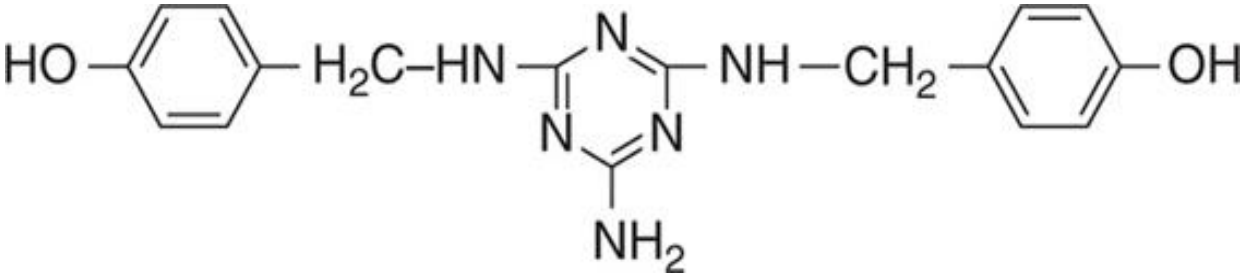


FIGURE 10.15 Melamine phenolic formaldehyde novolac.

- *Phosphorous containing resins and hardeners*. A commonly used compound used to make phosphorous containing resins and hardeners is DOPO (9,10-dihydro-9-oxa-10-phosphaphenanthrene-10-oxide), as shown in Figs. 10.16, 10.17 and 10.18. DOPO may be used to create epoxy resins which contain the DOPO chemistry for flame retardancy that are also reactive into the resin system. These resins are now commonly available, but many limit the range of T_g that can be achieved and are relatively more expensive. Hardeners based on DOPO can offer more flexibility in formulation of the resin system, and as a result can be used to develop higher-T_g resin systems that also have higher decomposition temperatures.

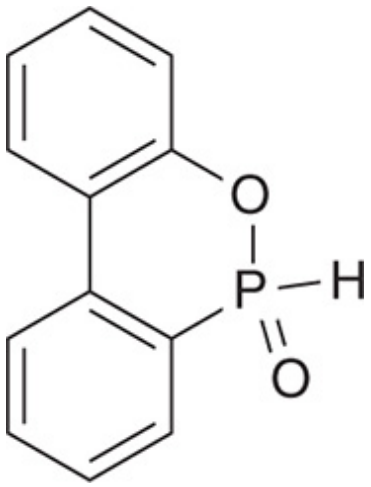


FIGURE 10.16 DOPO.

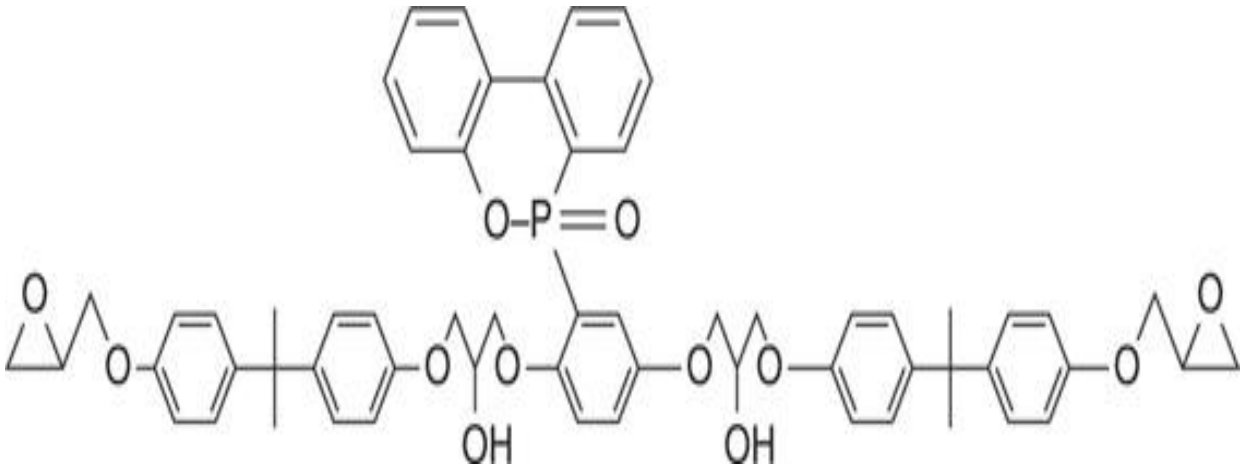


FIGURE 10.17 DOPO-HQ difunctional epoxy.

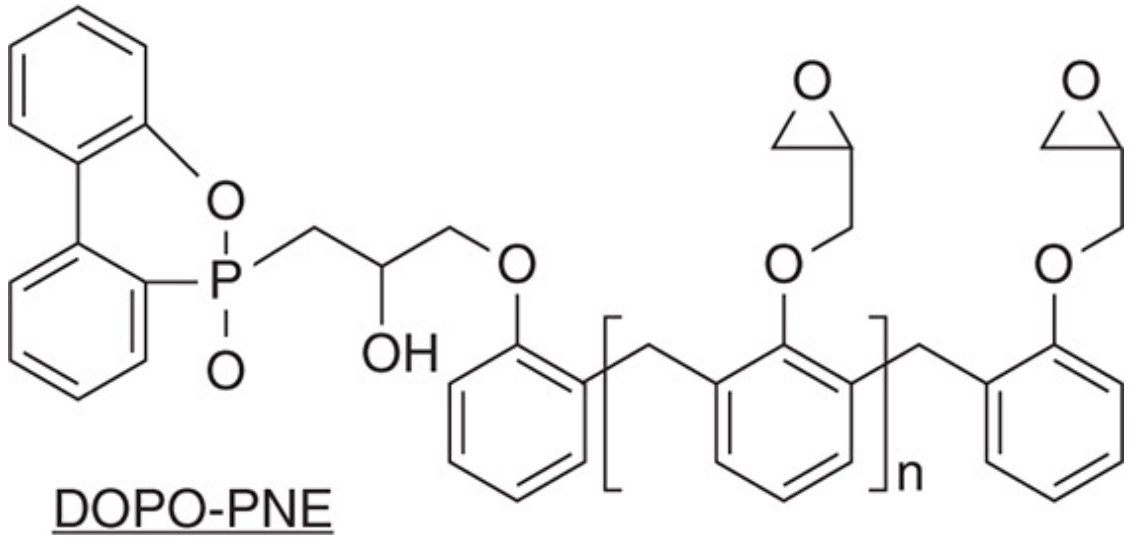


FIGURE 10.18 DOPO-based phenol novolac epoxy.

10.3.3 Other Resins and Formulations

For many of these resins, there are several different types of molecular structures that can be used to modify the ultimate properties of the base material. In addition, other types of resins are also in use or are being developed to meet the growing requirements for the various applications printed circuits are used in. Often, these resins are proprietary in

nature and therefore discussions of these products focus on their properties rather than the specific chemistry used to achieve the properties. In addition, fillers are increasingly being used to modify thermal expansion or electrical performance, or both. Fillers will be discussed shortly.

10.4 ADDITIVES

The resin systems discussed above will typically contain a variety of additives that either promote curing of the resin system or modify the properties in some way. Some important types of additives are given here:

10.4.1 Curing Agents and Accelerators

Each resin system contains organic components that must be reacted together in order to promote polymerization and cross-linking. Curing agents and accelerators are used to promote these reactions. Amine based curing agents have been commonly used to cure epoxy resins. Some of these, such as aliphatic diamines are used to cure epoxies at room temperature. Others, such as aromatic diamines require elevated temperatures. Figure 10.19 shows an example of curing epoxy with an aromatic amine. Note the –OH group formed on the new molecule. As shown in Fig. 10.4, the –OH can also crosslink with other epoxide groups.

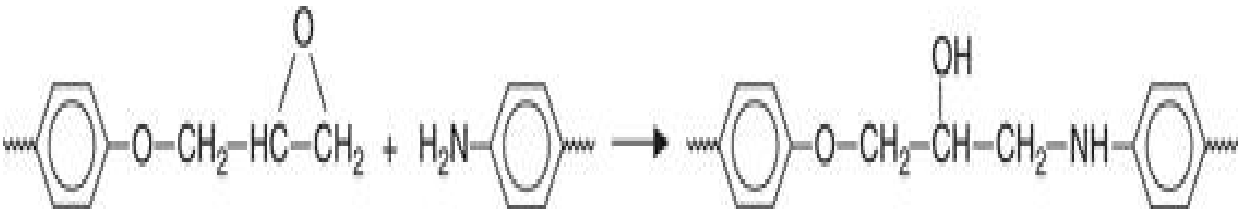


FIGURE 10.19 Curing epoxy with an aromatic amine.

Historically, the most common curing agent used in epoxy resin systems for printed circuit base materials has been dicyandiamide or “dicy.” However, nondicy systems have been developed to promote faster curing, reduce moisture sensitivity, and improve thermal stability. The choice of curing agent and accelerator is also driven by the resin type. Nondicy cured epoxy materials will be discussed further in Chap. 13. Figure 10.20 illustrates some of the curing reactions that occur as the resin system polymerizes, and Fig. 10.21 illustrates a phenol curing mechanism.

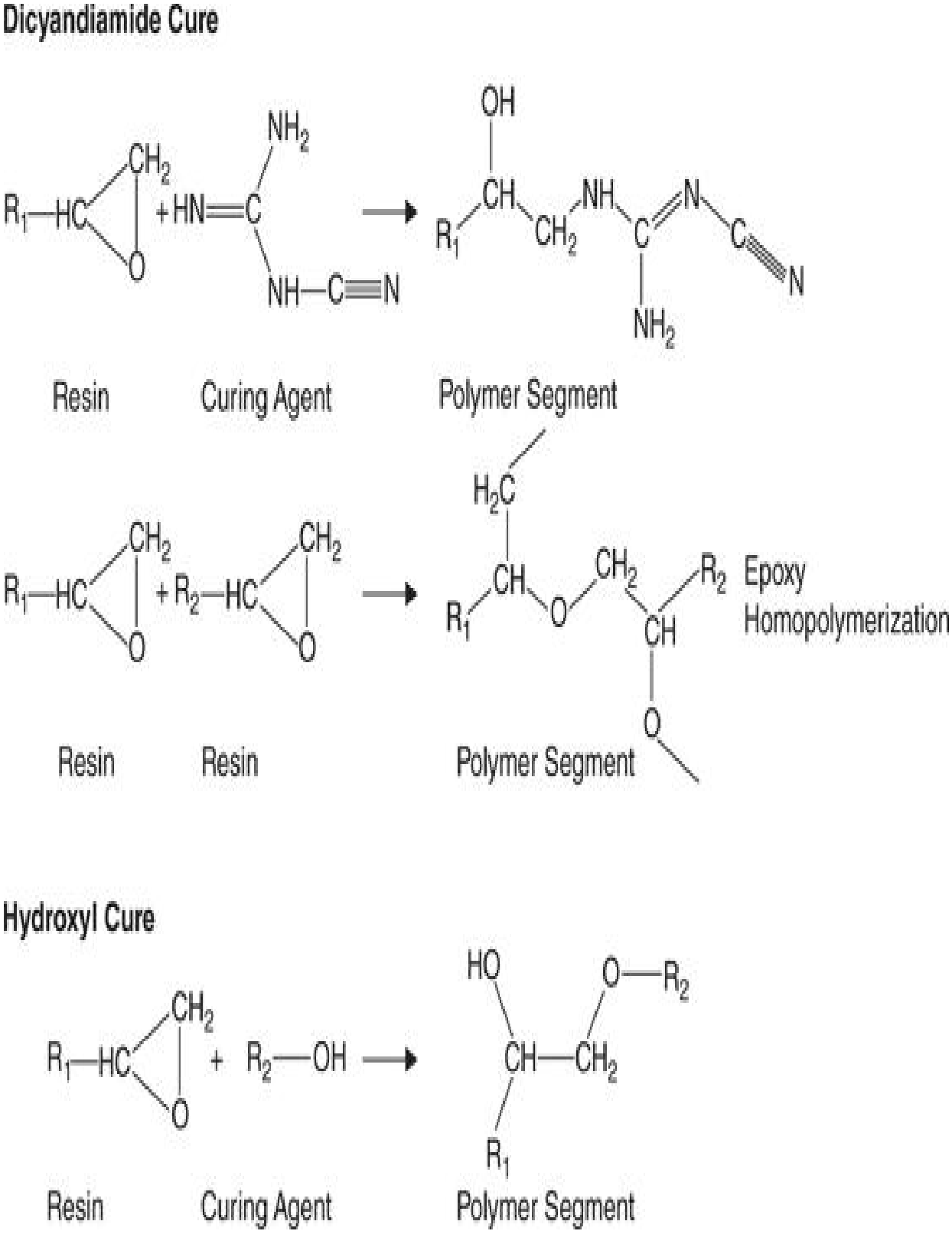


FIGURE 10.20 Epoxy curing mechanisms.

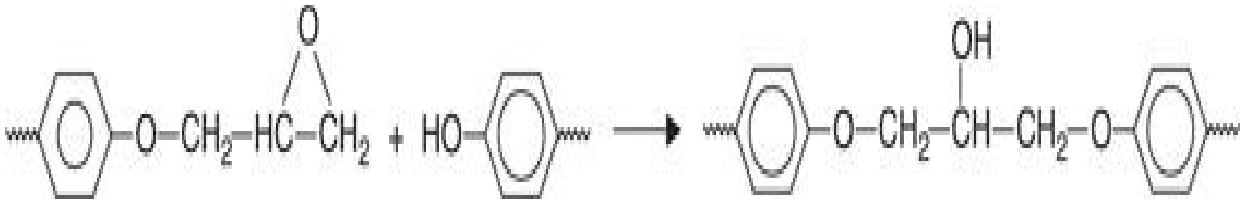


FIGURE 10.21 Phenol curing mechanism.

10.4.2 UV Blockers/Fluorescing Aids

Some resins naturally absorb ultraviolet light. Others absorb very little. There are two reasons why this property is important. First, some automatic optical inspection (AOI) equipment is laser based and relies on the resin system in the base material to fluoresce upon exposure, which allows the AOI device to detect the conductor pattern. The second reason involves photoimaging on very thin circuits, during the solder mask imaging process for example. In very thin circuits, if the base material does not absorb UV light sufficiently, the UV light from one side of the circuit board can pass through to the other side and cause unwanted exposure of the photoresist on the opposite side. Therefore, components that absorb UV light are sometimes added to resin systems that do not sufficiently absorb UV light.

10.4.3 Inorganic Fillers

Fillers are small particles that can be added to a resin system in order to modify the electrical or thermomechanical properties of the composite material. These materials range from talc, silica, kaolin clay powders, tiny hollow glass spheres, to a variety of other inorganic materials. These materials are typically used to tailor the properties of the base material for specific uses. For example, kaolin clay powders coated with a layer of palladium and dispersed within the base materials have been used as catalysts for

electroless copper plating. Hollow glass microspheres have been used to reduce the dielectric constant of materials. The most common use of fillers is to reduce thermal expansion and improve reliability. The reduced *z*-axis expansion helps offset the increased expansion and stress on plated through holes that results from the higher temperatures associated with lead-free assembly. They may also improve the machinability of materials in the drilling process and alter electrical properties such as Dk and Df. Talc and silica based fillers are commonly used for reduction in *z*-axis expansion.

The performance of fillers is a function of a number of factors, including the methods used to manufacture the fillers and the size and shape of the fillers. Materials incorporating a given filler composition (i.e., silica) may have different properties depending on the specific filler type and form. The amount of filler within the resin system will also change the overall properties, and the optimal amount requires consideration of a balance of properties. For example, some fillers may provide excellent thermomechanical properties, but may also increase drill bit wear.

10.5 REINFORCEMENTS

While there are also a variety of reinforcements used in base materials, woven fiberglass cloths are by far the most common. Other materials include paper, glass matte, nonwoven aramid fibers, nonwoven fiberglass and a variety of fillers. The advantages of woven glass cloths include a good combination of mechanical and electrical properties, a wide range of types for achieving various laminate thicknesses, and good economics.

10.5.1 Woven Fiberglass

The process of manufacturing woven fiberglass cloth begins with melting the various inorganic components required for a particular grade of glass. The molten components travel through a furnace and ultimately flow through specialized bushings to form the individual fiberglass filaments and yarns. These yarns are then used in a weaving process in order to manufacture the fiberglass cloth. The relative concentrations of the components used will affect the chemical, mechanical, and electrical properties of the fiberglass. The compositions of a few fiberglass types are provided in Table 10.3. Figure 10.22 illustrates the process used to manufacture the fiberglass yarns. The yarns are then woven into fiberglass cloths.

TABLE 10.3 Fiberglass Compositions

Component	E-Glass	NE-Glass	S-Glass	D-Glass	Quartz
Silicon dioxide	52–56%	52–56%	64–66%	72–75%	99.97%
Calcium oxide	16–25%	0–10%	0–0.3%	0–1%	
Aluminum oxide	12–16%	10–15%	24–26%	0–1%	
Boron oxide	5–10%	15–20%		21–24%	
Sodium oxide and potassium oxide	0–2%	0–1%	0–0.3%	0–4%	
Magnesium oxide	0–5%	0–5%	9–11%		
Iron oxide	0.05–0.4%	0–0.3%	0–0.3%	0.3%	
Titanium oxide	0–0.8%	0.5–5%			
Fluorides	0–1.0 %				

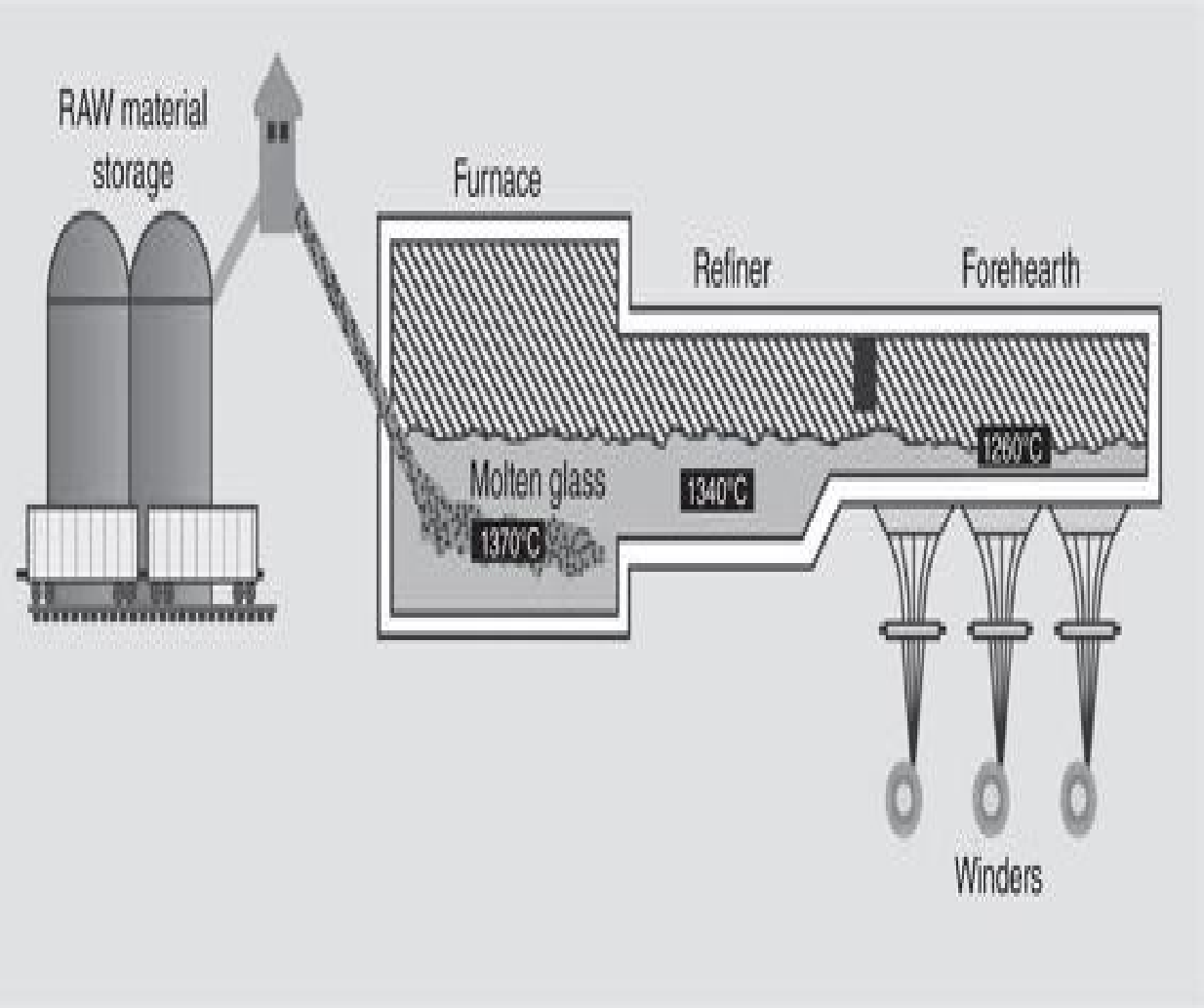


FIGURE 10.22 Illustration of fiberglass yarn manufacture.

E-glass is the most commonly used fiberglass for printed circuits. E-glass provides an excellent combination of electrical, mechanical, and chemical properties at a reasonable cost. NE-glass had been used in limited quantities, but usage has grown as the need for better electrical performance grows. NE-glass offers improved permittivity (Dk) and loss (Df) properties. Another glass type more recently introduced is L-glass. L-glass also offers improved Dk and Df properties in comparison to E-glass. However, NE and L glass are more expensive than E-glass. Note that the Dk and Df values in Table 10.4 are approximate and based on commercially available technical data sheets.

These measurements can vary based on measurement method and other factors, so are meant only to show that both NE and L glass offer improved Dk and Df values compared to E-glass, not to show the relative performance of NE and L glasses. S-glass provides greater strength but is more difficult to process through the mechanical drilling operation. Other glass types are less commonly used, though there are also low CTE glasses used in chip packaging substrates.

TABLE 10.4 Comparison of E-Glass and NE-Glass

Property	E-Glass	NE-Glass	L-Glass
CTE, ppm/°C	5.5	3.4	3.9
Dielectric constant @ 1 GHz	6.8	4.8	4.8
Dielectric constant @ 10 GHz	6.6	4.8	4.8
Dissipation factor @ 1 GHz	0.004	0.0015	0.001
Dissipation factor @ 10 GHz	0.0066	0.0035	0.003

There are several diameters of filaments available (Table 10.5), as well as many different yarn types. D, DE, E, and G filaments are the most commonly used. Combining the various yarn types in the weaving process leads to many different types of cloth styles. While there are also many different weave types, virtually all cloths for printed circuits use a plain weave (Fig. 10.23). The plain weave consists of yarns interlaced in an alternating fashion one over and one under every other yarn. This weave pattern provides good fabric stability. Some of the common plain weave cloth styles used for printed circuits are shown in Table 10.6. The fiberglass cloths are also coated with a finish or coupling

agent tailored for improving the bond between the glass filaments and the specific resin coated onto the glass. This coupling agent and the resin-to-glass bond that results, is an important consideration for CAF resistance, which will be discussed in Chap. 14.[2]

TABLE 10.5 Glass Filament Diameters

Filament Designation	Nominal Diameter (microns)	Nominal Diameter (10^{-5} inches)
BC	4	15.7
C	4.5	17.7
D	5	21.0
DE	6	25.6
E	7	28.0
G	9	37.0

FIGURE 10.23 Plain weave.

TABLE 10.6 Common Fiberglass Cloth Styles for Printed Circuit Base Materials—U.S. System

Style	Fabric Thickness (mils) (Reference Only)	Warp Yarn	Fill Yarn	Fabric Count (ends/in)	Weight (oz/yd^2)
101	0.95	ECD1800 1/0	ECD1800 1/0	75 × 75	0.48
104	1.1	ECD900 1/0	ECD1800 1/0	60 × 52	0.55
106	1.3	ECD900 1/0	ECD900 1/0	56 × 56	0.72
1017	0.53	BC3000 1/0	BC3000 1/0	95 × 95	0.36
1027	0.75	BC1500 1/0	BC1500 1/0	75 × 75	0.50
1035	1.1	ECD900 1/0	ECD900 1/0	66 × 68	0.88
1037	1.1	ECC1200 1/0	ECC1200 1/0	70 × 73	0.68
1067	1.4	ECD900 1/0	ECD900 1/0	70 × 70	0.91
1080	2.1	ECD450 1/0	ECD450 1/0	60 × 47	1.38
1086	2.0	ECD450 1/0	ECD450 1/0	60 × 60	1.60
1078	1.7	ECD450 1/0	ECD450 1/0	54 × 54	1.41
1500	5.9	ECE110 1/0	ECE110 1/0	49 × 42	4.84
1501	5.5	ECE110 1/0	ECE110 1/0	46 × 45	4.86
1504	4.9	ECDE150 1/0	ECDE150 1/0	50 × 50	4.36
1652	4.5	ECG150 1/0	ECG150 1/0	52 × 52	4.09
2013	2.76	ECE225 1/0	ECE225 1/0	47 × 45	2.39
2113	3.1	ECE225 1/0	ECD 450 1/0	60 × 56	2.30
2313	3.3	ECE225 1/0	ECD450 1/0	60 × 64	2.40
3313	3.3	ECDE300 1/0	ECDE300 1/0	60 × 62	2.40
3070	3.1	ECDE300 1/0	ECDE300 1/0	70 × 70	2.76
2116	3.7	ECE225 1/0	ECE225 1/0	60 × 58	3.06
2157	5.1	ECE225 1/0	ECG75 1/0	60 × 35	4.36
2165	4.0	ECE225 1/0	ECG150 1/0	60 × 52	3.55
7628	6.8	ECG75 1/0	ECG75 1/0	44 × 31	6.00
7629	7.1	ECG75 1/0	ECG75 1/0	44 × 34	6.19
7635	7.9	ECG75 1/0	ECG50 1/0	44 × 29	6.85

10.5.2 Yarn Nomenclature

Because there can be so many types of yarn manufactured from the available grades of glass and filament diameters, special nomenclature systems have been developed. The two systems used are the U.S. system and the SI/Metric system.

10.5.2.1 The U.S. System. An example of a yarn name in the U.S. system is ECD 450-1/0. This yarn is used in making a 1080 style glass cloth. Each letter and number in the name describes something about the yarn:

- *First letter:* describes the glass composition. Electrical grade, or E-glass is the most common grade used for manufacturing materials for printed circuits.
- *Second letter:* C indicates that the yarn is composed of continuous filaments. S would indicate staple filaments.
- *Third letter:* indicates the individual filament diameter (Table 10.5).
- *First number:* represents 1/100th the normal bare glass yardage in 1 pound of the basic yarn strand. In the example above, multiply 450 by 100 which results in 45,000 yards in 1 pound.
- *Second number:* represents the number of basic strands in the yarn. The first digit represents the original number of twisted strands. The second digit separated by the diagonal represents the number of strands plied or twisted together. 1/0 means that the yarn is a singles yarn (no or "zero" plying required).

The name may also include a designation indicating the number of turns per inch in the twist of the final yarn, and the direction of the twist. An example would be 3.0S, or 3 turns per inch with an "S" direction twist. An "S" twist has

spirals that run up and to the left. A “Z” twist has spirals that run up and to the right.

10.5.2.2 The SI/Metric System. An example of a yarn name in the SI/Metric System is EC5 11 1X2.

- *First letter:* designates the glass composition.
- *Second letter:* C indicates that the yarn is composed of continuous filaments. S indicates staple filament.
- *First number:* indicates the individual filament diameter expressed in microns.
- *Second number:* represents the TEX number of linear density. TEX is the mass in grams per 1000 meters of yarn. So 11 in the above example refers to 11 g/km.
- *Third number:* indicates yarn construction or the basic number of strands in the yarn. The first digit represents the original number of twisted strands and the second digit, after the X, indicates the number of these strands twisted or plied together.

10.5.3 Fiberglass Cloths[3]

With the possible combinations of glass compositions, filament diameters, yarn types, and the number of different weave patterns available, the number of possible fiberglass cloths can almost be unlimited. The effects that these glass fabrics have on the base material are driven by these variables. In addition, the fabric count, or the number of warp yarns and fill yarns also helps determine the properties of the fabric and the base material. Warp yarns are those that lie in the length (machine direction) of the fabric while the fill yarns lie across the warp direction. The warp direction is also commonly called the grain direction. Fabrics with a balanced amount of glass in both directions is called “square

weave” glass. Examples include 1067 and 1086 in Table 10.6. The fabric count for 1067 is 70 × 70 and for 1086 it is 60 × 60. Contrast these with the 1080 glass cloth, which is 60 × 47. This can have an impact on signal integrity and will be discussed further in Chap. 14.

As pointed out earlier, E-glass is the most commonly used glass type, and virtually all use what is called a plain weave. A plain weave results in a fabric constructed so that one warp yarn passes over and under one filling yarn (and vice versa). This weave pattern offers good resistance to yarn slippage and fabric distortion. Common fiberglass cloths used in materials for printed circuits are shown in Table 10.6, using the U.S. nomenclature system. The IPC specification IPC-4412 documents additional cloth styles as well as the SI/Metric nomenclature. Some common styles are shown in Figs. 10.24 through 10.30. At a given resin content, each style will yield a different nominal dielectric thickness. Having the flexibility of many glass styles and thicknesses is important for meeting controlled impedance and overall thickness requirements.

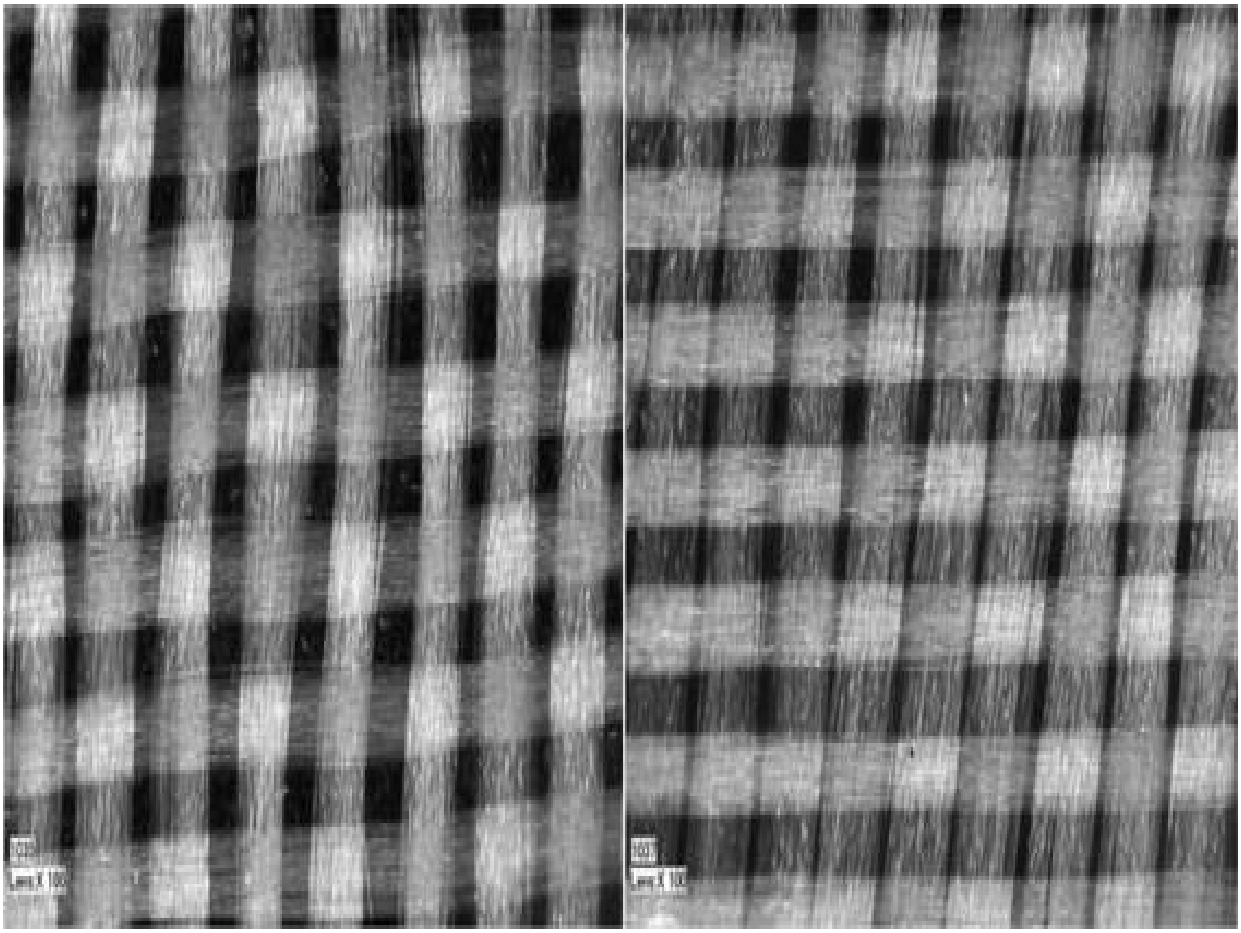


FIGURE 10.24 1037 Glass cloth used in an HDI PCB with stacked microvias.

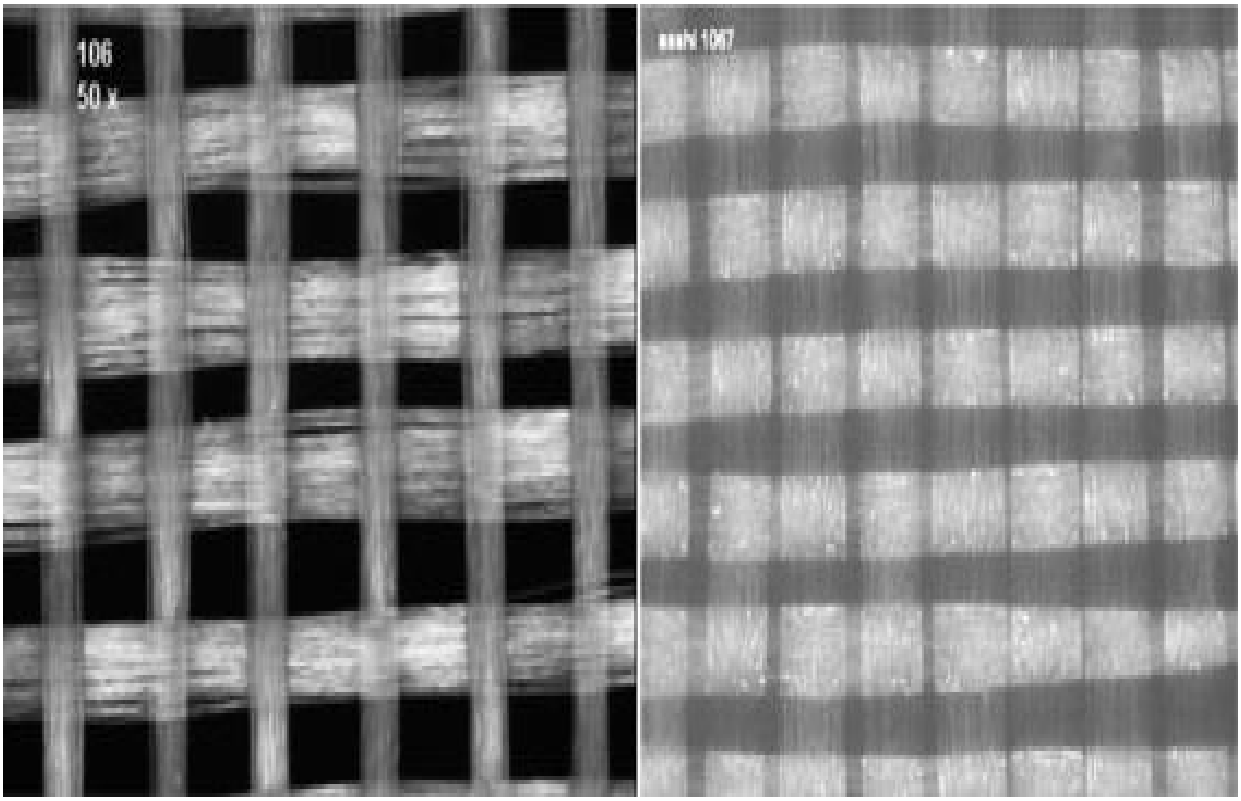


FIGURE 10.25 Expanding and spreading of glass filaments.

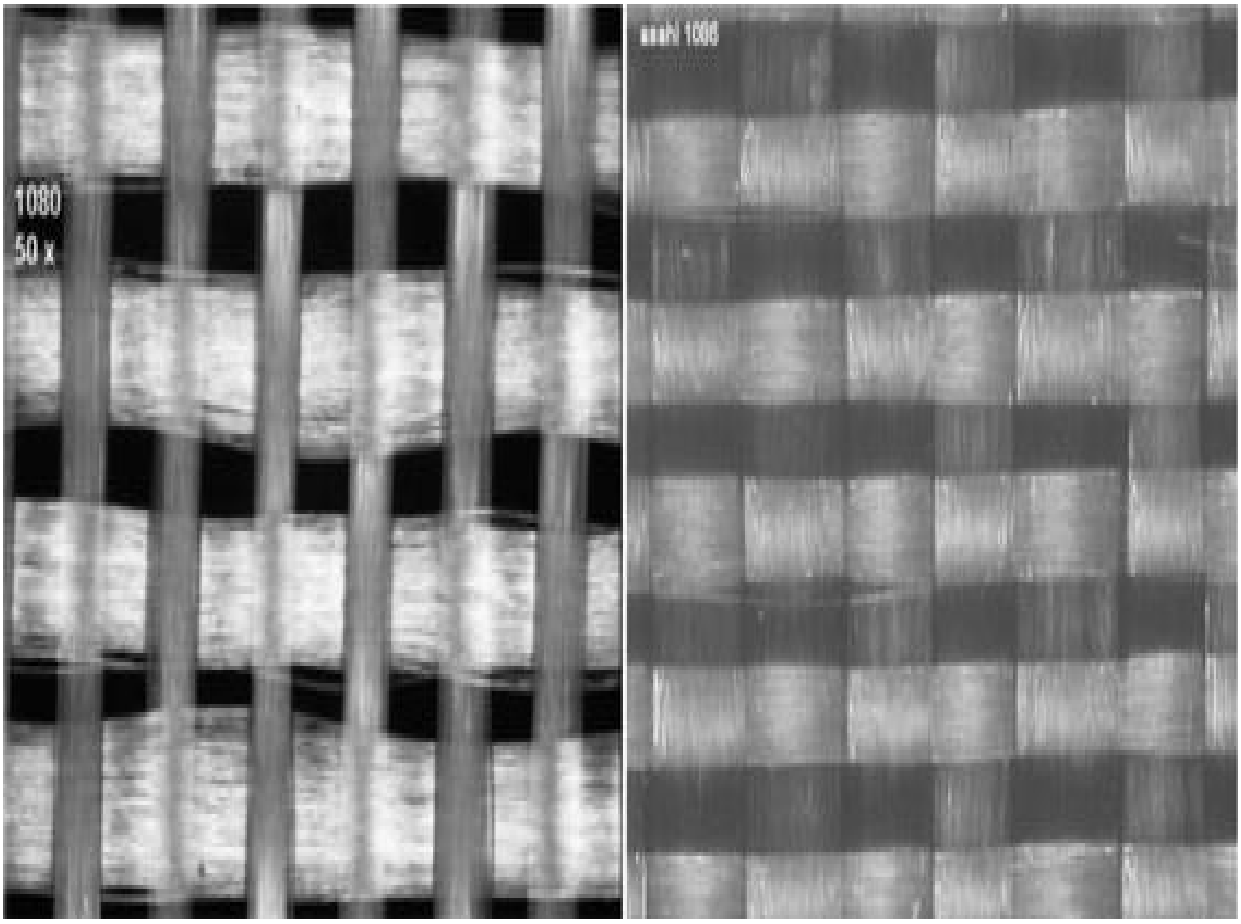


FIGURE 10.26 Microvias formed in a dielectric with a standard glass fabric (left) versus a dielectric with a spread fabric (right).

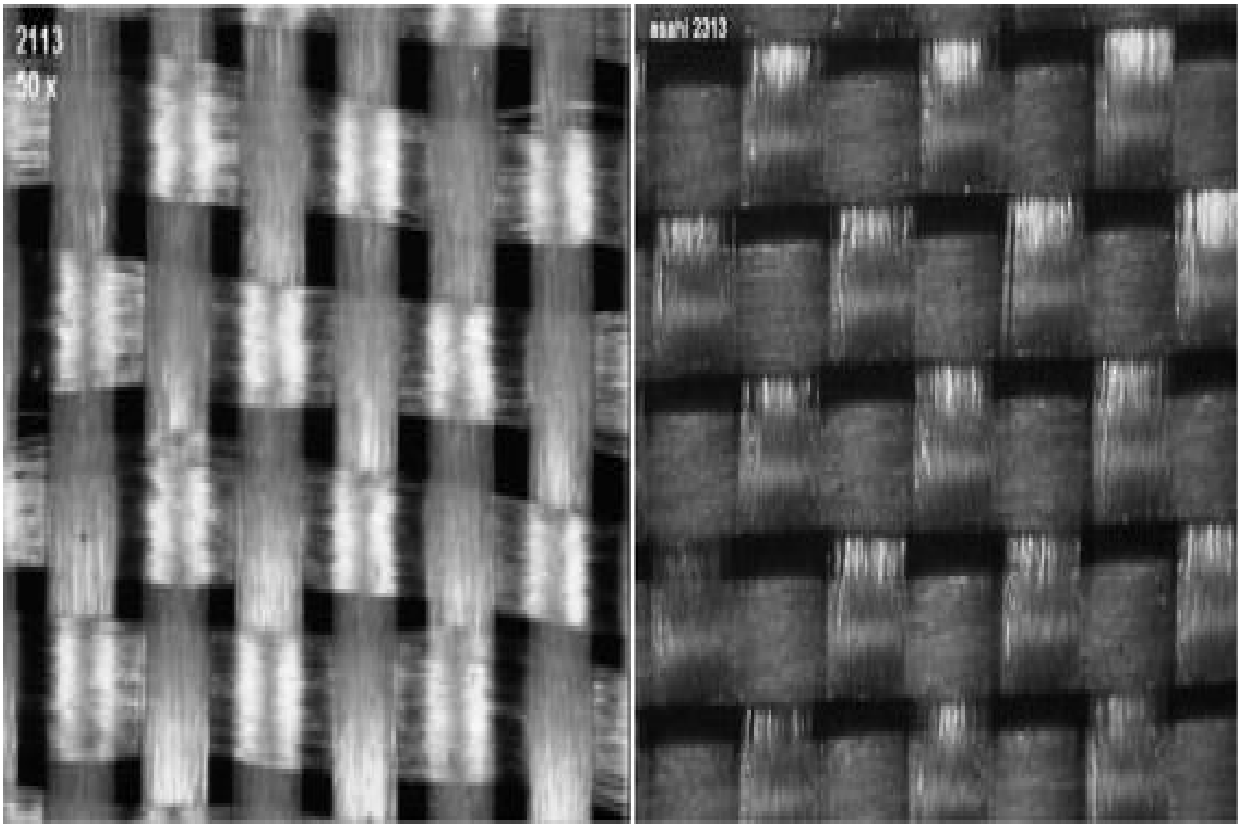


FIGURE 10.27 1035 and 1037 Glass gabrics.

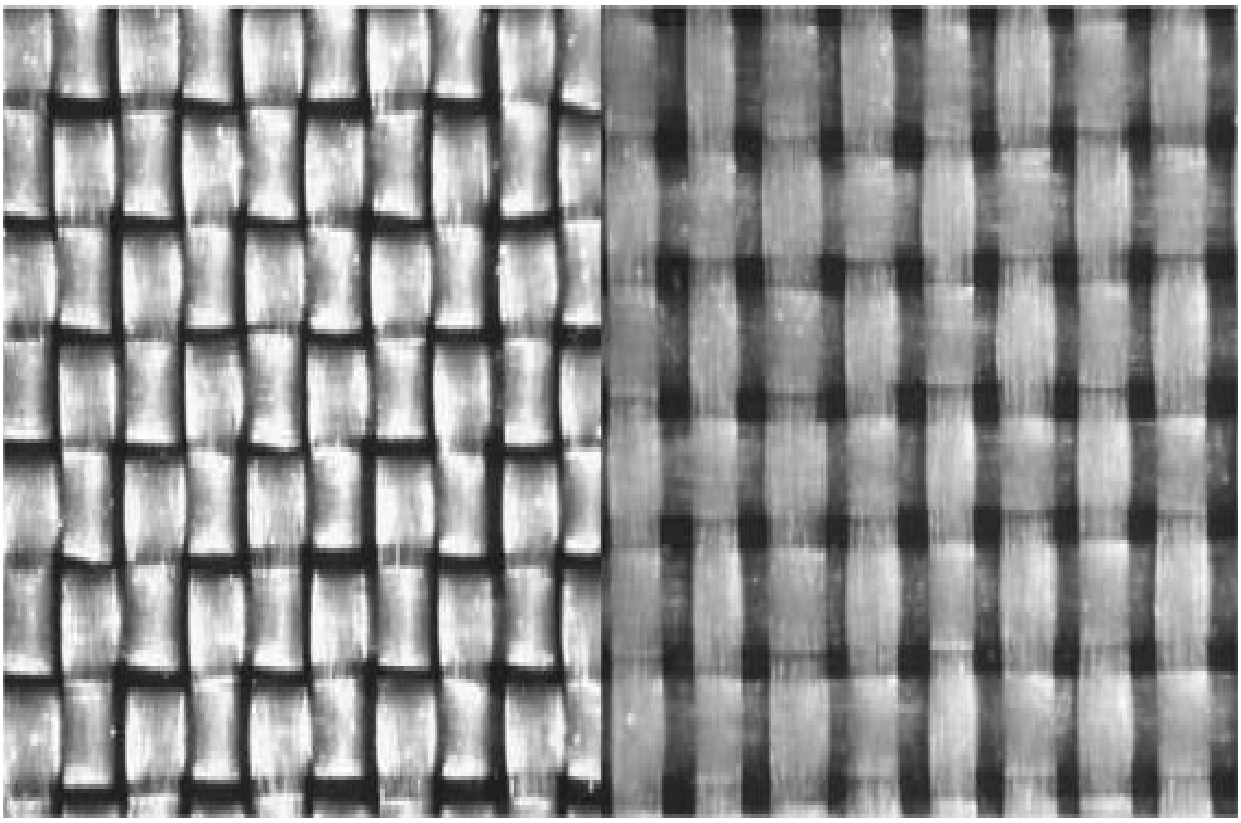


FIGURE 10.28 106 and 1067 Glass fabrics.

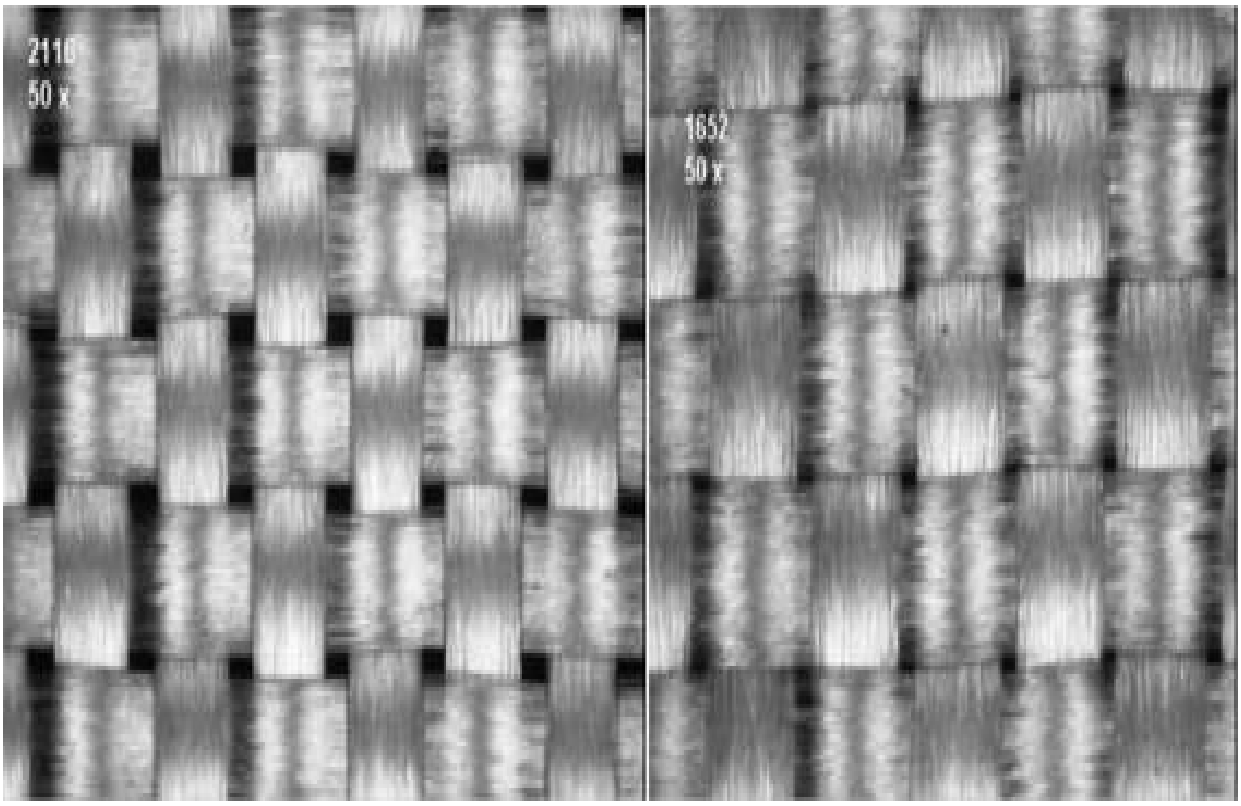


FIGURE 10.29 1080 and 1086 Glass fabrics.

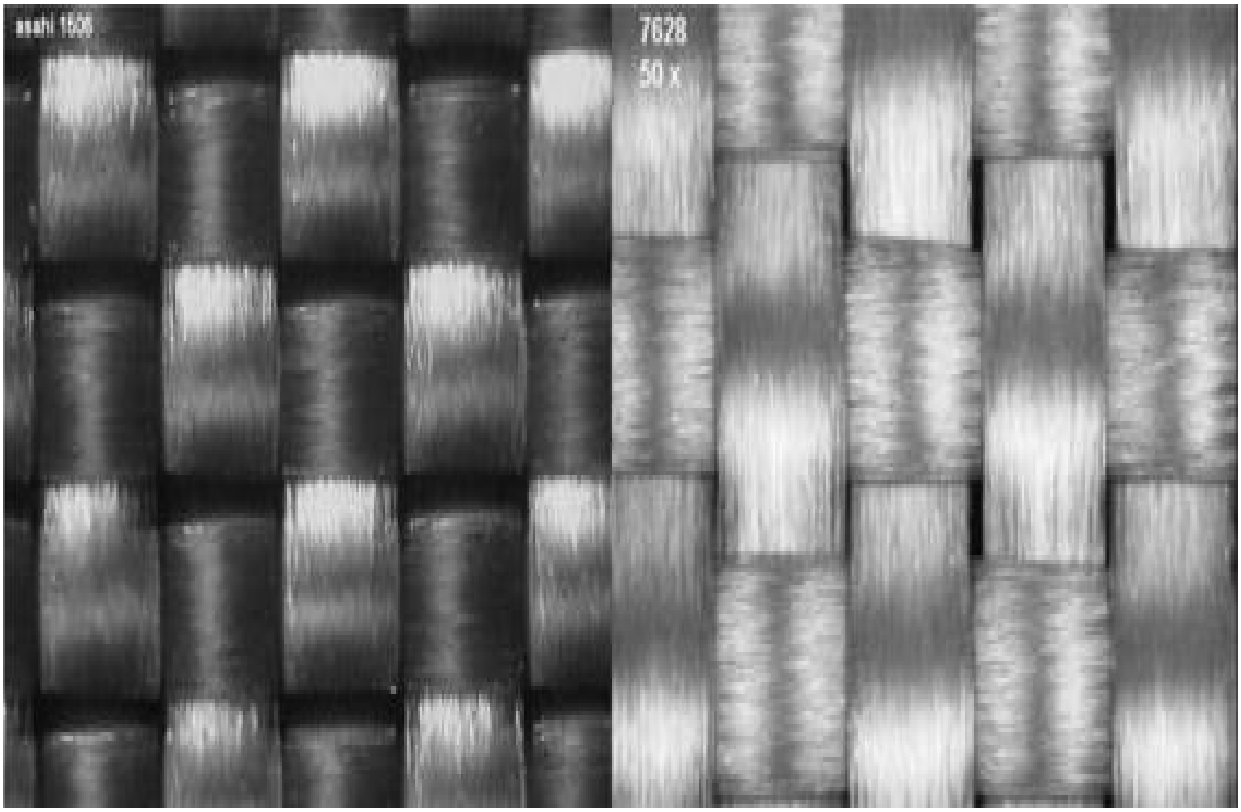


FIGURE 10.30 2113 and 2313 Glass fabrics.

In recent years, the use of many of the very thin, lightweight fabrics has dramatically increased. This has been driven largely by the need for very thin dielectrics in mobile devices such as smartphones and tablet computers. But use of these fabrics is also growing in thicker, higher layer count PCBs where the need to increase circuit density continues to necessitate thinner dielectrics, some of which require two plies of glass cloth in a thin dielectric. In smartphones and tablet devices, 1037 glass is common with the use of 1027 and 1017 growing. Figure 10.31 is an example of an HDI PCB using very thin glass cloth in a smartphone.

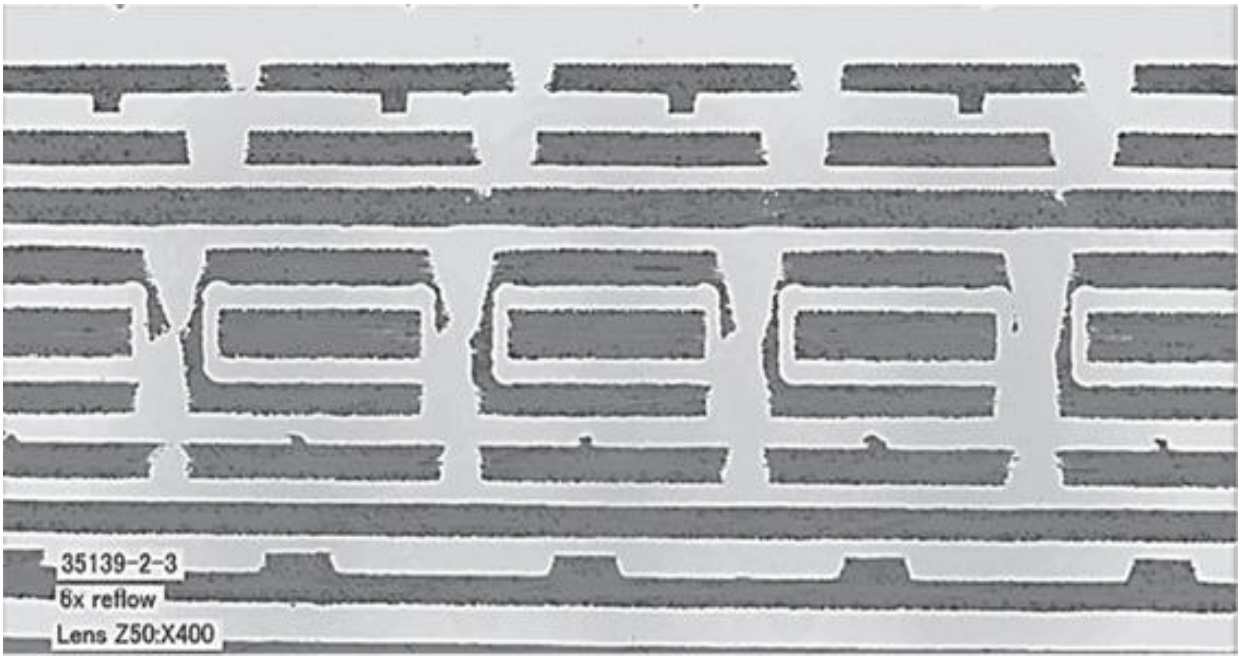


FIGURE 10.31 3070 and 3313 Glass fabrics.

In PCBs for devices such as servers, storage and telecommunications infrastructure equipment, 1080 and 106 glass cloth styles have been common for a long time, with styles such as 1086 and 1067 also now common and growing rapidly. Styles such as 1037, 1035, and even 1027 are beginning to be used in more applications as well. Some of these glass styles are commonly “expanded” or “spread,” where the filaments in a yarn are spread out after the weaving process. This results in a more uniform distribution of resin and glass in the laminate or prepreg material. Figure 10.32 illustrates expanding and spreading of the yarns and resulting glass fabrics. Initially such fabrics were used for laser drilling applications where microvias were part of the PCB design. Since resin will be laser ablated much faster than the glass, the more uniform distribution of resin and glass resulted in more uniform microvia quality. In fabrics with very glass-rich areas and large spaces between the yarns, the resulting dielectric would have very resin-rich areas and very glass-rich areas. In the glass rich areas, greater laser energy is required compared to the resin-rich

areas. At a given laser drilling setting, a glass-rich area might not be ablated sufficiently, while a resin-rich area may be over-ablated. The left photo in Fig. 10.33 shows a glass-rich area insufficiently ablated, as you can see part of a glass yarn still remaining over the innerlayer copper surface. The same laser setting was able to ablate to the inneralyer copper surface when a spread glass cloth was used, as shown in the picture on the right. This is also discussed in Chap. 25 on High Density Interconnection (HDI). In addition, expanding or spreading can also result in improved resin-to-glass wetting for CAF resistance, allow for better thickness control and dimensional stability, and also improve signal integrity. These topics will be discussed further in Chap. 14.

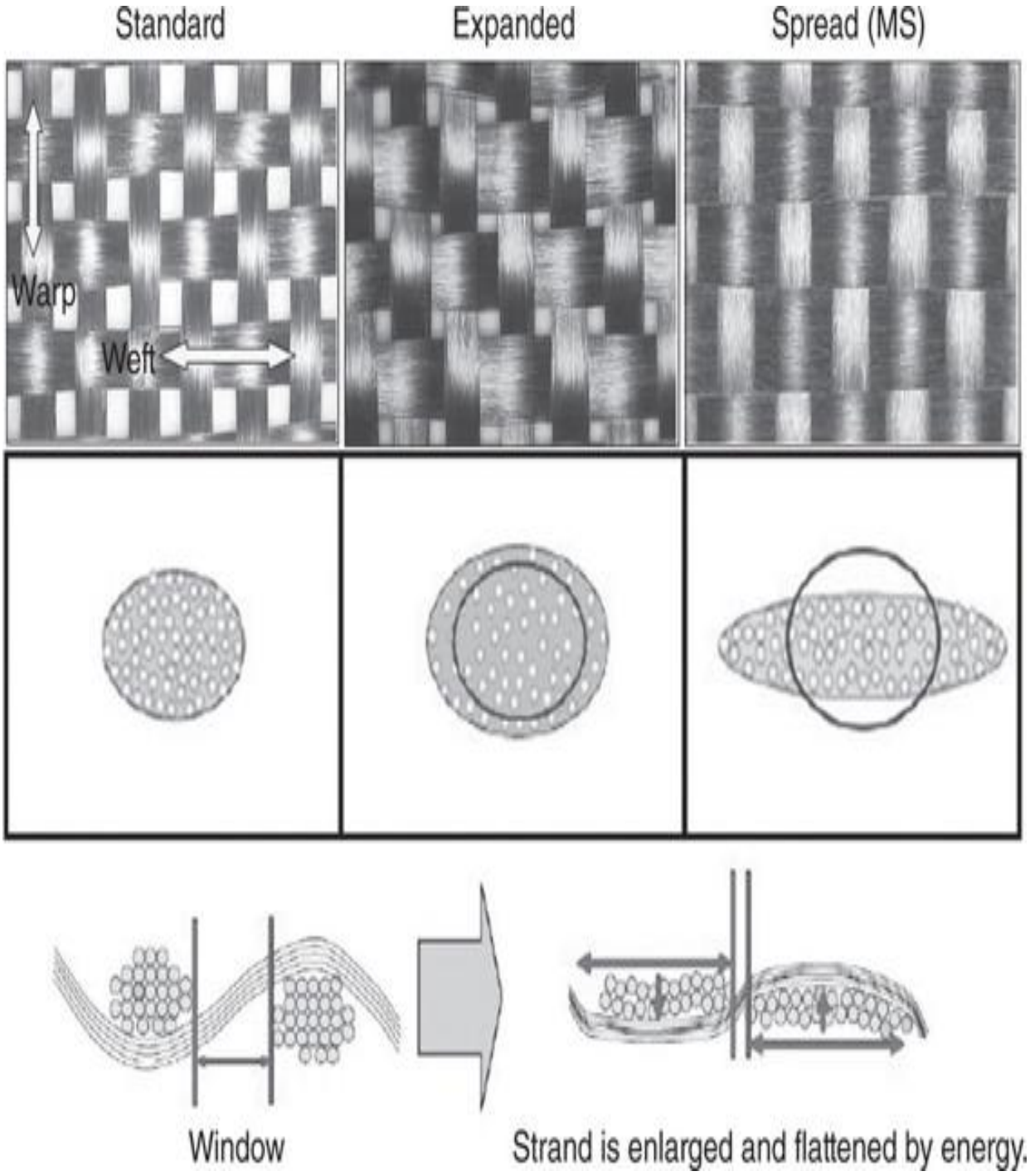


FIGURE 10.32 2116 and 1652 Glass fabrics.

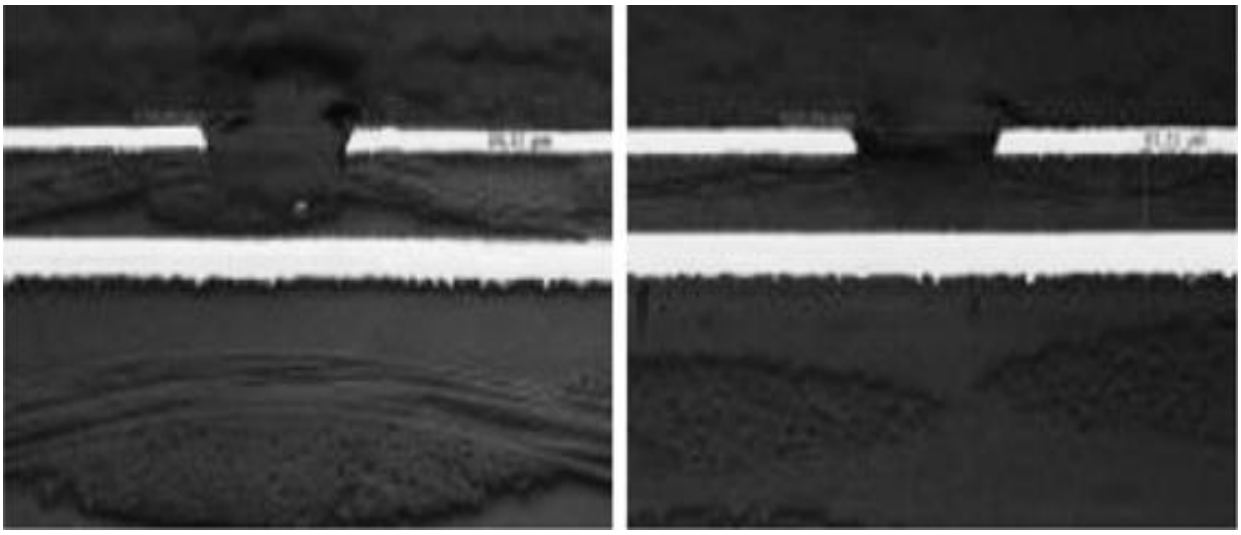


FIGURE 10.33 1506 and 7628 Glass fabrics.

During the manufacture of the filaments and woven fabrics, a variety of surface finishes may be applied to the glass in order to improve manufacturability and to help prevent abrasion, static, and to aid in holding the filaments together. The most important of these surface finishes to the laminate and printed circuit manufacturer is the coupling agent applied to the finished fabric. The coupling agent, typically an organosilane compound, aids in the wetting of and adhesion to the resin applied to the glass. It is important for the reliability of the finished circuit board that this coupling agent improves the resin to glass adhesion during both the circuit manufacturing process, for example, in mechanical drilling, as well as during the actual end use environment of the circuit. The coupling agent also plays a role in long term CAF resistance, which is discussed in Chap. 14. A variety of these compounds are commercially available, with the specific choice primarily driven by the type of resin to be applied to the fiberglass cloth. Figure 10.34 provides examples of silane coupling agents.

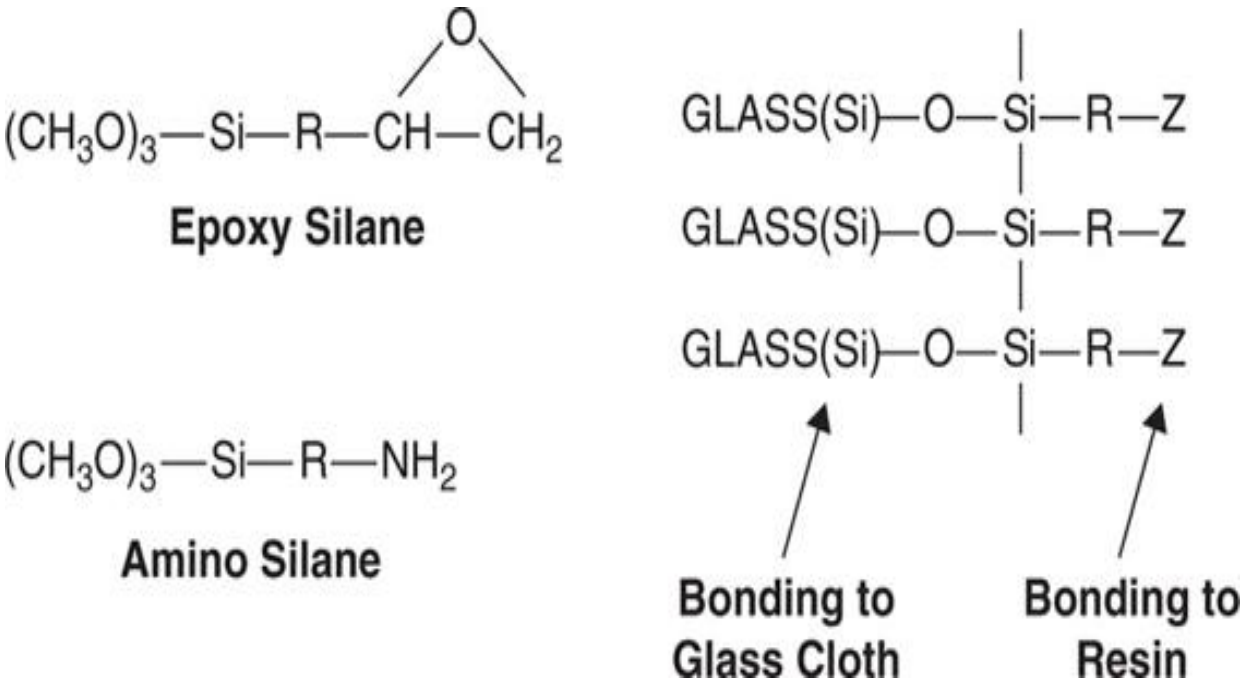


FIGURE 10.34 Examples of silane coupling agents.

10.5.4 Other Reinforcements

While woven fiberglass cloth makes up the overwhelming majority of the reinforcements used for printed circuit base materials, there are other types that can be used exclusively or in combination with woven glass fabric. These other reinforcements include the following.

10.5.4.1 Glass Matte. As opposed to woven cloths, glass matte reinforcement exhibits a more random orientation. Chopped strand matte consists of fiberglass strands that have been chopped into 1- to 2-in lengths and distributed evenly. Continuous strand matte, as the name implies, consists of continuous strands of fiberglass in a random, spiral orientation. Glass matte is used in the core of CEM-3, which is used in relatively unsophisticated products.

10.5.4.2 Aramid Fiber. As opposed to the inorganic chemistry of fiberglass reinforcements, aramid fibers consist

of aromatic polyamide organic compounds, and therefore exhibit different properties. The unique properties of aramid fibers can offer advantages in specific high-performance printed circuits and laminate based multichip modules (MCM-L). For example, aramid fiber reinforced materials are sometimes used in microvia applications since they are easily ablated by plasma or laser. Other interesting properties of aramid fibers are their low weight, high strength, and negative coefficient of thermal expansion (CTE) in the axial direction. When combined with the resin system, the resulting composite can offer reduced overall CTEs in the X-Y plane compared to conventional materials.

10.5.4.3 Paper. Cellulose-based papers can also be used as a reinforcement for base materials. Paper-based reinforcements are also used in conjunction with other reinforcements such as woven glass, and these materials can also allow punching of through holes rather than drilling. This makes them economical in some high-volume, low-technology applications including consumer electronics such as radios, toys, calculators and television games. Paper is used in FR-2, FR-3, and the core of CEM-1.

10.6 CONDUCTIVE MATERIALS

The primary conductive material used in printed circuits is copper foil. However, the trend toward circuit densification and higher operating frequencies has brought about recent developments in copper foil technology as well. In addition, copper foils subsequently plated with other metal alloys are employed to manufacture printed circuits with resistive components buried within a multilayer structure. Copper foil grades are shown in Table 10.7.

TABLE 10.7 Foil Grades from IPC-4562[4]

Grade	Foil Description
1	Standard electrodeposited (STD-Type E)
2	High ductility electrodeposited (HD-Type E)
3	High-temperature elongation electrodeposited (HTE-Type E)
5	As rolled-wrought (AR-Type W)
7	Annealed-wrought (ANN-Type W)
8	As rolled-wrought low-temperature annealable (LTA-Type W)
9	Nickel, standard electrodeposited
10	Electrodeposited low-temperature annealable (LTA-Type E)
11	Electrodeposited annealable (A-Type E)

10.6.1 Electrodeposited Copper Foil

The most common foil used in manufacturing printed circuits is electrodeposited copper foil (ED foil). ED foil is produced through the use of an electrochemical process where copper feed stock or scrap copper wire is first dissolved in a sulfuric acid solution. The purified copper sulfate/sulfuric acid solution is then used to electroplate copper onto a cylindrical drum typically made from stainless steel or titanium. Figure 10.35 illustrates the overall process used to make electrodeposited copper foil. This process results in a copper foil with a relatively smooth, shiny side, and a coarser matte side, as illustrated in Fig. 10.36. The shiny side mirrors the surface of the plating drum while the microscopically rough matte side is formed by the copper grain structure. By controlling the plating solution chemistry, the surface

condition of the plating drum, and the electroplating parameters, the properties of the copper foil can be modified for various usage environments. For example, mechanical properties such as tensile strength and elongation, as well as the surface profile of the matte side, can all be adjusted through control of these process variables. The foil produced in this process is then run through a treatment process. This treatment process typically plates copper nodules that further roughen the surface for adhesion, and also applies other metal barrier layers and antitarnish coatings, as shown in Fig. 10.37. Standard copper foil area weights and thicknesses were shown in Chap. 10, Table 10.6.

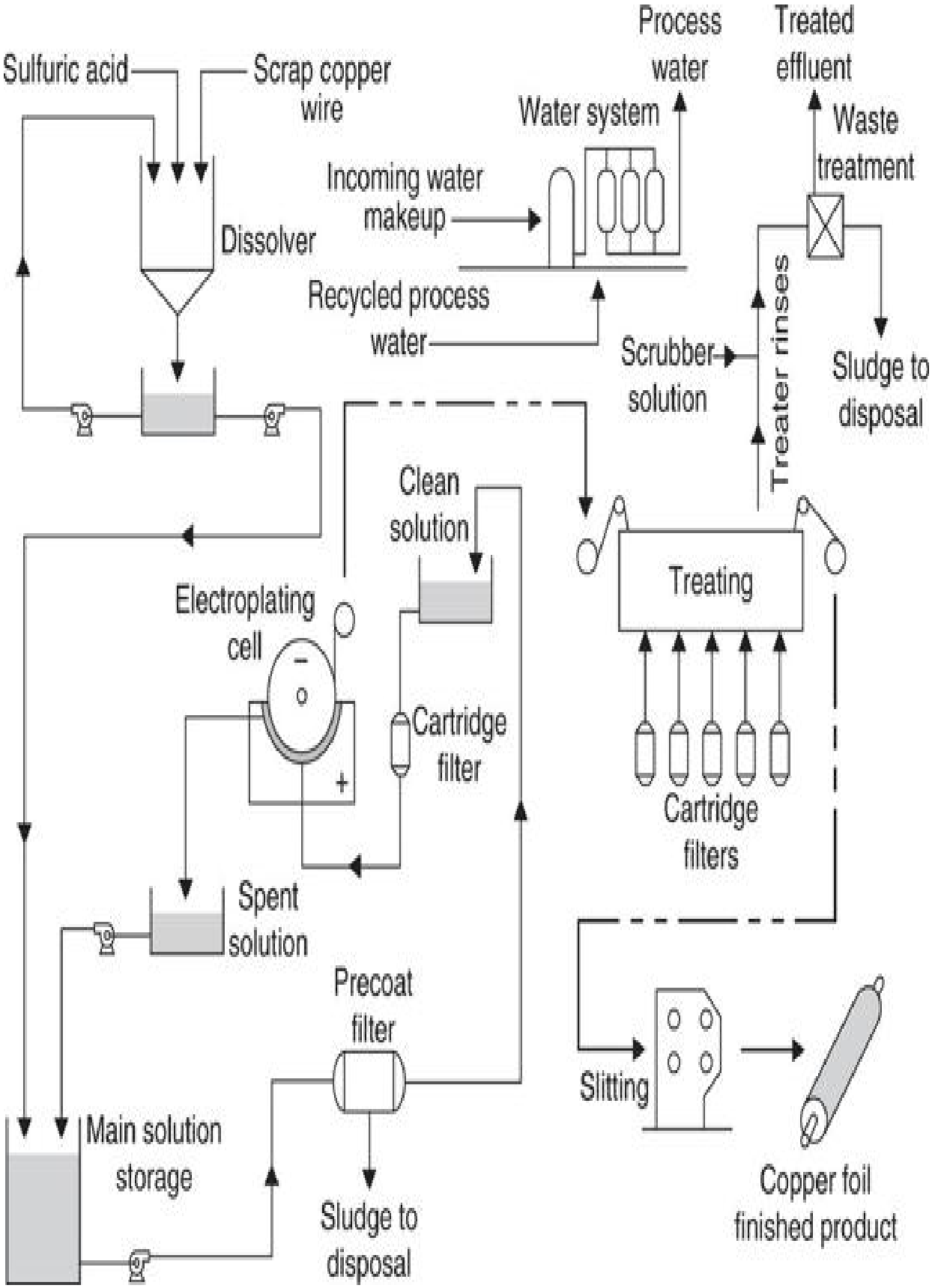

Sulfuric acid
Scrap copper wire
Process water
Treated effluent
Water system
Waste treatment
Incoming water makeup
Dissolver
Recycled process water
Scrubber solution
Treater rinses
Sludge to disposal
Clean solution
Electroplating cell
Treating
Cartridge filter
Cartridge filters
Spent solution
Precoat filter
Slitting
Main solution storage
Sludge to disposal
Copper foil finished product

FIGURE 10.35 Process for manufacturing electrodeposited copper foil.

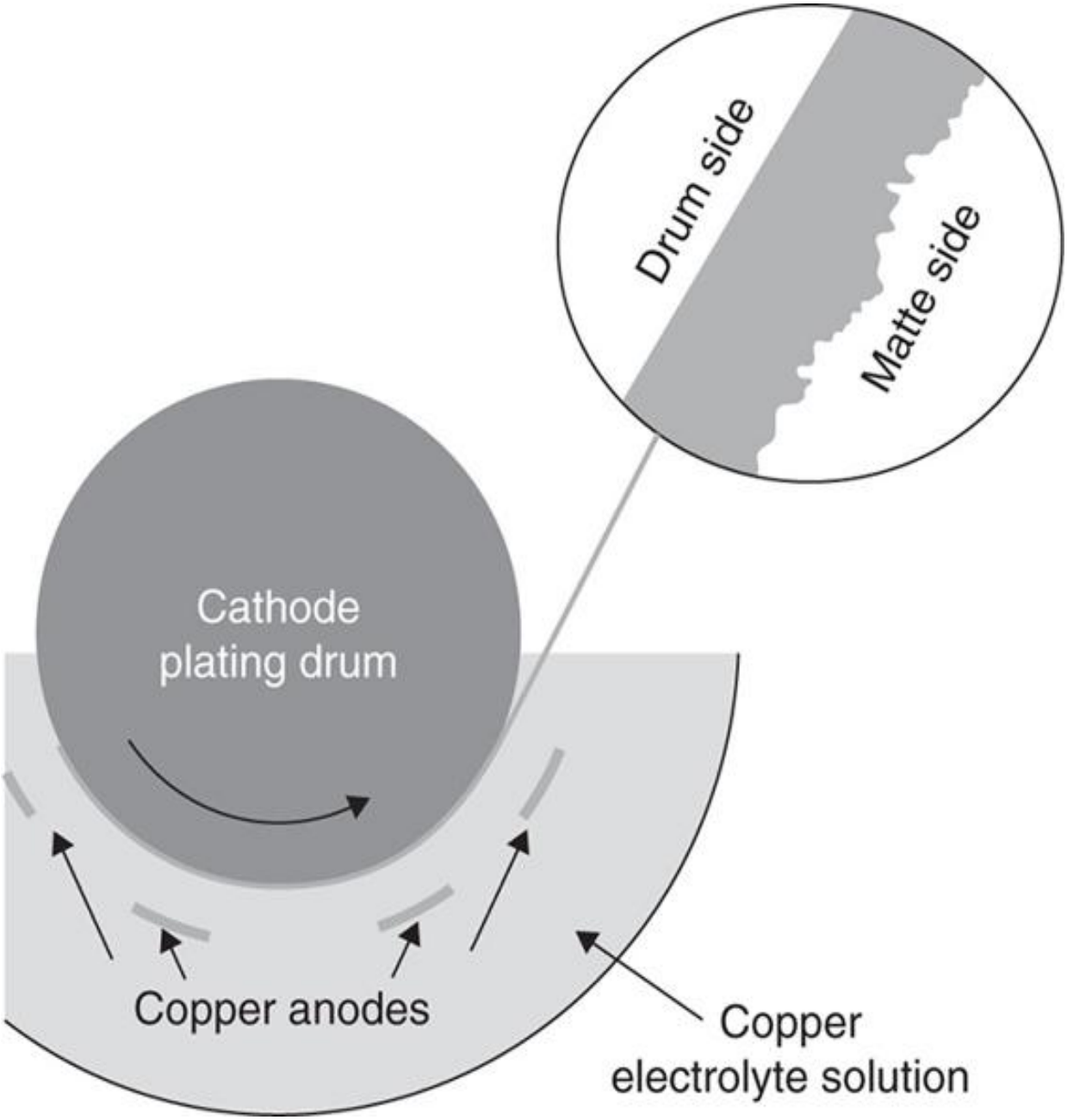


FIGURE 10.36 Electroplating copper foil.

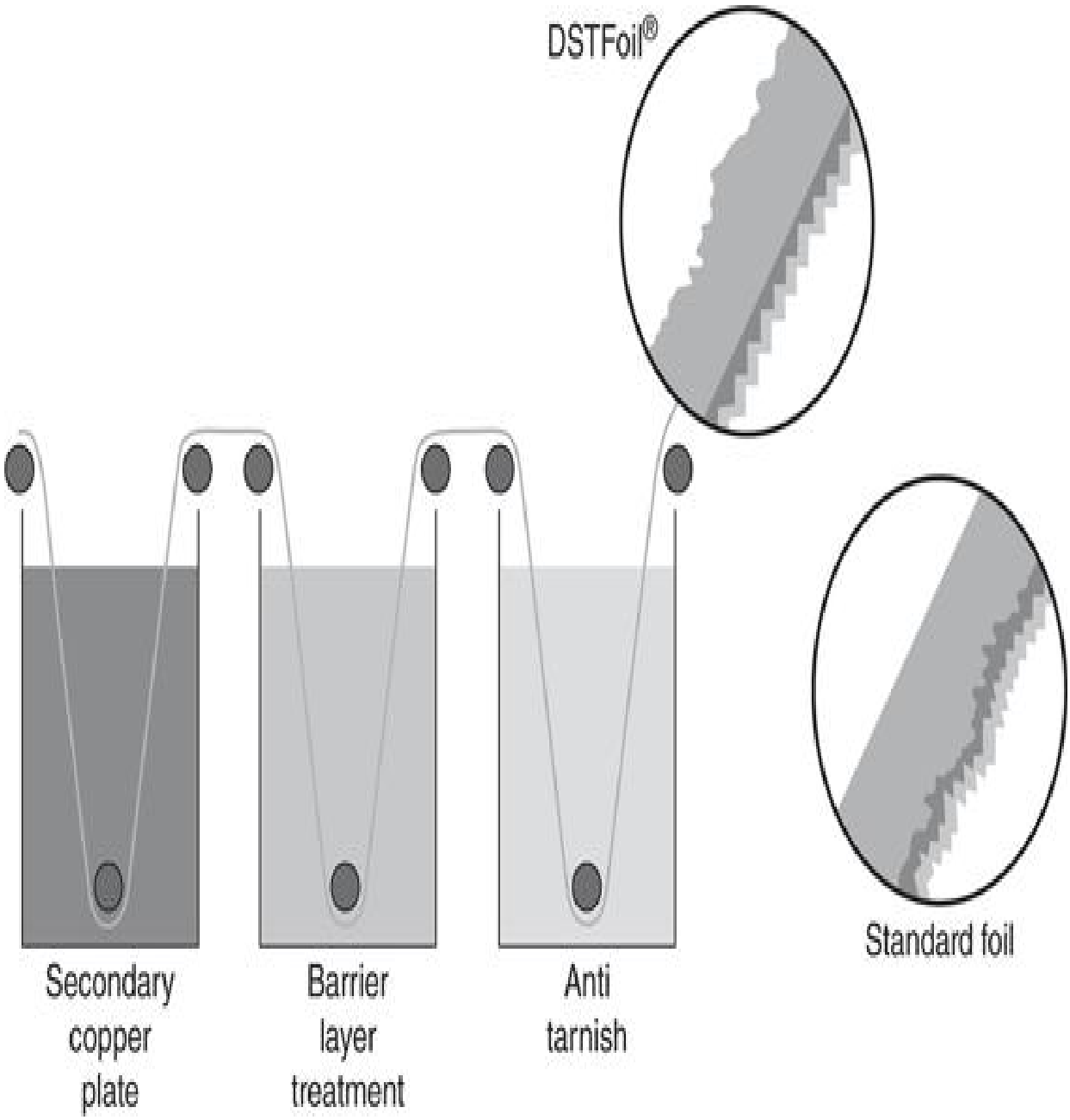


FIGURE 10.37 Treating of copper foil.

The foils most commonly used in printed circuit manufacturing are grade 1 and grade 3 foils. Unlike grade 1 foil, grade 3 foil must meet specific elongation requirements at elevated temperatures (180°C). Grade 3 foil, also commonly referred to as high-temperature elongation, or simply “HTE” foil, is widely used in base laminates used to

manufacture multilayer printed circuit boards. The increased ductility at elevated temperatures provides resistance to copper foil cracks when the multilayer circuit is thermally stressed and expands in the *z* axis. Changes to the plating bath are made to alter the grain structure of HTE foil. This results in different mechanical properties. Tables 10.8 and 10.9 show the tensile strength and ductility requirements for standard grade 1 copper foil and high-temperature elongation grade 3 copper foil. These requirements come from IPC-4562 “Metal Foil for Printed Board Applications,” which lists requirements for the other grades as well. It is recommended to check the latest revision of these specifications to confirm the current requirements.

TABLE 10.8 Tensile and Elongation Properties of Grade 1 Copper Foil

Property @ 23°C	½ Oz	1 Oz	2 Oz
Tensile Strength:			
kpsi	30	40	40
MPa	207	276	276
Elongation %	2	3	3

TABLE 10.9 Tensile and Elongation Properties of Grade 3 Copper Foil

Property	½ Oz	1 Oz	2 Oz
Tensile Strength @ 23°C:			
kpsi	30	40	40
MPa	207	276	276
Elongation % @ 23°C	2	3	3
Tensile strength @ 180°C:			
kpsi	15	20	20
MPa	103	138	138
Elongation % @ 180°C	2	2	3

The surface profile of the copper foil is also important in printed circuit manufacturing. On one hand, a relatively rough surface profile aids in the bond strength of the foil to the resin system. On the other hand, a rough profile may require longer etching times, which impact productivity and the geometry of the etched features. With longer etching times, there is an increased propensity to form trapezoidal circuit traces since there is more time for lateral etching of the conductor. This has obvious implications for manufacturing fine line circuits in high yield and controlling impedance properties. In addition, as circuit operating frequencies increase, roughness of the copper foil will impact signal attenuation. At higher frequencies, more of the electrical signal is conducted near the surface of the conductor. A rougher profile results in a longer path for the signal to travel, which also results in greater attenuation, or loss. As a result, high-performance materials for high-speed circuits require foils with low profiles that have adequate adhesion to the high-performance resin systems. This is the subject of much research and development and will be discussed further in Chap. 14.

Low profile and very low profile characteristics are included in the IPC-4562 specification and are summarized in Table 10.10. Figures 10.38 and 10.39 give an example of profile differences between these foils, as defined in this specification. However, there have been a number of new copper foils developed and now in volume use that have even lower profiles. New ranges for these lower profiles have not yet been established in this specification, though the committee responsible for this specification is working on this. As such, it is recommended to check the latest revision of this specification for any updates. In the meantime, some suppliers will call out the foil as VLP along with the average roughness, that is, a foil with an average of 2 µm roughness would be called VLP-2. This is becoming more and more important as the roughness has a significant effect on signal loss at high frequencies.

TABLE 10.10 Foil Profile Criteria

Foil Profile Type	Max. Foil Profile (µm)	Max. Foil Profile (µin)
S – Standard	N/A	N/A
L – Low profile	10.2	400
V – Very low profile	5.1	200
X – No treatment or roughness	N/A	N/A

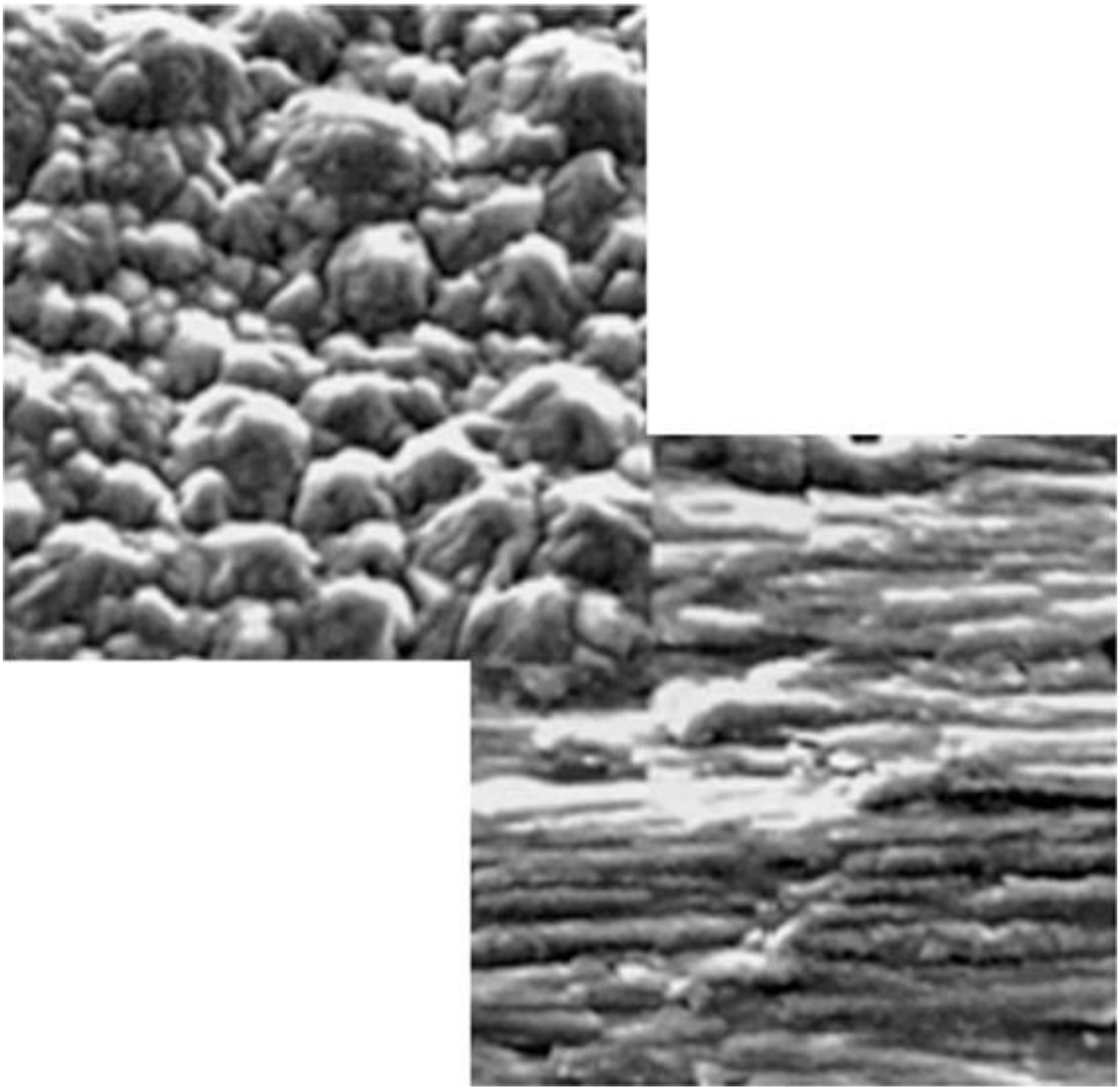


FIGURE 10.38 Cross section and matte side of standard grade 1 foil.

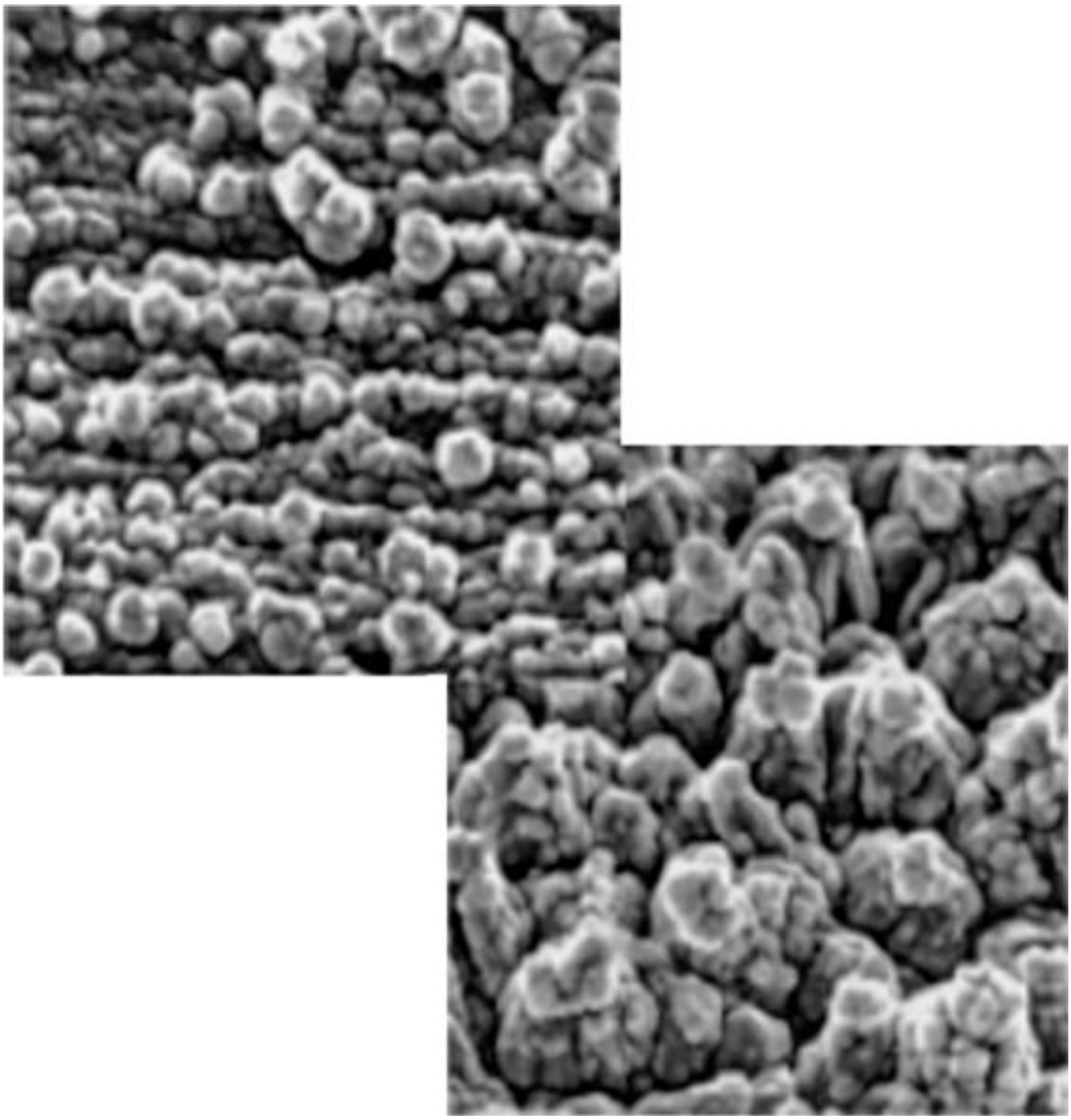


FIGURE 10.39 Cross section and matte side of low profile grade 1 foil.

Subsequent to the manufacturing of the base copper foil, a variety of surface treatments are typically applied, and these too will vary depending on the usage environments. These treatments fall into four categories.

10.6.1.1 Bonding Treatments or Nodularization. This treatment increases the surface area of the foil by plating

copper or copper-oxide nodules to the surface of the foil. The increased surface area results in increased foil to resin bond strengths. The thickness of this treatment is relatively small, but can be tailored for adhesion to high performance resin systems. The matte side images in Figs. 10.40 and 10.41 include these nodules.

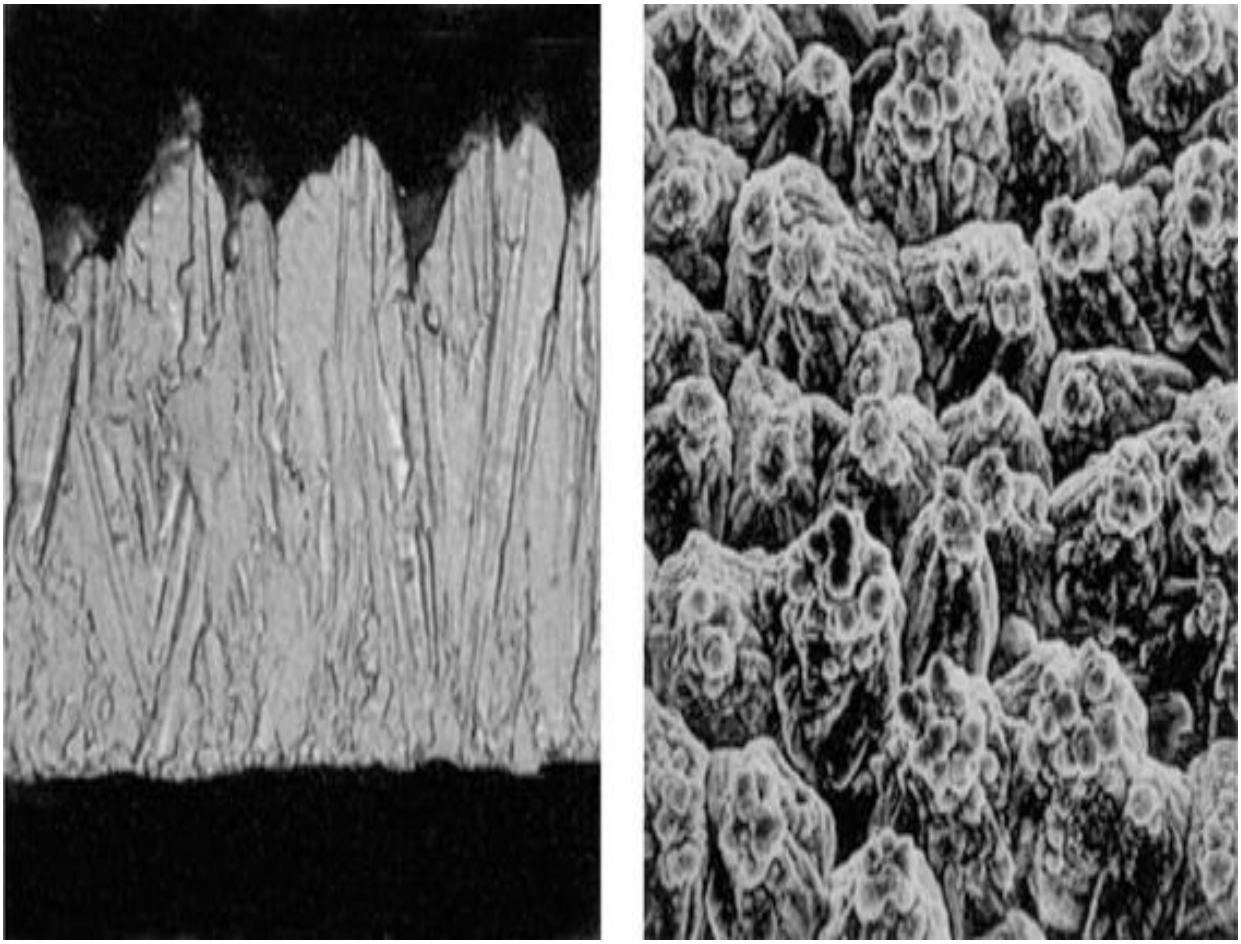


FIGURE 10.40 External sides for RTF (upper photo) and standard (lower photo) foils.

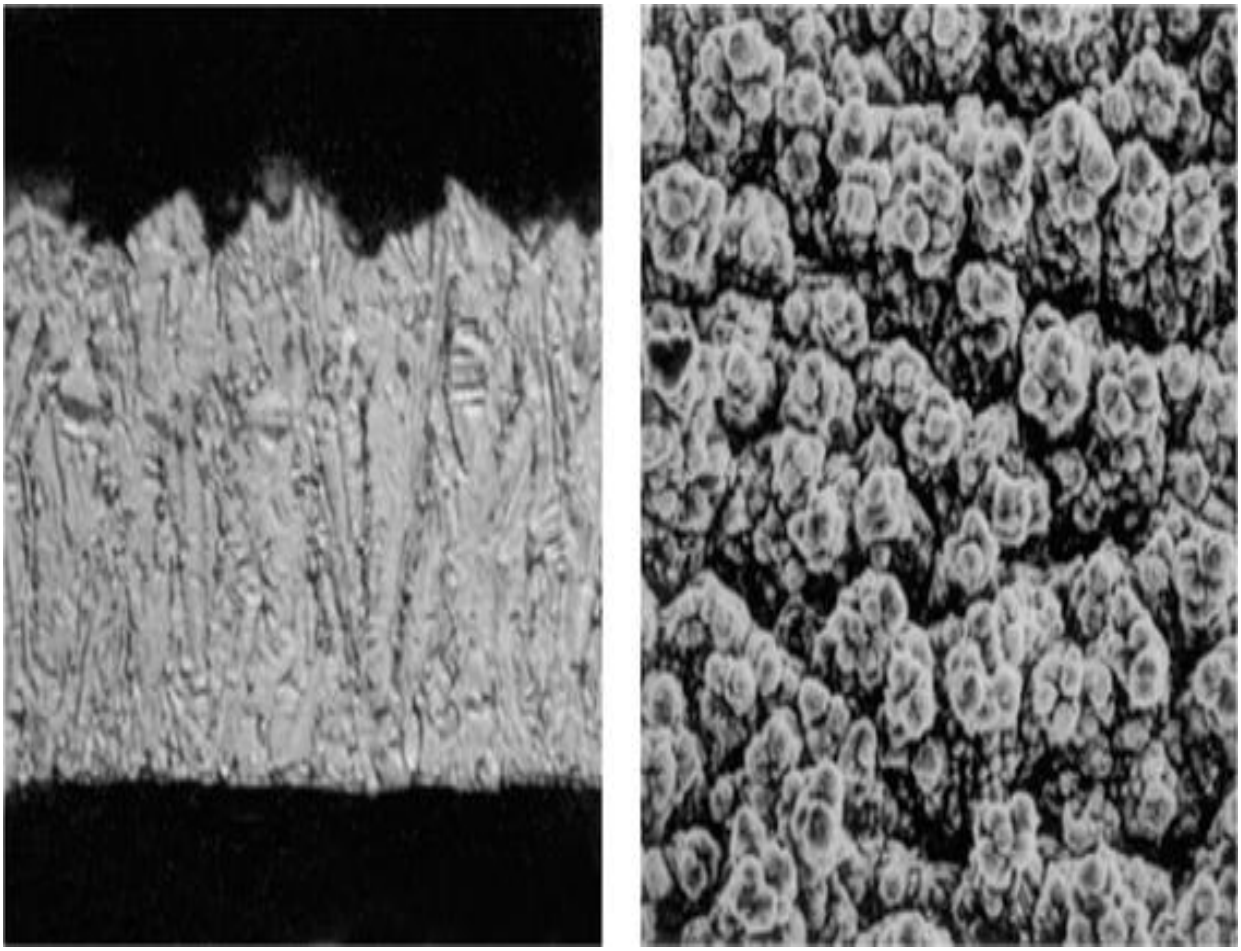


FIGURE 10.41 Sides bonded to laminate for RTF (upper photo) and standard foils (lower photo).

10.6.1.2 Thermal Barriers. A coating of zinc, nickel, or brass is usually applied over the nodules. This coating can prevent thermal or chemical degradation of the foil to resin bond during manufacture of the laminate, the printed circuit, and the circuit assembly. These coatings typically measure several hundred angstroms in thickness and vary in color due to the specific metal-alloy used, although most treatments are brown, gray, or a yellow mustard color. Low levels of arsenic have been used in foil treatments for a long time, though in recent times the use of arsenic-free foils is growing.

10.6.1.3 Passivation and Antioxidant Coatings. In contrast to the other coatings, these treatments are virtually always applied to both sides of the foil. Although many of these treatments have been chromium based, organic coatings can also be utilized. The primary purpose of these treatments is to prevent oxidation of the copper foil during storage and lamination. These coatings are usually less than 100 angstroms thick and are typically removed by the cleaning, etching or scrubbing processes normally used at the start of printed circuit manufacturing processes.

10.6.1.4 Coupling Agents. The use of coupling agents, primarily silanes like those used to promote fiberglass to resin adhesion, can also be used on copper foils. These coupling agents can improve the chemical bond between the foil and the resin system and can also be used to help prevent oxidation or contamination.

10.6.2 Drum Side Treated Foils or Reverse Treated Foils

Drum side treated (DSTFoil®) or reverse treated foil (RTF) is also an electrodeposited copper foil, but the treatments are coated onto the smooth drum side of the foil rather than the matte side, as with conventional electrodeposited foil (see Figs. 10.36 and 10.37). This results in a very low profile surface bonded to the laminate, with the rough matte side facing out. The low surface profile against the laminate aids in the production of fine circuit features on the innerlayer, while the matte surface can aid in photoresist adhesion. The low profile against the laminate can also improve electrical performance at high frequencies. In addition, in very thin laminates the low surface profile can aid in achieving consistent dielectric thickness with a reduced concern of inadequate dielectric separation between the corresponding

points on the tooth profile. These benefits come at the price of a slight reduction in peel strength.

10.6.3 Wrought Annealed Copper Foils

Wrought annealed foil is typically used in flexible circuit manufacturing because of its superior ductility. In contrast to an electrodeposition process, wrought annealed foil begins with a slab or ingot of copper that is worked through a series of rollers in conjunction with heat cycles to obtain the desired thickness and mechanical properties. The resulting grain structure of wrought annealed copper foil, which is very random compared to the columnar or fine-grain structure of electrodeposited foil, is a significant contributor to the differences in mechanical properties. In addition, wrought annealed foil consists of two very low profile sides, so the treatment steps account for any surface roughness. The tensile and elongation requirements for grade 7 wrought annealed copper are provided in Table 10.11. The requirements for other wrought foils are included in IPC-4562, and as always, the latest revision of these specifications should be checked to validate current requirements.

TABLE 10.11 Tensile and Elongation Properties of Wrought Annealed Foil

Property	½ Oz	1 Oz	2 Oz
Tensile strength @ 23°C:			
kpsi	15	20	25
MPa	103	138	172
Fatigue ductility % @ 23°C	20	35	65
Elongation % @ 23°C	5	10	20
Tensile strength @ 180°C:			
kpsi	10	13	18
MPa	69	90	124
Elongation % @ 180°C	3	5	10

10.6.4 Copper Foil Purity and Resistivity

IPC-4562 Metal Foil for Printed Wiring Applications also specifies the purity and resistivity of electrodeposited and wrought copper foils. Electrodeposited copper foils without treatment shall have a minimum purity of 99.8 percent, with any silver counted as copper. The value for wrought foils is 99.9 percent. Table 10.12 provides the resistivity requirements for electrodeposited foil. The maximum resistivity requirements for wrought copper range from 0.155 to 0.160 Ωg/m^2, depending on the weight.

TABLE 10.12 Maximum Resistivity of Deposited Foil

Weight Designator	Common Industry Terminology	Maximum Resistivity
E	5 µm	0.181 Ωg/m^2
Q	9 µm	0.171 Ωg/m^2
T	12 µm	0.170 Ωg/m^2
H	½ oz	0.166 Ωg/m^2
M	¾ oz	0.164 Ωg/m^2
1 oz and over (305 g/m^2)	1 oz...	0.162 Ωg/m^2

10.6.5 Other Foil Types

10.6.5.1 Double Treated Copper Foil. As discussed in the preceding text, the foil surface that is bonded to the base laminate is treated with coatings designed to improve foil to resin bond strength and reliability. In double treated foils, these coatings are also applied to the foil surface that forms the outside laminate surface. It is also possible to have a “reverse treated” double treat foil, meaning that the smooth surface is bonded to the laminate with the matte surface facing out, while both sides have been treated.

The advantage of double treat foil is that it eliminates the oxide or other surface preparation process typically used to prepare the innerlayer circuitry for multilayer lamination. However, no abrasion of this double treat coating can be tolerated, and removal of any surface contamination becomes difficult. This also makes double treated foil more sensitive to handling practices in the circuit manufacturing process.

10.6.5.2 Resistive Foils. Other treatments can also be applied to the base foil for use in manufacturing innerlayer circuits with *buried resistors*. This technology can enable the creation of resistors on internal layers of a multilayer circuit, with removal of many of the resistors commonly assembled on the outside of the multilayer circuit. This can improve board reliability and free up space on the outside of the board for active components. These foils typically use a resistive metal alloy coated onto the base foil. The laminate made with this foil can then be sequentially imaged and etched to produce the desired circuit pattern along with resistive components.

10.7 REFERENCES

1. Dow Technical Literature.
2. IPC-4412 Specification for Finished Fabric Woven from E-Glass for Printed Boards.
3. IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards.
4. IPC-4562 Metal Foil for Printed Wiring Applications.

CHAPTER 11

PROPERTIES OF BASE MATERIALS

Edward Kelley
Douglas Trobough
Isola Group, Chandler, Arizona

11.1 INTRODUCTION

A variety of base material properties are of interest to the printed circuit manufacturer, assembler, and original equipment manufacturer (OEM). These include thermal, physical, mechanical, and electrical properties. This chapter introduces a few of the more important properties and also provides some comparisons between material types. Most of the test methods used to evaluate these properties can be found in the IPC Test Methods Manual, IPC-TM-650, which includes test methods for many other properties as well.[1]

11.2 THERMAL, PHYSICAL, AND MECHANICAL PROPERTIES

Historically, the properties that received the greatest amount of attention were the glass transition temperature, T_g, and the coefficients of thermal expansion (CTEs), particularly in the *z* axis. With the advent of lead-free assembly processes, other properties have increased in importance as well. The most notable is the decomposition temperature, T_d. These properties were described in more detail in Chap. 10, and will be discussed again in Chap. 13, which focuses on the impact of lead-free assembly on base materials. However, some additional information and examples of the test data are included here, as well as comparisons of some common material types.

11.2.1 Thermomechanical Analysis T_g and CTEs

Materials undergo changes in physical dimensions in response to changes in temperature. The rates of expansion of fiberglass cloth reinforced materials differ in the respective axes of the material due to the directionality of the reinforcement. The length and width of the laminate, or printed circuit, are termed the *x*/*y* plane, whereas the axis perpendicular to this plane is the *z* axis.

Thermal expansion can be measured by thermomechanical analysis (TMA). TMA uses a device that measures a dimension of a sample versus temperature. Depending upon the orientation of the sample in the device, either the *x*/*y* CTE or the *z* axis CTE can be measured.

Figure 11.1 provides an example of a TMA scan on a high-T_g, filled FR-4 material designed to be compatible with most lead-free assembly applications. The T_g is determined by extrapolating the linear portions of the expansion curve to

the point where they intersect. In this case, a T_g of 154.45°C is measured. The z-axis CTE values are typically calculated both pre-T_g, also called “alpha 1” (α1), and post-T_g, also called “alpha 2” (α2). In this example, the pre-T_g CTE is measured at just over 45 ppm/°C, and the post-T_g CTE is measured at just over 219 ppm/°C. The total expansion from 50 to 250°C is also shown as a percent expansion value at 2.58 percent.

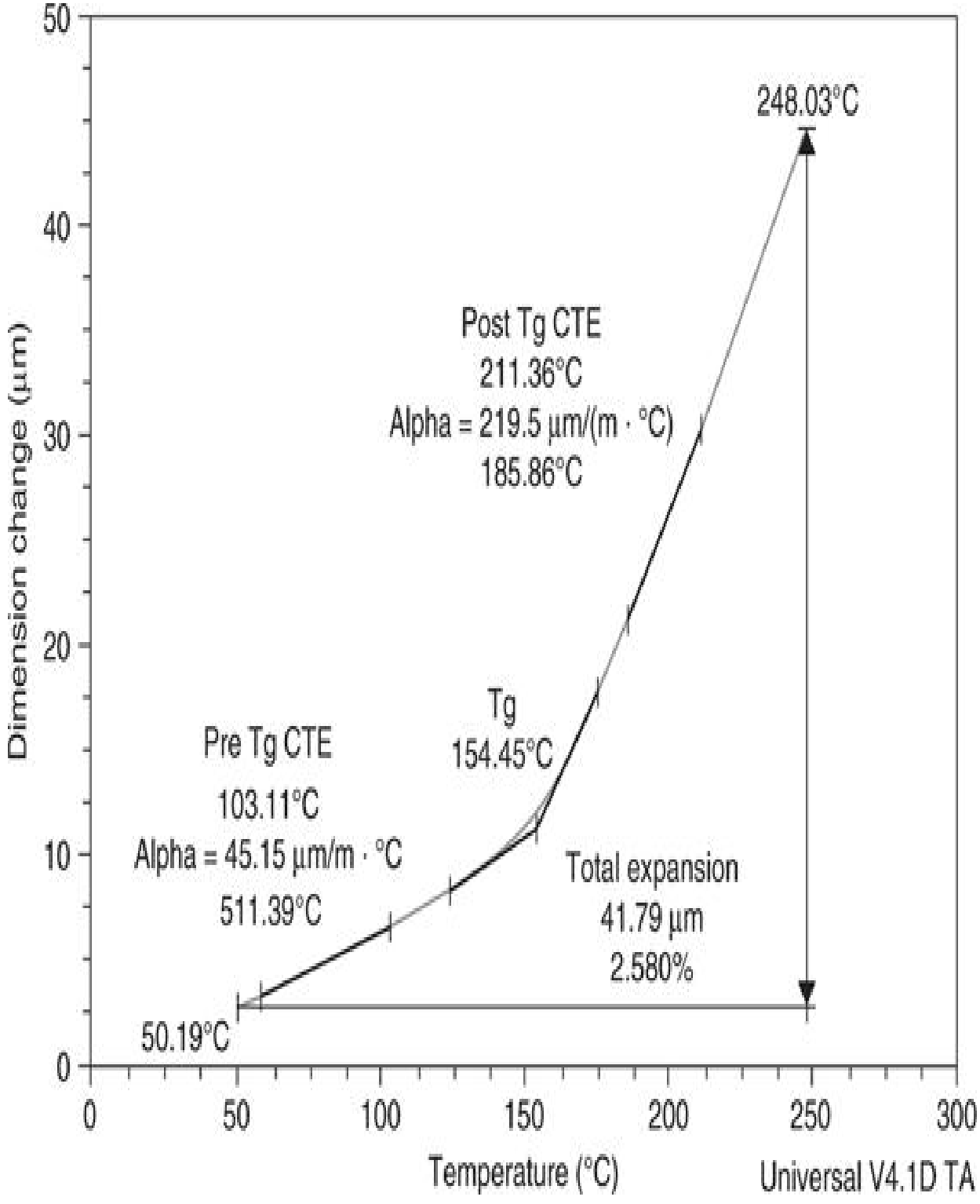


FIGURE 11.1 TMA scan illustrating T_g and CTE determination.

Thermal expansion in the *z* axis can significantly affect the reliability of printed circuits. Since plated through holes run

through the *z* axis of the printed circuit, thermal expansion and contraction in the base materials causes strain and can result in plastic deformation of the copper plated in the hole, and can also deform the copper pads on the surface of the printed circuit. Repeated thermal cycling can ultimately cause cracks in the plated copper, and several test methods have been developed to assess the reliability of printed circuits by exposing them to accelerated thermal cycling. Other things being equal, lower levels of thermal expansion in the base material will improve reliability of the plated through holes.

Thermal expansion in the *x*/*y* axes is of more importance when discussing the attachment of components to the printed circuit. This is of particular importance when chip scale packages (CSPs) and direct chip attach components are used because the difference in thermal expansion between the printed circuit board and the component can compromise the reliability of the bond between them as they undergo thermal cycles. While not generally a problem, the higher temperatures of lead free assembly have raised a concern about constructing a multilayer PCB with layers of dielectrics that have significantly different *x*/*y* CTE properties. The concern is that the dissimilar *x*/*y* CTE properties, if large enough, will result in enough stress to cause a separation or delamination between these layers. This may depend somewhat on the specific type of resin and glass cloth used. Furthermore, hybrid constructions, meaning PCBs that utilize different base material types in the same PCB, should be analyzed very carefully, as different base material types can have different CTE values even with a given fiberglass cloth style and resin content.

11.2.2 CTE Values

CTE values of some common materials at approximately 42 percent resin content are shown in Table 11.1.

TABLE 11.1 T_d and CTE Values at 42 Percent Resin Content of Some Common Base Materials

Material	T_g (°C)	Decomposition Temp., T_d (5% Wt. Loss), °C	Z-Axis Expansion (% from 50–260°C)	X/Y CTE (ppm/°C)
Standard T_g FR-4	140	320	4.2	15–17
Filled mid-T_g FR-4	150	330	3.3	13–14
Halogen free, filled mid-T_g FR-4	155	390	3.1	13–14
High-T_g FR-4	170	300	3.5	13–14
High-T_g/T_d FR-4	175	340	3.5	13–14
Filled high-T_g/T_d FR-4	180	340	2.8	13–14
Halogen-free high-T_g/T_d FR-4	180	395	2.9	13–14
Mid-loss epoxy	200	370	3.0	13–14
BT/Epoxy blend	200	350	3.4	13–14
BT/Epoxy blend-low Dk glass	200	350	3.4	11–13
Low loss epoxy blend	180	360	2.8	15–17
Low loss epoxy blend-low Dk glass	180	360	2.8	14–16
Very low loss	200	360	2.8	12–13
Halogen free very low loss	200	390	2.9	15–17
Ultra low loss	200	390	2.8	12–13
Polyimide	260	416	1.8	12–14

11.2.2.1 Controlling Thermal Expansion. The rate of thermal expansion is a function of the components used in the base material and their relative concentrations. The resin system will have a relatively high coefficient of thermal expansion compared to fiberglass cloth or other types of inorganic reinforcements.

In controlling *z*-axis expansion, the key factors to consider are the choice of resin system, the resin system T_g, and the resin content of the base materials. Fillers in the resin system, in addition to the fiberglass cloth, can also be used to lower the CTE of the material. Table 11.1 compares the thermal expansion of several commercially available base materials. These values can vary significantly based on the exact resin content of the material or PCB tested. In multilayer PCBs, the amount of copper in the sample will also have a significant impact as the *z*-axis expansion of copper is very low compared to the resin system.

Note the general difference in CTE values as T_g increases. A higher T_g delays the onset of the more rapid post-T_g rate of expansion. Also note that the filled materials have lower levels of *z*-axis expansion in comparison to equivalent unfilled materials.

11.2.3 T_g Determination by Other Methods

Besides TMA, two other methods are commonly used to measure T_g. These are differential scanning calorimetry (DSC) and dynamic mechanical analysis (DMA). DSC measures heat flow versus temperature rather than dimensional changes as measured by TMA. The heat absorbed or given off will change as the temperature increases through the T_g of the resin system. T_g measured by DSC is typically higher than measurements by TMA. DMA

measures the modulus of the material versus temperature and also typically results in higher measured values of T_g.

As more complex resin systems are developed, and as more blends of resins are used, it becomes more difficult to measure T_g by TMA. For example, if two resins are used that have somewhat different TMA T_g's, the combination of the two resins can make it difficult to get a clear transition in expansion rates. For these materials, DSC is the preferred technique for measuring T_g. Figures 11.2 and 11.3 provide examples of DSC and DMA scans, respectively, and the resulting measurement of T_g.

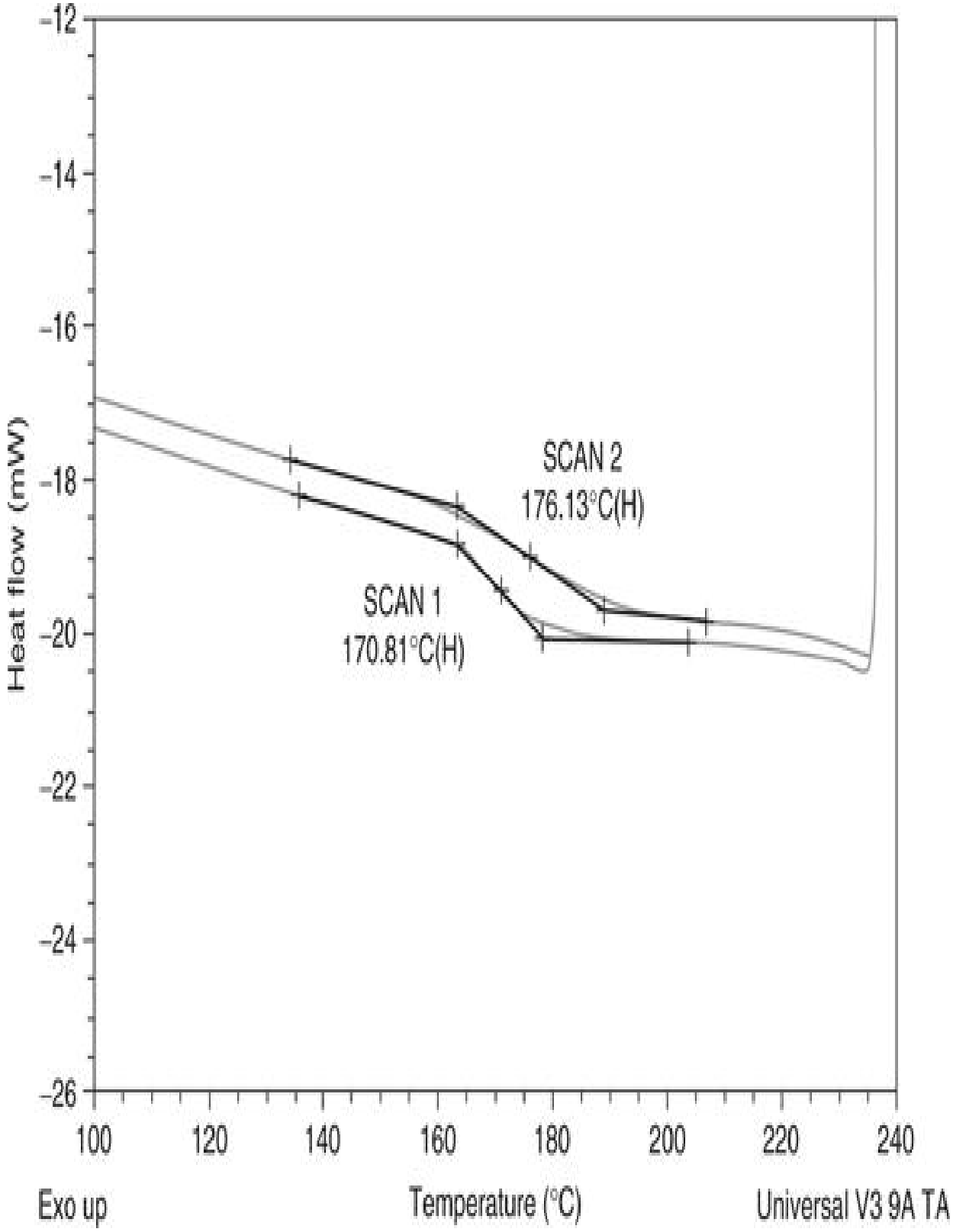


FIGURE 11.2 Measurements of T_g by DSC.

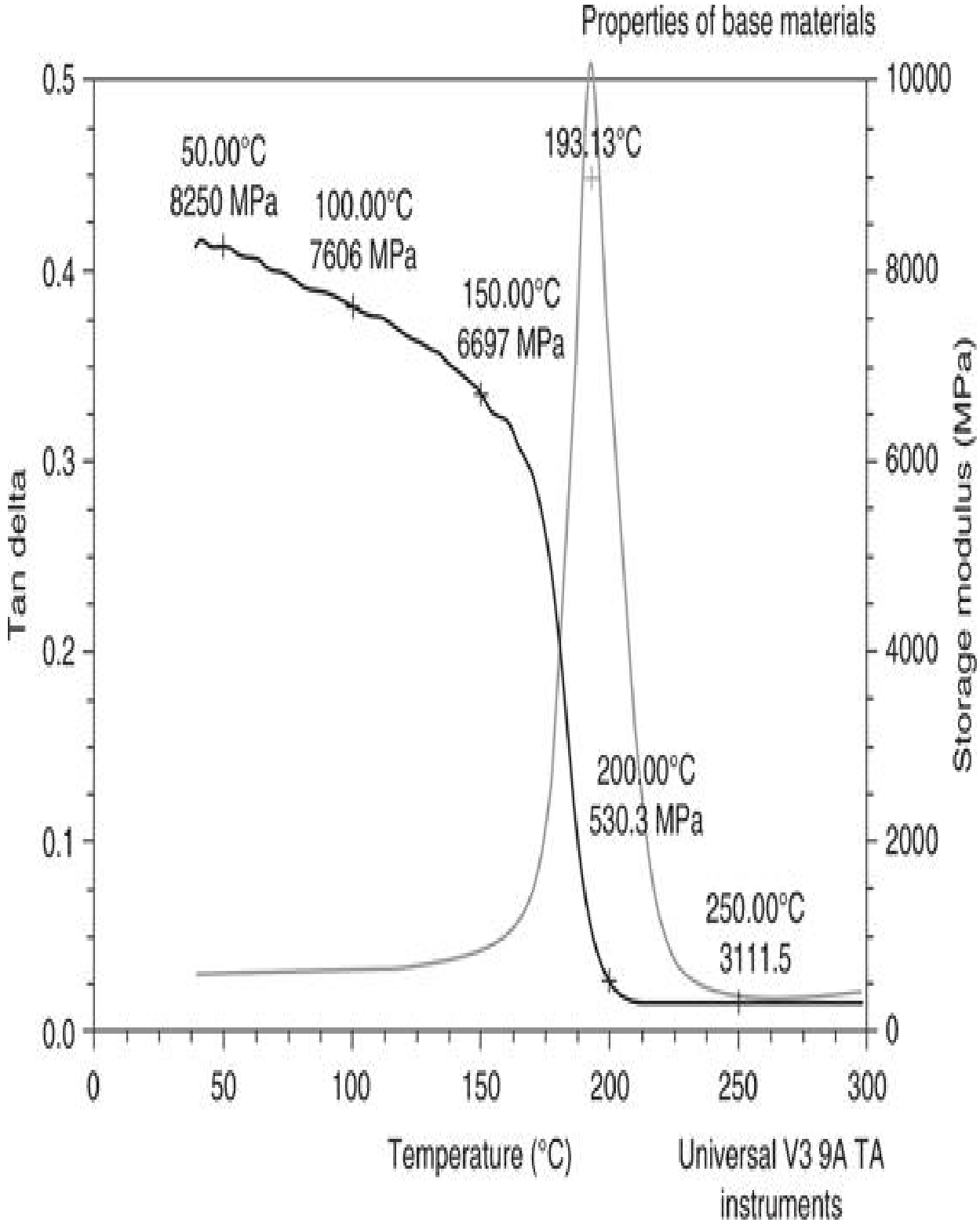


FIGURE 11.3 Measurement of T_g by DMA.

11.2.4 Decomposition Temperature

As a material is heated to higher temperatures, a point is reached where the resin system will begin to decompose. The chemical bonds within the resin system begin to break down and volatile components are driven off, reducing the mass of the sample. The decomposition temperature, T_d, is a property that describes the point at which this process occurs. The traditional definition of T_d is the point where 5 percent of the original mass is lost to decomposition. Table 11.1 shows 5 percent decomposition temperatures for several common materials. However, 5 percent is a very large number when multilayer PCB reliability is considered, and temperatures where lower levels of decomposition occur are very important to understand, particularly with respect to lead-free assembly. To illustrate this, consider Fig. 11.4.

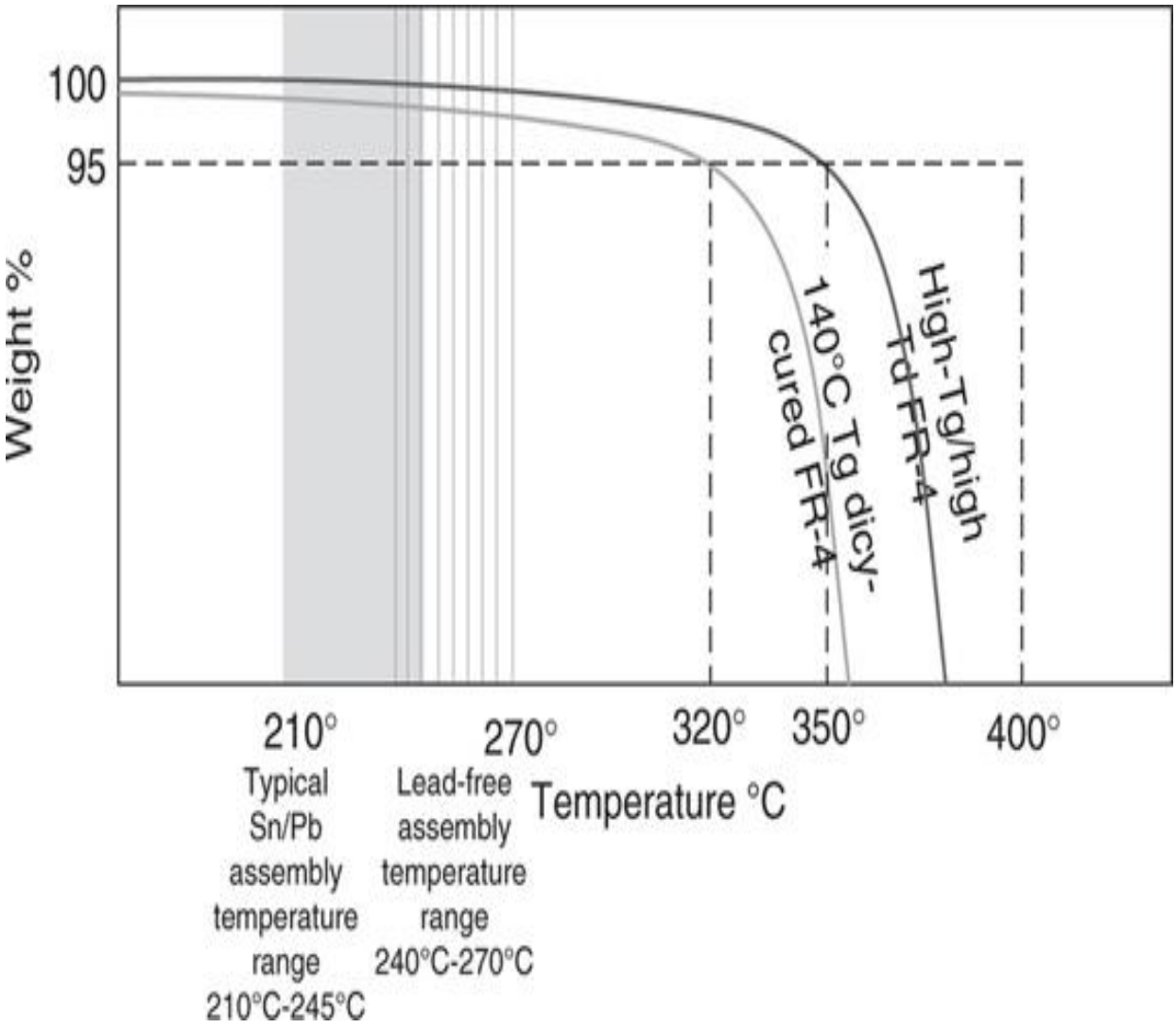


FIGURE 11.4 Illustration of decomposition temperature measurement.

In Fig. 11.4, you can see curves for two FR-4 materials. The 140°C T_g dicy-cured FR-4 has a decomposition temperature of 320°C by the 5 percent weight loss definition. The high-T_g/high-T_d FR-4 has a decomposition temperature of 350°C by the 5 percent weight loss definition. Many dicy-cured high-T_g FR-4 materials actually have decomposition temperatures in the range of 290 to 310°C, whereas the dicy-cured 140°C T_g FR-4 materials generally have slightly higher T_d values. The shaded regions indicate the peak temperature ranges for standard tin-lead assembly and lead-

free assembly. A very common question is, if a PCB will be assembled at 260°C, and the material has a decomposition temperature of 310 to 320°C, then why wouldn’t it be compatible with lead-free assembly?

The answer lies in the level of decomposition in the temperature ranges where assembly will take place. In the tin-lead temperature range, neither material exhibits a significant level of decomposition. However, in the lead-free assembly temperature range, the traditional dicy-cured FR-4 begins to exhibit 1.5 to 3 percent weight loss. This level of decomposition can compromise long-term reliability or result in defects such as delamination during assembly, particularly if multiple assembly cycles or rework cycles are performed. Figures 11.5 through 11.7 show thermogravimetric analysis (TGA) curves assessing decomposition temperatures for three types of base material.

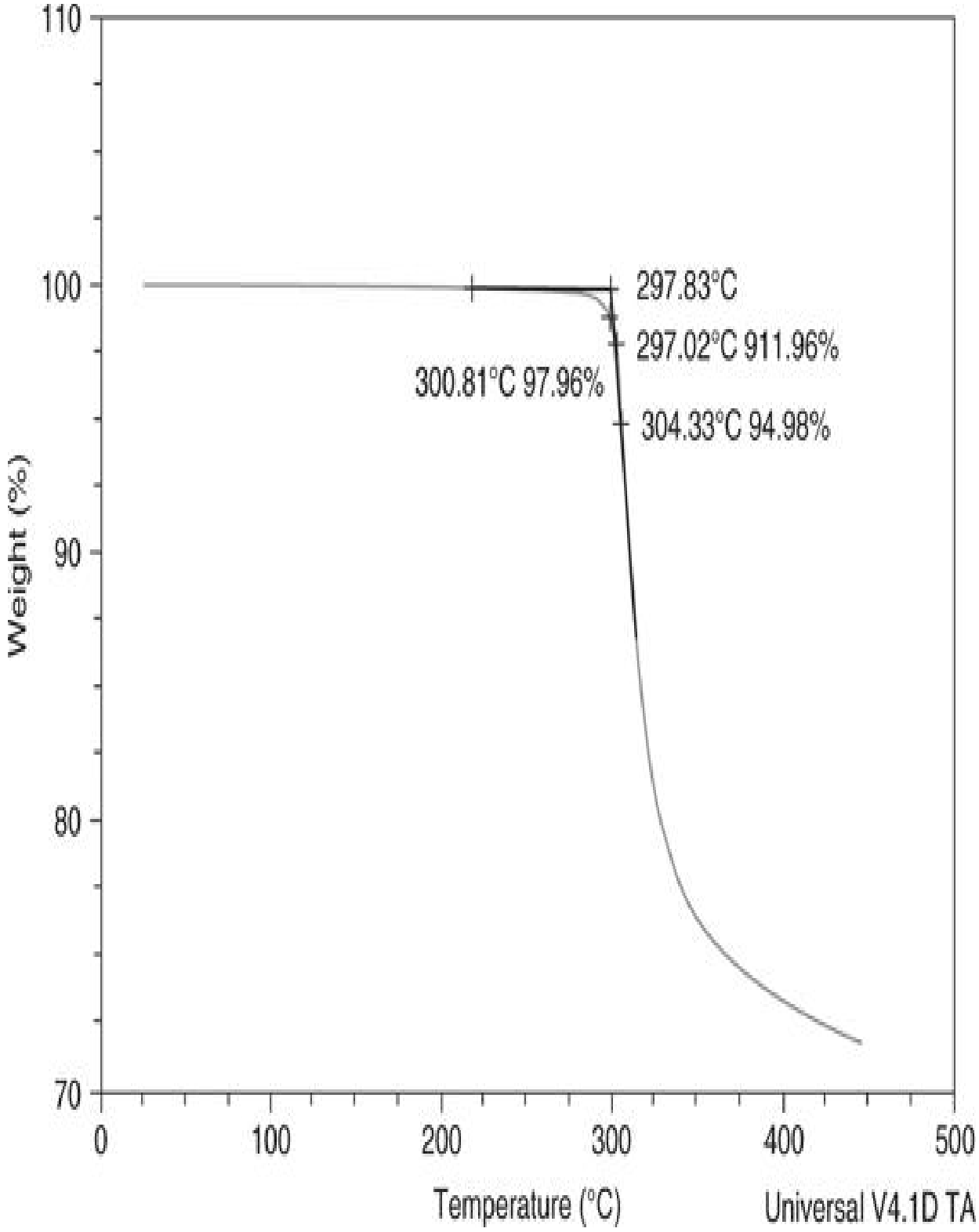


FIGURE 11.5 Decomposition curve for dicy-cured high-T_g FR-4.

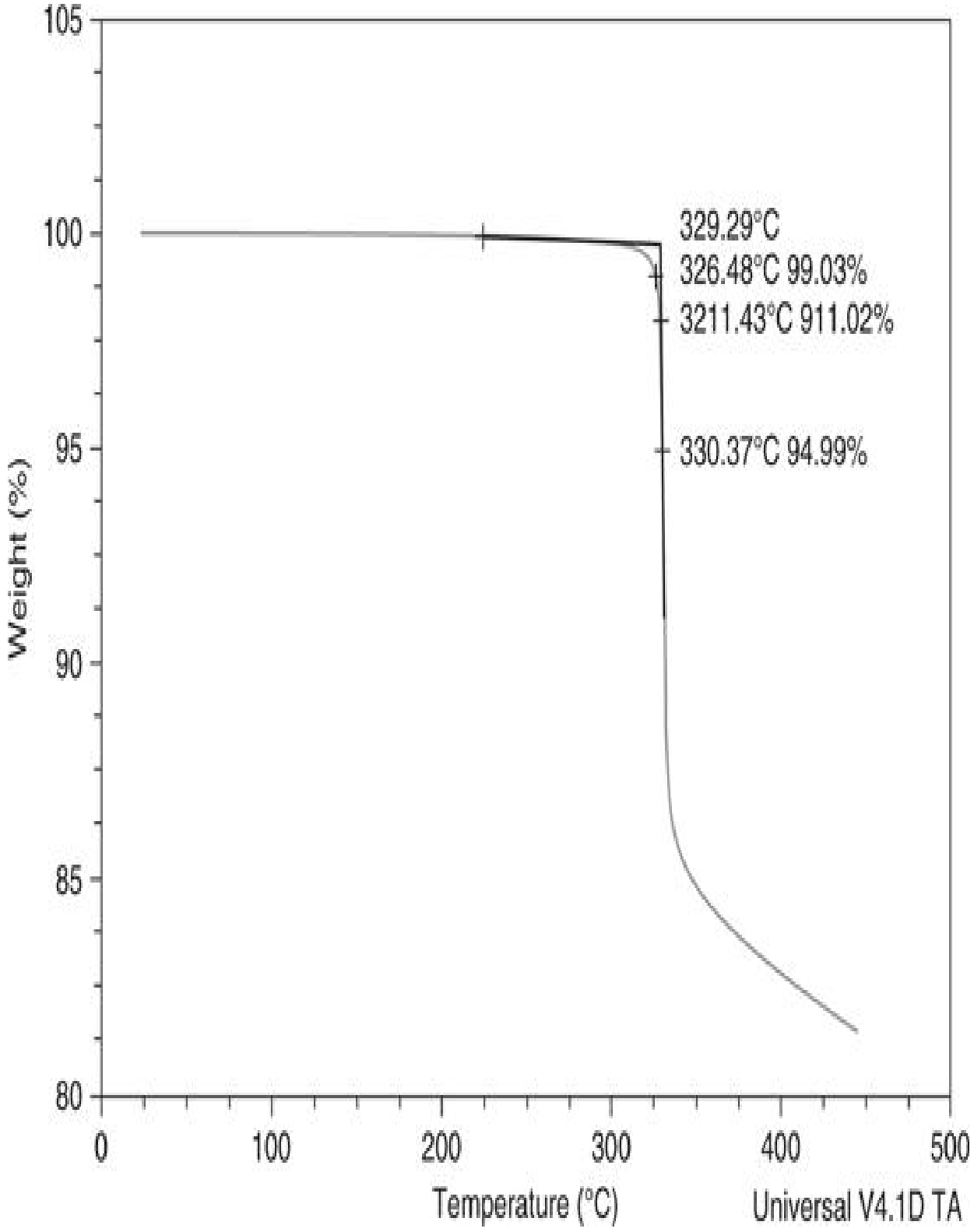


FIGURE 11.6 Decomposition curve for an enhanced high-T_g FR-4.

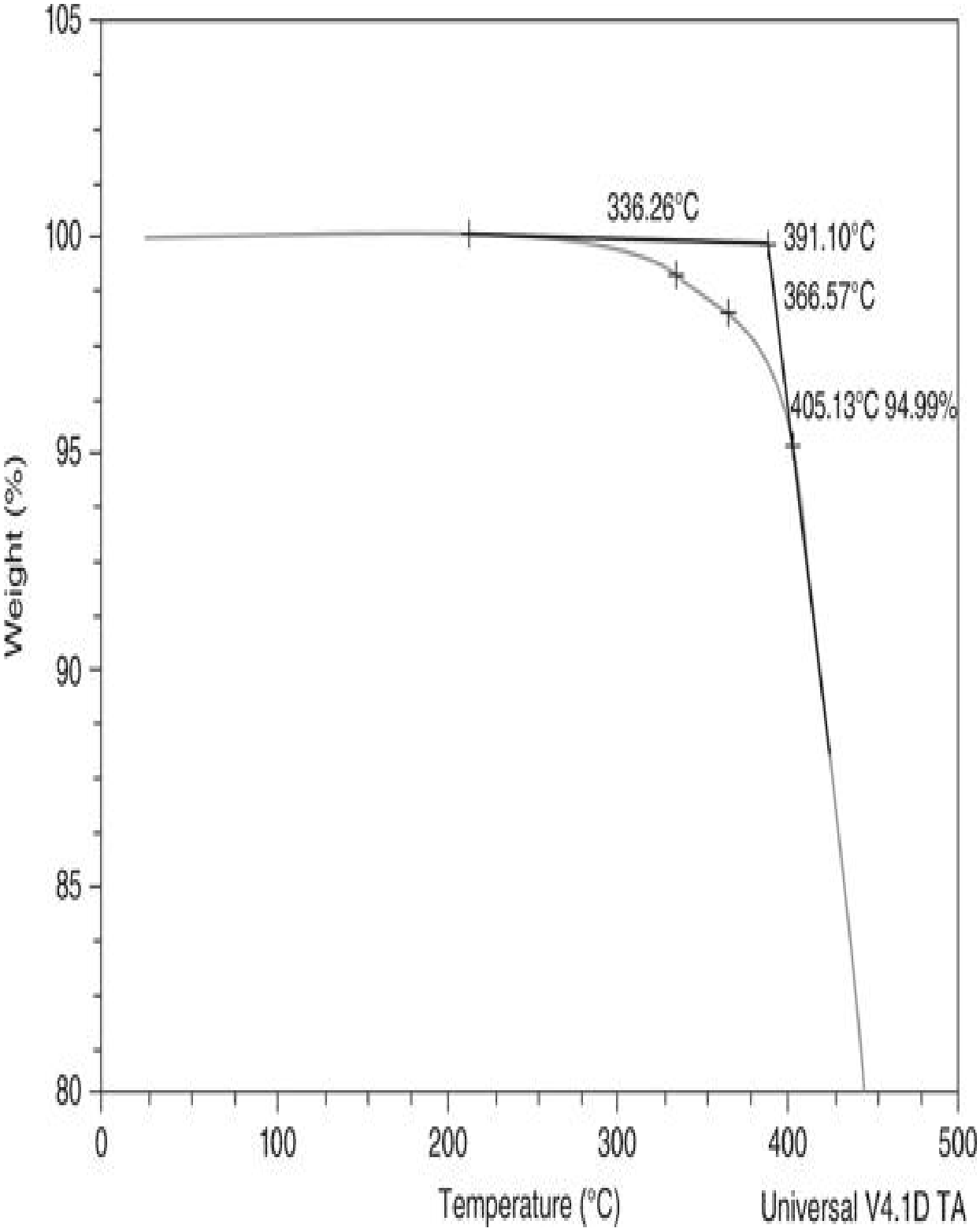


FIGURE 11.7 Decomposition curve for a low Dk/Df material.

These curves show different measurements for decomposition temperature. The value traditionally reported is the level at which 5 percent weight loss occurs, or where the mass is 95 percent of the starting sample mass. But as already discussed, this is a very high level of decomposition when considering PCB reliability. These curves also show 1 percent and 2 percent decomposition temperatures, as well as the “onset” decomposition temperature. The onset temperature extrapolates the linear portions of the curve. The point at which they intersect is reported as the onset temperature.

Note that in Figs. 11.5 and 11.6 decomposition occurs very rapidly, while in Fig. 11.7 decomposition is more gradual, highlighted by the much bigger range between 1, 2, and 5 percent decomposition temperatures. With the material in Fig. 11.7, the 5 percent decomposition temperature would be reported as 405°C, even though some decomposition is beginning around 336°C. This highlights the need to understand not just the 5 percent decomposition temperature, but lower levels as well.

Note that certain IPC-4101 specification sheets include values for the decomposition temperature. These values are based on the 5 percent decomposition value, and as just noted, this is a very high level of decomposition when assessing reliability.[2] So caution should be used when determining which specification sheet to use, or in establishing a specification for decomposition temperature. There are many materials that perform very well in lead-free assembly applications that have T_d values below 340°C by the 5 percent definition, which is a common value used. Alternatively, there are also materials that have T_d values well above 340°C that do not perform well in lead-free applications. The decomposition temperature is just one property to consider when selecting a material, and other properties are also important for reliability. Achieving the

right balance of properties for a given application is important.

11.2.5 Time to Delamination

Time to delamination refers to a specific test procedure used to measure how long a material will resist blistering or delamination at a specific temperature. The procedure utilizes a thermomechanical analyzer (TMA) in which a sample is heated to the specified temperature. The most common temperature used is 260°C. This test is commonly called a T260 test. Other temperatures are also used, such as 288°C or 300°C. Table 11.2 compares the performance of various material types. When reviewing this table, it is important to note that there can be large variation between similar materials across the manufacturers of these materials. T260 values can be affected by a number of factors: the specific resins and curing agents used in a given material, differences in CTE values between the components in the sample, the quality of copper bonding treatment, curing of the material during lamination, and in some cases volatile content. For example, note the lower T260 values reported for the 175°C epoxy versus the 140°C epoxy. Although the T260 value is shorter, thermal cycling tests typically show improved reliability with the 175°C T_g material because of the lower levels of thermal expansion that result with the higher-T_g material. The enhanced FR-4 materials, which use a different curing chemistry, generally exhibit better performance in both time-to-delamination tests as well as thermal cycling tests. Figure 11.8 is an example of a TMA scan on a multilayer PCB that evaluates T260 performance. The top curve plots the temperature while the other curve measures sample thickness. Delamination results in a rapid increase in sample thickness and indicates the endpoint for the test. Figure 11.9 is a T288 scan for the

same material. Note that times to delamination on PCBs are generally much shorter than times on either copper clad laminate or unclad laminate.

TABLE 11.2 Time to Delamination and Arc Resistance Data for Common Materials

Material	T_g (°C)	T260	T288	Arc Resistance (seconds)
Standard T_g FR-4	140	30	5	120
Filled mid-T_g FR-4	150	60	10	120
Halogen free, filled mid-T_g FR-4	155	60	10	115
High-T_g FR-4	170	10	2	90
High-T_g/T_d FR-4	175	45	10	125
Filled high-T_g/T_d FR-4	180	60	30	115
Halogen-free high-T_g/T_d FR-4	180	60	60	115
Mid-loss epoxy	200	60	20	120
BT/Epoxy blend	200	30	10	123
BT/Epoxy blend-low Dk glass	200	30	10	123
Low loss epoxy blend	180	60	60	137
Low loss epoxy blend-low Dk glass	180	60	60	137
Very low loss	200	60	60	139
Halogen-free very low loss	200	60	60	139
Ultra low loss	200	60	60	125
Polyimide	260	60	60	130

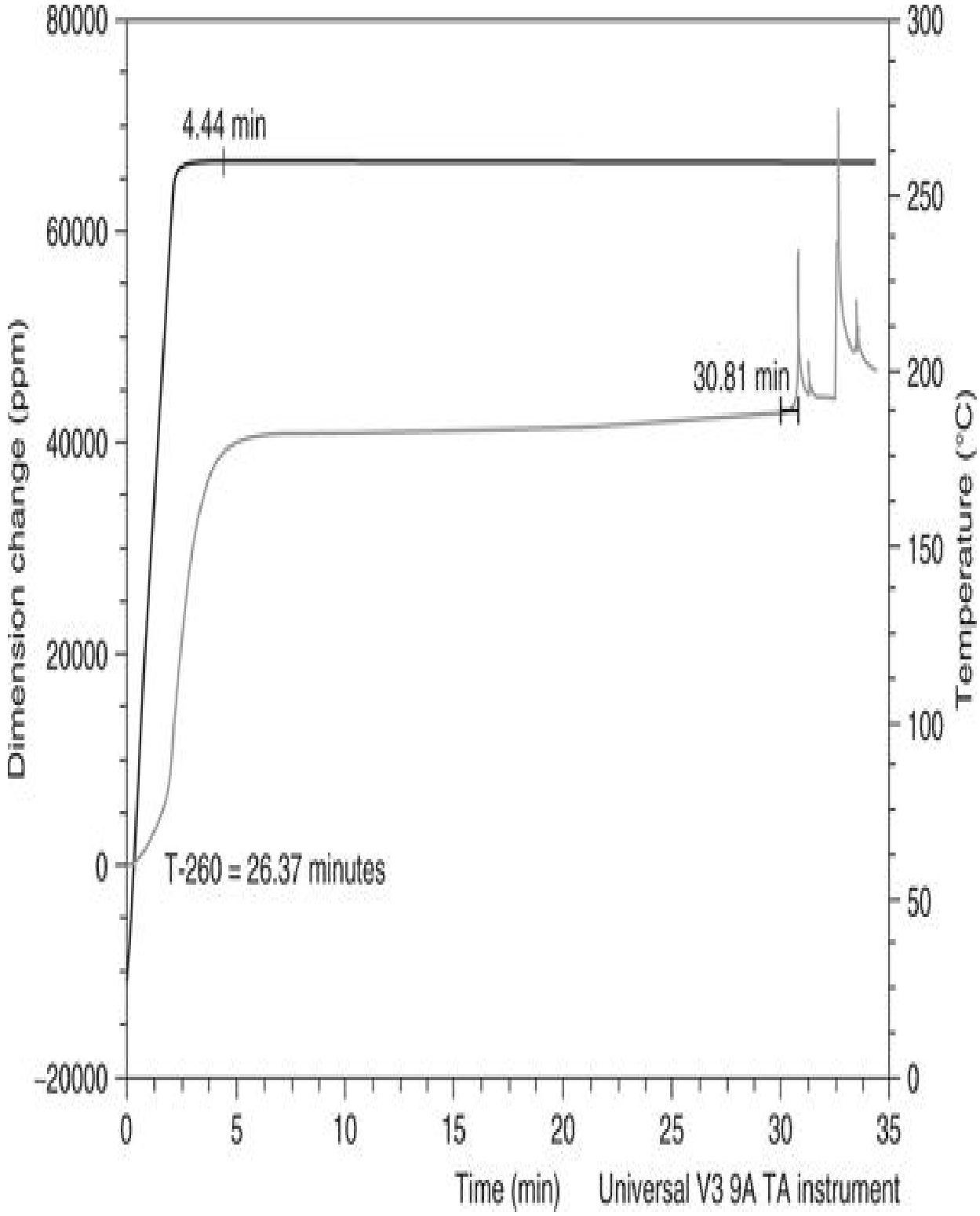


FIGURE 11.8 T260 example for an enhanced high-T_g FR-4.

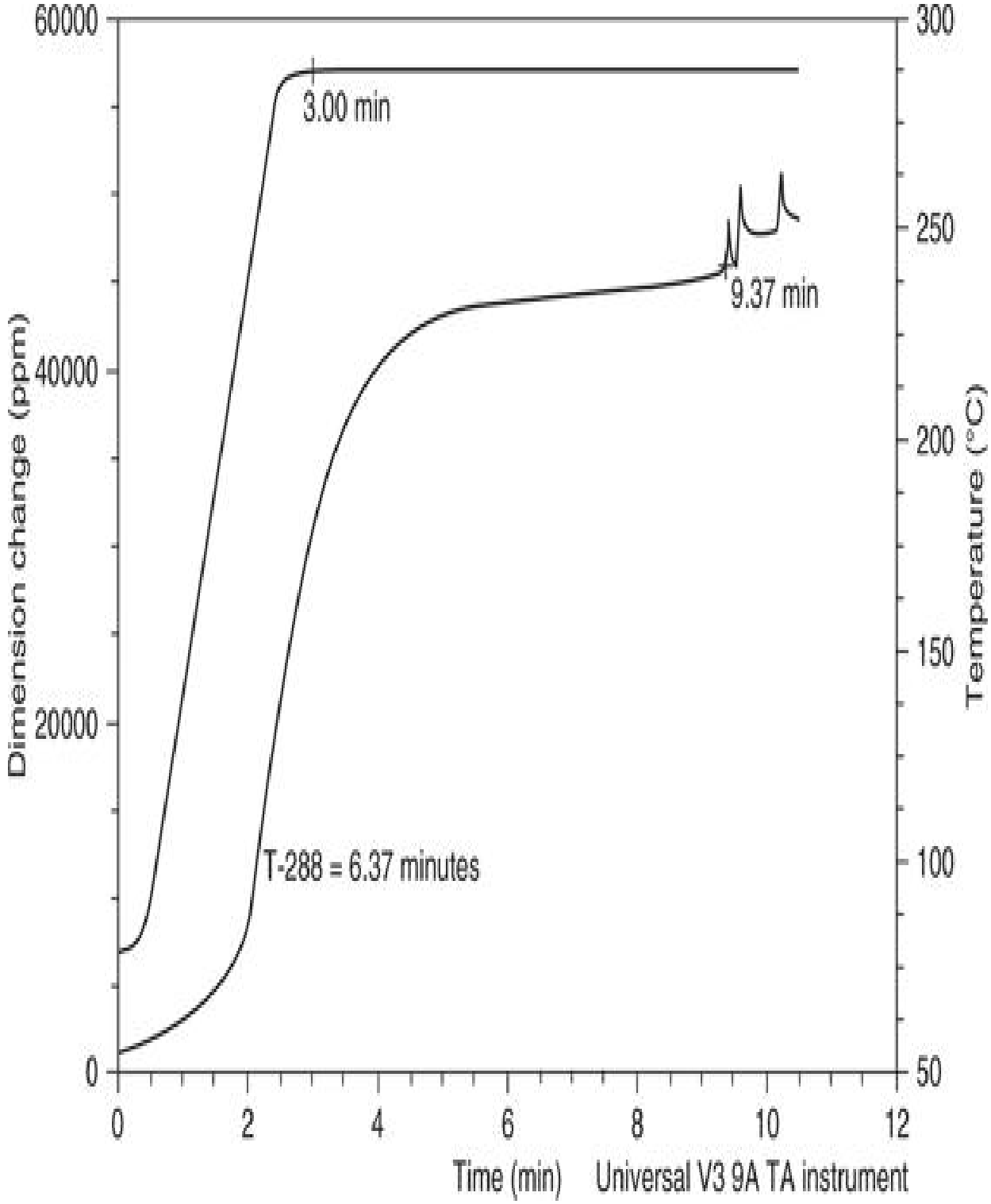


FIGURE 11.9 T288 example for an enhanced high-T_g FR-4.

Although time-to-delamination tests have received much attention as lead-free assembly processes have become common, it is important not to focus exclusively on one property or type of measurement when specifying laminate materials for lead-free applications. First, the correlation between time-to-delamination performance and lead-free assembly compatibility is not always clear. Long T260 or T288 times by themselves do not ensure good reliability in lead-free applications. Conversely, some materials with good but not necessarily great T260 or T288 times have exhibited excellent performance in lead-free applications. So although it is important to consider time-to-delamination performance when specifying materials for lead-free assembly applications, these values should not be looked at exclusively. A balance of several properties is necessary in these applications.

11.2.6 Arc Resistance

In this test technique, a low current arc is placed above the surface of a material. Arc resistance describes the time the material resists tracking, or forming a conductive path, under this condition. Arc resistance values are also shown in Table 11.2. Figure 11.10 illustrates the test technique.

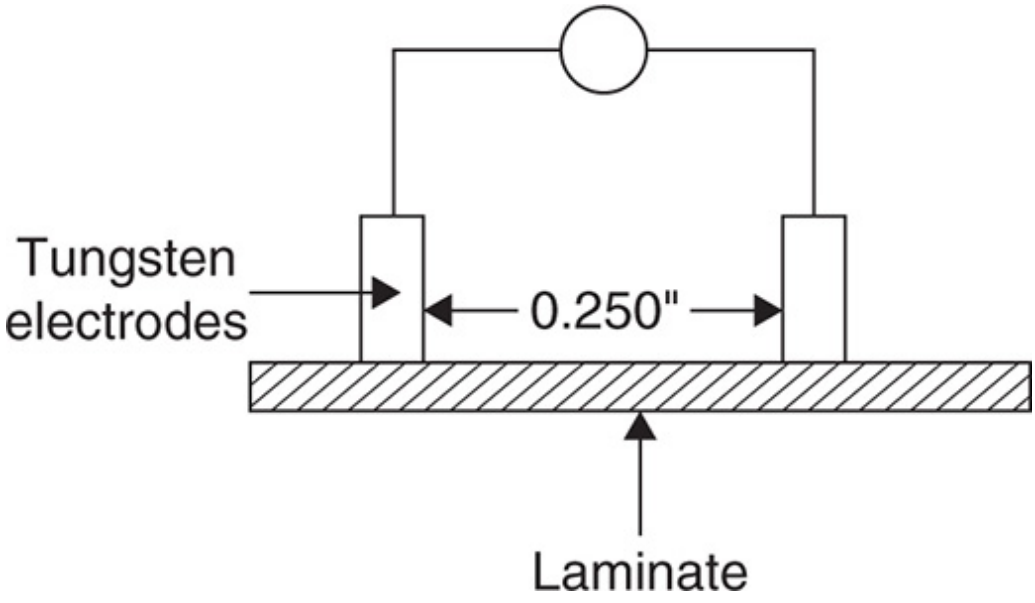


FIGURE 11.10 Arc resistance test technique.

11.2.7 Copper Peel Strength

Peel strength testing is the most popular method used to measure the bond between the conductor and the substrate. Peel strengths can be measured in the “as received” condition, after thermal stress, at elevated temperature, and after exposure to processing chemicals. The standard procedure requires that the sample consist of traces or strips of copper foil, or other metal to be tested, and that they be imaged onto the sample using standard printed circuit manufacturing processes. The strips should be at least 0.79 mm (0.032 in) in width for testing after exposure to processing chemistries and 3.18 mm (0.125 in) in width for the other tests. Metal cladding thickness can influence the measured peel strength and therefore it is accepted practice to use 1 oz cladding, and if a thinner cladding is used, it may be plated up to 1 oz thickness.

One end of the strip is peeled back and attached to a load tester such as a tensile strength tester equipped with a load cell. The peel strength is calculated per the formula:

$$\text{lb/in} = L_m/W_s$$

where L_m is the minimum load, and W_s is the measured width of the peel strip.

For testing after thermal stress, the sample is first floated on solder at 288°C for 10 seconds. For testing after exposure to processing chemistries, the sample is exposed to a series of conditions. First the sample is exposed to an organic stripper at 23°C for 75 seconds. Historically, methylene chloride has been used, but due to environmental concerns, equivalents are now allowed. After drying, the sample is then immersed in a solution of 10 g/L sodium hydroxide at 90°C for 5 minutes. The sample is rinsed and then exposed to 10 g/L sulfuric acid and 30 g/L boric acid at 60°C for 30 minutes. The sample is again rinsed and dried and then immersed in a hot oil bath maintained at 220°C for 40 seconds. Finally, the sample is immersed in a degreaser at 23°C for 75 seconds to remove the oil and then dried. Testing at an elevated temperature may be performed by placing the sample in a hot fluid or in hot air while performing the peel strength measurements. For FR-4 materials, 125°C is commonly used.

Table 11.3 shows 1 oz copper peel strength values in N/mm at various conditions for several common materials. It should be noted that the type of copper treatment and profile bonded to the laminate can have a big influence on copper peel strength values, and therefore the values in this table should only be used as a reference as they are taken from data sheets without reference to copper profile or treatment type.

TABLE 11.3 Peel Strength Values for Common Base Material Types with Standard Copper (N/mm)

Material	T_g (°C)	Low and Very Low Profile Copper	After Thermal Stress	At Elevated Temp.	After Exposure to Chemistry
Standard T_g FR-4	140	1.10	1.45	1.25	1.45
Filled mid-T_g FR-4	150	1.00	1.45	1.25	1.45
Halogen-free, filled mid-T_g FR-4	155	1.00	1.25	1.15	1.20
High-T_g FR-4	170	1.10	1.6	1.19	1.60
High-T_g/T_d FR-4	175	1.20	1.58	1.23	1.58
Filled high-T_g/T_d FR-4	180	1.10	1.25	1.15	1.25
Halogen-free high-T_g/T_d FR-4	180	1.00	1.25	1.05	1.25
Mid-loss epoxy	200	1.14	1.23	1.14	1.20
BT/Epoxy blend	200	1.1	1.31	1.39	1.31
BT/Epoxy blend-low Dk glass	200	1.1	1.31	1.39	1.31
Low loss epoxy blend	180	0.96	1.00		0.96
Low loss epoxy blend-low Dk glass	180	0.96	1.00		0.96

Note that peel testing is measuring force required to pull foil off of a material surface. Depending on the elasticity of the material tested, the effective surface area that the copper is being pulled from changes, as elastic materials will deform during the peel testing. An example is polyimide, long used for its thermal reliability characteristics. Polyimide exhibits low peel strength values as it is very hard and not very elastic, so it has a small area of contact to distribute the force. This illustrates that the absolute value of peel strength is not always the best indicator of quality or reliability.

Measuring and monitoring of peel strengths for a given material type for comparison to its normal values can be used as a process control tool, an inspection criteria, or for failure analysis purposes, but in choosing a material, a higher peel strength does not necessarily imply higher reliability in the end-use environment. Many of the advanced materials being developed and introduced into commercial use will exhibit lower peel strengths. Last, if drum-side treated foil, also called reverse-treated foil, is used, the peel strength values will be lower because of the lower surface profile. In fact, copper foils with lower and lower profiles are being developed for use in high frequency/high speed applications since the copper foil roughness will impact signal loss properties. These lower profile foils will generally result in lower peel strength values.

11.2.8 Water and Moisture Absorption

The ability of a material to resist water absorption, either from the air or when immersed in water, is important for printed circuit reliability. Besides the obvious concerns of moisture causing defects when a material is subjected to thermal excursions, absorbed moisture also affects the ability of a material to resist conductive anodic filament (CAF) formation when a bias is applied to the circuit, and can affect dielectric and loss properties as well.

The test method for measuring water absorption for metal-clad base laminates involves immersing a sample in distilled water at 23°C for 24 hours after etching off the metal cladding and drying the sample for 1 hour at 105 to 110°C and cooling in a desiccator. The sample is weighed after drying, immersed in water under the specified conditions, and weighed again. The water absorption is calculated as follows:

Increase in weight, percent = (wet weight − conditioned weight)/conditioned weight × 100

An additional moisture absorption test measures weight gain after 60 minutes at 15 psi.

11.2.9 Flammability

Underwriters Laboratories (UL) classifies flammability properties as 94V-0, 94V-1, or 94V-2. Definitions of these classifications are as follows:

11.2.9.1 94V-0. Specimens must extinguish within 10 seconds after each flame application (see Fig. 11.11) and a total combustion of less than 50 seconds after 10 flame applications. No samples are to drip flaming particles or have glowing combustion lasting beyond 30 seconds after the second flame test.

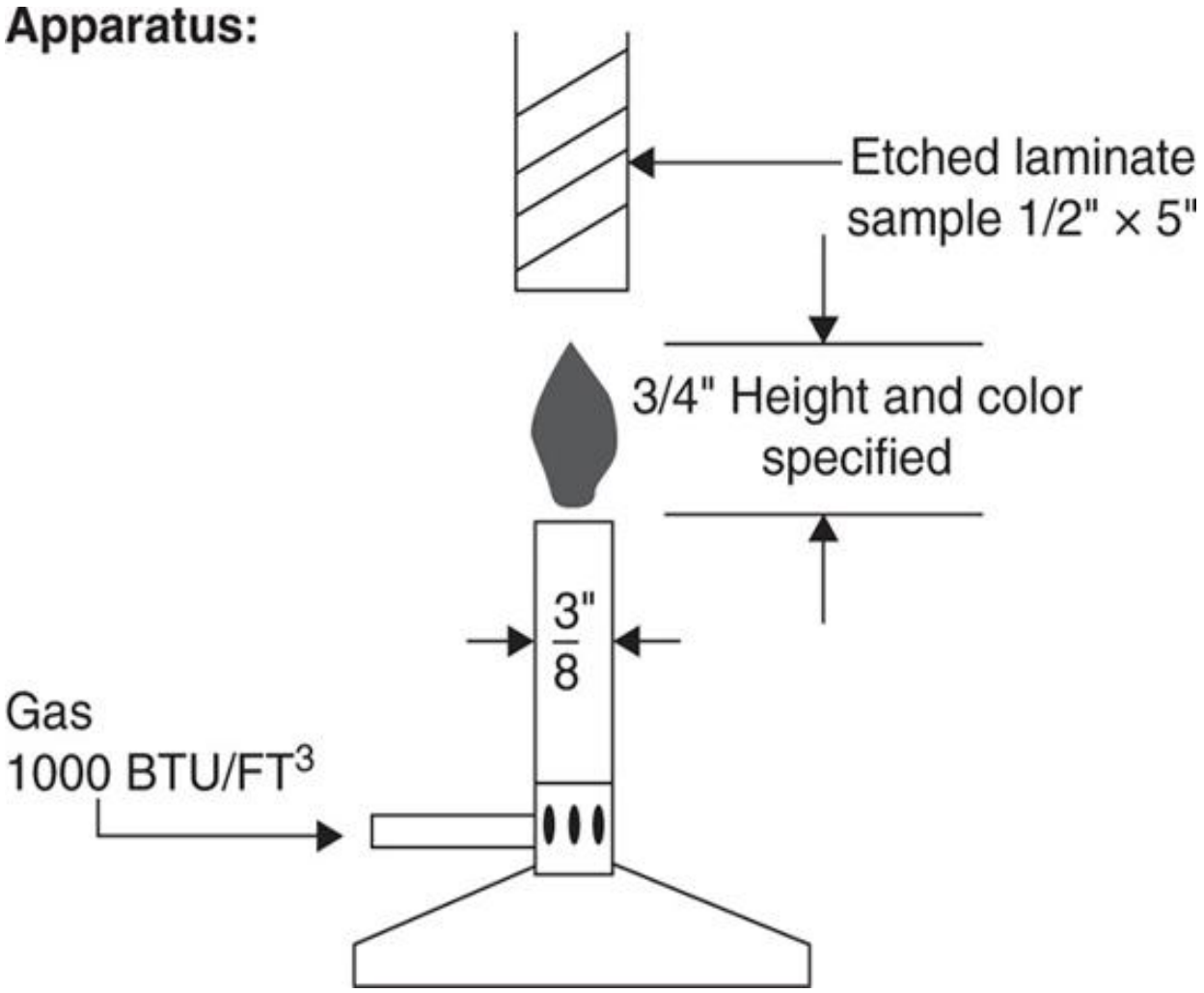


FIGURE 11.11 Flammability testing.

11.2.9.2 94V-1. Specimens must extinguish within 30 seconds after each flame application and a total combustion of less than 250 seconds after 10 flame applications. No samples are to drip flaming particles or have glowing combustion lasting beyond 60 seconds after the second flame test.

11.2.9.3 94V-2. Specimens must extinguish within 30 seconds after each flame application and a total combustion of less than 250 seconds after 10 flame applications. Samples may drip flaming particles, burning briefly, and no

specimen will have glowing combustion beyond 60 seconds after the second flame test.

11.3 ELECTRICAL PROPERTIES

A variety of base material electrical properties are important to understand when designing and manufacturing printed circuits. Some of the most important properties are discussed in this section. As noted earlier in the chapter, the demand for circuits operating at high frequencies requires materials with good permittivity and loss characteristics. These properties will be discussed further in Chap. 14.

11.3.1 Dielectric Constant or Permittivity

The dielectric constant can be defined as the ratio of the capacitance of a capacitor with a given dielectric material to the capacitance of the same capacitor with vacuum as a dielectric, as illustrated in Fig. 11.12. In other words, the dielectric constant is a measure of the ability of a material to store an electric charge. There are actually several test methods used to measure dielectric constant or permittivity and a complete discussion of these methods is beyond the scope of this chapter. However, it should be noted that measuring permittivity at high frequencies can be very difficult and that reported values can vary with the specific test method used. Therefore, when comparing the reported values for different materials, the best comparisons will be those that used the same test method. This will be discussed further in Chap. 14.

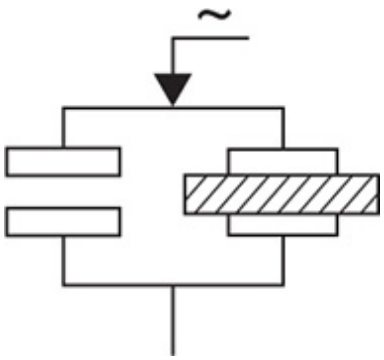


FIGURE 11.12 Dielectric constant.

Furthermore, the dielectric constant is not really a constant. As just implied, the dielectric constant will often vary with frequency and with temperature and humidity exposure. Last, even with the same material type, variations in resin content (resin-to-reinforcement ratio) normally affect the dielectric constant and the variation in glass content of woven materials leads to micro Dk variation. These variations will be further discussed in Chap. 14. Table 11.4 shows dielectric constants for some common fiberglass (E-glass) reinforced materials at 50 percent resin content.

TABLE 11.4 Dielectric Constants and Dissipation Factors of Common Materials

Material	Dielectric Constant					Dissipation Factor				
	1 MHz	1 GHz	2 GHz	5 GHz	10 GHz	1 MHz	1 GHz	2 GHz	5 GHz	10 GHz
Standard T_g FR-4	4.60	4.40	4.35			0.015	0.016	0.017		
Filled mid-T_g FR-4	4.25	3.95	3.90			0.020	0.022	0.023		
Halogen-free, filled mid-T_g FR-4	4.10	4.01	4.00	3.97	3.97	0.013	0.016	0.0167	0.0172	0.0172
High-T_g FR-4	4.10	3.95	3.93	3.92	3.92	0.013	0.0161	0.0167	0.0172	0.0172
High-T_g/T_d FR-4	4.20	4.15	4.10	4.00	3.90	0.0195	0.021	0.022	0.024	0.0245
Filled high-T_g/T_d FR-4	4.24	4.17	4.04	3.92	3.92	0.0180	0.0195	0.021	0.0225	0.0235
Halogen-free high-T_g/T_d FR-4	4.23	4.18	4.16	4.14	4.14	0.0120	0.0148	0.0154	0.0160	0.0165
Mid-loss epoxy	3.75	3.71	3.70	3.70	3.70	0.0107	0.0120	0.0125	0.0127	0.0130
BT/Epoxy blend		3.7	3.7	3.6	3.6		0.0090	0.0095	0.0100	0.0105
BT/Epoxy blend-low Dk glass		3.4	3.3	3.2	3.2		0.0080	0.0085	0.0090	0.0095
Low loss epoxy blend	3.70	3.65	3.64	3.63	3.63	0.0050	0.0058	0.0060	0.0067	0.0071
Low loss epoxy blend-low Dk glass			3.30	3.28	3.27			0.0064	0.0066	0.0064
Very low loss			3.45	3.45	3.45			0.0031	0.0031	0.0031
Halogen-free very low loss			3.44	3.44	3.44			0.0039	0.0039	0.0039
Ultra low loss			3.04	3.02	3.02			0.0021	0.0021	0.0021
Polyimide	4.3	4.0	3.76	3.74	3.74	0.0180	0.0180	0.0170	0.0190	0.0210

11.3.2 Dissipation Factor or Loss Tangent (Tan δ)

The dissipation factor in an insulating material is the ratio of the total power loss in the material to the product of the voltage and current in a capacitor in which the material is a dielectric (see Fig. 11.13). Many of the test methods used for measuring dielectric constant also measure the dissipation factor. Dissipation factor also varies with frequency, resin content, temperature, and humidity. Dissipation factor is discussed in more detail in Chap. 14. Table 11.4 also lists the dissipation factors of some common fiberglass (E-glass) reinforced materials. However, great care should be used when comparing values from material data sheets. Not all suppliers use the same measurement methods or sample resin contents. This can result in significant variation in reported values.

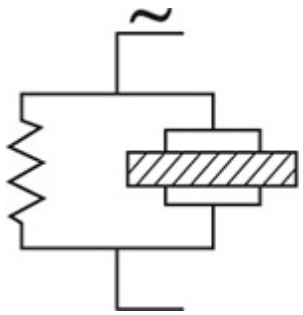


FIGURE 11.13 Dissipation factor.

11.3.3 Insulation Resistance

The insulation resistance between two conductors or plated holes is the ratio of the voltage to the total current between the conductors. Two measures of electrical resistance are volume and surface resistivities. Since these properties can vary with temperature and humidity, testing is normally performed at two standardized environmental conditions,

one involving humidity conditioning, the other involving elevated temperature. Humidity conditioning subjects the sample to 90 percent relative humidity and 35°C for 96 hours (96/35/90). The elevated temperature conditioning normally subjects the sample to 125°C for 24 hours (24/125).

11.3.4 Volume Resistivity

Volume resistivity is the ratio of the DC potential applied to electrodes embedded in a material to the current applied between the electrodes, typically expressed in megohm-centimeters. The measured current flows between electrodes 1 and 3, while stray current applied between the electrodes flows between electrodes 2 and 3, as shown in Fig. 11.14. Table 11.5 shows the volume resistivity values of some common fiberglass-reinforced material types.

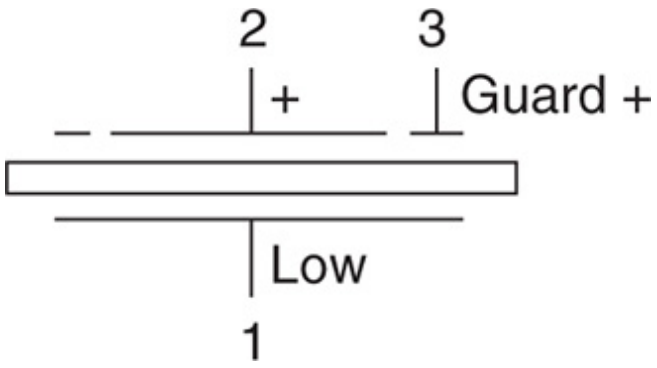


FIGURE 11.14 Circuit for volume resistance.

TABLE 11.5 Additional Electrical Properties of Common Base Materials

Material	Volume Resistivity (96/35/90)	Volume Resistivity (24/125)	Surface Resistivity (96/35/90)	Surface Resistivity (24/125)	Electric Str. (V/mil)
FR-4 Epoxy	10^8	10^7	10^7	10^7	1250
Filled FR-4 Epoxy	10^{10}	10^{11}	10^8	10^9	1250
High-T_g FR-4 Epoxy	10^8	10^7	10^7	10^7	1300
BT/Epoxy Blend	10^7	10^7	10^6	10^7	1200
Low Dk Epoxy Blend	10^8	10^7	10^7	10^7	1200
Cyanate Ester	10^7	10^7	10^7	10^7	1650
Polyimide	10^7	10^7	10^7	10^7	1350

11.3.5 Surface Resistivity

The surface insulation resistance between two points on the surface on any insulating material is the ratio of the DC potential applied between the two points to the total current between them. For surface resistivity, the measured current flows between electrodes 1 and 2, while stray current flows between electrodes 1 and 3, as shown in Fig. 11.15. Table 11.5 shows the surface resistivity values of some common fiberglass-reinforced materials.

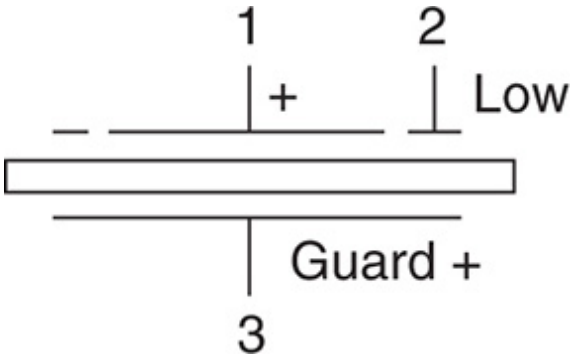


FIGURE 11.15 Circuit for surface resistance.

11.3.6 Electric Strength

Electric strength is a measure of the ability of an insulating material to resist electrical breakdown perpendicular to the plane of the material when subjected to short-term, high voltages at standard AC power frequencies of 50 to 60 Hz and is reported in volts per mil (see Fig. 11.16). Results can be affected by moisture content in the sample, so measurements may vary with different preconditioning environments. Unless otherwise noted, measurements are taken at 23°C, after preconditioning for 48 hours in distilled water at 50°C and immersion in ambient temperature distilled water for 30 minutes minimum, 4 hours maximum. Measurements are performed under an oil medium to prevent flashover on a small specimen. The values may decrease with increasing specimen thickness for an otherwise identical material.

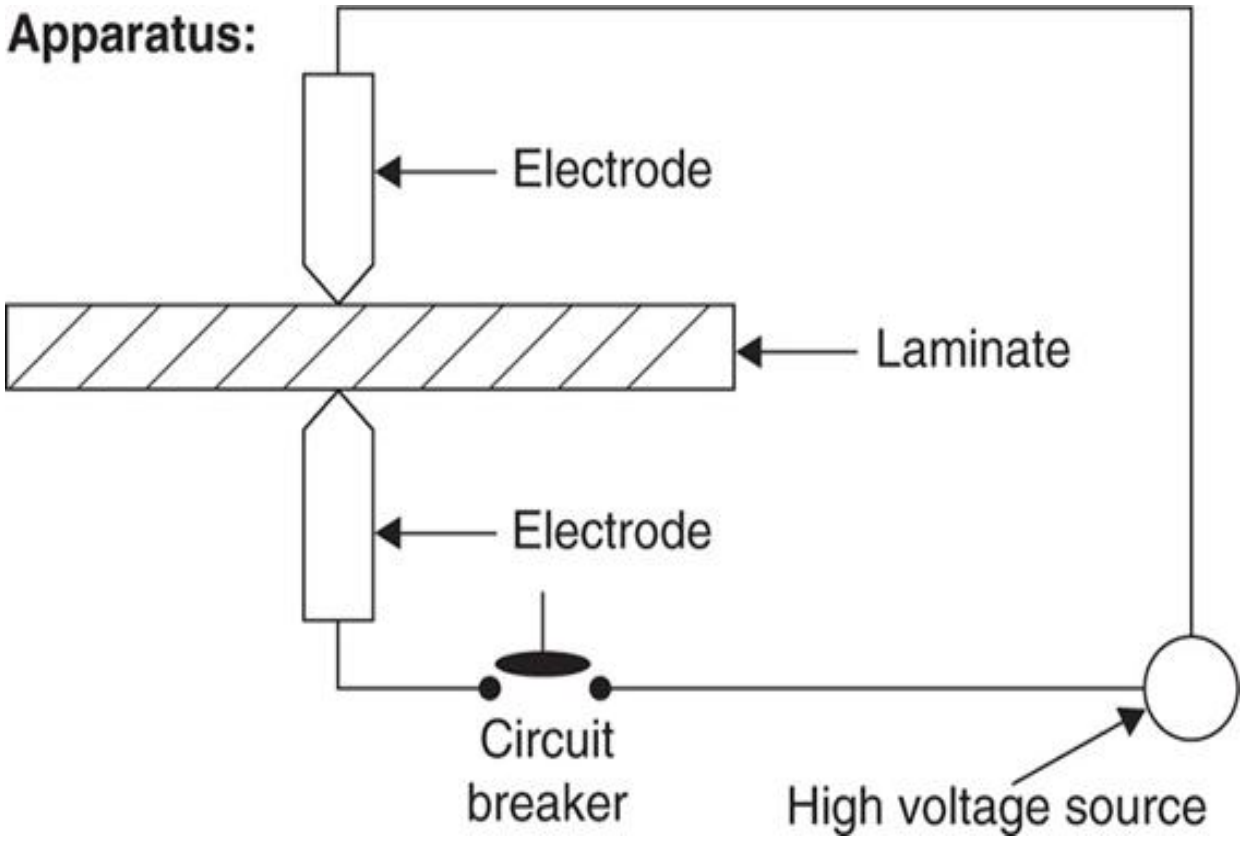


FIGURE 11.16 Dielectric strength.

11.3.7 Dielectric Breakdown

Dielectric breakdown measures the ability of rigid insulating materials to resist breakdown parallel to the laminations (or in the plane of the material) when subjected to extremely high voltages at standard AC power frequencies of 50 to 60 Hz (see Fig. 11.17). As with electric strength, values obtained on most materials are highly dependent on the moisture content and preconditioning method. Unless otherwise noted, measurements are performed at 23°C after preconditioning for 48 hours in distilled water at 50°C followed by immersion in ambient temperature distilled water for 30 minutes minimum, 4 hours maximum. Dielectric breakdown is also performed in an oil medium. Dielectric

breakdown for the materials shown in Table 11.5 is normally above 50 kV.

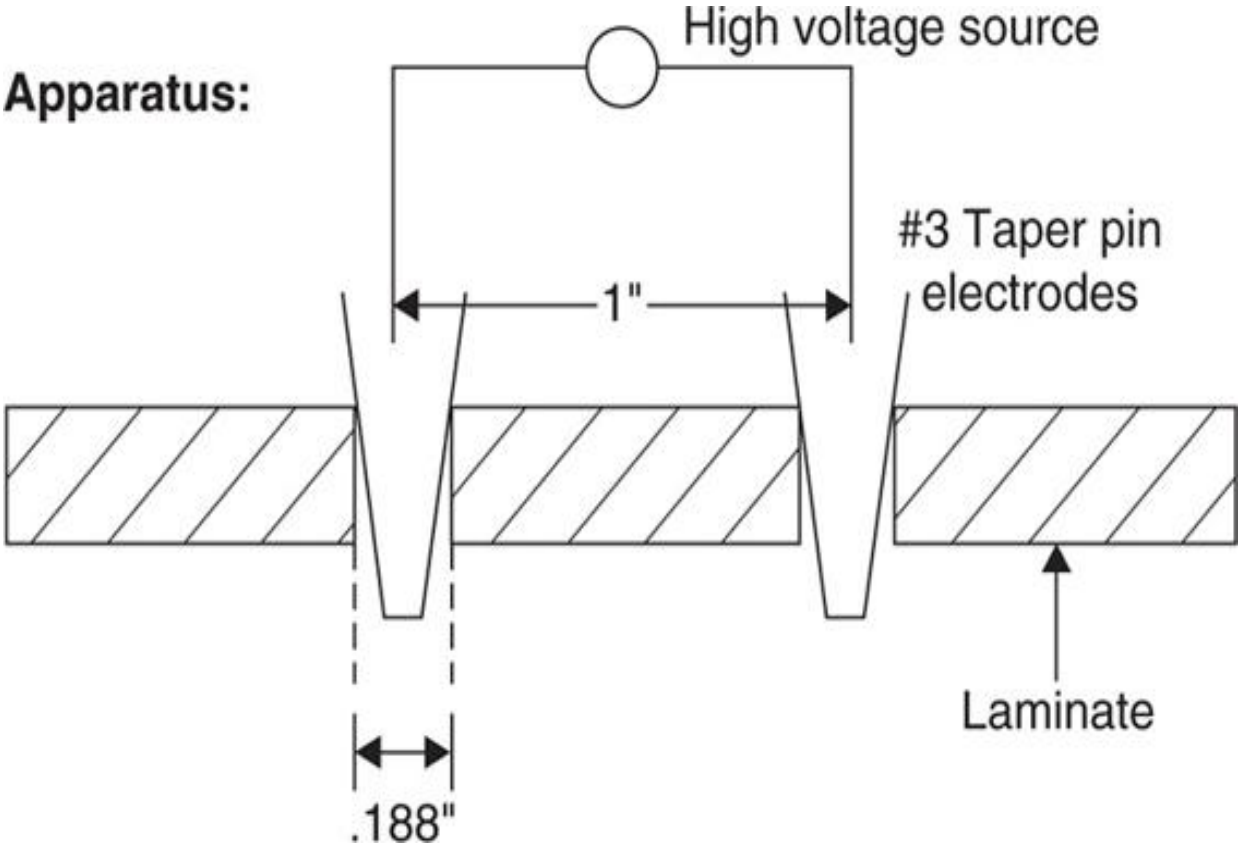


FIGURE 11.17 Dielectric breakdown strength parallel to laminations.

Last, it should be noted that electric strength and dielectric breakdown are measures of instantaneous failure of the dielectric material. These values do not imply long-term resistance to high-voltage values in most uses.

11.4 OTHER TEST METHODS

The test methods described in this chapter are just some of the relevant test methods contained in the IPC Test Methods Manual, IPC TM-650.[3] TM-650 also covers test methods applicable to the components of base materials, such as

copper foil and glass fabrics, as well as printed circuits. IPC TM-650 is available on-line at www.ipc.org.

11.5 REFERENCES

1. NEMA, “Industrial Laminating Thermosetting Products” Standard, 19911.
2. IPC-4101, “Specification for Base Materials for Rigid and Multilayer Printed Boards.”
3. IPC-TM-650 Test Methods Manual.

CHAPTER 12

BASE MATERIAL PERFORMANCE IN PCBs

Edward Kelley
Douglas Troboug h
Isola Group, Chandler, Arizona

12.1 INTRODUCTION

As the fundamental building block for printed circuits, base materials must meet the needs of the printed circuit board (PCB) manufacturer, the circuit assembler, and the original equipment manufacturer (OEM). A balance of properties must be achieved that satisfies each member of the supply chain. In some cases, the desires of one member of the supply chain conflict with another. For example, the need for improved electrical performance by the OEM, or improved thermal performance by the assembler, may necessitate the use of resin systems that require longer multilayer press cycles, less productive drilling processes, and the use of plasma desmear processes.

Lead-free assembly processes have driven the need for greater thermal reliability. Other trends are also driving the need for greater performance. These include

- Circuit densification
- Higher circuit operating frequencies

The density of IC packaging technologies, such as ball grid array (BGA) and chip scale packages, continues to increase. In turn, this requires greater interconnection density in the printed circuits onto which they are assembled. The need for increased density in the PCB impacts each of the components of the base material as well as the way in which they are manufactured. To achieve high levels of interconnection, component pitch densities result in smaller and more closely spaced plated through holes and circuit features. As the space between these holes and features decreases, the potential for conductive anodic filament (CAF) failures increases substantially.

Higher operating frequencies can also impact each of the three main components of base materials. Circuits operating at high frequencies are driving the use of materials with low dielectric constants, low dissipation factors, and tighter thickness tolerances. These performance issues and the impact to the printed circuit manufacturing process are discussed in this chapter.

12.2 METHODS OF INCREASING CIRCUIT DENSITY

There are basically three ways to increase printed circuit density:

1. Decrease conductor line widths and the spacing between them.
2. Increase the number of circuit layers in the PCB.
3. Reduce via and pad sizes, and via-to-via pitch.

Decreasing conductor line widths requires very-low-profile copper foils for high yields in circuit etching processes. However, other things being equal, lower profiles result in decreased foil adhesion to the dielectric. Balancing the copper surface profile for both adhesion to the dielectric and the ability to etch fine circuit features, not to mention the impact of surface roughness on electrical performance at high frequencies, is an important consideration. Copper foil manufacturers continue to research methods to improve the chemical adhesion between the foil and the various dielectric materials in use, relying less on a rough surface profile for mechanical adhesion, and allowing for very low profiles for circuit etching and lower conductor losses at high frequencies.

Increasing layer counts have resulted in both greater overall multilayer thicknesses and thinner individual dielectrics, making thickness control and thermal reliability more important than ever. Adding layers to a PCB also demands improved registration capabilities. One of the critical variables in controlling registration is the dimensional stability of the laminate material, which can become more challenging with the thinner laminates used as layer counts increase. Reducing via and pad sizes also requires improved laminate dimensional stability for registration of high layer count circuits, and smaller via-to-via distances require much more thermally robust materials.

12.3 COPPER FOIL[1]

One obvious method to increase printed circuit functionality is to put more circuitry per unit area of the circuit. Printed circuit densification has driven several improvements in copper foil technology. One of the first developments was high temperature elongation (HTE) foils. Other advances include low- and very-low-profile foils, thin foils, and foils for high-performance resin systems.

12.3.1 HTE Foil

HTE or class 3 copper foil exhibits improved elongation properties at elevated temperatures as compared to standard electrodeposited or class 1 copper foil. Typical elongation values for HTE copper foil range from 4 to 10 percent at 180°C.

The growth in multilayer printed circuits has resulted in HTE becoming the most commonly used foil, since its excellent ductility at elevated temperatures helps prevent innerlayer copper foil cracking. As a printed circuit experiences a thermal cycle, the base materials will expand. The *z*-axis expansion applies stress to the connection of the innerlayer foil and the plated hole. With HTE foil, the reliability of this connection is improved. This property is particularly important in thicker circuits and high resin content constructions where increased *z*-axis expansion occurs. Virtually all copper used in multilayer PCBs today are HTE.

However, there are many variants of HTE and the terminology can become confusing. For example, virtually all reverse-treated copper foil (RTF) used in multilayer PCBs also meets the requirements for high temperature elongation (HTE). But some people will use the term “HTE” copper to refer to foil on laminate with the drum side of the foil facing out, and “RTF” to refer to the drum side against the

laminate, even though technically both foils meet the HTE requirement.

12.3.2 Low-Profile and Reverse-Treated Copper Foils

Three classifications in IPC specifications describe the profile of the copper foil surface (Table 12.1).

TABLE 12.1 Copper Foil Profiles

Foil Profile Type	Max. Foil Profile (microns)	Max. Foil Profile (μ inches)
S—standard	N/A	N/A
L—low profile	10.2	400
V—very low profile	5.1	200
X—no treatment or roughness	N/A	N/A

Copper foil profile is important for etching of fine-line circuits. Figures 10.38 through 10.41 illustrate the difference between standard- and low-profile foils. As can be seen in those photos, the tooth profile of the standard profile foil is much more pronounced. The etching of the lower profile foil results in more control of the geometry of the circuit trace. In addition, in very thin laminates, the large tooth structure of the standard profile foil can result in inconsistent dielectric thickness, making impedance control more difficult, and can even result in electrical failures if the tooth structures from the opposing sides of the laminate protrude sufficiently.

Reverse-treated foils (RTFs) take this concept a step further. When copper foil is manufactured, there is a very

smooth, shiny side and a rougher matte side. Conventional technology involved treating the matte side and laminating this side to the base material. Reverse-treated foil, as its name implies, involves putting the treatments on the smooth, shiny side of the foil and laminating this side to the base material. This has two important effects. First, the side bonded to the base material has a very low profile that aids in etching very fine circuit traces. Second, the rougher matte side, which is now on the surface of the laminate, can improve photoresist adhesion. This enables the removal of surface roughening processes during PCB manufacturing and can also improve innerlayer imaging and etching yields. Figure 12.1 compares laminates made with conventional and RTF foils.

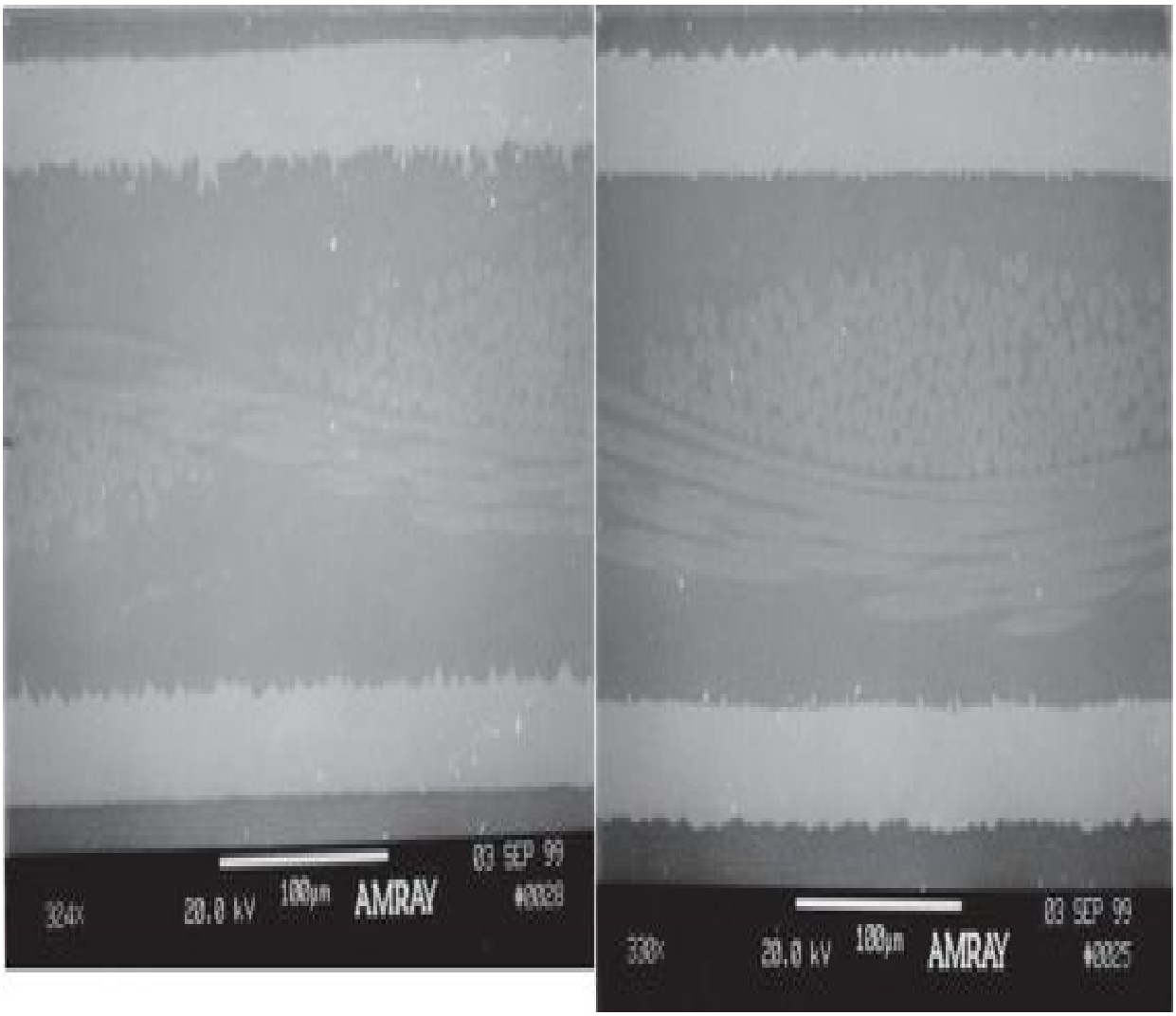


FIGURE 12.1 Comparison of laminates with standard (left) versus RTF (right) copper foils.

12.3.3 Thin Copper Foils

The capability to etch fine-line circuits is also improved through the use of thinner copper foils. Although limited current carrying capacity and higher resistance than thicker foils can limit the use of very thin foils on innerlayer circuits. These thin foils can be used on external layers since the outerlayer process involves plating on top of the foil to the desired overall thickness. HDI products primarily use this type of foil to allow for fine-line circuitry and controlled layer

thickness. 5.0 micron, 9.0 micron and 13.0 micron copper foils are mostly used. Processes to use 3.0 micron copper foil have also been developed.

12.3.4 Foils for High-Performance Resin Systems

Many of the high-performance resin systems such as BT, polyimide, cyanate ester, and even some high-T_g epoxies, especially those with high levels of inorganic filler, exhibit lower peel strengths and resistance to undermining of the copper foil when exposed to aggressive chemistries. For these applications, foils with increased nodularization and coupling agents tailored to the resin system are often used. The increased nodularization results in more surface area for mechanical adhesion whereas the specific coupling agent aids in chemically bonding the foil to the resin system.

12.3.5 Copper Roughness and Attenuation

As circuit operating frequencies increase, more of the signal travels in the outermost part of the conductor. The “skin depth”—that is, the region where much of the signal travels—is shown in Fig. 12.2 as a function of frequency. As shown in this graph, the skin depth approaches the average roughness of 0.5 oz copper foil above 1 GHz. Signal attenuation due to conductor losses related to the roughness of the foil becomes an important factor at these frequencies, and should be considered by the design engineer.

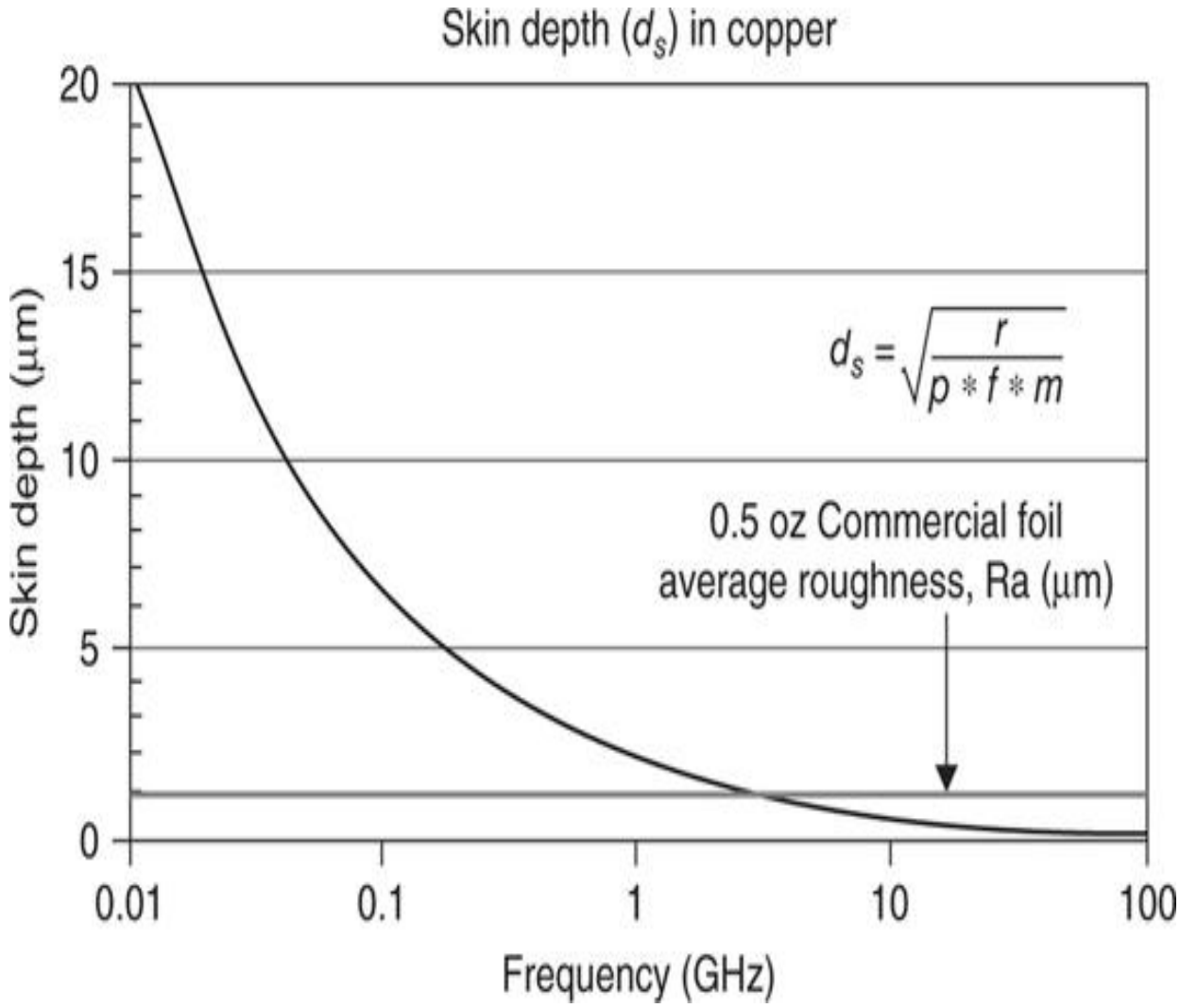


FIGURE 12.2 Skin depth versus frequency.

A study of several different copper foil types correlated roughness and attenuation values.[2] Figures 12.3 and 12.4 show pictures of the foils to highlight their relative roughness differences. Figure 12.5 shows the roughness distributions of these foils. Finally, in Fig. 12.6, the loss values associated with each of these foil types are graphed versus frequency. Up to about 1 GHz, there is very little difference in the observed loss across the several foil types. However, at higher frequencies, the difference becomes much greater, correlating to the roughness of the individual foil types; the

greater the roughness, the greater the measured attenuation.

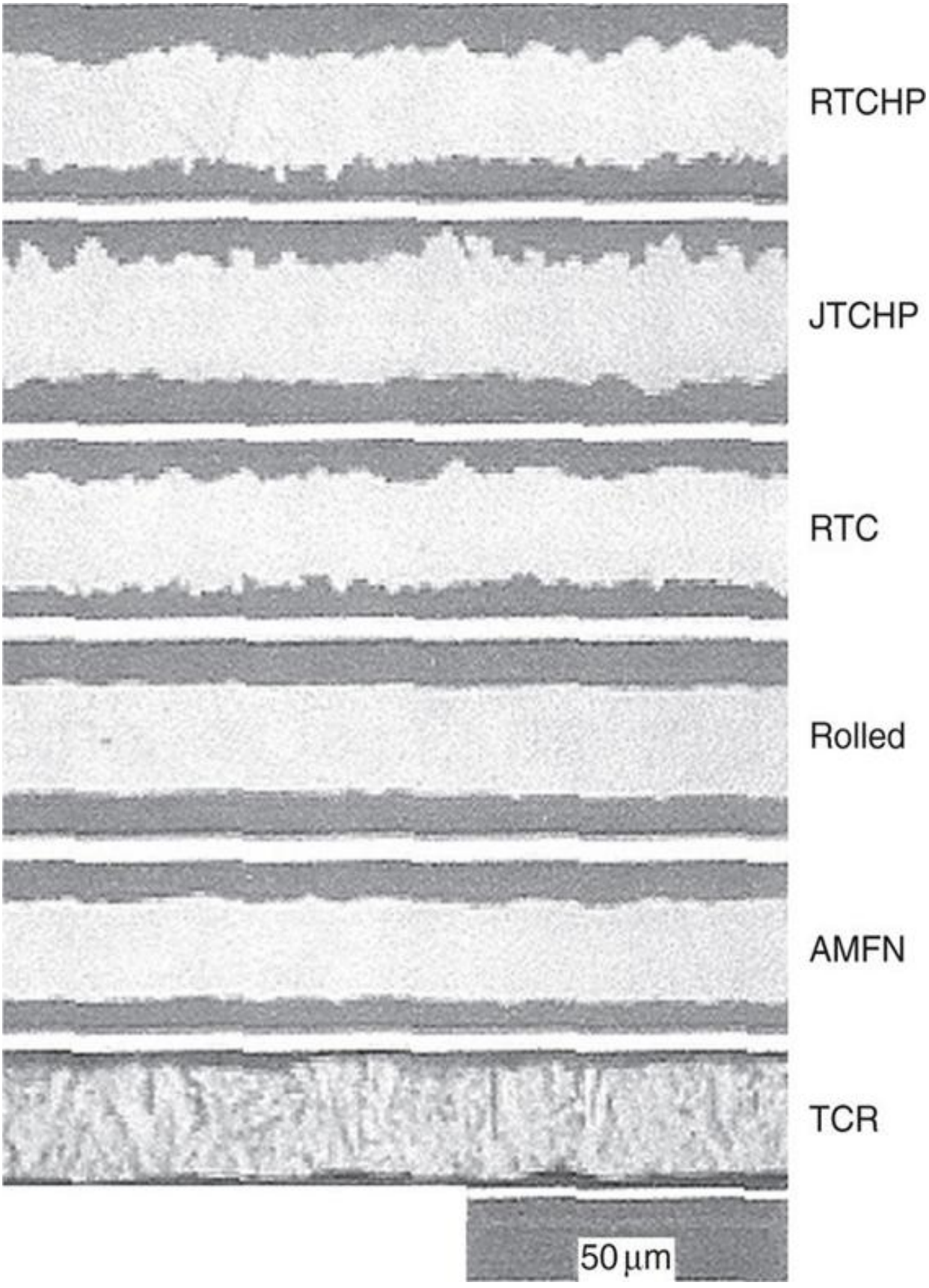

RTCHP
JTCHP
RTC
Rolled
AMFN
TCR
50 µm

FIGURE 12.3 Cross-sectional view of several copper foils.

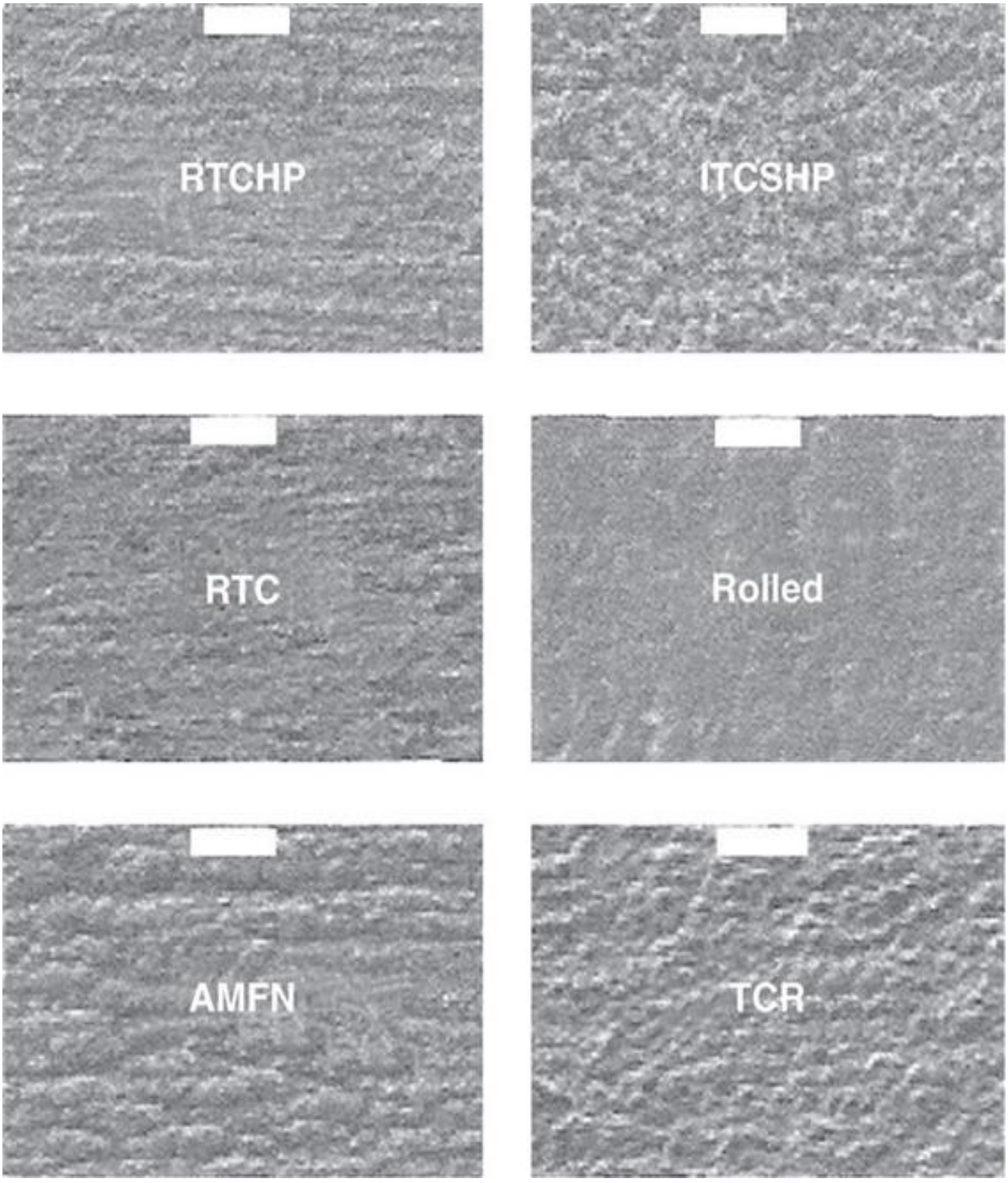


FIGURE 12.4 SEM views of several copper foils.

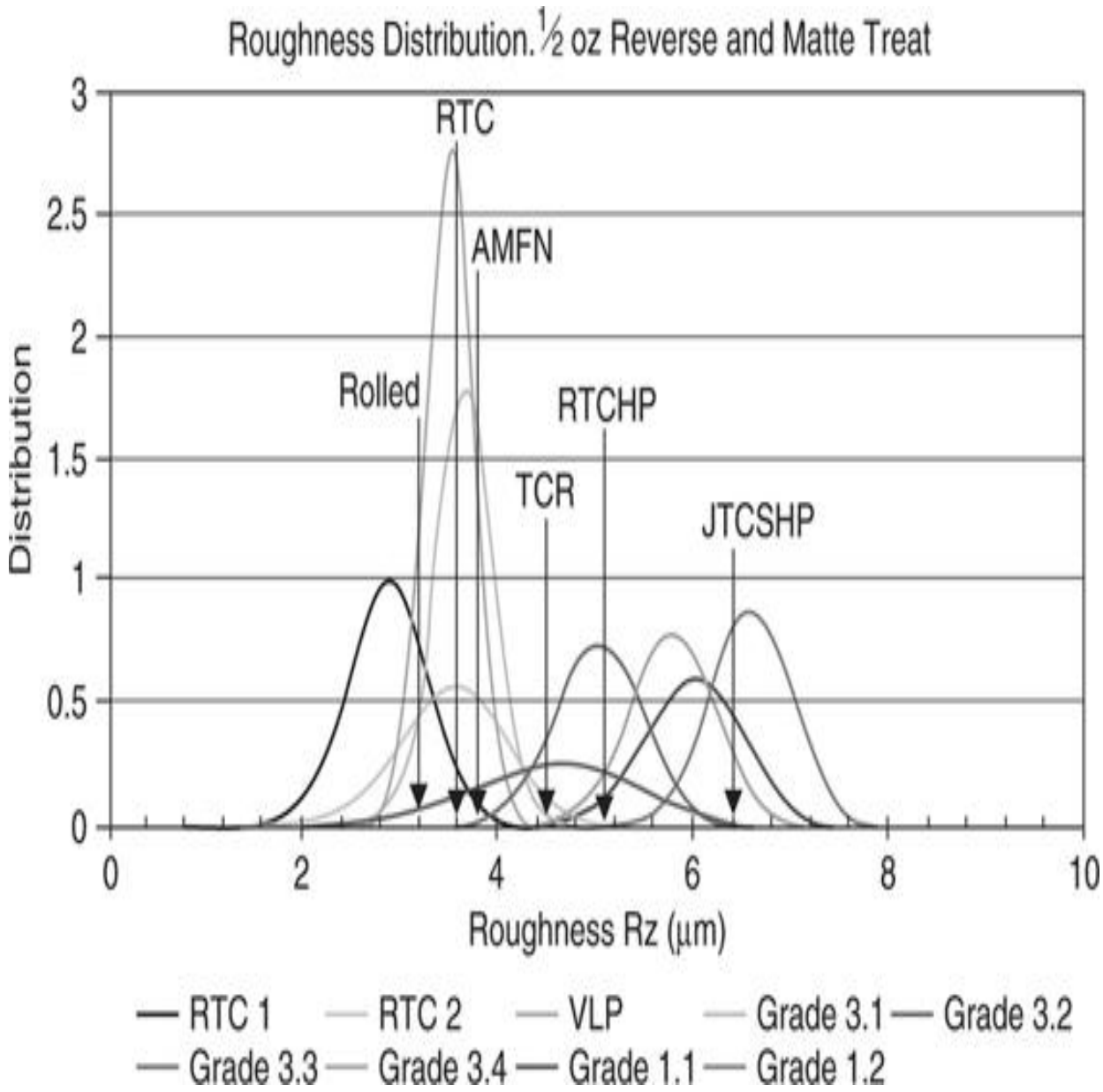


FIGURE 12.5 Roughness distributions for several foil types.

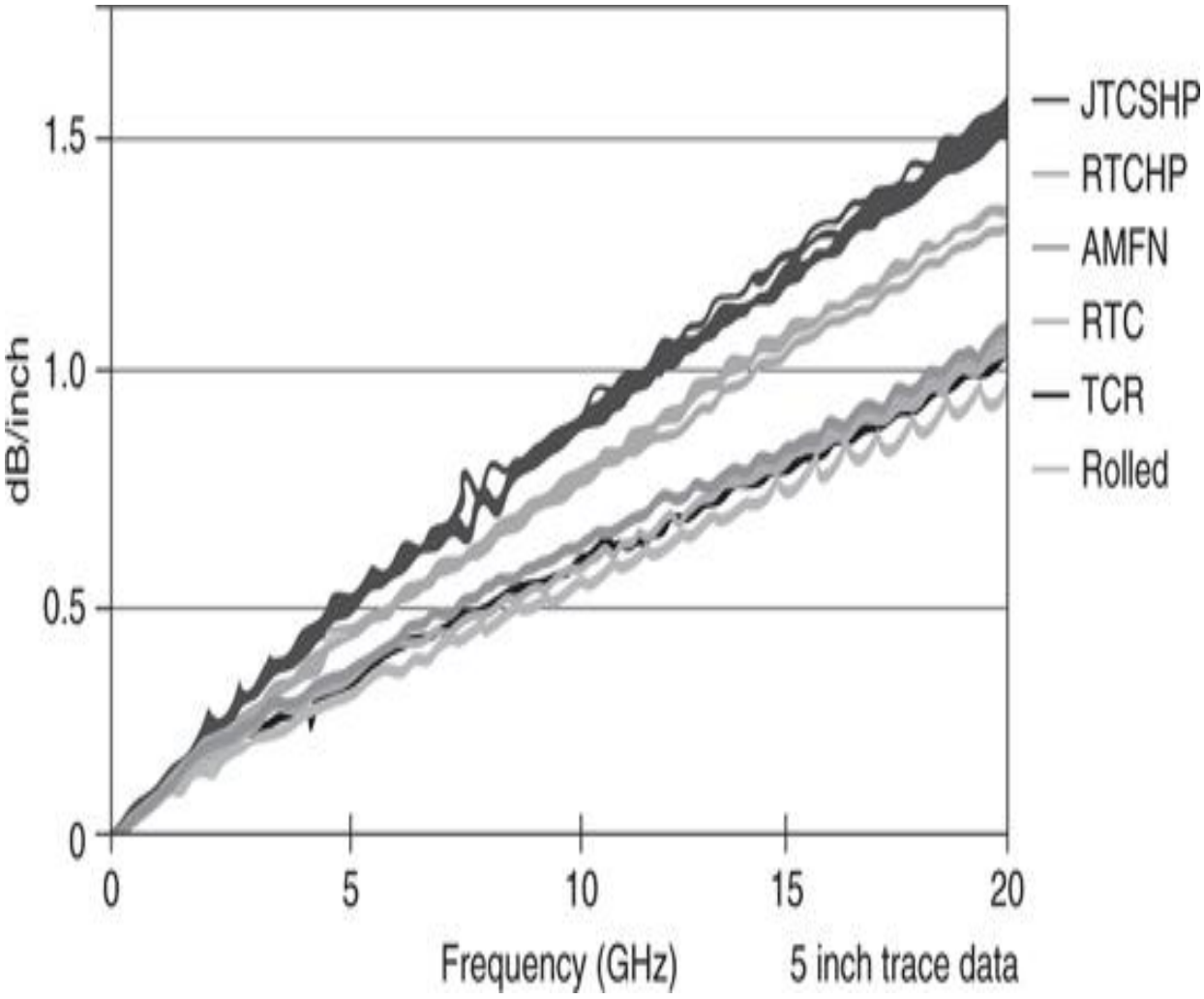


FIGURE 12.6 Loss versus frequency for several foil types.

Due to the marked improvement in performance with smoother copper surfaces, there have been significant enhancements made to copper roughness in recent years. There are no industry-standard roughness specifications for this class of copper foils currently, so they are generally marketed under trade names. However, the relevant IPC committee is working on this and the latest foil specification should be consulted. These foils are more expensive than the conventional RTF or VLP foils, so performance data for the foil should be investigated prior to use. The use of these foils becomes very beneficial at frequencies above 10 GHz.

The roughness that results from the oxide/oxide alternative surface preparation process during printed circuit manufacturing is also very important. Figures 12.7 and 12.8 compare the roughness obtained from two of these processes. The base copper foil and FR-4 resin system used were held constant. The test vehicles from which these cross sections were taken were also measured for attenuation. This measurement technique was used to calculate an effective dissipation factor, D_f, for these material sets. The measured D_f for the sample in Fig. 12.7, with the relatively smooth profile, was 0.021 at 1 GHz. The measured D_f for the sample in Fig. 12.8, with the rougher profile, was 0.026. Obviously, the rougher profile created by the oxide alternative process in Fig. 12.8 resulted in a significantly higher loss value.

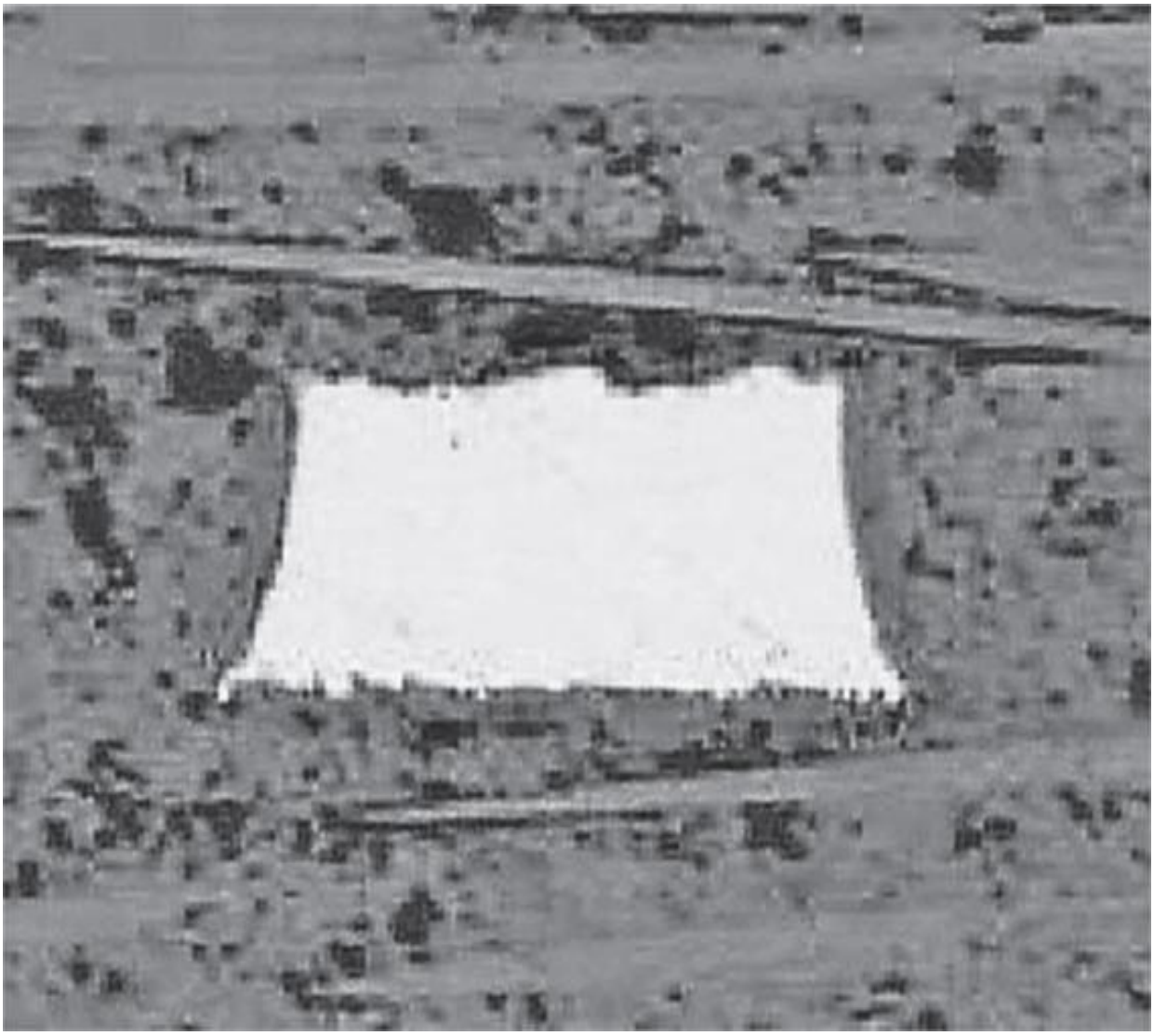


FIGURE 12.7 Copper profile obtained from process A.

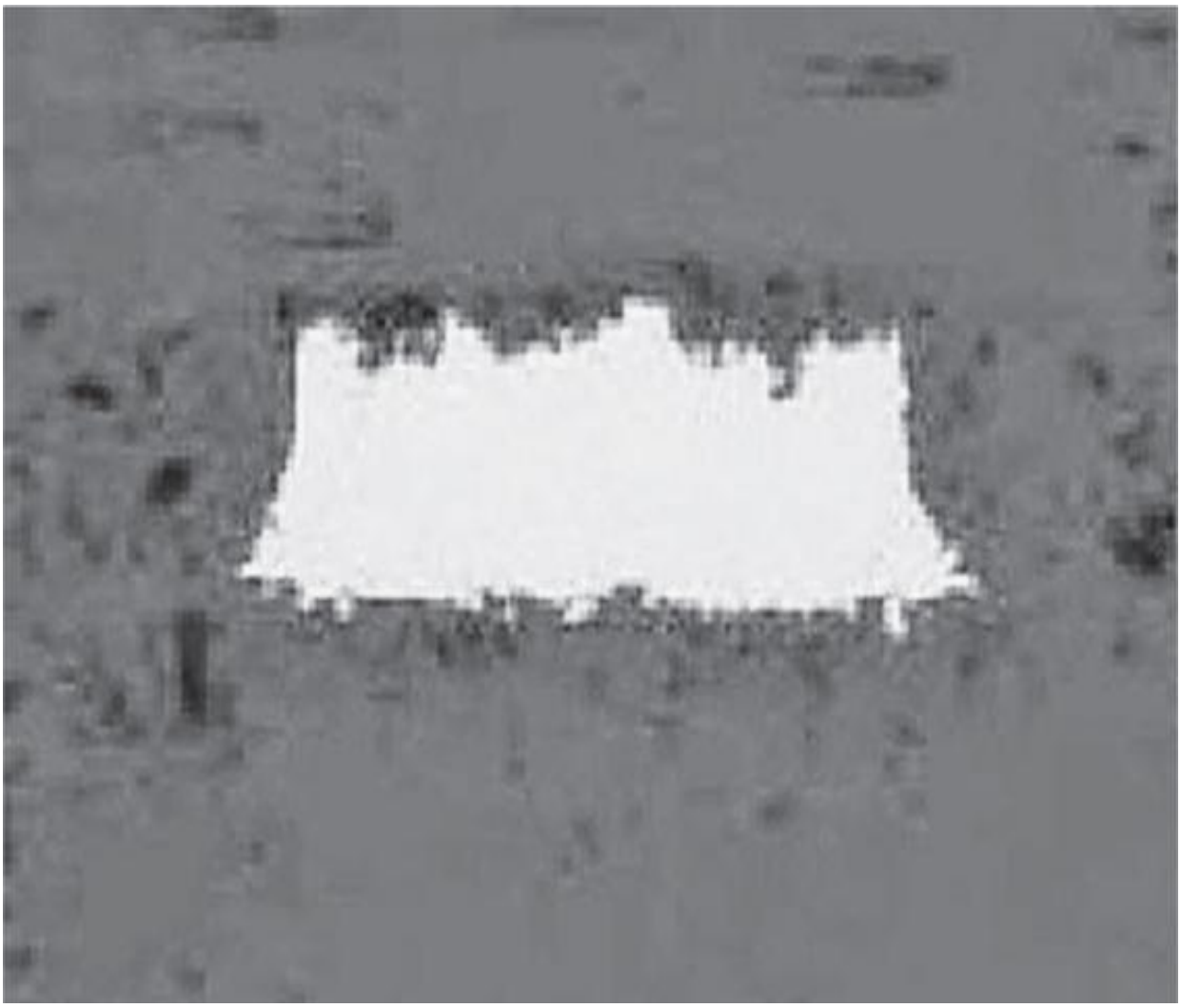


FIGURE 12.8 Copper profile obtained from process B.

12.4 LAMINATE CONSTRUCTIONS[3]

To satisfy requirements for impedance, layer count, and overall PCB thickness, a broad range of laminate dielectric thicknesses are needed. Table 12.2 shows many common laminate dielectric thicknesses, along with typical constructions and resin contents, though there are many more possibilities. Individual laminate suppliers may have preferred constructions, so not every construction shown in

this section will be available from every laminate supplier. In addition, some of the high-performance resin systems will have slightly different constructions or resin contents in order to target certain performance characteristics, such as dielectric constant.

TABLE 12.2 Common Laminate Constructions[4]

Laminate Thickness (in.)	Fiberglass Cloth(s)	Approx. Resin, %
0.0020	1-106	71–72
0.0025	1-1080	53–54
0.0025	1-1067	69–70
0.0030	1-2113	46–47
0.0035	1-1086	64–65
0.0035	1-2113	52–53
0.0040	1-2113	53–54
0.0040	1-3313	54–55
0.0040	1-106/1-1080	59–60
0.0040	2-106	68–69
0.0045	1-2116	50–51
0.0045	2-1080	55–56
0.0050	1-2116	52–53
0.0050	1-1652	42–43
0.0050	2-1080	56–57
0.0050	2-1067	69–70
0.0060	2-2113	46–47
0.0062	1-1080/1-2313	53–54
0.0080	1-7628	44–45
0.0080	1-2116/1-2313	49–50
0.0080	2-2116	45–46
0.0090	2-2116	50–51
0.0100	2-1652	42–43
0.0100	2-2116	52–53
0.0120	2-1080/1-7628	47–48
0.0140	2-7628	40–41
0.0210	3-7628	40–41

Also note that resin contents are based on weight. So care should be exercised when comparing different resin systems since the density can vary. A resin with a relatively high density will need a higher resin content by weight in order to achieve the same dielectric thickness.

12.4.1 Single-Ply versus Multiple-Ply Constructions

For many years multiple-ply constructions were the industry standard. Long ago, multiply constructions were found to be more reliable than single ply, mostly due to manufacturing quality of the time. Over the past 20 years, as quality levels greatly increased, single-ply constructions have replaced multiple-ply constructions as the standard on thicknesses up to 0.0050 in, though OEMs may still want two-ply constructions for some applications when possible. For thicknesses of 0.0050 to 0.0080 in, the use of single-ply versus multiple-ply varies with application. Above 0.0080 in, multiple-ply constructions are always used.

Within each range, there are often multiple cloth and resin content combinations that can achieve the desired dielectric thickness. The choice of laminate construction can significantly impact both cost and performance.

A single-ply construction will typically represent a cost savings compared to a multiple-ply construction, as well as generally having improved dielectric thickness control. Few applications actually require multi-ply constructions. These are mostly demanded by military/aerospace designers, and for dielectric layers between high voltage differential plane layers, or high power plane layers.

12.4.2 Resin Contents

As Table 12.2 illustrates, the same dielectric thickness can be achieved with multiple fiberglass cloth and resin content combinations. Constructions with relatively lower resin contents are often preferred since they result in less *z*-axis expansion and can therefore improve reliability in many applications. In addition, lower resin contents can also improve dimensional stability, resistance to warpage, and dielectric thickness control. On the other hand, constructions with higher resin contents result in lower dielectric constant values, which are sometimes preferred for electrical performance, which is discussed further in Sec. 12.8. In addition, a certain minimum resin content is required to ensure adequate resin-to-glass wet-out and to prevent voids from occurring within the laminate. The ability to wet out the glass filaments fully with resin is also important for CAF resistance. In summary, for each glass style, there is an optimal resin content range that balances the various performance requirements.

12.4.3 Laminate Flatness and Flexural Strength

When manufacturing the innerlayer circuit patterns, the flatness and flexural strength of the base material is important for successfully transporting these circuit layers through conveyorized equipment during PCB manufacture. This is particularly important for very thin laminates. If the laminate is curled, it can become caught or damaged inside this equipment. If the thin laminate with the circuit image sags on the conveyors, similar damage can occur.

For these reasons, it is sometimes preferred to use constructions with relatively high glass contents and use the thickest cloths possible, as this will result in greater flexural strengths, bearing in mind the performance requirements just discussed in Sec. 12.4.2. In addition, *balanced*

constructions, or those that use a symmetrical construction, are normally preferred to avoid curling. Asymmetrical constructions are more prone to curling and causing problems in conveyorized equipment in the PCB manufacturing process. Consider a 0.0080-in laminate as an example. Table 12.2 shows three constructions for this thickness, 1-7628, 1-2313/1-2116, and 2-2116. The asymmetrical 1-2313/1-2116 construction will be more prone to curling than the other constructions. A word of caution is warranted, however. Curling is but one property that must be considered. Dimensional stability, thickness control, electrical, thermal and possibly CAF properties must also be considered when choosing a construction.

12.5 PREPREG OPTIONS AND YIELD-PER-PLY VALUES

Just as there are a variety of base laminate constructions, there are a variety of prepreg options. Each fiberglass cloth style can be treated to multiple resin contents and flow values. While the same properties must be considered for prepreg materials as for base laminates, prepregs must also contain sufficient resin to flow and fill in the innerlayer circuitry of a multilayer circuit board. Since the innerlayer circuits can vary in terms of copper thickness and circuit density, a variety of resin content and flow value options are typically required when specifying prepreg styles. Higher resin contents may be needed when filling heavy copper weights and signal layers, while lower resin contents can be used against lighter copper weights and power or ground circuit patterns. And as noted above, some resin systems are more dense than others, so when choosing a prepreg resin content based on weight, the user should be aware that a higher resin content may be needed to ensure enough resin

volume for filling circuitry and thickness in the dielectric. Table 12.3 shows some common prepreg styles with various resin contents and thickness yields per ply.

TABLE 12.3 Common Prepreg Styles with Examples of Thickness for One Product[4]

Glass Style	Approximate Resin Content, %	Thickness, in*
106	66	0.00175
106	71	0.0020
106	75	0.00225
1067	70	0.0024
1067	74	0.0027
1080	57	0.0025
1080	64	0.0030
1080	66	0.00325
1086	64	0.0033
1086	68	0.0036
2113	50	0.0035
2113	55	0.0040
3313	55	0.0040
3313	59	0.0045
2116	50	0.0045
2116	52	0.00475
2116	55	0.00525
7628	40	0.0070
7628	42	0.00725
7628	44	0.0075
7628	45	0.00775

*Assumes a given flow value and represents thickness without filling innerlayer circuitry.

12.6 DIMENSIONAL STABILITY

As circuit layer counts grow and via-to-pad size ratios get tighter, the alignment or registration of the layers of circuitry become extremely important. Although several material and process variables contribute to the capability to achieve layer-to-layer and via-to-innerlayer feature registration, laminate dimensional stability is one of the most important. This is especially true in high-layer-count circuits that use thin laminates, since thinner laminates are generally not as dimensionally stable as thicker laminates.

12.6.1 Dimensional Stability Test Methods[5]

A common test method used to evaluate dimensional stability starts with a sample of a copper-clad laminate with scribed targets or holes in the four corners of the sample. Baseline measurements of the distances between these holes are taken prior to conditioning of the sample. One conditioning procedure involves etching the copper cladding off and remeasuring and determining the dimensional movement compared to the baseline. A second method subjects the sample to a thermal cycle, commonly a bake at 150°C for 2 hours. Again, measurements are taken after conditioning and compared to the baseline dimensions. A third method involves first etching the cladding off, measuring, subjecting the sample to the bake cycle, and measuring again. Each of these methods can be used as a process control tool in the laminate manufacturing process.

However, these test methods are of limited value to the printed circuit manufacturer, who etches circuit images on these laminates, combines them with prepreg materials and other laminates, and presses them together under

temperature and pressure to form a multilayer circuit. It is the predictability and consistency of laminate movement through the printed circuit manufacturing process, across a variety of circuit patterns and especially through the multilayer lamination cycle, that is of concern for the circuit manufacturer and ultimately for the designer who wants to increase circuit density. Multilayer lamination cycles commonly reach 185°C or higher, and normally exceed the T_g of the base material. Above the T_g, the resin softens and allows tension in the laminate to be released and is also subject to stresses from the surrounding materials and lamination pressure. Most of the movement of the laminate in the circuit manufacturing process occurs during this lamination cycle.

12.6.2 Improving Dimensional Stability

Although many variables in laminate and circuit manufacturing processes can influence dimensional stability, some common techniques involve laminate press cycle optimization, control of laminate resin contents, and the use of higher T_g materials. New materials and process techniques have also been developed to improve dimensional stability.

12.6.2.1 Laminate Manufacturing Process Considerations. Many laminate manufacturers reduce the lamination pressure at a specified point in their lamination cycle to minimize the stress that becomes stored in the finished product, which improves subsequent dimensional stability.

Other process controls in the laminate manufacturing process are also important for dimensional stability. Control of the raw materials, especially the glass cloth, can

contribute to dimensional stability. The tension applied to the cloth during the treating process, the heat rise, temperature, and pressure profiles during lamination, as well as laminate stack-up techniques during lamination can all affect dimensional stability. Consistency in these parameters will generally improve the consistency observed during the printed circuit manufacturing process.

12.6.2.2 Impact of RTFs. RTF copper foils typically allow the elimination of surface-roughening processes in the innerlayer circuit imaging process. These surface-roughening processes can be mechanical scrubbing processes that can stretch or distort thin laminates. In addition, variation in the mechanical scrubbing process over time can introduce lot-to-lot variation, which adversely impacts registration capabilities. RTF foil, which facilitates the removal of these scrubbing processes because of the improved photoresist adhesion to the matte side of the foil, can therefore result in improvements in registration capability.

12.6.2.3 Fiberglass Cloths and Resin-to-Glass Ratios. Each fiberglass cloth style used in laminates and prepregs has a resin content range that results in sufficient wet-out of the glass cloth, is relatively easy to control, and therefore results in more uniform thickness and more consistent dimensional stability. The specification of laminates and prepregs with resin contents in the desired ranges can result in improvements in dimensional stability and therefore registration capabilities. As a result, having a range of fiberglass cloth styles available is important to be able to achieve a wide range of dielectric thicknesses.

12.6.2.4 Nonwoven Reinforcements. Because of the woven, serpentine geometry of the yarns in fiberglass cloths, they can behave like springs when used as the reinforcement of base materials. During the resin treating process and the

laminate pressing operation, the fiberglass cloth is subjected to stresses that can be stored in the laminate as the resin is cured. These stresses can then be released during the circuit manufacturing process, causing dimensional changes.

Nonwoven materials can avoid these stresses. In one nonwoven material type, short, randomly oriented fibers are treated with the resin system. In a second type, linear strands of fiberglass are laid down in a balanced, cross-plied orientation, which resists subsequent stresses.

12.6.2.5 Multilayer Press Cycle Optimization. Most of the dimensional changes in the laminate occur during the multilayer press cycle when the temperature exceeds the T_g of the resin in the laminate. Above the T_g, the resin system in the laminate softens and allows any stored stress in the reinforcement to be released and allows the laminate to be affected by the adjacent materials and the pressure of the lamination cycle.

Understanding the rheology of the resin in the prepreg is important when designing the multilayer lamination cycle. The point at which the resin begins to melt, the point at which it begins to cure, and the relationship between the heat rise and the viscosity profile of the resin are all important. With respect to viscosity, not only is the minimum viscosity achieved important, but the length of time that the resin is below a certain viscosity, allowing the resin to flow and fill the internal circuit features, is also important. With an understanding of these parameters, it is possible to design “kiss” cycles, or “soak” cycles, where pressure and temperature profiles, respectively, are designed to improve performance, including dimensional stability.

In addition, although seldom done in practice, using a resin system in the prepreg materials that can be cured below the T_g of the resin system in the laminate can avoid the softening of the laminate resin system and therefore prevent

much of the movement that takes place. The resistance to the use of this technique is usually driven by a desire to keep the resin system same throughout the multilayer PCB.

12.7 HIGH-DENSITY INTERCONNECT/MICROVIA MATERIALS

One method used to increase circuit density is to use blind and buried vias. Rather than placing a via hole completely through the PCB, blind and buried vias go only partly through the multilayer circuit, joining only the layers that require connection. By not extending these vias through the entire multilayer, real estate on the other layers becomes available for additional circuit routing. Buried vias are those that are not visible from the outside of the finished circuit board, and are formed in a subcomposite or copper-clad laminate. Blind vias are those that are visible from the outside of the multilayer circuit but do not go completely through it. By limiting the size of these vias, you can significantly increase interconnection density. Microvia or high-density interconnection (HDI) printed circuit designs utilize these technologies to increase circuit density.

While the materials already discussed are used in blind and buried via applications using conventional processes, additional materials can be used to increase density using more specialized materials and process techniques. The specialized processes used to form microvias include laser ablation, plasma etching, and photoimaging, with laser formation by far the most common today.

The resin system will generally ablate much faster in laser drilling processes. Also, plasmas are not effective in etching through fiberglass. As a result, materials that use an alternative reinforcement or do not contain an inorganic

reinforcement have been developed for some types of applications.

For blind via applications, resin-coated copper foil can be used to form the external circuit layer and dielectrics between layers 1 to 2 and n to $n - 1$, using laser or plasma processes to form the vias. Buried vias could be formed in sequential processes. Two basic types of resin-coated copper foil have been used. The first type uses one layer of partially cured resin (see Fig. 12.9).

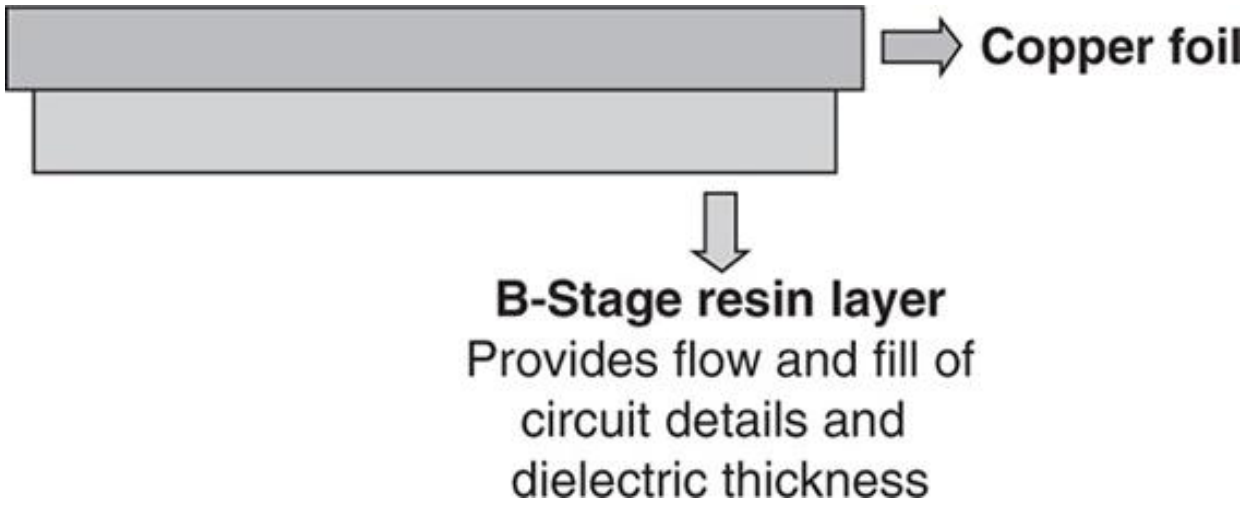


FIGURE 12.9 Resin-coated copper foil with a single layer of B-staged resin.

This resin-coated foil is then laminated to the rest of the multilayer circuit. A second type of resin-coated copper foil uses two layers of resin (see Figs. 12.10 and 12.11). The first layer is fully cured whereas the second is partially cured. This technique guarantees a minimum dielectric separation between the external foil and the circuitry on the next layer in, since the cured resin layer limits how close the internal circuit layer can get to the external foil.

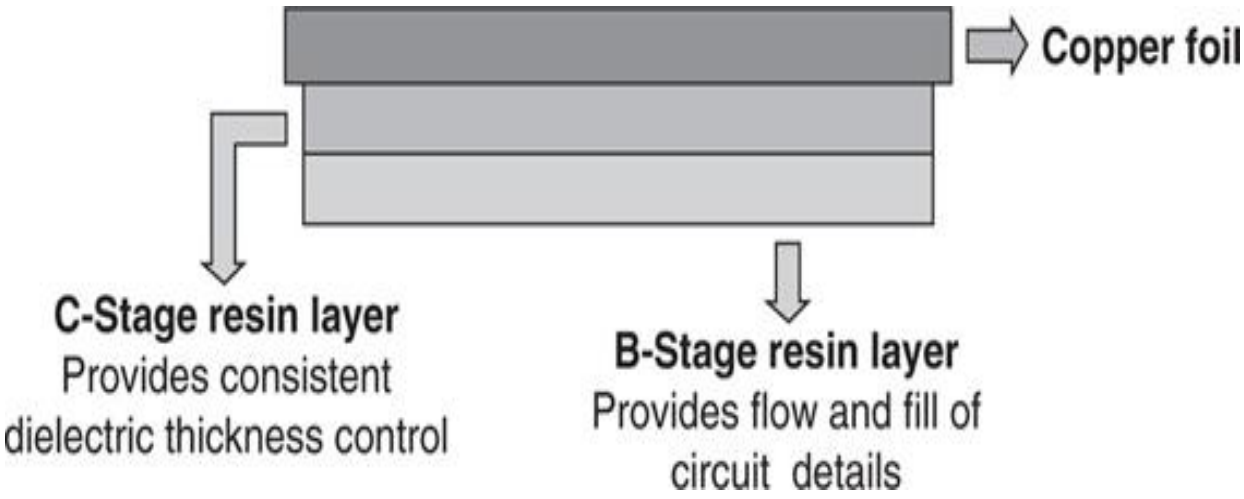


FIGURE 12.10 Resin-coated copper foil with a C-stage and B-stage layer.

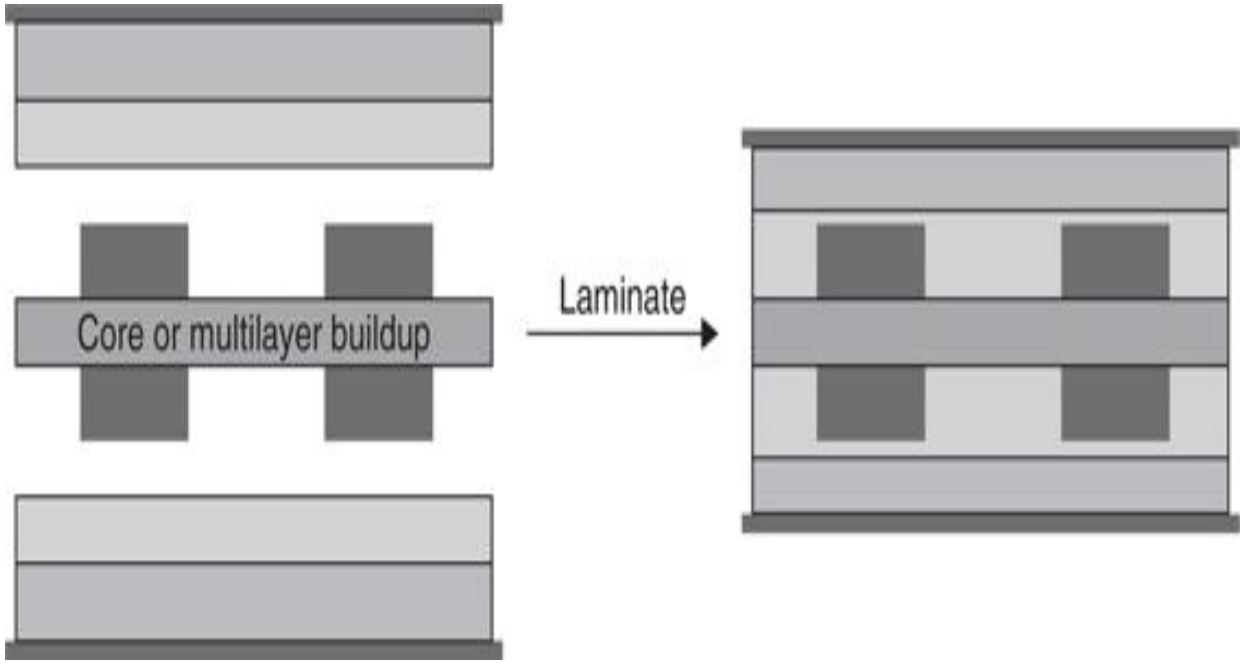


FIGURE 12.11 C-stage plus B-stage resin-coated copper foil laminated to PCB.

Other materials used in HDI designs utilize an organic reinforcement that can be laser ablated or plasma etched. These systems use proprietary polymer systems and can have a variety of properties.

Another process technique used in these applications involves photoimaging a permanent dielectric material in order to form the microvias. These photoimageable

dielectrics resemble plating resists but must be able to be catalyzed for subsequent plating operations that will form the external circuit image, and must adhere sufficiently to the rest of the multilayer circuit to provide long-term reliability.

12.8 CONDUCTIVE ANODIC FILAMENT GROWTH

Conductive anodic filament (CAF) formation is a term used to describe an electrochemical reaction in which conductive paths are formed within a dielectric material due to transport of metal or metal salts through the dielectric. These paths may form between two circuit traces, between two vias, or between a trace and a via, as illustrated in Fig. 12.12. CAF formation between a hole and a plane inside the PCB is also possible, and is similar in concept to hole-to-trace CAF formation. By definition, as circuit density increases, the space between these features decreases. With shorter paths between features, CAF growth becomes a more critical reliability consideration.

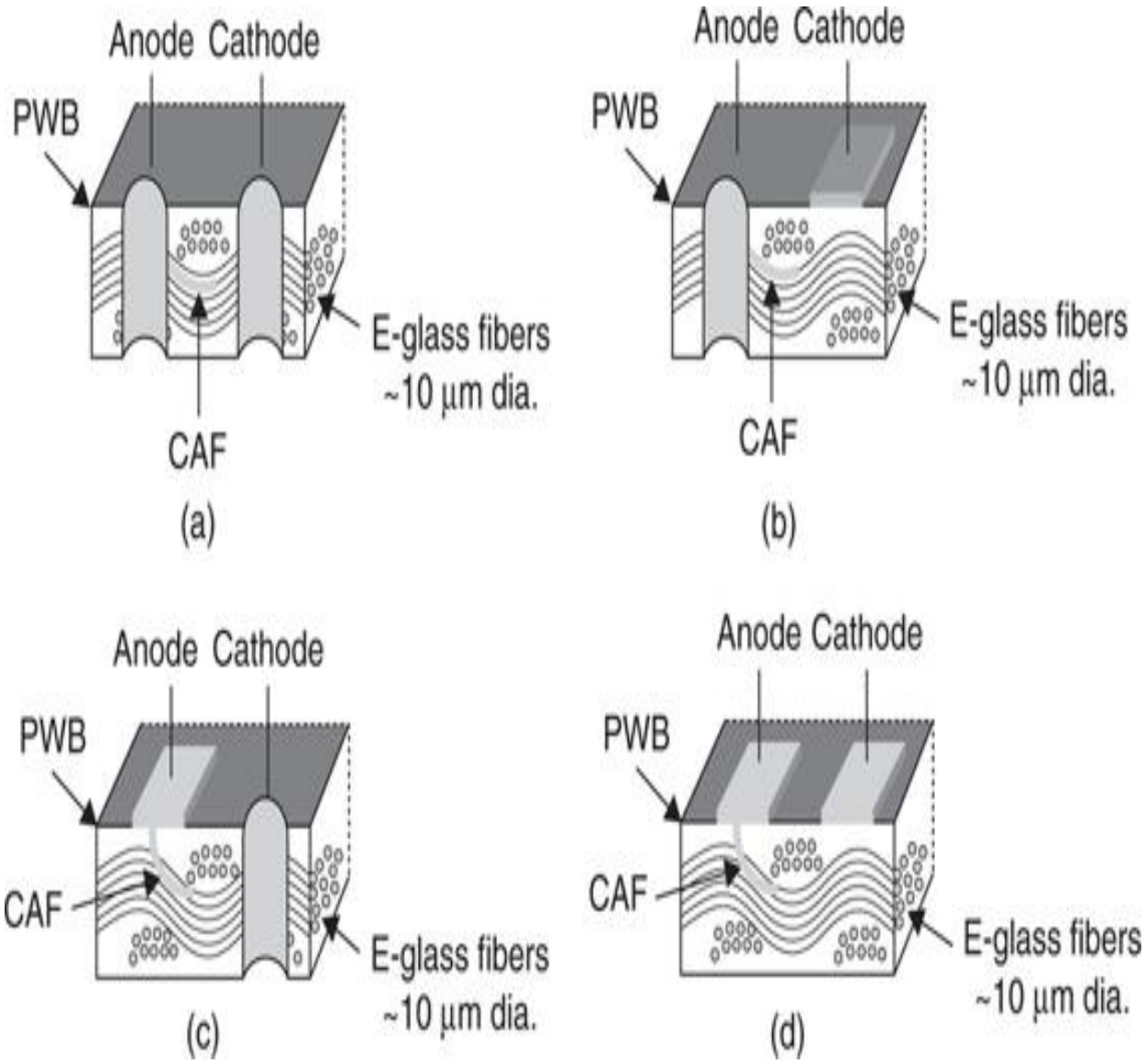


FIGURE 12.12 Pathways for CAF formation: (*a*) hole to hole, (*b*) hole to track, (*c*) track to hole, and (*d*) track to track.

For CAF growth to occur, a bias and a path for this filament growth must be present. In fiberglass-reinforced materials, a gap between the resin and the fiberglass filaments is the most common pathway. If the glass is not completely wet-out with resin, or if the bond between the resin system and the fiberglass filaments is insufficient or is compromised, the resulting gap can become such a path. Hollow fiberglass filaments can also provide a path. In addition, there must be a medium in which this electromigration can occur, such as

absorbed moisture that allows dissolved ionic species to migrate and promote the electrochemical reaction that leads to CAF. Figure 12.13 is an actual example of CAF formation.

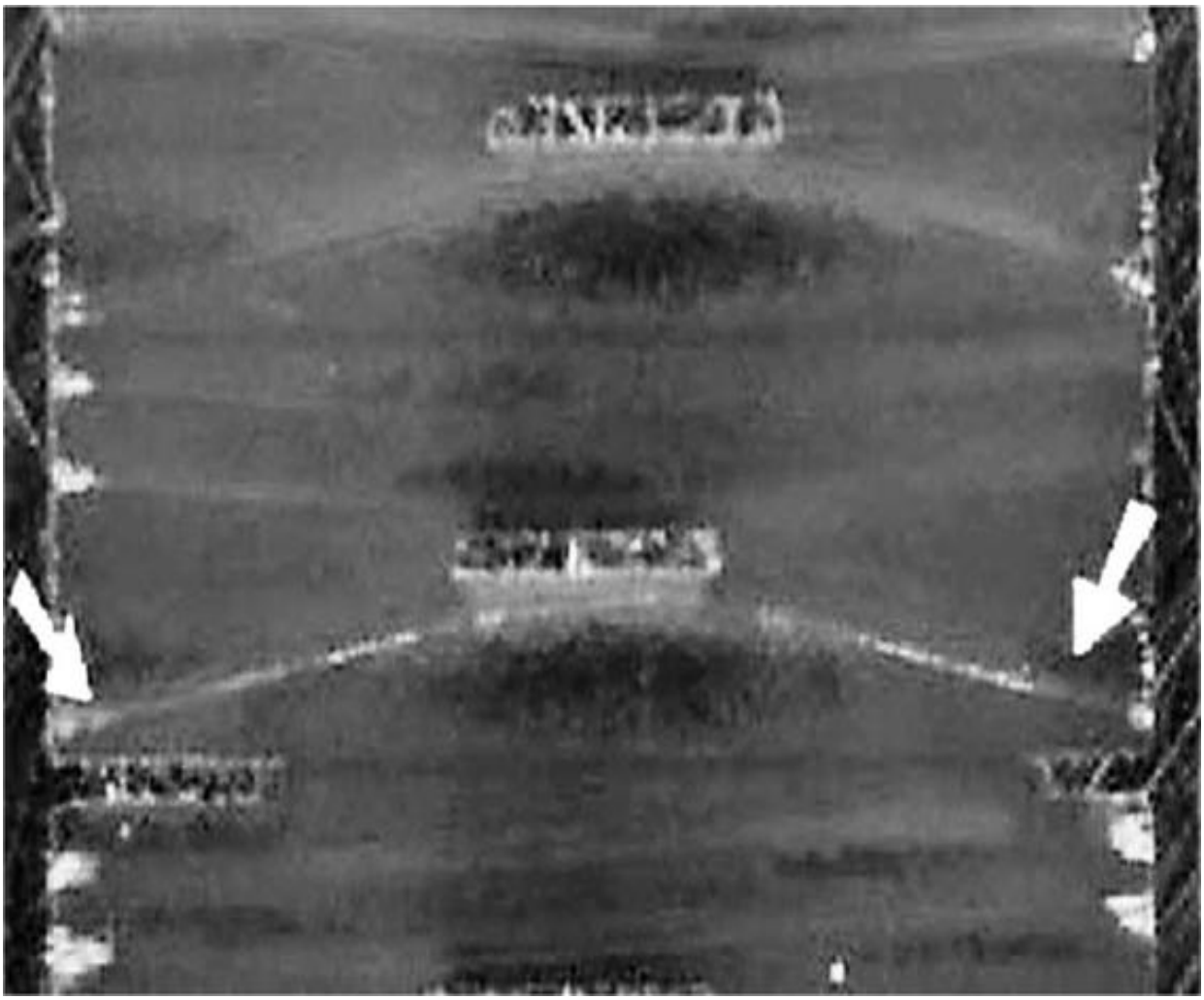


FIGURE 12.13 An example of CAF between two plated through holes.

End product use also influences the overall risk. In general, low voltage and office equipment environments where humidity is low, are lower risk. Outdoor uses, such as automobiles, military, airplanes, and outside electronics are much higher risk, as temperature and humidity levels in the operating environment can be higher.

Product design has a large role in determining CAF risk. If you are concerned about CAF formation in a product under

design, there are sources of good information on reducing CAF risk with design. This is the easiest and least expensive way to manage CAF risk.

A later chapter in this book is devoted specifically to CAF, and further discussion is provided in the next chapter on selecting materials, but the following items present some key findings of CAF research:

- CAF is a two-step process consisting of path formation and the electrochemical reaction.
- The filament is usually in the form of a copper salt.
- Moisture absorption can influence the rate of CAF formation, and there is a minimum threshold for moisture absorption below which CAF is unlikely to occur.
- Temperature can influence the rate of the electrochemical reaction.
- The level of voltage bias can also influence the rate of CAF formation.
- Resin-to-glass wet-out is critical in that it eliminates a potential pathway.
- Beyond glass wet-out, the bond between the resin and the glass is important to ensure that adhesion is not lost due to moisture or thermal stress. Selection of the coupling agent used to improve adhesion between the resin and the glass is critical in this regard, and different resin systems may require different coupling agent types. Figure 12.14 shows examples of silane coupling agents, where “R” represents various chemical species that can be modified for different applications.

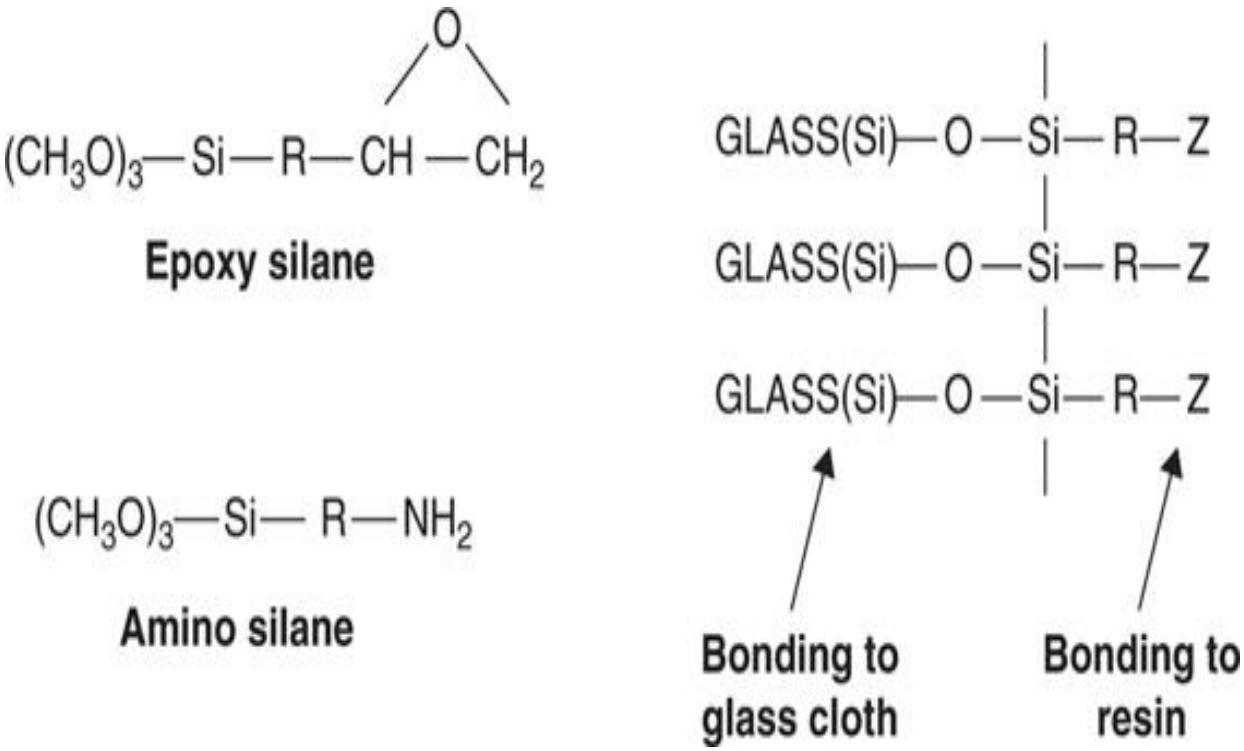


FIGURE 12.14 Examples of silane coupling agents.

- The cleanliness of the glass, both before coating with silane as well as prior to coating with the resin system, is important to ensure proper wetting and bonding of resin to glass.
- The curing agent used in the resin system can influence CAF formation. This may be due to the tendency of some curing agents to absorb moisture, or to the electrochemical nature of the specific curing agent, or both.
- Contaminants on the glass cloth or within the resin system can also accelerate CAF formation. For example, residual hydrolyzable chlorides present in some epoxy resins are known to catalyze electrochemical reactions that can lead to CAF.
- Resin system thermal stability and thermal expansion may influence performance as well, especially as lead-free assembly processes cause PCBs to be subjected to more severe thermal excursions. This is due to the possibility of

thermal decomposition of the resin causing reduced resin-to-glass adhesion or even voids within the laminate that can provide path- ways for CAF formation. With respect to thermal expansion, the higher temperatures of lead-free assembly result in a greater total stress at the resin-to-glass interface due to the CTE mismatch between them. If this stress is high enough, or the bond strength low enough, separation of the resin from the glass can occur and provide a pathway for CAF as well.

The processing used in printed circuit fabrication can also influence CAF resistance. Some of the factors to consider in PCB fabrication include the following:

- The innerlayer surface must be clean. Adequate rinsing of the innerlayers after chemical processes is important to minimize residual ionic contamination.
- Storage conditions and shelf life of prepreg materials are important to control to ensure adequate flow properties during multilayer lamination.
- Multilayer lamination processing is important to ensure good resin flow and full wetting of resin to glass in the prepreg layers. Vacuum, temperature, and pressure profiles are all important.
- Drilled hole quality is also important. With respect to CAF performance, minimizing resin- to-glass fracturing that can result in excessive wicking of plating chemistries is critical.
- Control of desmear and electroless copper-plating chemistries is also important. Minimizing any further attack of the resin-to-glass interface and plating into the dielectric are the key considerations. Good rinsing to minimize residual ionic contamination from these processes is also important.

12.8.1 CAF TESTING

Many different types of test vehicles are used to assess CAF performance, but most include the design features described in Fig. 12.12. Differences between common test vehicles include the distances between features, the thickness and layer counts of the PCBs, and the glass styles and resin contents used to build the PCB. All of these factors influence CAF, if not directly, as a result of the processes used to build the specific test vehicle. In addition, testing parameters such as bias, temperature, and humidity also influence results. Various OEMs will also have different requirements for the time of testing, with typical time requirements ranging from 500 to 1000 hours.

Figure 12.15 shows an example of CAF found in one test vehicle. In this case, the pathway formed between individual filaments of the glass cloth, either because they had not been sufficiently coated with resin or because resin decomposition, moisture, or other volatile compounds created a void.

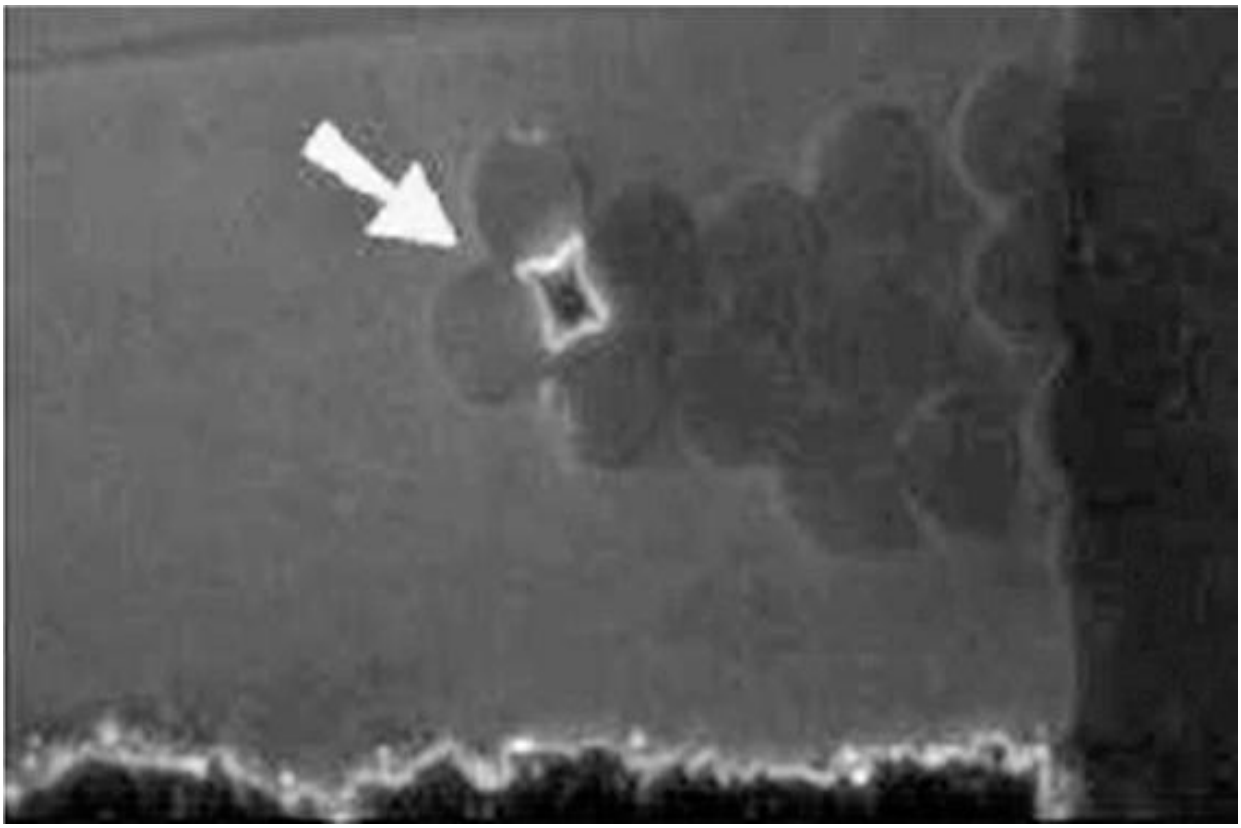


FIGURE 12.15 CAF formation between glass filaments in a PCB test vehicle.

A general suggestion for CAF testing is to perform failure analysis on at least some of the failed nets. The failures could be unrelated to material, as many fabrication issues cause the same results. Also, the failure may not be internal to the PCB, but along the surface, which is not a CAF type failure. The key is to make the correct decision about the material to use, and this will be discussed further in the next chapter.

Using material that has been functionally tested for CAF resistance is a recommended practice if you have concerns about products failing for CAF. Either set up your own testing or ask to see testing data run at an independent testing lab.

12.8.1.1 CAF Test Example #1. A common test vehicle used to assess CAF performance consists of a 10-layer PCB, often made of single-ply 2116 style dielectrics in each of the

core and prepreg layers, though other glass styles can and should be evaluated. Common test conditions are either 65°C/85 percent relative humidity (RH) or 85°C/85 percent RH, with 10 or 100 V bias. This test vehicle includes design features such as those shown in Fig. 12.12, but the hole-to-hole features are typically the most critically examined. In addition, placement of the holes relative to the glass cloth weave can influence results. When the holes are placed in line with the glass weave, the filaments can bridge the holes, providing a potential CAF pathway. If the holes are placed diagonal to the weave orientation such that no individual filament bridges two holes under test, this potential pathway is eliminated. In practice, holes placed in line with the glass weave are the most relevant for assessing CAF resistance. Hole spacing is a critical parameter, and this particular test vehicle examines holes placed approximately 10, 15, 20, and 25 mil apart. Although the definition of failure can vary slightly from OEM to OEM, the criteria usually consist of some minimum insulation resistance value, and often a maximum decrease in resistance of one order of magnitude, or “a decade drop in resistance.” Figure 12.16 provides results for one laminate material processed by one PCB fabricator.

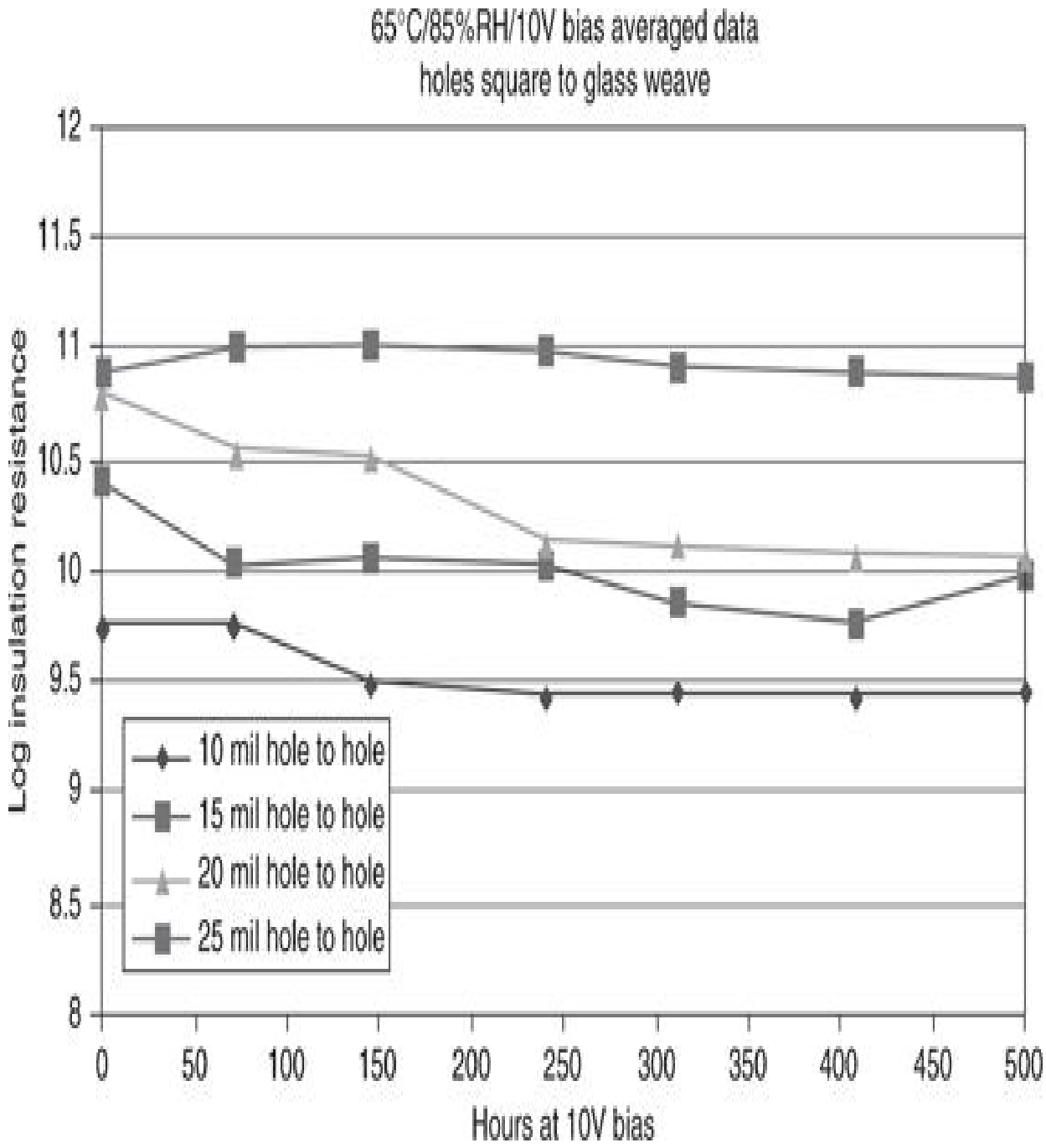


FIGURE 12.16 Insulation resistance CAF test results for example #1.

This chart plots average insulation resistance for 25 test coupons (on a log scale in this example) versus time in hours at a 10 V bias with 65°C/85 percent RH environmental conditions. It also shows the data separately for the 10, 15, 20, and 25 mil hole-to-hole spacings. Other things being

equal, average insulation resistance will be higher for holes spaced further apart, as this means there will be more dielectric between features. For this particular test, the average insulation resistance for each spacing did not decrease by an order of magnitude, indicating good results. However, it is also important to examine the individual coupons tested, and a common way to assess performance in this regard is to calculate the percentage of individual test coupons that pass or fail. Figure 12.17 provides this data for this same test, and shows results for the test material highlighted in Fig. 12.16 versus a control group that utilized a different laminate material.

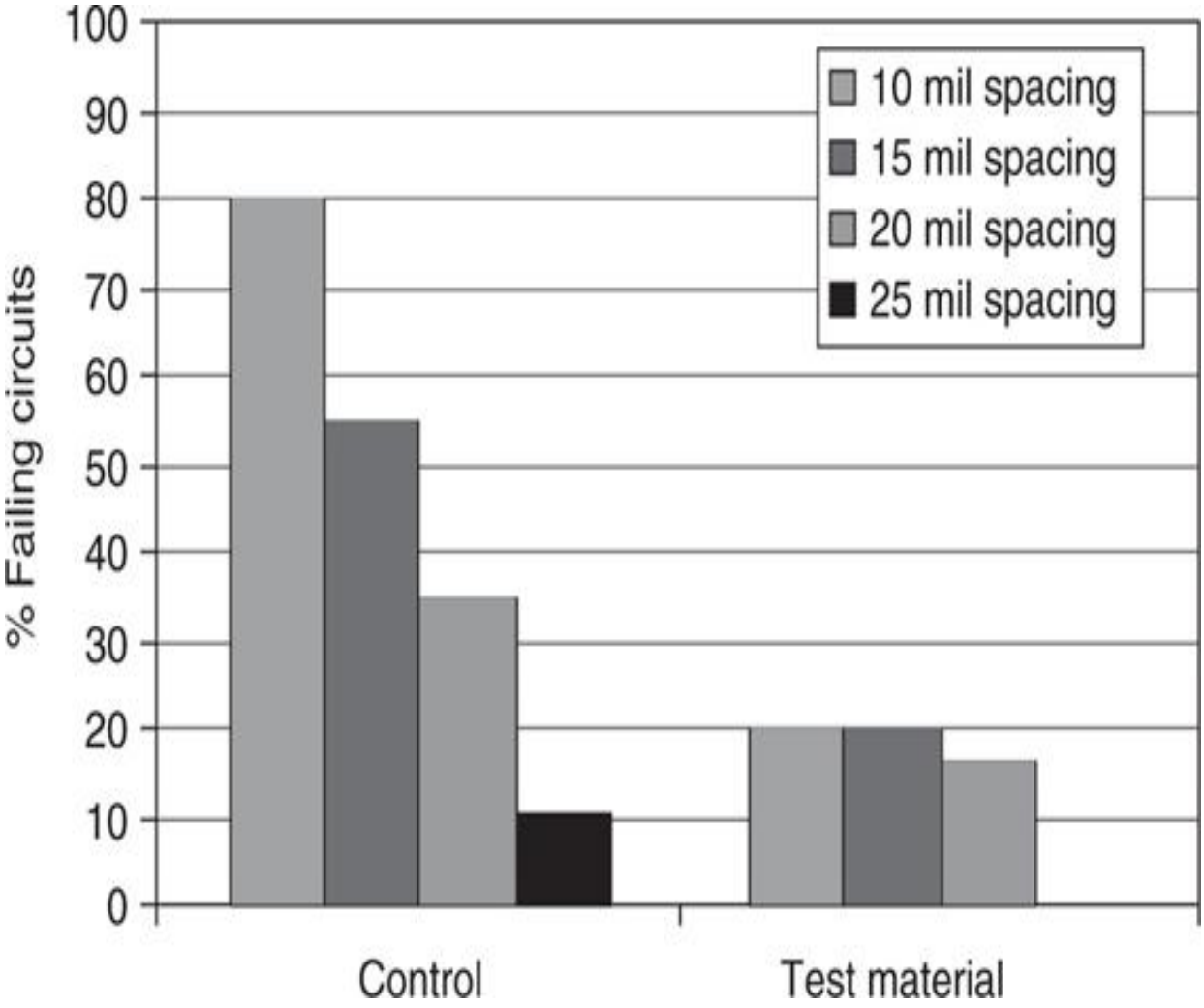


FIGURE 12.17 Percent failing coupons in CAF test example #1.

As is common, the control group shows fewer individual failures as the spacing between holes increase. The test material shows a much lower percentage of individual failures for each spacing. As stated earlier; however, it is important to perform failure analysis in order to determine if the failures in terms of insulation resistance were really caused by CAF, or by some other defect such as contamination.

12.8.1.2 CAF Test Example #2. In a second example, four commonly available FR-4 materials were compared by building the same CAF test vehicle as described in example #1. These materials are all promoted as being "CAF-resistant." The coupons were manufactured by the same PCB fabricator during the same time period. In this evaluation, the test conditions were 100 volts bias, 85°C and 85 percent RH. The same hole-to-hole spacings were evaluated, but for simplicity, Figs. 12.18 and 12.19 show only the data for the 15 and 25 mil spacings, respectively. It is common to use a 1 MΩ resistor in series with the test point in these tests, so where the average insulation resistance drops to 10^6 Ω (6 on the *y* axis of the chart), this indicates that the resistance has dropped excessively and it is the resistor that is now being measured. In this evaluation, materials A, C, and D all drop to this level at 500 hours of testing with 15 mil hole-to-hole spacings. At 25-mil spacings A and C both drop to this level. B and C do not, but C drops in resistance by more than one order of magnitude. Only material B drops by less than one order of magnitude at both spacings. By these criteria, materials A, C, and D would have failed this test. Only material B passed.

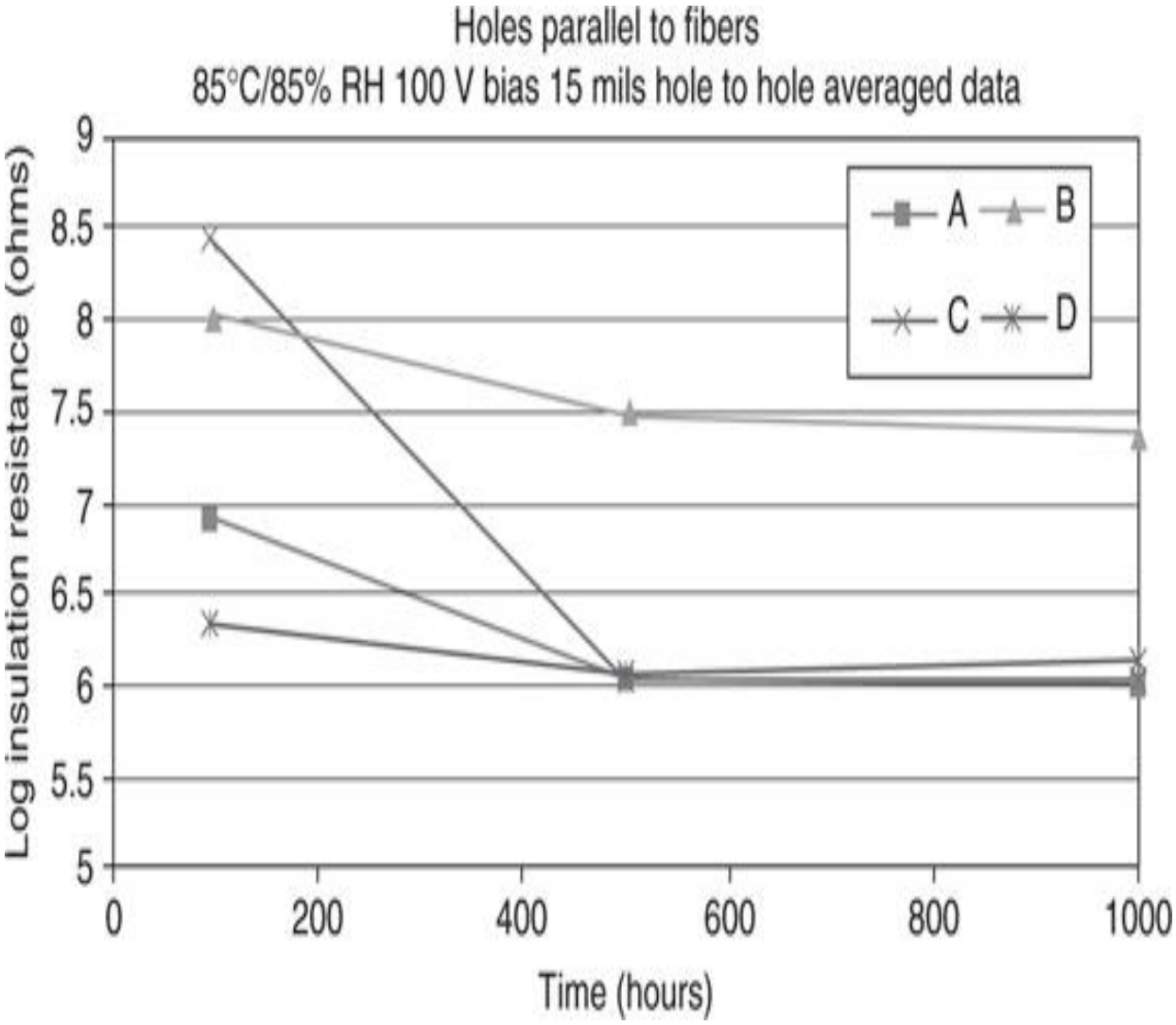


FIGURE 12.18 CAF results for 15-mil hole spacings in example #2.

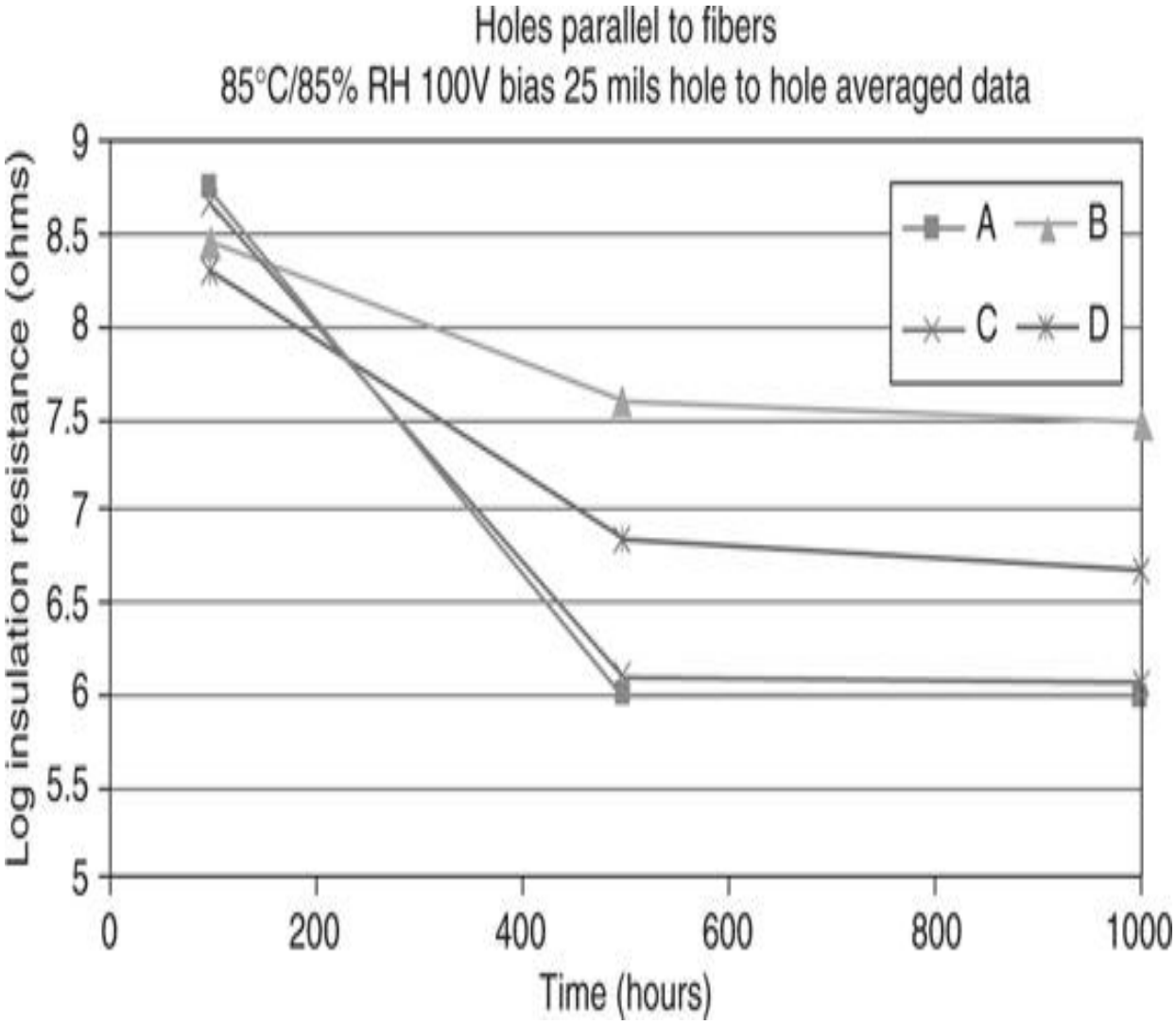


FIGURE 12.19 CAF results for 25-mil hole spacings in example #2.

12.8.1.3 CAF Test Example #3. In this third example of CAF testing, a different test vehicle design was used, and different temperature, humidity, and bias levels were also used. However, all the test coupons were manufactured at the same time by the same PCB fabricator, and in addition, the same resin system was used in groups 1 through 4. The differences between groups 1 through 4 involve different types of fiberglass cloth and differences in process controls used when treating the glass cloth with the resin system. This is the key point of this third example.

Figure 12.20 shows that while each group used exactly the same laminate material type, differences in glass cloth and treating process controls resulted in different CAF performance levels.

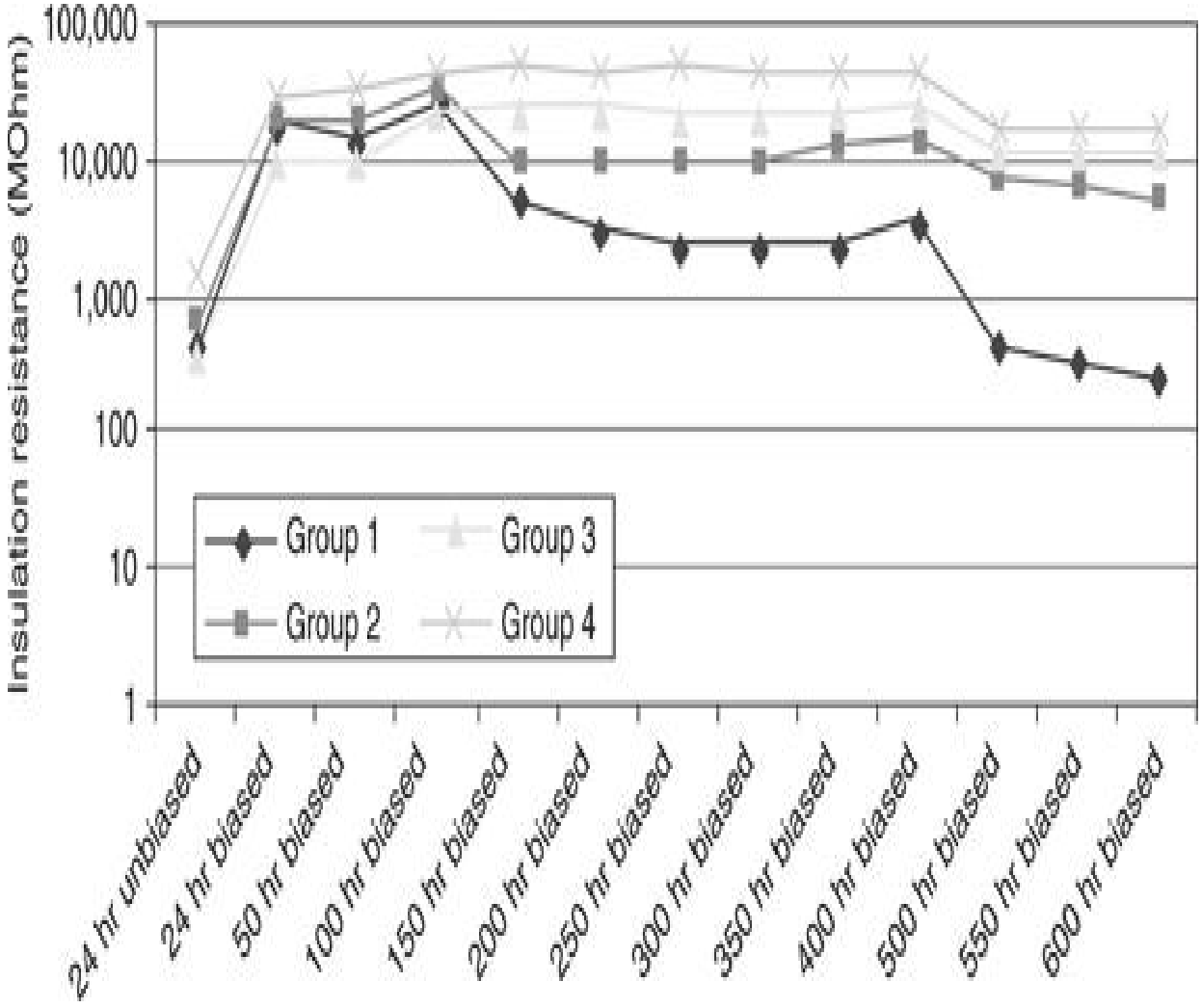


FIGURE 12.20 Results for CAF test example #3.

For each group, the chart shows average insulation resistance for a set of coupons over time. Clearly, the average insulation resistance varied by group, with group 1 showing the most significant decline in resistance. In addition, evaluating the individual coupons in each group provides additional insight into performance differences. In group 1, 40 percent of the coupons failed by 600 hours, with

the first failure occurring at 400 hours. In group 2, 20 percent of the coupons failed at 600 hours. Groups 3 through 5 did not have any failures in this test. So even though the resin system was the same for each group, differences in glass cloth and laminate manufacturing processes clearly can have a significant impact on CAF performance.

Chapter 14, covering material selection, will discuss this further and provide some recommendations for selecting materials when concerned about CAF.

12.9 ELECTRICAL PERFORMANCE

Base material electrical properties are an important consideration in sophisticated printed circuits operating at high frequencies. High data rates, measured in gigabits per second (Gbps), and high clock speeds make the dielectric constant (D_k) and dissipation factor (D_f) of base materials very important in high-speed digital circuits. Wireless and RF applications operating at very high frequencies also demand very low D_k and D_f values. Moreover, the consistency of these properties over a large frequency range is also important. These properties were defined generally in Chap. 12 as follows:

- *Dielectric constant/permittivity*. This is the ratio of the capacitance of a capacitor with a given dielectric material to the capacitance of the same capacitor with air as a dielectric. It refers to the ability of a material to store an electric charge.
- *Dissipation factor/loss tangent*. The property is the ratio of the total power loss in a material to the product of the voltage and current in a capacitor in which the material is a dielectric.

12.9.1 Importance of D_k and D_f

These properties are important because they affect signal transmission in the printed circuit. At low frequencies, a signal path in a printed circuit can typically be represented electrically as a capacitance in parallel with a resistance. However, as frequencies increase, at some point signal paths must be considered transmission lines where the electrical and dielectric properties of the base materials have a greater effect on signal transmission. A full discussion of capacitive versus transmission line environments is beyond the scope of this chapter, but the premise is to determine, for the transmission of a signal pulse of a given rise time, the acceptable length of a conductor before a significant voltage difference is realized along its length. Conductors longer than this critical value are then regarded as transmission lines. Because the velocity of signal propagation is inversely proportional to the square root of the permittivity of the dielectric, a lower permittivity value results in faster signal speeds and a longer rise distance. With a larger rise distance, larger conductor lengths are acceptable before a significant voltage drop is experienced. However, if the ratio of conductor length to rise distance is large enough, signal reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum plateau value, and pulse additions that occur under these circumstances may lead to false triggering of a device.

On the other hand, signal attenuation can result in missed signals. One of the causes of signal attenuation is dielectric loss. As the circuit operates, the dielectric medium absorbs energy from the signal. Attenuation of the signal by the dielectric is directly proportional to the square root of permittivity and directly proportional to the loss tangent. In addition, dielectric losses increase as frequencies increase. When a high bandwidth is desired, this effect has a greater

impact on the higher-frequency components, and the bandwidth of the propagating pulse decreases and degrades the rise time.

Because the permittivity and loss tangent vary with frequency, and other factors to be discussed later in this chapter, the degree to which these properties vary is also an important circuit design consideration. If these properties vary significantly with frequency, designing a circuit with devices that operate at various frequencies becomes that much more complex. In addition, operating within a given bandwidth becomes that much more difficult as different frequency components experience different dielectric properties, which in turn lead to differences in signal propagation and loss.

Therefore, base materials with low permittivity values and low loss factors are desired for high-speed, high-frequency printed circuits. In addition, consistency of these properties across frequencies is also required. Besides frequency dependence, since operating environments can also vary, the consistency of these properties across environmental conditions is also important and is discussed in the following sections.

12.9.2 High-Speed Digital Basics

Figure 12.21 is a representation of high-speed digital communication that involves sending bits of information coded in waveforms.

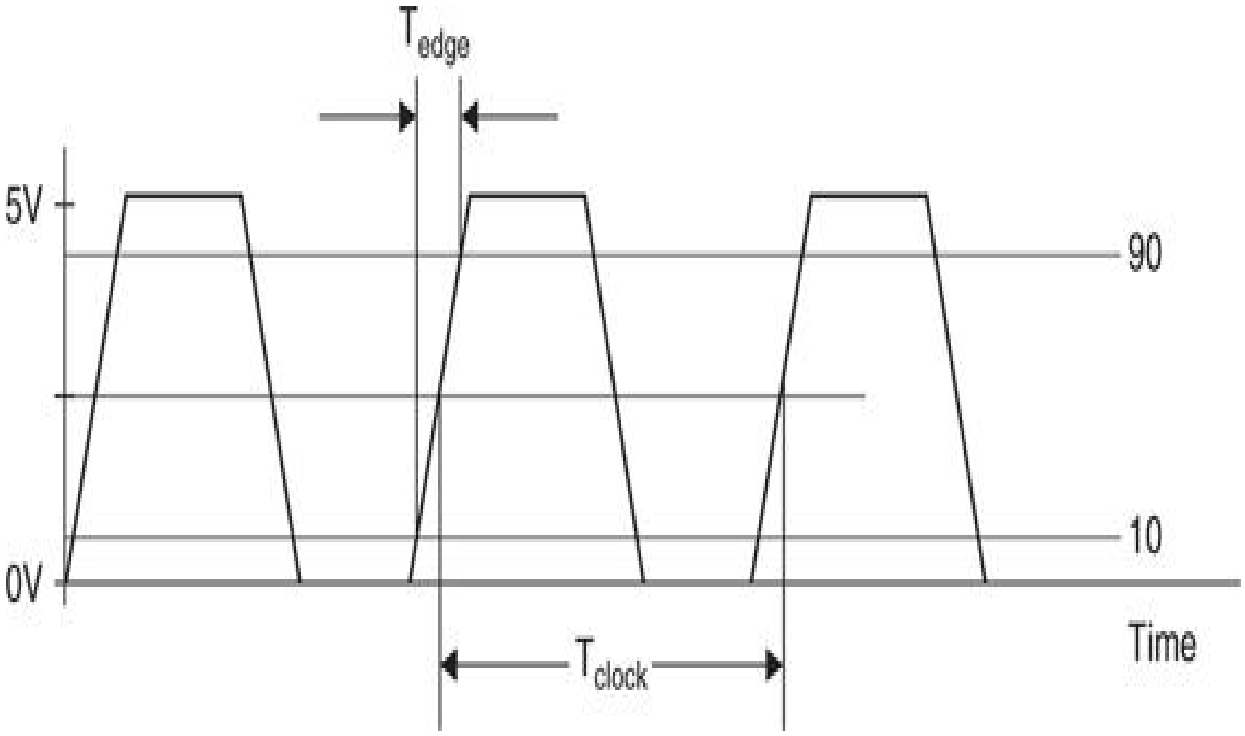


FIGURE 12.21 Digital communication.

The zeros and ones of binary information are coded on the rise time or on both the rise time and fall time. The high voltage represents 1 and the low voltage represents 0. The faster the rise time, the faster the signal. To achieve faster rise times, sinusoidal wave forms are superimposed on one another. The range of frequencies used is called the bandwidth, with the bandwidth given as 0.35/rise time. In short, a faster rise time allows for a greater range of frequencies, or greater bandwidth.

Figure 12.22 provides an example of eye pattern analysis. The eye opening size is related to these attributes: signal attenuation, rise time degradation, signal noise, and jitter. In this analysis, the height of the central eye opening is a function of amplitude degradation in the received signal. The width of the signal band at the corner of the eye measures the jitter. Signal attenuation and rise time degradation are a function of dissipation factor and frequency; lower dissipation factor (D_f) decreases the magnitude of change to

these factors. Jitter is caused by several factors, but small areas of varying dielectric constant (D_k) is an important material related cause. Transitions between the top and bottom of the eye show the rise and fall times of the signal.

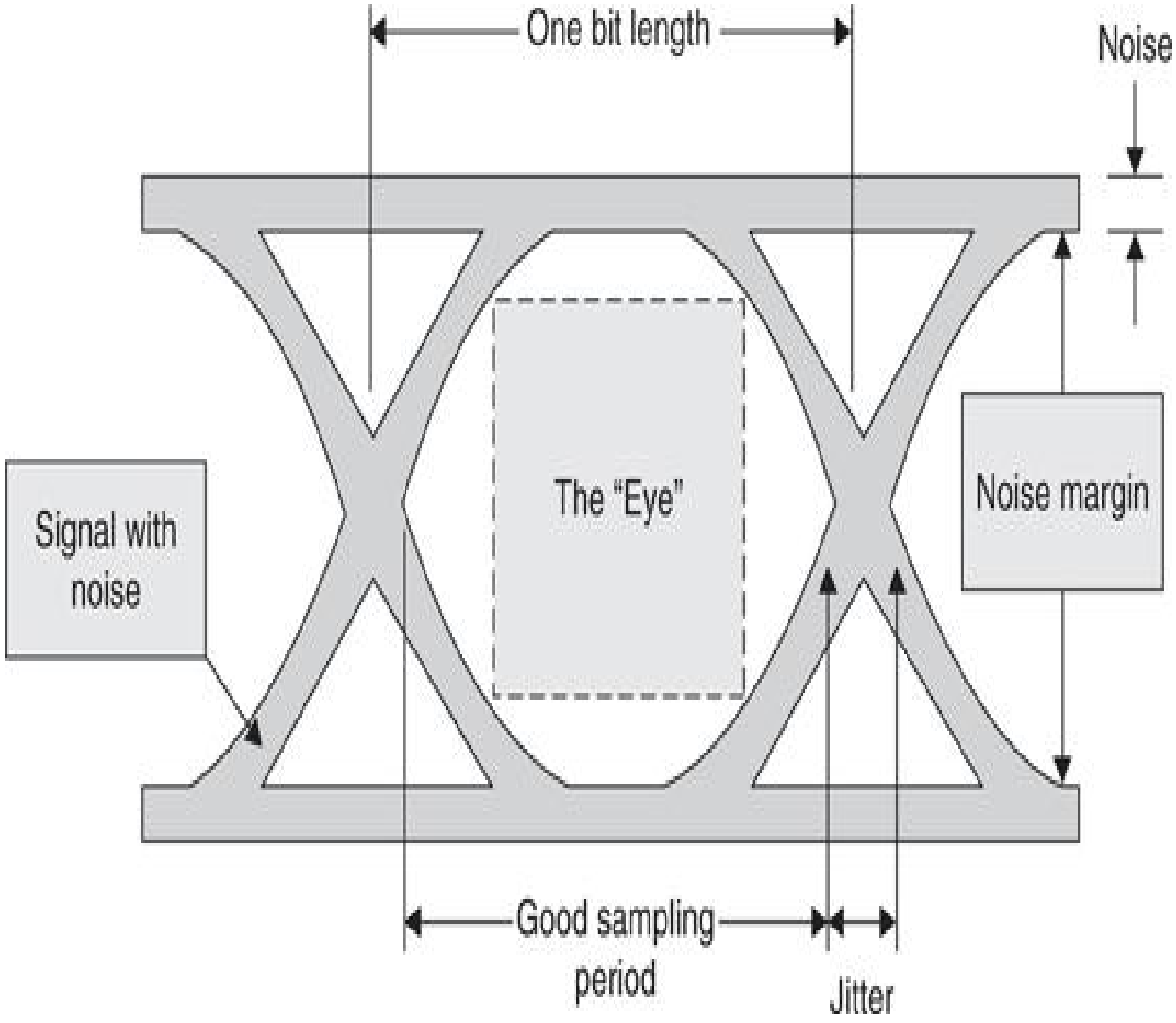
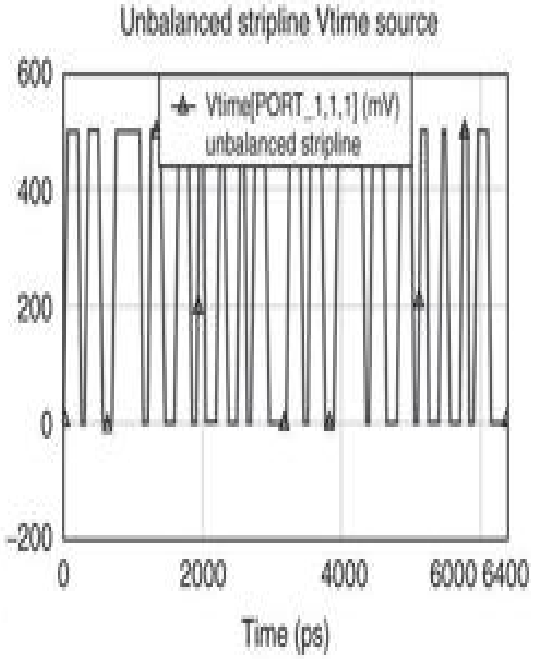


FIGURE 12.22 Eye pattern analysis.

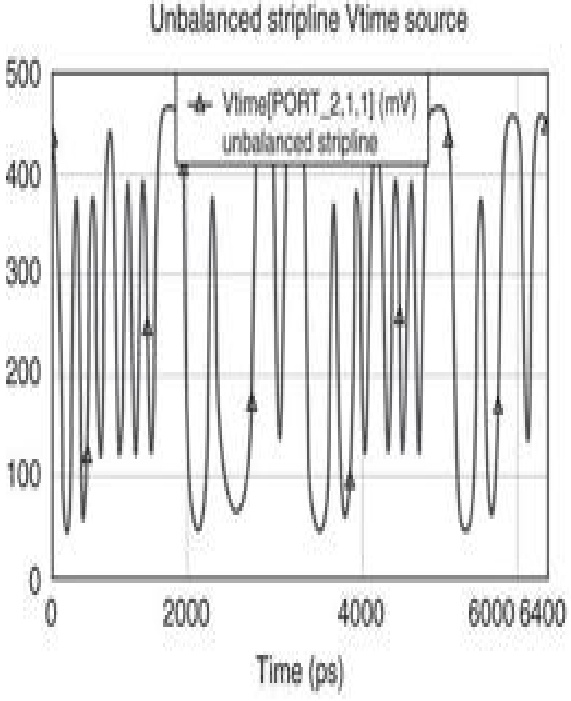
Figure 12.23 illustrates potential signal integrity differences when different base materials are used. The top chart shows an example of a 10-Gbps signal at the source. Note the pattern in this chart. It changes from 0 in the *x* axis (0) to its peak value (1). Now look at the chart in the lower-left corner of Fig. 12.23, representing the use of a standard

FR-4 material. Note the change in the pattern, particularly the decreased amplitude. When the signal degrades as illustrated here, the function of the circuit can be significantly impacted. Now examine the chart in the lower-right corner. This is for a low D_k/D_f material. Note the improved amplitude compared to the standard FR-4 material and a pattern much closer to the signal at the source. Figure 12.24 takes this analysis further. The chart in the upper-left corner is the signal at the source. This is as good as it gets. The remaining charts illustrate how the signal is affected with materials of increasing D_f. Note the diagram for the standard FR-4 under these conditions. This would represent an unacceptable condition, as the eye is almost completely closed. As the D_f is decreased from the FR-4 level, the pattern improves.

A 10 Gbps signal at source



After 40 inches through standard FR-4



After 40 inches through a low Dk/Df material

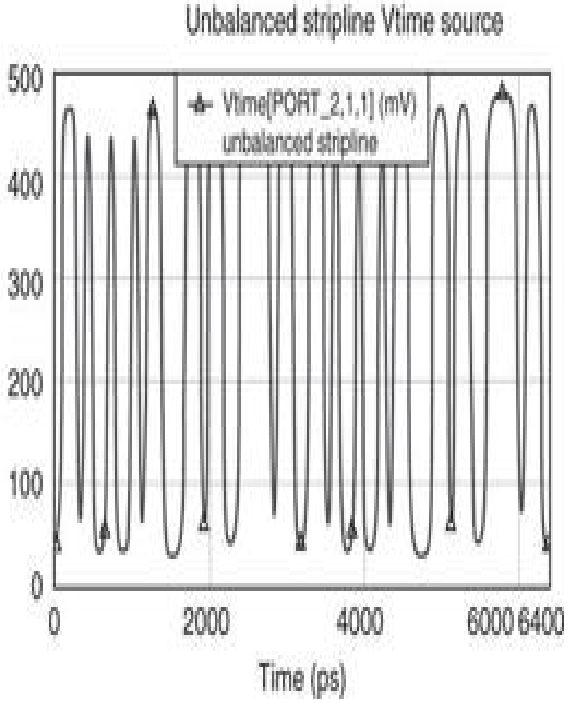


FIGURE 12.23 Substrate influence on signal integrity.

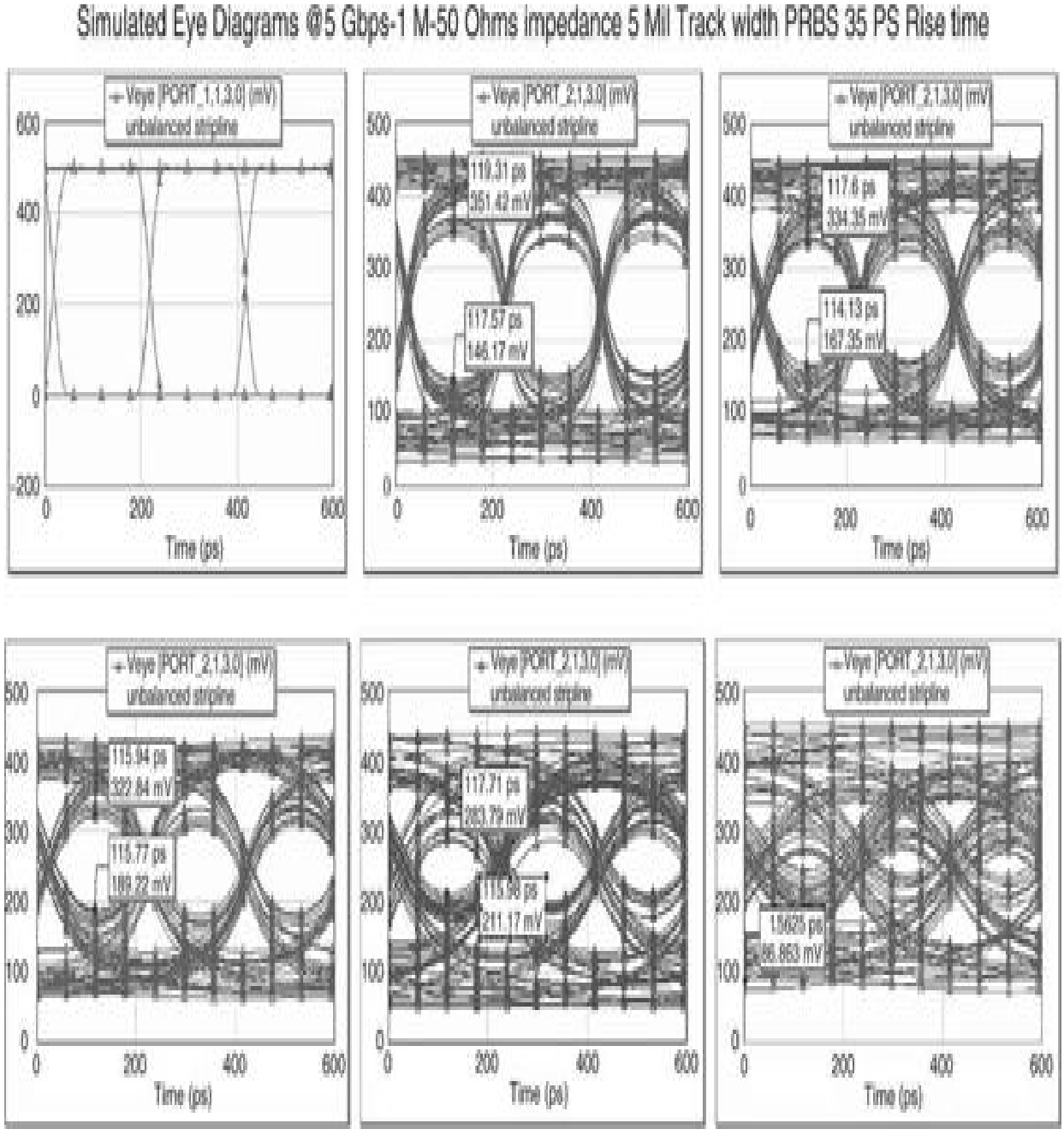


FIGURE 12.24 Simulated eye diagrams at 5 Gbps, 1 M, 50 Ω impedance, 5-mil track width.

Another way to illustrate the impact of D_f is to graph loss in decibels (dB) per unit length versus the D_f. Figure 12.25 provides a simulation of this relationship for a 5-mil line.

Because wider line widths are less “lossy” because of reduced skin effect, some of this can be compensated for by using a wider line. However, this negatively impacts circuit density. Figure 12.26 shows the impact of line width on loss for two different low D_k/D_f materials. In this case, material B would allow the designer to use a thinner line to increase circuit density while maintaining a given level of loss. For example, to keep the loss in this example below 15 dB/m, material A would require a line width of approximately 8 mils. However, with the same loss requirement, material B enables the line to be reduced to approximately 5 mils. This is a significant benefit in increasing circuit density.

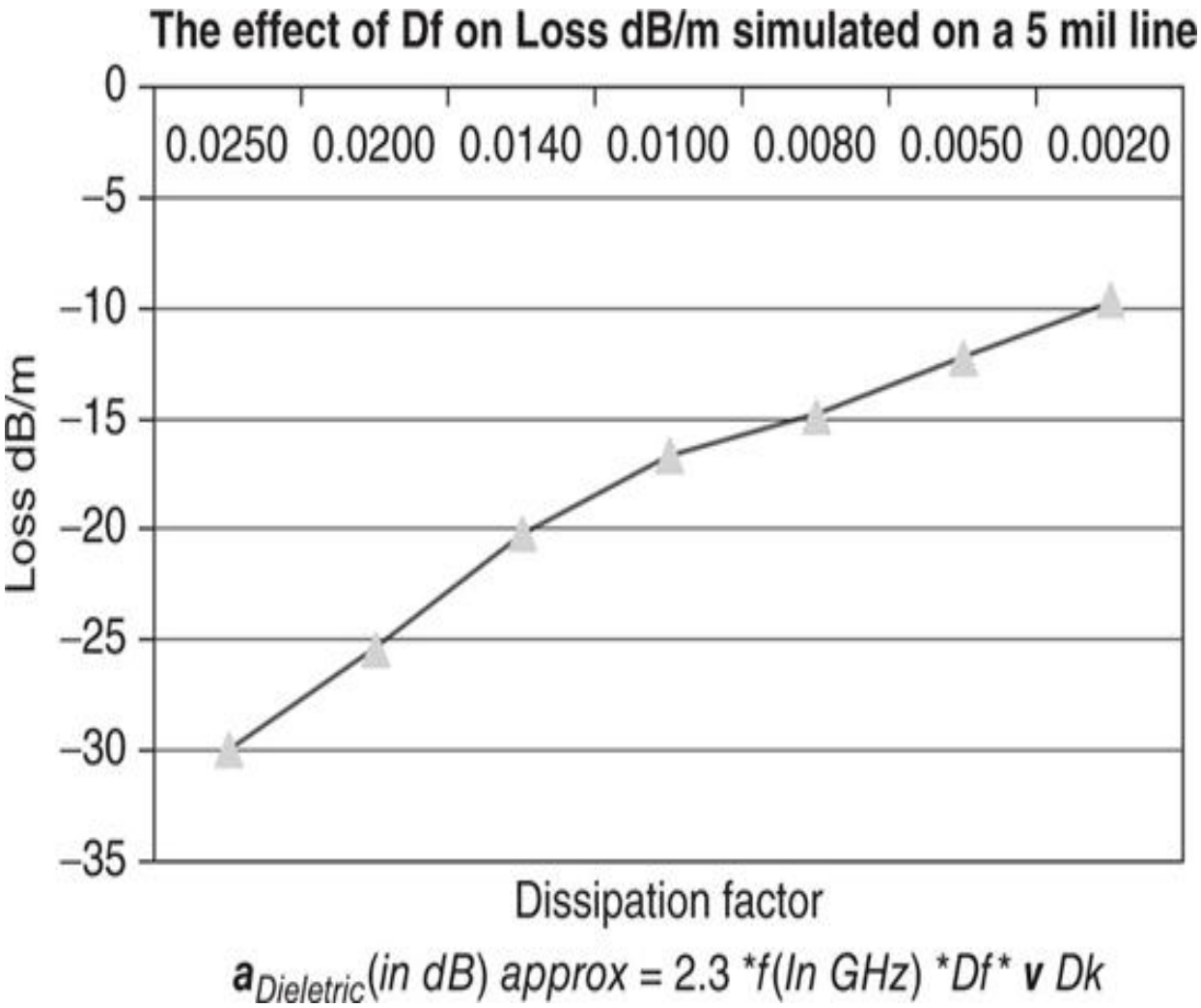


FIGURE 12.25 The effect of D_f on dielectric loss in dB/m simulated on a 5-mil line.

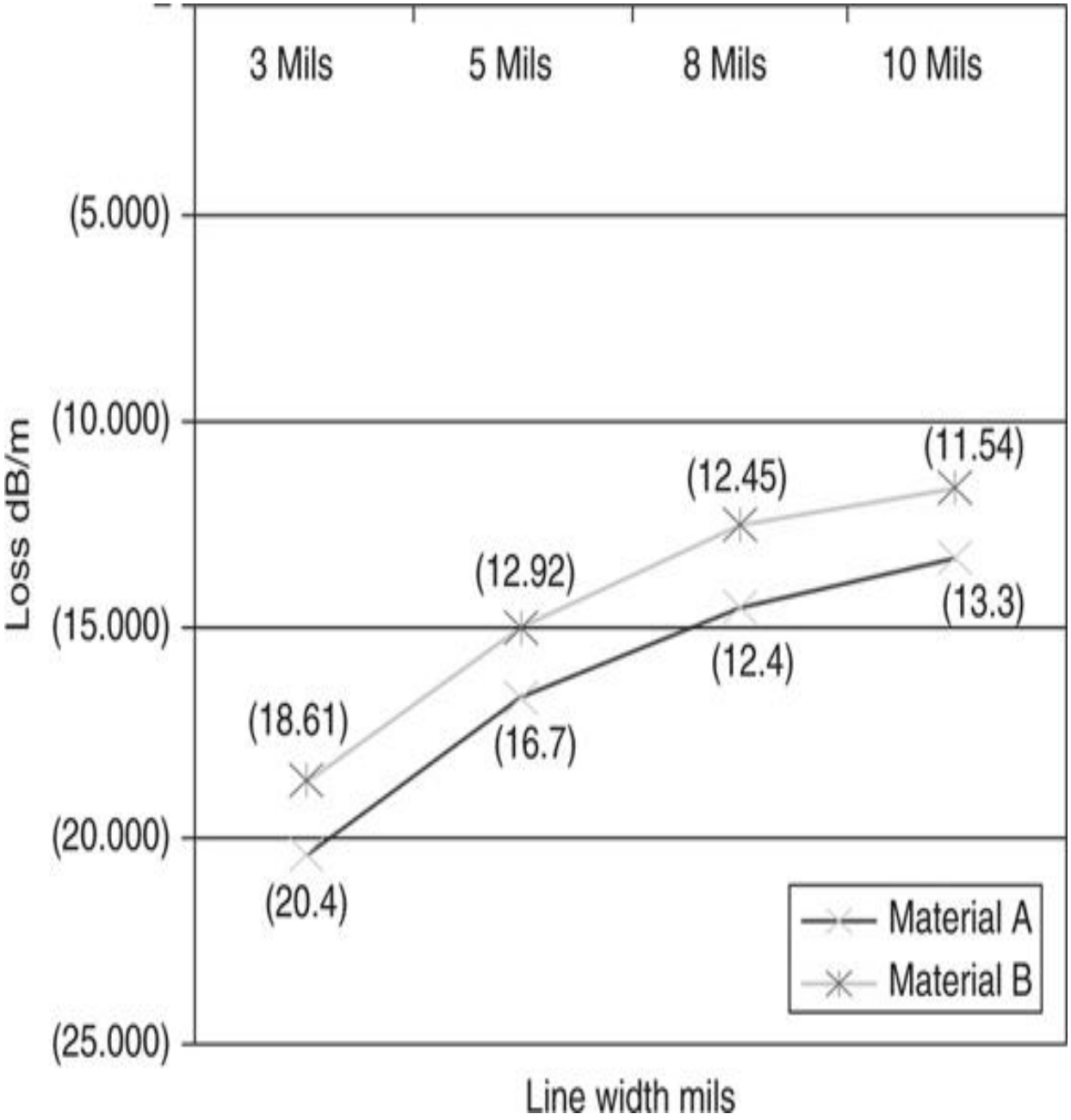


FIGURE 12.26 Effect of line width on loss for two material types.

12.9.3 Choosing a Base Material for Electrical Performance

The dielectric constant and dissipation factor of the dielectric material are determined by both the resin system and the reinforcement type. Therefore, each of these should be considered when choosing a material.

There are a large number of different low-dielectric, low-loss resin systems, most of which are proprietary resins only available from a single supplier. Likewise, a few different reinforcements and fillers are available that can be used to modify the electrical properties of the base material. Although E-glass is still the most commonly used fiberglass reinforcement, others are available and the use of low-D_k glass fabrics is growing rapidly. In addition, inorganic fillers are sometimes used to modify electrical properties as well. Table 12.4 provides electrical property data on some of the available fiberglass materials. Table 12.5 provides data on some of the base material composites available.

TABLE 12.4 Dielectric Constants and Dissipation Factors of Common Glass Types

Property	E-Glass	NE-Glass	L-Glass
Dielectric constant @ 1 GHz	6.8	4.8	4.8
Dielectric constant @ 10 GHz	6.6	4.8	4.8
Dissipation factor @ 1 GHz	0.004	0.0015	0.001
Dissipation factor @ 10 GHz	0.0066	0.0035	0.003

TABLE 12.5 Dielectric Constants and Dissipation Factors of Common Resin/Reinforcement Composites

Resin System	Reinforcement	D_k @ 1 MHz	D_k @ 1 GHz	D_f @ 1 MHz	D_f @ 1 GHz
Epoxy	E-Glass	4.4	3.9	0.020	0.018
Epoxy	Aramid fiber	3.9	3.8	0.024	0.020
Halogen-free epoxy	E-Glass	4.3	4.0	0.015	0.013
Epoxy/PPO	E-Glass	3.9	3.9	0.011	0.010
Modified epoxy	E-Glass	3.9	3.7	0.012	0.012
Epoxy blend	E-Glass	3.9	3.7	0.009	0.009
Epoxy blend	SI™-Glass	3.6	3.4	0.008	0.008
Low-loss blend	E-Glass	3.8	3.7	0.006	0.007
Very-low-loss blend	E-Glass	3.5	3.4	0.003	0.0036
Cyanate ester	E-Glass	3.8	3.7	0.008	0.011
Polyimide	E-Glass	4.3	3.9	0.014	0.015
APPE	E-Glass	3.7	3.4	0.005	0.007
PTFE	E-Glass	2.3	2.3	0.0013	0.0009
Hydrocarbon	E-Glass/Ceramic	3.4	3.3	0.0025	0.0024

Table 12.5 lists values for approximately 50 percent resin content. These values change as the resin content varies, with the magnitude of the change depending on the specific resin system. Also, comparable resin system types from various suppliers could differ. For example, since there are many types of epoxies, with a wide range of electrical properties, specific epoxy formulations from different material suppliers can exhibit somewhat different dielectric and loss properties. In addition, the test method used to

measure D_k and D_f, especially at higher frequencies, will have a significant impact on the reported value. When comparing materials, it is critical to compare values derived from the same test method, or at least to understand the differences in the test methods. The differences in test methods are beyond the scope of this chapter, but their importance should not be underestimated. The purpose of this table is to highlight the relative differences between various resin systems and reinforcement types. Chapter 15 will discuss this further.

A significant change since 2010 is the increase in functional testing being performed to assess electrical properties of different dielectric materials. These tests are standardized and are widely used in the industry. For higher frequencies, >10 GHz for example, or loss sensitive applications, these tests have been very useful for good decision making in selecting materials.

These values also vary with resin content and frequency. Figure 12.27 illustrates the dependence of the dielectric constant versus resin content for a few materials. Figure 12.28 shows the impact of resin content on the dissipation factor of an epoxy blend, and Fig. 12.29 shows the impact of frequency on D_k for a few of these materials. Beyond frequency and resin content effects, the dielectric constant and dissipation factor can also vary with temperature and moisture absorption.

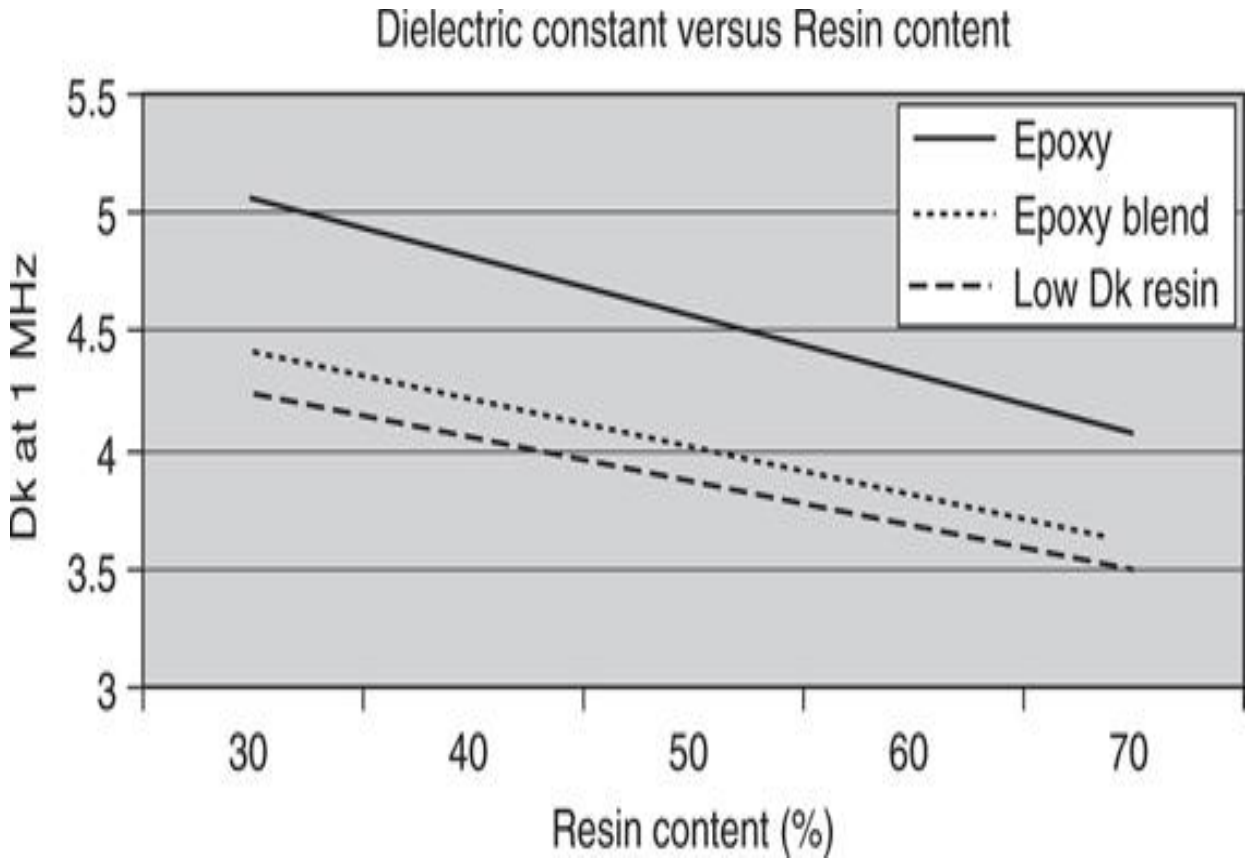


FIGURE 12.27 Dielectric constant versus resin content.

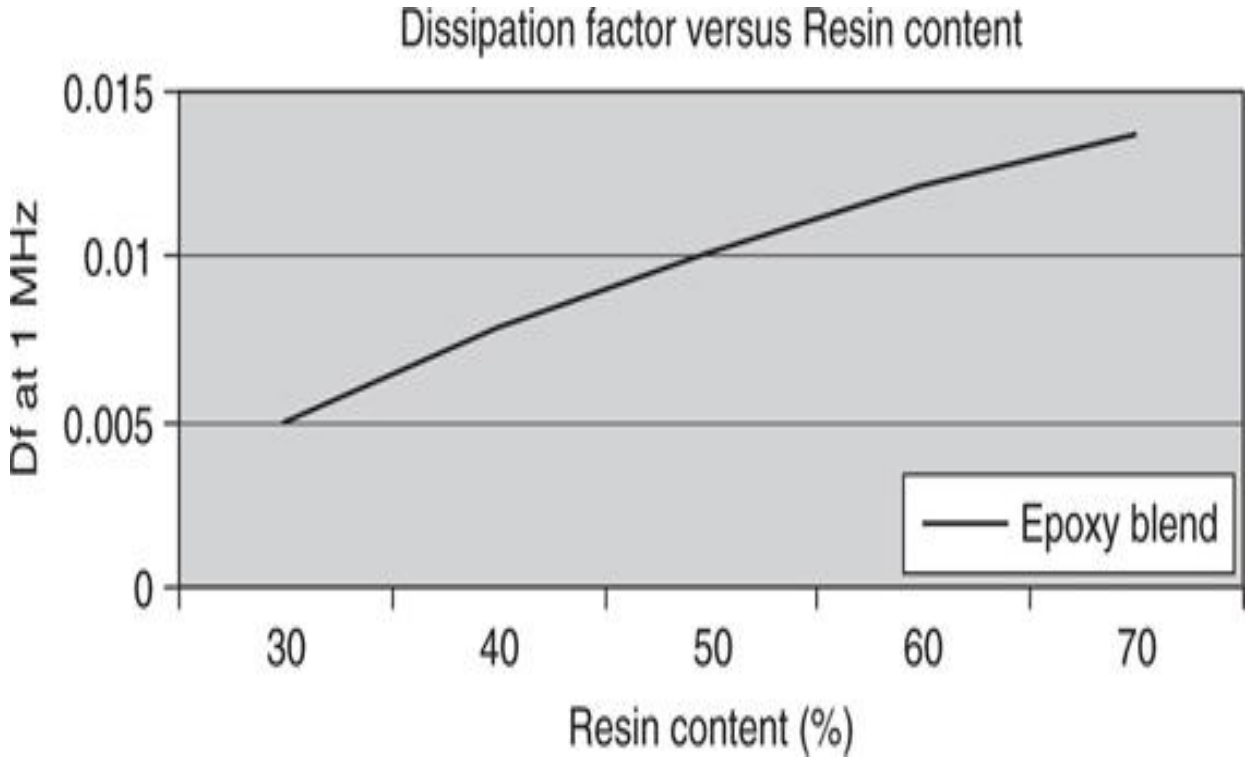


FIGURE 12.28 Dissipation factor versus resin content for a low D_k epoxy blend.

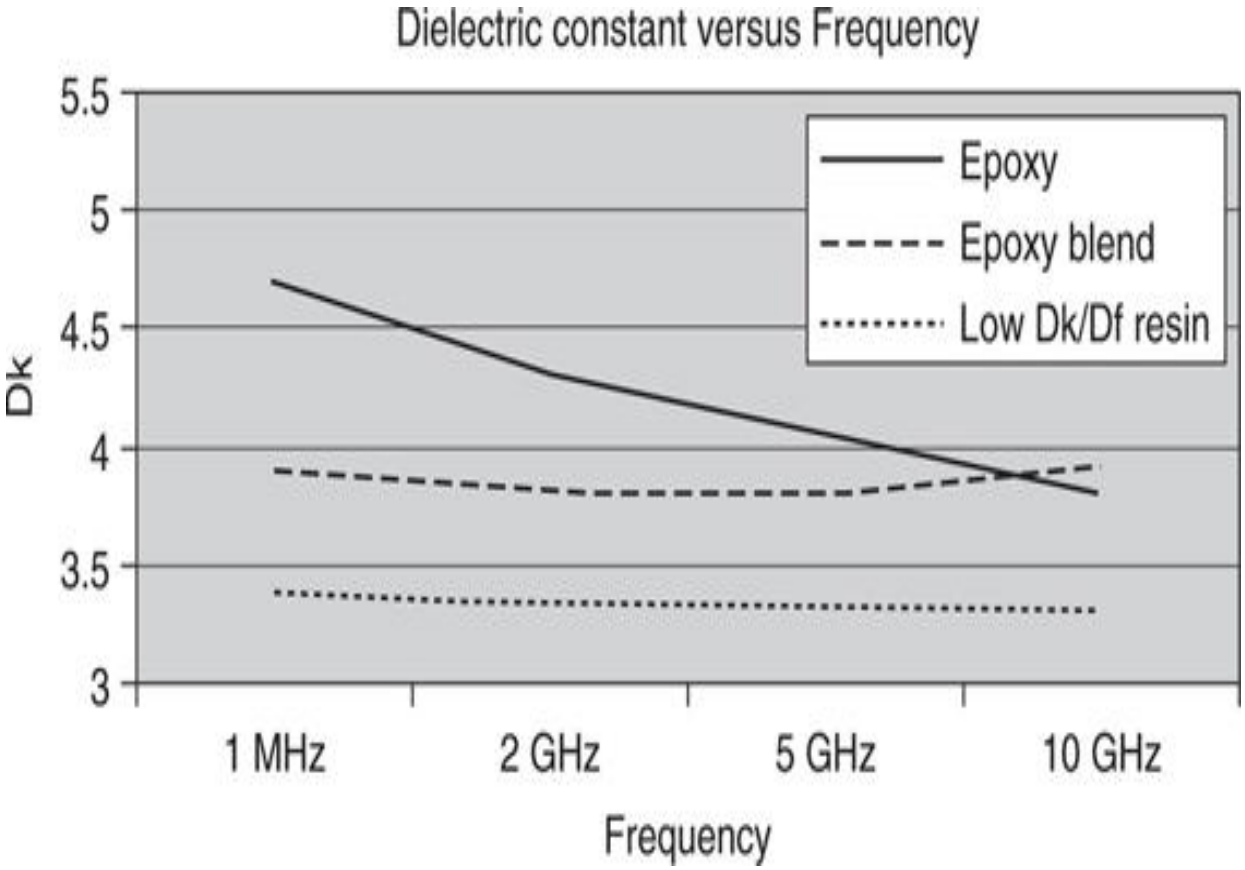


FIGURE 12.29 Dielectric constant versus frequency.

When choosing a material for a specific application, it is important to understand the operating conditions and environment in which the circuit will be used. Some resin systems exhibit less sensitivity to these conditions than others. For example, base material suppliers are continually developing resin systems to meet the demanding electrical properties requirements of high-speed and wireless applications, which include consistent properties over frequency ranges and environmental conditions. In short, different material types can have different responses to changes in frequency, resin content, temperature, and humidity conditions. These responses become more important to understand in high-speed, RF, and wireless applications.

In addition, when selecting a material, it is important not simply to select the material with the lowest dielectric constant or dissipation factor, since there are typically cost-performance trade-offs to be made. In general, the lower the dielectric constant and dissipation factor, the more costly the material, and very often the more difficult it is to process.

In summary, some general relationships include the following:

- The dielectric constant generally decreases with increasing resin content.
- The dissipation factor often increases with increasing resin content.
- The dielectric constant typically drops as frequency increases.
- The dielectric constant and dissipation factor typically increase as water absorption rises.
- The dielectric constant of E-glass is only mildly frequency-dependent and therefore lower resin contents result in less variation across frequencies.
- The dissipation factor generally rises with frequency, but may exhibit maxima at certain frequencies.

12.9.4 Electrical Performance of Lead-Free Compatible FR-4 Materials

Most of the FR-4 laminate materials developed for lead-free assembly applications use an alternative resin chemistry in comparison to the dicyandiamide (“dicy”) cured FR-4s used in the past. “Phenolic” or “novolac” cured epoxies are the most common of these materials. Although there is some variation between these materials, as a group they tend to exhibit somewhat different electrical performance compared to dicy-cured FR-4s. For most applications operating in lower

frequency ranges, the differences are not significant. However, as operating frequencies increase toward the higher end of “FR-4 applications,” and impedance control becomes more critical, these differences can become significant. Table 12.6 includes two common dicy-cured FR-4 materials (A and C) and two phenolic FR-4 materials compatible with many lead-free assembly applications (B and D). It also includes a lead-free compatible material (E) designed to improve D_k and D_f performance in comparison to the “phenolic” lead-free compatible materials. Note that different types of measurement systems can result in different measured values for D_k and D_f. Laminate resin contents and other factors also influence these properties. Thus, in Table 12.6 the comparisons between these materials are more important than the absolute values reported for each material. For these comparisons, the same measurement system and resin contents were used.

TABLE 12.6 Properties of Several Base Material Types

Product	Description	Glass Transition Temp., °C	Decomp. Temp., °C	% Expansion, 50–260°C (40% RC)	D_k @ 2 GHz	D_k @ 5 GHz	D_f @ 2 GHz	D_f @ 5 GHz
A	Dicy-cured, 140°C T_g FR-4	140	320	4.2	3.9	3.8	0.021	0.022
B	Phenolic, mid-T_g FR-4	150	335	3.4	4.0	3.9	0.026	0.027
C	Dicy-cured, high-T_g FR-4	175	310	3.5	3.8	3.7	0.020	0.021
D	Phenolic, high-T_g FR-4	175	335	2.8	3.9	3.8	0.026	0.026
E	Nondicy, nonphenolic	200	370	2.8	3.7	3.7	0.013	0.014

In Table 12.6, the improved phenolic FR-4 materials are clearly not as good in terms of electrical performance at

higher frequencies as the dicy-cured materials used in the past, particularly with respect to D_f. However, material E exhibits thermal properties comparable to the phenolic materials. In addition, the electrical performance of material E is even better than the dicy-cured materials, especially in terms of D_f performance. Figures 12.30 and 12.31 provide higher frequency D_f and D_k data for several lead-free compatible FR-4 materials in comparison to a dicy-cured, high-T_g FR-4, using a split-post resonant cavity test method. It also includes data for the nondicy/nonphenolic material. Note that there is a wide range of D_f values for the phenolic materials, and to a lesser extent some variation in D_k values as well. In comparison, the nondicy/nonphenolic material offers lower and more stable D_f properties and a slightly lower D_k.

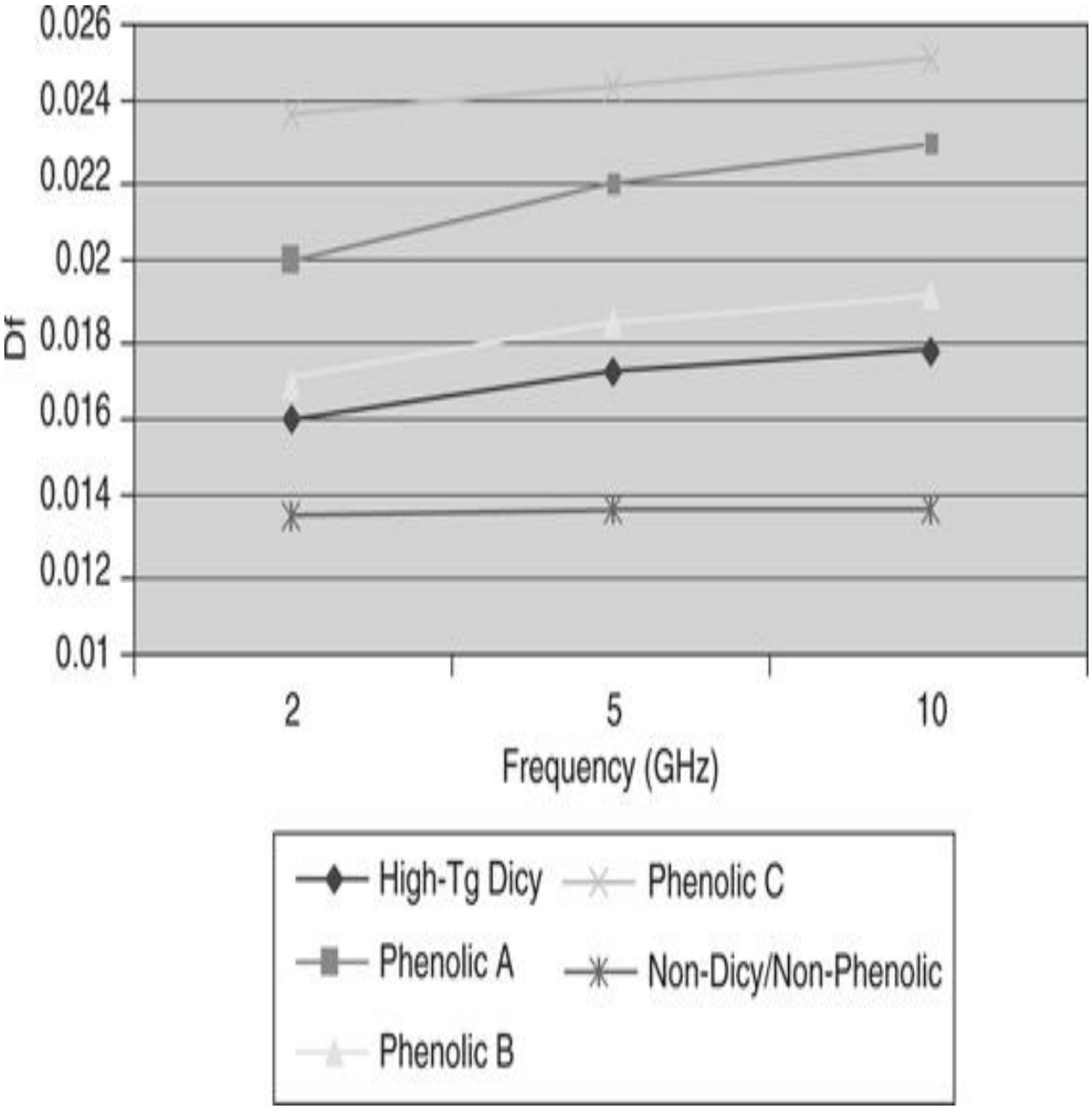


FIGURE 12.30 D_f versus frequency for lead-free compatible FR-4 materials.

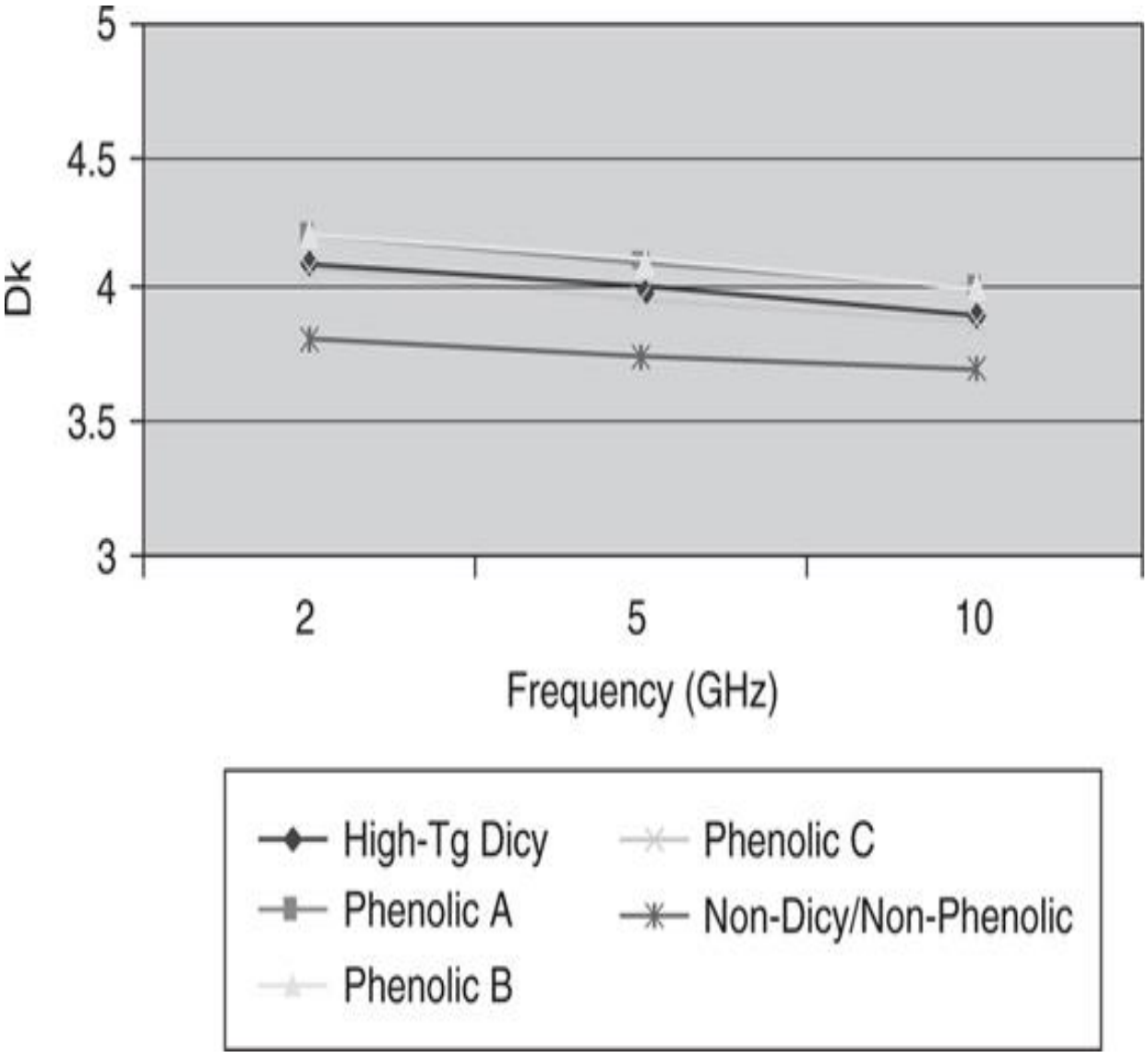


FIGURE 12.31 D_K versus frequency for lead-free compatible FR-4 materials.

Furthermore, Table 12.7 provides several laminate constructions for a common phenolic material, along with resin content and D_k data at 2 and 5 GHz. Note how different constructions and resin contents can vary in D_k. Table 12.8 provides the same construction data with D_f data at 2 and 5 GHz. Tables 12.9 and 12.10 provide this same data for the nondicy/nonphenolic material with additional data at 10 GHz.

TABLE 12.7 Laminate Constructions and D_K Data for a Common Phenolic FR-4

Core Thickness	Standard Construction	Resin Content	D_k @ 2.0 GHz	D_k @ 5.0 GHz
0.0025	1-1080	58	3.72	3.65
0.0030	1-2113	44	4.04	3.98
0.0035	2-106	65	3.58	3.50
0.0040	1-2116	45	4.02	3.96
0.0050	1-1652	42	4.10	4.04
0.0060	1080/2113	53	3.83	3.76
0.0070	1-7628	41	4.12	4.07
0.0070	2-2113	51	3.87	3.81
0.0080	2-2116	45	4.02	3.96
0.0095	2-2116	52	3.85	3.78
0.0100	2-1652	42	4.10	4.04
0.0120	2-1080/7628	47	3.97	3.91
0.0140	2-7628	41	4.12	4.07

TABLE 12.8 Laminate Constructions and D_f Data for a Common Phenolic FR-4

Core Thickness	Standard Construction	Resin Content	D_f @ 2.0 GHz	D_f @ 5.0 GHz
0.0025	1-1080	58	0.026	0.027
0.0030	1-2113	44	0.021	0.022
0.0035	2-106	65	0.028	0.029
0.0040	1-2116	45	0.021	0.027
0.0050	1-1652	42	0.020	0.021
0.0060	1080/2113	53	0.024	0.025
0.0070	1-7628	41	0.020	0.021
0.0070	2-2113	51	0.023	0.024
0.0080	2-2116	45	0.021	0.027
0.0095	2-2116	52	0.024	0.025
0.0100	2-1652	42	0.020	0.021
0.0120	2-1080/7628	47	0.022	0.023
0.0140	2-7628	41	0.020	0.021

TABLE 12.9 Laminate Constructions and D_K Data for a Non-Dicy/Non-Phenolic Material

Core Thickness	Standard Construction	Resin Content	D_k @ 2.0 GHz	D_k @ 5.0 GHz	D_k @ 10.0 GHz
0.0020	1-106	70	3.40	3.38	3.37
0.0025	1-1080	57	3.67	3.66	3.65
0.0030	1-1080	63	3.54	3.53	3.52
0.0035	1-2113	51	3.82	3.80	3.80
0.0035	2-106	65	3.50	3.48	3.48
0.0040	1-3070	49	3.87	3.85	3.85
0.0040	1-2116	45	3.97	3.96	3.95
0.0045	1-2116	49	3.87	3.85	3.85
0.0050	1-1652	42	4.06	4.04	4.03
0.0060	1080/2113	53	3.77	3.76	3.75
0.0070	1-7628	40	4.12	4.10	4.09
0.0070	2-2113	51	3.82	3.80	3.80
0.0080	2-2116	45	3.97	3.96	3.95
0.0100	2-1652	42	4.06	4.04	4.03
0.0120	2-1080/7628	47	3.92	3.91	3.90
0.0140	2-7628	40	4.12	4.10	4.09

TABLE 12.10 Laminate Constructions and D_f Data for a Nondicy/Nonphenolic Material

Core Thickness	Standard Construction	Resin Content	D_f @ 2.0 GHz	D_f @ 5.0 GHz	D_f @ 10.0 GHz
0.0020	1-106	70	0.0151	0.0154	0.0154
0.0025	1-1080	57	0.0136	0.0139	0.0139
0.0030	1-1080	63	0.0143	0.0146	0.0146
0.0035	1-2113	51	0.0130	0.0132	0.0132
0.0035	2-106	65	0.0145	0.0148	0.0148
0.0040	1-3070	49	0.0122	0.0130	0.0130
0.0040	1-2116	45	0.0121	0.0125	0.0125
0.0045	1-2116	49	0.0122	0.0130	0.0130
0.0050	1-1652	42	0.0110	0.0122	0.0122
0.0053	106/2113	56	0.0135	0.0138	0.0138
0.0060	1080/2113	53	0.0132	0.0134	0.0134
0.0070	1-7628	40	0.0104	0.0119	0.0119
0.0070	2-2113	51	0.0130	0.0132	0.0132
0.0080	2-2116	45	0.0123	0.0125	0.0125
0.0100	2-1652	42	0.0111	0.0120	0.0120
0.0120	2-1080/7628	47	0.0125	0.0127	0.0127
0.0140	2-7628	40	0.0114	0.0119	0.0119

12.10 ELECTRICAL PERFORMANCE OF LOWER D_K/D_F LEAD-FREE

COMPATIBLE MATERIALS

However, for performance at very high frequencies, lower D_k/D_f materials are preferred. While low D_k/D_f materials have been available for many years, the advent of lead-free assembly has complicated material selection, and in these applications not only are the laminate D_k and D_f properties critical, but their thermal properties are just as important. Many new lead-free compatible materials are available with differing electrical performance. Figures 12.32 and 12.33 provide D_f and D_k data for three different low D_k/D_f materials that are also compatible with lead-free assembly.

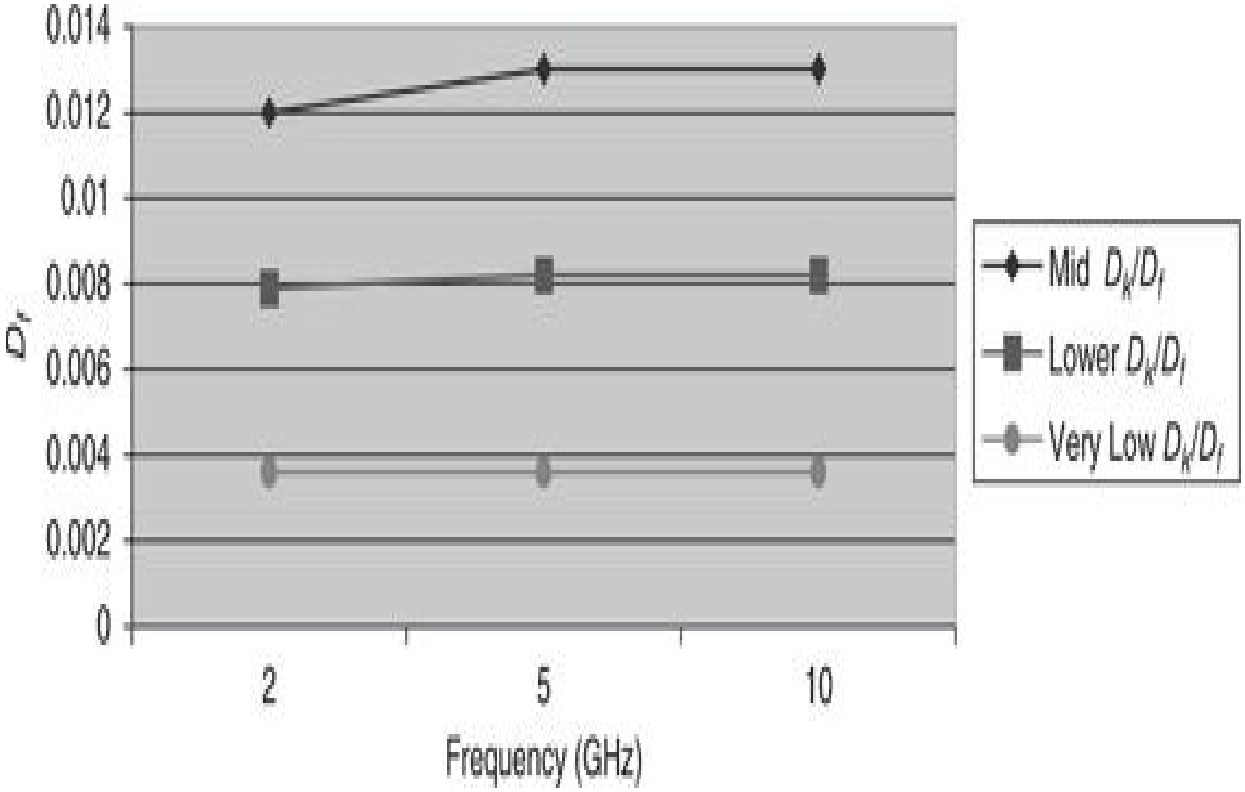


FIGURE 12.32 D_f versus frequency for low D_k/D_f, lead-free compatible materials.

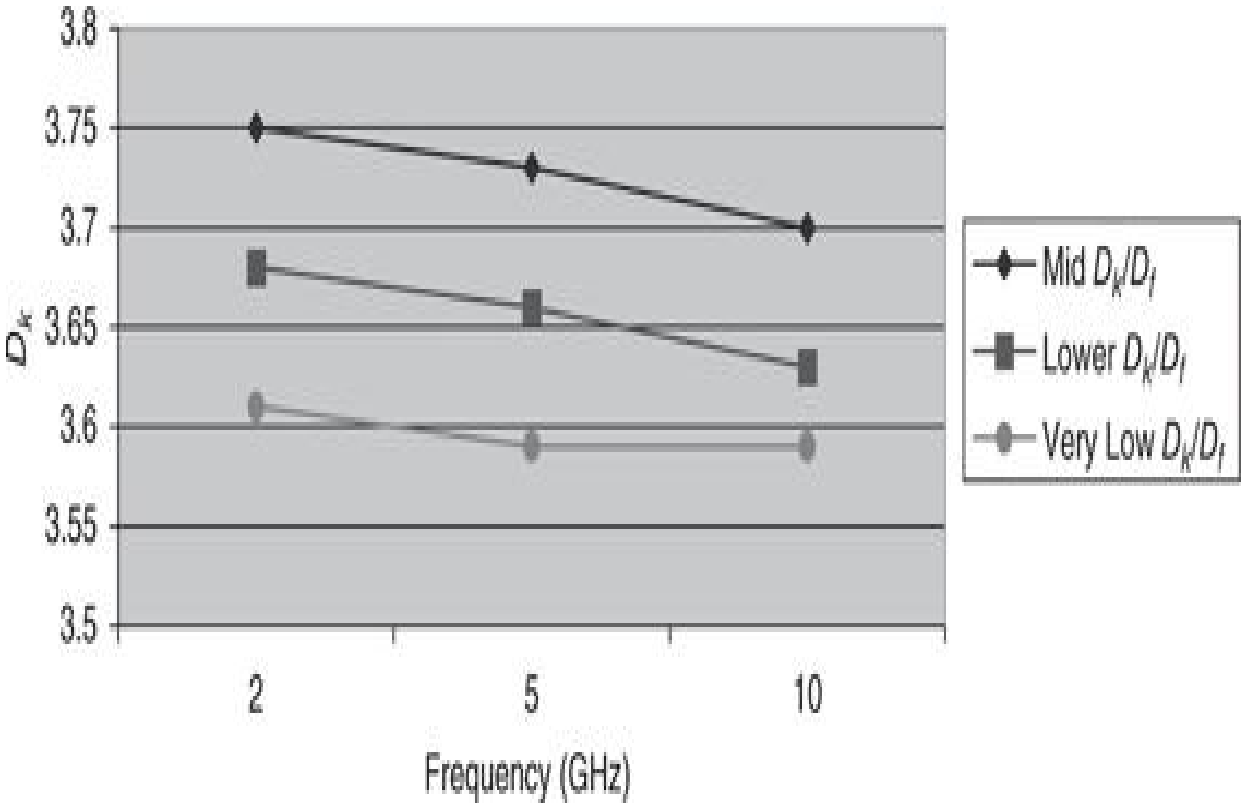


FIGURE 12.33 D_k versus frequency for low D_k/D_f, lead-free compatible materials.

Table 12.11 provides D_k and D_f data for the very low D_k/D_f material by construction and resin content. This sample of constructions illustrates how these properties vary with resin content in addition to frequency. For a full list of constructions available for any product, it is recommended that the manufacturer's data sheets be consulted.

TABLE 12.11 Laminate Constructions and D_k Data for a Low D_k/D_f Material

Thickness, in	Construction	Resin Content, %	D_k @ 2 GHz	D_k @ 5 GHz	D_k @ 10 GHz	D_f @ 2 GHz	D_f @ 5 GHz	D_f @ 10 GHz
0.0020	1-106	70	3.28	3.24	3.24	0.0058	0.0066	0.0072
0.0027	1-1080	60	3.51	3.47	3.47	0.0059	0.0066	0.0071
0.0030	1-1080	63	3.44	3.40	3.40	0.0059	0.0066	0.0071
0.0035	1-2113	51	3.73	3.70	3.70	0.0060	0.0066	0.0070
0.0040	1-3070	49	3.78	3.75	3.75	0.0060	0.0066	0.0070
0.0043	106/1080	62	3.46	3.42	3.42	0.0059	0.0066	0.0072
0.0050	106/2113	55	3.63	3.59	3.59	0.0060	0.0066	0.0071
0.0060	1080/2113	54	3.65	3.62	3.62	0.0060	0.0066	0.0071
0.0070	2-2113	52	3.70	3.67	3.67	0.0060	0.0066	0.0071
0.0080	2-3070	49	3.78	3.75	3.75	0.0061	0.0066	0.0070

12.11 RESIN AND GLASS MICRO-D_k EFFECTS

Another issue in high-speed circuits using differential pairs of conductors is skew, which we will describe shortly. Skew can arise from the differences in resin D_k versus glass cloth D_k when pairs of conductors are patterned in glass-rich areas of the dielectric versus resin-rich areas. The potential for skew arises from materials with large differences between the resin D_k and glass D_k, in dielectrics that contain glass cloth styles with large open areas between the yarns that make up the cloth.

Figure 12.27 provided an example of how D_k can vary with resin content, and Tables 12.7, 12.9, and 12.11 gave examples of laminate constructions with different resin contents, and the subsequent differences in D_k. This illustrates the potential D_k differences, although the D_k of E-glass and the D_k of most resins will have even larger differences. Now examine Figs. 12.34 and 12.35, which provide photographs of 106 and 1067, and 1080 and 1086, respectively.

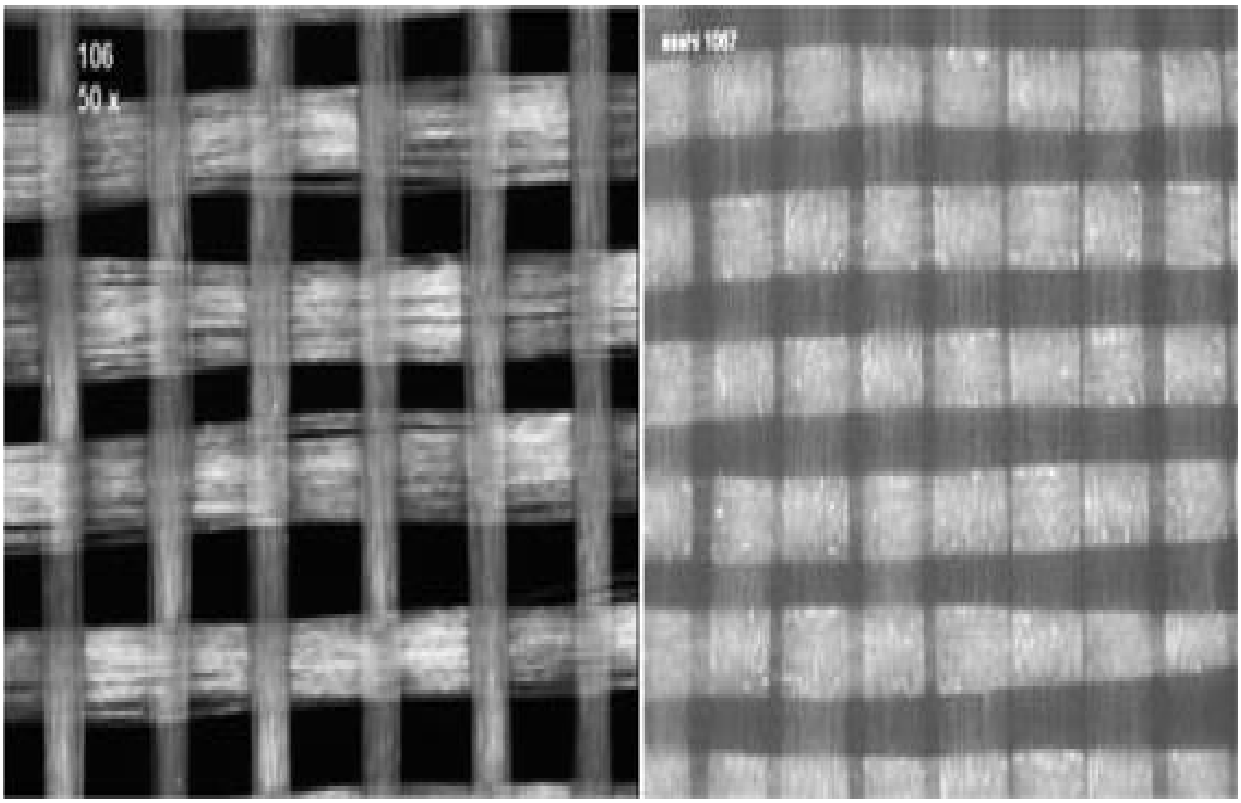


FIGURE 12.34 106 and 1067 Glass fabrics.

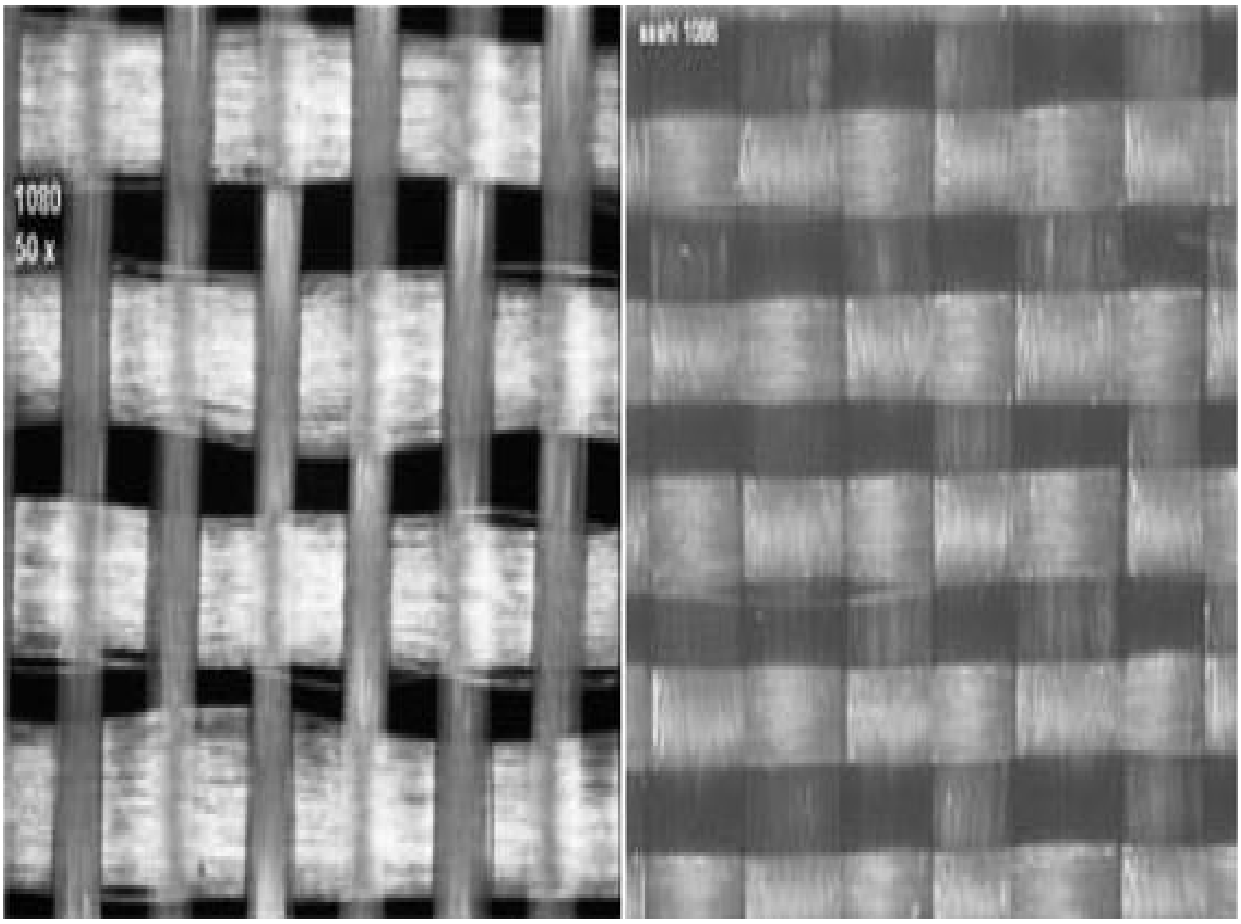


FIGURE 12.35 1080 and 1086 Glass fabrics.

In these figures you can see that 106 and 1080 glass cloth contain much open space between yarns. In Chap. 11, we discussed both spread and expanded glass cloths, and the 1067 and 1086 in these figures are examples. With spread and expanded glass cloths the filaments in the yarns are more homogeneously distributed. Now particularly in dielectrics that use glass fabrics with large open areas, conductors may be placed along glass yarns, in areas with much open space between yarns, or overlapping these areas. In PCB designs using differential pairs of conductors, it is critical that signals in the two conductors travel at the same speed, which is impacted by the D_k of the dielectric material. Skew refers to the difference in time that signals in the differential pair of conductors reach the receiver. If this

difference in time is large enough, then this leads to data errors. Figure 12.36 illustrates the potential for conductors to be imaged in glass-rich versus resin-rich areas. In Fig. 12.37 is an eye pattern without skew for a 2.5 Gb/S differential pair. Note the equal magnitude and opposite value at any time. In contrast, Figs. 12.38 and 12.39 are eye patterns with 40 picoseconds (ps) and 80 ps skew. Note how the eye closes as skew increases.

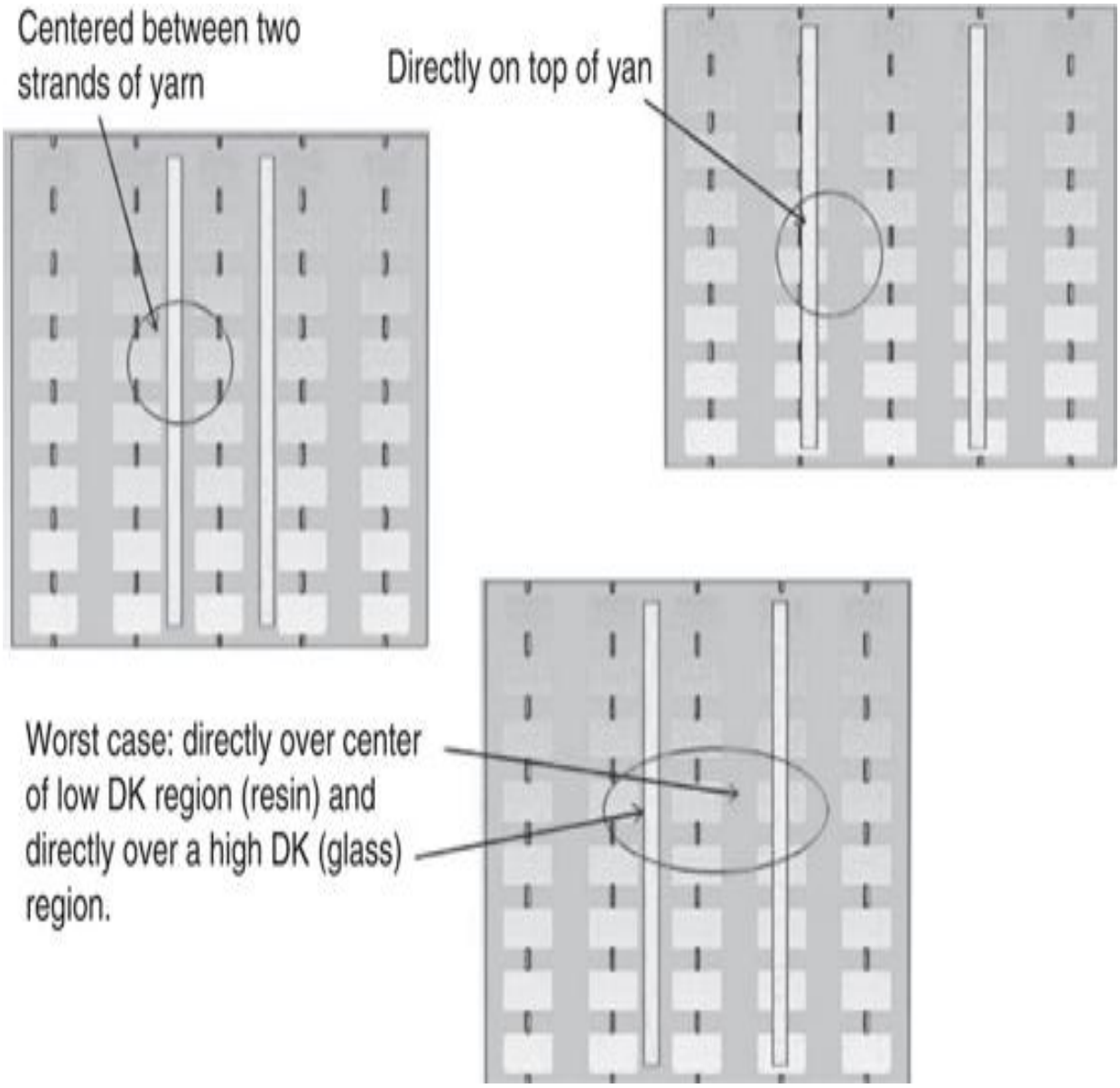


FIGURE 12.36 Illustration of conductors in glass-rich versus resin-rich areas.

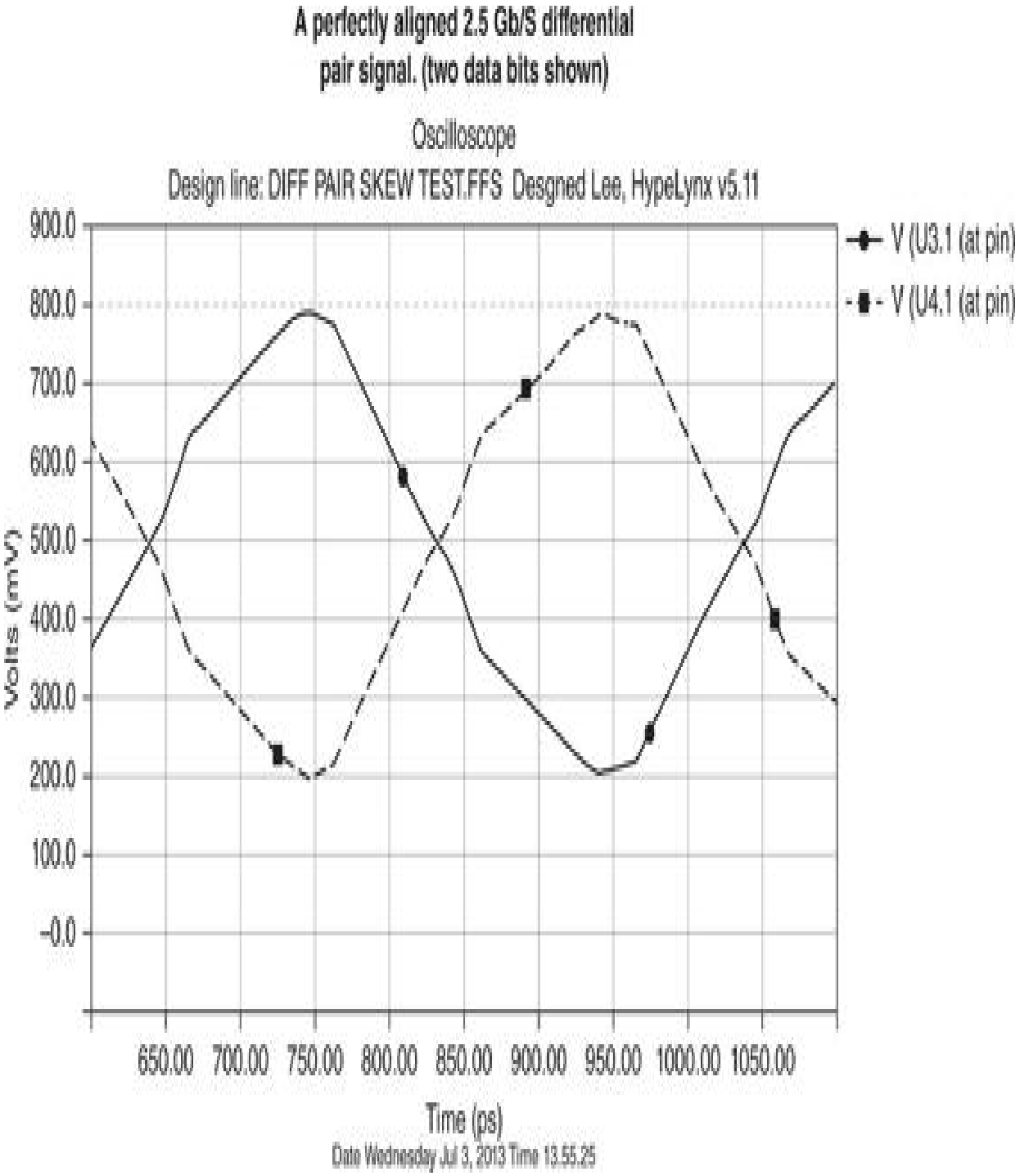


FIGURE 12.37 Eye pattern without skew.

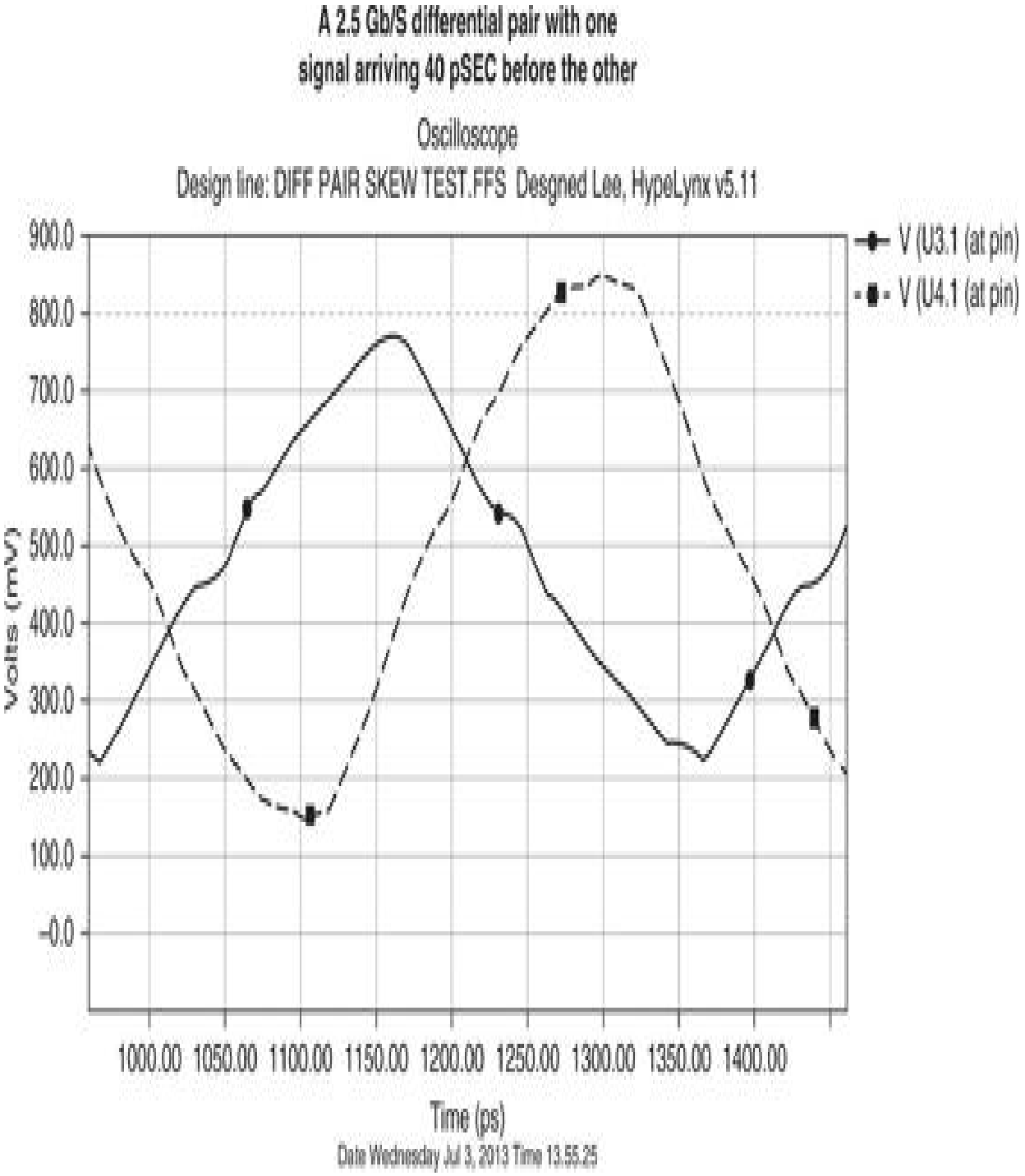


FIGURE 12.38 Eye pattern with 40 ps skew.

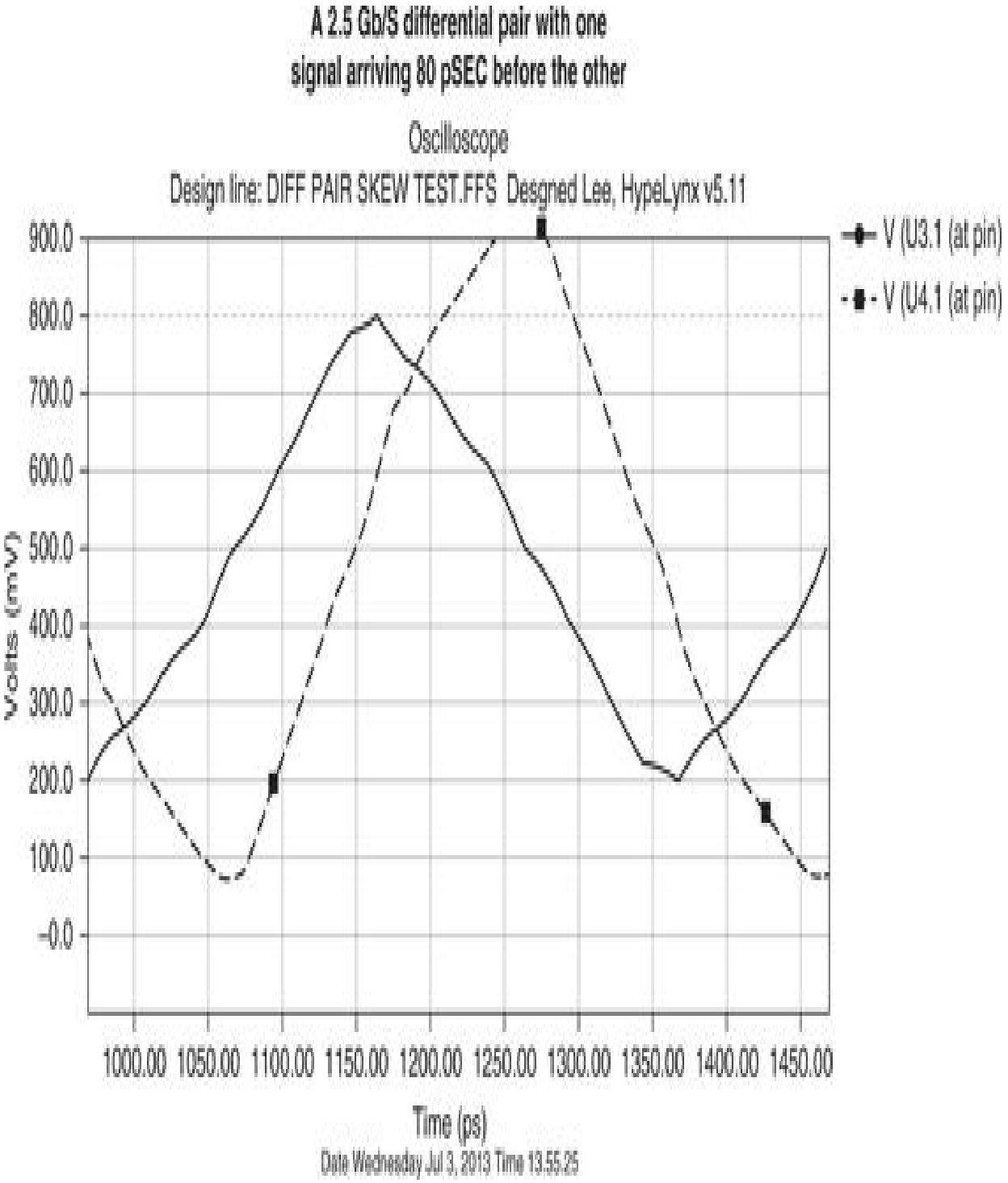


FIGURE 12.39 Eye pattern with 80 ps skew.

Skew has become a significant issue for very high speed PCB design, and there are a few ways that this has been addressed. Examples are

- The use of the expanded and spread glass cloth styles helps to mitigate some of the issue since this helps provide a more uniform distribution of resin and glass. These cloth styles generally cost more than the nonspread/nonexpanded glass cloths, so the benefit needs to be assessed versus the cost.
- The use of low-D_k glass cloth can help reduce the difference in D_k between resin and glass. Low-D_k glass cloth is more expensive than E-glass, and again presents a cost-benefit trade-off.
- Circuits can be rotated relative to the glass fabric so that conductors do not travel in-line with the yarns in the glass fabric. Normally this is achieved by imaging circuits at an angle relative to the length and width of the copper clad laminate. The cost of this approach depends on the size of the circuit relative to the size of the copper clad laminate, but the added cost can be very high if the circuit rotation reduces the number of circuits that can be imaged on the laminate, or if rotating requires a circuit to be built using a larger laminate size.
- Materials have been developed where there is very little difference in D_k between resin and glass and therefore across resin contents. In addition to the low skew that these products enable, this simplifies design of the laminate and prepreg styles used throughout the multilayer stack-up since they are uniform in D_k. Table 12.12 provides a few examples of core constructions with different resin contents, along with the D_k.

TABLE 12.12 Laminate Construction Examples for a Low Skew Material

Thickness, in	Construction	Resin Content, %	D_k @ 2 GHz	D_k @ 5 GHz	D_k @ 10 GHz	D_f @ 2 GHz	D_f @ 5 GHz	D_f @ 10 GHz
0.0025	1-1067	75	4.12	4.12	4.12	0.0054	0.0063	0.0070
0.0030	1-1078	69	4.12	4.12	4.12	0.0054	0.0062	0.0069
0.0035	1-3313	56	4.13	4.13	4.13	0.0053	0.0060	0.0066
0.0040	1-3313	61	4.13	4.13	4.13	0.0054	0.0061	0.0067
0.0040	2-1035	70	4.12	4.12	4.12	0.0054	0.0062	0.0069
0.0045	1-2116	57	4.13	4.13	4.13	0.0053	0.0060	0.0066
0.0050	1-2116	60	4.13	4.13	4.13	0.0054	0.0061	0.0067
0.0060	2-1078	69	4.12	4.12	4.12	0.0054	0.0062	0.0069
0.0070	2-3313	56	4.13	4.13	4.13	0.0053	0.0060	0.0066
0.0080	2-3313	61	4.13	4.13	4.13	0.0054	0.0061	0.0067

12.12 REFERENCES

1. IPC-4562 Metal Foil for Printed Wiring Applications.
2. Brist, Gary, Hall, Stephen, Clouser, Sidney, and Liang Tao, “Non-Classical Conductor Losses Due to Copper Foil Roughness and Treatment,” ECWC 10/IPC Expo 2005.
3. IPC-4101, “Specification for Base Materials for Rigid and Multilayer Printed Boards.”
4. Isola Group Product Reference & Technical Materials.
5. IPC-TM-650 Test Methods Manual.

CHAPTER 13

THE IMPACT OF LEAD-FREE ASSEMBLY ON BASE MATERIALS

Edward Kelley
Douglas Trobough
Isola Group, Chandler, Arizona

13.1 INTRODUCTION

The European Union's Restriction of Hazardous Substances (RoHS) directive has had a profound impact on all levels of the electronics industry supply chain, including the base materials used in printed circuit boards (PCBs). While debate over the net environmental benefits of this initiative continues, it is clear that all levels of the supply chain must continue to deal with the implications. Product groups with exemptions are approaching deadlines, and indeed, many of these product groups were, or are being forced to transition ahead of schedule due to component availability and constraints within the assembly services industry. The product groups granted initial exemptions are generally those with the most stringent reliability requirements, and

many involve complex PCB designs that even further complicate the issues with respect to base materials. This chapter will introduce the key issues related to base materials, the important properties with respect to lead-free assembly compatibility, and examples of material evaluation.

13.2 RoHS BASICS

RoHS restricts the use of

- Lead (Pb)
- Cadmium (Cd)
- Mercury (Hg)
- Hexavalent chromium (Cr^{VI})
- Polybrominated biphenyl (PBB)
- Polybrominated diphenyl ethers (PBDE)

The first four substances are metals used for a variety of applications, whereas the last two are generally used as flame retardants in plastic materials. It is important to note that these halogenated flame retardants are not generally used in laminate materials for printed circuits.

Chapter 11 discussed flame retardants in more detail. The key point to be made here is that the most common flame retardant used in base materials, tetrabromobisphenol-A (TBBPA), is not restricted. Furthermore, in FR-4 materials, TBBPA is generally reacted into one of the epoxy resins, and thus does not exist as a free-standing molecule, but is incorporated into the molecular backbone of the resin system.

The metals that are restricted are not used in base materials either. So from the standpoint of compliance, most laminate materials are acceptable. The key issue is the

restriction on the use of lead, and the implications that this has for assembly of components onto PCBs. Eutectic tin/lead (Sn/Pb) has been the primary solder alloy used in assembly of printed circuits, and has a melting point of 183°C. Peak assembly temperatures using eutectic tin/lead commonly reach 230 to 235°C. With the elimination of lead from electronics assembly, alternative solder alloys have been developed. These lead-free alloys have higher melting points. Tin/silver/copper (Sn/Ag/Cu) alloys, also called “SAC” alloys, are the most common lead-free solder alternatives, with the most common of these alloys having melting points around 217°C and peak assembly temperatures of up to 260°C. Assembly rework temperatures can be even higher. It is the increase in temperature to which PCBs are exposed to that is the primary issue with respect to base materials. In other words, the issue for base materials is not compliance with the restriction on the banned substances, but compatibility with the manufacturing processes and temperatures used.

13.3 BASE MATERIAL COMPATIBILITY ISSUES

The question of base material compatibility is very complex. This is the result of several factors. First, PCB design and construction have a significant impact on the base material properties required. Thin, low-layer-count PCBs may have different requirements than very thick, high-layer-count PCBs. Copper weights, aspect ratios, PTH-to-PTH pitch and other design features also have an impact. End-use application and the associated requirement for long-term reliability and electrical performance also impacts the decision-making process. The requirements for a cell phone, video game, or even a computer motherboard are very

different than those for high-end servers, telecommunications gear, avionics, and critical medical and automotive electronics. Finally, not all lead-free assembly processes are the same. Some designs experience peak temperatures of around 245°C, whereas others experience peak temperatures of up to 260°C, or even higher in some cases. Some PCBs may experience two to three thermal cycles, others up to five, six, or even more depending on how many reworks are allowed. All of this makes it impossible to recommend one base material type for all applications without either underspecifying the laminate material and risking defects during assembly or later on in the field, or over-specifying the material and paying too much for the material or limiting availability.

Beyond the complexity introduced by the PCB design and construction, there are fundamentally two issues:

1. Surviving lead-free assembly processes without defects
2. Maintaining the required level of long-term reliability for the given application

The critical base material properties required for each are summarized here, and discussed in more detail later in this chapter.

13.3.1 Surviving Lead-Free Assembly without Defects

The primary defects related to base materials that can occur during lead-free assembly include measling, blistering, or delamination. These defects are related to the thermomechanical properties of the base material, the decomposition properties of the material, as well as the interaction of these properties with any absorbed moisture that may be contained within the PCB during assembly,

which can be volatilized as the PCB is heated. Fundamentally, these defects represent either the creation of voids within the PCB due to the volatilization of moisture, retained solvents, other organic components including the by-products of resin decomposition, or the loss of adhesion between the fundamental base material components: glass cloth, resin system, and copper. The adhesion loss and subsequent blistering or delamination may be the result of pressure from volatilized components, mismatches between component thermal expansion rates, degradation of the components at the interfaces, or combinations of these factors. Figure 13.1 is an example of delaminations within a PCB after lead-free assembly processing. This PCB used a dicyandiamide (dicy) cured, high-T_g FR-4 base material. The left and right-side images in this figure are from the same area of the PCB, but photographed with different lighting to highlight the specific interfaces where delamination occurred.

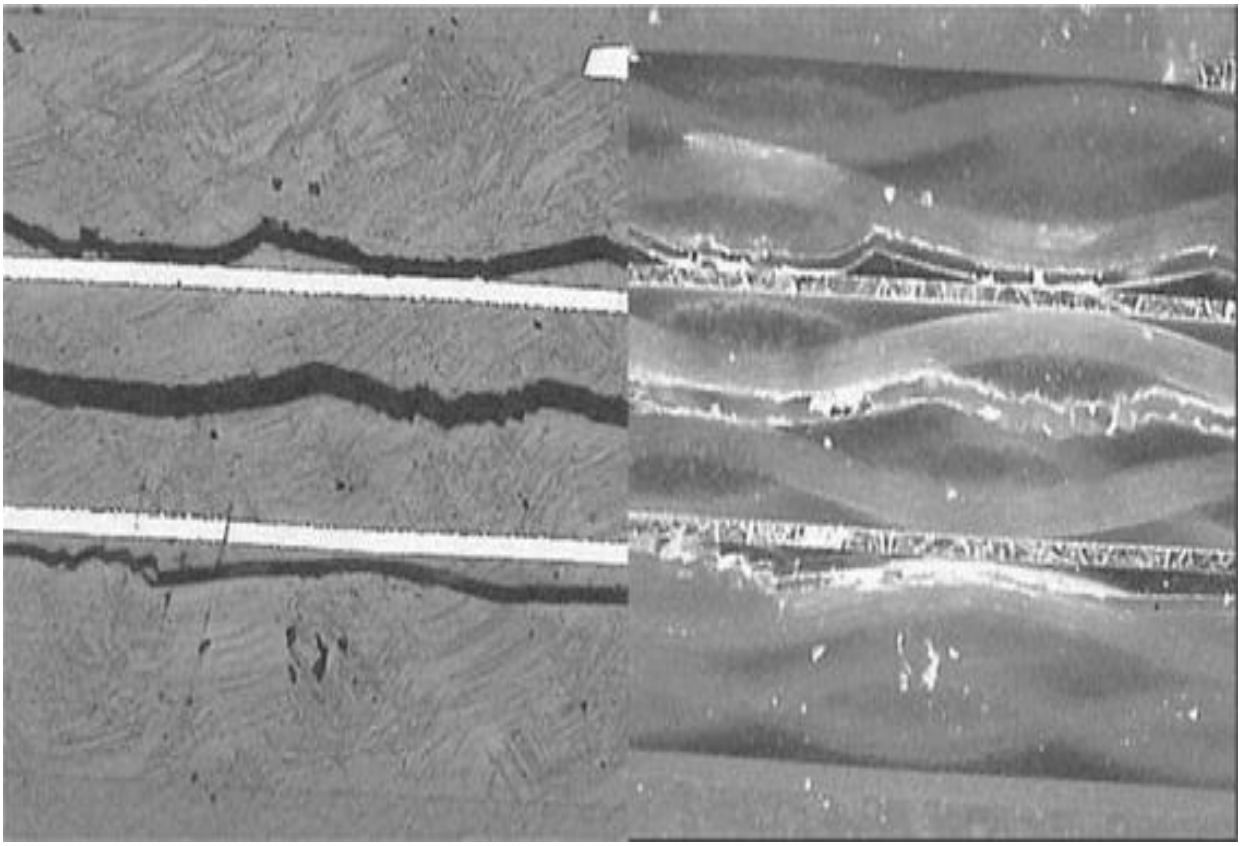


FIGURE 13.1 PCB delamination after lead-free assembly.

Among the key base material properties that relate to survivability in lead-free assembly processes are

- Decomposition temperature (T_d)
- Coefficients of thermal expansion (CTE_s)
- Moisture absorption
- Time to delamination
- Modulus

Time to delamination, or T260 time, which is the time it takes for a sample to delaminate when held at an isotherm temperature of 260°C, is not a fundamental base material property, but is a functional test related to the other material properties. In multilayer PCBs, this property can be affected

by the quality of the innerlayer copper surface preparation and multilayer lamination, among other things.

13.3.2 Lead-Free Assembly and Long-Term Reliability Issues

The second fundamental issue for base materials and PCBs is the impact to long-term reliability assuming a PCB has survived assembly. Other things being equal, the long-term reliability of a PCB assembled in a lead-free process with higher temperatures is not as good as a PCB assembled in a tin-lead assembly process with lower temperatures, unless the properties of a material are so robust that lead-free temperatures do not have an impact on the material. The magnitude of the difference is dependent on many factors. Some of the key properties of the base material with respect to long-term reliability include

- CTEs
- Glass transition temperature (T_g)
- Decomposition temperature (T_d)
- Moisture absorption

Additionally, the specific construction of the PCB in terms of resin content, the types of fiberglass cloth used, and the adhesion and long-term thermochemical compatibility between the resin system and copper which is plated within vias can have a significant impact on long-term reliability. Some of these factors relate to the impact they have on CTEs, both in the *z* axis as well as in the *x* and *y* axes. For example, using a very high resin content prepreg layer adjacent to a very low resin content layer increases the stress at the interface of these layers due to the differences in thermal expansion that result from the differences in resin-

to-glass concentrations. The higher temperatures of lead-free assembly result in a greater absolute level of expansion or stress at these interfaces. The distribution of the glass filaments within the resin system can have a similar effect. Within a given layer or prepreg, if there are “resin-rich” versus “glass-rich” areas, the differences in thermal expansion between these areas cause stresses that can lead to micro-delamination, or at the interface with a plated-through hole (PTH) will result in points of stress-strain discontinuity resulting from differences in the *z*-axis expansion values. It is not uncommon to see cracks in the PTH copper begin at these points.

Section 13.5 discusses the material properties relevant to both surviving lead-free assembly as well as ensuring long-term reliability. Although the test methods used to assess long-term reliability are beyond the scope of this chapter, where relevant, a brief description will be provided to help explain performance differences. However, before discussing these properties in more detail, Sec. 13.4 with Table 13.1 presents some of the concerns related to the components used to make base materials.

TABLE 13.1 Primary Lead-Free Issues for Base Material Components

Component	Lead-Free Assembly Impact	Potential Solutions	Related Considerations
Resin system	1. Peak assembly temperatures can reach point where resin decomposition begins. 2. Higher temperatures result in increased thermal expansion, delamination and stress on plated holes as a result. 3. Vapor pressure of absorbed moisture much higher at lead-free assembly temperatures; can lead to blistering/delamination. 4. "Phenolic" lead-free compatible materials often not as good for electrical performance, especially Df.	1. Formulate resin system with higher decomposition temperatures. 2. Formulate for lower coefficients of thermal expansion. 3. Evaluate materials for moisture absorption/release characteristics; drying processes in PCB fabrication and/or assembly. 4. Evaluate nondicy/ nonphenolic laminate materials with lower Df.	1. Reformulation can adversely affect electrical properties and manufacturability. 2. Can also impact mechanical properties and manufacturability. 3. PCB storage conditions during manufacturing and prior to assembly are much more important, especially humidity conditions. 4. Cost/performance trade-off. New materials now in high volume use that offer more choices.
Fiberglass cloth	Thermal and mechanical stress on resin-to-glass bond. Volatilized components can also stress this bond.	Cleanliness, moisture resistance and choice of proper coupling agent for resin adhesion more important.	Loss of resin-to-glass adhesion through thermal cycling could impact CAF resistance. Use of spread glass cloth may be beneficial.
Copper foil	Thermal and mechanical stress on resin-to-copper bond.	Improved copper surface treatments for improved adhesion, i.e., coupling agents.	Roughness impacts signal attenuation, especially at high frequencies.

13.4 THE IMPACT OF LEAD-FREE ASSEMBLY ON BASE MATERIAL COMPONENTS

The higher temperatures of lead-free assembly have an impact on each of the three main components of laminate materials: the resin system, the glass cloth, and the copper foil. Table 13.1 summarizes the key issues for each of these main components.

13.5 CRITICAL BASE MATERIAL PROPERTIES

Substantial work describing the impact of lead-free assembly temperatures on base materials and finished PWBs has been gathered. These works have identified the critical base material properties that must be considered when selecting a material for lead-free assembly applications, though work on this subject continues. Table 13.2 provides a summary of some key properties.

TABLE 13.2 Critical Base Material Properties for Lead-Free Assembly Applications

Property	Definition	Issue
Decomposition temperature, T_d	Measurement of weight loss from resin system degradation as a function of temperature. T_d is typically defined as the point at which 5% of the original mass is lost to decomposition, but other levels can also be reported, e.g., 1%, 2%, or "onset."	Resin decomposition can result in adhesion loss and delamination. A 5% level of decomposition is severe, and intermediate levels are important for assessing reliability since peak temperatures in lead-free assembly can reach onset points of decomposition. A high T_d by the 5% definition does not guarantee performance. Conversely, a low T_d by the 5% definition is not necessarily bad if the onset temperature of decomposition is high enough.
Glass transition temperature, T_g	Thermodynamic change in polymer from a relatively rigid, glassy state, to a softened, more deformable state.	Several properties change as the T_g is exceeded, including the rate at which a material expands versus temperature. Modulus also decreases significantly as T_g is exceeded.
Coefficients of thermal expansion, CTEs	Rate of change in physical dimension (in *x*, *y*, or *z* axis) as a function of temperature, expressed as a coefficient of thermal expansion. Can also be expressed as a percentage expansion over a given temperature range.	Resin system CTE values above T_g are much higher than below T_g. *Z*-axis expansion induces stress on plated vias. The higher temperatures of lead-free assembly result in more total expansion for a given material. Several mature lead-free-compatible materials incorporate inorganic fillers that reduce CTE values. *X*- and *y*-axis CTEs are also important for reliability at component and layer interfaces.
Moisture absorption	Tendency of a material to absorb moisture from the surrounding environment. Can be assessed by more than one method, including water soak or in an increased pressure and humidity environment.	Vapor pressure of water is much higher at lead- free assembly temperatures. Absorbed moisture can volatilize during thermal cycling and cause voiding or delamination. PWBs that initially pass lead-free assembly testing may exhibit defects after storage in an uncontrolled environment as a result of moisture absorption. This should be considered when evaluating materials and PWB designs.
Time to delamination	Not a fundamental property; measurement of the time for delamination to occur at a specific temperature, e.g., 260°C (T260) or 288°C (T288).	This property is related to decomposition temperature and adhesion between material components. Thermal expansion and moisture absorption can also influence results. In multilayer PWBs, the treatment of the internal copper surfaces is also critical, among other factors.

A very critical point that must be emphasized with respect to these issues is that although laminate manufacturers can easily make improvements in one property, doing so can often adversely affect other important properties. For example, it is relatively easy to formulate a resin system with a very high time to delaminate in conventional T260 or T288 tests, or to engineer a resin system with a very high decomposition temperature. However, this is often achieved at the expense of mechanical properties and can make the material more difficult to use successfully in conventional PWB manufacturing processes, or without sacrificing design flexibility. Interactions between these and other material properties such as hardness, modulus, and fracture toughness with the processes used in PCB fabrication can greatly influence the reliability of a PCB during and after assembly. For example, an increase in decomposition temperature with a simultaneous decrease in fracture toughness does little good if the PCB exhibits cracking or fracturing during scoring processes or similar defects during the mechanical drilling of tight pitch holes for PTHs. Therefore, achieving the best balance of properties to meet the needs of the OEM, Electronic Manufacturing Services (EMS) company, and PWB manufacturer is critical.

13.5.1 The Historical Focus on T_g

Chapter 10 explained how and why T_g has historically been one of the properties used to classify base materials, while Chap. 12 provided additional information on the measurement of T_g. In short, the historical focus on T_g as an indicator of reliability is probably the result of its effect on total *z*-axis expansion. However, because of differences in CTE values, even the relationship between T_g and thermal expansion requires further analysis. Figure 13.2 illustrates

the relation-ship between T_g and thermal expansion for the products in Table 13.3.

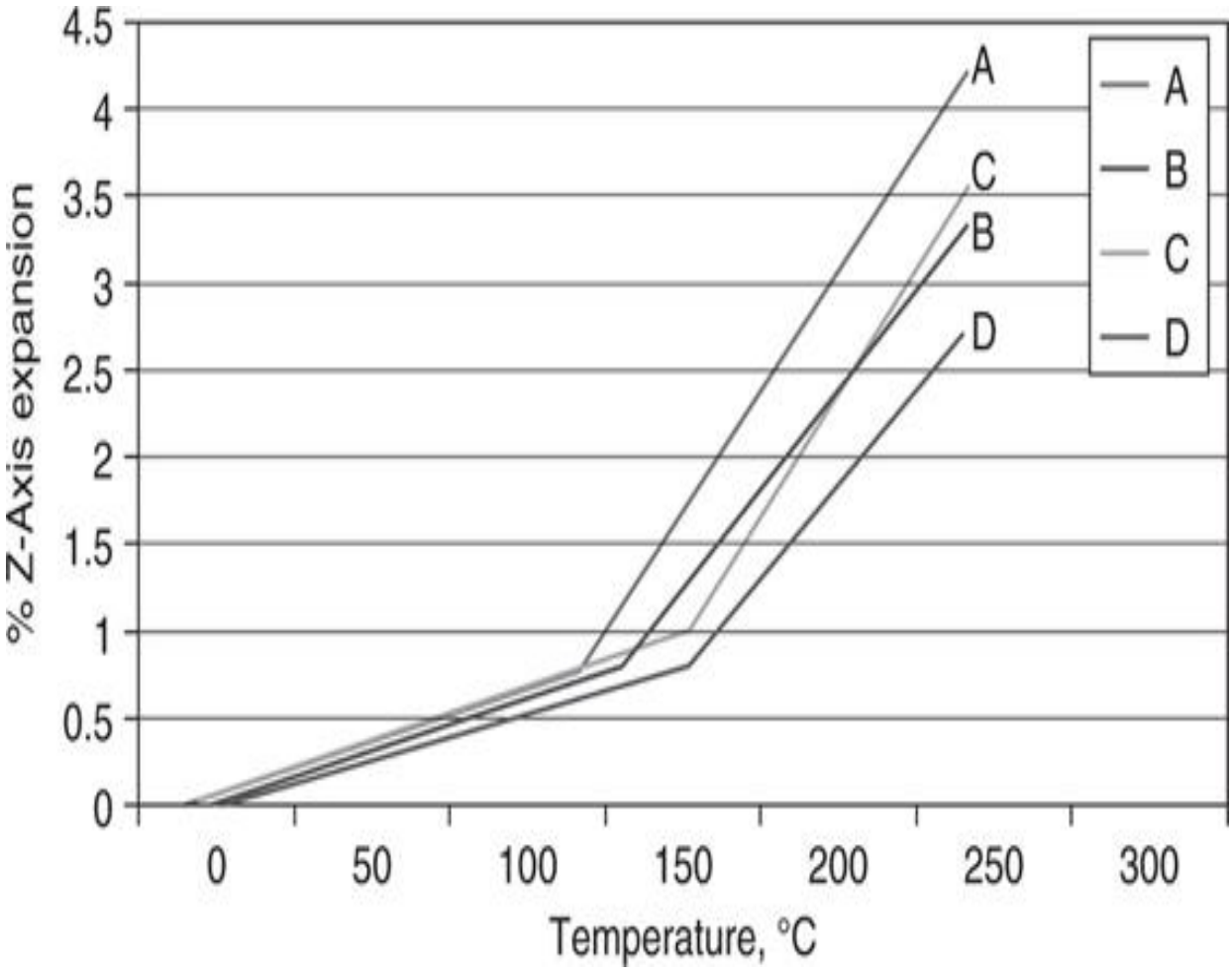


FIGURE 13.2 The impact of T_g and CTE values on total expansion.

TABLE 13.3 Properties of Some Common FR-4 Base Materials

Product	Description	Glass Transition Temp., °C	Decomposition Temp., °C	% Expansion, 50–260°C (40% Resin Content)
A	Traditional dicy-cured 140°C T_g FR-4	140	320	4.2
B	Phenolic" mid-T_g FR-4	150	335	3.4
C	Traditional dicy-cured High-T_g FR-4	175	310	3.5
D	Improved high-T_g FR-4	175	335	2.8

From Fig. 13.2, products with the same pre- and post-T_g CTE values (A and C, for example; note that above T_g the lines are parallel) differ in total expansion based on their T_g values. For example, the 175°C T_g material C exhibits less total expansion than the 140°C T_g material A because the onset of the higher post-T_g rate of expansion is delayed by 35°C. However, the 175°C T_g material D, with a lower CTE value, exhibits much less total expansion than the 175°C T_g material C even though the T_g values are the same. Furthermore, the 150°C T_g material B with reduced CTE values exhibits approximately the same total expansion (3.4 percent) as the 175°C T_g material C (3.5 percent). However, with a decomposition temperature that is significantly higher, this mid-T_g FR-4 material is much more compatible with lead-free assembly than the 175°C T_g material in this case, as it is a dicy-cured material.

13.5.2 The Importance of Decomposition Temperature

Although glass transition temperature (T_g) and *z*-axis expansion have been a primary focus of attention over the years, only with the introduction of lead-free assembly has the decomposition temperature (T_d) gained significant attention. The decomposition temperature has always been important in terms of reliability, yet most people have used T_g as a proxy for material reliability. One reason for this is that other things being equal, a higher-T_g results in less total thermal expansion, and therefore less stress on plated vias. What wasn't discussed is that it is common for dicy-cured, high-T_g FR-4 materials to exhibit somewhat lower decomposition temperatures than dicy-cured, 140°C T_g FR-4 materials. This is highlighted by the fact that most dicy-cured 140°C T_g FR-4 materials exhibit longer T260 times than dicy-cured high-T_g FR-4 materials. To highlight the importance of T_d, examine Fig. 13.3.

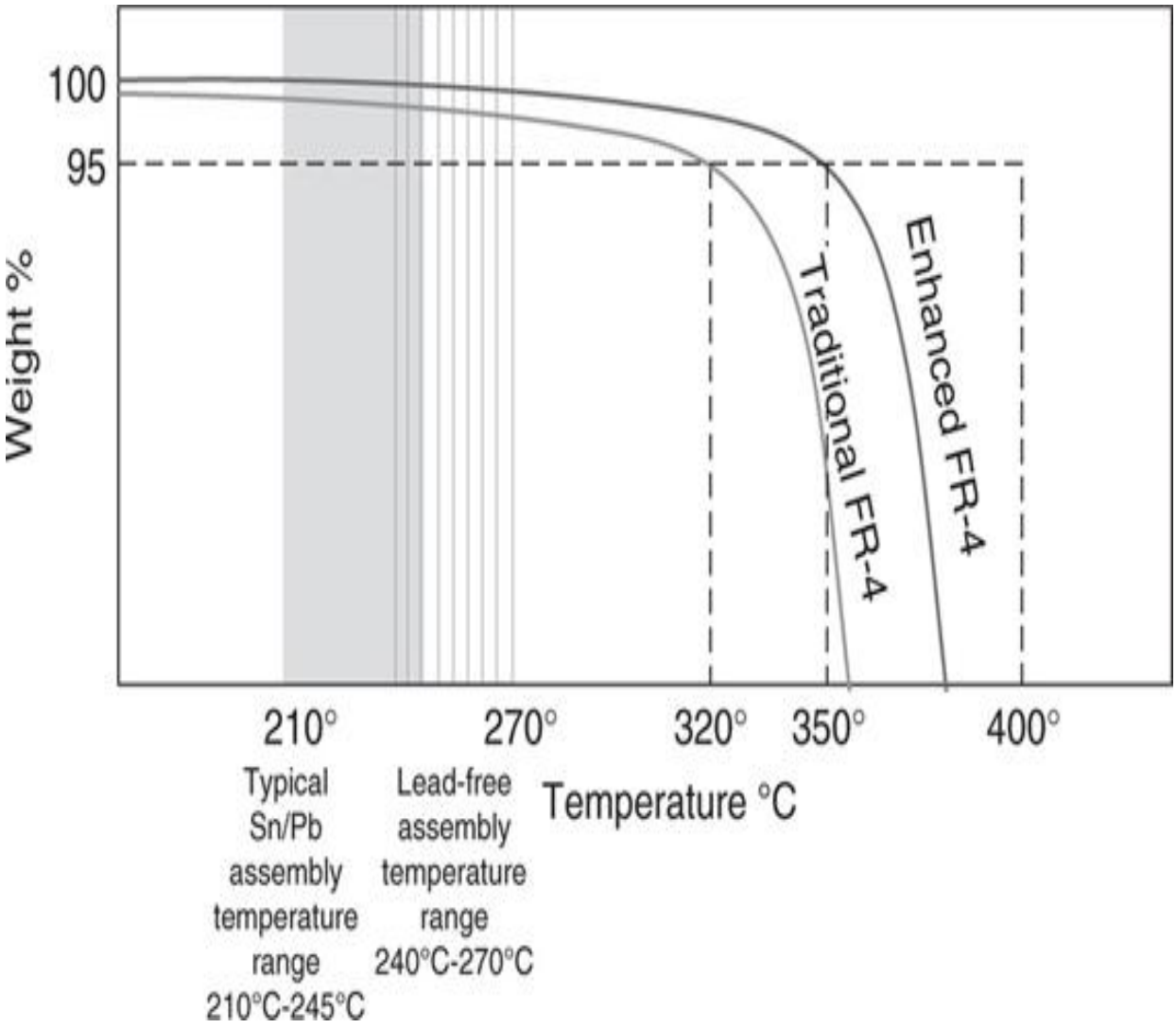


FIGURE 13.3 Decomposition curves for a traditional and improved FR-4 material.

The traditional dicy-cured, high-T_g FR-4 materials have T_d values in the range of 290 to 310°C. Traditional 140°C T_g dicy-cured materials are generally somewhat higher, with a typical example of a material with a T_d of 320°C shown in Fig. 13.3. In the typical tin-lead assembly environment, peak temperatures do not reach the point where decomposition is significant for either the traditional or enhanced products. However, in the lead-free assembly environment, peak temperatures can reach the point where a small but significant level of decomposition can occur for the

traditional dicy-cured materials, but not for the enhanced products.

This seemingly small level of decomposition in the conventional products can have extremely significant effects on reliability, especially if multiple thermal cycles are experienced.

On the other hand, as long as the temperatures experienced during assembly and rework do not exceed the temperature at which decomposition begins, there may not be further benefit to higher decomposition temperatures. In addition, the resin system modifications often made to increase T_d can sometimes lead to other problems, such as brittleness or hardness of the resin system that negatively impacts PCB manufacturability (as in drilling, scoring, and routing) or fracture toughness in tight pitch PTH areas. As not all lead-free-compatible materials use the same resin systems, great care should be used in selecting a material that balances the requirements of the OEM, assembler, and PCB fabricator. A simple review of a material data sheet or IPC slash sheet is not sufficient to guarantee success. Involvement with the base material supplier to fully understand the capabilities of a material and the processing required for success is vital. To expand on this, examine Figs. 13.4 through 13.6, which were also presented in Chap. 12.

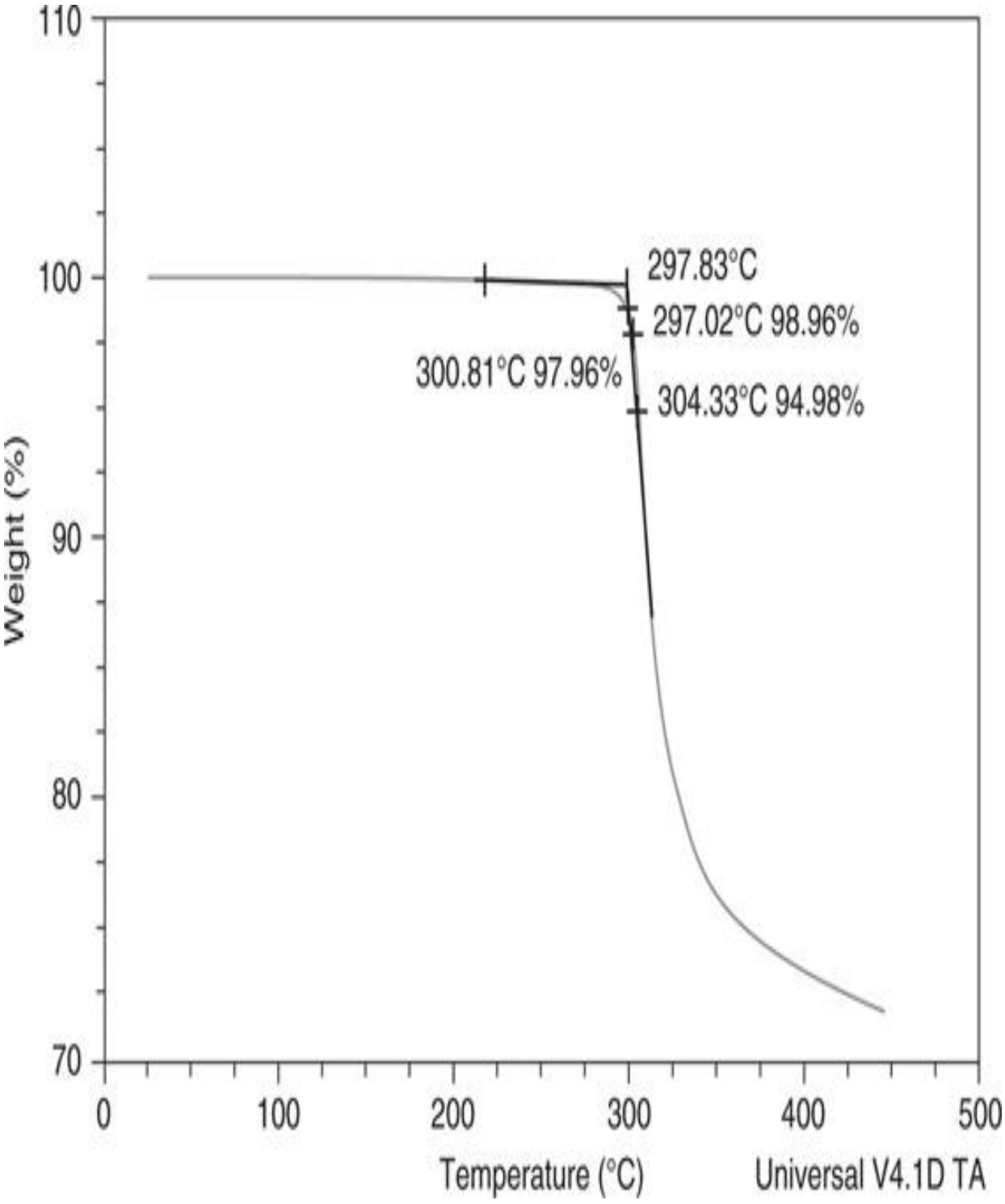


FIGURE 13.4 Decomposition curve for a standard dicy-cured high-T_g FR-4.

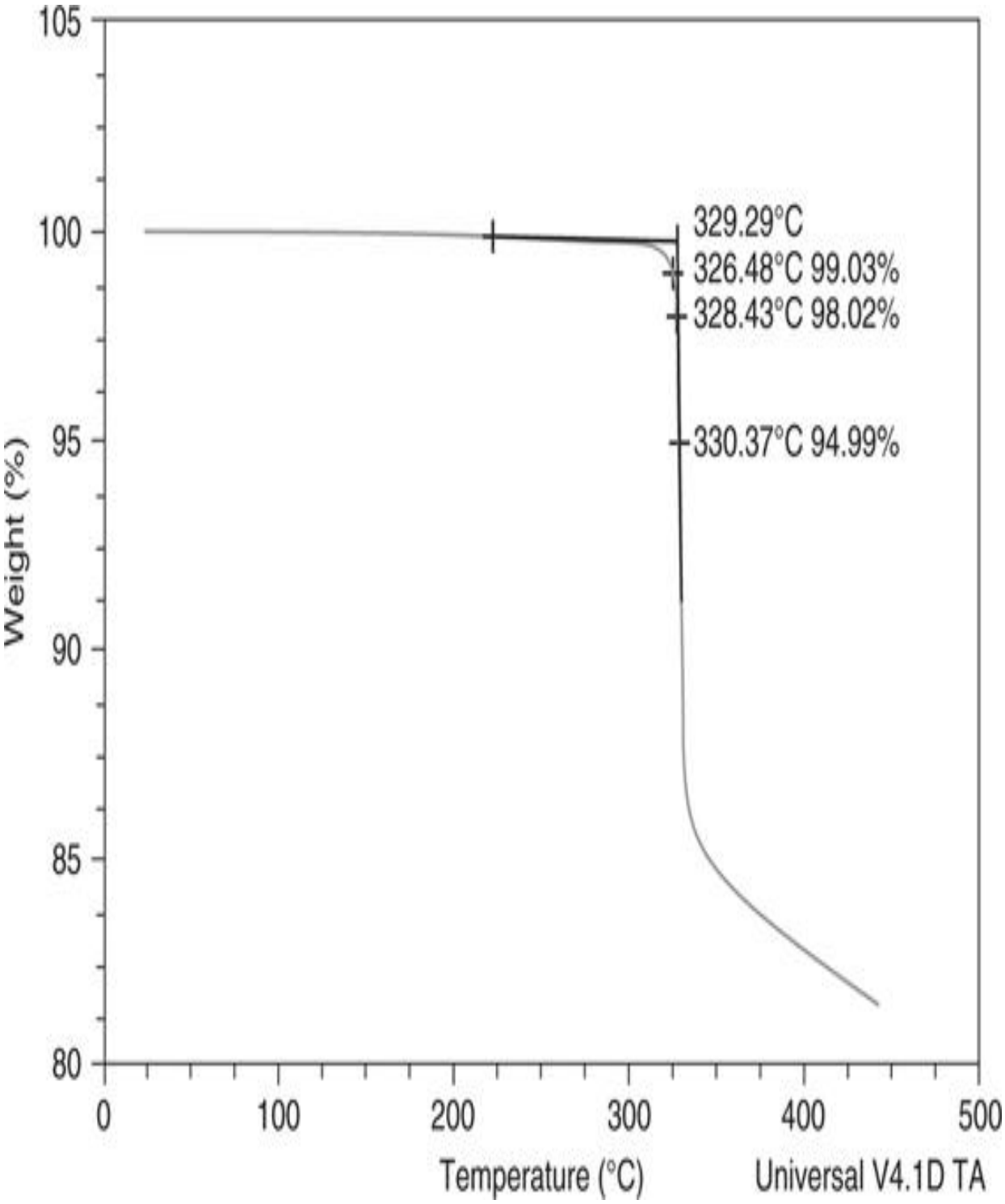


FIGURE 13.5 Decomposition curve for a phenolic high-T_g FR-4.

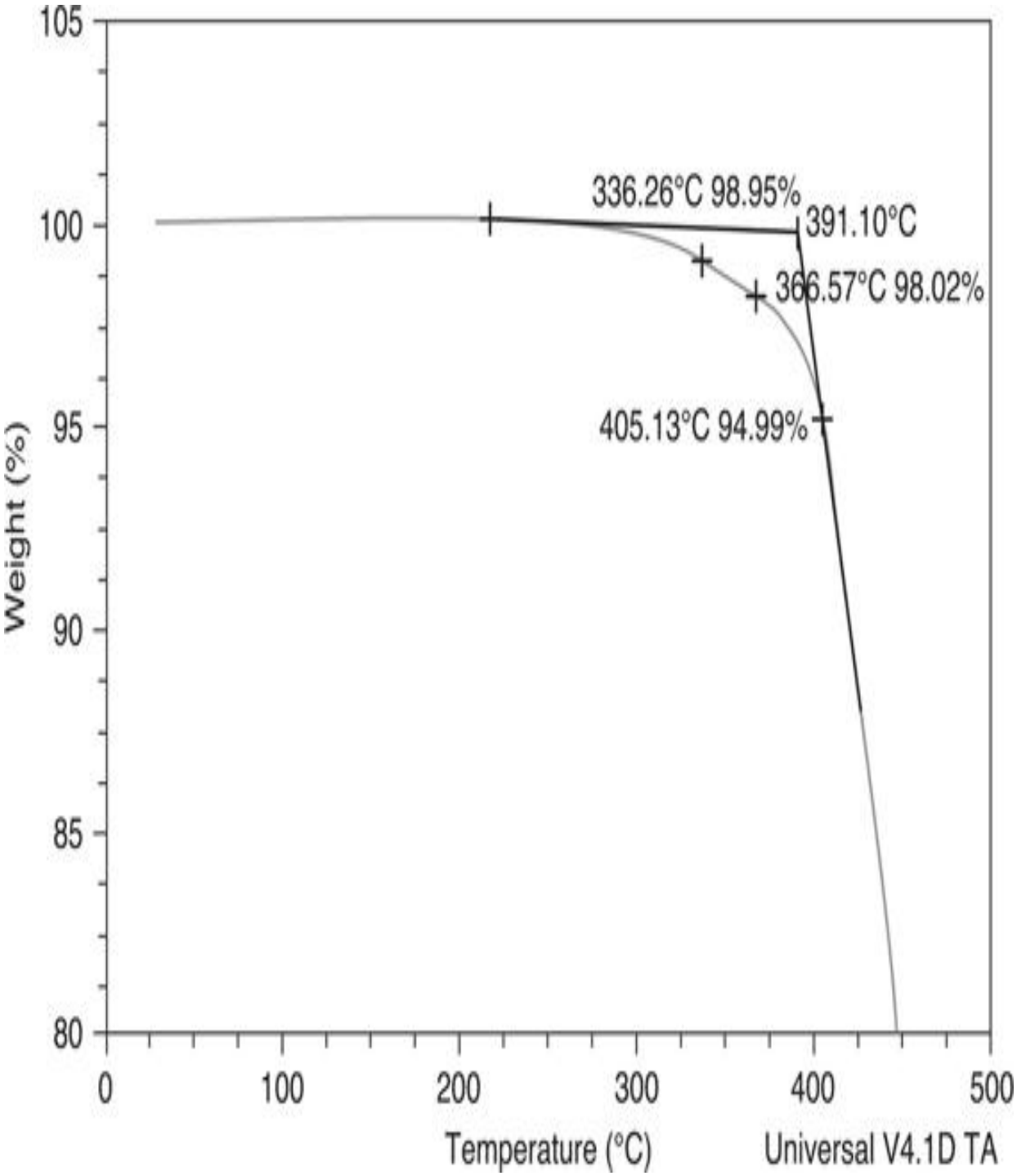


FIGURE 13.6 Decomposition curve for an alternative high-T_g/high-T_d material.

First, note the slope of the decomposition curve in Fig. 13.6. By the 5 percent decomposition definition, this material has a T_d of 405°C. However, looking at 1 percent and 2

percent values, the temperatures are 336°C and 367°C, which are significantly lower than a reported 5 percent value of 405°C. This is not to say that a 1 percent T_d of 336°C is bad. In fact, this material has exhibited exceptional reliability in lead-free applications. However, it does point to the need to understand decomposition levels other than the 5 percent level. In contrast, the material in Fig. 13.5 has a 5 percent T_d of 330°C with 1 percent and 2 percent T_d's of 326°C and 328°C, respectively. In this case, there is a very small difference between the 1 percent, 2 percent, and 5 percent values, and this material has also proven to have excellent performance in a broad range of lead-free assembly applications. Last, the dicy-cured high-T_g material in Fig. 13.4 exhibits a 5 percent T_d of 305°C with 1 percent and 2 percent values of 297°C and 301°C. This is also a small range of values, but in this case the absolute values are lower and begin to approach the range of temperatures that can be experienced, at least locally, in a printed circuit board that undergoes lead-free assembly and rework. Materials such as this have not performed with adequate reliability to be considered for anything but the simplest lead-free applications. In addition, if PCBs made with these materials are stored in uncontrolled environments and are allowed to absorb even a modest level of moisture, the combination of lower T_d's with the higher vapor pressure of water at lead-free temperatures can lead to catastrophic defects in assembly or severely degraded long-term reliability.

To take this a step further, examine the materials listed in Table 13.3. These are four FR-4 materials, with material C being the same material as shown in Fig. 13.4, and material D being the same as the material in Fig. 13.5. The impact of decomposition temperature when these materials are exposed to multiple thermal cycles to different peak temperatures is highlighted in Figs. 13.7 and 13.8. Figure 13.7 graphs cumulative weight loss (decomposition) for

these materials when cycled repeatedly to a peak temperature of 235°C. Clearly, there is little impact on resin decomposition when the peak temperature reaches 235°C. Figure 13.8 presents the same results when the peak temperature is increased to 260°C. The increase in temperature to 260°C has a severe impact on resin decomposition for the traditional dicy-cured FR-4 materials as they experience multiple thermal cycles, especially the high-T_g material (product C). The rapid degradation in material C after only a few thermal cycles highlights why this material is not recommended for lead-free assembly applications.

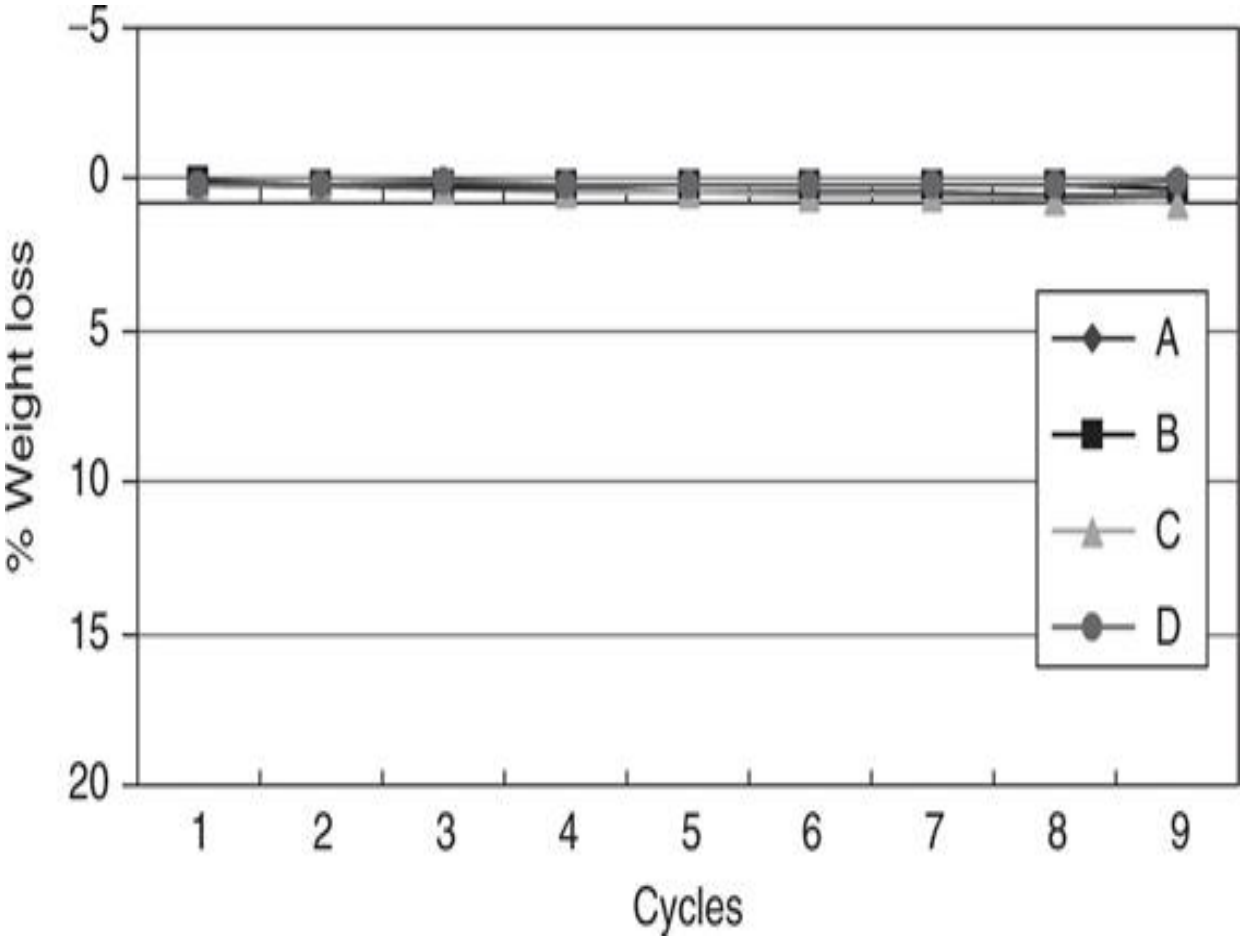


FIGURE 13.7 Decomposition through multiple cycles to 235°C.

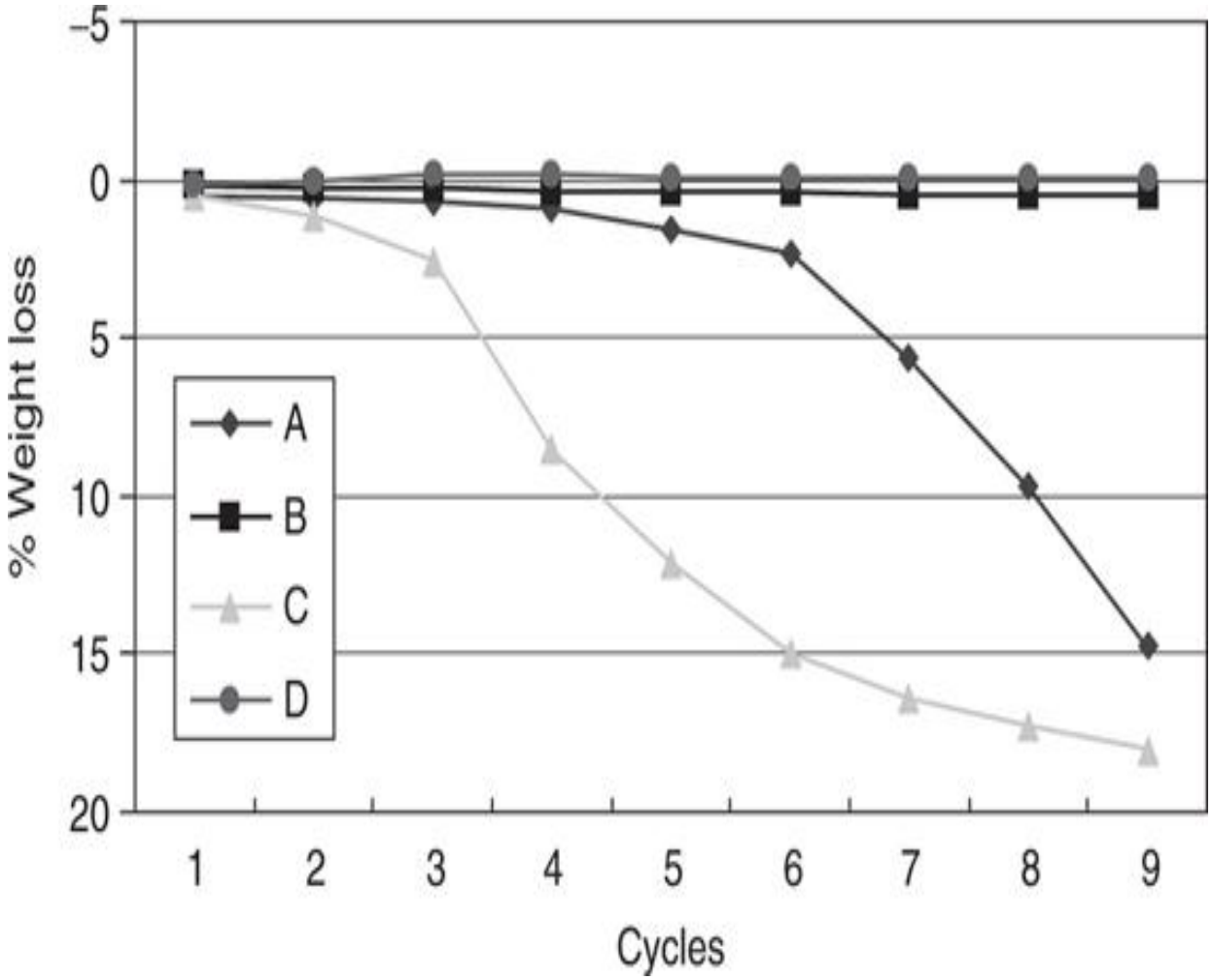


FIGURE 13.8 Decomposition through multiple cycles to 260°C.

13.5.3 Moisture Absorption

As pointed out in Table 13.2, the vapor pressure of water at lead-free assembly temperatures—260°C for example—is much higher than at eutectic tin-lead assembly temperatures such as 230°C. Figure 13.9 plots the vapor pressure of water, in both mm Hg and psi, versus temperature. At 230°C the vapor pressure of water is near 400 psi. At 260°C, it is close to 700 psi. Therefore, any absorbed moisture within a PCB during assembly can have a much greater impact in lead-free assembly, as the greater pressure stresses the adhesion between the base material

components and can also create small voids within the resin system.

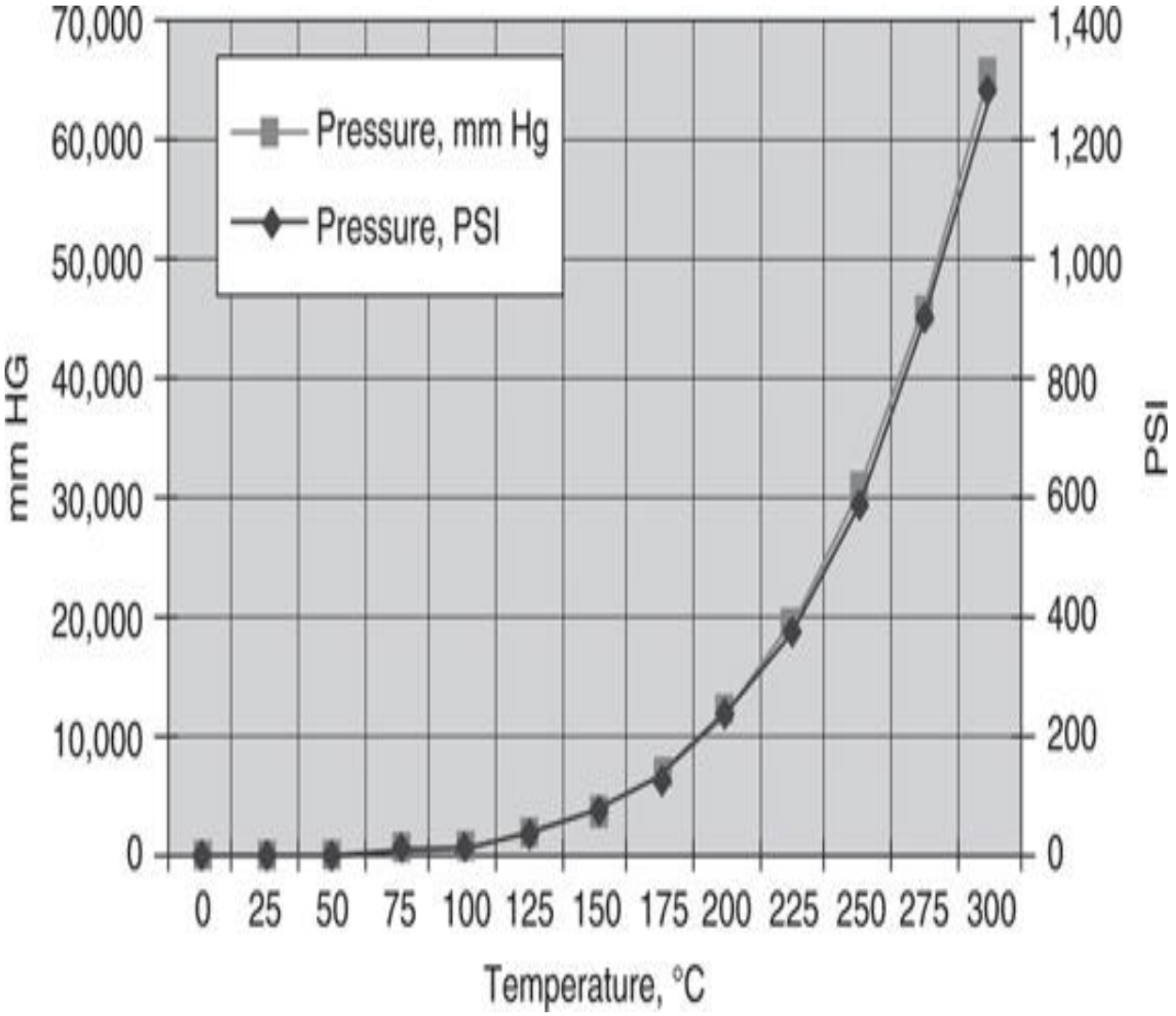


FIGURE 13.9 Vapor pressure of water versus temperature.

This means that much more care must be used in selecting materials for their moisture absorption properties. However, all common base materials absorb some level of moisture.

So the storage of these materials, both during manufacturing of the PCB as well as prior to assembly, must also be assessed. Additional drying or baking steps may be needed in some applications to drive off any absorbed moisture prior to exposure to high temperatures.

Additionally, it can be difficult to correlate actual performance with the moisture absorption data commonly found on material data sheets. One reason for this is that it may not be just the moisture absorption that is important, but the rate at which moisture can be driven from the material as well. As an illustration, consider the data in Fig. 13.10.

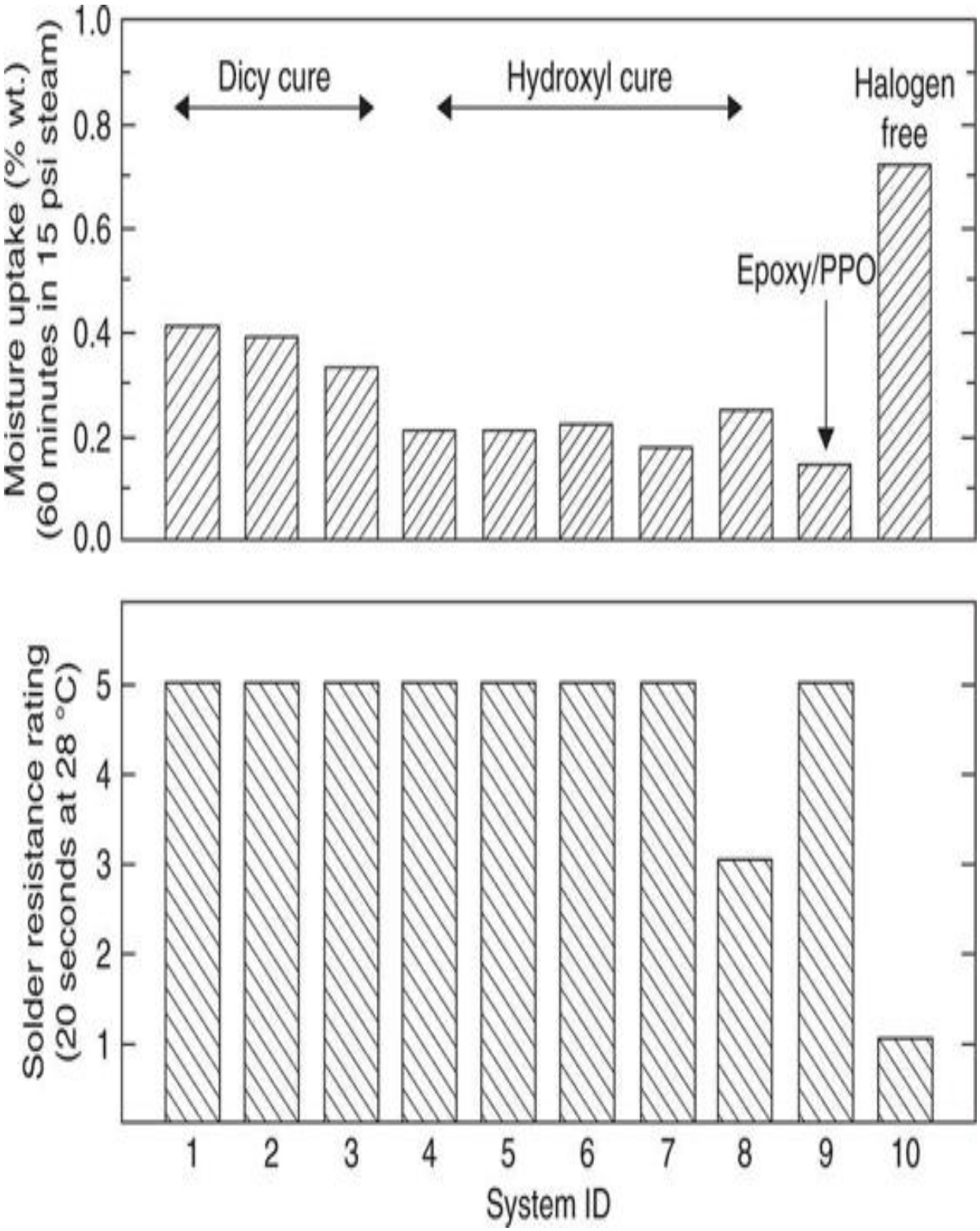


FIGURE 13.10 Moisture absorption versus solder shock resistance for several materials.

These materials were conditioned for 60 minutes in 15 psi steam and then solder shocked for 20 seconds at 288°C. Their moisture absorption was measured and compared to their performance in the solder shock testing. The particular halogen-free material shown in this graph exhibits a very high level of moisture absorption and does indeed exhibit poor solder shock resistance. However, with the exception of only one material, all the other materials exhibited good solder shock resistance in this test, even though their moisture absorption levels ranged from less than 0.2 percent to just over 0.4 percent. The one other material that exhibited some level of defects had an intermediate level of moisture absorption, around 0.3 percent. The point is that it is very difficult to draw conclusions about material performance based on reported levels of moisture absorption. Actual resistance to blistering or delamination may be affected by the interaction of the absorbed moisture with other properties of the material, such as modulus, yield and ultimate strengths. Additional reliability testing relevant to the application being considered is needed to make good decisions about material compatibility.

With respect to moisture absorption and the subsequent drying or baking of PCBs, consider the tests summarized by Figs. 13.11 and 13.12. In each test, several different types of base material were evaluated, including dicy-cured and phenolic-cured FR-4 materials, as well as low D_k/D_f and halogen-free materials. Figure 13.11 shows moisture absorption data for samples that were dried, then soaked in water at room temperature for five days, measured, and then baked at 125°C for 24, 96, and 120 hours. Samples from this test were then submitted to 35°C and 85 percent RH for seven days, measured, and then baked at 125°C for 24 and 48 hours. The results of this second test are shown in Fig. 13.12. Although these graphs show that the different types of materials may absorb somewhat different amounts of moisture, in each case the moisture was able to be driven

off by baking. Beyond this, little correlation could be found between the relative levels of moisture absorption and performance in lead-free assembly applications. Although the materials tested here that showed relatively low levels of moisture absorption have performed well in lead-free assembly applications, some that showed relatively high levels of moisture absorption in these tests have also performed well. The materials in this group that have not done well in lead-free applications fell somewhere in the middle in terms of relative moisture absorption. Thus, although moisture absorption is a critical property, it must also be evaluated within the context of other properties as noted above.

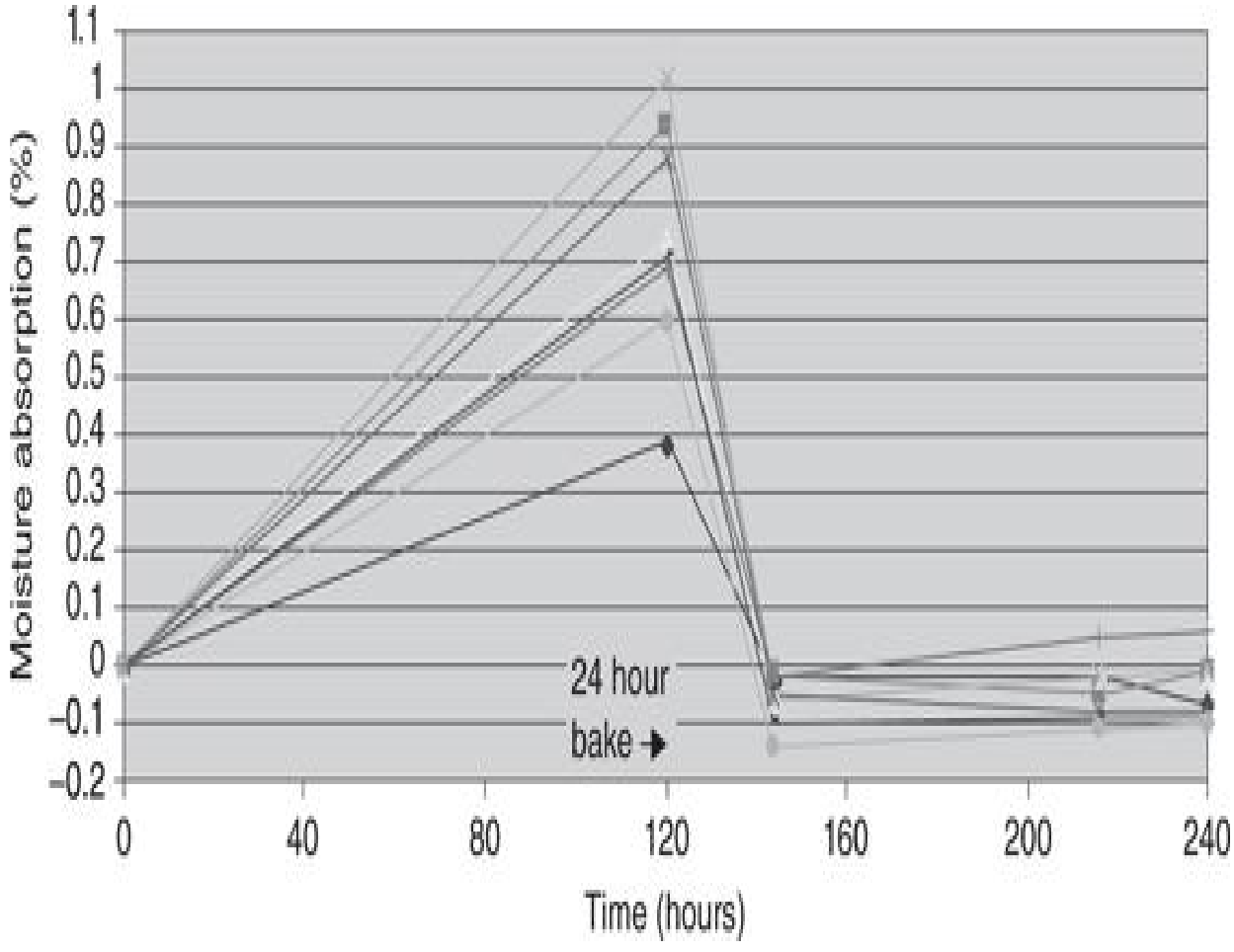


FIGURE 13.11 Percent weight change after a 5-day ambient moisture test and 125°C bake.

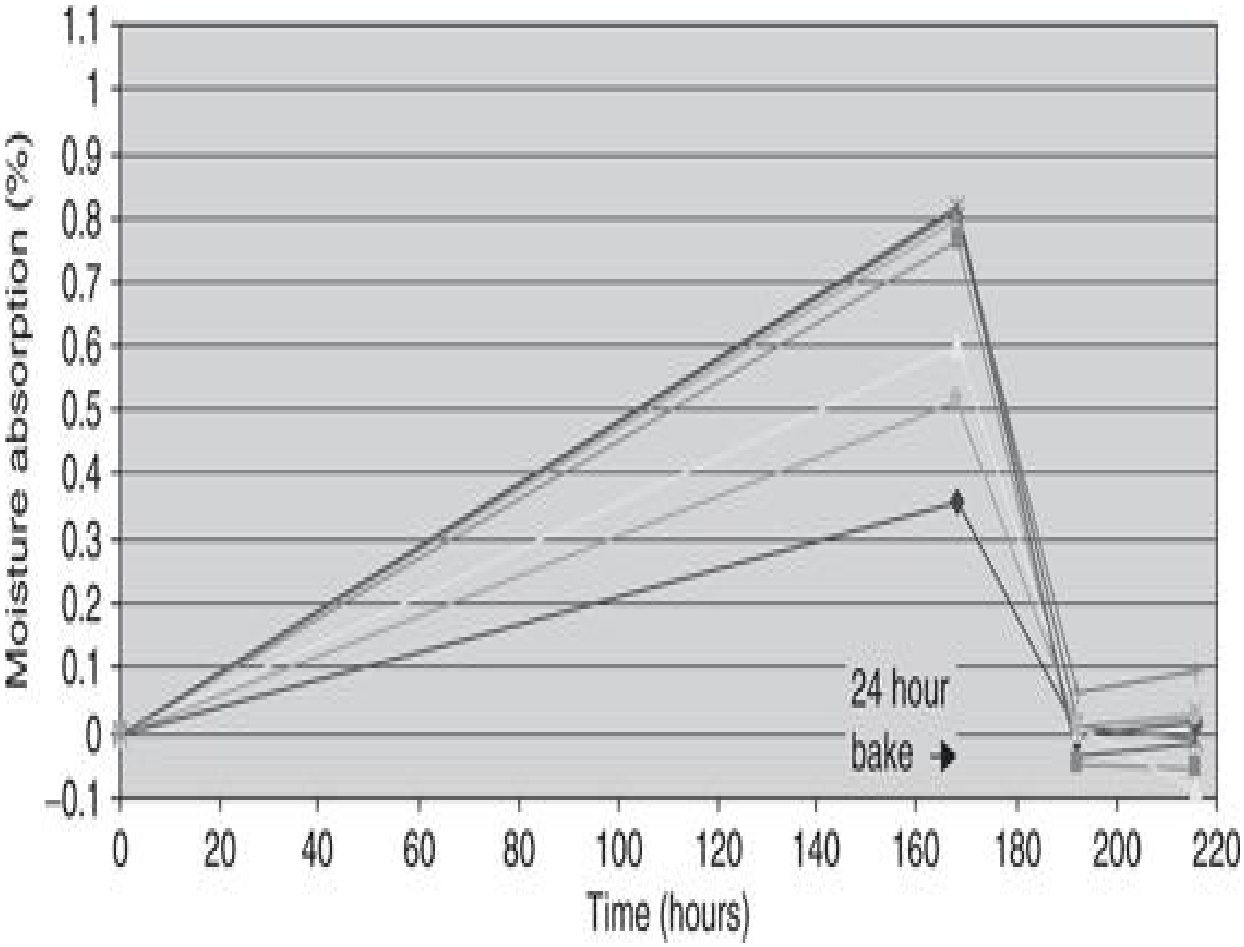


FIGURE 13.12 Percent weight change after seven days at 35°C/85 percent RH moisture test and 125°C bake.

13.5.4 Time to Delamination

The time to delamination, and how it is measured, was discussed in further detail in Chap. 12. This test method involves placing a sample of laminate or PCB in a thermomechanical analyzer (TMA) and heating the sample to a specific isothermal temperature, most commonly 260°C (T260) or 288°C (T288). The time it takes for the sample to delaminate is then measured and reported. Figure 13.13 is an example of a complex backplane PCB that was subjected to T260 testing. This PCB used a conventional dicy-cured high-T_g FR-4 material and delaminated before reaching 2

minutes. Note the charring and degradation of the resin system. Alternate resin systems, including alternate types of FR-4 materials, can offer significantly improved performance. Figure 13.14 compares time-to-delamination performance at different temperatures for four different resin systems: two dicy-cured FR-4s and two that use an alternate type of curing mechanism. Note that the materials using an alternative curing mechanism offer much longer times to delamination at each temperature, although all systems exhibit much shorter times as the temperature is increased.

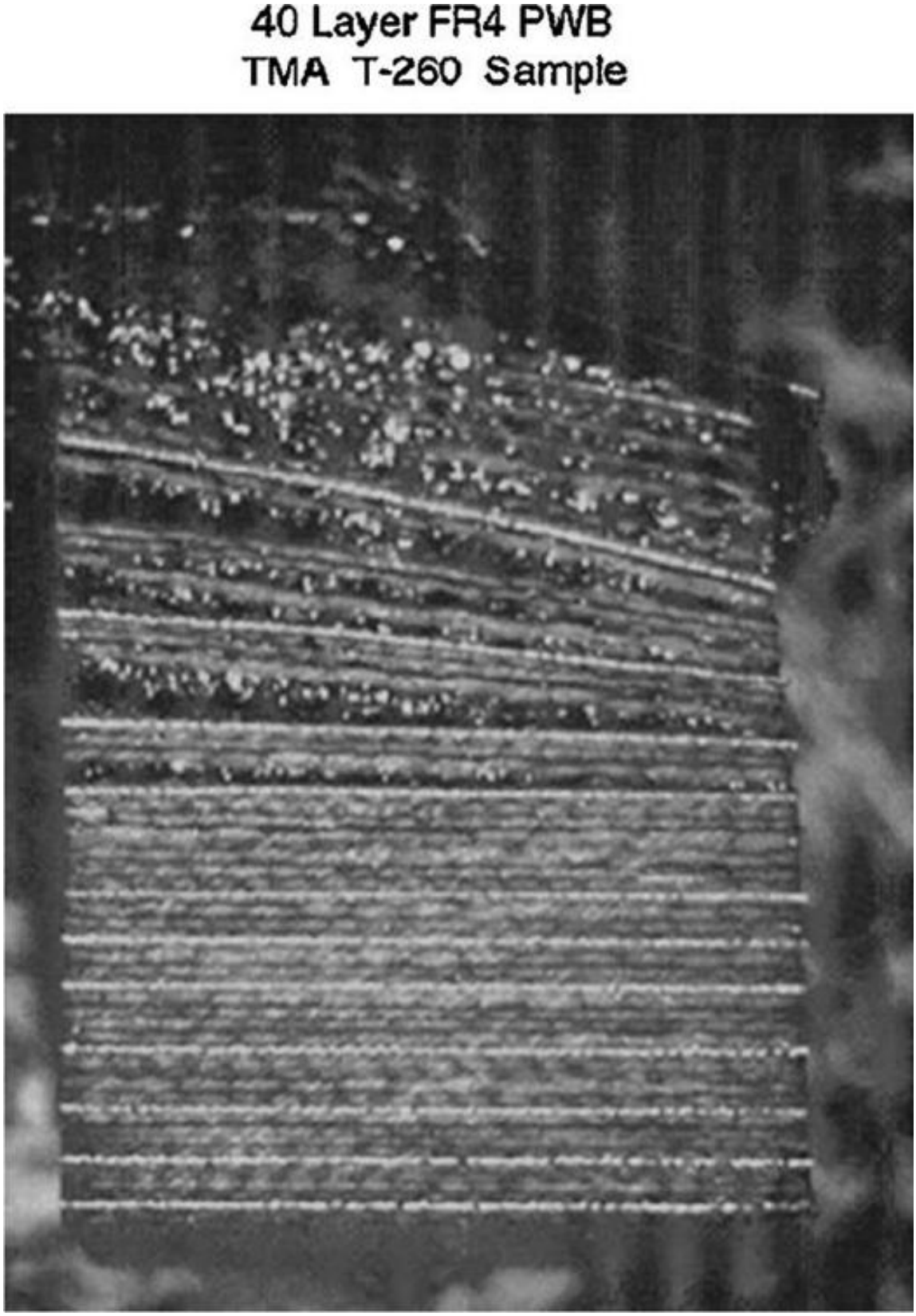


FIGURE 13.13 Delamination and resin decomposition after T260 testing.

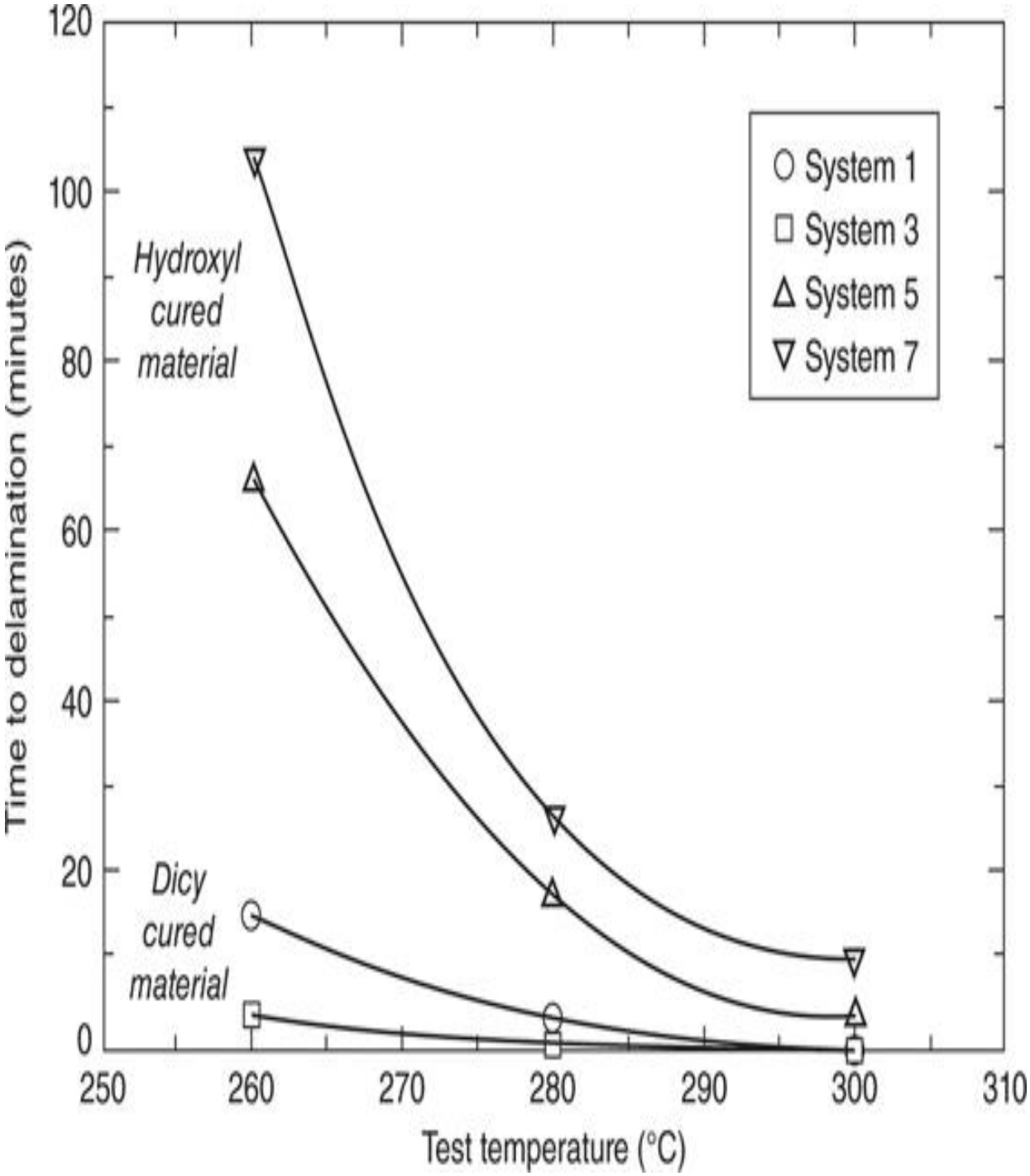


FIGURE 13.14 Time to delamination versus temperature for different resin systems.

Times to delamination also vary based on the type of sample measured. Laminates with the copper foil removed generally exhibit longer times than laminates with copper

foil. Clad laminates in turn exhibit longer times than multilayer PCBs. Figure 13.15 provides data on clad versus unclad samples for several material types in T260 and T288 testing. In multilayer PCBs, usually the interface between the resin and the internal copper surfaces will fail first. Time to delamination in multilayer PCBs is affected by the quality of the surface treatment of the internal copper layers, the quality of the multilayer lamination processing, as well as the type and condition of the bonding prepreg.

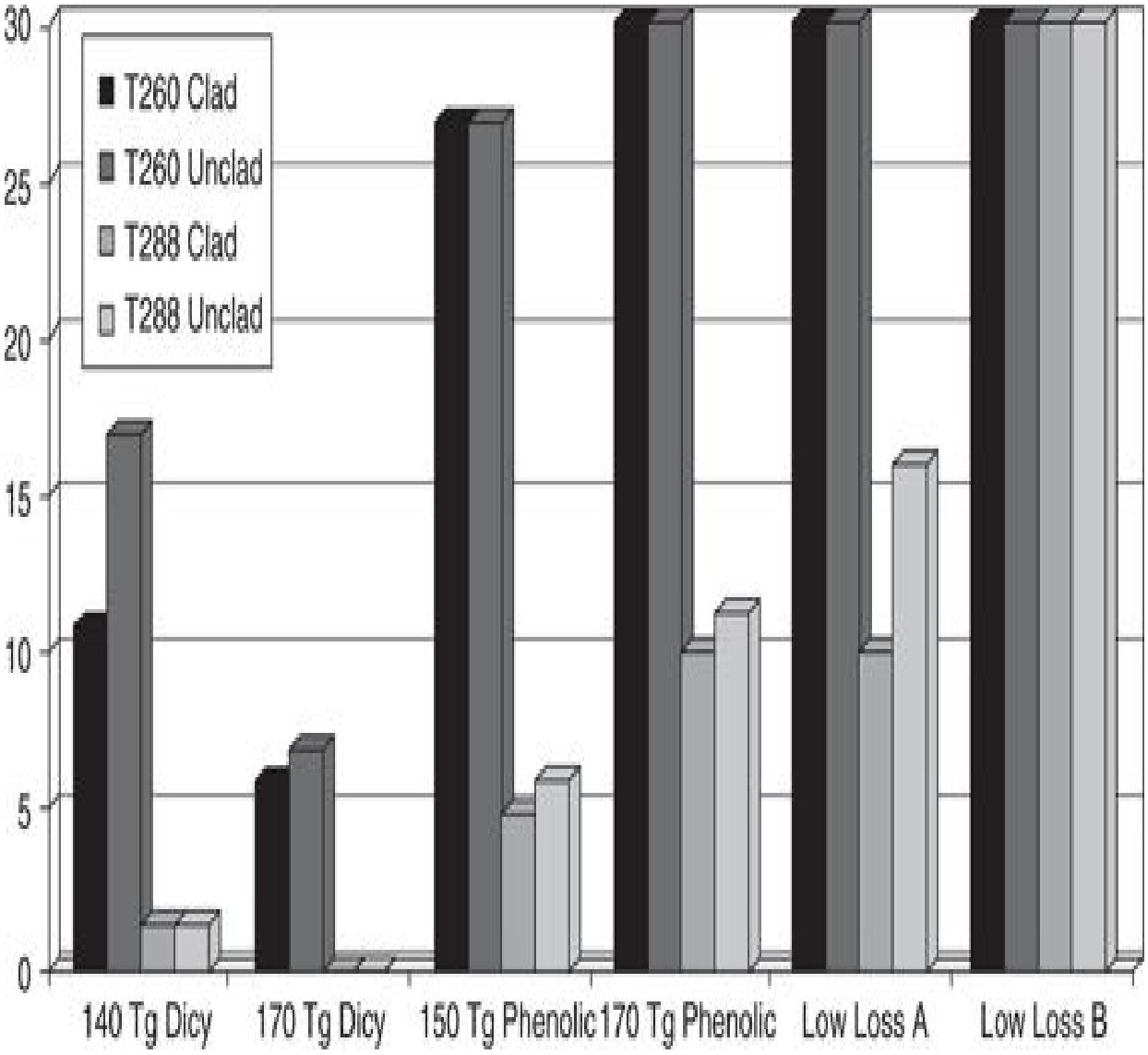


FIGURE 13.15 T260 and T288 testing on clad and unclad samples of several material types.

Time to delamination testing of multilayer PCBs has become a common test for lead-free assembly compatibility. However, several factors beyond the base material type can have an influence on performance. So care needs to be taken in assessing why a particular PCB might exhibit a low time to delamination. On the other hand, if a particular type of base material exhibits low times to delamination, little can be done in PCB manufacturing to improve performance. In short, a given material offers a certain performance entitlement. Whether this performance level is realized in the finished PCB is dependent on several factors, primarily related to PCB manufacturing processing. It should also be noted that, as with decomposition temperature, values beyond a certain level may not indicate that a material is more reliable.

13.5.5 The Impact of Lead-Free Assembly on Other Properties

Exposure to assembly temperatures can have a significant effect on the properties of base materials, including the T_g and modulus properties of the material. This is particularly true if the material is exposed to multiple thermal cycles. In addition, the magnitude of the effect is dependent on the specific peak temperature experienced. Figures 13.16 and 13.17 compare the effect of multiple thermal cycles on dynamic mechanical analysis (DMA) T_g for various material types when cycled to 235°C (Fig. 13.16) and 260°C (Fig. 13.17). When cycled repeatedly to 235°C, none of these materials exhibits a significant change in DMA T_g. However, when cycled repeatedly to 260°C, the dicy-cured materials show significant degradation in the measured DMA T_g, especially the high-T_g dicy-cured material.

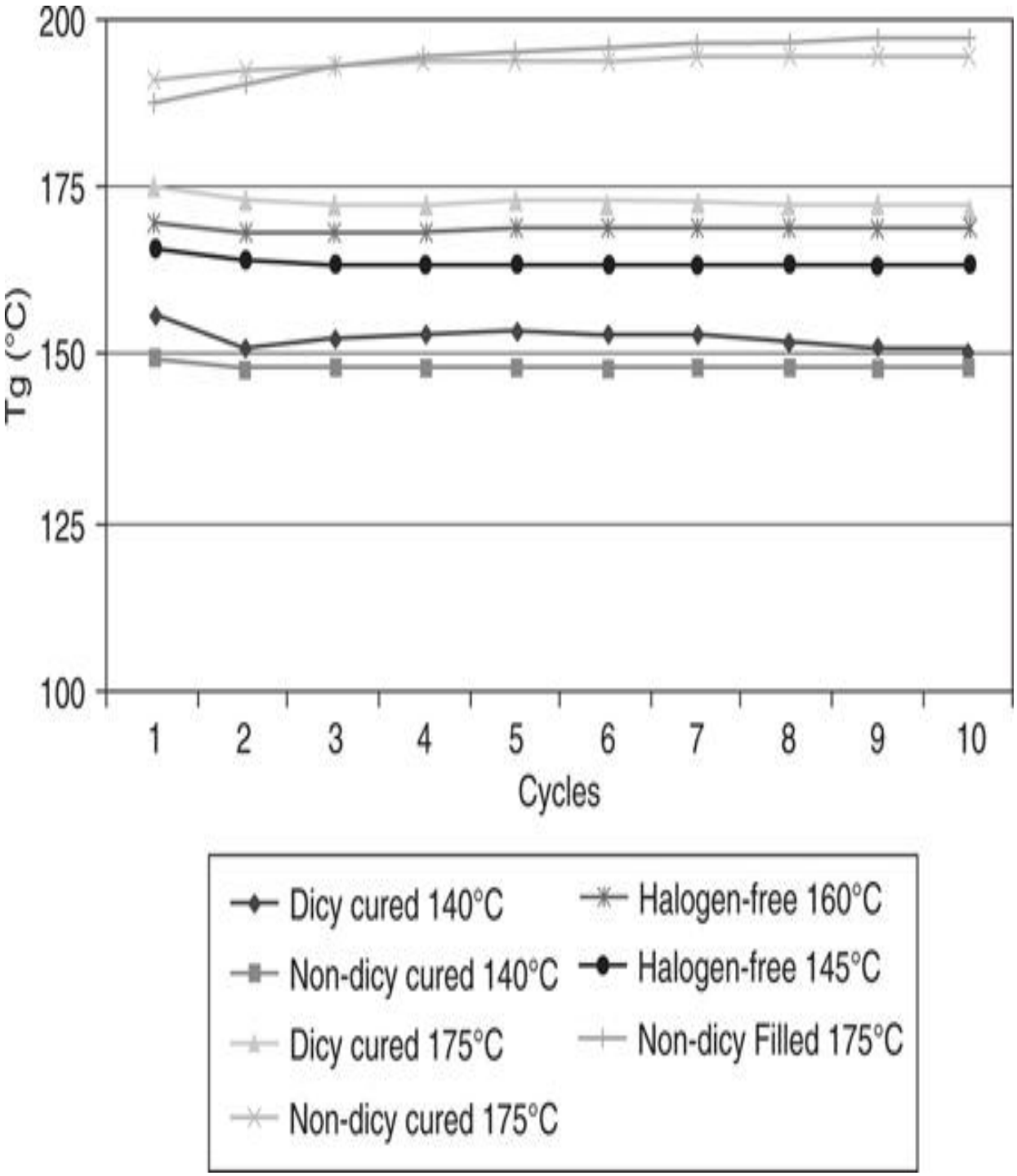


FIGURE 13.16 DMA T_g versus multiple thermal cycles to 235°C.

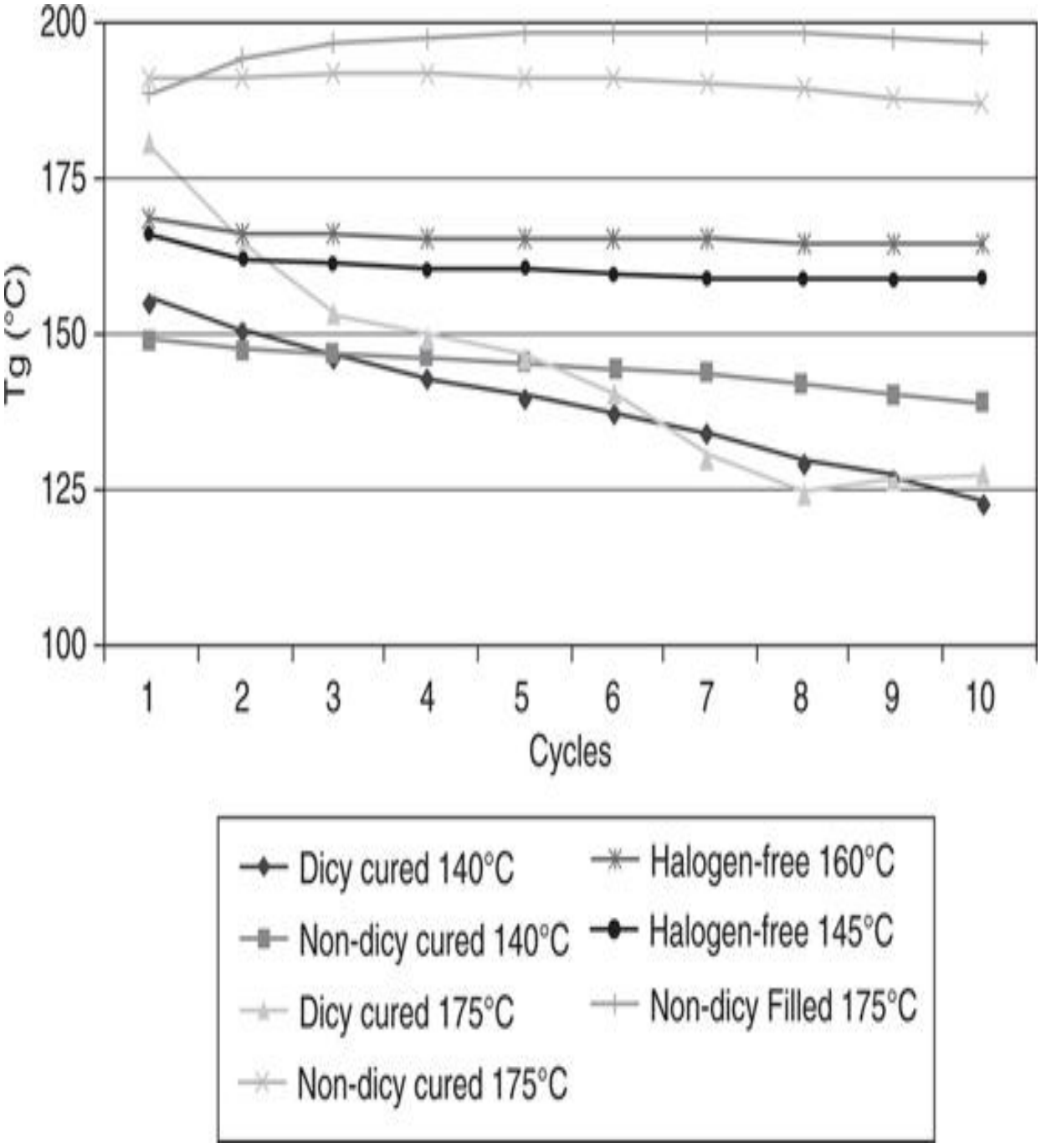


FIGURE 13.17 DMA T_g versus multiple thermal cycles to 260°C.

Figures 13.18 and 13.19 present similar data for measurements of the percent change in DMA modulus through multiple thermal cycles. Note that even when cycled to a peak temperature of 235°C, the high-T_g dicy-cured FR-4

material exhibits a consistent decline in DMA modulus. The 140°C T_g dicy-cured material exhibits a decrease only after several cycles.

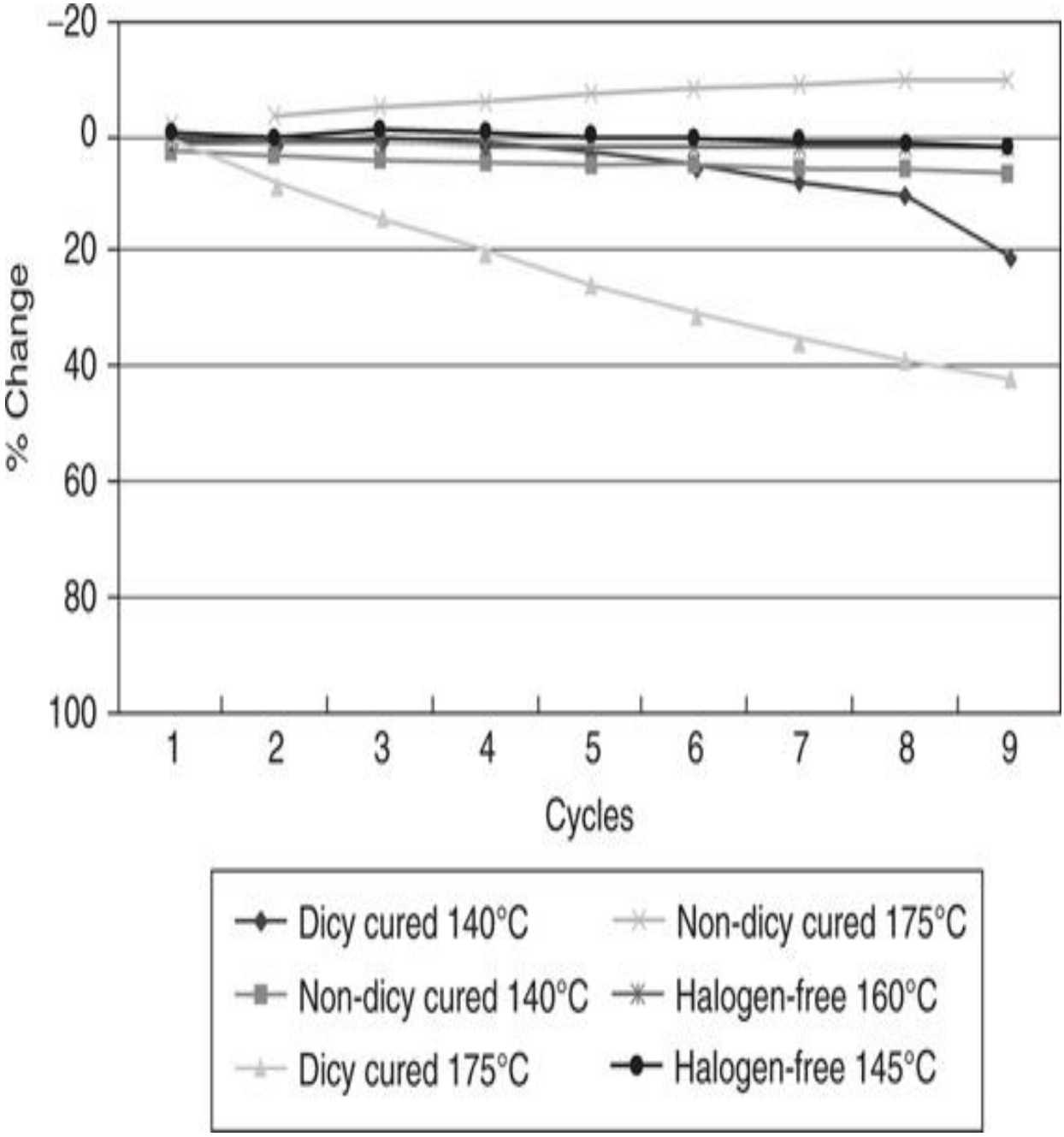


FIGURE 13.18 Percent change in DMA modulus versus multiple thermal cycles to 235°C.

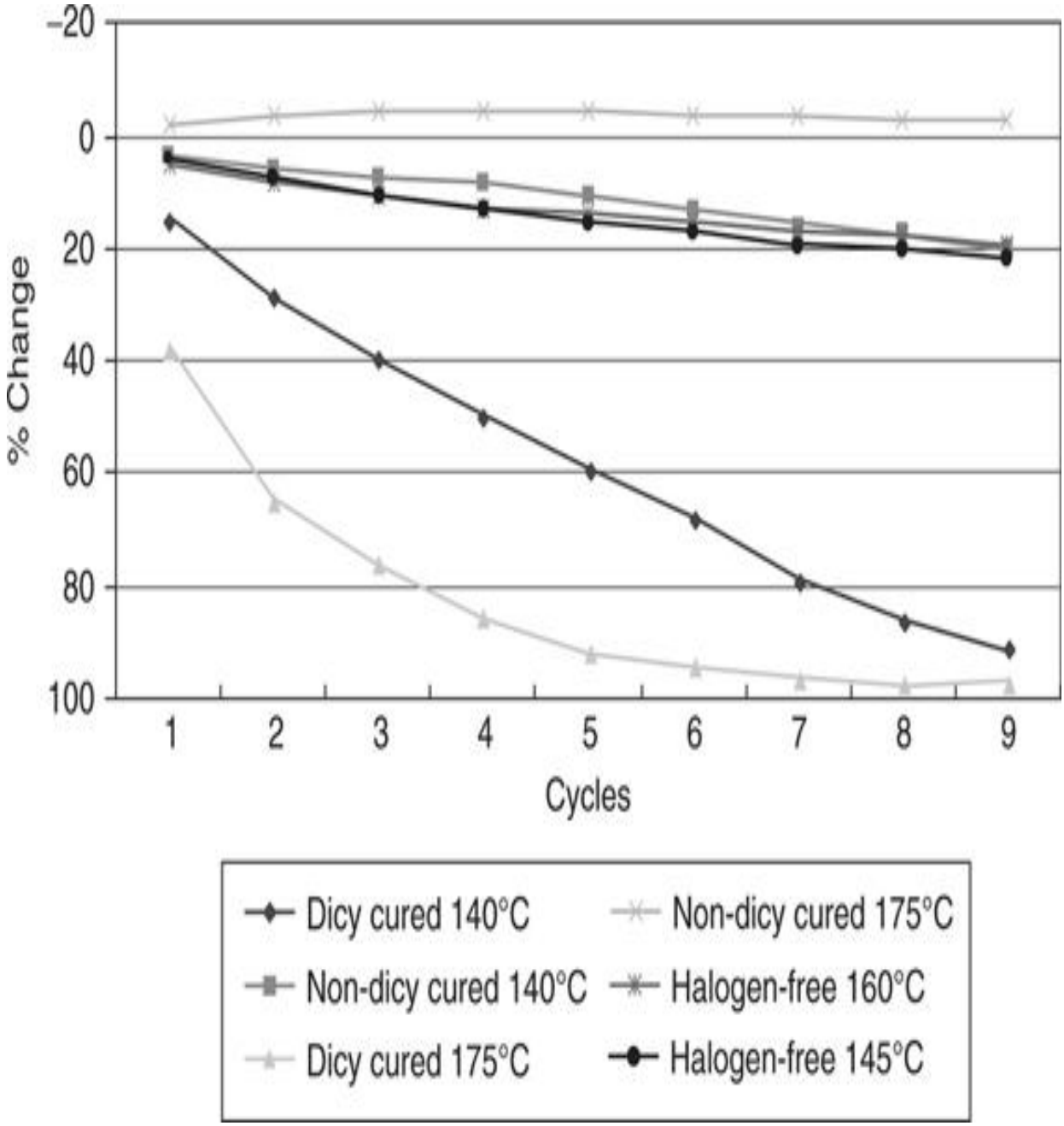


FIGURE 13.19 Percent change in DMA modulus versus multiple thermal cycles to 260°C.

When cycled to a peak temperature of 260°C, both of the dicy-cured FR-4 materials exhibit rapid declines in DMA modulus. In all of these cases, the nondicy (phenolic) FR-4 materials show little impact whether cycled to 235°C or

260°C. If anything, they exhibit very slight increases in T_g and modulus.

13.6 IMPACT ON PRINTED CIRCUIT RELIABILITY AND MATERIAL SELECTION

In addition to the works already cited, there have been excellent studies on the impact of lead-free assembly, specifically on PWB reliability. These works present statistical analyses showing the impact of lead-free assembly on PWB reliability and reach important conclusions regarding the base materials. Although there is not perfect agreement among all published works, the differences typically are the result of a different focus—for example, whether the focus is on complex, thick PWBs with stringent reliability requirements versus relatively less complex PWBs with shorter intended field lifetimes or less stringent reliability requirements. Conclusions include

- A minimum decomposition temperature is critical for lead-free assembly compatibility, but higher T_d's are not *always* better. Trade-offs with other properties, such as manufacturability, fracture toughness, and so on, make achieving the right balance of properties critical. Beyond a certain value, increases in T_d do not result in greater lead-free assembly reliability.
- T_g and CTE values are important because of the effects on thermal expansion, especially in thicker PWBs.
- Most dicy-cured high-T_g FR-4 materials are generally not compatible with lead-free assembly, or can be used successfully only in a very limited range of applications.

- Dicy-cured 140°C T_g materials may still be suitable for PWB designs with limited thickness and reliability requirements, particularly when intermediate peak temperatures are used in assembly. This is largely the result of these materials having slightly higher decomposition temperatures than the higher-T_g equivalents.
- Mid-T_g FR-4 materials with high decomposition temperatures are viable products for many lead-free assembly applications involving intermediate-complexity PWB designs.
- Materials with a sufficiently high-decomposition temperature, high-T_g, and reduced CTE values are suitable for the broadest range of applications, including complex PWBs assembled at 260°C peak temperatures.
- For reliability through assembly, total thermal expansion is important, which is affected by both pre-T_g and post-T_g thermal expansion values.
- For long-term field reliability, pre-T_g thermal expansion properties are more important as the temperature in the operating environment does not generally exceed the material T_g.
- Balancing material properties with PWB manufacturability is critical. Materials that exhibit excellent properties have failed because of difficulties experienced when fabricating the PWB, such as fracturing in drilling, routing or scoring, difficulty in texturing drilled holes for copper plating, resin recession, or hole wall pull-away during thermal stress.

13.6.1 Example of Material Types and Properties versus Assembly Reliability

To highlight a couple of these conclusions, consider the following test. First, multilayer PWBs made from the materials in Table 13.3 were processed through infrared (IR) reflow cycles at different peak temperatures. The PWB was a 10-layer, 0.093-in (2.6 mm) thick board “designed to fail,” meaning the copper weights and patterns, construction, and resin contents were chosen so that the board would be more sensitive to thermal cycles. In addition, the dwell time at the peak temperature was 1.5 minutes. This allowed differences in material performance to be detected more clearly. Figure 13.20 graphs the percentage of boards surviving six reflow cycles without any evidence of blisters, measles, or delamination.

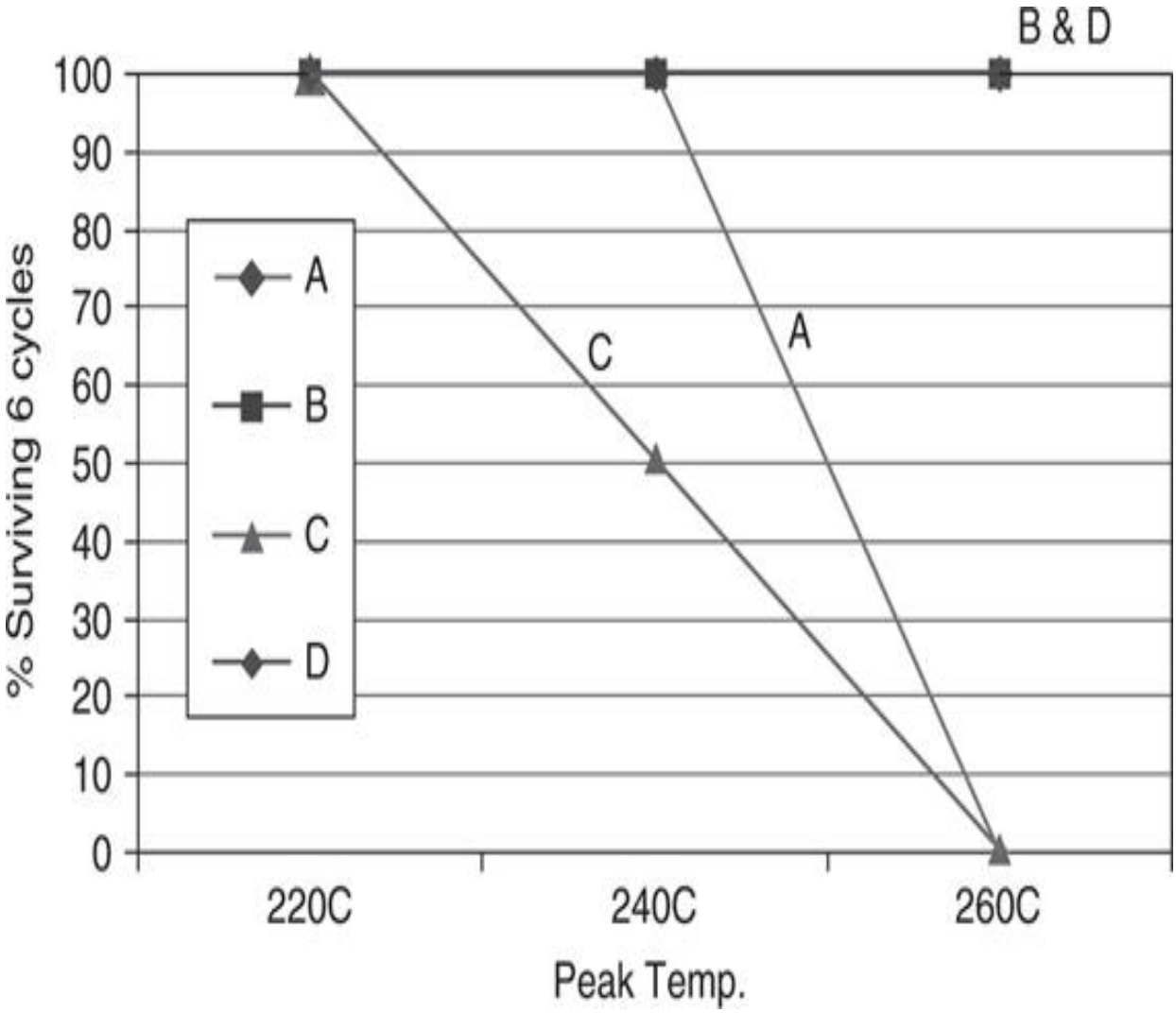


FIGURE 13.20 Survival after six reflow cycles at different peak temperatures.

Notably, the first material to exhibit defects is the conventional dicy-cured, high-T_g FR-4 material. This material began to exhibit defects when the peak temperature reached 240°C. At a peak temperature of 260°C, the conventional dicy-cured FR-4 materials, both the 175°C T_g and the 140°C T_g products, all exhibited evidence of defects. On the other hand, the materials with higher decomposition temperatures, both the 150°C T_g and the 175°C T_g products, all survived six cycles to 260°C.

13.6.2 Example of Material Types and Properties versus Long-Term Reliability

In another test, three high-T_g materials were evaluated through Interconnect Stress Test (IST) testing.[11] This particular test provided insight into the effect of thermal expansion and decomposition temperature on long-term reliability, as assessed by the IST method. The IST test method uses an electric current to heat test coupons that contain a network of plated through holes. The test samples are generally preconditioned several times to simulate exposure to assembly processes, and then cycled back and forth between an elevated temperature, most commonly 150°C, and room temperature. The samples are cycled in this manner until failure occurs, with failure generally being defined as a change in measured resistance of 10 percent. The materials evaluated in this example are described in Table 13.4.

TABLE 13.4 Materials Evaluated through IST Testing

Product	Description	Glass Transition Temp., °C	Decomposition Temp., °C	% Expansion, 50–260°C (40% Resin Content)
C	Conventional high-T_g	175	310	3.5
D*	High-T_g/high-T_d	175	335	3.4
D	High-T_g/high-T_d/ Reduced CTE	175	335	2.7

Note that the T_g values of these materials are the same, but differences exist in decomposition temperatures and

thermal expansion values. Product D* is similar to product D except that it has a higher level of thermal expansion. Product D* exhibits approximately the same thermal expansion as Product C, but Product D* has a higher decomposition temperature. Product D has both a high decomposition temperature and a very low level of thermal expansion. The PWB tested was a 14-layer, 0.120-in (3.1 mm) thick multilayer with 0.012-in (0.30 mm) diameter plated through holes. The average copper plating in the via was 0.8 mil (20.3 micron), although 1.0 mil (25.4 micron) had been requested. Figure 13.21 charts the average number of cycles to failure (10 percent resistance change in the plated via net) for each material type at each preconditioning level: as is (no preconditioning), three cycles to 230°C, six cycles to 230°C, three cycles to 255°C, and six cycles to 255°C.

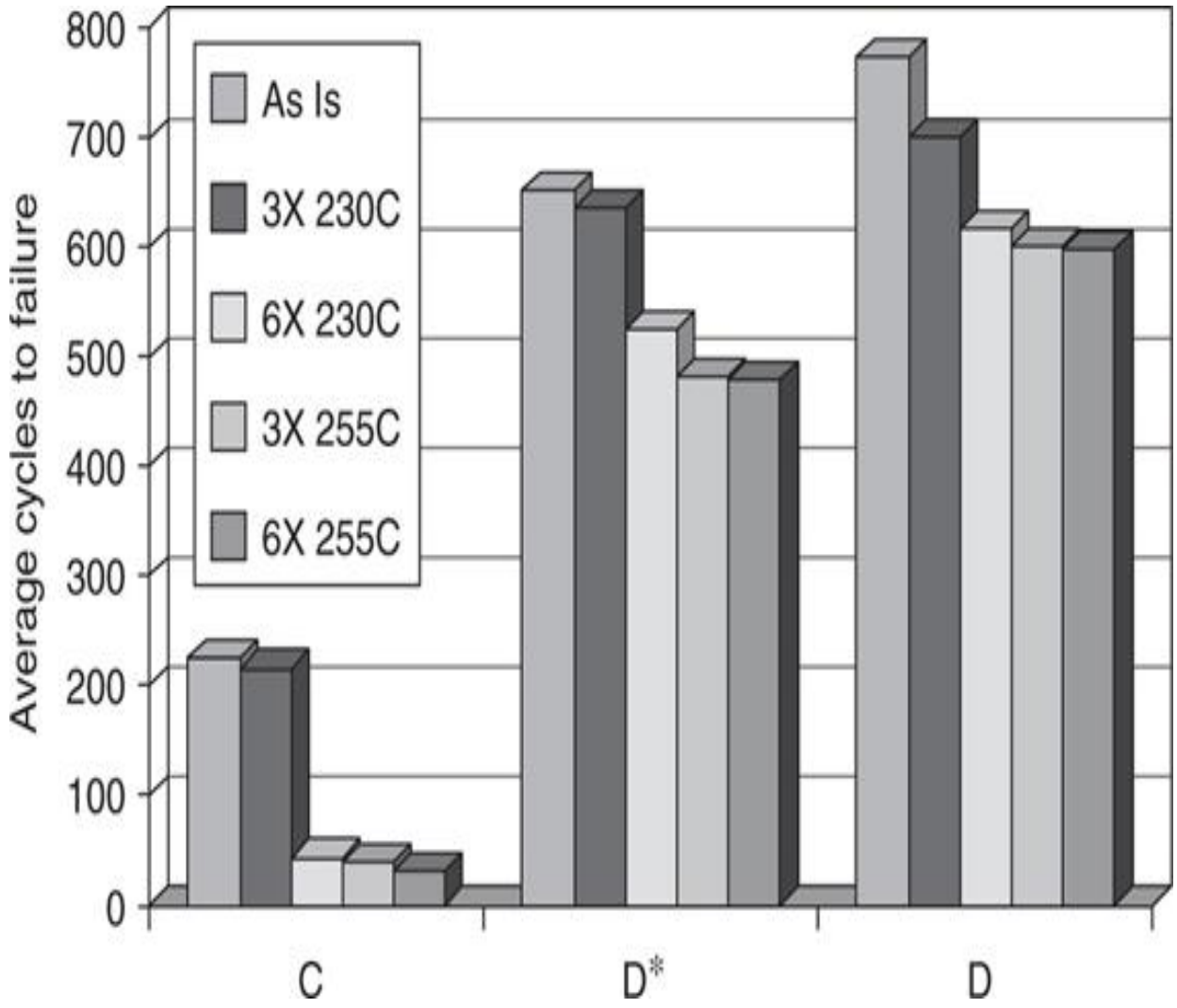


FIGURE 13.21 IST results for three 175°C T_g materials.

Clearly, the two materials with improved decomposition temperatures exhibit much better performance than the conventional high-T_g product. Also, in comparing product D to product D*, it appears that the lower thermal expansion of product D does offer improvement in the number of cycles to failure, but this improvement is smaller in comparison to the improvement due to the higher decomposition temperature, at least for this PWB design. The benefit of reduced thermal expansion becomes more important as the thickness of the PWB increases and as hole-to-hole pitch decreases.

As noted above, pre-T_g thermal expansion properties are especially important for long-term reliability, and other things being equal, materials with low pre-T_g CTEs will perform better than materials with higher pre-T_g CTEs in accelerated tests like IST. The High Density Packaging User Group (HDPUG) has also done extensive work in evaluating materials using more complex test vehicles, that among other things, compares multilayer PCB stack-ups with different levels of resin content, and therefore different levels of thermal expansion.

13.6.3 Understanding the Potential Impact on Electrical Performance

Most of the FR-4 laminate materials developed for lead-free assembly applications use an alternative resin chemistry in comparison to the dicyandiamide (dicy) cured FR-4s which were prevalent in the past. The most common FR-4 epoxy materials used today are commonly referred to as phenolic or novolac cured materials. Although there is some variation between these materials, as a group they tend to exhibit somewhat different electrical performance, particularly with respect to dielectric loss, or D_f (dissipation factor). For many applications the differences are not critical. However, as operating frequencies increase these differences can become very significant. Table 13.5 includes the same materials as Table 13.3, but also shows the differences in dielectric constant (D_k) and dissipation factor (D_f). It also includes a lead-free-compatible material designed to improve D_k and D_f performance in comparison to the phenolic lead-free-compatible materials. Note that different types of measurement systems can result in different measured values for D_k and D_f. Laminate resin contents and other factors also influence these properties. So when

examining Table 13.5, the comparisons between these materials are more important than the absolute values reported for each material. For these comparisons, the same measurement system and resin contents were used.

TABLE 13.5 Properties of Several Base Material Types

Product	Description	Glass Transition Temp., °C	Decomp. Temp., °C	% Expansion, 50–260°C (40% RC)	D_k@ 2 GHz	D_k@ 5 GHz	D_f@ 2 GHz	D_f@ 5 GHz
A	Dicy-cured 140°C T_g FR-4	140	320	4.2	3.9	3.8	0.021	0.022
B	Phenolic mid-T_g FR-4	150	335	3.4	4.0	3.9	0.026	0.027
C	Dicy-cured high-T_g FR-4	175	310	3.5	3.8	3.7	0.020	0.021
D	Phenolic high-T_g FR-4	175	335	2.8	3.9	3.8	0.026	0.026
E	Nondicy, nonphenolic	200	370	2.8	3.7	3.7	0.013	0.014

From this table it is clear that the thermally improved phenolic FR-4 materials are not quite as good in terms of electrical performance in the range of 2 to 5 GHz as the dicy-cured materials, particularly with respect to D_f. However, material E exhibits excellent thermal properties as well as good electrical performance.

13.7 SUMMARY

While most base materials comply with the RoHS directive, the question of compatibility with lead-free assembly processes is a more complex issue. The material properties that are important for lead-free assembly compatibility include

- Decomposition temperature (T_d)
- Coefficients of thermal expansion (CTEs)
- Glass transition temperature (T_g) (especially because of the impact on thermal expansion)
- Moisture absorption
- Time-to-delamination performance, which is not a fundamental material property, but is a simple method used to assess thermal stability of a composite material at different temperatures

While laminate manufacturers can easily make improvements in one of these properties, it is not as easy to make improvements without affecting other properties, including properties important for ease of manufacturing in the PCB fabrication process. Achieving the optimal balance of properties that consider the requirements of each level of the supply chain—from OEM to EMS to PCB fabricator—is crucial for success in lead-free assembly applications.

Dicy-cured FR-4 materials, especially the high-T_g dicy-cured materials, are significantly impacted by lead-free assembly temperatures, and are generally not recommended for lead-free applications. Phenolic-cured FR-4 materials, and particularly those containing inorganic fillers to reduce thermal expansion, have gained widespread acceptance in these applications. Nondicy, nonphenolic materials that offer good thermal and good electrical performance have also

been developed for lead-free applications where improved electrical performance at high operating frequencies are required.

13.8 FURTHER READING

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Smetana, Joe, Birch, Bill, Rothschild, Wayne, “A Standard Multilayer Printed Wiring Board for Material Reliability Evaluations.”

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CHAPTER 14
SELECTING BASE MATERIALS

Edward Kelley
Douglas Trobough
Isola Group, Chandler, Arizona

14.1 INTRODUCTION

The selection of the best base material for a given application can be very complex, particularly as circuit design complexity increases. To best approach this decision, it is important to understand the design parameters, the usage requirements, and the electrical performance requirements. Once these performance factors are understood, choosing the best material(s) can proceed in an orderly manner.

In performing this assessment, it is good to determine what performance factors are changing compared to designs currently in production. If the performance factors are essentially unchanged, continue with materials successfully used on prior designs. If the performance factors are being changed, focus on the changes to determine the required material type(s).

Material Qualification testing has become quite common at both large OEMs and PCB fabricators. The purpose of these qualifications is to create a “performance window” for a qualified material. Material qualification performance windows can be compared with the PCB design and performance requirements. If the performance requirement falls within currently qualified material performance window, then it can be selected. Qualification testing has been very successful at simplifying the material selection process.

A reference table of some performance factors is provided in Table 14.1:

TABLE 14.1 Performance Factor Examples in Selecting Materials

	Factor	Measurement	Effect
Design Parameters	Circuit Density	Hole Grid Pitch mm	Pitch ↓ Thermal Requirements ↑ CAF ↑
	Number of nets	Layer Count	Thickness + Resin content ↑ Thermal Requirements ↑ Hole Life ↑
	Thickness	mm	Thickness ↓ Thermal Requirements ↓ Hole Life ↓
	Size	Length x width	Size ↑ Thermal Requirement ↑
	Component Type	Thermal Mass	High Thermal Mass ↑ Thermal Requirements ↑
Usage Requirement	Office Environment		Standard Requirements IPC
	Outdoor usage	Temperature range	CAF Hole Life
	Use Temperature	Max Temperature	Thermal Reliability Hole Life
Elertrical Performance	Maximum Data Rate	Gb/sec	Frequency ↑ Loss ↑
	Frequency	GHz	Data rate ↑ Loss ↑
	Loss Budget	Db/in(mm)	Db/in(mm) ↓ Loss ↑
	Skew Budget	psec	Skew budget ↓ Micro Dk uniformity ↑

↓ factor reducing, requirements becoming easier
↑ factor increasing requirements increasing

Often, changes in performance requirements relate to thermal reliability, electrical performance, and CAF performance. With thermal reliability, there are two general considerations. First, the PCB must survive assembly processes, and the conversion to lead-free assembly makes this a much more challenging consideration as discussed in previous chapters. Second, the PCB must meet the requirements for reliability in the operating environment. In terms of electrical performance, the focus is on signal integrity as operating frequencies and data rates increase.

Finally, as circuit feature distances decrease, in particular hole wall-to-hole wall distances, CAF resistance becomes a more critical consideration. Each of these topics was discussed in previous chapters, so the emphasis in this chapter is to discuss how to approach base material selection with these performance requirements in mind.

14.2 SELECTING MATERIALS FOR THERMAL RELIABILITY

Chapter 13 discussed the impact of lead-free assembly on printed circuit boards (PCBs) and base materials, and also discussed many of the critical base material properties relevant to performance in lead-free applications. Refer to Table 12.2 for a summary of some of the key material properties:

- Decomposition temperature (T_d)
- Glass transition temperature (T_g)
- Coefficients of thermal expansion (CTEs)
- Moisture absorption
- Time to delamination, such as T260 and T288 tests

Also, the need to achieve the right balance of properties with ease of use in the PCB fabrication process, in addition to the requirements of assemblers and original equipment managers (OEMs), was highlighted.

This is the result of the impact that PCB fabrication can have on the performance of the material and finished PCB during assembly and in end-use application. A given material type offers a certain level of performance in the finished PCB. However, this level of performance may or may not be realized, depending on how the materials were processed

during fabrication. This makes it extremely complicated to make general recommendations on what material should be used in a given application. However, this section describes an approach in addressing this question. But first, some of the PCB fabrication and assembly issues that can affect performance are outlined.

14.2.1 PCB Fabrication and Assembly Considerations

The reliability of the assembled PCB in the end-use application is a function not only of the base materials selected, but how the materials were processed during PCB fabrication and component assembly. Different base material types may require different processing conditions in order to achieve the best results in the finished product. In reviewing these items, understand that these are general considerations that should be evaluated within the context of the specific fabrication and assembly processes and with regard to the specific materials being considered. The specific requirements for long-term reliability must also be considered. So while it is not possible to give exact, optimal processing conditions for all applications, the items that follow represent parameters that should be considered as products are converted to lead-free assembly.

14.2.1.1 Moisture Absorption. As discussed in Chap. 12, a given level of moisture absorption can be much more serious in lead-free assembly applications than it is for conventional tin-lead assembly applications. This is due to the increase in water vapor pressure at the higher temperatures of lead-free assembly. Figure 14.1 is a graph showing the vapor pressure of water versus temperature. At lead-free assembly temperatures, the pressure is much higher, which causes substantially more stress within the

laminate and on the interfaces within the PCB, including resin-glass, resin-oxide, resin-copper, and resin-resin interfaces. As a result, additional drying or baking processes may be needed to drive off moisture prior to processes involving thermal cycles.

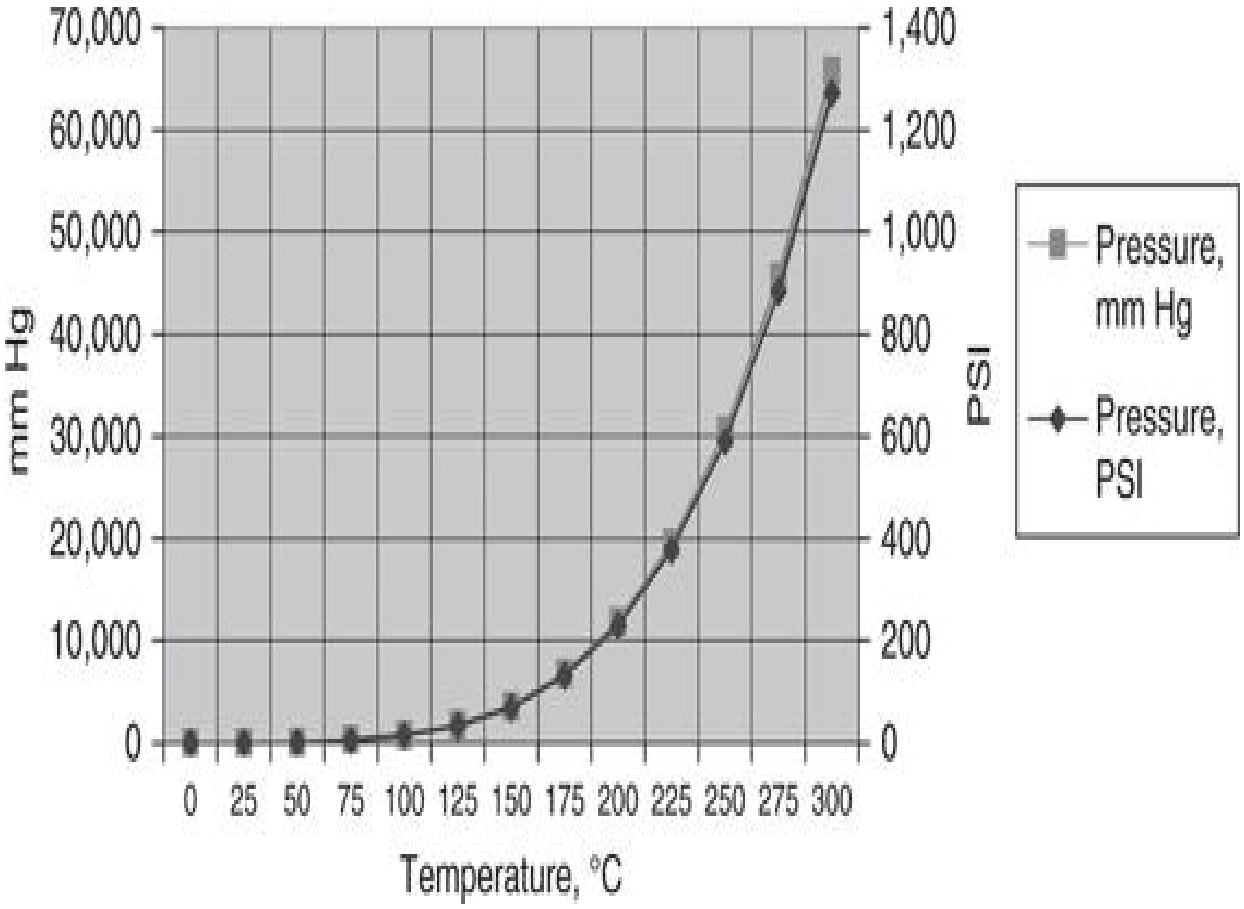


FIGURE 14.1 Vapor pressure of water versus temperature.

14.2.1.2 PCB Stack-Up. In terms of thermal reliability, one of the main considerations in selecting the stack-up of a multilayer PCB is to make sure that laminate and prepreg constructions use glass styles and resin contents suitable for the assembly environment. A particularly important consideration is to insure that prepreg resin contents are sufficient to fill innerlayer circuitry completely, and without resulting in what is called “glass stop,” where the fiberglass

cloth is pressed against the innerlayer circuit pattern, as discussed below.

A key factor in choosing the material BOM is the PCB stack-up. This factor crosses all material types, and requires some comments. There are two types of PCB materials: laminate and prepreg. Laminate is cured material with copper on both sides of the dielectic material. Prepreg is partially cured material that is the glue of the PCB.

Some important laminate choice factors:

- Laminate material is more consistent in thickness control than prepreg, particularly laminates made with a single ply of glass. This leads to improved control for electrical properties, particularly impedance. Making the laminate thinner than the prepreg layer takes full advantage of the increased thickness uniformity.
- Laminate material is made in a variety of thicknesses and glass constructions, which have differing electrical properties, in most materials. If the design has demanding electrical performance requirements, the electrical properties of different laminate types needs to be considered in making the selection.
- On thin laminate materials (<100 microns thick) used between planes at differing voltages, it is common to use laminate made with two plies of glass. This is more expensive than laminate built with one ply of glass.

Some important prepreg choice factors.

- The main purpose for prepreg is to fill the areas between copper features with resin and glue the laminate circuit layers together. It is very important that there be enough resin available to fill all the areas between copper features and provide a little extra to create a buffer between the glass and copper layers. While the reliability impact of this phenomenon can vary across material types, it is a best

practice to design the stack-up so that there is at least some resin buffer between the innerlayer copper pattern and the fiberglass cloth. Figure 14.2 shows two different PCB designs exhibiting glass stop. The cross section on the left of Fig. 14.2 shows a more minor case of glass stop while the cross section on the right, which is a design with very heavy copper weight on the innerlayer, is severe glass stop. Glass stop represents a reliability concern for both thermal reliability as well as CAF resistance. Lack of resin is one of the more significant causes of design failures during assembly and in field usage.

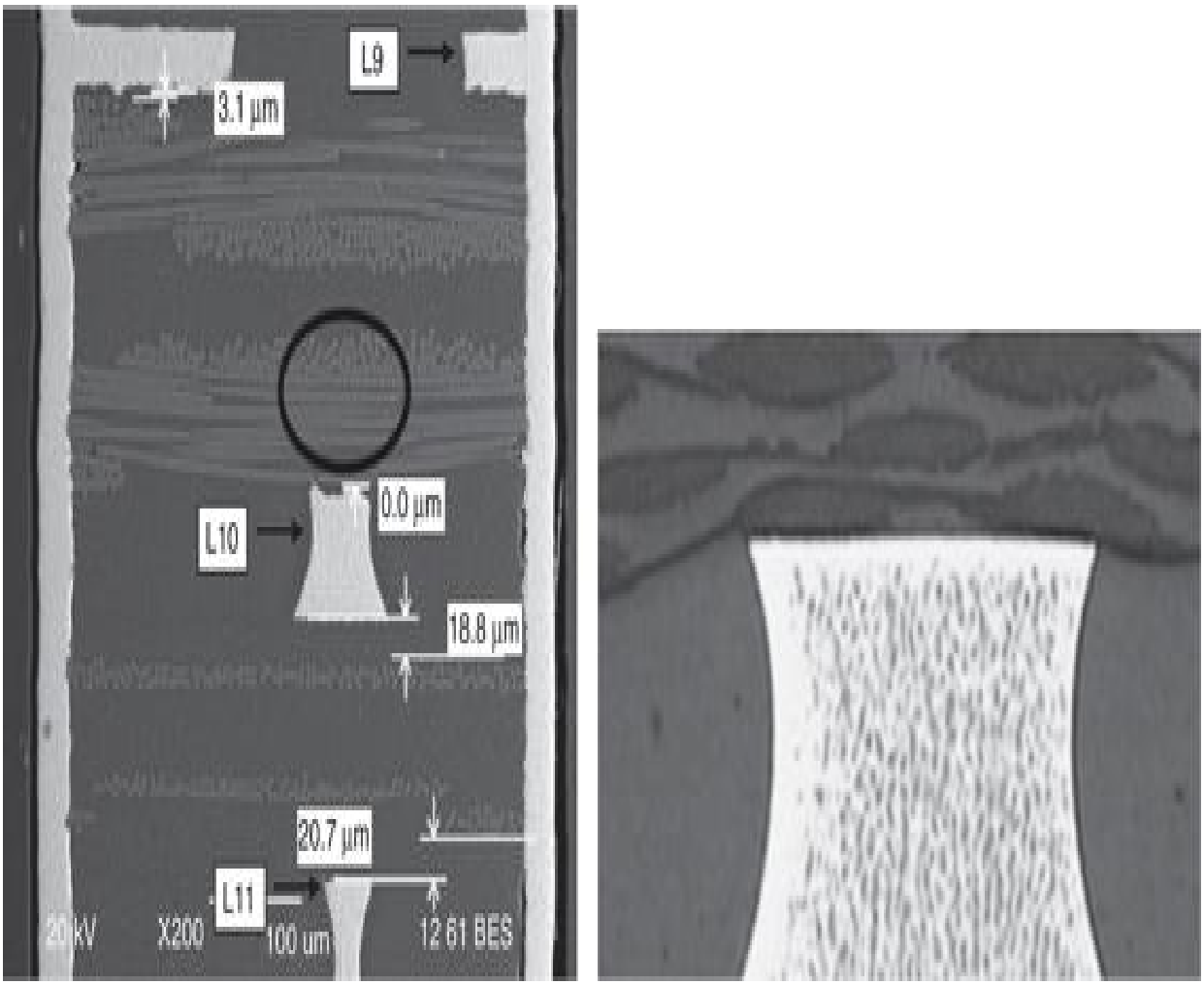


FIGURE 14.2 Cross sections exhibiting “glass stop.”

- For cost and control purposes the use of a single ply of prepreg is preferred, in most cases. It is important to make sure that this single layer has adequate resin, per previous point. Thin single ply is higher risk between plane layers with different voltages.
- Large areas without copper, or with significantly reduced copper content on plane layers can be a serious problem on higher layer count or boards with thick copper. These areas require a lot of resin to fill and often lead to glass-stop and even resin voids. In some cases these areas of the PCB will be much thinner than average leading to PCB processing problems or assembly issues. Add copper fill in these larger open areas when allowed to the design. If not allowed, choose prepreg types with additional resin volume.
- Most suppliers sell prepreg by resin content. This value is based on weight and not on volume, so different types of materials will have different resin volume for the same resin content. Prepregs should be selected by glass style and thickness. The available resin for fill is prepreg thickness—glass thickness.

CTE mismatches between layers can also be a concern if adjacent dielectrics have very different resin contents or if dissimilar resin systems with very different CTE and modulus values are used. While not usually a dominant consideration, this should be considered when designing the multilayer stack-up in particularly demanding applications. Table 14.2 contains examples of X-Y CTE values for some common glass styles.

TABLE 14.2 *X*- and *Y*-Axis CTE Values for Some Common Glass Styles

Glass Style	X-Axis CTE	Y-Axis CTE
106	22.2	22.2
1080	16.9	19.4
2113	14.3	14.9
2116	14.7	14.9
1652	14.1	14.1
7628	12.1	14.9

14.2.1.3 Oxide and Oxide Alternative Processes.

During PCB fabrication, the internal copper surfaces are generally chemically treated to improve the adhesion between the resin system and the copper layer. Two primary types of processes are used. The first involves an oxidation of the copper surface to micro-roughen the surface, usually followed by a reduction step to improve chemical resistance of this layer in subsequent processes. The second type of process is referred to as an oxide alternative, or oxide replacement process. These processes generally use etching chemistries, which also roughen the copper surface to provide greater surface area for resin bonding, and often use proprietary chemistries designed to further enhance adhesion and chemical resistance. In short, compatibility of the resin system with the oxide or oxide alternative is critical for any application, but becomes even more important in lead-free assembly applications due to the increased stress on the resin to innerlayer copper bond. The reduced oxides can also be degraded at higher temperatures, and this degradation can be influenced by the type of resin system and temperature at which the resin system must be laminated at. Functional testing of the

compatibility of the resin-to-oxide/oxide alternative surface is recommended.

14.2.1.4 Multilayer Lay-Up Prior to Lamination. In addition to the oxide and oxide alternative processing discussed in the previous section, the hold time between this process and multilayer lay-up and lamination is also important. This is due not only to the possibility of oxidation of the innerlayer surfaces, but to the potential for moisture absorption by the exposed resin surfaces on the innerlayer, for the reasons already discussed. For some high performance resin systems, moisture may also interfere with resin curing reactions, making it even more important to dry the cores prior to lamination.

So the hold time between surface preparation and lamination should be minimized, and the storage of the innerlayers prior to lay-up should be in a temperature- and humidity-controlled environment to reduce the likelihood of absorbing moisture. Typical environmental conditions for this storage are 68°F or 20°C, and a maximum of 50 percent relative humidity (RH), although lower humidity levels are recommended.

Similarly, the prepreg materials used in constructing the multilayer PCB must be stored in a temperature- and humidity-controlled environment. This is due not only to the potential for moisture absorption, but also because the shelf life and performance of the prepreg can be significantly impacted by temperature and humidity conditions prior to use. This can often be a subtle point, but it is a critical one, especially as lead-free applications demand greater performance from the base materials. Again, storage conditions generally should be no worse than 68°F or 20°C and 50 percent RH for typical FR-4 materials, although some high-performance materials can be even more sensitive and perform better if stored in even cooler or drier environments. Some of the high-performance materials may even require

vacuum desiccation prior to use. This is a fairly common practice for polyimide materials, for example. Finally, storage of the multilayer books prior to lamination should ideally be done in a controlled environment, with the hold time between lay-up and lamination also minimized.

14.2.1.5 Multilayer Lamination Processing. Multilayer lamination cycles must be designed around the specific material being used. However, there are some general recommendations that can be applied to most materials:

- *Prelamination vacuum*. Expanding on the discussion of moisture absorption, it is important to apply a vacuum to the lamination books prior to ramping up the temperature and curing the resin in the prepreg. This removes moisture that could volatilize during the lamination cycle. Drawing a vacuum can also remove other volatile components such as residual solvents in the prepreg materials. This is an often overlooked factor that can be vitally important. Recommended vacuum times can depend on the actual moisture levels of the materials used, but generally range from 15 to 30 min. It is important during this time that the materials are not heated too much. In addition, as mentioned in the previous section, some materials, such as polyimides, are often vacuum-desiccated prior to lay-up.
- *Heat rise and pressure application*. For a given type of resin system, it is important to understand the rheology of the resin in the prepreg as a function of the rate of temperature rise. This, along with the proper application of pressure, ensures adequate filling of the internal circuitry and good wet-out of the resin into the fiberglass filaments. Complete wet-out of the internal circuitry and good resin flow on the oxide or oxide alternative surface are important for reliability in subsequent thermal cycles. This is also discussed in Sec. 14.2.2.2.

- *Stress relief pressure profiles*. It is important to have sufficient pressure on the lamination book, as the resin in the prepregs are heated and begin to flow into the innerlayer circuit patterns. The actual pressure needed can vary with the type of material being used and the level of vacuum achieved during the process. However, after the resin cures to a certain point and stops flowing, a reduction in pressure can help reduce the levels of stress in the multilayer PCB. This can improve reliability in subsequent thermal cycling. The reduction in pressure is typically to the range of 50 to 75 psi.
- *Cool down rate*. After the product has been held at the proper temperature for the proper period of time, which will depend on the type of material used, the rate at which the product is cooled is also important. In general, slower cooldown rates will minimize warpage and residual stress in the finished product. However, slower cooldown rates can adversely impact productivity, so a reasonable balance must be identified. In many cases, a slow cooldown through the T_g of the resin system, followed by a somewhat faster cooling rate after the product cools below T_g, represents a good balance of performance and productivity.

14.2.1.6 Drilling. Many of the materials designed for compatibility with lead-free assembly, as well as those developed for high-speed/high-frequency applications, require optimization of drilling parameters. These resin systems can have higher modulus values and be harder, impacting not only the optimal drill parameters but accelerating drill wear and leading to lower acceptable hit counts.

14.2.1.7 Desmear Processing. Many of the resin systems in volume use today are more chemically resistant than the materials used in the past. Adjustments may be

needed in the times and/or temperatures used for solvent swelling and permanganate desmear processes, and the supplier of these chemistries should be consulted when transitioning to new materials. The processing guidelines provided by the laminate material supplier will also typically provide recommendations for desmear processing. For many advanced products, plasma desmear may be required. This is true for most high-speed materials.

14.2.1.8 Surface Finishes. If a lead-free hot air solder leveling (HASL) process is used, the higher temperatures required by the lead-free alloys should be considered when selecting the base material. The common alternatives to HASL typically do not involve a bake process or significant thermal cycle. Although this is good in terms of the reduced thermal cycling exposure to the base material, it also results in one less opportunity for moisture to be removed from the PCB prior to assembly. This should be considered when deciding whether a drying step is needed prior to assembly.

14.2.1.9 Assembly Temperatures. Given that there is a range of temperatures used in assembly processes, including lead-free assembly processes, it is critical that the base material be selected knowing what the peak assembly temperatures will be. In the lead-free assembly temperature range, seemingly small differences in temperature can have significant impacts on both reliability in assembly as well as long-term reliability. For example, many materials that are perfectly acceptable for assembly at 245°C will not be suitable at 260°C, depending on the PCB design features such as hole-to-hole pitch, copper weights used, etc.

14.3 SELECTING A BASE MATERIAL FOR THERMAL RELIABILITY

14.3.1 Overview of Test Vehicles and Test Methods

A very common request from PCB fabricators, electronic manufacturing services (EMS) companies, and OEMs is whether a given material is compatible with lead-free assembly. Although everyone is looking for a simple answer, the solution becomes complex because of the range of PCB designs (board thicknesses, layer counts, copper weights, via pitch, and so on) as well as the differences in lead-free assembly processes, such as the specific peak temperature and number of thermal cycles a PCB will experience. In addition, people usually want to use the least expensive material that is suitable for a given application. So although it is easy to specify an advanced product for lead-free compatibility, the approach taken here is to balance cost and performance.

There are a variety of test vehicles and test methods used to assess thermal reliability of base materials at the PCB level. The variants exist because of the wide range of designs used as well as the wide range of requirements for long-term reliability. The reliability requirement for a PCB used in a cell phone or other consumer electronics device that is used for a relatively short time frame will be different than for a network infrastructure device that will be in service for decades, or for an automobile, or in aerospace and avionics applications. As such, a full discussion of these test methods is beyond the scope of this chapter. However, we can outline approaches to material evaluation, qualification and selection based on some common industry practices, which include

- Using test vehicles or actual PCB designs that represent certain levels of PCB technology and using these to evaluate new materials through multiple assembly processes at the temperatures of interest. The test

vehicles are inspected after different numbers of assembly simulations for blisters, delamination, or other defects. Testing is typically performed in the as-manufactured condition, and sometimes after temperature and humidity conditioning as well.

- These same test vehicles, or specially designed test vehicles are used to assess long-term reliability. Typically, specially designed coupons are used in the test vehicle or built along with the actual PCB design. These coupons are typically put through accelerated testing to assess long-term reliability, and typically focus on plated-through hole reliability. These coupons are often tested in the as-manufactured state as well as after different numbers of assembly simulations at different temperatures.
- There are multiple test methods used to assess long-term plated through hole reliability, including air-to-air thermal cycling and oil-to-oil thermal cycling. A very common test method in use today uses an electric current to repeatedly heat a sample to the desired temperature. The resistance of a series of plated holes is monitored as the test vehicle is thermally cycled, with failure usually defined as an increase in resistance of over 10 percent. “IST” testing, which was briefly described in Chap. 13, is one such test.[1] Figure 14.3 is an example of IST coupons. In this figure there are two coupons, one with a 1.0-mm hole-to-hole pitch, and a second with a 0.8-mm hole-to-hole pitch. In short, while the science behind the requirements for the temperature range and number of cycles to failure is beyond the scope of this chapter, the OEM will typically define the requirement based on the type of electronic device the PCB will be used in and how long it is designed to be in service. The coupon designs can also be used to evaluate performance of different hole sizes, aspect ratios and hole-to-hole pitch.

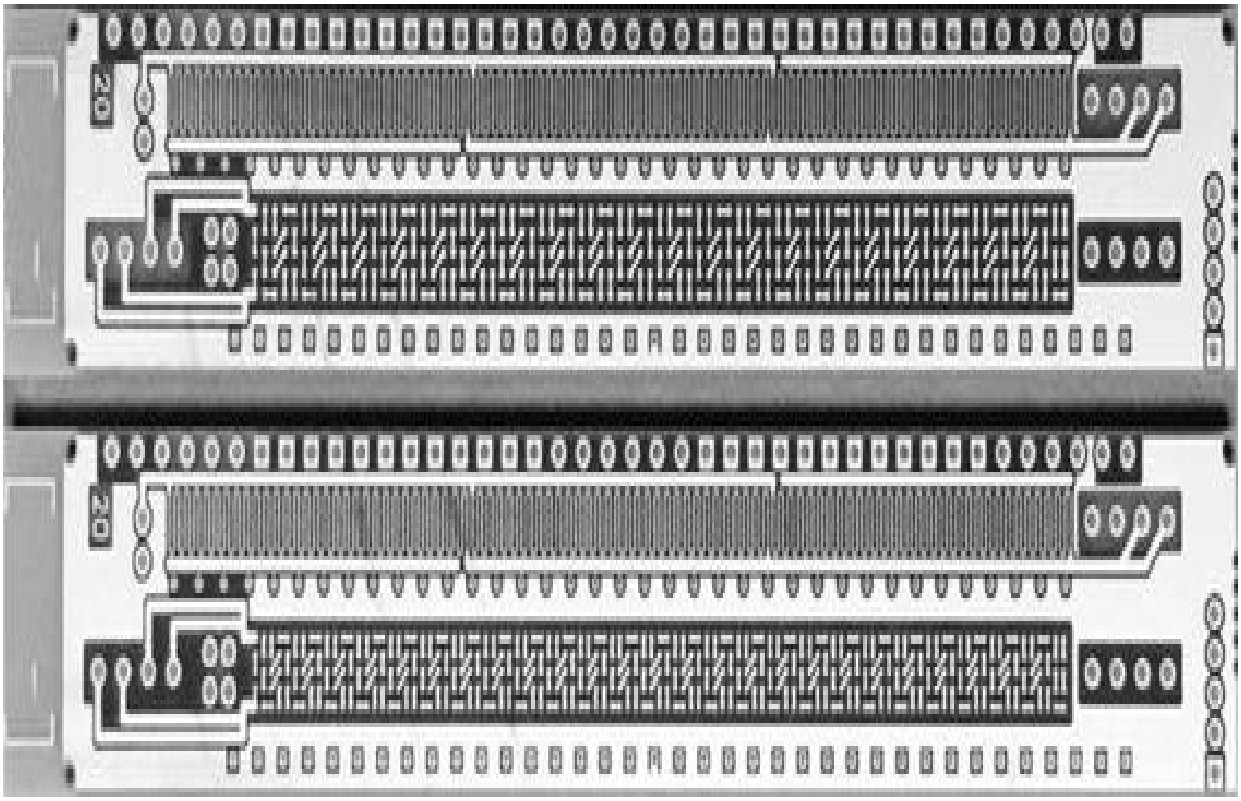


FIGURE 14.3 IST coupon used for thermal cycling testing.

- In the automotive industry for example, there are multiple levels of thermal reliability testing depending on the specific application of the PCB and the operating environment. Test vehicles are designed with layer counts, overall thickness, hole size and hole-to-hole pitch levels based on the design criteria to be used in the actual printed circuits. While some other industries have used only one or two test vehicle designs to qualify all materials, if the test vehicle is much more difficult than actual PCB designs, then the risk is over specifying the material, which can have significant cost impacts or reduce availability. As such, more and more OEMs are dividing qualification criteria into levels that represent certain ranges of PCB technology.

14.3.1.1 "Standard FR-4" Material Selection. As explained in Chap. 13, with the introduction of lead-free

assembly, substitutes for the dicy-cured FR-4 epoxy materials had to be developed and introduced. While some very simple lead-free applications still use these materials, in general they are not suitable for lead-free assembly applications. Phenolic or novolac-cured epoxies were developed to provide improved thermal performance in lead-free applications, and tested through the methods outlined above. Table 14.3 summarizes the performance of these materials.

TABLE 14.3 General Recommendations by Lead-Free Peak Temperature Range

Category	240–245°C Peak Temperatures	250–260°C Peak Temperatures
Dicy-cured 140°C T_g FR-4s	May be suitable for PCBs of limited thickness and complexity where a limited number of thermal cycles will be experienced.	Generally not recommended, but may be suitable for low-technology applications where a limited number of thermal cycles will be experienced.
Dicy-cured high-T_g FR-4s	Generally not recommended; even though initial results may be positive, extended storage in an uncontrolled environment prior to assembly could lead to problems.	Not recommended.
Phenolic mid-T_g FR-4s	Suitable for a broad range of applications because of the higher decomposition temperature and overall thermal expansion being similar to standard high-T_g materials.	Suitable for a broad range of applications because of the higher decomposition temperature and overall thermal expansion being similar to standard high-T_g materials. Consider higher T_g versions for thicker, more complex PCBs.
Phenolic high-T_g FR-4s	Compatible in the broadest range of designs and applications. Recommended when long-term reliability is critical.	Compatible in the broadest range of designs and applications. Recommended when long-term reliability is critical.

14.3.1.2 General Approach to Material Selection. With the many studies and reliability tests that have been performed on the conventional FR-4 epoxy materials, selection of these materials is relatively straightforward. However, as the demands for better electrical performance accelerate, and interest in halogen-

free materials grows, new materials are almost constantly being introduced. As such, there is often less industry experience with these materials to draw from, and furthermore, these materials can be more sensitive to variations in the PCB manufacturing process, in addition to variations in the PCB design. So while the approach to evaluating materials as described above is still valid, it is extremely difficult to give general recommendations. Industry groups such as the High Density Packaging User Group[2] (HDPUG) and the International Electronics Manufacturing Initiative (iNEMI) have sponsored many valuable testing programs to help build the knowledge base required.

In addition, most PCB manufacturers have their own testing programs that take into account the requirements of their end markets, the PCB designs they build, and the manufacturing equipment and processes they use, among other factors. So while there is no single method used in selecting materials, the example below provides a very general format used for determining which materials are suitable for different applications.

Since most PCB fabricators will manufacture a range of PCB designs, and often for various end markets, they need to develop a system for categorizing the acceptability of different materials in different applications. Some of the key variables include

- The peak reflow temperatures the PCB is exposed to in assembly and rework processes. As discussed in Chap. 13, there is a range of temperatures used for lead-free assembly processing, and seemingly small differences in temperature can have very significant impacts on reliability. It is common to categorize material compatibility at 245°C and 260°C, for example. While only a 15°C difference, this can be the difference between good results and bad.

- The number of reflow and rework cycles that a given PCB can be exposed to. As you would expect, the more exposures to reflow temperatures, the more thermally reliable a material needs to be. Common test requirements are 3 times (3×), 5×, 6×, 8× and up to 10×. As mentioned earlier, testing is sometimes performed after temperature and humidity conditioning as well.
- PCB layer count and thickness. With higher layer count, it is common for the individual dielectrics to be thinner and have higher resin contents. With higher resin content, more thermal expansion is experienced at reflow temperatures, as well as in thermal cycling tests designed to assess long-term reliability. In the thermal cycling tests for long-term reliability, the peak temperature is normally below the material T_g. As such, the pre-T_g CTE is a critical factor in these tests. As board thickness increases, the total thermal expansion will be greater.
- Plated through hole size, aspect ratio and hole-to-hole pitch. In general, as hole-to-hole pitch decreases, the demand for greater thermal reliability increases. As PCB thickness increases, this becomes more critical. Testing of PCBs at 2.5 mm thickness and above, with 0.8 mm hole-to-hole pitch and below, is a very active area for testing of new materials.
- Innerlayer copper thickness. In designs where innerlayer copper thickness can be 2 oz or greater, resin content selection and resin flow and fill properties become more important. The issue of glass stop was described in Chap. 13, and the potential for this condition increases as copper thickness increases. In addition, many of the resins used in new materials for high-speed/high-frequency applications have higher minimum viscosities when the resin is melted during the multilayer lamination cycle. As a result, it is more challenging to get good resin flow and fill into thick copper patterns. In addition, where multiple prepreg layers

are used to insure adequate resin volume for filling thick copper layers, a high resin viscosity can make it difficult for resin to flow through the fiberglass cloth and assist in filling the innerlayer circuit pattern, especially if there is little space between the yarns in the cloth. While the spread and expanded glass cloths have benefits for laser drilled via quality, signal integrity performance and resin-to-glass wetting for CAF performance, these glass styles are not preferred when there is a need to allow resin from adjacent prepreg layers to flow through a glass cloth to assist in filling the innerlayer circuit pattern. This also makes an understanding of resin melt viscosity important when designing a PCB stack-up and in setting up lamination cycles. Figure 14.4 is an example of a dynamic viscosity plot for a phenolic FR-4 epoxy. A sample of 106 prepreg is used in this example, with resin viscosity on the *x* axis and temperature on the *y* axis. Note how faster heat rise rates (1 to 3.5°C/min heat rise rates are shown) lead to lower minimum viscosities. Minimum viscosity decreases from 732 pascal-seconds (Pa-s) to 163 Pa-s in this range of heat rise rates. Figure 14.5 shows viscosity curves for two different material types at a 2°C/min rate of rise, and Fig. 14.6 shows the same materials with a rate of rise of 3°C/min. These used 2116 prepreg. Note the large difference in minimum viscosity between the two material types, as well as the decrease in minimum viscosity for both products as the rate of rise increases from 2 to 3°C/min.

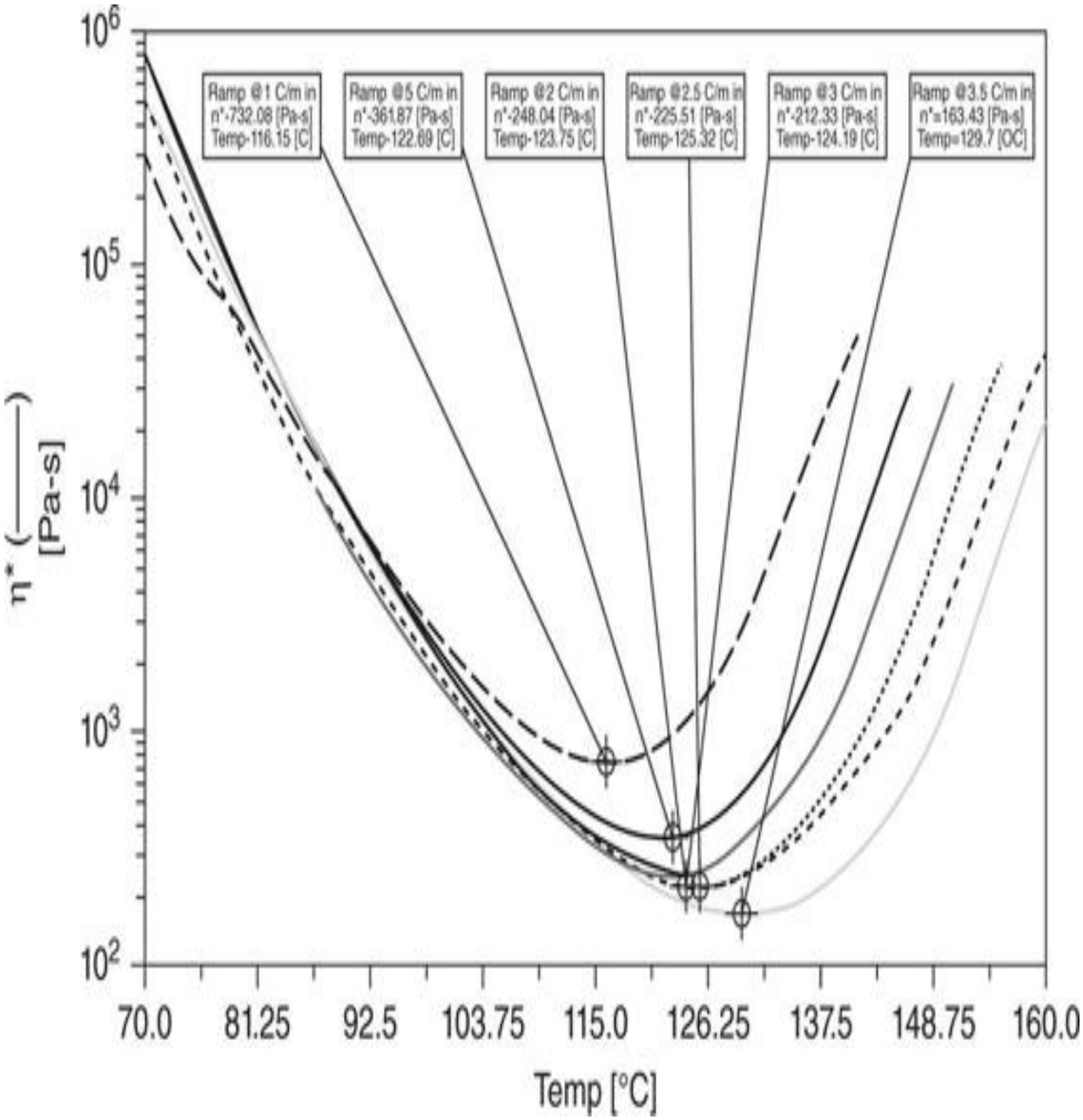


FIGURE 14.4 Dynamic viscosity curves for one material at different heat rise rates.

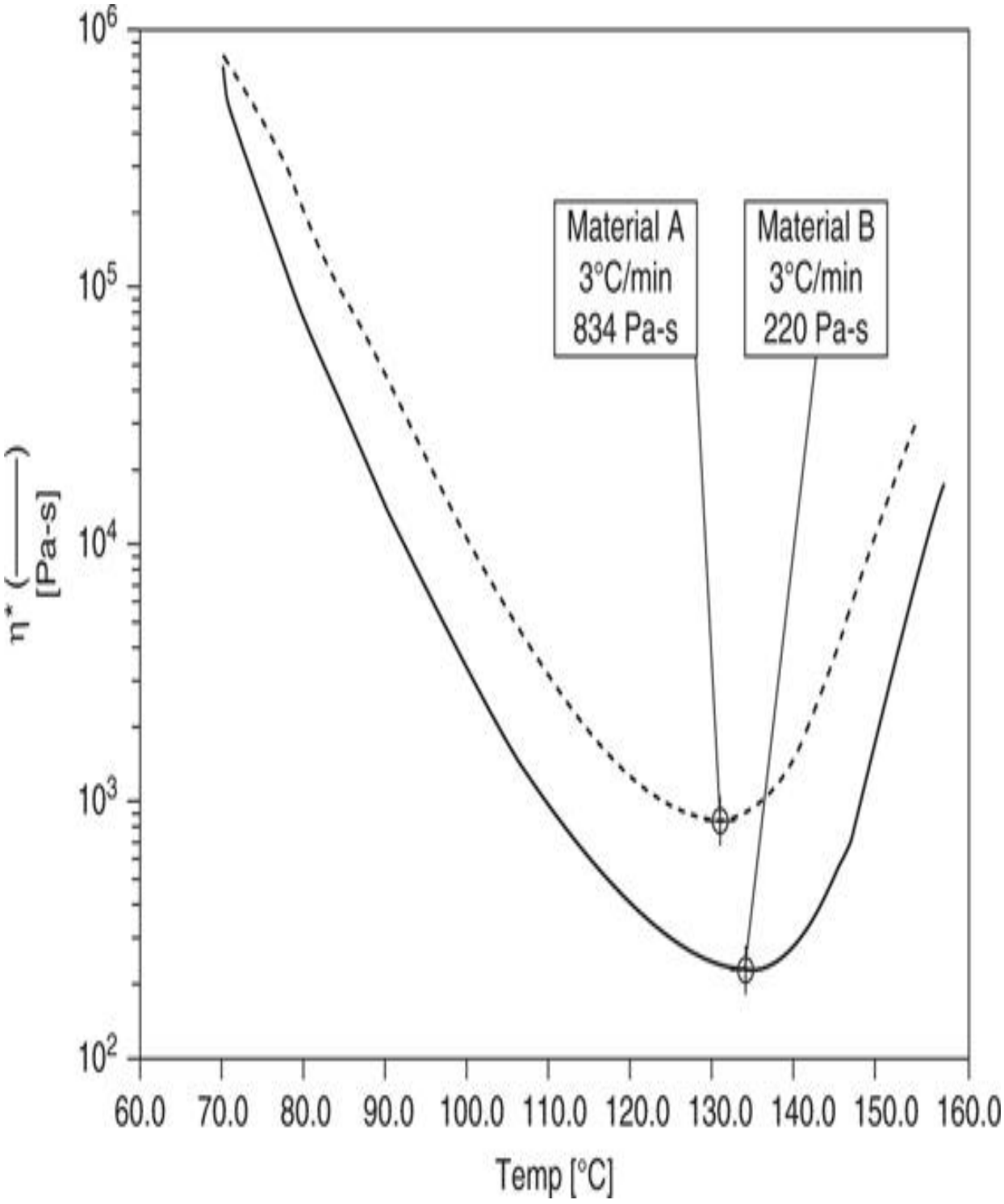


FIGURE 14.5 Dynamic viscosity curves for two different materials at 2°C/min heat rise rate.

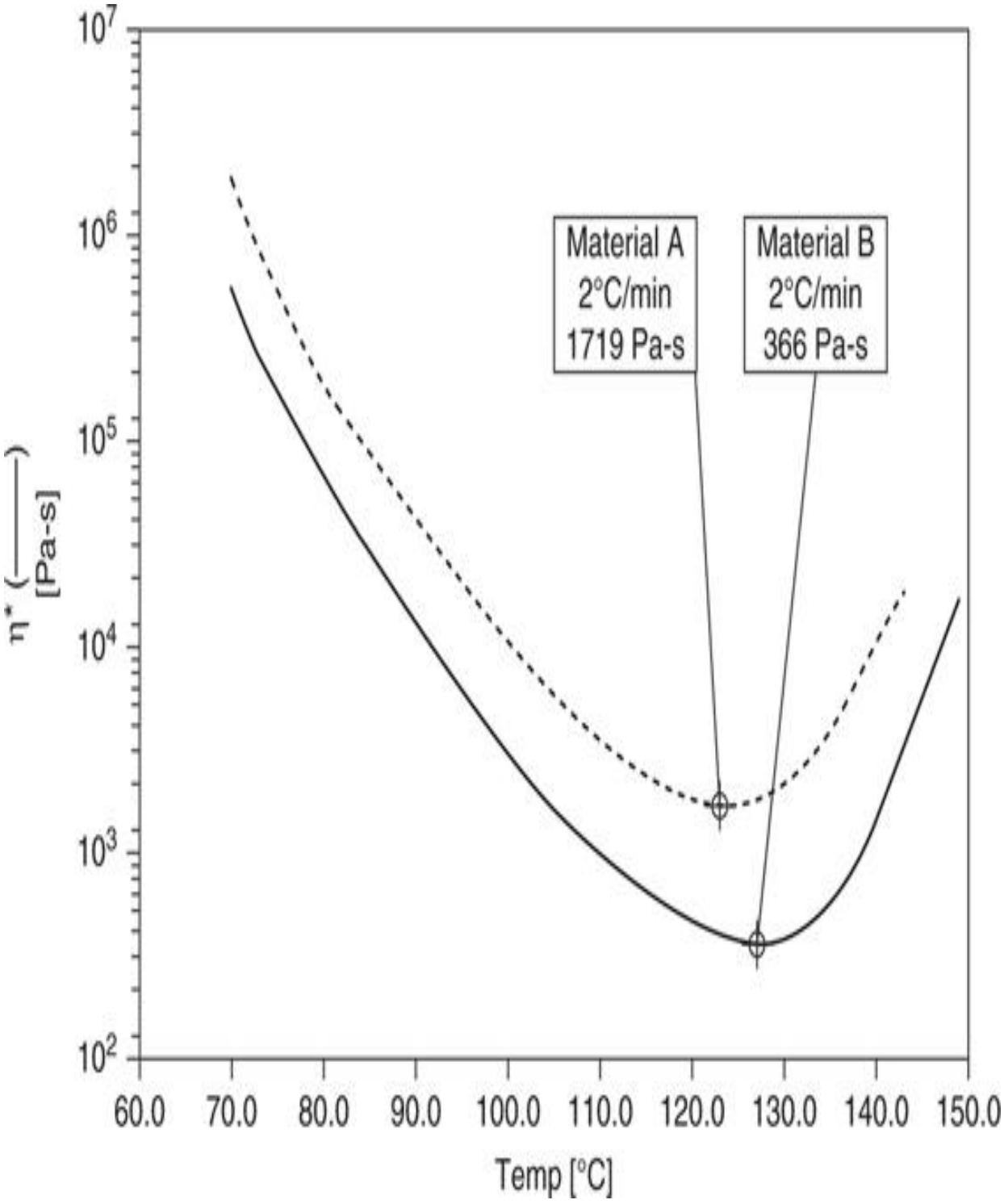


FIGURE 14.6 Dynamic viscosity curves for two different materials at 3°C/min heat rise rate.

With these variables in mind, and through the testing methods described earlier, one way to categorize material thermal performance is shown in Fig 14.7. Bear in mind that this is just one way to categorize performance across material types, and each manufacturer may devise their own system. Also, Fig. 14.7 is an arbitrary example. However, it is not unusual for some products to perform well at 245°C, but not perform as well at 260°C. Or some may be reliable at 1.0 mm pitch but be less reliable at 0.8 mm pitch, which may also depend on innerlayer copper weights or overall resin content.

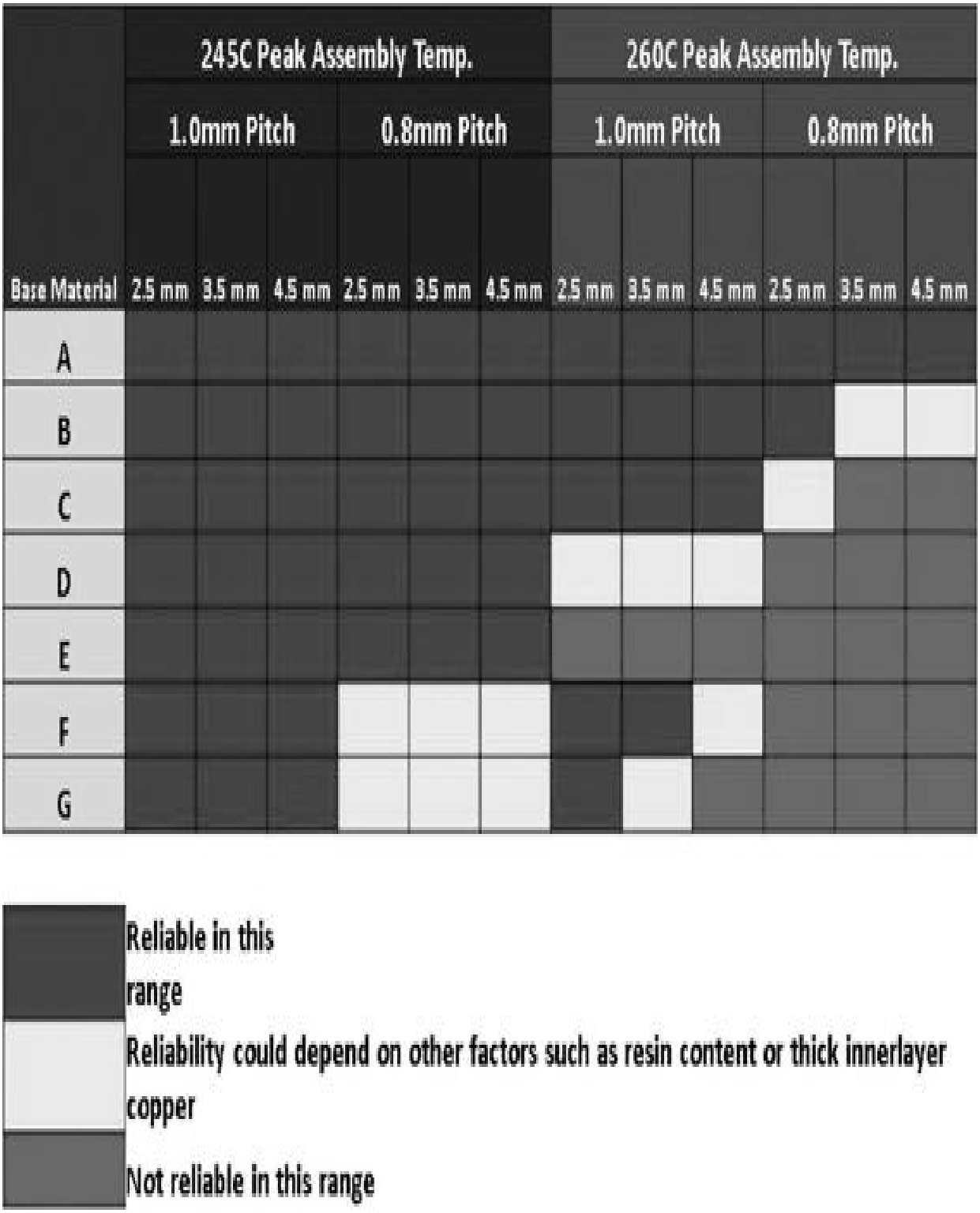


FIGURE 14.7 Example of material thermal reliability rating.

14.3.2 IPC Specification Sheets

IPC specifications and specification sheets for different material types were introduced in Chap. 10. This included IPC-4101, Specification for Base Materials for Rigid and Multilayer Printed Boards, and IPC-4103, Specification for Base Materials for High-Speed/High-Frequency Applications. IPC-4101 in particular contains a number of specification sheets for different types of base materials. Many of the more recently added specification sheets were developed with the demands of lead-free assembly in mind, and include properties such as decomposition temperature, thermal expansion, T260 and T288 values.

However, there are some important limitations to these specification sheets that should be well understood. First, the specifications refer to the laminate materials, and not to the PCBs made with the material. For example, a specification sheet with a requirement for the T_g to be a minimum of 170°C refers to the laminate, and not to a multilayer PCB made with that same material. There are a few reasons why the measured T_g on a PCB could be different than the laminate material. Second, just because a material meets the requirements of a specific specification sheet, even one that has requirements for decomposition temperature, thermal expansion and time to delamination, doesn't mean that the material will be reliable in a given lead-free application. Conversely, just because a material does not meet all the requirements stated in a given specification sheet, does not mean the material is unsuited for a given application. The material performance should be validated through testing such as that described above.

It is also critical to understand that no one property will guarantee success in lead-free applications. All of the variables outlined in this chapter must also be considered when specifying a material. When faced with uncertainty, the

natural tendency is to overspecify each property. Not only could this cause the user to pay too much for a material, but overspecifying specific properties can also lead to functional problems. These problems can be the result of the interaction between advanced materials and the PCB fabrication processes required to manufacture reliable PCBs.

Take decomposition temperature, T_d, as an example. Although the 5 percent level of decomposition is the standard reported value, this is a very high level of decomposition from the standpoint of PCB reliability. It is important to understand when decomposition begins and how close this temperature is to actual assembly and rework process temperatures. A material with a reported T_d, based on the 5 percent level, of 325°C may perform just as reliably, or even more reliably, than a material with a 5 percent T_d value of 340°C, depending on what the decomposition characteristics are in the lead-free assembly and rework temperature ranges. Specifying materials with significantly higher T_d values may not improve reliability, and may potentially add cost and difficulty to the manufacturing process if the higher T_d material is more difficult to process—for example, if the lamination times are longer, or if it is harder to drill. Although future specification sheets may include T_d values based on lower levels of decomposition, it is very important to understand these properties in some detail and specify the appropriate material for a given application.

Last, a potentially valuable use of the specification sheets is to use them as a baseline. A given specification sheet that meets most of the requirements desired by the user can be selected. The user can then call out exceptions to the values on the sheet, or add or delete other requirements. One example could be peel strength when very low profile copper foils are used to improve signal integrity. Existing peel strength values may be too high for some materials with

extremely low profile copper foils. In this case, if thermal reliability of the material with the desired copper foil has been validated by the user, then they can reference a certain specification sheet and make an exception to the peel strength requirement.

14.3.3 Summary

The question of whether a given laminate material is compatible with lead-free assembly can be very complex due to the many variables in PCB design and manufacturing. In addition, there are variations in lead-free assembly processes. Specifically, peak temperatures, dwell times at peak temperatures, heatup rates, cooldown rates, and rework processes can all vary and complicate this decision. As stated earlier, the temperature range from 240 to 260°C is critical for laminate materials; some materials may be successful at the low end of this range but fail at the higher end.

Critical base material properties with respect to lead-free assembly applications include

- *The decomposition temperature*. Some minimum value is needed, but above that minimum level, higher values are not always better.
- *Thermal expansion properties*. Improved materials have reduced levels of thermal expansion.
- *Glass transition temperature*. A higher glass transition temperature delays the onset of rapid thermal expansion and therefore reduces total expansion within a temperature range.
- *Moisture absorption*. In particular, if PWBs are stored in an uncontrolled or humid environment prior to assembly, drying of boards prior to assembly or selection of a

material less prone to moisture-related problems should be considered.

- *Time to delamination*. T260 and T288 values are a simple way to screen materials for compatibility with lead-free assembly. However, testing at higher temperatures or requiring excessive times may not be necessary.

Balancing these properties with the level of reliability required along with PWB manufacturability and assembly concerns is vital.

14.4 SELECTING MATERIALS FOR ELECTRICAL PERFORMANCE

As with thermal reliability, there are many factors that affect the performance of a PCB in terms of electrical performance. The components that make up the base material as well as the processes used to make the PCB can all affect performance. Many of these factors were discussed in previous chapters. So in the following sections we will summarize some of the key considerations related to the base material components and PCB processes, and then discuss how base materials are categorized and measured. For an overview of skew issues in differential signaling, refer to Sec. 12.11 in Chap. 12

14.4.1 The Influence of Base Material Components on Electrical Performance

Each of the three basic components that comprise a laminate material has an impact on the electrical

performance of the composite structure. The key factors were discussed in Chap. 10, and summarized here:

- *Resin system*. Clearly the resin system, which includes any inorganic or organic fillers, has an enormous impact on the electrical performance. The Dk and Df of the resin system are the primary factors to consider when selecting a resin system. Recall that for most common materials the resin content selected in in the laminate and prepregs will result in different values of Dk and Df. Usually as resin content increases the Dk will decrease and Df will increase. An exception to this was discussed in Sec. 12.11 in Chap. 12 when discussing skew in differential pairs of signals. In this section a material that had very uniform Dk properties regardless of resin content was described. In general, lower Dk/Df resin systems will incur added costs.
- Glass cloth. Historically E-glass has been by far the most common type of fiberglass cloth used in PCBs. In recent years the use of lower Dk glass fabrics has been growing significantly. In addition, the use of spread/expanded glass cloths has also been increasing. While these fabrics have other benefits, some of the increased usage is due to the improved uniformity of Dk across the dielectric. This was also discussed in Sec. 12.11 of Chap. 12. There is some cost premium associated with spread/expanded glass fabrics, and the low Dk glass cloths are also more expensive than standard E-glass.
- *Copper foil*. The primary consideration with copper foil is surface roughness, as discussed in Chap. 12. As operating frequencies increase, the impact of copper surface roughness becomes increasingly important, and can be a dominant factor at very high frequencies. Copper foil manufacturers continue to develop extremely low profile copper foils that still have suitable bond strength to advanced resin systems. These foils are also sold at a premium to more standard foils. Table 14.4 provides

simulation data for loss in dB/in using a 20-mil long, 4-mil stripline with ½ ounce copper and four different types of copper foil with decreasing levels of surface roughness from “standard” profile to “EVLP,” which has an extremely low surface roughness. In addition, the table provides simulation data for three material types at three different frequencies. From this table you can get an idea of the impact of copper foil roughness and operating frequency on the performance of three types of resin system. As conductor width will also affect loss, Table 14.5 presents data for a 6-mil stripline so that a comparison can be made with the 4-mil stripline.

TABLE 14.4 Single-Ended 4 mil ½ oz Stripline—20 Inches Long

	dB/Inch @ 4 gigahertz			dB/Inch @ 8 gigahertz			dB/Inch @ 12 gigahertz		
Foil	A	B	C	A	B	C	A	B	C
Standard	0.588	0.533	0.484	0.913	0.811	0.712	1.223	1.069	0.908
RTF	0.532	0.477	0.426	0.839	0.732	0.630	1.126	0.972	0.807
VLP	0.491	0.436	0.384	0.781	0.675	0.570	1.055	0.901	0.734
EVLP	0.459	0.404	0.351	0.737	0.631	0.524	1.001	0.846	0.678

TABLE 14.5 Single-Ended 6 mil ½ oz Stripline—20 Inches Long

	dB/Inch @ 4 gigahertz			dB/Inch @ 8 gigahertz			dB/Inch @ 12 gigahertz		
Foil	A	B	C	A	B	C	A	B	C
Standard	0.479	0.424	0.359	0.765	0.658	0.536	1.035	0.880	0.691
RTF	0.437	0.382	0.318	0.707	0.601	0.477	0.964	0.809	0.603
VLP	0.407	0.352	0.288	0.665	0.559	0.435	0.912	0.757	0.568
EVLP	0.384	0.329	0.265	0.632	0.526	0.403	0.872	0.718	0.528

In addition to the individual components, the laminate manufacturing process can also have some impact. In short, control of resin contents, dielectric thickness uniformity and degree of cure of the resin system can all influence the electrical performance of the finished laminate.

14.4.2 PCB Manufacturing Influences on the Base Material

There are a few key processes within the overall PCB manufacturing process that can influence the material performance. These include

- *Innerlayer circuit etching*. Control of line widths and geometries will influence impedance control and attenuation. Wider circuit traces will result in less loss, but the width is typically specified by the circuit designer.
- *Innerlayer surface preparation*. The oxide or oxide alternative processes can have a significant impact on loss as a result of any increase in surface roughness they create. Figure 14.8 showed an example of differences that can be observed through these processes.

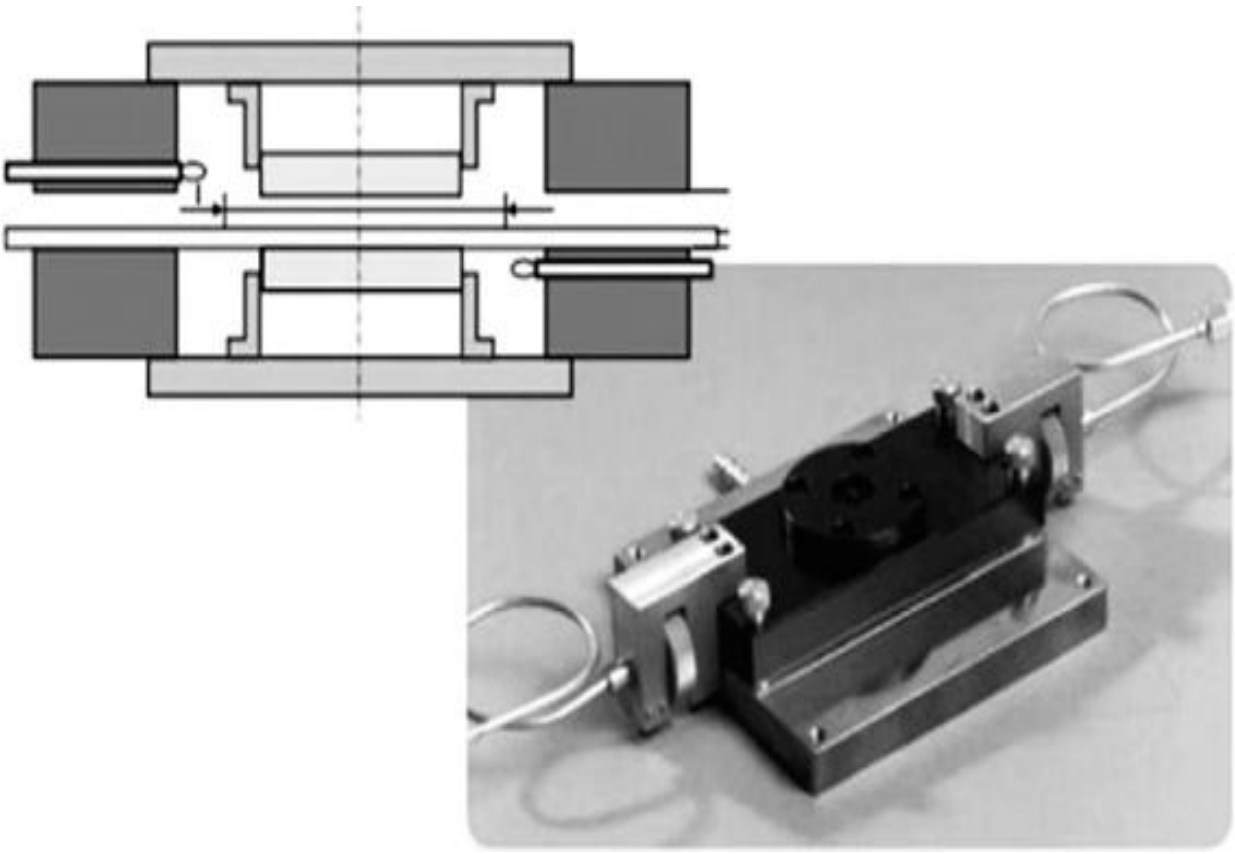


FIGURE 14.8 Example of resonator used in SPDR method.

- *Multilayer lamination*. Achieving good cure of the resin in the prepregs is important as it can affect the dielectric Dk and Df properties. Moisture can interfere with the curing of some high performance resin systems, and therefore it can be important to fully dry the innerlayer laminates prior to lay-up of the multilayer. Proper storage of the prepregs prior to use is also important.

14.4.3 Classification of Base Materials for Electrical Performance

Historically the most common way to classify materials was simply by reporting Dk and Df values. However, both Dk and Df vary with resin content, frequency, and test method. This also made it very difficult to compare materials based on

supplier data sheets, as different suppliers use different test methods or resin contents. Furthermore, measurements on the base laminate materials, with some methods using unclad laminates and therefore not taking into account the impact of copper, often did not correlate well to actual performance in the PCB. So in more recent years, test methods that characterize material performance in the finished system have been developed. Some of these will be described shortly.

While many OEMs have their own system of classification for electrical performance, it is common to specify ranges of dissipation factor, Df, or loss. A common classification is shown in Table 14.6.

TABLE 14.6 Examples of Classification of Materials by Df

OEM	Test Method	Df Categories				
A	Uses impedance optimization coupons and TDR/TDT hardware	Standard Loss 0.020–0.023	Mid Loss 0.014–0.020	Low Loss 0.008–0.015	Very Low Loss 0.004–0.008	Ultra Low Loss <0.004
B	S-parameter measurements	High Loss >0.020	Standard Loss 0.014–0.020	Mid Loss 0.010–0.015	Low Loss 0.005–0.010	Ultra Low Loss <0.005

Table 14.4 highlights that different OEMs may have different preferred test methods, as well as different terminology and categories for loss levels. Most of the preferred methods used by OEMs require multilayer PCB structures and use insertion loss measurements to extract effective Dk and Df values. Some are also able to de-embed the effect of copper surface roughness. In others, PCB structures with different types of copper foils and/or oxide processes can be compared to understand these influences.

Unsurprisingly, as material Df decreases there is typically an increase in cost. In terms of industry usage and using the categories defined by OEM “B” in Table 14.4, high loss materials represent the highest volumes in PCB manufacturing, however for some OEMs their use of materials in this category has peaked. Standard loss materials as defined by OEM B have grown in usage in recent years. While volumes of mid-loss and low-loss materials are relatively smaller, they are experiencing faster growth rates. Ultra-low loss materials are the focus of much current development work, and are expected to grow in coming years. These ultra-low loss materials are expected to use very low loss resin systems along with ultra-low profile foils and low-Dk/Df glass cloths.

As noted above, there are many test methods used to assess base material electrical performance. While a full discussion is beyond the scope of this chapter, there are some increasingly common methods used by OEMs and fabricators to assess material performance at high frequencies, and a recent technical paper published by the High Density Packaging User Group (HDPUG) discussed and compared several of these methods.[3] One example given in this study was to select one material and measure Df by multiple test methods. The range of Df values measured by four different methods was 0.002 to 0.008, highlighting the need to understand what test method is used to assess a material.

IPC test method 2.5.5.12 describes five methods for determining the amount of signal propagation loss caused by material characteristics of conductors in PCBs, and is a good reference for those looking for more technical details, along with the HDPUG technical paper already cited. Table 14.7 is an overview found in the IPC test method. There are other methods also briefly described below.

TABLE 14.7 Overview of Test Methods from IPC-TM-650 2.5.5.12

	EBW	RIE	SPP	SET2DIL	FD
Instrument	TDR	TDR/VNA	TDT	TDR/TDT	VNA/TDT
Stimulus	Selected for appropriate spectral content	250 ps or specified	11-35 ps	11-35 ps	300 KHz to 10 GHz or as specified
Coupon	>5 cm	1.25 cm and 20.32 cm or as specified	3.0 cm and 10.0 cm	4" (8" effective length)	20.32 cm or as specified
SW	Scope Algorithm	Algorithm and IPC website pointer	Algorithm and IPC website for software	Algorithm	Algorithm
Probe	Matched impedance probe	Matched impedance probe	Matched impedance probe, RF connector	High Frequency hand-held probe	Matched impedance probe, RF connector
Test Quantity	Maximum slope in MV/sec	Averaged loss (dB)	Tan δ ε_r, α, β, and Z_o vs. frequency	SDD21 vs. frequency	Loss fit and slope
Applicability	Printed board fabrication testing	Printed board fabrication testing	Printed board material qualification, printed board model generation	Printed board fabrication qualification and testing	Printed board fabrication testing, printed board design guide specification

A few of the more common test methods used widely today include

- *Split post dielectric resonator (SPDR)*. Historically a very commonly used method. This method utilizes unclad

dielectrics and therefore does not include the influence of the conductor. Many laminate material data sheets report values based on this method as well as the parallel plate method (IPC 2.5.5.9). However, the values reported by these methods often do not reflect the effective Dk and Df on actual PCBs. Figure 14.8 is an example of the resonator.

- *Stripline resonators*. Stripline resonators use either a metal clad substrate or a conductor placed in very close contact to the dielectrics under test. IPC 2.5.5.5 is an example, though there are other methods as well, such as the Bereskin stripline method. Figure 14.9 shows examples of the equipment set up used.

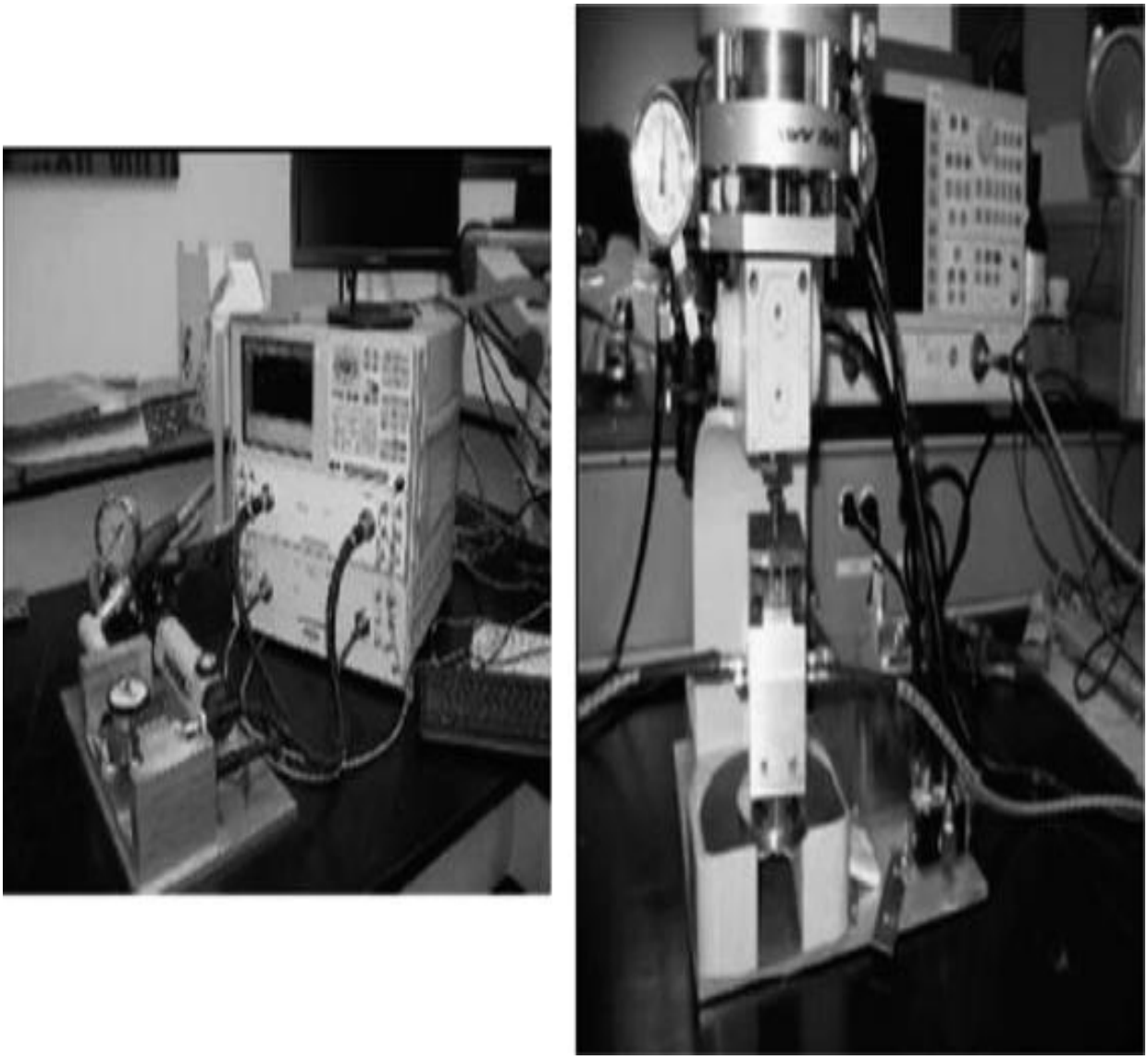


FIGURE 14.9 Fixture used in IPC and Bereskin methods.

- *Short pulse propagation (SPP)*. Described in IPC 2.5.5.12, uses time domain reflectometry/time domain transmission (TDR/TDT) equipment and characterizes insertion loss and effective Dk/Df. Typically multilayer test vehicles using both a high resin and low resin stack-up are assessed in order to assess Dk/Df variation with resin content. Figure 14.10 illustrates SPP testing.

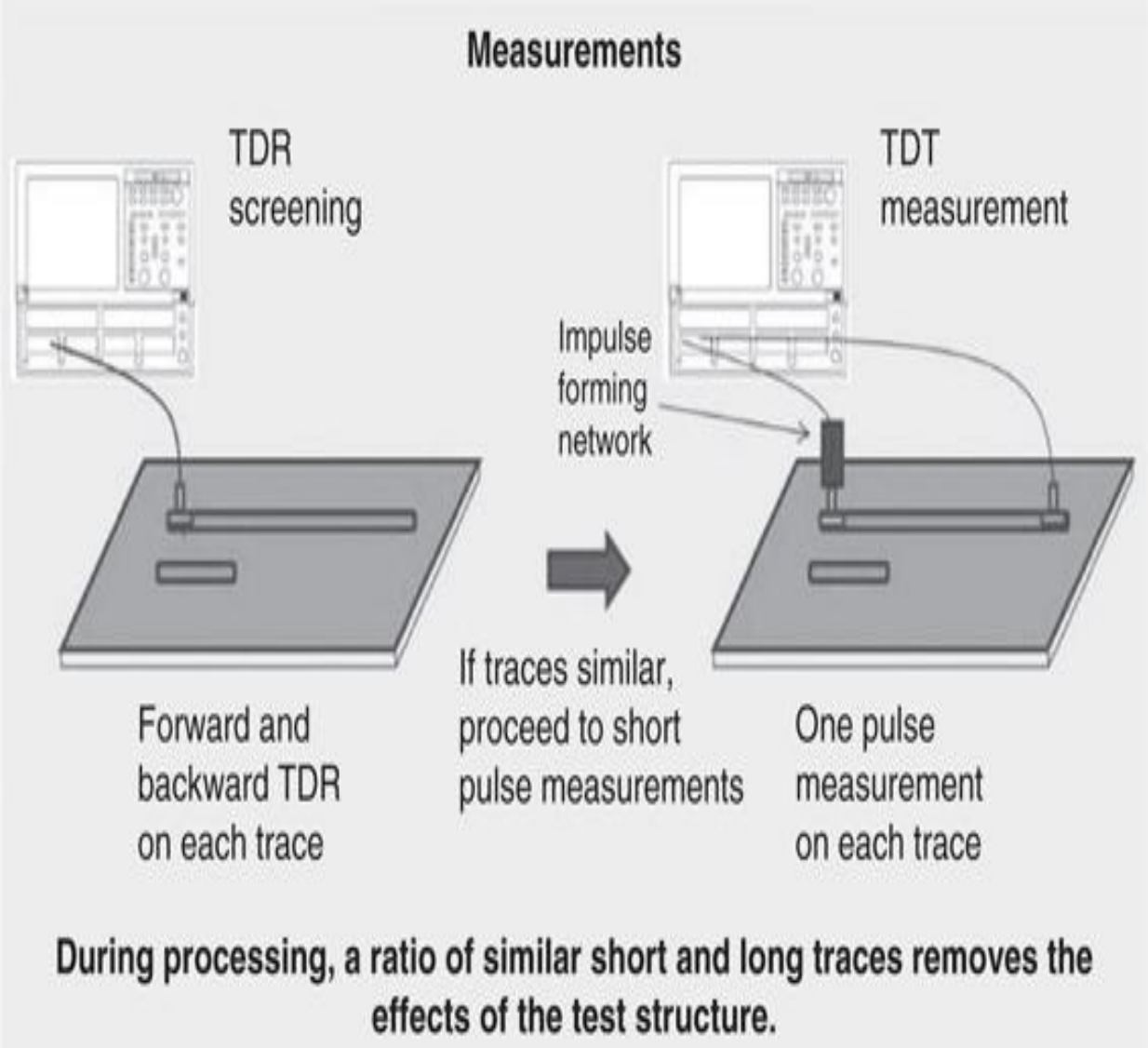


FIGURE 14.10 Illustration of SPP methods. (*From Introbotics Corp.*)

- *Single ended time domain to differential insertion loss (SET2DIL)*. Also described in IPC 2.5.5.12, SET2DIL is a relatively inexpensive and easy way to measure PCB insertion loss in volume manufacturing environments. SET2DIL also uses TDR/TDT hardware and is used to measure both stripline and microstrip interconnects (Fig. 14.11). Commonly used to report insertion loss at 4 and 8 GHz.

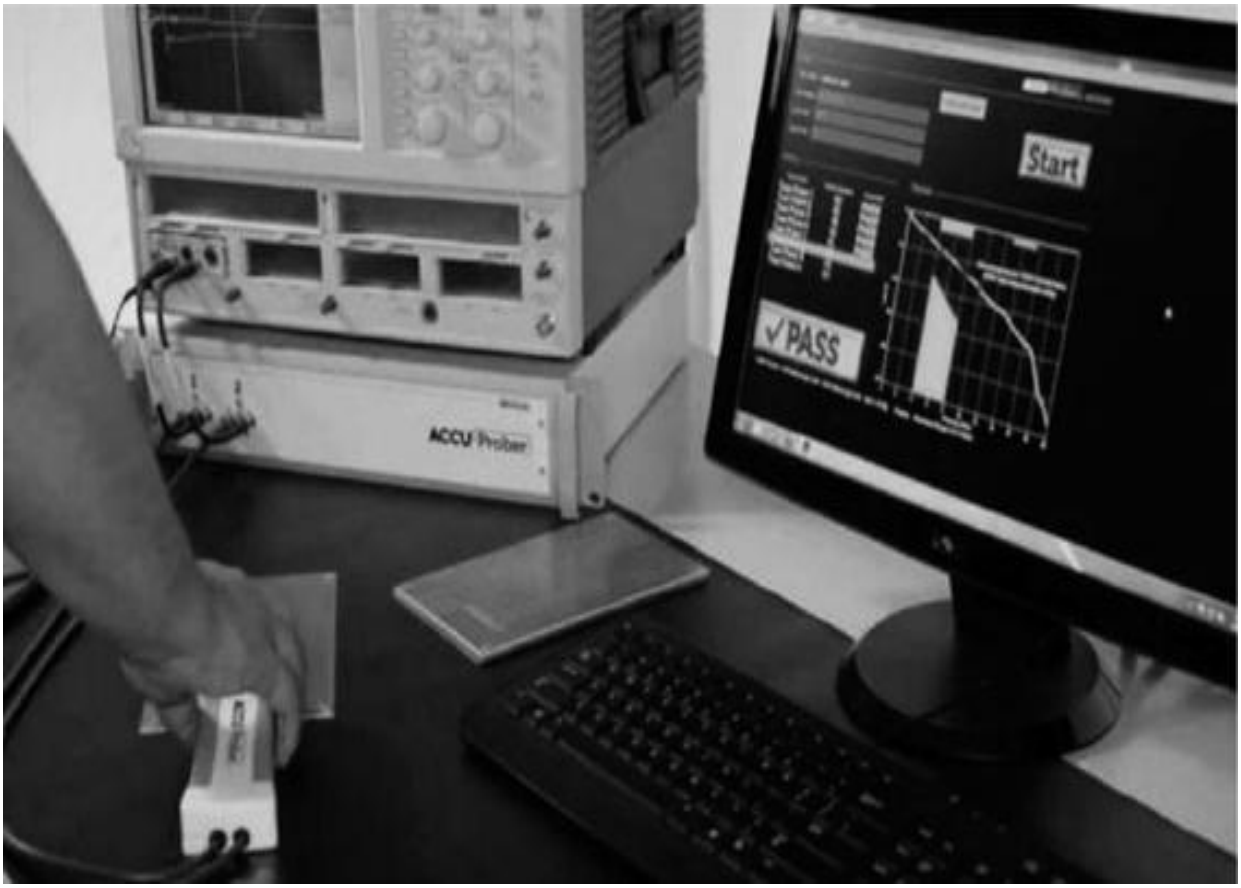


FIGURE 14.11 Example of SET2DIL measurement. (*From Introbotics Corp*.)

14.4.4 Summary

As with thermal reliability, OEMs and fabricators are using various test vehicles and methods to assess base material electrical performance and to classify materials into various performance categories. In fact, many users will first assess the electrical performance of a material in order to understand what level of performance it offers, and will then proceed to test thermal reliability and possibly CAF performance as we will discuss shortly. The end result might be a list of materials as in Fig. 14.7 for each level of electrical performance, as in Table 14.6. Such a material database would allow for easy selection of materials for new applications.

14.5 CAF RESISTANCE

Many aspects of CAF were discussed in Sec. 12.8 of Chap. 12. In addition, there is a chapter dedicated to CAF later in the book. So we refer the user to these sections of the handbook for more information, and here will outline some general conclusions that are useful when selecting materials. Also, an additional example of a CAF test vehicle will be described along with examples of CAF test results. As this discussion will make clear, performing failure analyses when failing insulation resistance measurements are observed is critical in understanding performance. There are reasons why a failed insulation resistance may have nothing to do with the base material performance.

14.5.1 General Considerations When Selecting Materials

From the years of research on CAF, there are several general conclusions that can assist the user when selecting materials. These include

- All base materials have some level of CAF resistance, but even materials promoted as “CAF-resistant” can vary widely in actual performance.
- The test vehicle design has a significant impact on results. The closer the circuit features, the more likely that CAF failures will occur. In addition, the other attributes of the test vehicle design can impact the fabrication variables that influence CAF—for example, the thickness of the PCB and drilled hole sizes can lead to high aspect ratios that can be more challenging to manufacture. As a result of these factors, there is not universal agreement on what

constitutes a “CAF-resistant” material. This can vary by OEM and application.

- One type of resin system can vary in performance based on other factors, such as the glass cloth quality and the controls used during laminate and prepreg manufacturing.
- The specific glass styles can also impact performance. Although 7628 glass was the focus of much attention in CAF testing historically, 106 and 1080 styles can be challenging as well, in that getting full resin-to-glass wetting can be challenging with these styles. The spread/expanded styles such as 1067 and 1086 are easier in completely wet-out with resin for improved performance. In short, getting complete wet-out of the resin to the glass filaments is critical.
- It is critical to define appropriately the performance level required and to design a test vehicle and test protocol that reflects the requirements of the application. Failure to do so can result in either underspecifying the material attributes and risking PCB failures or overspecifying the material and paying too much for it.
- For resistance to CAF growth, the resin system and the bonding of the resin system to the fiberglass cloth are key considerations. Coupling agents, typically silanes, are used to promote adhesion between the fiberglass filaments and the resin system. The molecular structure of the coupling agent includes a portion that bonds well to the fiberglass surface and other portions that bond well to the resin system. Specific coupling agents have been developed for specific resin types. Achieving a good bond between the fiberglass filaments and the resin system with an appropriate coupling agent helps prevent this interface from becoming a path for CAF growth.
- Low rates of moisture absorption and low levels of ionic contamination within the resin system also aid in resisting CAF growth. Epichlorohydrin is a precursor material used

to make epoxy resins. The use of this compound can result in residual hydrolyzable chlorides in the epoxy resin. In the presence of moisture, these hydrolyzable chlorides form ionic species that can promote electromigration. When CAF resistance is a critical consideration, the use of high-purity resins may be required.

- Lead-free assembly can stress the resin-to-glass bond, and even cause some level of resin decomposition, which can create microvoids within a PCB and cause failures in materials that are not robust enough for the lead-free assembly process used.
- On the other hand, many lead free compatible materials will actually improve in CAF performance after exposure to lead-free assembly. It is recommended that lead-free preconditioning on CAF coupons be performed prior to testing. Many OEMs will want to test in both the “as received” condition as well as after multiple reflow simulations to understand any change in performance.

14.5.2 Example of CAF Test Vehicle, Test Results and Findings in Failure Analyses

Figure 14.12 is an external photo of a multilayer CAF coupon that has been used to assess many different materials. This coupon is being used in a larger test vehicle that contains many other types of coupons that test, among other things, thermal reliability. From the surface you can see that there are two orientations for the rows of holes, and perhaps not as obvious, two hole-to-hole distances. While the other discussions of CAF noted that there are different types of CAF formation, including hole wall to hole wall, hole to plane or hole to trace, trace to trace, and layer to layer, generally the most challenging feature is hole-to-hole. The coupons in

Fig. 14.12 have two orientations so that both dimensions of the glass fabric are tested. In some cases, the warp (or grain) direction has filament bundles that are more densely packed and therefore can be more difficult to completely wet-out with resin. This is one reason to test both dimensions.

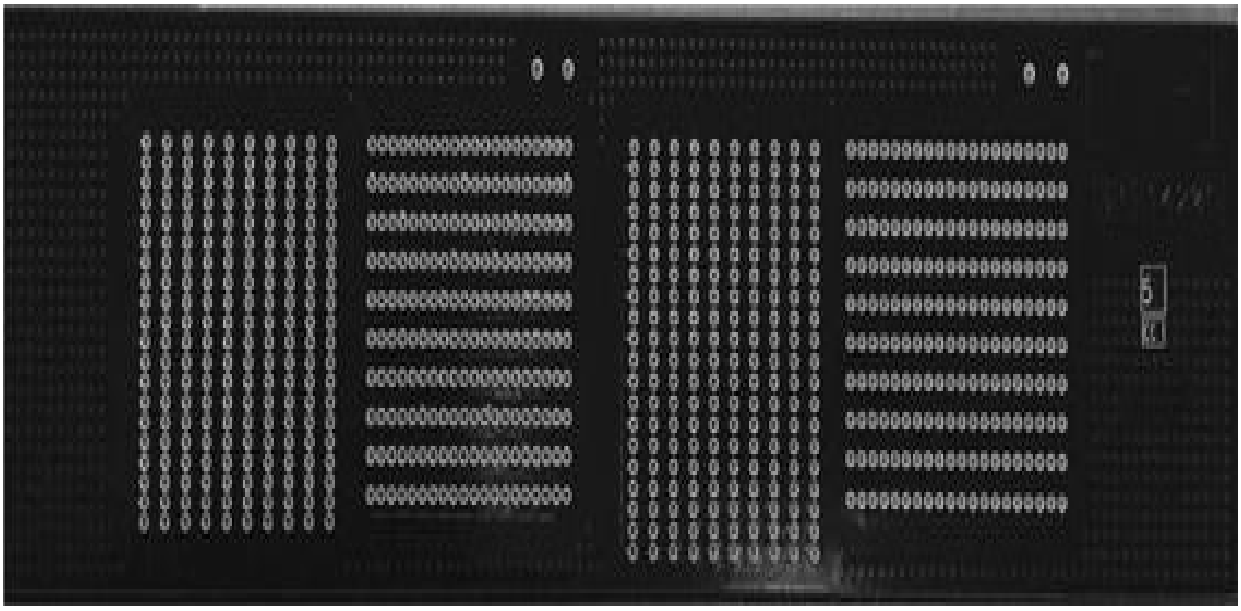


FIGURE 14.12 Example of a common CAF coupon. (*Courtesy of Alcatel-Lucent*.)

Another test vehicle design which is used to test the various types of CAF referenced above is shown in Fig. 14.13. Figure 14.14 shows the design of the hole wall-to-hole wall coupons in this test vehicle. Note the wall-to-wall distances, the number of opportunities for failure, and the two different drilled hole sizes, which allows an assessment of the impact of drilled hole quality. These coupons are generally tested in both the as manufactured condition as well as after multiple lead-free reflow cycles.

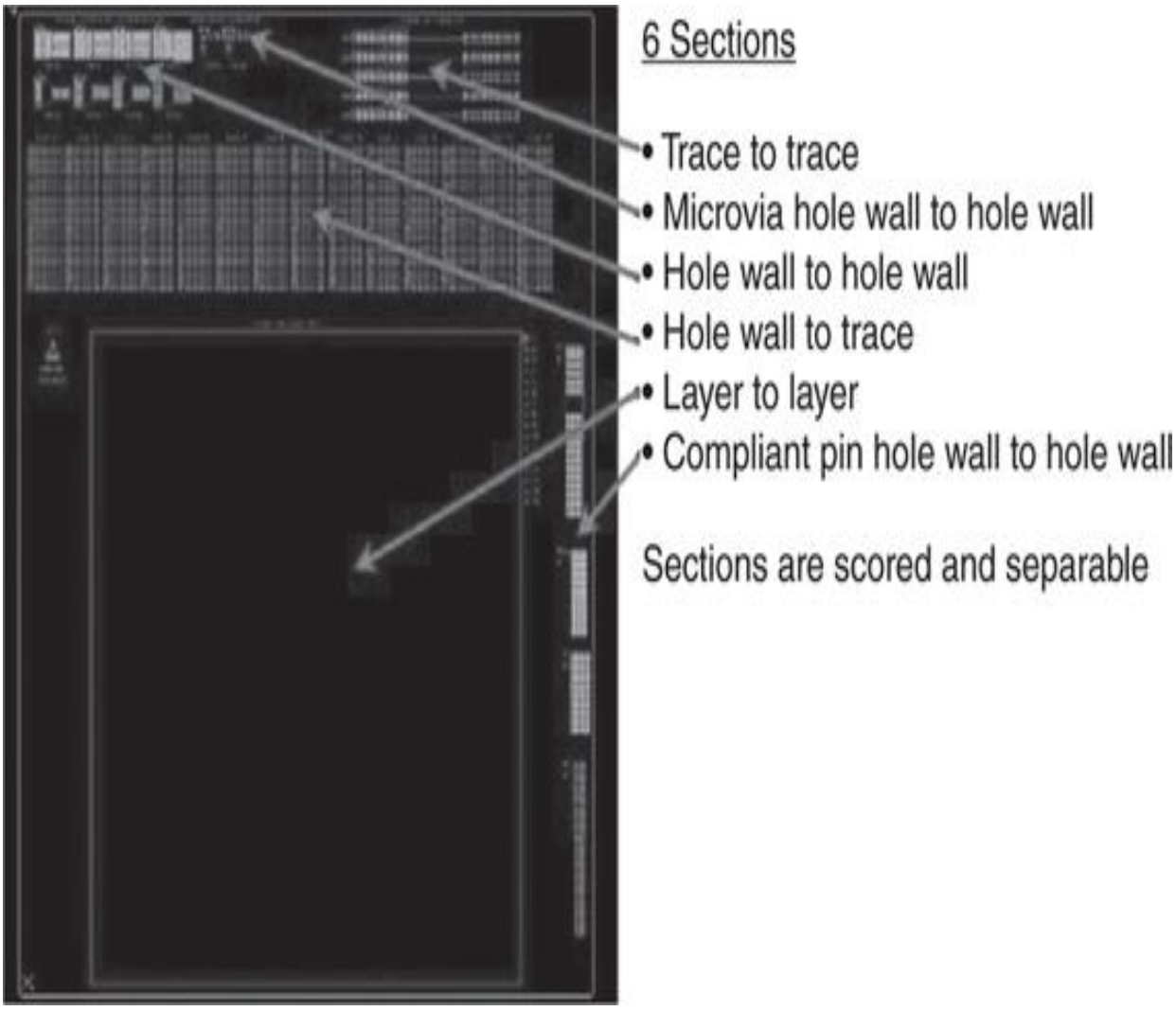


FIGURE 14.13 Example of A CAF coupon with multiple design features. (*Courtesy of Alcatel-Lucent*.)

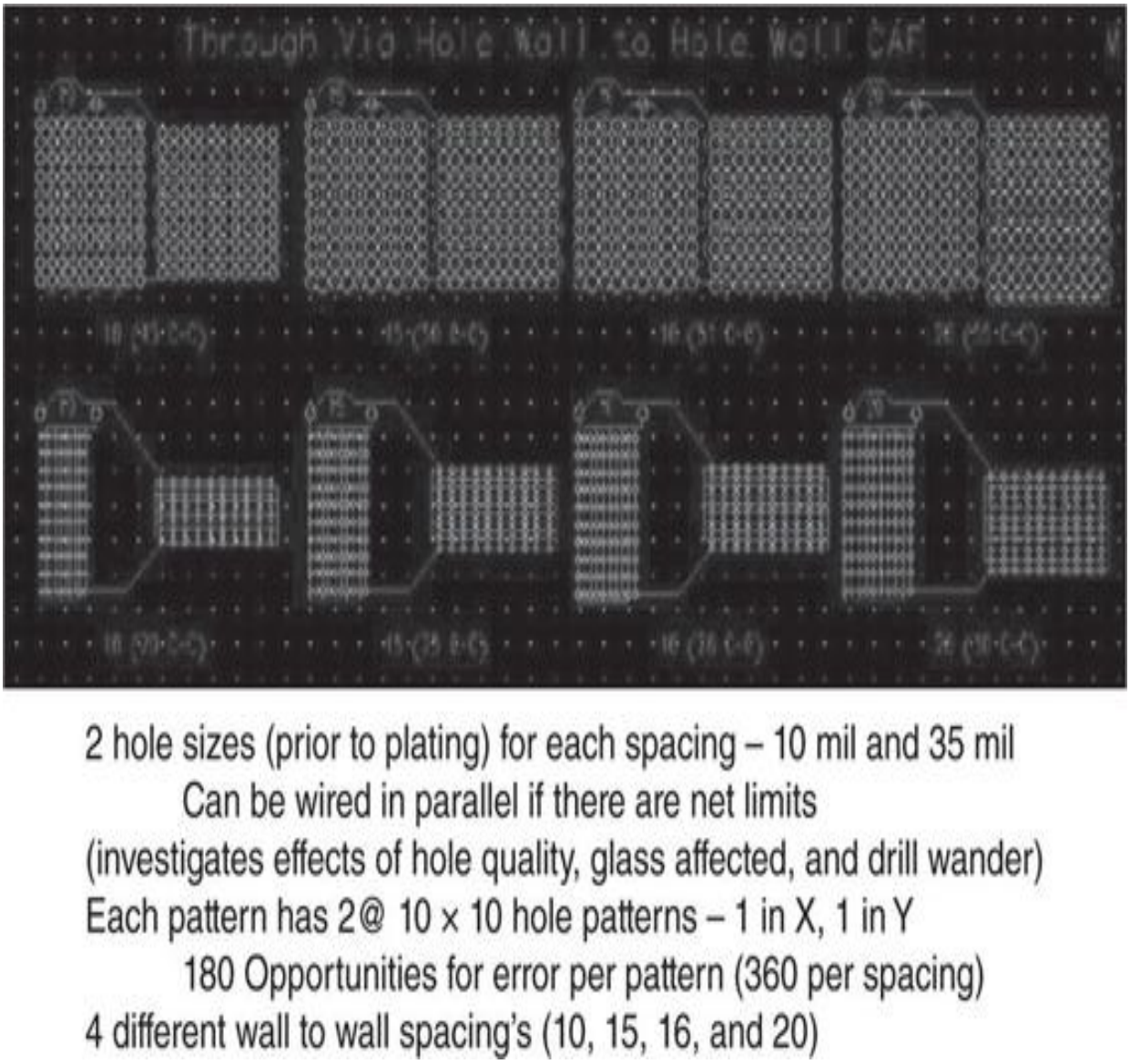


FIGURE 14.14 Example of CAF coupon design with multiple hole wall to hole wall spacings. (*Courtesy of Alcatel-Lucent*.)

Figure 14.15 graphs the insulation resistance for eight coupons with 10-mil drilled holes at a 16-mil hole wall-to-hole wall distance after 3× lead free reflow cycles. The coupons are conditioned at the test temperature and humidity for 96 hours prior to the application of steady state bias. This explains the apparent dip in resistance at time “0” in the chart. It is normal to have a high initial resistance reading and then a drop in resistance after temperature and

humidity conditioning and the application of the test voltage. Test conditions normally used for this test vehicle are 65°C, 85 percent relative humidity and 100 V. The minimum duration required is 500 hours, but it is preferred to go to 1000 hours. Failure is typically defined as an order of magnitude drop in resistance from time 0, or a drop in the absolute resistance below 10^8 Ω. The results in Fig. 14.15 are very good. Insulation resistance is very stable throughout the 1000 hours.

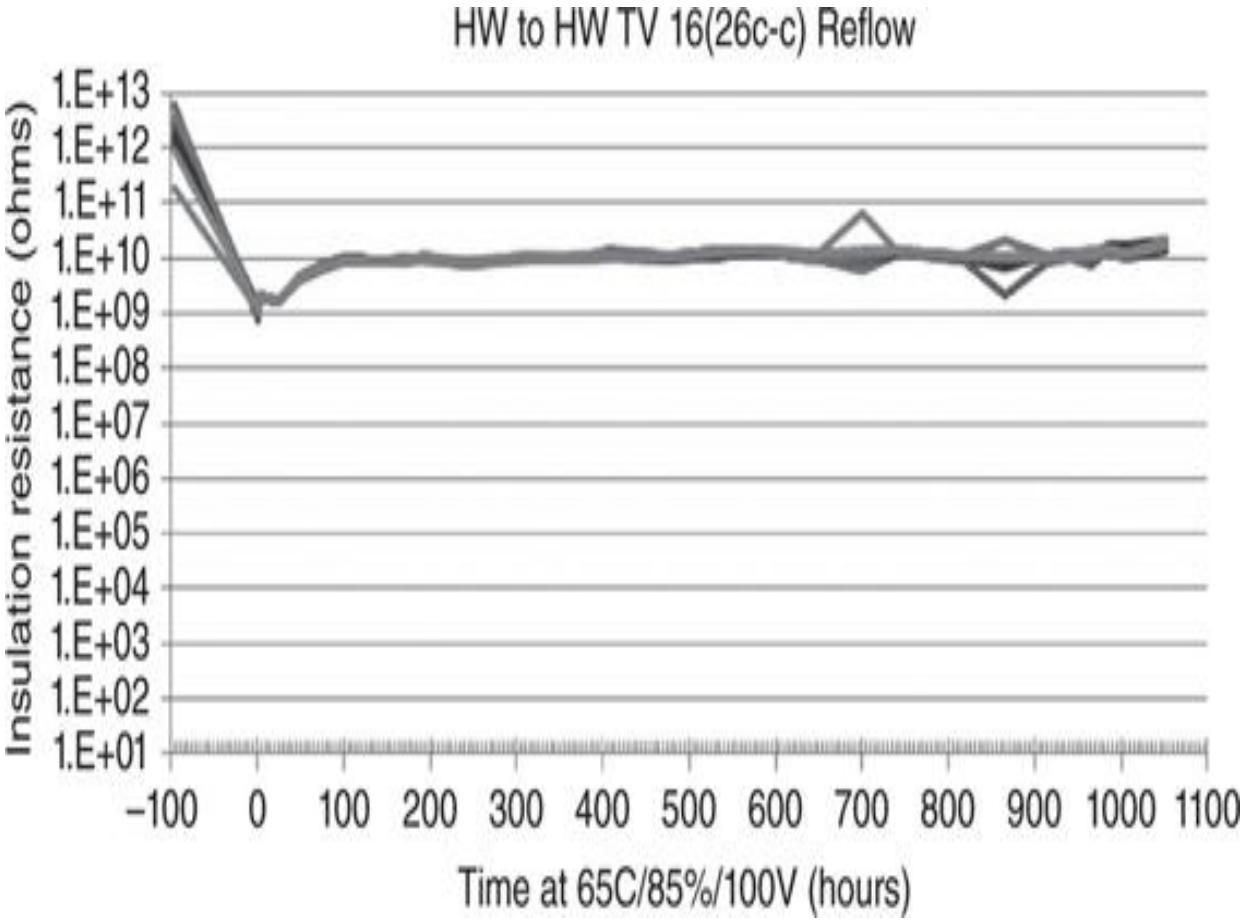


FIGURE 14.15 Example of CAF test results after lead free reflow 10-mil drilled hole size at a 16-mil wall-to-wall distance. (*Tested at i3 Labs*.)

Figure 14.16 shows test results for the exact same resin system and test conditions, but with a different glass cloth supplier and silane finish used in the laminate and prepreg

materials. In this case the result are extremely poor, with some coupons failing almost immediately. Figure 14.17 is an example of failure analysis results for failed coupons in this test.

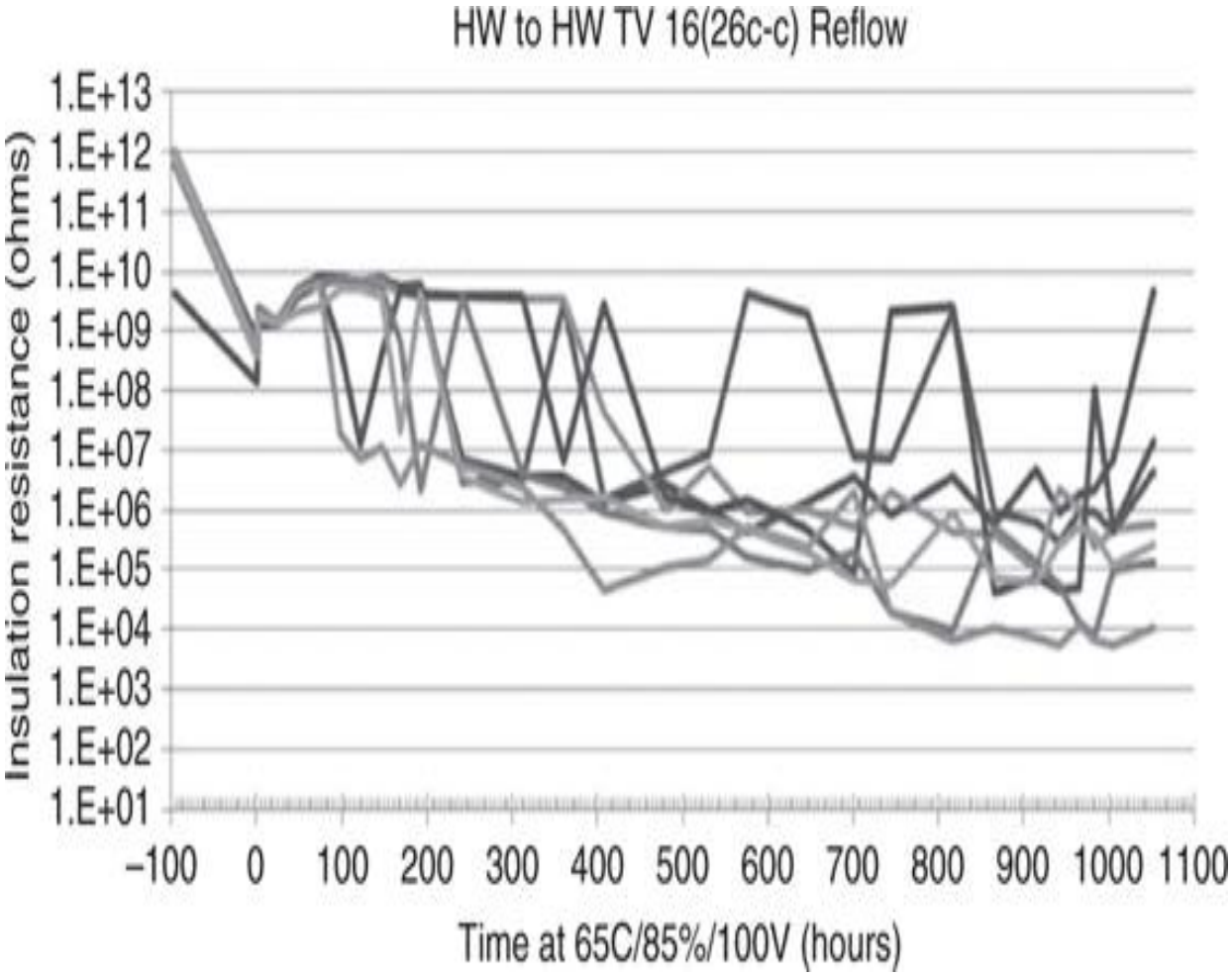


FIGURE 14.16 Example of CAF test results after lead free reflow 10-mil drilled hole size at a 16-mil wall-to-wall distance with alternate glass supplier and silane finish. (*Tested at i3 Labs*.)

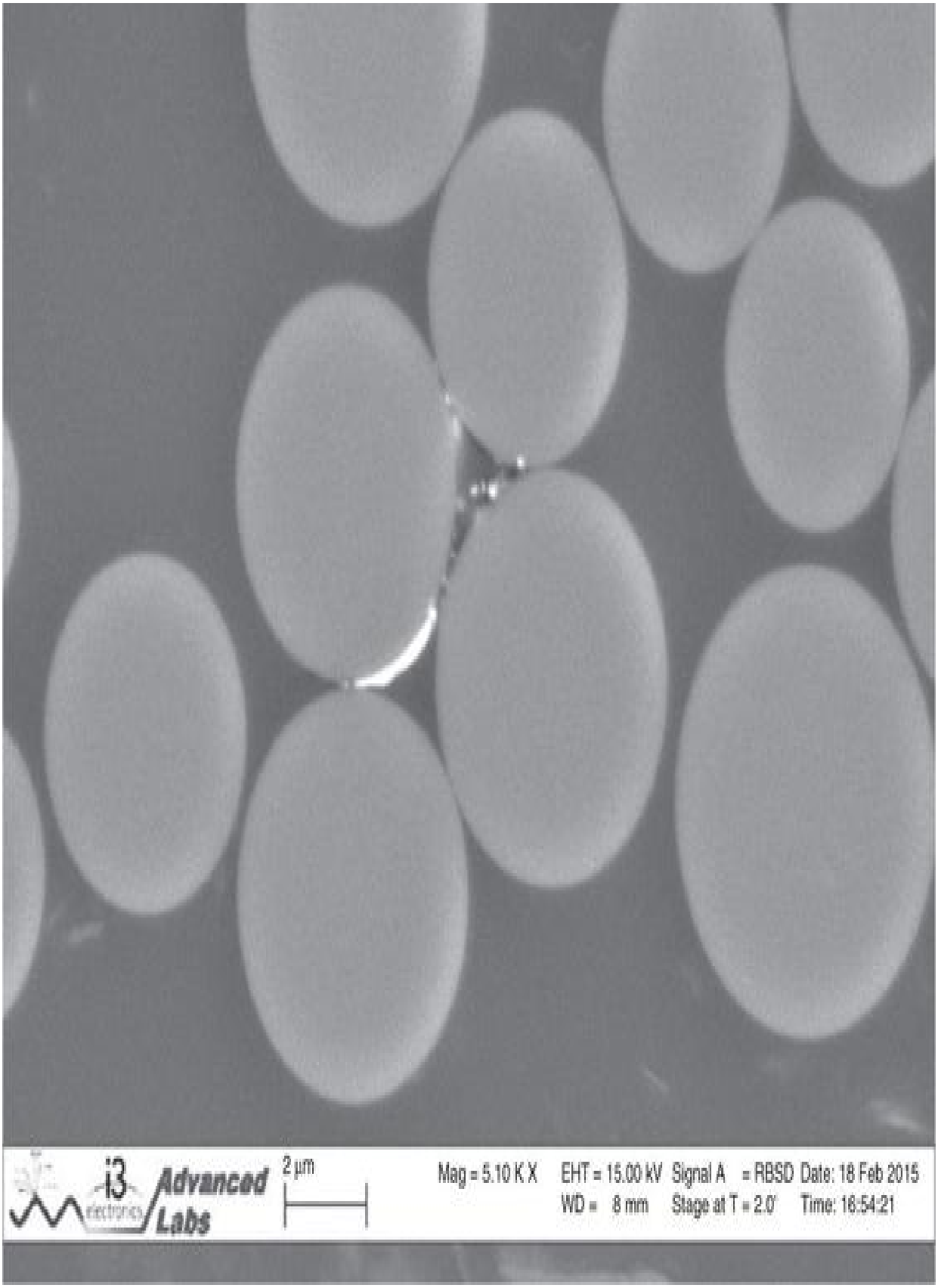

i3 electronics
Advanced Labs
2 µm
Mag = 5.10 K X
EHT = 15.00 kV
WD = 8 mm
Signal A = RBSD
Stage at T = 2.0°
Date: 18 Feb 2015
Time: 16:54:21

FIGURE 14.17 Failure analysis for a coupon from Fig. 14.16. (*Analysis by i3 Labs*.)

The failure analysis in in this case showed copper migration along the resin-to-glass interface. EDX results exhibited not just copper metal, but other elements indicating that the conductive filament contained a copper salt, which is indicative of a true CAF failure. In this case, the glass cloth and silane source could not be qualified for use.

Figures 14.18 and 14.19 show CAF test results for another test sample. In this case, while there were failures in the insulation resistance testing, the failure analysis showed that the failure was not due to CAF, but to silver surface finish residues on the surface of the coupon. Figure 14.20 shows an insulation resistance failure due to embedded contamination. The contamination was a fiber that, through FTIR analysis and matching, was determined to be a rayon fiber. In Fig. 14.21 is a failure analysis where a hollow glass filament provided a pathway for copper migration to occur.

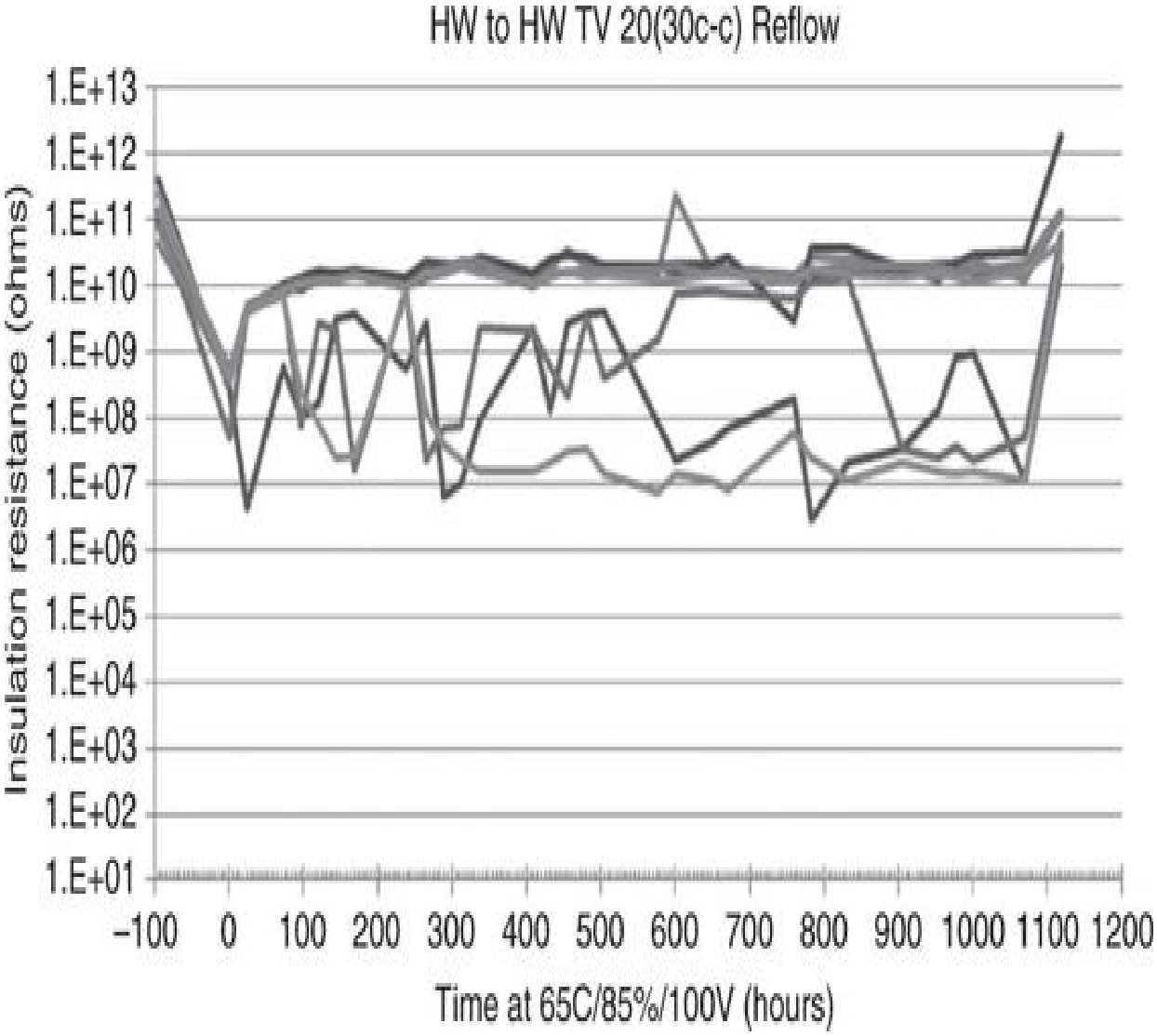


FIGURE 14.18 Example of CAF test results after lead-free reflow, 10-mil drilled hole size at a 20-mil wall-to-wall distance, sample C. (*Tested at i3 Labs*.)

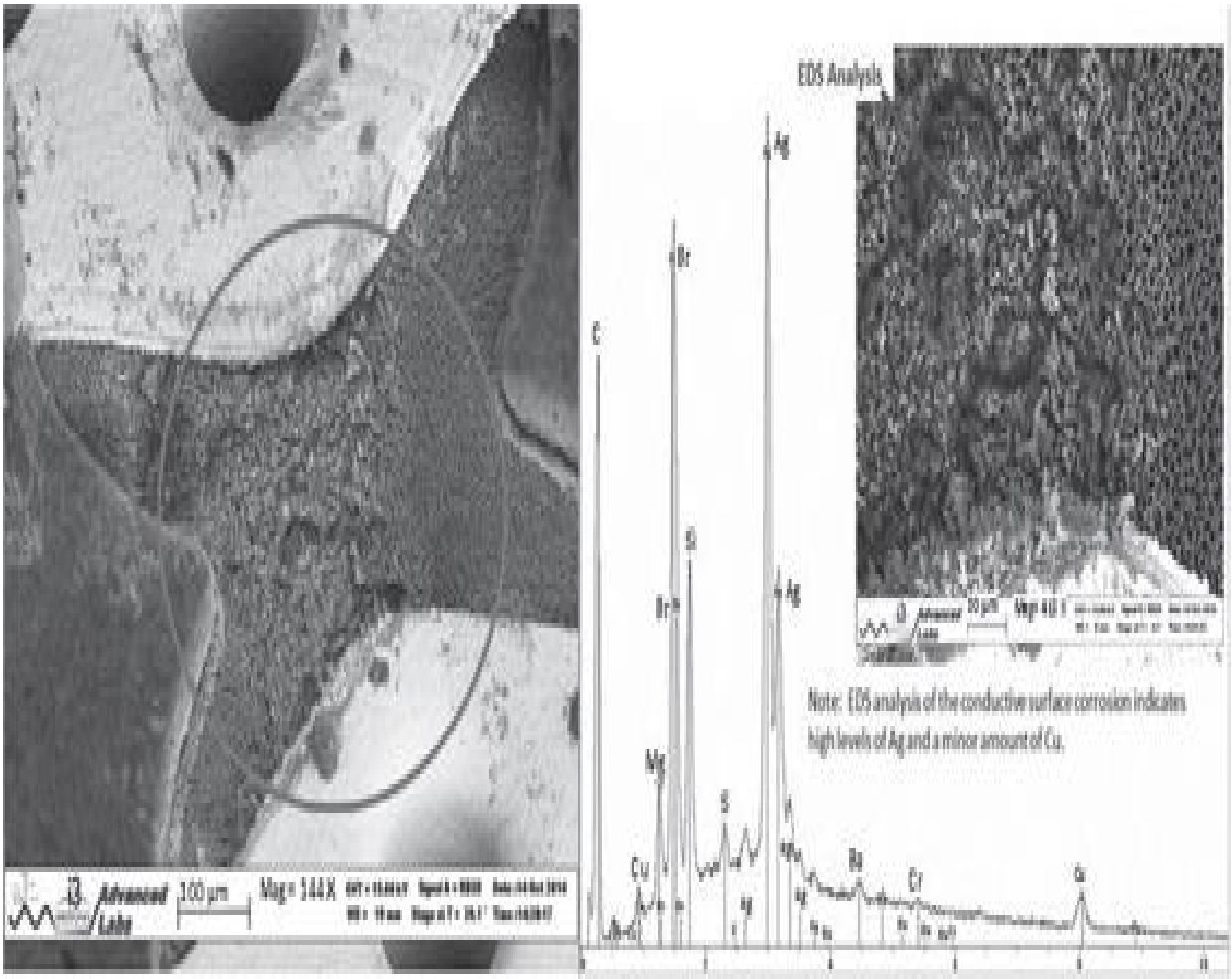


FIGURE 14.19 Failure analyses for coupon from Fig. 14.18. (*Analysis by i3 Labs*.)

FIGURE 14.20 Insulation resistance failure due to embedded contamination. (*Analysis by i3 Labs*.)

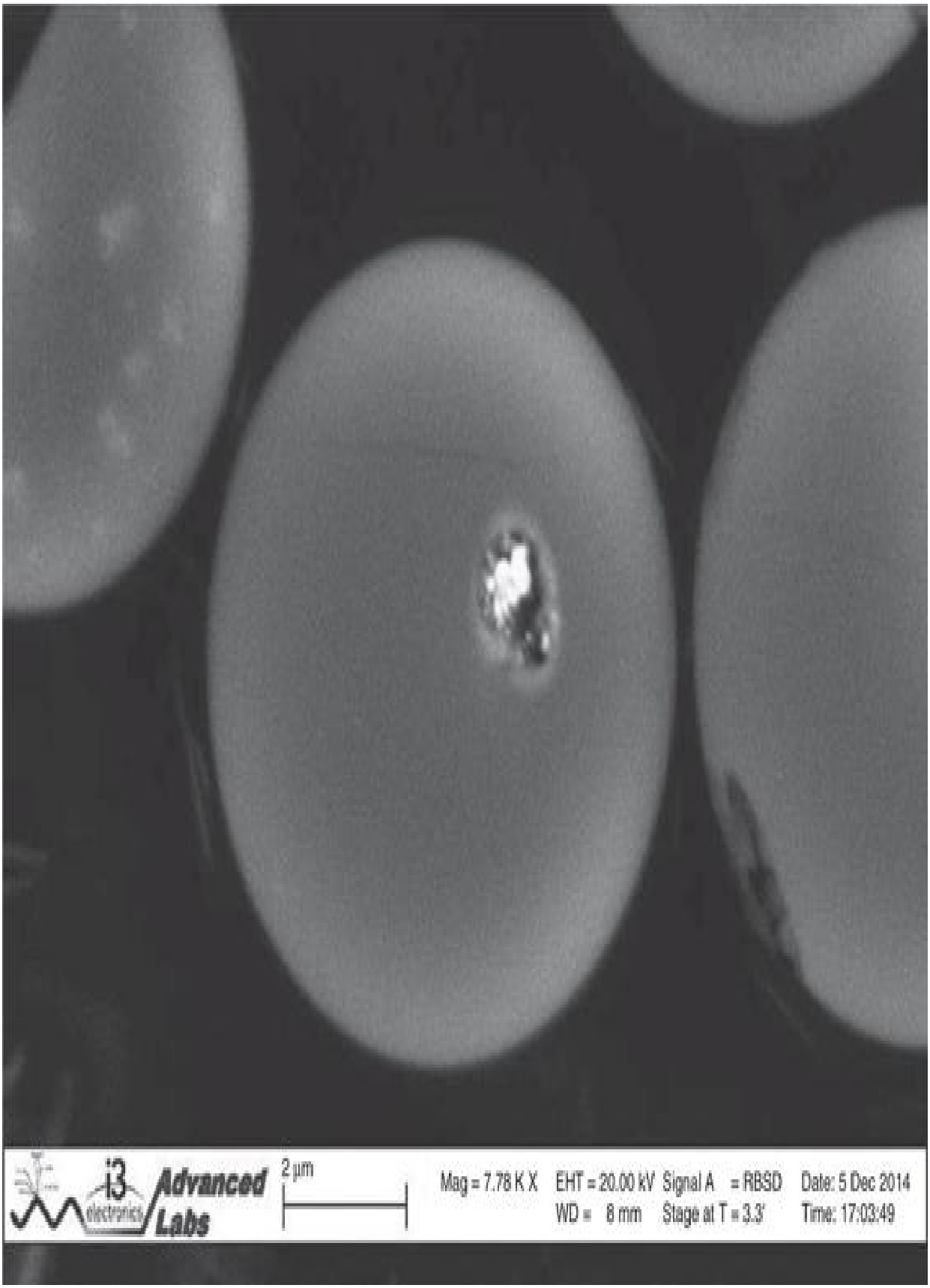

i3 electronics
Advanced Labs
2 µm
Mag = 7.78 K X
EHT = 20.00 kV
WD = 8 mm
Signal A = RBSD
Stage at T = 3.3'
Date: 5 Dec 2014
Time: 17:03:49

FIGURE 14.21 Insulation resistance failure due to hollow glass filament. (*Analysis by i3 Labs*.

14.5.3 Final Comments on CAF

- The examples above are intended to highlight the importance of performing failure analysis subsequent to any insulation resistance failures in order to determine if the failure is truly the result of CAF or some other cause.
- The test vehicle described in this section can also utilize different stack-ups in order to test specific glass styles and resin contents.
- It is important to match the CAF test vehicle design and test protocol to the design features of the PCB in question. Using a test vehicle that is much more stringent than the actual PCB design risks ruling out acceptable, lower cost materials. On the other hand, not testing down to the minimum feature distances of the PCB risks selection of materials that may not offer adequate CAF resistance.

14.6 REFERENCES

1. Birch, Bill, “Quantifying and Benchmarking New PWB Materials Reliability, Electrical Performance and Thermal Properties Following Exposure to Today’s Lead Free Assembly Environment,” HDPUG presentation at EIPC-Berlin, June, 2015.
2. Smetana, Joe, Birch, Bill, and Rothschild, Wayne, “A Standard Multilayer Printed Wiring Board for Material Reliability Evaluations,” Alcatel-Lucent Material Reliability Test Board Used in High Density Packaging User Group Studies.
3. Sauter, Karl, and Smetana, Joe, “High Frequency Dk and Df Test Methods Comparison, High Density Packaging User Group (HDP) Project,” February, 2015.

CHAPTER 15

LAMINATE QUALIFICATION AND TESTING

Michael Roesch
Hewlett-Packard Company, Palo Alto, California

Sylvia Ehrler
Feinmetall GmbH, Herrenberg, Germany

15.1 INTRODUCTION

Copper-clad laminate materials (single- or double-sided) are the base material for almost all printed circuit boards (PCBs). The properties of these materials have a large influence on the quality of the final product and therefore need to be understood and tested prior to release/manufacturing.

15.1.1 Impact of RoHS and Lead-Free Requirements

With a change toward RoHS-compliant “lead-free” assembly processes, laminate materials and complete printed circuit boards are facing a set of increased challenges:

- *Laminates* Materials have to survive the increased thermal stress of repeated lead-free assembly cycles. Due to the higher melting temperature of lead-free solders, a peak temperature during reflow of 260°C must realistically be expected (30°C to 40°C higher than eutectic soldering profiles). Most printed circuit boards will be required to withstand at least five such assembly cycles, but that number may increase to six and higher for more complex assemblies. A rule of thumb states that a 10°C increase of temperature doubles the reaction energy starting degradation or decomposition of the resin compound. The increased peak temperature therefore requires new or improved laminate materials with a higher decomposition temperature and enhanced thermal stability. New laminate test methodologies are also needed to assess the impact of the higher assembly temperatures.
- *PCB reliability* There should not be any degradation in the reliability of the printed circuit boards after assembly compared to boards assembled using traditional soldering profiles. When the same laminate material is used, plated through holes will see an increase in thermal expansion stresses after an equal number of assembly cycles with higher peak temperatures. This means that if the same laminate is used, the reliability margin of the PCB has decreased. To achieve comparable reliability of boards after both eutectic or lead-free soldering, a change in the base material is most likely. Additional PCB reliability concerns include innerlayer bonding, conductive anodic filament (CAF) growth, and dielectric strength, particularly with reduced dielectric thicknesses.
- *PCB performance* In addition to the preceding reliability challenges posed by lead-free assembly processes, it also

has to be guaranteed that all other performance characteristics of the printed circuit board stay the same. This includes dielectrical properties such as dielectric constant D_c (which influences impedance), dissipation factor D_f, and thermomechanical properties such as copper peel strength, glass transition temperature, or coefficient of thermal expansion (CTE). These properties should not be affected by the assembly processes applying higher temperatures.

15.1.2 Material Evaluation Process

In almost all cases, the laminate manufacturer will provide a set of data for its specific materials. This datasheet is a good starting point and can certainly be used to evaluate laminates at an early state of a project. Often, though, it will be necessary to perform additional tests in the PCB facility to verify or complement the manufacturer’s data to ensure that the laminate materials meet the requirements of manufacturing and assembly processes.

This chapter introduces the most important laminate properties and their characterization methods and has been revised to reflect RoHS-compliant manufacturing process and temperature requirements. It will serve as a quick reference guide for the printed circuit board specialist as well as an introduction to laminate testing for those who are new to the field. Laminate properties according to industry standards such as the National Electrical Manufacturers Association (NEMA) and IPC will be introduced. Then the actual test methods will be discussed in the form of a best-practice guide. This guide will help the PCB specialist make quick decisions during the testing process. Methods to test mechanical, thermomechanical, and electrical properties of printed circuit board materials will be described. The focus will be on how the tests are performed, what the results

actually mean in today's manufacturing environment, and how relevant the obtained test data are. In addition to the raw base material testing, the chapter will introduce a best-practice qualification guide to assess interactions between manufacturing processes and laminate properties.

15.2 INDUSTRY STANDARDS

A number of different industry standards can be used to evaluate copper-clad laminate properties. Many of the test methods for similar properties are very comparable, though, and in the end the materials engineer must decide which standard to use as a basis for his or her characterization. In some cases, it may even be necessary to define a new characterization method to qualify a laminate material for a specific customer application or a particular requirement.

15.2.1 IPC-TM-650

This document is the most comprehensive and most widely used compilation of copper-clad laminate test methods. It is administered by IPC (Association Connecting Electronic Industries) and available in print or online.[a]

Most of the test methods described in this chapter are based on the test manual IPC-TM-650. It contains industry-approved test techniques and procedures for chemical, mechanical, electrical, and environmental tests on all forms of printed wiring and connectors. An IPC test method is a procedure by which the properties or constituents of a material, an assembly of materials, or a product can be examined. These test procedures do not contain acceptability levels for specific properties.

15.2.2 IPC Specification Sheets

IPC publishes a wide variety of technical specification sheets for PCB and printed circuits assembly (PCA) products. A few are important in this context:

- *IPC 4101, "Specifications for Base Materials for Rigid and Multilayer Printed Boards," Rev. B 06/06* This document contains specification sheets for laminate materials used to manufacture PCBs for commercial and military applications. The minimum requirements for key material properties can be found in these specification sheets.
- *IPC 4103, "Specification for Plastic Substrates, Clad or Unclad, for High Speed/High Frequency Interconnections," 01/02* This document contains specification sheets for Teflon (polytetrafluoroethylene, or PTFE) and other laminate materials used to manufacture PCBs for high-speed or high-frequency applications.
- *IPC 4104, "Specification for High-Density Interconnect (HDI) and Microvia Materials," 05/99* This document contains specification sheets for materials used in HDI and microvia applications.

15.2.3 ASTM

The American Society for Testing and Materials (ASTM) develops standard test methods and specifications that are in some cases related to laminate materials. They will be referenced as appropriate. More information can be found online.[b]

15.2.4 NEMA

NEMA publishes standards on laminated thermosetting materials. The last published version is the LI 1-1998 Standard for Industrial Laminated Thermosetting Products, which includes the latest information concerning the manufacture, testing, and performance of laminated thermosetting products. Most copper-clad laminate materials are named according to NEMA grades, but it is important to understand that NEMA grades represent only material categories and not one individual material. One of the most commonly known material grades is FR-4, which is often thought of as a specific laminate material. This is not the case, however, as each NEMA grade represents a material class defined by properties that fall into a certain class. Thus, properties of different laminate materials from different suppliers that fall into the same class (FR-4, for example) may not be identical. More information can be found online.[c] (For a more detailed discussion of FR-4, see Sec. 6.4.)

15.2.5 NEMA Grades

Table 15.1 shows technical and industrial laminate grades as they apply to the most important printed circuit board materials.

TABLE 15.1 NEMA Grade Material Designations and Properties

NEMA grade	Resin system	Reinforcement	Description
XXXPC	Phenolic	Paper	Phenolic paper, punchable
FR-2	Phenolic	Paper	Phenolic paper, punchable, flame-resistant
FR-3	Epoxy	Paper	Epoxy paper, cold punchable, high insulation resistance, flame-resistant
CEM-1	Epoxy	Paper-glass	Epoxy paper core and glass on laminate surface, flame-resistant
CEM-2	Epoxy	Paper-glass	Epoxy paper core and glass on laminate surface
CEM-3	Epoxy	Glass matte	Epoxy non-woven glass core and woven-glass surface, flame-resistant
CEM-4	Epoxy	Glass matte	Epoxy non-woven glass core and woven-glass surface
FR-6	Polyester	Glass matte	Polyester non-woven glass, flame-resistant
G-10	Epoxy	Glass (woven)	Epoxy woven glass, not flame-resistant
FR-4	Epoxy	Glass (woven)	Epoxy woven glass, flame-resistant
G-11	Epoxy	Glass (woven)	High-temp epoxy, woven glass, not flame-resistant
FR-5	Epoxy	Glass (woven)	High-temp epoxy, woven glass, flame-resistant

15.3 LAMINATE TEST STRATEGY

Laminates contain different reinforcement materials (woven/non-woven glass/organic fibers, expanded PTFE, etc.), resin types (phenolic, epoxy, cyanate ester, polyimide, BT, etc.), resin formulations (blended, functionality, etc.),

hardeners (dicyanodiamide [dicy], phenol-novolak, cresol-novolak, p-aminophenol, isocyanurate, etc.), and sometimes filler particles (ceramic or organic). The ratio of all of these individual components can vary widely. To define a test strategy for laminates, it is important to understand the different main components of the materials as well as the conditions during manufacturing, as these will have a large influence on their properties and quality.

The evaluation and qualification of a laminate material can be a quite complex task and the new requirements for lead-free processing have specifically increased the focus on the thermal characteristics of laminate materials. A number of different qualification test methods are available to the materials engineer. However, very often not all of them are relevant or necessary for the final product. At the same time, the materials engineer faces pressure to produce quick results driven by shorter development cycles and increasing product and process requirements. The organization of the test methods described in this chapter follows a proposed best-practice guide aimed to help perform full material evaluations efficiently and at the same time address the new requirements of lead-free processing. The sections allow quick decisions, especially when a number of materials are being evaluated at the same time.

15.3.1 Data Comparison

The first step in every material evaluation is data comparison and assessment. This step may already allow the elimination of some material candidates without performing actual tests.

The first and most important thing to understand is the state of the material that is being considered. Is it an established material formulation that has a solid history at other manufacturing locations, or is it a newly developed

material that has not seen mass production yet? New developments often do not come with complete data sheets that allow an early assessment, whereas the laminator can often provide one for established materials.

Cost is another important factor. The laminator can provide guidance about volume pricing for the new material.

Other considerations are the history of the supplier, in terms of having met previous commitments and whether the material is already in high-volume production. If it is a new material that has not yet been ramped to high volume, if no more than one PWB manufacturer is using it, and if no second source can be identified, then these facts may be a red flag when considering the material for use.

15.3.2 Two-Tier Test Strategy

The qualification procedure proposed in this chapter follows a two-tier test strategy that enables quick decisions during a material qualification program. The first set of tests is easy to perform and focuses on key properties that should be evaluated when testing a new laminate material. Failure to pass any of them will likely result in rejection of a material for manufacturing. If multiple materials are being evaluated, the first tests will allow the easy elimination of the least probable candidates.

The second set of tests is an expanded set of qualification tests that focuses on all key properties that are commonly evaluated for laminates. However, the final decision about a qualification test plan for a new laminate should always be driven by product-level requirements, which means that additional laminate tests as well as board-level tests may need to be added to the set of tests described in the following section.

15.4 INITIAL TESTS

This first set of tests is most commonly performed when starting a material evaluation and qualification project. The tests can be performed easily and give some early indications of whether the material exhibits any major problems.

15.4.1 Surface and Appearance

This test is one of the very first tests to happen as the new material arrives in the shop. The laminate is inspected for its appearance and visual quality. Often the materials engineer will be able to assess the quality of the product without applying specification guidelines. Even packaging and shipping materials should be used to assess the laminator's overall quality control.

IPC-TM-650 method 2.1.2 and method 2.1.5 define procedures for how to inspect the surface and appearance of copper-clad laminates. These standards should be applied only to surface areas that are pertinent to the finished board. More than 90 percent of the copper will usually be removed during manufacturing, and a new material should not be discarded solely for cosmetic reasons. On the other hand, for areas that will contain edge card connector pads or very fine-line traces, these surface standards must be applied.

The specifications categorize the longest permissible dimensions of any copper pits and dents and define a point value-based rating system (as shown in Table 15.2).

TABLE 15.2 Longest Permissible Dimensions

Longest dimension (mm)	Point value
0.13–0.25	1
0.26–0.50	2
0.51–0.75	4
0.76–1.00	7
Over 1.00	30

The total point value for an area of 300 mm × 300 mm of laminate determines the material class (as shown in Table 15.3).

TABLE 12.3 Material Class

Class	A	B	C	D	X
Total point count	<30	<5	<17	0	Requirements agreed upon
		All dents <0.38 mm			

In addition to copper pits and dents, the specifications contain procedures on how to inspect for scratches, wrinkles, and inclusions.

15.4.2 Copper Peel Strength

The copper peel strength of copper-clad laminates is an indicator for a variety of their performance characteristics. It indicates the bond strength of the copper circuitry of a double-sided printed circuit construction after manufacturing and any successive assembly or repair cycles. To assess the copper bond strength of the outerlayer circuitry of a multilayer construction accurately, it is necessary to take a close look at the exact build-up and copper foil used in the construction and to build specific test vehicles that are similar to the original stack-up. Copper peel strength measurements have grown increasingly important as circuit traces and pads are becoming smaller. In addition, this test allows an assessment of any potential weaknesses in multilayer constructions and identifies the interface that might delaminate first after thermal stress. The higher the initial bond strength of a material, the better. For all characterizations after thermal stress in the temperature range of lead-free assembly, it is also important to look at the decrease of bond strength. This is especially important for applications that require multiple reflow operations and one or more repair cycles.

The test method is specified in IPC-TM-650, method 2.4.8, and the applicable test patterns are specified in IPC TM-650, method 5.8.3. Figure 15.1 shows an actual test pattern using a sample 100 mm × 100 mm coupon with 4-mm-wide copper strips.

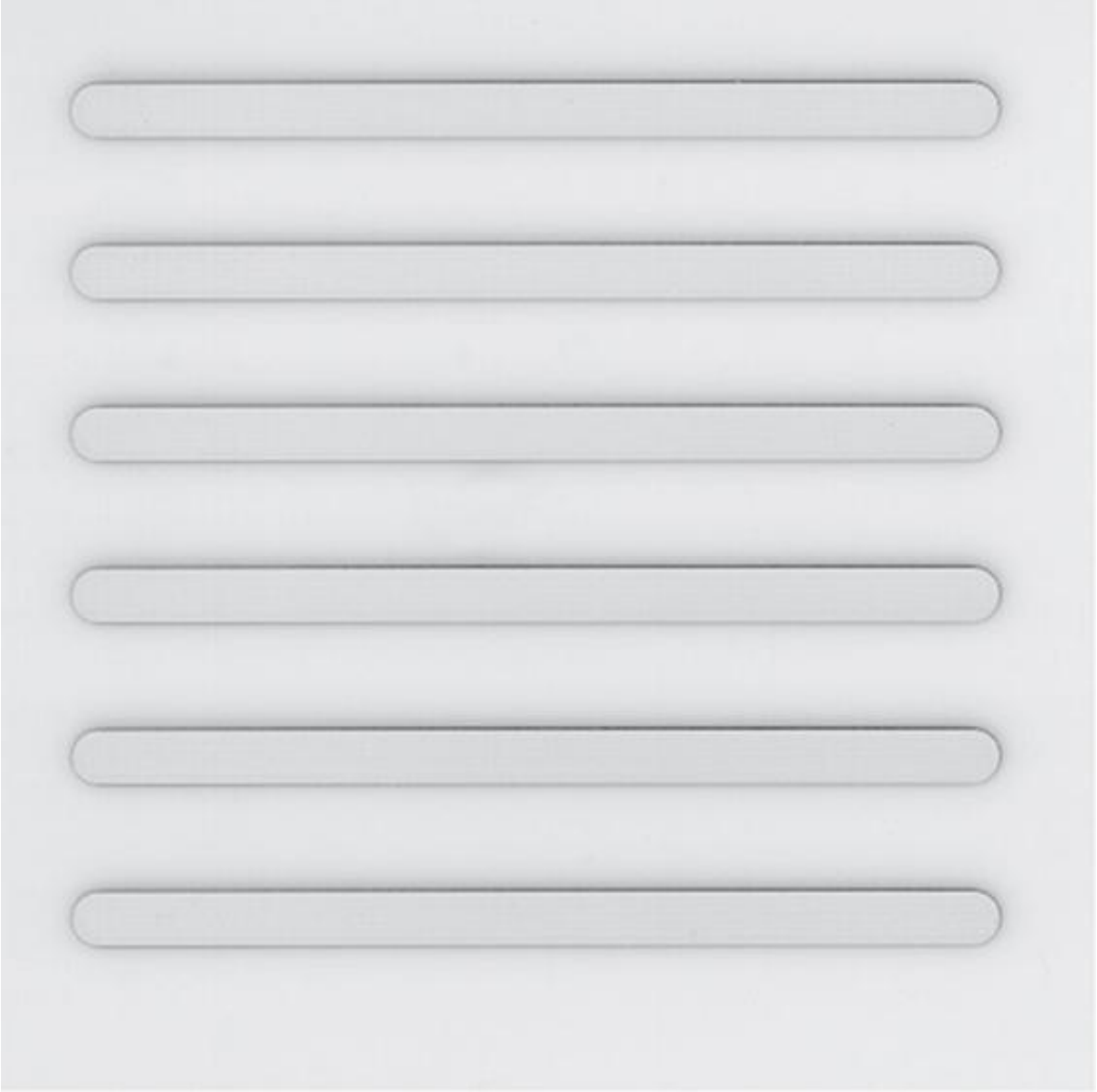


FIGURE 15.1 Test pattern used for a copper peel strength test.

The material being tested should be processed using the same fabrication steps that will be applied for the actual product. IPC-TM-650, method 2.4.8, recommends a specimen size of 50.8 mm × 50.8 mm (2.0 in. × 2.0 in.) and a minimum sample size of two for both the warp and fill (X and Y) direction of the laminate. The end of the test strip is peeled off so that a tensile tester can clamp it. The load cell should be calibrated to account for the weight of the clamp. The copper foil strip is then peeled from the material at a

rate of 2 in. per min. The measured value is dependent on the copper thickness. The thicker the copper foil, the more force is required to deform it plastically. The value is also dependent on the angle at which it is being pulled. Therefore, it is always important to specify the thickness of the copper foil tested and to maintain a peeling force radius of 90° during the test. The minimum load is determined as specified and the peel strength is calculated using Eq. 15.1:

$$\text{lb/in} = L_M/W_S \qquad (15.1)$$

where L_M = Minimum load
W_S = Measured width of peel strip

Copper bond retention after exposure to soldering or touch-up temperatures is measured as outlined in IPC-TM 650, method 2.4.8, condition B. The test samples are covered with silicone grease before floating them on the solder pot at 288°C for 5 to 20 sec. to avoid solder contamination on the test strip. After allowing the samples to cool down to room temperature and removing the grease, the test is performed in the same way as previously described. It is important to inspect the specimen for any blistering or delaminations prior to testing (see also the discussion of solder shock testing in Sec. 15.5.2) as this may interfere with the test procedure and may indicate that the laminate material has problems with solder shock resistance.

Another factor that can influence the adhesion strength of the copper foil is exposure to processing chemicals during manufacturing. Details about this test method can be found in IPC-TM 650, method 2.4.8, condition C. This test is usually performed only if specific requirements at the end-product level call for it or if the material during manufacturing exhibits low copper bond retention properties.

Minimum copper peel strength values for unstressed material should be 1 N/mm or higher. The acceptable values after thermal stress are 0.8 N/mm and 0.55 N/mm after process solutions. Measurements taken at elevated temperature (125°C) should yield a minimum value of 0.7 N/mm. The authors recommends using the preceding values as guidelines and validating acceptable minimum values with actual product requirements.

15.4.3 Solder Shock

The solder shock test is one of several methods to assess the thermal resistance of copper-clad laminates. It is easy to perform and represents another key test during the early assessment of a material. There are a number of different methods to choose from, which will be described in detail in Sec. 15.5.2. During the initial assessment of the material, it is important to choose at least one of the described test methods to make certain that the material meets the minimum requirements, especially if the material is used in higher-temperature lead-free assembly processes. Aside from solder shock testing of bare laminate material, it is also recommended that the PCB engineer consider PCB-level temperature shock as well as repeated reflow testing with a particular focus on resin-reinforcement delaminations. This will ensure that not only the raw material but also the completed PCB will be able to withstand the required temperature regime.

15.4.4 Glass Transition Temperature (T_g)

A further important data point within the initial assessment is the determination of the glass transition temperature (T_g).

Different test methods are described in more detail in Sec. 15.5.2. For the first assessment, one method should be selected. When choosing the method, it is important to make sure that the test procedure is compatible with the material in test (for some materials, the glass transition can be determined only using dynamic mechanical analysis [DMA]). A minimum of two samples should be tested. If a data sheet of the material is available, the measured value should correspond with the manufacturer's data (within the measurement accuracy of the equipment). The values of T_g1 and T_g2 (measured on the same sample) should not be more than 7°C apart. If T_g2 is significantly below the T_g1 measurement, this may be a strong first indication that resin system degradation has started during the measurement procedure. It is recommended to confirm this finding using the T_d measurement procedure.

15.4.5 Thermal Decomposition Temperature (T_d)

The determination of the thermal decomposition temperature (T_d) completes the initial assessment. This is a new test methodology, and both ASTM and IPC test procedures are available. IPC-TM-650, method 2.3.40, is called "Procedure to Determine the Thermal Decomposition Temperature T_d Using Thermo Gravimetric Analysis (TGA)," and the ASTM methodology is called "Standard Test Method for Rapid Thermal Degradation of Solid Electrical Insulating Materials by Thermo Gravimetric Analysis." In both cases, the test methodology is based on thermogravimetric analysis (TGA) of a laminate specimen that is heated with a set ramp rate assessing the onset and process of decomposition. At first, the thermoset laminate resin passes the glass transition point where the polymer changes from a rigid, brittle, and

“glasslike” state to a softer and more rubberlike material. As the material is heated further, the three-dimensional cross-linked structure begins to break down and individual bonds in the polymer structure open. As decomposition continues, gaseous decomposition products are set free, which can be detected as a loss of mass of the sample in test. This usually goes hand in hand with visible damage to the sample (delamination and/or strong discoloration) and significant changes in the mechanical properties of the laminate.

A dry test specimen of 2–20 mg is heated at 5°C/min to 150°C and then held at that temperature for 15 min. This ensures that the sample is completely dry and establishes the base weight used to characterize the weight loss. Then the sample is heated at 5°C/min up to a temperature of 800°C and the weight loss is continually recorded. The temperature at which a 5 percent weight loss of the sample is detected is defined as the T_d.

Although this test methodology is a good gauge of the thermal stability of laminate materials, the method and results must be evaluated carefully to ensure that correct conclusions are drawn from the results. For example, the results of this test are dependent on the surface/volume ratio of the specimen in test-specimens of the same weight, but different surface areas will show different results. The sample with the large surface area loses weight at a faster rate and therefore shows a lower T_d. Samples with a large percentage of nondecomposing filler or reinforcement material will also behave differently as the measured weight change is based only on the resin content of the sample. This again will lead to a seemingly higher measured T_d, which may lead to erroneous conclusions. Finally, the process of decomposition is as important as the determined value of T_d and a comparison of the onset of weight loss may also be a valuable parameter to assess when comparing laminate materials using this methodology.

In general, a higher T_d value is desirable for materials that are being selected for lead-free assembly processes as this indicates that the laminate withstands the higher assembly temperatures with an increased margin.

Figure 15.2 shows an example of different T_d measurements for three different laminate materials. It shows the typical decomposition rates for some sample materials and also highlights how the assessment of a material can change if different criteria are chosen. If the IPC value of 5 percent weight loss is chosen, then M3 is superior to M1 and M2. But if the materials engineer decides that the onset of weight loss (decomposition) is critical for the application, then M3 is the worst performing material. The authors recommend using materials with a high onset temperature as well as a high 5 percent decomposition temperature.

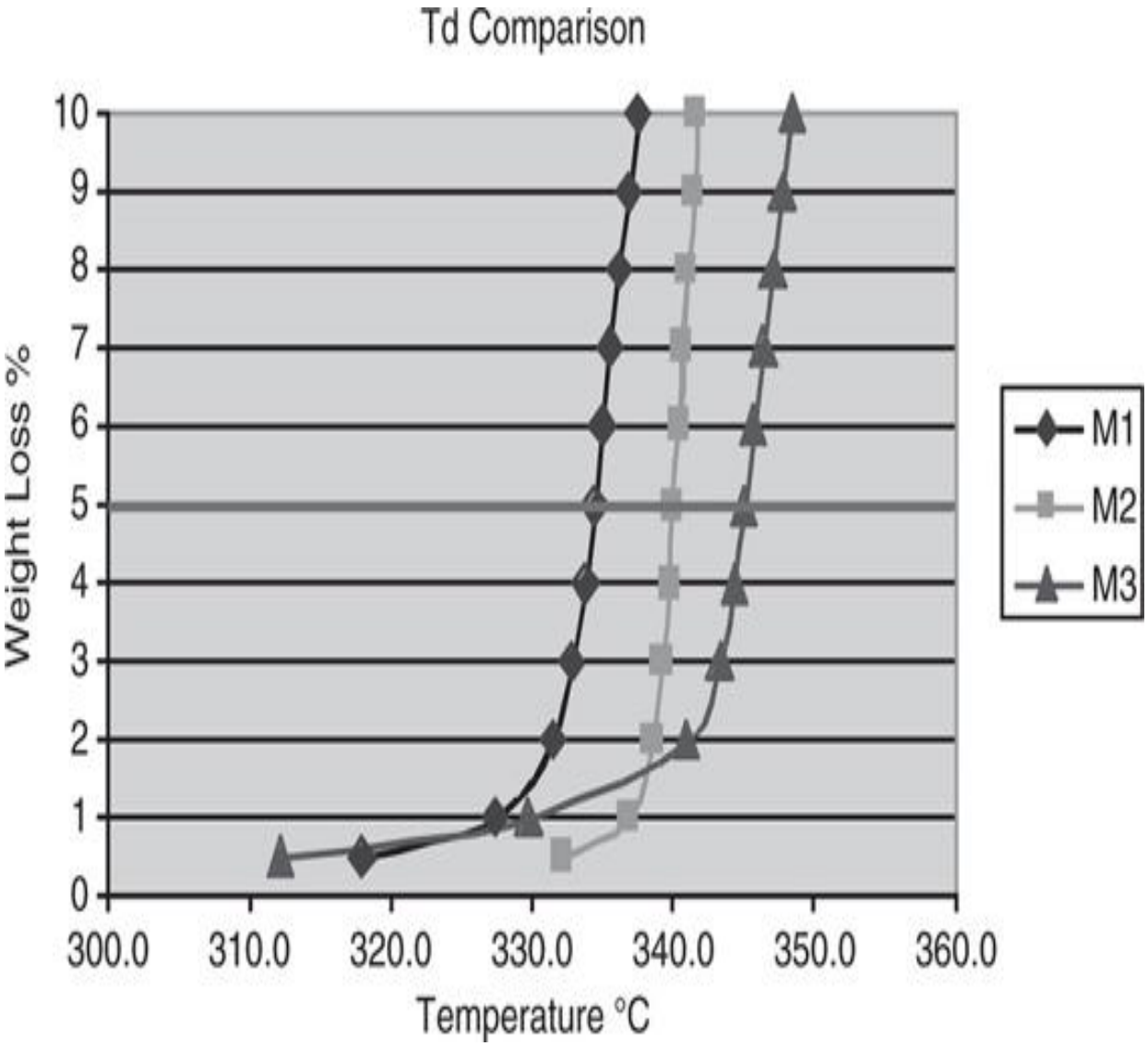


FIGURE 15.2 Example of different T_d measurements for three different laminate materials. (*T_d GraphCourtesy of Helmut Kroener, Multek*.)

15.5 FULL MATERIAL CHARACTERIZATION

The following set of characterization methods summarizes the most commonly used test methods to qualify copper-clad laminates for manufacturing. It is intended to guide the materials engineer through the laminate qualification

process. Yet it can only serve as a best-practices guide, as the final set of qualification methods will vary for each material and should always be driven by its specific application.

15.5.1 Mechanical Tests

Commonly used mechanical tests include tensile tests, flexural strength tests, and copper peel strength tests.

15.5.1.1 Modulus and Tensile Strength (Tensile Test). The test method to determine modulus and yield stress for copper-clad laminates described in this section is based on ASTM D 882, “Standard Test Methods for Tensile Properties of Thin Plastic Sheeting.” Other relevant industry standards are IPC-TM-650, method 2.4.19 (for flexible laminate materials), and IPC-TM-650, method 2.4.18.3 (for deposited organic free films). Elastic modulus and yield stress are always determined by the same method.

The elastic modulus is the indicator value for the stiffness and strength of a composite material under load, whereas the yield stress indicates the maximum load the material can take in x/y direction before it brakes. The modulus is the more important of the two values. It is used to differentiate materials and their actual strength during qualification testing. The elastic modulus is also one of the key properties of a material that need to be understood when performing computational modeling of packages and printed circuit board assemblies. In many applications, materials with different properties are combined, which leads to thermomechanical stresses that cause fatigue or interfacial failures. Computational modeling is often used when there is not sufficient time or resources available to perform actual product test, but fast reliability assessments are needed.

The standard test specimen for this test consists of a strip of laminate material 152.4 mm (6 in.) long and 15.7 mm (0.5 in.) wide. A minimum of 10 samples should be prepared and all copper must be removed before testing. It is important that only samples with identical thickness and glass stack-up be tested, as this will allow a meaningful comparison of the materials in the test. The test engineer also must ensure that both the warp and fill direction of the laminate composite are measured and documented separately.

After the samples are cut, they need to be inspected for any fractures, delamination, or roughness along the edges and if necessary they need to be sanded. The cross-sectional area of each specimen is calculated from the width and thickness in the measurement area. Then the individual samples need to be conditioned at 23°C (73.4°F) and 50 percent relative humidity (RH) for 24 hours. Although most specifications recommend conditioning of the material prior to cutting and preparation of the samples, the authors recommend first cutting the specimens to size and then conditioning them. This ensures more uniform properties of the individual samples.

The tests are performed using a standard tension and compression apparatus, which can be operated at a controlled rate of crosshead movement. The load-extension curve should be recorded and the specimen tested until it breaks. If extensometers are used, it is necessary to minimize the stress on the sample at the contact points of specimen and indicator.

The tensile strength is calculated by dividing the maximum load at break by the original minimum cross-sectional area. The unit is megapascals (MPa). Dividing the elongation at break by the initial gauge length and multiplying it by 100 will calculate percent elongation. When extensometers are employed, only the length of the section between them is used; otherwise, the distance between the grips represents the initial gauge length. Young’s modulus is calculated by

drawing a tangent to the linear portion of the stress-strain curve, selecting any point on this tangent, and dividing the tensile stress at that point by the corresponding strain. The unit is gigapascals (GPa). For all calculations, the values for 10 samples should be recorded and the average calculated.

In addition to the absolute values for the different mechanical properties, the stress-strain curve gives the materials engineer information about the elastic and plastic portion of the deformation in the laminate samples. The elastic (linear) part of the deformation is restorable, whereas plastic changes in the materials are not. Figure 15.3 shows a typical stress-strain curve.

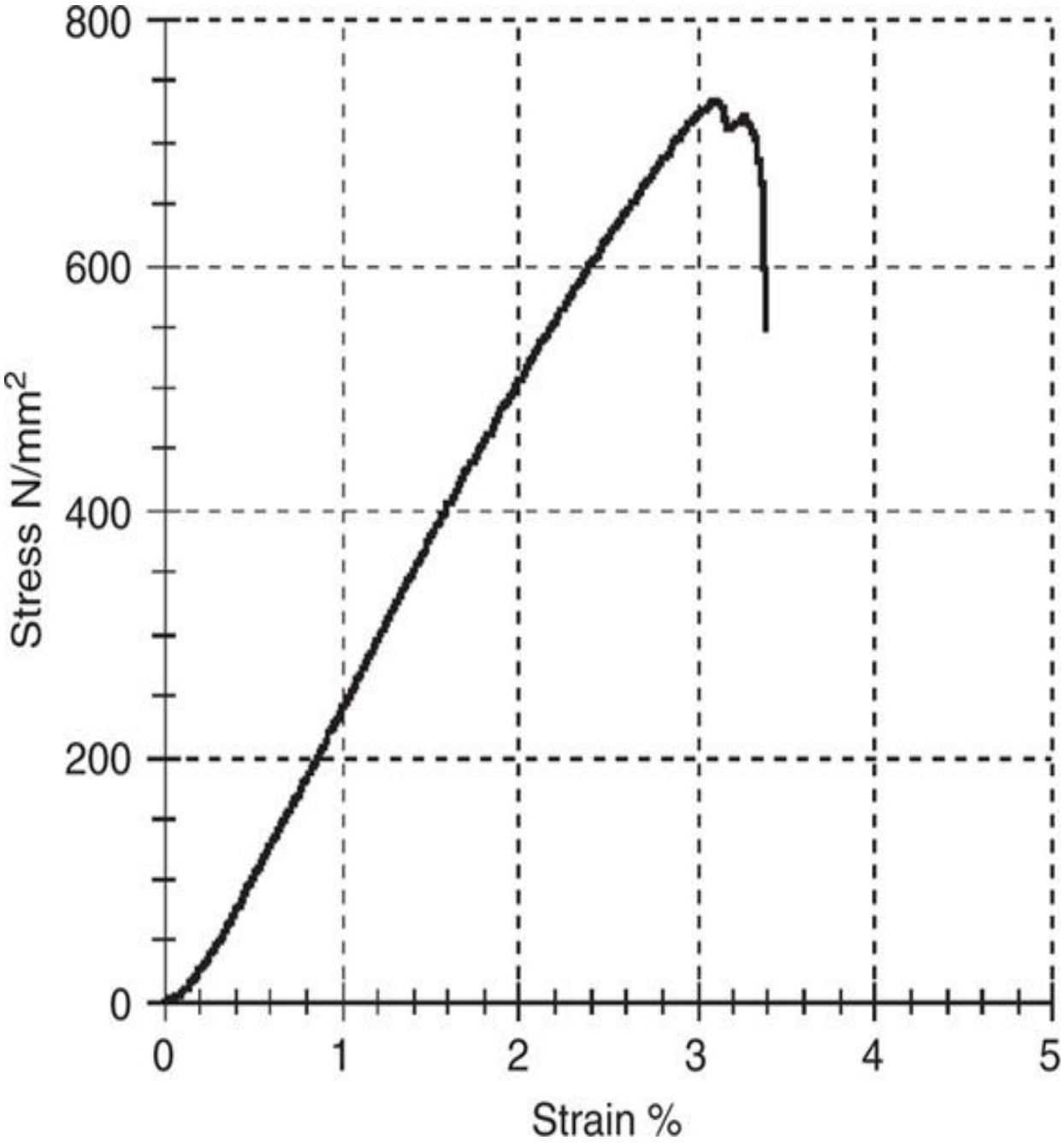


FIGURE 15.3 Typical stress-strain curve.

15.5.1.2 Flexural Strength. The test method to determine the flexural strength of copper-clad laminates is based on ASTM D 790 (“Flexural Properties for Un-Reinforced and Reinforced Plastics and Insulating Material”) and IPC-TM-650, method 2.4.4B (“Flexural Strength of Laminates at Ambient Temperatures”). The test method described in the

preceding section to determine the modulus in tensile mode does have the inherent problem that the glass reinforcement and its properties have a large influence on the results. This may be avoided when testing copper-clad laminates in flexural mode. Here the attributes of the resin system have a greater influence on the outcome of the test. When comparing the test results of different laminate materials, it is important to compare only data that were generated using the same test method.

This test also requires that the copper be completely removed from the laminate material by means of standard etching processes. The specific size (length and width) of the samples and test parameters (test span and speed) are dependent on the thickness of the laminate and can be found in IPC-TM-650, method 2.4.4. See Fig. 15.4 for a typical flexural strength measurement curve.

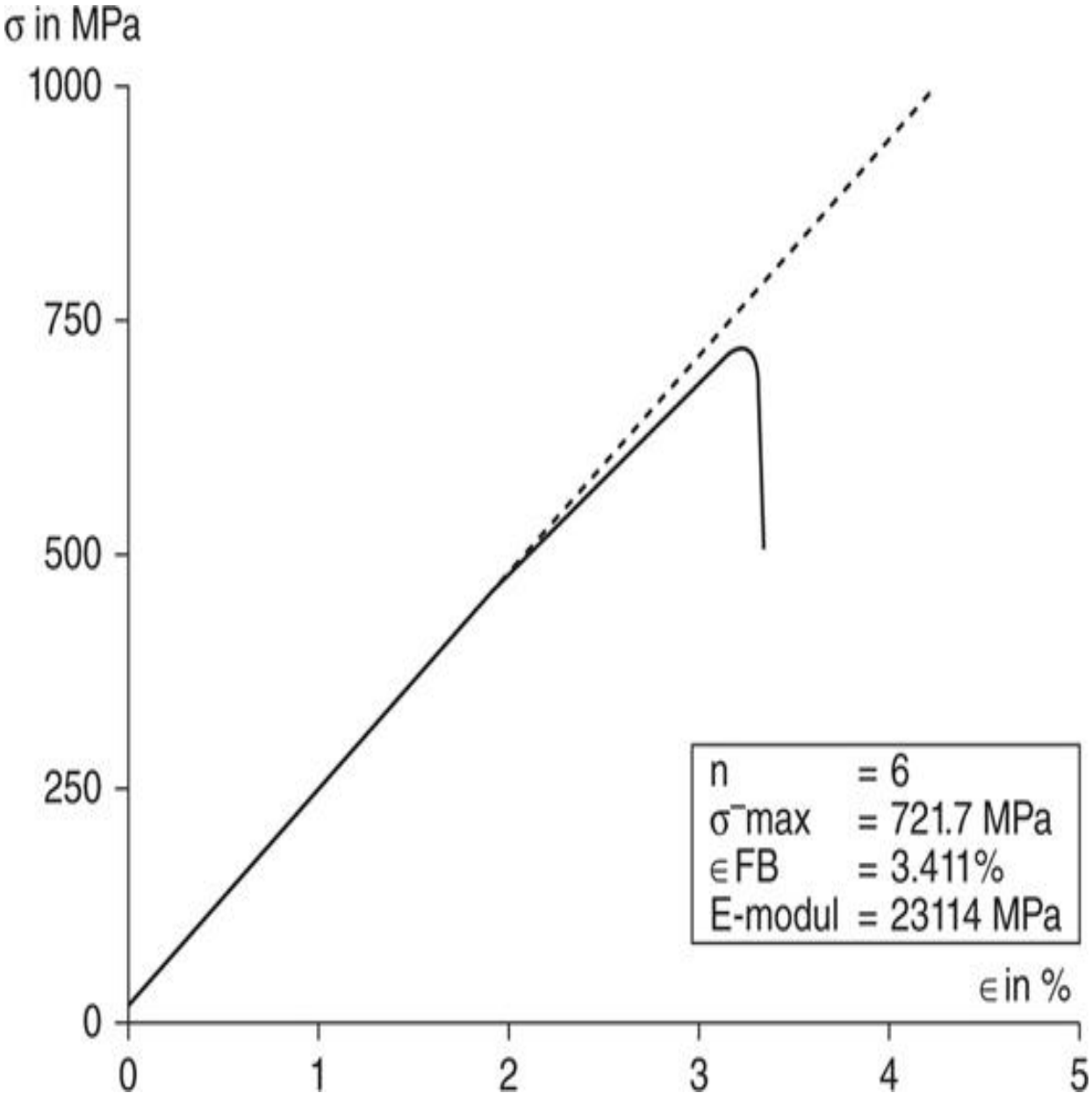


FIGURE 15.4 Typical flexural strength measurement curve.

The samples are conditioned to room temperature. They are then centered on the supports of the standard tension and compression test apparatus with the long axis of the specimen perpendicular to the loading nose and support. The samples are loaded at the defined speed and tested until they break. The load at breakage should be recorded. Use Eq. 1.2 to calculate the flexural strength.

$$S = 3PL/2bd^2 \qquad (15.2)$$

where S = Flexural strength (psi)
P = Load at breakage (lb.)
L = Span (in.)
B = Width of specimen (in.)
D = thickness (in.)

15.5.1.3 Copper Peel Strength (Before and After Thermal Stress). Test methods are described in Sec. 15.4.2 and results can be transferred to this point in the evaluation. To complete the data, perform additional tests if necessary after specific thermal stress (solder dip, reflow with different peak temperatures, and/or different dwell times) or after exposure to plating solutions.

15.5.2 Thermomechanical Tests

Properties that are tested thermomechanically include T_g, CTE, thermal resistance, solder dip resistance, and solder float resistance.

15.5.2.1 Glass Transition Temperature T_g (DSC, TMA, and DMA). The resin systems used in today's copper-clad laminates are almost all three-dimensionally cross-linked thermoset polymers. This means that the materials are manufactured (in a curing reaction) into a hard final product and cannot be remelted many times the way thermoplastic polymers can. In many cases, different resin systems are blended to create a material with specific properties. The functionality of the individual resins and their ratio in the blend define the properties of the thermoset. The degree of cure of the hardened thermoset resin system can be

described by characteristics such as percent of uncured monomer and heat of final cure or by mechanical properties such as hardness, modulus, and yield stress. But one of the most commonly used characteristics to describe the degree of cure and cross-link density of a thermoset polymer is the glass transition temperature (T_g).

The simplest definition of the T_g of a laminate is to call it the temperature at which the mechanical properties of a laminate change (deteriorate) rapidly. It is at this temperature that the polymer changes from a rigid, brittle, and “glasslike” state to a softer and more rubberlike material. However, this should not be confused with the melting point of a crystalline substance or the extreme softening of a thermoplastic polymer. In a thermoset material at T_g, the relative mobility of the cross-linked polymer molecules changes. Below T_g, they are immobile and the material is rigid; above T_g, the relative mobility of the molecules increases and slight movements are possible, which leads to a loss of mechanical strength in the material. Although all of the methods described in this section enable us to determine a specific glass transition temperature for laminate materials, it also needs to be emphasized that the glass transition in thermoset resins is not a single defined temperature. It usually occurs within a temperature range (for some resin systems, the range can span as much as 100°C), and the T_g is determined within this range.

In addition, the difference between T_g and T_d must be pointed out here. T_g is the temperature at which mechanical properties of the material change, whereas T_d is the temperature where the material starts to irreversibly degrade. If one wants to assess a laminate’s capability to withstand high-temperature lead-free processing temperatures, T_d is the more relevant measure. T_g is relevant when assessing loss of mechanical strength which

can lead to PCB warpage, bowing, and increased z-axis expansion, which in turn can have a significant impact on PCB reliability.

There are a number of different measurement techniques to determine the T_g. The most commonly used methodologies are thermal analysis techniques. Other techniques are available (such as spectral analysis and electrical characterization), but their use is limited and therefore they will not be discussed here. The three thermal analysis methods that will be discussed in this section are as follows:

- Differential scanning calorimetry (DSC)
- Thermomechanical analysis (TMA)
- Dynamic mechanical analysis (DMA)

All of these techniques measure slightly different property changes in the laminate material and therefore the values that are obtained will be different. They usually will follow this simple rule of thumb:

$$T_g \text{ (DMA)} > T_g \text{ (DSC)} > T_g \text{ (TMA)}$$

15.5.2.1.1 T_g by Thermomechanical Analysis (TMA). Thermomechanical analysis measures dimensional changes in a material as it is heated from room temperature to a preset final temperature. The change in length (width or height) of the specimen with the change in temperature determines the CTE of the material. At T_g, the expansion coefficient of the material changes and it is this property change that is used to determine the T_g by TMA.

The test procedure is specified in IPC-TM-650, method 2.4.24C. The specimen should have a minimum thickness of 0.51 mm and at least two samples taken from random locations in the material need to be tested. Any copper

cladding needs to be removed by etching. The treatment of the copper foil leaves a negative imprint on the laminate surface, which can lead to problems during the measurement right below the actual glass transition temperature. Therefore, the surface of the specimen should be sanded lightly prior to testing. The edges of the sample should also be smooth and burr-free. Use care to minimize stress or heat on the specimen.

The samples need to be preconditioned for 2 hours at 105°C (221°F), then cooled to room temperature in a desiccator. The actual measurement should be started at a temperature no higher than 35°C (95°F); an initial temperature of 23°C is recommended. Unless otherwise specified, a scan rate of 10°C (18°F) per min. is commonly used. The temperature ramp needs to be continued at least 30°C (54°F) above the anticipated transition region. The T_g is defined as the temperature at which the two tangent lines for the thermal expansion coefficient intersect. Figure 15.5 shows an example of a typical TMA scan. The material has a T_g of 136.7°C.

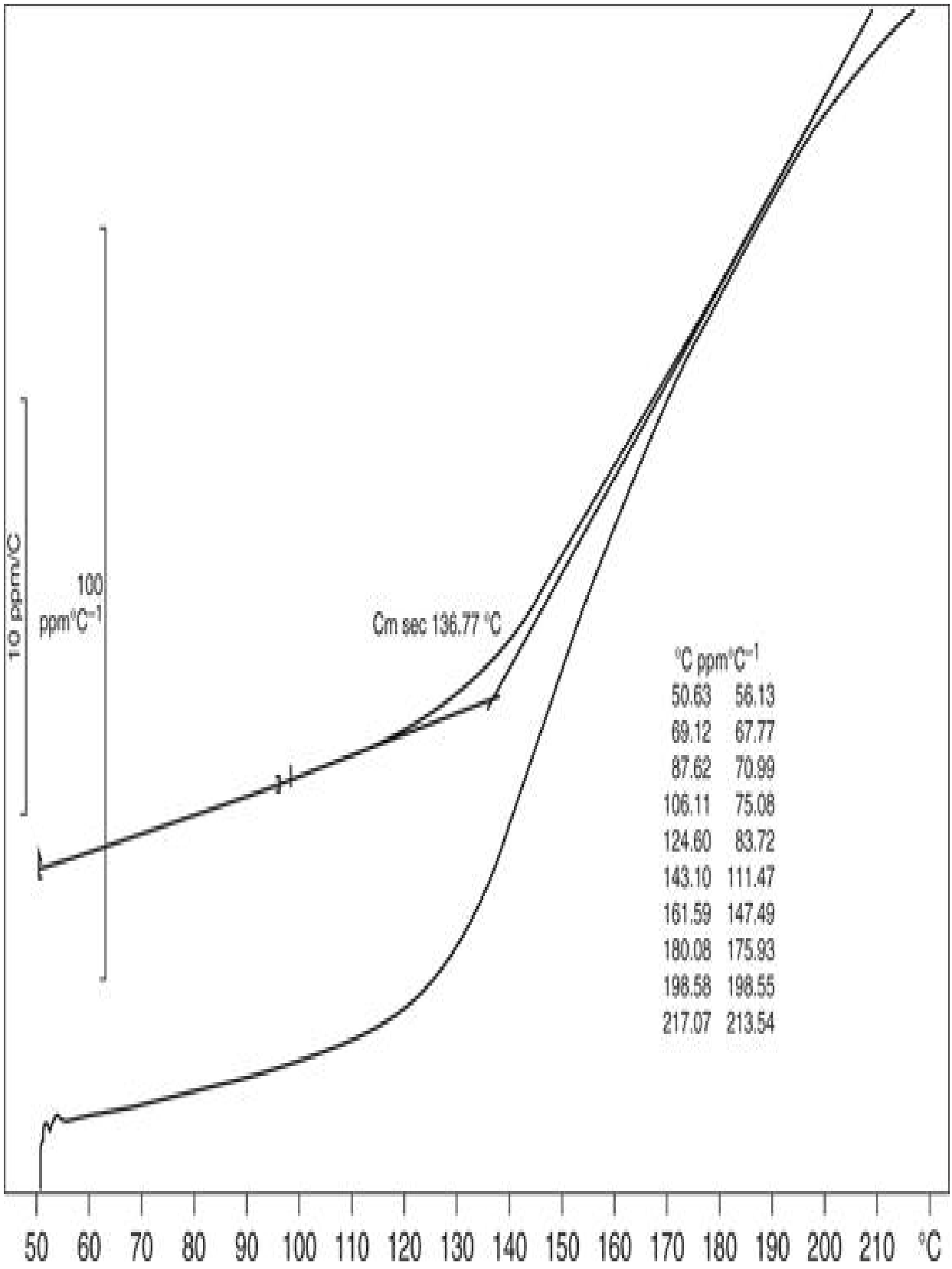


FIGURE 15.5 Typical TMA scan.

It is recommended to retest the same sample after allowing it to cool down to room temperature to determine whether the measured value for T_g2 is comparable to the measured value of T_g1. If T_g1 is significantly lower than T_g2, then this could be an indication that the sample material was not fully cured when it was tested the first time. If T_g1 is significantly higher than T_g2, that could indicate that the sample material has already started to decompose and was approaching T_d. The authors recommend further testing if these measurements differ by more than 5°C.

15.5.2.1.2 T_g by Differential Scanning Calorimetry (DSC). Differential scanning calorimetry measures the difference in heat absorption or emission from a test specimen in comparison to a reference sample (usually nitrogen gas). This makes the technique applicable to determine a variety of property changes in polymer materials. It can detect the exothermic cure reaction, crystallization energy, and residual reactivity in polymers, as well as endothermic melting points. For epoxy-based resin systems, DSC is a well-suited technique as these materials go through a crystalline transition at T_g and this property change can be used to determine the glass transition. For other resin systems that are more amorphous and have a T_g that occurs over a wider range (such as polyimides), the detection may be more difficult by DSC than TMA.

The test procedure is specified in IPC-TM-650, method 2.4.25C. The specimen should be a solid piece weighing between 15 mg and 25 mg. In the case of very thin materials, multiple pieces may be used. The specimen should be of the size and configuration that fits within the sample pan of the DSC equipment. All of the specimen preparation needs to take place before preconditioning to avoid any moisture influence prior to testing. Sample edges should be smoothed and burrs removed by light sanding or

an equivalent method to achieve proper thermal conduction. Use care to minimize stress or heating of the specimen. Even though the IPC test method allows samples to be tested with copper cladding, the authors recommend testing only without copper cladding. This increases the relative mass of polymer in the DSC sample pan and leads to a better signal and detection of T_g.

The samples need to be preconditioned for 2 hours at 105°C (221°F), then cooled to room temperature in a desiccator for at least a half-hour prior to testing. Place the specimen in a standard aluminum sample pan with an aluminum lid. For reference purposes, a cover lid crimped onto the sample pan should be used. Start the scan at a temperature at least 30° lower than the anticipated onset of T_g. Unless otherwise specified, a scan at a rate of 20°C/min (36°F/min) is recommended and the temperature ramp needs to be continued at least 30°C (54°F) above the anticipated transition region. The glass transition temperature is determined using the heat flow curve. In many cases, the DSC equipment will have applicable software installed to determine T_g. A tangent line is fit onto the curve above the transition region, and a second tangent line is fit below the transition region. The temperature on the curve halfway between the two tangent lines, or 1/2 *d* Cp, is the glass transition point T_g. Figure 15.6 shows an example of a DSC scan where the material has been scanned twice. The T_g of the first scan was 192.9°C. The second scan yielded a slightly higher value of 195.3°C (likely caused by additional curing of the material).

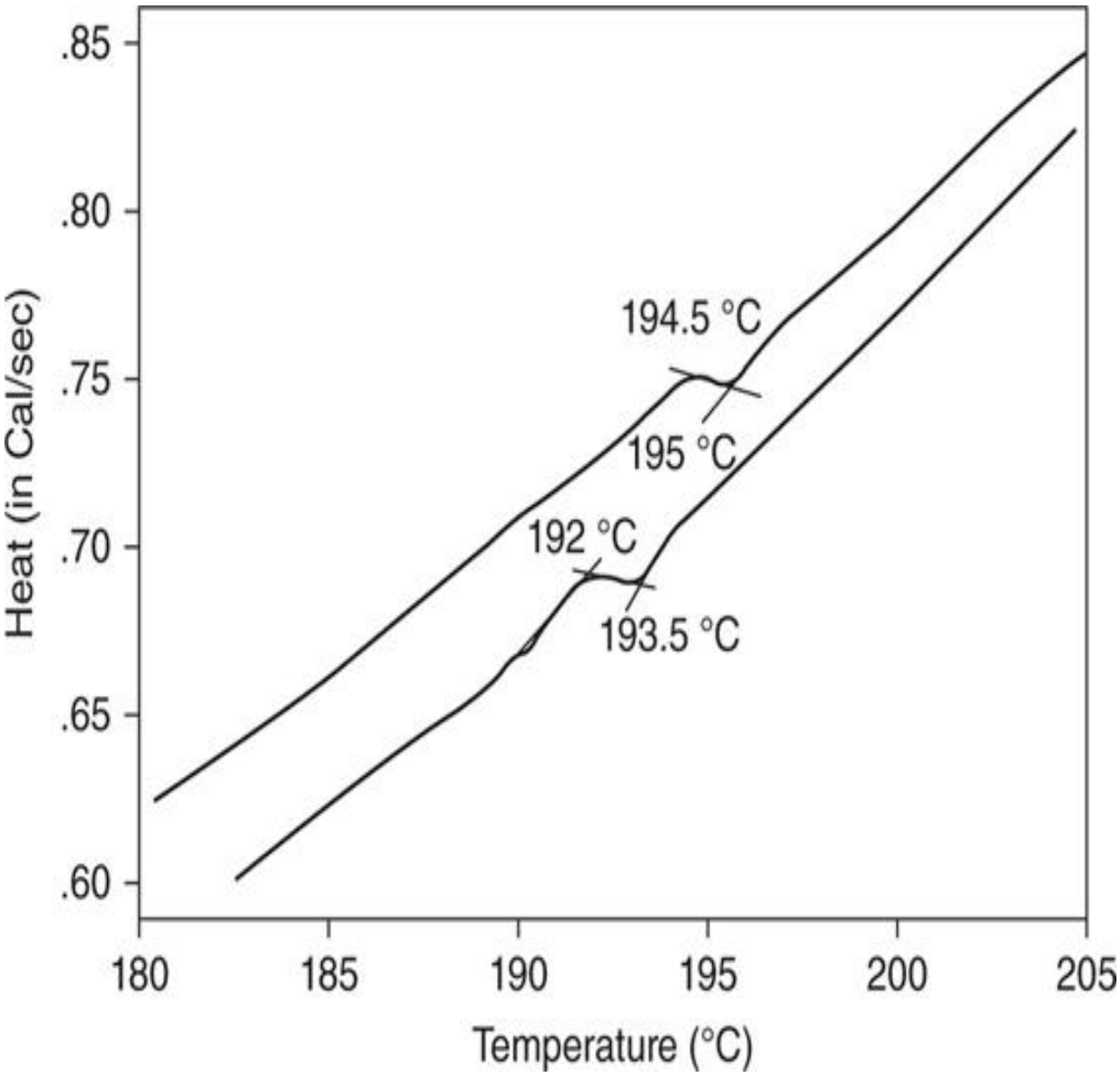


FIGURE 15.6 Example of a DSC result.

15.5.2.1.3 T_g by Dynamic Mechanical Analysis. Dynamic mechanical analysis (DMA) applies an oscillatory stress or strain on the sample while the temperature is increased during the experiment. The ability of the material to elastically store the mechanical strain energy changes during the heat cycle as it changes its viscoelastic behavior from glassy to rubbery. This property change determines the glass transition temperature by DMA.

The test procedure is specified in IPC-TM-650, method 2.4.24.2. The test specimen should consist of a strip of laminate material compatible to the measuring equipment. For all samples with woven reinforcement, it is necessary to make sure that the specimens are cut parallel or perpendicular to the woven structure. The analysis is based on an assumption of constant specimen geometry; therefore, the test specimens must be stiff enough not to deform plastically during the experiment. All copper needs to be etched off.

While the IPC-method recommends preconditioning of the samples at 23°C and 50 percent RH for at least 24 hours prior to testing, the authors recommend preconditioning similar to that employed for TMA or DSC measurements. Samples are baked for 2 hours at 105°C (221°F), then cooled to room temperature in a desiccator for at least a half-hour prior to testing. The sample is mounted in the fixture making sure that it is perpendicular to the clamps. Both clamps are tightened using torque screwdrivers to ensure that the sample does not slip during the measurement and that no stresses have built up around the sample that could negatively influence the results. The sample is loaded with a frequency of 1 Hz (6.28 radian/sec) while it is heated in dry nitrogen or dry air at a rate of no faster than 2°C per min. The temperature ramp needs to be continued at least 50°C above the transition region. The glass transition temperature is defined as the temperature corresponding to the maximum in the tan δ versus temperature curves at a frequency of 1 Hz. Tan δ is calculated from Eq. 15.3.

$$\tan \delta = E''/E' \qquad (15.3)$$

where $E'' =$ loss modulus

$E' =$ storage modulus

Figure 15.7 shows an example of a typical DMA scan. The material has a T_g of 193.17°C.

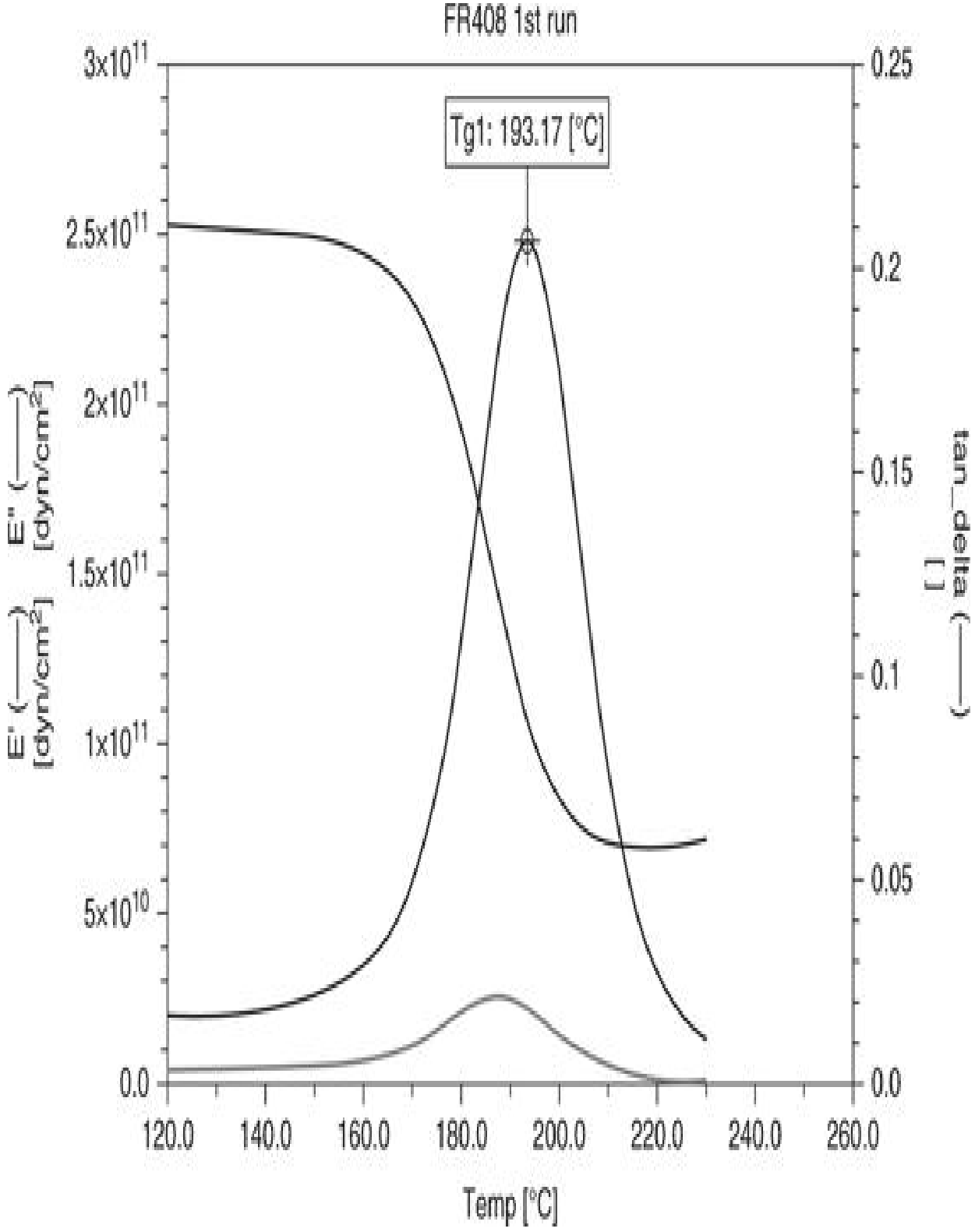


FIGURE 15.7 Typical DMA scan.

15.5.2.2 Coefficient of Thermal Expansion. The coefficient of thermal expansion (CTE) describes the property of materials to expand as they are being heated. Because of the reinforced composite construction of most laminates, the CTE in x and y direction is usually different from the CTE in z direction. By convention, the x direction corresponds to the warp direction of the reinforcement, whereas the y direction corresponds to the fill direction of the fabric. The z direction is the direction perpendicular to the plane of the laminate. The difference between the values is caused by the reinforcement, which severely restrains the expansion in x and y, whereas the resin can expand unrestrained in the z direction.

For copper-clad laminate materials used in printed circuit boards, the CTE in x, y, and z direction is of great importance. The x and y direction is critical because of all the components that will be mounted on the final printed circuit board. The greater the mismatch between the laminate material and the soldered components, the higher the risk that temperature changes will lead to solder fatigue and eventually to a reduction in the reliability of the board. The z direction is of equal importance because the expansion of the laminate during thermal cycles will lead to stresses in the copper plating (CTE of 17 ppm/K) of the plated through or buried holes in the board. A low z-axis CTE and high T_g are therefore generally desirable for increased through hole reliability.

A number of different measurement techniques are available to determine the CTE of copper-clad laminates. The most commonly used is TMA following IPC-TM-650, method 2.4.24C, as described in Sec. 15.2.1. When determining the CTE of a laminate, the temperature scan must start at a temperature sufficiently lower than the specified temperature range for which the CTE is being determined to allow the heat rate to stabilize. The typical scan rate is also 10°C (18°F) per min. and the scan should be continued to at

least 250°C (482°F). Because the expansion properties of the material change at T_g, there are usually two CTE values that are being reported: the CTE below T_g is commonly referred to as $a_{1,}$ and the CTE above T_g as a_2 (see Eq. 15.4).

$$\text{CTE:}\alpha = \Delta L/\Delta T \text{ ppm/K} \qquad (15.4)$$

where ΔL = change in length
ΔT = change in temperature
K = degrees Kelvin

In the TMA scan example (Fig. 15.5), the material has a z-axis CTE(a_1) of ~ 65ppm/K and a z-axis CTE(a_2) of ~150ppm/K.

The CTE in x and y direction can also be measured by TMA, although care must be taken during the preparation of the sample to avoid any influence of reinforcement material on the TMA probe. The results are strongly dependent on the properties of the reinforcement fabric.

Another method to determine the x- and y-axis CTE of laminate materials employs strain gauges. This method is described in IPC-TM-650, method 2.4.41.2. Many details need to be taken into consideration when making use of this method. The strain gauges need to be calibrated for the specific temperature range and the adhesive used to attach them needs to be stable over the whole range. Special care needs to be taken during specimen preparation and gauge attachment. It is recommended to run one heat cycle prior to the actual measurement to remove any residual stresses. More details can be found in IPC-TM-650.

15.5.2.3 Thermal Resistance. The thermal resistance of laminate materials is one of the key properties, especially in light of the lead-free processing conditions. It is the most

important indicator of the performance of printed circuit boards during assembly operations. As already mentioned in the Sec. 15.1, most printed circuit boards will be required to withstand at least five reflow cycles with a peak temperature in the range of 260°C, but that number may increase to six and above for more complex assemblies. During exposure to these process temperatures, the laminate cannot delaminate or begin decomposition. Another important factor that can be assessed with thermal resistance tests is the performance of the laminate in printed circuit board applications that expose the board to high-operating temperatures. Several different test methods should be considered when qualifying laminates.

15.5.2.3.1 Solder Dip Resistance. The test method is described in IPC-TM-650, method 2.4.23. The original purpose of this test technique was to assess the solderability of the laminate surface, but today it is often used to assess the ability of laminate materials to withstand the temperatures in a molten solder bath. It is important to note that the original IPC methodology has not been revised in a long time and the current version may not reflect the actual temperature requirements of lead-free processing. The authors still feel that this method is a very good assessment and differentiation technique for laminate materials and recommend that either solder pot temperatures or exposure times are increased if the laminates are intended for use in lead-free assembly processes. Performance factors that are being considered are resistance to softening, loss of surface resin, scorching, delamination, blistering, and measling.

The material will be tested in three different surface configurations: (1) a surface upon which no metal cladding was ever applied (if possible), (2) a surface with the metal cladding removed by standard etching processes, and (3) a surface with metal cladding as received. The sample size for all specimen is 1¼ in. × 1¼ in. thickness and three samples

are required for each surface configuration. All samples are tested using the same procedure.

Preclean the samples by immersing them for 15 sec. in 10 percent hydrochloric acid (HCl) (by volume) and then rinse in water. The HCl should be at a temperature of 60°C (140°F). Dry the specimen quickly to avoid excess oxidation of the sample. Dip the sample into a flux agent and allow draining for 60 sec. before proceeding with the solder dip. Stir and then skim the surface of the molten solder with a clean stainless steel paddle to ensure that the solder is of uniform composition and at a temperature of 245°C (473°F). Immerse the specimen edgewise into the molten solder. The insertion and withdrawal should be at a rate of 1 in. per sec. and the dwell time in the solder should be 4 sec. Upon withdrawal, allow the solder to solidify by air-cooling while the specimen is in a vertical position. Thoroughly remove the flux.

The samples are examined for any evidence of discoloration or surface contaminants, loss of surface resin, softness, delamination, interlaminar blistering, or measles. The specimens having metal cladding also need to be examined for blistering or delamination of the metal foil from the laminate material.

15.5.2.3.2 Solder Float Resistance. This test addresses the thermal resistance of the laminate material floating on the solder bath. Because this method subjects the sample to a thermal gradient across the z-axis of the material similar to an actual wave solder operation, the results of this test are particularly important and—as mentioned previously—either solder pot temperatures or exposure times should be increased if the laminates are intended for use in lead-free assembly processes.

The test method follows IPC-TM-650, method 2.4.13. At least two samples need to be tested for each material and they should be taken from random locations. For double-clad laminate, the copper foil needs to be removed from the

backside of each specimen by using standard etching processes. The test samples need to be preconditioned in an air circulating oven at 135°C for one hour to remove any excess moisture that could lead to premature failures. After preconditioning, the specimens can be held in a desiccator at room temperature. After attaching the sample to the solder float test fixture, float it for 10 sec., foil side down, on the surface of the molten solder at a temperature of 260°C (for method A) or 288°C (for method B). Then remove the sample and tap the edges to remove any excess solder. Thoroughly clean and visually examine the sample for blistering, delamination, or wrinkling.

In case more than one material is being qualified and no failures are being observed after testing for 10 sec. or if the goal is to determine the weakest point in the laminate and test to failure, then the authors recommend increasing the solder float time incrementally or repeating the test with the same sample until failures are observed.

15.5.2.3.3 T260 (TMA). Aside from testing materials in solder baths, there is one other technique to verify the thermal resistance of laminates. This test method is described in IPC-TM-650, method 2.4.24.1, and is used to determine the time to delamination of laminates and printed boards using a TMA system (see also sec. 15.5.2.1.1).

The sample requirements are identical to the ones for determination of the T_g by TMA. A minimum of two specimens should be tested, which can be taken from random locations of the material. Materials are tested as received; the metal cladding is not removed. The samples are preconditioned for 2 hours at 105°C (221°F), and then cooled down to room temperature in a desiccator. The TMA temperature ramp should start from an initial temperature no higher than 35°C (95°F) at a scan rate of 10°C/min. After the scan reaches the specified isothermal temperature, hold at that temperature (onset) for 60 min. or until failure. The

time to delamination is determined as the time from the onset of the isotherm to failure. Failure is defined as any event or deviation of the data plot where the thickness is shown to have irreversibly changed. On occasion, some materials will delaminate before the isotherm is reached. In this case, the temperature at the time of failure is recorded. For epoxy laminates and similar materials, the recommended isothermal temperature is 260°C (500°F). For materials intended for lead-free processing and for polyimides and other high-temperature materials, increasing the isothermal temperature to 288°C (550°F) is recommended.

15.5.3 Electrical Characterization

Electrical properties include D_c and D_f, surface and volume resistivity, and dielectric strength breakdown.

15.5.3.1 Dielectric Constant (D_c) and Dissipation Factor (D_f). The dielectric constant (also known as permittivity, D_c, and ε_r) is defined as the ratio of the capacitance of a capacitor with a given dielectric (laminate) to the capacitance of the same capacitor with air as the dielectric. It is a measure of the ability of a material to store electrostatic energy and determines the relative speed that an electrical signal will travel within that material. The higher the D_c, the slower the resulting signal propagation speed will be. The signal speed is inversely proportionate to the square root of the dielectric constant. It is not an easy property to measure or to specify, because it depends not only on the material properties and the resin-to-glass ratio, but also on the test method, test signal frequency, and the conditioning of the samples before and during the test. It also tends to shift with temperature. Still, D_c values are important for computer simulations that are used to predict the

performance of impedance-controlled high-end multilayer constructions, especially when new laminate materials are considered. See Fig. 15.8 for a schematic representation of the test.

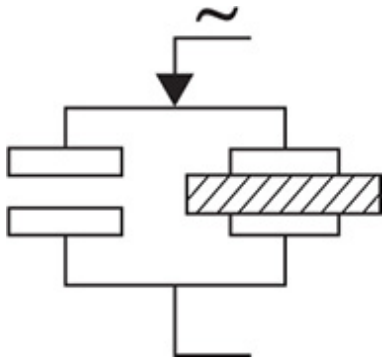


FIGURE 15.8 Dielectric constant test.

Related to the dielectric constant is the dissipation factor (D_f) or loss tangent. This is a measure of the percentage of the total transmitted power that will be lost as electrons dissipate into the laminate material. See Fig. 15.9 for a schematic representation of the test.

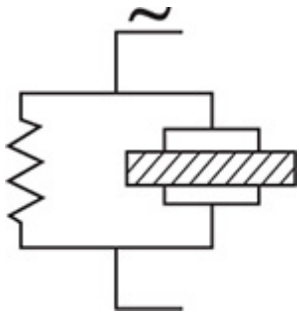


FIGURE 15.9 Dissipation factor test.

Several test methods are specified in IPC-TM-650 to determine the dielectric constant and the dissipation factor (methods 2.5.5, 2.5.5.1, and 2.5.5.2). Both methods 2.5.5 and 2.5.5.2 test laminate material with fully removed copper. At least three samples need to be tested because of the large influence of the dielectric thickness on the determined

value. Method 2.5.5.1 employs samples with an etched pattern. All of these measurements are based on the capacitance of the corresponding sample. With this capacitance and the area and thickness of the sample capacitor it is possible to calculate the dielectric constant.

The dissipation factor is determined with methods 2.5.5.1 and 2.5.5.2. In one case, the value can be read from the equipment display (Agilent Technologies Mdl 4271A); in the other, it can be calculated from the measured sample conductance and capacitance and the measuring frequency.

15.5.3.2 Surface and Volume Resistivity. Electrical resistivity of laminate materials is differentiated between specific surface resistance and volume resistance. The surface resistance s characterizes the electrical resistance between two conductors along the surface of the laminate material. The volume resistance ρ describes the electrical resistance between two layers of conducting copper along the z-axis of the laminate material. The higher the values for both of these electrical properties, the better, as this ensures proper isolation of individual copper conductors in the printed circuit board.

Both resistance values are determined according to IPC-TM-650, method 2.5.17. All resistance measurements are done with equipment capable of measuring up to 10^{12} meg-ohm while applying 500 volts direct current to the test specimen (Agilent Technologies 16008A). The sample's size is 101.6mm × 101.6mm for laminates thicker than 0.51 mm and 50.8 mm × 50.8 mm for laminates below 0.51 mm thickness. The test pattern according to method 2.5.17 should be applied to the samples using standard photo and etch processes.

All measurements are performed by applying 500 volts direct current. The voltage needs to be applied to the samples for 60 sec. before taking the resistance reading to allow the test structures to stabilize. The surface resistance

is determined between the outer ring electrode and the inner solid electrode. The volume resistance is determined between the solid front and back electrodes after changing the connecting cables appropriately. The values for volume and surface resistivity can be calculated from the measured resistance values as shown in Eqs. 15.5 and 15.6.

Volume resistivity ρ (meg-ohm-cm)

$$\rho = (R*A)/T \qquad (15.5)$$

where R = Measured resistance in meg-ohms
A = Effective area in square cm
T = Average thickness of specimen in cm

Surface resistivity σ (meg-ohms)

$$\sigma = (R*P)/D \qquad (15.6)$$

where R = Measured resistance in meg-ohms
P = Effective perimeter of electrode in cm
D = Width of test gap in cm

15.5.3.3 Dielectric Strength Breakdown. The dielectric strength of a laminate material is its ability to resist electrical breakdown. The dielectric strength defines a specific voltage that the laminate resists for a specified time whereas the dielectric breakdown voltage defines the maximum voltage at which the laminate fails. These properties can be measured perpendicular to the reinforcement (z-axis) or parallel to the reinforcement (x-y axis). The more important value is the z-axis strength because more and more thin prepreg and laminate cores are being used in high-end multilayer applications. The minimum

thickness in the laminate is defined as the shortest distance between the copper treatment peaks that needs to resist the desired test voltage. The values for dielectric strength vary with test setup, temperature, humidity, frequency, and wave shape, but are, if tested under controlled conditions, comparable between materials.

The test method following IPC-TM-650, method 2.5.6.2, describes the determination of the perpendicular electric strength of laminates. Four specimens should be tested. The sample size is recommended to be 4 in. × 4 in. with any copper cladding removed. Unless otherwise specified, the samples need to be conditioned for 48 hours in distilled water at 50°C. After that, the samples are immersed in ambient temperature distilled water for a minimum of 30 min. to allow the samples to achieve temperature equilibrium without a substantial change in moisture content. The test is performed at ambient temperature (23°C). Relative humidity is not significant as the tests are performed under oil. Samples are inserted into the high-voltage test equipment and tested to failure at a 500volts/sec. increase. The results are reported in volts/mil.

The test method (see Fig. 15.10) following IPC-TM-650, method 2.5.6, describes the determination of the parallel electric strength of laminates. Four specimens should be tested: two in machine direction, and two in the transverse direction for reinforced materials. The samples size is recommended to be 3 in. long by 2 in. wide with any copper cladding removed. Two holes 0.188 in. in diameter are to be drilled along the centerline of the 3 in. dimension and midway between the edges in the 2 in. dimension, with a spacing of 1 in. center to center. Conditioning and test setup in oil is identical. Electrodes are inserted in the holes and the samples are tested to failure at a 500 volts/sec. increase. The results are reported in kilovolts (KV).

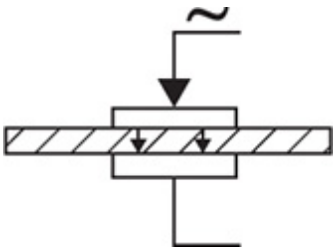


FIGURE 15.10 Dielectric strength breakdown

15.5.4 Other Laminate Properties

Other laminate properties to consider include flammability and water absorption.

15.5.4.1 Flammability. The flammability of laminate materials is classified according to Underwriters Laboratories (UL) specifications. All of the tests are performed using a standard test setup under an exhaust hood using a Bunsen burner as a source for the flame. The categories are as follows:

- *UL-94-V-0* Specimens must extinguish within 10 sec. after each flame application and within a total of less than 50 sec. after a total of 10 flame applications. No samples are to drip flaming particles or exhibit glowing combustion that lasts for more than 30 sec. after the second flame test.
- *UL-94-V-1* Specimens must extinguish within 30 sec. after each flame application and within a total of less than 250 sec. after a total of 10 flame applications. No samples are to drip flaming particles or exhibit glowing combustion that lasts for more than 60 sec. after the second flame test.
- *UL-94-V-2* Specimens must extinguish within 30 sec. after each flame application and within a total of less than 250 sec. after a total of 10 flame applications. Samples may drip flaming particles or burn briefly, but no specimen may exhibit glowing combustion that lasts for more than 60 sec. after the second flame test.

In most cases, the laminator will provide results for these tests routinely. In the case of new materials for which the laminator has not supplied any flammability data, it may be a good idea to check this property. This does not require an elaborate test setup, and you can get a first indication by igniting a sample specimen under an exhaust hood using a lighter.

15.5.4.2 Water Absorption. Depending on their specific molecular composition, every laminate material will absorb a certain amount of water. This will happen not only during the many wet processing steps in printed circuit board manufacturing but also as a result of exposure to normal environmental conditions. The absorbed moisture may change the properties of the laminate and increase the risk of blistering and delaminations during high-temperature processes such as reflow soldering.

The test method, according to IPC-TM-650, method 2.6.2.1, determines the amount of water that is absorbed by a laminate material sample when immersed in water for 24 hours. The test is easy to perform and the results for different laminates are readily comparable.

The test samples for this test need to be 2 in. long by 2 in. wide. The thickness is not specified but should not vary widely when more than one material is characterized. The edges of the samples need to be sanded smooth and copper cladding is to be removed using standard etching processes. The samples are preconditioned in a drying oven for 1 hour at 105°C (221°F), cooled down to room temperature in a desiccator, and weighed immediately after removal. Then the samples are placed in distilled water at 23°C. It is important to place the samples on their edge to maximize the laminate area exposed to water. After 24 hours, the samples are removed, dried with a dry cloth, and immediately weighed. The moisture absorption is reported in percent weight increase.

15.5.5 Additional Tests

In addition to the previously described test methods, many more can be found in IPC-4101 and in the test methods manual IPC-TM-650. All of these tests address laminate properties that may have a significant impact on the performance of the final product. The final decision as to which qualification tests to include or exclude always needs to be made on a case-by-case basis depending on the performance requirements for the printed circuit board.

At the same time, there are a number of laminate qualification tests that rarely will be performed in the printed circuit manufacturing facility. In many cases, the laminate supplier will perform a number of qualification tests itself and share the results with its customers. This may in many cases be sufficient, especially after a close relationship between the supplier and the PCB manufacturer has been established.

15.5.6 Prepreg Testing

During the qualification of a new laminate material, it may also become necessary to perform prepreg-specific tests to verify its quality. The most commonly tested properties of prepregs are resin content, flow during mutilayer processing, and gel time. Details about additional properties and all corresponding test methods can be found in IPC-4101.

15.6 CHARACTERIZATION TEST PLAN

Table 15.4 summarizes all of the test procedures.

TABLE 12.4 Laminate Characterization Test Plan

1. Step	Data comparison	Unit	Test result
	Material available in production volume	yes/no	
	Material cost	$/m^2	
	Material data sheet available	yes/no	

2. Step	First test runs in small volume	Unit	Test method	Conditioning	Data sheet	Test result
	Surface and appearance		IPC-TM-650, method 2.1.2 & 2.1.5	As received		
	Copper peel strength laminate Condition A	N/mm	IPC-TM-650, method 2.4.8	As received		
	Copper peel strength laminate Condition B	N/mm	IPC-TM-650, method 2.4.8	Solder pot 288°C/10s		
	Solder shock laminate 288°C/10s	Pass/fail	IPC-TM-650, method 2.4.23	As received		
	Solder shock laminate 288°C/60s	Pass/fail	IPC-TM-650, method 2.4.23	As received		
	Glass transition temperature (DSC, TMA, or DMA)	°C	IPC-TM-650, as applicable	As received		
	Decomposition temperature (T_d)	°C	IPC-TM-650, method 2.3.40	As received		
	Z-axis expansion laminate TMA	ppm/°C	IPC-TM-650, method 2.4.24	As received		

3. Step	Material characterization	Unit	Test method	Conditioning	Data sheet	Test result
	Dielectric constant (1 MHz)	–	IPC-TM-650, method 2.5.5.2	24h/23°C/50%		
	Dielectric constant (1 MHz)	–	IPC-TM-650, method 2.5.5.2	96h/35°C/90%		
	Dissipation factor (1 MHz)	–	IPC-TM-650, method 2.5.5.2	24h/23°C/50%		
	Dissipation factor (1 MHz)	–	IPC-TM-650, method 2.5.5.2	96h/35°C/90%		
	Surface resistance	MW	IPC-TM-650, method 2.5.17	24h/23°C/50%		
	Surface resistance	MW	IPC-TM-650, method 2.5.17	96h/35°C/90%		
	Volume resistance	MW cm	IPC-TM-650, method 2.5.17	24h/23°C/50%		
	Volume resistance	MW cm	IPC-TM-650, method 2.5.17	96h/35°C/90%		
	Dielectric withstanding voltage	V/mil	IPC-TM-650, method 2.5.6	48h in 50°C H_2O		
	Glass transition temperature (DSC)	°C	IPC-TM-650, method 2.4.25C			
	Glass transition temperature (TMA)	°C	IPC-TM-650, method 2.4.24C			
	Glass transition temperature (DMA)	°C	IPC-TM-650, method 2.4.24.2			
	Decomposition temperature T_d	°C	IPC-TM-650, method 2.3.40	As received		
	CTE x,y (α_1)	ppm/K	IPC-TM-650, method 2.4.41.2			
	CTE x,y (α_2)	ppm/K	IPC-TM-650, method 2.4.41.2			
	CTE z (α_1)	ppm/K	IPC-TM-650, method 2.4.24			
	CTE z (α_2)	ppm/K	IPC-TM-650, method 2.4.24			
	Water absorption	%	IPC-TM-650, method 2.6.2.1			
	Flammability		UL-94			

15.7 MANUFACTURABILITY IN THE SHOP

During the qualification of a new material, it is also crucial to run the laminate through the production processes to check whether they are compatible. Table 15.5 summarizes all the steps that are necessary to control.

TABLE 15.5 Summary of Production Steps

Compatibility with innerlayer (IL) process steps
Preclean
Resist lamination
Exposure
Develop, Etch, Strip
Punching
IL-Automatic optical inspection
IL-Repair/outerlayer (OL)-repair
Blackoxide/oxide alternatives
Compatibility with multilayer process steps
IL drying
Lay up
Press cycle
Edge routing
Dimensional stability check
Compatibility with process steps from drill to electroless copper
Drilling
Brush/Pumice/Deburr
Desmear/Plasma Desmear/Other
E’less copper or similar process

Compatibility with soldermask process step

Compatibility with different finish metallization processes

Electroless Ni/Au
Immersion Sn
Immersion Ag

Compatibility with routing process

The first process step is innerlayer processing. Here, a change in stiffness of the new laminate material can have a significant impact on the processability in horizontal manufacturing lines. This is especially important for thin cores. A change in the copper quality of the new laminate may impact the adhesion of the innerlayer photoresist and can also affect the copper etch rates. During automatic optical inspection (AOI), it is necessary to verify the contrast between copper circuitry and laminate and adjust the AOI settings if necessary. In case of necessary innerlayer repairs, the settings for the welding process may need adjustment to avoid thermal damage of the laminate and ensure reliable interconnects. The last step during innnerlayer processing is copper blackoxide. Here, it is necessary to verify the compatibility of the employed blackoxide (reduced/nonreduced or alternative) to the base material to obtain a sufficient innerlayer bond strength of the multilayer product. The dimensional stability of the innerlayers must be measured after the multilayer cycle to adjust the innerlayer scaling factors of the new material.

The next step after multilayer lamination and edge routing is drilling. A change in the thermomechanical properties of the laminate may impact the quality of the drilled holes, and adjustments to drill speeds or desmear settings may be necessary. After metallization and plating, the adhesion of the copper in the plated through hole as well as reliable contacts to all innerlayers must be verified.

The adhesion of soldermask may also change as well when a new material is introduced. This is especially critical in combination with any metal finish process steps (such as electroless Ni/immersion Au, immersion Sn, and immersion Ag). In addition to having a negative impact on soldermask adhesion, these processes in combination with new laminates can also lead to nonselective metal plating or skip plating. One of the last manufacturing steps that should be evaluated during the introduction of a new laminate material is board routing and scoring. Here the use of a new base material with changed stiffness or different reinforcement may lead to necessary process adjustments.

[a] Available at http://www.ipc.org/html/testmethods.htm.

[b] Available at http://www.astm.org.

[c] Available at http://www.nema.org.

PART 4

ENGINEERING AND DESIGN

CHAPTER 16

PLANNING FOR DESIGN, FABRICATION, AND ASSEMBLY

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

16.1 INTRODUCTION

Advances in interconnection technologies have occurred in response to the evolution of component packages, electronic technology, and increasingly complex functions. Therefore, it comes as no surprise that various forms of printed wiring remain the most popular and cost-effective method of interconnections.

Manufacturing, assembly, and test technologies have responded by improvements in their technologies. These increased capabilities have made selection of technologies, design rules, and features so complex that a new function has developed to allow for the prediction and selection of design parameters and performance versus manufacturing costs. This is the planning for design, fabrication, and assembly. This activity has also been called *design for*

manufacturing and assembly or sometimes-*predictive engineering*. It is essentially the selection of design features and options that promote cost-competitive manufacturing, assembly, and test practices. Later in this chapter, we will offer a process to define producibility unique to each design or manufacturing process. Section 16.3.4 describes a process to define producibility unique to each design.

The purpose of this chapter is to provide information, concepts, and processes that lead to a thoughtfully and competitively designed printed circuit, ensuring that all pertinent design and layout variables have been considered.

16.1.1 Design Planning and Predicting Cost

Reducing costs to remain competitive is a principle responsibility of product planning. On the average, 75 percent of the recurring manufacturing costs are determined by the design drawing and specifications.[1] This was one of the conclusions found by an extensive study that General Electric conducted on how competitive products were developed. Manufacturing typically determines production setup, material management, and process management costs (see Fig. 16.1), which are a minor part of the overall product cost.

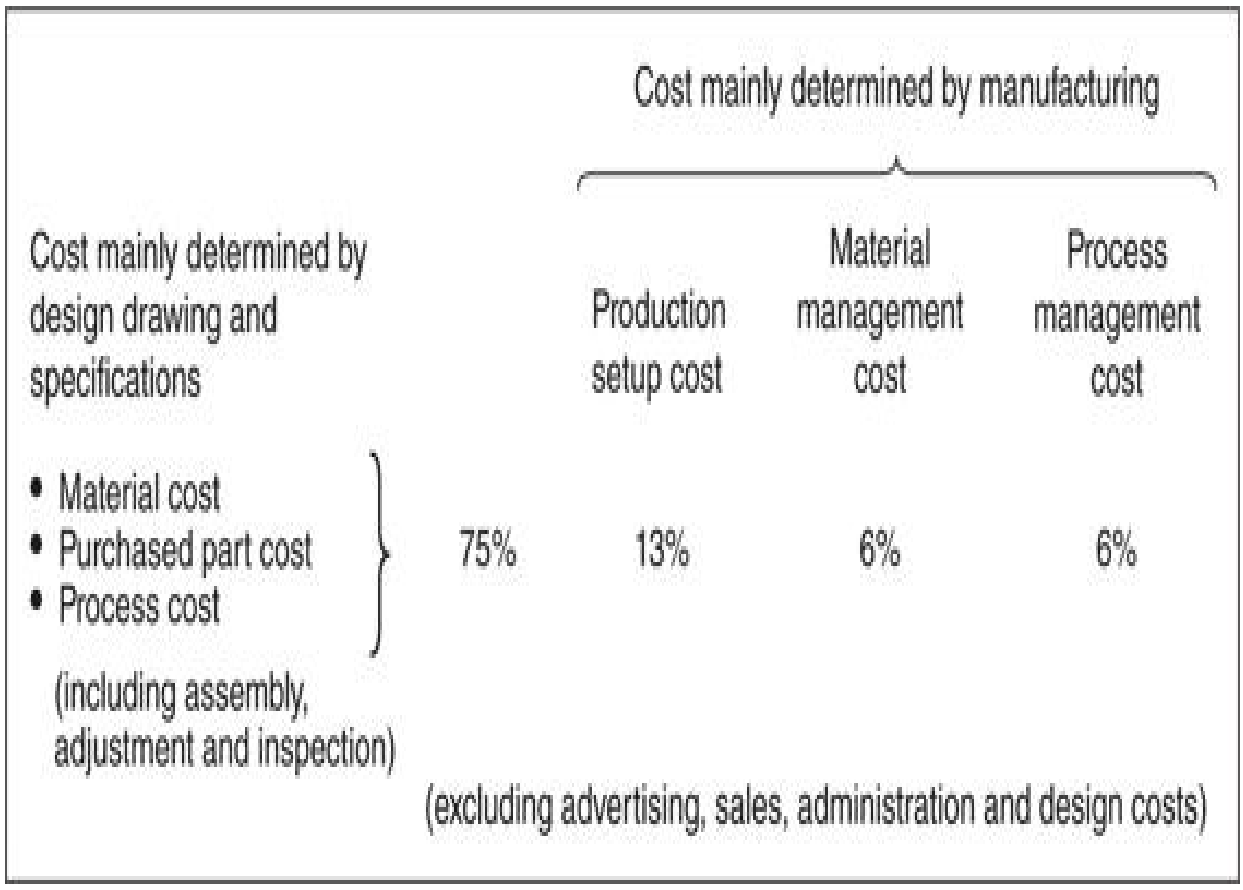


FIGURE 16.1 Design determines the majority of the cost of a product.

Time to market along with competitive prices can determine a product's ultimate success. Having the first of a new electronic product on the market has many advantages. By planning the printed wiring board (PWB) layout and taking into consideration aspects and costs of PWB fabrication and assembly, the entire process of design and prototyping can be done with minimum redesign (or respins).

16.1.2 Design Planning and Manufacturing Planning

Electronics is one of the biggest enterprises globally. It is common for design to be done in one hemisphere and manufacturing in another. It is also common for

manufacturing to be done in a number of different places simultaneously. An integrated approach must be adopted when the intention is to rationalize fabrication and assembly as part of the entire production system and not as individual entities, as shown in Fig. 16.2. This dispersed manufacturing must be taken into consideration during the design planning and layout process. No finished product is ever better than the original design or the materials from which it is made.

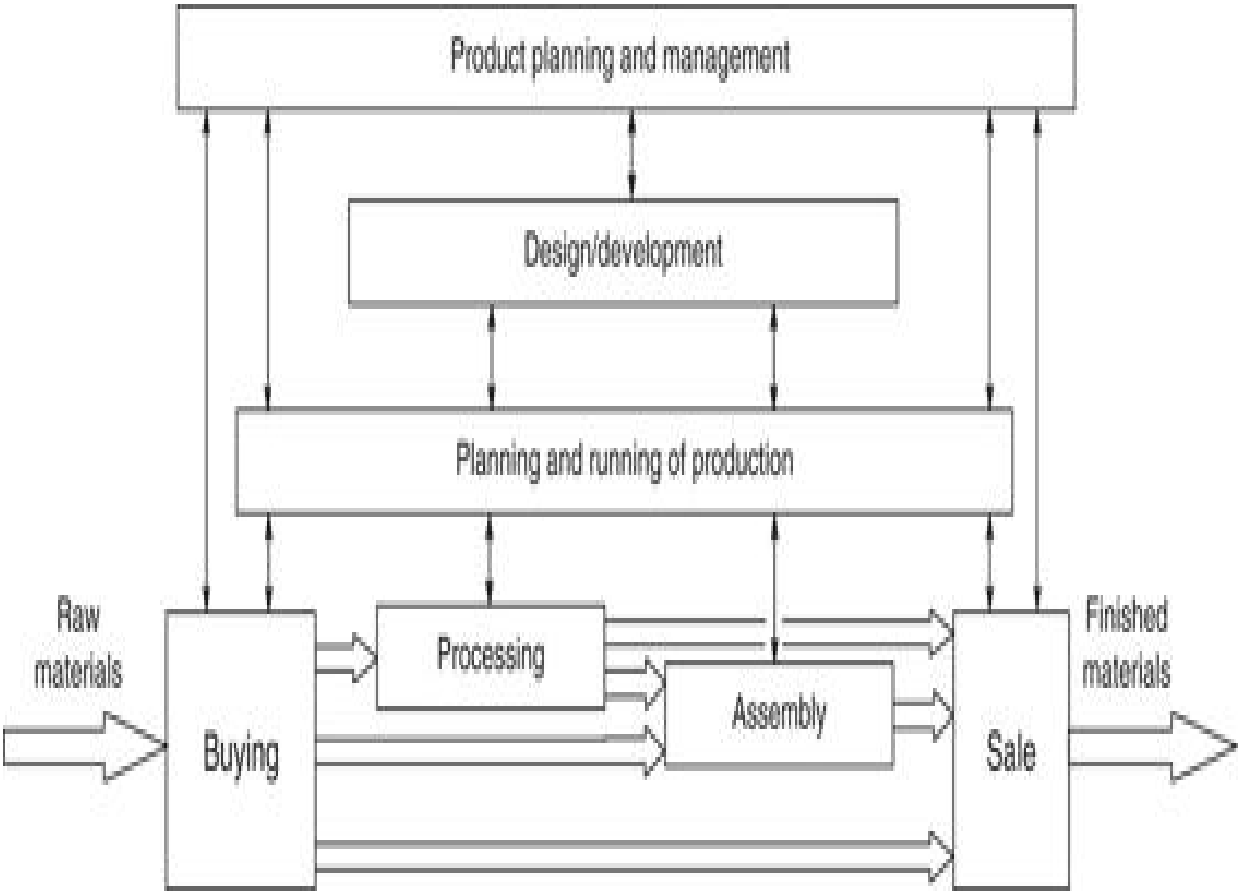


FIGURE 16.2 Fabrication and assembly rationalized by planning and design.

16.2 GENERAL CONSIDERATIONS

The planning process central focus will be the trade-offs between the loss and gain in performance for layout,

fabrication, assembly, and test versus the costs in these domains. Therefore, some major considerations will be discussed in the following sections:

- New product design process (Secs. 16.3.1 and 16.3.2)
- The role of metrics (Secs. 16.3.3 and 16.3.4)
- Layout trade-off planning (Sec. 16.5)
- PWB fabrication trade-off planning (Sec. 16.6)
- Assembly trade-off planning (Sec. 16.7)

16.2.1 Planning Concepts

Planning for design, fabrication, and assembly (PDFA) is a methodology that addresses all the factors that can impact production and customer satisfaction. Early in the design process, the central idea of PDFA is to make design decisions to optimize particular domains, such as producibility, assemblability, and testability, as well as to fit into a product family, such as custom automated manufacturing. Planning takes place continuously in the electronic design environment (see Fig. 16.3). The data and specifications flow in one direction, from product concept to manufacturing. During the design process, 60 percent of the manufacturing costs are determined in the first stages of design when only 35 percent of the design engineering costs have been expended. The typical response is shown in Fig. 16.4.[1]

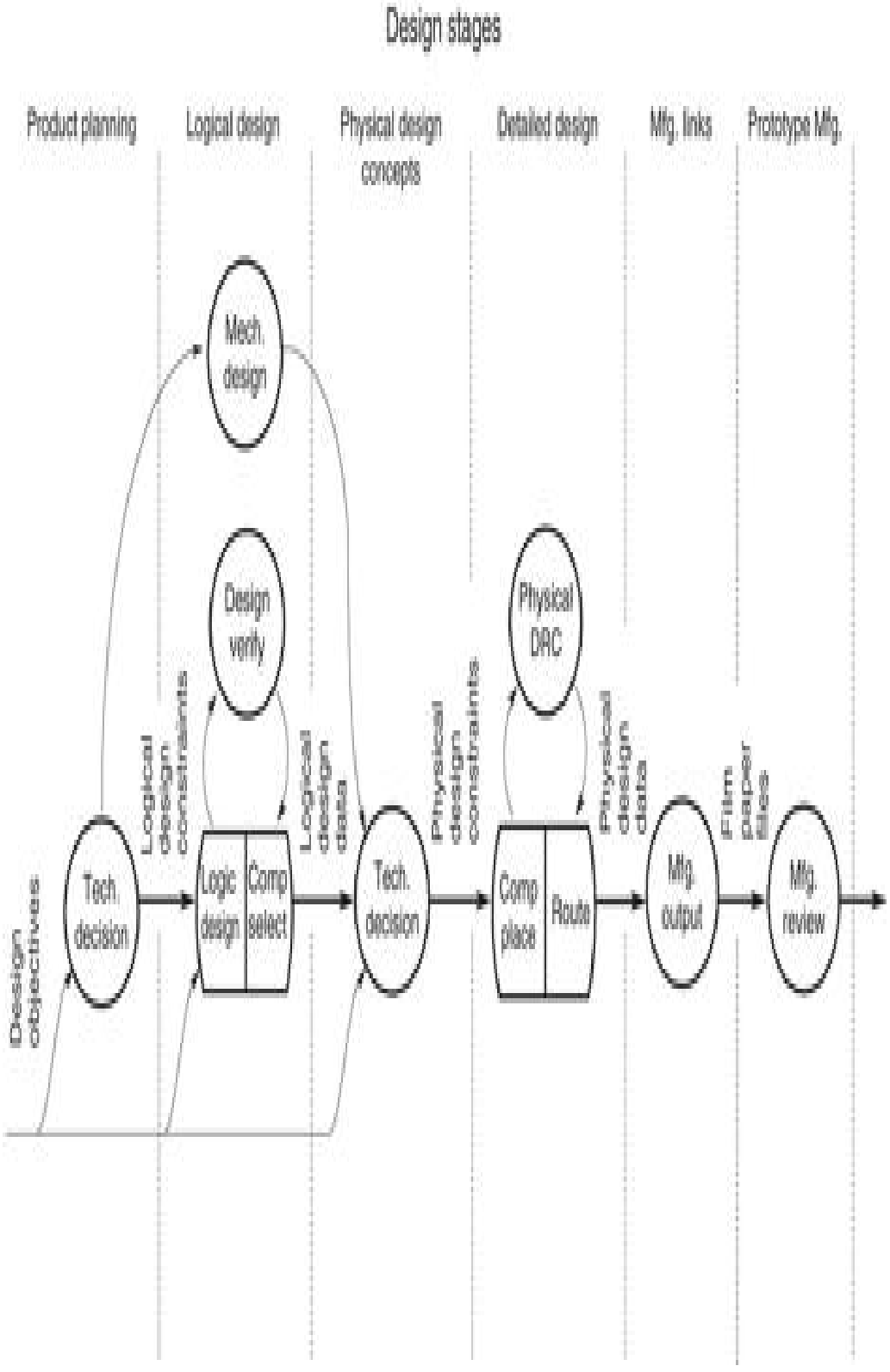

Design stages
Product planning
Logical design
Physical design concepts
Detailed design
Mfg. links
Prototype Mfg.
Mech. design
Design verify
Physical DRC
Design objectives
Tech. decision
Logical design constraints
Logic design
Comp select
Logical design data
Tech. decision
Physical design constraints
Comp place
Route
Physical design data
Mfg. output
Film, paper, files
Mfg. review

FIGURE 16.3 Electronic design environment.

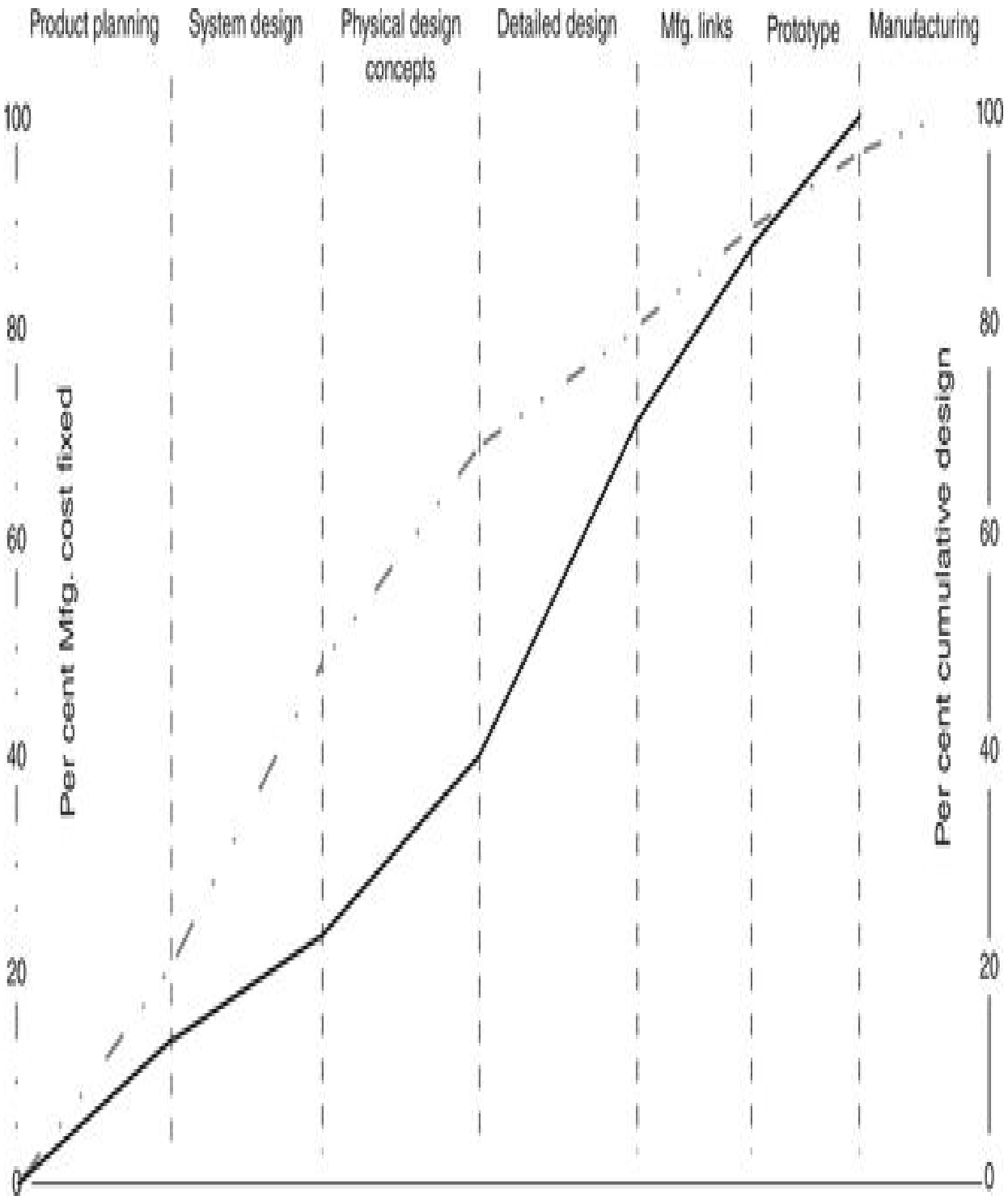


FIGURE 16.4 Design cost accumulation versus intrinsic manufacturing costs.

16.2.2 Producibility

Producibility is now regarded as an intrinsic characteristic of a modern design. Like the concept of quality in manufacturing, such a characteristic must be built in, not inspected in. Producibility must be designed in; it cannot be a “checkpoint” in the design process or inspected in by tooling.

16.3 NEW PRODUCT DESIGN

The keys to superior producibility in new product design can be found in the expanded design process. One of those keys is the role of metrics or data-based analysis of planning trade-offs.

16.3.1 Expanded Design Process

The new expanded design process that incorporates planning, trade-offs, and manufacturing audits is shown in Table 16.1. The process is made up of 12 separate functions that incorporate the planning and trade-offs sections in this book:

TABLE 16.1 The Expanded Electronics Design Process

Function	Purpose
Specification	User-supplied constraints and ideas formulate executable specifications.
Capture of system description	Technology trade-off analysis: balance of loss and gain in various domains' performance versus cost.
Synthesis	Generation of a netlist from the executable specifications.
Trade-off	Selection of layout, fabrication, and assembly features versus cost.
Physical CAD	Conversion of netlists to system and module layouts.
Simulation	Detailed analysis of design structures to support all other design (CAD) activities.
Design advisor	Continuous display of design rated by performance rules.
Manufacturability audit	Check of design to manufacturing design rules and capabilities.
Tooling	Conversion of module layouts to panel layout.
MFG	Conversion of module layouts to physical products (fabrication or assembly).
PDM database	Enterprise wide database containing all product information (product data management, or PDM) including design files, libraries, manufacturing information and revisions, etc.
Internet	Multiteam designs via access over the Internet.

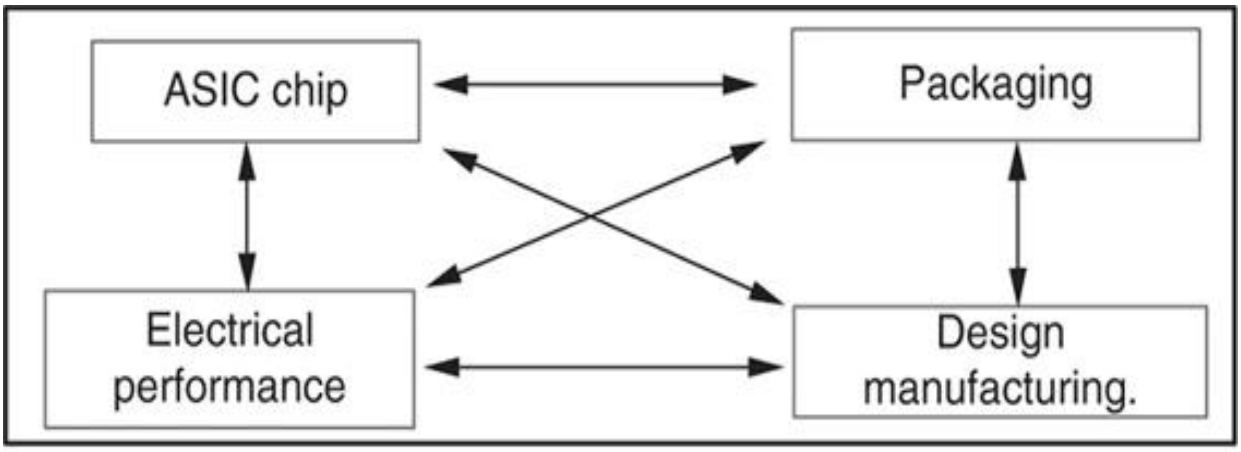
This differs from the more conventional design process (as seen in Fig. 16.3) by the inclusion of four important functions:

- The formal technology trade-off analysis during the specification phase
- Detailed trade-off selection of features for layout, fabrication, and assembly
- Design advice during component placement and routing

- Manufacturing audits to review the finished layout for producibility, time to market, and competitiveness

16.3.2 Product Definition

The initial new product design stage is specification and product definition. This key step takes ideas, user requirements, opportunities, and technologies and formulates the executable specifications of a new product. During this operation, the ability of technologists who may lack any manufacturing experience to predict what will happen in manufacturing can affect both time to market and ultimate product costs. Figure 16.5 shows the technology trade-off analysis that requires the balance of loss and gain in various domains performance versus costs. Size and partitioning for integrated circuits (IC) and application-specific integrated circuit (ASIC) must be balanced with overall packaging costs and the resultant electrical performance. All of these factors affect the manufacturing and product cost.



Technology tradeoff analysis: balance of loss and gain in various domains' performance versus cost.

FIGURE 16.5 Specifications determine product partitioning and producibility.

Another definition of this process could be called a "verified design."[2] A verified design is one that was predicted from models or measures that have been correlated to past designs. This is in contrast to the traditional approach, which is a "nonverified design," or trial and error. This is diagrammed in Fig. 16.6. The advantage of the verified design can be a significant reduction in redesigns to achieve the original product objectives.

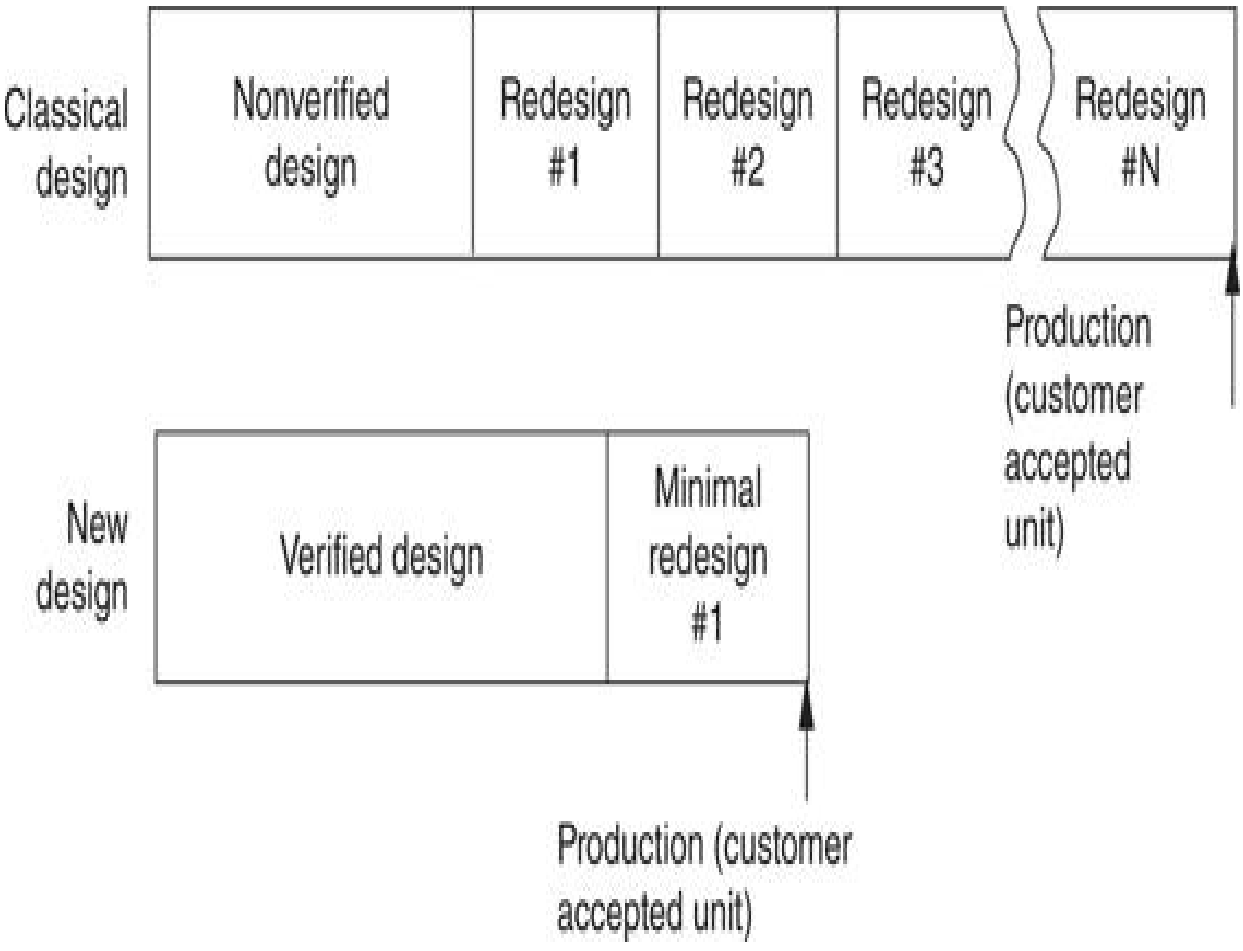


FIGURE 16.6 A design incorporating trade-offs versus traditional design.

16.4 SPECIFICATION: CAPTURE OF SYSTEM DESCRIPTION

16.4.1 Metrics for Predicting and Planning Producibility

Metrics are data and statistically backed measures, such as wiring demand (Wd) (see Sec. 16.5.1). These measures can be density, connectivity, or, in this context, producibility. These measures are the basis for predicting and planning. When such measures are used in the design process, two categories are applied to a product. Only the metrics can be shared by all in the design team. The nonmetrics provide little assistance in design.

16.4.1.1 Metrics

16.4.1.1.1 Metrics. Both the product and the process are measured by physical data using statistical process control (SPC) and total quality management (TQM) techniques (predictive engineering process).

16.4.1.1.2 Figure of Merit. Both the product and the process are scored by linear equations developed by consensus expert opinion (expert opinion process).

16.4.1.2 Nonmetrics

16.4.1.2.1 Opinion. Opinion, albeit from an expert, is applied after or concurrent with design (manufacturing engineering inspection process).

16.4.1.2.2 No Opinions. No attempt to inspect or improve the design is done during the specification, partitioning, or design stage (over the wall process).

Metrics also establish a common language that links manufacturing to design. The producibility scores form a nonopinionated basis allowing a team approach that results in a quality, cost-competitive product (Fig. 16.7).

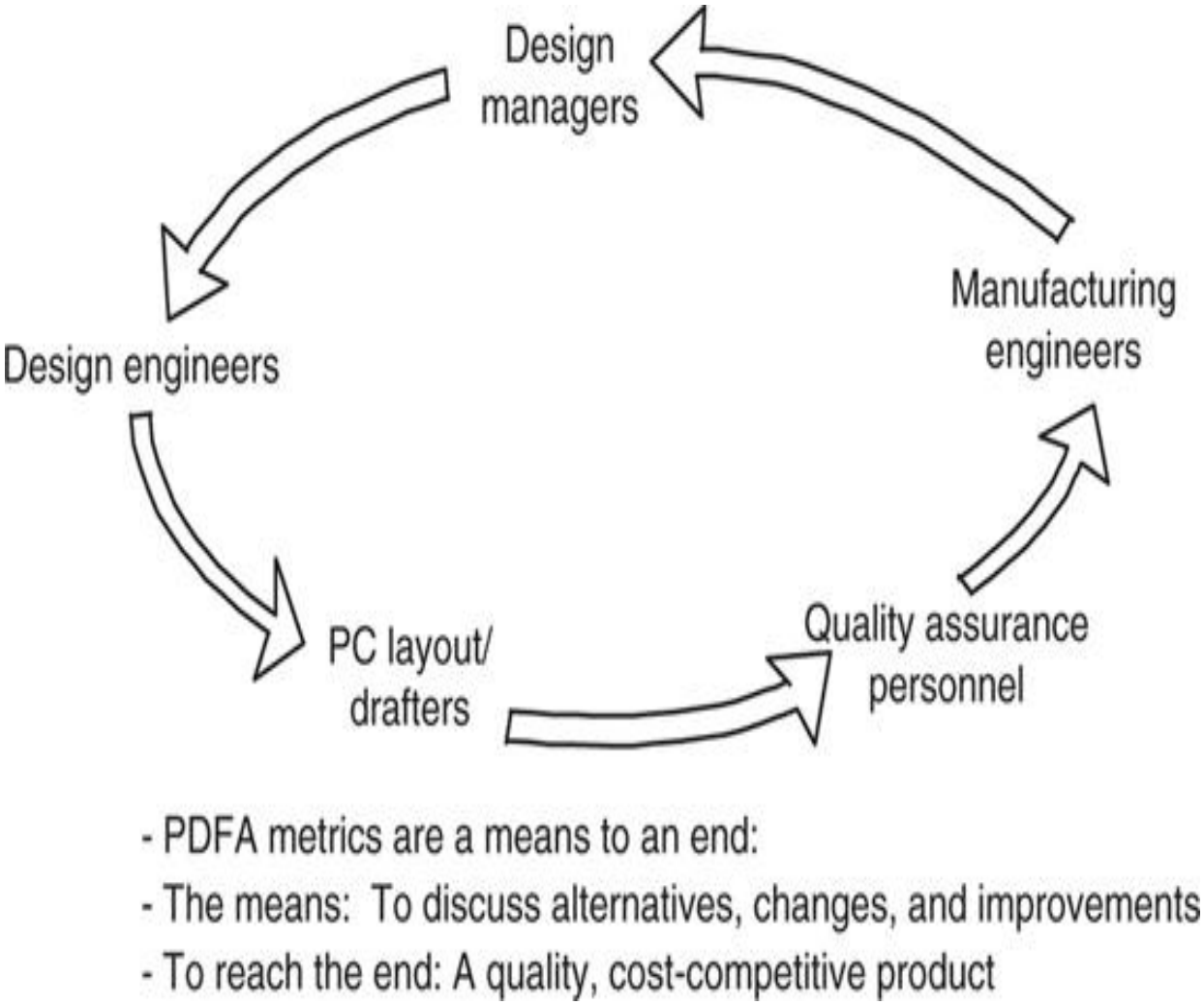


FIGURE 16.7 The benefits of metrics as a common design language.

The strategy in applying these measures is shown in Fig. 16.8. The analysis process is unique to every individual and company, but certain conditions have to be met and considered if the product is going to be successful. If the score meets producibility requirements, then select this approach; if not, then evaluate other opportunities and repeat the process. In the rest of this chapter, measures and metrics are introduced that provide insight for layout, fabrication, and assembly planning.

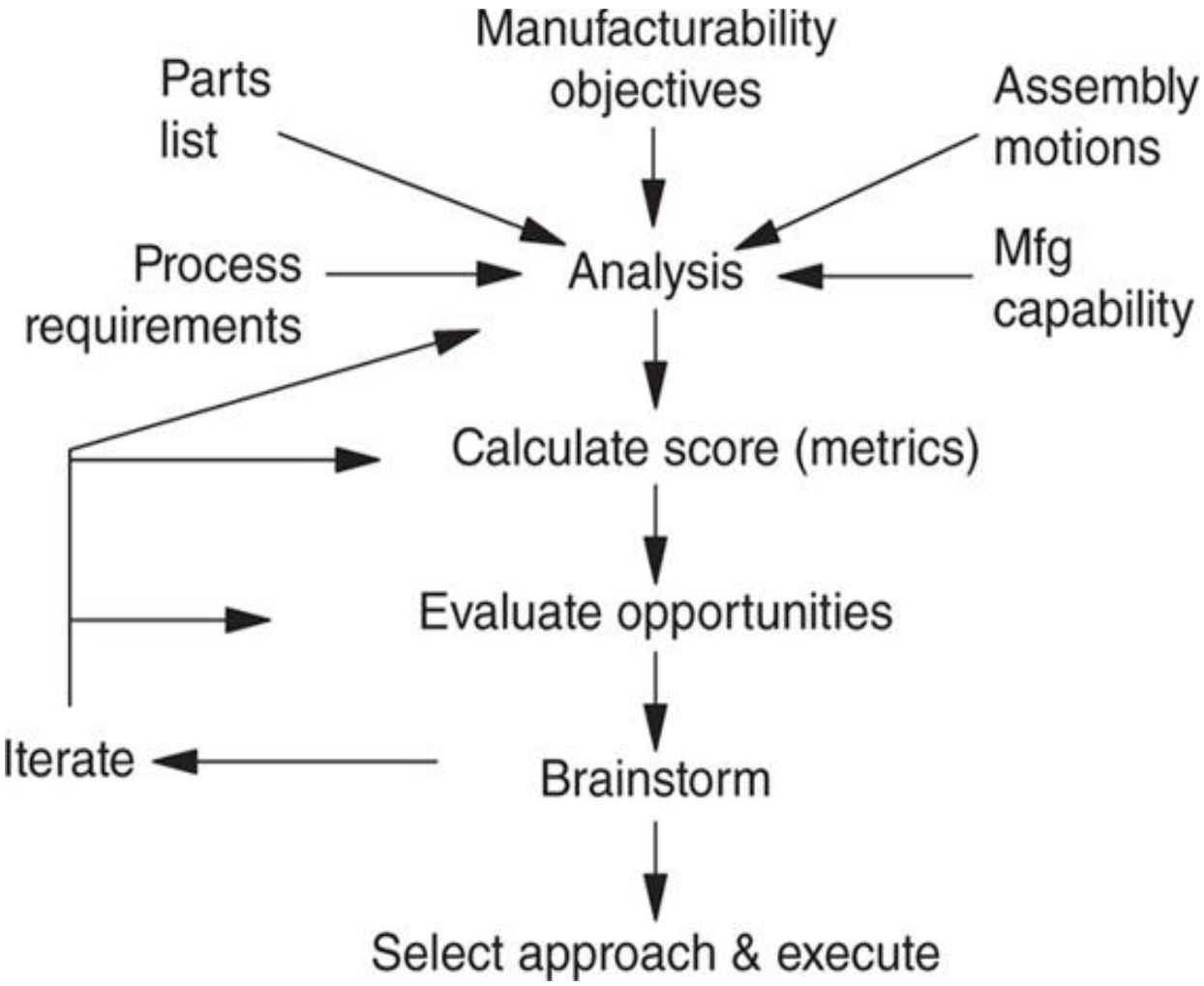


FIGURE 16.8 A process using measures and metrics to obtain a producible product.

16.4.2 Nonmetrics

It is always preferable to have metrics when discussing producibility. But if metrics are not available, then the opinions of experts are better than no opinions at all. The problem with opinions is that they are difficult to defend and explain, and when used in relation to producibility, many times they vary with each person. Sometimes, the opinion process is implemented with good intentions, by having experienced production experts review a new design. This is the *expert opinion process* and although it is sometimes

successful, it is difficult to replicate and often results in building barriers between manufacturing and design. That is why the figure of merit process is so popular. For a small amount of work by experts, it produces a scoring procedure that can be used and understood by all.

16.4.3 Figure of Merit Metric

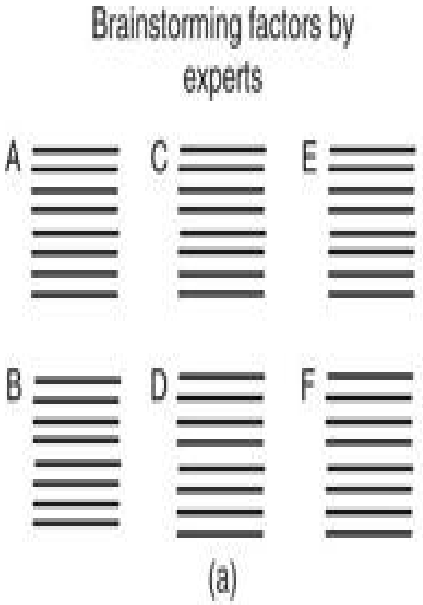
Metrics are the preferred measures for design planning, but their availability for predicting producibility is often limited. Metrics also can take many months to develop and the amount of experimentation may make them costly. The measure that is much more cost-effective and quicker to develop is the figure of merit. The figure of merit (FOM) is the result of one or two days of work by a group of design and manufacturing experts. The process consists of eight steps:

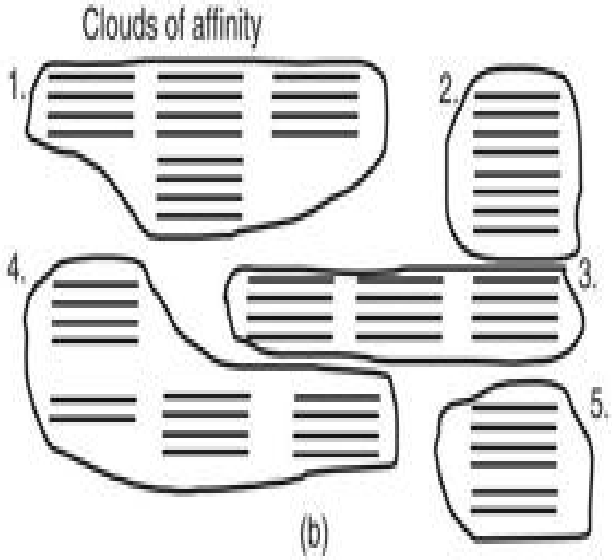
1. Define or identify the new measure to be developed.
2. Determine why the measure was selected. Ensure the relevance of the measure to communication.
3. Survey the customers. Identify what the measure is that customers need to have communicated.
4. Identify needs and expectations and collect data.
5. Brainstorm contributing factors and variables.
6. Determine the major contributors and normalize scores. Use multivote, paired-ranking, ranking voting, or Pareto techniques to verify data if available. These are the coefficients (Cx) of the equation.
7. Construct FOM factor weightings (FWx). Fill in FOM table values for 1, 25, 50, 75, and 100.
8. Construct a linear equation model (coefficient score × FOM weightings).

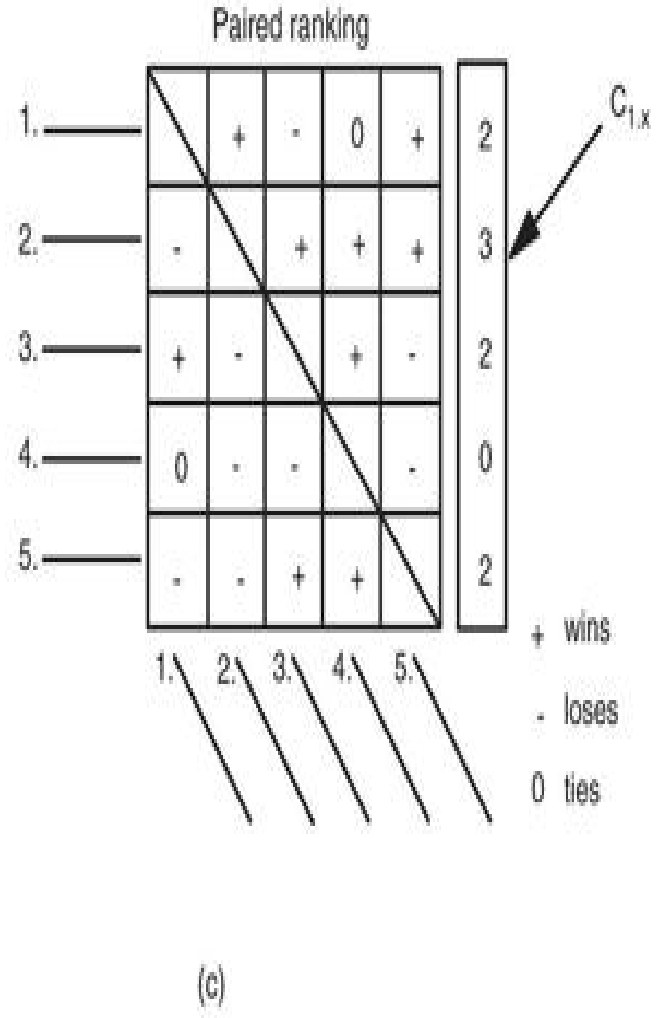
16.4.4 Figure of Merit Linear Equation

This FOM procedure uses classical TQM techniques to brainstorm, rank, and formulate an equation that will score producibility, assemblability, or any other measure that can be used in design planning. The two factors used in the producibility score are made up of the (1) the coefficient, Cx, and (2) the factor weighting, FWx.

16.4.4.1 Coefficient, Cx. The coefficients in the producibility score are the result of brain-storming all the possible contributors to producibility that can affect the product (Fig. 16.9*a*). These are grouped into common ideas or factors by such techniques as clouds of affinity or Kay-Jay (Fig. 16.9*b*). These factors are ranked by voting or other Pareto techniques such as paired ranking, as seen in Fig 16.9*c*. Whatever the method of voting, the values are normalized by dividing by the smallest nonzero value. The resulting voting scores form the coefficients, Cx. Those factors with no votes are zeros and drop out of consideration.


Brainstorming factors by experts
A
C
E
B
D
F
(a)


Clouds of affinity
1.
2.
3.
4.
5.
(b)


Paired ranking
1.
2.
3.
4.
5.
+ - 0 +
- + + +
+ - + -
0 - - -
- - + +
2
3
2
0
2
$C_{1,x}$
1. 2. 3. 4. 5.
+ wins
- loses
0 ties
(c)

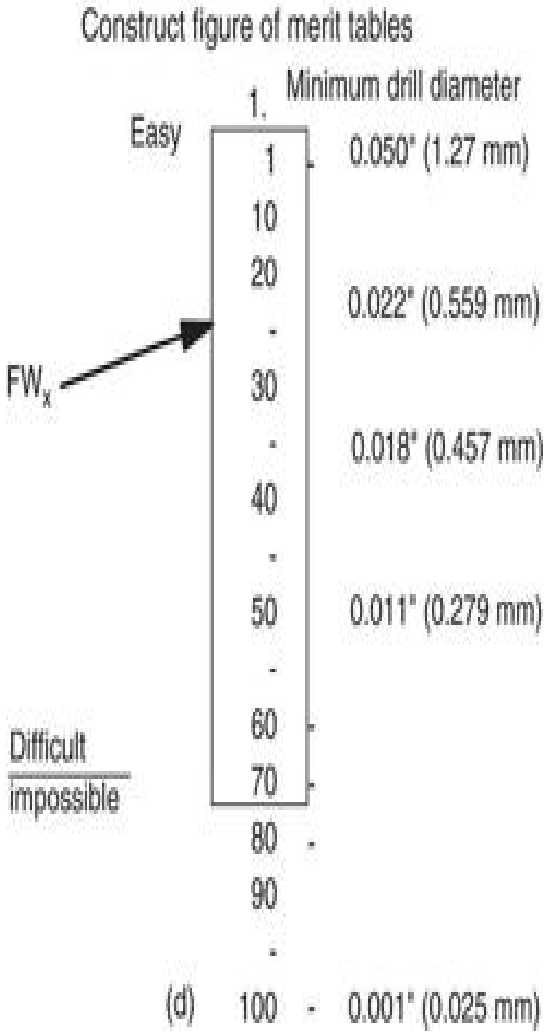

Construct figure of merit tables
Minimum drill diameter
1.
Easy
1
10
20
30
40
50
60
70
80
90
100
0.050" (1.27 mm)
0.022" (0.559 mm)
0.018" (0.457 mm)
0.011" (0.279 mm)
0.001" (0.025 mm)
FW_x
Difficult
impossible
(d)

FIGURE 16.9 Elements of the figure of merit process: (*a*) brainstorming factors; (*b*) grouping similar ideas; (*c*) ranking factors; and (*d*) assigning values to factors.

16.4.4.2 Factor Weightings, FWx. Each factor that emerges from the ranking process is calibrated by assigning values from one (1) to one hundred (100), as seen in Fig. 16.9*d*. The 1 factors are easy to manufacture, and the 100 factors are impossible today but may only be very difficult in a few years.

The resulting scoring equation will look like and be used as shown in Eq. (16.1).

$$\text{SCORE} = (\text{C1})(\text{FW1}) + (\text{C2})(\text{FW2}) + (\text{C3})(\text{FW3}) + (\text{Cn})(\text{FWn}) + \cdots \tag{16.1}$$

where Cx = coefficients based on ranking
FWx = factor weightings of assigned values (1 – 100)

For example, assume that the producibility of a bare PWB may be scored with the preceding equation if the FOM process established the following factors:

- Size of the substrate: C1 = 1.5
- Number of drilled holes: C2 = 3.0
- Minimum trace width: C3 = 4.0

Now assume that the proposed PWB design specifies the following:

- Size of the substrate: FW1 = 36
- Number of drilled holes: FW2 = 18
- Minimum trace width: FW3 = 31

The producibility SCORE would equal:

$$232 = 54 + 54 + 124 = 1.5 \times 36 + 3.0 \times 18 + 4.0 \times 31$$

The SCORE can be used if it is calibrated based on the prior history of this type of product. Prior products are scored with the FOM linear equation [Eq. (16.1)]. Those products that went into production smoothly and presented minimum problems determine the minimum SCORE that should be sought. The SCORE from products that were a problem, had to be reengineered, or presented delays in introduction determines the SCORE that the design should exceed if problems occur and producibility is to be obtained.

16.5 LAYOUT TRADE-OFF PLANNING

Predicting density and selecting design rules are two of the primary planning activities for layout. The actual layout of a PWB is covered in Chaps. 17, 18, and 21. The selection of design rules not only affects circuit routing but profoundly affects fabrication, assembly, and testing.

16.5.1 Balancing the Density Equation

With the need for more parts on an assembly and the trend to make things smaller for portability or faster speeds, the design process is a challenging one. The process is one of balancing the density equation with considerations for certain boundary conditions such as electrical and thermal performance. Unfortunately, many designers do not realize that there is a mathematical process to determine the routing rules of a printed circuit. Let me briefly explain. The density equation, as seen in Eq. (16.2) and Fig. 16.10, has two parts: the left side, which is the component wiring demand, and the right side, which is the substrate wiring capability.

Component PWB Wiring Demand < PWBs Design Rules & Construction Wiring Capabilities (16.2)

where PWB wiring demand = total connection length required to connect all the parts in a circuit

PWB wiring capability = substrate wiring length available to connect all the components

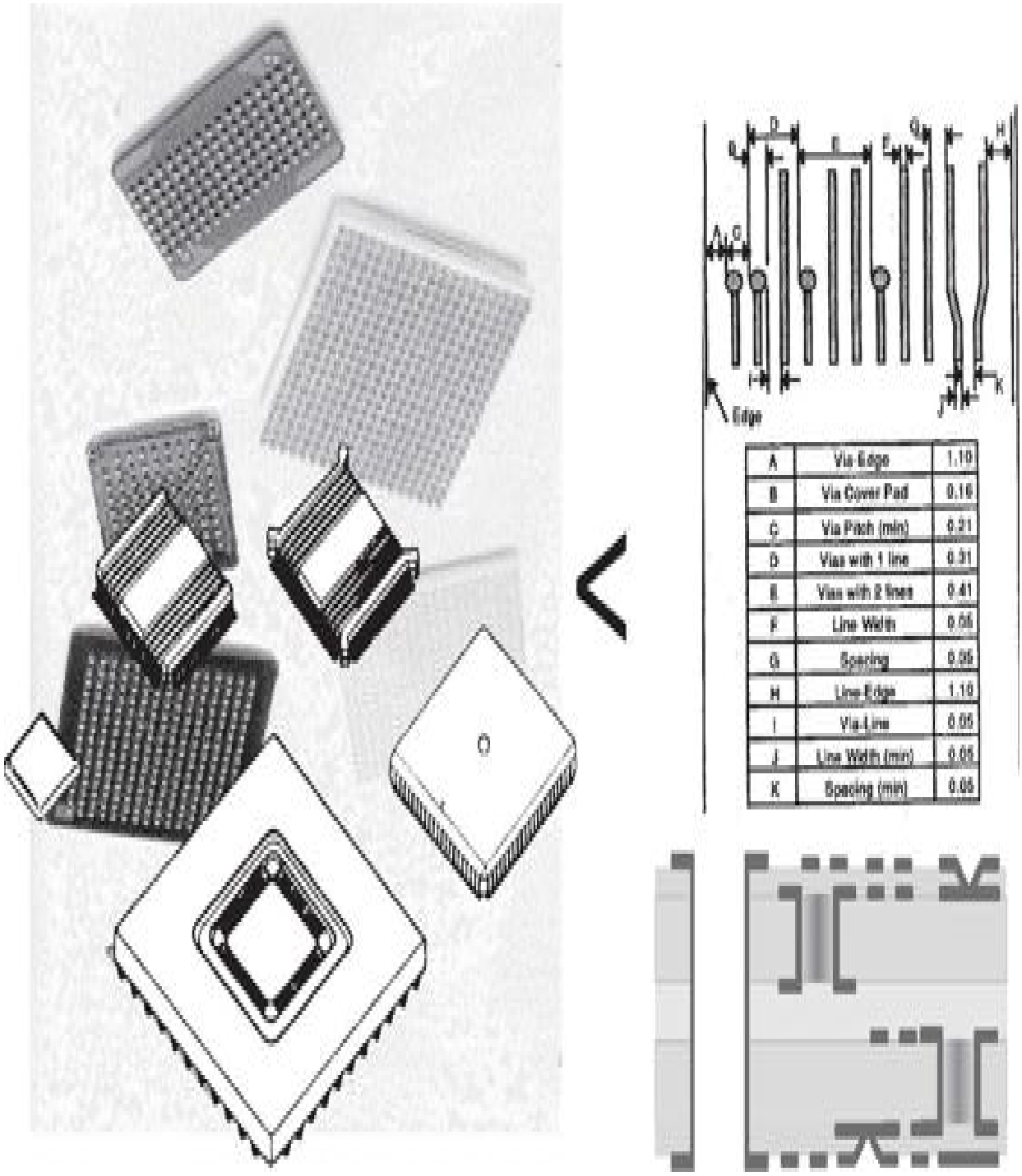


FIGURE 16.10 Balancing the density equations to achieve an optimal layout.

Four conditions can exist between wiring demand and substrate capability:

- *Wiring demand > substrate capability*. If the substrate capacity is not equal to the demand, the design can never be finished. There is not enough room for either traces or vias. To correct this, either the substrate has to be bigger or components have to be removed.
- *Wiring demand = substrate capability*. Although theoretically optimum, this condition leaves no room for variability and it would take an unacceptable amount of time to complete the design.
- *Wiring demand < substrate capability*. This condition should be your goal. There should be enough extra capacity to complete the design on time with only a minimum of over specification and costs.
- *Wiring demand << substrate capability*. This is the condition that usually prevails. By PCB layout, the schedule is tight and timing is all important. Many choose tighter traces or extra layers to help shorten the layout time. This increases the manufacturing costs 15 to 50 percent higher than is necessary, which is sometimes called the sandbag approach. It is unfortunate, as the preceding models would help to create a better-planned environment.

16.5.2 Wiring Demand (W_d)

Wiring demand is the total connection length (in inches) required to connect all the parts in a circuit. If the design specifies an assembly size (in square inches), then a wiring density in inches per square inch or centimeter per square centimeter is created. Models early in the design planning process can estimate the wiring demand. Three cases can control the maximum wiring demand:

- The wiring required to break out from a component such as a flip chip or chip scale package

- The wiring created by two or more components tightly linked, such as a central processing unit (CPU) and its cache or a digital signal processor (DSP) and its input/output (I/O) control
- The wiring demanded by all integrated circuits and discretes collectively

Models are available to calculate the component wiring demand for all three cases; see Sec. 16.5.3. Since it is not always easy to know which case controls a particular design, it is usually to calculate all three cases to see which one is the most demanding and thus controls the layout.

Wiring demand is defined by Eq. (16.3).

$$W_d = W_c \times \varepsilon \text{ (in cm/square cm or in./square in.)} \qquad (16.3)^3$$

where W_d = wiring demand
W_c = wiring capacity
ε = PWB layout efficiency (determined in Sec. 16.4.3)

16.5.3 Wiring Capacity (W_c)

Substrate wiring capacity is the wiring length available to connect all the components. It is determined by two factors:

1. *Design rules*. These rules specify the traces, spaces, via lands, keepouts, and such that make up the surface of the substrate.
2. *Structure*. This factor determines the number of signal layers and the combination of through and buried vias that permit interconnection between layers and the complex blind, stacked, and variable depth vias available in high-density interconnection (HDI) technologies.

These two factors determine the maximum wiring available on the substrate. To figure the wiring available to meet the demand, multiply the maximum wiring by the layout efficiency. The data are straightforward except for layout efficiency. Layout efficiency expresses what percentage of wiring capacity can be used in the design. Equation (16.4) shows the formula for determining wiring capacity for each signal layer. The total substrate capacity is the sum of all the signal layers.

$$W_c = T \times L/G \text{ (in cm/square cm or in/square in)} \quad (16.4)$$

where T = number of traces per wiring channel or distance between two via pads
L = number of signal layers
G = wiring channel width or length between centers of the via pads

16.5.4 Layout Efficiency

Layout efficiency is the percentage of capacity from design rules and structure that a designer can deliver on the board. Layout efficiency is the ratio of the actual wiring density that it takes to wire up a schematic versus the maximum wiring density or W_d divided by W_c. Layout efficiencies, for ease of calculations, are typically assumed to be 50 percent. Table 16.2 provides a more detailed selection of efficiencies.

TABLE 16.2 Typical Layout Efficiencies

Design Scenario	Conditions	Efficiency*, %
Through hole, rigid	Gridded CAD	6–12
Surface mount/mixed	W/wo back side passives, gridless CAD	9–16
Surface mount/mixed	W/back side actives, gridded CAD	8–14
Surface mount only	W/wo back side passives, gridless CAD	Up to 18
Surface mount/mixed	1-sided blind vias, gridless CAD	Up to 20%
Surface mount/mixed	2-sided blind vias, gridless CAD	Up to 28
Built-up technologies	2-sided micro-blind vias, gridless CAD	Up to 35%

*Determined from analysis of printed circuit designs (actual wiring capacity from the CAD system divided by maximum wiring capacity (Eq. 16.4).

16.5.5 Selecting Design Rules

To calculate a potential set of design rules and signal layers, first the wiring demand (W_d) should be calculated. Wiring models help accomplish this.

16.5.5.1 Wiring Demand Models. Seven wiring models are reported in the literature, but the first three are used commonly. The three wiring models include:

- Coors, Anderson & Seward Statistical Wiring Length[4]
- Toshiba Technology Map[5]
- Hewlett Packard (HP) Design Density Index[6]

The other four wiring models include:

- Equivalent ICs per square inch[7]

- Rent's Rule[8]
- Section Crossing[9]
- Geometric Analysis[10]

16.5.5.1.1 Coors, Anderson, and Seward Statistical Wiring Length. This wiring demand model is based on a stochastic model of wiring involving all terminals. The probable wire length is calculated based on the distance of a second terminal and the spatial geometry of all other terminals. This is the most recently determined wiring model and represents the most practical approximation of surface mounting technology. Equation (16.5) presents the mathematical model that results.

$$d = D * N_i/A \text{ (in per sq. in)} \tag{16.5}$$

where D = ave. interconnection distance (in): $D = E(x)*G$

$E(x)$ = expectation of occurrence

G = pad placement grid (in)

N_i = total number of interconnections

A = routing area (sq. in)

Equation (16.6) for $E(9x)$ is the

$$E(x) = -\frac{1}{a}\frac{((S-T)(Sa-2))e\text{^}aS+S(2-(S-T)a)e\text{^}a(S-T)-2T}{(S-T)e\text{^}aS-Se\text{^}a(S-T)+T} \tag{16.6}$$

where $S = M + N$

$T = (M\text{^}2 + N\text{^}2)\text{^}.5$

$a = \ln \alpha$

$\alpha =$ empirically derived constant $= 0.94$

$M =$ board width of grid point $=$ (width/G) + 1

$N =$ board length of grid point $=$ (length/G) + 1

$N_i = 2*Nt/3$

16.5.5.1.2 Toshiba's Technology Map. The packaging technology map is a simple technique to predict a PWB, chip-on-board, or MCM-L wiring demand and its assembly complexity. By plotting components per square inch (or components per square centimeter) against average leads per component on a Log-log graph (see Fig. 16.11), you can calculate the wiring demand W_D in inches per square inch (or centimeters per square centimeters) and assembly complexity in leads per square inch (or leads per square centimeter). Equations (16.7) and (16.8) show the equations for these two metrics.

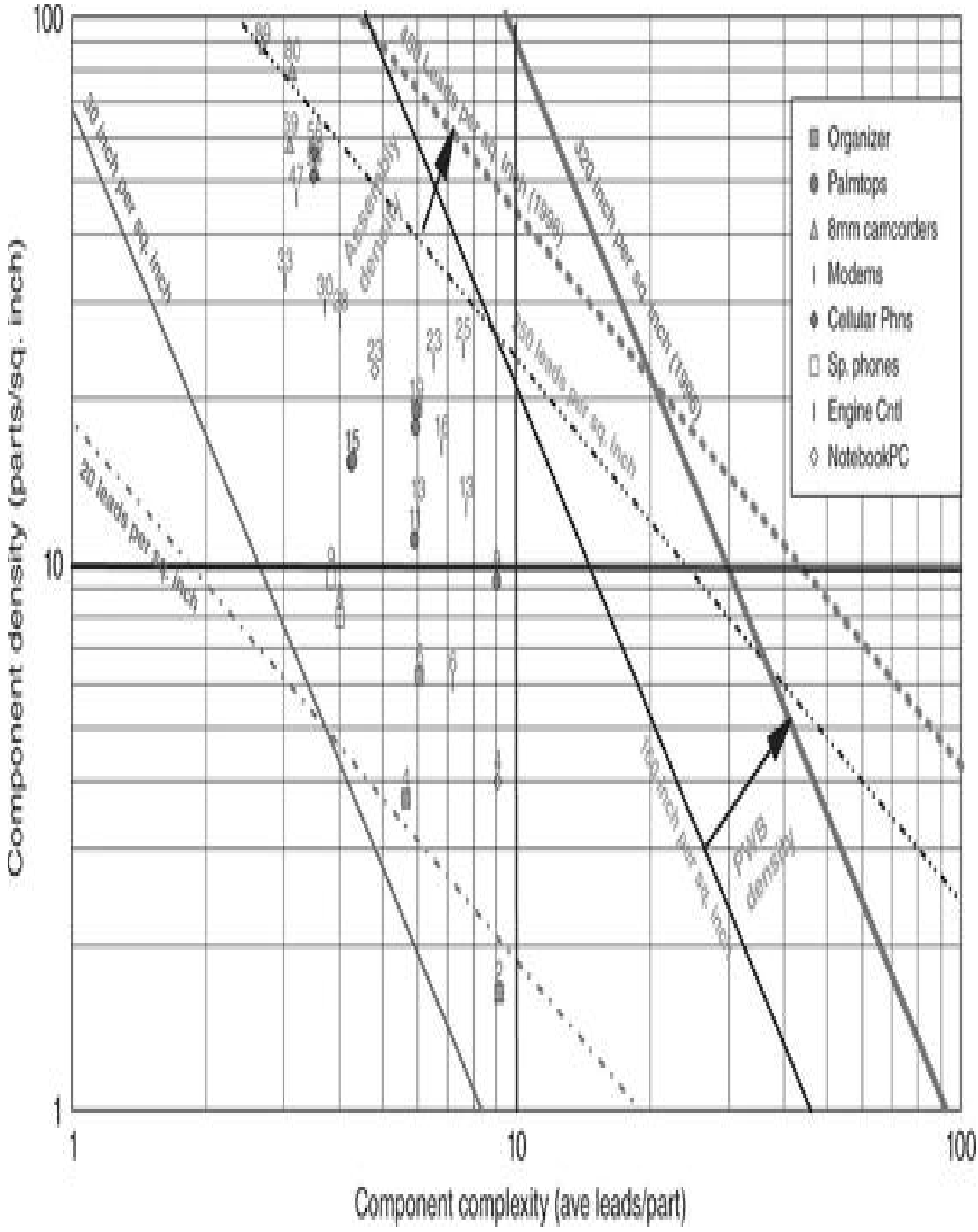


FIGURE 16.11 Packaging technology map.

$$\text{Wiring demand } W_D = \beta \times (\text{comp})^{0.5} \times (\text{leads}) \tag{16.7}$$

where β = wiring coefficient (typically 3.5 but can vary from 2.5 to 4.0 on average; notes/net is a good approximation)
comp = components per board area in sq. in or sq. cm leads = average leads (connections) per component

$$\text{Assembly complexity} = (\text{comp}) \times (\text{leads}) \tag{16.8}$$

where comp = components per board area in sq. in or sq. cm
leads = average leads (connections) per component

Using these two equations, Fig. 16.12 shows lines of constant wiring demand (in cm. per sq. cm or in per sq. in) and assembly complexity (in leads per sq. cm. or sq. in) that can be plotted on this chart (see Fig. 16.11).

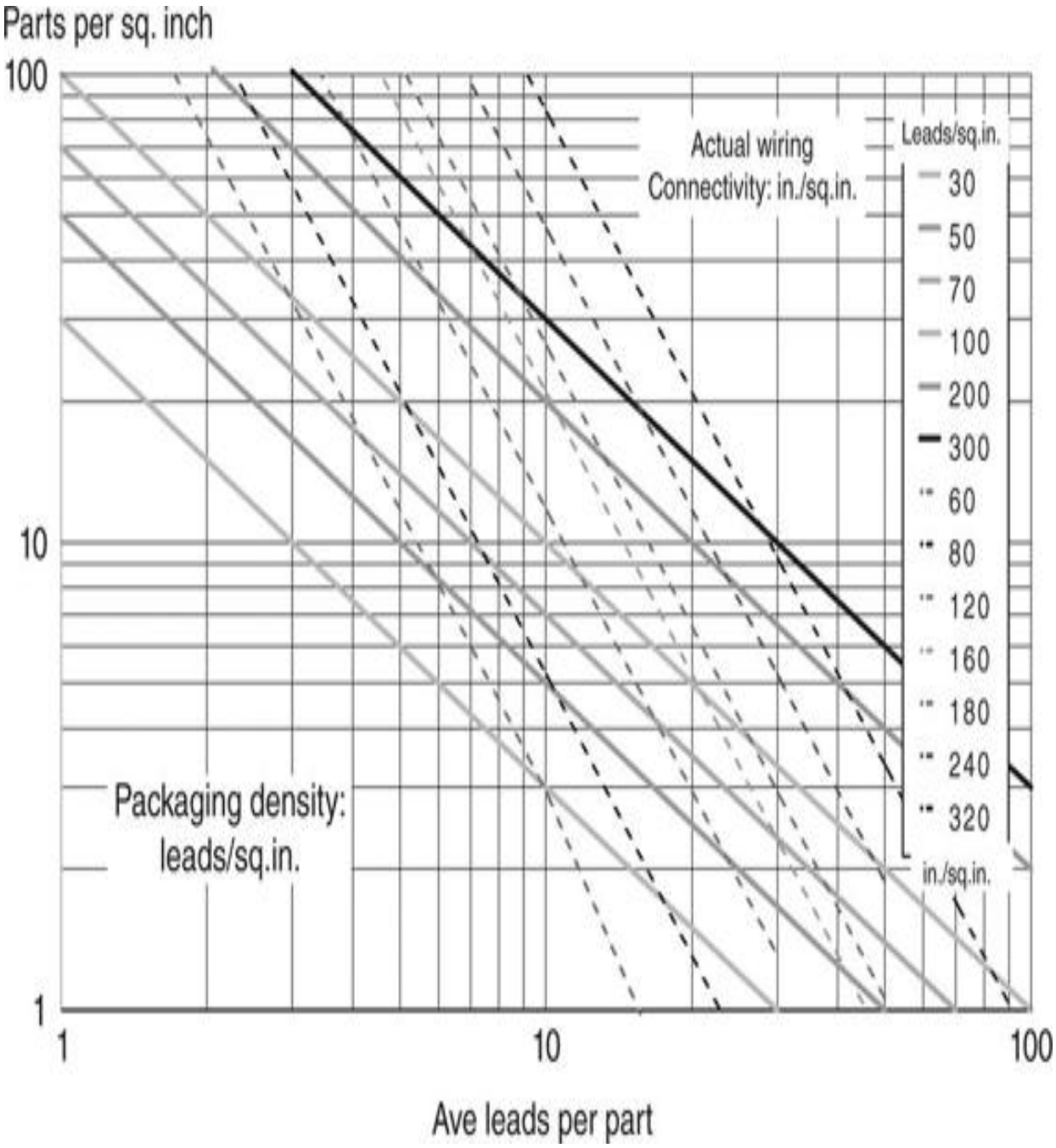


FIGURE 16.12 Wiring and assembly density.

16.5.5.1.3 HP's Design Density Index. Another metric is called the design density index (DDI). It is a correlation of the actual design rules for a PWB compared to the DDI metric. Equation (16.9) gives DDI, and Fig. 16.13 shows a typical calibration chart.

$$DDI = 13.6 \times (EIC/board\ area)^{1.53} \quad (16.9)$$

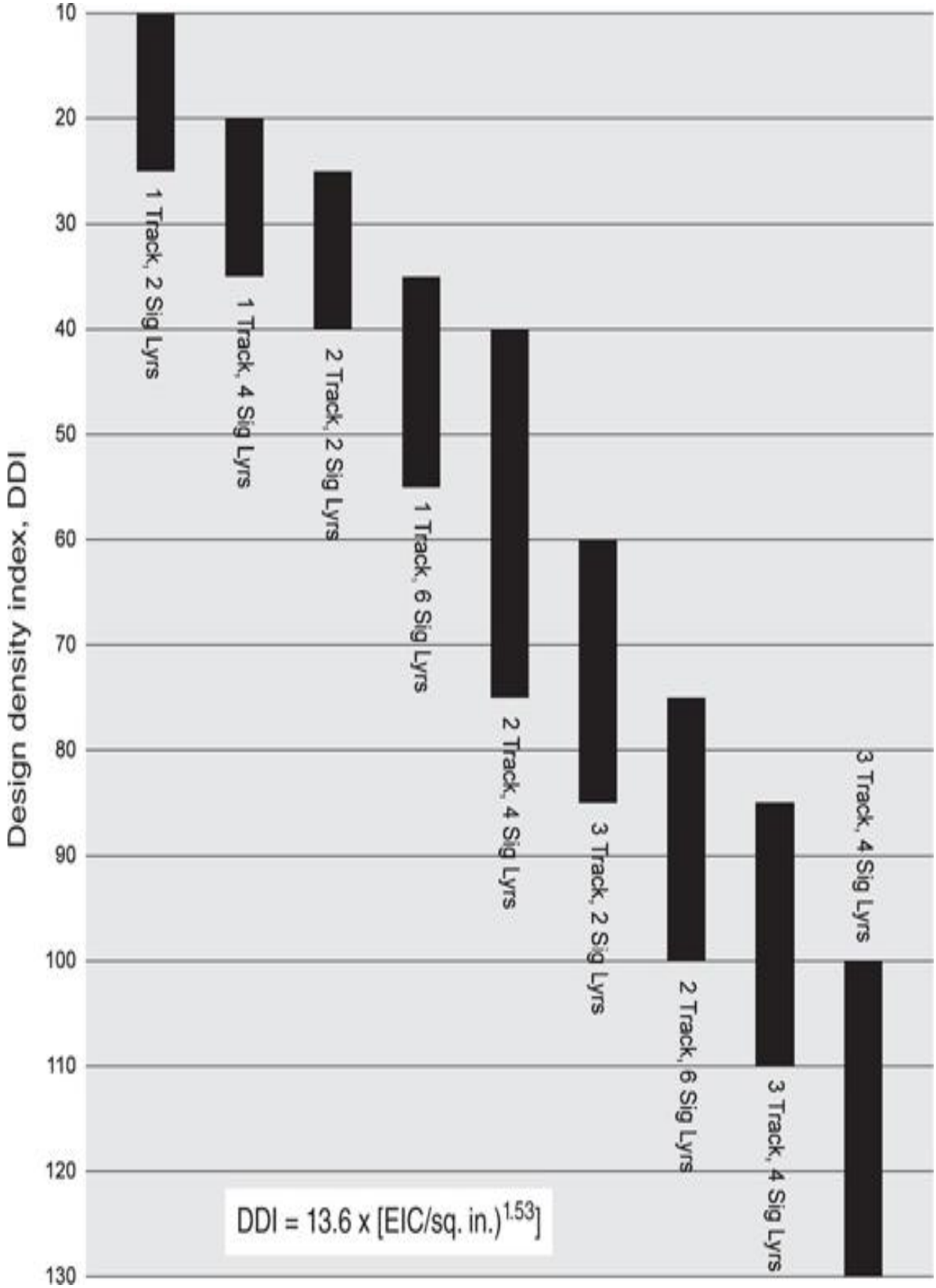

Design density index, DDI
10
20
30
40
50
60
70
80
90
100
110
120
130
1 Track, 2 Sig Lyrs
1 Track, 4 Sig Lyrs
2 Track, 2 Sig Lyrs
1 Track, 6 Sig Lyrs
2 Track, 4 Sig Lyrs
3 Track, 2 Sig Lyrs
2 Track, 6 Sig Lyrs
3 Track, 4 Sig Lyrs
3 Track, 4 Sig Lyrs
DDI = 13.6 x [EIC/sq. in.)^1.53]

FIGURE 16.13 Design rules and layer count for various DDIs.

The chart shown in Fig. 9.13 gives a good visual record in PWB layout of a company's efficiency. As various PC boards are charted, their DDIs form a distribution. This distribution is a form of layout efficiency (ε) since at the bottom of the distribution, more EICs are connected than at the top of the distribution.

16.5.5.1.4 Density of Equivalent ICs. EIC per unit area has been a traditional measure of density since the introduction of CAD systems in the early 1970s. A simple measure of the number of electrical connections required per unit area of the board, it remains in use with surface mounting technology and is usually referred to as EIC density. An EIC is the total number of leads of the components divided by 14 or 16, the old number of pins on a dual-inline package (DIP). Many people also use 20 as a divisor. Equation (16.10) defines EIC density mathematically in EIC/sq. in.

$$\text{EIC density} = \text{connections}/16/\text{board area} \tag{16.10}$$

where connections = total component leads

board area = top surface board area (in sq. cm or sq. in)

16.5.6 Typical Example of Wiring Demand Calculation

As an example, take a typical consumer electronic board with these characteristics:

- Design: consumer PCB, all through hole components
- Components: 86
- Leads: 1540

- Size: 16.6 in × 16.5 in = 57 sq. in
- EIC/sq. in = 110/57 sq. in = 1.93 [using Eq. (16.10)]
- DDI = 13.6 × $(1.93)^{1.53}$ = 316.7 ~

Figure 16.13 advises two tracks on two signal layers [using Eq. (16.9)].

16.6 PWB FABRICATION TRADE-OFF PLANNING

The metrics for PWB and chip-on-board (COB) fabrication involve with trade-offs between the performance objectives and the PWB price. Calculating prices requires the PCB characteristics and manufacturing yield. Manufacturing yield requires producibility estimates. Three items are required to predict PCB prices:

- Fabrication complexity matrix
- Prediction of producibility and first-pass yield
- Relative price as a function of a price index

16.6.1 Fabrication Complexity Matrix

The fabrication complexity matrix is supplied by a PWB fabricator. It relates the various design choices on a PWB to design points. These points are based on the actual prices that a fabricator will charge for these features. They are calculated by dividing the actual costs and the values by the smallest nonzero amount. Typical factors that fabricators can use to price a printed wiring board include the following:

- Size of the board and number that fit on a panel

- Number of layers
- Material of construction
- Trace and space widths
- Total number of holes
- Smallest hole diameter
- Solder mask and component legends
- Final metalization or finish
- Gold-plated edge connectors
- Factors specific to the design

A typical fabrication complexity matrix would look like Table 16.3. This is not a complete matrix, but does show the design factors and the design points assigned to each.

TABLE 16.3 Example of Fabrication Complexity Matrix

Factors	Pts.	Highest	Pts.	High Middle	Pts.	Low Middle	Pts.	Lowest
No. of layers	12	8	8	6	4	4	1	2
Trace width (mils)	8	4	5	5–6	3	7–8	1	10
No. of holes	10	5000–8000	5	3000–5000	3	10000–3000	1	>10000

16.6.2 Predicting Producibility

The simple truth about printed circuit boards, multichip modules, and hybrid circuits is that the design factors such as those listed previously can have a cumulative effect on manufacturing yield. These factors all affect producibility. Specifications can be selected that individually may not adversely affect yields but cumulatively can significantly reduce yields. A simple algorithm is available that collects these factors into a single metric, in this case called the complexity index (CI). It is given in Eq. (16.11).

$$\text{Complexity index} = \frac{(\text{area})(\text{holes/unit area})^{\wedge 2}(\text{no. layers})^{\wedge 3}}{(\text{min. trace width})(\text{min. annular ring})(\text{min. hole dia.})} \quad (16.11)$$

where area = top area of the substrate to be designed
holes = total number of drilled holes, blind, buried, and through
holes/unit area = holes divided by board Area
trace width = the minimum trace width on the substrate
layers = the total number of layers in the substrate
annular ring = ½ the difference between the via land and the hole dia.
hole dia. = finished hole size

where area, number of holes, minimum trace width, number of layers, and minimum tolerance (absolute number) are the factors of the board being designed.

16.6.2.1 First-Pass Yield. The first-pass yield equation derives from the Wiebel probability failure equations.[11] Equation (16.12) is of a more general form of the equation typically used to predict ASIC yields by defect density.

$$\text{FPY\%} = \frac{100}{\text{Exp}[(\log \text{CI}/\text{A})^{\wedge}\text{B}]} \quad (16.12)$$

where FPY = first-pass yield
CI = complexity index
A, B = constants

To determine the constants A and B in Eq. (16.12), a fabricator will need to characterize their manufacturing process. Selecting a number of printed circuits currently being produced that have various complexity indexes does

this, ideally some low, medium, and high. The first-pass yield (at electrical test without repair) of these printed circuits for several production runs is recorded. Any statistical software program[12] that has a model-based regression analysis can now determine A and B from the model [Eq. (16.13)].

$$\text{FPY} = f[x] = 100 \div \text{EXP}\{\text{LOG}(\text{complexity} \div \text{PARM}[1])\text{^}\text{PARM}[2]\} \qquad (16.13)$$

$$\text{where PARM}[1] = \text{A}$$
$$\text{PARM}[2] = \text{B}$$

The first-pass yield will follow the examples in Fig. 16.14. Constant A determines the slope of the inflection of the yield curve, whereas constant B determines the *x*-axis point of the inflection.

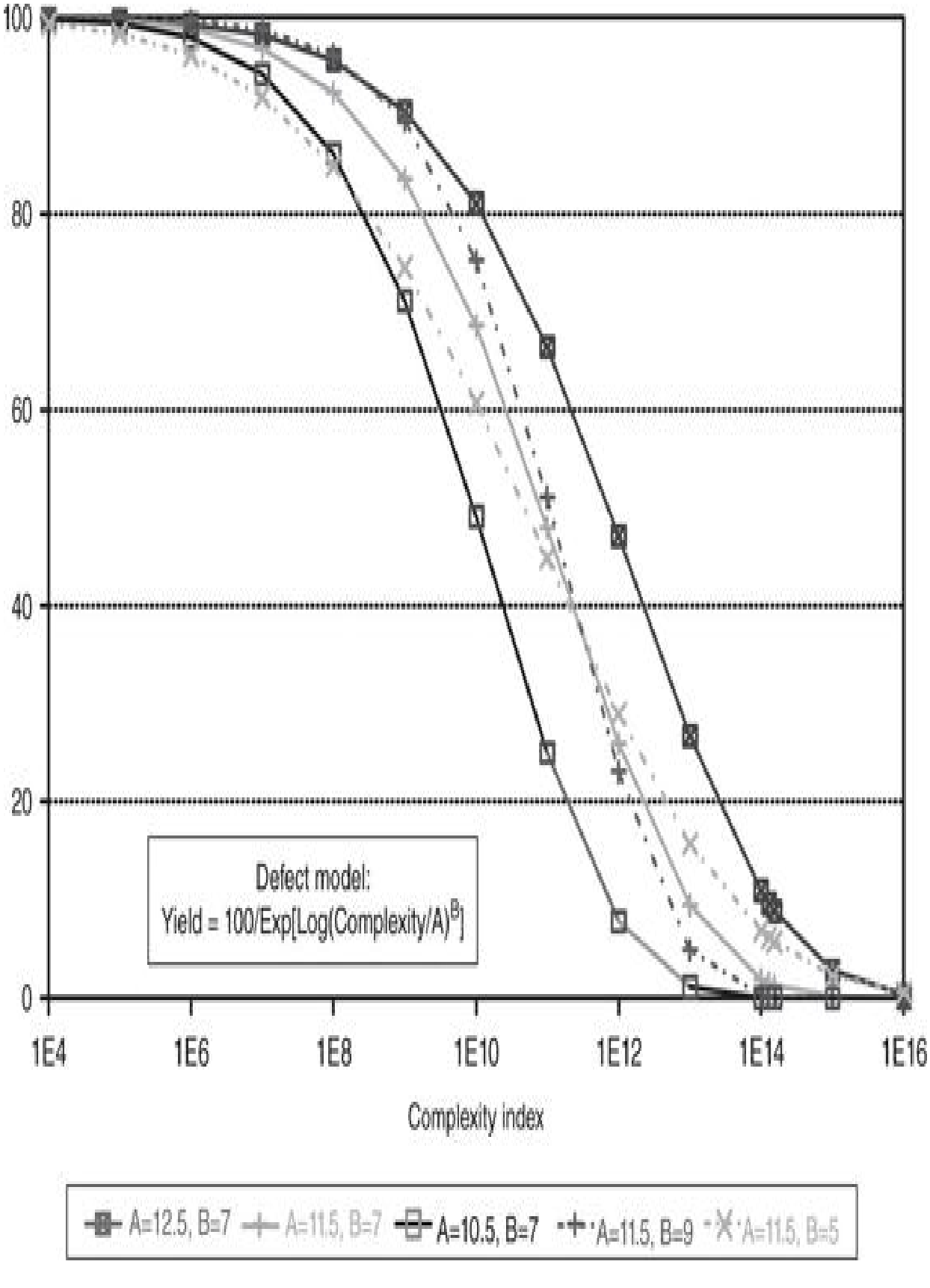

100
80
60
40
20
0
1E4
1E6
1E8
1E10
1E12
1E14
1E16
Complexity index
Defect model:
Yield = 100/Exp[Log(Complexity/A)^B]
A=12.5, B=7
A=11.5, B=7
A=10.5, B=7
A=11.5, B=9
A=11.5, B=5

FIGURE 16.14 Estimated first-pass yield as a function of PWB design complexity.

Alternatively, any spreadsheet can be used to determine constants A and B. The [REGR] function in a spreadsheet like Excel™ or Lotus 1-2-3™ is used. The [REGR] function is defined as: (=LINEST(known_y's, known_x's,TRUE,TRUE). To use this function, you must first put the FPY function into the form $y = Ax + B$. This is done by creating two columns: complexity index (which we will call X1) and yield. A third column is created for {log[log(X1)]}, whereas a fourth column is created for {log[ln(-yield/100)]}. Provide the regression function with column 4 as known_ys and column 3 as known_xs. The regression function will return 10 values; FIT (slope & int.), sig-M (slope & int.), r2, sig-B(slope & int.), F,df (slope & int.), and reg sum sq (slope & int.). The constant B is equal to the FIT (slope) and the constant A is 10^[−FIT(int.)/FIT(slope)]. (Remember, to calculate an array, follow these steps: highlight the array on the spreadsheet; type the array formula, making sure that the cursor is in the edit bar; then press CTRL + SHIFT + ENTER.)

16.6.2.2 Yield Calculation Steps. To calculate the first-pass yield coefficients, there are six steps:

1. Collect design attributes of 10 to 15 currently running boards with various size and layers (see Table 16.4).

TABLE 16.4 Example of PCB Part Information and Calculated Complexity Index

P/N	PCS SIZE Length (in.)	Width (in.)	Hole Quantity	Hole Density	Layers	Thickness (mil.)	Min. Trace Width (mil.)	Min. Annular Ring (mil.)	Min. Hole Size (mil.)	Aspect Ratio	Complexity x1
#1	11.500	9.210	4842	45.7	6	82.7	6	4	12	6.89	1.14E+06
#2	11.500	8.900	3217	31.4	8	62.0	5	5	8	7.75	2.01E+06
#3	6.050	1.090	379	57.5	4	46.2	6	5	12	3.85	1.49E+04
#4	5.210	4.330	1538	68.2	6	72.4	6	5	10	7.24	5.46E+05
#5	6.050	1.410	868	101.8	6	50.0	6	5	14	3.57	1.62E+05
#6	7.240	11.460	5274	63.6	8	61.9	5	5	14	4.42	2.17E+06
#7	11.460	6.510	6015	80.6	8	61.9	6	5	8	7.74	8.00E+06
#8	9.600	10.370	4970	49.9	12	47.0	5	5	13	3.62	4.77E+06
#9	11.790	9.490	6034	53.9	10	62.0	5	5	12	5.17	5.60E+06
#10	12.780	4.200	4038	75.2	12	62.0	6	5	10	6.20	1.08E+07
#11	6.050	1.455	554	62.9	6	50.0	6	5	14	3.57	6.40E+04
#12	5.380	5.670	1118	36.7	4	55.1	7	5	18	3.06	1.27E+04
#13	1.250	2.660	220	66.2	4	32.0	7	8	14	2.29	2.72E+03

2. Collect the first-pass yield information for these selected boards, at least 10 runs (see Table 16.5).

TABLE 16.5 Example of PCB Production Yields from 10 Runs

P/N	First-Pass Yield (at Electrical Test)										
Run	1	2	3	4	5	6	7	8	9	10	Average
#1	92.6	84.9	86.9	82.9	90.0	95.2	90.1	92.4	93.0	92.0	90.0
#2	85.6	85.7	94.2	86.2	86.6	86.7	86.6	89.7	95.6	85.6	88.2
#3	95.6	93.9	93.6	97.8	97.3	95.1	94.2	96.2	96.9	91.6	95.2
#4	92.3	93.3	95.0	92.6	94.5	95.5	93.5	89.7	88.8	89.8	92.5
#5	94.8	97.6	96.4	96.6	94.1	93.2	94.3	93.2	91.8	91.2	94.3
#6	86.8	85.3	88.1	90.8	86.5	87.0	88.0	87.2	86.5	88.9	87.5
#7	90.3	80.9	86.3	87.9	87.1	92.7	87.3	87.6	82.4	88.9	87.1
#8	89.3	87.0	86.6	83.5	91.6	90.1	87.5	86.2	88.1	87.3	87.7
#9	87.2	87.9	86.6	85.7	89.4	87.3	90.6	86.5	85.9	82.9	87.0
#10	86.6	88.1	82.6	84.4	88.0	87.0	79.0	87.0	88.0	80.0	85.1
#11	92.7	92.7	97.2	95.1	96.9	94.3	93.4	95.3	91.6	96.6	94.6
#12	93.8	95.3	98.2	96.3	94.1	95.9	94.2	92.3	94.8	95.6	95.0
#13	99.2	98.6	99.1	98.7	97.9	99.6	99.6	99.1	99.0	99.3	99.0

3. Calculate the board complexity index and average yield.

4. Prepare a spreadsheet of transformed CI (x1) and Yield (Y) (see Table 16.6).

TABLE 16.6 Example of Excel™ Transformation Setup for Complexity and Yield Data

Sample	Complexity X1	YIELD Y	Log-Log (x1)	Log in (−Y/100)	Log-Log Fit All Data	Error All Data	Log-Log Fit Avg. Only	Error Avg. Only
#1-1	1144136	92.6	0.78	−1.11	90.6	−2.0	90.1	−2.5
#2-1	2006116	85.6	0.80	−0.81	89.4	3.8	88.9	3.3
#3-1	14909	95.6	0.62	−1.35	97.0	1.4	96.7	1.1
#4-1	546435	92.3	0.76	−1.10	92.0	−0.3	91.5	−0.7
#5-1	162158	94.8	0.72	−1.27	94.1	−0.7	93.6	−1.1
#6-1	2167611	86.8	0.80	−0.85	89.2	2.5	88.7	1.9
#7-1	8002482	90.3	0.84	−0.99	86.1	−4.2	85.6	−4.7
#8-1	4773612	89.3	0.82	−0.95	87.4	−1.9	86.9	−2.4
#9-1	5604279	87.2	0.83	−0.86	87.0	−0.2	86.5	−0.7
#10-1	10848424	86.6	0.85	−0.84	85.3	−1.3	84.8	−1.8
#11-1	64014	92.7	0.68	−1.12	95.4	2.7	95.0	2.3
#12-1	12737	93.8	0.61	−1.19	97.2	3.4	96.9	3.1
#13-1	2716	99.2	0.54	−2.10	98.4	−0.8	98.2	−1.0
#1-2	1144136	84.9	0.78	−0.78	90.6	5.7	90.1	5.2
#2-2	2006116	85.7	0.80	−0.81	89.4	3.7	88.9	3.2
#3-2	14909	93.9	0.62	−1.20	97.0	3.1	96.7	2.8
#4-2	546435	93.3	0.76	−1.16	92.0	−1.3	91.5	−1.7
#5-2	162158	97.6	0.72	−1.62	94.1	−3.5	93.6	−4.0
***	***	***	***	***	***	***	***	***
#11-13	64014	96.6	0.68	−1.46	95.4	−1.2	95.0	−1.6
#12-13	12737	95.6	0.61	−1.35	97.2	1.6	96.9	1.3
#13-13	2716	99.3	0.54	−2.13	98.4	−0.9	98.2	−1.1
				AVG Error	—	**0.4**	—	**0.0**
				STD DEV	—	**4.4**	—	**4.5**

5. Calculate regression coefficients (see Table 16.7).

TABLE 16.7 Example of Excel™ Regression Results

	All Data		AVG Only	
Log-log Fit	Slope	Int.	Slope	Int.
FIT	3.17	−3.48	3.06	−3.38
Sig-M	0.18	0.13	0.34	0.25
R2, sig-B	0.73	0.19	0.88	0.12
F, df	312.60	115	81.75	11
Reg sum sq	11.01	4.05	1.14	0.15
B	3.17		3.06	
A	12.57		12.66	

6. Calculate A and B from regression fits.

16.6.2.3 PCB Part Information. Collect design attributes of 10 to 15 currently running boards with various size and layers (see Table 16.3).

16.6.2.4 PCB Production Yield Data. Collect the first-pass yield information for these selected boards, for at least 10 runs (see Table 16.5)

16.6.2.5 Calculating the Board Complexity Index and Average Yield: Regression Analysis Methodology. To determine the constants A and B in Eq. (16.12), you can use any statistical software program that has a model-based regression analysis. The model is shown in Eq. (16.13). Table 16.6 shows an example of an Excel™ spreadsheet setup, and Table 16.7 shows the regression results.

16.6.3 Example of a Complete PWB Complexity Matrix

This section presents an example of how one company approached this planning process as part of its PWB design for manufacturing program.

16.6.3.1 PWB Fabrication Complexity Matrix. The PWB fabrication complexity matrix (FCM) that this company developed is shown in Table 16.8. This FCM is built on a “per panel” basis of 18 in by 24 in rather than a “per board” basis. Also, volume is assumed to be in a preset amount.

TABLE 16.8 Example of One Company’s Fabrication Complexity Matrix

Fabrication Factors	Pts.	Highest	Pts.	High Middle	Pts.	Low Middle	Pts.	Lowest
Material of construction	147	Polyimide	88	BT	49	FR-4	40	CEM III
No. of layers	196	12 layers	137	8 layers	89	4 layers	36	2-sided
No. of holes/panel	270	<20,001	180	10,001–20,000	90	3001–10000	27	>3000
Min. Trace/spacing	25	2 mil.	10	3–4 mil.	6	5–6 mil.	1	<=6 mil.
Gold tabs	48	3 Sides	32	2 Sides	16	1 Side	0	None
Annular ring	30	>2 mil.	21	2–4 mil.		4–6 mil.	1	<6 mil.
Solder mask	25	2 S Dry film	17	2 S LPI	7	1 S LPI	5	Screened
Metalization	75	Electroless Ni/Au	69	Selective lead-free solder coat	46	Immersion silver	29	SMOBC/ organic coat
Min. hole dia.	166	<= 8 mil.	84	9–12 mil.	69	13–20 mil.	5	<20 mil.
Controlled impedance tolerance	105	+/–5 %	62	+/–10 %	30	+/–20 %	0	None

Points are per PANEL. For board: Divide by no. per PANEL

16.6.3.2 PWB Complexity. Figure 16.14 shows this company's first-pass yield. The curve with $A = 11.5$ and $B = 9.0$ was current for 6 months. Price index is the total points from the complexity matrix divided by the first-pass yield.

16.6.3.3 Relative Costs. The price index data for this company is shown in Fig. 16.15. The price index (PI) can vary from 150, which corresponds to a 70 percent price reduction,

to a PI of 1000 which corresponds to a 275 percent increase in price.

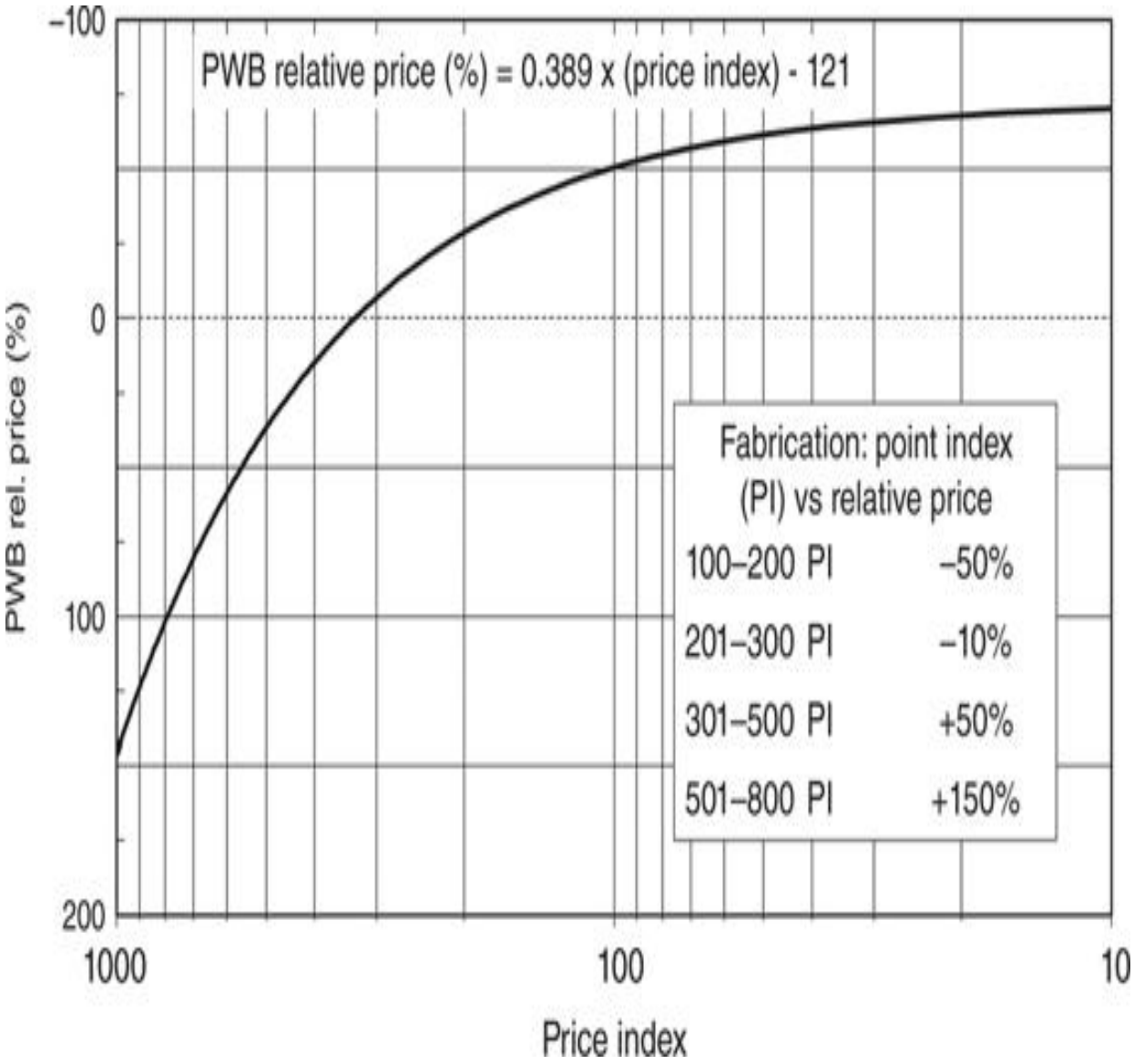


FIGURE 16.15 PWB relative price as a function of the price index.

16.6.3.4 PWB Fabrication Example. Let's continue with the consumer electronics board example from Sec. 16.4.5. Table 16.9 lists the initial design characteristics of the printed circuit and the resultant total design points. Table 16.10 shows the calculation of the complexity index,

estimated first-pass yield, and resultant price index and price adjustment.

TABLE 16.9 One Company's Fabrication Complexity Makeup

Fabrication Factors	PWB Design #1	Points	FCM
Mat'l of construction	FR-4	49	FR-4
No. of layers	six	137	Six layers
No. of holes	$1655 \times 6 = 9930$	90	3001–10,000
Min. trace wd.	0.008 in	6	6–8 mil
Gold tabs	None	0	None
Annular ring	0.010 in	1	<6 mil
Solder mask	2-sided LPI	17	2-sided LPI
Metalization	SMOBC/SSC	69	SMOBC/SSC
Min. hole dia.	0.025 in	5	<20 mil
Cont. impedance	None	0	None
TOTAL POINTS =		374	

TABLE 16.10 One Company's Initial Consumer Board Characteristics

Size	516.0 sq. in
No. of layers	Six layers
No. of holes	1655
Min. trace width	0.008 in
Tolerance (+/−in)	0.003
Complexity index	68.06
First-pass yield	90.7%
Price index	412.3
Rel. price	+ 14.5%

$A = 35, H = 1000, L = 2, T = .01, T_O = .01$

The wiring demand indicates that a 0.007 in trace and a 0.008 in spacing (two track) for a 1.100-in grid (channel) represent more density than is required (see Sec. 16.4.5). A one-track wiring on two signal layers could achieve the required wiring density or a 0.012-in trace with a 0.013 in spacing. The size required a panel layout, as shown in Fig. 16.16*a*, of six per panel. A reduction of 14 sq. in. in the board size would allow eight boards on a 18 in × 24 in panel (see Fig. 16.16*b*).

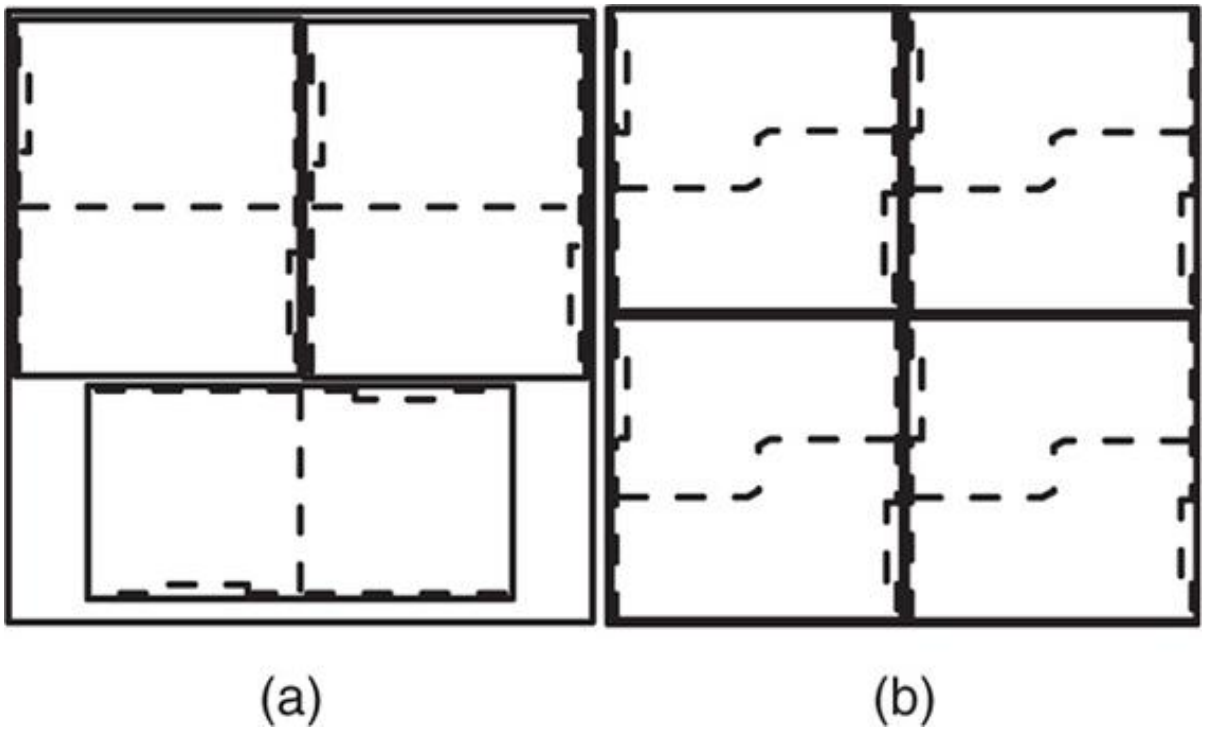


FIGURE 16.16 Fabrication panel layout of the consumer electronics board: (*a*) the original design; (*b*) the final layout.

A simple Gate Array ASIC was employed to reduce the small-scale ICs until 14 sq. in of space was freed up. The final optimized PCB had the fabrication factors seen in Table 16.11. The boards were eight up on a panel (Fig. 16.16*b*) and had a higher producibility by a 18 percent reduction in its complexity and an overall price reduction of 24.7 percent.

TABLE 16.11 One Company's Final Consumer Board Characteristics

Size	43.6 sq. in
No. of layers	Four layers
No. of holes	1156
Min. trace width	0.012 in
Tolerance (+/−in)	0.003
Complexity index	55.8 (24.0)
First-pass yield	96.7%
Price index	331.9
Rel. price	−10.2%

$A = 35, H = 1000, L = 2, T = .01, T_O = .01$

16.7 ASSEMBLY TRADE-OFF PLANNING

The metrics of assembly trade-offs relates factors of process, component selection, and test to assembly prices. Yields and rework are factored into the points of the Assembly Report Card. The point total provides an estimation of the relative prices of assembly and test.

16.7.1 Assembly Complexity Matrix

The PCB assembler supplies the assembly complexity matrix. This matrix relates various process assembly and test choices that the assembler provides along with component size, orientation, complexity, and various other known qualities to the costs of providing for these design choices.

To relate these qualities to the costs, the matrix allocates design points. Typical factors that affect assembly costs are

- One-pass or two-pass infrared reflow
- Wave solder process
- Manual or automatic parts placement
- Odd-shaped parts
- Part quality level
- Connector placement
- Test coverage
- The ability to diagnose tests
- Assembly stress testing
- Repair equipment compatibility

By collecting all the costs associated with assembly, test, and repair and then normalizing these costs with the smallest nonzero value, a matrix such as shown in Table 16.12 can be produced.

TABLE 16.12 Factors in an Assembly Complexity Matrix

Factors	Pts	Highest	Pts	Middle	Pts	Lowest
Solder process	35	1 pass IR	20	2 pass IR	0	IR and wave solder
Placement	8	100% auto	5	99%–90% auto	0	>90% auto
Digital test coverage	9	<98%	3	98%–90%	0	>90%
Manual attachment	8	100% Auto	25	Brackets	0	Post solder assembly

16.7.2 Example of an Assembly Complexity Matrix

An example of the assembly complexity matrix is the Assembly Report Card created by IBM-Austin. This complexity matrix has 10 factors that range in points from 0 to 35. The total points can affect the prices from a 30 percent discount to a 30 percent penalty. Table 16.13 illustrates this assembly complexity matrix trade-offs with design points.

TABLE 16.13 Assembly Complexity Matrix Defined as an Assembly Report Card

Assembly factors	Points	A	Points	B	Points	C	Points	D
Assembly process	35	2-pass IR	25	IR/wave B/S passives	20	IR/wave ≤ 5 B/S actives	0	IR/wave >5 B/S actives

- 2-pass IR is lowest-cost process due to low defect/repair level.
- Maximize SMT content, some PTH OK.
- Back-side SMT attachment with a wave solder process requires the use of adhesive.
- Back-side actives have a high defect level when the wave solder process is used.

Stress tests	15	0 hours	12	≤3 hours in situ	6	≤6 hours in situ and ≤3 hours static	0	<6 hours

- Stress test is a high-cost process step due to cost of chambers, fixtures, and process time.
- Stress test can be eliminated by using robust components, design, and process.

Parts SPQL	10	No high hitters	7	<2 high hitters	4	<4 high hitters	0	>5 high hitters

- Parts SPQL is the quality level of the parts used in the process (shipped product quality level).
- High hitters are parts known to have a high defect rate.

ICT digital test coverage	9	>98% coverage	6	>95% coverage	3	>90% coverage	0	<90% coverage

- The key to high test coverage is the selection of major components that have built-in testability and a PWB design with 1 test point per net.

Diagnosability	9	≤10 min	6	≤20 min	3	≤30 min	0	>40 min

- Effectiveness of diagnostic tools provided by the card designer influences diagnostic time.

Placement/insertion	6	100% auto	4	≥95% auto	2	≥90% auto	0	<90% auto

- Elimination of manual component placement and insertion reduces process time, defects, and process cost.

Manual attachment	6	100% auto	4	Simple bracket	2	Difficult bracket	0	Post-solder assembly

- Simple bracket = <1 min assembly time
- Difficult bracket = >1 min assembly time
- Post-solder assembly = manual solder operation

Connector selection	4	Auto assembly and retention and keyed	2	Manual and retention and keyed	1	Manual and retention	0	Manual

- Manually inserted connectors that are keyed and have retention reduce defects.
- Prepackaged SMT connectors that can be automatically placed are considered equivalent to keyed with retention.

Handling damage exposure	3	No handling list violations	2	<3 handling list violations	1	<5 handling list violations	0	>6 handling list violations

- Single inline packages (SIPs) > 0.5 in high
- Memory SIMM connectors with plastic latches
- Unshrouded headers over 0.5 in high

Repair	3	100% auto	2	≥90% auto	1	<90% auto	0	<90% auto and difficult

- Auto repair refers to the use of semiautomated repair tools for the removal of large components and connectors.
- A difficult repair is one that takes >10 min.

16.7.2.1 SMT Assembly Report Card. The IBM Assembly Report Card's[13] 10 assembly trade-off factors are shown in Table 16.13. The report card was the work of many assembly engineers with the help of the accounting

department. The report card was introduced in early 1990s; within 2 years, through the use of the report card, assembly point scores were averaging around 75 instead of the earlier 50, with its Gaussian distribution. Remember, higher scores indicate more producibility. This effect can be seen in Fig. 16.17. The scores are no longer normally distributed.

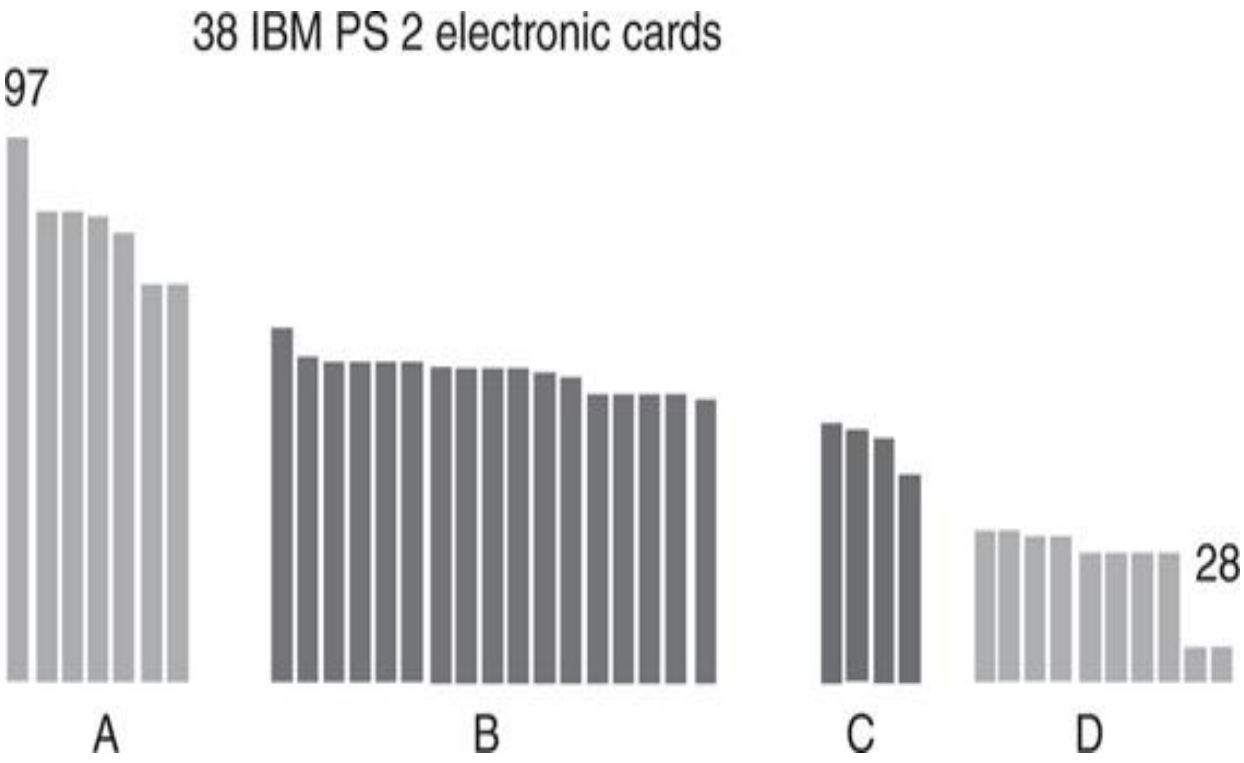


FIGURE 16.17 Improvement in producibility scores as a result of the Assembly Report Card.

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CHAPTER 17

PHYSICAL CHARACTERISTICS OF THE PCB

Lee W. Ritchey
Speeding Edge, Napa Valley, California

17.1 INTRODUCTION

Advances in semiconductor technology in the first decade of the 21st century have had a dramatic effect on what can be done in a single integrated circuit. Transistor gate lengths as small as 22 nanometers have made possible integrated circuits with performance at ultra-high speeds and incredible transistor densities.

At the turn of the 21st century the upper limit on transistor count of an integrated circuit was 200 million with data speeds as high as 2.5 gigabit per second (Gb/s) over a single data path. Currently, integrated circuits are commonly made with more than a billion transistors with data rates as high as 28 Gb/s over a single data path.

This advance in integrated circuit technology has made possible products that could only have been imagined a few

years ago. In addition to all of the products that have been in use for many years, two very diverse new product categories have developed around these advances. These are the ultra-density cell phones and tablets that have crept into every aspect of our lives and, driven by these same devices, the ultra high performance routers, switches and servers that provide all of the Internet services.

The first of these has driven component packages to lead pitches as small as 0.4 mm or 16 mils with components on both sides of the printed circuit board (PCB) substrate. This has given rise to buildup PCBs and laser drilled blind vias as small as 0.1 mm or 4 mils. This technology had driven laminate manufacturers to develop ultrathin laminates and prepregs that have glass weaves that are uniformly spread out to improve the quality of laser drilled blind vias.

The effect of these changes is not apparent when one looks at the size of the cell phones and tablets as the external packages remain relatively the same. What these changes have done is make it possible to put entire systems, such as GPS, in the same package with the phone as well as allow the user to surf the Web and watch real-time TV and movies. This is remarkable innovation made possible by improvements in IC technology.

The second of these has driven the performance of routers, switches and servers to unprecedented highs in a very short time period. Figure 17.1 is a terabit router introduced in 2002. It uses half a rack, weights 350 lb (160 kg) and consumes seven kilowatts of power. Figure 17.2 is the same terabit router 5 years later in 2007. It is only 1U high, weighs 22 lb (10 kg) and consumes 700 W.

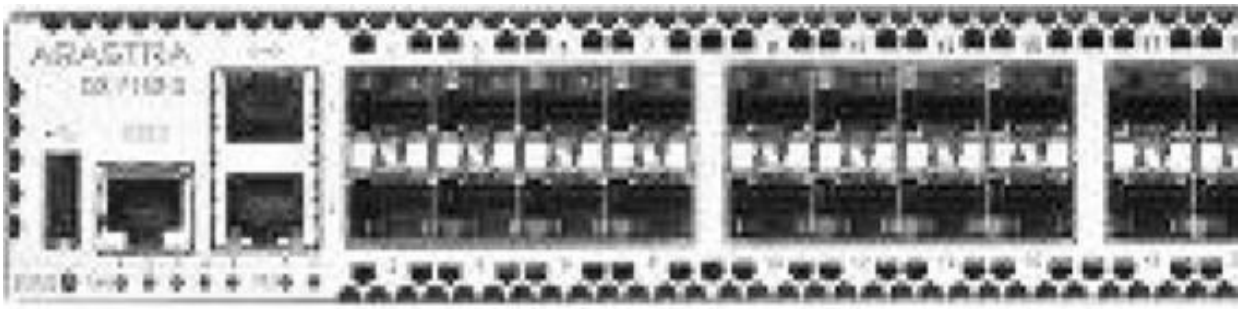


FIGURE 17.1 A terabit router in 2002.

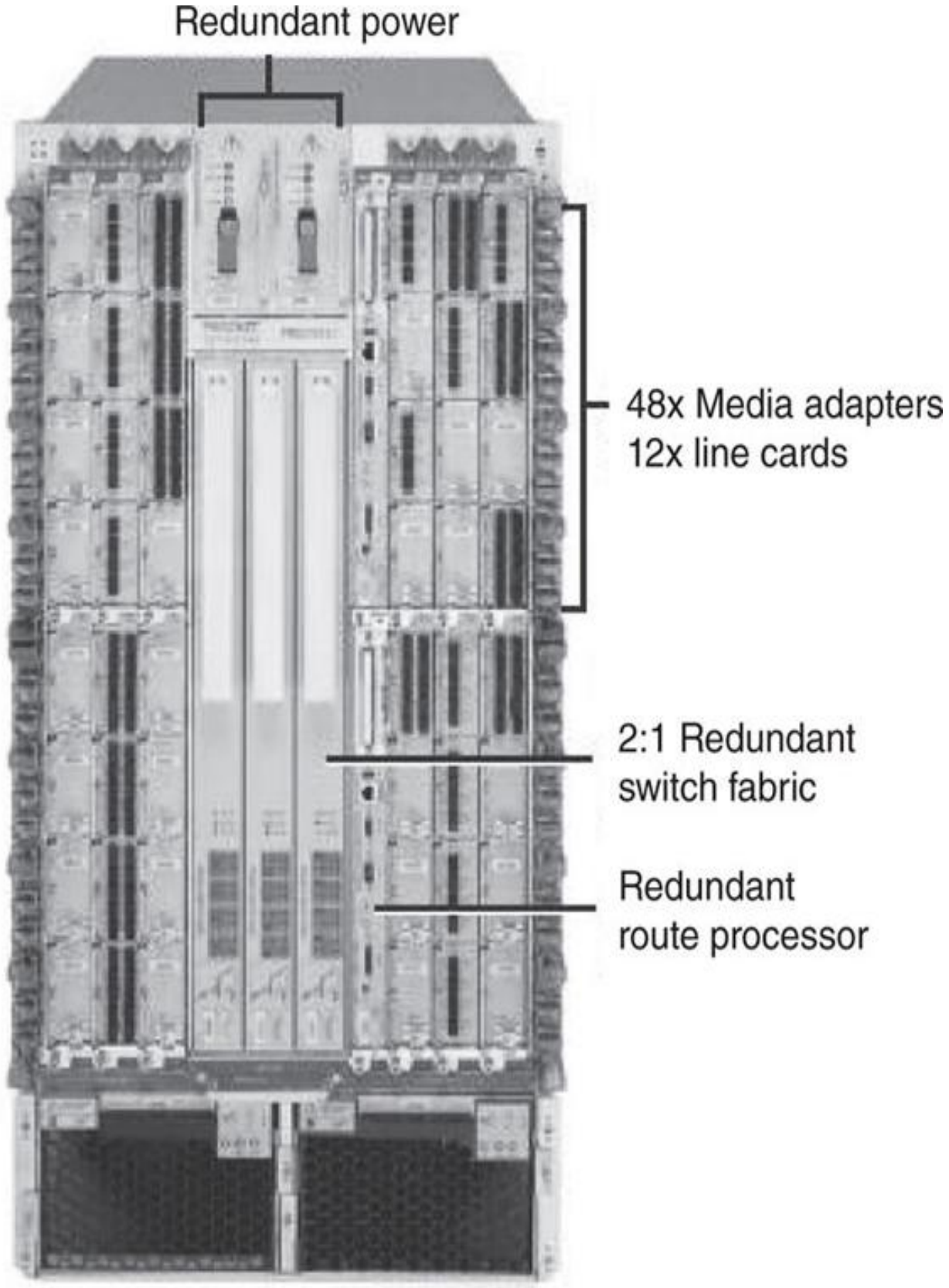

Redundant power
48x Media adapters
12x line cards
2:1 Redundant
switch fabric
Redundant
route processor

FIGURE 17.2 A terabit router in 2007.

More recently, the capacity of the 1U router shown in Fig. 17.2 has increased to 2.5 terabits (Tbs) in the same size package with 32 each 40 Gb/s ports across the front panel. Where technology takes performance seems to have no limits.

The fastest signal on a PCB in the 2002 router was 2.5 Gb/s. The fastest signal on a PCB in the 2007 router is 10 Gb/s. The routers being developed in 2014 will contain signals as fast as 32 Gb/s. These “digital” signals are operating it the frequency band once considered microwave. As a result, laminate considerations that once applied only to RF and microwave are integral to success with these products. Among these are copper loss, loss in the laminates and uniformity of the glass weave, none of which were issues as recently as 2000 with digital products. In fact, demands placed on laminate suppliers by the digital world are more difficult than those by the RF microwave community.

The difference between RF and digital world has blurred as a result of the speed increases in digital electronics. RF and microwave have usually involved signals in excess of a few megahertz while digital was confined to below 100 megahertz. As described above, high performance digital products now operate in the same frequency spectrum as many microwave products, blurring the line between these two technologies.

17.2 TYPES OF PCBs OR SUBSTRATES

Since the last edition of the *Printed Circuits Handbook* many changes have taken place in how PCBs and substrates are made. Some of the technologies such as hybrids, and

multichip modules have nearly vanished from the marketplace. Multiwire PCBs have vanished completely. Others have become commonplace, such as buildup PCBs which are the backbone of every cell phone.

17.2.1 Single and Double Sided PCB

These PCBs have conductor patterns on one or both sides of a base laminate with or without plated through holes to connect circuits on the two sides. These are the workhorse of consumer electronics, automotive electronics, and the RF/microwave industry. They are the lowest cost choice for consumer electronics. Laminate materials range from resin impregnated paper to low loss Teflon™ for RF applications.

17.2.2 Multilayer PCBs

As the name implies multilayer PCBs have more than two layers. Multilayer PCBs with as many as 50 layers have been successfully designed and manufactured. The inner layers may be a combination of signal layers and plane layers used to distribute power to the components mounted on the outside layers. Connections are made between the outer layers and the inner layers with plated through holes or vias. Laminates used to fabricate multilayer PCBs are nearly all composites of woven glass cloth and one of several resin systems. The resin system is chosen to satisfy requirements such as high temperature operation, dielectric loss, dielectric constant, cost and the ability to withstand high humidity or harsh environments such as space or down oil wells.

17.2.3 Flexible Circuits

These circuits are made by laminating copper foil to one or both sides of a flexible substrate such as Kapton® or Kevlar®. They can range from a single conductor layer to multiple layers. They are most often used to replace a wire harness with a flat circuit to save weight and space. Common applications include cell phones, video cameras disc drives and avionics.

17.2.4 Flexible Rigid or Flex-rigid

As the name suggests, these are combinations of flexible circuits and rigid PCBs in a single unit. The flexible portion of the assembly is made first and included in the lamination process of the rigid portion. This process eliminates wiring harnesses associated with connecting PCBs to connectors. The principal applications of this method are aerospace and military electronics where weight and reliability are major concerns.

17.2.5 Backplanes

Backplanes are special cases of multilayer PCBs. In general, the contain large numbers of connectors into which are plugged daughter cards. In most cases, these connectors are press fit into the holes in the back plane as opposed to soldering the pins into the holes. As a result, these PCBs do not get exposed to the high temperatures of soldering and can be much thicker without concern that the plated through holes might fail to *z*-axis expansion.

Most of the backplanes in use at the present time are part of very large routers and switches that are in the backbone of the Internet or server farms. Demands for very high data path bandwidth have driven the signal speeds on these backplanes to as high as 28 Gb/s. At these speeds, the

parasitic capacitance of the plated through holes required by the press fit connectors can degrade performance. As a result, these backplanes are often fabricated by back drilling away the unwanted portions of these plated through holes, further complicating the fabrication process.

Another problem that is encountered with these very high speed backplanes is signal degradation due to the nature of the glass weave used in the laminates as well as loss in the copper due to surface roughness. These will be discussed in the materials section of this chapter.

17.2.6 Buildup Double-Sided PCBs

Buildup PCBs are PCBs that have a multilayer core made using the multilayer fabrication process. Additional layers are added to this core by laminating material to the outside and then connecting circuits on these new outside layers to the inner core using laser drilled or chemically etched blind vias. Figure 17.3 is cross section of a buildup PCB with a six-layer core that has two outside layers added showing the laser drilled blind vias connecting the added layers to the inner core resulting in an eight layer PCB.

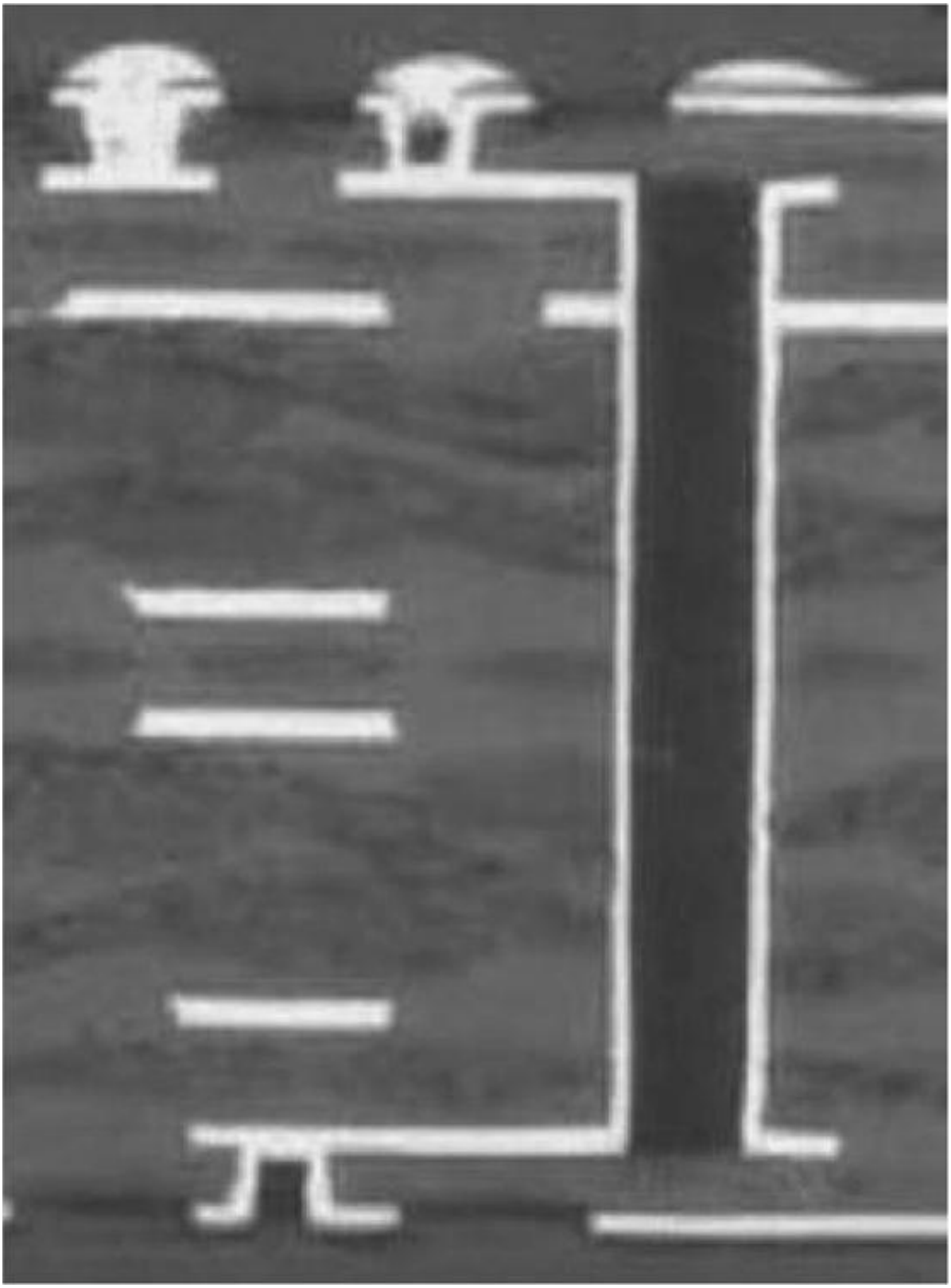


FIGURE 17.3 Cross section of a buildup PCB with a six-layer core and two buildup outer layers.

Clearly, creating an eight layer PCB using this method results in a more expensive assembly than if the eight layers were all created in the assembly process that created the six layer core. The reason that buildup technology is used is to allow components to be mounted on both sides of the PCB so densely that the component leads cannot be connected to internal circuits with through hole vias. This fabrication method is the backbone of products such as cell phones that would not be possible in their current size without it. A second market for buildup PCBs is the multilayer substrates of very high pin count ball grid arrays (BGAs) such as field-programmable gate arrays (FPGAs).

It is common to design buildup PCBs with as many as three buildup layers added to each side of the core.

17.2.7 Multichip Modules

Prior to the recent advances made in integrated circuit manufacturing it was necessary to fabricate analog, RF and digital integrated circuits as different ICs. When a product required a combination of these, they were often mounted as bare integrated circuits in a multichip module. It is now possible to design integrated circuits so that all of these functions are on a single IC. As a result, the need for multichip modules has all but vanished.

17.3 METHODS OF ATTACHING COMPONENTS

A wide range of methods has evolved for attaching components to PCBs. The methods chosen as well as the combinations of methods chosen for a product have a substantial impact on the final cost, ease of assembly,

availability of components, ease of test, and ease of rework. The five basic attachment combinations are: through-hole only, through-hole mixed with surface-mount on one side, surface-mount one side only, surface-mount both sides, and surface-mount both sides with through-hole.

17.3.1 Through Hole Only

All component leads attach to the PCB by being inserted into holes that pass through the PCB. The components may be secured by wave soldering or by pressing into holes that result in an interference fit (press fit). Assembly involves a component placement operation followed by a wave-soldering operation. This method is still the workhorse of the low-cost consumer electronics industry.

17.3.2 Surface Mount Only-Single Sided

This type of package is made up of only surface-mount parts all mounted on the same side of the PCB. Assembly is a one-step process that involves placing all components and soldering them in place using some form of solder reflow.

17.3.3 Surface Mount Only-Both Sides

This type of package contains surface-mount components on both sides. Assembly is a two-step process that involves placing all components on one side and reflow soldering them, followed by placing all components on the other side and reflow soldering them. In addition to more complex assembly operations, designing and testing this type of

assembly is much more complex, as parts often share the same area on opposite sides of the PCB, causing conflicts when trying to locate vias and test points.

17.3.4 Press Fit with Combinations of Above Methods

Components such as connectors and PGAs are attached to the PCB with through-hole technology. All other components are mounted using surface-mount packages. This is the most common method used to assemble electronics products. Assembly is a two-step process that involves placing all surface-mount parts and soldering them in place with a solder reflow system, then inserting all through-hole parts and soldering them in place in a wave-soldering operation. Alternatively, the through-holes may be hand-soldered if the quantity is small.

17.4 COMPONENT PACKAGE TYPES

17.4.1 Introduction

Over time, a wide assortment of packages has been developed to house components. Selecting the correct package type for each component is one of the most important parts of the design process. Package types chosen affect ease of design, assembly, test, and rework, as well as product cost and component availability.

17.4.2 Through Hole–Solder

This class of component is characterized by parts that have wire or formed leads. These leads pass through holes drilled

or punched in the PCB and are soldered to lands on the back side or to plating in the holes. This is the original package type used for electronic components. A major benefit of through-hole components is the fact that every component lead passes all the way through the PCB. Because of this, there is automatic access to any PCB layer to make connections. Further, every lead is available on the bottom of the PCB, so test tooling is easy to construct. With the advent of surface-mount components, through-hole is used primarily for connectors and pluggable devices such as microprocessors mounted in PGA packages.

Through-hole packages are often preferred for ICs and other components that dissipate large amounts of heat, because of the relative ease with which heat-sinking devices can be fitted to them. In addition, it is much easier to provide a socket for a through-hole device. This eases the task of changing programmable parts and microprocessors when it is necessary to upgrade a system.

> *Caution:* Integrated circuits in through-hole packages are becoming difficult to find as they are displaced by surface-mount equivalents and should be avoided in new designs unless a secure supply of components is available for the production life of the design.

17.4.3 Surface Mount

This package type is the mainstream choice for packaging electronic components of every type, including connectors. Its principle characteristic is that all connections between a component lead and the PCB or substrate is made with a lap joint to a pad on the surface of the PCB. This has both advantages and disadvantages. On the advantage side, since there are no holes piercing the PCB, wiring space on inner layers and on the reverse side is not consumed with

component lead holes. Because of this, it is usually possible to wire a PCB in fewer layers than would be true with through-hole parts. Another and larger benefit is the fact that surface-mount components are always smaller than their through-hole equivalent, making it possible to fit more parts in a given area.

The main disadvantages of surface-mount components stem from the fact that there are no leads to easily grip with instrumentation probes and that there may not be access to the leads from the reverse side for purposes of production testing. This gives rise to the need to add a test pad to most nets on the back side in order to perform production test. It also gives rise to the need for very expensive, complex adapters in order to provide access to leads on processors and other complex devices to probe their inputs and outputs when performing diagnostic work.

Yet another disadvantage of surface-mount parts stems from their small size. It is more difficult to remove heat from SMT packages than it is for their through-hole equivalent. In some cases, such as high-performance processors, the heat generated by the IC is too high to permit proper operation in an SMT package.

17.4.3.1 Fine Pitch Leaded. Fine pitch is a special class of surface-mount components. This class is characterized by lead pitches lower than 0.65 mm (25 mils). These fine lead pitches are usually driven by very high lead count ASICs (160 pins and up) or by the extreme miniaturization requirements of PCM-CIA (Personal Computer Memory Card Industry Association) cards, PDAs (personal digital assistants), and other small, high-performance products. The motivation for designating a special fine-pitch-component class of surface-mount parts is the extra difficulty of successfully testing, assembling, and reworking these parts on PCBs, as well as in building PCBs with accurately formed patterns and solder masks to mate with the leads of fine-pitch parts. Fine-pitch

parts are the source of most manufacturing defects in a well-run SMT assembly line. The defects stem from lack of coplanarity of the leads, bent leads, insufficient solder on the joints, and poor alignment of the leads to the patterns on the PCB.

Successful manufacture using fine-pitch components involves very tight cooperation among the PCB designer, the PCB fabricator, the component manufacturer, and the PCB assembler/tester. It almost always involves specialized assembly, test, and rework tooling. Design is most often done by convening a series of meetings of the engineering personnel of all these groups to evolve a set of rules, processes, equipment, tooling, and components. These meetings need to start at the product development stage and continue to be held until the proper pad shapes and sizes have been established and the production process is stable.

17.4.3.2 Ball Grid Arrays. BGA is a relatively new technology that is a cross between pin grid arrays and surface-mount. High-pin-count IC die are mounted on a multilayer substrate made from ceramic or organic material. The die are connected to the substrate using standard wire-bond techniques and encapsulated in epoxy or another form of cover. The bottom side of the substrate contains an array of high-melting-point solder balls which connect to the wire-bond pads through the multilayer substrate. These balls mate with a matching array of pads on the PCB and are reflow soldered during the same operation as all other surface-mount parts. (See Fig. 13.11.)

The appeal of BGA technology is as an alternative to high-pin-count, fine-pitch SMT ICs. As mentioned earlier, assembling high-pin-count, fine-pitch SMT parts is very difficult, owing to the fragile nature of the component leads. BGAs represent a much more robust package during component-level test and during assembly.

As with most technologies, there are some disadvantages to BGAs. Among these are

- The solder joints are hidden from view, so inspecting them requires x-rays.
- The solder joints are not accessible for rework, so the soldering process must have a very high success rate.
- Part removal requires special tooling.
- The pattern on the PCB surface is an array of pads that require one via each all the way through the PCB, hampering routing.
- All component leads are concentrated in a much smaller area than the equivalent part in a fine-pitch SMT package. This concentrates the wiring in a small area pierced with many vias. As a result, the BGA PCB will likely have more wiring layers than the equivalent SMT PCB.
- The BGA package is more expensive than the equivalent fine-pitch SMT package, by as much as three times.

17.4.3.3 Flip-Chip ICs. Flip-chip technology involves plating raised pillars of metal on the bonding pads of ICs, turning them upside down, and attaching them to a matching pattern on a substrate. The substrates are most often silicon and precision ceramics. From this description, it can be seen that this is a very specialized packaging method. To succeed, a source of tested good bare die with plated-on pillars must be available. This situation occurs almost exclusively in very high performance supercomputers where the ICs have been specially designed for the application or in very high volume applications such as pagers and cellular phones.

17.4.3.4 Wire Bonded Bare Die. As the name implies, this method of assembly involves attaching bare IC die directly to a substrate using an adhesive or reflowing solder and connecting the bonding pads to pads on the PCB using

wire-bond techniques. Virtually all digital watches and many other similar consumer products use this assembly technique. It is very inexpensive when used in very high volume products with only a single IC to connect.

17.5 MATERIALS CHOICES

17.5.1 Introduction

The combination of lead-free soldering requirements and the ever increasing frequencies of signals traveling across laminates have resulted in a whole series of new laminate systems that far outperform those that have been in use since the start of PCB fabrication.

17.5.2 Polyimide Systems

Polyimide-based laminate systems were the work horse of applications that required the ability to withstand high operating temperatures and the stress of rework. This is the primary advantage of this resin system. Its disadvantages include more difficult lamination processes, costlier laminate costs and the tendency to absorb enough moisture that an assembly would fail leakage tests unless it was backed dry and coated with a material that served to water proof it. Development in laminate systems have created alternatives that do not have these disadvantages. New designs should not be done using polyimide for these reasons.

17.6 FABRICATION METHODS

A wide variety of fabrication methods has been developed to meet the needs of the electronics industry. The following descriptions are quick summaries of each method intended to acquaint the reader with their advantages and disadvantages and likely applications. Detailed treatments are presented elsewhere in this book.

17.6.1 Punch Forming

Punch forming is used in the manufacture of very low cost, single-sided PCBs such as are used in many consumer electronic products. The process involves printing and etching the conductor patterns on one side of a laminate substrate, usually paper-reinforced epoxy. All holes are punched in a single stroke by a die containing a pin and opening for each hole. The PCB outline is formed in a second die that “blanks” it from the panel in which it is processed.

Often, several PCBs will be contained in a single panel sized to travel through the assembly process. After a PCB is punched out of the panel, it is forced back into the vacant hole and is held in place by interlocking fibers along the edges of the PCB. After assembly and testing is complete, each PCB is pressed from the panel. This is known as *crackerboarding* and is aimed at reducing overall manufacturing costs.

17.6.2 Roll Forming

Roll forming is a process used to manufacture flexible circuits in very large quantities. This is the lowest-cost method for the manufacture of flexible circuits. However, it involves substantial tooling, so it is applicable only for very high volume products. Examples of PCBs manufactured using this method are printer head connections, disk drive head

connections, and the circuits used in cameras and camcorders. The PCBs can be single-or double-sided.

Roll forming resembles newspaper printing in that the process starts with a large roll of copper-clad laminate that is fed through a long process line containing stations which perform each operation on a continuous basis, starting with printing the conductor pattern, etching it, forming the holes, testing, and blanking from the roll itself. The process can include lamination of a cover insulator layer over the conductors as well.

CHAPTER 18

ELECTRONIC DESIGN AUTOMATION AND PRINTED CIRCUIT DESIGN TOOLS

Andy Shaughnessy
Managing Editor, The PCB Design Magazine *and* PCB Design 007, *Seaside, Oregon*

18.1 DESCRIPTION OF PCB DESIGN TOOLS

Electronic design automation (EDA) software tools are used to design printed circuit boards (PCBs), integrated circuits (ICs), and electronic systems. For our purposes, we're primarily concerned with the tools used to design PCBs.

In a nutshell, PCB design software tools are used to turn the concept for a PCB into a finished design, in a data format that manufacturers can use to fabricate and assemble the final PCB.

These are typically Windows-based tools, though a few are native Mac or Linux systems. The tools are built around a

group of software algorithms, detailed sequences of actions that can be used to perform certain tasks. Because algorithms are sequential, processes such as autorouting and simulation can take hours to perform. Graphic processing units (GPUs), made up of hundreds of simple processors, are sometimes used to accelerate specific algorithms.

The underlying code for many of today's PCB design tools was written in the 1990s, and the original code remains. But tool vendors have been updating the software ever since, particularly the graphical user interface (GUI), because of growing demand by PCB designers for more user-friendly systems.

PCB design software tools run the gamut, from free tools that can be used to design simple single-sided boards, to midrange tools in the $10,000 to $20,000 price point, all the way up to enterprise-level tools that cost well over $100,000, not including 15 percent per year for maintenance support.

The free and lower-cost design tools are typically used by do-it-yourselfers and designers of lower-technology PCBs, and they don't have many extra features. Some of these are open-source tools that will never be adopted by a corporation because of security concerns. But the high-end design software suites boast all of the "bells and whistles." Features such as constraint management, DFM functionality, concurrent design, parts library management, and signal integrity and EMC analysis are often integrated into these tools, which are used to design the most complex high-speed PCBs.

PCB design tools have become almost universally modular, allowing customers to purchase only the exact functionality required by the complexity of their PCB designs. For instance, not all companies need the concurrent design function, which allows more than one designer to work on a design simultaneously. But this functionality is critical for larger companies that have design teams working around the clock, and around the globe. See Fig. 18.1.

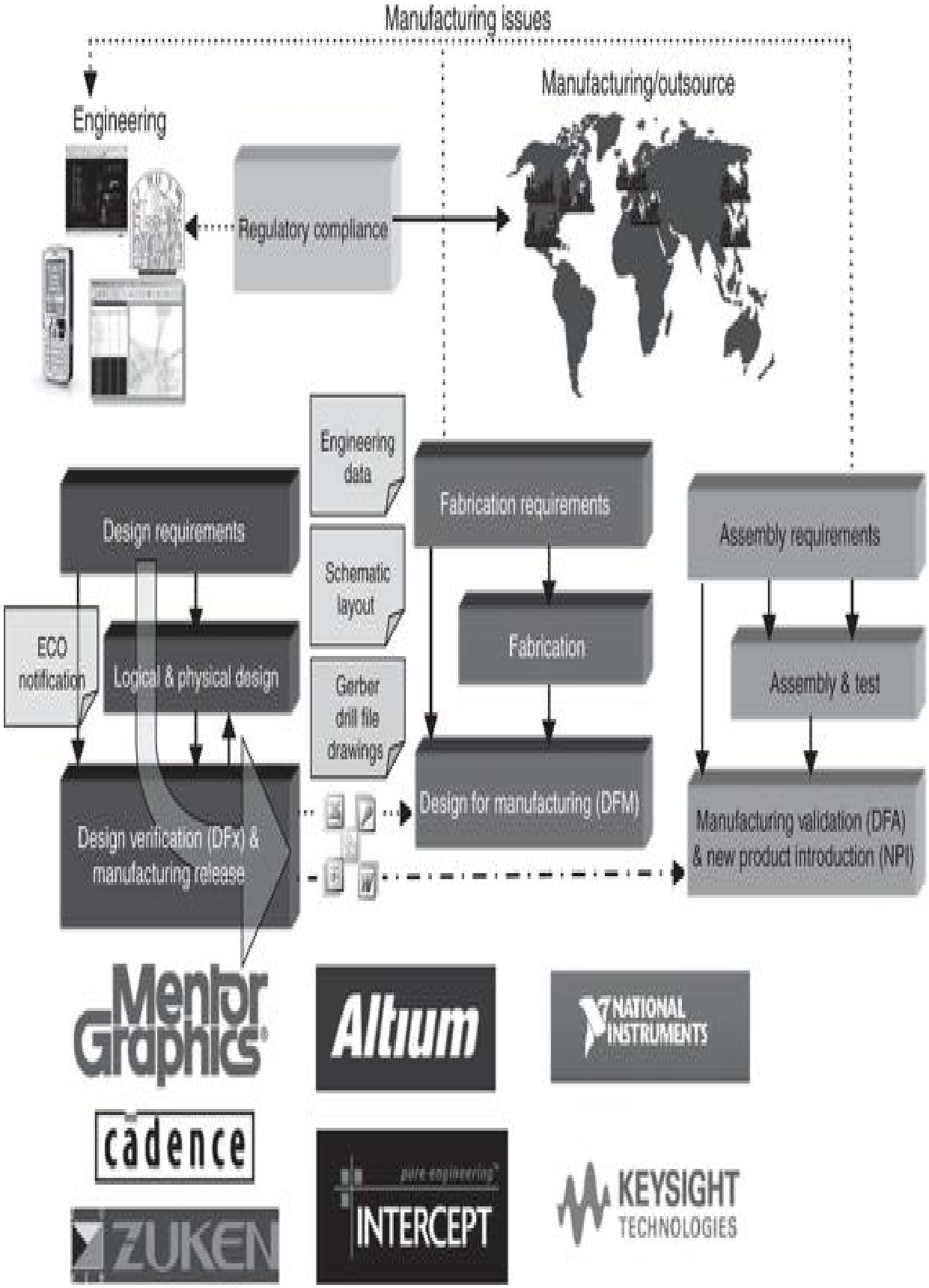

Manufacturing issues
Engineering
Manufacturing/outsource
Regulatory compliance
Engineering data
Design requirements
Fabrication requirements
Assembly requirements
Schematic layout
ECO notification
Logical & physical design
Fabrication
Assembly & test
Gerber drill file drawings
Design for manufacturing (DFM)
Design verification (DFx) & manufacturing release
Manufacturing validation (DFA) & new product introduction (NPI)
Mentor Graphics
Altium
NATIONAL INSTRUMENTS
cadence
pure engineering
INTERCEPT
KEYSIGHT TECHNOLOGIES
ZUKEN

FIGURE 18.1 The process of designing, fabricating, and assembling a PCB may take place across several continents. (*Courtesy of Happy Holden*.)

PCB designers now find themselves working in disciplines that were once firmly in the engineers' realm, such as thermal management, electromagnetic compatibility (EMC), signal integrity, and power integrity. Today, even some of the low-cost EDA vendors are integrating signal integrity capabilities into their tool flows.

18.2 USING PCB DESIGN TOOLS

18.2.1 Schematic Capture Tools

The design process begins when an engineer decides which components must go on the board, and he/she creates a schematic. The schematic can be created with a schematic capture toolwhich is often included in the PCB layout tool platform. This tool has made hand-drawn schematics nearly obsolete.

The advent of modern schematic capture tools has also all but eliminated the need to create a "breadboard" or protoboard before beginning a design. Tools now allow schematics to be created concurrently with the PCB layout. Simulation of the circuit sometimes begins at this early stage.

The design of the entire circuit board is contained in the finished schematic file, which is converted into a netlist. The netlist contains all of the interconnectivity information for the PCB—all of the component footprints, pins and the nets (or nodes) that connect to each pin. The electrical engineer hands off this netlist to the PCB designer.

18.2.2 PCB Layout Tools

The designer loads the netlist into the PCB layout tool. These tools no longer just “connect the dots.” Modern PCB layout software tools prompt users to select the number of layers required, units of measurement (metric or imperial), design constraints, default sizes of copper traces, vias, and clearance, and much more. These tools have become increasingly automated over time.

18.2.2.1 Autorouting. The designer places land patterns (footprints) of critical components and circuits; USB connectors, for instance, must be on the board’s edge for accessibility, while other parts may need to be close to the power source. The rest of the components can then be placed. Many design tools offer advances such as interactive placement replication for components and circuits that are used frequently. Tools often come loaded with components libraries that feature footprints of the most commonly used parts, which minimizes or eliminates the time designers must spend searching third-party sites for components.

After all of the parts are placed, the designer can begin routing the copper traces that will connect the various components. The layout tool’s autorouter software, will take a fraction of the time required for hand-routing but usually only connects about 80 per cent of the nets, with the remaining 20 percent being hand-routed.

On multilayer boards, routing is more complicated because the signal travels from one layer to the next through copper-plated through-holes known as vias. But vias can be routed by hand or with any of today’s autorouters.

18.2.2.2 Design Rules Check. After routing is finished and the board is cleaned up, the designer then checks for errors. Most PCB design tools include a design rules check (DRC) that checks the whole PCB for errors, such as traces that touch, holes that are too small, etc.

18.2.2.3 Data Transfer. During postprocessing the design file is translated intoa data transfer format that PCB manufacturers can use to fabricate and assemble the board. For decades, the majority of PCB designs have been output in Gerber, a machine control language (now owned by Ucamco) that was never intended for this task. As such, Gerbers don't contain all of the information the fabricator needs, so the designer must also send the fabricator separate NC (numerical control) drill files and other documentation.

Relative newcomers ODB++ and IPC-2581are single-file formats which contain all of the information necessary to fabricate and assemblea PCB. ODB++ is owned by Mentor Graphics; IPC-2581 is vendor-neutral. Some OEMs handoff design data in more than one format, but despite its limitations, Gerber is still the most popular data transfer format.

18.2.3 Signal Integrity and EMI/EMC Software Tools

Signal integrity simulation and analysis software tools are relative newcomers to the PCB design community. Until the late 1990s, most PCB designers didn't worry much about signal integrity. Rise times (the time required for a signal to rise from 10 to 90 percent of its final value) were not fast enough to be a problem on most boards. But with today'sincreased rise times and clock speeds, even short traces can become victims of crosstalk, ringing, and ground bounce.

Signal integrity tools allow the user to calculate atiming budget and address impedance mismatches, which contribute to reflections and crosstalk. Now, signal integrity tools provide pre-layout and postlayout simulations, often bundled into the design tool itself, so the designer can begin

simulating circuitsat the schematic level before committing to the final design. These tools can help designers avoid SI problems early in the process by choosing, for instance, the best layer stackup for the board.

Similarly, electromagnetic interference (EMI) was not much of a challenge until fairly recently. EMI on a PCB generally refers to the radiated emissions that emanate from wires, cables, or other parts of the board that serve as unintended antennas. These emissions may interfere with otherelectronic devices, which is frowned upon by the Federal Communications Commission and other regulatory organizations around the globe.

EMI tools include electromagnetic field solvers and circuit solvers. These tools are used to simulate the EMI behavior of rise and fall times, clock frequencies, andswitching rates, across the system’s frequency range. These often-pricey tools allow designers and engineers to make tradeoffs between the drive for EMC and budget-straining design constraints. As is the case with signal integrity, potential EMI challenges are best addressed as early in the design cycle as possible. EMI can keep your end-product from reaching the marketplace if the PCB or system fails the electromagnetic compliance (EMC) testing required by the FCC.

18.3 MAJOR PCB DESIGN TOOLS

The major PCB design software tools are used by global OEMs to design complex PCBs for the most sophisticated electronic products. Some of these enterprise-level tools offer capabilities for multiboard and system design, along with concurrent design and partitioning for companies with geographically diverse design teams. Many of these tools have a fairly steep learning curve. The enterprise-level EDA tool vendors are primarily publically traded companies.

18.3.1 Mentor Graphics—Xpedition and PADS

18.3.1.1 Xpedition. Mentor Graphics acquired Xpedition when Mentor merged with VeriBest in 1999. Formerly known as Expedition, the expanded Xpedition Enterprise platform includes everything from schematic capture through DFM tools. (Mentor also offers the Xpedition Package Integratorplatform for IC packaging teams). Xpedition is a complete integrated design flow platform. It shares a common constraint definition between schematic capture and layout. Features include design data management, an integratedplace-and-route editing environment, interactive sketch routing, and an RF module; it can handle embedded passives, microvias, and flex designs. Xpedition supports concurrent team layout and MCAD collaboration, and is integrated with Valor's DFM flow, including DFF analysis rules. The HyperLynx signal and power integrity tool is integrated into Xpedition. See Fig. 18.2.

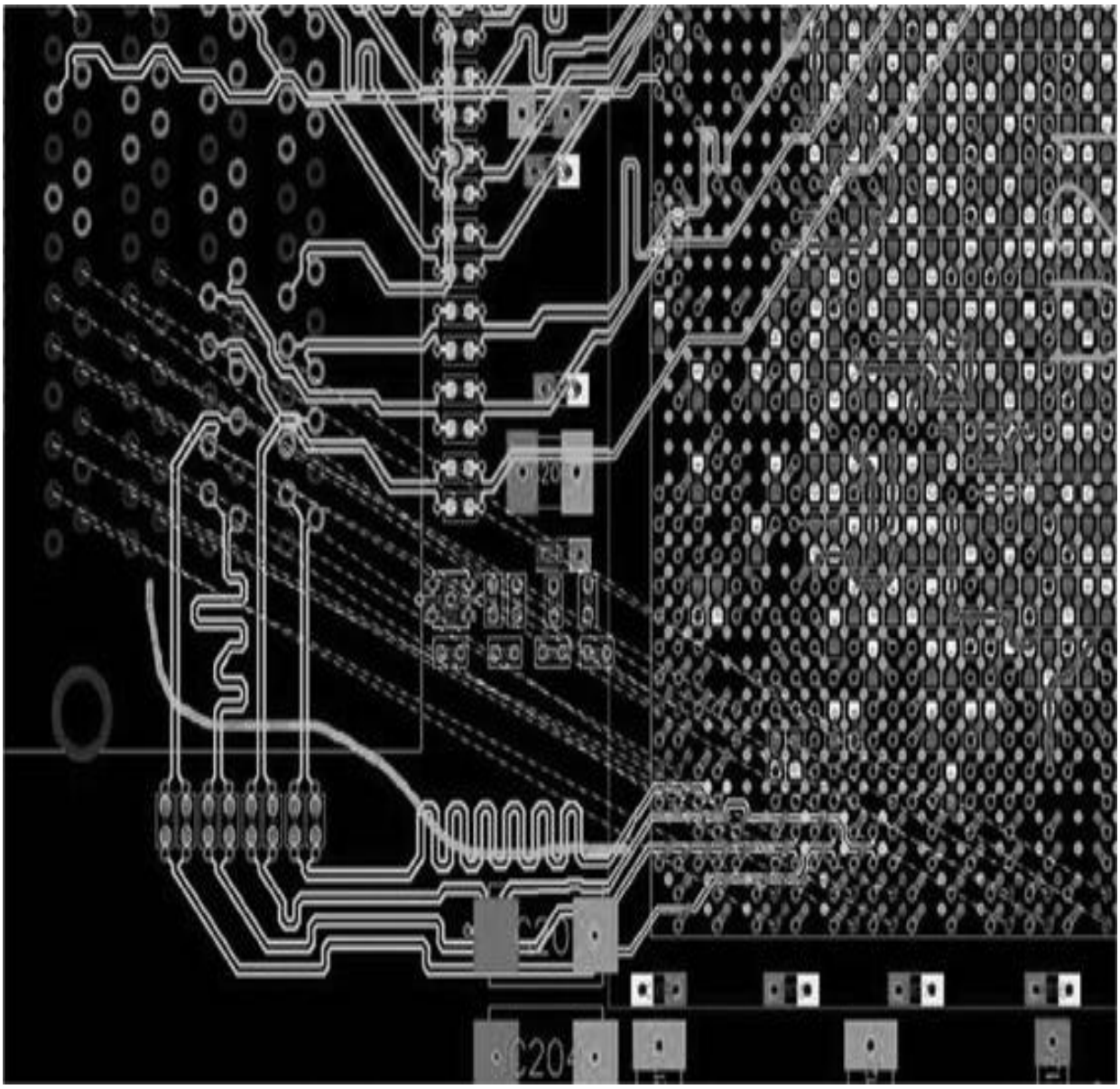


FIGURE 18.2 A screen shot of a PCB design created with Mentor Graphics' Xpedition. (*Courtesy of Mentor Graphics*.)

18.3.1.2 PADS. PADS Software was founded in 1977 by industry icon Gene Marsh, who was also involved in the early years of Racal-Redac. Now part of Mentor Graphics after a series of mergers, the PADS design software tool is still beloved by longtime users for its user-friendliness.

Not quite as sophisticated as Xpedition, PADS can still handle complex designs, though it offers fewer features and options than its big brother. PADS is known for its fairly quick

learning curve, and it's one of the most widely used PCB layout tools today. PADS includes schematic design, library management, constraint management, pre- and postlayout signal integrity analysis, and ECAD-MCAD collaboration tools. The layout tool features push-and-shove route editing, design reuse, cross-probing between schematic and layout, and it supports RF, differential pairs, nested vias, and virtual nets.

18.3.2 Cadence Design Systems—Allegro and OrCAD

18.3.2.1 Allegro. Cadence Design System's Allegro suite was developed to handle the most complex high-speed designs. The Allegro platform includes tools for simulation, design authoring, design publishing, FPGA-PCB co-design tools, and signal and power integrity tools (from the acquisition of SI tool company Sigrity).

Allegro PCB Designer is a scalable constraint-driven design environment. It includes a front-to-back constraint management tool and a complete placement and routing environment with placement replication, advanced interconnect planning, and signal and power integrity simulation. Design tool features real-time plowing/healing with dynamic shape technology, interactive push/shove etch editing, RF/analog and mixed-signal design, interactive floorplanning, hierarchical route planning, and design partitioning.

18.3.2.2 OrCAD. OrCAD Systems Corporation was founded in Hillsboro, Oregon in 1985, developing a line of tools for PCB layout, verification and simulation, and FPGA design. The company gained a PCB layout tool and autorouter from its acquisition of Massteck in 1995, and the PSpice simulation tool from its merger with MicroSim in

1997. OrCAD went public in 1996 and was itself acquired by Cadence in 1999.

The OrCAD lineup includes a variety of design tools, from the free OrCAD Lite through the OrCAD PCB SI signal integrity simulation tool. OrCAD PCB Designer Professional features placement and circuit replication, differential pair simulation and routing support, interactive floorplanning, blind and buried via support, a schematic part and library editor, and pre- and postroute signal integrity analysis. A variety of apps are available for OrCAD. The OrCAD Capture schematic capture tool remains a favorite in the design world, even among designers who use competing tools for PCB layout.

18.3.3 Zuken—CR-5000, CR-8000, and CADSTAR

18.3.3.1 CR-5000. CR-5000 is Zuken's most advanced design software for single board design. Features include concurrent PCB and FPGA design, constraint-driven design with DFM verification, support for design variants and version control, circuit rules check, and EMC, signal and power integrity analysis. The Dragon autorouter was designed to reduce the set-up time required by some autorouters. It generates routing strategies based on checks run by its "routing consultant." The router is optimized for high-performance, high-density routing, and routes differential pairs to reduce skew and uncoupled length.

18.3.3.2 CR-8000. CR-8000 is a system-level, multiboard product-centric design tool built from the core of CR-5000. But CR-8000 allows users to design the whole product, as well as multiple PCBs. CR-8000 adds Design Force, a native 3D graphics tool offering improved product visualization to help designers see the impact of changes upon the final

product. It comes equipped with a tablet for two-handed design, allowing users to pan and zoom with the tablet in one hand while working with a mouse in the other.

18.3.3.3 CADSTAR. CADSTAR started out as more of an entry-level layout environment, but over the years it hasacquired some of the features of its big brothers. Developed for single PCBs, CADSTAR now offers a complete flow from schematic to output, with 3D mechanical integration, signal integrity simulation, power integrity analysis. CADSTAR's place-and-route editor has a grid-free, spatial data structure and rules-driven architecture. It is also available in a free version.

18.3.4 Altium—Altium Designer

Altium's PCB design tools reside on the lower end of the price-point scale, but they manage to offer some capabilities normally seen in higher-end rival tool sets. Its ECAD-MCAD integration permits users to import 3D STEP models directly into the PCB design environment. Altium Designer can handle high-speed, mixed-signal PCBs, and features design verification, validation, and reuse capabilities. It has a unified schematic and PCB design tool, with native 3D modeling, and it's optimized for rigid-flex design as well.

18.3.5 Intercept Technology—Pantheon

Intercept Technology began in 1983 as an R&D company, and moved into EDA by developing CAD translators. Intercept offers a full range of PCB, RF, and hybrid design tools. The Pantheon layout tool was introduced in early 1996 and underwent a full GUI update in 2011. It offers a 3D

design environment, auto-interactive routing, concurrent design capabilities, and DFM verification through design rule checks, engineering rule checks, and manufacturing rule checks.

18.3.6 Keysight Technologies (Formerly Agilent EEsof)—EDA ADS

Agilent, itself a Hewlett-Packard spinoff, spun off its electronics measurement and EDA businesses as Keysight Technologies. Keysight's EEsof EDA Advanced Design System is an RF, microwave and high-speed design environment targeted at wireless communications, networking, and mil-aero companies. ADS offers schematic, layout, electro-thermal co-simulation, X-parameter model generation, and three full-wave, native 3D electromagnetic technologies for laminate/PCB, IC, package, and 3D EM co-design.

18.3.7 National Instruments—Ultiboard and Multisim

The Ultiboard layout tool and Multisim schematic capture tool were developed by the Canadian company Electronics Workbench, which National Instruments acquired in 2005. Multisim was soon integrated with NI's existing LabVIEW graphical programming platform. Primarily aimed at the education market, Ultiboard and Multisim are also available in professional-level packages for PCB designers and researchers.

18.4 LOWER-COST PCB DESIGN TOOLS

These desktop-level design tools offer some of the capabilities of their enterprise-level cousins, but at a fraction of the cost. Usually developed by private companies, these layout tools are a favorite of the “do-it-yourself” and hobbyist communities, but some are even used by PCB designers at the corporate level. These tools don’t typically offer higher-end capabilities such as HDI (high-density interconnect), concurrent design, or multiboard design, but the learning curve is minimal.

18.4.1 Labcenter Electronics—Proteus

Labcenter’s Proteus PCB design platform offers a variety of capabilities, with prices for some packages starting at several hundred dollars. Features include schematic capture, PCB layout, SPICE simulation, a shape-based autorouter, design/connectivity rule checking, and 3D visualization.

18.4.2 CadSoft—Eagle

CadSoft’s Eagle PCB design tool serves both the professional and teaching communities, with prices starting under $100. Eagle (Easily Applicable Graphic Layout Editor) features a schematic editor, layout editor, and an integrated design rules-driven autorouter with ripup-and-retry. Eagle is also popular withthe DIY audience, in part due to its availability in Linux. Also available in a free package for hobbyists and students.

18.4.3 Westdev Ltd.—Pulsonix and Easy-PC

18.4.3.1 Pulsonix. Pulsonix is an integrated schematic capture and PCB design editor. It includes an autorouter, SPICE-based simulation, hierarchical schematics, via stitching, chip-on-board capabilities, the ability to add fanouts to existing BGA footprints, and differential pair broadside coupled pairs. Pulsonix also supports blind and buried vias, embedded components, and rigid-flex designs.

18.4.3.2 Easy-PC. Easy-PC includes some of the capabilities of Pulsonix, but it's targeted more at the educational and hobbyist markets, and at a reduced price point. Features include a bill of materials composer, online DRC, SPICE simulation, integrated autorouter and placement, forward and backward annotation, and cross-probing between schematic and PCB layout.

18.4.4 DEX2020—AutoTRAX

AutoTRAX is the brainchild of one man, Iliya Kovac, who developed the entire design tool himself. Built on an open-format XML file structure, it features schematic capture, PCB layout, a hierarchical project manager, and design reuse capabilities.

18.4.5 Visionics—EDWinXP

Visionics, a subsidiary of Norlinvest Ltd., offers a range of software tools, from EDA to documentation and programming. The EDWinXP design tool features a schematic editor, mixed-mode and SPICE simulation, PCB layout editor, fabrication manager, EM analyzer, 3D library editor, automatic component placement, autorouter, and design rules checking.

18.4.6 IBF—TARGET 3001

TARGET 3001 is a descendant of the company's RULE layout tool, a DOS program released in 1989 and adopted by European hobbyists. TARGET 3001 features SPICE-based simulation, 3D viewing, an autorouter, and a component management system. It supports rigid-flex, chip-on-board technology, assembly variations, and RoHS-compliant design. Toyota used TARGET 3001 to design cable harnesses in their Formula 1 car.

18.4.7 Novarm—DipTrace

Novarm was founded in 2002 by engineering graduates of Ukraine's National Mining University. The DipTrace PCB design suite includes features such as cross-module library management, STEP and IGES 3D import/export, real-time design rules check, shape-based autorouter with support for third-party routers, 3D modeling, and a newly revamped GUI.

18.5 FREE PCB DESIGN TOOLS

Free PCB design tools comprise one of the most interesting segments in EDA tools. It's easy to see why this group continues to grow: Most hobbyists and do-it-yourselfers do not want, or need, to purchase a full-featured PCB design tool, and many PCBs still have fewer than 10 layers. Some of these are proprietary tools offered by fabricators as value-adds to draw manufacturing business; others are developed by open-source software groups, with thousands of members offering feedback. This segment is worth watching.

18.5.1 Altium—CircuitMaker

CircuitMaker is Altium’s big move into the free and low-cost PCB design software market, and some users find it has much of the feel of the full-featured Altium design tools. The free extensible base programincludes 3D design and analysis, and add-ons are available at a cost. Users can collaborate online and comment on designs in real time, and designs are saved to the cloud.

18.5.2 Sunstone Circuits—PCB123

Introduced by Sunstone Circuits in 2002 as value-add to its prototype fabrication business, PCB123 has developed into a full-featured PCB layout tool. It was developed to create designs specifically for Sunstone to build, so PCB123 won’t output a Gerber file that you can take to another fabricator. It provides real-time quotes for parts and fabrication during design, and Sunstone guarantees on-time shipping for orders created with PCB123.

18.5.3 ExpressPCB

ExpressPCB is a prototype manufacturer, and it’s also the name of the company’s free PCB design software. ExpressPCB software includes the ExpressSCH schematic tool, and it allows users to design a two-layer or four-layer PCB, with instant quotes available when the design is finished. Designers can order PCBs directly from the ExpressPCB program.

18.5.4 Advanced Circuits—PCB Artist

PCB Artist is a free PCB design program operated by quickturn fabricator Advanced Circuits. PCB Artist is equipped with a schematic tool, PCB layout tool, backward/forward design integration, autoplacement, single-sided autorouting, DRC error reports, and improved copper pour.

18.5.5 KiCad—EDA Software Suite

KiCad is an open-source PCB design software suite. It runs on FreeBSD, Linux, Windows, and Mac OS X. It works with a variety of component libraries, and can import components from other EDA tools. KiCad includes features such as schematic capture, a PCB layout editor, an autorouter, and 3D viewer.

18.5.6 RS Components—DesignSpark PCB

DesignSpark PCB is a free PCB layout tool available through RS Components and Allied Electronics. The program displays an advertisement each time the program is restarted. It can design PCBs up to 1 sq. m in size. Comes equipped with schematic capture, PCB layout editor, and autorouter. DesignSpark PCB can generate a bill of materials automatically, and it currently boasts over 200,000 users.

18.5.7 ZenitPCB—ZenitPCB Layout

ZenitPCB is freeware for personal or semi-professional use on single- and double-sided PCBs up to 800 pins. It allows hobbyists to import a netlist file from other schematic capture programs such as OrCAD, PADS, Multisim, or Eagle.

Features schematic capture, a PCB layout tool, an online DRC, and a component library with over 1000 footprints.

18.5.8 Osmond—OsmondPCB

OsmondPCB design software is available only for Mac users. It’s free for users creating designs with fewer than 700 pins, with an inexpensive license required to output Gerber files for designs above 700 pins. Allows designers to work in metric or imperial units, and is compatible with DesignWorks’ schematic capture.

18.5.9 gEDA—gEDA PCB

The gEDA project was launched in 1998. The group has created a full, open-source suite of free EDA tools for electrical circuit design, schematic capture, analog and digital simulation, and PCB layout. Each tool is independent of the rest, and some have been developed into more full-featured tools than the others.

18.5.10 Fritzing—PCB View

Fritzing is a publically funded, open-source software group that supports PCB designs up to two layers, primarily for hobbyists. With Fritzing, designers can take a simple breadboard circuit, copy it into the program, and then create a schematic and PCB artwork. Fritzing permits manual routing and autorouting, generates a bill of materials, and can export Gerber files or etchable PDFs for DIY production.

18.5.11 EasyEDA—EasyEDA Editor

Developed by a self-described “tiny hackers team,” EasyEDA is a free Web-based EDA suite. It integrates schematic capture, PCB layout, and SPICE simulation. Because it’s Web-based, there’s no installation involved, and all data resides in the cloud. EasyEDA is integrated with the DangerousPrototypes open-source parts libraries.

18.6 SIGNAL INTEGRITY AND EMC TOOLS

These third-party simulation and analysis tools are primarily targeted at global electronics OEMs. (The major PCB tool companies have all integrated signal integrity capabilities into their design flows, including Mentor’s HyperLynx and Cadence’s Sigrity) These tools are generally sophisticated and costly, and usually used by designers and engineersdeveloping high-speed, complex PCBs for cutting-edge electronic products.

18.6.1 SiSoft—Quantum Channel Designer and Quantum-SI

18.6.1.1 Quantum Channel Designer. Signal Integrity Software (SiSoft) started as a high-speed design consulting company in 1995, and began developing their own tools in-house. Quantum Channel Designer provides system-level design and analysis for multigigabit serial links. It offers statistical, time-domain, and crosstalk analysis, and can run thousands of simulation experiments to investigate design tradeoffs and their impact.

18.6.1.2 Quantum-SI. Quantum-SI offers integrated signal integrity, timing, and crosstalk analysis, providing pre-

and post-layout simulations with waveform processing. It analyzes the whole design for composite effects of SI, crosstalk, and timing. Quantum-SI can conduct SI and timing analysis at the chip's core, the pad of the I/O, or the pin of the package of the source and target components.

18.6.2 ANSYS—HFSS and SIwave

18.6.2.1 HFSS. ANSYS acquired the Carnegie Mellon spinoff Ansoft in 2008, gaining that company's famed HFSS (High-Frequency Structural Simulator) finite element method solver. Used to simulate 3D full-wave electromagnetic fields, HFSS can be used to solve a variety of RF, microwave, and high-speed challenges. It allows engineers to evaluate signal integrity and electromagnetic interference in connectors, transmission lines, and vias on PCBs.

18.6.2.2 SIwave. SIwave is a design platform for signal and power integrity, and EMI analysis of PCBs and packages. It features hybrid field solver technologies, which permit frequency-domain and time-domain analyses in planar structures. It can conduct resonance mode analysis to help determine impedance variations between the planes of a PCB.

18.6.3 Polar Instruments—Si9000e

Polar Instruments offers a wide range of tools for signal integrity and controlled impedance design. The Si9000e is a PCB transmission line frequency-dependent boundary element field solver that models transmission line loss and impedance at given frequencies. It extracts RLGC matrices and plots a range of transmission line information for your PCB. Si9000e is also available integrated with Polar's Speedstack stackup design tool and documentation system,

allowing designers to create the best layer stackup for achieving signal integrity.

18.6.4 CST—CST Studio Suite

Computer simulation technology (CST) has developed a variety of signal integrity and EMC software tools, most of which are available in the company's flagship tool platform. CST Studio Suite allows users to perform signal integrity and EMC/EMI simulations while designing PCBs, cable harnesses, antennas, and filters. It also includes 3D circuit co-simulation and synthesis, and tools for thermal and mechanical stress analysis.

18.6.5 Sonnet Software—Sonnet Suites

Sonnet Software's tools are designed primarily for high-frequency RF and microwave electromagnetic analysis of PCBs and other applications. Sonnet Suites offers electromagnetic modeling of all PCB layout details, including parasitics and cross-coupling. Features include calibrated internal ports and a netlist interpreters, which permit S-parameters to be incorporated into EM simulation.

18.6.6 E-System Design—Sphinx

E-System Design was founded in 2009 around the Sphinx signal and power co-simulator. Sphinx is a signal and power frequency domain solver for PCBs, IC packages, and electronic systems. Based on the Multilayer Finite Difference Method (M-FDM), it takes into account all layer coupling

effects, and lets users perform “what if” analysis by adding layers, vias, and capacitors.

18.6.7 IBM/Moss Bay EDA—EMSAT

IBM’s EMSAT is an EMC rule-checking program for PCB designs; Big Blue requires that all of its new PCB designs be checked with EMSAT. EMSAT EMC and signal integrity tools offer a postlayout check for common violations that lead to EMC and SI degradation. Moss Bay EDA, the exclusive distributor for EMSAT, has partnered with Intercept Technology to pair EMSAT with Intercept’s Pantheon viewer, which displays any violations.

18.6.8 EMS Plus—FEMAS

EMS Plus’ Fast Electromagnetic Analysis Suite (FEMAS) is based on full-wave solutions to Maxwell’s equations. It features a 2D cross-sectional analysis tool, which allows users to find impedance, coupling, and S-parameters for PCB sections. RLGC matrices can be found as a function of frequency and converted to S-parameters. Link path analysis permits S-parameter file concatenation, time-domain analysis, and frequency-domain analysis.

18.7 KEY QUESTIONS TO CONSIDER

The following is a list of questions one might ask the various EDA tool vendors regarding their PCB design tools. When you are benchmarking software within a group of similar EDA tools, or between different groups of tools, keep these points in mind:

- How is the purchase price structured and what features come with each price structure? What are the annual support costs for each tool’s structure?
- How easy is it to enter schematics and electrical net features?
- How easy is it to enter, update and maintain the library of components for the tool?
- How easy is it to update, edit or change the electrical characteristics of each net?
- What other softwaretools (yours and third-party)interface with this tool? Is the transfer interactive, batch or one-way?
- How user-friendly is the user interface regarding toolbars, drop-down menus, short-cuts, etc.?
- What options are available for timing, bus routing and autorouter control?
- What options are available for stackup creation, via constructions, trace entering pads, and impedance calculations?
- How detailed are the DRCs, and do they have various levels to define dimensions?
- Can the DRC used on the final artwork version be sent to vendors?
- Does the manufacturing output cover the three major formats, Gerber, ODB++ and IPC-2581?
- How much work is required to update designs for different software revisions?
- Can designs or parts of the design be saved and reused on other designs?
- Can designs be modified and controlled for different parts or schematic options?
- What tools are available to do gate and pin swaps for FPGAs?

18.8 FURTHER READING

18.8.1 Major PCB Design Tools

www.altium.com
www.cadence.com
www.intercept.com
www.keysight.com
www.mentor.com
www.ni.com
www.zuken.com

18.8.2 Lower-Cost PCB Design Tools

www.cadsoftusa.com
www.diptrace.com
www.ibfriedrich.com
www.kov.com
www.labcenter.com
www.pulsonix.com and www.numberone.com
www.visionics.a.se

18.8.3 Free PCB Design Tools

www.4pcb.com/free-pcb-layout-software/
www.circuitmaker.com
www.easyeda.com
www.expresspcb.com
www.fritzing.org
www.geda-project.org/
www.kicad-pcb.org
www.osmondpcb.com

www.rs-online.com/designspark/electronics/eng/
www.sunstone.com/pcb123
www.zenitpcb.com

18.8.4 Signal Integrity and EMC Tools

www.ansys.com
www.cst.com
www.ems-plus.com
www.e-systemdesign.com
www.mentor.com
www.mossbayeda.com
www.polarinstruments.com
www.sisoft.com
www.sonnetsoftware.com/

18.8.5 PCB Design Trade Shows

DesignCon—www.designcon.com
IPC APEX EXPO—www.ipcapexexpo.org
PCB Design West—www.pcbwest.com

18.8.6 PCB Design Publications

EE Times—www.eetimes.com
Printed Circuit Design & Fab—www.pcdandf.com
The PCB Design Magazine—www.thepcbdesignmagazine.com

CHAPTER 19
THE PCB DESIGN PROCESS

Lee W. Ritchey
Speeding Edge, Napa Valley, California

19.1 INTRODUCTION

There are two common methods for designing printed circuit boards (PCBs). These are to build a hardware prototype and check it out on the bench to see if it works, or, to simulate all aspects of the design prior to building it to maximize the likelihood that signal integrity, power delivery, thermal management, logic accuracy and timing stability are adequate to assure proper operation over all likely operating conditions. Figure 19.1 is a typical hardware prototyping design process.

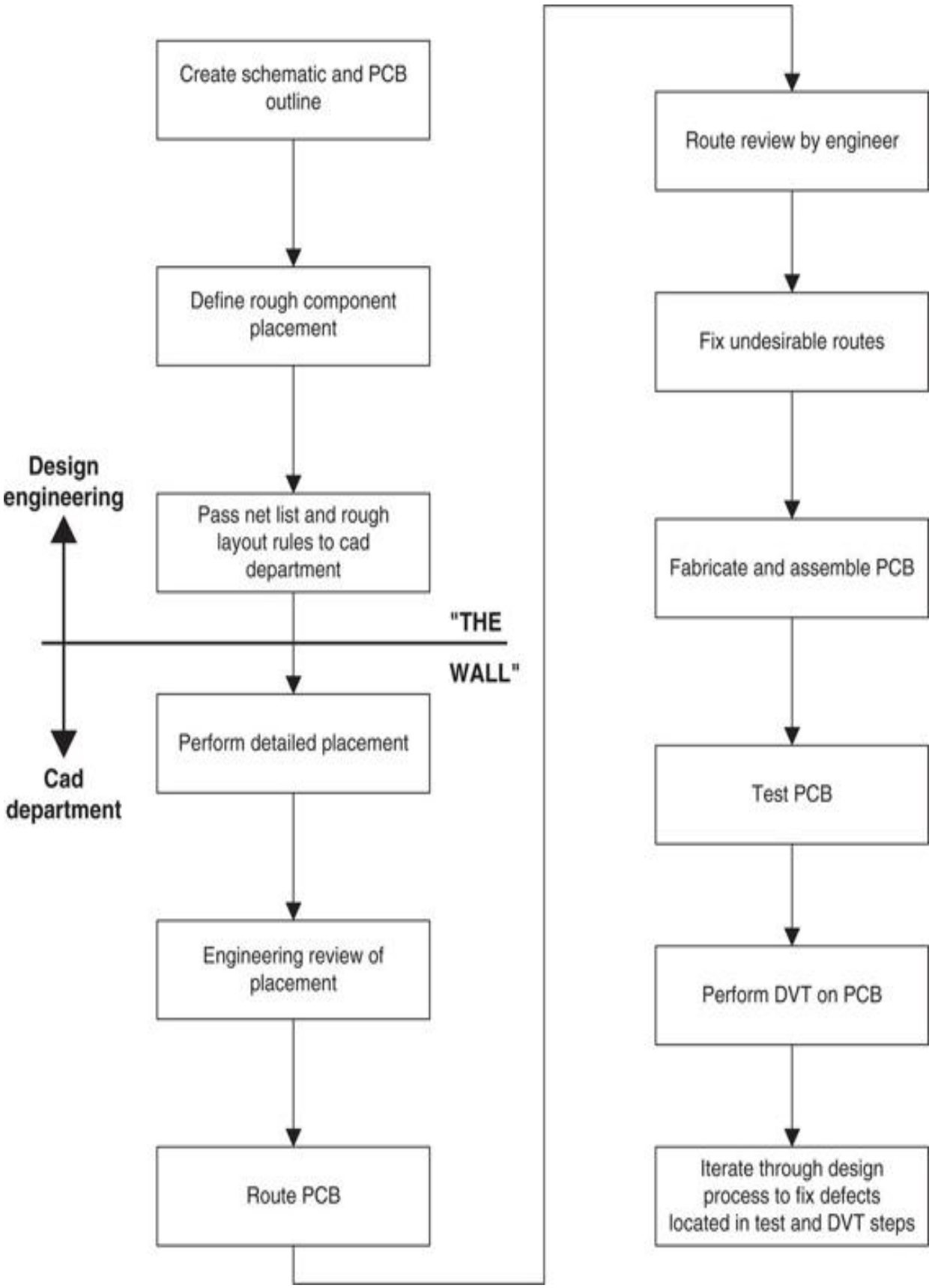

Create schematic and PCB outline
Define rough component placement
Design engineering
Pass net list and rough layout rules to cad department
"THE WALL"
Perform detailed placement
Cad department
Engineering review of placement
Route PCB
Route review by engineer
Fix undesirable routes
Fabricate and assemble PCB
Test PCB
Perform DVT on PCB
Iterate through design process to fix defects located in test and DVT steps

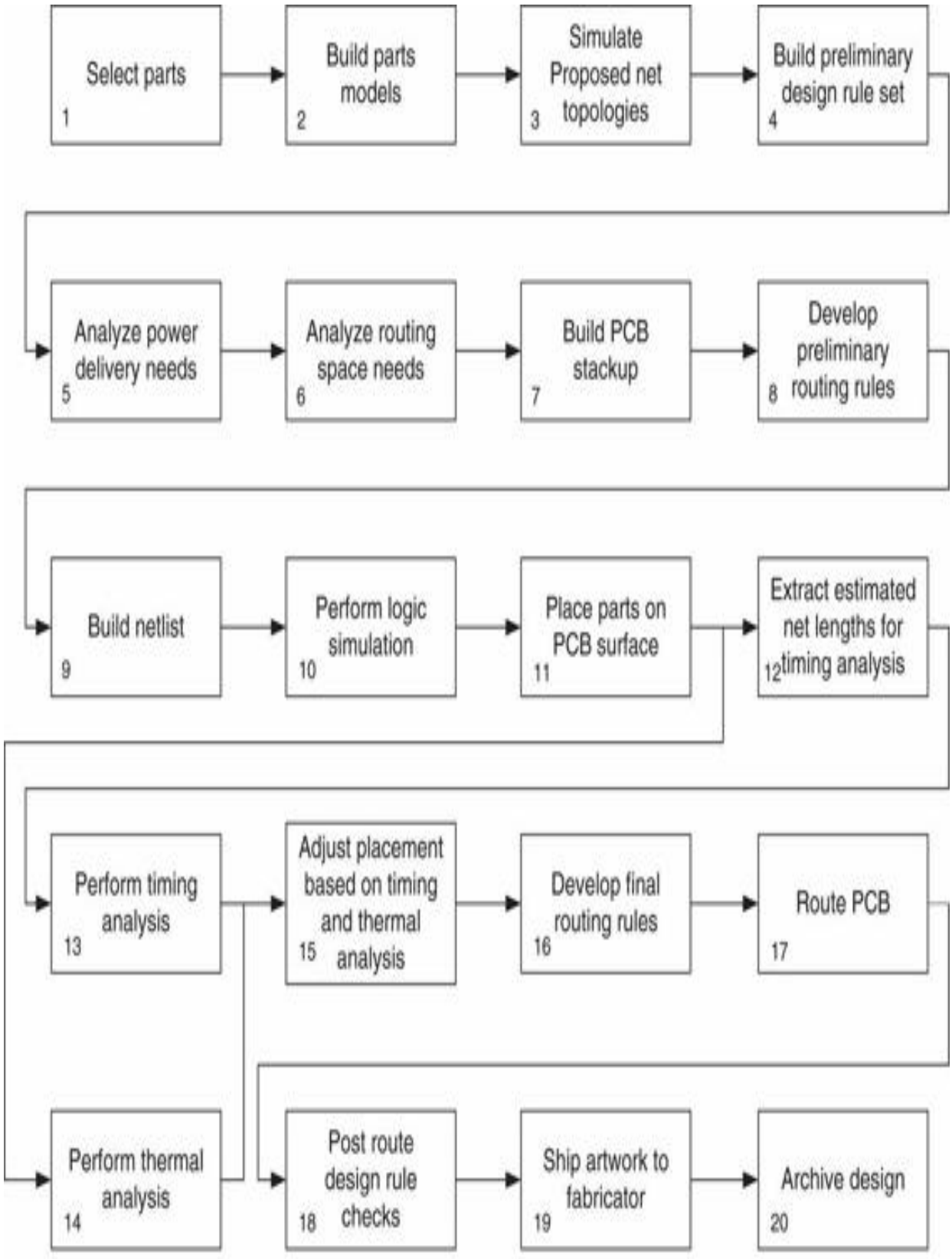
FIGURE 19.1 A hardware prototyping design flow.

This design process is typified by several, sometimes many, iterations of the PCB in order to isolate all of the logic, software and wiring defects until a level of performance is reached that is deemed stable at which point the decision is made to go into volume production and ship product to end users. The weakness of this design process is that there is no easy way to test the wide variations in component speeds, delays, gains and other parameters that occur during normal production. Further, it is often a long, drawn-out process that consumes large amounts of time and technical staff often causing a product to miss its market window. Even when the process results in a prototype that performs properly there is no way to guarantee that the design is stable. All that can be stated is that the units under test meet their specifications. It is not possible to draw the conclusion that the design itself is unconditionally stable. In fact, it is often the case that problems arise in production that must be fixed with engineering change orders (ECOs). Because of this, it is easy to make the case that Design Verification Test (DVT)-style product development testing is worse than no testing at all. The reason is passing a DVT test gives the false impression that the design is stable and that is not always true.

It is easy to argue that hardware prototyping and DVT-style testing are worse than not testing at all. The reason is that passing a DVT test gives the false sense that the design is stable.

Figure 19.2 is a PCB design flow that accounts for all of the variations that may occur during normal manufacturing and operations. It is often referred to as virtual prototyping. This flow has all of the major steps involved in arriving at a

design that is “right the first time.” It focuses on designs that are entirely digital, but could easily be modified to include analog and RF circuits as well.



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A PCB design flow with all simulation steps

FIGURE 19.2 A “virtual” prototyping design flow.

Some form of this design flow has been in use for many years in the development of high performance computers as well as complex ICs. In both cases, the original design flows did not include the level of simulation and analysis shown in this flow. The simulation and analysis steps were added one at a time as the complexity and cost of being wrong got higher. This is the situation that most PCB designers find themselves in today with the speed and complexity of modern logic.

When I present this design flow to students in my classes, often one or more engineers will respond with the statements that “there isn’t time to do all that simulation” or that “management won’t let them do that level of design analysis.” Instead, the hardware prototyping process shown in Fig. 19.1 is used. These same engineers will admit that their designs often go through three or four “spins” of the PCB and some have even admitted that 10 spins is not uncommon. When the cost of that time is properly accounted for, the virtual prototyping methodology always proves to be less expensive.

If virtual prototyping is a more reliable and less expensive way to arrive at a stable design, why isn’t it universally used to design PCBs? That is a fair question. In my experience, it is usually due to an engineering department evolving from pure logic design that didn’t require significant electrical engineering to succeed to complex, high-speed designs that could not be made stable without this level of engineering. Two things must happen. One is the design staff needs to acquire significantly different skills in order to operate the design tools in the process and the other is management needs to realize that hardware prototyping is not capable of producing stable designs and that it is necessary to support the design team with the tools and training needed to make

the changes. Sure, this is tough to do, but necessary in order to insure survival.

The design flow shown in Fig. 19.2 suggests a linear flow from start to finish. In actual practice, there are iterations among several blocks as trade-offs are made between things such as routability, thermal stability, timing margins and minimizing layer count. It also shows a single pass at routing the PCB preceded by a large number of analytical steps. The objective of all the steps leading up to routing is to make sure the design rules are well enough developed that routing involves following trace width, trace spacing, trace length and layer specifications. These are the types of input that a PCB layout system works with whether auto- or hand routing is used to place the actual traces on each layer.

19.2 THE VIRTUAL PROTOTYPING PROCESS

As mentioned earlier, the objective of the PCB design process is to arrive at a working PCB with the minimum amount of rework, preferably, none. Figure 19.2 is such a design process. Taking the blocks in Fig. 19.2 one at a time.

19.2.1 Select Parts

In this step, the objective is to select the components, ICs, connectors, capacitors, heat sinks, resistor packs and PCB materials that will make up the final design. As part of this selection process, enough information must be obtained from the manufacturer to allow the analysis and layout process to unfold. Among the information needed is

- IBIS models of all I/O.

- Worst case timing information.
- Mechanical package characteristics.
- Logic models of the parts.
- Power information including current variations during operation.
- Thermal characteristics of the parts and their packages.

19.2.2 Build Parts Models

Each analytical step in the flow-steps 3, 5, 6, 10, 11, 12, 13, 14, and 17 requires an entry into the tool library for each part. Some models, such as IBIS models, logic models and timing models will be supplied by the IC manufacturer. The other models will need to be built by the owner of each tool set.

It should be pointed out that all operations that come after parts model or library creation depend on the accuracy of the models created at this stage. A common error is to assign the task of creating library models to clerical personnel or technicians since it is a tedious task. The risk that is associated with this approach is that library entries will have errors in them that may not be detected until the PCB is built and assembled. An example of this is to build the component footprint as its mirror image. Once a library element has been built, it needs to be checked for accuracy by a second person qualified to detect errors in the model. In some cases, such as IBIS models, it may be necessary to check the model against actual hardware in order to insure the model accurately represents the real part.

The entire design process turns on the accuracy of the parts models created at the start of a project. It is imperative that this task be

assigned to personnel who are technically capable of creating accurate models. This function is usually referred to as library management and has a librarian hired for the purpose of insuring that all libraries are accurate.

19.2.3 Simulate Proposed Net Topologies

At this point it may seem premature to simulate nets in the proposed design since a schematic has not yet been created. However, it is possible to do this as long as IBIS or SPICE models are available for each driver and receiver that will be used in the actual design. As operating frequencies have climbed ever higher it is not only possible to do this, it is imperative that this step be performed as early in the design process as possible in order to insure the drivers and loads will perform properly.

How is it possible to simulate nets at this point? All that is needed to perform simulations is proposed transmission line impedances, driver models, load models, clock frequencies or data rates and estimated transmission line lengths. In almost all cases, the transmission line impedance will be 50 Ω. With this information, any good transmission line simulation tool can be used to examine the behavior of each net type and arrive at termination rules as well as worst-case voltage margins and insights into the effect of loading and termination on timing. Examples of this kind of simulation are shown in Chap. 1 of Vol. 1 of the book set listed at the end of this chapter.

At this stage in the process the number of nets is not known. What are known is the types of nets that will appear

in the design, such as, gigabit Ethernet, SPI-4, DDR, and so on as shown in Fig. 19.3. What is possible is to divide the design into classes of nets where all the members of a class share the same signal integrity needs. Once this has been done, it is only necessary to simulate one member of each net class in order to determine how all of the members of a class are to be terminated and routed. Figure 19.3 is the result of such a simulation exercise. The class name shown for each entry is then added to each net in the net list in a data field provided for this purpose.

TYPICAL TECHNOLOGY TABLE

CLASS NUMBER	CLASS NAME	TECH NOLOGY		FREQ.	QTY	IMPED ANCE	LAYERS	TERM TYPE	STUB LENGTH	TRACE WIDTH	SPACING IN CLASS	SPACING TO OTHER CLASSES	LENGTH TUNE	ROUTE ORDER
1	10GE	GB DIFF	DIFF	9.6 GB/S	8 PR	50	2	INT	0	STKUP	10	20	100	1
2	10GE CLK	GB DIFF	DIFF	4.8 GHz	2 PR	50	2	INT	0	STKUP	10	20	100	2
3	XAUI	GB DIFF	DIFF	3.125 GB/S	32 PR	50	2	INT	0	STKUP	10	20	300	3
4	XAUI CLK	GB DIFF	DIFF	1.55 GHz	2 PR	50	2	INT	0	STKUP	10	20	300	4
5	1GE	GB DIFF	DIFF	1 GB/S	4 PR	50	2	INT	0	STKUP	10	20	300	5
6	GMII	3.3CMOS	SE	125 MHz	48	50	ANY	N/A	0	STKUP	6	15		6
7	66USOA	3.3CMOS	SE	150 MHz	66	50	ANY	SER	0	STKUP	6	15		7
8	66USOB	3.3CMOS	SE	150 MHz	66	50	ANY	SER	0	STKUP	6	15		8
9	66US1A	3.3CMOS	SE	150 MHz	66	50	ANY	SER	0	STKUP	6	15		9
10	66US1B	3.3CMOS	SE	150 MHz	66	50	ANY	SER	0	STKUP	6	15		10
11	IFCLK	3.3CMOS	SE	150 MHz	1	50	ANY	SER	0	STKUP	10	15		11
12	SRAMADDR	3.3CMOS	SE	100 MHz	16	50	ANY	N/A	0	STKUP	6	15		12
13	SRAMDATA	3.3CMOS	SE	100 MHz	32	50	ANY	N/A	0	STKUP	6	15		13
14	SRAMCLK	3.3CMOS	SE	100 MHz	1	50	ANY	SER	0	STKUP	6	15		14
15	4/8FLADDR	3.3CMOS	SE	15 MHZ	8	50	ANY		0	STKUP	6	15		15
16	4/8FLDATA	3.3CMOS	SE	15 MHZ	8	50	ANY		0	STKUP	6	15		16
17	4/8FLCLK	3.3CMOS	SE	15 MHZ	0		ANY			STKUP				
18	JTAG	LVTTL	SE	1 MHz	5	50	ANY	N/A	0	STKUP	6	15		17
19	32MFLDATA	3.3CMOS	SE	40 MHz	16	50	ANY	N/A	0	STKUP	6	15		18
20	32MFLADD	3.3CMOS	SE	40 MHz	22	50	ANY	N/A	0	STKUP	6	15		19
21	32MFLCLK	3.3CMOS	SE	40 MHz	5	50	ANY	N/A	0	STKUP	6	15		20
22	I2C	3.3CMOS	SE	SLOW	4	50	ANY	N/A	0	STKUP	6	15		21
23	GPIO_IN	3.3CMOS	SE	150 MHz	19	50	ANY	SER	0	STKUP	6	15		22
24	RS-232		SE	SLOW	2	50	ANY	N/A	0	STKUP	6	15		23
25	GPIO_OUT	3.3CMOS	SE	150 MHz	21	50	ANY	SER	0	STKUP	6	15		24
26	MDC/SCL	3.3CMOS	SE	8 MHz	4	50	ANY	N/A	0	STKUP	6	15		25
27	MDIO/SDA	3.3CMOS	SE	8 MHz	4	50	ANY	N/A	0	STKUP	6	15		26
28														
29	BLANK	3.3CMOS	SE				ANY							27
30	GTX_CLK	3.3CMOS	SE	125 MHz	1	50	ANY	SER	0	STKUP	6	15		28
31	TX_CLK	3.3CMOS	SE	125 MHz	1	50	ANY	SER	0	STKUP	6	15		29
32	RX_CLK	3.3CMOS	SE	125 MHz	1	50	ANY	SER	0	STKUP	6	15		30
33	EXT_CLK	3.3CMOS	SE		1	50	ANY	SER	0	STKUP	6	15		31
34														
35	CRY_CLK	3.3CMOS	SE		1	50	ANY	SER	0	STKUP	6	15		32
36	+1P0V	PWR					8							
37	+1P2V	PWR					8							
38	+1P5V	PWR					12							
39	+1P8V	PWR					16							
40	+2.5V	PWR					19							
41	Rocket_2.5V	PWR					19							
42	+3.3V	PWR					4							
43	+5V	PWR					TRACE			200				

Length tuning tolerance is ±.

Differential pair spacing is minimum spacing. Members of a pair can be spaced more than this if needed to.

All ground planes tied together at every device ground pin.

STKUP = See stackup for trace width for each layer.

Layers 1 & 22 are not routing layers.

Routing layers are 2, 5, 6, 9, 10, 13, 14, 17,18,21

Lengths are in mils.

FIGURE 19.3 A typical design rule set presented in the technology table format.

As the IC industry migrates from the "TTL" method of specifying drivers to the transmission line management method, it is not uncommon to discover that some of the drivers that have been used with slower designs are not capable of driving transmission lines. By performing this analysis early in the component selection process, it is possible to avoid using drivers that are not capable of performing at the speeds needed.

19.2.4 Build Preliminary Net List

This step is better recognized as making a schematic. However, it is not always necessary to create a full schematic as is the case with a backplane. This preliminary net list or schematic is used to estimate routing needs, etc.

19.2.5 Analyze Power Delivery Needs

It is not possible to develop a PCB stackup until the power delivery needs of a design are established. Chapters 32 to 37 of Vol. 1 of *Right the First Time: A Practical Handbook on High Speed PCB and System Design* by Lee Ritchey cover how to estimate power delivery needs and arrive at the number of planes required, number and types of bypass capacitors needed and how to place them. Chapters 18, 20, and 21 of this book provide additional design guidance for doing this part of the design task.

19.2.6 Analyze Routing Space Needs

This step involves looking at the number of wires that are needed to connect up all of the devices in a design and estimating how many signal layers will be needed to contain them all. Accurately estimating signal layer needs requires experience with routing similar types of PCBs. It is best done by examining previous designs of similar complexity and extrapolating from there or by conferring with an experienced PCB designer. From experience with many past designs, the signal layer count is usually determined by the highest pin count IC in the design.

19.2.7 Build PCB Stackup and Assign Planes to Power System

Once the number of signal layers has been estimated and the number of power and ground planes has been determined, it is finally possible to create a PCB stackup that has the required number of layers arranged such that they provide an adequate environment for all of the transmission lines and properly deliver power to all components. Chapter 4 of Vol. 1 has a complete explanation of how to design PCB stackups.

19.2.8 Develop Preliminary Routing Rules

Routing rules are the instructions to PCB layout personnel on how to connect all of the signal and power nets in a PCB design. When designs are simple, it is easy enough to make a written list of how to handle each net. However, when designs get complex and devices have hundreds or even thousands of connections, this method breaks down. Over many years, PCB layout tools have been designed that are able to follow predefined rules based on how each net is

labeled. Figure 19.3 is an example of the way rules are recorded for such design systems. The class name is added to each net name in a data field provided for that purpose. The information in the rest of the table is loaded into route control files in the PCB layout system. As routing proceeds, the router, whether manual or automatic, examines the class name and then follows the routing rules listed in the route control files.

The routing rules consist of trace widths allowed; signal layers allowed; spacing to other signals; location of terminations and length matching as needed.

19.2.9 Build Netlist

This netlist is different from that created in step 4 in that it contains the net class information developed in step 8. It will be used with the placed PCB to assess routability and perform timing analysis.

19.2.10 Perform Logic Simulation

Virtually all logic designs have a large amount of software or firmware that must be developed along with them. There is the need to do two things at the same time. These are ensure the logic is correct and ensure that the software or firmware is correct. This creates an immediate conflict for the hardware engineering organization. In order for the software development team to do its job, it needs a logical model or hardware model on which to operate and debug the software. If a hardware model is rushed through the design process, it is certain to have errors in it that will have to be fixed by making design changes in the hardware and building new PCBs—a process that consumes large amounts of schedule time.

The solution to this problem is to build a logic simulator or emulator that represents how the hardware will be built and use that to debug software. If errors are found in the logic model, they can be fixed in minutes instead of days or weeks. In this way, both the software and logic can be debugged with the lowest cost and delay. Once both the software and logic are determined to be error free, the net list from the logic model can be used to correct the hardware net list with the assurance that the hardware will be right the first time.

19.2.11 Place Parts on Surface

Once the above steps have been completed, it is time to place all of the components on the PCB to insure that they will fit properly as well as satisfy routability, timing constraints and thermal needs. It is at this point the PCB design actually becomes physical. Actions taken during this step include creating the PCB outline in the CAD system, defining keep-out areas and placing all of the parts.

19.2.12 Extract Estimated Net Lengths for Timing Analysis

Once the parts have been placed on the surface of the PCB and combined with the net list that defines how the signal pins are to be connected to each other, the lengths of the connections can be estimated. The usual method of estimating potential interconnect length is by assuming that all points will need to be connected using only wires that travel in the *x* and *y* axes. This is what is known as the Manhattan length. (In dense PCBs it is necessary to use only X and Y routing in order to maximize the use of the routing

layers. (This concept is explained in Chap. 46 of Vol. 1 of the *Right the First Time* handbook.)

The Manhattan length of all of the connections can be extracted as a file for use by the timing analysis tools employed in Sec. 19.2.13.

19.2.13 Perform Timing Analysis

Timing analysis consists of estimating the time required for each logic operation to be completed. Time is required for the signals to propagate through the logic elements themselves and along the interconnects or transmission lines. When logic speeds were slow, the time delay through the logic elements was far greater than that on the interconnects. As a result, timing analysis involved only adding up silicon delays, both worst case and best case. Modern logic is so fast that the time delays on the interconnects are often as large as or larger than that in the silicon delays. As an example, one recent large system has a worst-case silicon delay of 3 nSec and a wire delay of 6 nSec. Clearly, checking timing using only silicon delays would not properly account for the overall timing needs of the system.

As a result of the contribution to time delay from the interconnects, timing analysis cannot take place until after the components are placed on the PCB surface and interconnect delays added to overall path delays. In addition, the timing analysis toolset must be capable of adding “wire delays” into the timing model. Timing analysis tools are discussed in Chap. 9 of RTFT Vol. 1.

It is common to discover that timing margins cannot be met if the PCB is routed with the components in their current placement. The placement is adjusted until timing margins can be met. Once this condition has been satisfied, two further analyses must be performed- thermal analysis and routability analysis.

19.2.14 Perform Thermal Analysis

Thermal analysis involves constructing a 3D model of the PCB and its components along with the container in which it will be housed. The devices that generate heat are modeled as heat sources with appropriate body shapes and heat sinks. The flow of cooling air is simulated and the temperature gradients across the PCB are calculated and displayed. If hot spots are detected, actions such as altering the placement of heat sources, adding heat sinks or increasing air flow are taken to eliminate the hot spots.

19.2.15 Adjust Placement Based on Thermal and Timing Analysis

It is common during the previous analysis steps to discover that a design will not meet its timing or thermal goals unless the placement of components is adjusted. Based on the results of these simulations, component locations are changed to improve the results. This is an interactive process that may involve several iterations through the two processes if the design is complex.

19.2.16 Develop Final Routing Rules

Once the component placement has been demonstrated to meet logical correctness, timing margins and thermal goals, the actual routing of the PCB can take place. The first step in this process is to examine the routability by examining the distribution of wires or the wire load. The most common tool for doing this is a plot known as a “rat’s nest.” Figure 19.4 shows the rat’s nest of a typical PCB containing a high pin count FPGA and several other high pin count ICs along with connectors and I/O modules. It is a plot of all the component

pins and the wires that connect them shown in a point-to-point or “as the crow flies” display before the actual routing has taken place. From this display, an experienced PCB layout person can assess the likelihood of connecting up or routing all of the wires in the signal layers available in the stackup. It may be concluded that placement changes would allow the PCB to be successfully routed. If such changes are made, it will be necessary to repeat the timing and thermal simulations to ensure those requirements are not altered by the new placement.

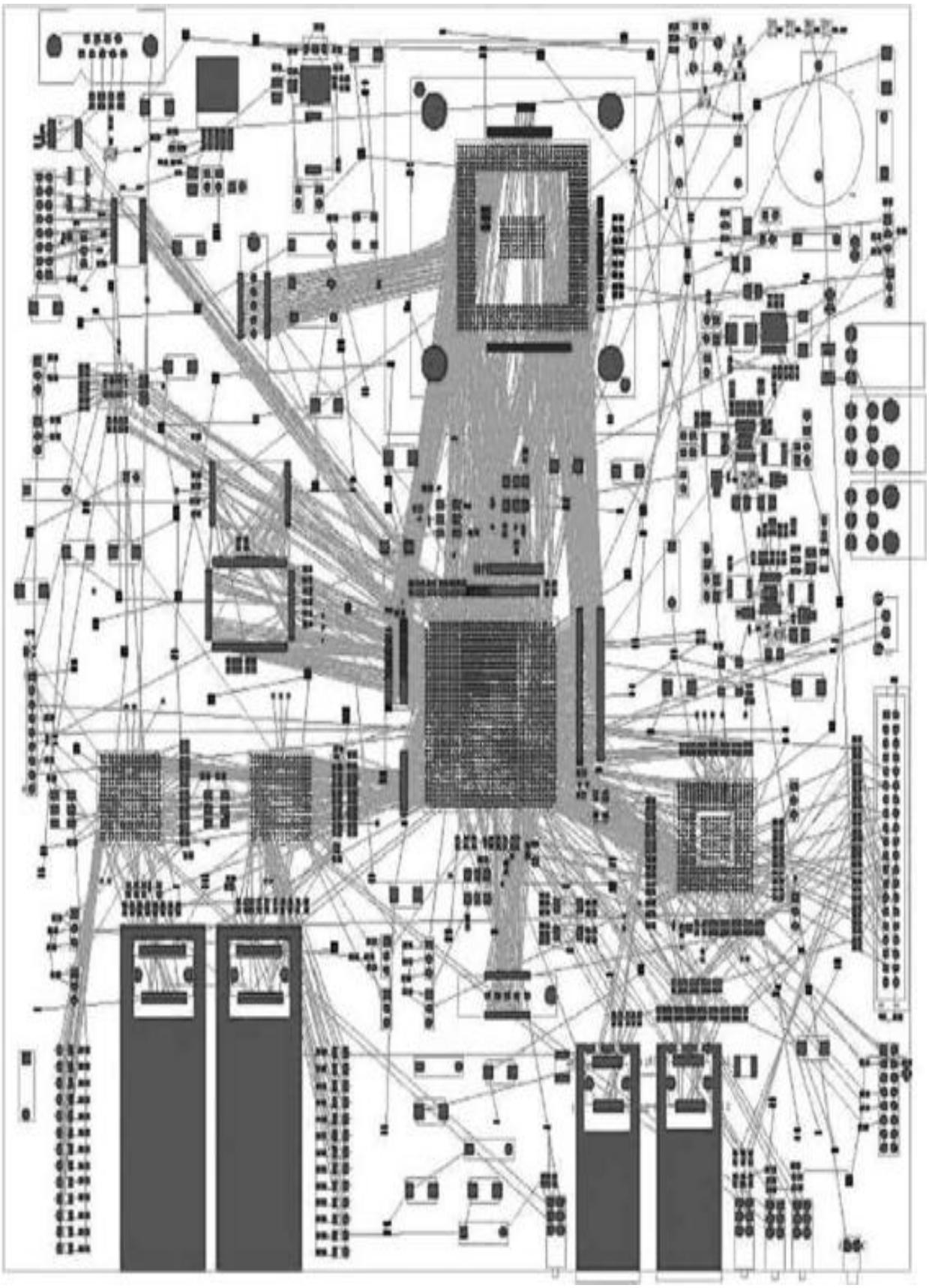


FIGURE 19.4 Typical preroute rat's nest or wire load plot.

Once the routability, timing and thermal goals have been met, it is time to finalize the routing rules that were developed in step 8. The reason this step is necessary is that the best way to connect up some multipoint nets is not obvious from the way they look in the rat's nest. An example of this is given in Chap. 10 of *Right the First Time* handbook. For those cases, it is necessary to extract the proposed net from the placement and simulate it using a good transmission line analysis tool. From this simulation, the best way to connect up the points in such nets can be determined.

Based on what is learned through the above analysis, the specifications in the Technology Table are updated and the design is ready to go through the actual routing process.

19.2.17 Route PCB

Routing a PCB is the process of taking each connection in the net list and resolving it into actual traces in the PCB signal layers. Before performing the actual routing, there are several checking steps that need to be done to ensure the finished route will be correct. The first of these checks is to verify that the net list in the PCB design system is error free. This is done by using checking programs to ensure there are no unwanted connections between different nets; that there are no single pins that should be connected into a net and that the net list accurately matches the schematic. The next check is to ensure that there are no mechanical interferences between components. Other checks are performed that ensure each transmission line has a proper termination and that the termination is located on the net where it should be and that all nets have drivers and loads.

After the checking steps have been successfully completed, the nets or wires are either hand or autorouted following the rules defined in the Technology Table. Of the two, autorouting has the advantage that it is both faster and more repeatable than hand routing and, in the interest of time, is preferred.

A common statement that is made about autorouting is that it cannot be relied on to properly route high-speed signals and, therefore, hand routing is required for all “critical” signals. This statement is usually made by someone who has “thrown” a high-speed design at an autorouter and got an unsuccessful outcome. As I investigate such events, it turns out that the autorouter was given no high speed routing instructions to follow. It is no surprise that the outcome is unusable. In these cases, the user has assumed that “high-speed” autorouters know what to do with all nets. In other words, the assumption has been made that the router has knowledge of what should be done to each net to ensure it complies with appropriate rules. This error is often made when the topic of high-speed design and the tools that are used as part of it comes up. The assumption is made that the skill is in the tool—which it never is.

I often illustrate the difference between hand and autorouting by relating my experiences as I grew up. My father was a master carpenter. When I was very young, all he had to work with were hand tools. With them, he made elegant cabinets. I took the same tools and made irregular little blocks of wood. As time went by, his shop was converted to power tools. Now, he made elegant cabinets much faster and I made irregular little blocks faster! Not having the skill, I chose to go into engineering and spare my father the embarrassment of watching me grow up to be a poor carpenter. So it is with routing PCBs. The skill is in the engineer, not in the tool. When properly used, autorouters produce superior designs in far less time than what can be achieved with hand routers.

19.2.18 Postroute Design Rule Checks

Postroute design rule checking has many steps. The first step is to insure that all of the wires in the net list have been routed in the PCB and that none of them accidentally touches any other wires or any power or ground terminals. Other steps include checking to see that all of the length matching has been done correctly; that spacing between nets is correct and that clearances around component holes and mounting holes is correct. There are specially designed postrout checking tools that are sold for this purpose. These are discussed in Chap. 9 of Vol. 2 of *Right the First Time* handbook.

A popular postroute operation is to perform board-level signal integrity analysis. There are several tool vendors that supply tools to do this. It is possible to do post layout SI on the whole board, but is difficult to do and comes after the horse has left the barn. If SI analysis is delayed until after layout has been completed, the result is likely to be the design has many violations and must be done again. It is far better to do the signal integrity engineering up front, as is described in this book, and arrive at post layout with a “right the first time” PCB.

There will be occasions when a few very critical nets may need to be checked with postroute SI analysis, but in general, this is too late in the process to be making this level of check.

Postroute full board signal integrity analysis is difficult to do and comes too late in the design process. It’s too late to lock the barn door because the horse has already escaped.

19.2.19 Ship Artwork to PCB Fabricator

This step is made up of several operations. They result in a complete document set that will be used to fabricate the PCB; to test it at the bare board level; to assemble it and to test it at the loaded board level. The documents required by a PCB fabricator in order to manufacture and test the bare PCBs are listed in Chap. 47 of Vol. 1 of *Right the First Time* handbook.

The steps involved at this stage are

- Create film layer files needed to plot film for all layers of the PCB. These are often referred to as Gerber files.
- Create bare board test net list.
- Create fabrication drawing.
- Create drill files.
- Create artwork for silk screens and solder masks.
- Create final bill of materials for the assembly.
- Create pick-and-place files to be used to assemble parts onto the PCB.

19.2.20 Archive Design

The design process up to this point has involved large amounts of time to create it. It is a valuable asset that needs to be protected in the event it is needed again to make modifications or to generate new manufacturing documentation. The process of saving a design file for future use is known as archiving. With modern design methods, all of the design records are likely to be in electronic form and are relatively easy to store away. This is a step in the design process that is often skipped or done poorly. When the time

comes to make new manufacturing documents or changes to the design, the records are incomplete or missing.

In order to insure the design files are available when needed, a disciplined archiving system needs to be installed. It is advisable to create at least two copies of the design files, one for on-site storage and one for offsite, secure storage. This latter set of records is the insurance in the event of the loss of on-site records due to fire or other calamitous events.

19.3 MAKING THE CONVERSION FROM HARDWARE PROTOTYPING TO VIRTUAL PROTOTYPING

When an engineering group decides to move from the hardware prototyping methodology to the virtual prototyping methodology described in this book and elsewhere, the size of the task can be overwhelming and it is often difficult to decide where to start. If all of the methods are incorporated at the same time, the design process is sure to grind to a halt and no product development is done, not a realistic choice. How, then, does an engineering group make this conversion?

Adopting the virtual prototyping methodology involves acquiring a new set of design tools. It also involves learning a new set of skills. Because of this, it is advisable that tools be added to the process one at a time. The places in the process where the most failures occur with the present logic technologies are transmission line management and power delivery. Therefore, it is advisable to introduce tools and methods to address these two issues first. As the skill level rises in these areas, the remaining tools can be added.

Note: References are made throughout Chap. 16 to two books written by the author. These are *Right the First Time: A Practical Handbook on High Speed PCB and System Design*, Vols. 1 and 2 by Lee Ritchey and John Zasio. These are available from the website, www.speedingedge.com.

CHAPTER 20

ELECTRICAL AND MECHANICAL DESIGN PARAMETERS

Bill Hargin

Z-zero, Redmond, Washington

Mark I. Montrose

Montrose Compliance Services, Inc., Santa Clara, California

20.1 ELECTRICAL AND MECHANICAL DESIGN PARAMETERS OVERVIEW

Everything that happens in the process of building a printed circuit board (PCB) that transmits signals from A to B and B to A works against signal quality. This is the underlying reason we spend so much time with “signal integrity”—the electrical world and the physical world are fighting against each other. This chapter addresses a number of the issues of concern, with the hopes of helping the reader end up on the winning side of this perpetual scrum.

Signal integrity relates to the quality of an *electrical_signal* that propagates between circuit components. Section 20.2 covers digital signal integrity (SI) in some detail, and a decent grasp of SI will provide a significant advantage with all aspects of electrical integrity in PCB design—including electro-magnetic compatibility (EMC) and power distribution network (PDN) design. As Fig. 20.1 implies, if a hardware engineer or PCB designer makes a design change that impacts signal integrity (SI), it's likely that the change will also have an impact on the power distribution network and electromagnetic compatibility (EMC). Likewise, changes to the PDN will have impacts on both SI and EMC, as well. Their physics are inescapably intertwined.

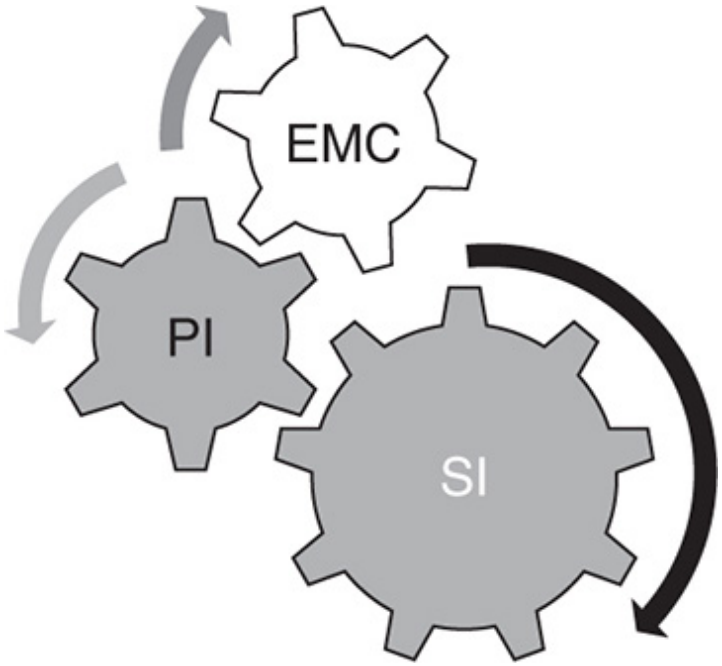


FIGURE 20.1 The physics of PCB signal integrity (SI), power distribution network (PDN) design, and electromagnetic compatibility (EMC) are inescapably intertwined.

The key issue of concern for PCB designers is ensuring both analog and digital signal transmission between circuits and interconnects occur without any loss of signal fidelity.

Power integrity, discussed in Sec. 20.3, is a critical design aspect in any PCB design. Voltage and current levels must be within integrated-circuit manufacturers' margins to ensure that components function as designed. Power integrity analysis must be performed to ensure optimal voltage and current is available at all times—particularly around components that demand a good bit of current.

If the voltage on a power or return plane droops due to lack of energy charge, generally minimized through use of decoupling capacitors, this "bounce" will appear between planes as a propagating RF signal that may cause harmful disruption to other components or radiated from the PCB when this propagating field hits the physical edge of the board, a via or even radiated from the package of an active component in the *z* axis. Both would produce EMI events—discussed further in Sec. 20.4.

Both the direct and indirect relationships between signal integrity and electromagnetic compatibility (EMC) or electromagnetic interference (EMI) are important for designers to grasp. A board or system may pass functional test requirements, essentially meeting SI requirements, but that does not necessarily mean that it will adhere to government EMC standards. Conversely, a PCB that fails EMC testing may function properly, or more likely, will have some serious signal and/or power-integrity issues. For example, a fast driven, long clock signal with improper termination may "ring" like crazy—and EMC engineers will see the results of that high-frequency ringing in the compliance lab months after the clock was improperly optimized for SI. As a result, it's helpful for engineers to be comfortable working in both the time and frequency domains at the same time.

20.2 INTRODUCTION TO DIGITAL SIGNAL INTEGRITY

Before going into signal quality from a voltage versus time standpoint, it's helpful to consider SI at a more foundational level. If you look in a college communications book, you'll see something similar to the basic Communications Model, depicted in Fig. 20.2. A "sender" encodes a message, to be decoded by a "receiver." Whether the receiver receives the intended message is largely determined by the volume (amplitude) of the sender's communication, and how much external noise is competing with it. In the end, whether the communication was successful—where the intended message was sent and received—is determined by the receiver alone.[1]

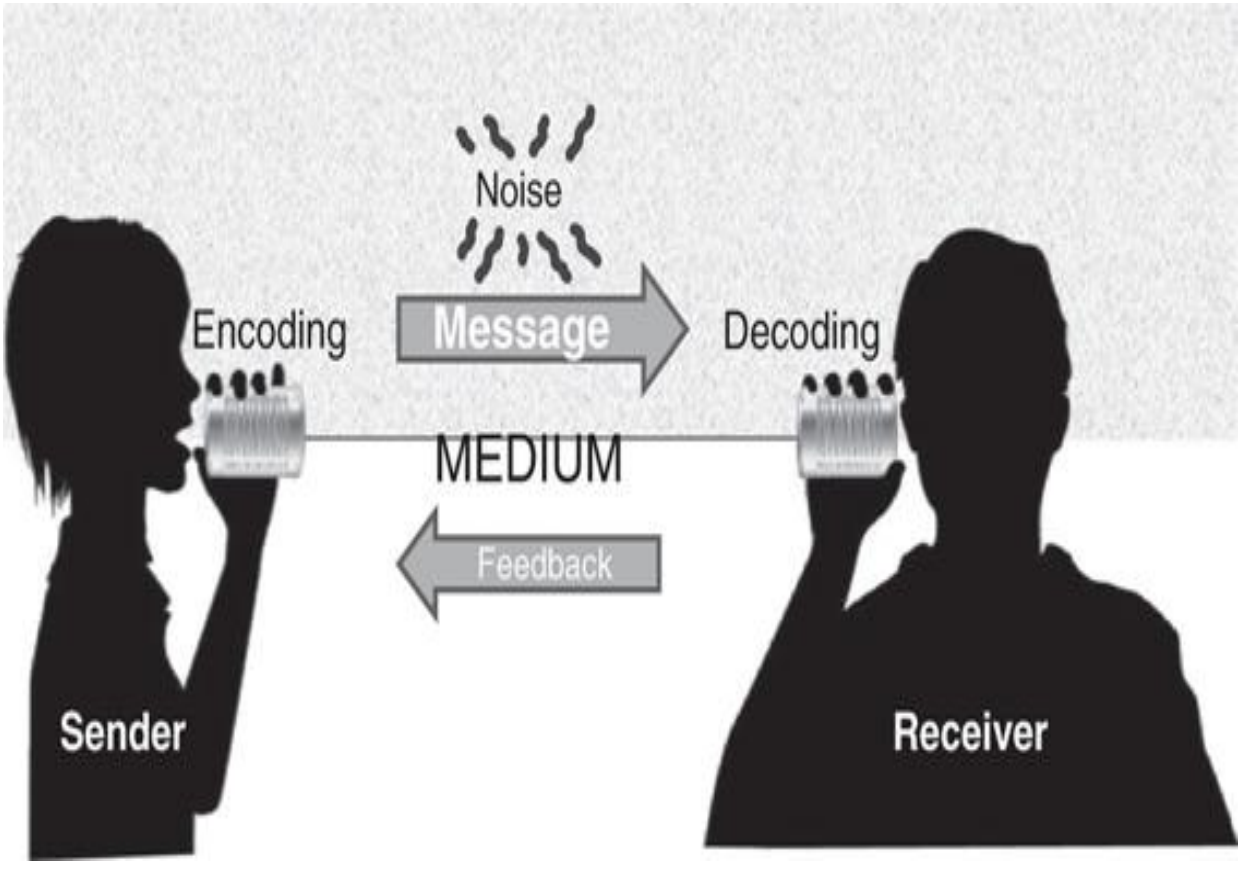


FIGURE 20.2 The communications model—similar to what you might find in a communications textbook—is a good place to start when learning electrical signal integrity.

Carrying the analogy over to the electrical world, the sender is a driver IC, and the medium includes connectors, cables, BGA balls, BGA breakouts, vias, PCB traces, and the dielectric medium.

Unfortunately, everything that happens in the process of building a PCB that transmits signals from A to B and B to A works against signal quality. This is the underlying reason we spend so much time with “signal integrity”—the electrical world and the physical world are fighting against each other.

The quality of an actual electrical signal is determined by its waveform shape. If a waveform shape deteriorates too much, it can cause a number of different problems, including functional failure, “flaky” or intermittent performance, or—worst of all—failure in the field. Figure 20.3 contrasts a representation of a digital signal in an introductory electrical engineering text book versus the same signal in a manufacturer datasheet, versus possible results for a “receiver” waveform on an actual PCB. It’s the non-ideal physical medium between the sender—a driver IC—and the receiver IC that causes delays and functional degradation of the signal.

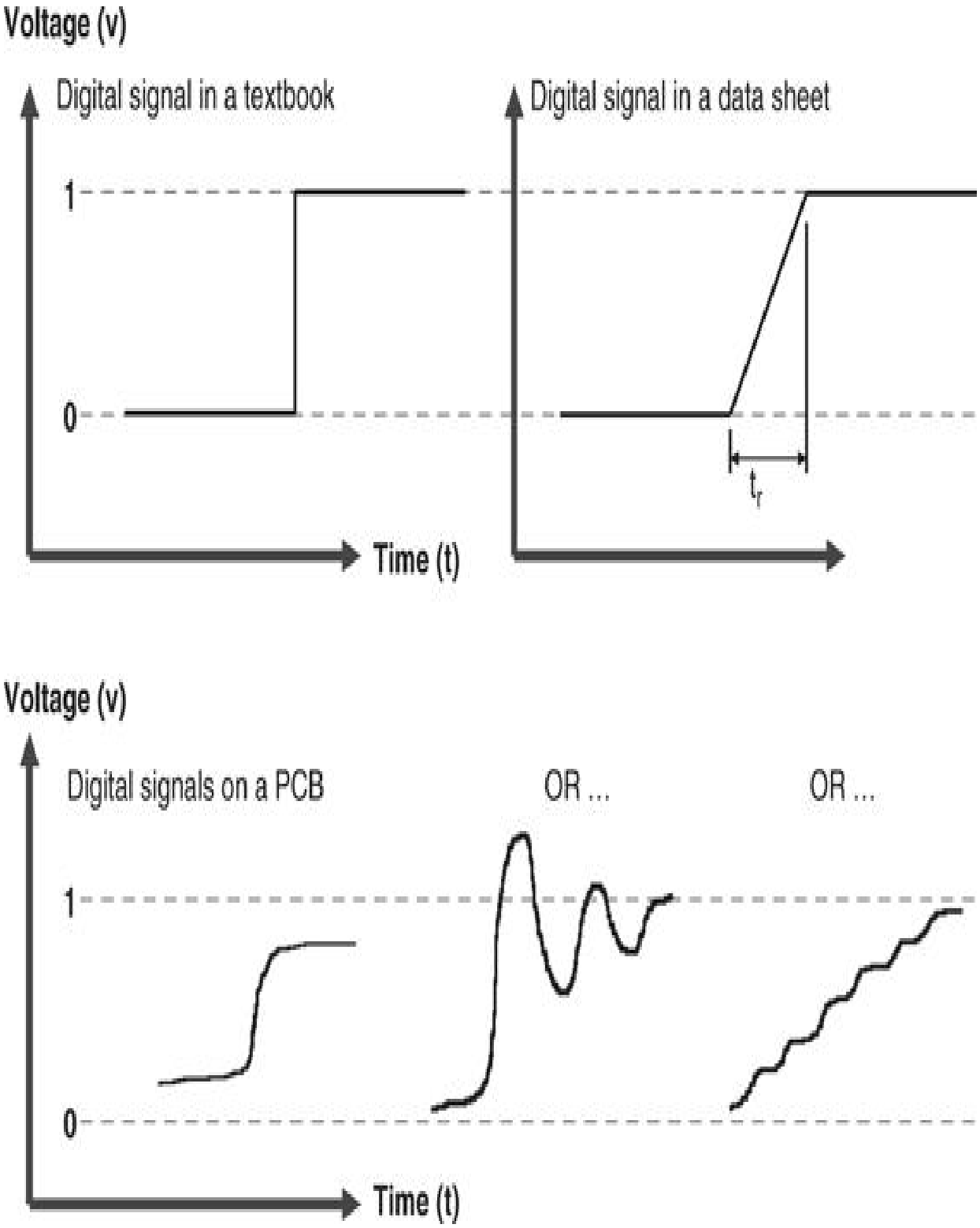


FIGURE 20.3 A representation of a digital signal in an introductory electrical engineering text book versus the same signal in a manufacturer datasheet, versus possible results for a “receiver” waveform on an actual PCB.

20.2.1 Possible Waveform Errors during Signal Transmission

Whenever a signal is propagated between a driver and receiver, degradation of the signal waveform may occur from that of the “textbook signal.” A sample list of issues that may affect the quality of a signal during propagation is provided below. This is not a comprehensive list, but gives an overview of concerns that signal integrity engineers must deal with during a product design. All of the items below occur due to the *physical implementation* on a PCB that includes both core and pregreg material selection, as well. (See Figs. 20.4 and 20.5.)

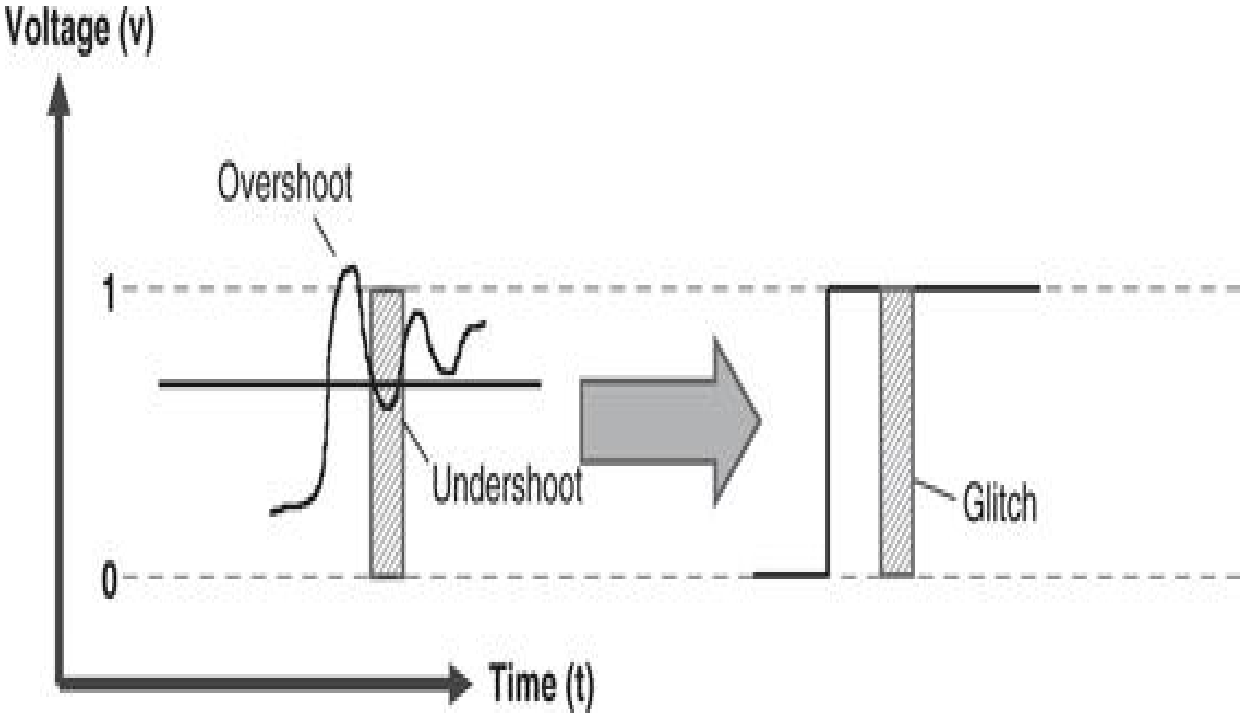


FIGURE 20.4 Ringing at a receiver, leading to an undershoot condition, which results in a threshold error. Also referred to as “false clocking” or “glitching.”

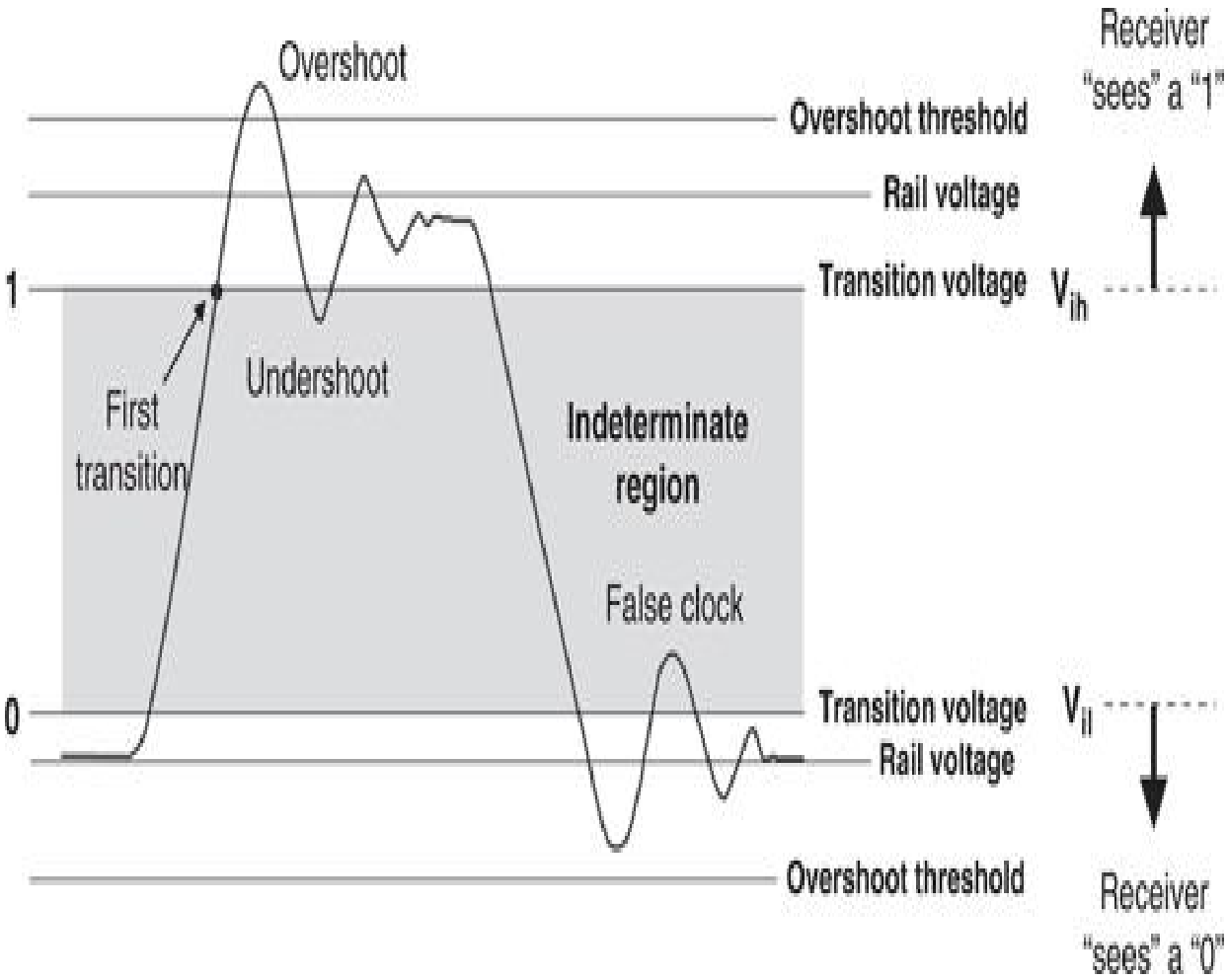


FIGURE 20.5 Receiver voltage thresholds, Vil and Vih, determines whether a receiver "sees" a logic 1 or a logic level 0, and whether the channel performs as intended.

- Threshold errors/false clocking/glitching
- Overshoot
- Undershoot
- Oscillation/ringing
- Delay errors
- Crosstalk
- EMI/EMC problems

Having poor signal integrity can cause PCBs to malfunction, behave intermittently or show performance

variations from different production runs. The waveform in Fig. 20.5 goes into a little more detail on some of the requirements for a signal to produce the intended performance behavior. The first thing to note is the "Indeterminate region" that's grayed out. The upper "transition voltage" on this is referred to as Vih, or "voltage input, high." This is the voltage above which a specific integrated-circuit manufacturer guarantees that the receiver will switch high. Similarly, Vil, or "voltage input, low" is the voltage below which a receiver is guaranteed to switch low. Any voltage states in between Vil and Vih are "indeterminate." If a signal wanders back and forth across that threshold (i.e., undershoot) that's the condition that can lead to false clocking. A detailed timing discussion is beyond the scope of this chapter, but these thresholds are also used in "flight-time" calculations in a timing budget.[2]

20.2.2 What Specifically Causes Signal Integrity Problems?

It's common to think of high frequencies as the main problem—and there are a number of concerns associated with higher frequencies; but it's important to understand signal integrity, specifically, in more detail. At a high level, signal integrity problems are caused by: (1) fast driver edge rates, (2) comparatively long interconnects between driver/receiver pins, and (3) impedance discontinuities or mismatches.

20.2.3 Fast Driver Edge Rates

The "edge rate"—sometimes called the "switching speed," or "rise time" or "fall time"—for a driver IC can typically be found in a component data sheet. Rise time, or T_r, is usually

measured as the time it takes for a driver output to ramp from 0 V to 10 percent of its voltage swing to 90 percent of its upper-rail voltage.

Present switching speeds have made circuit board routing significant. Component packages, PCB traces and vias, connectors and cables all have parasitic inductance and capacitance that are essentially transparent at slow driver switching speeds. (For example, a 10 ns driver edge from 20 years ago.) A circuit board trace simply looks like a resistive load to a driver IC. But, at driver edge rates faster than 2 ns, these inductive and capacitive elements become a much bigger concern, along with the propagation velocity down the trace—and managing signal quality through this maze of inductance and capacitance becomes as big of a job (if not bigger) as laying out and routing the board. Couple this with the fact that many of today's edge rates are below 100 ps (0.100 ns), and it's clear why there's so much concern about SI.[2]

20.2.3.1 What's a Transmission Line? A transmission line is any structure that propagates an electromagnetic field between a source and receiver. Examples of transmission lines include

- Circuit board traces
- Coaxial cable
- Any cable assembly configuration
- Power and return planes
- Free space

Every transmission line is described as a media for signal propagation that includes inductance (L), capacitance (C), resistance (R) and conductance (G) per unit length. These parameters are determined by the transmission-line cross section. The cross-sectional L and C components are used to determine the transmission line's impedance as well as

signal propagation velocity or delay.[2] Above roughly 300 MHz, additional resistive “lossy” elements begin to take on significant value as well.[3]

At any point along the transmission line, a signal requires a complete current loop in order to propagate. The distributed capacitance of the transmission line provides the means of establishing this loop during signal transitions.

20.2.4 Physical Transmission Line Characteristics

There are two primary trace cross-section types found on PCBs shown in Fig. 20.6, and possibly 50 or more derivatives that are beyond the scope of an introduction to signal integrity. The two most common configurations are

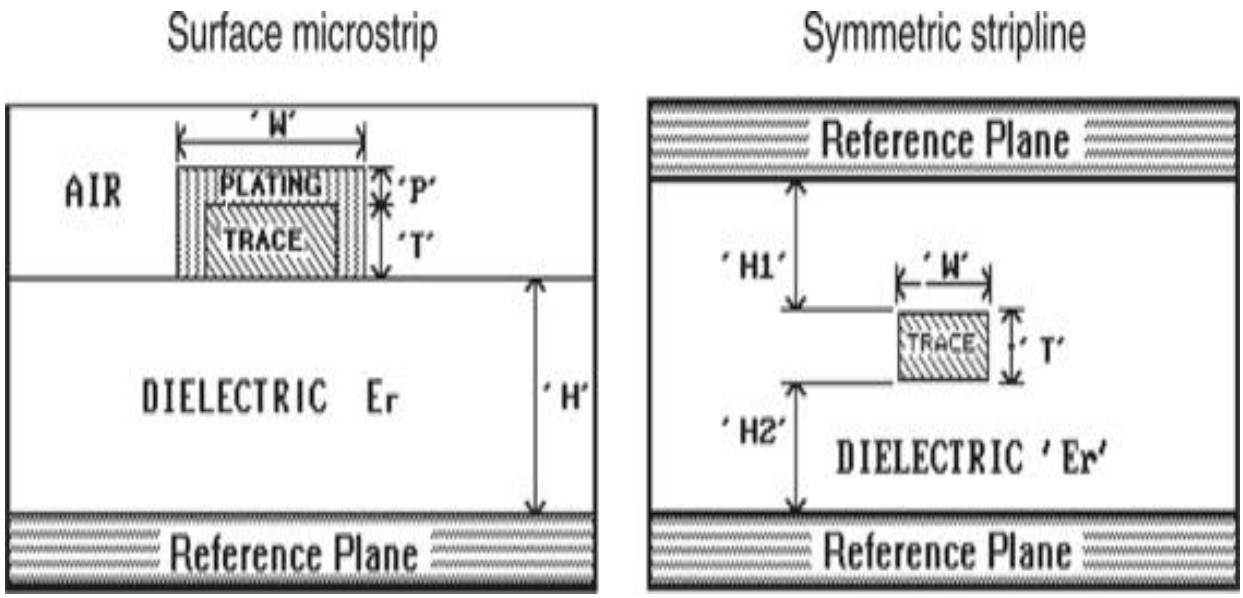


FIGURE 20.6 The two most common signal or transmission-line configurations are surface microstrip and symmetric stripline.

- *Striplines*. The most common trace configuration on a PCB is the stripline, which are traces located on inner layers of

the circuit board stackup, sandwiched between copper reference planes.

- *Microstrips*. Signals on a PCB's outer layers are referred to as surface microstrip or microstrip lines.

Stripline configurations are more common than microstrip lines because on a *multilayer* (*n* layers) board stackup, only two outer (microstrip) layers are available, and up to $n - 2$ stripline layers are possible, assuming each internal layer is considered as a candidate for signal trace routing. There are essentially two kinds of basic stripline configurations: "symmetric" or "balanced," which include one signal layer sandwiched between two reference planes; and "asymmetric" or "imbalanced," which include two signal layers sandwiched between two reference planes. Symmetric stripline routing is recommended for maximum crosstalk immunity.[4]

There are several physical characteristics of transmission lines that determine the four key electrical characteristics discussed in Sec. 20.2.5 below:

1. *Dielectric height (H)*. The thickness of the dielectric material between the signal trace and the nearest reference plane after PCB fabrication in the *Z*, or vertical direction.
2. *Dielectric constant (Er or Dk)*. A measure of the relative capacitance of the transmission medium, as compared to a vacuum. Typical Dk (or Er) values range from 3.5 to 4.3 on a PCB. More expensive materials can have Dk values as low as 3.3, while a vacuum has a Dk of 1.0, which also applies to air. A less common name for the dielectric constant is *relative permittivity*.
3. *Trace Width (W)*. The width of the PCB trace, typically measured in mils, thous, or microns (um). When etched on a PCB, traces take on a trapezoidal shape. To simplify, an estimated rectangular width is often used.

4. *Trace thickness (T)*. This is the vertical thickness of a signal trace in the Z direction. Signal layers that are designed on half once copper, for example, typically start at roughly 0.7 mil thickness prior to etching, and finish at roughly 0.6 mil after etching and cleaning during PCB fabrication. Double these numbers for 1 oz copper. A surface microstrip is usually plated, so the original copper foil of 0.0006 (or 0.0007) inches is usually plated up to three times its original thickness, to a finished thickness of between 0.0018 and 0.0021 in. The finished thickness is used to determine the track impedance, discussed below.

These four physical parameters determine the cross-sectional inductance and capacitance of a transmission line, which can then be used to determine the four key electrical characteristics of a transmission line, outlined below.[5]

From a practical perspective, microstrip signals are usually implemented on the finished printed circuit with a coating of solder mask (Dk ~3.3/3.4). In this case, the structure is that of a coated microstrip and will have a different impedance than the microstrip that assumes air (Dk = 1.0) is above the conductor. Any additional coatings, like conformal coatings or thermal blankets, will also change the transmission lines impedance.

20.2.5 Four Key Electrical Characteristics for Transmission Lines

There are four primary characteristics associated with transmission line routing on a PCB. Each of these characteristics is derived from the cross-sectional geometry of the structure[3]:

1. *Propagation velocity*. Signals do not propagate down transmission lines instantaneously. The speed of a signal varies inversely with the capacitance of the medium, which is tied to the dielectric constant (Dk) of the laminate material as well as the inductance per unit length. The relationship for propagation velocity is shown in Eq. (20.1*a*). As a rule-of-thumb, stripline signals travel about 5.8 in/ns for FR-4 material with a Dk around 4.0, roughly half the speed of light. Signals travel a bit faster on microstrip lines because air has an $E_r = 1.0$, roughly ¼ that of a standard FR-4 dielectric material.
2. *Time delay, or "propagation delay."* Signals traveling on a PCB trace experience propagation in addition to logic delays, which can be significant in high-speed systems. Propagation delays are affected by the length of the trace, anything affecting the inductance or capacitance related to the geometry of the trace, the location of the trace within the PCB stackup, and the materials in the PCB stackup. The delay per unit of trace length is the inverse of the propagation velocity relationship, as shown in Eq. (20.1*b*). The easiest way to calculate propagation delay through a stripline is to multiply the speed of light, 85 ps/in, by the square root of the dielectric constant of the material. For a 10-in (25.4 cm) stripline trace through a material with a Dk of 4.0, the total "propagation delay" would be 1.7 ns.
3. *Characteristic impedance (Z_0) of the transmission line*. PCB traces look just like a resistance until a reflected wave comes back. With typical values for PCB traces that range from 40 to 65 Ω, Z_0 (Z zero) determines ratio of current and voltage propagating through a trace, both forward and return. Detailed IPC-4121 equations have been documented and modified over the years to approximate Z_0, but—at a high level—Z_0 is generally represented as shown in Eq. (20.1*c*). Field-solver software

can calculate Z_0 to within an ohm, typically, for single-ended signals.

4. *Reflections*. Energy reflections occur at the end of a transmission line, or at any impedance change along the way. Impedance changes can come from any number of physical changes along the signal path. Managing this is often called “impedance matching.”[6]

(a) Propagation Velocity (b) Propagation Delay (c) Characteristic Impedance

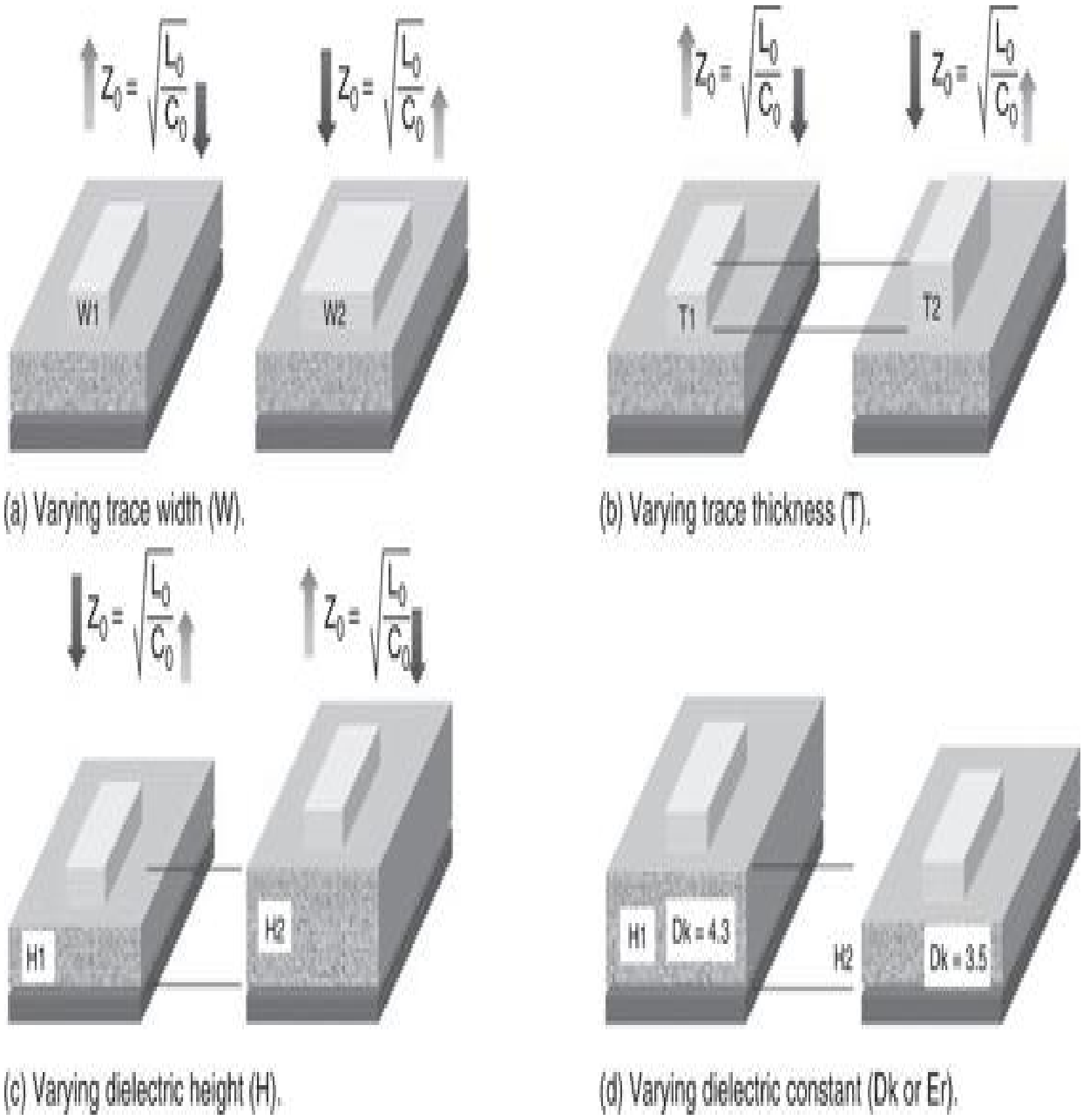
$$v = \sqrt{1/LC} \qquad \text{Delay (Td)} = \text{Length} \times \sqrt{LC} = \text{Length} \times 85\sqrt{DK} \qquad Z0 = \sqrt{L/C} \tag{20.1}$$

Equation (20.1*a–c*) shows three key electrical relationships for transmission lines.

20.2.6 Characteristic Impedance (Z_0)

Correctly calculating single-ended signal impedances is a key step in the PCB design process. The IPC-4121 specification includes some general approximations for determining trace impedance. There are a number of commercial, software-based field solvers available for the task, as well.[7]

Impedance planning is most easily performed with a capable, easy to use electromagnetic field solver that automatically solves Maxwell’s equations.[1,4] When planning a specific transmission-line’s cross section impedance, it is very helpful to consider the *capacitance* of the copper trace in reference to its closest reference plane(s). Figure 20.7 a–d highlights some of the trade-offs.[8]



(a) Varying trace width (W).

(b) Varying trace thickness (T).

(c) Varying dielectric height (H).

(d) Varying dielectric constant (Dk or Er).

FIGURES 20.7 *a–d* Four ways to adjust trace impedance—primarily considering capacitance. (*Adapted from Rod Strange, Fast Edges*.)[8]

- Widening a signal trace from W1 to W2 will *increase the capacitance* in the denominator of the generic characteristic impedance relationship, resulting in a lower impedance.
- Increasing trace thickness from T1 to T2 will also *increase the capacitance* in the denominator of the generic

characteristic impedance relationship, resulting in a lower impedance.

- Increasing dielectric height from H1 to H2 results in a *reduction in the effective capacitance* of a trace, and therefore a higher impedance.
- Reducing capacitance with a relatively low-Dk dielectric material will increase the impedance if the same cross section is used, but enables designers to use thinner dielectrics to achieve the same target impedance.

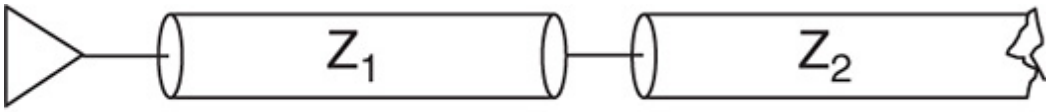
Some rules of thumb exist for “ball park” impedance planning, as well. A quick approach is to consider that the ratio of the line width to dielectric thickness is 2:1 for a 50-Ω microstrip in FR-4.[5] If the dielectric thickness is 3.5 mils, the line width is roughly 7 mils for a 50-Ω line. Again, this relationship is corroborated by Fig. 20.7*a*.

20.2.7 Signal Reflections on a Transmission Line

If you have ever dribbled a basketball in an empty gym, you’ve heard the sound waves bouncing off the six parallel surfaces of the gym. Echoes are reflected sound waves. Water surface waves created by wind that bounce off a floating bridge, forming similar waves that move away from the bridge are reflections, as well. Both examples are similar to reflected voltages on a transmission line, except the solid wall would be represented by an open circuit at the end of a line, just like a receiver in its default, high-impedance state.

A signal reflection, the root of most signal integrity, crosstalk and EMI issues, occurs whenever a signal sees an impedance discontinuity, or a change within the characteristic impedance of the transmission line. Figure

20.8 and the associated equation show the simple relationship that predicts signal reflections.[6]



$$\% \text{ Voltage reflection} = \frac{(Z_2 - Z_1)}{(Z_2 + Z_1)}$$

FIGURE 20.8 The % voltage reflection relationship. Any time a signal passes through a change in impedance, a voltage reflection will occur.

There are three possible voltage reflection scenarios:

1. When $Z_2 > Z_1$, reflection is *positive*.
2. When $Z_2 = Z_1$, reflection is 0 percent.
3. When $Z_2 < Z_1$, reflection is *negative*.

Anything causing a delta between Z_2 and Z_1, including variations in board stackup, changes in trace width, BGA breakouts, stubs, vias, loads, connector transitions, or large power plane discontinuities will lead to a voltage reflection. Careful pre-layout impedance planning is a critical part of a proactive impedance-control process.

At the source, reflection from the far end reflects again. Source reflections are usually antireflections because driver impedance is lower than line impedance. Signal reflections cause the overshoot, undershoot and ringing seen on receiver waveforms.

The relative significance of a reflection is impacted by a number of factors, including the actual impedance difference, as outlined above, the length over which the impedance difference occurs relative to the overall length of the transmission path, and the technology's tolerance for noise. Detailed attention to each of these issues is beyond

the scope of this introductory chapter, which will assume that care has been given to minimize unnecessary impedance discontinuities wherever possible.

20.2.8 The Length at Which a Trace Becomes a Transmission Line

There are a number of different opinions, as to when a trace reaches the “critical length,” and becomes a transmission line—where designers need to worry about all of these effects, like parasitics, impedance matching and reflections. Rules have been suggested, stating that the length of a line in nanoseconds can be no more than 1/3, ¼, 1/6, or 1/10 the driver’s switching speed. Before discussing any of these “rules” in detail, it’s helpful to be reminded that the answer all depends on the receiver. If the receiver can “understand” a signal clearly, with a high level of confidence, that’s a good answer.

One rule of thumb is to make the line length in nanoseconds no more than 1/6 the driver’s switching speed. As discussed earlier, in FR-4, a signal propagates at 5.8 in/ns (round to 6 in/ns).

Let’s look at our driver’s edge rate to determine this rule-of-thumb’s recommended line length. Signal propagation during first incidence of waveform down a transmission line is sometimes called the “transition electrical length” or TEL.[6]

$$\text{Transition electrical length} = T_{\text{rise}}\ (\text{ns}) * 6\ (\text{in/ns}) = 1.0\ (\text{ns}) * 6\ (\text{in/ns}) = 6\ \text{in}$$

This means that the initial transition of the signal travels six inches down the line before the signal finishes switching. Multiply this by 1/6 (the rule-of-thumb) to produce the maximum (recommended) line length using this driver. Of course, for a 1 ns driver edge, and assuming the 6 in/ns approximation, the sixes cancel, and the result is a

maximum line length of 1.0 inch in the unterminated case. (More on that later.) If you simulate this configuration—with a 1.0-in driver edge—you will see some still ugly ringing, as shown in the “1 in” waveform in Fig. 20.11. Clearly, this puts the 1/3, ¼, and 1/6 rules for the maximum route length for a transmission line in question. Simulating high-speed signals of concern is always advisable over naively applying rules of thumb. The remainder of this chapter—including the “3 T’s”—will help with the basic concepts. (Note: For FR-4, rather than doing all of the multiplication above, just use the rise time in nanoseconds as the maximum line length since 6 × 1/6 = 1.)

20.2.9 Impedance Mismatches

Before going into detail on using the “3 T’s” to address signal-reflection problems, it’s important to address impedance mismatches at a more general level. Reflections occur at any impedance discontinuity according to the following relationship[6,3]:

$$\%\ \text{Voltage reflection} = 100 \times \frac{z_2 - z_1}{z_2 + z_1} \tag{20.2}$$

Anything causing a delta between Z_2 and Z_1, including variations in board stackup, trace-width variations, changes in trace width, BGA breakouts, stubs, vias, loads, connector transitions, or large power plane discontinuities will lead to voltage reflections. Some of these reflections—if significant enough—cannot be resolved using the 3 T’s. For this reason, careful pre-layout impedance planning is a critical part of a proactive impedance-control process.

The relative significance of a reflection is impacted by a number of factors, including the actual impedance difference, as outlined above, the length over which the

impedance difference occurs relative to the overall length of the transmission path, and your technology's tolerance for noise. Detailed attention to each of these issues is beyond the scope of this chapter, which will assume that care has been given to minimize unnecessary impedance discontinuities wherever possible.

20.2.10 The "3 T's"

The techniques for managing these effects on digital signals can be broken into three broad categories, sometimes referred to as "the 3 T's"[9]:

1. *Technology*. Select driver technology that's fast enough to meet your functional needs, but as slow as possible.
2. *Topology*. Select topologies that meet timing requirements while minimizing the impact of signal reflections.
3. *Termination*. Manage signal reflections using passive components.

The challenge is that there are thousands of such choices to be made when designing a PCB, and trade-offs must also be managed vis-à-vis timing requirements, and electro-magnetic compliance (EMC)—discussed further in Sec. 20.4.

20.2.10.1 The First "T": Triage by Technology. There are several strategies for dealing with nonideal routing. The first is to know which nets can afford to suffer from arbitrary routing and which truly cannot. A three-tier "technology triage" strategy, as outlined in Fig. 20.9 works best.[10]

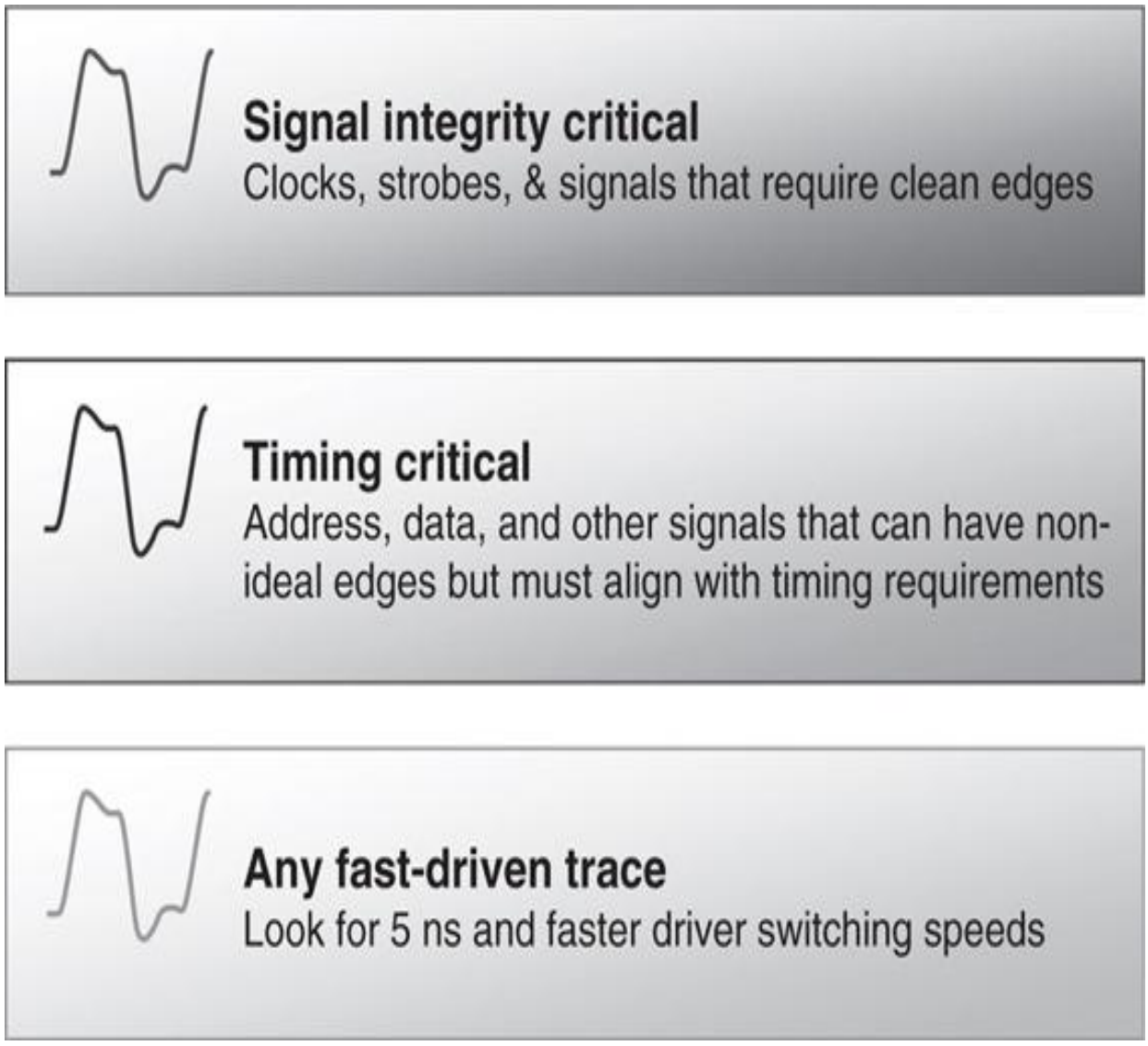


FIGURE 20.9 A three-tier “technology triage” strategy.

1. Nets that are “signal-integrity-critical” (clocks, strobes, and other signals that must have clean waveforms).
2. Nets that are “timing-critical” (address, data, and other signals that can have nonideal waveforms but must align with your timing requirements).
3. Signals with driver edge rates that are faster than 5 ns. The remaining slower-driven signals can be ignored from a signal integrity standpoint.

Figure 20.10 shows the effect of increasing driver edge rates on a 5-in (127-mm) trace. The 10 ns and 5.0 ns drivers produce clean receiver waveforms. The faster 2.5 ns and 1.0 ns drivers, however, produce reflections and ringing on their respective receiver waveforms.

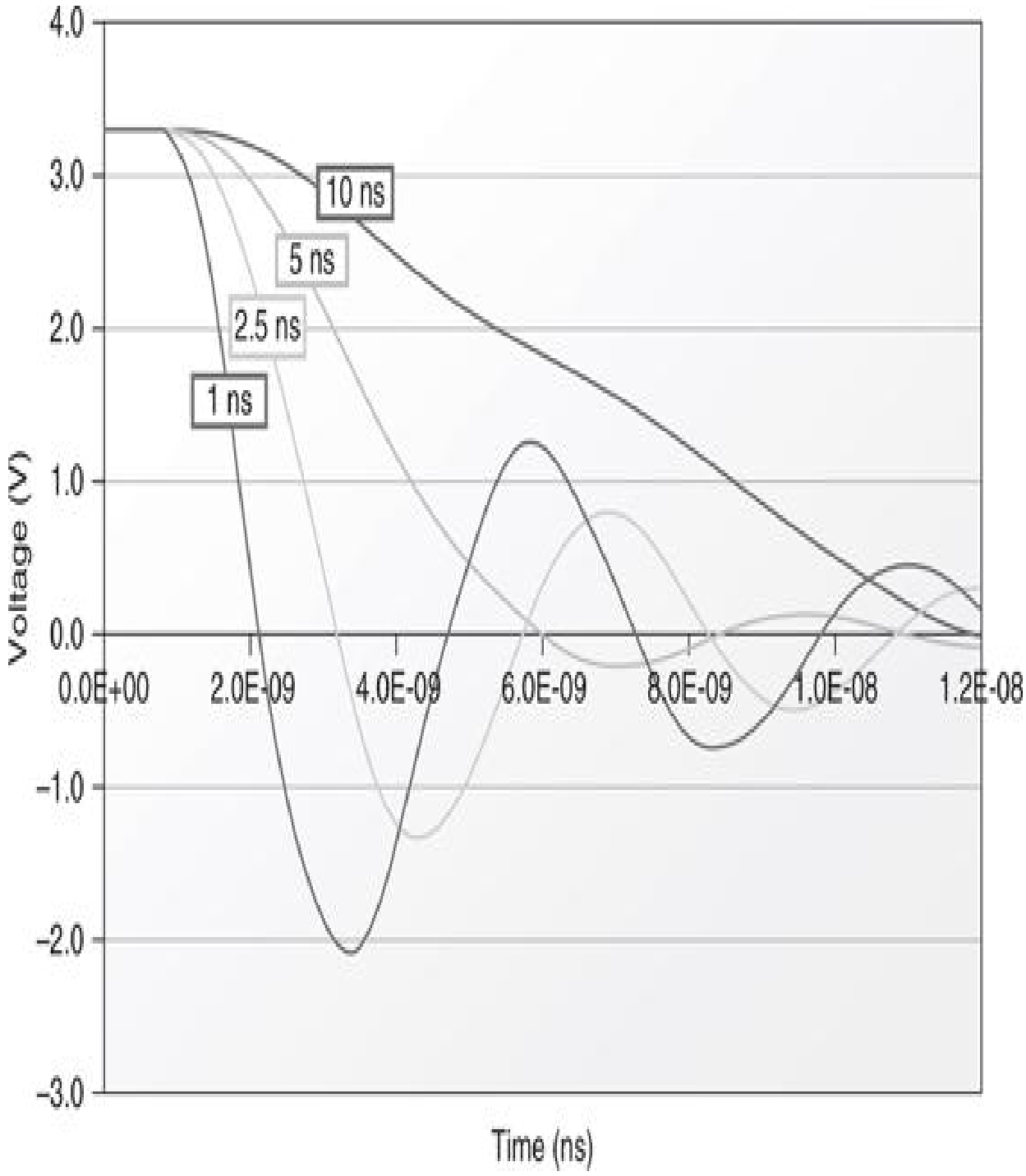


FIGURE 20.10 The effect of driver edge rates on a 5-in trace.

The 10 ns and 5 ns edges look fine, with reflections and ringing effects appearing on the receiver waveforms for the faster 2.5 ns, and 1 ns drivers. For subnanosecond driver switching speeds, receiver waveforms get progressively worse.[9]

20.2.10.2 The Second "T": Topology, Signal Integrity and Timing. Signal integrity problems tend to disappear when nets are short relative to how fast they are driven, as reflections settle much more quickly. Figure 20.11 illustrates this clearly. The 1-ns receiver waveform from Fig. 20.10 provides a point of reference. Recall that the net was 5 in long (127 mm), with a 1.0-ns driver switching speed. Shortening this point-to-point topology to 1 in (25 mm) produced a much better-looking waveform. Shortening this trace to a one-half inch (12.5 mm) produced an even better-looking signal. Though academically instructive, an engineer certainly wouldn't want to specify more than a few carefully planned high-speed nets with a half inch maximum length requirement! Additional alternatives are discussed in the next session, the third "T."

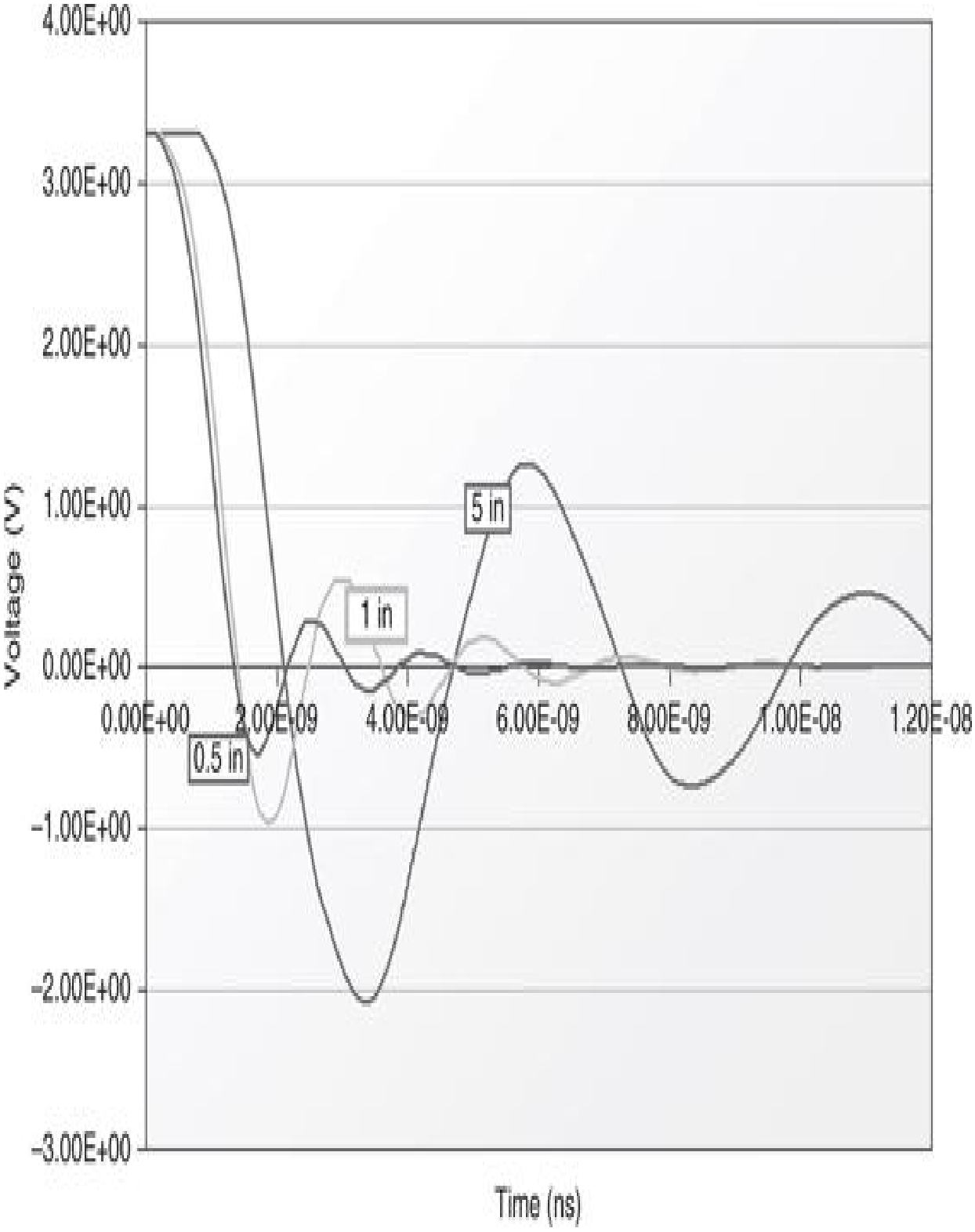


FIGURE 20.11 Shortened trace lengths reduce the impact of reflections on receiver waveforms for a 1-ns driver output.

Sometimes, departures from normal “good-practice” routing can actually be a key to solving tough signal-integrity problems. For example, consider the case of a clock net with multiple receivers, each of which is skew-sensitive (i.e., the clock must arrive at each receiver at very close to the same time). In this case, a daisy-chain route may not be ideal because it delivers the signal to each receiver in a serial fashion, inherently creating skew. Figure 20.12 shows this clearly.

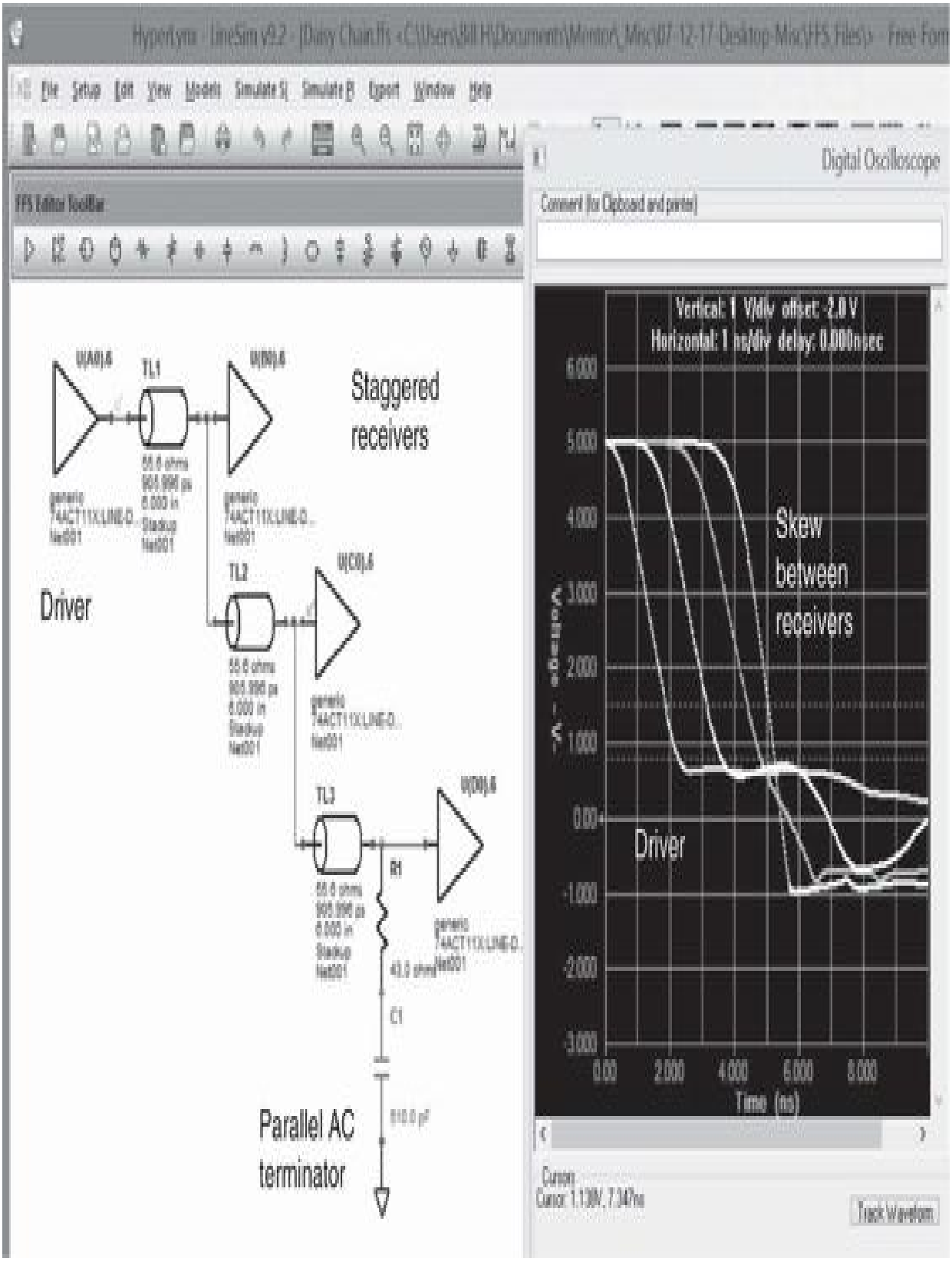

Digital Oscilloscope
Comment (to Clipboard and printer)
Vertical: 1 V/div offset: -2.0 V
Horizontal: 1 ns/div delay: 0.000nsec
Staggered receivers
Driver
Skew between receivers
Parallel AC terminator
Time (ns)
Cursor
Track Waveform

FIGURE 20.12 Daisy chain routing, shown in this transmission-line view, often leads to skew between receivers. (*Simulation courtesy of Mentor Graphics HyperLynx*.)

For cases like this, a superior routing scheme may be a “star” pattern in which each receiver, or small subsets of receivers, has its own routing branch with all branches meeting at or very near the driver IC. Note the advantages of this topology: each receiver can be placed approximately the same delay length from the driver (no skew), and each receiver is considerably more isolated from other receivers than on a daisy chain (reduced susceptibility to receiver-to-receiver reflections).

On the other hand, star routing introduces several new problems. Underscoring the interrelationship and trade-offs associated between the 3T’s, the parallel (star) combination of multiple branches presents the driver IC with a low impedance, meaning that the driver must be capable of dynamically sinking and sourcing a considerable amount of current. In practice, one may need to use a stronger driver technology for this routing topology. For example, a 24-mA driver instead of an 8-mA, as shown in Fig. 20.13. More on this topology in the next section, termination.

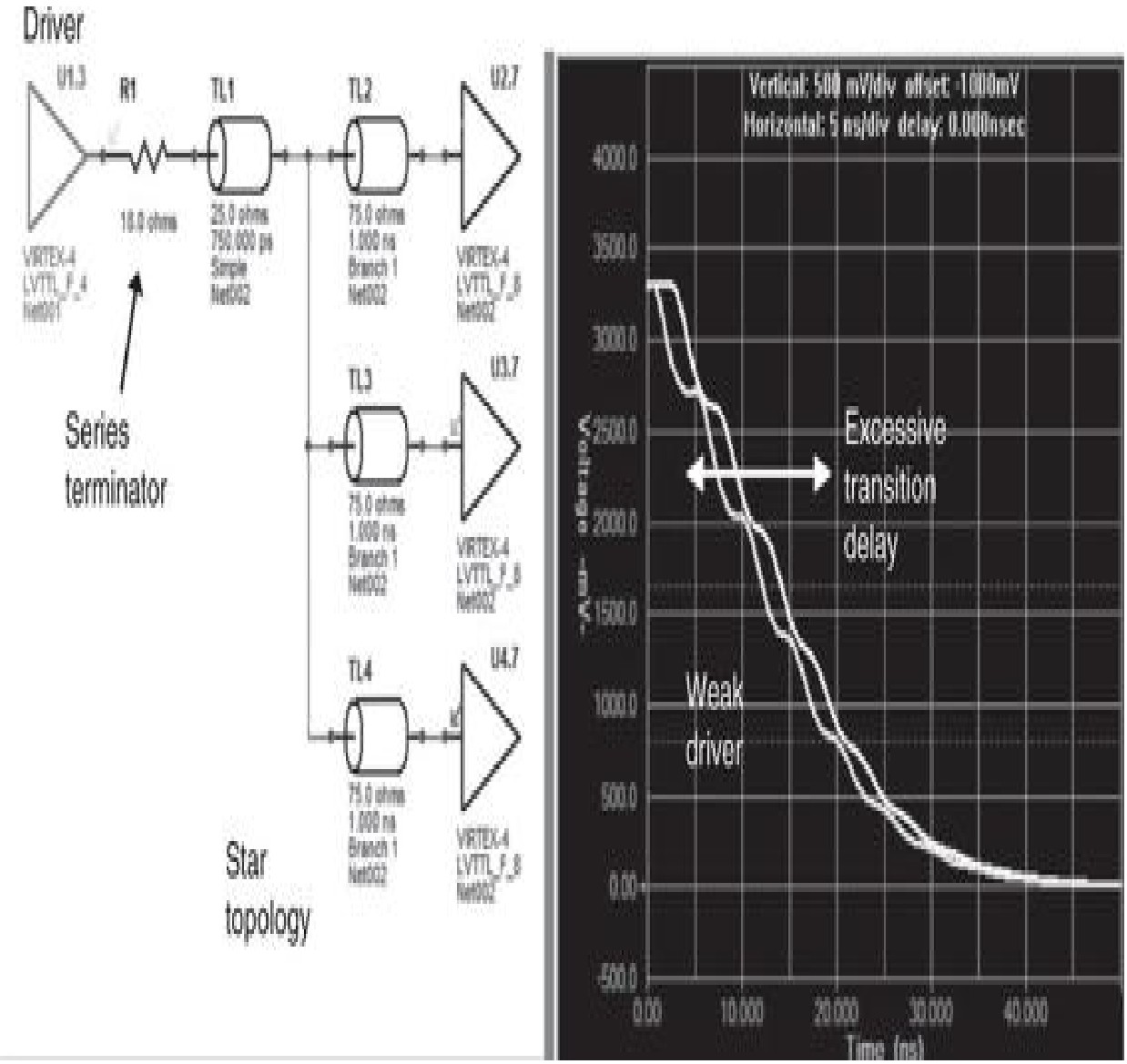


FIGURE 20.13 Loading and trace length determine the drive strength required to reach the desired signal transition at each receiver. Here, we see a driver that is too weak for the parallel, low-impedance star topology. It would be better in this case to use a stronger 24 mA buffer.

20.2.10.3 The Third "T": Termination. The benefits of improved signal quality from optimizing termination schemes on fast-driven signals is absolutely critical—impacting whether the product works at all. When providing termination we must consider:

- Which nets to terminate?

- *Termination strategy*. What type of termination to use is based on routing topology and design requirements?

20.3 WHICH NETS TO TERMINATE AND WHAT TYPE OF TERMINATION TO USE

As a general rule, any line with an edge rate faster than about 5 ns on nets running longer than an inch should be considered a candidate for termination.[1]

The classic methods of terminating transmission lines—where the nets on a digital PCB constitute the lines—are fairly well known. Designers can terminate the source, the far end, both, or employ “distributed” terminations at several locations—for example, in the case of multidrop or daisy chain connections.

Using parallel DC termination, the transmission line is pulled at its far end to a power-supply voltage through a resistor equal in value to the impedance of the line. Parallel AC termination adds a capacitor in series with the DC resistor, to eliminate the DC loading.

Series or “source” termination replaces the end-of-the-line terminator with a resistor at the driver end of the line; the resistor’s value should add to the driver’s impedance to equal the line’s characteristic impedance.

Variations on these methods are possible, too. For example, Thevinin terminations involve two parallel DC terminating resistors pulled to opposite power supplies, to reduce DC current.

There are some basic guidelines when selecting a termination methodology:

- Source termination is useful in point-to-point/one-directional connections.
- Far-end termination is useful in multipoint connections.
- Distributed termination can be helpful if you have a plug-in system with variable configuration.

Each of these techniques has advantages and disadvantages. Parallel DC termination is the simplest scheme, both from the standpoint of component count (only one), and the choice of value (equal to the line impedance), but it burns the most power and may unacceptably load the driver IC. AC termination requires an additional component (more expensive), and additional engineering effort—to find the optimal capacitor value. But the addition of the capacitor does reduce power consumption.

Series termination seems simple (only one component), but it is not always trivial to find the optimal component value because it depends on the driver impedance, which may be unknown, and varies with semiconductor processing. Also, series terminators do not work properly unless the receiver ICs are clustered near the end of the net, because series termination works by creating a voltage “plateau” that persists until a reflection is received back from the end of the line. Receivers midway or near the beginning of a line may experience unacceptable timing results.

Consider the daisy chain topology presented in Fig. 20.12. The waveforms in Fig. 20.14 show a series topology leading to unacceptable skew between the first receiver and the one at the end of the net in a daisy-chain configuration.

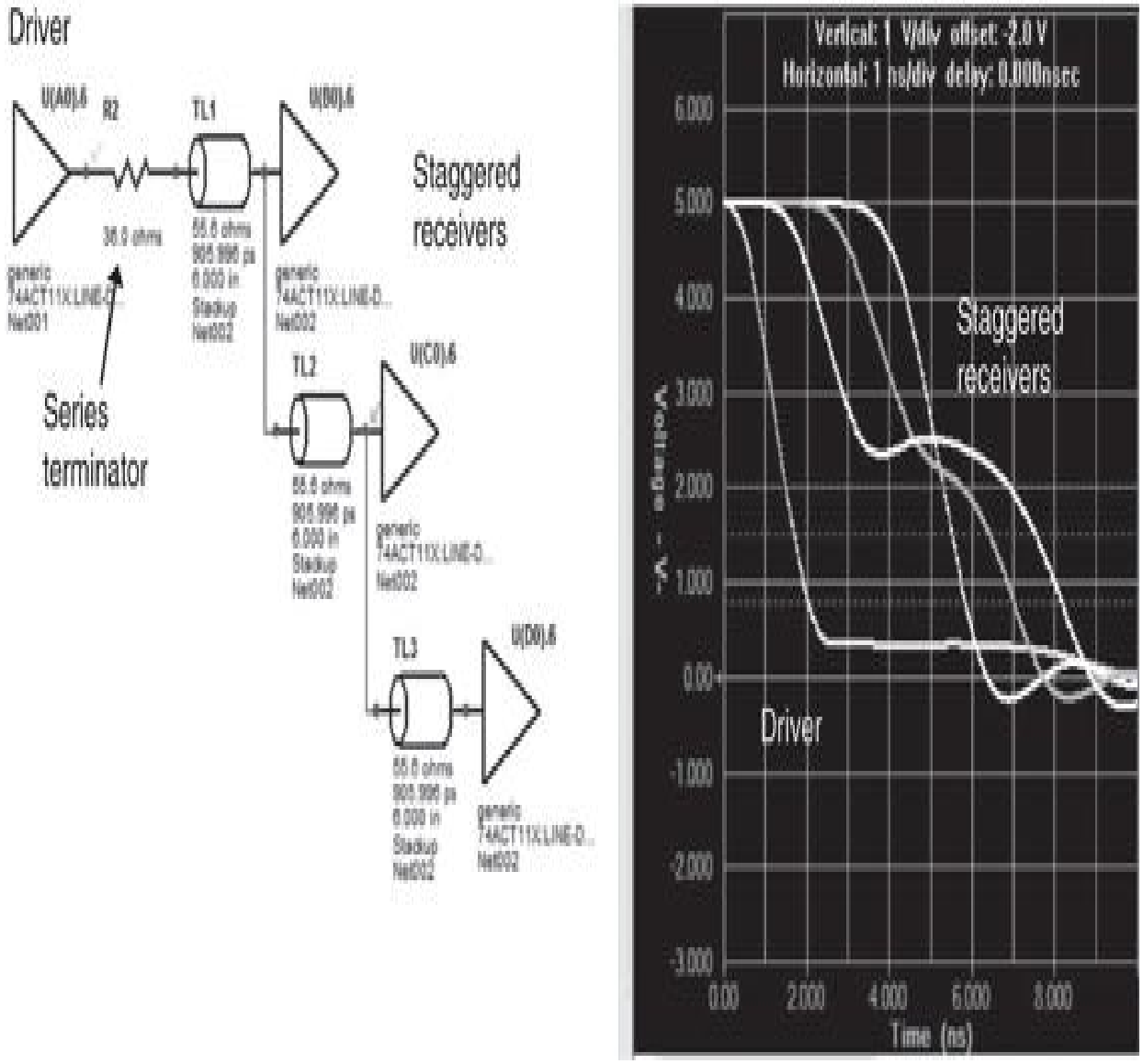


FIGURE 20.14 Series termination causes a voltage plateau at intermediate receivers. Parallel AC termination is generally better suited for daisy-chain topologies.

There are several ways to terminate at a junction or star connection that was introduced earlier. One possibility is a series termination at every driver. This has the advantage of reducing settling time at the receiver, while consuming a minimum amount of power. Several conditions must be met for a single series termination strategy to be effective. First, each branch must be close to the same length in delay terms; otherwise, reflections coming back from each branch

are not in sync and end up “bleeding” from branch to branch. Also, each branch must be the same impedance (or close), or it will not be possible to choose an effective single resistor value. If branches are longer than three-quarters of an inch, it makes sense to make their parallel impedances equal to the inbound line impedance from the driver. If driving from multiple I/Os, consider the distributed termination strategy.

PCB designers can also terminate at the junction itself by changing the trace impedance, or by using parallel DC termination. This method will damp reflections quickly, but will also attenuate the signal.

The appropriate choice of termination depends on network topology and signal direction. For nets that have complex routing patterns where it’s not been possible to conform to a pure daisy-chain route, or where multiple drivers are involved, it may be difficult to find a termination scheme that works, even in theory. This is where a “what if” simulation software can be an indispensable ally in quickly comparing alternatives.

20.3.1 Digital Crosstalk

Crosstalk is unwanted electromagnetic field coupling generated *between* transmission lines—causing unwanted noise generated between signals. It occurs when two or more nets on a PCB are coupled to each other electromagnetically (even though conductively, they’re not connected at all). Such coupling can arise any time two nets run next to each other for any significant length. When a signal is driven on one of the lines, the electric and magnetic fields it generates cause an unexpected signal to also appear on the nearby line, as shown in Fig. 20.15.

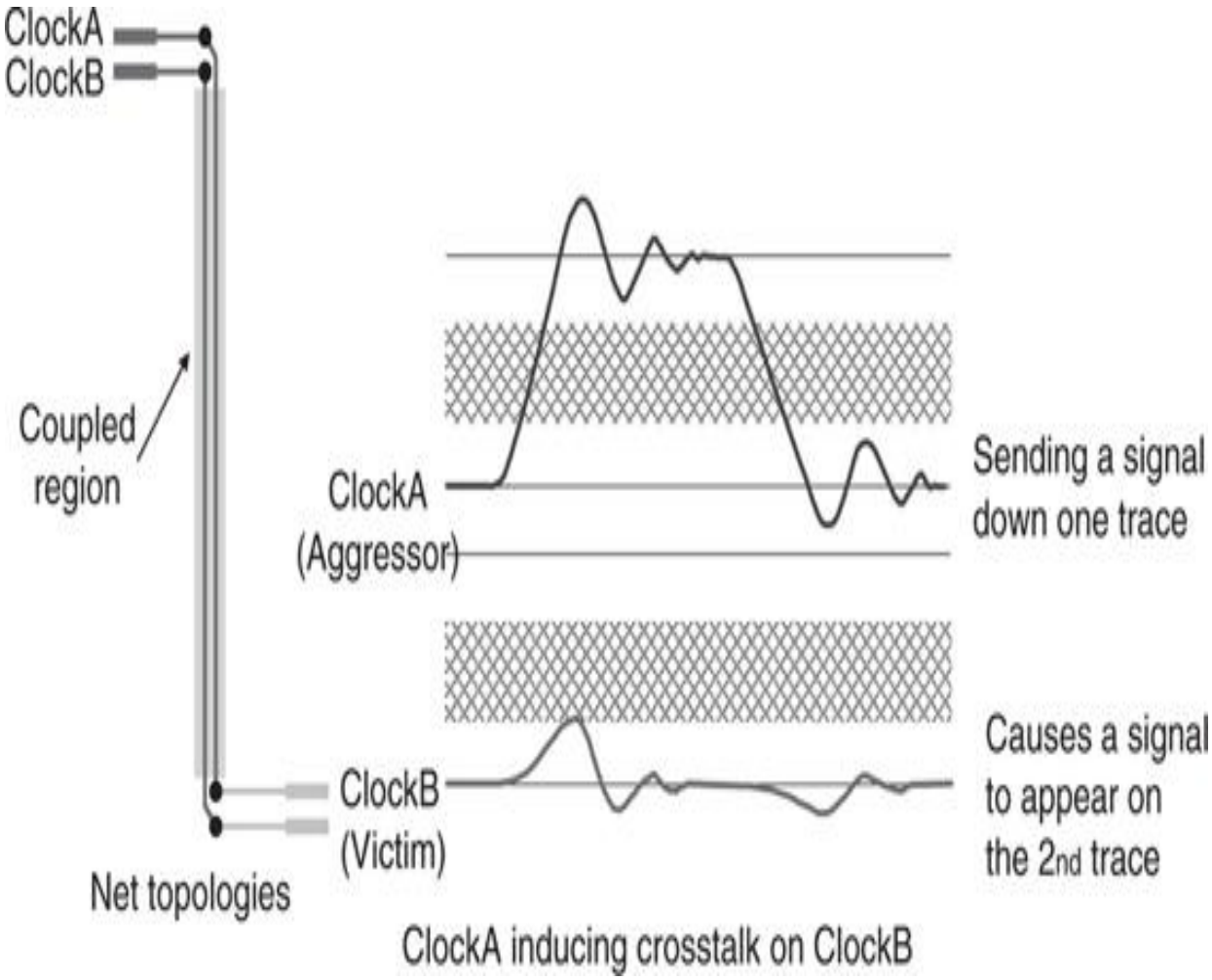
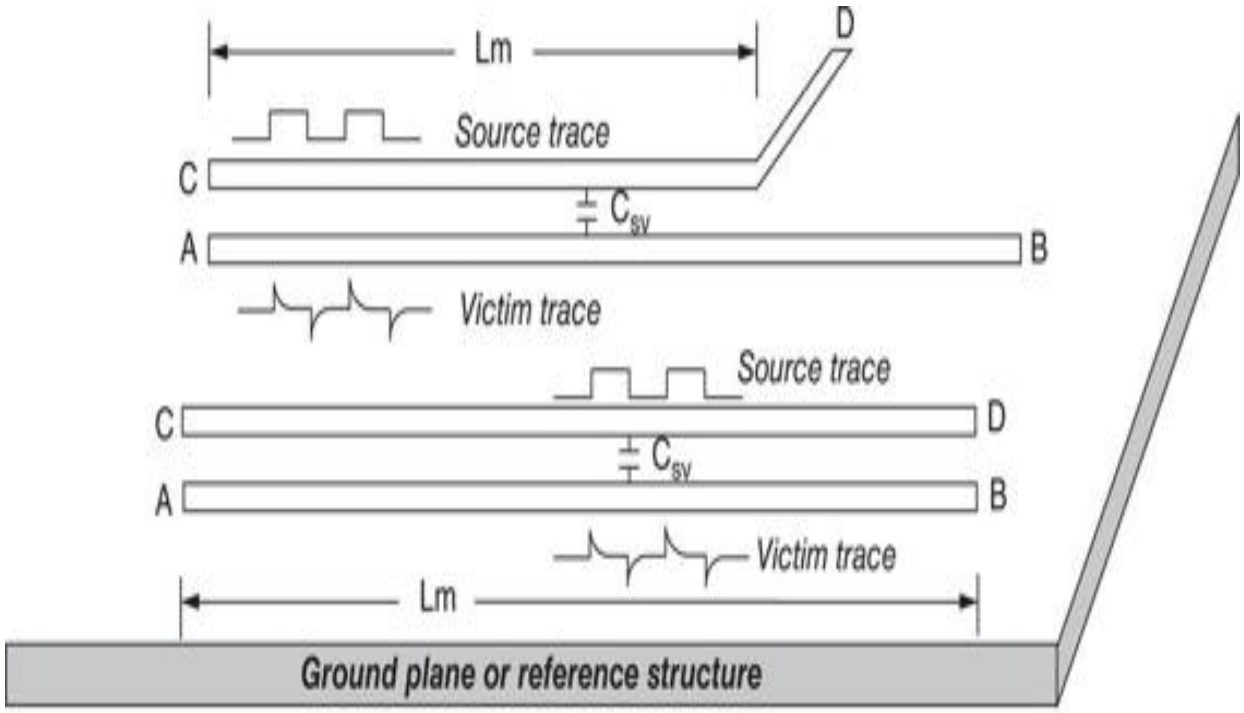
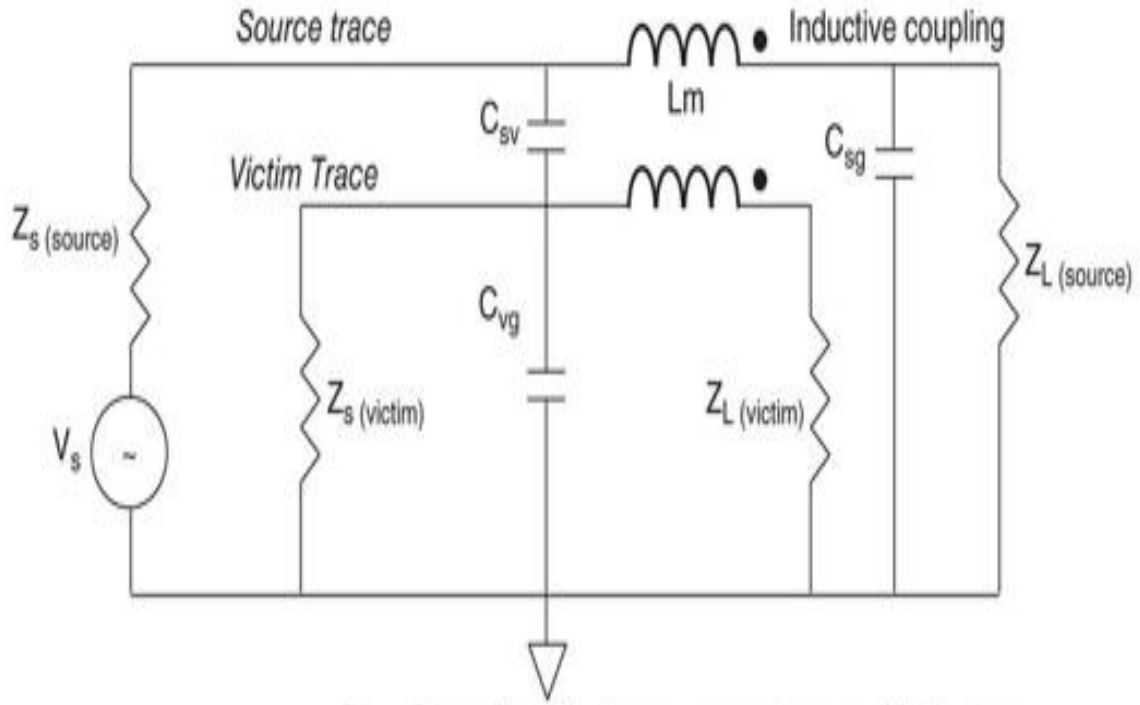


FIGURE 20.15 Crosstalk occurs when two or more neighboring traces couple together.

Crosstalk includes a capacitive element—known as "capacitive crosstalk," and an inductive component—known as "conductive crosstalk."[3] Each of these elements is illustrated in Fig. 20.16.[11] "Source," in this figure, denotes the source of the unwanted crosstalk, or the aggressor signal.





$$Z_v = \frac{Z_{s\,(v)} \times Z_{L\,(v)}}{Z_{s\,(v)} + Z_{L\,(v)}}$$

C_{sv} = Capacitance between source trace and victim trace
C_{vg} = Capacitance between victim trace and ground
C_{sg} = Capacitance between source trace and ground

FIGURE 20.16 Physical and electromagnetic representation of transmission lines that cause crosstalk to occur.[11]

A number of factors combine to create an unwanted crosstalk signal: the length over which the traces are coupled, the distance between the traces, their positions in the PCB stackup, what driver ICs are used on both the "aggressor" and the "victim" lines, whether or not the lines are terminated, and so forth.[2]

Crosstalk is a particularly hard phenomenon to anticipate and control unless you're able to simulate it, because there is almost no way of *intuitively* knowing how much crosstalk voltage and current will develop due to a given coupling. Nevertheless, there are semi-conservative design guidelines that can be useful—though almost always at the expense of board real estate.[10]

Examples include the "3H rule," where traces are spaced at three times the dielectric height, relative to the nearest reference plane; and the "3W rule," where trace spacing is held to three times the trace width. Each of these approaches can widen a bus width considerably.

20.3.2 Description of Crosstalk in a PCB

In crosstalk parlance, the "aggressor" signal or trace switches logic states and may cause a crosstalk event to occur. The "victim" transmission line responds by developing an unintended signal. The effect is three dimensional in nature. Victims can be adjacent, above or below the aggressor, as shown in Fig. 20.17.

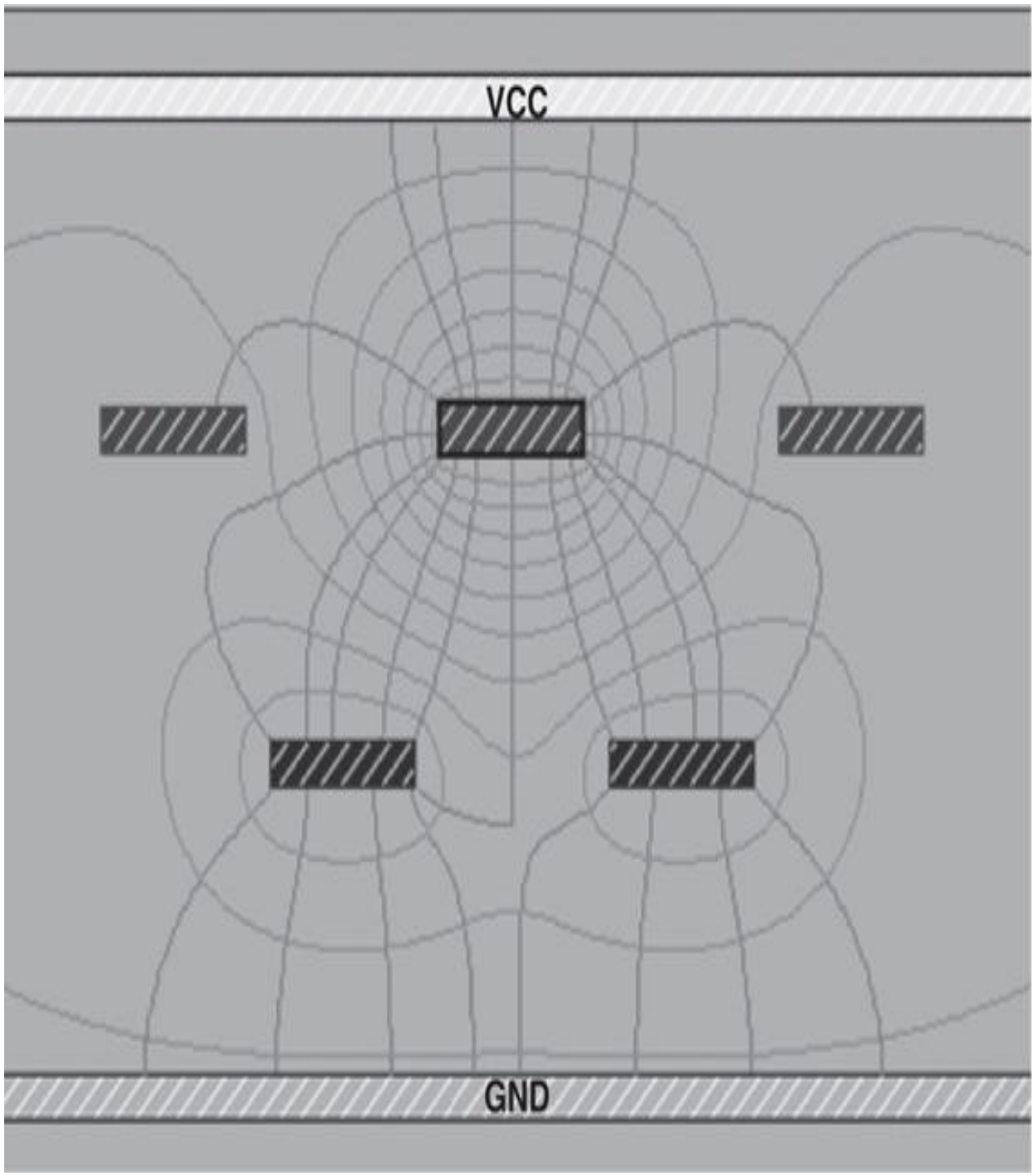


FIGURE 20.17 Victim nets can be above, below, or adjacent to an aggressor net.

Two coupled signals are imposed upon the victim net: a forward signal, and a backwards signal. The “forward” pulse travels along with the aggressor’s signal; and a “backward”

pulse travels back from the aggressor signal. Crosstalk at the victim's far end is called "far end crosstalk," or FEXT, and coupled voltage at the near end is called "near end crosstalk" (NEXT). Figure 20.18 shows both forward and backward crosstalk scenarios.

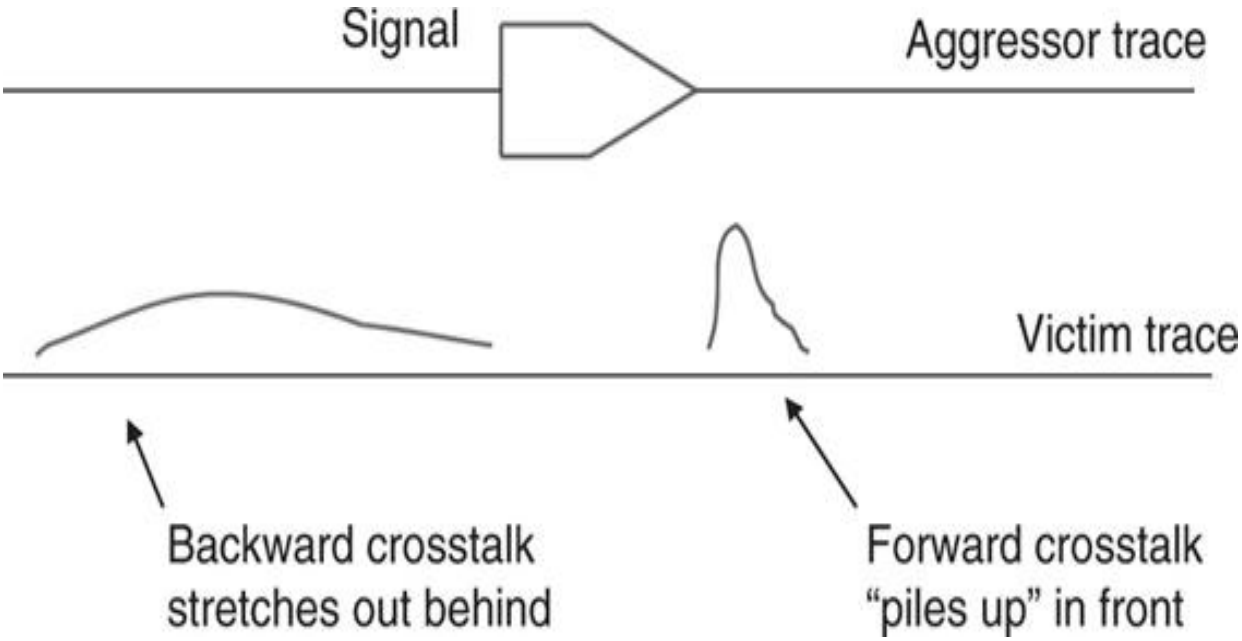


FIGURE 20.18 An illustration of both forward and backwards crosstalk on a victim trace.

The backward signal often ends up traveling forward after reflecting off of a driver. *Current* is injected into the victim by electric fields (the lines that run orthogonal to the traces in Fig. 20.17) that are caused by capacitive coupling interactions traveling between the aggressor to the victim nets. These interactions are effected by surface area and distance, and generally terminate at adjacent conductors.

Voltage is induced upon the victim by magnetic fields. These are inductive (transformer) coupling interactions, which are somewhat circular—surrounding the aggressor and victim nets. These interactions are *not* generally stopped by conductors, and can therefore extend around multiple adjacent conductors.[10]

20.3.3 Guidelines to Minimize Crosstalk

The most common crosstalk design rules involve trace to trace separation. A PCB designer might, for example, set an auto-router to 4-mil trace width, and 4-mil spacing. This will, of course, maximize router completion; but the resulting design will result in 20 to 60 mV of crosstalk. Adjusting noise-sensitive victims to more than 6-mil trace-to-trace spacing can help avoid this problem, as shown in Fig. 20.19.[10]

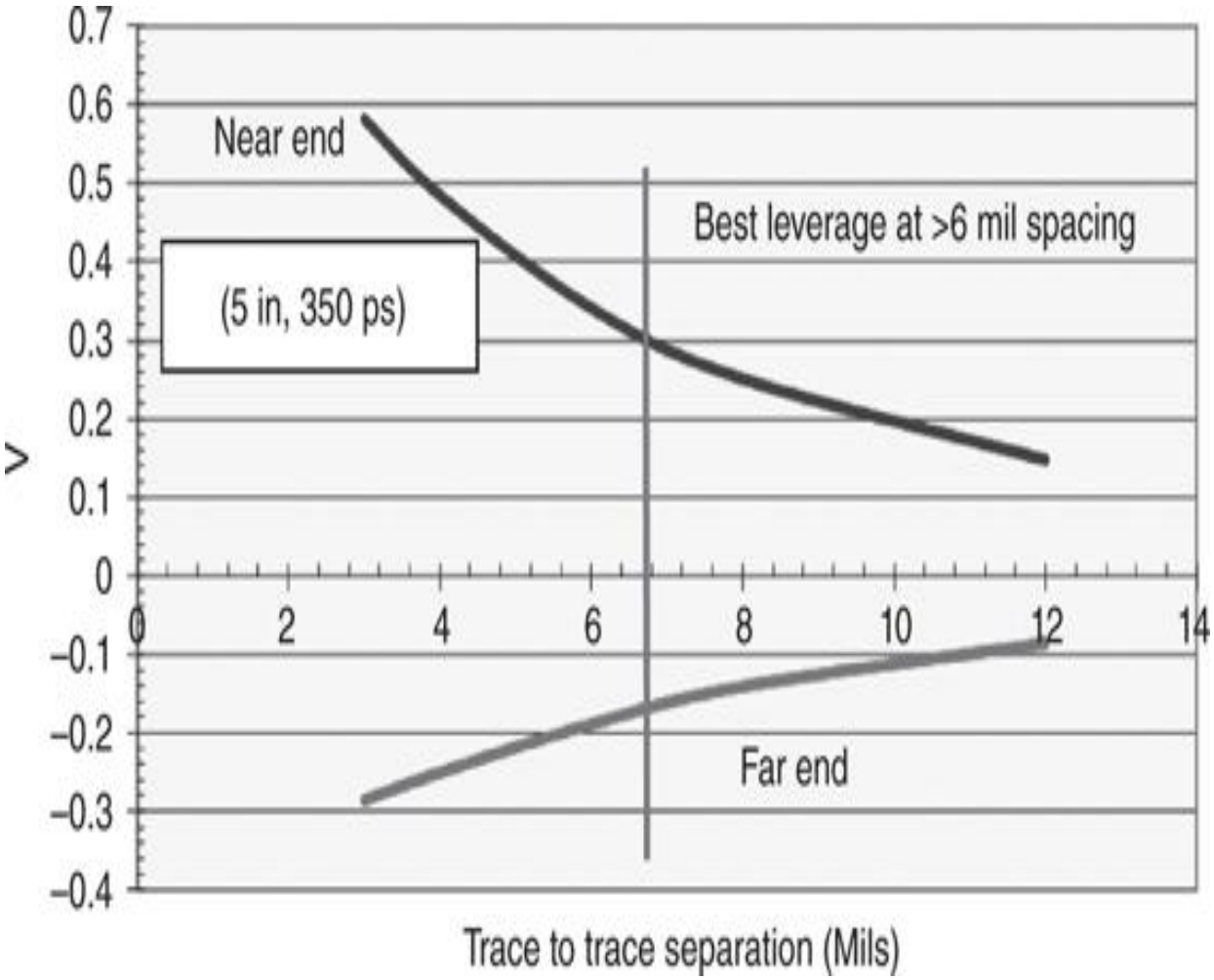


FIGURE 20.19 Using two parallel, 5-in lines, the graph shows the curves for NEXT and FEXT beginning to flatten out at around 7-mil spacing between aggressor and victim nets. Tighter spacing, to the left of the vertical line, results

in more crosstalk, and wider spacing—to the right side of the vertical line will result in diminishing benefit.

20.3.4 Dielectric Effects and Reference-Plane Distance

Since electric fields terminate at reference planes, traces physically close to reference planes have reduced crosstalk. Capacitive trace-to-trace coupling drops off quadratically with the distance from the reference plane(s)—so traces within 4 mils of a reference plane will be much more immune to crosstalk than a trace 6 or more mils from the nearest reference plane. And symmetric striplines—because of their relative proximity to not one, but two reference planes—have relatively higher immunity than microstrip signals.

Moreover, there's a dielectric constant effect to consider. High dielectric constants (Dk), concentrate the electric field, resulting in relatively poorer crosstalk performance, in a roughly linear relationship between Dk and capacitive crosstalk.

20.3.4.1 Example: Crosstalk on a Bus. The following process ensures no more than 200 mV of crosstalk can occur between transmission lines.

A typical bus in a modern digital system contains many physically parallel traces—16, 32, 64 or more. To analyze crosstalk on such a bus, you can narrow the scope to a single "victim" trace, with "aggressor" nets on either side.

Starting with coupled, coplanar 6.0-mil wide (W) (0.15 mm) stripline traces running parallel for 12 in (305 mm) with trace-to-trace separation of 8.0 mils (S) (0.208 mm), the dielectric constant (Dk) is 4.3, with a height (H) of 5.0 mils (0.127 mm), as shown in Fig. 20.20.

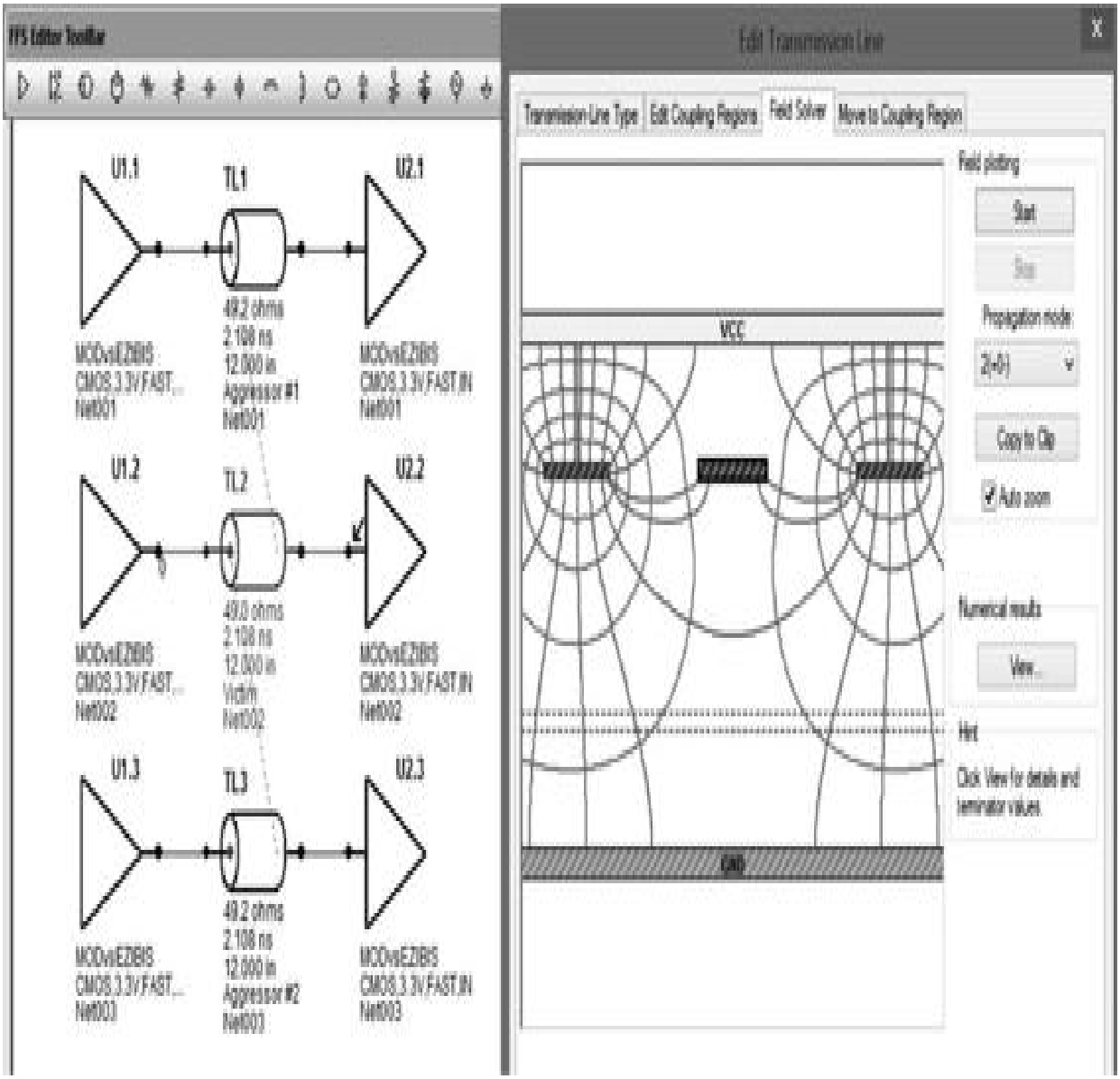


FIGURE 20.20 Crosstalk is easily illustrated with the aggressor-victim-aggressor example shown. (*Shown with Mentor Graphics LineSim*.)

Simulation results from Mentor Graphics LineSim, are shown in Fig. 20.21 using the parameters above. In the figure we clearly see far-end crosstalk based on this configuration.

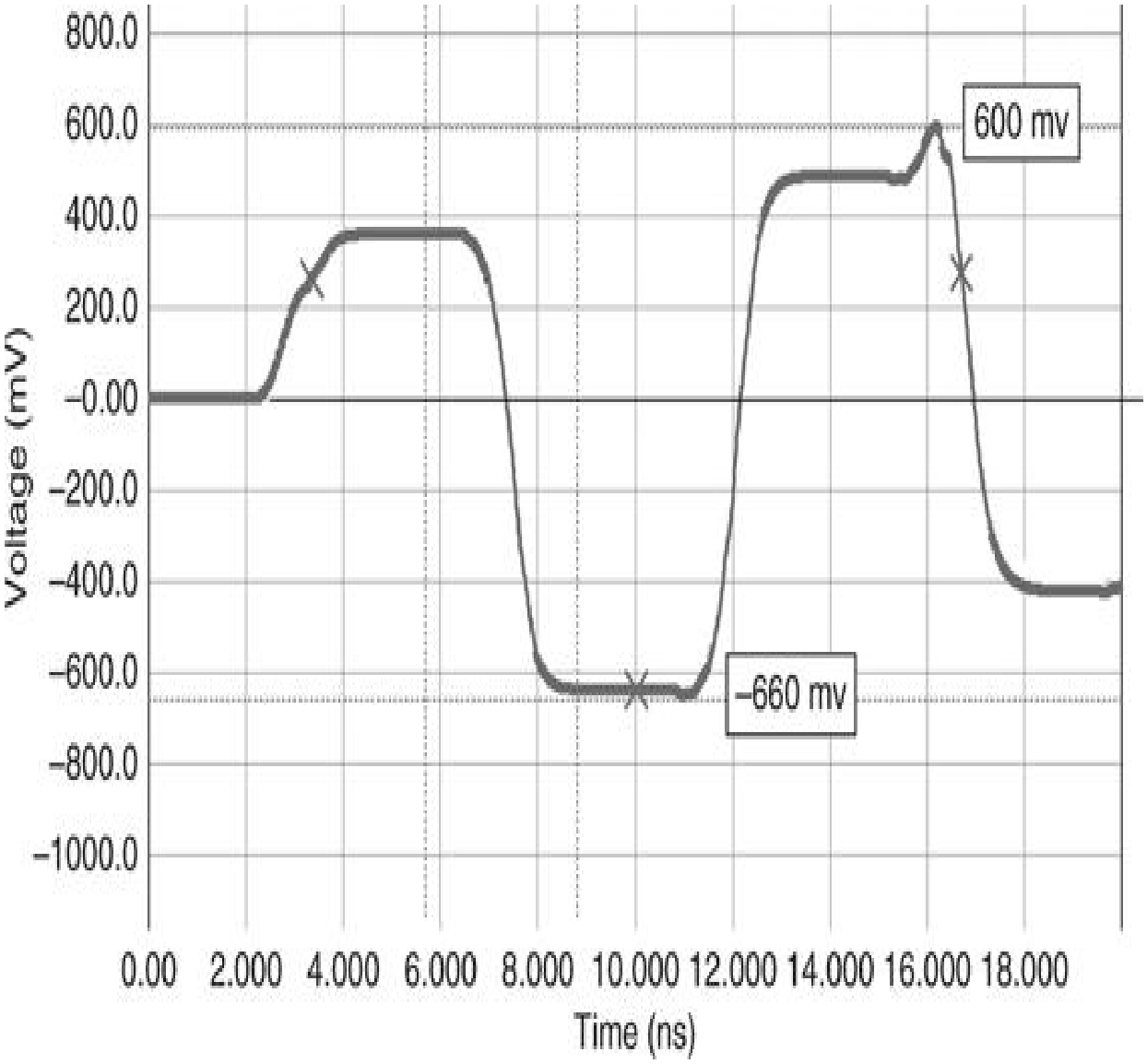


FIGURE 20.21 Far end crosstalk (FEXT) on the victim net shown in Fig. 20.20.

With 590 ps (0.59 ns) driver-switching speeds on the two aggressor nets, and no signal injected on the victim net, we have about 600 mV on the positive side that will be injected into the far-end victim waveform; and 660 mV on the negative side—both well beyond our design criteria of 200 mV maximum crosstalk.

Crosstalk is a complex effect that is influenced by many different geometric factors: for example, driver-IC technology (Tr, Tf, output impedance and drive strength), trace width

(W), copper weight (T), parallel-line length (Lp), trace separation (S), PCB stackup (layer ordering, Dk, and dielectric thickness, H), and line-end termination (crosstalk generally requires more-complex termination than single-line reflections).

Rules-of-thumb exist for controlling crosstalk, but if you really want to know how to minimize crosstalk while controlling cost on your specific design, you need a good simulation tool. In the following section, we'll go through an iterative process for dealing with crosstalk on the design in Figs. 20.20 and 20.21.[10]

20.3.5 Copper Thickness

A crosstalk lever that might be overlooked sometimes is the copper thickness. Up until now, signals have used 1 oz copper. One might think that reducing copper thickness will reduce capacitive coupling, though simulation shows that the result doesn't turn out to be significant in practice. Nevertheless, for the remainder of this discussion, we'll half-ounce copper in the analysis.

20.3.6 Reducing Parallel Coupling Length to Decrease Crosstalk

One common technique for reducing crosstalk is to reduce the length over which aggressors and victims run parallel to one another. This poses some practical problems on the routing side—as those traces ended up being parallel on a board for a reason—but it's instructive to see what happens when the parallel coupling region is reduced by 50 percent, from 12.0 in (305 mm) to 6.0 in (152 mm). Surprisingly, this change does not end up reducing crosstalk at all—simply moving peak crosstalk amplitudes to the left in the time

domain. Reducing parallelism alone, as a crosstalk lever, isn’t quite as powerful as we might think it is.

20.3.7 Increase Trace Separation to Decrease Crosstalk

Another common technique to decrease crosstalk is to increase the separation, S, between the traces. Increasing trace separation from 8 to 12 mils results in a reduction of crosstalk to 400 mV on the positive side, and −400 mV on the negative side—still well beyond where we would like to be; and in the process of making this change we’re using up a good bit more board space.[3]

20.3.8 Modifying the Dielectric Material

There are many ways besides trace separation and parallelism to affect crosstalk values. One that is sometimes overlooked is the PCB stackup assignment and where the trace is routed relative to a reference plane. Recall that we started with a Dk = 4.3. What happens if we try to reduce capacitive crosstalk by using a lower-Dk material, say D = 3.8?[3] Through simulation, it turns out that the improvement from this change alone is negligible; however, in the process of using half-ounce copper, and reducing the capacitance (Dk) of the dielectric, trace impedance increased from roughly 50 Ω to just under 57 Ω. (Remember: Impedance is inversely related to the square root of trace capacitance, which is tied to the capacitance of the dielectric.) So, reducing the dielectric thickness (H) from 5.0 mils to 4.5 mils between the stripline layer of interest, and the nearest reference plane increases the capacitance again, pulling the impedance back to around 50 Ω. The combination of these

factors gets us much closer to our goal, resulting in 211 mV on the positive side down to about 230 mV—more than a 60 percent improvement, but still above our target of 200 mV.

Reducing trace width (W), which increases impedance (Z_0), and then narrowing the dielectric thickness (H) to pull the impedance back down to around 50 Ω is another potential way to reduce crosstalk. Reducing width (W) to 5.0 mils (0.127 mm), and height (H) to 3.75 mils (0.95 mm) results in roughly 200 mV of both positive and negative crosstalk.

By narrowing trace width (W) to 5.0 mils (0.127 mm), the overall bus with will decrease by the number of bits minus 1. With an interest in gaining more margin—while keeping the overall bus width in line with the original width—adding another mil to the spacing [i.e., taking S from 8.0 (0.203 mm) to 9.0 mils (0.228 mm)] results in plenty of margin: 160 mV on the positive side, and 170 mV on the negative side.

Table 20.1 summarizes effects on the topology in Fig. 20.20, and their relative impact on FEXT—ranked by relative reduction in worst-case crosstalk.

TABLE 20.1 Simulation Results for Reducing the Crosstalk Shown in Figs. 20.20 and 20.21

Rank	Description	FEXT Reduction, %
	Original configuration: W = 6 mils; T = 1 oz; Lp = 12 mils; S = 8 mils; Dk = 4.3; H = 5 mils	0
	Reduce copper thickness (T) to ½ oz	~0
	Reduce parallel length (Lp) from 12 to 6 mils	~0
4	Increase trace separation (S) from 8 to 12 mils	~33
	Reduce capacitive crosstalk: Dk = 3.8	~0
3	T = ½ oz; Dk = 3.8; H = 4.5	~60
2	Reduce W from 6.0 to 5.0 mils, and H to 3.75 mils	~65
1	Reduce W from 6.0 to 5.0 mils, H to 3.75 mils, and increase S to 9.0 mils	~75

Reducing trace width (W), which increases impedance (Z_0), and then narrowing the dielectric thickness (H) to pull the impedance back down to around 50 Ω is another potential way to reduce crosstalk. Reducing W to 5.0 mils (0.127 mm), and H to 3.75 mils (0.095 mm) results in roughly 200 mV of both positive and negative crosstalk. By narrowing trace width (W) to 5.0 mils (0.127 mm), the overall bus with decreased by the number of bits minus one.

Figure 20.22 shows the top four ways of reducing crosstalk on this particular bus design. The resulting design rule is to use W = 5.0 mils (0.127 mm), Dk = 3.8, H = 3.75 mils (0.095 mm), and S = 9.0 mils (0.228 mm).

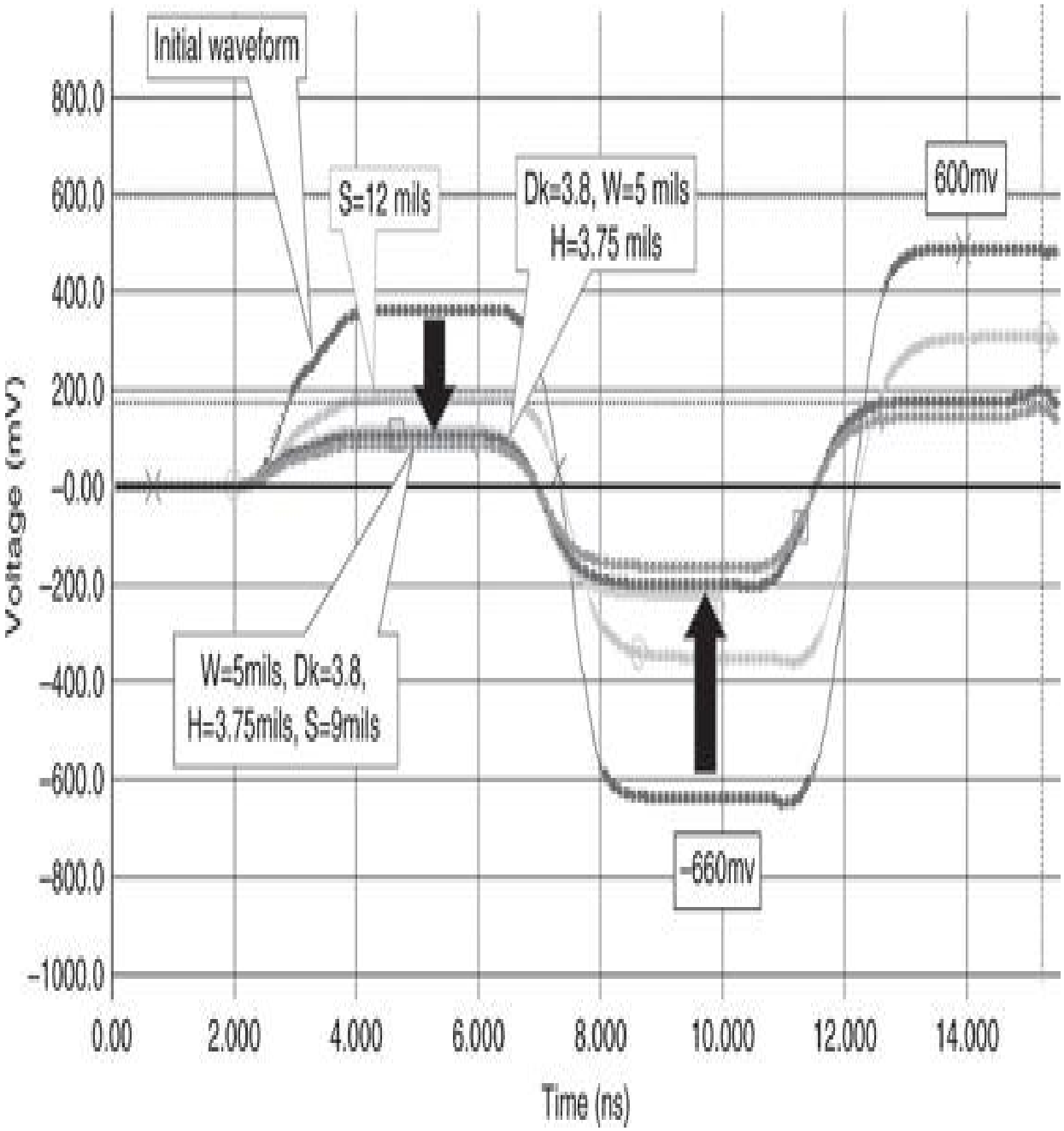


FIGURE 20.22 Top four ways of reducing crosstalk on Fig. 20.20 bus design. Resulting design rule is W = 5.0 mils, Dk = 3.8, H = 3.75 mils, and S = 9.0 mils.

20.4 INTRODUCTION TO DIFFERENTIAL SIGNALING

The single-ended, high-speed buses that have been discussed in this chapter so far persistently became wider and faster over the years until signal integrity issues, such as skew, crosstalk, SSN, and similar concerns forced a fundamental change in signaling strategy in the mid-1990s. This is when *low-voltage differential signaling* (LVDS) was introduced by integrated-circuit manufacturers as an alternative to "single-ended signaling," primarily for the rejection of common-mode noise.

In a differential signal, the driver IC, ideally, sends perfectly matched signals of opposite polarity down two well-matched lines, or as close to identical as possible. The *difference* in amplitude between these two signals, one positive and the other negative, is what the receiver sees as the incoming signal. A key reason for this approach is to combat *common-mode noise*. It is the same principle used with a noise-canceling microphone, which picks up ambient noise, inverts it, and feeds it into the microphone with the sender's voice to cancel it out.

The goal is for near-complete symmetry between the incoming signals, both in terms of timing (propagation delay) and voltage. To achieve this, the following factors should be considered:

- Trace-length matching is important.
- External noise, such as crosstalk should be symmetrical.
- The glass weave under each half of the "differential pair" should be the same … If it's not, we refer to the timing difference as "glass-weave skew" (typically measured in ps).

Figure 20.23 shows single-ended receiver waveforms that a differential receiver reads as V_{diff}, the difference between D+ and D−. If everything is designed properly, the AC common-mode noise at the bottom of the figure will be minimized.[12]

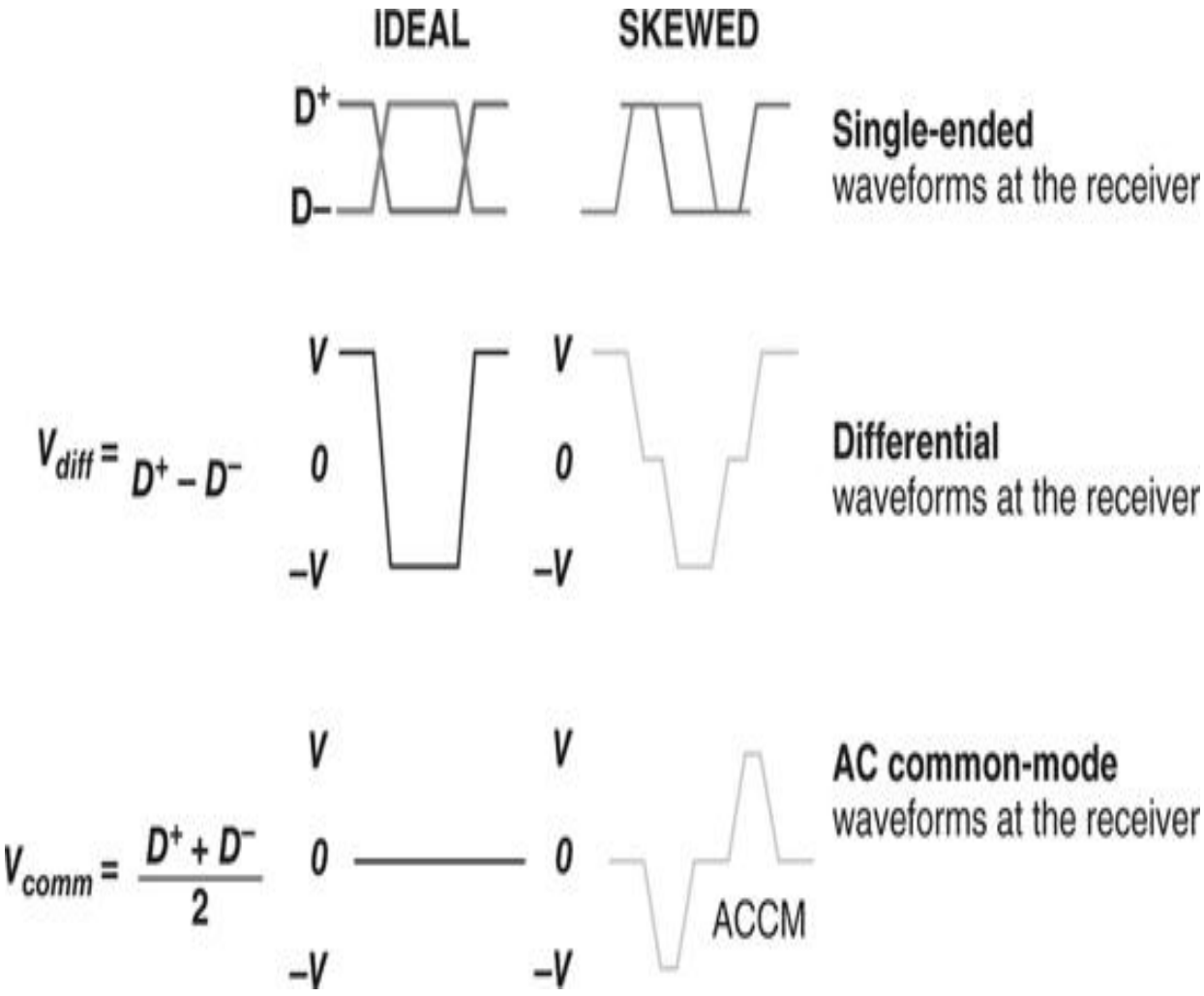


FIGURE 20.23 Single-ended receiver waveforms that the differential receiver read as V_{diff}, the difference between D+ and D−. If everything's designed properly, the AC common-mode noise at the bottom of the figure will be minimized.

With a differential signal, an external noise source such as a CMOS driver in close enough relationship for crosstalk to occur will couple into both halves of the differential pair (roughly) equally. Most differential component providers recommend differential impedances (Z_{diff}) at 100 or 85 Ω for optimal noise cancelation and performance.

20.4.1 Introduction to Multi-Gigabit-per-Second SERDES Signaling

The common-mode noise rejection benefits provided by LVDS were helpful, and differential signaling became an industry standard as a result, however differential signaling alone was not enough to solve the growing speed problem.

Initially, only clocks used differential signaling; when source-synchronous logic like early DDRx architectures began to become prevalent in the late nineties—data lines went differential, and data paths became narrower—presenting a hybrid form of signaling between old parallel (single-ended) architectures and fully asynchronous approaches.[13]

As a result, the networking/computer industry began turning away from parallel signaling to asynchronous serial interconnects—with embedded clocks—utilizing techniques that have been used in telecommunication and military applications for years.

Figure 20.24 shows a contrast between a wide, parallel bus interface, with an external clock, and a differential, serial architecture—with the clock embedded in the bit stream.[13]

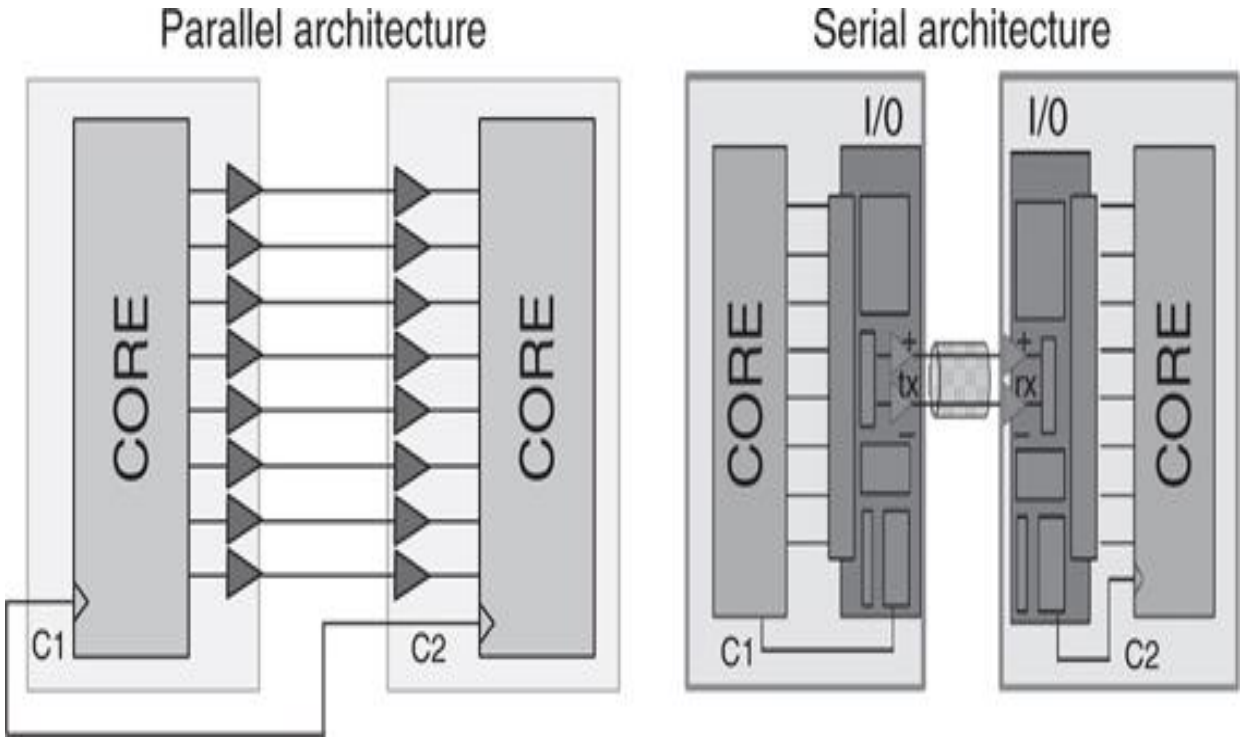


FIGURE 20.24 A graphical representation of the architecture of a wide, parallel bus is compared to a differential, serial architecture.

For signals faster than 1 GHz, transmitted for distances longer than 10 in (25.4 cm), loss is the principal signal-integrity concern. A super-fast driver edge will emerge from the end of the transmission path with reduced amplitude and a slower rise time. This effect becomes particularly serious when the degraded rise time is comparable to the bit period of the signal. Inter-symbol interference (ISI) results when the shape of the received waveform becomes dependent on the prior combination of bits.

20.4.2 Balancing a Loss Budget

The most general way to control loss on a backplane is to avoid impedance discontinuities through transitions. This means keeping the same ratio between *L* and *C* throughout the signal path.

Every link needs a link budget, with typical end-to-end attenuation budgets for multi-gigabit-per-second SERDES links ranging from 10 to 15 dB, or lower with equalization at the receiver.[14]

As with any budgeting exercise, exact (dB) figures for each item are not required, but it is important to have a budget for each major element. If you are hunting for the last decibel, just knowing that one part of the system is twice as important as another. This provides a huge design benefit as far as knowing where to focus engineering resources.

A component manufacturer will typically explicitly specify a loss budget for the component. It is also possible to derive the budget. The relationship for estimating an interconnect loss budget is[15]

$$\text{Attenuation budget (dB)} = 20 \times \log\left(V_{\text{RX,min}}/V_{\text{TX,min}}\right)$$

This loss figure reveals attenuation requirements before employing preemphasis or equalization. At a high level, there are two areas on a backplane interconnect where loss can occur:

- Transition regions that include the BGA package, vias, and connectors
- The line card and the backplane itself

20.4.3 Loss at Backplane Interconnect Transitions

A BGA package represents a very small piece of the overall loss budget, typically 0.5 dB or less on each end at frequencies below 2 GHz. At 3.0 GHz, each package would contribute 0.8 dB to total channel loss.

Connectors in a high-speed system take another chunk out of the loss budget. As a general rule, look for connectors with

a differential impedance of 85 to 100 Ω, this will result in well under 3 dB of loss at the target frequency.

At gigabit rates, poorly designed vias can contribute 0.5 to 1.0 dB of loss, each, against the total loss budget. The degradation effects posed by vias are influenced by the unique characteristics of each individual via, including the proximity of nearby return paths, the number and location of pads in the pad stack, pad size and shape, the layers on which the traces connect and the associated via length (through, blind or buried), spacing between differential vias and "stubs" (that is, any portion of the via that is not necessary for signal transmission).

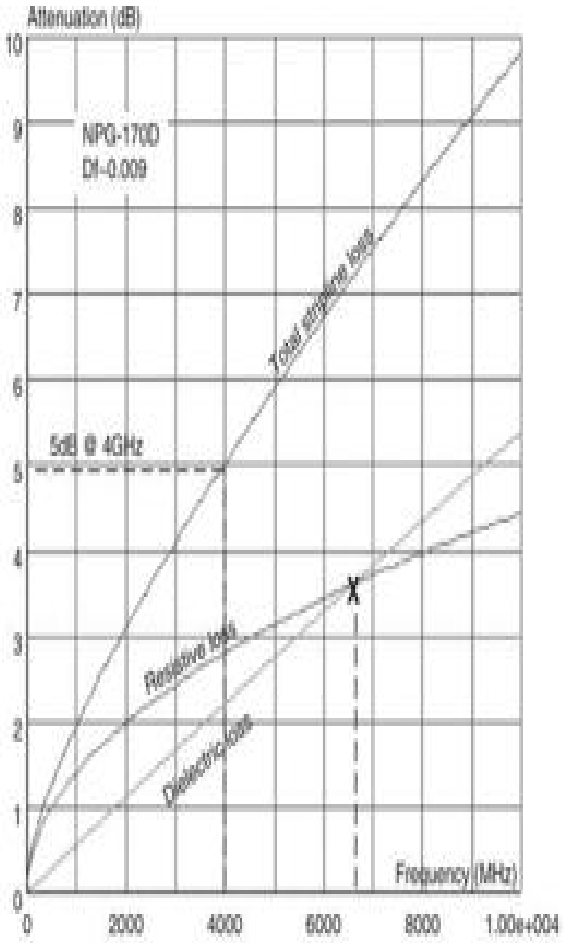
Approaches for mitigating the negative effects of vias include blind and buried vias (shorter than through-hole vias), backdrilling, using smaller pads and only the pads that are needed, using large antipads, and carefully locating bypass capacitors and stitching vias close to vias on high-speed nets. These techniques can reduce via effects to less than 0.25 dB.[14]

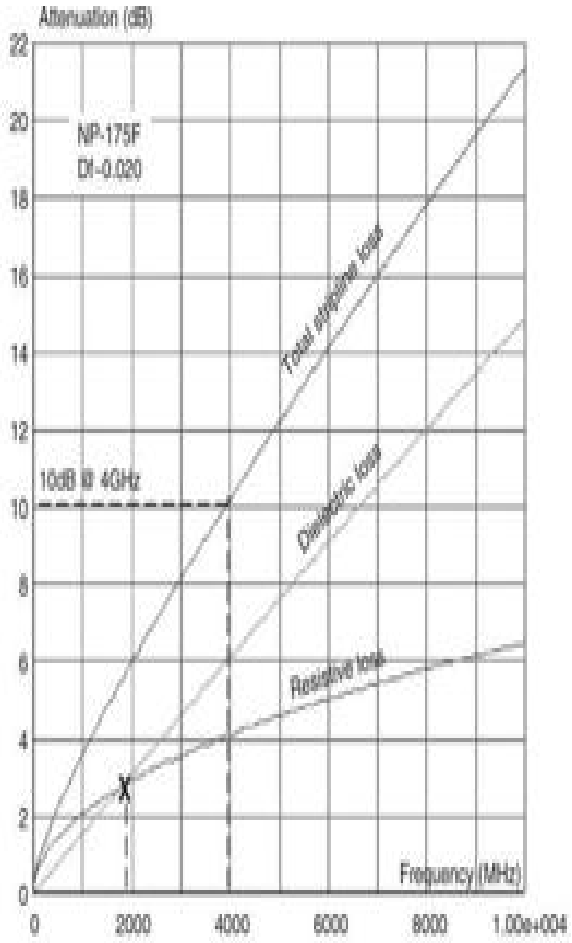
20.4.4 PCB Interconnect Loss

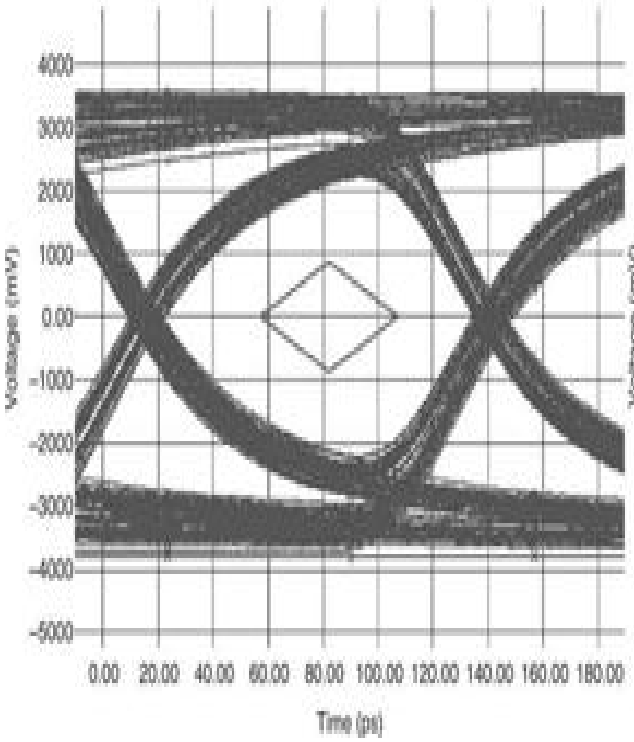
There are three primary ways to control PCB interconnect loss:

1. Reduce resistive loss by widening traces. "Skin effect" is the result of reduced cross-sectional area in a trace, so this solution is somewhat self-explanatory. Trace width changes tend to be relatively more effective at reducing loss at frequencies below the cross-over frequency discussed below.
2. Reduce dielectric loss using low-loss dielectrics. To reduce dielectric loss, consider more expensive materials with lower loss tangents—typically represented as "Df," or "dissipation factor."

3. Reduce dielectric loss and resistive loss by shortening lines. Dielectric loss is a function of the material used and the length over which a signal is transmitted. Resistive loss is tied to the line width and the line length. An example of this is shown on the left in Fig. 20.25.


Attenuation (dB)
NPG-170D
Df=0.009
5dB @ 4GHz
Total dielectric loss
Resistive loss
Dielectric loss
Frequency (MHz)
0
1
2
3
4
5
6
7
8
9
10
0
2000
4000
6000
8000
1.00e+004


Attenuation (dB)
NP-175F
Df=0.020
10dB @ 4GHz
Total dielectric loss
Dielectric loss
Resistive loss
Frequency (MHz)
0
2
4
6
8
10
12
14
16
18
20
22
0
2000
4000
6000
8000
1.00e+004


Voltage (mV)
4000
3000
2000
1000
0.00
-1000
-2000
-3000
-4000
-5000
0.00
20.00
40.00
60.00
80.00
100.00
120.00
140.00
160.00
180.00
Time (ps)

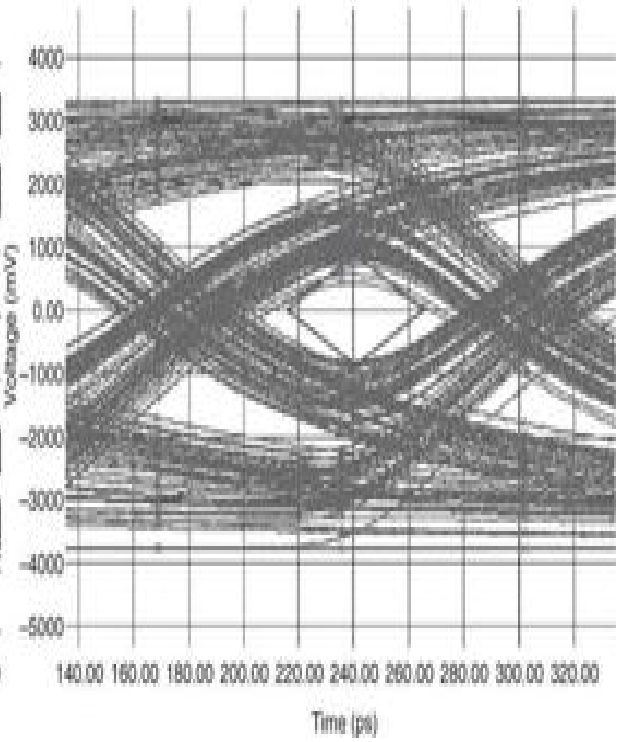

Voltage (mV)
4000
3000
2000
1000
0.00
-1000
-2000
-3000
-4000
-5000
140.00
160.00
180.00
200.00
220.00
240.00
260.00
280.00
300.00
320.00
Time (ps)

FIGURE 20.25 *Top*: Loss (dB) as a function of frequency for two differential, stripline channels with different materials, lengths, and slightly different stackup cross sections. The view to the left has a total stripline loss of 5 dB (not including vias and BGA breakouts), and the view to the right shows a higher-loss material with 10 dB of total loss. *Bottom*: The resulting eye diagrams, with a PCI Express eye mask for reference. (*Simulations with Mentor Graphics HyperLynx*.)

Figure 20.25 shows two sets of loss curves, as a function of frequency, and consideration for a few of the different types of loss, resistive, which includes skin effects; and dielectric loss, which is tied to material properties. The view to the left shows 5.0 dB of total loss through a 12-in differential pair. The second example shows 10.0 dB of total loss through a similar stripline, but using a higher-loss dielectric material, and 17-in differential traces. This view of a transmission-line cross-section is useful for tasks such as stackup planning, loss budgeting, and material selection. Using this or a similar software tool, a designer can quite easily gain an understanding of the PCB trace components of your loss budget. Depending on the trace properties, it's reasonable, as these examples show, to design in trace losses that vary pretty widely, resulting in eye patterns that are quite different. The open eye shows quite a bit of margin with respect to the diamond shaped PCI Express eye mask.

5.0 dB Example: 12-in stripline trace, *W* = 4.5 mils, Er = 3.75, loss tangent = 0.009*
Loss results (at 4 GHz): Loss_{TL} = 5.0, loss_{Res} = 2.9, $\text{loss}_{\text{Dielectric}}$ = 2.1 dB
Crossover frequency = 7.86 GHz
*Nan Ya NPG-170D halogen free

10.0 dB Example: 17-in stripline trace, *W* = 4.5 mils, Er = 3.9, loss tangent = 0.02*
Loss results (at 4 GHz): Loss_{TL} = 10.0, loss_{Res} = 4.0, $\text{loss}_{\text{Dielectric}}$ = 6.0 dB
Crossover frequency = 1.78 GHz

*Nan Ya NP-175F FR-4

Below the crossover frequency (the point at which dielectric loss begins to dominate), increasing trace width provides more loss-reducing leverage than reducing the loss tangent. This is important when you are searching for ways to trim a few decibels from your total loss budget. Note, too, that the frequency at which these two loss curves cross is about 75 percent lower for the standard loss FR-4 on the right in Fig. 20.25.

PCB material changes can be considered—to drive down dielectric loss. However, when considering material changes to balance your attenuation budget, you need to carefully consider impacts on manufacturing costs. Lower loss materials almost always come at a higher cost.

20.4.5 Compensating for Loss at the Chip Level

At high frequencies and across long backplanes, it is likely that you will still need some help at the end of the design process. That is where the FPGA or ASIC itself can compensate for loss outside your budget.

There are two primary ways to control loss at the chip level:

1. *Transmitter preemphasis*. Boost the initial voltage of each edge to compensate for high-frequency loss.
2. *Receiver equalization*. With equalization, the incoming signal's high-frequency components are amplified to compensate for loss.

In practice, you can build fairly long, inexpensive channels ranging from 12 to 18 dB while leaving additional margin for crosstalk and reflections, correcting these losses with TX and

RX equalization for low bit-error-rate performance. Although it is possible to estimate rise-time degradation and loss, the only way to get a realistic prediction of actual results—including crosstalk and reflection effects—is to use a software simulator with these capabilities.[14]

20.5 INTRODUCTION TO POWER INTEGRITY

Every electronic product, regardless of application, requires a carefully planned power distribution network (PDN) to ensure functional operation while achieving EMC compliance—particularly at today's high operating frequencies. Many components on PCBs are sensitive to fluctuations in the power distribution system. Without a stable power distribution system, issues may develop from switching noise on planes, affecting nearby components based on charge storage, power fluctuations, spikes, voltage droops, blackouts, along with a host of other items that may cause functional disruption in addition to undesired EMI that radiates from the edges of the PCB. Additional background on PDNs is found in Ref. 11.

In this section, the word "*ground*" is sometimes replaced by the word "*return*" or "0V." There is no "true ground" in a PCB with regard to power distribution. We have voltage and 0 V reference. Voltage travels from the power generating section, and according to Ampére, must "return" to its source.

20.5.1 The Need for Optimal Power Distribution

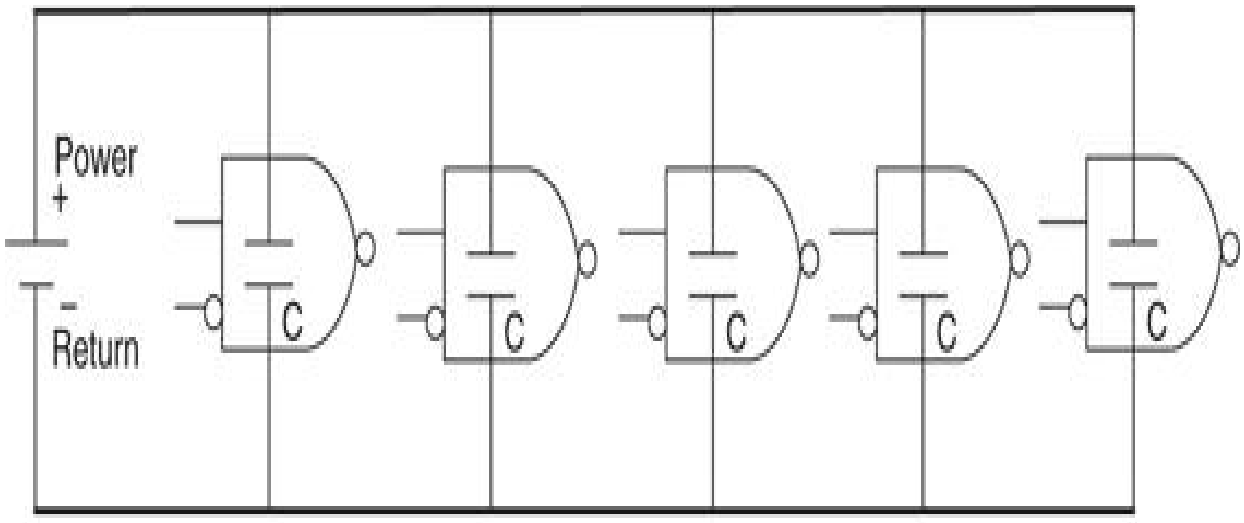
An optimal power distribution system is required to provide stable operating voltages, typically with 5 percent or lower voltage ripple, with minimal switching noise for all components to ensure functional operation.

Key concerns when designing a PDN include

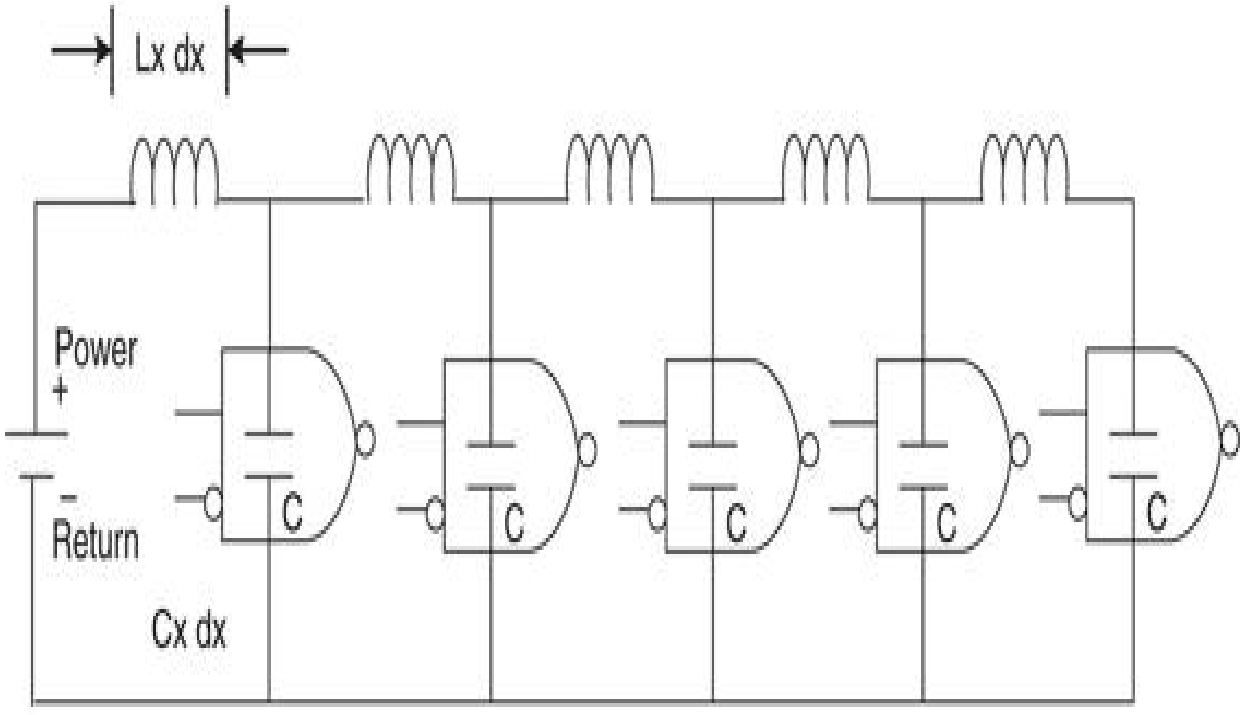
1. Use of a low-impedance connection between circuits to minimize voltage drops in the power transmission path.
2. Between components there is always a finite physical distance to transfer charge. This means a finite voltage drop will occur across this interconnect due to transmission path inductance. Depending on the inductance of this interconnect, significant fluctuations of power may occur, potentially affecting signal integrity and causing an EMI event.

20.5.2 Power Distribution Network as Transmission Lines

Power distribution networks can be represented as a two conductor transmission line with inductance, capacitance, impedance and propagation delay—just like transmission lines. The differences between a plane and trace are in physical dimensions only. Planes are wide in both the *x* and *y* axes while signal traces are, of course, narrow. Both transmission structures propagate a signal, or power, between devices. And a return path must also be present in both cases, as illustrated in Fig. 20.26.



Ideal Power Distribution Network–Multiple Loads



Real-Life Power Distribution Network–Multiple Loads

FIGURE 20.26 A power distribution network is in reality a transmission line system with inductance between each item connected to the power and return rail.[11]

In order to provide optimal power integrity, there must be very low impedance within the PDN interconnects between components using either trace(s) or plane(s). The reason we must have low impedance is easily described by Ohm's law (20.3), shown in both time and frequency domain format for the impedance portion of the equation. The subscript (*t*) refers to "with respect to time." If we have less impedance (*Z*) in a transmission line, with a fixed voltage requirement, a maximum amount of current is available to the component, with minimum voltage bounce and switching noise.

$$\Delta V = \Delta I \times Z$$

where

$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V(t)}{I(t)} \qquad (20.3)$$

The easiest way to lower total transmission plane impedance is to minimize inductance (numerator) or increase total capacitance (denominator). We can thus reduce impedance on a PCB through the process of

- Reduction of total loop area between conductors—including the *Z* direction—minimizing total loop inductance in the transmission line structure.
- Putting power and return planes very close to each other in the layer stackup—to achieve greater capacitance and reducing loop inductance.
- Increasing a conductor's width reduces inductance and increases capacitance, with respect to another conductor or its associated return path.

The key thing to remember is that minimizing ripple on the voltage rail is best achieved by reducing Z_{PDN}, the

impedance of the PDN. Lowering interconnect impedance also allows for greater drive current to components.[16]

20.5.3 Different Types of Discrete Capacitors Used in Power Distribution Networks

There are two basic applications to consider when choosing a capacitor to ensure a stable PDN; bypassing and decoupling. These two terms are sometimes interchanged when discussing the need to have a high quality PDN. Proper understanding of the differences is an important key to successful PCB layout.

- *Bypass capacitors*, or “bulk bypass” capacitors have larger capacitance values, such as 1 to 1000 µF, that helps maintain constant DC voltage and current levels within a PDN. Bypass capacitors ensure there is sufficient “bulk” power, both voltage and current, available to all components within a specific radius of operation. Consider them as very large charge storage reservoirs. These capacitors provide a valuable function up to about 10 MHz. Bulk bypass capacitors are recharged by the power supply.
- *Decoupling capacitors* minimize or decouple switching energy from digital components from being injected into the power distribution network with every edge transition, both low and high. Digital components both source and sink current, and with each transition, a finite amount of charge must be available to ensure the PDN does not drop below operational voltage levels—typically targeting 5 percent or lower fluctuation. Decoupling capacitors provide a localized source of DC power—particularly useful in reducing peak current surges propagated across the board up to around 200 MHz.

Above 200 MHz, instantaneous, localized power delivery then comes from the power and return plane pair located somewhere within the stackup of a multilayer PCB, or from on-die capacitance. Decoupling capacitors are recharged from the bulk capacitor(s). The planes directly under the component are then recharged by both the bulk and decoupling capacitors, strategically located throughout the layout. An overall view of a PDN is shown in Fig. 20.27. The key to providing maximum power delivery is to minimize spreading as well as the interconnect inductance between both component and capacitor to the PDN, which is commonly performed with breakout traces and vias. This interconnect inductance combines the equivalent series inductance, or ESL, of all of the loop elements in Fig. 20.27.

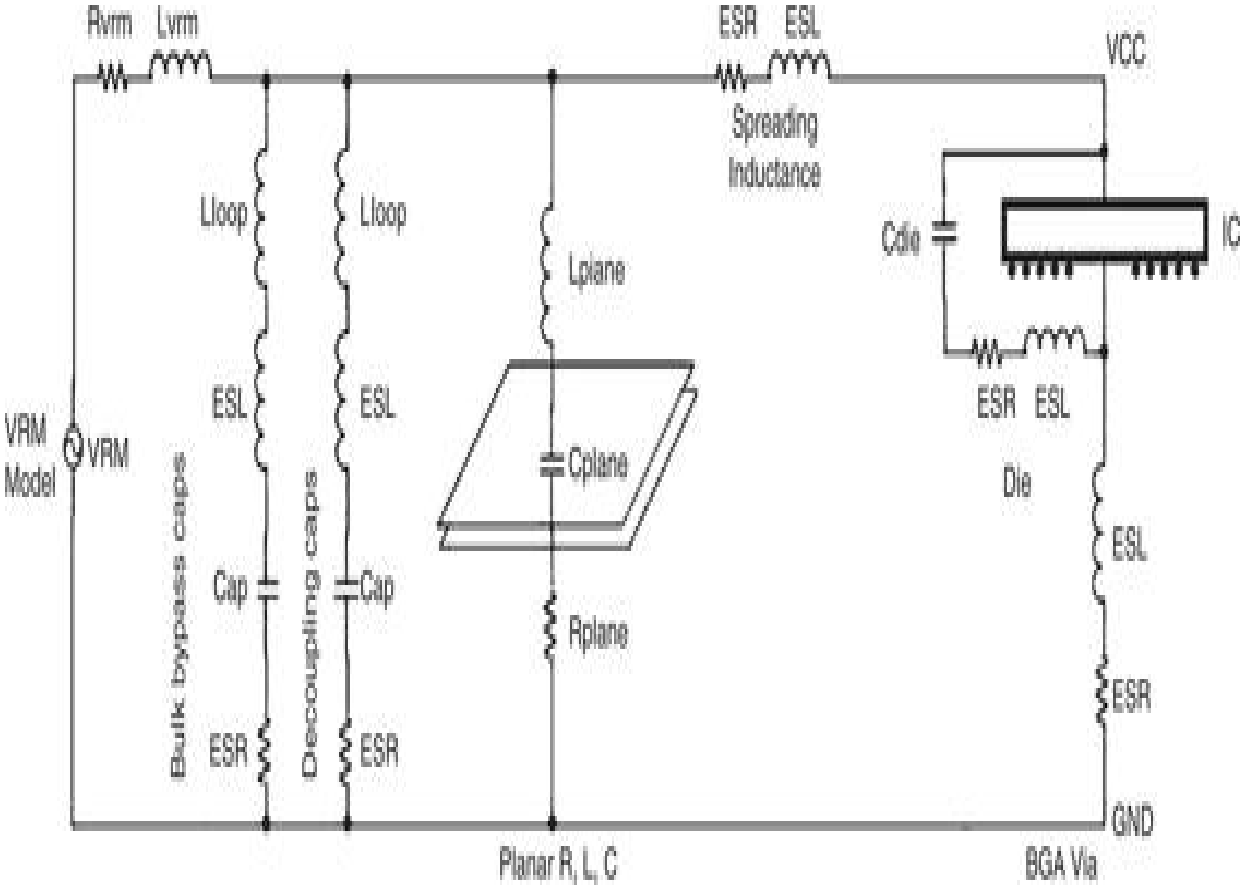
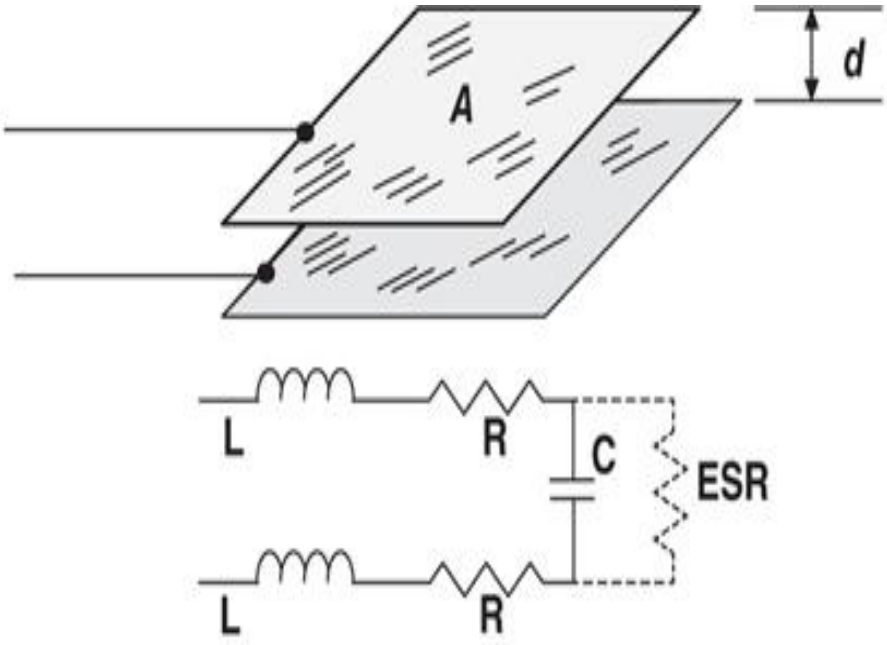


FIGURE 20.27 Power distribution network illustrating various internal capacitance structures.[17]

20.5.4 Physical Characteristics of a Capacitor When Applied to PDN Applications

Capacitors are modeled as an *RLC* circuit, where *L* (inductance) relates to both external lead length interconnect and body construction, *R* (resistance) inherent within the dielectric material between the plate, and *C* (total capacitance). A schematic representation is shown in Fig. 20.28, with variable "*d*" representing the physical spacing between the two plates.



Interconnects internal to the capacitor plates contain both inductance and resistance – *ESR* is mainly the resistance inherent within the dielectric material

FIGURE 20.28 Capacitor model with resistance, inductance and capacitance.[11]

At a calculable frequency (20.4), the series combination of *L* and *C* becomes resonant, providing very low impedance and effective RF energy shunting at that specific frequency.

At frequencies above self-resonance, the impedance of the capacitor becomes increasingly inductive and performance, especially when used in decoupling applications, becomes less effective. Both bypassing and decoupling applications are significantly affected by lead inductance in addition to the physical trace length interconnect between capacitor and the PDN though vias, so anything that a PCB designer can do to minimize these “loop elements” is advantageous.[17]

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{20.4}$$

where f = self-resonant frequency, or where the impedance of the capacitor is at a minimum (Hz)
L = total inductance of the circuit (includes trace interconnect through vias to internal planes) (henrys)
C = value of the capacitor (farads)

Capacitors reach their minimum impedance at their self-resonant frequency (SRF), which is determined by total capacitance and *ESL*. This includes the interconnect inductance between the component and PDN, including vias, and is shown in Fig. 20.29, where the capacitor performs as a capacitive structure up to its SRF. Above its SRF the capacitor behaves inductively. Inductance restricts the flow of charge delivery.[17]

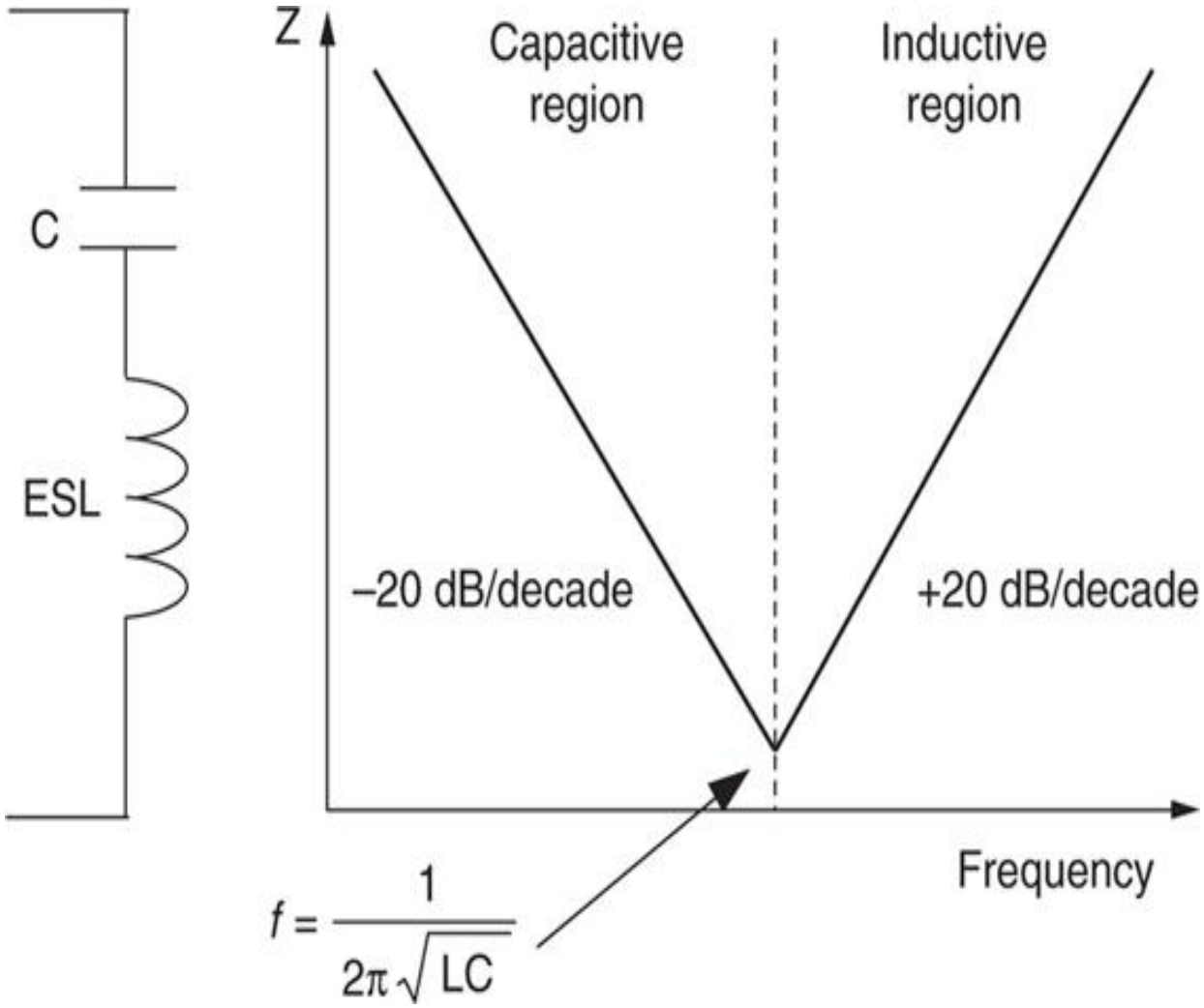


FIGURE 20.29 Impedance plot of a capacitor showing both capacitive (left of the SRF frequency, f) and inductive (right of SRF) regions of performance. The capacitor provides charge in the capacitive region but is inductive above self-resonant, and useless for the purpose of providing local charge storage energy.[11]

To meet the target impedance at a particular frequency, a capacitance value can be chosen that will resonate at the desired frequency per (20.4). At this frequency, its impedance will be equal to its *ESR* (equivalent series resistance).[17]

When many capacitors with the same value are placed in parallel, both *ESL* and *ESR* are reduced in proportion to the number of devices provided. Total capacitance also increases, which is highly desirable—though these benefits

come at the expense of both the components and more importantly, board space.

A serious concern when using two capacitors of different values lies in the belief that they provide a large spectral distribution of decoupling deals with their combined antiresonant frequency. Using typical values of 100 nF and 1 nF caps in parallel means they have a SRF at 16 MHz and 170 MHz respectively, but with an antiresonant frequency at 120 MHz, shown in Fig. 20.30. If there are any switching frequencies at 10, 20, 30, 40, or 60 MHz, a harmonic of these frequencies can cause a serious radiated EMI event to occur at 120 MHz. Balancing between pulling the PDN impedance curve, Z_{PDN}, down across a wider frequency band versus the battle with antiresonant effects has been the subject of many PCB engineering discussions over the years. Unfortunately, panaceac solutions do not exist for making all of the trade-offs.

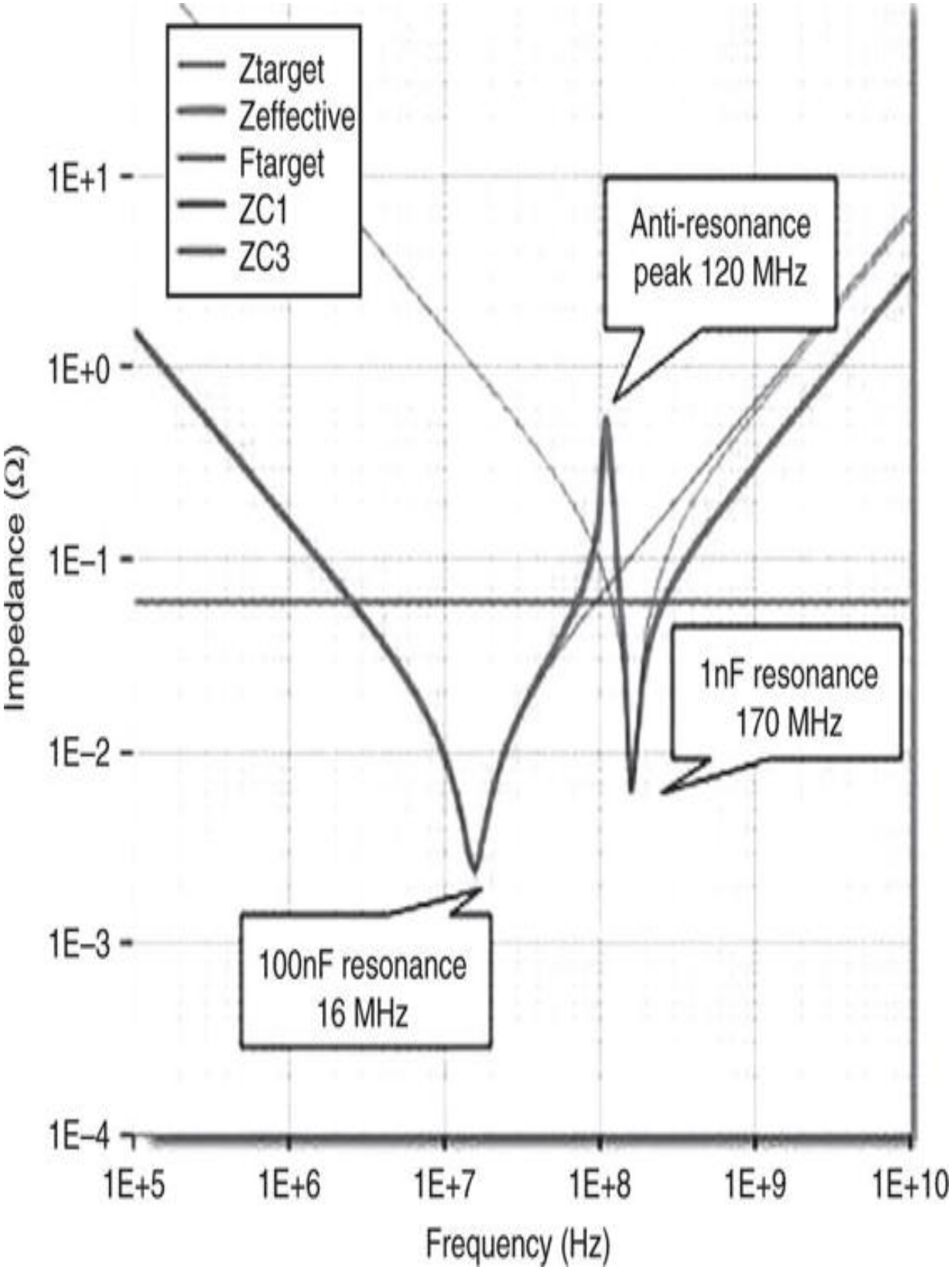

Ztarget
Zeffective
Ftarget
ZC1
ZC3
Anti-resonance
peak 120 MHz
1nF resonance
170 MHz
100nF resonance
16 MHz
1E+1
1E+0
1E−1
1E−2
1E−3
1E−4
Impedance (Ω)
1E+5
1E+6
1E+7
1E+8
1E+9
1E+10
Frequency (Hz)

FIGURE 20.30 Illustration of the antiresonant frequency when two capacitors of different values are used in an effort to provide a broad spectrum of decoupling.[17]

20.5.5 Lead Length Inductance Related to Mounting Configuration

The mounted inductance, or ESL of a capacitor, has three components that describe the loop in which current must flow: (1) capacitor footprint; (2) distance from the plane; and (3) power plane spreading inductance. The footprint for a capacitor consists of via placement with respect to the pad, the length and width of connected traces, as well as characteristic inductance that dominates the total ESL value.

The key to successful PDN design when using discrete capacitors for energy delivery below 200 MHz lies in minimizing loop inductance in the interconnect. This interconnect includes the breakout trace and the physical distance to planes internal to the stack assignment through a highly inductive via. Typical mounting configurations are provided in Fig. 20.31.

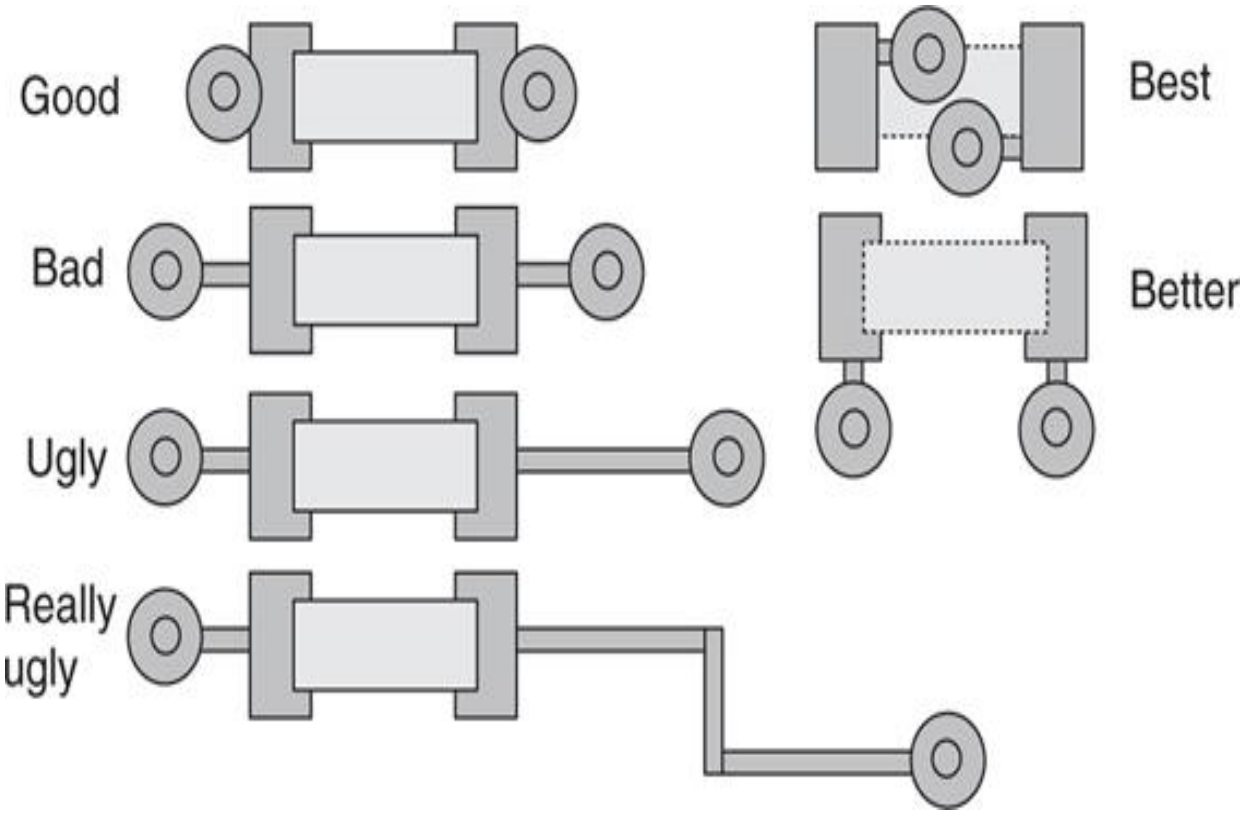


FIGURE 20.31 Inductance associated with mounting a capacitor for decoupling purposes.[11]

Using numerical analysis, calculated decap inductance is on the order of

- Surface traces 10–15 nH/in (25.4–38.1 nH/cm)
- Vias for capacitor to plane interconnect 0.40–1 nH (200–500 pH each)
- Plane inductance 0.1 nH

When determining total amount of charge that a capacitive system has, which includes discrete components and a power/return plane pair, there are basically three variables: (1) total area between the metal plates; (2) distance or separation between the plates; and (3) the dielectric constant between the plates.

In Fig. 20.32 we have a simplified illustration of a capacitor with two metallic plates having a finite area (A), separation (d), and dielectric constant (ε_r), which is a frequency-dependent value of the material used to create the capacitor, whether the capacitor is a discrete component, or parallel planes on a circuit board.

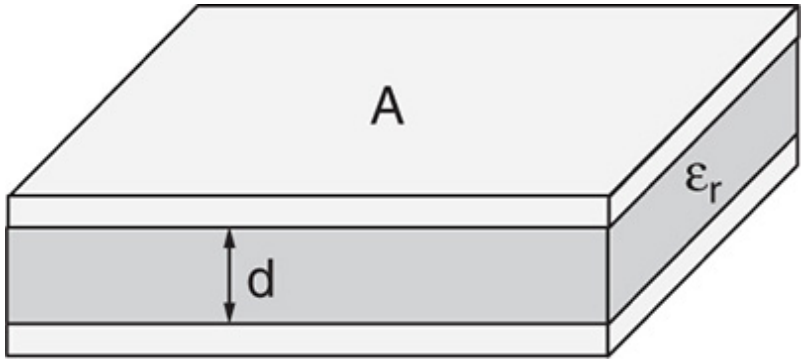


FIGURE 20.32 Typical capacitor configuration with the two plates acting as the power and return planes with a dielectric material between the plates. This material has a frequency dependent dielectric value.

Internal plane capacitance, used in conjunction with discrete decoupling capacitors to provide a stable power distribution network can be calculated by Eq. (20.5).

$$C_{pp} = k\frac{\varepsilon_r A}{d} \tag{20.5}$$

where C_{pp} = capacitance of parallel plates (pF)
ε_r = dielectric constant of the board material
A = area between the parallel plates (square inches or cm)
d = distance between the plates (inches or cm)
k = conversion factor (0.2249 for inches, 0.884 for cm)

The least inductive means of providing a large amount of energy charge is through use of power and return planes embedded internal to a multilayer PCB stackup. These planes provide energy from 150 MHz and up into the GHz

range. Discrete capacitors cease to provide their energy storage function due to inductance at an upper limit of around 250 MHz. By the time capacitors go inductive, the planes have already started to provide charge—with very little additional inductance.

The use of ultra-thin, high dielectric constant (Dk) dielectrics can significantly improve the effectiveness of the PDN. Standard FR-4 technology is limited to 2-mil thickness, dielectric constants of around 4.0, and a capacitance density of only 49 to 68 pF/cm^2 (0.31 to 0.43 nF/in^2). Thinner, less than 1.0-mil (<25-um) cores, especially those filled with high dielectric ceramic particles such as barium titanate, are now being used for the power distribution in today's high-frequency designs.

Some of these laminates have a dielectric thicknesses in the range of 8 to 14 microns (0.31 to 0.55 mil) and dielectric constants up into double digits. In combination, these features deliver a higher capacitance density of 0.3 to 3.6 nF/cm^2 (2 to 23 nF/in^2), and much lower loop inductance. A list of example materials for distributed capacitance can be seen in Table 20.2. Each offers many benefits when used for decoupling high speed digital electronics, including:

TABLE 20.2 A List of Example Materials for Embedded or Distributed Capacitance. (CCL = copper-clad laminate or core material; RCF = resin-coated foil.)

Distributed Capacitance Materials											
Type(CCL/ PP/RCF)	Thickness (mil)	Thickness (mm)	Capacitance (nF/in^2)	Capacitance (pF/cm^2)	Dk @ 1 MHz	Dk @ 1 GHz	Dj @ 1 MHz	Dj @ 1 GHz	Description	P/N	PWB Processing
CCL	0.24	0.006	19.663	3183.3	21.0	18	0.025	0.08	3M ECM	C2006	Sequential Lam
CCL	0.63	0.016	10.701	1705.1	30.0	26	0.019	0.035	FaradFlex	BC16T	Sequential Lam
CCL	0.47	0.012	10.041	1591.6	21.0	18	0.025	0.08	3M ECM	C1012	Sequential Lam
CCL	0.31	0.008	7.492	1193.7	10.5	10	0.016	0.021	FaradFlex	BC8TM	Both side Etching
CCL	0.55	0.014	6.129	976.6	15.0	13	0.025	0.08	3M ECM	C0614	Sequential Lam
CCL	0.47	0.012	4.590	698.3	9.6	8.5	0.019	0.021	FaradFlex	BC12TM	Both side Etching
CCL	0.31	0.008	3.190	508.2	4.4	3.48	0.015	0.016	FaradFlex	BC8M	Both side Etching
CCL	0.47	0.012	2.104	335.2	4.4	3.5	0.015	0.02	FaradFlex	BC12M	Both side Etching
CCL	0.48	0.012	1.639	261.1	3.5	3.5	0.005	0.0054	InterraHK	HK4	Both side Etching
CCL	0.63	0.016	1.569	250.1	4.4	3.5	0.015	0.02	FaradFlex	BC16M	Both side Etching
CCL	0.71	0.018	1.108	176.5	3.5	3.5	0.005	0.0054	InterraHK	HK4	Both side Etching
CCL	0.94	0.024	1.052	167.6	4.4	3.48	0.016	0.021	FaradFlex	BC24M	Both side Etching
CCL	0.98	0.025	0.913	145.5	4.0	3.8	0.02	0.022	Sanmina	BC-1000	Both side Etching
CCL	1.00	0.025	0.787	125.3	3.5	3.5	0.005	0.0054	InterraHK	HK4	Both side Etching
CCL	2.00	0.051	0.494	78.8	4.4	4	0.02	0.022	Sanmina	BC-2000	Both side Etching
CCL	3.00	0.076	0.307	48.9	4.1	3.94	0.012	0.014	Standard	Any Laminate	Both side Etching
Film	1.97	0.050	3.633	582.1	32	—	0.007	—	NipFlex	NA	Sequential Lam
Prepreg	1.10	0.028	0.877	139.7	4.3	3.6	0.009	0.0093	106 LD	106 LD	Sequential Lam
Prepreg	1.30	0.033	0.744	118.5	4.3	3.6	0.02	0.022	1067 LD	1067 LD	Sequential Lam
Prepreg	1.18	0.030	0.742	118.2	3.9	3.4	0.02	0.022	1037 LD	1037 LD	Sequential Lam
Prepreg	1.30	0.033	0.675	107.5	3.9	3.4	0.02	0.022	1067 LD	1067 LD	Sequential Lam
Prepreg	1.70	0.043	0.568	90.6	4.3	3.6	0.02	0.025	1086 LD	1086 LD	Sequential Lam
Prepreg	1.73	0.044	0.558	88.9	4.3	3.6	0.02	0.022	1078 LD	1078 LD	Sequential Lam
Prepreg	1.77	0.045	0.533	84.9	4.2	3.5	0.02	0.022	1080 LD	1080 LD	Sequential Lam
Prepreg	2.00	0.051	0.427	68.0	3.8	3.72	0.012	0.0156	106	106	Sequential Lam
Prepreg	2.50	0.064	0.351	55.9	3.9	3.87	0.012	0.0152	1080	1080	Sequential Lam
RCF	0.79	0.020	12.843	2046.4	45.0	43	0.021	0.023	FaradFlex	MC45TR	Sequential Lam
RCF	1.97	0.050	5.137	818.6	45.0	43	0.021	0.023	Oak-Mitsui	MCF-HD-45	Sequential Lam
RCF	1.0	0.025	0.899	143.2	4.0	3.8	0.019	0.021	Oak-Mitsui	MHCG100G	Sequential Lam
RCF	1.6	0.041	0.534	85.0	3.8	3.3	0.015	0.018	Oak-Mitsui	MR500/100(LM)	Sequential Lam

- Lowering impedance of power distribution network
- Dampening board resonances
- Reducing noise on power planes
- Reducing radiated emissions
- Possibly replacing large numbers of discrete decoupling capacitors
- Possibly replacing discrete SMT filter capacitors

There are a lot of nuances to the design of optimal power distribution that are beyond the scope of this introduction. Reference 11 provides details on the design of power distribution networks across a broad spectrum of PCB layouts.

20.6 INTRODUCTION TO ELECTROMAGNETIC COMPATIBILITY[18,19]

Every electronic product, with few exceptions, must comply with international requirements related to electromagnetic compatibility (EMC). What is not recognized by many is that the field of electromagnetics is the foundation of everything that uses electricity or the movement of time-variant electrons in a transmission line, both at AC and DC potential. James Clerk Maxwell published a series of equations that describes the propagation of electric and magnetic fields within a transmission line with respect to time. His four equations are based on two from Gauss, one from Faraday (a.k.a. the Right Hand Rule) and Ampére's law. All four equations are in both differential and integral form of calculus. The reference from Ref. 11 provides an easy way to

understanding field propagation without going too deep into the math.

The field of EMC is defined as the ability of electrical and electronic products to operate within their intended environment of use (e.g., industrial, commercial, residential, military and the like) without causing harmful interference to other electrical systems, and conversely must be able to withstand any external electromagnetic event that could cause functional harm to itself. EMC is a highly specialized field of electrical engineering divided into two parts: emissions and immunity.

Emissions. The first aspect of the field of EMC is the unwanted generation of harmful radio frequency (RF) emissions called electromagnetic interference (EMI) or simply “emissions.” This unwanted energy is generated by digital components located on a PCB assembly though a complex process that creates both radiated fields and/or conducted currents. The frequency range of RF energy covers the electromagnetic spectrum from anything greater than DC to light (300 GHz). PCBs are utilized in applications within this frequency spectrum and beyond, including terahertz communication systems.

The main concern regarding propagation of undesired RF energy is to protect telecommunication systems such as commercial broadcasts from harmful disruption in addition to other electrical systems containing components susceptible to electromagnetic field disturbance. This includes itself along with internal circuitry located near unintentional radiators on the same PCB.

International requirements are legally mandated in North and South America, the European Union, most of the Asian continent and many other countries worldwide. Failure to meet legally required emission limits, both radiated and conducted, with a certified test report from an assessed or accredited EMC test laboratory, means it is illegal to market,

merchandise, sell or install a product within the country’s borders.

Immunity. The second part within the field of EMC related to immunity or susceptibility. Both words refer to the same electromagnetic principle. One refers to aspects of a system, viewing it as protecting components internal to an enclosure from outside interference (immunity), or viewing aspects of harmful RF energy outside the unit penetrating to the inside (how susceptible the system is to electromagnetic field disruption).

With regard to immunity, this concern is always at the component level. Most analog components are sensitive to high levels of electromagnetic field disturbance. PCB construction has minimal effect related disruption of operational circuits thus, further discussion on immunity is outside the scope of this chapter. Excellent resources exist to learn more about immunity requirements at the system level.

20.6.1 How EMI Is Generated from a PCB

There are three primary areas of concern when designing a PCB to ensure EMC compliance and that the system does not cause harmful interference to not only the outside environment, but to adjacent circuits and components through the process of crosstalk. (Crosstalk can be viewed as EMI at a very localized level.)

1. Proper transmission line routing based on numerous design requirements.
2. Ensuring optimal power distribution to all components, which minimizes transient-voltage fluctuations in both the power and return (a.k.a. ground) planes.

3. Ensuring proper referencing of signals to power and ground planes.

20.6.2 Transmission Line Routing to Ensure Optimal Signal Integrity

Using transmission line theory, traces are used to send signals between components. The signal propagated is actually an electromagnetic field that travels from source to load along with a return for the current to satisfy Ampére's law. Any losses within a transmission line become the magnitude of undesired common-mode current that is developed and which propagates as either an unintentional radiated field or conducted currents.

There are two modes of signal propagation, differential and common. Differential-mode is the signal of interest between source and load along with its return path. No loss of electromagnetic energy occurs. The electromagnetic field in the source path is 100 percent identical to the electromagnetic field in the return path travel, however the return path is in the opposite direction. With equal and opposite magnetic field propagation between the two transmission lines coupling to each other, we have optimal signal integrity and no EMI.

However, if there is a loss of electromagnetic energy in either the source or return path, this loss within the electromagnetic field must still return to its source based on Kirchhoff's law. A portion of the electromagnetic field, the loss portion, will take an undesired propagation path through parasitic capacitive coupling to an adjacent transmission line such as free space or a metallic interconnect. These unintentional, common-mode currents, are at the root of all emissions problems.

Thus, to minimize emissions is to ensure optimal signal integrity—minimizing or eliminating unnecessary energy loss

in transmission line structures. Ringing on a periodic signal, for example, is a guaranteed emissions source. Any impedance discontinuity, in fact, associated with transmission line routing results in common-mode energy transfer from the transmission line to the outside world.

20.6.3 RF Return Paths[20,21]

All signals require a source transmission line and return path for the electromagnetic field that propagates within every transmission line. Very frequently, the signal conductor is easily seen on the schematic and the return is neither shown nor mentioned. It is implied that the return current magically returns to the source through the power and ground pins of components, which is true for strictly DC systems. As soon as there is current changing with respect to time with units of hertz, we enter the AC domain. Once the frequency is above 100 kHz, all components are considered to be propagating RF signals with an electromagnetic field and not with steady state voltage levels. The rise and fall times of digital components are the AC portion of a signal, while logic level “0” and “1” are DC. Therefore, there are two types of current present at the same time, AC and DC. There is a significant difference between how AC current (the electromagnetic field), and DC current (steady state) flows in every transmission line.

RF current, or signals operating above 100 kHz, must propagate between components using any transmission line path possible, generally the one with the lowest impedance. This transmission line path includes transference of the electromagnetic field due to parasitic capacitive coupling to a nearby metallic structure (adjacent trace or plane) or system enclosure through free space. If there is no low-impedance conductive path (<377 Ω), free space (at 377 Ω) becomes the transmission line. *Free space is exactly what*

we do not want, especially with regulatory compliance concerns and EMC compliance.

Return currents at DC voltage levels travel through either the power and/or 0 V return plane. While single-sided PCBs may be a cost-effective implementation for a simple design, the probability is high that this configuration will not pass various EMC test requirements if digital components are utilized, unless the digital rise and fall times are very slow such as >1 microsecond, with a very short transmission line route between source and load. Adding a 0-V reference plane, or making the stackup of the PCB a multilayer assembly, will enhance overall performance related to signal integrity and EMC compliance.

Any physically large copper or metal laminate in a multilayer stackup provides an optimal return path with minimal impedance for RF return currents. The DC voltage potential of the plane (i.e., +3.3 V, +5 V, +12 V) is not a major concern. Multilayer boards obviously cost more, but the functionality gains in SI and PDN performance, as well as improvements in EMC, more than compensate for the additional expense in manufacturing the board, typically.

Figure 20.33 illustrates the return path for both low- and high-frequency signals. At lower frequencies, the return current for DC referencing is through the path of *least resistance*, which in this case is a direct path back to the source using the power plane for signals transitioning to the logic level high state; and the return plane for transitions to logic level low.

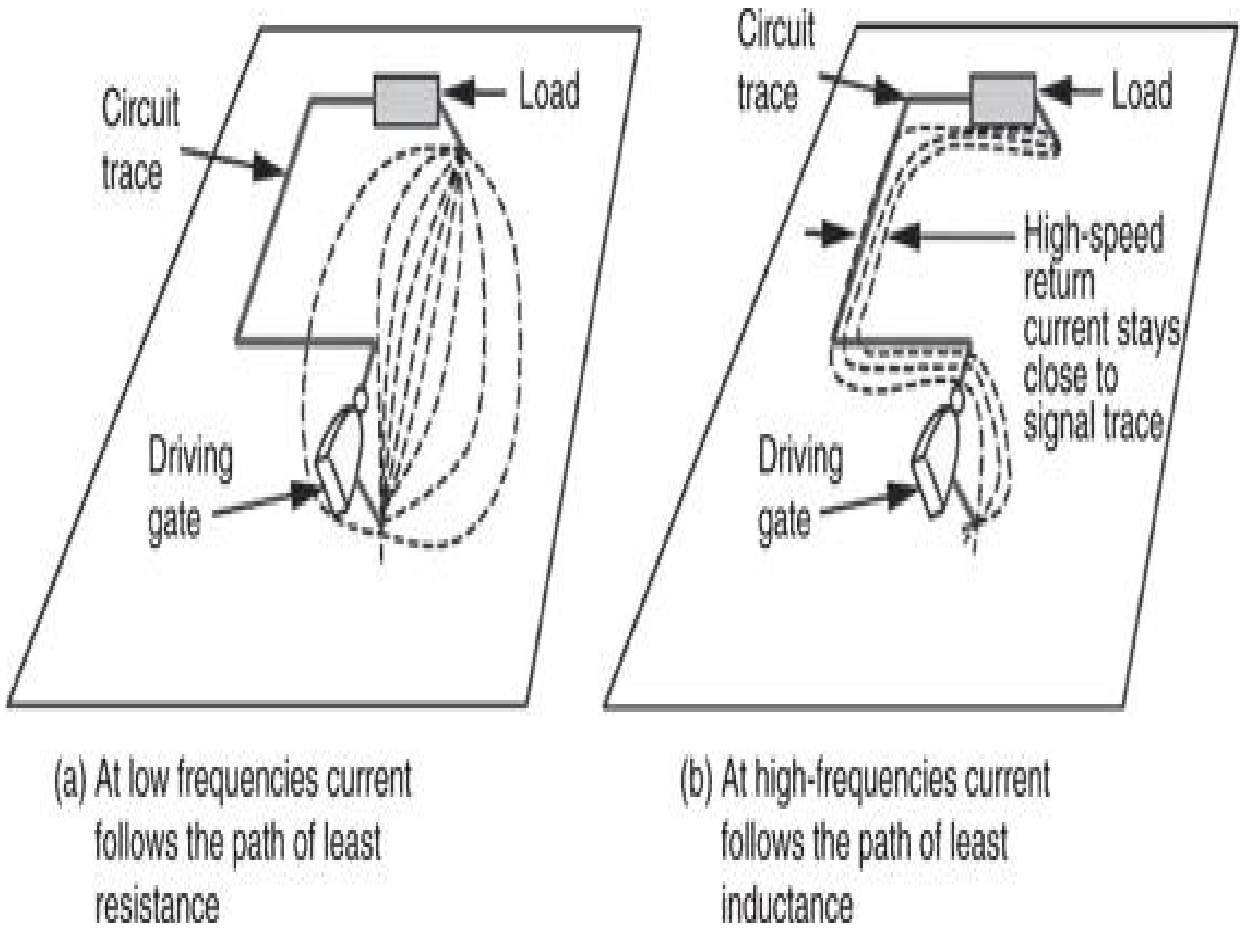


FIGURE 20.33 Current return path, both high and low frequency.[4]

For higher frequencies, generally above 100 kHz, the RF or AC return current takes a different path or the path of *least inductance*. Every electromagnetic field requires a mirror image of itself using a return path that is physically located as close to the source path as possible in order to couple its magnetic field lines, per Faraday and Ampére's law. This return path exists as a result of partial mutual inductance, a complex topic reserved for discussion in books listed in the Reference section requiring extensive use of high-order math.

To simplify discussion on the difference between the path of least resistance and least inductance, Eq. (20.6) illustrates the concept.

$$Z = R + jX_L \tag{20.6}$$

where Z = total impedance of the transmission line
R = resistance of the transmission line (a fixed value) [DC current]
X_L = inductive reactance (a variable value) [AC current]

$$jX_L = 2\pi fL$$

where f = frequency of the signal
L = inductance of the transmission line

Assume the characteristic resistance of a trace is 10 mΩ. This is very low and DC current flows easily in the return path (the path of least resistance).

The inductance of this same transmission line is 100 nH, a typical value for a short trace route. When the frequency of the electromagnetic field propagating in the transmission line increases, the value of X_L starts to become very large in direct portion to frequency. For example, at 1 MHz, X_L = 630 mΩ. At 100 MHz, X_L = 63 Ω. At 1 GHz, X_L = 630 Ω. The impedance of free space is 377 Ω. The total impedance of the transmission line is the combination of both DC resistance and AC inductive reactance. Above 100 kHz, the resistive portion essentially falls out of the equation and is a variable we can ignore.

Per Ohm's law, $V = IZ$, where Z is from (20.x). The AC return current at higher frequencies is unable to return in a direct manner if the transmission line is >377 Ω, so, for the 1 GHz case, the AC return current must then propagate through free space as unwanted radiated EMI, regardless of the path the DC return current takes.

By physically bringing a signal-transmission line closer to an adjacent plane or ground pour—regardless of DC potential

—the inductance becomes lower by a significant amount through the process of partial mutual inductance, a topic beyond the scope of this discussion. With carefully planned current return paths in close proximity to the original signal, electromagnetic field lines for the original signal and its return cancel each other at higher frequencies, thus minimizing unintentional, common-mode currents.

20.6.4 Violations or Splits in an RF Return Path

For an RF return plane to be effective, all signal traces must be physically located adjacent to a solid, undisturbed return —generally, copper planes and signal paths. No high speed, digital signal should cross an isolated or open area such as slots or gaps in adjacent planes. If any signal, or even a power/return trace is routed across such a gap, the result is typically a larger physical loop area for RF return current to flow toward getting back to the source. RF loop currents now created can then couple to an adjacent signal layers across this absence of copper area, resulting in unintended common-mode currents—a key element in crosstalk emissions, PDN noise, and differential.

Figure 20.34 illustrates a violation of the image plane or disruption of the RF return path for AC signal propagation. The return plane can now no longer function as a solid, undisturbed RF return path. The signal trace in Fig. 20.34 is the solid line going horizontal and the RF return path with a longer route is the dashed line. The percentage of RF current flow is directly proportional to distance from the impedance discontinuity area. The vertical lines are slots located in the adjacent return plane.

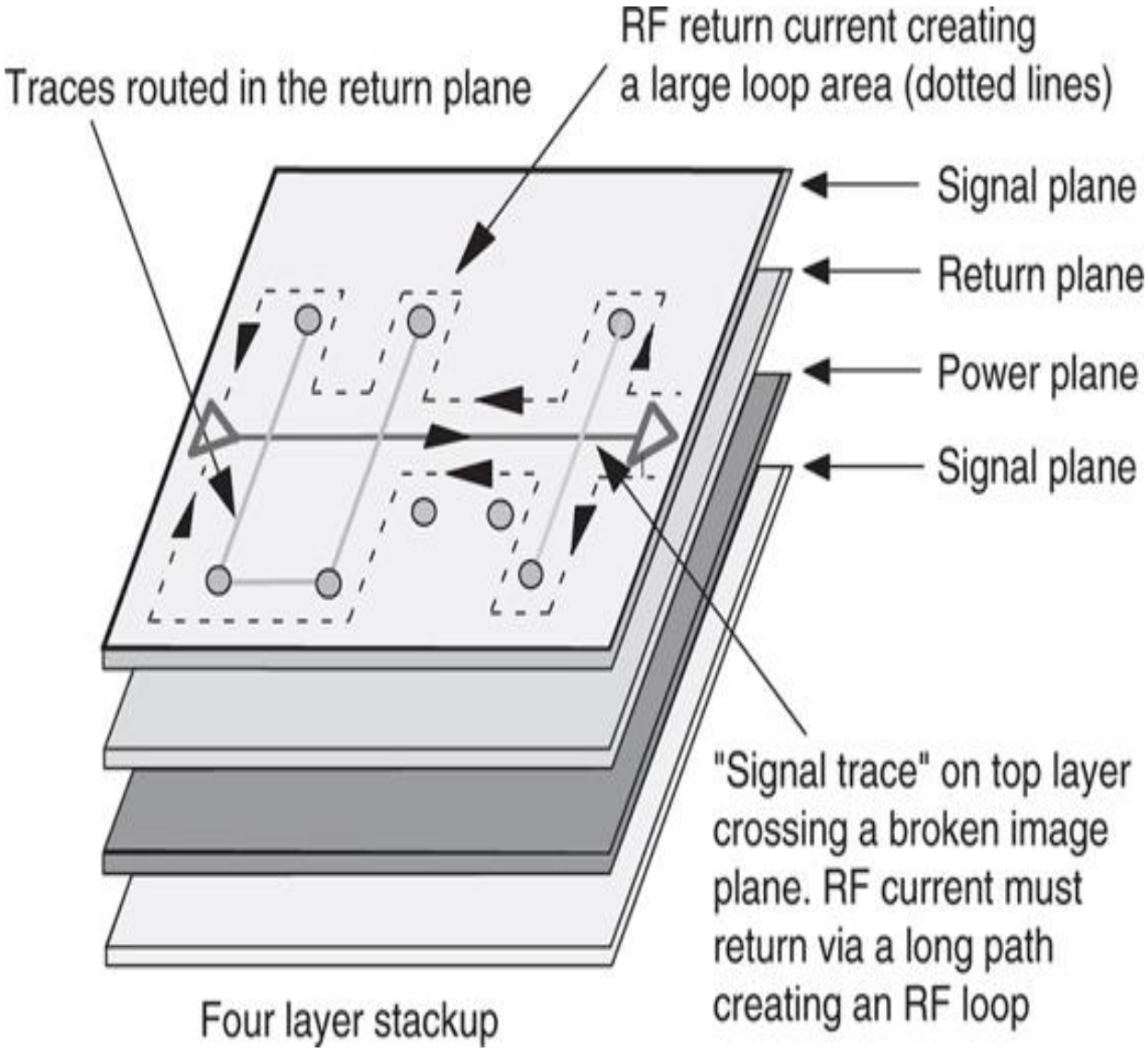


FIGURE 20.34 Image plane violation with a single trace.[11]

Should any transmission line have a disturbed RF return path, undesired EMI will develop. This is easily visualized with a coaxial cable with the braid removed, but not the center conductor. The return current on the braid will find a discontinuous path at infinite impedance and make the jump through free space, at 377 Ωs, which is less than infinity, and find its return path on the other side of the split. Once this energy enters free space to make the jump, we now have an EMI problem, and yet the circuit itself may still function without degradation.

20.6.5 Grounding Concepts and Methodologies

The word “ground,” when used alone, is ambiguous.[3] In reality, both digital and analog circuits operate off a voltage potential difference between a 0 V reference (a.k.a. ground) and a nominal power supply voltage. To be accurate, we should use the term “0 V” or “return” for power distribution since there is no literal “earth ground” on a PCB. If the word ground is to be used, preceding it with by an adjective makes sense. When someone says they have a ground plane, it’s helpful to know whether it’s a “digital” ground plane, “analog” ground plane, “ESD or chassis” ground plane, “thermal” plane, “protective earth for functional safety” ground, or another type of ground plane.

The subject of grounding is fairly involved. A number of high-quality textbooks have been written on this topic, some of which are noted in the Reference section at the end of this chapter. Nevertheless, a brief overview on grounding and referencing associated with PCBs is presented here.

20.6.6 Signal Referencing

When a PCB signal travels between transmitter and receiver pins, either the power or ground plane acts as the RF return, as seen in Fig. 20.35.

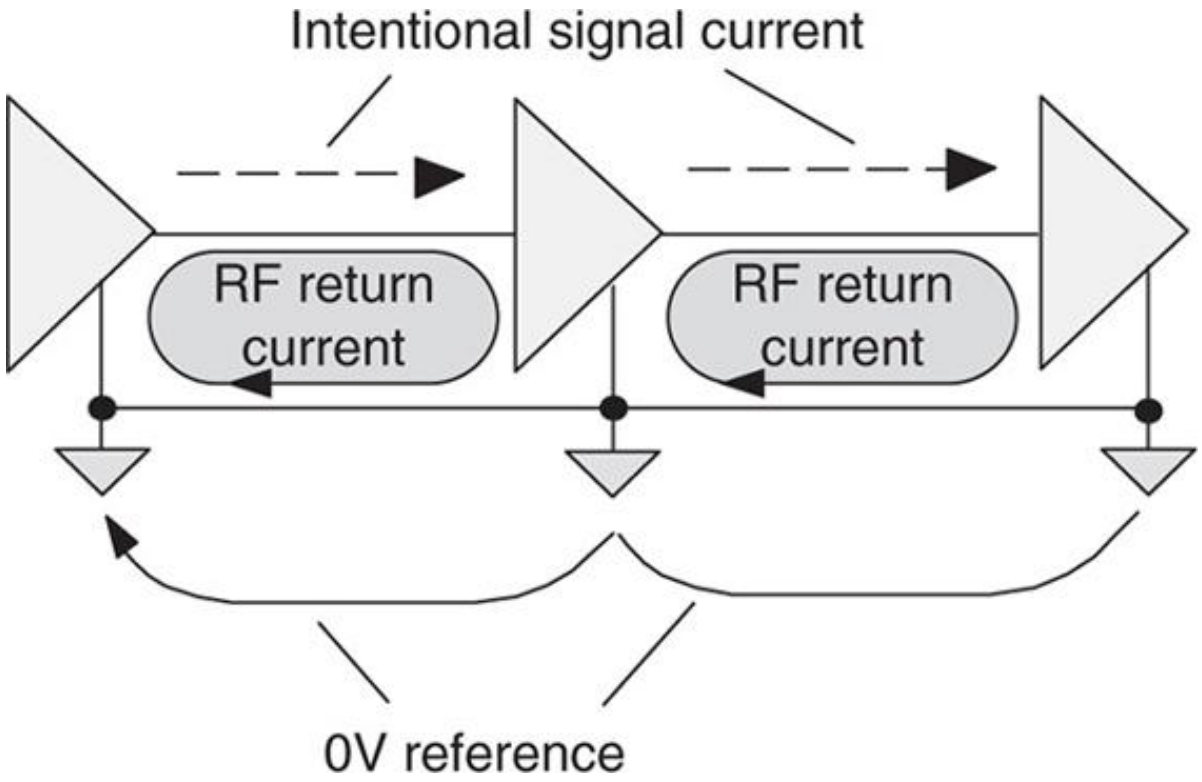


FIGURE 20.35 Referencing signal propagation for functional operation between components.

The majority of design concerns associated with EMC lie in referencing circuits to each other. All components must be at a specific voltage reference above a-0 V reference for functionality reasons. With regard to a PCB, components are referenced to a common point, typically a plane in order for logic circuits to determine a valid transition state. If the reference level between two circuits is not at the same potential, functionality concerns may occur, such as noise margin erosion and unpredictable threshold levels required for optimal logic switching. This is in addition to possible creation of a ground-noise voltage potential or undesired common-mode current.

20.6.7 Grounding System Methodologies[22]

When implementing a referencing methodology on a PCB, several types are commonly used. For each methodology, a hybrid combination may exist. Different methodologies may be used at the same time, but only if the designer understands the concept of RF current flow and RF return paths, differentiating between RF return and safety or chassis ground, which are at a completely different potential.

20.6.8 Single-Point Grounding Methodology

The single-point grounding methodology is one in which all returns are tied to a common reference point, usually at the power source, either AC or DC. This grounding methodology prevents RF currents from propagating between dissimilar circuits, usually at different voltage or reference levels or even different bandwidths of operation. Single-point grounding also prevents sharing of common RF return paths for undesired RF loop currents that produces common-impedance coupling.

There are two primary topologies when using single-point grounding—series and parallel, as shown in Fig. 20.36. Depending on the application, either will provide the same functionality. Single-point grounding is optimal when the switching speed of all components is below 100 kHz and 1 MHz! If signals are above 100 kHz to 1 MHz, multi-point grounding becomes the methodology of choice. This is because the interconnect between the PCB and chassis ground contains minimal inductance (e.g., PCB is screwed and secured to a standoff) versus a very high inductive wire with several orders of magnitude higher inductance.

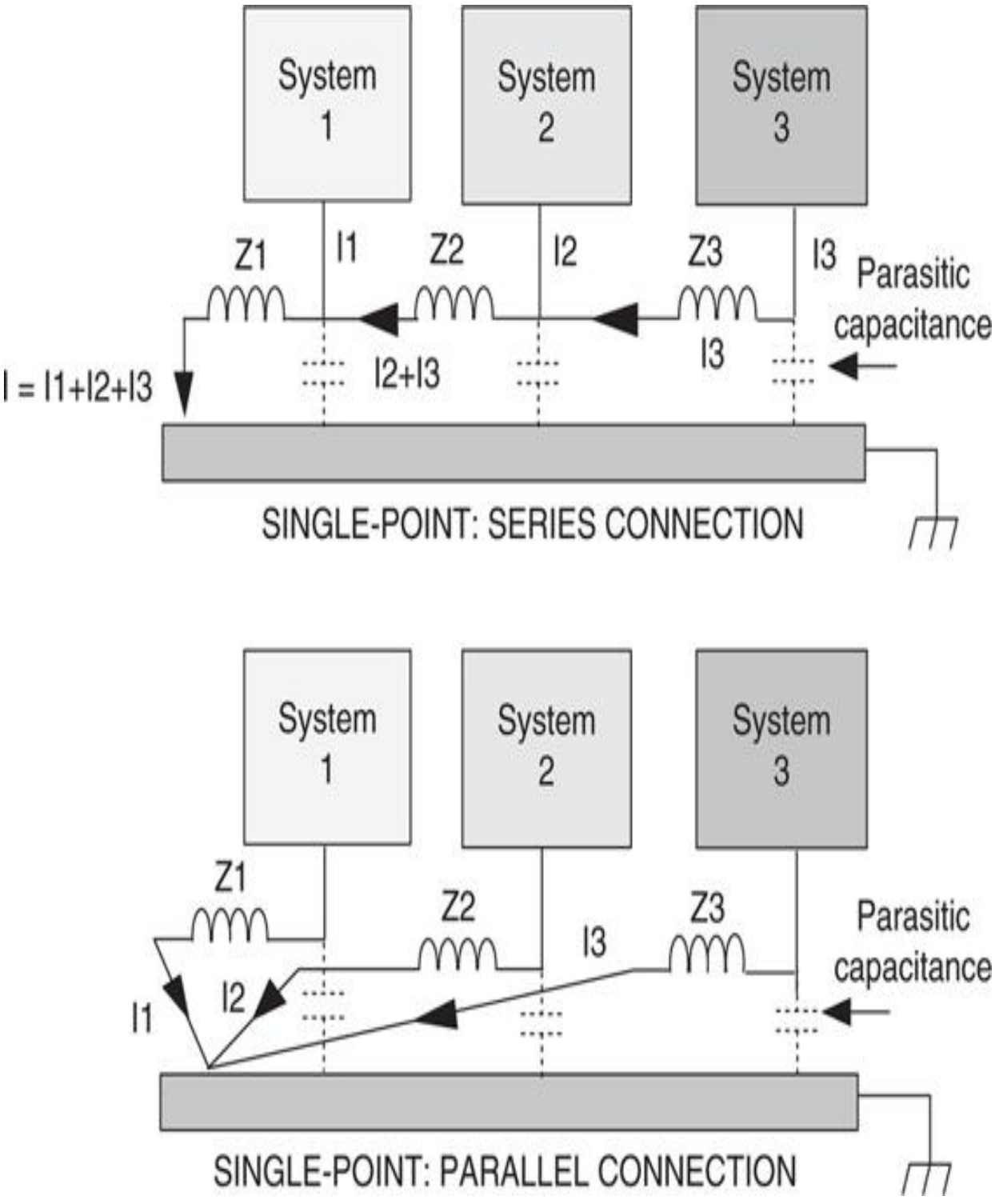


FIGURE 20.36 Single-point grounding methods. (Note: Inappropriate for high frequency operation, generally above 100 kHz to 1 MHz.)[11]

20.6.9 Multiple Connections to Single-Point Reference (a.k.a. Multi-point Grounding)

Higher frequency PCBs generally require all 0 V reference plane(s) be connected to a common reference point, usually a metal chassis or enclosure, or a plane internal to a PCB assembly commonly called the ground plane. The correct definition of multipoint grounding should be "*multiple connections to a single point reference*." This definition will become obvious with the discussion that follows.

Multiple connections to a signal-point reference, or multipoint grounding, minimizes plane impedance present for all RF current return paths. This is because there are no wires or physically long interconnects to tie functional subsystems together. Loop inductance is also minimized significantly. Loop inductance is the primary reason why single-point grounding starts to become ineffective above several 10's of kHz. When a bond connection occurs between a 0-V reference plane and a metal enclosure, the entire system is essentially at one reference potential. This one reference potential is shown with the *chassis ground* symbol in Fig. 20.37, lower right corner. Regardless of the number of circuits identified on a schematic using a symbol such as digital ground, analog ground, chassis ground, ESD ground, and the like, they must eventually connect together somewhere which means there is only *one* 0V reference in the system, or true single-point referencing. Proper connection of different ground or reference potentials is thus critical for both signal integrity and EMC compliance.

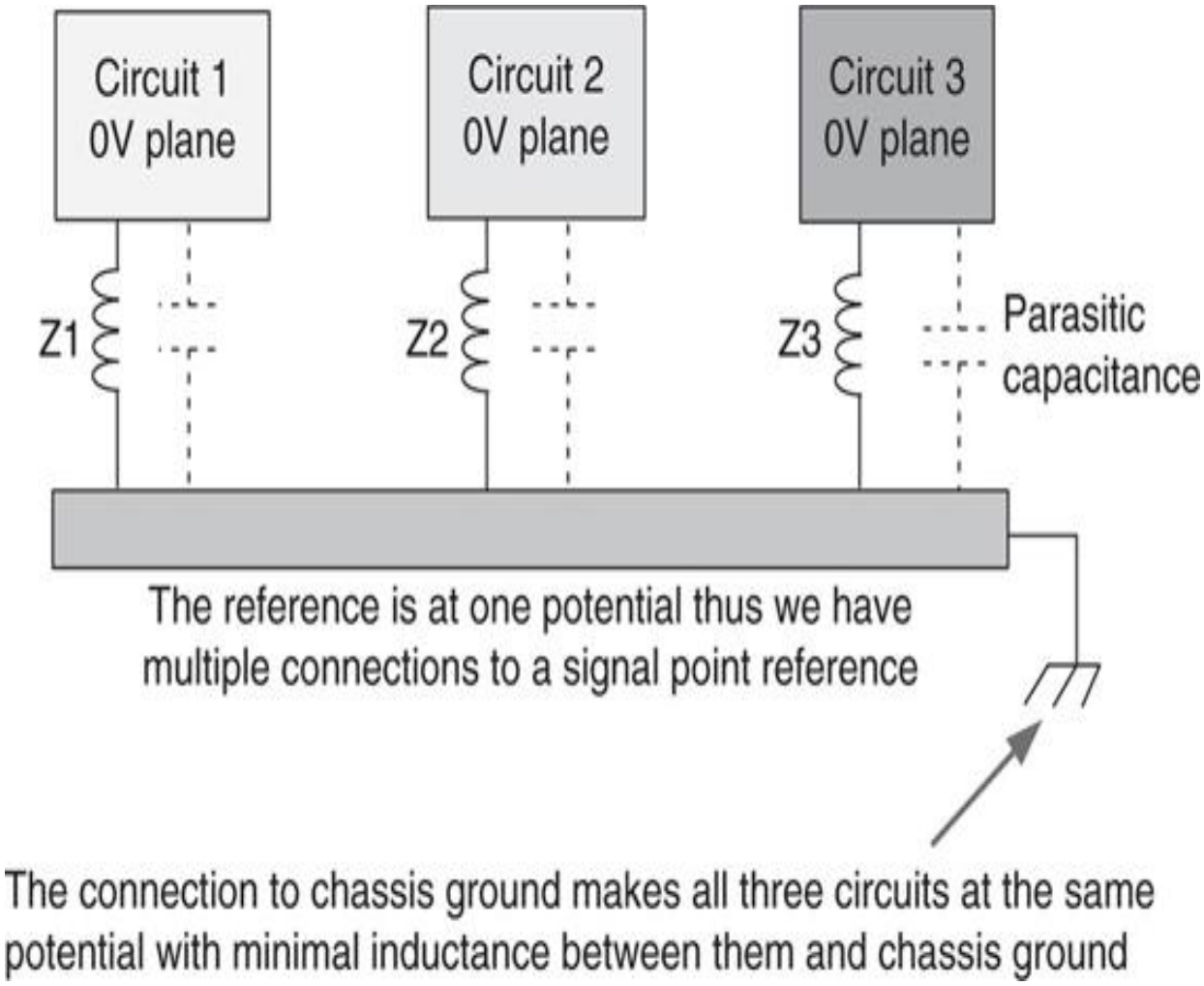
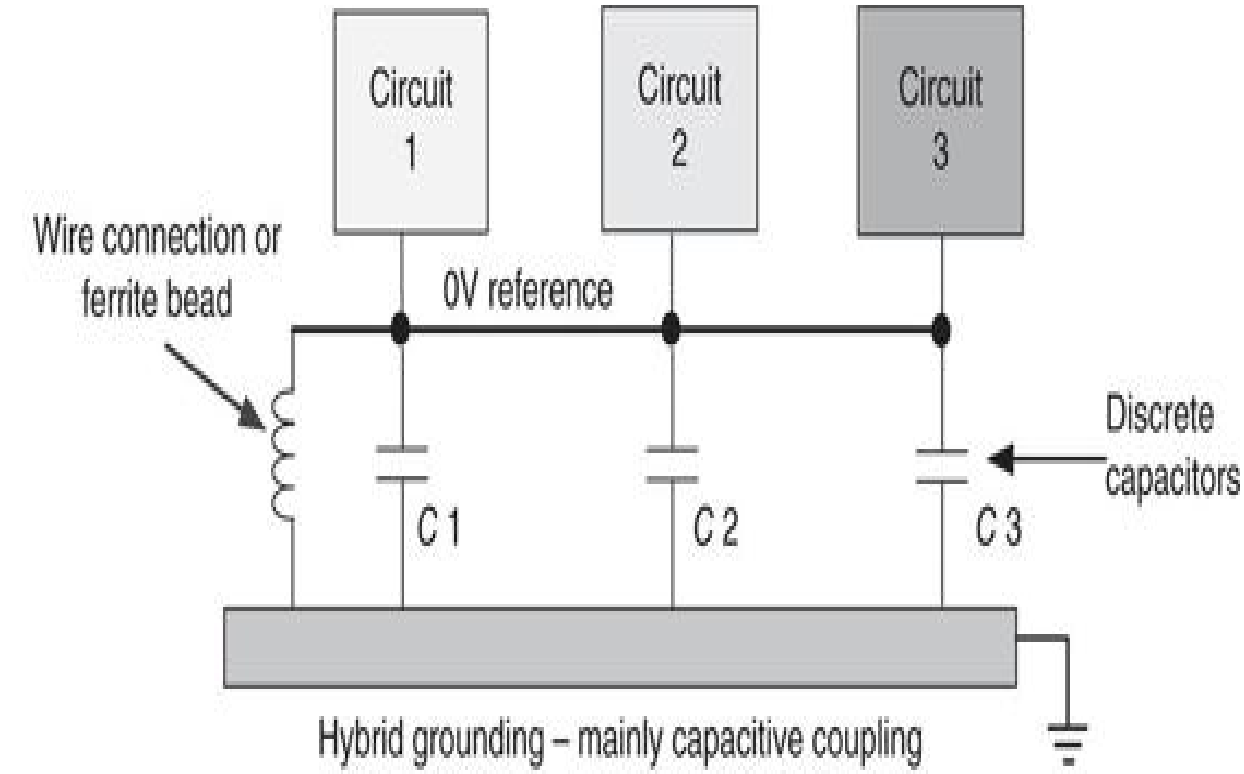


FIGURE 20.37 Multiple connections to a single point reference methodology (a.k.a. multipoint grounding).[11]

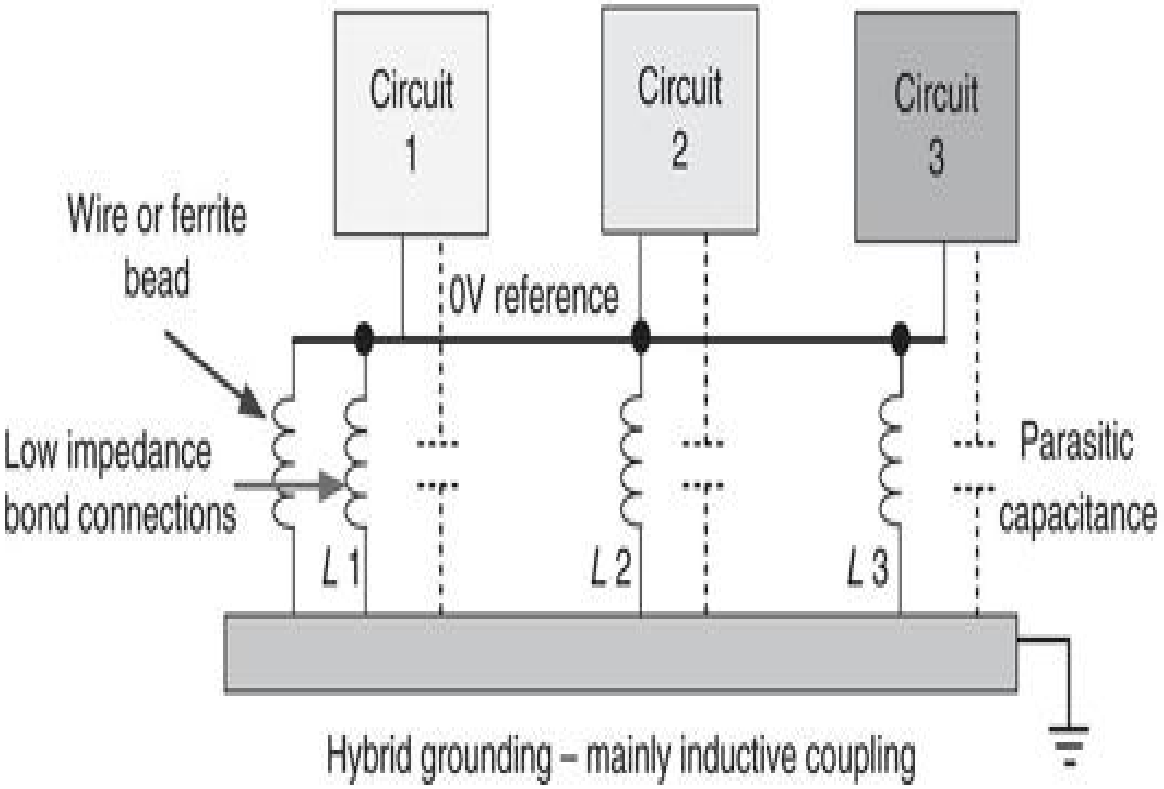
20.6.10 Hybrid Grounding

A hybrid ground system is a combination of both single and multiple connections to a single point reference, also called multi-point grounding. This configuration is used when mixed frequencies and assemblies are utilized in the same enclosure. This enclosure may contain several PCBs, each with a separate power supply, as well as separate, remotely located disk-drive assemblies, as an example. Figure 20.38 shows two hybrid topologies. For the capacitive coupling version at lower frequencies, the single-point configuration is

dominant, whereas the multi-point configuration works better at higher frequencies. This is because of parasitic capacitance present that shunts high-frequency RF currents to a 0-V reference after the single-point interconnect goes inductive. The key to success is to understand or know all frequencies present and the desired path of RF return current flow.



Hybrid grounding – mainly capacitive coupling



Hybrid grounding – mainly inductive coupling

FIGURE 20.38 Hybrid grounding methodology.[11]

The inductively coupled version is utilized when multiple ground-stitch locations must be connected to a chassis-ground reference for safety reasons, and lower-frequency connections for operational purposes. Parasitic capacitance still exists, which could cause a resonance condition to occur, along with undesired EMI by allowing eddy currents to propagate between each loop area.

20.6.11 Two Reasons for a Ground Reference in a PCB—Electrical Product Safety

A primary reason related to grounding is to ensure that a protective earth-bond connection exists in systems having hazardous voltage levels that can cause a shock hazard or electrocution. This is a legally mandated international requirement if the product has any hazardous voltage equal to or greater than 42.2 VAC or 60 VDC. Many units are connected to an AC mains network that carries 115 or 230 VAC, which makes them hazardous. If any hazardous voltages exist, the system must be connected to a true earth ground external to the assembly. This solid earth ground connection reduces the voltage difference between the exposed conducting surface, or a metal enclosure, and person physically touching the energized chassis enclosure.

Safety ground is achieved by the proper connection and routing of a permanent and continuous, low impedance, adequate fault capacity conductor that travels between an energized power source and load, or earth ground, as shown in Fig. 20.39.

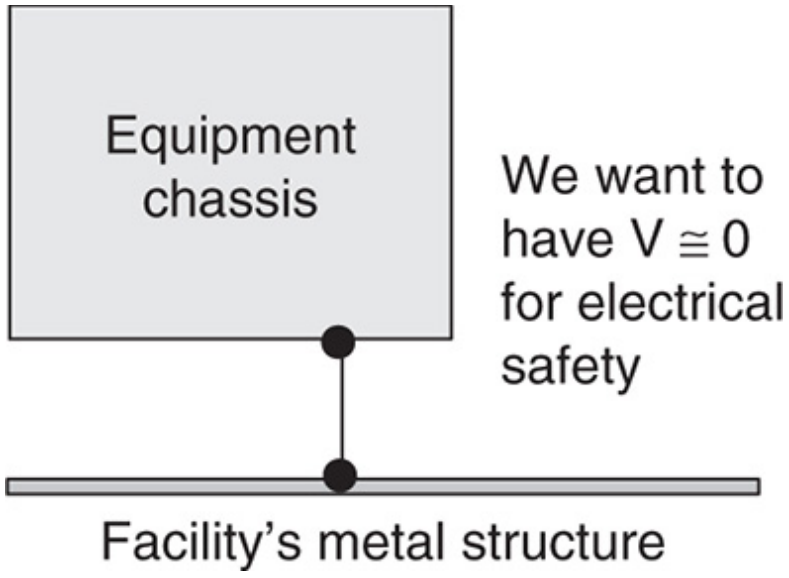


FIGURE 20.39 International creepage and clearance distance requirements between conductors.

International product safety requirements have certain tests to ensure leakage or abnormal currents are not present. This is because PCBs may contain hazardous voltages. These include power supply assemblies, telecommunication circuits, relay-driven instrumentation control units, power switching modules, etc.

When routing AC or high-voltage traces, one must use sufficient trace width and spacing to comply with legally mandated creepage and clearance requirements, as well as current carrying capability and heat dissipation. Maintaining physical distance between two elements at hazardous voltage potential requires compliance with *spacing requirements* published in safety standards. These spacing requirements are referred to as "creepage and clearance." The following definition of creepage and clearance below is identical between all international product safety standards. Illustrations of creepage and clearance measurement distances are shown in Fig. 20.40.

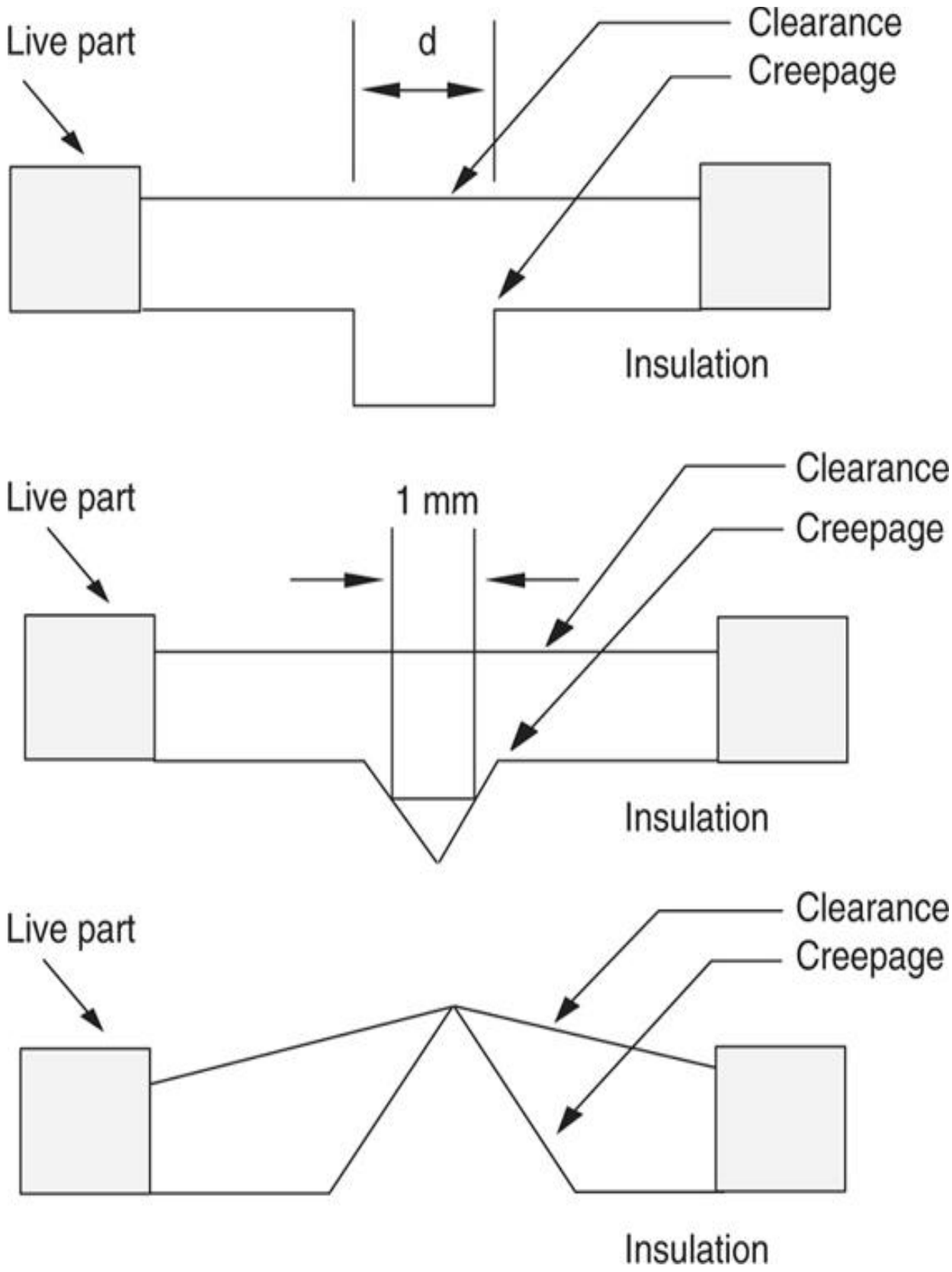

Live part
d
Clearance
Creepage
Insulation
Live part
1 mm
Clearance
Creepage
Insulation
Live part
Clearance
Creepage
Insulation

FIGURE 20.40 International creepage and clearance distance requirements between conductors.

- Creepage is the shortest path between two conductive parts, or between a conductive part and the outside, bounding surface of the equipment, measured along the surface of the insulation.
- Clearance is the shortest distance between two conductive parts, or between a conductive part and the bounding surface of the equipment, measured through air.
- The bounding surface is the outer surface of the electrical enclosure considered as though metal foil was pressed into contact with the accessible surface of insulation material.

When dealing with ground currents, it's important to remember that current must always return to its source, per Ampere's law. This return current may take numerous paths with various amplitudes proportional to the finite impedance within each path, including free space through parasitic coupling, both inductive and capacitive. This fault current could injure people or domestic animals.

20.7 INTRODUCTION TO MECHANICAL DESIGN REQUIREMENTS

The design intent of PCB is to physically support active and passive components to perform a useful function. PCBs are almost always provided in some enclosure, either metal or plastic. Regardless, everything electrical is based on its mechanical structure used to physically support both components and transmission lines.

There are three general configurations of PCB assemblies, related to mechanical assembly:

1. *Functional module*. A section of a PCB where various assemblies are interconnected to provide a functional use. These modules may be separate or integrated into one assembly. Examples of a functional module is a power supply, digital interfaces, analog processing, I/O interconnects, plug-in disk drive assemblies, adapter cards, wireless modules, and a host of other items used at the same time on one assembly. Both electrical and mechanical interconnects occur between modules.
2. *Plug-in module*. This may or may not be an optional module used to extend the capabilities of a system. A plug-in module typically plugs into a motherboard, a backplane or external interconnect. A plug-in module must be mechanically supported on one edge by some type of connector along with other physical support on the other sides.
3. *Mechanically mounted module*. This is a module mounted and/or supported in a mechanical assembly or housing with a number of mechanical fasteners around its periphery. The most common mechanically mounted module is a motherboard frequently found in personal computers and communication equipment using one or more mechanical fasteners, such as screws, clips and standoffs.

All forms of PCBs have common requirements necessary to meet their functional requirements, although there will be significant variations due to product definition requirements. For example, the requirement for board flatness due to bow and twist may be different for a plug-in module than for a mechanically mounted assembly. The requirements for number and location of mounting fasteners for a mechanically mounted module will be different for a relatively thick PCB with low-mass components than for a simpler assembly with high-mass components.

The following list of factors must be considered and evaluated during the design and assembly process:

- Configuration of the physical structure; size, and form factor
- Need for mechanical attachment and mountings
- Compatibility with EMC and other environmental concerns
- Method of mounting such as horizontal or vertical as a consequence of other factors such as dust and moisture
- Other factors requiring special attention, such as thermal management, shock and vibration, humidity, salt spray, dust, altitude, and radiation
- Degree of support
- Retention and fastening
- Ease of removal

20.7.1 General Mechanical Design Requirements

The general mechanical design requirements for PCBs and the assembly include the methods of dimensioning, mounting, insertion and removal of plug-in components or assemblies, retention and extraction. Frequently, the mounting method is predetermined as a design requirement with existing hardware. In other situation, the printed board designer has a choice in determining which mounting method is more suitable after considering such design factors as the following:

- Physical size and shape based on form, fit and functional requirements
- Input/output locations for connectors
- Area and volume restrictions

- Accessibility requirements
- Ease of repair/maintenance
- Modularity requirements
- Type of mounting hardware
- Thermal management
- Electromagnetic compatibility

20.7.2 Dimensioning and Tolerancing

Dimensioning and tolerancing for PCBs and their assemblies must ensure that the product is appropriately designed for proper form, fit, and functional requirements for the complete product life cycle. This includes manufacturing to end use or disposal. Dimensioning and tolerancing is critical during the design, manufacturing, assembly, inspection, test and acceptance phases.

Regardless of the dimension and tolerance standards used, there should be at least two primary data references called datums (Fig. 20.41). The purpose of a datum is to ensure the integrity and accuracy of alignment during the manufacturing of a multilayer assembly. In general, it should be a nonfunctional hole or a surface feature that is used as the primary datum reference for final dimensional measurements. The datum reference should not be a machined edge that is formed in the last phases of the manufacturing, fabrication or assembly process in a secondary machining operation.

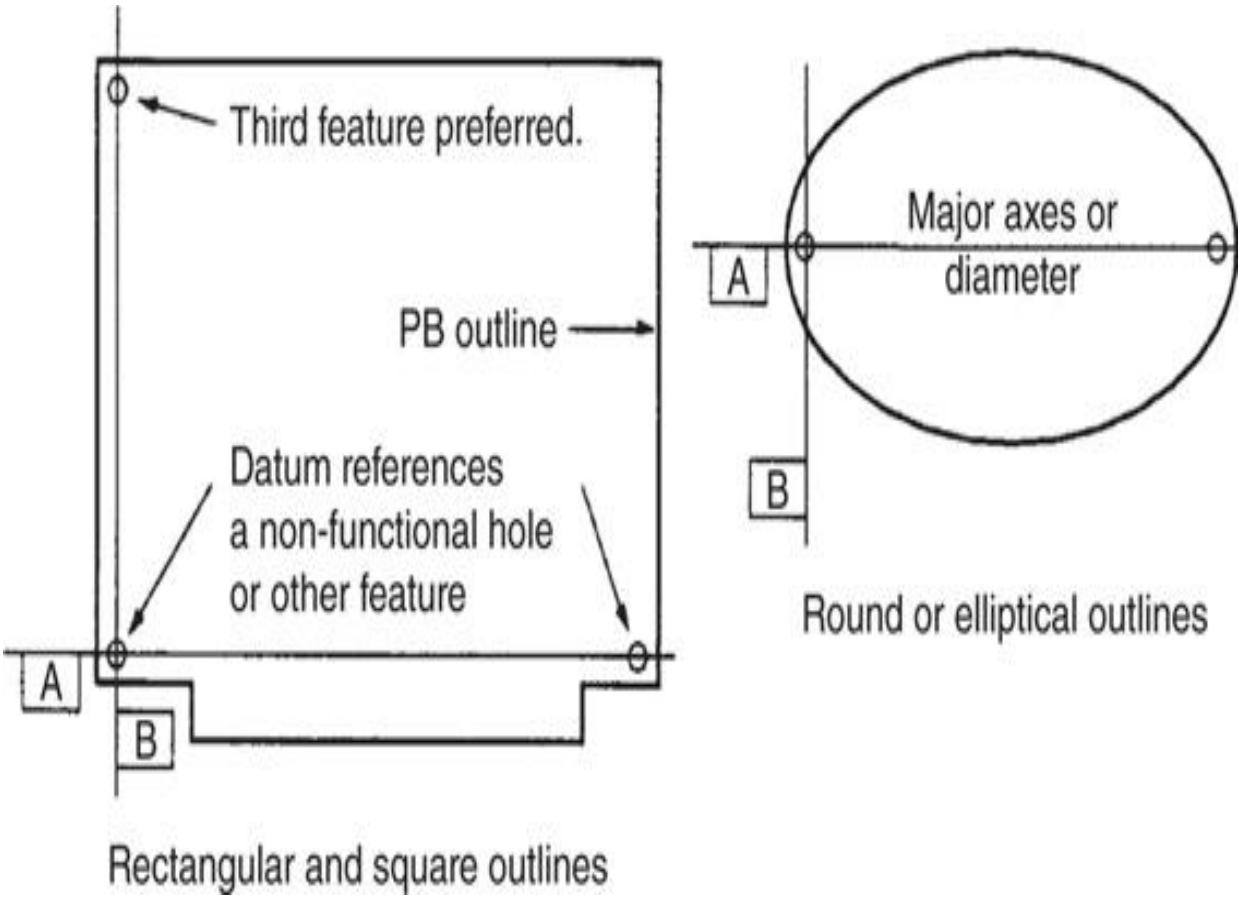


FIGURE 20.41 Illustration of a PCB using datum as a references to ensure accuracy of manufacturing.

20.7.3 Mechanically Mounted Printed Board Assemblies

PCB assemblies should be designed to ensure that both mechanical and electrical grounding requirements remain unchanged throughout its product life cycle. The following are generally accepted requirements and practices for mechanically mounted assemblies:

- The PCB assembly should be supported within 25 mm of the edge of on at least three sides.
- Fabricated printed boards having a thickness from 0.7 to 1.6 mm should be mechanically supported on 100-mm or

lower intervals. Assemblies thicker than 2.3 mm or less should use 1.3-mm intervals.

- Fasteners should not be located on less than assembly with a small thickness, or a fastener’s head diameters, whichever is less, from the edge of the assembly.

20.7.4 Physical Support for PCB Installed in a Card Cage

One advantage of using plug-in printed board assemblies (PBAs) is the ability to add or remove a board within an enclosure for manufacturing or maintenance purposes. Use of mechanical card guides makes it easy for changing configurations and upgrading functional performance. There are many hardware designs available for the purpose of providing a card guide securement method. The design is predetermined or may be developed based on the size and shape of the board assembly. The degree of dimensional accuracy needed to ensure proper mating alignment, along with the mating connector system is important for operational performance and in some application, is used to minimize board edge radiated emissions between the power and return planes. The metal card guide thus functions as an EMI shield.

20.7.5 Retaining PBAs

Shock, vibration, and normal handling requirements necessitate that any assembly be secured or retained in the system by some form of mechanical device. Some retaining systems are attached as hardware to the board during assembly. Other retaining systems are built into the mounting hardware when the board is installed in a card cage. The selection of a proper retaining system is

important, since the retaining devices may reduce the amount area on the board for component mounting and interconnections, and can add significantly to the cost of the electronic equipment.

20.7.6 Extracting PBAs

A number of unique methods have been developed and applied to solve the various problems of extracting board assemblies from their enclosures. The most common industry-standard extractor is injection-molded plastic hardware that is free to partially rotate when attached with a pressed-in pin. Many of these extraction tools use a minimum of space, thereby maximizing available area for components and conductor routing. They also protect both the board and the associated mating connector(s) from damage during the extraction process.

The following should be considered when selecting among the many different types of extraction tools:

- The area available for attachment
- The extractor’s effect on the mounting pitch of the assembly
- The need for special provisions such as mounting holes, mounting clearance holes and notches
- The size of the extractor, especially if the extractor is to be stored in the equipment with which it is used
- The need for an extraction device that is permanently attached to the assembly, usually by riveting
- The need for specially designed considerations, such as load-bearing flanges, in the assembly mounting chassis or cage hardware
- The suitability of the extractor to be used with a variety of board sizes, shapes, and thicknesses

- The cost of using the extractor, both in piece price and added design costs
- Degree of access required to engage and use the extraction tool

20.7.7 Shock and Vibration

Shock, vibration, flexing, and bowing can be functional performance and reliability concern especially for larger sized assemblies. For many board assemblies, the worst-case exposure to shock and vibration occurs in nonfunctional or operational usage during shipping and other forms of transportation from one location to another, or possibly during functional use when the product containing is inadvertently dropped on the floor. Other board assemblies are designed to withstand specified levels of shock and vibration in transportation. The design requirements for shock and vibration vary, depending on each family of general requirements. For example, there are nonoperating shock and vibration requirements for vehicular, train, ship, and air transportation which include various procedures and requirements for packaging. The shock and vibration functional design requirements vary and are dependent on the application. Some sources of shock and vibration are very obvious while others are not. The levels and duration of shock and vibration vary significantly in each application: An electronic sensor mounted on a vehicle’s axle is different from the radio mounted in the dashboard. There are also differences among ground-based, rack-mounted, industrial control equipment, aircraft, aerospace, and munitions applications. Some vibrations are subtle, low-level continuous, and are frequently caused by electric or gas motor-driven rotating machinery and equipment. Continuous low-level vibrations can induce *mechanical fatigue* in some electrical/electronic equipment.

20.7.8 Mechanical Shock

Mechanical shock is be defined as a pulse, step or transient vibration where the excitation source is nonperiodic. Shock is a suddenly applied or increment of force by a sudden change in the direction or magnitude of a velocity vector. With few exceptions, shocks are not easily transmitted to electronic equipment due to their relatively light mounting frames and structures. Most shock to electronic equipment in the consumer, commercial, and industrial markets are due to dropping during handling or transportation, the exceptions being electronic sensors or equipment mounted to heavier mounting frames such as vehicle axles and punch-press-like equipment, or military equipment subjected to air dropping or to explosive forces such as munitions. Most shock impact forces result in a transient type of dampened vibration, influenced by the natural frequencies of the mounting frame. Generally, shock either results in instantaneous failure or functions as a stress concentrator by reducing the effective strength of the connection or lead for subsequent failure due to additional shock(s) and vibration.

20.7.9 Vibration

Vibration is a term that describes oscillation in a mechanical system, and is defined by the frequency or frequencies of oscillation and amplitude. Board assemblies that are subjected to extended periods of vibration will often suffer from fatigue failure, which can occur in the form of broken wires or component leads, fractured solder joints, and cracked conductive patterns or broken contacts on electrical connectors. The frequency(s) of vibration, resonances, and amplitude(s) all influence the rate of failure.

Flexing and bowing is the result of induced shock and vibration into the printed board assembly (PBA). Different

mounting methods have differing susceptibilities to shock and vibration. In general, most small functional modules are manufactured as components and are frequently encapsulated with a polymeric potting material into a solid mass. They therefore have minimal shock and vibration requirements within the module. The plug-in modules are restrained on one edge by the edge-board connector(s) and to some extent along the two other sides by mechanical guides. This leaves only one edge of the assembly free to flex from shock and vibration or to bow from residual manufacturing or assembly stress.

However, a handle along the free edge of the PBA or a restraining bar can be located across the center of the free edge of the assembly and mechanically attached for support at the ends of the restraining bar to mounting hardware such as a card cage. Generally, the mating edge-board connector has a molded-plastic body that provides mechanical support to the mated edge-board connector and has sufficient compliance in the electrical contacts to maintain good electrical connections within the connector’s performance specifications. Mechanically mounted PBAs can be more of a shock and vibration concern for three main reasons:

1. The board assembly can be very large, physically.
2. The board assembly is misused as a mechanical support structure for high-mass components, such as magnetic components that include iron-core transformers and inductors, power supplies, and large functional modules.
3. The board assembly is not included in the mechanical design definition.

20.7.10 Major Shock and Vibration Concerns

Major shock and vibration concerns include the following:

- Flexing between assemblies may cause shorts between adjacent boards or to the enclosure.
- The fundamental mode is the primary mode of concern because it has the large displacements that cause fatigue damage to solder joints, component leads, and connector contacts.
- Continuous flexing of an assembly will fracture component leads and, more important, surface-mounted component solder joints due to mechanical fatigue failure.
- Movement of an assembly within its mechanical guides will be amplified due to shock and vibration or harmonic resonance.
- Fatigue life modeling mounted components has become significantly more complex due to in-use simultaneous application of both vibration and thermal cycles. Vibration strains and thermal strains should be superposed for more representative modeling.

20.8 TYPES OF EDGE MOUNTING FOR CIRCUIT BOARDS

Methods of analysis and minimization from effects of shock and vibration on PCB assemblies are the same as in other engineering applications. Similar solutions can be used. PCB assemblies are designed and manufactured in a wide range of shapes and sizes, with rectangular being the most common. PCBs are a multi-degree-of-freedom system, the fundamental mode which is of primary importance because it has the large displacements that are the primary cause of fatigue failure in solder joints, component leads, and connector contacts. Most vibrational fatigue damage occurs at the fundamental or natural frequency as displacement is highest and stress is maximized. Edge or boundary

conditions are terms used to define the method of attachment of the assembly to a fixed structure, or more generically to a panel on a mounting frame. The term *free edge* is used to define those edges that are not restrained and are free to move and/or rotate outside of their normal mounting structure. The terms *supported edge* or *simple support* is sometimes used to define an edge that is restrained in out-of-plane movements but is allowed rotational movement around the board's edge. The terms *fixed edge* or *clamped edge* are used to define an edge that is restrained in both out-of-plane and rotational movements. Illustrations of both definitions for fixed edge, supported edge, and free edge, and their applications, are shown in Fig. 20.42.

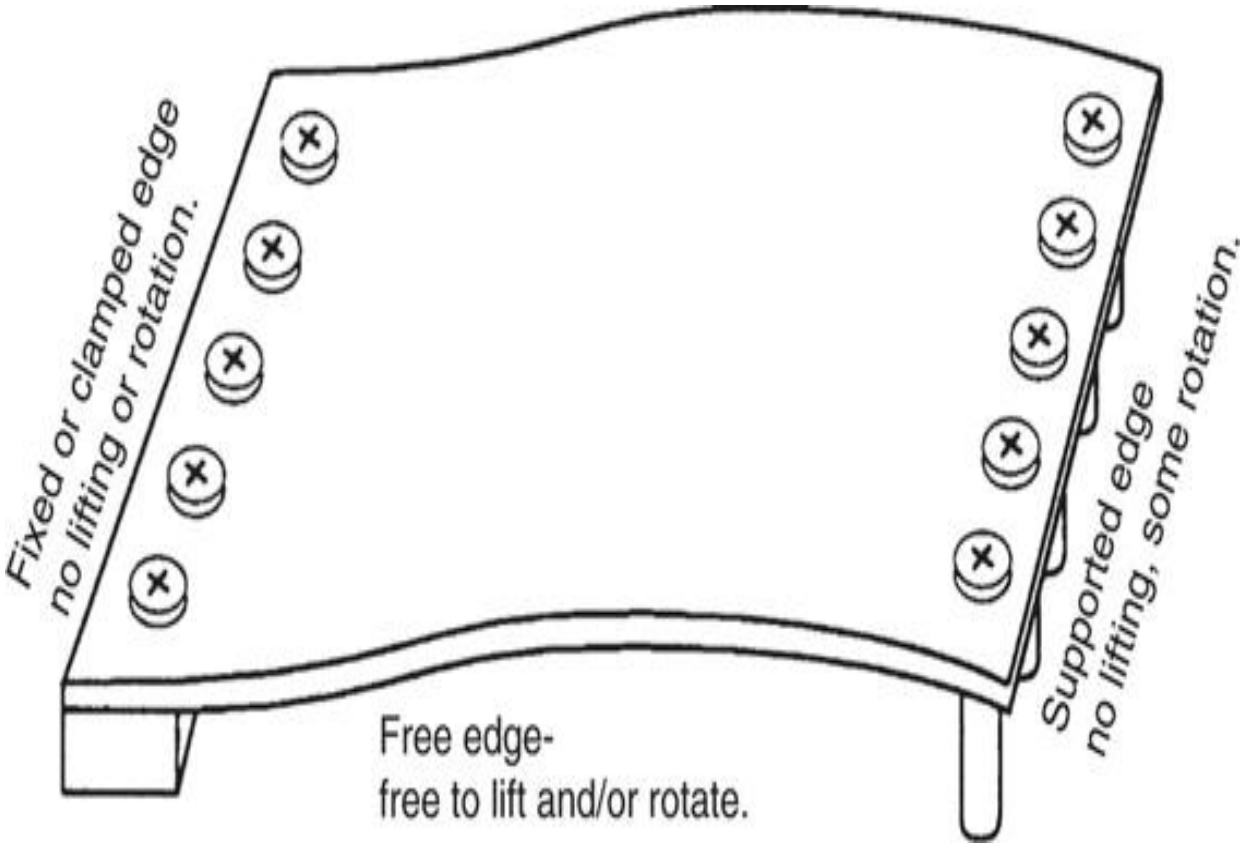


FIGURE 20.42 The method of mounting contributes to shock and vibration concerns.

20.8.1 Board Deflection

The amount of strain on a physical component is a function of the maximum deflection of the assembly when subjected to shock, vibration, twisting, and bending. Components mounted closest to the center of the assembly are subjected to the greatest strain, illustrated in Fig. 20.43.

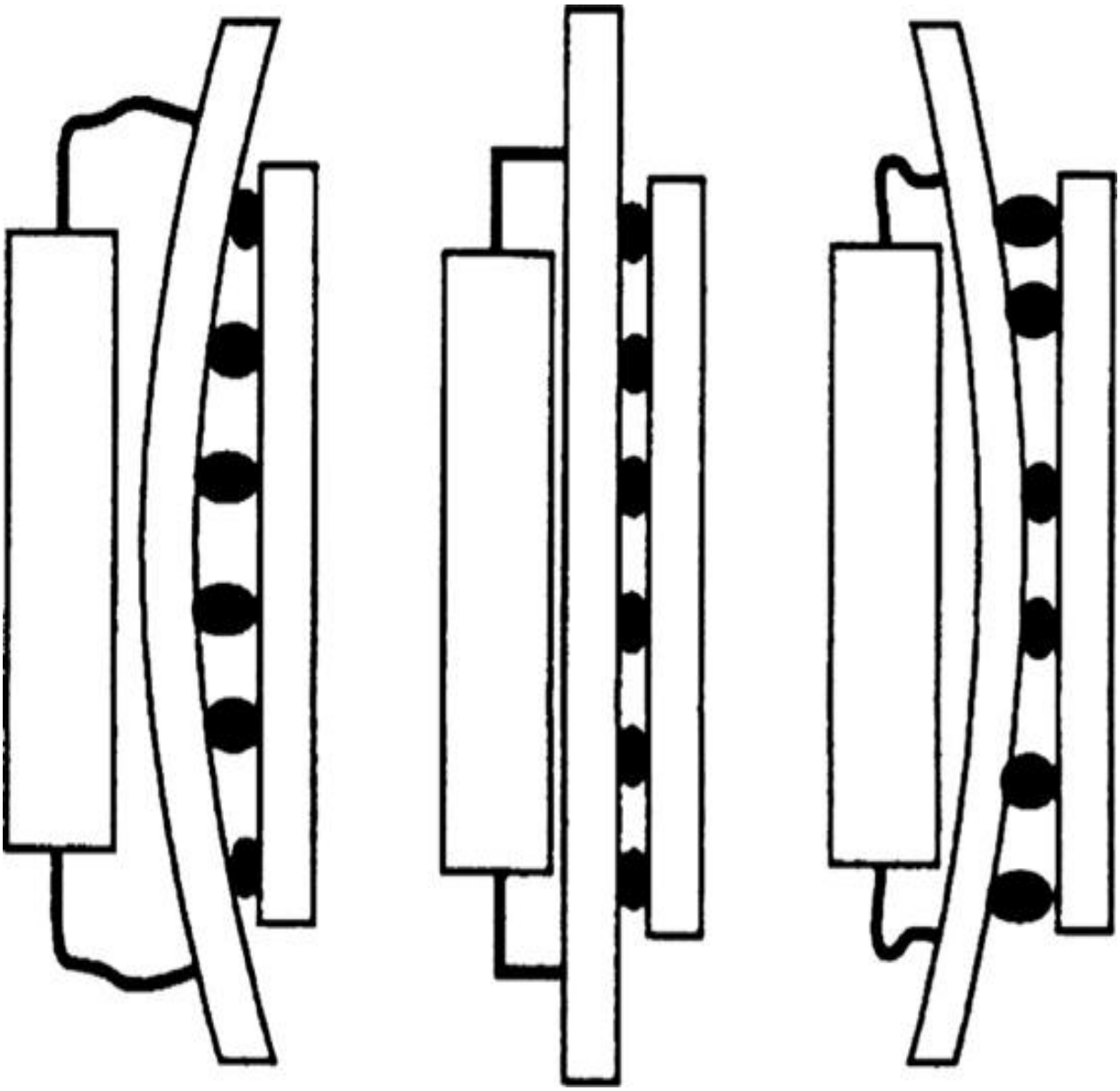


FIGURE 20.43 Bending in a printed circuit board during shock and vibration, with the most severe stresses applied to the components mounted centermost on the assembly.

A set of empirical maximum deflection (d) calculations has been developed by Steinberg. His latest equation[7] has more parameters than previous equations, reflecting the sophistication and requirements for modern PCB designs. These new equations have units adjusted from inches to mm [Eq. (20.7)].

$$\delta = \frac{k\,0.00022B}{ct\sqrt{L}} \tag{20.7}$$

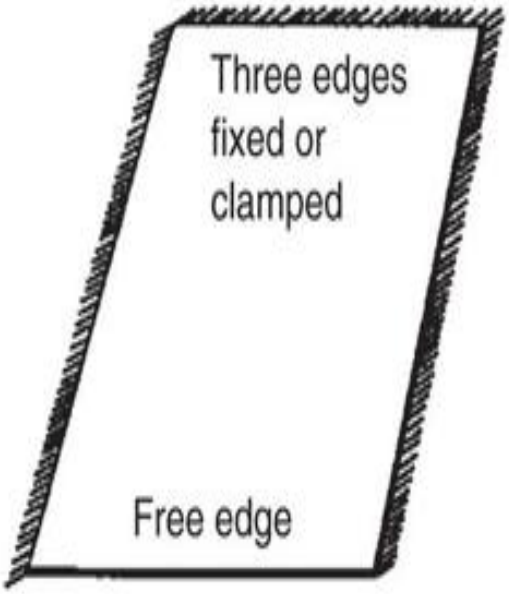
where k = units conversion coefficient; for inches $k = 1$, for mm, $k = 25.4$
B = length of PB edge parallel to component located at center of board (worst case), mm
L = length of component, mm
t = thickness of the board material, mm
c = 1.0 for standard DIP
= 1.26 for DIP with side brazed leads
= 1.0 for PGA with four rows (one row extending along the perimeter of the edge)
= 2.25 for CLCC

Analysis of the maximum deflection calculation formula reveals that components with some compliance built into their component mounting and electrical terminations can be subjected to about twice the vibrational deflection as packaging, provided component size, the PCB dimensions and thickness are equivalent. The latest equation for maximum deflection calculations is rated for 10 million stress reversals when subjected to harmonic (sinusoidal) vibration, and 20 million stress reversals when subjected to random vibration. It must be understood that this equation is a first approximation for predicting solder joint life.

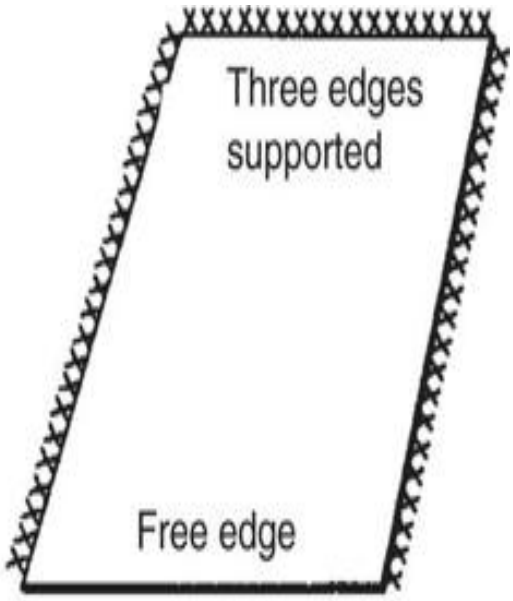
20.8.2 Natural (Fundamental) Resonance of Printed Board Assemblies

The mechanical mounting of a PCB and their components is a key design consideration in the ability of the assembly to withstand shock and vibration. The overall size of the assembly is not a major factor, provided a suitable mechanical support structure is included as a part of the product definition requirements. There numerous ways to mount panels using various combinations of free edges, supported edges, fixed edges and point supports and by calculating fundamental resonances. The following four examples compare the fundamental natural resonances of the same rectangular shaped assembly using different edge-mounting techniques.

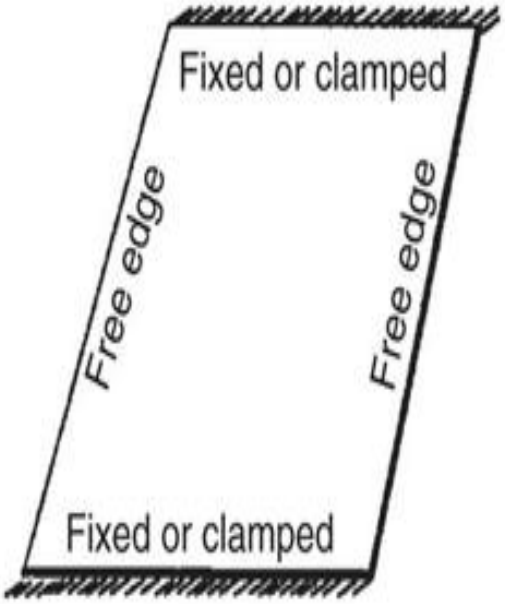
In the following examples—demonstrations of the sensitivity of assemblies to their methods of mounting is provided for comparative purposes (Fig. 20.44). The following are the design requirements and material parameters that were used for the calculations:



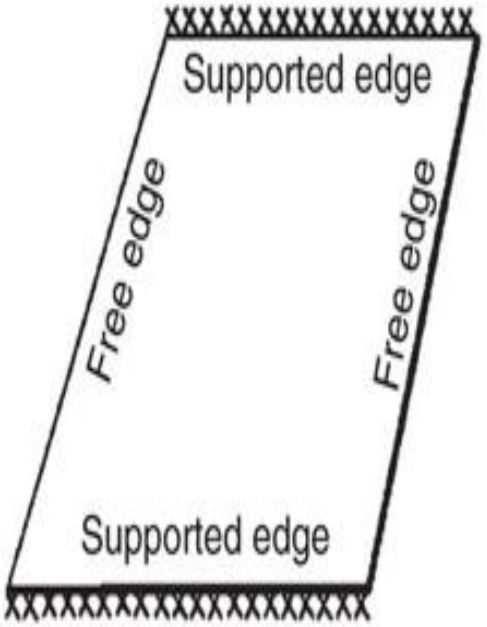
Fundamental resonance frequency
128 Hz



Fundamental resonance frequency
53 Hz



Fundamental resonance frequency
67 Hz



Fundamental resonance frequency
30 Hz

FIGURE 20.44 The same assembly can have a wide range of natural resonances depending on the mounting method, which is why shock and vibration concerns are a critical design consideration.

$$D = \frac{Et^3}{12(1-\mu^2)} \tag{20.8}$$

where D is the plate bending stiffness.

$$M = \frac{w}{g} \tag{20.9}$$

$$f_n = C_o P_o \sqrt{\frac{Dab}{M}}\ Hz \tag{20.10}$$

where f_n is the natural resonant frequency.

20.8.2.1 Methods of Reinforcement and Snubbers. PBAs are stiffened using one or more methods to raise the natural resonant frequency sufficiently above the shock and vibration threat. The most obvious means to achieve this is to change the method of retaining or mounting in the next higher level of assembly. Frequently, though, this may not be an acceptable option due to the resources and schedule changes that may be necessary for extensive redesign. However, some simpler modification in the design may meet functional requirements. Sometimes changing the plug-in guide from a loose supportive guide to a tighter spring-loaded or clamping-type guide may be sufficient. Other methods are to add ribs or stiffeners, additional single-point mounting locations, or *snubbers* across the surfaces of the assemblies.

20.9 ACKNOWLEDGMENTS

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CHAPTER 21

THE BASICS OF PRINTED CIRCUIT BOARD DESIGN

Susy Webb

Design Science, Sugar Land, Texas

There are mountains of information one must gather and understand in order to design any printed circuit board (PCB). Interested parties may be coming from any of a number of different places with any amount of information they know about board design. The purpose of this chapter is to introduce those interested parties to the concepts involved in designing a PCB, without being either overly simplistic or complicated in the approach. It will cover as many of the concepts as possible, while assuming that there is at least some knowledge of the subject matter. Also, there are sometimes different terms in the industry that mean the same thing, so there is a listing of terms at the end of this chapter to use as a cross-reference.

21.1 SOFTWARE SELECTION

The first thing that is needed is the computer software to do the job. There are many different kinds to choose from for both schematic entry and PCB design with additional add-ons that will do an increased level of layers and constraints, auto routing, simulation, even work with the company's MRP system. The PCB designer must evaluate what the needs would be for the types of PC boards to be designed. If only the most basic boards will be produced and they will be a minimum number of layers, one of the free computer softwares on the Web might work for that company. Those softwares are extremely fundamental, however, and should be considered only for the most basic of boards. If the designs will be complex with many parts, many constraints and many layers, one of the higher end software tools may be needed. Even the major software vendors have a range of different levels of what their software will do, and they can help the designer work out which version of the tool might work best for them. It would be most prudent to gather information from several different software vendors before making a decision as to which one will work best for the company's needs.

21.2 STANDARDS

There are standards for almost everything that is done in the design world, and they are generally set up by volunteer committees of experts. They are compiled by subject matter and available in written or electronic forms from IPC (Association Connecting Electronics Industries, Bannockburn, Ill. www.ipc.org). The IPC serves all the disciplines associated with PCBs. Designers should get copies of all the standards that apply to the kind of work they will be doing, become familiar with them, and refer to those standards often. If the information or terminology contained therein is confusing,

the first publication on the designer's list of must haves might be IPC-T-50, which is the "Terms and Definitions" document. Most of the IPC documents have a cost associated, but they may save the designer from a world of problems they might otherwise encounter.

Examples of design standards are as follows:

- IPC 222x—Generic Standards on Designing Printed Boards (including flex and MCM)
- IPC-2611—Documentation Requirements
- IPC-A-600—Acceptability of Printed Boards
- IPC-A-610—Acceptability of Assemblies
- IPC-6011—Generic Performance Specification
- IPC-6012—Qualification and Performance for PCBs
- IPC-SM-840—Solder Mask
- IPC-4101—Materials for Rigid Boards
- IPC-ET-652—Electrical Testing

21.2.1 Classes of Board by Application

The IPC also has devised classes and levels to help users determine the type of board they are designing as compared to others. IPC performance classes set the standard for how well the product must work. They are as follows:

Class 1 are general electronics like toys, games, and general products. If these products fail, there are no large ramifications.

Class 2 are dedicated service electronic products like business and industry machines and communications equipment. Uninterrupted service is desired, but not life threatening.

Class 3 are high reliability electronic products like military and medical where interrupted service could be life threatening.

21.2.2 Producibility Levels

IPC producibility levels communicate the degree of difficulty of manufacturing the features of the board in production. Those levels are:

Level A General Design Complexity—preferred

Level B Moderate Design Complexity—standard

Level C High Design Complexity—reduced producibility

21.2.3 General Standard Objectives

There are other industry standards that may be required for a specific type of board such as computer, telecom, medical, etc. These standards might have requirements for boards such as size, shape, mounting, and connector location that determine whether that board will properly interface into any like system. The military has its own set of very tight standards that govern how those boards will be built and assembled. There are even standards from American National Standards Institute (ANSI) and the Electronics Industries Alliance (EIA), which governs dimensioning and tolerancing of electronic components. That is done so that when a part says it is an SOIC, for example, it actually matches that tolerance standard set up and can be used as a replacement for another SOIC.

Some companies set up standards for the way work is done within that company as well, in order to insure that the flow of information is the same for every project and every

person in the department. Companies that are interested in standardizing might include

- The flow of work
- Library issues
- Processes and responsibilities
- Input, output, and saving specifications
- Notes, stackups, naming, and numbering
- Reference information
- Anything else that is important to that company

Additionally, some companies choose to set up their own standards for fabrication and assembly that cover issues like exactly what is expected from the fabricator, what are the deliverables? Are repairs, modifications, or X-outs allowed? What are the panelization, and electrical testing issues? What permissions are needed?

Since PCB design is very precise work, all of these types of standards (and more) may be necessary to ensure consistent quality. If the designer is involved in setting up these standards within his or her company, they might choose to set up checklists to remind them of the important issues on that or any project. An input checklist might include all mechanical, electrical, organizational and testing criteria, while an output checklist can be used as a reminder for any items needed to complete the project.

Standards are important because there are many ways to achieve the same goals in PCB design, and there are many people to communicate with. The designers, purchasing agent, fabricator, assembler, technician, etc. all have to speak the same “language” so there is less chance of misunderstanding and miscommunication. The design methods and documentation used will be the most clear, concise and understandable for all involved if they all reference the same set of standards. Many of the

illustrations contained in this chapter were inspired by information from the IPC standards.

21.3 THE SCHEMATIC

Occasionally, the PCB designer is asked to enter the schematic, or make modifications to it, so it is helpful to have an understanding of the way it flows. The connectivity information for the PC Board comes from the schematic. The schematic designer creates drawings of symbols representing the parts to be connected on the board to perform the electrical functions that are needed. The pins on those symbols represent the pins on the parts and the connectivity between those pins represents the connections, or nets, to be made on the board.

21.3.1 Standards for Schematics

Not surprisingly, there are standards for drawing schematics too. One of the most important is that the circuits should flow from left to right on the page (see Fig. 21.1). This means that is it helpful when reading the schematic if the inputs are on the left side of the symbol or page and the outputs are on the right. It helps if the pieces of a connector are brought out to the edge of the page, as they are easier to find there. Also, the power connections are generally kept to the top of a symbol, and the ground connections are kept to the bottom. It is very helpful if all pins on every symbol are shown whether used or not so that there is never any guess as to whether a pin was not used or was forgotten. If a symbol has multiple parts, called gates, they must all be shown for the same reason. It is very helpful for the board designer if the circuit designer places all the decoupling capacitors near the part they will be used on so that he or

she knows which pins the circuit designer planned to decouple. And lastly, a grouping of symbols on a schematic will generally correlate to a desired grouping of parts on a board.

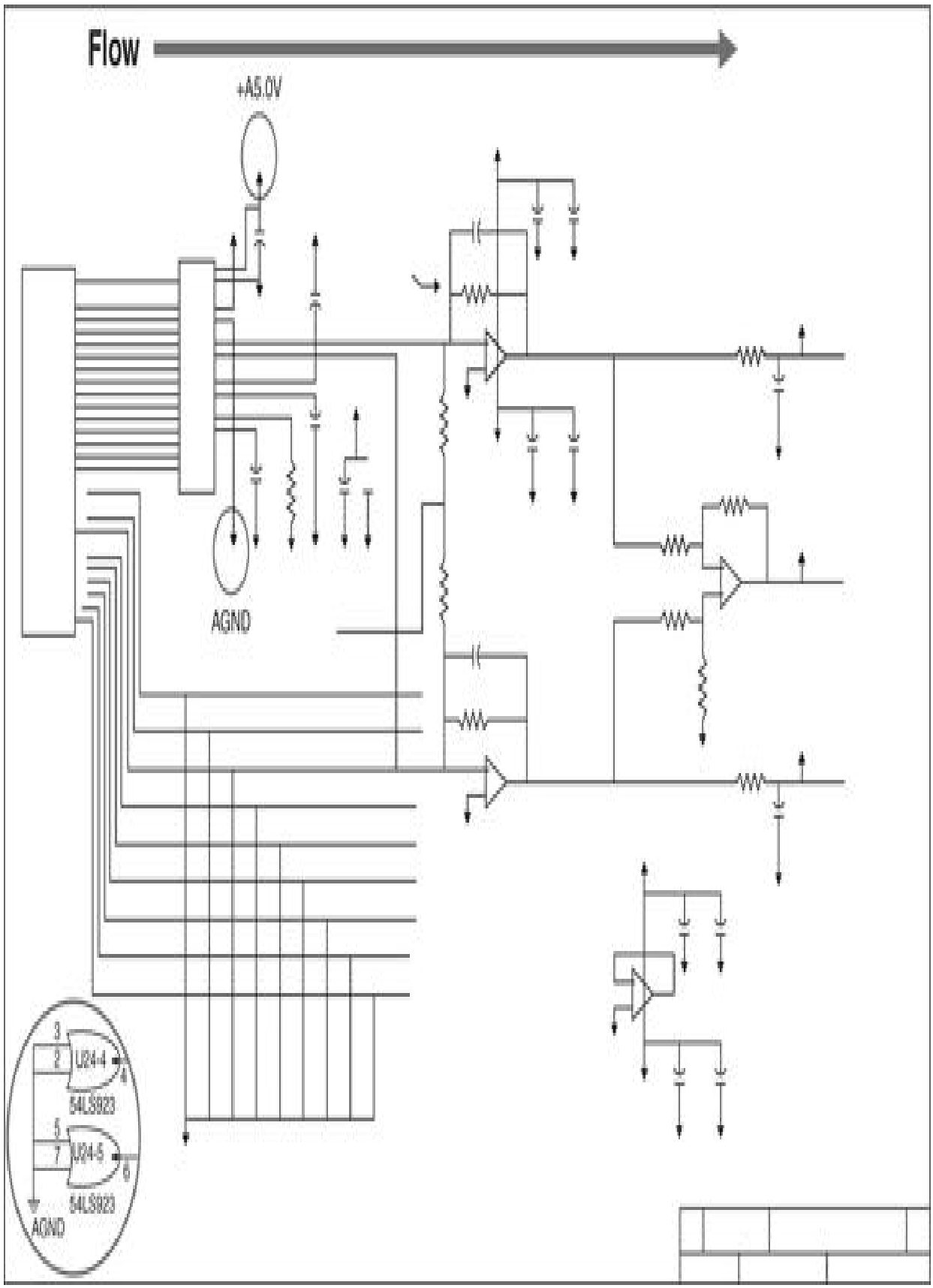

Flow
+A5.0V
AGND
3
2
U24-4
4
54LS923
5
7
U24-5
6
54LS923
AGND

FIGURE 21.1 A schematic page set up for good flow pattern (resolution to small annotations).

21.3.2 Schematic Software

The schematic software may output several other helpful bits of information. As mentioned, the main purpose is to correlate each symbol to a part and each part will correspond to a footprint on the board. The software can be used for a block diagram, which is very helpful for getting an overview of the entire circuit with a minimal amount of information. It will also assign a different reference designator to each part based on the kind of symbol it is and the number of them on the schematic. A list of all the parts contained in the schematic called a parts list or bill or materials (BOM) can be extracted for help in ordering everything for the board. Special groupings of parts, design rules, and other bits of information may also be extrapolated. The software will also compile all the parts and connectivity into a net list that will translate everything into the PCB software.

21.4 PARTS

There are a multitude of parts that may be used on a PCB and each has its own needs for mounting, soldering, cleaning, etc. The parts that connect into holes through the board are called through hole devices (TH). Their leads connect through the holes with solder or pressure. See Fig. 21.2. The PCB goes through many heating expansions and contractions as it is being assembled and used, and the bends in many of their leads (called strain relief) help to account for the difference in thermal expansion between the

board material and the part. Those bends can flex slightly back and forth to keep the device from cracking.

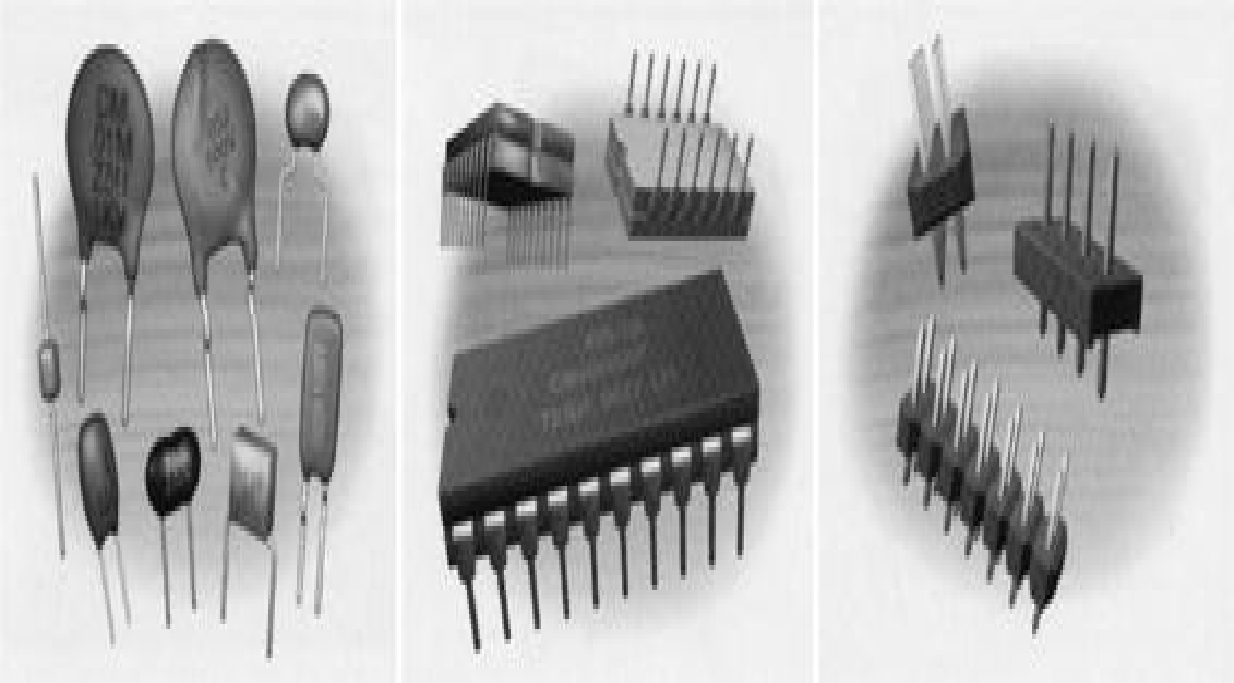


FIGURE 21.2 Examples of through hole devices.

Another type of device connects to the board by soldering the leads onto a pad on one side only. Those are called surface-mounted devices. These devices are generally smaller than their through hole counterparts, so the strain relief is not as needed as on the larger parts. Some surface-mounted parts do have strain relief though. See Fig. 21.4. The majority of the newest parts made are in this surface-mount category. See Fig. 21.3.

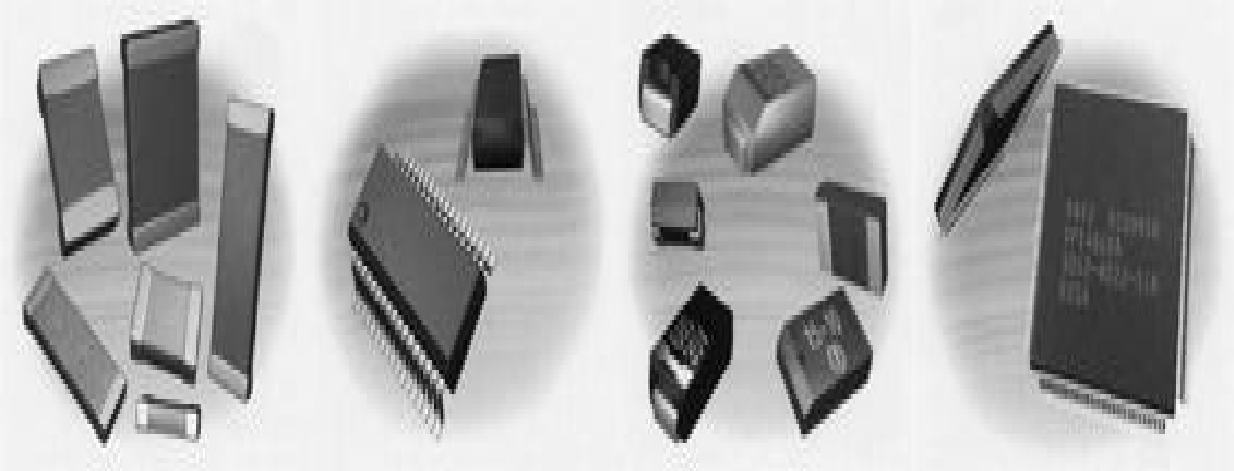


FIGURE 21.3 Examples of surface-mounted devices.

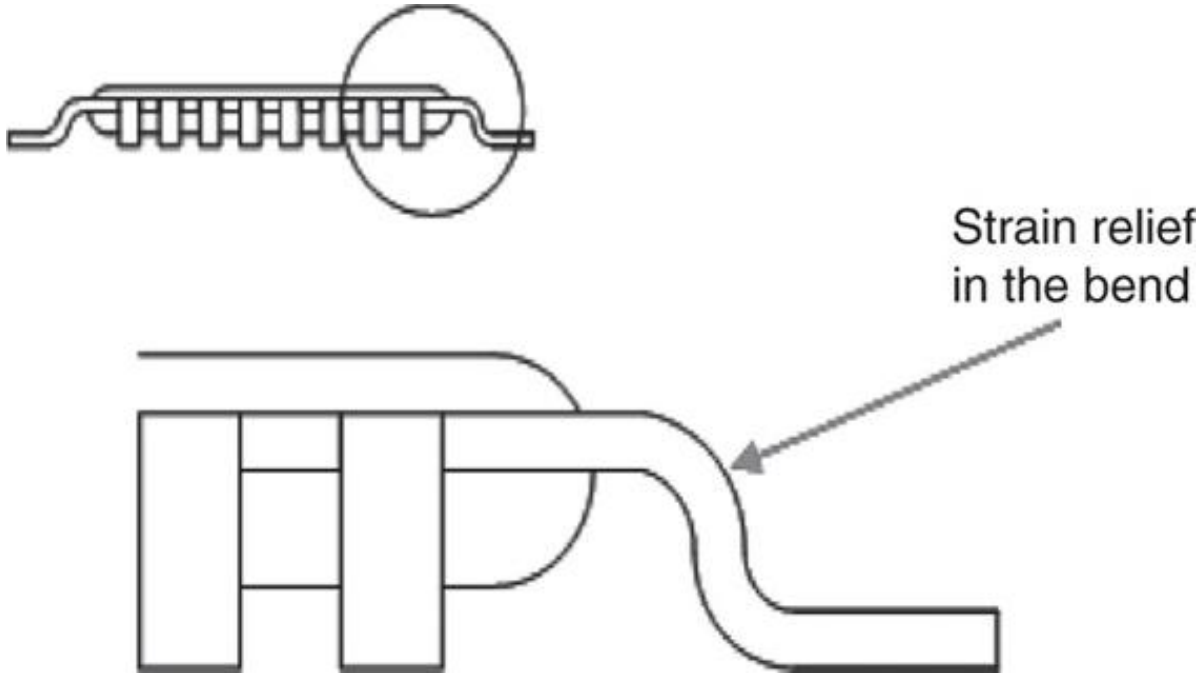


FIGURE 21.4 A surface-mounted device with strain relief.

21.4.1 FOOTPRINTS

The footprints are the actual landing pattern for the leads of the electronic parts. This is where they will be placed and soldered into place on the board. The footprint will consist of the pad and solder mask opening for each connection point

(lead, ball, etc.) in a pattern set up by the device. The footprint may also contain silkscreen information, assembly information, reference designator, pin numbers, placement boundary, paste mask, an origin, and orientation information. See Fig. 21.5.

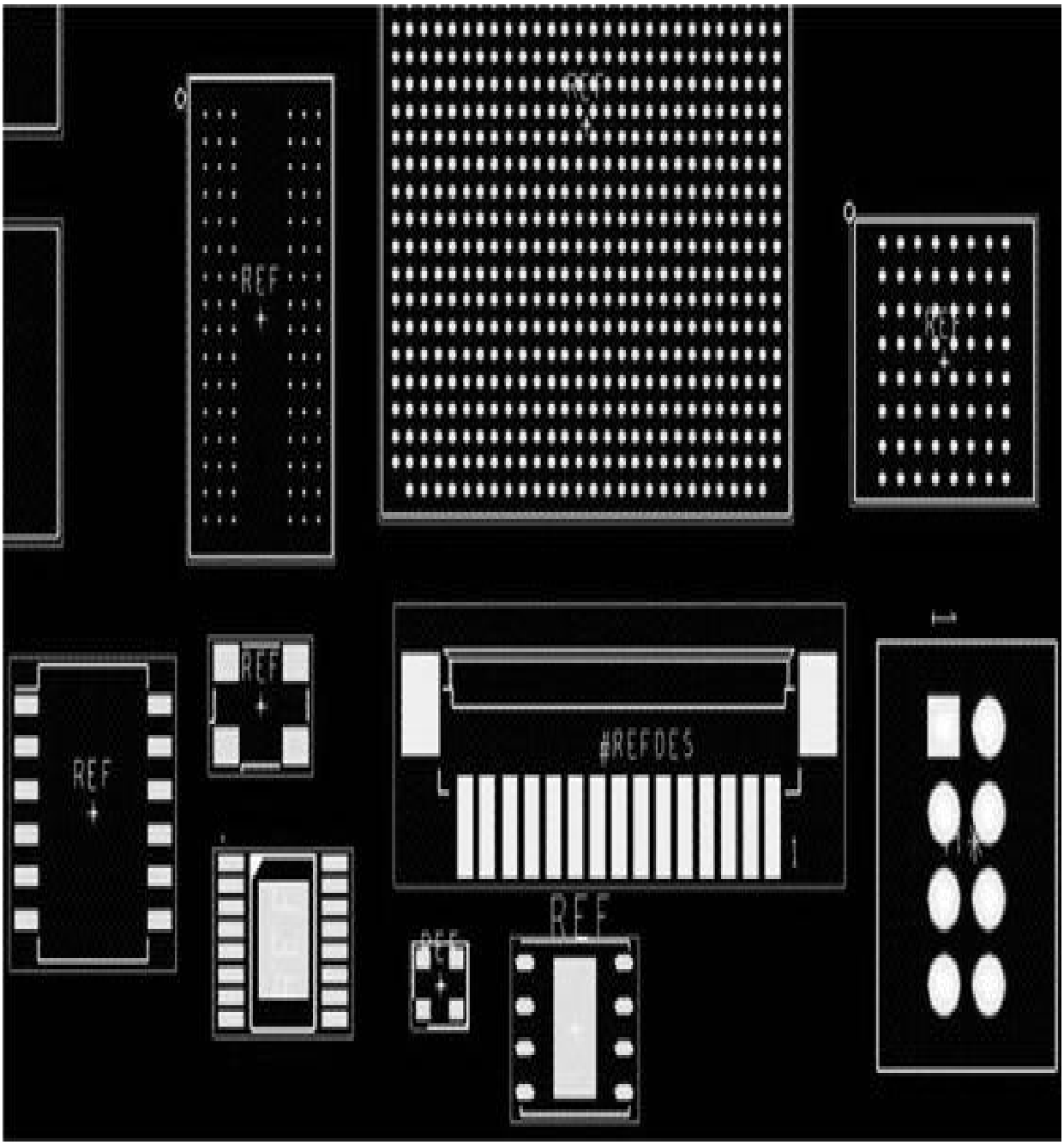


FIGURE 21.5 A few example footprints.

The footprints are usually made generically without ties to a particular part, pin function, or connection and that information is then assigned when the schematic net list pulls the footprints and connections into the PCB database. In other words if there are two or more symbols on the schematic that have different functions but their electronic body size is *exactly* the same, they might each use the same footprint. The pins on part A would take on the net list properties from its schematic part and the pins from part B would take on the net list properties from its schematic part and they might be completely different. Each individual part's needs must be considered carefully before assigning it to a footprint.

Several things are very important in footprint design. Obviously it needs to have the correct number of pads in the correct locations. The origin of the footprint will tell the assembly machine where to pick up the part for placing it onto the board. And the orientation of the footprint will lead assembly to install the part in the correct position. The height of the part will affect the size of the pads that will be used because of the amount of solder needed, and the board designer can use included information on the height of the part to check where things will fit in a 3D manner. The footprint will also need the correct silkscreen outline so the designer will know where the edges of the part are, and the correct placement boundary so that they will know how close other parts can get to that part.

Attributes are helpful to include in part information. They might include things like the manufacturer's part number, what the part is or does, special layout needs, whether the pin is a source or load, and the signal's rise time. These bits of information keep the important information right at hand when using a part. They might be placed on a "construction" layer of the part, or entered into it as part or pin attributes when the netlist comes into the PCB.

Using a naming convention is for all parts makes it very easy to find parts in the library. IPC has a naming convention that includes part type, lead span, size, height and number of pins. Other part libraries available on the Web have other naming conventions, or the designers can choose one of their own that works for them as long as it meets all of their needs.

21.5 PADSTACKS

Each connection on a footprint will be made with a padstack, and those will be very different for through hole and surface-mounted leads. The through hole padstacks must accommodate connection pads for each layer of the board, solder mask for the top and bottom, antipads and thermal pads where necessary. The antipad completely isolates a pad on a plane layer from the plane so there is no short, while the thermal pad makes a small connection to a plane. See Fig. 21.6. The surface-mounted pads are simpler, needing only one connection pad on the outer layer, a solder mask and solder paste pad. The solder paste pad will become the opening for the solder paste to be applied for soldering the part to the board. See Fig. 21.7.

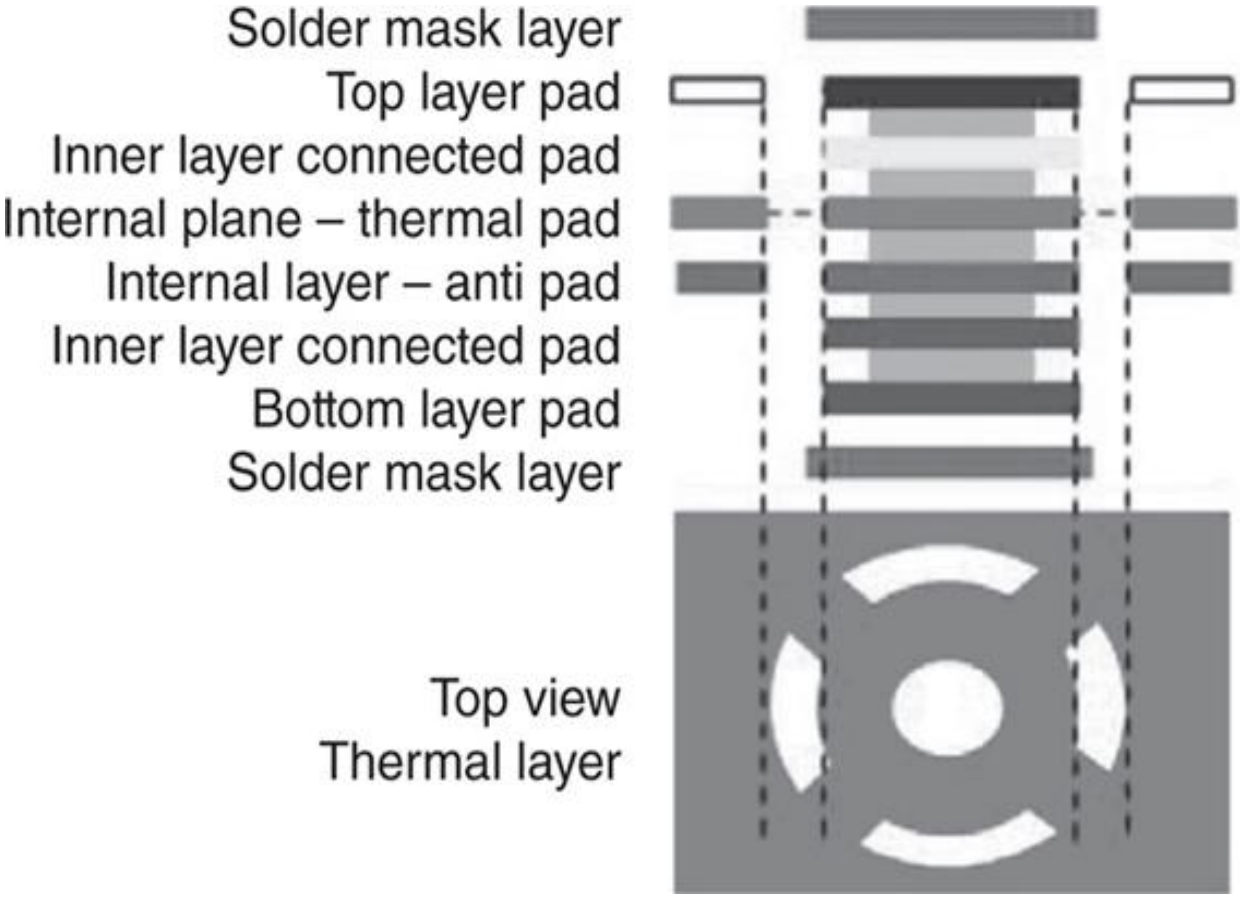


FIGURE 21.6 Through hole padstack.

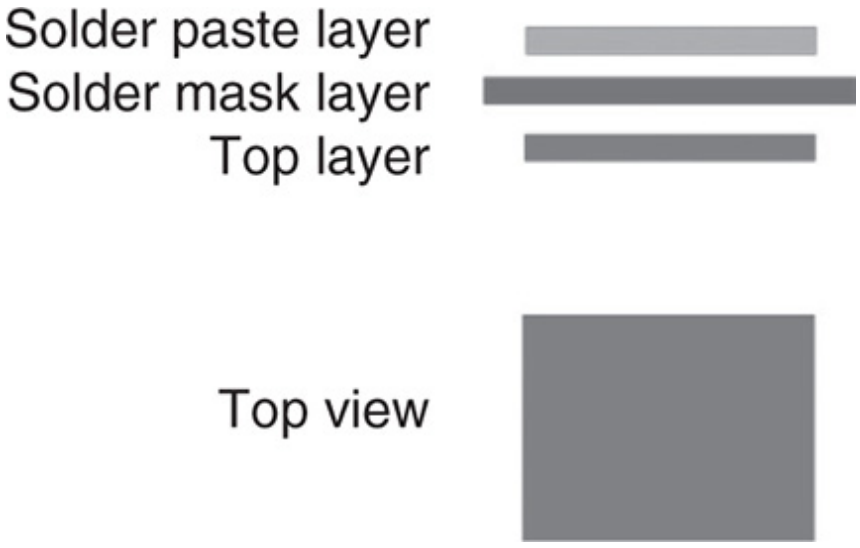


FIGURE 21.7 Surface-mounted padstack, side and top view.

It is a good idea to have a standard for the padstack design too. The size, shape and pad to hole ratio can vary fairly dramatically depending on the source of the information used to make them. IPC has set up standards for these issues as well, and they can be used for every footprint built. For surface-mounted parts, they have set up three categories—minimum sized, nominal sized, and maximum sized which allows for designers to use a more personalized approach to the IPC standard depending on the normal density of their boards. Whichever standard is chosen, it is a good idea to always follow it. Consistency in the way things are done helps multiple designers working together, fabricators, testers, and assemblers.

The choice of an individual part for inclusion into a board can be based on many things besides just function. Among other things, the size, shape, voltage, pitch, and ease of use should be considered. The physical shape and pin location of the pins can be less than clear and can cause problems with assembly if not clarified. If the part is high speed, it can be very important that the power and ground pin locations are very close together. See Fig. 21.8 for some physical part comparisons.

Footprint	Positives	Negatives
SMT	Small, low impedance, power/ground pins	Fanout
Thru	Easy route any layer	Larger, hi imp, P/G
BGA	Lg. amt of info	Rework issues
QFP	Lg. amt of info	Size/pin count ratio
Discrete	Place where needed	More physical parts
R-Pak	Less space, better tol	Distance to route
Embedded	No space, good place	Complexity of design

FIGURE 21.8 Part comparisons.

21.6 STARTING A NEW BOARD

When starting to design a new board, the mechanical issues of the entire project should be fully understood. Any mechanical limitations like height restrictions, rounded corners, cutouts, external connectors, etc. must be considered from the very earliest moments of design. This will ensure that everything fits into its allotted space. Is this board a part of something larger, or is it the complete set of electronics involved? One must understand how and when the board will fit into its area. That will affect the orientation of the board (which side is top) and whether cables and plugs will need to be installed prior to installation. The text on the board should be aligned with the top edge of the

board. That will make it easy to read any text on the board while it is in operation.

One way to be absolutely certain that the board being designed will fit into the size and space expected is to interact closely with the mechanical people and their files. All corners, curves, cutouts, dimensions, and keepout areas must be considered. A way all this mechanical interaction with other boards or devices can be brought into the PCB database is with a .dxf, .emn file or something similar from the mechanical drawing. That can be placed on a nonfunctional layer and converted into the board outline and hole location so that there is no possibility for error. Since the mechanical people are generally the ones that make the connectors, switches, and plugs fit perfectly together, all that information can be brought into the PCB in the same way the board outline was for a sure fit of those items as well. See Fig. 21.9.

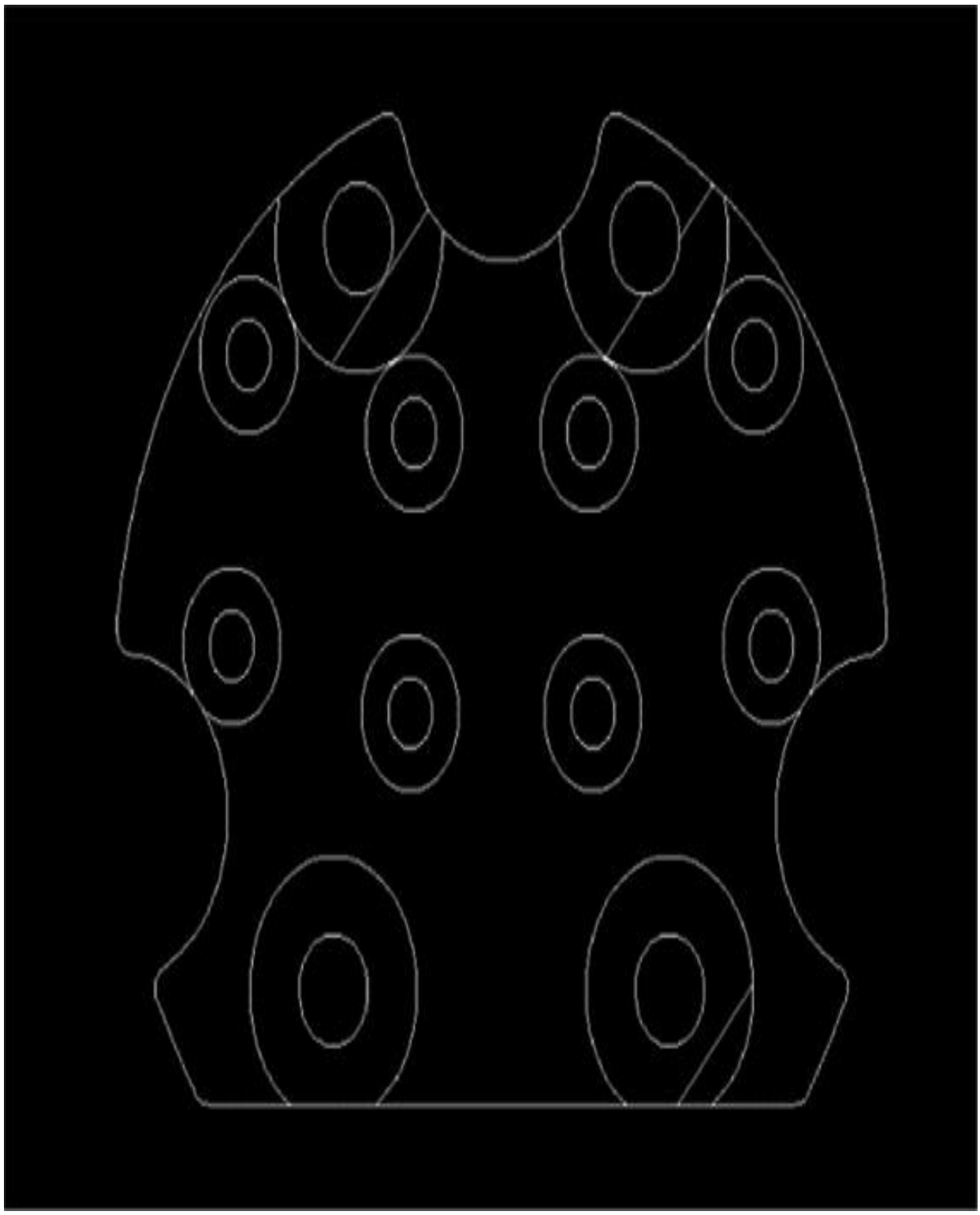


FIGURE 21.9 Bring in a .dxf file for accuracy.

Another early consideration is to understand the parts involved. The designer should gather data sheets and reference information for all the major components on the board. They can provide information about the part and pin function, the signals and their rise time, the need for timing constraints leading to matched length, any and all critical signals and busses, and the size and shape of the part. Many times they will also contain suggested footprint, cleaning, soldering, and lead-free information. While the information contained therein my not always apply to every PCB design, it should always checked for consideration.

This is also a good time to look at the footprints used for the parts chosen. Some of the things to look for would be: will the parts route well together for the flow of a signal or bus (see Fig. 21.10), do they have good indication of how the pins are numbered for testing, are they easy to place when manufacturing, can the programmable pins be changed for best routing, and are there other parts of the same density on the board so that one single part is not driving the board to a higher complexity unless absolutely necessary.

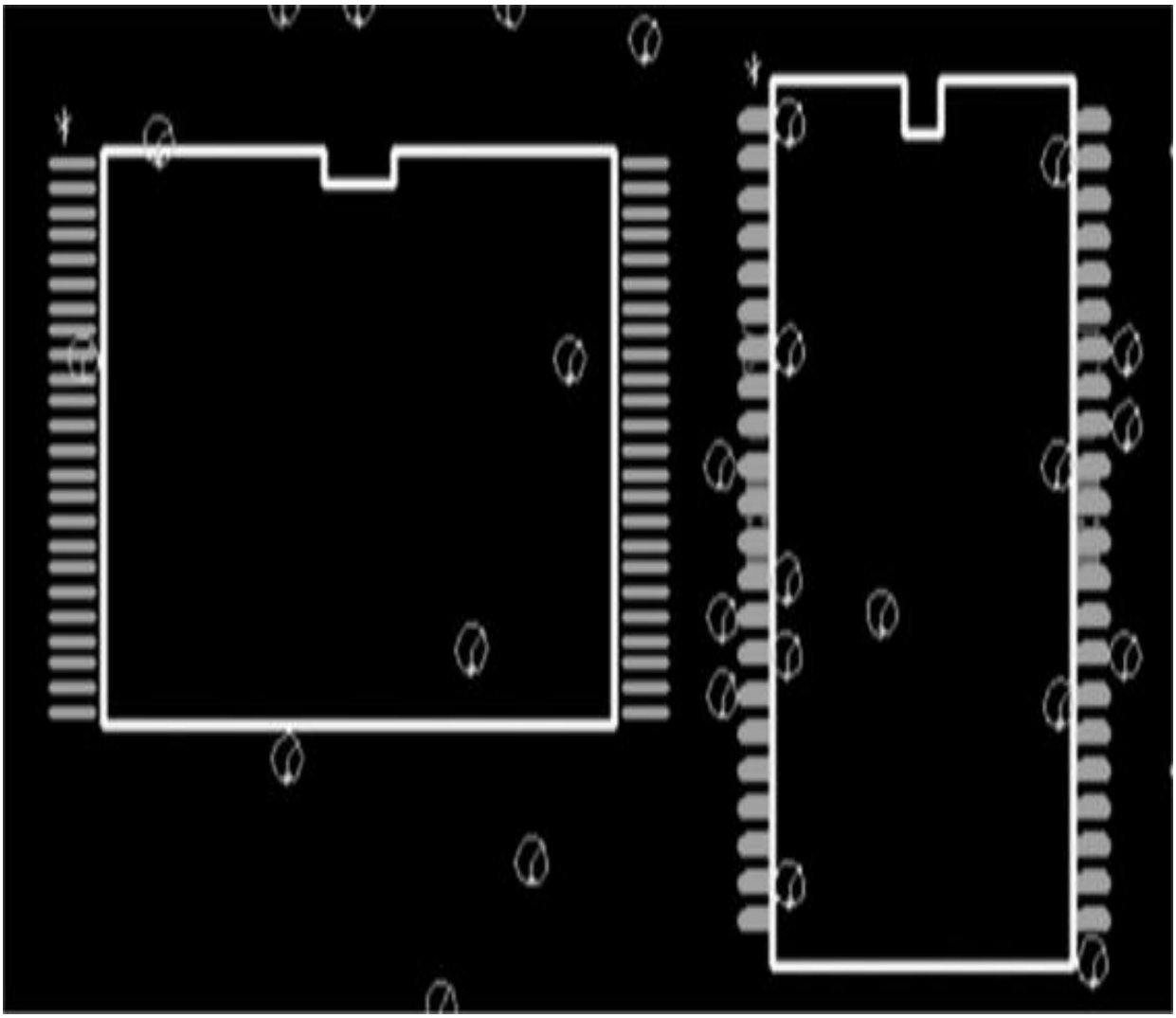


FIGURE 21.10 Will parts work together for the flow of a bus?

Now is the time to begin the setup of the new board within the software. Lots of input is required to do that, and many decisions have to be made. The schematic must be ready to make a “clean” netlist and import into the board with all the parts and library paths set up correctly. The board size and shape must fit into its enclosure, so clearances, tolerances, and keepout areas must allow for those things. The basic software information like grids, precision needed, via sizes, constraints, etc. must be set up. The designer will need to know some information about the board like mounting, air flow, testing. And they will need to know certain bits of

electronics like high current, important, noisy, differential, or high speed signals and impedances needed in order to start the process.

As mentioned, other things that may be important to a board are its orientation, mounting, and testing. The parts on the board may require that there is access to them or that there is cooling, and if there is a fan or venting, those parts must be placed for maximum cooling. It may be important to note the way the board will be mounted to its enclosure for keepout areas and grounding. Mounting holes or rails and anything that will be in a “fixed” location should be brought in and locked into place now too. A designer should know before starting a board if it will be subjected to testing such as shock and vibe, temperature, EMI, HAST, and any of many more tests, so that he or she may set up the board rules accordingly.

A brief discussion of the grid system might be useful. Usually a grid system is used for placing parts as that is the easiest way to line them up in rows and columns which is the best way to build channels for lots of signals to flow through an area. As large a grid as possible makes it is easy to align the parts.

However, some designers use a grid system for routing and vias, and some do not. If the proper constraints are input into the board database, the software will keep the signal routing the correct distance from everything else, or flag it with an error if it does not, but that will not necessarily be centered on a grid. This could allow a signal to route between two rows of pins or vias in an uncentered way which could easily become a signal integrity problem when any of those signals or pins are the higher speed signals of today’s current technology. A grid system of routing also allows any extra room in an area to fall to bigger spacing which is good for manufacturability.

At this point, the software can then be set up in the way that best accommodates this particular board. If more of the

parts are built in a metric grid system, then a metric grid should be set up on the board to use for placement and routing. The precision is the number of decimal places used or allowed after the whole number. Metric boards are often set up for 4 decimal places and boards in mils (Imperial) are already on the small grid of 0.001 in (1 mil), so the number of decimal places after that is often 2. The density of the board will help to set up the default via size that will be used in routing. If the board will be fairly wide open, the via size may be larger than if the parts and routing will cause space to be very tight. It is a good idea to talk to the manufacturer about their “normal” size via and pad and the smallest via hole that they allow without an up-charge. Before any placement or routing occurs, the most basic constraints will be entered. These might include the default trace width and spacing, any signals with critical length or spacing, and differential signals.

It is also important to decide the board thickness at the start of the process in order to design the board’s stackup. While manufacturers can make up numerous board thicknesses, there are some that are used a lot more often than others. The most common by far is 0.062 in thick. The intended number of routing and plane layers should be decided, and the copper thicknesses planned based on current need. The stackup will help determine how the signals will travel through the board and also help determine impedance control and return current because those are partially set up by the distance between the trace and its closest plane. Now is also the time to determine if any special board material will be needed for lead free, high speed signaling, heat dissipation, or any other reason.

At this point, bringing a netlist into the board will bring all the parts and their connections into the database. Most softwares have a quick way of placing all those parts in a more or less random arrangement outside the board outline

(see Fig. 21.11). There, they are available for the designer to begin his or her placement.

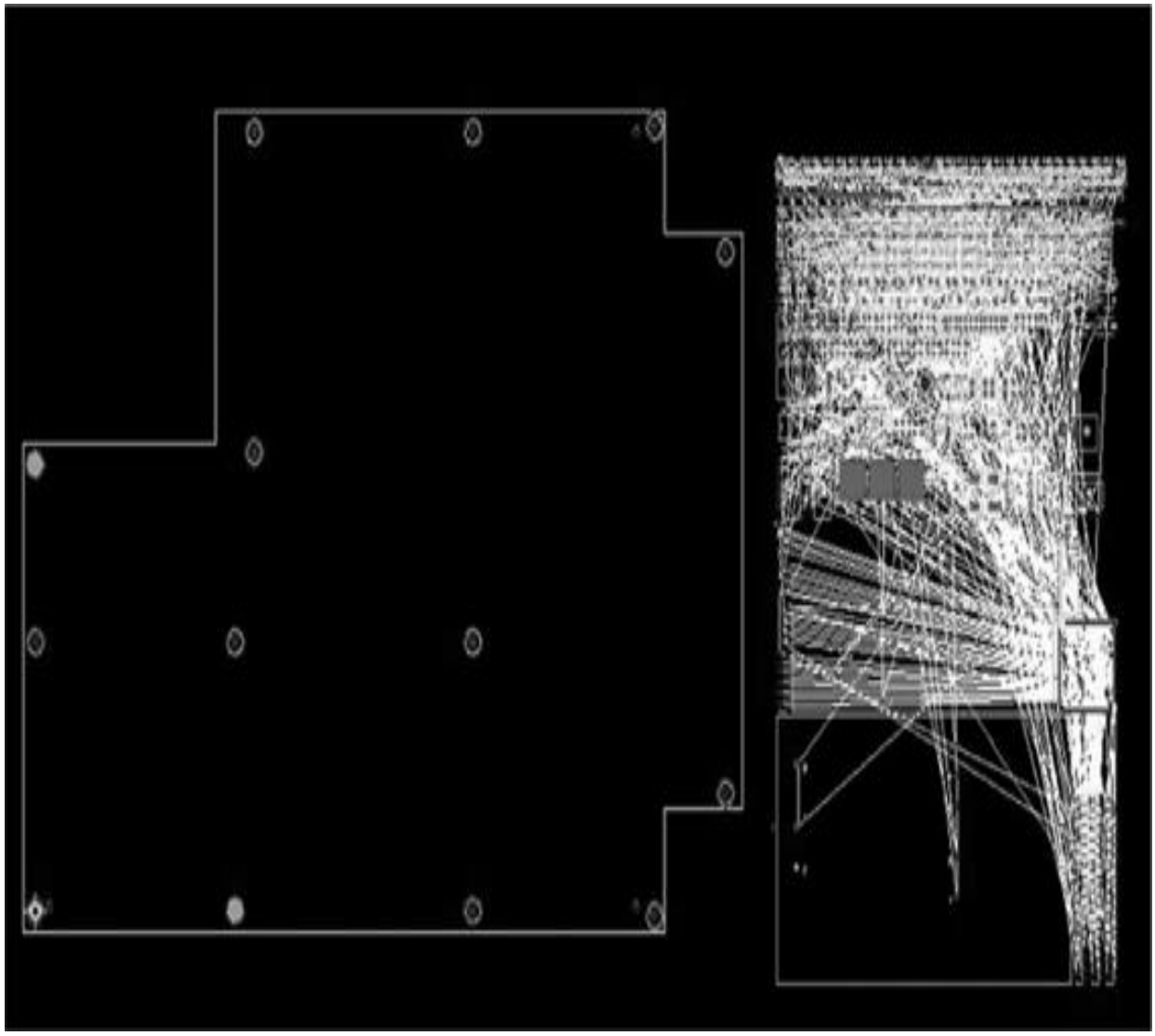


FIGURE 21.11 Netlist brings parts into random locations outside the board outline.

There are many ways to organize all the information given to us from the schematic into something understandable and manageable prior to placement on the board. Sometimes, groupings are done at the schematic level that will carry over into the board. Some people like to organize the parts as they are placed into the board. Others prefer to organize the

parts into “blocks” or regions outside the board outline to see what goes together and how it fits with other groupings of parts (see Fig. 21.12). The added benefit of this grouping step is that the designer gets familiar with the schematic, parts, and circuit, and how they all fit together in the bigger picture. The methodology used for this organizational step really only needs to make sense to the designer as long as things get grouped as they need to be electrically on the board.

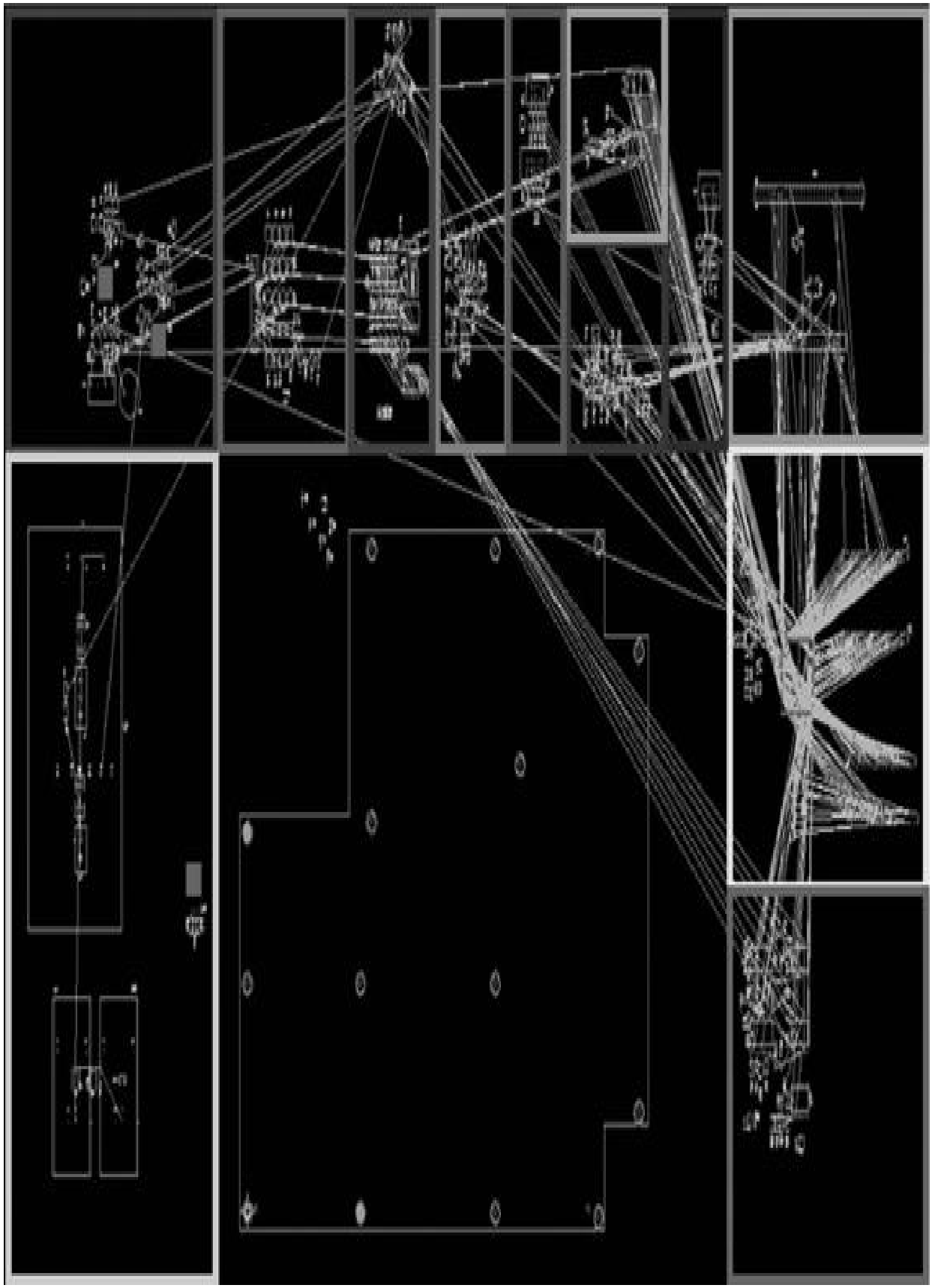


FIGURE 21.12 Group parts outside board outline.

21.7 PLACEMENT

It is helpful at this point to study the total space allotment on the board. Just as a block diagram helped to simplify and understand the schematic, making a block diagram for the PCB can be helpful. One can choose the size and shape of the sections on the board that will be used for each section of analog, digital, high speed, I/O, filtering and ESD, power supplies, etc. (see Fig. 21.13). A little planning on how these parts and sections will interconnect can easily be used for placing parts and later when routing them. The groups of parts can then be moved around as needed and collapsed closer and closer until they fit within the designated area and the board outline.

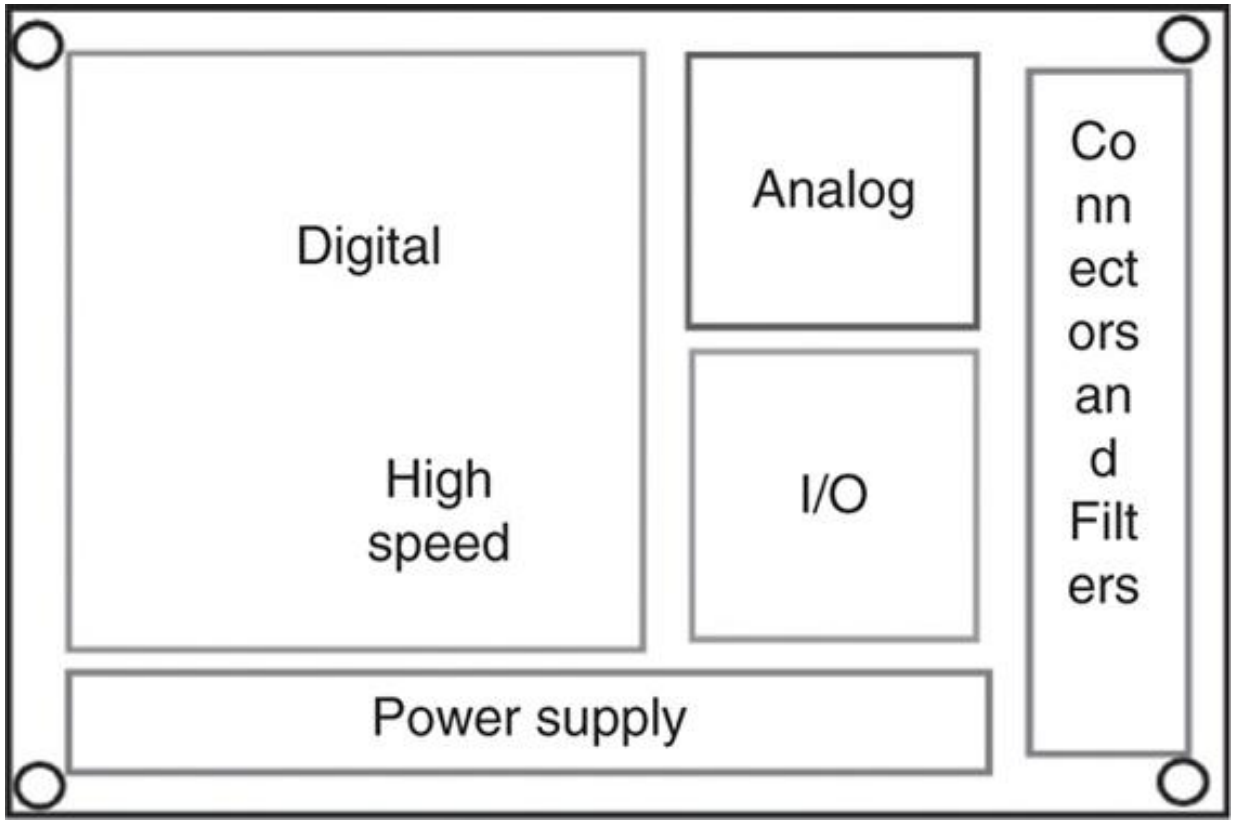


FIGURE 21.13 PCB block diagram.

When placing parts inside the board outline, understand that there is no ONE right way to place parts on a board that always works best. One of the first issues to decide is whether the parts will be placed on one side of the board or both sides. It is helpful to manufacturing if parts are only placed on one side of the board, but it may be helpful for the electronics if they are placed on both sides. For example, capacitors and termination resistors can get very close to ICs when placed on the opposite side, and connectors may have their cables turn and orient themselves correctly just by placing them on the back side of the board. If some of the major parts were built on metric grid and some on an imperial grid, then one grid or the other should be chosen for all the interconnecting signal routing between them. The grid with the most complex parts (like BGAs) may work very well for the fanout and routing of all those parts.

There are benefits to following electronic rules for placement, so parts should always be placed for best signal integrity and load distribution. That means that the placement should probably follow the schematic placement (if grouped there) as much as possible because the circuit designer generally places parts in functional groups on a page or pages in the schematic. If the circuit designer does not do that, knowledge of good signal integrity practices is a must for the board designer. Additionally, if the parts are grouped by logic family and voltage, one power plane layer can easily be subdivided for all the voltages needed on the board. That is helpful for keeping signals routed to return against that power plane within one enclosed area where they don’t cross splits in planes. The next priority would be to minimize trace length where possible because the signals should not have to travel farther than necessary because they can pick up or deliver noise to/from other signals. Lastly

the parts might be placed for the best fit and flow on the board.

Some people like to find and place all the parts that are in fixed location and then work from the outside edge in toward the center to place the parts, but it is almost never a good idea to place parts solely by using the netlist because that gives no priority to important parts and nets over less important ones.

There are a few tricks that will help the designer have a better picture of what is going on as he is placing and routing the board. These include BGA placement, color coding, alignment, “rough in” routing, and grouping parts.

BGAs are generally placed on a grid that is ½ their ball grid. In other words, when a 0.8-mm pitch BGA is placed on a 0.4-mm grid, it is quite easy to fan out the signals to a via and have that via be a uniform distance from all other pads and vias within the part boundaries. The routing for the signals will then be placed on a 0.2-mm grid which will also space them uniformly between the BGA pads and vias. That is very good for the integrity of those signals and all the ones around it, as we never want signals too close to other vulnerable signals or pads that might accept some energy from a noisy trace.

Color coding has the designer assigning a different color to each major bus or net so that it is easy to identify where each one begins and ends, and any parts that are connected together. If those colors are matched to colors applied to the schematic or block diagram, the designer’s eye can quickly move back and forth from one to the other without searching. It also makes it very easy to see where different nets are on major components like BGAs so that they can be placed to optimize routing. See Fig. 21.14.

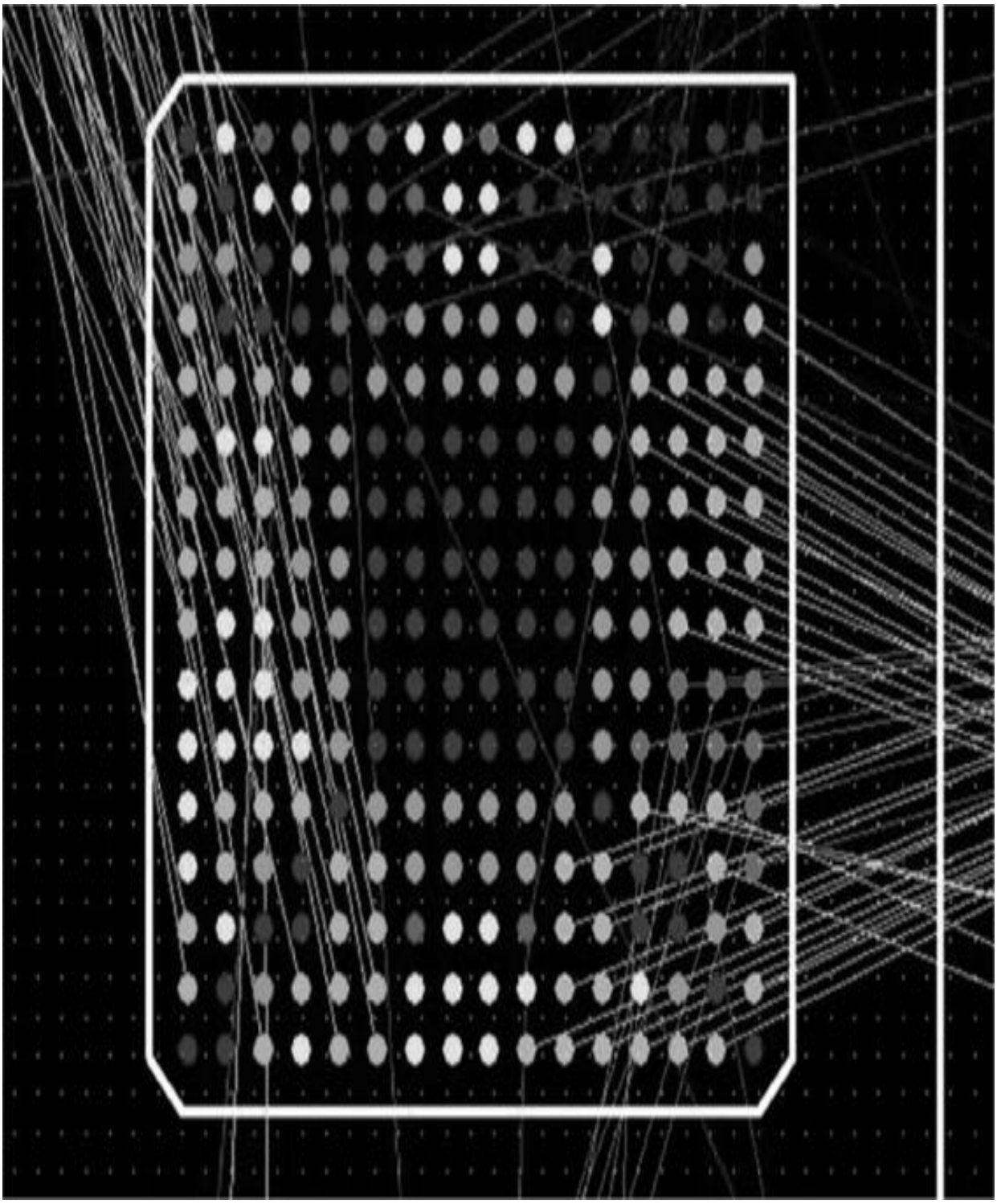


FIGURE 21.14 Color coding of nets.

When placing parts, alignment is very helpful for routing too. See Fig. 21.15. If the edges of the parts are in rows and

columns, it’s easy to get entire busses to flow nearby using the space available. The fanout vias can also be lined up in rows and columns to allow for routing between one part and another.

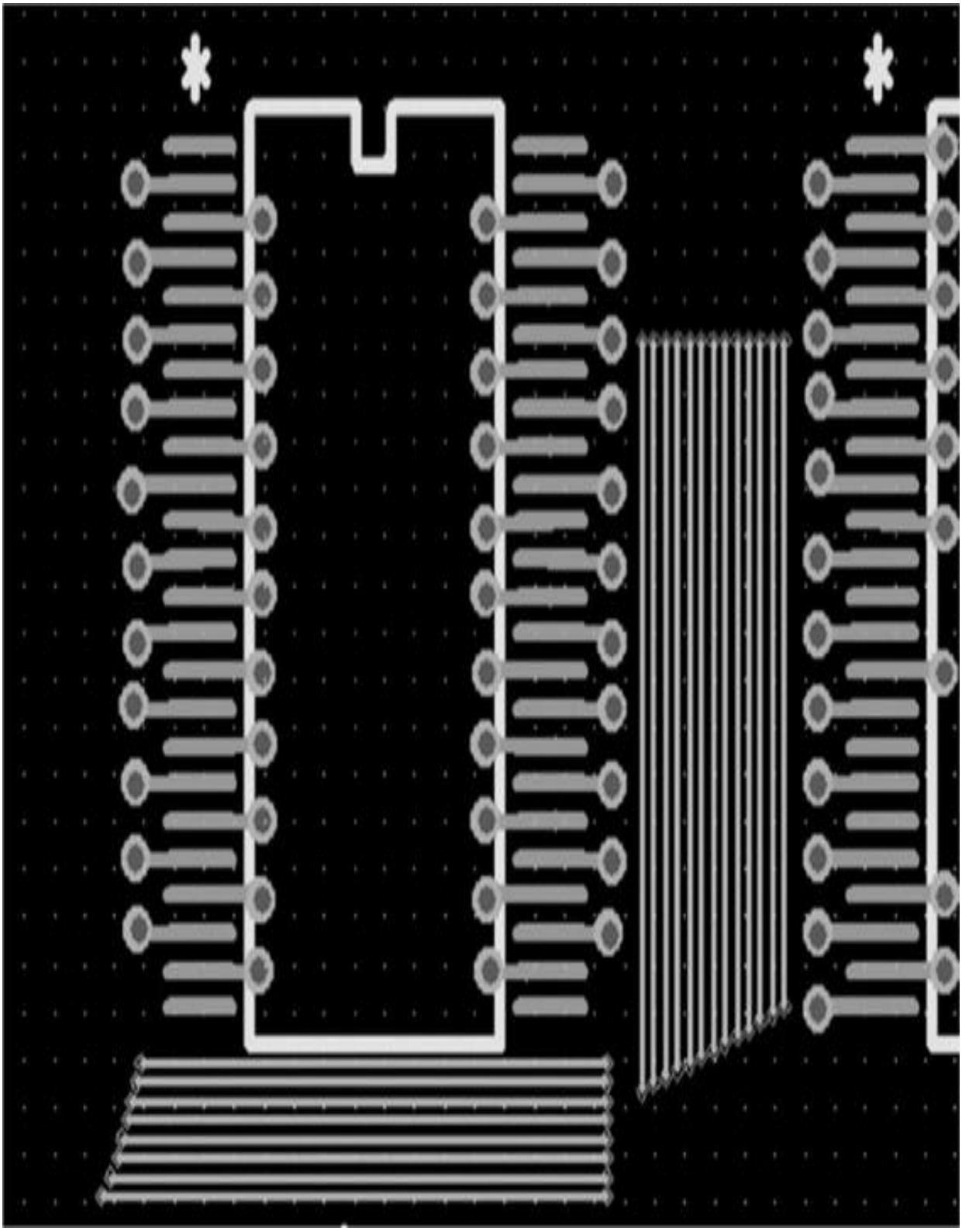


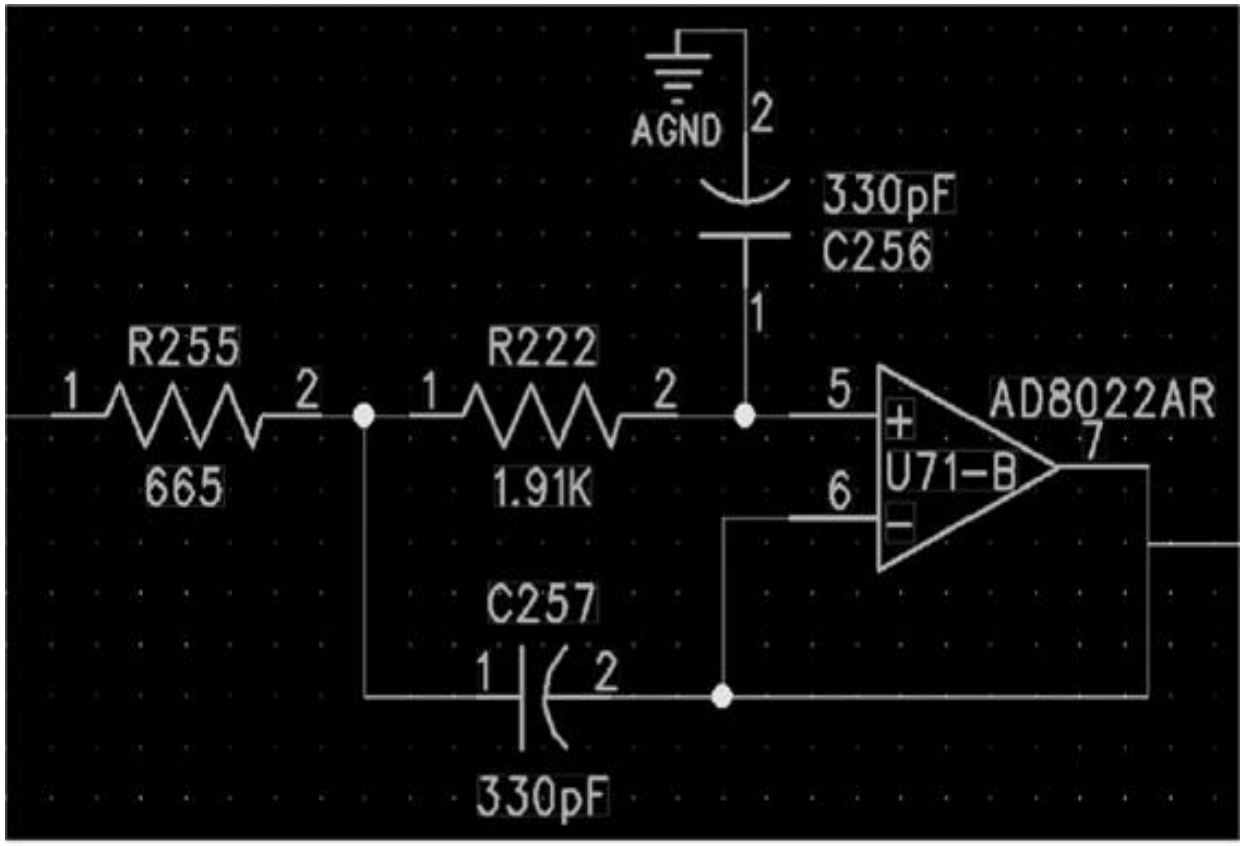
FIGURE 21.15 Alignment of parts and vias.

Figure 21.15 also shows an example of “rough in” routing. When there are a number of signals to go between parts or rows of vias, those parts or vias can be placed with “placeholder” signals routed between them with the proper spacing to see exactly how much room is needed between those placed parts before they are put onto the board. That is especially helpful when a board will be dense with components. And it is good for an area that has clocks or differential signals passing through it as they both will need extra spacing around them because of interference possibilities. The parts can then be moved closer or farther away as needed to accommodate the spacing needed. Another example of this process would be to bring a number of signals through (or out of) a small area or connector, to see exactly how much room the group of signals will take.

Orientation of the parts in a N-S or E-W direction is not very important because the pick and placement machines will be able to place them automatically no matter what. While it used to be an issue of concern on a board, it no longer carries any real weight in the placement of the design.

A few words must be said about analog component placement which can be much more critical than digital. Analog signals are very sensitive and can easily be corrupted, so their parts and signals should be kept in their own region of the board, away from digital parts and signals. They should be placed very close to one another with the connections as short as possible so there is no chance of them picking up noise. It is a good idea to start at the input device to a group of analog parts and place the parts working toward the output device. That way, the input and output devices are not close to one another. Many people use what is called the “clothesline” method to place analog parts. In that scenario, the signals that go through the parts “are” the clothesline, and all others parts and signals hang

off the clothesline. See Fig. 21.16. *No* digital parts or signals should be placed in or go through an analog region.


AGND
2
330pF
C256
1
R255
R222
1
2
1
2
5
AD8022AR
+
U71-B
7
665
1.91K
6
−
C257
1
2
330pF

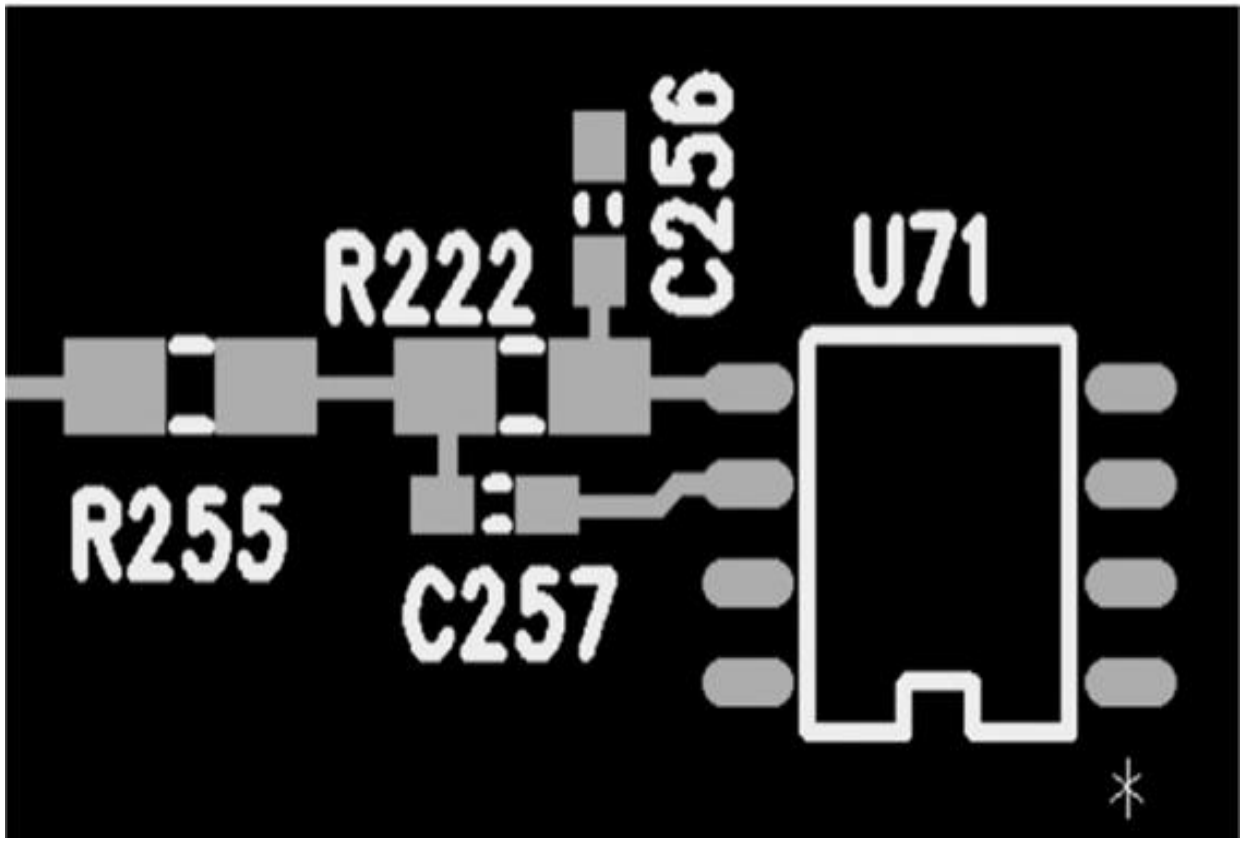

C256
R222
U71
R255
C257

FIGURE 21.16 Use the clothesline method for analog parts.

As the designer is placing parts, he must be thinking about how he is going to route those parts. We don't want signals flowing through areas that have nothing to do with those signals as that may cause interference. Routing needs can also affect the location of parts, the grouping and orientation of parts, and how the connections are made between parts. One of the ways people keep track of their routing plans is with a routing map. Basically, that is a picture of the board with the parts placed, and lines drawn in a different color for each the routing layers to indicate the intended routing. Every route line is not needed so a single line can indicate the intended flow for a whole bus.

Once a designer has taken the time to place parts close together, making his own grouping of them helps to keep them together. This ensures that if one item gets moved, all parts in the group move with it. That way, an IC doesn't get moved across the board with its decoupling caps or termination devices left behind accidently.

Placement should not be considered a rigid or inflexible thing. It should always be somewhat flexible so that when routing requires that one or more parts have to move, they can. The integrity of the placement and routing is by far the most important issue.

21.8 PLANES

It is very beneficial to plan the planes very early in the design process. This will help the designer know how many layers are needed in addition to the routing layers and in what order they should be placed in the stackup. Every signal is a closed loop and the energy that is a signal must return back to its source. So, each power plane and every routing layer must have a return plane (normally ground)

placed right next to it in the stack so the signal energy has a place to return that will not interfere with anything else. The designer must pay as much attention to where the return path will be as he does to where the signal routing is since it is not actually drawn as a trace as a routed trace is.

The signals will return on the closest layer to their routing in the stackup as this is the path of least impedance. This is called transmission line routing. The digital signal and its return will flow very close together between the routing and return layers and should not be separated in any manner. If either one crosses a split in a plane they will be separated, and signal integrity problems very likely will result. Since the ground planes are not split, these layers give a good clean return path to the signals on the adjacent layers. That is not to say that signals cannot return on the power layer, they can. However, if the power layer is used for return, the signal must be the same voltage as the area it is traveling through AND it must not cross the splits in the planes. These plane layers should be of a solid copper plane as opposed to a cross hatch pattern.

Since the parts should have been grouped as much as possible by their power needs, a separating line can be drawn between the different power areas creating multiple shapes on one single power layer that is split for as many powers as needed. See Fig. 21.17. In general, the ground layers should not be split. If digital and analog parts are segregated into their own areas, and their signals stay routed within those areas, their return current will stay in those areas too.

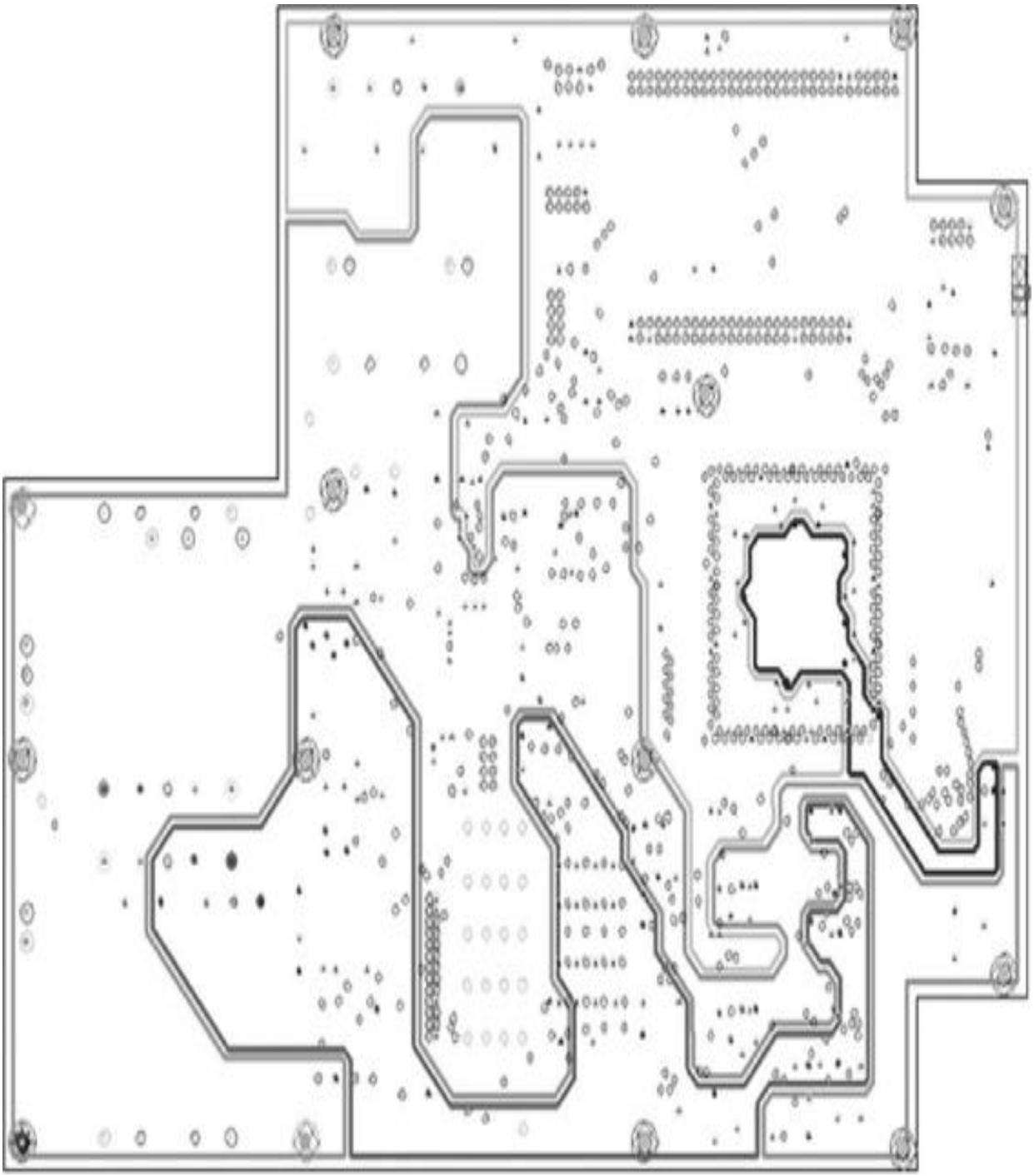


FIGURE 21.17 A power plane with separation drawn for different voltages.

21.9 STACKUP

The materials that constitute most PCB boards are thin sheets of copper and dielectric material. The dielectric can be either core material which is fully cured dielectric material and usually has copper adhering to one or both sides, or prepreg material which is only semi-cured dielectric material and is used as a filler between core layers and often as an outer layer. Because it is semi-cured, the prepreg material will melt when the layers are pressed together and so it will act as a glue.

Fabricators prefer to build stacks in a “foil construction” with the thin layer of copper foil and prepreg material as the outer layers and core layers alternating with prepreg layers internally. That is less expensive for them because there are fewer core layers of material to buy and there are fewer etching steps in the processing. Core material can be used as outer layers if needed, but there are time and cost issues involved. Figure 21.18*a* shows a routing layer as an outer layer in foil construction while 21.18*b* shows a routing layer as an outer layer on core construction.

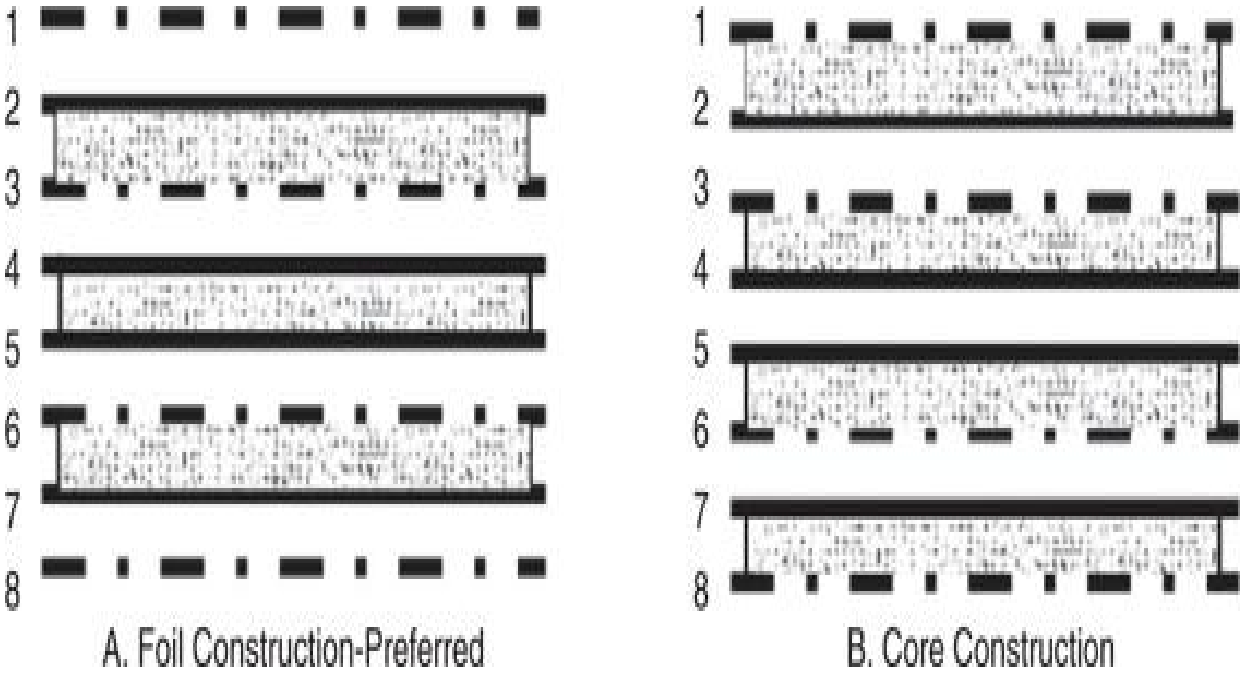


FIGURE 21.18 Foil construction versus core construction.

PCB Boards should always have an even number of layers in their stack with the same type of layer (routing or plane) above the center line as below the center line. This makes a balanced construction for the fabricator that will help to keep the boards from warping. Another thing that helps to balance the board is adding poured planes into any open areas on any layer. That will help keep over etching to a minimum in areas that have few traces or pads on a given layer. Tying those poured planes to power or ground has the added benefit of creating extra built-in capacitance for the ICs to use and keeps an unconnected plane from picking up noise from some other signal in the area.

Setting a PCB stackup can be a complex procedure, but there are a few more general “rules” that are helpful.

It is almost always a good idea to have a power and ground plane right next to each other in the center of the stack, so that is a good place to start. This sets up useful capacitance to help the power distribution system work properly. These two planes should have a minimum spacing between them of 0.003 to 0.010 in to provide the maximum capacitance. The exception to this rule is that it cannot be done this way in four-layer designs.

The placement of routing layers is also important. Two signal routing layers are allowed next to each other in the stack as long as they have return planes on either side of them. That way, the return planes will be the lower impedance path and will keep the signal from trying to return on the other signal layer. There should never be more two signal layers next to each other in the stack though. And there should not ever be more than one signal layers as the outer layer on the board. If there are two routing layers as the outer layers, there is no place for the signals on the outermost layer to return and it is very difficult to control impedance. See Fig. 21.19.

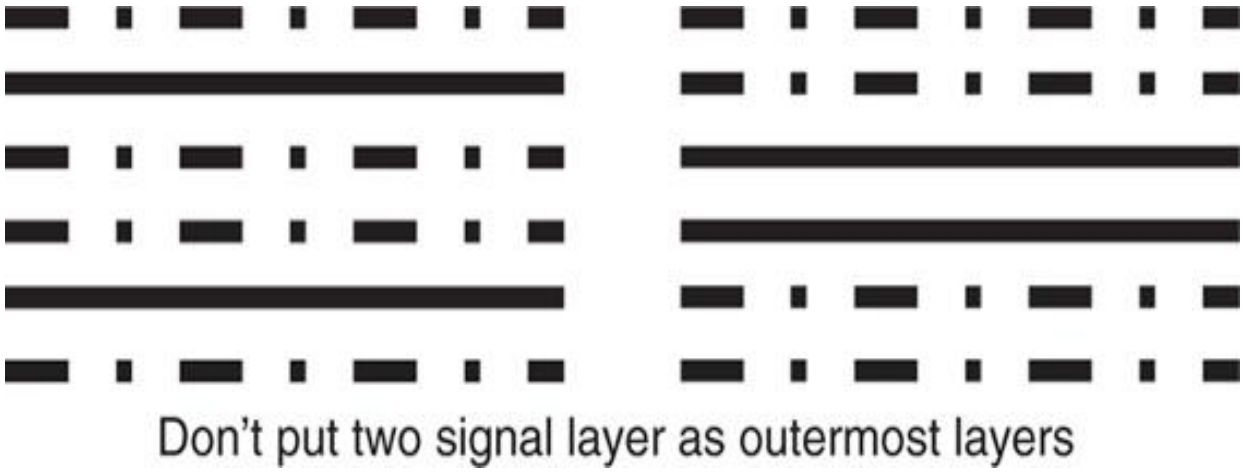


FIGURE 21.19 Routing and plane configurations.

It is important to understand that impedance control is partially set up by the copper thickness and the distance between the trace and the nearest plane. So, any boards that have controlled impedance traces or differential pairs should have their stackup coordinated with a fabricator who can help with traces, spacing, and distances between layers. In fact, it’s always a good idea to have a fabricator check out a proposed stackup to make sure it will accomplish what is needed.

21.10 ROUTING

As mentioned earlier, there are many IPC standards that are available to help with designing, fabricating, and manufacturing PCB boards. The entire IPC-222x series is about design and there are many pictures and charts to reference there. One chart in IPC-2221 in particular is the “PWB Design/Performance Tradeoff Checklist Considerations.” This chart lists a feature (like dielectric thickness to ground, for example), tells a parameter that is affected by it (in this case, crosstalk) and if that parameter increases or decreases if the feature is increased. This is a

particularly helpful chart for people who are not used to the way PCB items affect each other.

One of the first things to think about after placement is entering constraints. Even simple boards will need constraints to determine the default trace widths and spacing. Complex boards will need many more items controlled. Classes can be set up in the constraint manager to group any nets that will need the same constraints like trace width, spacing, layer control, sequencing, length matching, etc. Any net that needs to be controlled for any reason should be given a name because that will protect them from future edits accidently destroying their constraints. Designers will want to add in enough constraints to do what is needed, but no more than necessary. It may be helpful to have a discussion of the rules to be set up with the circuit designer to be sure everyone's needs will be met.

Pin and gate swapping must also be considered before routing can begin. Many components have gates inside them whose connections can be swapped to provide a better flow for signal integrity and routing.

These components range from simple groups of "like" gates like the 74LS00 and the 74LS04 shown in Fig. 21.20, or very complex programmable devices. Either way the pins in the gate and the gate in the device must be identical in function in order to be swappable. In the gate is like the 74LS00, the input pins [example 1 and 2 (1A and 1B)] can be swapped with each other, or one whole gate of three (1A, 1B, and 1Y) can be swapped with another gate within the device. Programmable gates are only internally accessible and must be programmed into the part in the pin order that is needed and available. Color coding is very useful for the board designer when organizing how to swap the gates.

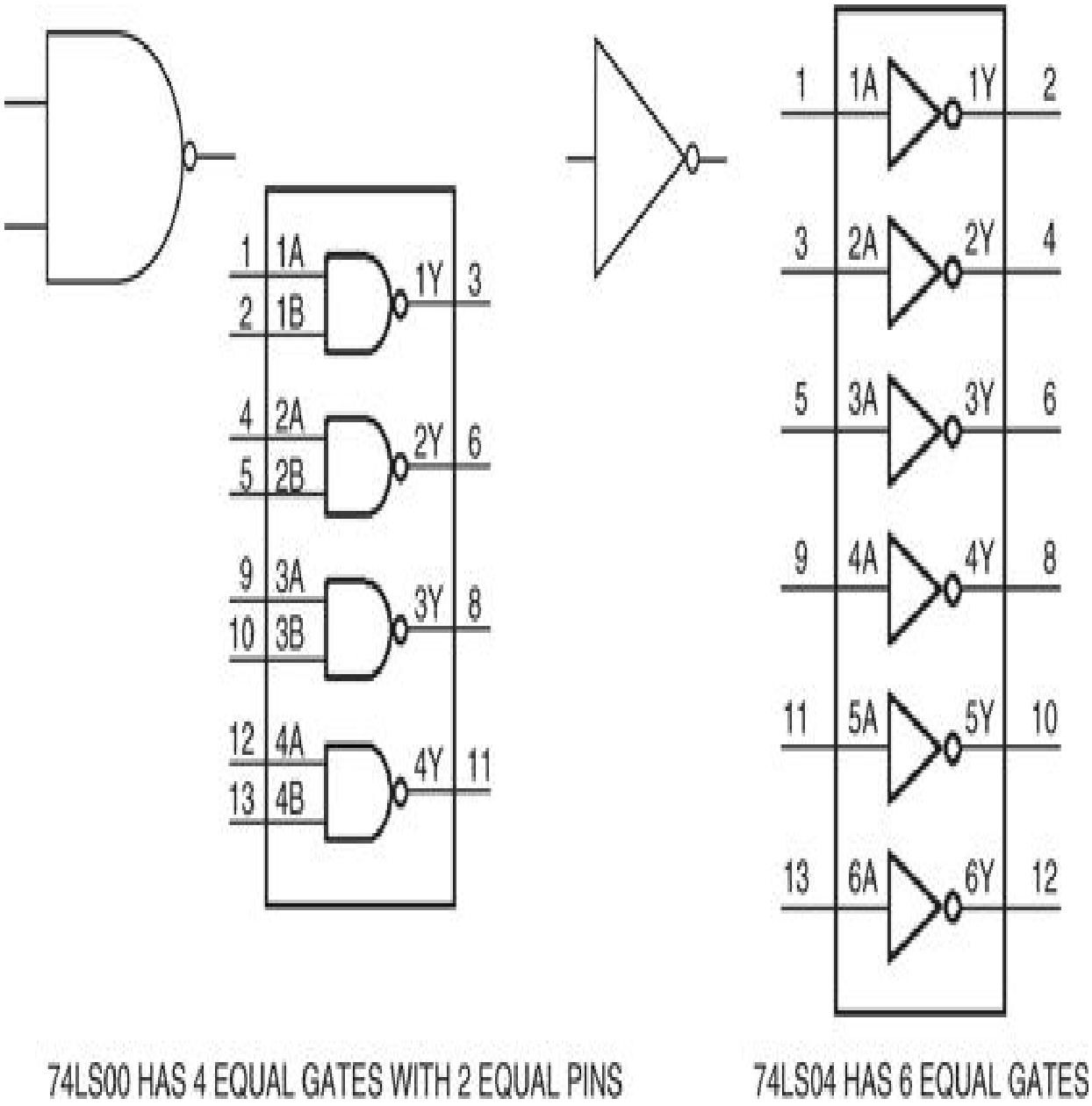


FIGURE 21.20 Simple parts with gates.

Now is the time to plan what widths the traces will be. Some things that help determine trace width are desired impedance, stackup, current carrying capacity, temperature rise allowed on the traces, and the ability of the fabricator. Even if a particular impedance is not needed for the signals, it is still a good idea to control the trace impedance layer to layer. That way when a signal changes from one layer to

another there is not an impedance mismatch, which can cause a reflection. For normal routing, pick an impedance number near 50 to 60 Ω (ohms) and stick to it on each layer of the board. That might prove to mean different trace widths are needed on internal layers in order to achieve the same impedance, but that is generally pretty easy to set up to do automatically within the software. The trace width and spacing are generally equal values. If there is any extra room available, it should go to spacing rather than trace width to make the fabrication easier. It is always important to keep those trace widths within the abilities of the fabricator for the project, and not to use smaller trace widths than necessary. It may also help to look at the distance between the leads on the parts and try to set the chosen trace width to something that can go between the leads or balls of the ICs or BGAs.

Often when surface-mounted components are placed on a board their signals cannot route away from the pads on that same layer. Those signals will need to be fanned out to a via that will take them to connections and routing on another layer of the board. At a minimum, the power traces should be fanned out early so that their vias secure their place before any other routing starts and fills up the space. The fanout vias on BGAs and some other complex parts might also be placed early because it’s easier to take them off if they are not used rather than try to add them later when the area is filled. BGAs are often fanned out into either an X or a + pattern so that the power and ground planes can get into the center of the part and provide good power integrity. See Fig. 21.21.

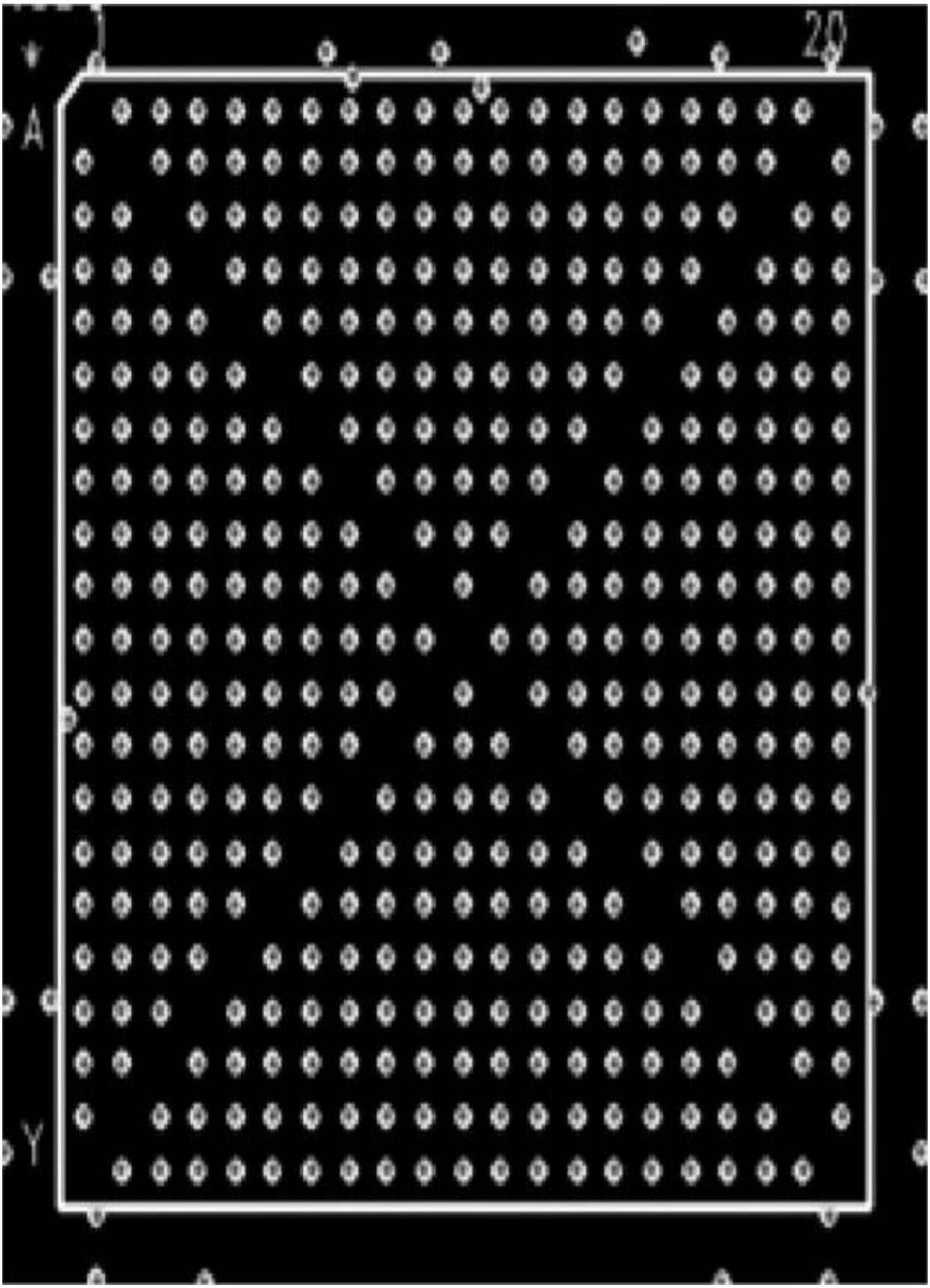

1
20
A
Y

FIGURE 21.21 A BGA that is fanned out into an X pattern (only the vias are visible).

The signal vias can also be placed in an “as routed” manner or set up in a fan out grid pattern such as the one in Fig. 21.22 where the vias are lined up in rows and columns. If the board will be fairly dense with lots of parts and routing, the gridded pattern is probably the best option. Routing and return would then go around or between those gridded vias in a north-south or an east-west pattern, as needed. Again only one grid, either Imperial or metric, should be used for fan out patterns so that the vias and routing will line up correctly.

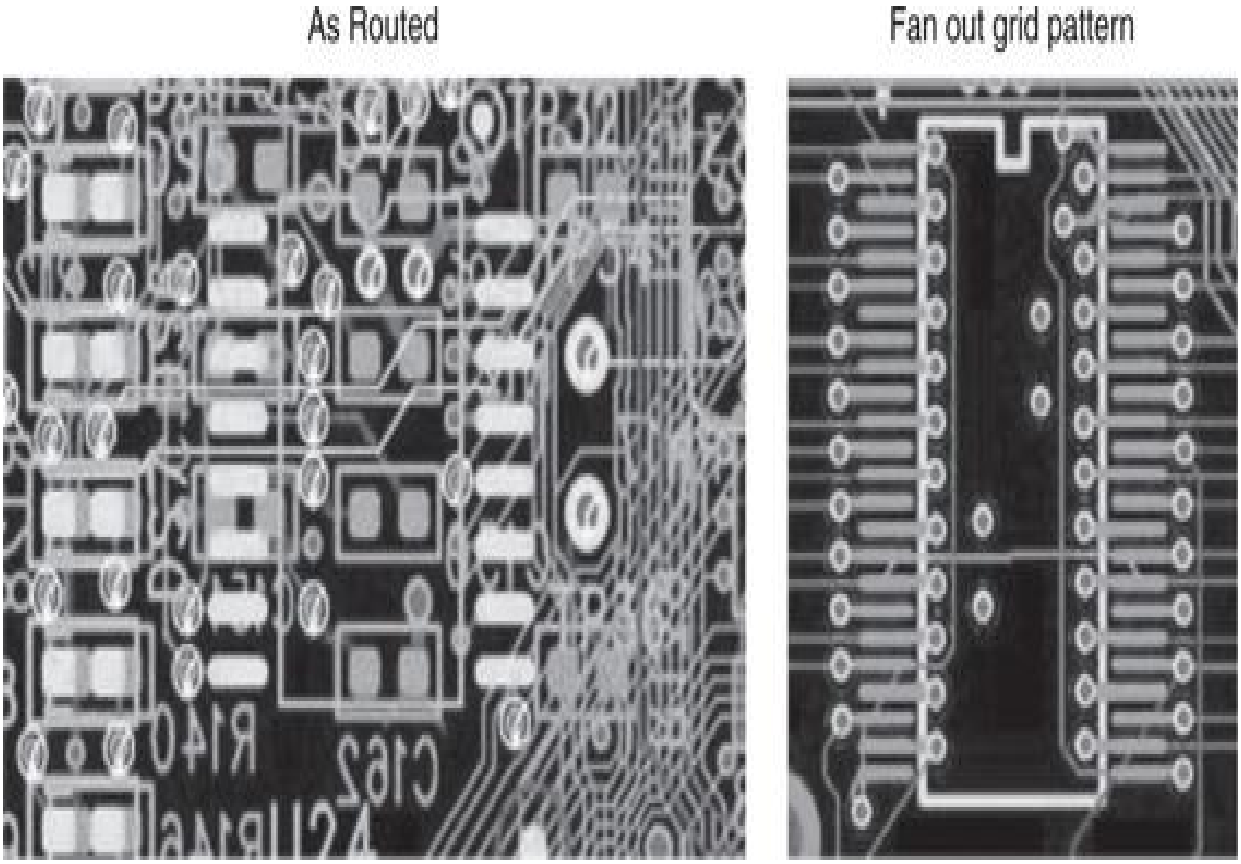


FIGURE 21.22 An “as routed” pattern and a simple fan out grid pattern.

The fan out grids can get much more complex and set up many routing channels as shown in Fig. 21.23 or with a

dominant flow in one direction over the other as shown in Fig. 21.24.

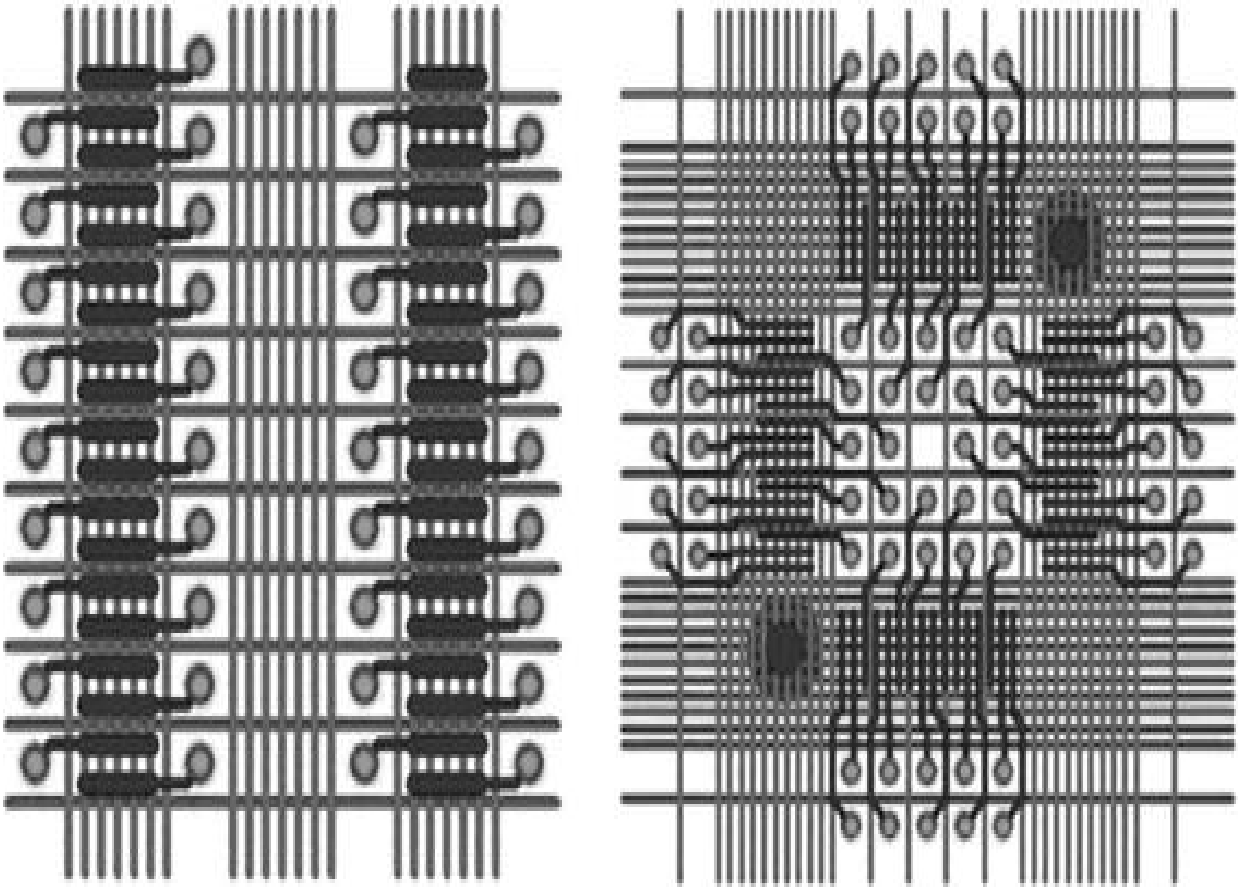


FIGURE 21.23 Via grid setup for routing channels.

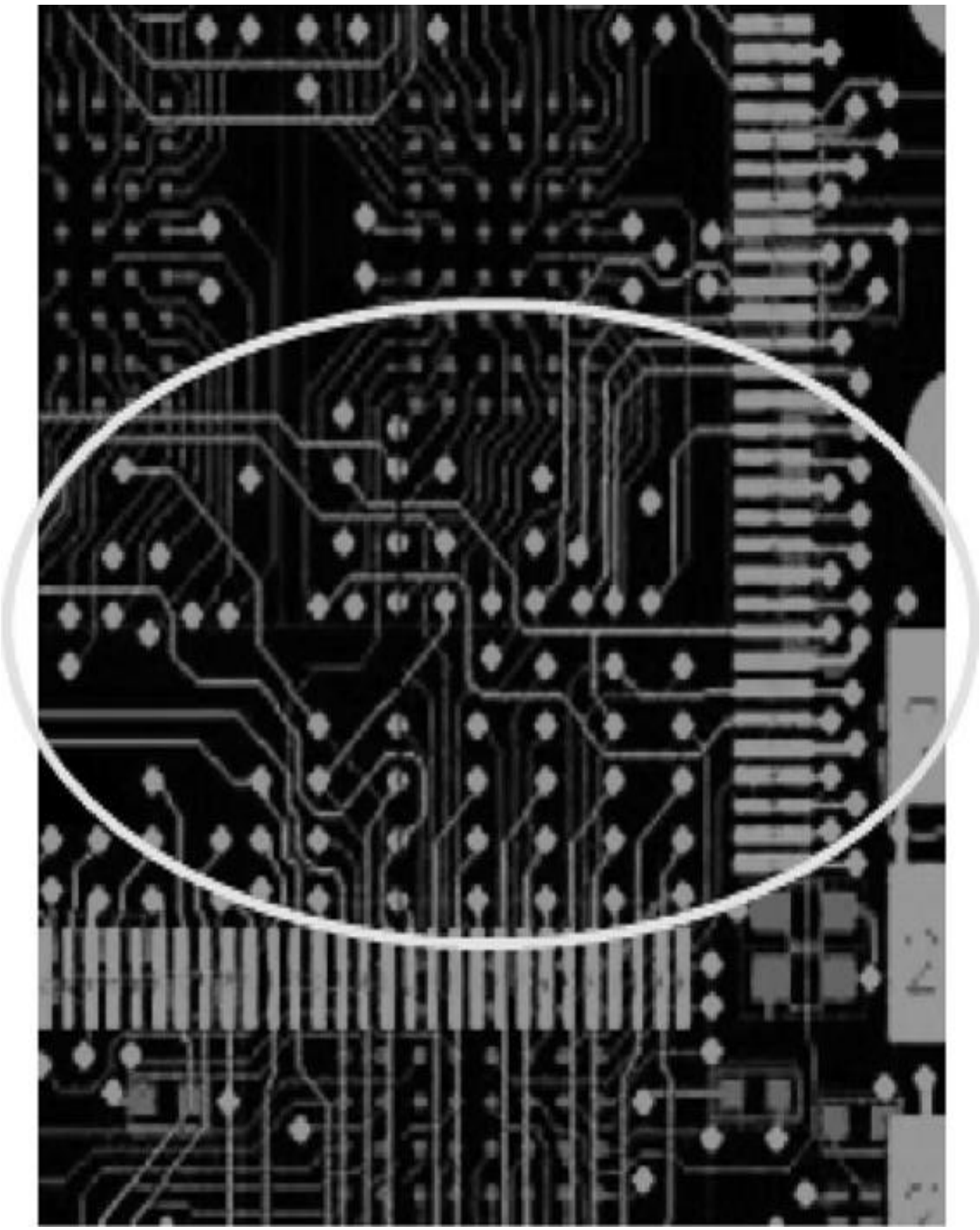


FIGURE 21.24 Via grid setup for north-south dominant routing.

One way to start the routing process is to go to the densest area of the board and work there first. That area will help determine layer count because it will need the most routing. The BGA escape pattern is an example of this because there are a limited number of channels to route out of a BGA on any given layer. This area will also help to show if the placement will need to be tweaked a little here or there to accommodate the density of routing there. It is also a good idea to plan to minimize routing on outer layers where possible because it is best for signal integrity to route all important signals internally. Slower signals can probably route on outer layers.

To begin the process, establish the routing direction for each layer in those dense areas. Any time signal layers are next to each other, the routing should be in perpendicular directions so that they can't interfere with each other. Look at the rats on the parts in those dense areas to see if they lead to an obvious routing direction. If not, check the size and shape of the board to see which layers might more likely lend themselves to more routing out and away from that dense area. Above all, remember to route according to the routing map established earlier.

Check into which signals are considered important or critical. These usually include clocks, strobes, high-speed signals, noisy signals, and any major busses. It is important to understand what is important about these signals and how to control them. Read and understand the data sheet and reference information and discuss it all with the circuit designer.

As mentioned, it is important to think about how the parts will be routed as they are being placed. There are several routing schemes that are commonly used. See Fig. 21.25. Busses are generally routed in a daisy chain pattern from driver to load(s). Clocks generally route in a star or 'branch by n' pattern. T-routing is used for a group of loads that are lumped together. Termination and decoupling devices will

probably need careful placement and routing to ensure that they work as needed.

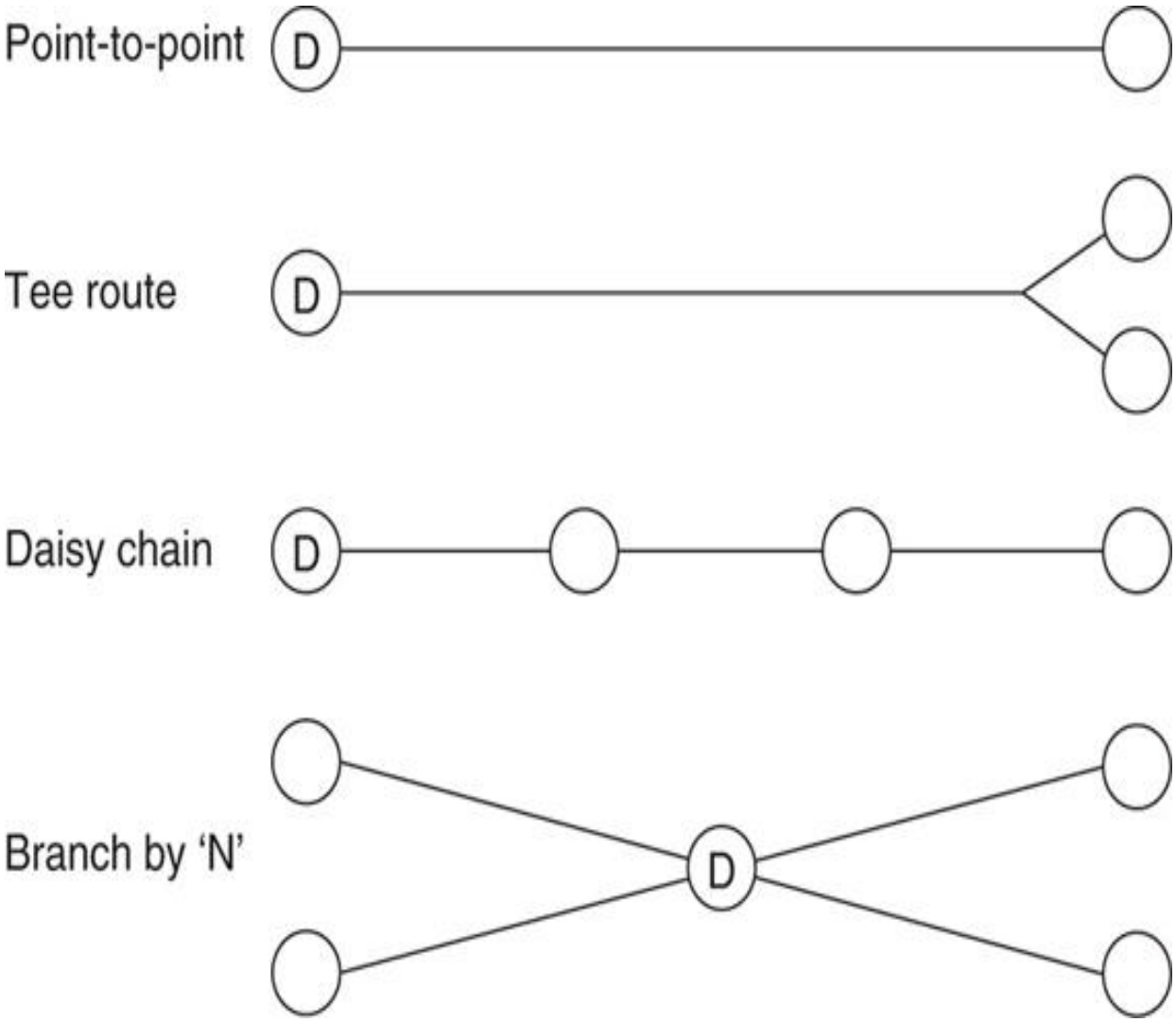


FIGURE 21.25 Most common routing schemes.

There are many ways to accomplish routing. One approach that may work well is to route in the order listed below:

1. Route power connections in a fanout to vias
2. Route I/O connections
3. Route critical nets
4. Protect or "lock" criticals until/unless changes are necessary

5. Analog signals (and parts) next, and isolate from digital
6. Any location specific signals
7. General routing

If there are like signals (like a bus) that need to flow from one region of the board to another, they can be grouped together into routing channels. Since they are probably all switching at the same time, the spacing between them can be the same as the trace width without much concern for crosstalk. See Fig. 21.26. However, if signals are put into channels that are different from each other, there can be crosstalk from one signal to another if there is minimum spacing.

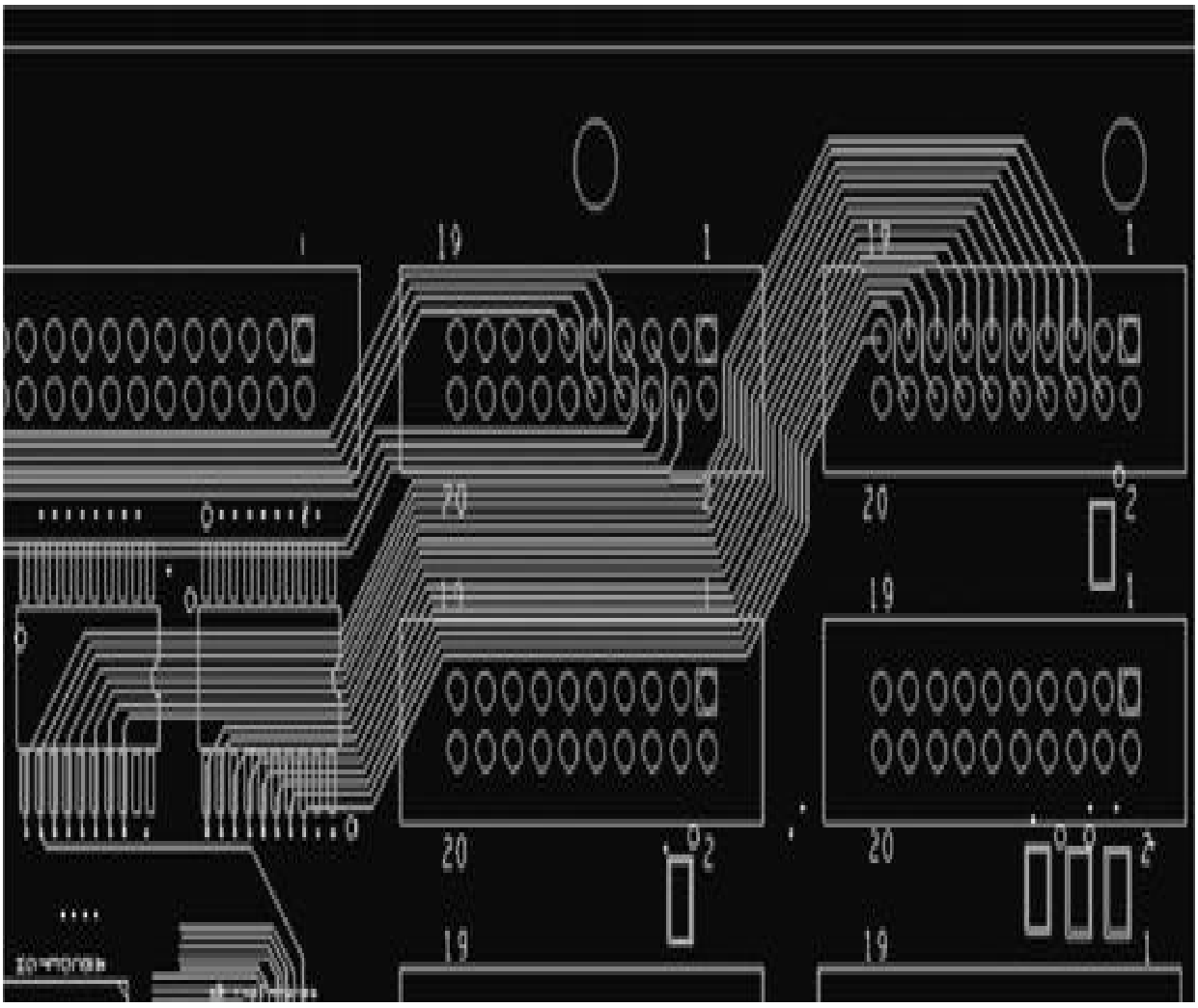


FIGURE 21.26 Routing channels.

Additionally, room must be left during routing for any vias, turnaround room, and changes of direction that are necessary. And one must plan for the return current for each and every signal. One way to do that is to turn on only the routing layer being used and its return plane. Look for any splits or roadblocks to the return current and fix them or reroute the signal.

Here are a few general tips that may help with routing:

- One should be able to discern a noticeable routing direction on any given layer, meaning that most of the signals on that layer would route in the same general direction (E-W or N-S).
- Trace entry into pads should not leave an acute angle which may cause fabrication issues.
- Trace width should be no more than approximately 60 percent of the pad size it is entering for heating reasons during assembly.
- Keep all routing within its own power or ground region for return purposes.
- Do not route traces across splits in planes as that cuts off signal return possibilities.
- Do not route any traces on the power or ground layers. They could cut off return current in that region of that layer.
- Via the caps and ICs to the planes if they are more than 0.100″ apart for best power connection.
- Keep input and output signals separated so they cannot interfere with each other.
- Don’t route high speed traces near the edges of the board for best EMI control.
- The use of slightly larger vias for power connections may be helpful to move current from layer to layer, when

needed.

- Look for ways to route signals on one layer, without any vias. That keeps other layers clear of via holes and so is good for routing on that layer.
- Keep extra spacing between noisy signals like clocks or strobes and any other routing to minimize interference from the clock to other signals.
- Keep extra spacing between differential pairs and any other routing or vias to minimize any routing interference on the pair.
- Copy and paste repeating circuits or routing where possible to reduce time needs.
- When adding serpentine routing to match lengths, be sure there is three to four times the trace width between loops to keep the signal from jumping across segments and ignoring the loops.
- Don’t route signals through a BGA that have nothing to do with that BGA. They may cause or collect interference.
- Spread out routing whenever possible to minimize crosstalk.
- Change routing layers only when necessary … but change layers when necessary.

Some people choose to work with an autorouter. There are some pros and cons to doing that. In general, an autorouter is much faster than a designer at making connections. An autorouter might be fairly accurate at suggesting how many layers a board may need or if the placement set up by the designer will work effectively. They are very good at fanning out signals from complex devices. However, they often fail to complete their task on high density, low layer count boards. This is because autorouters work by taking a signal along a certain path and when there is a road block, changing layers. If there are not many layers to change to, the router will have problems. There is also a fair amount of time needed to

set up the rules for an autorouter, and to do the cleanup after routing.

On the other hand, a good board designer will design a board with much greater signal integrity because the will not necessarily route to change layers at a road block, but rather might consider all the options and ramifications to routing a signal in a certain way and will choose the best path. These traces tend to be shorter and have fewer vias, which often helps to keep a board to a lower layer count. A board designer can also do layer paired routing which is very good for containing the high speed energy of most current technology. Basically, layer paired routing means that a signal routed on a layer that returns on a certain plane switches to the signal layer on the other side of that same plane when it needs to change direction. See Fig. 21.27. This contains the energy to that particular area of those particular layers of the board, rather than letting it spread out all over the board.

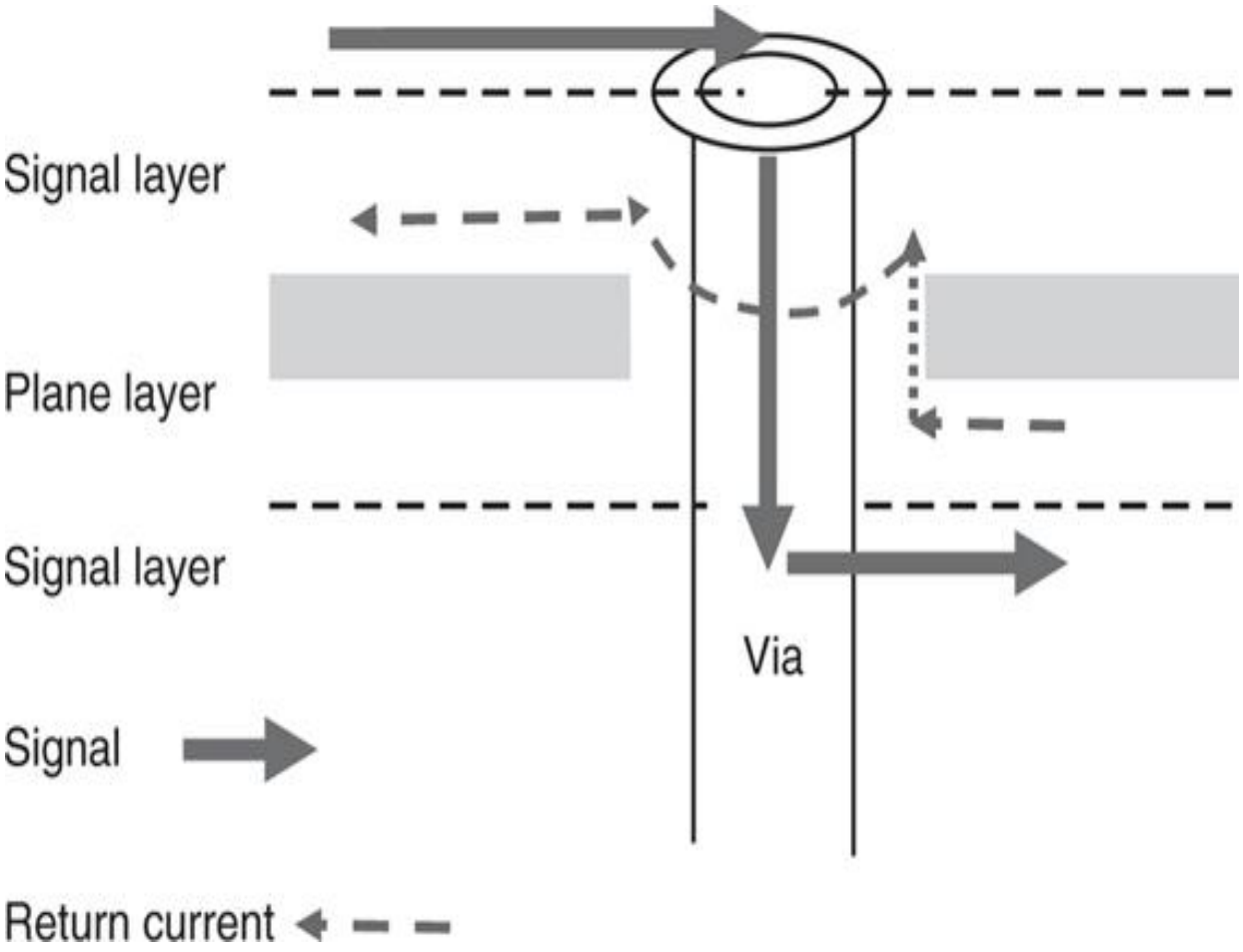


FIGURE 21.27 A close-up of layers involved in layer paired routing.

Some choose to route all the important or critical connections by hand, and then place the board into the autorouter to finish things up.

Notes placed into a blank layer of the database may be helpful in several scenarios. They may cause a person remember what they were doing if they are pulled off the project to work on something else. When they return to the original project, they will know exactly what they were doing. They may help with notes about placement or routing changes that are needed but haven’t been accomplished yet. And if someone has to make changes to the board as an ECO later on the notes can explain why things were done a certain way.

When routing, remember that every board is different and each will have its own set of priorities. One set of rules will not work for every board! Find out all you can about the parts and signals on the board at hand and what might work best for that particular board.

21.11 FINISHING

After the board is routed, there is still work to do….

One of the steps between designing and finishing a board is to run Design Rule Checker (DRC). It is always ideal to have a clean DRC report with no errors at all. There are occasions, however, when there will be errors that cannot or will not be cleared. (This might be something that you would document in text in the board design file.) All the constraints that were entered into the software should be checked to make sure that they were accomplished. Also, there should be a check for unconnected nets or pins, any differential pairs, noisy signals next to any other signals, same net trace spacing, and anything else that might be particular to this board.

At this point, the board might be resequenced. This is done so that when people are checking, testing or working with the board it is easier to find components. Most boards are resequenced in a gridded pattern of left to right and top to bottom on the top side and then the bottom side is done the same way. See Fig. 21.28. This renumbering can then be annotated back to the schematic so that the two are in sync. At that point, it is a good practice to import the newly resequenced schematic netlist one more time into the newly resequenced board to make sure that they are the same.

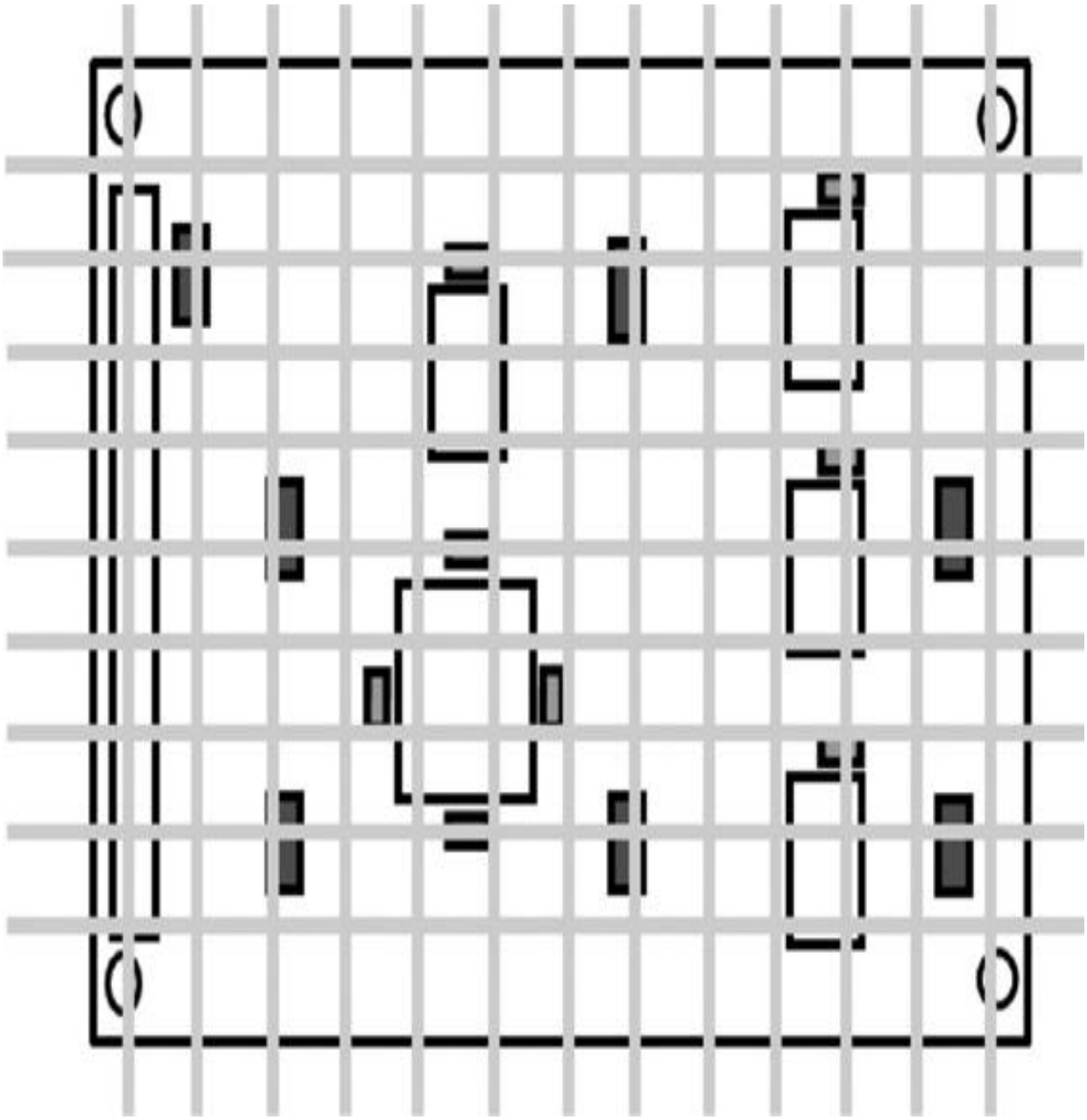


FIGURE 21.28 Gridded resequencing pattern.

Since the reference designators have been resequenced, their position might have changed. Now is a good time to move the text and reference designators so that they are easy to read, easy to see which component each belongs to, that they are placed outside the component area, and that they don’t fall on top of any pads or vias. If it is placed on pads or vias, it will be deleted during the fabrication

processes and so will be useless. If there is no room for the reference designator right next to the part but there is room close by, a line or leader can be drawn between them as shown in Fig. 21.29. Some designs are just too complex for reference designators and so the Assembly drawing must be carefully drawn to show which components are located where.

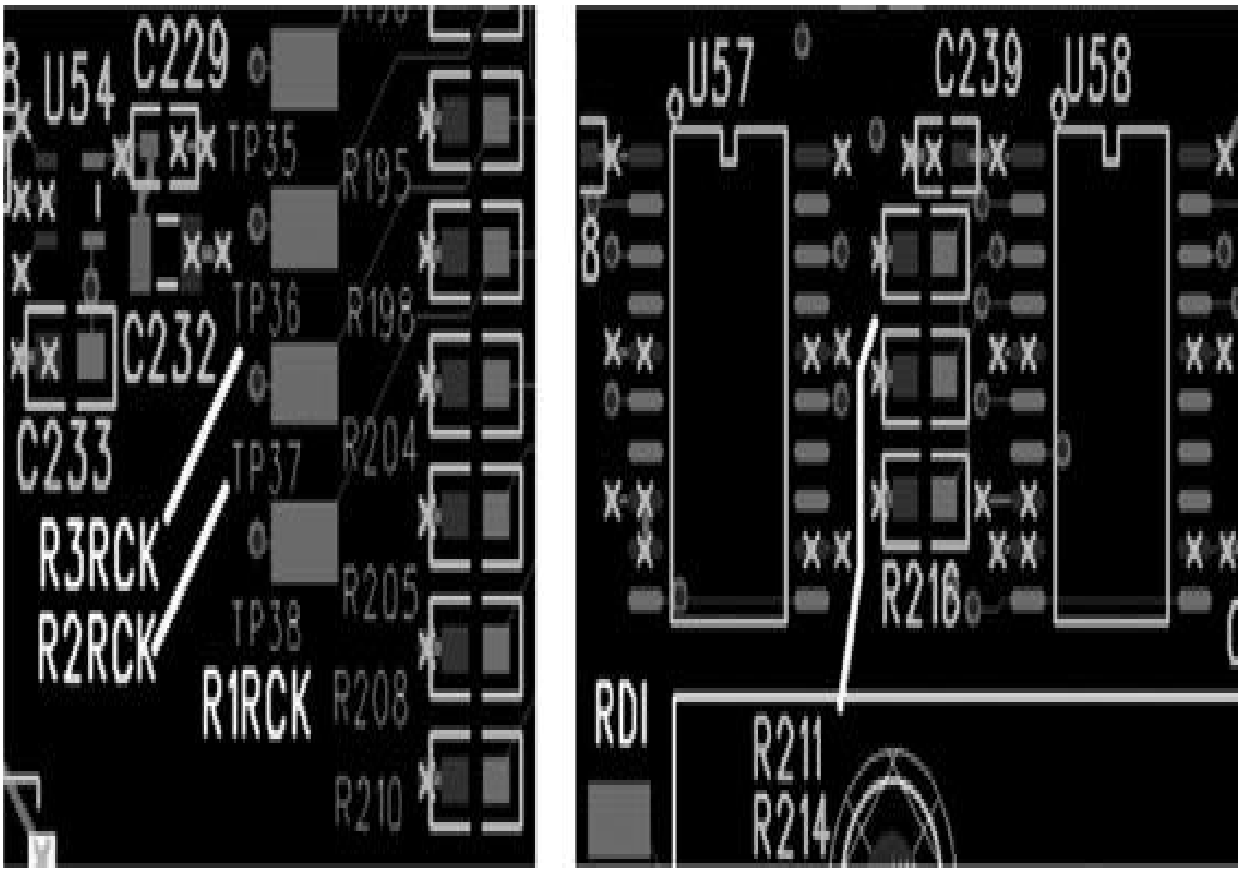


FIGURE 21.29 Reference information with a leader to location.

In addition to the reference designators, there may be other documentation that will be needed on the board. That might include company name, board name, assembly number, test point names, made or assembled in USA, pin or polarity indicators, and of course the complete outline of the part, all in silkscreen. Once again, make sure that the new silkscreen information does not fall onto pads or vias.

The board can then be set up for its fabrication drawing information. Outline dimensions and tolerances can be added to the “fab” layer. It is important that any notes that are added on the fab drawing be checked out by the fabricator to ensure that they mean the same thing to them as they do to the board designer. The drill schedule should include every individual size of hole to be drilled, the tolerance for each (usually ±0.003 in), whether plated or nonplated, and the quantity. There should also be a detailed drawing of the stackup for the board that includes layer name, copper weight, the amount of plating, dielectric thickness between layers, and the impedance if control is required. There will need to be good communication with the fabricator to be sure they have everything they need to complete the board.

The output files from the PCB software will be Gerber files, ODB++ files, or IPC 2581 files. The fabricator may want to give his preferences as to which kind of files he prefers to receive. At a minimum, the individual layers of the output files should be looked at carefully to ensure that they are the same as the board files after the translation. And it is also helpful to check an individual layer with its associated layers (example top layer with top silkscreen layer) to be sure that they will work together as expected. A list of all the files that are sent to fabricator helps him know what he has received. When questions come up, it is also good that they have contact information for the board designer. Anything the designer can do to make fab or assembly easier, will lower the cost of the board.

The output files might include, but are not limited to, fab and assembly documents, auto insertion files for the pick and place machines, IPC-D-356 file of the netlist connections, an ascii file of the database (if appropriate), and any special fab or assembly information. If there is a company standards document, it may be included as well.

21.12 SAVING

Make a new copy of the database every day while working and include the date in the name. That way, if any problem occurs, the most that will be lost is a single day's work. It would be good to save a minimum of a few days' worth of data so that one can revert to an older way things were done, if necessary. It's also a good idea to save a copy of the board at certain milestones. For example, if it is saved as XXXB4resq, the database is still available if something goes wrong in the process of re-sequencing.

When the project is completed, everything should be copied to its permanent home on the network, and possibly make that directory read only so nothing can arbitrarily be changed. This will be the "master" information for starting any changes (ECOs) to the board and all other documentation and databases might be deleted so that there is never any question as to which copy of the database is the latest or correct one.

21.13 CONCLUSION

This is by no means meant to be everything that is needed to design a PCB, but it is only a beginning. Hopefully it is a reasonable start. There are many sources of information available to the novice designer for questions that are not answered here. They might include user's forums, conferences, IPC Designer's Council meetings, technical support personnel, fabricators and assemblers, and anyone in your network of PCB designers.

Antipad—an opening in a plane that is larger than the pad so that the pad will not make connection

BGA—a component called a Ball Grid Array

BOM—Bill Of Material or parts list

DXF—a mechanical file format

EMI—ElectroMechanical Interference

ESD—Electro-Static Device

FANOUT—the process of bringing a trace from a surface-mounted pad to a via to change layers

FLEX—a PCB made on flexible material

HAST—Highly Accelerated Stress Test

I/O—a connection that flows onto or off of the board

IPC—Association Connecting Electronic Industries

MCM—MultiChip Module

MRP—Manufacturing Resource Planning system

Netlist—a compilation of all the parts and interconnections on the schematic

Padstack—a group of pads, each used on a different layer of a PCB for interconnect

PCB—Printed Circuit Board

QFP—a component called a Quad Flat Pack

R-PAK—resistor pack

Schematic—the document that contains the symbols and their interconnects to all the other symbol

SM—Solder Mask

SMT—Surface Mount Technology—parts that solder directly to pads on one layer of the PCB

SOIC—Small Outline Integrated Circuit

TH—Through Hole—parts whose leads solder through holes in the PCB

Thermal pad—a pad connecting a TH to a plane with small copper spokes

Via—a through hole on a board that is solely meant to move a signal from one layer to another

X-out—a board in a panel or array that has been identified as imperfect

CHAPTER 22

CURRENT CARRYING CAPACITY IN PRINTED CIRCUITS

Mike Jouppi
Thermal Management Inc., Centennial, Colorado

22.1 INTRODUCTION

Current carrying capacity refers to the steady state temperature rise of a conductor in a printed circuit board (PCB) when current is applied. When multiple conductors have a simultaneously applied current, the rules for sizing traces changes and the parallel conductor rule must be followed.

This chapter assumes that the reader has some experience with conductor sizing charts. There are many charts found in various sources. This chapter concentrates on charts presented in IPC-2152, Standard for Determining Current Carrying Capacity in Printed Board Design, and the charts they replaced. The charts that were replaced have a long history dating back to the mid-1950s and were last published in IPC-2221.

There are many claims through using the Arrhenius function that electronics reliability is directly related to its operating temperature. Each 10°C temperature rise reduces component life by 50 percent. Conversely, each 10°C temperature reduction increases component life by 100 percent. Regardless of whether this is exactly true or not, it is still worth keeping electronics as cool as possible and optimizing reliability and the return on investment.

An accurate estimate of component temperatures requires consideration of all heat sources. Current carrying capacity and the temperature rise of the PCB traces is one aspect of electronics thermal management.

This chapter is written to help provide a basis of understanding for current carrying capacity in printed circuits and bring attention to IPC-2152. The purpose is to discuss how certain aspects of a circuit board affect the temperature rise of a trace. PCB thickness, dielectric material, number of copper planes, distance from trace to copper plane, size of the copper plane, environment and more, all impact the temperature rise of a trace.

It is not possible to collect test data and create charts for every variation of dielectric material, board thickness, number of layers, and all other ways that a PCB can be constructed. What is presented in IPC-2152, by the IPC-1-10b task group,[a] is a standard configuration. The standard configuration is called a baseline, which is used to compare how certain aspects of the board change the temperature rise of the trace when compared to the baseline. The baseline is for a specific material (polyimide), specific thickness [1.78 mm (0.07 in)], and specific size board with only traces that is defined in IPC-TM-650 2.5.4.1a.

22.2 CONDUCTOR (TRACE) SIZING CHARTS

There is very little public information that defines conductor sizing charts. Therefore, the first part of this chapter discusses the data that was used to create the external conductor sizing chart last published in IPC-2221. The importance of this discussion is to draw attention to some of the variables that impact trace temperature rise, which will then lead into the internal conductor sizing chart in IPC-2221. Following that discussion will be information used to create IPC-2152 and why there is such a significant difference between the old and new charts.

22.2.1 Conductor Sizing Chart Development

Conductor sizing charts were first introduced in 1956. Work performed at the United States National Bureau of Standards from January to December 1955 is documented in NBS Report 4283, dated May 1, 1956.[1] This work was the first data set published when printed circuit techniques were first gaining widespread acceptance for military and industrial applications. The work documented in that report was not considered complete and the design guide was labeled tentative; see Fig. 22.1. The charts in that report were published in a multitude of Mil-Std-275 revisions, which were then continued in IPC-D-275 and last published in IPC-2221. This history is captured in the appendix of IPC-2152.

Design chart
(Tentative)

For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.
(Note: See design guide on preceding page for use of this chart).

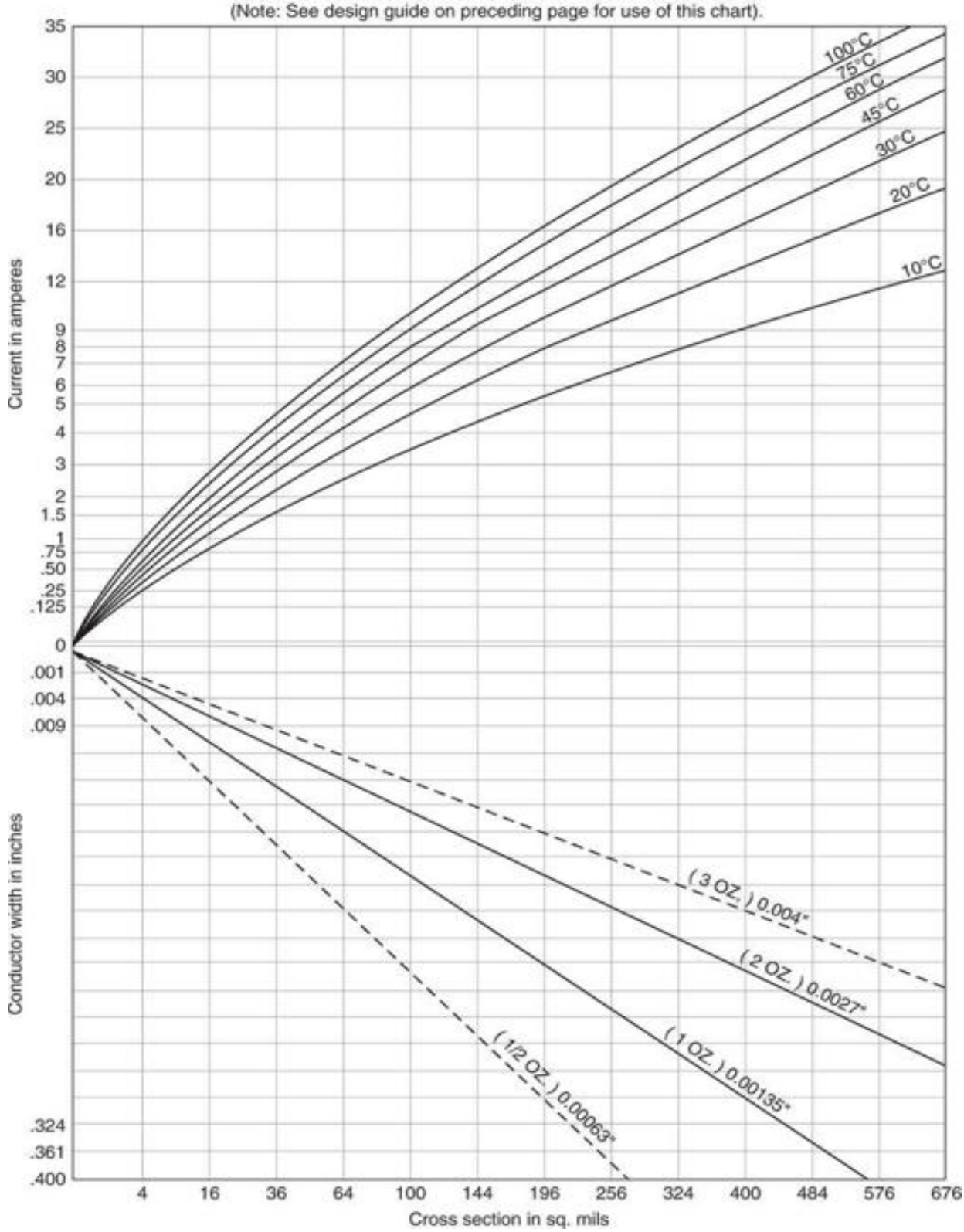


FIGURE 22.1 National Bureau of Standards tentative chart (1955).

The old charts were developed by applying current to traces and measuring the temperature rise of the trace in many different types of boards. The boards varied in thickness, board material, conductor weight, and some with copper planes on the back side of the board. The copper planes have a significant impact on trace temperature rise. A curve fit through all of these mixed sets of trace heating data skews the ability to accurately predict a trace temperature rise or a group of parallel traces.

The original trace heating data was collected only on external conductors. The trace heating data included traces on phenolic and epoxy boards, board core thicknesses of 0.03125, 0.0625, and 0.125 in, with ½, 1, 2, and 3 oz copper weight traces, as well as from boards with and without copper planes on the back side of the board. A plot of some of the original data is shown in Fig. 22.2. The test vehicle description for the data points shown in Fig. 22.2 are listed in Table 22.1. Figure 22.1 was used to create the old external chart that was last published in IPC-2221; see Fig. 22.3.

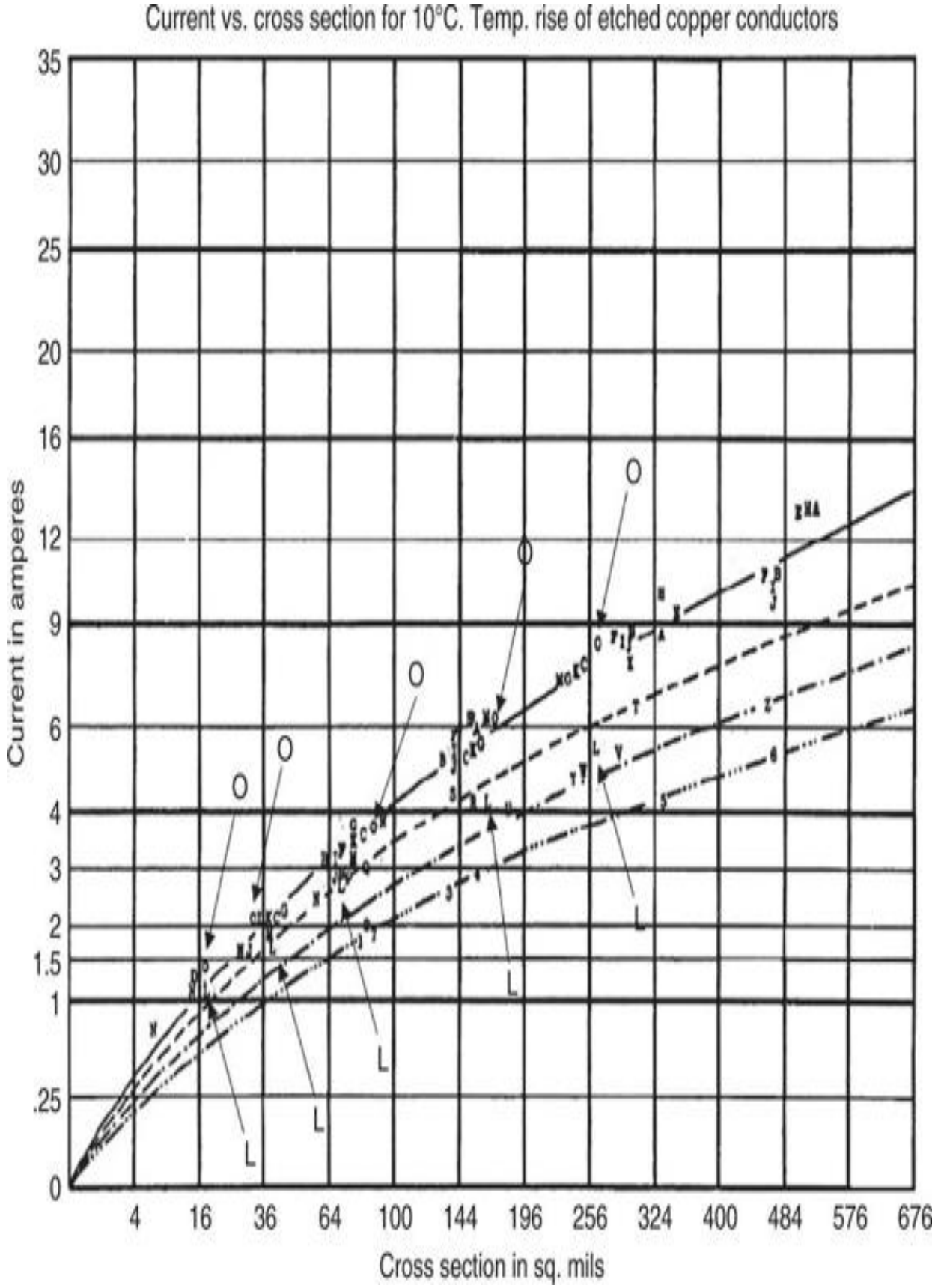

Current vs. cross section for 10°C. Temp. rise of etched copper conductors
Current in amperes
35
30
25
20
16
12
9
6
4
3
2
1.5
1
.25
0
4
16
36
64
100
144
196
256
324
400
484
576
676
Cross section in sq. mils
O
L

FIGURE 22.2 National Bureau of Standards 10°C chart (data for 1955 chart).

TABLE 22.1 NBS Chart Conductor Data Test Vehicles (1955)

Materials, processing, and conditions used in determining the temperature rises of various etched conductors.

Code	Material and Core Thickness (in)	Copper Thickness (in)*	Additional Processing	Test Temp °C	Test Method**
A	5–7 XXXP 1/16	.0027KK	None	50	IR & TC
B	2–7 XXXP 1/16	.004K	None	50	IR & TC
C	4–7 XXXP 1/16	.00135K	None	50	IR
D	4–10 Epoxy 1/16	.00135K	None	50	IR & TC
E	5–7 XXXP 1/16	.0027K	None	60	IR & TC
F	2–7 XXXP 1/16	.0027K	None	60	IR
G	4–7 XXXP 1/16	.00135KK	None	60	IR
H	5–7 XXXP 1/16	.0027KK	None	25	IR
I	2–7 XXXP 1/16	.004K	None	25	IR & TC
J	5–10 Epoxy 1/8	.0027K	None	25	IR
K	4–7 XXXP 1/16	.00135KK	None	25	IR
L	5–10 Epoxy 1/32	.00135K	None	25	IR
M	4–10 Epoxy l/16	.00135K	None	25	TC
N	2–7 XXXP 1/16	.00067K	None	25	IR

O	5–10 Epoxy 1/16	.00135KK	None	25	IR
P	4–10 Epoxy 1/16	.00135K	Coated with .005" Epoxy Resin	25	IR
Q	2–7 XXXP 1/16	.00135K	Coated with .002" Insulating Varnish	25	IR
R	5–7 XXXP 1/16	.0027K	Coated with .001" Silicone Spray	25	IR
S	4–7 XXXP 1/16	.00135K	Coated with .003" Insulating Varnish	25	IR
T	2–7 XXXP 1/16	.0027K	Coated with .006" Silicone Resin	25	IR
U	2–7 XXXP 1/16	.00135K	Dip soldered 10 sec. 250 °C	25	IR
V	2–7 XXXP 1/16	.0027K	Dip soldered 10 sec. 250 °C	25	IR
W	10–7 XYXP 1/16	.00135K	Dip soldered 10 sec. 250 °C	25	IR
X	5–10 Epoxy 1/8	.0027K	Dip sold. and Coated with .005" Epoxy Res.	25	IR & TC
Y	4–7 XXXP 1/16	.00135K	Dip soldered 10 sec. 250 °C	25	IR
Z	2–7 XXXP 1/16	.0027K	Dip soldered 10 sec. 250 °C	25	TC
1	5–7 XXXP	.00135	Core Removed Conductor in Free Air	25	IR
2	6–16 G-5	.00135	Core Removed Conductor in Free Air	25	IR
3	2–7 XXXP	.00135	Core Removed Conductor in Free Air	25	IR
4	5–7 XXXP	.0027	Core Removed Conductor in Free Air	25	IR
5	2–7 XXXP	.0027	Core Removed Conductor in Free Air	25	IR
6	2–7 XXXP	.0027	Core Removed Conductor in Free Air	25	IR
7	4–10 Epoxy	.00135	Core Removed Conductor in Free Air	25	IR

*K denotes single-clad material, and KK denotes double-clad material.

**IR = IR drop measurement; TC = thermocouple measurement.

(For use in determining current carrying capacity and sizes of etched copper conductors for various temperature rises above ambient.)

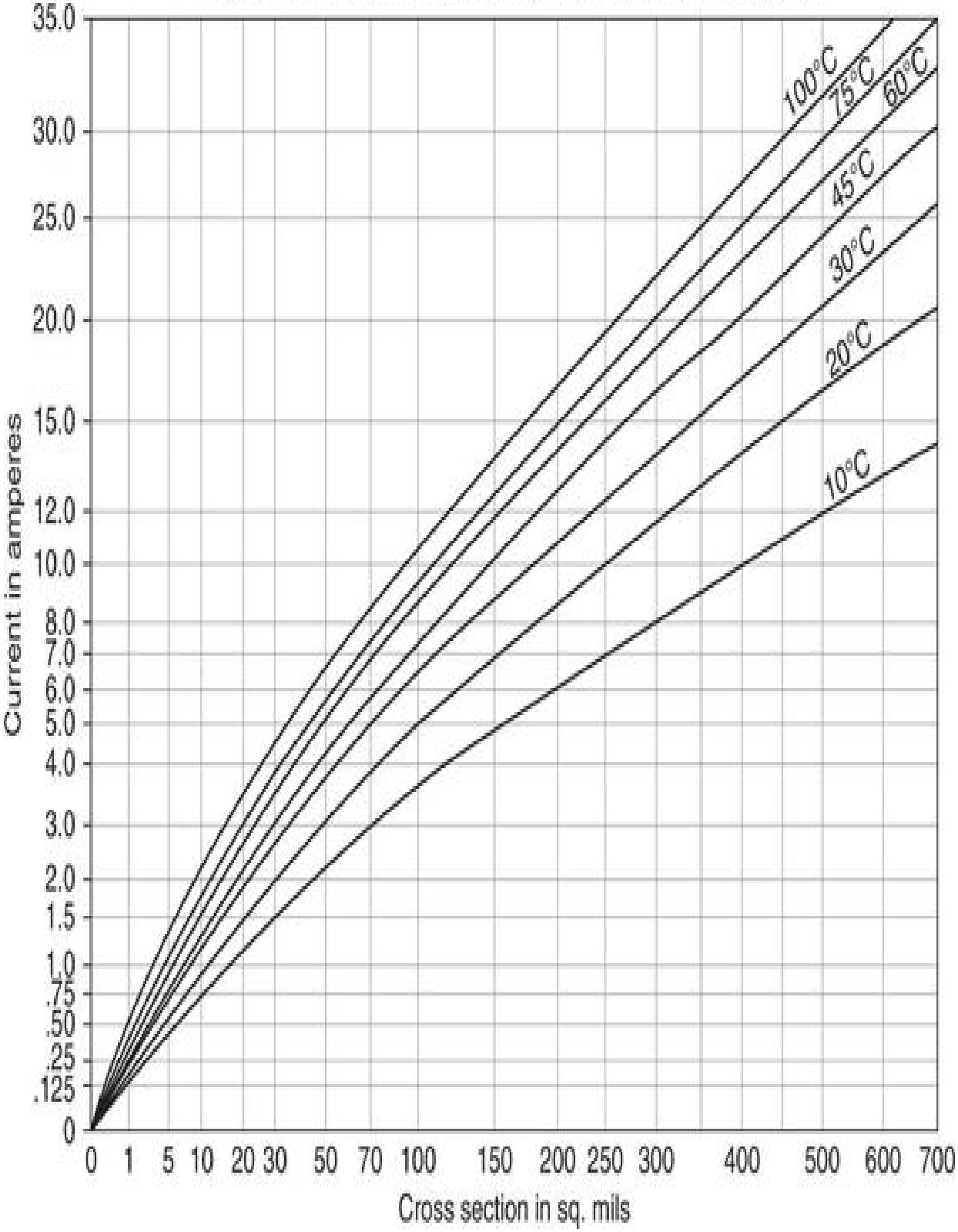


FIGURE 22.3 IPC-2221 external conductor sizing chart (old chart).

There are many observations to be made when looking at Fig. 22.2 and Table 22.2. When making the observations one must keep in mind the time period (mid-1950s), the instrumentation available and accuracy of the data. Four observations are discussed:

1. The first observation is that the dominant characteristic for current carrying capacity is the cross-sectional area.
2. Second, a noticeable reduction in current carrying capacity is seen for the thinner core material (L) at 1/32 in. Data collected for IPC-2152 observed a reduction in current carrying capacity as core thickness decreased, which although is not discussed in this chapter, brings attention to flex circuits.
3. Third, the influence of a copper plane on the core is shown to have significant impact for the thinner core (O). This influence of the copper core is less pronounce for the thicker boards where the distance from the trace to the plane is a greater distance. Data and thermal modeling of conductors for IPC-2152 clearly shows that there is a significant drop in the conductor temperature rise as the distance from a conductor to a copper plane decreases.
4. The last observation is that conductors in free air have the least current carrying capacity. The thermal conductivity of the epoxy and phenolic cores were not reported, although have a value that is approximately 0.354 W/m-K. Air has a thermal conductivity of approximately 0.026 W/m-K. The point here is that a trace conducts more energy into a core with high thermal conductivity than air with low thermal conductivity, neglecting any discussion on the convective and radiative losses.

TABLE 22.2 Dielectric Thermal Conductivity

Material	kx (W/in-C)	ky (W/in-C)	kz (W/in-C)
FR-4	0.0124	0.0124	0.0076
Polyimide	0.0138	0.0138	0.0085

In general, many people believed that internal conductors ran hotter than external conductors for a given cross-sectional area and current level. This fallacy was created by the old internal conductor sizing chart shown in Fig. 22.4. The casual observer would believe this internal conductor sizing chart was developed by performing current carrying testing on internal conductors, when actually the current is just ½ the current from the external conductor sizing chart; see Fig. 22.3. Testing from 2001 to 2004 show internal conductors operate at a similar temperature, but slightly cooler than external conductors for current carrying capacity (see Figs. 22.7 and 22.8).

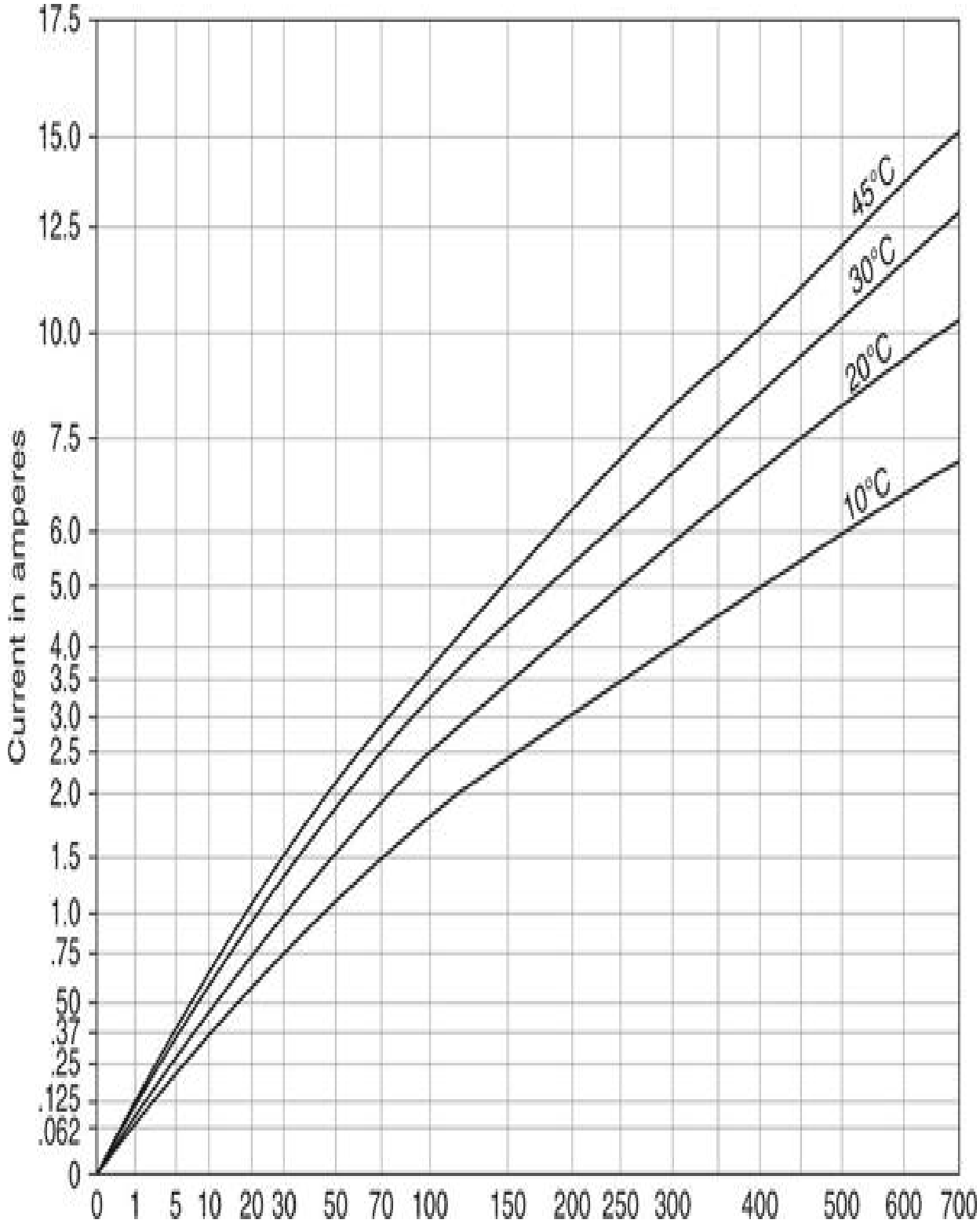


FIGURE 22.4 IPC-2221 internal conductor sizing chart (old chart).

22.3 BASELINE CHARTS

IPC-2152, “Standard for Determining Current Carrying Capacity in Printed Board Design,” was developed by the IPC-1-10b task group.[b] They defined a set of charts called baseline charts that are used to determine the temperature rise of a trace and assess variables that influence that trace temperature rise. An example of the difference between what is calculated using the old internal trace sizing chart and the new is shown in Fig. 22.5.

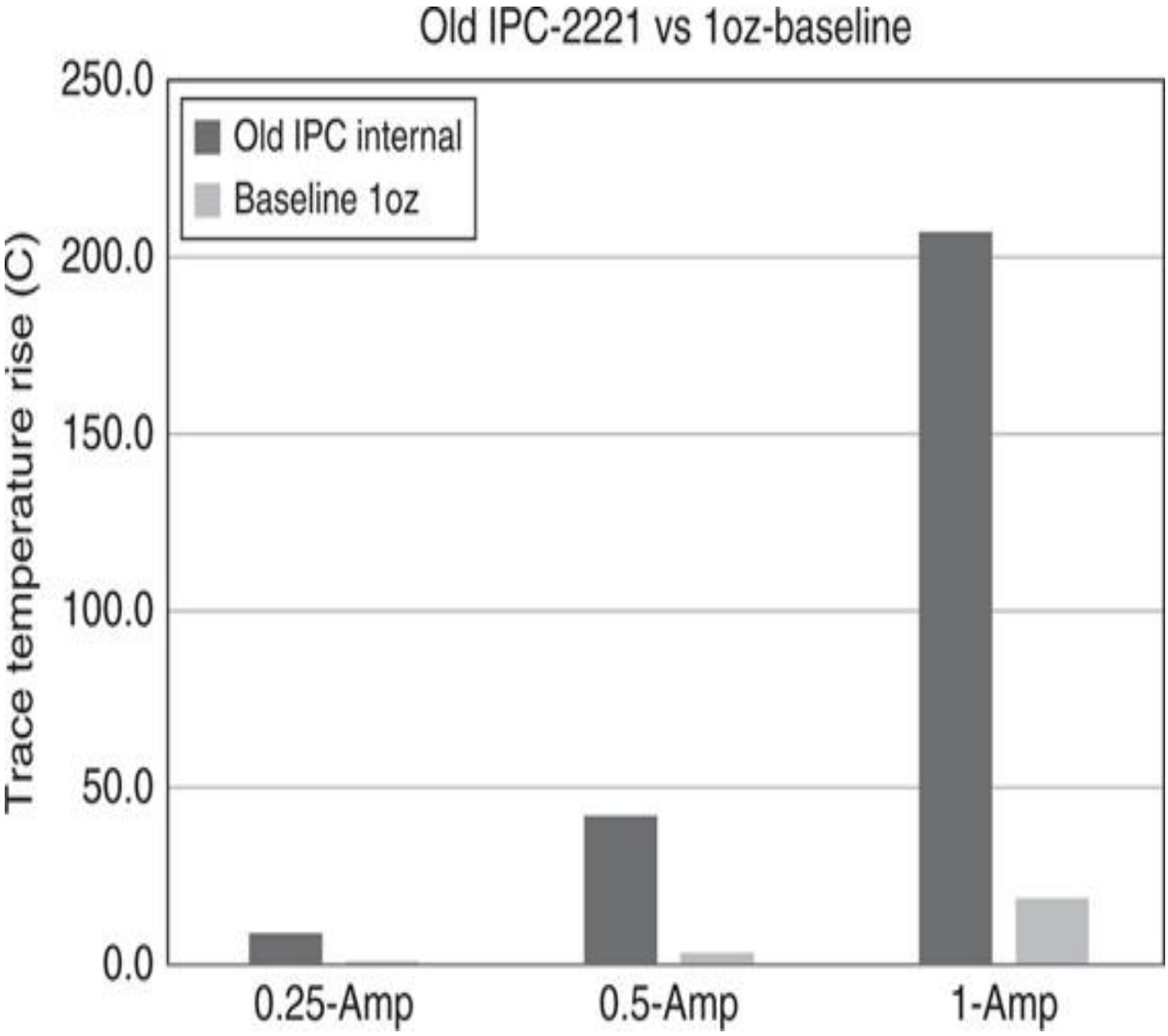


FIGURE 22.5 Old chart versus new baseline for a 0.005-in-wide, internal 1-oz trace.

The *baseline charts* were developed from current carrying capacity testing using polyimide PCBs, 1.78 mm (0.07 in) thick, with no internal copper planes. Test vehicles were developed and current carrying capacity testing was performed following IPC test method, IPC-TM-650-2.5.4.1a, “Conductor Temperature Rise due to Current Changes in Conductors.” An advantage of using a baseline chart is that it provides a more accurate trace temperature estimate in general, as well as when extrapolating the data for higher current estimates and trace cross-sectional area greater than 700 sq. mils.

Two internal baseline charts, 1 oz and 2 oz internal traces, and one external baseline chart are presented; see Figs. 22.6 through 22.8. These charts represent a subset of data collected for ½-, 1-, 2-, and 3-oz copper weights, FR-4 and polyimide boards, and printed wiring boards (PWB) with board thicknesses of 0.965 mm (0.038 in), 1.498 mm (0.059 in), and 1.78 mm (0.07 in), all of which are discussed in IPC-2152.

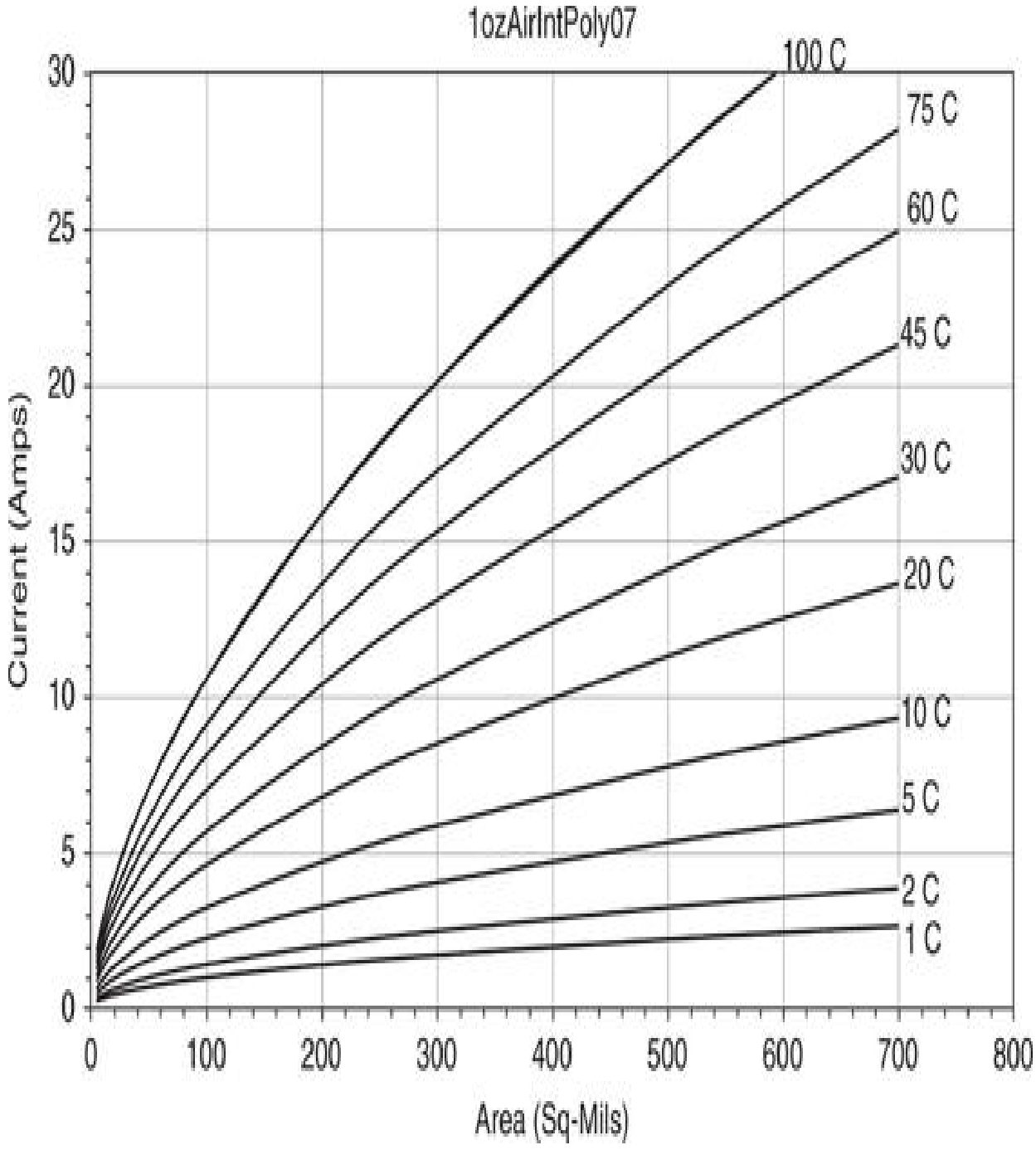


FIGURE 22.6 One-ounce internal conductor chart (new IPC-2152).

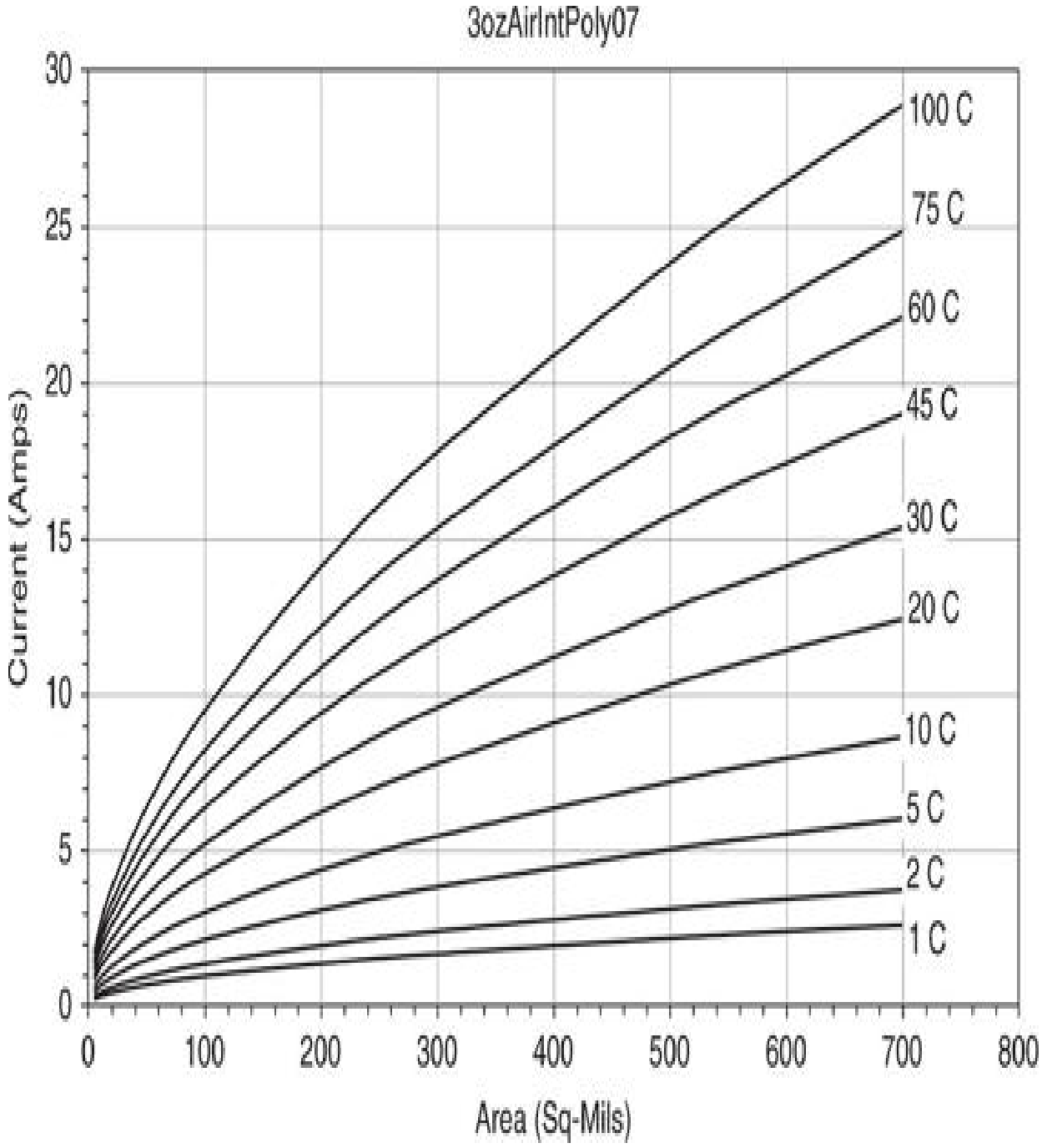


FIGURE 22.7 Three-ounce internal conductor chart (new IPC-2152).

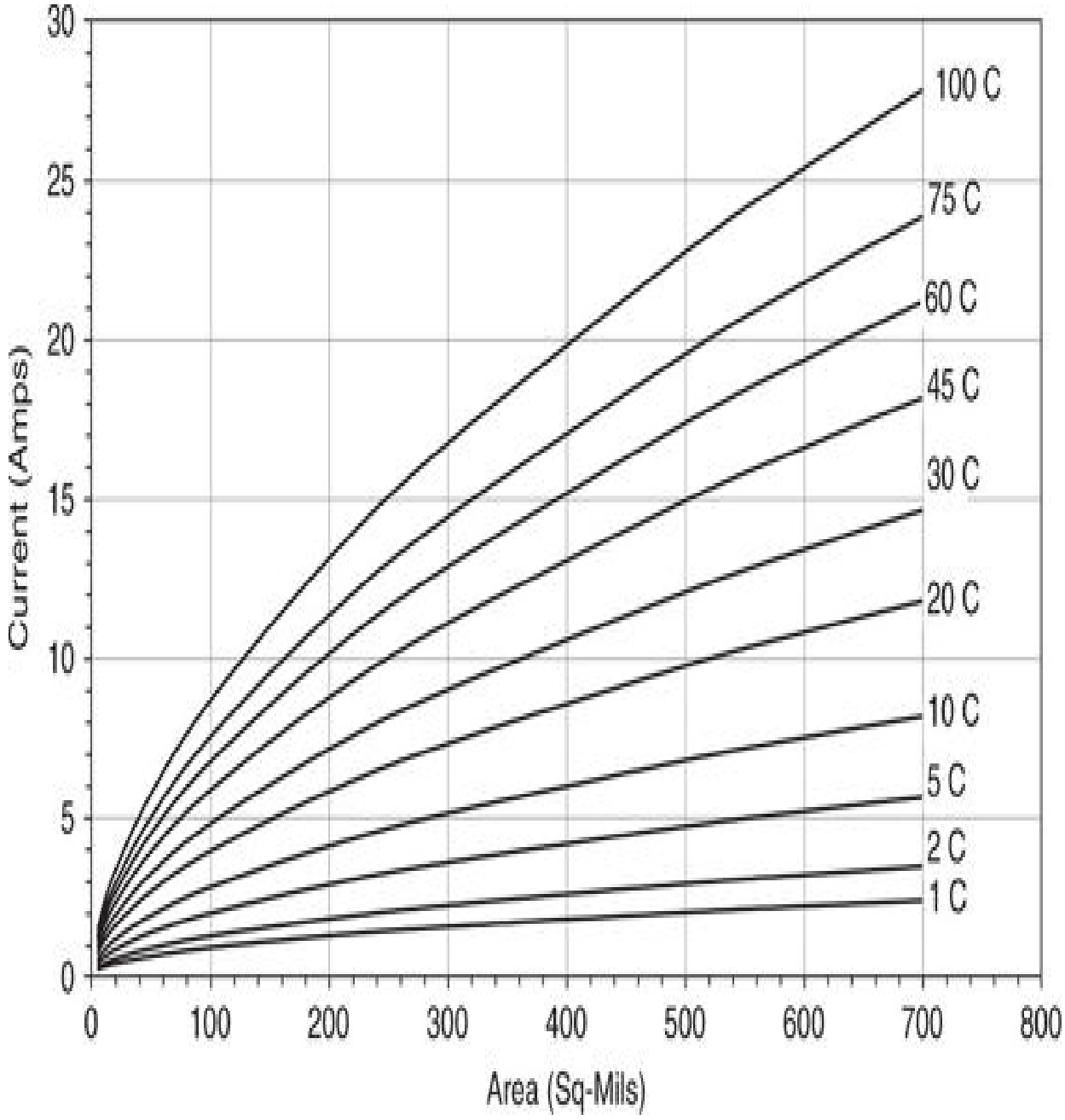


FIGURE 22.8 Three-ounce external conductor chart (new IPC-2152).

22.3.1 Baseline Testing

The baseline test vehicle is a polyimide PCB that is 1.78 mm (0.07 in) thick, designed, and tested following IPC-TM-650-

2.5.4.1a. The steady-state conductor temperature rise was investigated as a function of the following parameters:

- Current level
- Cross-sectional area of the trace
- Copper weight
- Board thickness
- Board material
- Environment (still air, vacuum)
- Distance from a trace to a copper plane

The IPC-2152 baseline charts are

- 3 oz external (0.07 in polyimide in air)
- 2 oz external (0.07 in polyimide in air)
- 3 oz internal (0.07 in polyimide in air)
- 2 oz internal (0.07 in polyimide in air)
- 1 oz internal (0.07 in polyimide in air)
- ½ oz internal (0.07 in polyimide in air)

Examples of the baselines charts are presented in Figs. 22.6 through 22.8. Figure 22.6 represents the data set for 1-oz internal conductors with a 0.07-in thick polyimide core in an air environment. Figure 22.7 is for the same core and environment, although the copper weight is 3 oz. There is a small effect on trace temperature rise as conductor weight increases, it can be seen in the charts for the 1 oz and 3 oz traces, most noted at higher temperature differences. Figure 22.8 represents data collected for 3 oz external conductors. Temperature differences are observed between internal and external traces, for the same board material, board thickness, environment and cross-sectional area; when comparing Figs. 22.7 and 22.8.

22.3.2 Copper Planes (Modeling)

The baseline test vehicle has no copper planes in the core. This is not representative of a large percentage of designs, therefore computer modeling was used to investigate the impact of copper planes on trace temperature rise. Copper planes help spread the heat and lower the temperature rise of what would otherwise be a hot spot created by the trace.

Copper planes add another dimension to trace heating, because the trace temperature is then dependent on the size of the copper plane and the distance from the trace to the plane. The modeling assumes an ideal copper plane with no holes or cutouts. Charts are provided in IPC-2152 to account for the influence of copper planes and an estimate for the reduction in trace temperature rise. They are not recommended as a trace sizing tool, but rather an approach toward estimating margin in a design. An example of the influence of a 1-oz internal copper plane on a 5-mil trace is shown in Fig. 22.9.

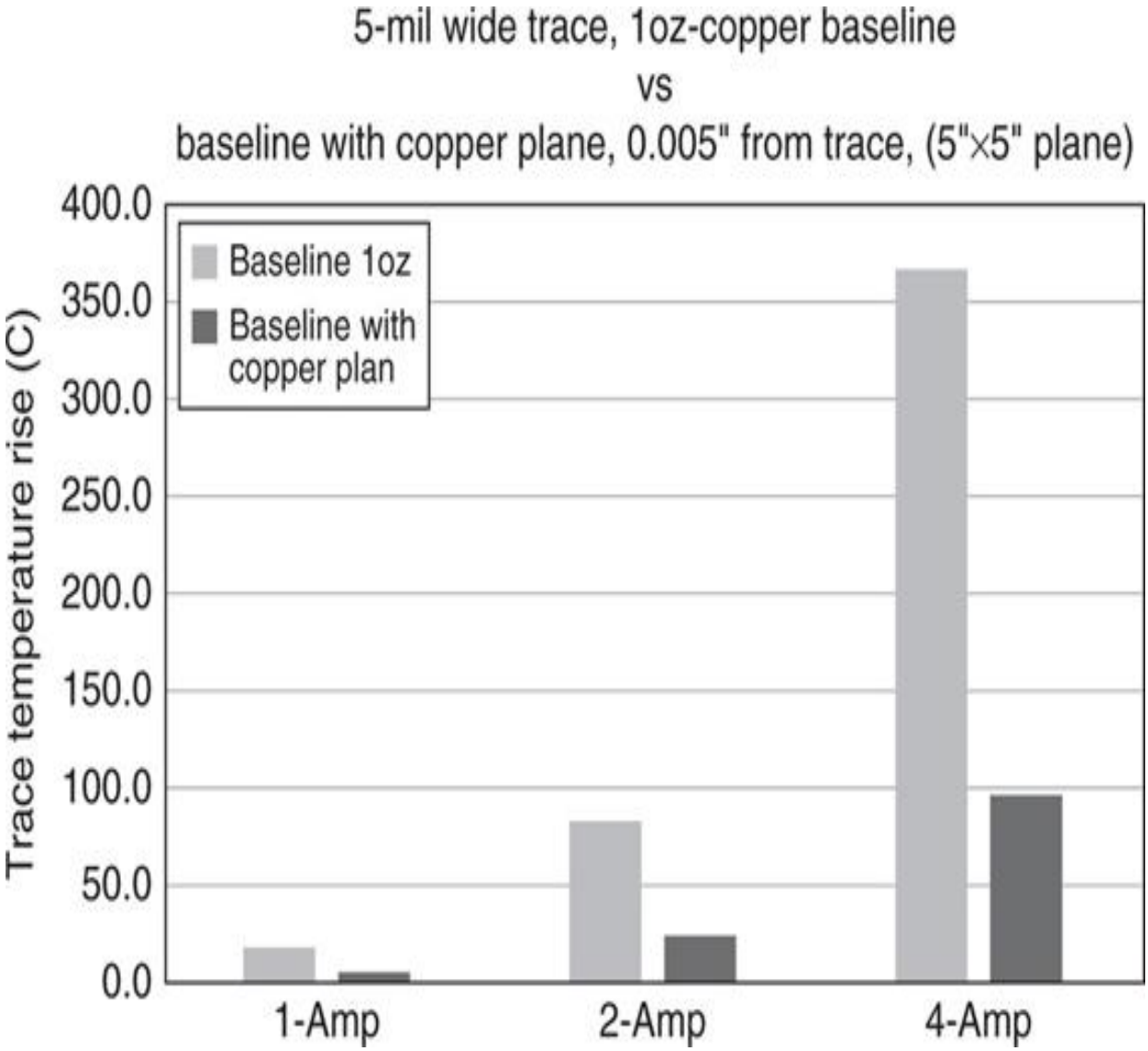


FIGURE 22.9 One-ounce baseline for a 0.005-in-wide, internal 1 oz trace versus with 1 oz internal plane (new IPC-2152).

22.3.3 Board Material

FR-4 boards were tested in addition to the 0.07-in core polyimide boards. The FR-4 board core material was 0.038 in for one set and 0.059 in for the other. The thermal conductivity had a secondary effect compared to the board thickness. The measured thermal conductivity for the two laminates tested are listed in Table 22.2.

22.3.4 Board Thickness

The thickness of the board affects the trace temperature rise. When comparing test results for the 0.038-in and 0.059-in-thick boards to the baseline board, 0.07-in thick, as the board thickness decreased the trace temperature rise increased. For example, using the 1 oz, air, baseline chart; a 0.0088-in-wide trace, carrying 1 amp, produces a 10°C rise in trace temperature. That same trace in a 0.059-in-thick test board had a 12.1°C rise and a 0.038-in-thick board had a 13.3°C rise.

22.3.5 Environments

Data was collected in a still air environment and in vacuum for the baseline charts (Fig. 22.10). Results in a vacuum environment run hotter than in an air environment as expected. In a vacuum, the internal and external traces run approximately at the same temperature.

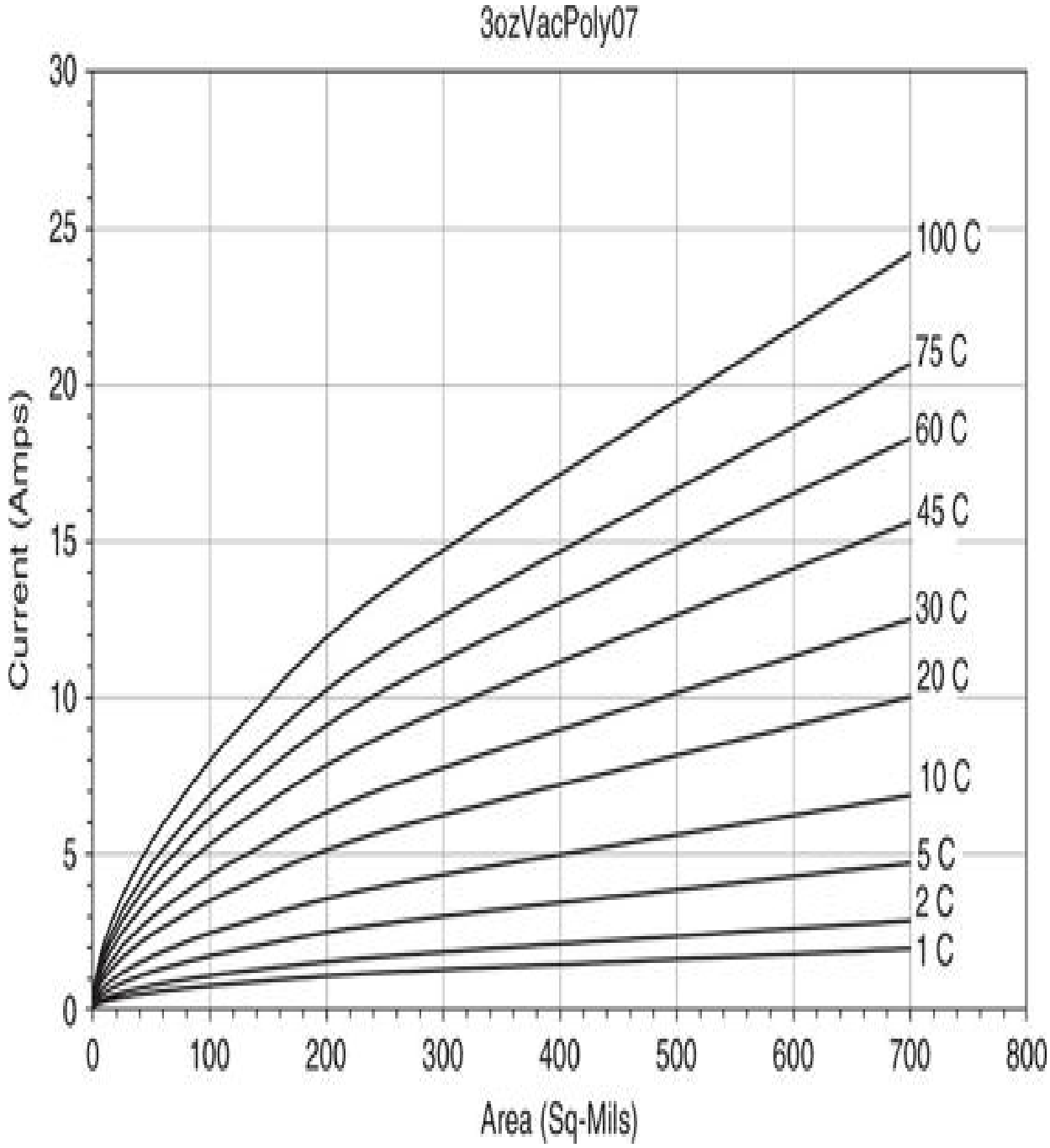


FIGURE 22.10 Three-ounce external/internal conductor chart (vacuum, new IPC-2152).

22.3.6 Copper Thickness

Copper thickness should be considered when sizing electrical traces. IPC-2221 specifies the minimum acceptable copper

thickness for internal and external layers as shown in Table 22.3 and 22.4,[2] The IPC printed circuit Process Capability, Quality, and Relative Reliability (PCQR[2]) database identifies end process copper dimensions for conductors. When sizing traces for a given current level, consideration should be given to the end product.

TABLE 22.3 Minimum Internal Copper Foil Thickness[c]

Internal Conductor Thickness after Processing		
	Minimum Thickness	
Copper Foil	(μm)	(in)
⅛ oz	3.5	0.000138
¼ oz	6	0.000236
⅜ oz	8	0.000315
½ oz	12	0.000472
1 oz	25	0.000984
2 oz	56	0.002205
3 oz	91	0.003583
4 oz	122	0.004803

[c]*IPC-2221, "Internal Layer Foil Thickness after Processing, Copper Foil Minimum," Table 10-1*

TABLE 22.4 Minimum External Conductor Thickness[d]

External Conductor Thickness after Plating		
	Minimum	
Base Copper Foil	(μm)	(in)
⅛ oz	20	0.000787
¼ oz	20	0.000787
⅜ oz	25	0.000984
½ oz	33	0.001299
1 oz	46	0.001811
2 oz	76	0.002992
3 oz	107	0.004213
4 oz	137	0.005394

[d]*Ibid., Table 10-2*

22.3.7 Parallel Conductors

“Parallel conductors” is an evolving term. They were first defined by the following: “For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-section of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.” No definition was given to closely spaced and this led to a lot of confusion about what conductors should be considered. IPC-2152 has color plots that are provided as

an aide to help get a sense of the heat spreading in an effort to illustrate and define “closely spaced” conductors.

All conductors that are simultaneously carrying current are heat sources that should be evaluated together as a part of the PWB thermal management design plan. Observe the number of traces that are above and below each other, from side to side, as well as throughout the rest of the PWB. Using those conductors the total current can be summed and a cross-section can be defined.

Estimating power losses for all conductors, simultaneously carrying current, is a simple way to start estimating any areas of concerns for conductor sizing. If the wattage for the specific design starts to become a significant percentage of the total power dissipated on the board, it becomes apparent that some design choices should be made.

Managing the temperature rise of traces by accounting for their power dissipation, and power density, in a preliminary thermal analysis prior to final layout is a time saving step in the design process.

Some of the most difficult areas to manage are when there are odd shaped geometries, such as around connectors where traces may be necked down to get around power pins, and copper planes that have a lot of cutouts and keep-outs for vias. These areas have potential for significant heating and are best solved with a thermal analysis tool.

22.3.8 Other Areas of Study

There are many areas of current carrying capacity that deserve more study, such as flex circuits, edge effects, mounting configurations, vias, microvias, high-speed effects, neck downs around connectors and the conduction path through the connector, and high-current pulses.

Recent investigations into high-current pulses have shown interesting results, where the trace was fusing earlier than

expected. These studies were preliminary, but help shed light on the need for understanding the limits to approaches we take to solve problems that may or may not have the research performed to support all of our assumptions.

22.4 Summary

New charts have been developed to help determine current carrying capacity in printed circuits. The new IPC-2152 baseline charts are conservative for most applications. They can be used to determine a trace temperature rise for a given current level for other board thicknesses, environments, and when copper planes are present. The flexibility of using the IPC-2152 charts is determined by how well the user understands the baseline charts.

Large differences are found between the old and new charts primarily due to collecting data for both external and internal traces. The difference that is observed between the old and new charts is a significant step and as the development of IPC-2152 continues there will be additional significant steps.

22.5 REFERENCES

1. Hoynes, D.S., “Characterization of Metal-Insulator Laminates, by Progress Report to Navy Bureau of Ships,” National Bureau of Standards Report 4283, January 1955–December 1955. (The National Bureau of Standards is now the National Institute of Standards and Technology [NIST].)
2. IPC-2221, “Internal Layer Foil Thickness after Processing, Copper Foil Minimum,” Table 10-1.

[a] The 1-10b task group is chartered to maintain IPC-2152, Standard for Determining Current Carrying Capacity in Printed Board Design. [IPC-2152 is published by the Institute for Interconnecting and Packaging Electronic Circuits (IPC); www.ipc.org.]

[b] The 1-10b task group is chartered to maintain IPC-2152, Standard for Determining Current Carrying Capacity in Printed Board Design. [IPC-2152 is published by the Institute for Interconnecting and Packaging Electronic Circuits (IPC); www.ipc.org.]

CHAPTER 23

PCB DESIGN FOR THERMAL PERFORMANCE

Mike Jouppi
Thermal Management Inc., Centennial, Colorado

23.1 INTRODUCTION

The reliability and electrical functionality of electronic components is partially determined by the temperature at which they operate. As such, control of the component temperatures in the system is an important design consideration. Factors that impact device temperatures include the power at which they operate, the air flow surrounding them, heat generation upstream to them, the environment in which the system operates (either indoors or outdoors), the system orientation (either vertical or horizontal), and a variety of printed circuit board (PCB) layout and design properties. These PCB design factors include the design of the copper (Cu) traces contacting the components, the number and area of Cu planes that are connected to them, any thermal vias that might be designed between them and the spreading planes, the proximity of

other devices that dissipate power, and any cuts in the thermally conducting layers. Additional PCB features that impact the thermal performance of components include chassis screws, connectors, edge guides, and shields.

To control component temperatures, PCB factors that impact thermal energy flow must be considered in the design phase of the PCB layout. These factors include many complex interactions that make application of simple equations to calculate system temperatures impossible. For example, the historical equation used to calculate component temperatures from a thermal resistance parameter called theta-*ja* (θ_{ja}) as shown in Eq. (23.1) is not applicable in modern systems. This is stated clearly in the Joint Electron Device Engineering Council (JEDEC) standard for θ_{ja}.[1] θ_{ja} is not a constant. It is a function of the PCB onto which the component is placed and can vary by a factor of two or more as a function of the PCB design layout. Therefore, if component temperatures are calculated using Eq. (23.1), wildly erroneous estimates may be accepted, which might lead to a system design that fails thermally.

$$T_{\text{junction}} = T_{\text{ambient}} + (\theta_{ja} * \text{power}) \tag{23.1}$$

where T_{junction} = the temperature of the active portion of the component
T_{ambient} = the temperature of the air at a specified location
θ_{ja} = the thermal resistance of the component as defined by JEDEC
power = the power of the component

This chapter describes best-design practices that enable the PCB designer to achieve the best possible thermal performance for a given design. As there is no method to calculate analytically the combined impact of the methods described, the designer is encouraged to use sophisticated tools to model the final component temperatures.

23.2 THE PCB AS A HEAT SINK SOLDERED TO THE COMPONENT

The PCB can be considered to be a heat sink that has been soldered to the leads or solder joints of the electronic component. The physical design of the PCB dramatically impacts its efficiency as a heat sink and the temperatures at which the components operate. Figure 23.1 helps to illustrate this point. Here, a packaged component (shown in cross section) is attached to the PCB. Heat is generated by current flowing through electrical resistances on the active surface of the die. This raises the temperature of the surface, resulting in a thermal gradient. Thermal energy (heat) flows from regions of high temperatures to regions of lower temperatures. For the component illustrated in Fig. 23.1, heat flows from the die through the die attach, then through any Cu metallization in the package substrate, then through the solder joints into the PCB. If there are good thermal conduction paths in the PCB, the heat spreads out over a large area of the PCB, allowing the potential for efficient convection and radiation into the environment. If there are few heat transfer paths in the PCB, the component is insulated and the temperature increases.

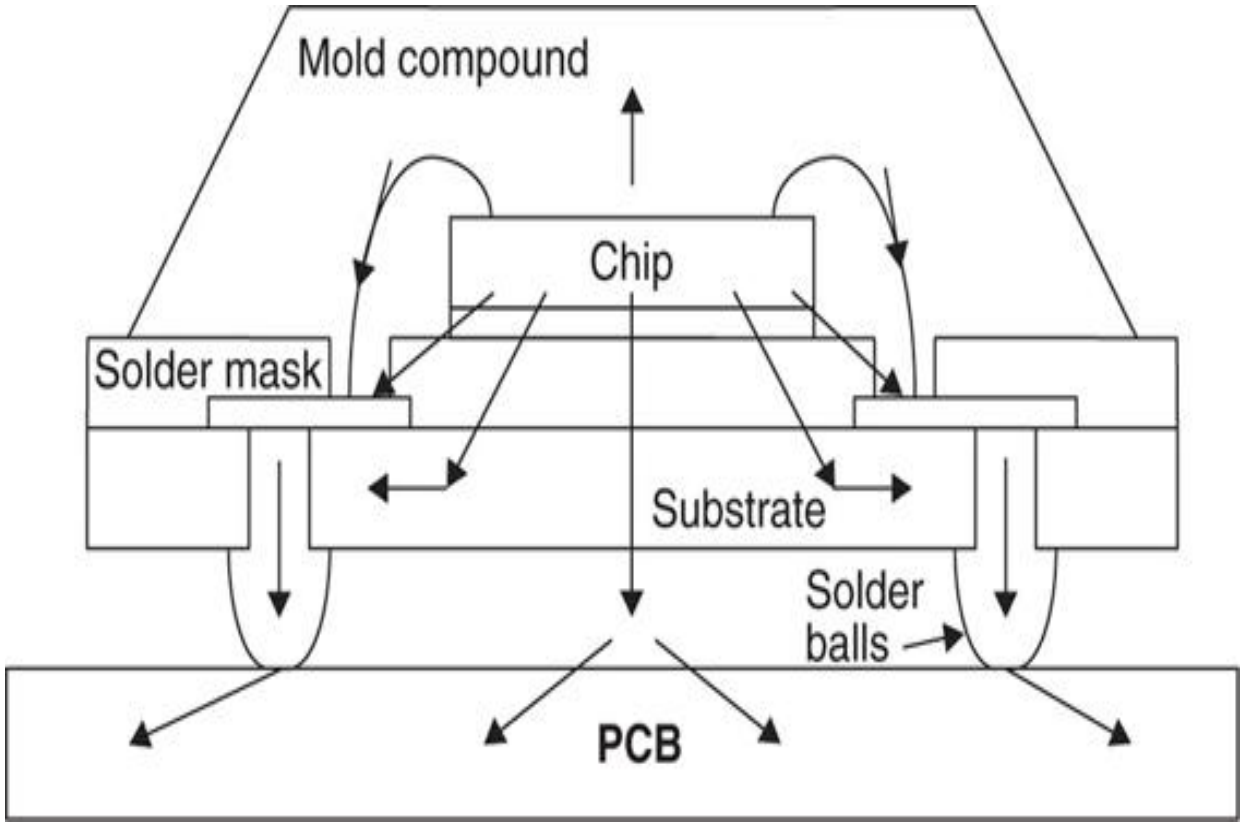


FIGURE 23.1 Cross-section of an electronic component on a PCB. The arrows indicate heat conduction paths.

How important is the PCB to the thermal performance of components? Depending on the PCB design, up to 60 to 95 percent of the thermal energy can be dissipated by the PCB. This type of performance can be achieved by PCBs that meet the following criteria:

- Large spreading planes to conduct heat away from the components
- Sparsely populated PCBs with large areas for convection and radiation
- Long traces interconnecting the components, again to conduct heat away from the components
- Sufficient spacing of PCBs in a system rack to enable adequate convection

Failure to meet these conditions will result in reduced thermal dissipation from the PCB, higher component operating temperatures, degraded device reliability, and perhaps even lack of electrical functionality.

23.3 OPTIMIZING THE PCB FOR THERMAL PERFORMANCE

To optimize the PCB's thermal performance, it is important to consider the trace layout, the thermal planes, and the thermal vias. Component spacing on the PCB and the maximum PCB power dissipation (thermal saturation) are also critical.

23.3.1 The Impact of the Trace Layout

The thermal conductivity of a material is a measure of the thermal energy that can flow through the material under an applied temperature gradient. Figure 23.2 shows a plate of material where two sides are held at different temperatures, T_1 and T_2. Experimentally, the one-dimensional thermal energy transferred through this material is found to be governed by Eq. (23.2).

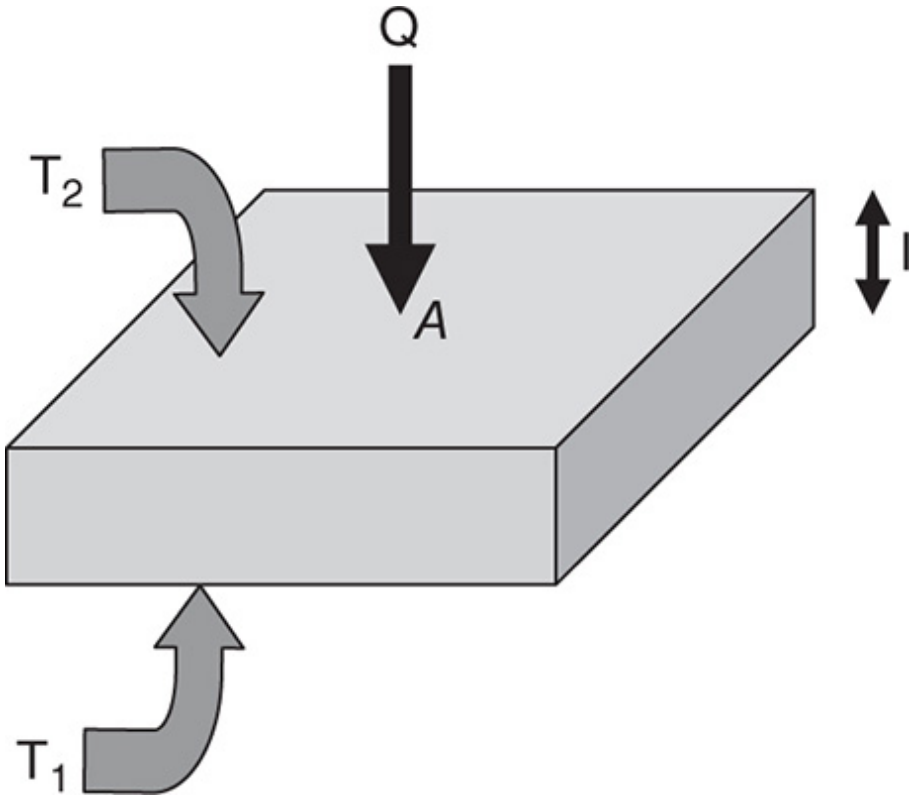


FIGURE 23.2 Typical thermal conductivity test schematic showing a block of material with area A constrained by two different temperatures, T_1 and T_2, on opposing faces. Q indicates the heat flow direction when T_2 is greater than T_1.

$$q = \frac{kA}{l}(T_1 - T_2) \qquad (23.2)$$

where q = the heat energy
A = the area of the plate
l = the thickness of the plate
k = the thermal conductivity of the material
T_1, T_2 = the applied temperatures on the plate's opposing faces

Table 23.1 lists typical thermal conductivity values important to PCB and electronic components. Where a range of material properties is given, multiple factors determine the exact thermal conductivity value. These factors can

include the filler percentage and composition in a polymer, or in the case of silicon (Si), the doping type and level. Material property measurement or vendor data should be used to determine the thermal conductivity of the specific material of interest. One alloy of Cu is shown to demonstrate that the Cu alloy composition can play a role in the thermal conductivity of metals. These material properties are valid at room temperature (~23°C). Due to the temperature-dependent nature of thermal conductivity, further references for these properties should be pursued when operation is expected at temperatures above 85°C or below −25°C.

TABLE 23.1 Typical Thermal Conductivity Values[2,3]

Material	k(W/m-°C) at 25°C
Air	0.0026
Copper (pure)	386
Copper EFTEC-64T	301
FR-4 (in-plane)	0.6–0.85
FR-4 (out-of-plane)	0.25–0.3
Solder mask material	0.15–0.5
IC encapsulant	0.6–1.0
Silicon	110–149

It is critical to note that the thermal conductivity of Cu is three orders of magnitude greater than the conductivity of most polymers such as PCBs and solder mask materials. This means the majority of the thermal energy will be conducted through the Cu, which implies that the layout of the Cu traces and power planes will be critical to the thermal performance of the PCB as a heat sink. Figure 23.3 shows this graphically. In this model, an eight-pin small- outline

integrated circuit (SOIC) package dissipating 1 W was soldered to a single-layer FR-4 PCB of 1.57 mm thickness. The temperature rise above ambient is plotted as a function of the trace length connected to the device pins. As shown, the device temperature changes by ~40 percent for this variation in trace length. The data show that to get the lowest possible temperatures, the longest possible traces should be used to spread heat away from components. Equally important, the widest possible traces should be used. These thermal design optimizations need to be made within the constraints of the electrical performance requirements such as the system time delay budget.

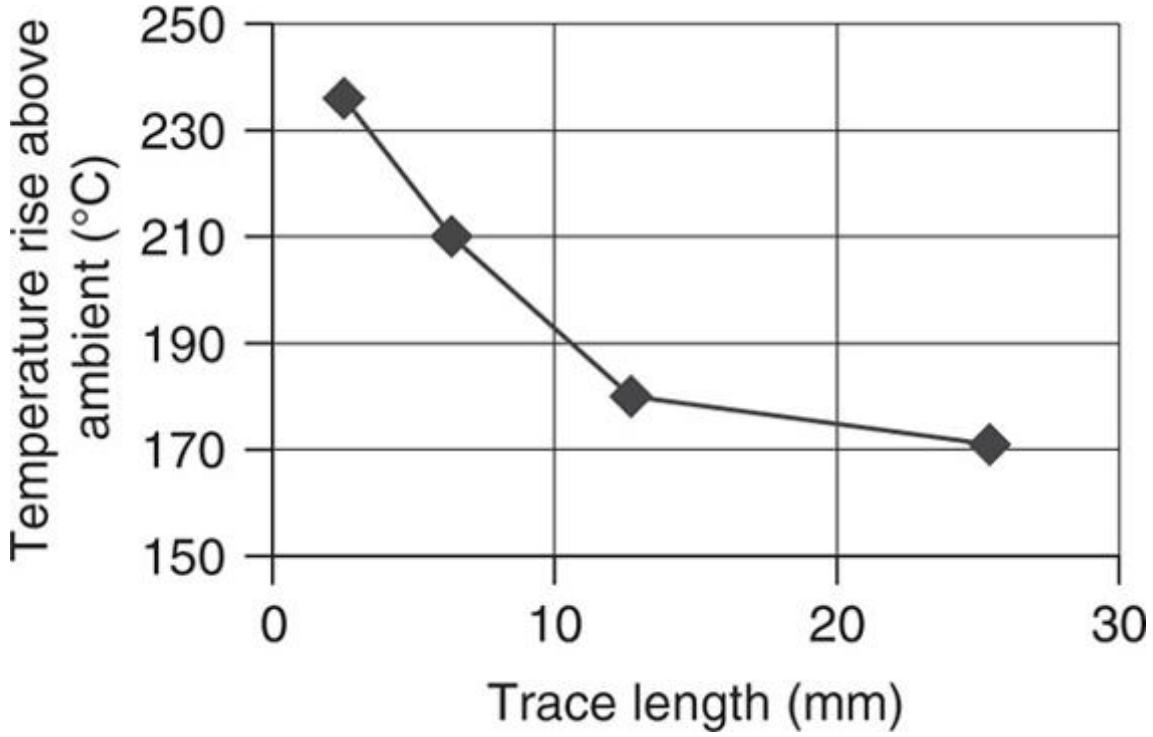


FIGURE 23.3 Modeled temperature rise above ambient thermal performance of an 8-pin SOIC powered at 1 W as a function of the trace length.

An important feature of thermal management is evident from this chart. After a trace length of about 15 mm, there was little additional improvement as the trace lengthened further—seeking thermal optimization by increasing the

trace length had reached a point of diminishing return. Often, once a specific parameter has been optimized, further changes in that parameter lead to little additional efficiency gain. Intuitively, heat flow can be thought of by analogy to fluid flow through pipes of different diameters. The pipe with the smallest diameter limits the fluid flow rate for a given fluid pressure. If the diameter of this constriction is made larger, the next smallest pipe diameter becomes the next constriction. Thermal resistance is analogous to the resistance to fluid flow in this pipe illustration. Once a thermal resistance restriction has been minimized, the thermal conduction “bottle neck” moves to a different portion of the problem.

The PCB trace thickness is another important parameter that interacts with the trace length and width. If the traces are thick, they offer less thermal resistance to heat transfer. If the traces are thin, their thermal resistance is increased and the heat will not spread as far. For best thermal performance, use the thickest possible Cu foil material with the thickest possible electroplating. Unfortunately, the trace thickness is often specified to achieve the best possible etch performance for tight pitch routing, which in turn gives the smallest PCB with the fewest signal layers and lowest cost. Within these limits, ensure that Cu traces are as thick as possible. Use them to provide direct thermal conduction paths to thermal features such as thermal vias, thermal side rails, or thermal conduction screw holes.

23.3.2 Thermal Planes

Cu planes in the PCB can provide very effective heat spreading for the electronic components. The intent is to conduct the heat over as large an area as possible in order to optimize convection and radiation heat loss from the PCB. Figure 23.4 shows a cross-sectional view of a PCB

highlighting features that make good thermal planes. These include

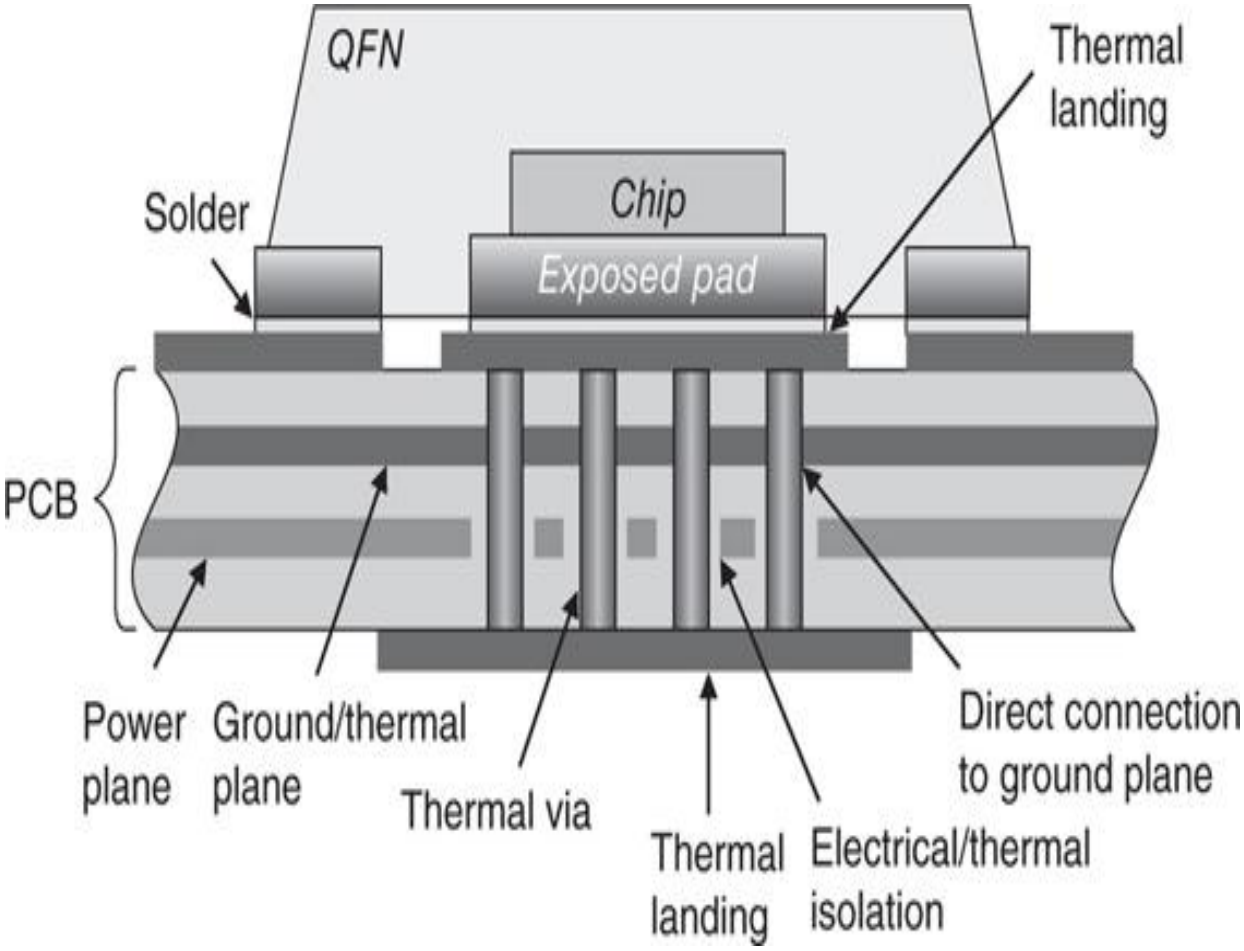


FIGURE 23.4 A typical four-layer PCB cross section showing a package with an exposed pad soldered to a thermal landing that is in turn connected to the PCB ground plane through thermal vias. The vias are isolated from the power plane for electrical reasons. In this figure, the ground plane would become the thermal spreading plane assuming it was continuous over a large area.

- A thermal landing (sometimes called a thermal collection plate) or solder land to gather the heat that the device is shedding
- Thermal vias to conduct heat from the thermal landing into a buried plane (most often either the power or ground plane)
- Continuous Cu to spread the heat

- A possible thermal landing on the bottom side of the PCB where an indirect heat sink might be attached
- Isolation areas to ensure that the thermal vias don't short all planes in the PCB

Many integrated circuit (IC) packages are optimized to "dump" power into such thermal planes in the PCB. Figure 23.5 shows images of packages with exposed pads that are intended to be soldered to thermal collection plates on the PCB. The die of these packages are glued directly to these exposed pads, giving a very low thermal resistance into the PCB. This thermal resistance can be found from vendor data sheets and might be listed as theta-*jc* (θ_{jc}), for junction to case, or as theta-*jp* (θ_{jp}), indicating junction to pad resistance. Ball grid array (BGA) packages often include thermal balls that are designed with optimized thermal conduction paths to the die inside the package. These balls should be soldered to thermal collection lands for spreading heat throughout the PCB. Often, thermal ball arrays include both power and ground balls, allowing at least two PCB planes to be used for spreading, thereby increasing the spreading efficiency of the PCB.

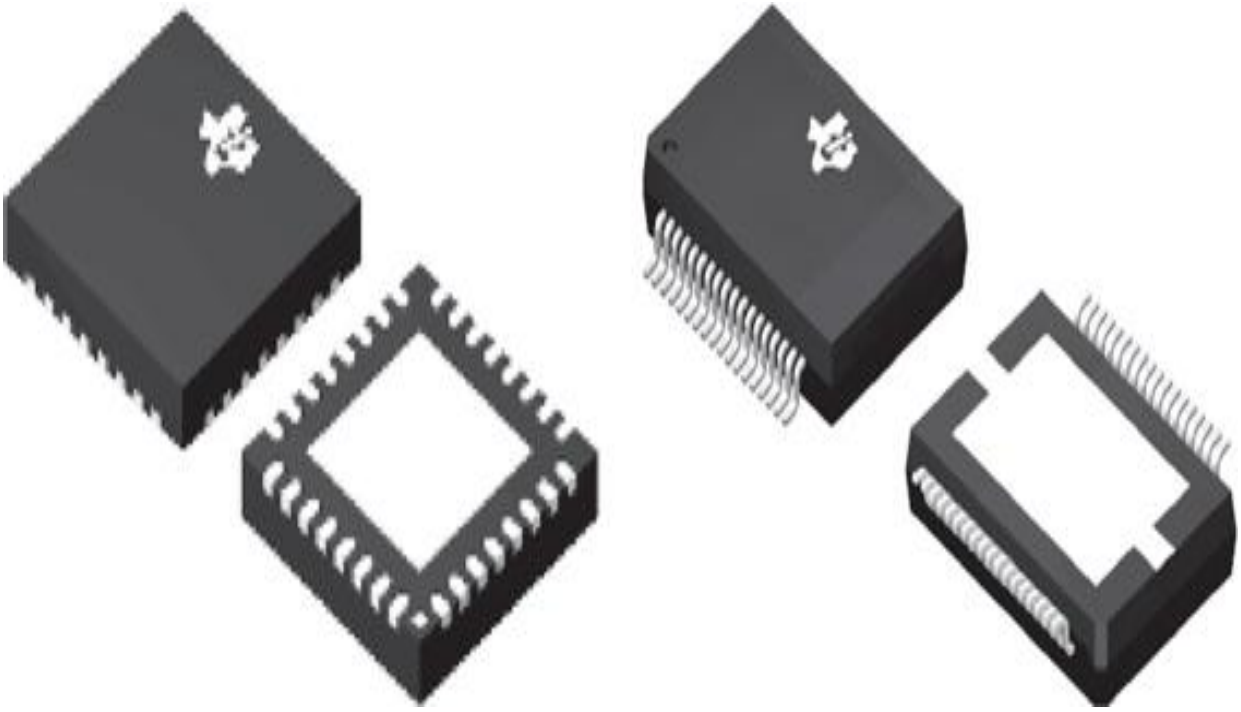


FIGURE 23.5 Two package types with exposed thermal “slugs” on the bottom of the package intended to be soldered to thermal spreading elements on the PCB.

Large thermal spreading elements that must be soldered to the PCB can sometimes present manufacturing problems. Improper control of solder paste leading to too much paste under these large thermal pads can result in “floating” the components on a pool of molten solder during reflow. When this happens, continuity yield suffers as the package tends to tilt one way or the other, lifting high side leads off their solder lands. Some users faced with this problem eliminated the solder between the exposed thermal pad and PCB, which led to high operating temperatures and severely degraded reliability in the field. The solution to the floating package problem is to optimize the solder paste volume, not to eliminate the thermal conduction path to the PCB. Always connect thermal management features of electronic components to the appropriate thermal collection pattern, which should then be connected through thermal vias into a

thermal plane. Failure to do so will result in devices not running at the expected thermal efficiencies.

Figure 23.6 shows the impact of thermal spreading plane area on the thermal performance of a 12- × 12-mm chip scale package (CSP) BGA-type package with 49 thermal balls. When the thermal plane size is small, the thermal performance is poor, whereas when the thermal plane size is large, the thermal performance improves by a factor of two or more. Often, suppliers of components with exposed thermal attach pads will also provide guidance as to the recommended size and shape of the thermal planes. It is best to ensure that the maximum plane area be close to the component; there shouldn’t be a large thermal resistance getting from the component into the plane. Maximize the area of the thermal spreading planes to maximize thermal dissipation.

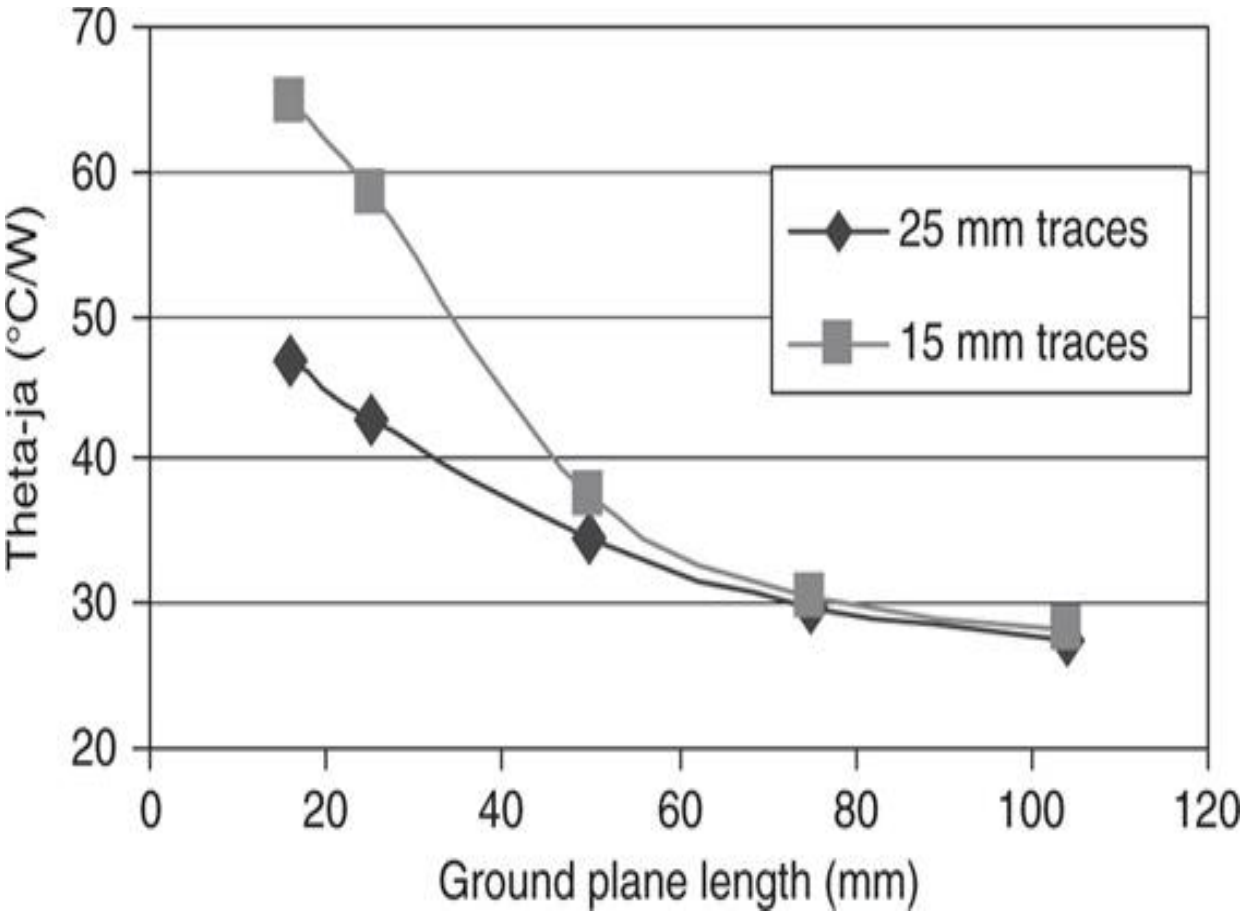


FIGURE 23.6 The effective θ_{ja} of a 12- × 12-mm chip scale package (CSP) with 49 thermal balls as a function of the (x, y) length of a continuous thermal plane under the package. Two trace lengths were assumed, showing different amounts of coupling of heat from the traces into the plane.

It is important to point out that the plane must be continuous, that is, with few or no isolation breaks in the Cu area. Since the thermal conductivity of Cu is about 1000 times higher than that of the FR-4, a 1-mm FR-4 break in a plane offers about the same thermal resistance as a 1000 mm span of Cu. A model result showing the impact of an electrical path break in a thermal plane is shown in Fig. 23.7. Here, a small 7- × 7-mm device with an exposed solder pad was intended to be cooled by a specific size of PCB area. However, due to electrical constraints, a 0.25-mm electrical noise isolation break was placed halfway down the plane to produce a quiet island. The PCB designer didn't think this

would have much impact, but thermally, it cut the plane size by half. As shown in the figure, there was a 29°C temperature drop across this single 0.25-mm break in the thermal plane and the component temperature increased by 33°C. For best thermal performance, don’t hamper thermal spreading in a thermal plane with continuous electrical isolation cuts.

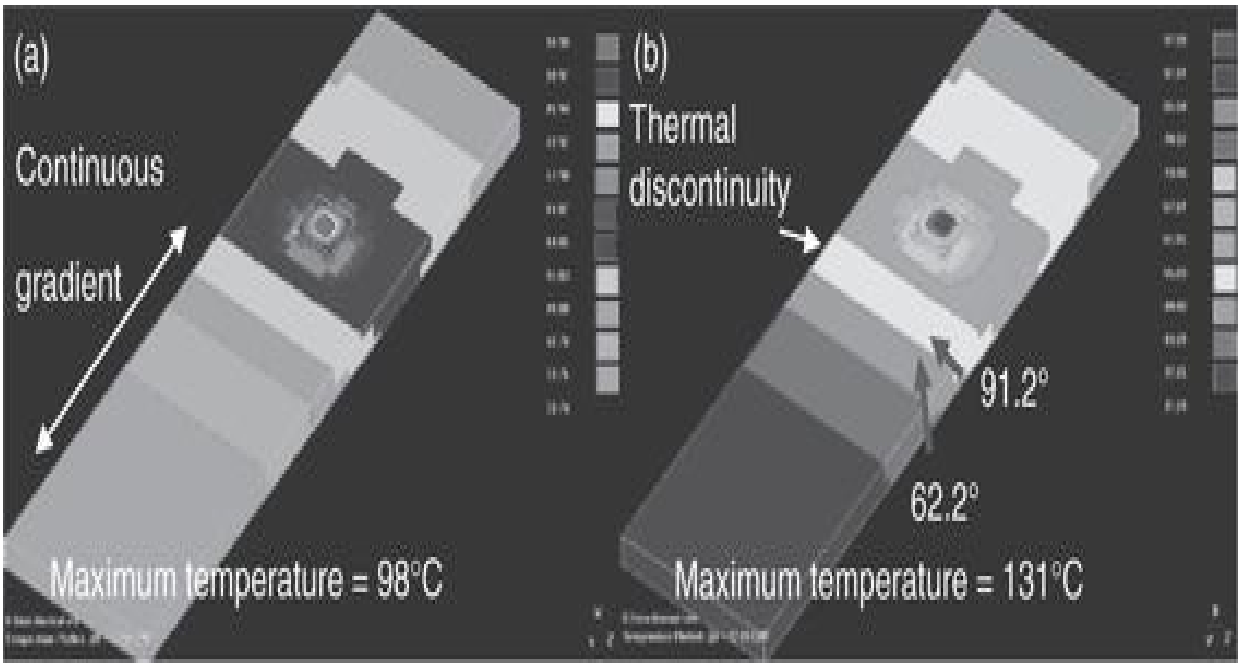


FIGURE 23.7 Thermal contours of a component on an isolated section of PCB in two configurations: (*a*) with a solid thermal plane over the section of PCB, (*b*) with a 0.25-mm electrical isolation zone in the thermal plane. The isolation zone increased the component temperature by 33°C.

Sometimes, the overall thermal performance of a PCB can be enhanced by carefully utilizing isolation cuts in the PCB to thermally segregate components that can afford to run at higher operating temperatures. For example, if a series of power regulator components can operate at junction temperatures of 150°C but are dumping so much heat into the PCB that the digital components’ maximum junction temperatures are exceeded, it might be effective to cut the thermal plane between the power regulator components and

digital portion of the PCB. This design technique will cause the temperatures of the power components to rise, but will lower the temperatures of the digital components. Of course, care must be taken to ensure the Cu connecting to the power regulation devices can carry the required current, so judicious application of this design technique is advised.

For the best spreading performance, the thickest possible Cu should be used in the construction of the thermal planes. If a thermal plane is to be 0.5 oz Cu thickness (23.8 µm), it is wise to double this plane with another thermal plane, giving an effective 1 oz layer of Cu to spread the heat over the PCB surface. Little additional advantage is gained when the thickness of all planes for spreading thermal energy is greater than 2.8 oz Cu.

23.3.3 Thermal Vias

Thermal vias are simply those that connect the thermal lands or thermal collection plates to the thermal planes. They are formed using the same processing techniques that are used for the PCB's electrical vias. However, unlike electrical vias, the primary intent of a thermal via is that it conducts thermal energy efficiently into the thermal planes. As such, a number of conditions should be met:

- There should be at least one thermal via associated with each thermal ball of a BGA package.
- The density of thermal vias under a thermal landing should be maximized within the limits of what can be allowed without degrading the PCB mechanical integrity.
- If the PCB uses through hole vias, the plating thickness should be maximized to optimize thermal conduction.
- If the PCB uses build up technology and nested vias are possible, nested vias should be used to connect to the thermal plane.

- If the PCB uses build-up technology but nested vias are not allowed, the shortest possible path between vias should be used to route the thermal energy into the spreading planes.

Figure 23.8 shows the proper way to connect thermal vias to power or ground planes. A web or spoke via connection is not recommended, as either constricts heat flow into the thermal plane. The exit side of the thermal via should have a Cu ring to anchor it to the PCB. Common thermal via dimensions for exposed pad packages are 1.0 to 1.2 mm center-to-center spacing, 0.3-mm drill diameter, with 0.025-mm Cu plating thickness or higher. Through hole thermal vias should be filled with solder, epoxy, or solder mask to avoid wicking solder from the thermal joints or thermal balls that might otherwise create an open or a reliability hazard.

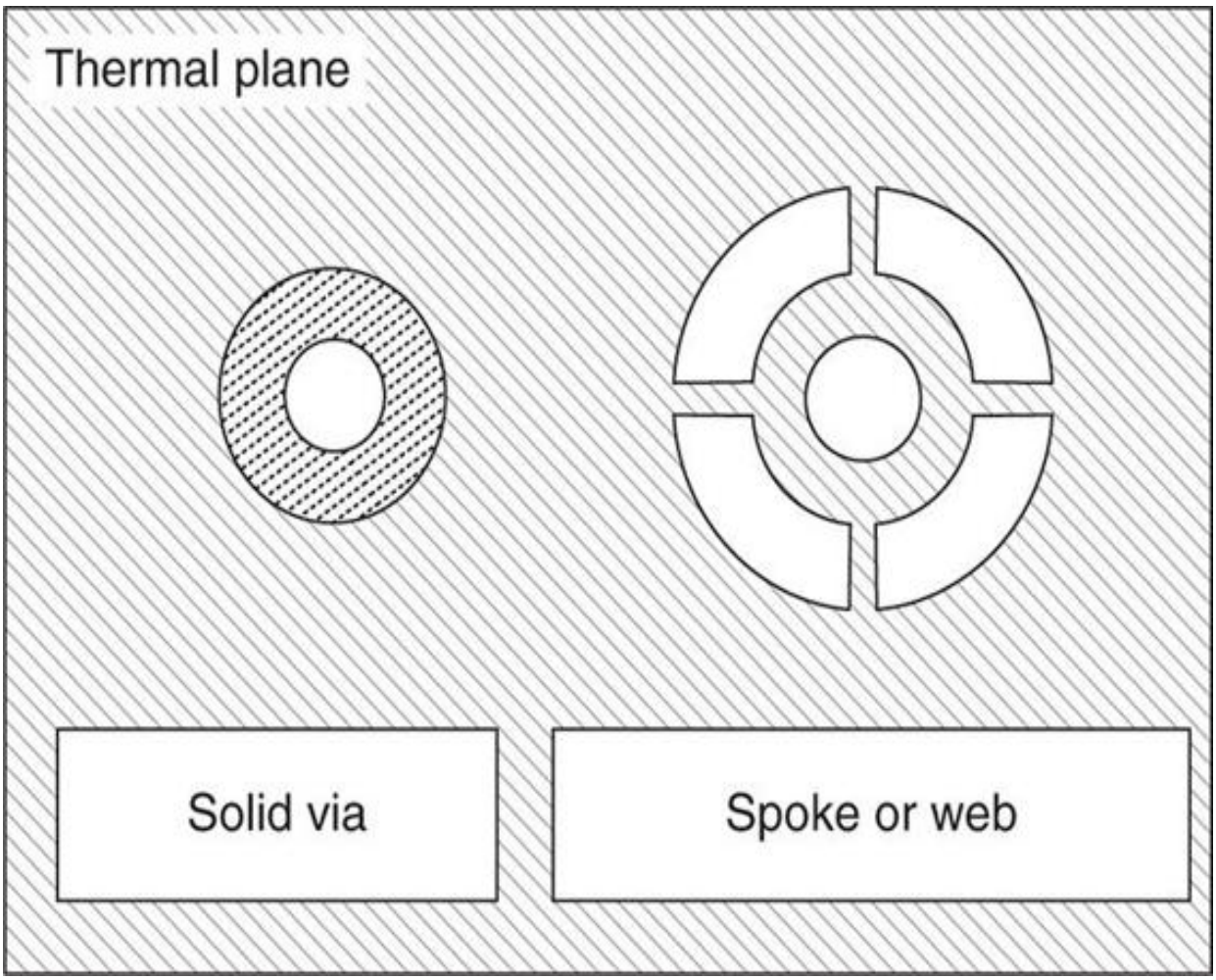


FIGURE 23.8 An illustration of two possible thermal via connections to the thermal spreading plane. The first via is a solid connection, which is recommended. The second via connection is made with a spoke or web connection to the thermal plane. This is not recommended for a thermal via.

The thermal resistance of an individual thermal via can be easily calculated from the via diameter, the via plating thickness, and the via length between the thermal land and thermal plane using Eq. (23.3).

$$\theta_{via} = \frac{l_{via}}{k * \pi * \left(\left(\frac{\text{diameter}_{via}}{2} \right) - \left(\frac{\text{diameter}_{via} - (2 * T_{plating})}{2} \right)^2 \right)} \tag{23.3}$$

where θ_{via} = the via's thermal resistance (°C/W)

k = the thermal conductivity of Cu (W/mm-°C)

diameter_{via} = the via's drill diameter (mm)

$T_{plating}$ = the Cu plating thickness in the via (mm)

l_{via} = the via's length between the thermal land and thermal spreading plane

Substituting some typical values such as a drill diameter of 0.3 mm, a plating thickness of 0.025 mm, a via length of 0.38 mm, and a thermal conductivity of 0.389 W/mm-°C, the typical thermal resistance of a thermal via is found to be 45°C/W. Since a thermal resistance is analogous to an electrical resistance, equations for calculating parallel resistance can be used to calculate the effective thermal resistance of a thermal via array. Using Eq. (23.4) below, a 4 × 4 array of vias is found to give a thermal resistance of 2.8°C/W. It is evident that the thermal performance of a component can be optimized with a relatively small number of thermal vias [see Eq. (23.4)].

$$\frac{1}{R_{\text{total}}} = \sum_{i=1}^{n} \frac{1}{R_i} \tag{23.4}$$

where R_{total} = the total resistance of the via group

R_i = the resistance of each individual via

Evaluating the thermal via resistance as a function of trace plating variability, a 0.015-mm-thick plated via with the same dimensions as the preceding will have a thermal resistance of 73°C/W. Thus, the thermal performance of a PCB is sensitive to variations in the plating thickness of its thermal vias. To ensure thermal via performance, the plating thickness in the via should be checked. This is usually performed by parallel polishing down from the surface of the

PCB rather than through a cross-sectional polishing of the via. When cross-sectioning a via, if sectioning plane does not intersect the exact center of the via, an incorrect plating thickness will be measured; this problem does not occur when parallel polishing into the depth of the PCB.

23.3.4 Component Spacing on the PCB

There is a finite spreading thermal resistance to any PCB as a function of its thickness and the number of planes in the PCB. Eq. (23.5) is a simple equation to calculate the in-plane thermal conductivity of a PCB as a function of the spreading plane thicknesses versus the FR-4 material layers. For example, if a 1.57-mm-thick FR-4 board has a single solid thermal spreading plane that is 0.036 mm thick, the effective in-plane thermal conductivity of the plane is 8.9 W/m-°C. This is substantially lower than the thermal conductivity of pure Cu, which is 386 W/m-°C. Therefore, thermal spreading through the PCB with a single plane will be worse than thermal spreading through a plate of Cu with the same thickness as the PCB.

$$k_{\text{effective}} = \frac{\sum_i k_i t_i}{\sum_i t_i} \tag{23.5}$$

where $k_{\text{effective}}$ = the PCB's effective in-plane thermal conductivity
k_i = the thermal conductivity of the ith layer
t_i = the thickness of the ith layer

The net effect of the limited spreading resistance of a PCB is that component temperatures will rise as they are clustered more tightly on a PCB of a given size and

construction. For example, Table 23.2 shows the maximum component temperature of four small devices on a 100- × 100-mm PCB containing two buried planes. As the components were moved closer to each other, the device temperatures increased from 81.6 to 98.4°C, representing an increase of 30 percent compared to the ambient temperature of 25°C. To make the best use of a PCB as a heat sink spreader, the power of individual components should be distributed as evenly as possible on the PCB to minimize hot spots.

TABLE 23.2 Case Example of Component Temperature versus PCB Spacing

Component Spacing, mm	Maximum Temperature, °C
50	81.6
25	84.4
12.5	92.9
8	98.4

The location of a component with respect to the air flow is also important. As air flows across power sources on a PCB, it picks up heat and increases in temperature. Components in the air flow downstream from high-power devices are heated by the warmer air. Air temperatures can easily rise 10 to 30°C just past a high-powered component such as a microprocessor, power amplifier, or power regulator block. If a component is running too hot, one possible solution is to move it as far upstream in the air flow as possible such that it receives the coolest air.

23.3.5 Thermal Saturation of the PCB

When the power of individual components has been evenly distributed over the PCB surface such that further geometrical rearrangement of the components or further optimization of the trace and thermal plane design is ineffective in cooling the components, thermal saturation of the PCB is said to have occurred. At this point, the power dissipation capability of the PCB becomes the factor limiting the component temperatures. The maximum power dissipation of a PCB with good thermal planes and evenly distributed power sources is in turn limited by a number of geometrical and system-level factors. These include

- The air stream velocity
- Any air ducting or shrouding around the PCB
- The configuration of heated surfaces around the PCB
- The altitude at which the PCB is operating
- The orientation of the PCB with respect to gravity

Each of these parameters impacts either the convection or radiation from the PCB. Convection is the heat transfer mechanism whereby heat is removed from the PCB through conduction of thermal energy into the gas or fluid that surrounds the PCB. In a natural convection environment, the heating of the air around the PCB causes its density to decrease. In the presence of a gravitational field, the less dense air will rise, carrying away heat with it—fresh, cool air moves in to replace the heated air. In a forced-air environment, the heated air is “blown” away from the surface by cooler air, which in turn becomes heated through the conduction of thermal energy from the PCB. The heat removed from a surface of area *A* due to convection, either natural or forced, can be represented by the simplified one-dimensional Eq. (23.6).

$$q = hA(T_{\text{surface}} - T_{\text{ambient}}) \qquad (23.6)$$

where q = heat
h = convection coefficient
A = surface area
$T_{surface}$ = the average temperature of the surface
$T_{ambient}$ = the temperature of the ambient air

Equations to calculate the convection coefficient *h* are beyond the scope of this chapter. Convection is a function of (1) the PCB size, with smaller PCBs having higher convection efficiencies; (2) the PCB orientation, with vertical PCBs being more efficient; (3) altitude, with lower altitudes being more efficient than higher altitudes; and (4) air ducting, with ducting tending to make the PCB more efficient in forced air environments.[4]

Radiation is the removal of heat from a surface by the emission, or “radiation,” of photons. These photons are generated when thermally excited atoms collide with each other, resulting in overlapping electron energy states. Since electrons are fermions, meaning no two electrons can occupy the same energy band, when the energy states of two electrons overlap during the collision, one electron is forced into a higher, empty energy state. This reduces the momentum of the colliding atoms, ensuring that energy is conserved. After collision, the displaced electron decays back to its initial energy state, giving up a photon of energy in the process. At the surface of the object, this photon is emitted, carrying away some of the thermal energy, while in the bulk of the material, this photon is reabsorbed by neighboring atoms. The simplified one-dimensional equation that describes the total energy loss from a surface due to radiation is shown in Eq. (23.7). This equation for radiation neglects heat that the PCB might reabsorb from heated objects such as power supplies around it, but does include an ambient temperature radiation reabsorption.

$$q = \varepsilon \sigma A(T^4_{\text{surface}} - T^4_{\text{ambient}}) \tag{23.7}$$

where q = heat

ε = the emissivity of the surface

σ = the Stefan-Botzmann constant (5.67×10^{-8} W/m^2-K^4)

T_{surface} = the PCB surface temperature

T_{ambient} = the ambient temperature

The emissivity of the object is a unitless number that describes how efficiently a surface radiates. It varies from 0, which is a surface with no radiation that is perfectly reflective, to 1, which is a perfectly radiative and absorptive black surface. The emissivity of the surface is a function of both the type of material that composes the surface as well as the roughness of the surface. Typical solder mask material has an emissivity ranging from 0.85 to 0.95. Typical exposed Cu trace has an emissivity ranging from 0.1 to 0.3 depending on the roughness and oxidation condition of the Cu.

It is important to note that the area of the PCB plays a major role in both of these equations. This is intuitive; the larger the PCB, the more heat it can dissipate. In combination, the preceding equations can be used to estimate the power that a given PCB at a given temperature can dissipate. For example, Fig. 23.9 shows the best-case power that can be dissipated by a series of PCBs ranging in size from 10 × 10 cm to 20 × 20 cm. The PCBs were assumed to be oriented horizontally in an unobstructed natural convection environment of 25°C with no significant neighboring radiating surfaces. Convection was allowed to vary as a function of temperature. Most importantly, the power was assumed to be uniformly distributed over the PCB such that there were no thermal gradients on the PCB. This is a major assumption, meaning that the power dissipation figures in the chart are best-case, a condition that no

practical PCB will attain. The chart indicates that 50 W can't realistically be dissipated in natural convection from a PCB that is 10 × 10 cm, but it can be dissipated by the 15 × 15 and 20 × 20 cm PCB. The 15 × 15 cm PCB will rise 80°C above the ambient to dissipate 50 W, while the 20 × 20 cm PCB will rise only 50°C to dissipate the same power. This graph has been formatted to look the same as typical heat sink curves that are available from many vendors.

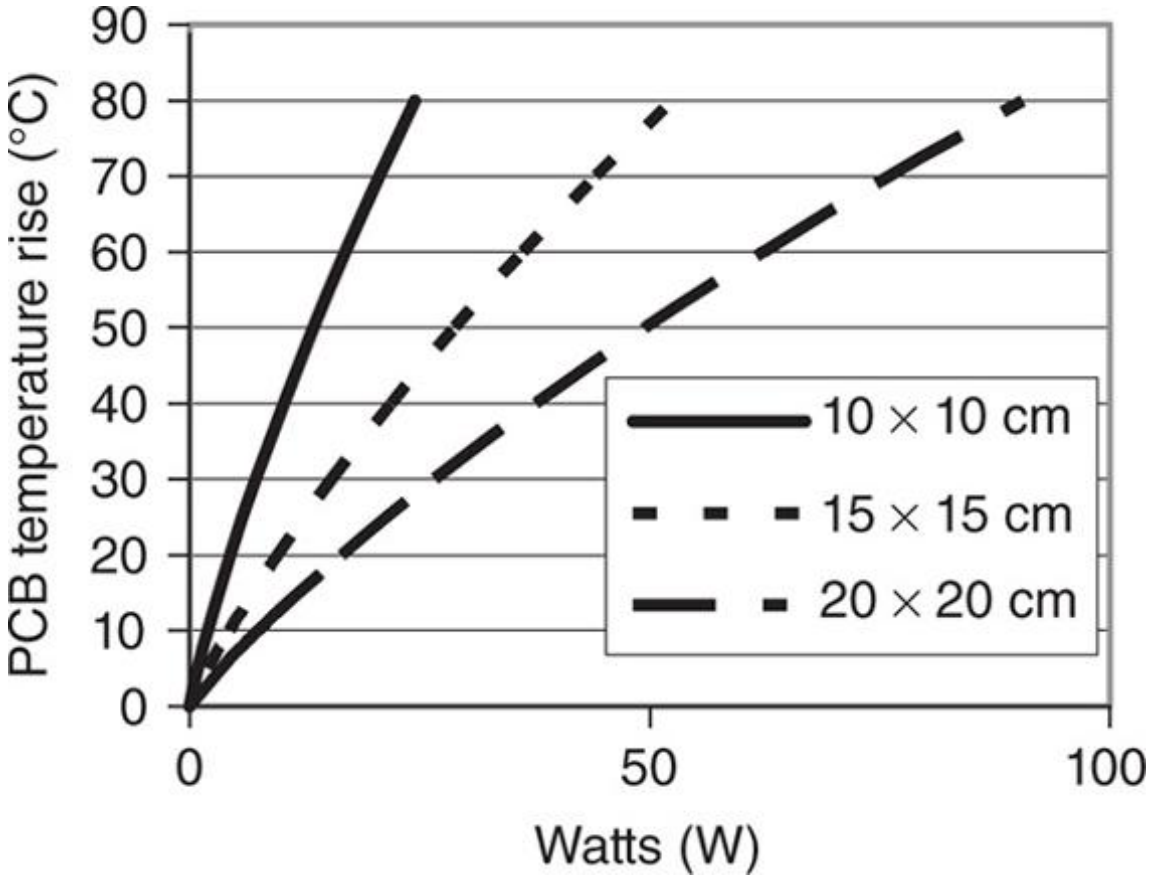


FIGURE 23.9 Temperature rise above 25°C of a horizontal PCB in natural convection as a function of PCB size and power dissipation. Both convection and radiation are dissipating the power.

23.4 CONDUCTING HEAT TO THE CHASSIS

When the PCB is thermally saturated and the component temperatures are still too high to be tolerated at the maximum obtainable system air velocity, other means of conducting heat from the PCB to even larger area system structures are required. The chassis of the system is often the largest surface area structure in the system, is exposed to the ambient air, and often makes a good sink for heat that cannot be dissipated by the PCB alone. Mechanisms to conduct heat into the chassis include chassis screws, gap fillers, connectors, and side rails. Sometimes, radio frequency (RF) shields that are appropriately connected to components can provide additional heat sinking.

23.4.1 Chassis Screws

A properly designed chassis screw thermal sink connection in a PCB includes connection to the thermal spreading plane of the PCB, through hole plating, and a thermal contact area for the screw and stand-off sleeve to clamp onto. This configuration is shown in Fig. 23.10. The thermal screw should be as close to the hot electronic component as possible to minimize thermal resistance into the chassis. As well, the chassis where the thermal screw attaches should have a high thermal conductivity to spread the heat away from the screw. Preferably, the chassis should be made of metal. If a plastic chassis is used, molding a plate of aluminum (Al) into the plastic will improve its thermal heat spreading capability. A plastic chassis alone is usually a poor thermal spreader and may not provide substantial thermal performance enhancement.

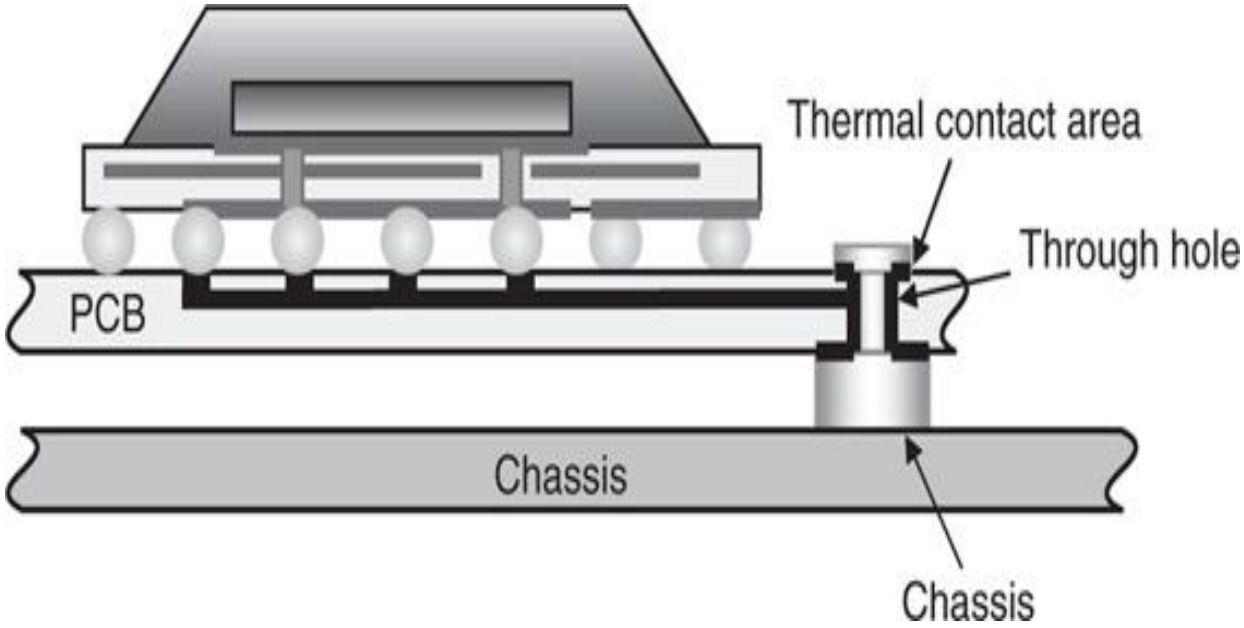


FIGURE 23.10 Schematic of a chassis screw implementation for sinking heat to the chassis. The thermal screw mounts through a plated through via that is shorted to the thermal plane as shown. The thermal plane conducts heat from the thermal balls of the PBGA package.

How much improvement might be expected from using the chassis of an enclosure for cooling? This depends substantially on the enclosure construction and the location of the chassis screw with respect to the hot component. In one example, a device was cooled with a thermal screw that connected between a hard drive PCB and the hard drive enclosure. Connecting the device thermally to the hard disk drive resulted in a 10 percent thermal enhancement.

23.4.2 Gap Fillers

It is sometimes not possible to use screws for conducting heat to the chassis. In other cases, large areas of high-power density might need to be sunk into the chassis. In these instances, another type of thermal conduction path is available that lends itself to conducting heat to the chassis: gap fillers. Gap fillers are thermal compounds that fill the gap between the PCB and chassis whose sole purpose is to

conduct heat to the chassis. There are many different types of gap fillers. The most common is a soft, flexible silicone rubber material that has been filled with thermally conducting particles to enhance its bulk thermal conductivity. Sometimes, thermally filled foams are used. When the soft, compliant material is compressed between the PCB and chassis, it conforms to the protruding components on the PCB, making a good thermal connection. Important criteria to consider in selecting elastomeric gap fill materials are the thickness needed, the thermal conductivity required, and the pliancy of the material. A variety of materials with varying compositions are readily available on the market. There is normally a trade-off between the pliancy of the material and the thermal conductivity, with higher thermal conductivity materials exhibiting less compliancy.

Plastic sacks filled with a thermal fluid are sometimes used as gap filler materials. The fluid is usually optimized to produce convection in the gap of interest. The convection in the fluid can give an effective thermal conductivity that is substantially higher than the conductivity of the fluid alone.

23.4.3 Connectors

Connectors can either provide a direct or indirect means of conducting heat from the PCB. Direct conduction occurs in those system configurations where the PCB is plugged into an edge connector or back plane socket, or is held in place with an edge guide. To take advantage of these direct connect thermal features, it is necessary to extend thermal planes into the areas where the connection or clamping occurs. The connector, clamping, or edge guide should have as large a contact area as possible to optimize thermal conduction of heat from the low thermal conductivity PCB material. In some military applications, the PCB is built

around a thick Cu core that is clamped by the edge rail of the card cage. The thick Cu core provides very effective thermal conduction from the PCB into the edge rail, which is then cooled by a system of channels containing either moving air or moving water.

Indirect conduction of heat from the PCB can occur when cables are plugged into connectors on the PCB. These indirect conduction paths are much harder to include accurately in system-level thermal analyses, but can provide some margin in a PCB thermal design. Care must be taken, however, to ensure that these plug-in cables don’t block critical airflow paths that would lead to overheating.

23.4.4 RF Shields

RF shields are used over sensitive RF and analog circuits to minimize electrical interference with the circuit function or to minimize electrical radiation from the circuit into the surrounding environment. RF shields are usually made of a thin metal which is soldered to ground on the PCB. In most instances, the RF shield is a continuous plate or box that encloses the circuits. Unfortunately, this continuous box creates a dead zone in the air flow directly above the components within the box, degrading natural convection for those components. To enhance the thermal performance of components within RF shields, perforations or meshing of the RF shield cage is recommended. If these perforations are kept less than 1/10 the wave-length of the shielded electromagnetic radiation, the RF shield will function adequately to quiet the circuit and block out extraneous signals while allowing air flow through the shield to cool the interior components.

If additional steps are taken, the shield can be used to spread heat from hot components inside the shield over a larger section of the PCB, thereby maximizing convection

and radiation cooling for the heated components. Figure 23.11 shows a schematic of a shield over a stacked package component. It is normally difficult to conduct heat from the top device in such a stack to the PCB, but when the RF shield is brought into contact with the top device, heat can conduct into the shield and down to the PCB. It is suggested that the thermal connection between the shield and the electrical components be made with a thermal epoxy or thermal grease after the shield is soldered in place to avoid issues with mechanical tolerances or interference between the shield and the components. If the high-powered components to be cooled reside immediately outside the shield, it is possible to conduct heat from them into the shield such that the shield behaves as a heat sink.

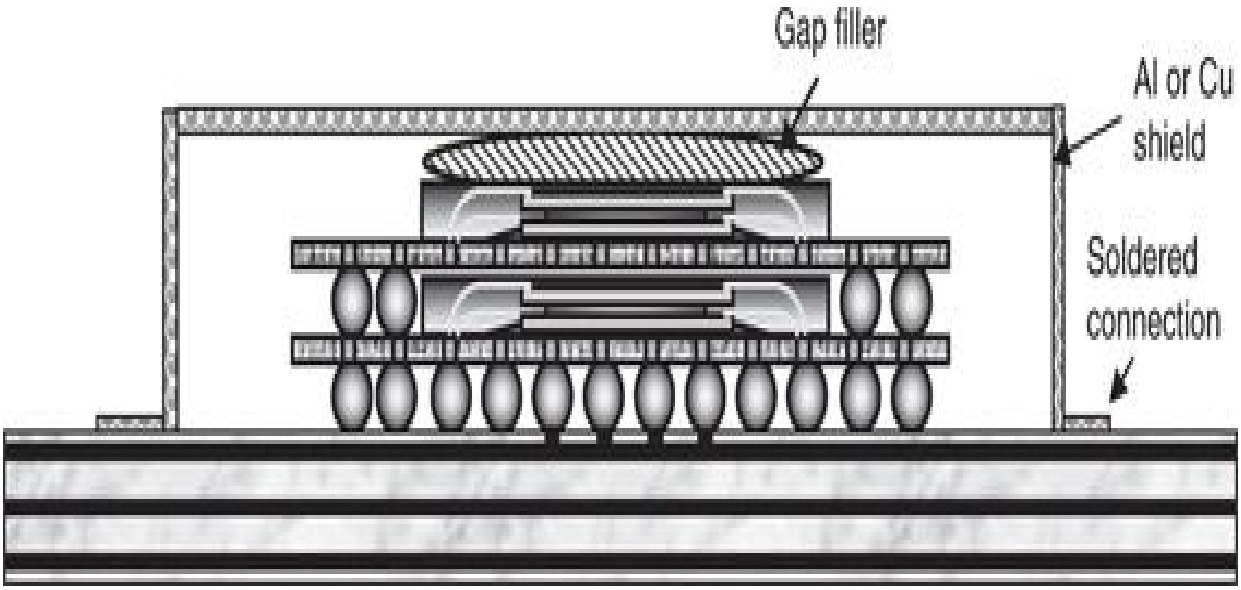


FIGURE 23.11 A stacked package configuration on a PCB with a perforated RF shield that is being used to spread heat from the top package. Thermal gap filler material such as thermal grease is used to conduct the heat from the top package into the RF shield.

23.5 PCB REQUIREMENTS FOR HIGH-POWER HEAT SINK ATTACH

Most IC components with power dissipations of 2.5 W or higher require attached heat sinks to dissipate the power. These heat sinks are often glued or clamped to the components with few special constraints placed on the PCB. If a large number of components requiring heat sinks are placed on the PCB, it is important that the PCB be thick enough to handle the weight of the attached heat sinks, especially if the system environment subjects it to vibration or mechanical shock. High-powered components in the 50 to 300 W range require special PCB design features to handle the high-loading force of the heat sink against the electronic component. Clamping forces of 20 to 200 lb are possible for these high-power heat sinks in order to get the best possible thermal contact between the heat sinks and components. One such high-power heat sink configuration is shown in Fig. 23.12.[5] Here, the heat sink is spring loaded against the package with tensioned screws which tighten into a bolster plate. The bolster plate provides the rigidity needed to avoid bending and damaging the PCB under the spring loading. A mylar film between the bolster plate and PCB minimizes electrical shorting of the fixture to the PCB. For such heat sink constructions to work, no components can be placed between the PCB and bolster plate.

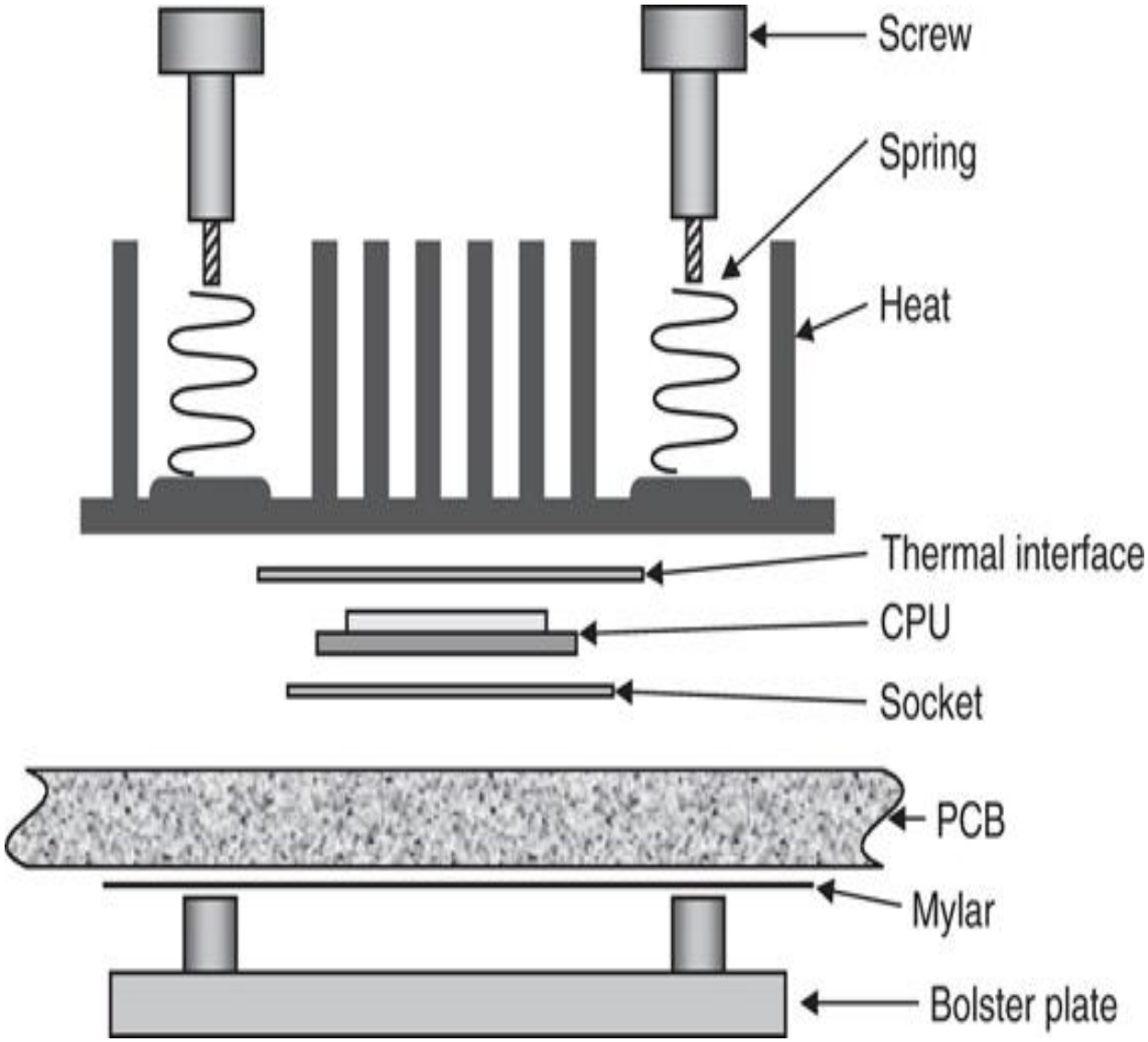


FIGURE 23.12 Cross section of a mechanical design for a high-power heat sink clamped on a microprocessor. The bolster plate on the bottom of the PCB minimizes PCB warpage and breakage.

23.6 MODELING THE THERMAL PERFORMANCE OF THE PCB

Each of the many PCB thermal optimization techniques described in this chapter will have some amount of impact on the thermal performance of the system. Determining the relative impact of a single optimization is difficult to perform

analytically. When an entire ensemble of optimization techniques is employed across multiple devices operating at a variety of powers, analytical solutions of the thermal problem become impossible. The simplicity of system-level temperature calculations implied by Eq. (23.1) is misleading unless the effective θ_{ja} of each component in the specific system is known a priori. Since the impact of the PCB design on the thermal performance of the system must be determined before design completion and tooling, the question becomes how to quantify the impact of the PCB thermal features. Relayout and redesign of the PCB to fix thermal issues once tooling is generated is prohibitively expensive and leads to noncompetitive design cycle times. The only predictive method currently available that addresses this need is computer simulation, which can incorporate all relevant PCB design features, perform a thermal analysis, and report back the component temperatures to identify problem locations.

Many commercial computer simulation tools exist, ranging in complexity, accuracy, and cost. Computational fluid dynamics (CFD) programs incorporate equations that solve the problems of air flow around the PCB, thermal conduction from the PCB into the air, and thermal conduction within the PCB. Solutions using CFD don’t require special knowledge of convection coefficient equations, thereby making the modeling process easier and less prone to convection coefficient calculation errors. Accuracy of CFD analysis can be as high as ±5 percent. CFD codes tend to be slow, however, taking substantial computer resources to run a reasonably complex model. A step down from CFD are codes that employ user supplied convection coefficients that are applied to the PCB and component surfaces. These solutions can be quite accurate, though no more than ±10 percent precision can be projected without substantial correlation to experimental data.

Whichever analysis code is selected, it should be capable of reading in data from the user's PCB layout tool and should be capable of incorporating the specific thermal conduction paths that were optimized for component performance. It should be able to handle relatively complex system-level structures and should be capable of inputting a variety of thermal characteristics of the components. Postprocessing identification of PCB regions and components above limit temperatures is a plus. The code should run fast enough to enable multiple design iterations to optimize the PCB layout without slowing down the design cycle.

23.6.1 System-Level Thermal Modeling Phases

System-level thermal analysis normally includes three phases due to the complexity of the task and the difficulty of inputting a fully detailed system design into a tool. The first phase concentrates on airflow optimization through the system to minimize any dead zones in the cabinet. The PCBs, cables, fans, and other air blockages are included in the analysis during this phase. The second phase includes dissipation of power on the PCB by applying power areas to the PCB. During this phase, it is fairly easy to change locations of power sources to optimize the air cooling paths. The final phase is the fully detailed phase, which includes the PCB layout geometries and details of the electrical components. By the time phase three is reached, there should be few remaining major iterations for thermal optimization.

During each phase of thermal modeling, the solids of the components, PCB, and system enclosure must be defined to the code. These solids are meshed by the code, a process through which the objects are broken into tens of thousands of discrete nodal points. The computer calculates thermal

parameters such as temperature and heat flow at each of these nodal points as a function of neighboring nodal points rather than trying to solve analytical equations for the thermal fields. If the meshing is fine enough, the calculated solution will be very accurate. If the meshing is too coarse, errors will creep into the model. There is a trade-off between accuracy and run time in computer simulations; models with coarser meshes usually run much faster than models with fine meshes. It is best for users to become familiar with the mesh sensitivity of their chosen modeling tool to optimize run time versus accuracy before running critical analyses.

When performing a CFD system-level analysis to determine temperatures on a PCB, it is important to include all airflow obstructions that might change the convection on the PCB and its components. Common airflow obstructions include cables, RF shields, daughter cards, brackets, air filters, capacitors, transformers, memory single in-line modules (SIMs), power regulators, and hard drives. Failure to include these air blockages in the modeling process can result in systems that run too hot or that suffer from thermal shutdown. External blockages should be accounted for as well. Cabinet vents should not be located where a user might carelessly toss a magazine or CD cover. The impact of accumulated dust over the lifetime of the system should also be considered, as the dust can substantially reduce convection.

From a PCB layout standpoint, the highest velocity air stream on the board may well occur between two tall components if they block the airflow path. The blockage causes the air to be channeled through the gap, resulting in higher air velocities. High-power electronic components can sometimes be more effectively cooled by placing them in this channeled air stream. Locations to avoid for high-power components are the leeward side of air blockages, immediately downstream of high-power components, or on the bottom center of a natural convection-cooled PCB.

23.6.2 Required Component Thermal Parameters

Thermal models of a PCB loaded with detailed models of components in a system can become very complex with many nodes. Such analyses can run for days and weeks, making them impractical. As well, it is often impossible to get detailed models of each component to be used in a system. To address these issues, the industry has developed two levels of component thermal abstraction. The first method reduces the electrical component's thermal behavior to two thermal resistances, θ_{jc}, which represents the thermal resistance from the active portion of the component to the top component surface, and theta-*jb* (θ_{jb}), which represents the thermal resistance between the active portion of the component to a point on the PCB at the edge of the component. The component is then represented to the system as shown in Fig. 23.13. The thermal resistance from the top of the component to the ambient, R*a*, is calculated either through CFD or from the convection coefficients. It also includes radiation heat losses. Thermal conduction through the PCB to other components and to the air is calculated by the simulation tool. Accuracy of a two-resistor component thermal model temperature delta with respect to the ambient is in the ±20 percent range, even when using CFD. The parameters θ_{jc} and θ_{jb} are usually available in the component supplier's data sheets. If not, the supplier should be contacted for the information.

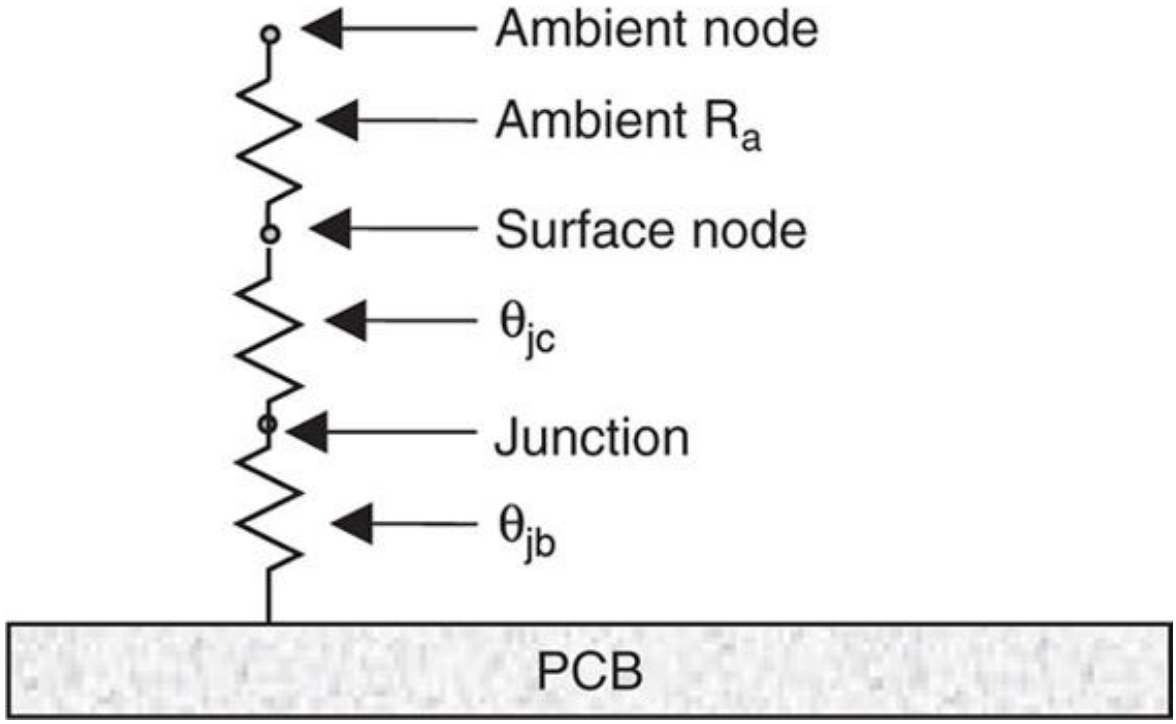


FIGURE 23.13 Thermal conduction representation of an electrical component by two thermal resistances, θ_{jc} and θ_{jb}. The resistance to ambient (R_a) is the result of convective and radiative heat loss.

A more complex modeling configuration has been developed to improve thermal estimations from ±20 percent to ±5 percent. Called a *compact model*, these resistor network topologies better represent heat flow within the package and from one side of the package to another. Compact models should therefore be used whenever they are available. Often, the system design engineer must ask the component supplier for them since they are not commonly printed in data sheets. Many tools allow the user to mix compact component models with the simpler two-resistor models.[6]

23.6.3 Handling Cu Traces and Power Planes

Due to the complexity of meshing the fine geometries of a PCB trace layout, many if not most modeling tools include the ability to “smear” Cu layers into solid sheets. A smeared layer is a single sheet whose average thermal conductivity is equivalent to the thermal conductivity of the detailed trace layer. Unfortunately, most tools use an incorrect averaging technique to determine the effective thermal conductivity of a layer. The tool asks for the percent Cu coverage in the trace layer. Based on this input, the tool then calculates the thermal conductivity of the trace layer as the weighted average between the Cu conductivity and the insulator conductivity. For example, if a 100 percent coverage of Cu layer has a thermal conductivity of 380 W/m-°C, a 95 percent coverage of Cu would have an effective conductivity of 360 W/m-°C, and a 0 percent Cu coverage layer would have a conductivity of 0.8 W/m-°C. Smearing in this fashion neglects critically important details such as isolation regions that might cut through thermal spreading planes. Therefore, trace smearing using a conductivity averaging scheme should be avoided.

If the modeling tool can’t represent the PCB in full complexity, some attempt should be made to perform a better estimation of the thermal conductivity in Cu spreading layers connected to critical components. The overall smeared thermal conductivity of the plate should be replaced with patches of thermal conductivity that account for heat flowing either parallel or perpendicular to the Cu conductors. Equations (23.8) and (23.9) can be used to estimate parallel and series thermal conductivities in Cu layers respectively. Figure 23.14 shows graphically what is meant by a parallel thermal conductivity. Here, multiple stripes of thermally conductive materials pass thermal energy from the top to bottom. Each material channel can be considered as a thermal resistor. The thermal resistance of each resistor can be calculated as a function of its cross-sectional area (thickness × width) and thermal conductivity,

and the effective parallel resistance can be backed out [Eq. (23.8)].

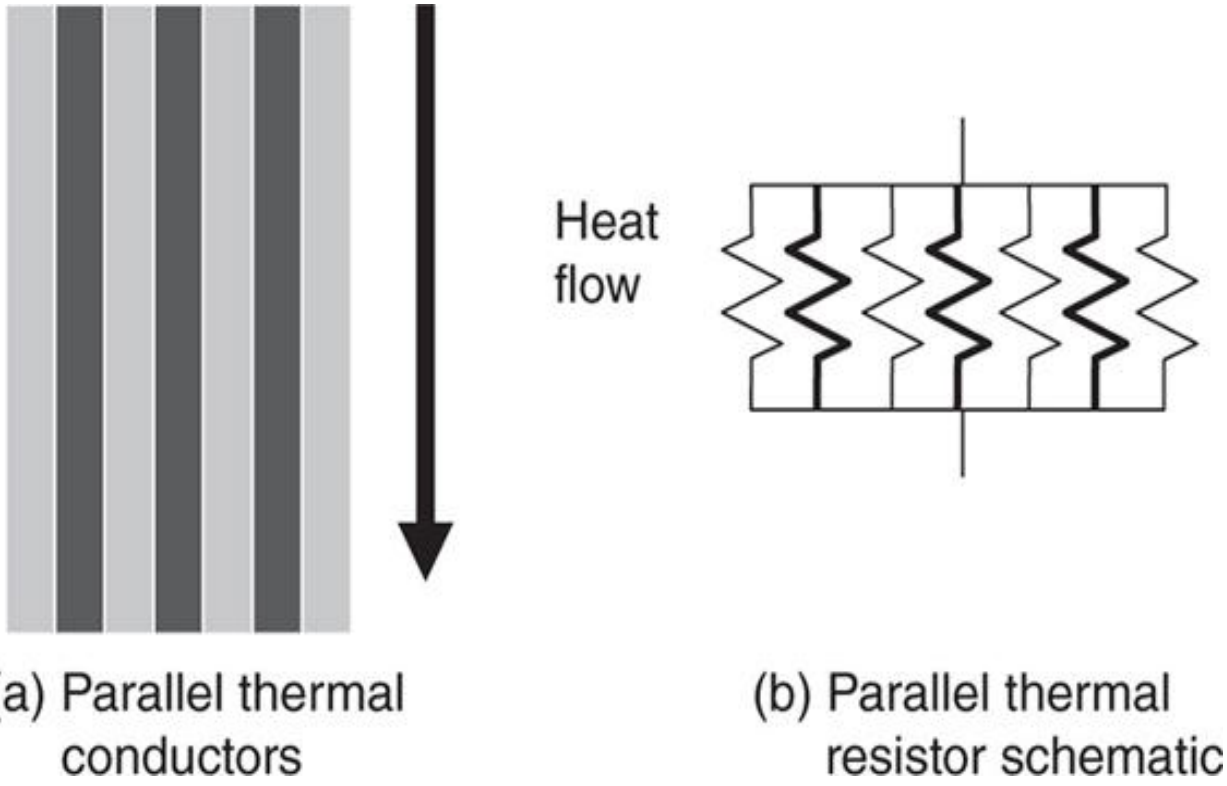


FIGURE 23.14 A diagram to illustrate how heat flowing along parallel conductors can be represented through electrical analogy to electrical resistors in parallel. The parallel resistance representation is used in the derivation of Eq. (23.8).

$$k_{\text{parallel}} = \frac{\sum_i k_i \cdot \text{Area}_i}{\sum_i \text{Area}_i} \tag{23.8}$$

where k_{parallel} = the effective thermal conductivity of a plate where the heat flows parallel to the conductors
k_i = the thermal conductivity of the ith material
area_i = the area of the ith material (thickness of stripe × width of strip)

In the case of series thermal resistances, the dimension of interest is the length of each section of material in the direction of the heat flow [see Eq. (23.9) and Fig. 23.14].

$$k_{series} = \frac{\sum_i \text{Length}_i}{\sum_i \frac{\text{Length}_i}{k_i}} \tag{23.9}$$

where k_{series} = the effective thermal conductivity of a plate where the heat flows perpendicular to the conductors

k_i = the thermal conductivity of the ith material

length_i = the length of the ith stripe parallel to the heat flow path

23.7 HEAT SOURCES

When performing any thermal analysis one must consider all the sources of energy into a system and how all the energy leaves the system. Thermal management of printed circuit assemblies (PCAs) involves assessing all the energy inputs and outputs. Components are the most common energy input. Although, traces and planes, connectors and sometimes energy input from other PCAs require consideration when evaluating a given design.

Many components need to be evaluated at both steady state and transient conditions. JEDEC standards address many of the conditions necessary to evaluate the heat transfer from the component junction-to-board in air environments. Unfortunately, this is not performed for components in a vacuum environments. The component junction-to-case thermal resistance is considered valid, more or less for vacuum environments, but the case-to-board thermal resistance is negatively impacted in vacuum compared to air environments. Conduction through the leads can be a large thermal resistance and must be evaluated on a component-by-component basis. In most cases, the

radiation losses between the component and board are assumed negligible.

Traces and planes can be a challenge to evaluate. Traces require more attention now than ever due to higher density designs and the introduction of IPC-2152, Standard for Determining Current Carrying Capacity in Printed Circuits. IPC-2152 introduced new conductor sizing charts that are used by PCB designers to size electrical conductors in printed circuit boards (PCBs). Many companies have not changed their design practices as a process from when they used the conductor sizing charts last published in IPC-2221.

Chapter 22 includes a history behind the IPC-2221 charts. It also discusses the difference that is observed between the IPC-2221 charts and new charts published in IPC-2152. One reason that electronics have not had heating issues as a result of trace heating is that the old charts used for sizing internal conductors was not only conservative, but it was not based on trace heating data. See Chap. 22 for further discussion. Circuit Board Designers, Electrical Engineers, Mechanical/Thermal Engineers and Managers should be required to understand these topics.

23.8 ACKNOWLEDGMENT

This chapter was edited from the original written by Darvin Edwards of Texas Instruments, Dallas, Texas, for *Printed Circuits Handbook*, 6th ed. (Clyde F. Coombs, Jr., ed.), McGraw-Hill, New York, 2008.

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CHAPTER 24

EMBEDDED COMPONENTS[a]

Vern Solberg
Solberg Technical Consulting, Saratoga, California

24.1 INTRODUCTION

Historically, electrical components have been mounted on the outside of printed circuit boards (PCBs), either with through hole leads or with terminations all on a single side (surface mount) with the interconnection traces embedded inside the board. Technology, however, has been developed to embed electrical components inside the board also. The earliest component to be embedded were resistors, which are made by etching a pattern on a sheet of resistive material and then connecting them with the rest of the circuit through the standard multilayer process. In addition, capacitors are formed from thin dielectric material between closely spaced copper-foil planes, and inductor elements are formed by etching coils of the copper conductive foil during innerlayer manufacture. These fabrication techniques have expanded to include the ability to “place” very thin and small outline discrete passive components inside the board.

This allows the normal multilayer board pressing operation to encapsulate these placed components.

24.2 DEFINITIONS AND EXAMPLE

Components. The following are the electrical units that make up all electrical devices.

Passive components. These components––including resistors, capacitors, or inductors—influence electrical flow in a circuit, but do not cause a gain in current or voltage.

Active components. In contrast, these components can provide gain in an electronic circuit.

Integrated passive arrays. Multiple passive devices may be packaged in either a leaded or surface-mount technology (SMT) package or sometimes in arrays of all the same value. *Integrated passive component* is a general term for multiple passive components that share a substrate and packaging. Most typically, integrated passives are on the surface of a separate substrate that is then placed in an enclosure and surface-mounted on the primary interconnect substrate, in which case they are called *passive arrays* or *passive networks*. This chapter discusses only embedded components.

24.3 APPLICATIONS AND TRADE-OFFS

Embedding components are not appropriate for all electronic packaging. A board designer must consider several factors when deciding whether to use embedded components or not. Use of discrete components, whether on the surface or placed inside the board, involves incremental costs in that

the more components that are used, the higher the cost. However, the trade-off is that the cost of fabricating one formed embedded component is about the same as that of forming an entire layer of those components. Another factor to consider is that surface-mount components can have the same size and shape for widely differing electrical values. Formed embedded components on a single layer are larger and can increase electrical value. Widely differing electrical values may require more than one layer of embedded formed material.

24.3.1 Advantages

Advantages from embedding components inside the board include

Reduction in board area (enabler). Reduction in surface area results in more circuits per fabrication panel. Reduction in board size can yield a smaller board for the same functions, as components are now inside the board.

Increase in functionality, higher density (enabler). The surface area is the same, but some other function can be added. For example, the designer can increase cell phone capability by adding a Bluetooth connection to the ear piece receiver.

Improvement in performance (enabler). Higher speeds, shorter paths, and lower noise are possible. For example, cell phones can be enhanced with built-in digital cameras or even video cameras.

Improvement in total assembled costs. System cost is key; the higher board price is often offset by a lower bill-of-materials purchased for the system, as fewer standard components are needed.

24.3.2 Disadvantages

Disadvantages of embedding components include

- Quality can be affected; in particular, meeting tolerances can be more difficult.
- Trimming embedded resistors is slow and expensive.
- The design is “parametric” where designer sizes components.
- Technology implementation does not give all values needed.
- Some capacitance values are not obtainable commercially (>100 nF/cm^2).
- Manufacturers of sheet resistor materials make only one decade of values.
- The cost of prototypes can be high.
- Resistors cost the same whether one or thousands are made per layer.
- Test tools are lacking.
- Test voltages may cause dielectric breakdown.
- Charge-up time for capacitors may limit test speed.
- Rework is not possible inside the board.
- Additional capital investment is required.

24.3.3 Principles of Cost Trade-Off

The circuit design tools identify the resistors and capacitors that must be added to make an electronic circuit functional. The tools simulate circuit operation and “size” the resistors and capacitors as appropriate. Whether a resistor is purchased and mounted on the board surface or formed inside the board from a layer of resistive material has little effect on the electrical operation of a circuit. Therefore, if

many resistors can be formed inside the board from the same series of chemical steps, the inclusion of perhaps thousands of internal resistors costs no more than adding one internal formed resistor. The critical economic analysis is to find the cost of adding internal formed resistors and then dividing by the number that can be used internally to see whether embedded resistors inside the board make sense.

24.4 DESIGNING FOR EMBEDDED COMPONENT APPLICATIONS

24.4.1 Resistors

Resistors were the first component to be embedded in a multilayer board, making it a truly three-dimensional interconnection and circuit system. While early designs were custom for each application, over time design standards and “best practices” have been developed, which allow for successful inclusion of resistors, and other components, without the need to start from the beginning. The following discussion provides these for resistors, with subsequent. Sections providing similar information for other components.

24.4.1.1 Resistor Terminology. The designer must size embedded formed passive resistors. This is in contrast to the “library selection” of conventionally manufactured resistors that are selected from a table of available components. The principle of embedded resistors is given by the following formula for a term ohms per square; this means that any square area defined in the material will have the same resistance and that by grouping squares appropriately, the designer can define the resulting resistance.

Resistance in any resistor is determined by Eq. (24.1):

$$R = \rho L/A \qquad (24.1)$$

where R = resistance in ohms
ρ = resistivity
L = length of the resistor
A = cross-sectional area (resistor thickness times resistor width)

Note: Resistivity (ρ) is a material property. It is a constant at a given temperature and expressed in resistance units (ohms) for area and length. For example, the resistivity of copper is $\rho = 7.09\ e^{-7}\ \Omega\ in^2/in$.

Sheet resistance (R) is a commonly used term to describe raw materials used in embedded formed resistors. These materials are manufactured in sheet form with a constant thickness, giving a uniform R value for any square resistor. Therefore, the material is specified by its sheet resistance value, given in ohms/square (Ω/). Resistance of a specific resistor is simply designed by changing the ratio of length to width. For example, 100 Ω material forms a 100-Ω resistor in any square configuration while a resistor element that is three squares long by one square wide would be 300 Ω, as illustrated in Fig. 24.1. On the other hand, a resistor element that is two squares wide by one square long would provide a 50-Ω resistor element.

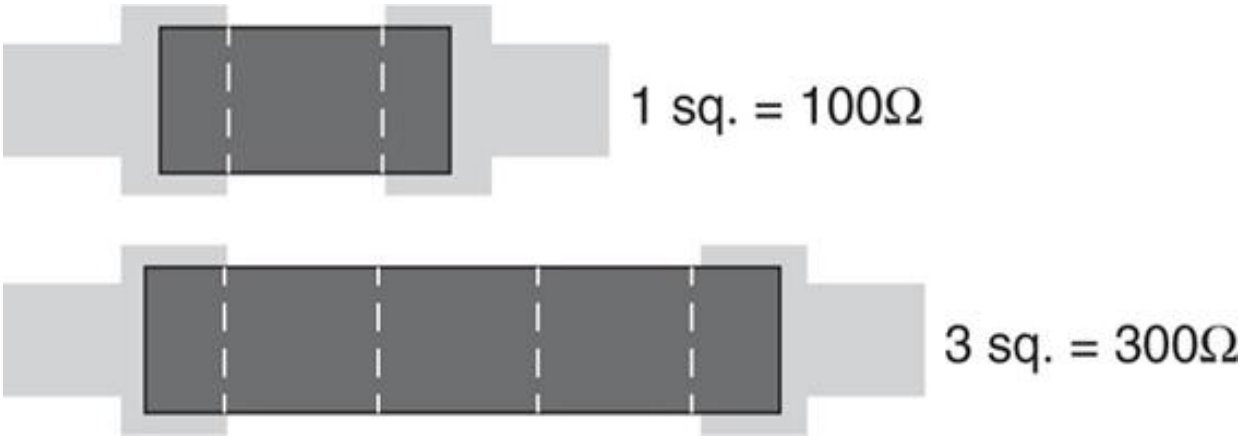


FIGURE 24.1 Printed resistor elements using 100-Ω ink or paste material.

24.4.1.2 Resistor Design Parameters. The circuit board designer is responsible for sizing the resistor to give the appropriate value. Material suppliers have given their sizing parameters to computer-aided design (CAD) software companies for entry in their component libraries. Additionally, the manufacturing tolerances for each supplier product have been communicated to computer-aided manufacturing (CAM) suppliers. Figure 24.2 gives typical design parameters for sizing both the active embedded formed resistor area and the termination pads for the traditional copper innerlayer upon which the resistor is built.

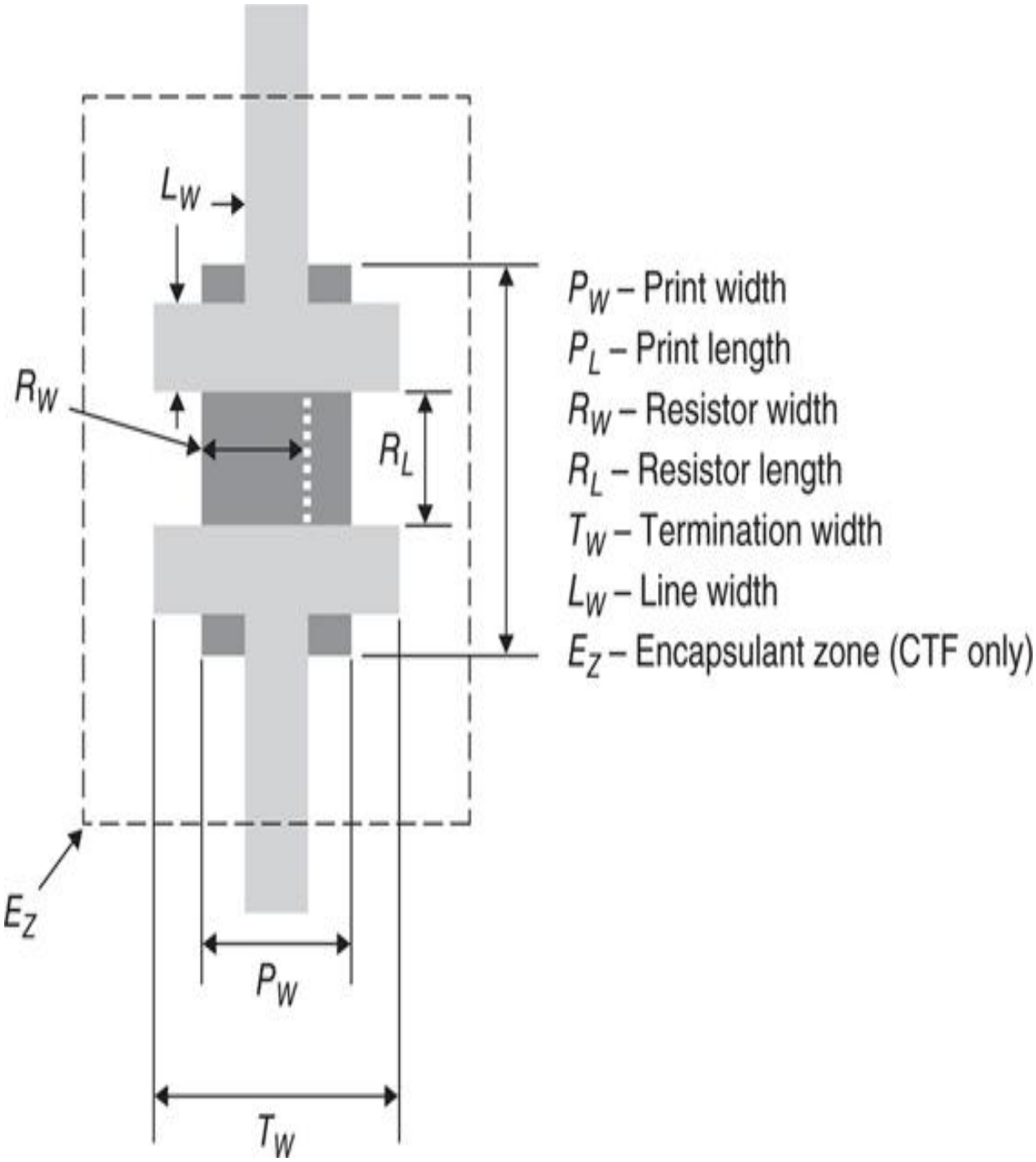


FIGURE 24.2 Resistor terminations.

24.4.1.3 Serpentine Resistor Design. The examples previously furnished exhibit very basic value geometry requirements. To maximize the number of resistor elements on the circuit layer and achieve greater utilization of the

process, alternative techniques can be considered. By adjusting the geometry of the resistor element, the designer is able to create a relativity wide range of values. The serpentine resistor example shown in Fig. 24.3 demonstrates the flexibility in designing resistor elements requiring more complex values.

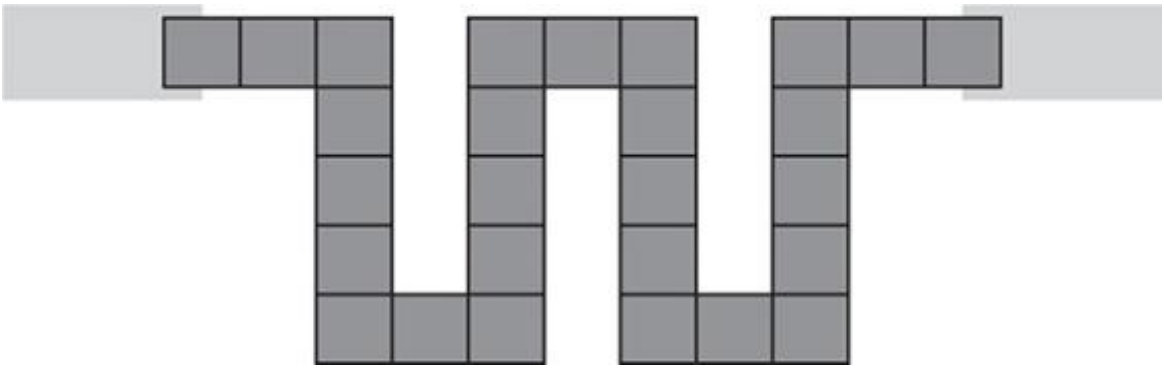


FIGURE 24.3 Printed serpentine resistor element.

A serpentine resistor value can be calculated as a bar resistor (1.0R value per square) with the exception of the corner squares (right-angle bends). Due to the change in current density at right-angle paths, the effective value number of the corner square is 0.56R.

24.4.2 Capacitor Design

All production formed capacitors use laminate-like materials. Most typically, the capacitor manufacturer starts with an especially flat copper foil on at least one side. This copper foil is precisely coated with the dielectric material: filled polymer. Either the top foil electrode is then laminated or two layers of coated foil are bonded polymer to polymer.

24.4.2.1 Capacitor Terminology. Capacitors are electrical elements that store charge on parallel electrode plates. They are not batteries that operate chemically.

Capacitors store more charge with closer parallel electrode plates. The higher the dielectric constant between the plates the more charge is stored. The value of embedded capacitors will be defined by dielectric area as well as dielectric thickness. The Eq. (24.2) will aid the designer in calculating formed capacitor values.

$$C = A \times D_k \times K/t \tag{24.2}$$

where C is the value of the capacitor, A is the area of the formed planar capacitor $L \times W$ D_k is the dielectric constant of the capacitor material t is the thickness between the capacitor plates K is a conversion constant = 8.854×10^{-14} farads/cm.

24.4.2.2 Capacitor Design Parameters. Similar design tolerance for capacitor design parameters (compared to resistors in Sec. 24.4.1) is available for capacitors, as shown in Fig. 24.4.

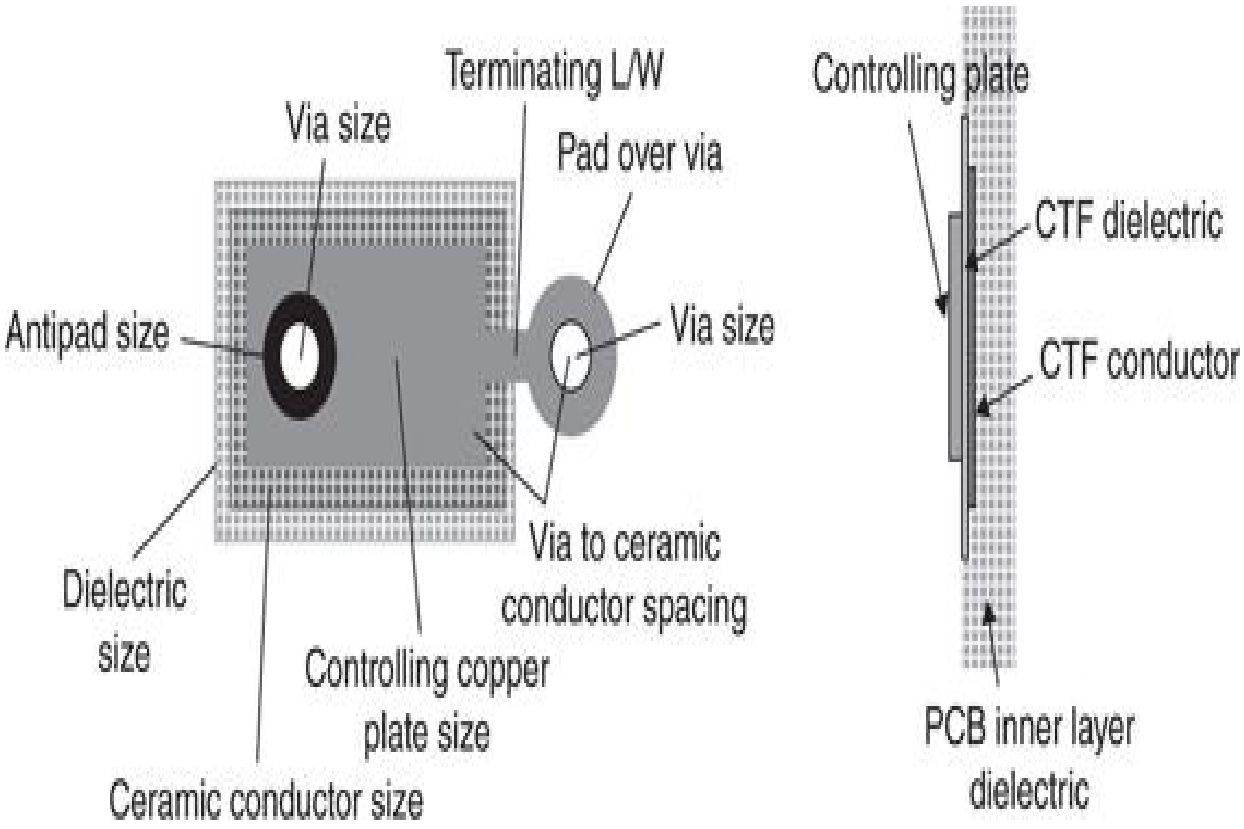


FIGURE 24.4 Capacitor design features.

Even conventional epoxy glass laminate has some capacitance value, and the oldest formed embedded capacitors were carefully controlled using thin conventional glass/epoxy laminate layers. Both epoxy resin and E-glass have dielectric constants of about 4 D_k, not a particularly large value. Eliminating the glass and adding compounds such as barium-titanate to the epoxy or polyimide resin, however, dielectric constants can be expanded into the 10 to 20 D_k range. When higher capacitance values are needed, dielectric containing ceramic or inorganic compositions must be adopted. More advanced technologies demonstrate dielectric constants in the 100 to 2000 D_k range to enable the forming of larger value capacitors inside the circuit board layer system. These larger capacitors are useful for decoupling, one of the primary uses of capacitors.

Thickness is the divisor in the capacitance formula. The thinner dielectric layer between copper planes will yield a higher device capacitance value. Early formed embedded distributed capacitors simply used the readily available 100-micron (4-mil) epoxy/glass innerlayer construction, common in multilayer circuit boards. Then, thinner woven glass allowed 50-micron glass/epoxy layers, doubling the device capacitance. Finally, polymer only or barium-titanate-filled polymer enabled further reduction of the dielectric layer thicknesses (as thin as 8 microns). This improved dielectric provides 6 to 20 times higher capacitance value of the original 100-micron epoxy glass. Because of the special fabrication and handling required for manufacturing the thinner dielectric material, there is increased cost. A cost/benefit analysis will help illustrate the trade-offs between common dielectric material and the more premium materials. Key factors the designers must weigh are overall cost against the area gained using the smaller-size-for-higher-capacitance values of the filled polymers.

24.4.3 Inductors

Inductors use the magnetic effects of electrons traveling in wires to influence the travel speed of other electrical signals. Typically inductors are a coil configuration. No special material technology has been demonstrated for inductors. These spirals of copper circuitry are typically formed similarly to the copper-conductive traces of innerlayers. Formed inductors are current loops configured to induce a magnetic field for storing and controlling inductive energy. Inductance (measured in henry) is an effect that results from the magnetic field that forms around a current carrying conductor. Current flowing through the inductor creates a magnetic field that has an associated electromotive-field that opposes the applied voltage. This counter

electromotive-force (emf) generated opposes the change in voltage applied to the inductor and current in the inductor resists the change but does rise. This is known as *inductive reactance*. It is opposite in phase to capacitive reactance. Routing the circuit conductor into a spiral creates a larger magnetic field that can increase inductance.

The energy (measured in joules, in SI) is stored by an inductor is equal to the amount of energy required to establish the current flowing through the inductor, and therefore the magnetic field. This is given by the following equation:

$$E_{\text{stored}} = \frac{1}{2} LI^2$$

where L is inductance and I is the current flowing through the inductor.

A combination of line width, number of turns, shape and conductor length define the inductance value. A spiral inductor can be formed on a single layer for simple low value applications (Fig. 24.5) or by employing two or more circuit layers for the more complex requirements.

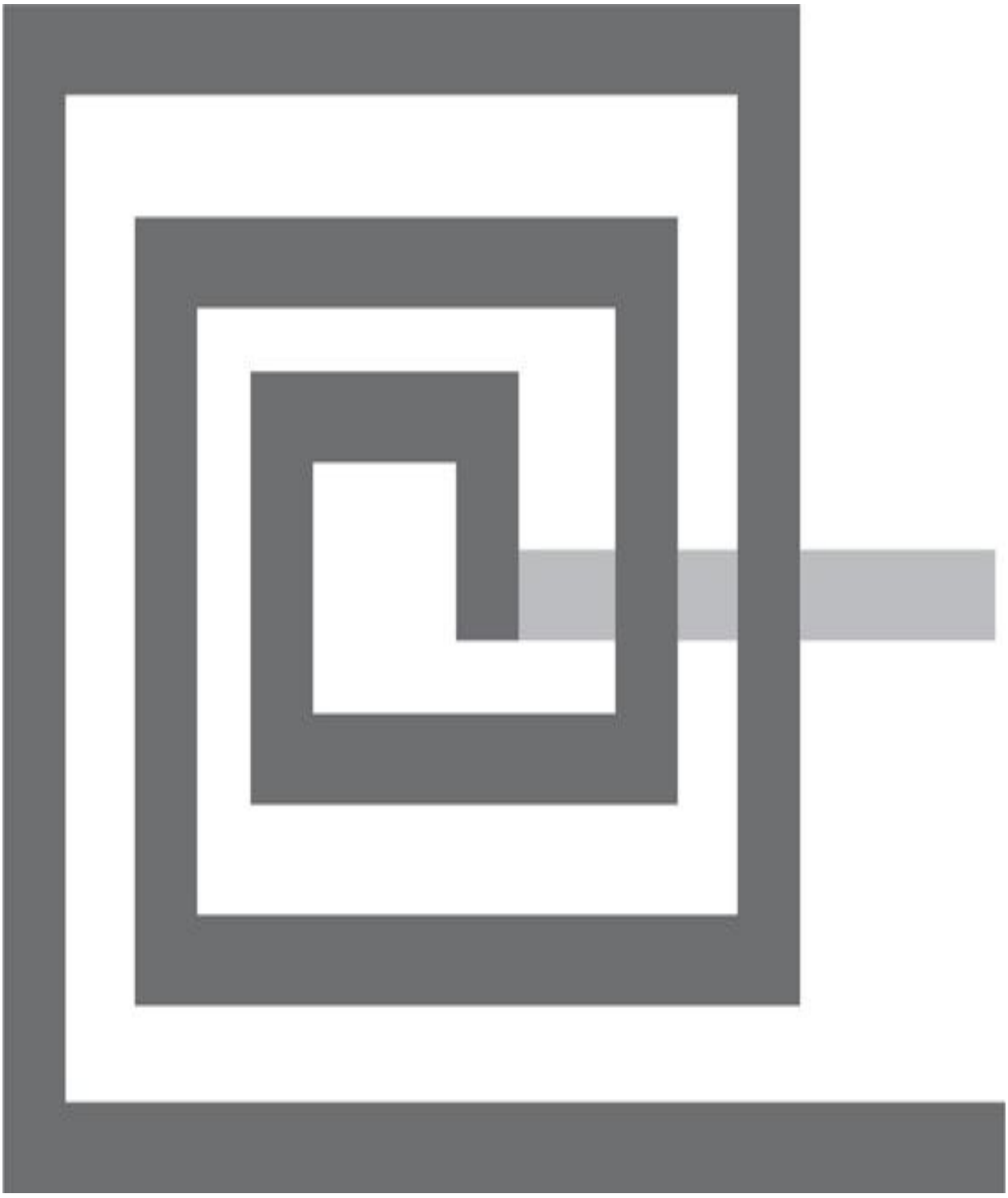


FIGURE 24.5 Printed or etched spiral inductor element.

Software tools are available to refine the inductor pattern development process. Spiral inductor layout traditionally relied on approximate quasi-static models and verification

using electromagnetic field solvers. Software developers have created interface tools for high-performance EM simulation. The software also enables optimization of the inductor as well as facilitating the design of spiral circuit components.

24.5 MATERIALS

24.5.1 Resistor Materials

Resistors, discrete or formed, are actually very poor electrical conductors when compared to copper. Their function is to restrict the flow of electricity in a circuit. Common compositions of resistors include metal oxides, carbon particles, or small conductive particles separated widely by an organic polymer. Conventionally, the value of a resistor is rated in ohms, with higher values restricting more current. Also, resistors are sized by tolerance in percentage, allowable maximum current, and parameters that deal with the electrical frequency of operation.

Material suppliers have designated the range of resistance values that are optimum for their material. The designer determines the length and width that is allowable in the design, and then determines which material to specify for manufacture so that the final resistor value is achieved in the allocated circuit board space.

Formed embedded resistors of similar values are designed on one specific layer so that the maximum economic value is achieved for that layer.

Materials are also available that can combine mixed values of resistance on one layer. Polymer thick films (PTF) are applied by successive screen print/cure cycles so that all the desired resistance values can be made on one layer. Also, some sheet capacitance manufacturers laminate a layer of

resistor foil as one electrode in their construction. Therefore, a fabricator can mix resistance and capacitance on one sheet type raw material.

24.5.2 Resistor Fabrication Details

Several different raw materials and processing systems are used to fabricate embedded resistors. The most commonly used are listed in this section.

24.5.2.1 Photoprint. Photoprint involves a supplier coating a thin, resistive layer on a copper-foil sheet and selling this to either a laminate supplier or directly to the board fabrication shop. The fabricator uses two imaging and etching steps: the first to image the copper conductors on the layer, and the second to size individual resistors by using a second, different etchant solution, specifically for the resistor composition. Typically, alkaline etchants are used in step one, and acidic etchants are used in step two.

24.5.2.2 Screen or Stencil Print. Screen or stencil print is the operation of adding specific resistive paste compositions directly to the etched innerlayer. Polymer compositions (PTF) are cured directly at normal board exposure temperatures (150 to 200°C). Ceramic compositions cure at much higher temperatures (900°C), so the sequence of manufacturing operations is changed. Copper foil first has the uncured ceramic paste screened. Then firing of the paste occurs in a nitrogen blanketed oven. The foil, with cured ceramic resistors, is laminated to B stage epoxy, and the epoxy layer cured to C stage with resistors pressed into the resin. Finally, the innerlayer copper traces are etched, exposing the embedded ceramic resistors.

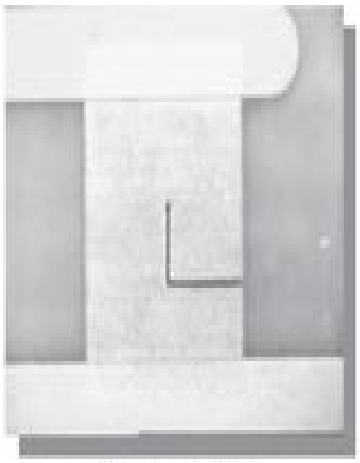
24.5.2.3 Plating. Plating is an additive process where the copper layer is first etched. Then the layer is catalyzed for electroless plating, and photoresist is applied. Resistor

locations are imaged into the resist and the pattern developed. Exposed catalyst in the proper areas then initiates plating of the resistors. The resist is stripped, background catalyst is removed, and the resistors are in the proper locations.

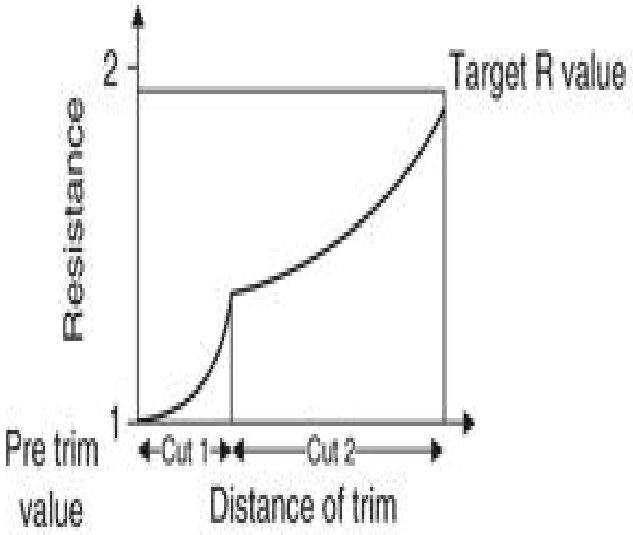
24.5.2.4 Inkjet Printing. Inkjet printing is the additive process of applying appropriate resistor materials (usually PTF-type compositions) directly to etched innerlayers. Resistors are applied one at a time, in contrast to the mass screening of conventional PTF. It is also possible to print several resistor value compositions before a final single cure step.

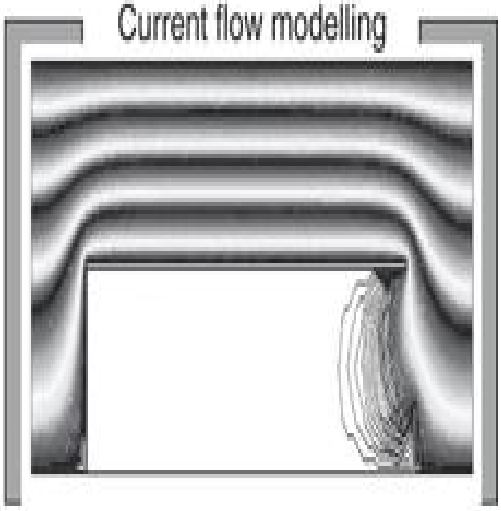
24.5.2.5 Photoimageable Discrete. In a photoimageable discrete process, resistive compositions have been dispersed in traditional solder mask–like materials, which are applied to the surface of an etched layer. Imaging and development leave the desired geometry resistor after the development step.

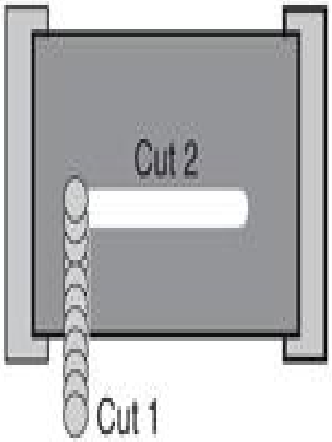
24.5.2.6 Resistor Trimming. Resistor trimming is a necessary step. All of the resistors given here have been shown trimmable to very precise values. This is normally done in with a modified laser machine, adapted from trimming ceramic surface mount discrete resistors. Either the machine uses a probe card pattern to measure the values of a number of resistors at one time or it uses a flying probe technology from electrical test to measure and trim a single resistors. The flying probe system is used in hybrid circuit manufacture and the probe card system is standard for arrays of resistors from discrete component suppliers. An interpretation of the laser trim process is shown in Fig. 24.6.



Finished trim
(Material courtesy McDermid)







Pulsed laser machining

FIGURE 24.6 Resistor trimming.

24.5.3 Capacitor Fabrication

Formed capacitors can be planar or discrete. Capacitance value is achieved using materials of different dielectric constants and different dielectric thicknesses. The planar capacitor simply sandwiches a dielectric material between two layers of copper foil typical of that illustrated in Fig. 24.7.

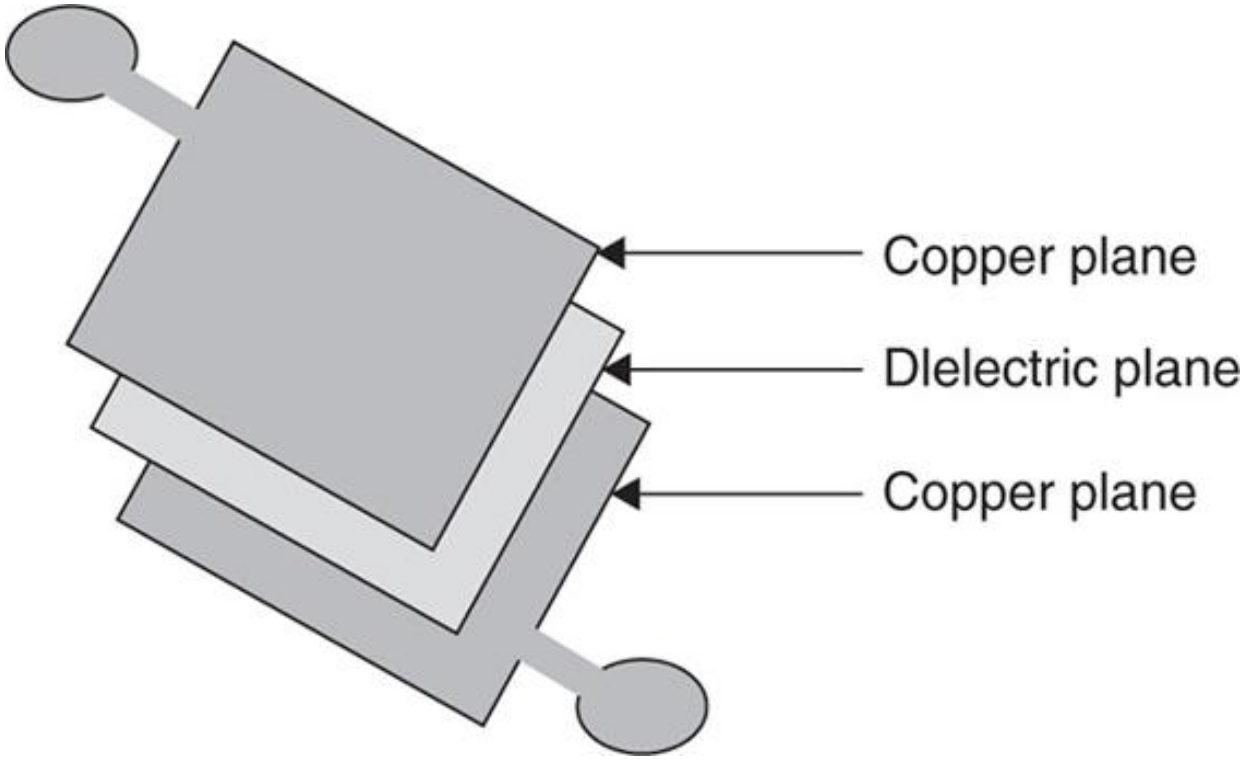


FIGURE 24.7 Planar capacitor.

The dielectric layer may be a common organic composite, polyimide, an organic polymer thick film or ceramic thin film (CTF) composite. The polymer thick film or ceramic thin film (CTF) composite dielectrics can be applied for both discrete and planar capacitors. The PTF material density is equal to 20 pF/mm^2 while CTF materials will have a density rating of approximately 24 nF/mm^2.

The most common commercially available capacitor technology is a laminate structure that relies on a thin glass reinforced epoxy composite that is furnished with copper foil on both sides. Companies are also supplying a barium titanate filled polyimide and epoxy material that can provide a much broader and higher capacitance density. Also supplied as the laminate, the fabricator simply places a layer within the printed circuit board structure. Because it is a para-electric material, it furnishes a relatively low capacitance density compared to a crystalline ferroelectric material. In this case, the total capacitance available is limited only by the area of the circuit board and given a suitable sized board the materials can be used for decoupling where higher capacitance density is required.

24.5.3.1 Planar Capacitors. Power and ground planes within the EPCB structure are often used to furnish a common capacitance value to the entire circuit, providing both current and voltage to enable the power supply in meeting the demands of the active components. The power source can be either AC or DC. Power and ground planes are commonly furnished as adjacent layers in the layer stack-up. When required, the designer can add additional power and ground planes or pairs of power and ground planes within the board.

The general description of a planar capacitor is basically two copper layers separated by a thin (~25 µm) dielectric layer. Because these Cu planes extend across the entire substrate, the plated through-hole vias or micro-vias connecting to the power and ground planes can be placed very close to the power and ground inputs of teach device. This close coupling results in lowering loop inductance. Low inherent inductance will deliver current to the device on a very short time scale, greatly damping fluctuations of the voltage at the device input.

Normally, embedded formed polymer capacitors are made from purchased sheet materials. It is difficult for the board fabricator to apply a liquid dielectric formulation precisely to laminate, but one photolithographic capacitor formation technique has been developed. Unneeded dielectric is removed with a developer solution similar to liquid photoimageable solder mask.

24.5.3.2 Formed Discrete Capacitors. A majority of the capacitors designed into an electronic circuit will function as a decoupling element. In regard to forming capacitor elements within the circuit layers, the industry has developed a number of buried capacitor materials with high dielectric coefficients. In most cases, a higher dielectric coefficient is desirable since the strength of the capacitor is directly proportional to its dielectric coefficient. The 'planer' capacitor in particular, is one that basically separates parallel copper foils. These foils generally provide the power and ground layers of the substrate.

24.5.3.3 Thin Film Capacitor Dielectrics. The capacitor dielectric selected for separating the copper surfaces of the power and ground plane are most likely to be either an organic polymer thick film (PTF) or ceramic thin film (CTF) composite. These dielectrics can be applied for both discrete and planar capacitors. The PTF material density is equal to 20 pF/mm^2 while CTF materials will have a density rating of approximately 24 nF/mm^2.

There are a number of companies supplying polyimide (PI) as the dielectric for capacitors. Polyimide dielectric laminate can be processed like thin flexible circuit laminate through the develop/etch/strip process steps. Although furnished with copper foil on both sides, the dielectric remains somewhat flexible and can be imaged and etched with conventional PCB fabrication processes to define the capacitor outline.

24.5.4 Inductor Fabrication Process

Formation of inductors simply involves the design in copper circuitry, and then careful imaging and etching to ensure close tolerance conductors. PCB planar spiral inductors can be used as antennae or components for forming high frequency matched filters in a RFID system.

The term “spiral” is not always a literal description of the formed inductor element. The spiral inductor, depending on their specific application, can be designed in a number of different shapes Sizing of inductors is dependent on a number of parameters:

- Line width
- Spacing
- Geometry

Single layer copper spiral inductor can only reach about 10 nH; however, multilayer spiral inductor can reach up to 30 nH. Adding a ferromagnetic material either as a core within loops of copper or lying beneath or sandwiching a spiral can possibly extend the inductor value into the 100 nH range. The detail in Fig. 24.8 furnishes the basic physical parameters for designing the spiral inductor on the embedded PCB structure.

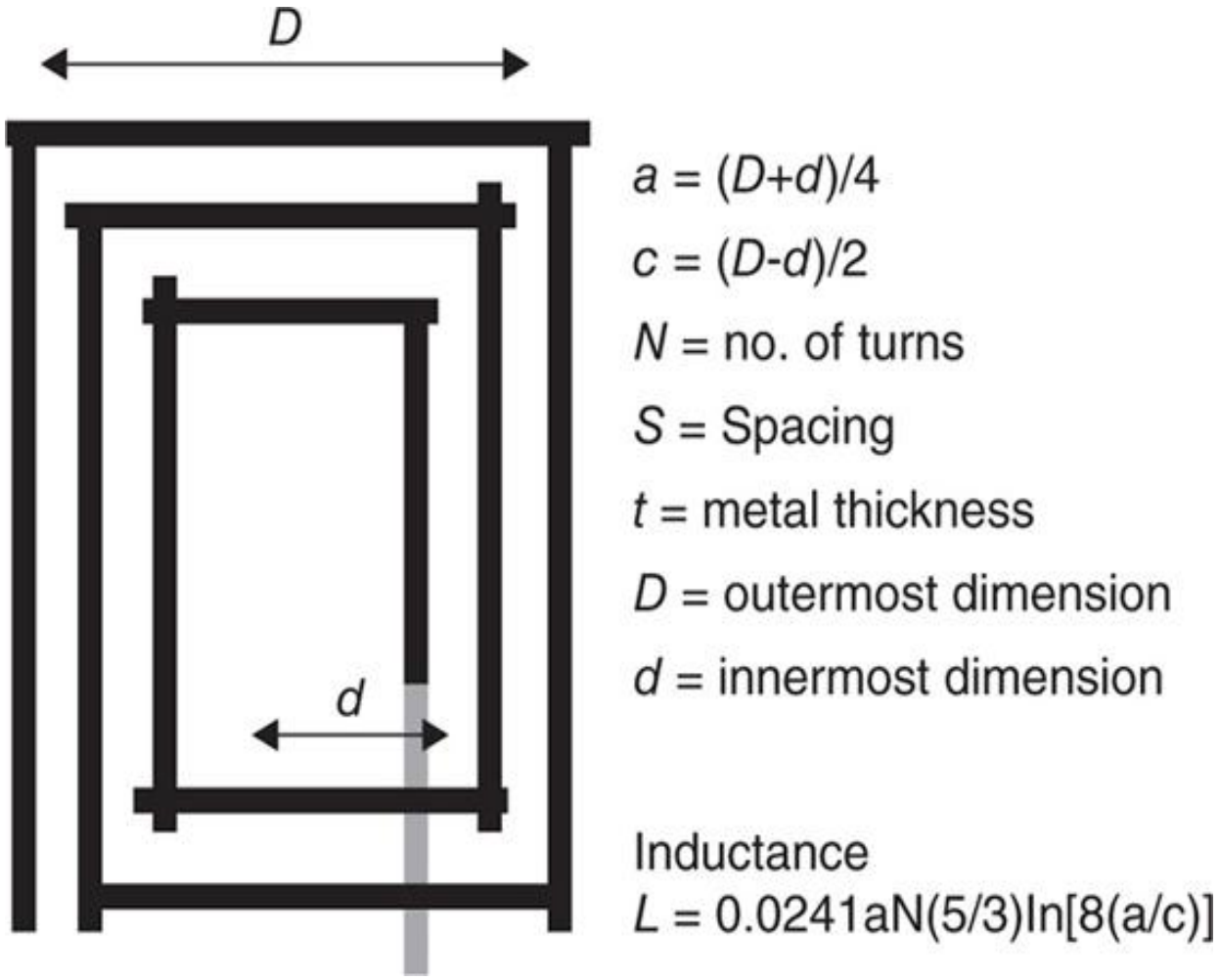


FIGURE 24.8 Spiral inductor design parameters.

As noted, the resistances and inductances of a formed spiral inductor can also be calculated using a number of commercially available software tools.

24.5.5 Active Integrated Circuit Fabrication

Forming active elements: transistors, memory, integrated circuits (ICs) within the circuit structure is possible but the processes and materials are not as widely available to the commercial PCB fabricator. Semiconducting polymers make

up the source, drain, and gate of the integrated circuit and are applied by inkjet or screen printing.

24.5.5.1 Formed Transistors. Discrete elements can be integrated into the circuit structure using thin films of organic or inorganic compounds. One printable inorganic semiconductor adapts an amorphous combination of InGaZnO that can be cured at low temperature. Electrodes in these transistors are typically metal but they may consist of conductive organic compounds.

24.5.5.2 Formed Memory. Based on the use of functional polymer material and flexible films, memory functions have been developed to provide data storage within the circuit structure. These unique materials are ideally suited for consumer products such as personalized toys and online-enabled game cards, authenticity identification, smart packaging, displays and all-printed RFID applications.

24.5.5.3 Formed Logic. The “printing inks” used in creating semiconductor functions consist of conducting and semiconducting conjugated polymers and/or other nano materials that are formulated into solvents. Printing is done one layer at a time (semiconductor, conductor, insulator, resistor, and dielectric). Each deposited using advanced printing systems enabling feature sizes as small as 10 µm and the layers must align precisely for the device to function properly.

There is continued development for a wide range of components for embedded printed circuit board (EPCB) applications. Most of these active component-forming processes rely on proprietary methodologies and material sets and will likely require licensing from the developing companies.

24.6 MATERIAL SUPPLY TYPES

24.6.1 Resistor Materials

Formation of the resistor by the designer, working with the board fabricator, involves making a material selection. All resistor values are not possible with each raw material technology. Table 24.1 shows the various forms of the raw resistor material.

TABLE 24.1 Embedded Formed Resistor Supplier Types

Process	Technology
Photoprint (sheet resistor material)	Thin-film etch (NiCr, Pt, NiP)
Screen or stencil print	Polymer thick-film addition (PTF)
	Ceramic thick-film addition (CTF)
Plating	Selective addition
Inkjetting	Selective addition
Photoimageable discrete	Photopolymer (filled)

Table 24.2 gives the range capability of the various resistor manufacturing technologies.

TABLE 24.2 Embedded Formed Resistor Ranges

Resistance, Ω	10	100	1000	10e4	10e5	10e6
Photoprint (NiCr, NiP)	X	X	X			
Photoprint (Pt)		X	X	X		
Screen or stencil print (PTF)	X	X	X	X	X	X
Screen or stencil print (CTF)	X	X	X	X	X	X
Plating	X	X	X			
Inkjetting	X	X	X	X		
Photoimageable discrete	X	X	X	X		

Where materials are sold in foil form or plated, only one value of resistors can be produced per layer. Since the resistive material is consistent across the panel, the final value of the finished resistor is determined by the length-to-width ratio. If the resistive material is made at 100 Ω per square properties, a resistor that is one unit wide and five units long will have a value of 500 Ω. Or, if the resistor is one unit long and five wide, the value will be 20 Ω. Practical resistor ranges evolve from the basic properties of the starting foil material.

Paste compositions, both polymer and ceramic, can have different dispersions of resistive particles and can yield widely variable resistance values. However, to limit manufacturing steps, selection of certain paste values, usually 10 to 15 times apart, are used. Thus, a design with resistors from 10 to 100,000 Ω could use pastes of 100 Ω per square, 1000 Ω per square, and perhaps 50,000 Ω per square.

A graphical representation of various formed resistor configurations is shown in Fig. 24.9.

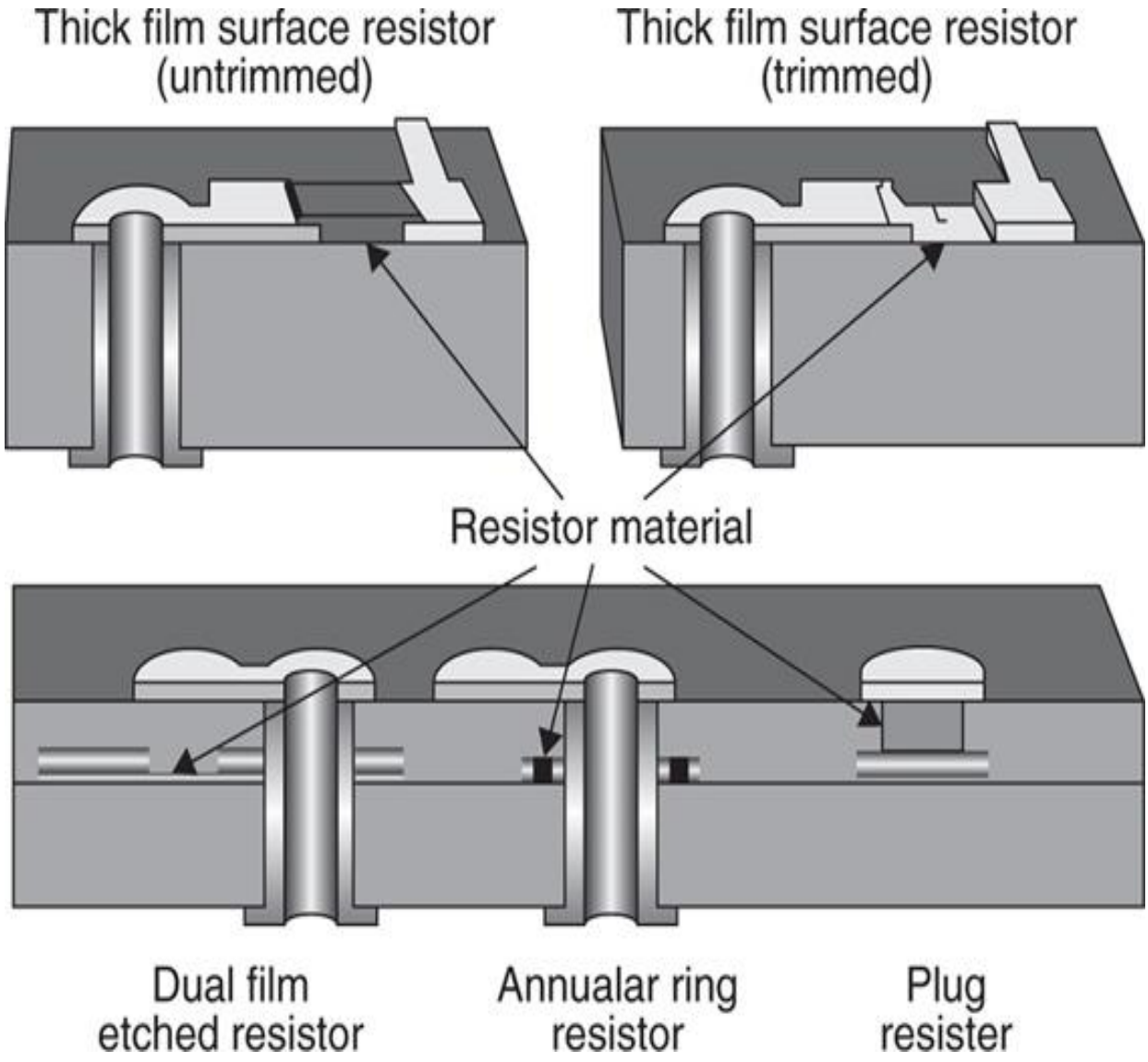


FIGURE 24.9 Embedded formed resistor configurations.

24.6.2 Capacitor Materials

Capacitors are needed in a great range of values. Capacitors may be the conventional “discrete” or a whole capacitance sheet may be used—*distributed capacitance*. Distributed capacitance is quite useful electrically, when high-speed integrated circuits need voltage immediately to turn on or off. The distance to voltage planes may be too long in some

designs and will not allow efficient electrical operation of very fast integrated circuits.

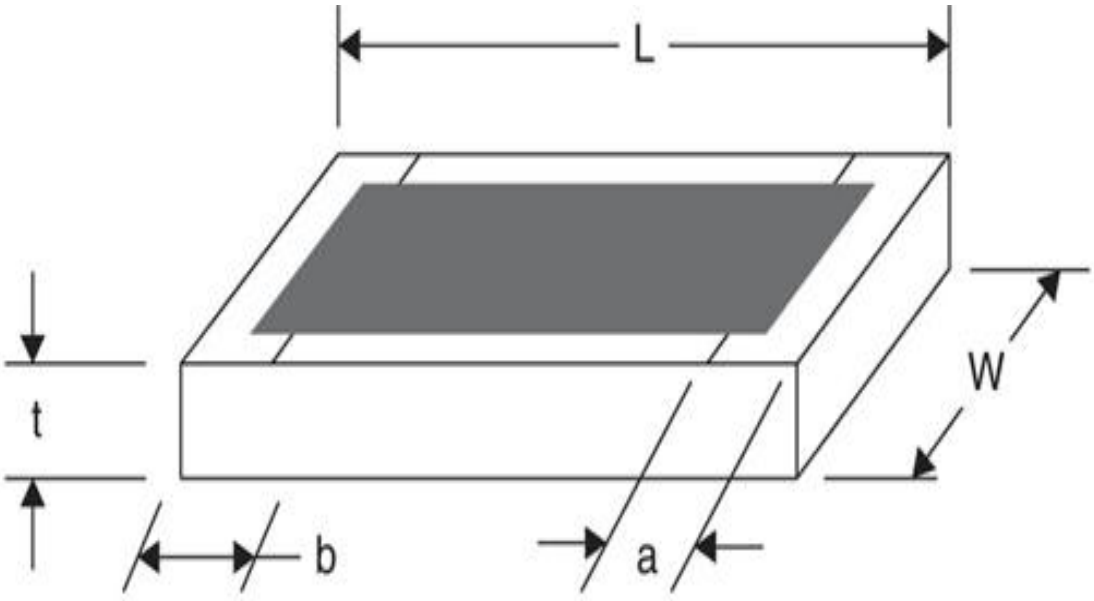
Depending on the technology applied, the area used to make the formed embedded capacitor can vary. Both area and dielectric will determine capacitor values. The value of capacitor can vary from a pico-farad to a few micro-farads. Low pico-farad elements are best suited for the formed embedded capacitors for applications generally associated with timing, decoupling, and filtering.

TABLE 24.3 Embedded Formed Capacitor Technologies

Process	Technology	Dielectric Constant	Micron Thick	Capacitance of a 1 sq. cm Area
Etched copper planes	FR-4/glass, copper clad laminate	4.5	50	78 pF/cm^2
			25	156 pF/cm^2
	Polyimide (filled) copper-clad laminate	11.0	14	700 pF/cm^2
	Polyimide (unfilled) copper-clad laminate	3.5	25	122 pF/ cm^2
	Proprietary dielectric (filled) copper-clad laminate		24	140 pF/cm^2
		4.2	12	310 pF/cm^2
	Epoxy (filled) copper-clad laminate	15	16	850 pF/cm^2
Screen or stencil printed discrete	Ceramic thick-film	1500	25	93 nF/cm^2 (93,000 pF/cm^2)
Photoimageable discrete	Photopolymer (filled)	22	11	1.5 nF/cm^2 (1500 pF/cm^2)
Emerging	Sol gel formation	150	0.5	150–300 nF/cm^2

An alternative to forming component parts, many companies are placing discrete passive components within the multilayer circuit. Although a majority of the discrete passive devices may remain mounted on the outer surfaces of the interposer or substrate, embedding passive component elements within the innerlayers of the structure will enable greater utilization of the outer surfaces for larger passive and packaged semiconductor component mounting.

24.6.2.1 Discrete Resistors. Discrete resistors are commercially available in the standard 0201 and 01005 type package outlines. In regard to the value range available in the smaller package outlines, ceramic based thick film SMT resistors are available in all of the standard values with tolerances of 5 percent for thick film resistors and 0.5 percent for the thin film type resistors. The overall thickness specified for the commercially available discrete resistor is 0.13 mm for the 01005 outline device and 0.23 mm for the 0201 outline variation (Fig. 24.10).



Type (Inch size)	Dimensions (mm)				
	L	W	a	b	t
01005	$0.40^{+0.02}$	$0.20^{+0.02}$	$0.10^{+0.03}$	$0.10^{+0.03}$	$0.13^{+0.02}$
0201	$0.60^{+0.03}$	$0.30^{+0.03}$	$0.10^{+0.05}$	$0.15^{+0.06}$	$0.23^{+0.03}$

FIGURE 24.10 Thin small outline resistor.

The resistors described above are considered standard and have a relatively broad source of supply. Thinner passive components than those shown may be available from companies with specific interest in supporting the embedded component market.

24.6.2.2 Discrete Capacitors. The discrete SMT capacitor family also includes 01005 and 0201 outline. The dielectric type, working voltage and value range for the

smaller device outlines, however, is somewhat limited. The 01005 and 0201 type capacitors with a C0G dielectric, for example, are available in a value range between 5.0 and 100 pf. The X7R dielectric capacitors, on the other hand have a value range 68 to 470 pF for the 01005 type and 68 to 10,000 pF. A number of companies are supplying the small outline capacitor with thickness of 0.20 mm for the 01005 type component and 0.30 mm for the 0201. A very thin (0.15 mm) capacitor family is available from some sources but the value range may be limited.

A unique and very thin (0.13-mm-thick) chip capacitor family is available that utilizes a silicon technology and a tightly controlled wafer fabrication process to produce capacitors that are said to have excellent placement loss and consistent capacitance. Described by the manufacturer as a metal-insulator-semiconductor (MIS) the chip capacitors are primarily designated for use as DC blocks in wire-bond assembly. These components are available with capacitance values from 0.8 to 1000 pF and are useful from VHF to millimeter wave bands. The outline of the component grows progressively with the specific capacitance value from a tiny 0.23 × 0.30 mm outline for the 0.8 pF capacitor to 1.5 × 1.70 mm outline for the 1000-pF capacitor.

24.6.3 Placing Active Component Elements

Progress in developing high density embedded component substrate capability has accelerated through the cooperation and joint development programs between a number of government, industry and technical universities. In addition to these joint development programs, several independent development laboratories and package assembly service providers have developed proprietary processes for specific applications. Embedding active components within the

substrate interposer will require the adoption of a methodology that is well outside the more traditional multilayer PCB fabrication processes. Some semiconductor components are easy candidates for integrating into the substrate while other may involve more complex processes.

24.6.3.1 Attachment and Termination. Semiconductor elements may be mounted on the core structure with their active face up or down. There are a number of methods being used for interconnecting uncased semiconductor components. The face-up attachment method will likely require the fabricator to provide a cavity within the laminate structure to compensate for the die thickness and termination profile. The initial mounting of the die traditionally adopts an adhesive material (liquid or film) for securing the die element to the substrate interposers' surface. Both wire-bond and ribbon-bond processes may be applied for completing the die-to-substrate interface. Following the die attach and termination process the die element is commonly encapsulated with an epoxy compound that, when cured, becomes a homogeneous part of the substrates structure. For some applications, the prepreg resin coating may furnish enough material during the lamination press cycle to flow into the cavity to complete the encapsulation process (Fig. 24.11).

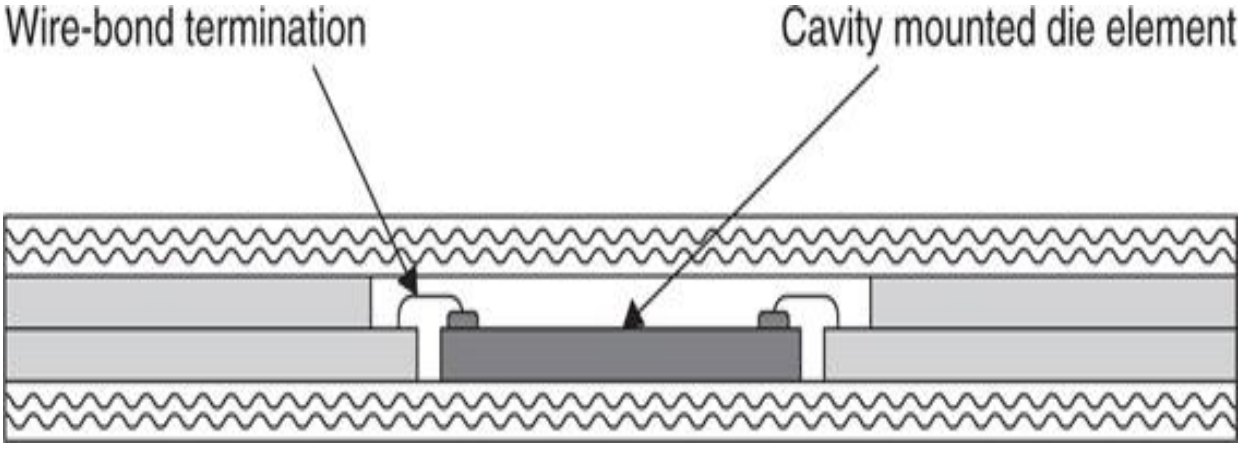


FIGURE 24.11 Cavity-mounted die element.

24.6.3.2 Flip-Chip Attachment. Mounting the semiconductor in the facedown orientation (flip-chip) requires additional preparation to the die element. The most basic process provides a solder compatible copper metallization to each wire-bond site. The bond sites are then furnished with a small volume of solder alloy that, when heated to a liquid state, form a raised bump feature for subsequent soldering onto mating lands provided on the substrate surface (Fig. 24.12).

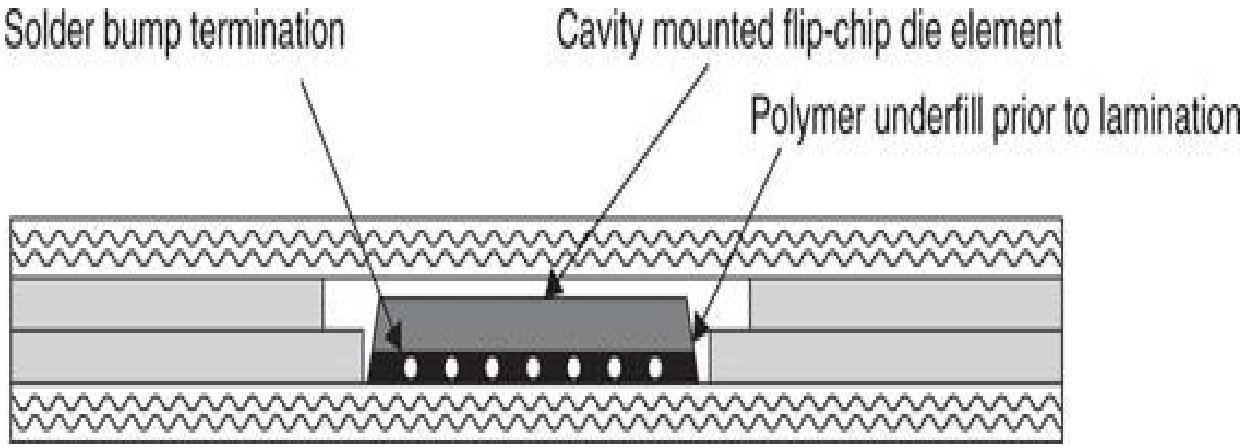


FIGURE 24.12 Cavity-mounted flip-chip die.

Reflow solder processing is the most common technique for flip-chip assembly and a substantial infrastructure already exists for supplying systems for both high and low volume manufacturing. Common methods for mass reflow soldering include hot air/gas convection, infrared, conduction, and vapor phase.

To ensure long-term reliability, the solder alloy composition selected must be compatible with the contact alloy and surface finish supplied on the mounting structure. In addition, both temperature and the cycle time required for soldering the lead-bearing solder and the lead-free solder can differ a great deal. The tin/silver/copper alloy compositions, for example, become liquidus at a

temperature range that is much higher than the eutectic tin/lead alloy and the time duration for completing the joining process may need to be extended as well.

24.6.3.3 Micro-via Terminated Die Element. Many companies favor attachment of the semiconductor die with the active surface facing away from the substrates core or base structure. In preparation for direct micro-via to die bond pad interface the bond sites on the die element must be prepared with a compatible Cu alloy contact surface. Typical of the passive device shown above, it is common to provide a recessed cavity in the substrate to compensate for the semiconductors thickness. This allows the semiconductor to be completely encased by the substrate resin materials during the lamination process (Fig. 24.13).

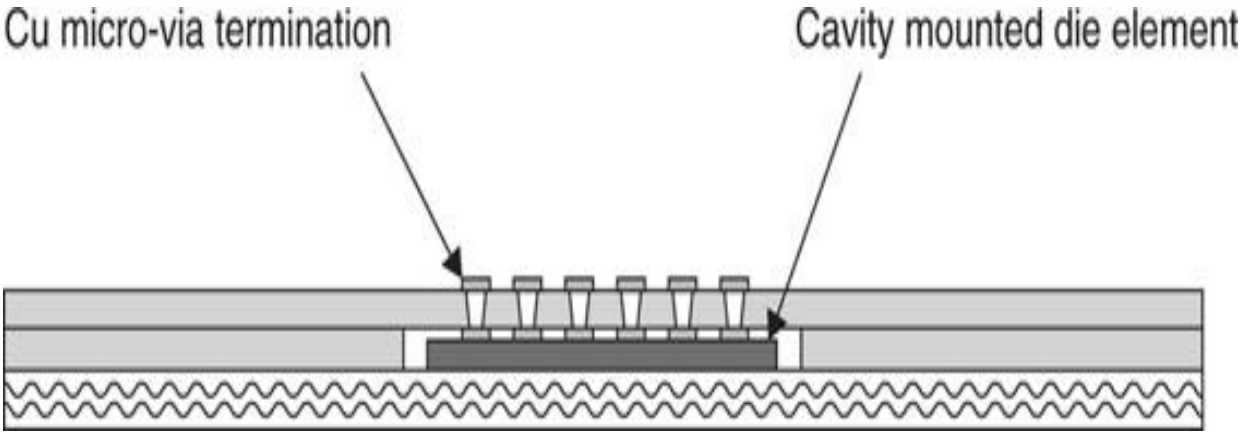


FIGURE 24.13 Micro-via terminated die element.

One key benefit of the face-up mounting option is improved thermal dissipation. When the die element is mounted onto a solid copper plane, any heat generated by the semiconductor during operation can be distributed over a wider area.

24.6.3.4 Combining Formed and Placed Components. When combining formed components and

placed components the designer must consider economic and performance goals:

- The formed passive components are generally very economical because they can be easily implemented during PCB fabrication. The main drawback is the limitation of value range. Beginning with a single base value, the designer will be limited to a single resistance per square and the stability of the target values will be impacted by the effects of aging of the substrate material, operating temperature and any conditions that would promote excessive moisture absorption. The general consensus is to ‘form’ the non-critical value components and “place” the components requiring closer value control.
- The placed passive components will have the greater latitude for value and tolerance stability. Placing components, however, requires a number of processes considered well outside the normal PCB fabrication process flow. Systems will need to be available for depositing solders or conductive materials, precise placement of the components, and capability for reflow soldering or thermal curing the attachment material. If plated copper via’s will be used for component interface, they too will require copper plating on their terminal features.

24.6.3.5 Process Planning for Formed and Placed Components. In the event that both formed and discrete placed components are to be combined within the same embedded PCB structure, there are a few ground rules regarding component location. Mixing formed and placed components on the same layer should be avoided. This is because the processes for forming and the process for discrete component termination are quite different. Because the formed components require unique printing curing or photoimaging and developing processes, they can be easily

damaged if not protected. The protection may be a coating of polymer or the lamination of glass reinforced clad with copper foil or resin coated copper foil. The discrete components selected for embedding should be on separate layer(s) of the PCB (Fig. 24.14).

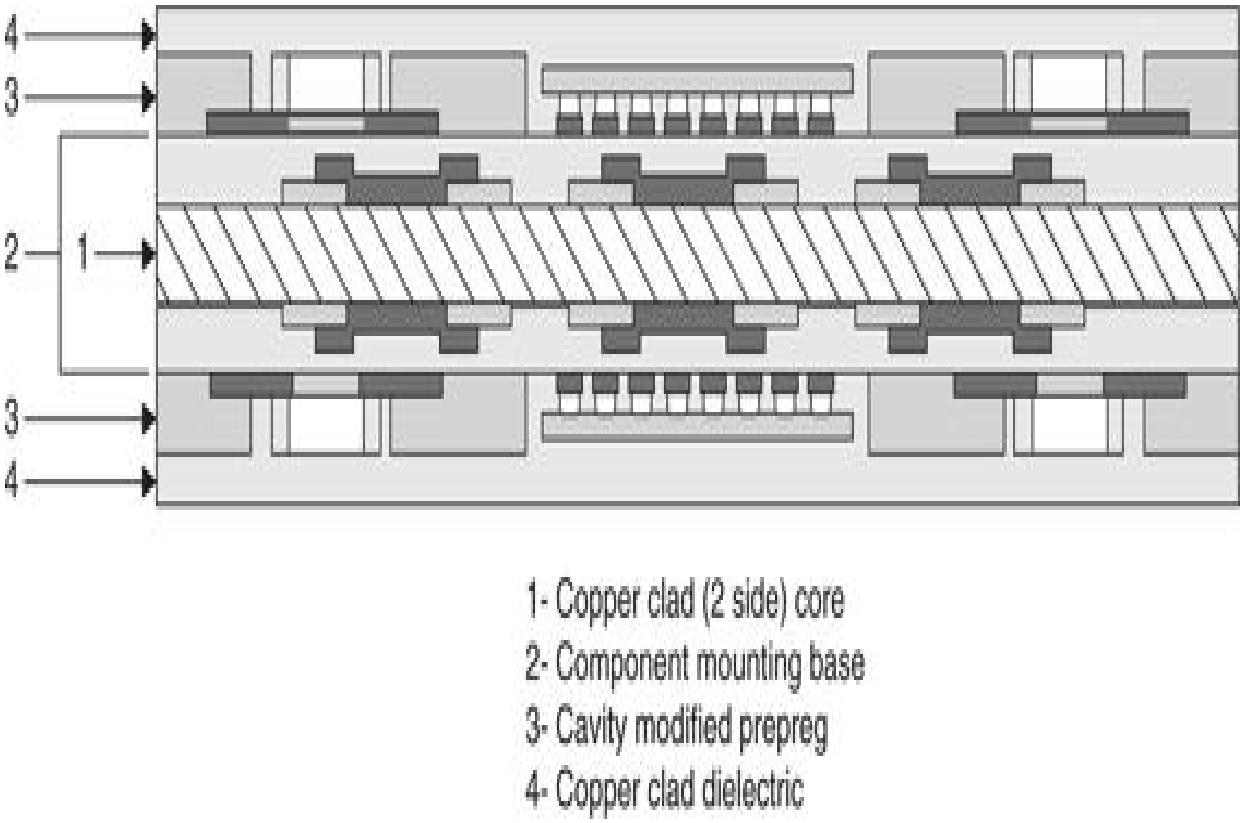


FIGURE 24.14 Combining formed and placed components *(source: IPC-7092)*.

When planning the embedded component PCB the designer must consider the fabrication process flow. The process flow will go well beyond the sequence typically applied to conventional multiple layer PCB fabrication. Embedding formed components will have very little impact on the fabrication sequence, however, placing and terminating discrete components with in the PCB structure will require processes not typical of those commonly available in PCB shops. An example of a process flow

combining formed and placed components within the same PCB structure is shown in Fig. 24.15.

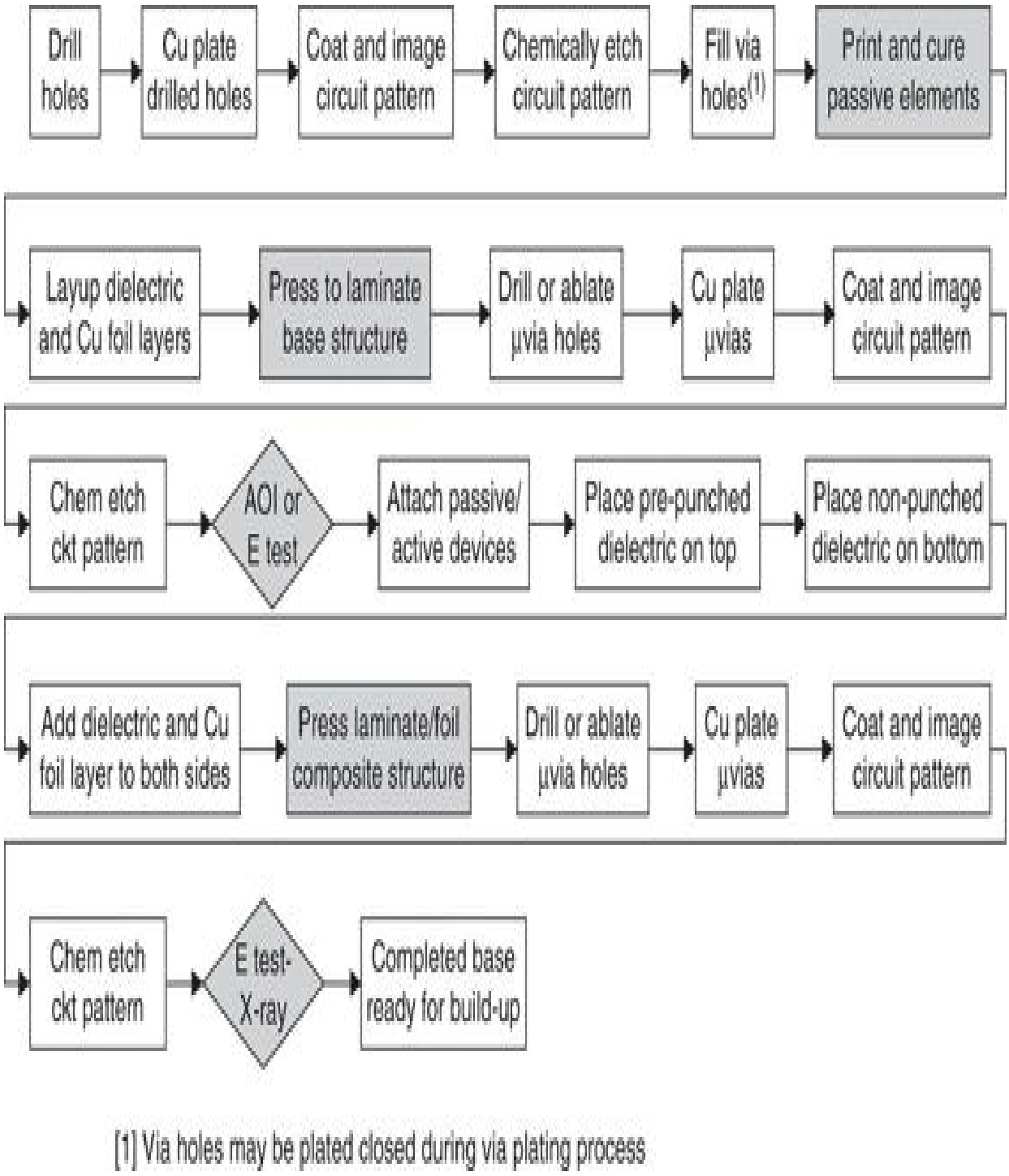


FIGURE 24.15 Embedded component process flow diagram *(source: IPC-7092)*.

24.6.3.6 Bill of Material Preparation. The BOM for the embedded component substrate or PCB will be segmented to reflect the location or layer where the component parts are mounted or formed. To assist in identifying each components location it is recommended that the designer establish a reference designation system on the schematic diagram that corresponds to the circuit layer on which the component it is located. Furthermore, when creating a BOM the designer should consider who would be using it. It may be used internally or for communication between several manufacturing partners and suppliers or confined to a single suppliers manufacturing facility.

24.7 CONCLUSION

Further reading and standards are available in the newly completed IPC-7092, Design and Assembly Process Implementation for Embedded Components. This 150-page document covers embedded discreets and formed components as well as embedded active devices.

24.8 ACKNOWLEDGMENT

The author acknowledges Dennis Fritz, MacDermid Incorporated, Waterbury, Connecticut, for writing this chapter for Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

[a] This chapter was originally written by Dennis Fritz, MacDermid Incorporated, Waterbury, Connecticut, for Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

PART 5

HIGH-DENSITY INTERCONNECTION

CHAPTER 25

INTRODUCTION TO HIGH-DENSITY INTERCONNECTION TECHNOLOGY

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

25.1 INTRODUCTION

The use of more complex components with very high input/output (I/O) counts has pushed the board fabricator to reexamine techniques for creating smaller vias, and many new or redeveloped processes have appeared on the market. These processes include revised methods of creating holes, such as laser drilling, micro-punching, and mass etching; new methods for additively creating dielectric with via holes using photosensitive dielectric materials; and new methods for metallizing the vias such as conductive adhesives and solid post vias. All of these methods share some common traits. They all allow the designer to increase significantly routing density through the use of vias in surface-mount

technology (SMT) pads, to reduce size and weight of product, and to improve the electrical performance of the system. These types of boards are generically called high-density interconnects (HDI). An HDI board typically will have, as an average, over 110 to 130 electrical connections per square inch (20 connections per sq. cm) on both sides of the board.

25.2 DEFINITIONS

Printed wiring boards (PWBs) with microvia hole structures are called different names, such as HDI, sequential build-up (SBU), and build-up multilayer (BUM). However, HDI covers a broader range of high-density wiring boards such as extremely high-layer-count multilayer boards (MLBs) without microvia holes. MLBs with microvia holes are not necessarily built sequentially, nor do they necessarily have build-up structures. These definitions are not appropriate for the discussions in this chapter, and therefore we shall address MLBs with microvia holes simply as *microvia hole boards* (all microvia hole boards are essentially multilayer boards).

Some trade and academic organizations define the microvia hole to be a hole of a certain diameter or less. For example, the Association Connecting Electronics Industries (IPC) defines a microvia hole as a hole with a diameter equal to or less than 150 μm. However, when a surface blind via (SBV) hole is formed between layer 1 (L1) and layer 3 (L3), the diameter of such a hole is typically 250 μm in order to facilitate reliable plating, but the hole is still considered a microvia hole. Since all microvia holes are essentially SBVs and are normally small in diameter in order to increase circuit density, it seems more appropriate to define the microvia hole as an SBV without limiting its diameter. As long as a hole has SBV structure, it is defined as a microvia hole throughout this chapter.

The first microvia PCB in general production, Hewlett Packard's FINSTRATE, was put into production in 1984 (see appendix a at the end of this chapter). It was a copper-core, build-up technology that had direct wire- bonded integrated circuits (ICs). After laminating layers of plasma-metalized polytetrafluoroethylene (PTFE) to the copper core, vias were mechanically drilled through the copper core and then insulated with PTFE. Additional through holes were then drilled along with 5 mil blind vias. The first photodielectric microvia board was produced in volume in Japan by IBM-Yasu (see appendix b). This is the SLC technology with two build-up layers on one side of the four conventional FR-4 layers. These can be seen in Fig. 21.1 in the 5th edition of *Printed Circuits Handbook*.

25.2.1 HDI Characterization

This generation of printed boards is characterized by very small blind, buried, and through vias made by techniques other than mechanical drilling. To turn blind vias into buried vias, these process techniques are repeated and the layers are "built up," hence the name *build-up* or *sequential build-up circuits* (SBU).

This type of printed circuits actually started in 1980, when researchers started investigating ways to reduce the size of vias. The first innovator is not known, but some of the earliest pioneers include Larry Burgess of MicroPak Laboratories (developer of LaserVia), Dr. Charles Bauer at Tektronixs (who produced photodielectric vias)[1] and Dr. Walter Schmidt at Contraves (who developed plasma-etched vias). Laser-drilled vias were used in mainframe computer multilayers in the late 1970s. These were not as small as the laser-drilled vias today and were produced only in FR-4 with great difficulty and at great cost.

The first production build-up or sequential printed boards appeared in 1984, starting with the Hewlett Packard laser-drilled FINSTRATE computer boards, followed in 1991 in Japan with Surface Laminar Circuits (SLC)[2] by IBM and in Switzerland with DYCOstrate[3] by Dyconex. Figure 21.1 in the 5th edition of *Printed Circuits Handbook* shows one of those first Hewlett Packard FINSTRATE boards and one of the first IBM SLC boards (see this chapter's appendix).

Since the introduction of SLC technology in 1991 (see Fig. 2.5), many variations of methods for mass producing HDI wiring boards have been developed and implemented. However, if one technology is to be picked as a winner judged in terms of volume produced, laser-drilling technology is the one. Other methods are still used by a number of PWB manufacturers, but in a much smaller scale.

The purpose of this chapter is to examine a variety of microvia hole formation technologies, structures, and materials.

However, a greater emphasis will be placed on the laser-drilling process (*laser via* hereafter) since it is the most popular process today and it seems its popularity will grow in the future. It must be understood that via hole formation is just one element of fabricating HDI wiring boards. Fabrication of HDI wiring boards with microvia holes involves many new processes not common to conventional board fabrication. Therefore, additional emphasis will be placed upon these new fabrication processes that are common to other microvia technologies.

25.2.2 Advantages and Benefits

Four main factors drive printed boards to require higher wiring densities:

- More components can be placed on both sides of the printed circuit.
- Components are closer together.
- Size and pitch of components are smaller while the number of I/Os is increasing.
- Smaller geometries allow faster transmission of signals and reduce signal crossing delay.

At the same time, enhanced performance is required for faster signal rise times, reduced parasitics, reduction of radio frequency interference (RFI) and electromagnetic interference (EMI), fewer layers, and improved high-temperature performance and reliability. HDI provides all of these advantages and more.

25.2.3 HDI Traditional PCB Comparison

The interactions among PCBs, components, and assemblies are best seen by the packaging technology map (see Fig. 1.2). Components are characterized by the average I/Os per part, assemblies by the components per sq. cm and I/Os per sq. cm, and the printed circuit by its wiring density in cm per sq. cm. Figure 25.1 shows the approximate crossover between the traditional printed circuit board and the next generation with microvias.[4]

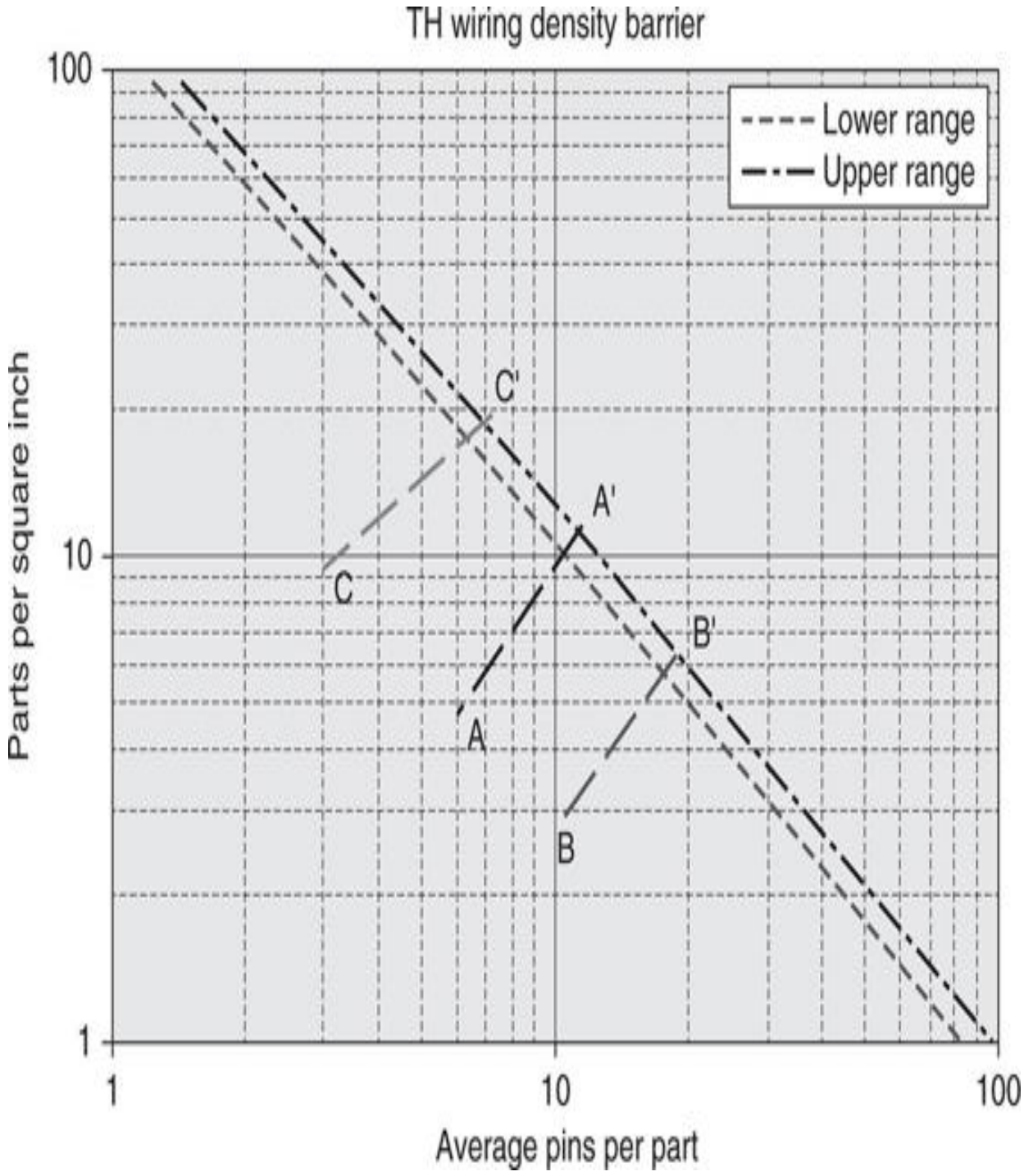


FIGURE 25.1 The through-hole density barrier. If the ends of an electrical net contain an SMT pad connected by a trace and a via hole, then there is only so many such connections (using conventional design rules' spacing) that can be placed in any square area. This *through-hole barrier* is shown crossing this technology roadmap. To cross the barrier (and prevent via starvation), the fabricator must stack vias using blind and buried vias and such.

25.2.4 Design, Cost, and Performance Trade-Offs

The HDI structure is cost-effective for higher-density assemblies shown throughout this chapter. The relative price of HDI versus relative density is depicted in Fig. 25.2. Cost parity (for similar wiring densities) is achieved with a four-layer HDI microvia at approximately an eight-layer, through-hole printed circuit multilayer. Wiring capacities and densities greater than an eight-layer multilayer can be achieved at a lower price with a properly designed HDI substrate. At very high densities, there are no through-hole multilayers that can meet the wiring capacities and density demand necessary, whereas HDI can easily meet the requirements.

N Layers	A THRU-HOLE N blind via' buried via		B HDI BLIND 1+N+1 L1-L2 none		C HDI BL/BU 1+bN+1 L1-L2 L2-L(N-1)		D 1BU BLIND 1+N+1 skip via L1-L3 L2-L(N-1)		E 2BU BLIND 2+N+2 staggered L1-L2, L2-L3 none		F 2BU BL.BU 2+bN+2 staggered L1-L2, L2-L3 L2-L(N-1)		G 2BU BL.BU 2+bN+2 staggered L1-L2, L2-L3 L3-L(N-2)	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.62	20	0.83	40	1.05	80	1.26	135	1.38	135	--	--	--	--
6L	0.78	20	0.99	60	1.24	160	1.46	200	1.60	200	1.74	260	1.91	280
8L	1.00	30	1.21	120	1.49	180	1.74	240	1.90	240	2.06	300	2.25	320
10L	1.30	40	1.51	200	1.83	210	2.11	260	2.30	260	2.50	400	2.73	440
12L	1.70	60	1.92	210	2.31	230	2.62	300	2.85	300	3.10	600	3.37	650
14L	2.24	70	2.48	220	2.95	250	3.32	360	3.61	360	3.91	800	4.25	860
16L	2.97	80	3.22	260	3.81	300	4.25	420	4.61	440	5.00	1000	5.43	1100
18L	3.92	100	4.21	300	4.95	400	5.47	560	5.93	580	6.42	1250	6.96	1350
20L	5.14	105	5.48	360	6.41	500	7.04	680	7.62	700	8.23	1500	8.90	1600
22L	6.67	110	7.08	400	8.23	600	8.99	800	9.70	840	10.45	1800	11.27	1850
24L	8.53	125	9.03	460	10.41	700	11.32	>1000	12.17	>1000	13.07	>2000	14.04	>2000
26L	10.68	130	11.30	500	12.92	800	13.96	>1000	14.96	>1000	16.00	>2000	17.11	>2000
28L	13.09	135	13.83	540	15.65	900	16.82	>1000	17.93	>1000	19.09	>2000	20.32	>2000
30L	15.63	140	16.50	580	18.47	100	19.73	>1000	20.94	>1000	22.18	>2000	23.48	>2000
32L	18.17	145	19.17	620	21.21	>1000	22.53	>1000	23.79	>1000				
34L	20.59	150	21.69	660	23.73	>1000								
36L	22.79	160	23.96	700	25.94	>1000								
38L	24.68	180	25.91	740										
40L	26.26	200												

FR-4 Based (other mat'la will raise the RCI)
RCI=Relative Cost Index to 8L
DEN=Density: Ave Pins/Square Inch

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THRU-HOLE VS. STACKING MICROVIAS HDI: COST, PIN DENSITY & WIRING DENSITY

ID		A		H			I			J			K		
Type		THRU-HOLE		2 BUILD-UP Blind & Buried			3 BUILD-UP Blind & Buried			4 BUILD-UP Blind & Buried			4/5 BUILD-UP Blind & Buried		
Stackup		N		2+bN+2			3+bN+3			4+bN+4			4+4 & 5+5		
Microvias		none		Stacked L1-L2-L3			Stacked L1-L2-L3-L4			Stacked L1-L2-L3-L4-L5			Stacked L1-L2-L3-L4-L5		
Buried Vias		none		L3-L(N-2)			L4-L(N-3)			L5-L(N-3)			Every Layer Microvias		
Stackup & Via Models															
		RCI	DEN	RCI	DEN	TWD	RCI	DEN	TWD	RCI	DEN	TWD	RCI	DEN	TWD
Signal Layers	4L	0.6	20	--	--	--	--	--	--	--	--	--	--	--	--
	6L	0.8	20	1.9	300	140	2.3	300	148	2.7	300	180	2.9	500	250
	8L	1.0	30	2.3	500	175	2.7	600	250	3	700	270	3	800	300
	10L	1.3	40	2.7	600	245	3	800	290	4	900	340	4	1000	350
	12L	1.7	60	3	1000	280	4	1000	333	4	1000	380	4	1200	400
	14L	2.2	70	4	1200	350	5	1200	370	5	1200	405			
	16L	3	80	5	1300	405	5	1300	420						
	18L	4	100												
	20L	5	105												
	22L	7	110												
	24L	9	125												
	26L	11	130												
	28L	13	135												
	30L	16	140												
	32L	18	145												

RCI = Relative Cost Index
DEN = Density: Pins/Square Inch
TWD = Total Wiring Density

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FIGURE 25.2 (*a*) Relative price and density comparison between conventional through-hole (TH) boards and HDI microvia boards with different structures. The relative cost index (RCI) is actual production pricing of boards normalized to the eight-layer price. The density (DEN) is a measure of the maximum average pins (leads) per sq. in (for both sides of the PCB). The diagonal lines are equivalent density boards. These are for FR-4 printed circuits; (*b*) relative price and density comparison for conventional TH boards and Stacked HDI microvia boards.

25.2.5 Specifications and Standards

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has been working on standards and specifications for high-density interconnecting structures. Three standards and a guideline are the documents that are available from the IPC. The four documents are

- *IPC-2315*. "Design Guide for High Density Interconnecting Structures and Microvias"
- *IPC-2226*. "Design Standard for High Density Interconnecting Structures and Microvias"
- *IPC-4104*. "Standard for Qualification and Conformance of Materials for High Density Interconnection Structures and Microvias"
- *IPC-6016*. "Standard for Qualification and Performance Specification for High Density Interconnection Structures"

The IPC standards that cover HDI design rules, materials, and specifications are

- *IPC-2226*. This specification educates users in microvia formation, selection of wiring density, selection of design rules, interconnecting structures, and material characterization. It is intended to provide standards for use in the design of PCBs utilizing microvia technologies.
- *IPC-4104*. This standard identifies materials used for high-density interconnection structures. A series of specifications (slash sheets) are defined for specific available materials. Each sheet outlines engineering and

performance data for materials used to fabricate high-density interconnecting structures. These materials include dielectric insulator, conductor, and dielectric/conductor combinations. The slash sheets are provided with letters and numbers for identification purposes. For example, if a user wishes to order from a vendor and reference the specification sheet number 1, the number “1” would be substituted for the “S” in the preceding designation example (IPC-4104/1). To start the ordering process, one can use the slash sheets in the IPC-4104 document in combination with relevant IPC documents for each material sets (e.g., IPC-CF-148, IPC-MF-150, IPC-4101, IPC-4102, IPC-4103, etc.).

- *IPC-6016*. This document contains the general specifications for high-density substrates not already covered by other IPC documents.

25.3 HDI STRUCTURES

The IPC HDI Structure Subcommittee, which is responsible for defining performance requirements, used the following methodology to specify HDI products. Since a microvia can be any shape—including straight wall, positive or negative taper, or cup—determining the methods used for producing microvias can be segmented into three methodologies (A, B, or C), as noted in Table 25.1.

TABLE 25.1 Ten Process Methods Utilized to Produce Microvias

Hole Formation	Microvia Process*
Mechanically drilled	A
Dry-etched (plasma)	A
Mechanically punched	A
Abrasive blast	A
Laser-drilled	A
Post-pierced	B
Photo-formed	A
Insulation displacement	B, C
Wet-etched	A
Conductive bonding sheets	C

*A: create hole, then make conductive; B: create conductive via, then add dielectric; C: create conductive via and dielectric simultaneously.

All of these technologies provide approximately the same high-density design rules. These design rules endow build-up technologies with four to eight times the wiring density of conventional, all-drilled through-hole vias. The ten via profiles are depicted in Fig. 25.3.

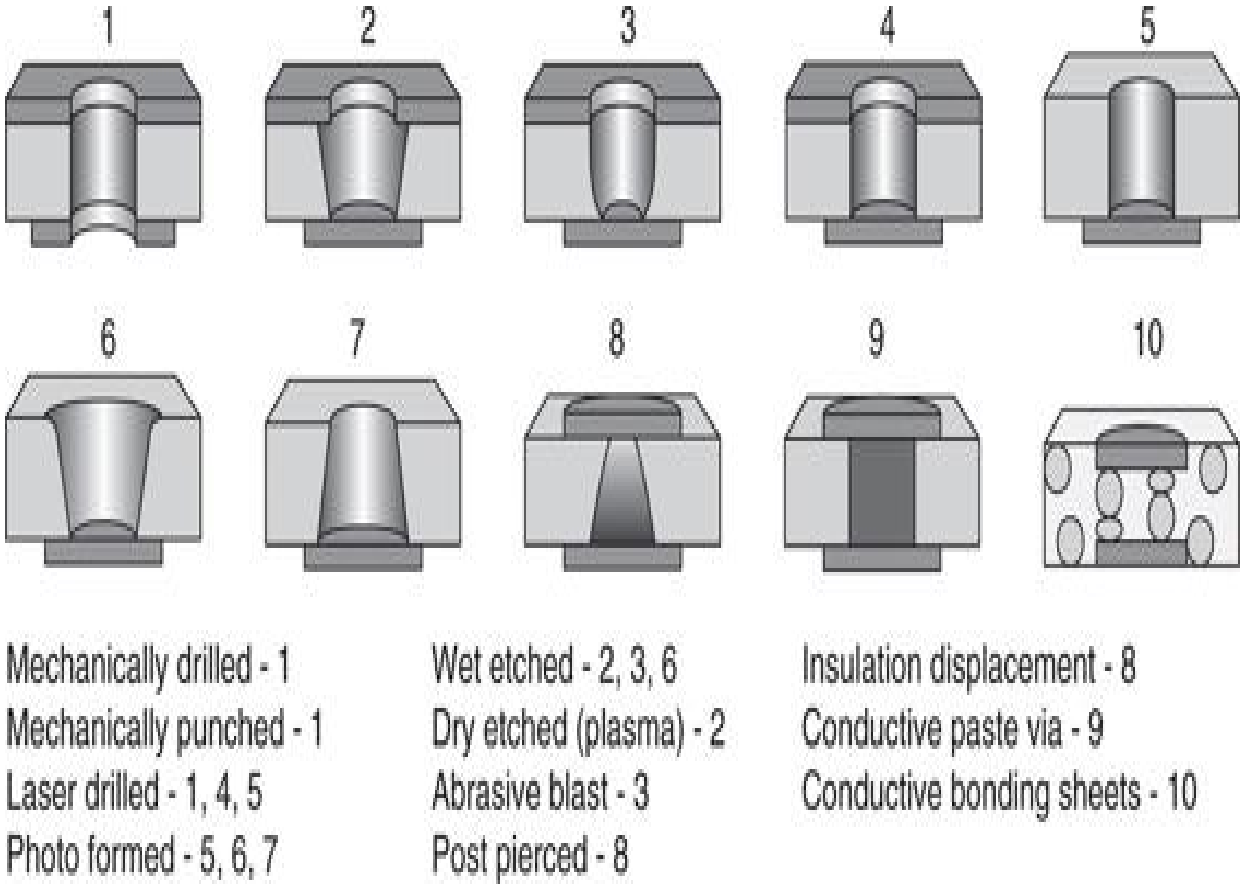


FIGURE 25.3 Representative microvia profiles and the processes that produce them.

The structure of the high-density interconnection is by type: Type I, Type II, Type III, Type IV, Type V, and Type VI (see Table 25.2). However, some of these type constructions are based on which microvia material is to be used. Thus, the following definition applies to all high-density interconnect substrates (HDIS).

TABLE 25.2 Description of the Six IPC HDI Type Structures of IPC-2226

Type I	1[C]0 or 1[C]1, with through-vias from surface to surface
Type II	1[C]0 or 1[C]1, with through-vias buried in the core and from surface to surface
Type III	≥2[C]≥0, 2 or more HDI layers added to through-via in core or from surface to surface
Type IV	≥2[P]≥0, where P is a passive "substrate with no electrical connecting functions"
Type V	Coreless construction using layer pairs
Type VI	Alternate construction using conductive pastes

[C], printed circuit core; [P], passive substrate core; 0, 1, and 2, number of build-up layers on each side of the core [C] or [P].

The core, defined as [C], can be identified as an A, B, or C type core. Thus, [CA] is a core with internal vias only; redistribution makes contact with the surface. [CB] is core with internal and external (through microvia structures). High-density interconnecting structures make contact with the innerlayers of the core. [CC] is passive core, in which there are no interconnections.

25.3.1 Construction

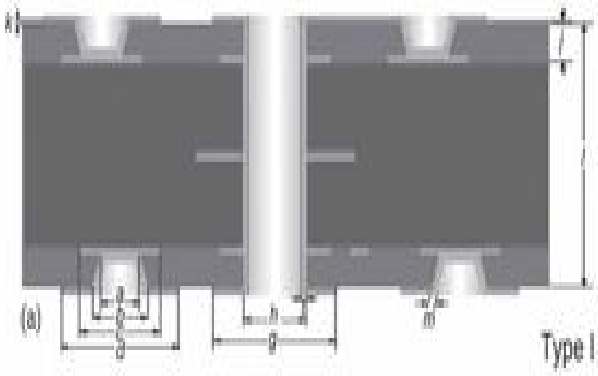
Type I to Type VI constructions currently describe all known HDI build-up structures, but as the technology evolves, new ones are likely to be created. The notation used is as follows:

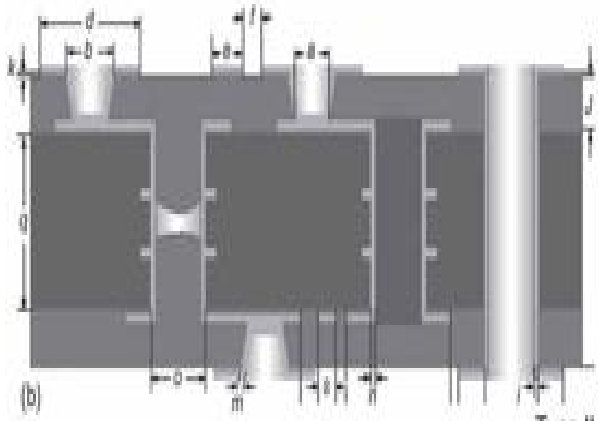
x[C]x

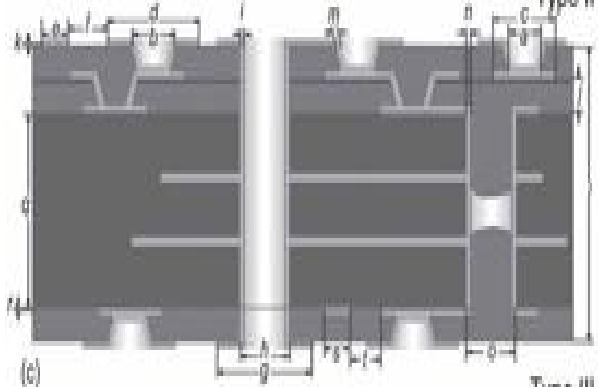
where x = 0, 1, 2, 3, etc. (that is, the number of build-up layers on that side of the core) [C] = a standard laminated core of materials, with or without vias of *n* layers

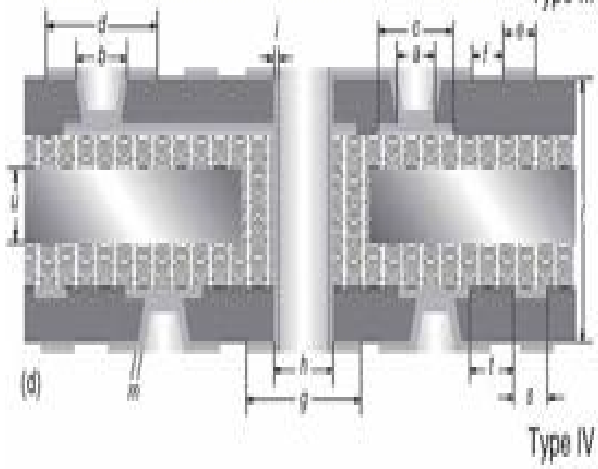
25.3.1.1 Type I Constructions. This construction (1[C]0 or 1[C]1) describe an HDI in which there are both plated microvias and plated through holes used for interconnection.

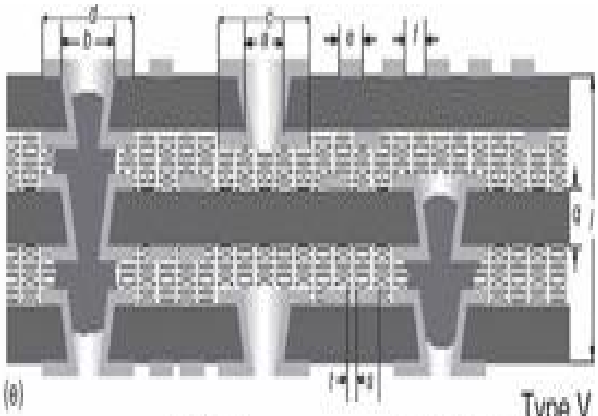
Type I constructions describe the fabrication of a single microvia layer on either one side (1[C]0) or both sides (1[C]1) of an underlined printed circuit substrate core. The printed circuit core substrate is typically manufactured using conventional printed circuit techniques. The substrate may be rigid or flexible and can have as few as one circuit layer or be as complex as a prefabricated multilayer printed circuit with buried vias. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric connecting layer 1 to layer 2 and layer n to layer $n - 1$. Through holes are then drilled, connecting layer 1 to layer n. Then the microvias and through holes are metallized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed. Figure 25.4*a* shows this construction as illustrated in IPC-2226.

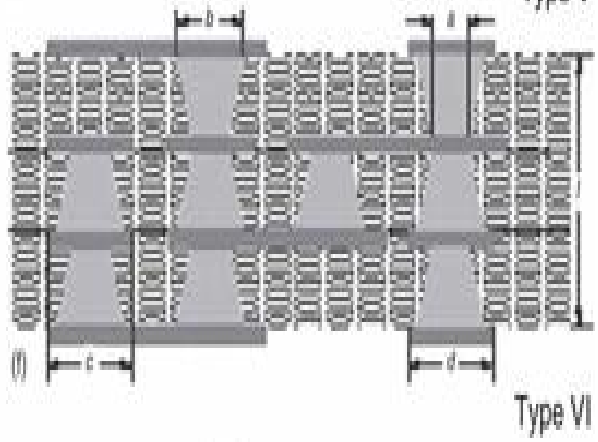

(a)
Type I


(b)
Type II


(c)
Type III


(d)
Type IV


(e)
Type V


(f)
Type VI

Build-up material
Prepreg/adhesive
Soldermask
Core material
Flex
Conductive paste
Bumper conductive
Conductive ink/hole fill
Vendor copper
Plating
Anisotropic conductive material

FIGURE 25.4 IPC-2226 microvia structures from Type I to Type VI.

25.3.1.2 Type II Constructions. Type II (1[C]0 or 1[C]1) has the same HDI layers as Type I. The difference is the core, [C]. Type II allows through vias to be placed in the core before the HDI layers are applied. The processes are the same except for the cores through vias being filled before the HDI layers are applied. Figure 25.4*b* shows this construction as illustrated in IPC-2226.

25.3.1.3 Type III Constructions. This construction (2[C]0) describes an HDI in which there are both plated microvias and plated through holes used for interconnection. Type III constructions describe the fabrication of two microvia layers on either one side (2[C]0) or both sides (2[C]2) of an undrilled or drilled printed circuit substrate core. The printed circuit core substrate is typically manufactured using printed circuit techniques. The substrate may be rigid or flexible and have as few as one circuit layer or be as complex as a prefabricated multilayer printed circuit with buried vias. A single layer of dielectric material is then placed on top of the core substrate. Microvias are formed in the dielectric, connecting layer 2 to layer 3 and layer $n - 1$ to layer $n - 2$. This first microvia layer is either metallized or filled with conductive material and then circuitized. A second layer of dielectric material is then placed on top of this circuitized layer and microvias are formed connecting layer 1 to layer 2 and layer n to layer $n - 1$. Through holes are then drilled connecting layer 1 to layer n. The microvias and through holes are then metallized or filled with conductive material. Layer 1 and layer n are circuitized and fabrication is completed. Figure 25.4*c* shows this construction as illustrated in IPC-2226.

25.3.1.4 Type IV Constructions. This construction (1[P]0 or 1[P]1 or >2 [P] > 0) describes an HDI in which the build-up layers are used over an existing drilled and plated

passive substrate. The printed circuit or metal core substrate is typically manufactured using conventional printed circuit techniques. This substrate may be rigid or flexible. Figure 25.4*d* shows this construction as illustrated in IPC-2226.

25.3.1.5 Type V Constructions. The Type V construction describes an HDI where there is no core. Both plated and conductive paste layer pairs are interconnected through a colamination process. The multilayer is created with an even number of layers (two-sided flex or rigid layer pairs) laminated together at the same time that the interconnections between the even and odd layer are made. This is not a build-up process; it is essentially a single-lamination-parallel process. Figure 25.4*e* shows this construction as illustrated in IPC-2226.

Layer pairs are prepared using conventional processes of etching, plating, drilling, and so on, or by conductive paste processes. The layer pairs are laminated together using B-stage resin systems or some other form of dielectric adhesive into which conductive paste vias have been placed.

25.3.1.6 Type VI Constructions. Type VI describes constructions of HDI in which the electrical interconnections and wiring can be formed simultaneously. Another variety forms the electrical interconnections and the mechanical structure simultaneously. The layers may be formed sequentially or colaminated. The conductive interconnect may be formed by means other than electroplating, such as anisotropic films/pastes, conductive pastes, dielectric piercing posts, and so on. Figure 25.4*f* shows this construction as illustrated in IPC-2226.

25.3.2 Design Rules

The designer should be aware that not all fabricators have equal capabilities in the areas of fine-pitch imaging, etching, layer-to-layer alignment, via formation, and plating. For this reason, the HDI design guide categorizes design rules into two categories: the preferred producibility range and the reduced producibility range. For simplicity of design, this handbook will further divide the design rules into three category ranges: A, B, and C, with A being the easiest to produce and C being the most difficult. If more stringent design standards are selected, the number of fabricators that can produce such a board is limited. Circuits produced with design rules in the A category will be easier to produce, will have higher yields, and therefore can be fabricated at lower cost. To keep costs at a minimum, you should select the design rules most appropriate for the application:

- *Category A*. This specification allows conventional HDI processes to be used with relaxed tolerances. It should have the highest yield and lowest cost. It is estimated that 100 percent of HDI fabricators can meet these design rules.
- *Category B*. This is the conventional HDI process. It is estimated that 75 percent of HDI suppliers can meet these design requirements under production conditions.
- *Category C*. Top-level fabrication shops, representing 20 percent of the total HDI fabricators, can meet these design rules. Panel sizes are often reduced to increase yield, which increases the final cost. Production volumes are presently limited, with special attention required during the production process. These rules require smaller panels and more exotic fabrication techniques. They are generally required only in electronic packages, chip-on-board (COB), flip-chip interposers, or MCM applications. At present, yields are lower and costs are high. It is estimated that fewer than 20 percent of all fabricators can achieve these design rules in limited production or prototype volumes.

Typical HDI design rules are given in Fig. 25.5. This figure bridges the two design categories from the specification IPC-2226, “Design Standards for HDI and Microvias.”[5] This is a Type III HDI structure.

Symbol	Feature	Category A micron [mil]	Category B micron [mil]	Category C micron [mil]
a	Microvia hole diameter at target land (as formed)	125-200 [5-8]	100-200 [4-8]	75-250 [3-10]
b	Microvia diameter at capture land (as formed, no plating)	350/14	300/12	250/10
b-1	via in SMT pad width	300/12	250/10	250/10
c	landing pad diameter	350/14	300/12	250/10
d-1	conductor/landing pad spacing on rigid innerlayer	125/5	100/4	75/3
d	pad to pad spacing on innerlayer	125/5	75/3	75/3
e-1	conductor line width on landing layer	125/5	100/4	75/3
e	conductor width on innerlayers	125/5	75/3	75/3
f	min. finished hole size - fhs (plated through-hole)	250/10	200/8	150/6
g, o	surface via pad (fhs + annular ring x 2) min.	fhs+350/14	fhs+300/12	fhs + 250/10
	through-hole pad diameter	600/24	500/20	400/16
h	trace spacing on rigid outerlayer	125/5	100/4	87/3.5
l	trace width on rigid outerlayer	125/5	100/4	87/3.5
k	fhs drill hole plane clearance on innerlayer (fhs + annular ring x 2)*	fhs + 700/28	fhs + 66/24	fhs + 500/20
	surface conductor to unplated hole	250/10	200/8	200/8
n	min. unplated hole diameter	350/14	300/12	300/12
m-1	min. HDI dielectric thickness	75/3	62.5/2.5	50/2
ar	Min. aspect ratio, (m-1)/a	< 1.0	1.0	1.0
z	min. board thickness	725/29	600/24	500/20
m	min. core thickness	100/4	62.5/2.5	50/2
p	min.prepreg thickness	100/4	62.5/2.5	50/2
i	min. plated thickness	25/1	25/1	30/1.2

FIGURE 25.5 Typical HDI design rules with corresponding dimensional symbols for IPC-2226 figures. Illustrated is an IPC Type III HDI structure for categories A, B, and C. (*Source IPC-2226, "Design Standards for HDI and Microvias."*)

25.4 DESIGN

HDI and microvias place a new burden on printed circuit design. The various IPC types impose significant changes in the multilayer stack-up from a conventional board. But additionally, microvias can be implemented in many different ways and with different design rules. This section presents just a few of the design issues.

25.4.1 Multiple Layers of Microvia Holes

For interconnecting IC substrates with hundreds of I/O terminals, a single layer of microvia holes may not be sufficient to satisfy interconnection requirements. Double, triple, or even quadruple microvia hole layers may be necessary whether the board is a motherboard or a chip package substrate. When microvia holes are made only between adjacent layers (see Fig. 25.6), all three microvia processes—photovia, plasma via, and laser via—can be used. However, when a design requires microvia holes that must connect beyond adjacent layers—such as L1 and L3 (skipvia)—laser via processing is the only practical option.

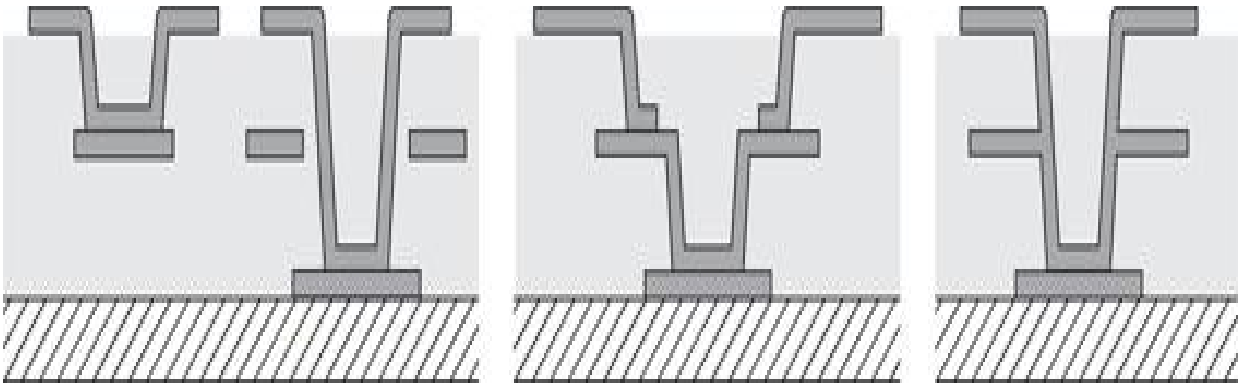


FIGURE 25.6 Microvia connections beyond adjacent layers.

25.4.2 Design Tools

Printed circuit design has become one of the most important functions in the electronic product realization process.[6] The demands on printed circuit design keep mounting. The reasons for this increasing demand include the following:

- To regain time for product schedules
- To lower the cost of fabrication and assembly
- To enable new area-array components, such as chip scale packages (CSPs), micro-BGA, and flip-chip interposers
- To decrease the time to market
- To improve electrical performance for high frequency and to reduce EMI

Bringing the process back under control requires a methodology that involves planning the printed circuit layout process with predictive wiring density models. The other benefits include reducing printed circuit fabrication and assembly costs.

25.4.2.1 Required Features of HDI CAD Toolsets and Autorouters. A partial list of features that computer-aided design (CAD) tools require to design HDI boards includes the following:

- Optimization of a mixed via by a router
- Autorouting of cost budget for mass via generation
- Buried or blind via control on the layer
- Via padstack control (landless)
- Staggered via control
- Pad within pad
- Blind via push/shove during manual routing
- Any angle routing
- Manufacturing process rules at all design phases
- Buried components

Some of these features have already been discussed in previous chapters.

25.4.2.2 Autorouters. Autorouters have been a part of printed circuit design systems for many years. An autorouter will automatically place vias and traces on the printed circuit based on the schematic and part geometries. Elaborate configuration menus drive the appropriate placement of these features. A special autorouter is required for HDI structures, because many HDI processes employ mass via generation as used for SLC technologies. These processes produce all the vias simultaneously and at any desired diameter. Since the cost of vias is rather insignificant, the autorouter should have the capability of achieving a near-zero via cost. When the routing is done, a different but more optimized design results.

25.4.3 Trade-Off Analysis

After a product has been partitioned, the circuit has been designed, and the components have been selected, the physical design must be planned with an eye toward achieving the lowest manufacturing cost while meeting all

performance and operating boundary conditions. This is especially true for HDI designs. Conventional through-hole printed circuit design has not changed too much over the years. Finer geometries, more layers, and surface mounting have been added, but the conventional design process remains essentially the same. Microvias and HDI, however, introduce many changes to the design process and require new design rules and layer structures. Experience and history will not help here. The unfortunate truth about printed circuit layout is that there is an almost infinite number of combinations of layer structures and design rules that can satisfy the schematic and bill of materials. With all these choices, especially the new ones that HDI offers, a trade-off tool is required to find the best set of design rules and features that allows the rapid design of a printed circuit board, is producible, and meets all the performance expectations while providing the lowest total manufacturing costs. When used early in the design process, before the actual physical design of the printed circuit, the tools require predictive models that can anticipate cost and performance. Information and processes for planning a HDI design can be found in Chap. 19 of this handbook. Trade-off information of through-hole density and relative costs can be seen in Fig. 25.2.

25.5 DIELECTRIC MATERIALS AND COATING METHODS

This section provides an overview of the dielectric and applied conductive materials used in microvia and via filling. Some of these materials can be used in both IC chip carrier and PWB HDI applications. The discussions are focused on the HDI PWB arena and on materials for which information is readily available. In Sec. 25.5.2, cross-references are made

to the relevant material specifications of the IPC/JPCA-4104 specification for HDI and microvia materials. A brief material roadmap discussion is included to illustrate material property trends.

Figure 25.7 shows the compatibility of laser via, photovia, and plasma via methods with four basic surface dielectric structures on which microvia holes are to be formed. Although laser via methods can cope with all four dielectric structures, photovia and plasma via methods are applicable to only one structure, respectively, as shown in the figure. This is one reason why laser via is more widely used today. Another wiring layer is built over the existing microvia holes, which become buried via holes (BVHs).

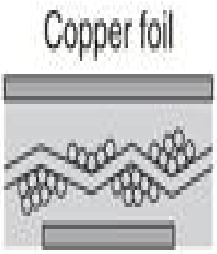
	Standard configuration 	RCC	Thermally curable resin	Photoimageable resin
Photovia	X	X	X	O
Laser via, CO_2	O	O	O	O
Laser via, yag	O	O	O	O
Plasma via	X	O*	X	X

FIGURE 25.7 Compatibility of via hole formation methods with four basic dielectric layer structures.

The specification IPC-4104 will define material requirements for HDI applications. This IPC specification applies only to the *surface HDI layers*, the conventional multilayer core materials are covered by IPC specification IPC-4101B.

25.5.1 Materials for HDI Microvia Fabrication

Figure 25.8 shows a material and technology selection flowchart for use when choosing dielectric materials. In using the flowchart, you should ask the following questions regarding the dielectric you are considering:

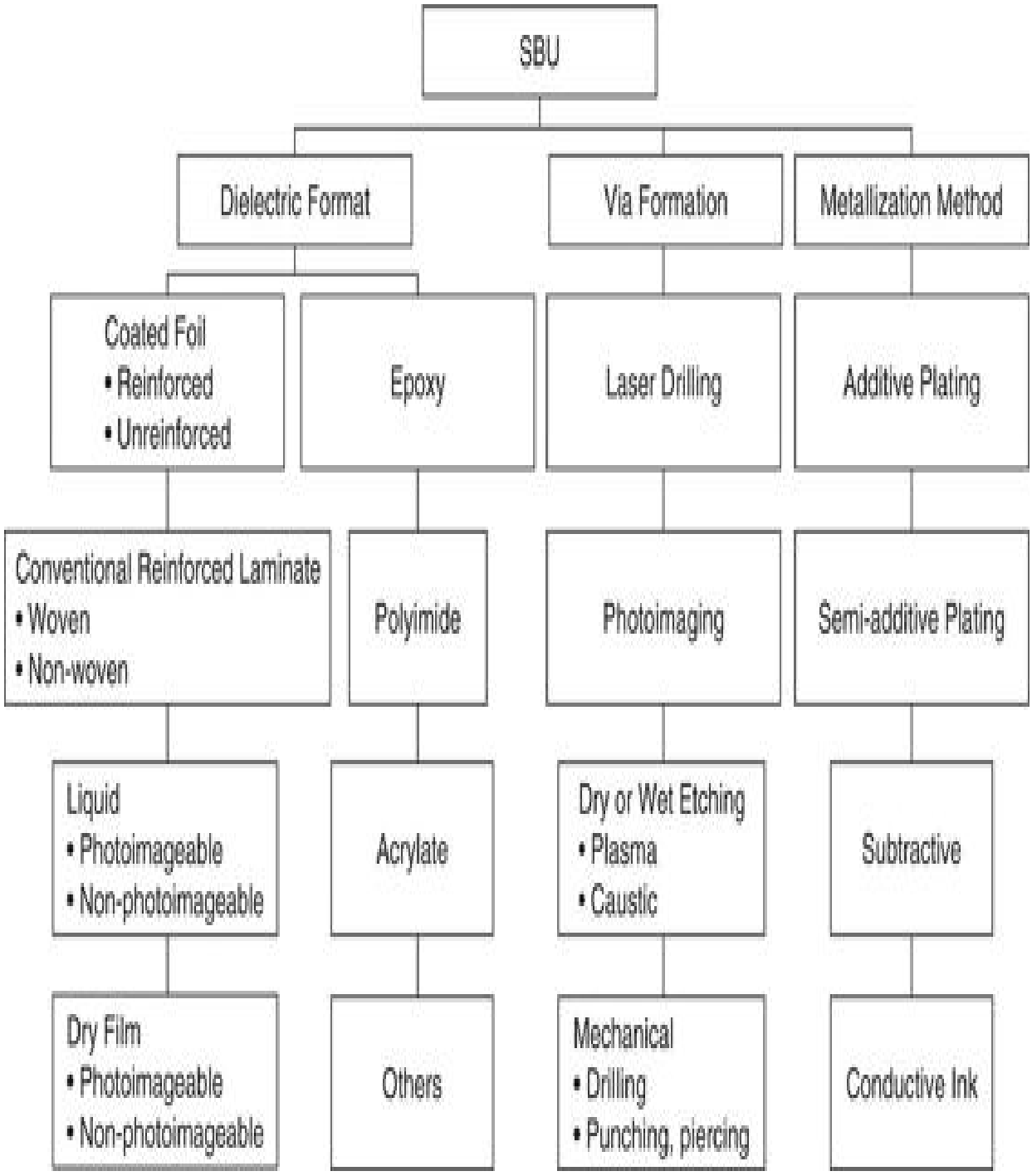


FIGURE 25.8 Material and technology choices for SBU fabrication. (*Courtesy of DuPont*.)

- Will the dielectric use chemistry compatible with current chemistry used by core substrate material?

- Will the dielectric have acceptable plated copper adhesion? [Many original equipment manufacturers (OEMs) want ≥6 lb/in (1.08 kgm/cm) per 1 oz (35.6 μm) copper.]
- Will the dielectric provide adequate and reliable dielectric spacing between metal layers?
- Will it meet thermal needs?
- Will the dielectric provide a desirable "high" T_g for wire bonding and rework?
- Will it survive thermal shock with multiple SBU layers (i.e., solder floats, accelerated thermal cycles, multiple reflows)?
- Will it have platable, reliable microvias (i.e., will it have latitude to ensure good plating to the bottom of the via)?

25.5.1.1 Copper-Clad Dielectric Materials. Due to relative ease of implementation, copper-clad dielectrics are used on a larger scale than unclad dielectrics. Copper-clad dielectrics provide a method that requires the least number of changes in manufacturing flow because they typically use the same dielectric and reinforcements found in standard PWBs. Copper-clad-based materials have a longer history in making blind vias than any other method. This makes many designers, OEMs, and PWB fabricators more comfortable with copper-clad-based materials.

These materials can be nonreinforced or reinforced. The reinforcement can be woven or nonwoven and can be aramid, glass, and so on. These dielectrics are suitable for via formation by laser or other mechanical removal methods.

Due to its wide availability and familiarity, FR-4 material is often initially evaluated in laser-drilling microvias. Reinforced with thin 106 or 1080 woven glass (since thicker glass is more difficult to vaporize with lasers, but there is 1086 uniform-woven glass just for laser ablation), one- or two-ply

laminates are selected with a resin content close to 70 percent. The “laser drilling” is done by ablation of the via using a conformal mask or a directly focused beam, with either an ultraviolet (UV) Nd:YAG or a CO_2 laser. These materials may also be coated on a copper foil. Typical applications use single-side-clad material where the copper clad is used as the outer layer and the C stage is bonded to the subcomposite. These materials are suitable for via formation using methods such as plasma or laser. To meet fine circuitry and smaller via needs, very thin copper is available. Another approach, practiced by many Asian PWB fabricators, is to thin down incoming copper clad by etching and/or planarizing the copper surface precisely.

25.5.1.2 Unclad Dielectric Materials. If the dielectric is reinforced, microvias are formed by laser drilling or other mechanical means. If it is nonreinforced, it can be photoimageable in addition to the previous choices. To add conductivity, subtractive processing is the standard manufacturing practice in the United States and Europe. Semi- or fully additive techniques have been practiced in continuous high volume only in Asia, most notably Japan. In Japan, which leads the world in microvia production, about 22 percent of manufacturing begins with a non-copper-clad dielectric material.

Japan has long accepted the additive manufacturing methodology for creating circuits on the board surface as well as the through-hole connection.

The trade-off between clad and unclad dielectric materials follows a benefit analysis similar to that used for subtractive versus additive processing. Copper-clad-based material is fabricated using standard practices familiar to most shops. However, it innately generates more waste and has a higher cost due to the subtractive nature of the manufacturing sequence. In addition, copper-clad materials demonstrate

limitations in fine-line capability similar to those seen with standard manufacturing methods used today.

Unclad dielectrics require considerable resources for optimized plating of copper to achieve reliable and consistent copper peel strengths. Unclad dielectrics and thin copper-clad dielectrics, however, gain in importance as the requirements for line and space geometries reach ≤75 µm and required via sizes are lower than 75 µm in diameter. Figure 25.9 depicts the influence of base copper on the aspect ratio of a via. The base copper increases the aspect ratio, making it more difficult to plate the via, and can cause issues with bottlenecking whereby the via plates shut at the top without sufficient plating in the bottom. Other data show that thinner copper etches more uniformly, which helps the cause for controlled impedance.

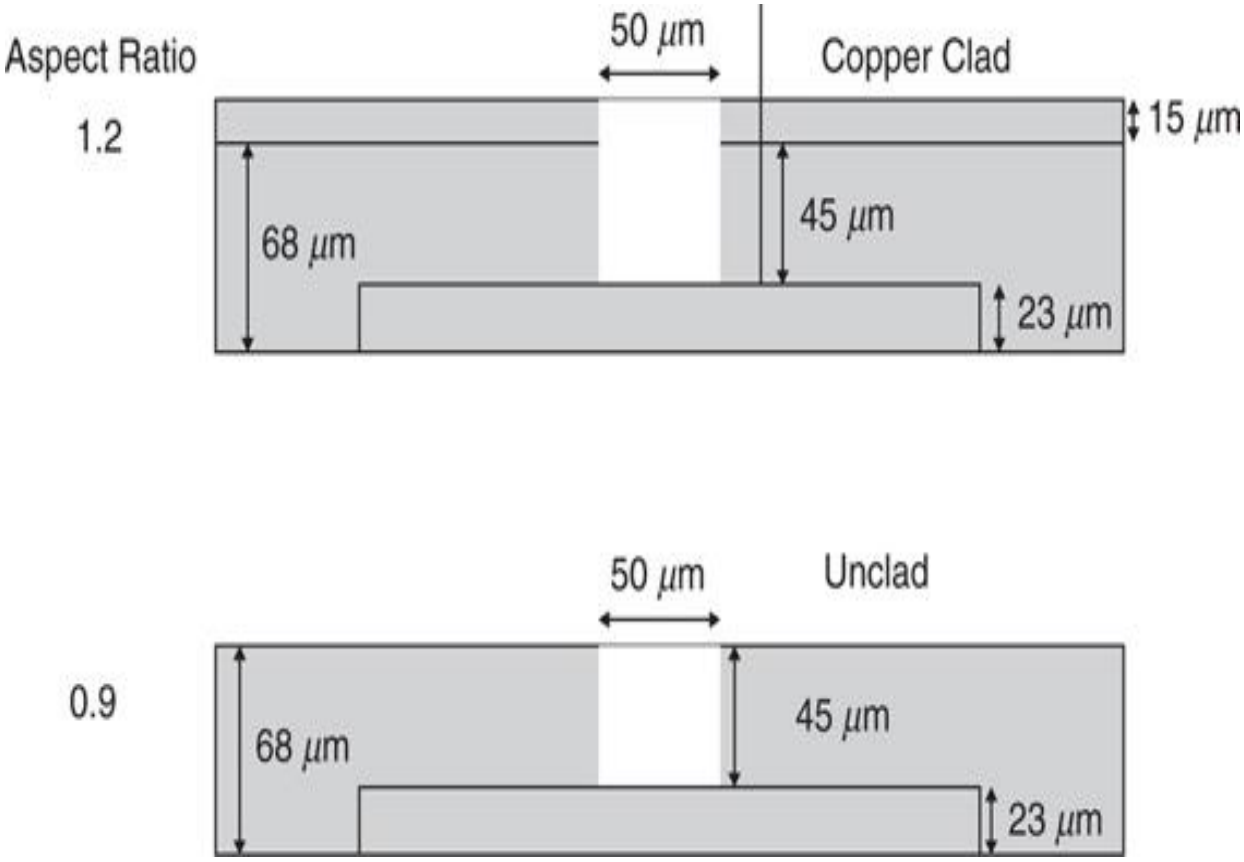


FIGURE 25.9 Impact of 1.2 oz base copper on the aspect ratio of a 50-µm via. (*Courtesy of Vantico*.)

25.5.1.3 Clad versus Unclad Dielectric Materials.

Table 25.3 compares the utilization of clad versus unclad dielectric materials as circuit geometry shrinks. This table shows that as the technology requirements get tougher, the trend toward using unclad dielectrics increases. As line and space requirements get denser, and via diameters get smaller, requirements for chip package substrates to use unclad or thin copper dielectrics increase. In the case of mobile phones and other portable applications, for example, it is foreseen that by the year 2015 lines and spaces will be down to 5 to 15 µm, respectively, and via sizes to 10 µm, with a subsequent high usage of unclad material.

TABLE 25.3 Utilization of Unclad Dielectrics by Key Market Segments[4]

	Chip Package substrates	Cellular, Camcorder, PDA	Computer/ Telecommunication*
HDI penetration	High	High	Low
Line/space and via diameter (year 2013)	10-µm lines and spaces; 25-µm via diameter	50-µm lines and spaces; 100-µm via diameter	100-µm lines and spaces; 125-µm via diameter
Use of unreinforced dielectrics	High	High	Low
Use of unclad dielectrics	High	Med, but increasing	Low

*Excluding laptop computers.

25.5.2 Examples of HDI Microvia Organic Substrates

From a mechanical standpoint, materials may be grouped as reinforced and nonreinforced laminates and prepregs, as in Fig. 25.8. Reinforced materials are generally better in dimensional stability, lower in coefficient of thermal expansion (CTE), and less sensitive to thermal cracking, whereas nonreinforced materials often have a lower dielectric constant (D_k) and may be photoimageable. This can be seen in Fig. 25.10, which shows the D_j versus D_k (at 1 MHz) of various resins and reinforcements.

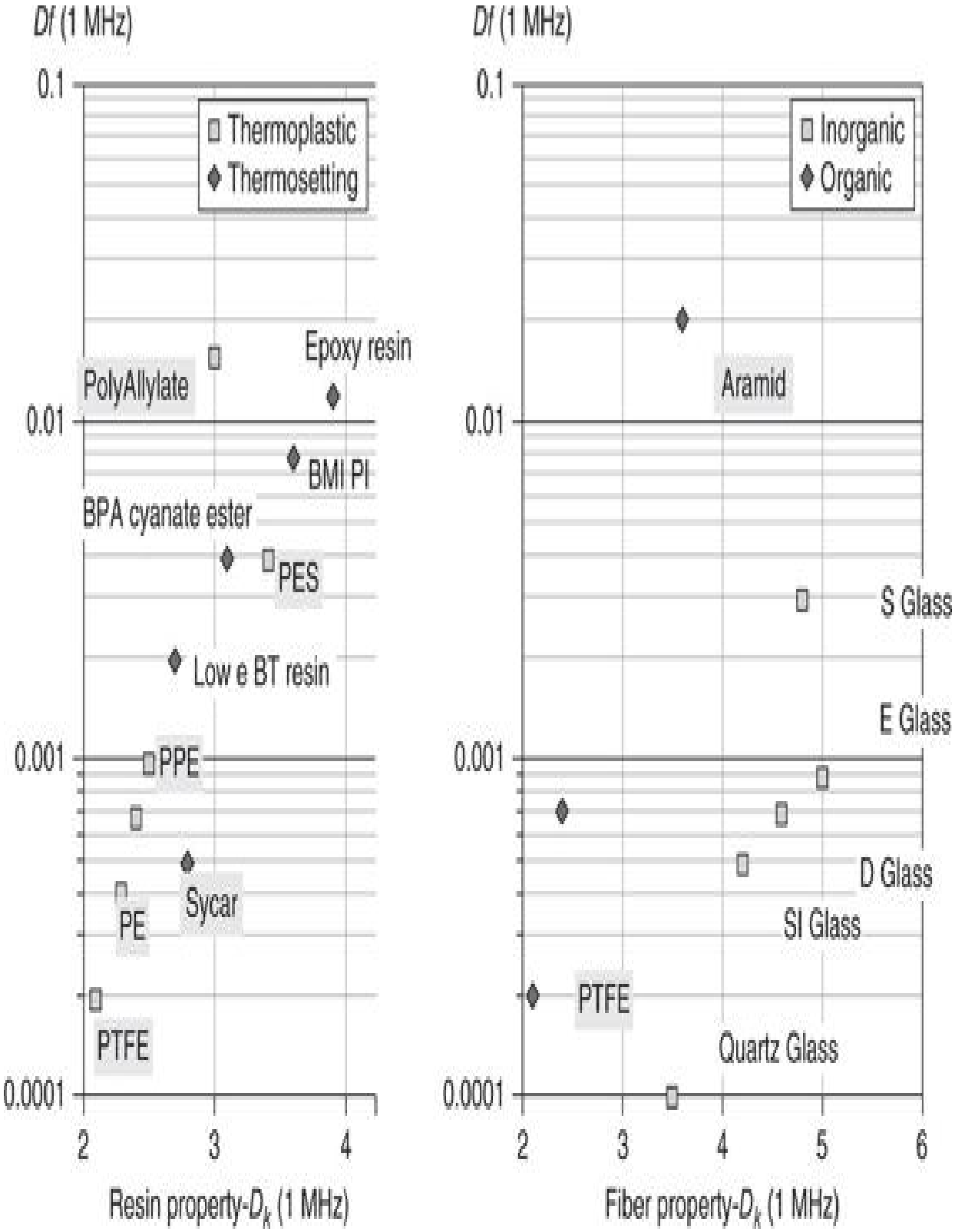


FIGURE 25.10 Dielectric options of resins and reinforcements by dissipation factor (D_j) versus dielectric constant (D_k). (*Source: Holden Consulting*.)

25.5.2.1 Nonreinforced Dielectric Materials. Nonreinforced dielectric materials include resin-coated copper foils, unclad photoimageable dielectric materials, and non-photoimageable dielectric materials.

25.5.2.1.1 Resin-Coated Copper Foils. Resin-coated foils are the most common materials used for build-up multilayer microvia applications. Many product variations are available and fit well within the existing multilayer-manufacturing infrastructure. Epoxy-based coated foils are the most common and have performance properties similar to FR-4 but with no glass reinforcement. Peel strengths, thermal performance, and electrical properties are excellent. A variety of other resin systems are also being developed and starting to be used for coated foil build-up applications. Resin-coated foils come in two general types with either one or two resin layers. One-pass coated foils have a single B-stage layer designed to flow, fill, and provide thickness control at the same time. Two-pass-coated foils have a C-stage resin layer adjacent to the foil and a B-stage layer for flow and fill. The fully cured C-stage layer acts as a “stop” during the lamination process, typically enabling better thickness control. Resin-coated foils are available in a variety of thicknesses, yielding between 1.0 mil (25 micron) and 3.0 mil (76 micron) thick, finished dielectric layers. Copper foils most commonly used are 1/2 oz (18 micron) and 3/8 oz (13.34 micron), but there is substantial interest in thinner copper foils for improved laser efficiency and better fine-line circuitry definition.

25.5.2.1.2 Other Resins. Since build-up technology is still in its relative infancy but evolving rapidly, many different and diverse approaches are being investigated for the resins used and variations on the via-formation process. Low-D_k/D_j resins such as polyphenylene ether (PPE) are being used to address signal speed and integrity demands in resin-coated foil build-up structures. Another approach is to use additively plateable resin and use the copper as a sacrificial carrier,

eliminating the need to laser through copper. An additively plateable resin has the characteristic of high surface adhesion to electroless copper or direct metallization. The sacrificial foil makes it compatible with normal multilayer lamination processes, saving the need for expensive coating machinery, while also protecting the thin dielectric from harm until it is laminated to the printed circuit. This also gives excellent surface topography for good peel strength. The properties of a resin-coated foil are given in Table 25.4. See IPC- 4104 specification sheets 12, 13, and 19 through 22 for more complete material performance information.

TABLE 25.4 General Properties of Resin-Coated Copper (RCC)

	Units	Via Foil	Conditioning
Dielectric constant at 1 MHz	—	3.4	C-24/23/50
Dissipation factor at 1 MHz	—	0.0205	C-24/23/50
Electrical strength	V/mil	1776	D-48/50
Insulation resistance	MΩ	2.65×10^5	C-96/35/90
Surface resistivity	MΩ	6.60×10^8	E-24/125
Surface resistivity	MΩ	4.71×10^8	C-96/35/90
Volume resistivity	MΩ-cm	7.17×10^7	E-24/125

Source: Allied-Signal.

Laminate suppliers should be contacted when special needs arise, as the resulting composite will require understanding of fabrication and design issues.

Resin-coated foils come in two general types:

- One-pass coated foils have a single B-stage layer designed to flow and fill and to provide thickness control,

all at the same time.

- Two-pass coated foils have a C-stage resin layer against the foil and a B-stage layer for flow and fill. The fully cured C-stage layer acts as a “stop” during the lamination process, typically enabling better thickness control.

With the exception of the laser process, all the basic technology to produce SBU using resin-coated foil is the same as, and found in, most multilayer PWB production operations.

Another alternative is to use additively platable resins. In this approach, the copper foil acts as a sacrificial carrier. The process is similar to that described earlier, but the first step after lamination is to etch off all the copper chemically. This eliminates the need to laser through copper and makes acquisition of registration targets simpler. The structure left behind by the copper also gives excellent surface topography to the resin for good peel strengths from the subsequent additive plating step. This approach allows for extremely fine feature definition and much greater laser efficiency.

25.5.2.1.3 Unclad Nonreinforced Photoimageable Dielectric Materials. Material chemistry options for this group include epoxies, epoxy blends, polynorbornenes, and polyimides. They can be applied as liquid or dry film, negative or positive imaging, and can be solvent or aqueous developable. To improve the dielectric’s adhesion to copper, most dielectric suppliers require a copper pretreatment with a black oxide or conversion coating (oxide replacement) prior to application of the dielectric. Most of these materials are either epoxy or epoxy- and novolac-based to provide high T_g and good plating, and most provide adhesion values for plated copper of at least 1.1 kg/cm at a 25-µm copper thickness. Typically these dielectrics are metallized using conventional solvent swell and permanganate etching techniques. The liquid materials use only safe solvents

(those not known to lead to harmful health effects with prolonged exposure. Typical microvias are seen in Figs. 23.27, 29.5, and 29.12.

A unique advantage for photoimageable materials is that the speed used to make small or large vias is the same. With the growing need to make embedded reactives (passives), large rectangular areas need to be opened up to place these devices. Currently, this is only economical with photoimaging. Most photoimageable materials are easy and fast to laser-drill because they are nonreinforced. See IPC-4104 specification sheets 1, 2, 7 through 10, and 16 for more complete material performance information. A partial list of available materials is shown in Table 25.5. Properties of photodielectrics can be seen in Tables 25.6 and 25.7.

TABLE 25.5 Partial List of Six Photodielectrics Available on the Market

Ciba	Probelec™ 81/7081 liquid dielectric
Dupont	ViaLux™ 81 photodielectric dry film
Enthone-OMI	Envision® PDD-9015 photodefinable liquid dielectric
MacDermid	MACu Via-C photodefinable liquid dielectric
Shipley	MultiPosit 9500 CC liquid dielectric
Morton	DynaVia2000™ photoimageable dielectric dry film

TABLE 25.6 Comparison of Four Photoimageable Dielectrics for Electrical and Mechanical Properties *(Courtesy of Holden Consulting)*

Factors	Epoxy	Acrylate	Polyimide
Cost	Excellent (+2)	Excellent (+2)	Poor (−1)
Processability	Excellent (+2)	Excellent (+2)	Poor (−1)
Performance:			
MIR	Good (+1)	Fair (0)	Fair (0)
D_k	Fair (0)	Fair (0)	Good (+1)
T_g	Fair-good (0)	Poor (−1)	Excellent (+2)
CTE	Good (+1)	Poor (−1)	Excellent (+2)
% Moisture	Good (+1)	Good (+1)	Poor (−1)
Adhesion on lam.Cu	Excellent (+2)	Good (+1)	Poor (−1)
Deposited Cu adhesion	Good (+1)	Good (+1)	Poor (−1)
Overall rating	+10	+5	0

Key: Excellent = +2, Good = +1, Fair = 0, Poor = −1

TABLE 25.7 Partial List of Liquid and Film Dielectrics for HDI Available on the Market

	Product A	Product B	Product C	Product D
Product	L-PID, Neg.	L-PID, Neg.	L-PID, Neg.	DF-PID, Neg.
Material	Epoxy	Epoxy	Polyimide	Epoxy
Insulation resistance		1–10 E+13^		8 E+13Ω
MIR		1–4 E+9Ω		1.5 E+11Ω
D_k @ 1 MHz	3.2	4.0–3.4	2.8	3.4
10 MHz				4.1
1 GHz				4.2
Loss factor @1 MHz	<0.01	0.02	0.004	0.007
1 GHz		0.015		0.01
Breakdown voltage (between layers)		>2000		
E-migration	Pass	Pass		Pass
T_g	140–180°C	135°C	300°C	170°C
Peel Strength	>9 N/cm	14 N/cm		
	>5 lb/in	8 lb/in		
TCE (ppm/°C)	60–70	60–70		60–70
Tensile modulus		3000–3500 N/mm²		4.0 E+5 psi

25.5.2.1.4 Nonphotoimageable, Nonreinforced Dielectric Materials. This group can be laser-drilled, plasma-etched, and/or mechanically treated to form microvias. As stated earlier, many of the photoimageable dielectrics are laser-drillable.

As with the photoimageable group, to improve the dielectric's adhesion to copper, most dielectric suppliers require a copper pretreatment with a black oxide or

conversion coating (oxide replacement) process. See IPC-4104 specification sheets 6, 11, 17, and 18 for more complete material performance information. A partial list of materials is seen in Table 25.8.

TABLE 25.8 Partial List of Commercially Available Nonphotoimageable, Nonreinforced Dielectric Materials and Their Suppliers

Osada Ajinonomoto	ABF dry film
Tamura	TBR-25A-3 thermoset ink
Taiyo	HBI-200BC thermal cure ink
MacDermid	MACuVia-L liquid dielectric
Enthone-OMI	Envision® liquid dielectric
3M	Electronic bonding film
B. F. Goodrich	Polynorbornene liquid dielectric

25.5.2.2 Reinforced Dielectric Materials. Copper-clad dielectrics for HDI can be rein- forced, as in FR-4, or unreinforced, as in coated copper foil. The dielectrics can be epoxy, as in FR-4, or polyimide, cyanate ester, bismalene-triazine (BT), PPE, or PTFE. Reinforcements are typically glass cloth, but there are a variety of glass as well as aramid paper and exotic fibers such as quartz or carbon fiber.

25.5.2.3 Laser-Drillable, Woven-Glass Laminate. A new family of prepregs for HDI consists of uniform-glass prepregs such as 1086 and 1087 glass. This glass is a thinner fabric than the typical 1080 glass cloth; it has more glass plies but they are spread uniformly across the fabric. Table 25.9 describes the differences between the conventional 1080 glass cloth and the 1080 LD (laser-drillable) and the new 1086 LD prepreg. Figure 25.11 shows these two glass prepregs. Table 25.10 compares the performance of RCC, conventional 1080 prepreg (PP), and the new 1086 LD

prepreg, whereas Fig. 25.12 shows laser-drilled microvias in the two different prepregs. Additional details can be found in Chaps. 10, 11, and 12 of this Handbook.

TABLE 25.9 Comparison of Conventional 1080, 1080 LD, and the New 1086 LD Prepregs *(Courtesy of NanYa Plastics)*

Fabric Type	Base Weight (g/cm^2)	Resin Content	Warp × Fill (W + F)	Warp	Width	Fill	Width	Thickness	
				mm	mil	mm	mil	mm	mil
1080	48	62	60 × 48	0.19	7.48	0.264	10.39	0.057	2.24
1080 LD	48	62	60 × 48	0.280	11.02	6.44	17.3	0.045	1.77
1086 LD	55	62	60 × 61	0.288	11.3	0.395	155.7	0.045	1.77

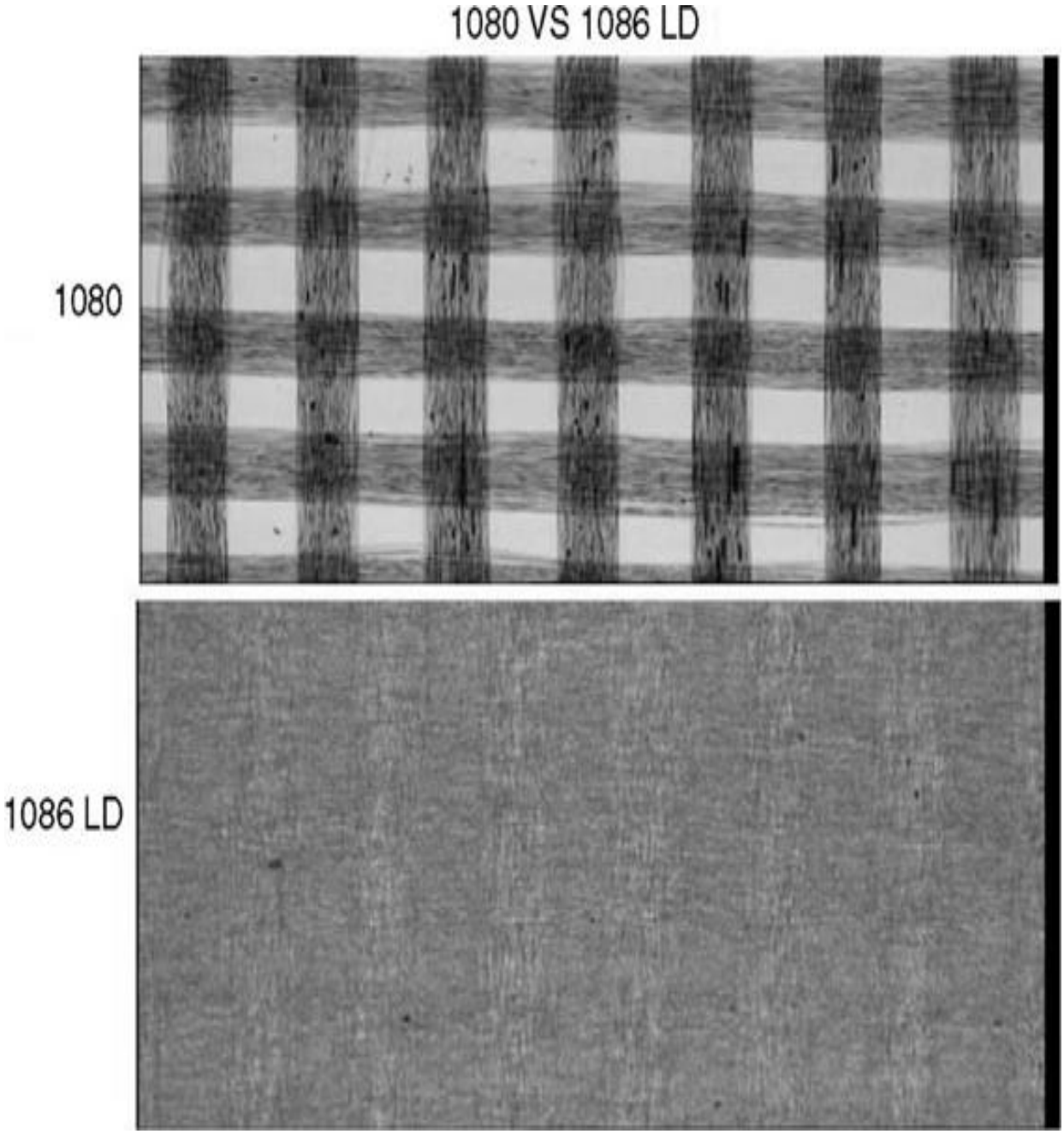


FIGURE 25.11 Photos of conventional 1080 prepreg and the new laser-drillable 1086 LD uniform-glass prepreg. (*Courtesy of NanYa Plastics*.)

TABLE 25.10 Comparison of the Performance of RCC, Conventional Prepregs, and the New Laser-Drillable 1086 LD Glass Prepreg *(Courtesy of NanYa Plastics.)*

Build-Up Layer	RCC	Convention P/P	1086 LDP
Dimension stability	Poor	Good	Better
Thickness control	Poor	Good	Good
Surface smooth	Good	Good	Better
Rigidity	Poor	Good	Good
Handling	Good	Good	Good
Drill ability	Excellent	Poor	Good

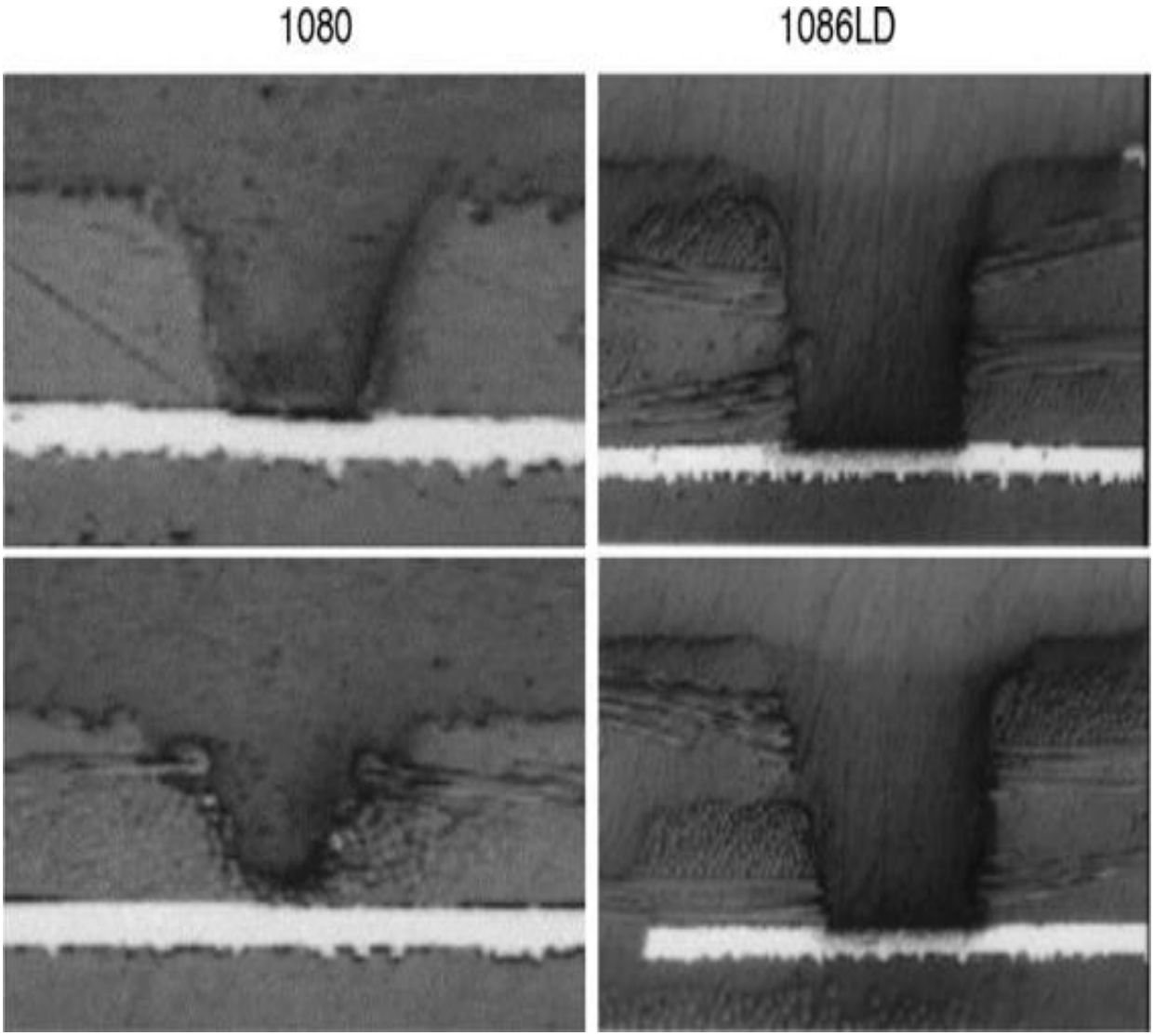


FIGURE 25.12 Photos of cross sections of laser-drilled vias in conventional prepregs and the new, uniform, laser-drillable 1086 LD prepregs. (*Courtesy of NanYa Plastics*.)

25.5.2.4 Aramid-Reinforced, Nonwoven, Nonglass Laminate.

In 1965, scientists at DuPont discovered a method for producing an almost perfect polymer chain extension using the polymer poly-p-benzamide. The key structural feature of this molecule is the paraorientation on the benzene ring, which allows it to form rod-like structures with a simple repeating molecular backbone. The term *aramid* now refers generically to organic fibers in the aromatic polyimide family. Kevlar was the first para-aramid fiber to become familiar, due to its use in bullet-resistant vests and as a lightweight, high-strength structural reinforcement. Aramid- reinforced prepregs and laminates have proven their functionality for a number of years in high-reliability applications and more recently in consumer electronics.

The low CTE of aramid non-woven reinforced prepreg and laminate provides a closer match to the CTE of the silicon chip. Depending on the type of resin and the resin and copper content of the laminate and the prepreg, the CTE of the PWB can be tailored to between 10 and 16 ppm/°C (Fig. 25.13). This allows the designer the option of finding a best fit of the CTE of the PWB to the CTE of the components.

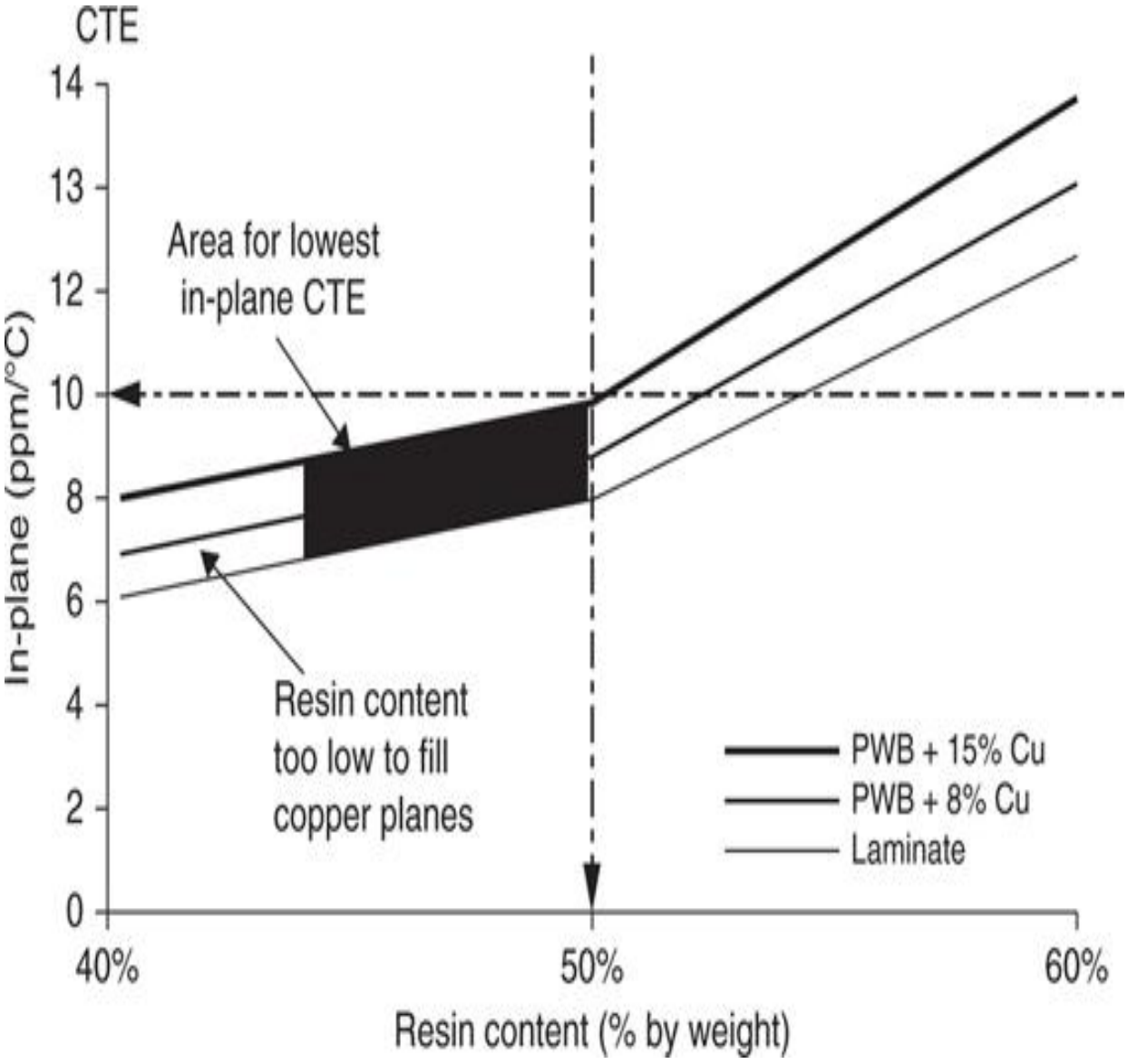


FIGURE 25.13 Impact of copper and resin content on in-plane CTE. (*Source: DuPont*.)

Reliability can be designed in by PWB designers, as they know which component packages are used, what the CTE requirements of these packages are, and what the life-expectancy requirements of the electronic equipment are. The ability to tailor in-plane CTE has made nonwoven aramid-reinforced PWBs one of the most favorable material options for avionics, satellites, and telecom applications where long life expectancy and high reliability are needed. In

mobile phone applications, where chip scale packages (CSPs) are commonly employed, low-CTE nonwoven aramid reinforcement extends solder joint life as much as three times over FR-4 and resin-coated foil (RCF). After more than 1000 thermal cycles (−40 to +125°C), nonwoven aramid-reinforced epoxy resin does not crack, as is common with nonreinforced dielectrics.

Aramid-reinforced laminate and prepreg allow fast microvia hole formation and at the same time maintain the performance characteristic of a smooth surface for fine-line conductor imaging. The ablation speed of nonwoven (aramid) laminates and prepregs is close to that achieved when using nonreinforced materials such as resin-coated foil, dry film, or liquid dielectrics. Since aramid laminates are very stable, they allow the fabrication of double- sided, very thin, etched innerlayers, which are then pressed to a multilayer package in a single pressing cycle. Thus, these thin innerlayers can be processed in parallel. Aramid-reinforced material is a cost-effective alternative when laser hole formation is used to form single- and multiple-layer interconnects, and is compatible with FR-4 materials used in the core of aramid–FR-4 mixed constructions. Laser drilling of stepped microvia holes is accomplished in one subsequent operation (see Fig. 25.14). This allows the designer to interconnect up to four layers on each side of the inner core without sequential processing—a substantial productivity advantage for the PWB fabricator that results in the lowest possible manufacturing cost. See IPC-4104 specification sheets 5 and 23 for more complete material performance information.

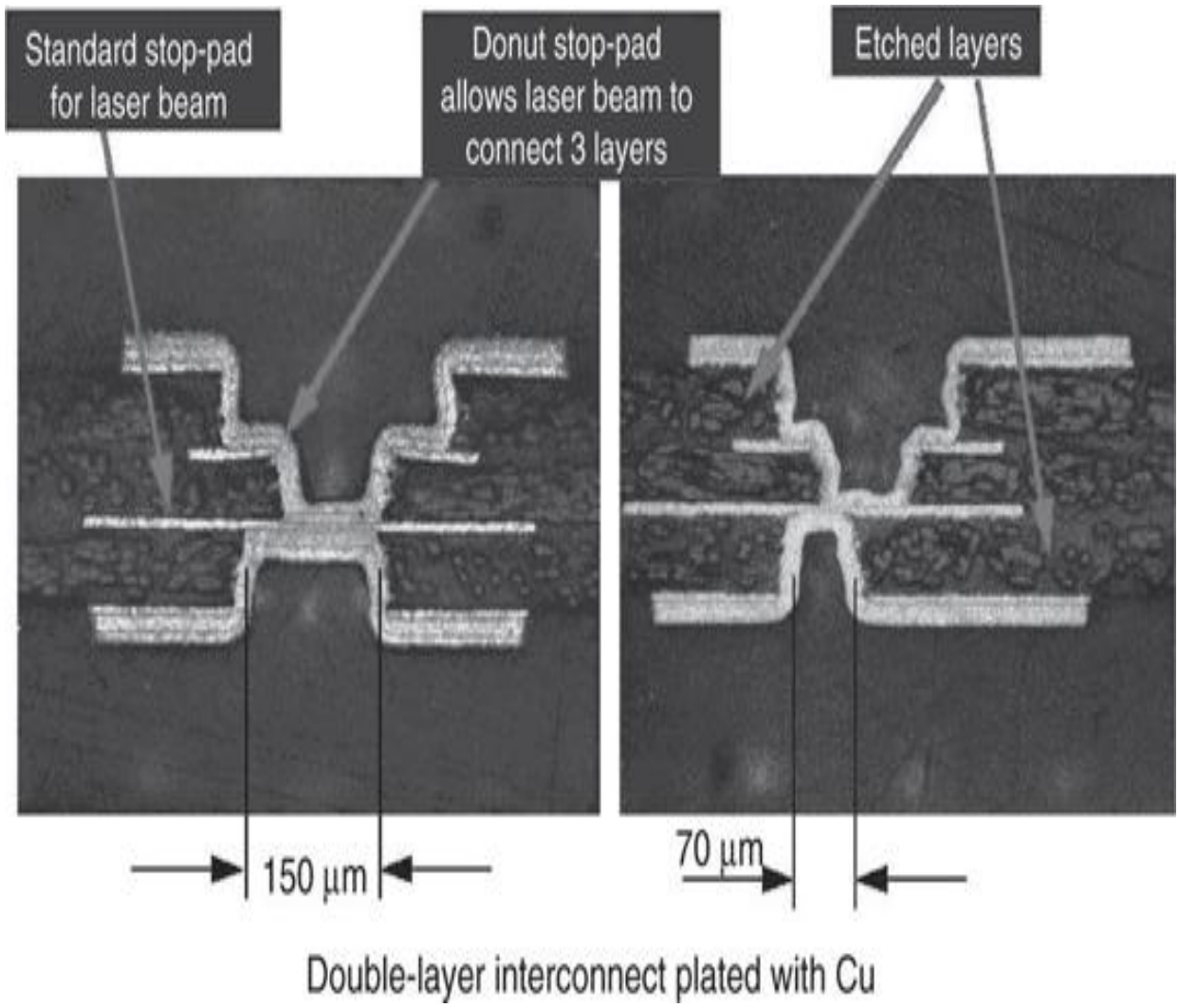


FIGURE 25.14 Photos of conventional and skip-microvias laser-drilled in Thermount materials. (*Courtesy of DuPont*.)

25.5.3 Via Filling

The demand for filling of through holes with epoxy resin or conductive paste has been rising ever since surface-mount technology became widely adopted in the PWB industry.

25.5.3.1 Basics. Following are the traditional examples of the types of applications that require via filling processing capability:

- Preventing acid residue from attacking the Cu plating at the through-hole opening, which can in turn cause an open circuit
- Averting mishandling due to loss of vacuum during board-level assembly or during vacuum- assisted transport in production
- Avoiding blowout of flux and/or solvent residue during assembly and solder reflow
- Stopping flux from dripping from the through holes to the opposite side of the PWB
- Keeping solder resist ink from migrating into through holes during screen printing, which can cause formation of nodules at the through-hole opening during solder plating and/or gold plating
- Enhancing the planarity of solder resist on the surface of filled through holes and the planarity of core layer for SBU PWBs
- Improving the stability of solder paste printing volume for via-in-pad designs
- Preventing the migration of solder into through holes in via-in-pad designs

The filling of through holes with nonconductive resin and conductive materials using dispensing, screen-printing, and roll-coating methods has been extensively evaluated and tested. Of the three basic methods described earlier, screen printing is the most common process. It allows for efficient, selective filling of large numbers of through holes.

25.5.3.2 Via-Filling Materials. Selection of the proper resin-based material is the most important objective when using a screen-printing process to fill through-hole vias in build-up multilayer cores. In particular, the primary issues to be considered when choosing an appropriate fill material are

- Ease of printing

- Ease of grinding (planarizing)
- Adhesion to hole wall and panel surface

The most commonly used materials for permanently filling through holes include single- cure (thermal) resins, photoimageable dielectrics, conductive pastes, and the dual-cure (UV + thermal) epoxy resin utilized in the Noda screen flat plug process. Following are brief descriptions and comparisons of the characteristics of each of these types of via-fill materials.

25.5.3.2.1 Conventional Prepregs and RCC. In fabricating a base core with a pattern, the core panel is usually panel-plated and the pattern is made with a dry-film tenting process. Some fabricators seem to prefer pattern plating, however. The choice depends on the fabricator's familiarity with these processes. After the pattern is formed, dielectric material is laminated over the core (in the case of prepreg, with copper foil) and the holes can be filled with resins, depending on the plated hole diameter and the thickness of the core. It is generally agreed that when the diameter of plated holes is equal to or less than 0.3 mm *and* the core thickness is equal to 0.6 mm or less, these holes can be filled effectively by the lamination process (although the resin thickness of 80 µm is preferred in the case of RCC). See Fig. 25.15.

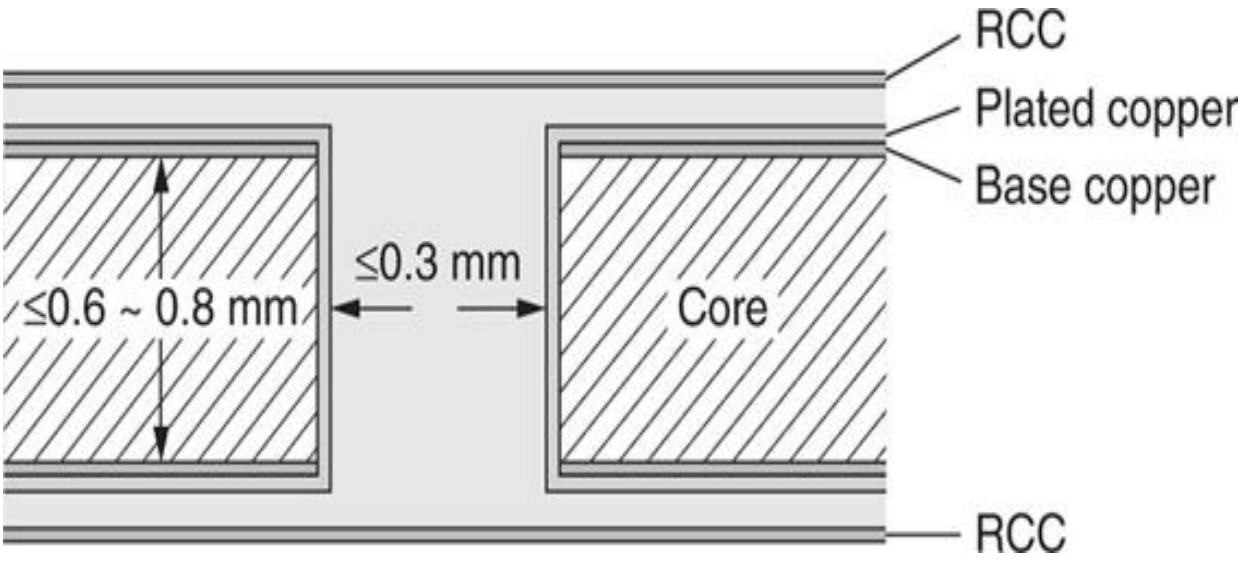


FIGURE 25.15 Conditions under which the through hole can be filled with resin by RCC lamination.

When the diameter/thickness conditions are not met, it is necessary to fill the holes using a separate process. A screening process does this from one side of the panel with polyester screen with an oversized hole pattern. After hole filling and curing the resin completely, the fabricator removes excess resin using a belt sander (#600 to #800) or a ceramic brush. Figure 25.16 illustrates the process. This is a tricky but necessary operation for microvia board makers, particularly for photovia processing.

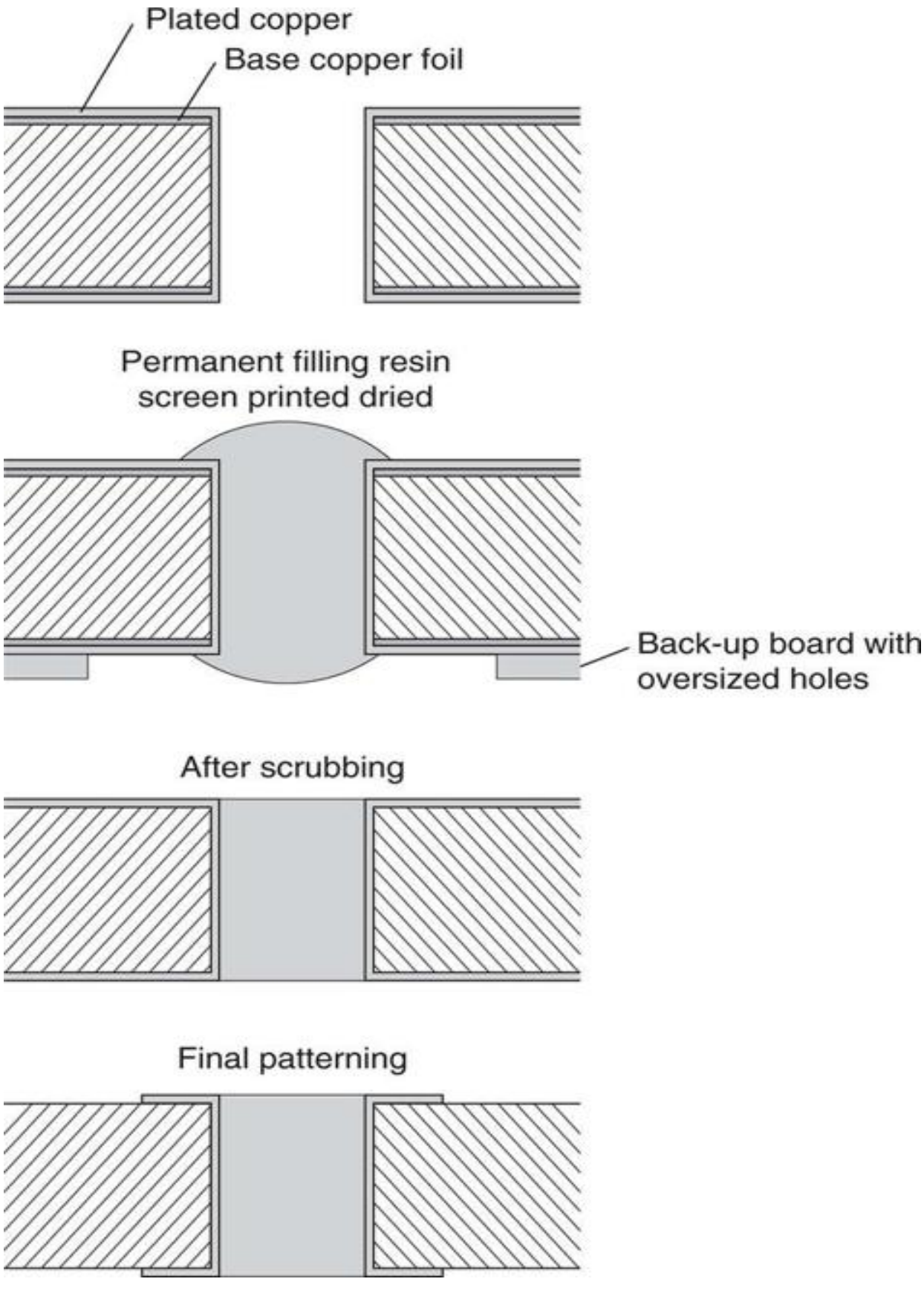

Plated copper
Base copper foil
Permanent filling resin
screen printed dried
Back-up board with
oversized holes
After scrubbing
Final patterning

FIGURE 25.16 Hole filling and surface scrubbing.

Hole filling is costly but yields a few advantages over simultaneous hole filling by lamination of RCC or prepreg. The edge of the plated holes is well protected; therefore, forming finer annular rings on the base core by tenting is easier. There is no concavity problem over the hole that can cause difficulties in later processes.

25.5.3.2.2 Dual-Cure (UV+ Thermal) Epoxy Resin. The main purpose for using a dual-cure epoxy resin is the stability of the B-cured material and the ease with which it can be removed by grinding during planarization. A homogeneous, semicured state can be reached because the liquid environment within the UV exposure system helps to control the temperature and stabilize the intensity of UV light. Furthermore, because the temperature of the liquid environment is kept low, the expansion of air bubbles that may have been trapped in the fill material at room temperature is prevented.

In formulating epoxy resin via-fill ink, one must consider the adhesion between the fill material and the copper plating in the hole barrel. Normally it may seem suitable to use a material that does not include an acrylic component. However, some suppliers have found it more beneficial to add an acrylic component because of its resistance to moisture absorption. They determined that it would be preferable to improve the ink's adhesion to copper by pretreatment with a black oxide or chemical etching process. This is similar to the approach taken by many dielectric suppliers.

25.5.3.2.3 Photoimageable Dielectrics. An advantage of a dielectric being photoimageable is that unwanted material is washed off during development, thus eliminating the planarization step. Typically, one screen pass is sufficient to fill or plug vias, but two passes can also be used to maximize hole filling. Standard screen-printing equipment is needed

with a bed-of-nails or dimple plate to maximize air release out of the plugged holes. If a squeegee is being used, single-sided application is recommended. Two coats are recommended to minimize the effects of material. Cores as small or smaller than 0.030 in (0.76 mm) require a secondary coating application.

25.5.3.2.4 Conductive Paste. In addition to the previous advantages of via filling stated earlier, conductive via fills also dissipate heat, increase electrical conductivity in the hole, and allow a via-in-pad design option (Fig. 25.17). The latter advantage is another way to recover real estate.

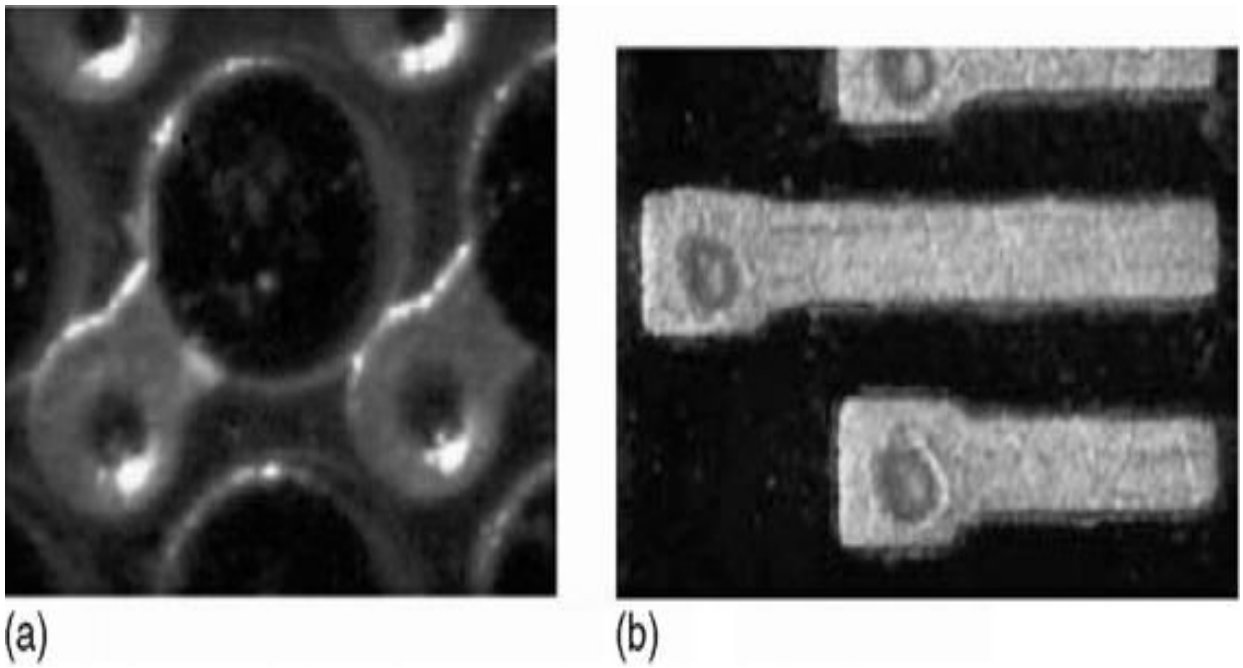


FIGURE 25.17 A via-in-pad option with conductive via fill: (*a*) traditional "dog-bone" design; (*b*) via-in-pad design. (*Courtesy of DuPont*.)

One example is a screen-printable paste made of silver, copper, and epoxy. The optimum mix of metal particle shapes and sizes bonded together with epoxy resin produces essentially zero shrinkage. In general, the plated or unplated through hole is filled with paste using a stencil-printing process. After drying and curing, the plugged through holes are planarized and plated to make them solderable. Some

typical design rules are an aspect ratio of 1:1 to 6:1 with vacuum assist, a via size of 6 to 25 mil (152 to 635 µm), and a core thickness of 6 to 85 mil (152 to 2159 µm). The product is extremely reliable during assembly.

25.5.3.2.5 Single-Cure (Thermal) Resin. Typically, thermally cured resins exhibit good adhesion strength to copper. Unfortunately, the rate of heat dissipation throughout the filled core material is unstable, making it difficult to achieve a reliable semicured state prior to planarization.

As a result, a rapid and unpredictable rise in temperature is likely to occur; as such, it is imperative to fill the holes completely, leaving no voids, if this type of material is to be used.

25.5.3.2.6 Solder Mask Ink. Using this type of material, it is relatively easy to fill the hole. However, the presence of volatile elements (solvents) and the degree of shrinkage during curing have a significant effect on the stability of the manufacturing process. In the case of small diameter through holes, the solvent residue may remain in craters or dishes at the mouth of the hole opening. Furthermore, the copper adhesion strength of these materials is typically lower than that of other hole fill materials.

25.5.3.2.7 Resin-Coated Foil (RCF). Similar to the potential problems faced with photoimageable dielectrics, there is a divergence between the material characteristics required for hole filling and the characteristics that are desirable for an innerlayer dielectric-copper material. Nonetheless, it is likely that the RCF foil materials will prove to be acceptable for filling vias in the limited range of specific applications that exhibit a low-aspect ratio between hole diameter and core thickness.

Liquid dielectric resin is coated more or less the same way as in photovia. However, there is a fundamental difference between photovia and laser via dielectric. In laser via

processing, the resin is fully cured before laser drilling (microvia formation). This is a big advantage over photovia materials since the resin movement after hole formation is much more stable than in the case of photovia processing in which resin is fully cured after holes are formed. This resin (hole) movement makes pattern-imaging registration difficult for photovia processing.

25.6 HDI MANUFACTURING PROCESSES

This section discusses processes that employ non-drilling via-hole formation techniques. Through-via drilling is possible below 0.20 mm (0.008 in), but cost and practicality discourage this. Below 0.20 mm (0.008 in), laser and other via-formation processes are more cost-effective. Each of the five major via-hole formation processes used for printed circuits is discussed in the following sections.

- Photovia
- Plasma via
- Laser via
- Solid (paste) via
- Insulation displacement via

The manufacturing process for each microvia technology begins with a base core, which may be a simple double-sided board carrying power and ground planes or a multilayer board carrying some signal pattern in addition to power and ground planes. The core usually has plated through holes (PTHs). These PTHs become BVHs. Such a core is often called an *active core*.

25.6.1 Photovia Process

Prior to dielectric material coating by any of the methods described previously, the copper surface of the base core must be treated by an adhesion promotion process to ensure good adhesion of dielectric material to the copper surface. Today, very few manufacturers use oxide treatment for this purpose. The most popular adhesion promotion treatment is a special etching process offered by many suppliers of chemicals. This step is common to all microvia processes.

Dielectric resin is semicured after coating to eliminate tackiness, and then the hole pattern is exposed by photoexposure processing. The usual photodeveloping process creates microvia holes and the dielectric is fully cured, typically at 160°C for about 1 hour. Then, the panel goes through a permanganate etching process to remove any residual resin at the bottom of the hole and simultaneously create microporous surfaces that act as an anchor and ensure desirable peel strength after copper plating.

The level of peel strength is controversial. Minimum peel strength required for chip package substrates is about 600 g/cm^2, but motherboard users, particularly cell phone makers, demand a minimum of 1.0 kg/m^2 or more in order for cell phone handsets to withstand drop tests. Laser via materials usually yield stronger peel strength because of fillers that can be added to dielectric resin. When etched, these fillers generate a superior microporous surface structure needed for strong peel strength.

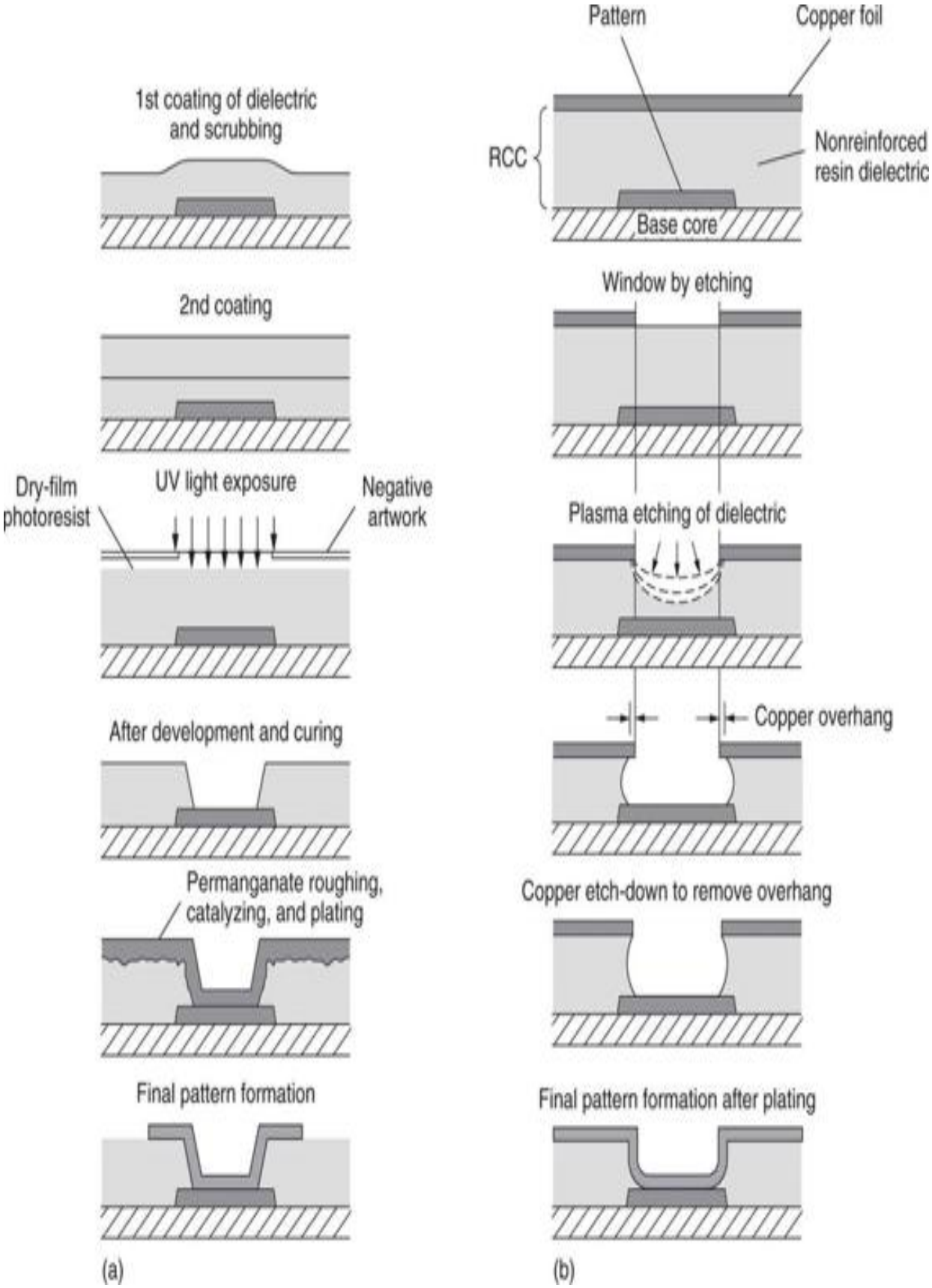
After permanganate etching, the panel is catalyzed and metallized in an electroless copper bath and panel-plated galvanically to desired thickness. Some photovia process practitioners roughen the resin surface mechanically by brushing or liquid horning prior to catalyzing. Then, the conductor pattern is formed by dry-film tenting and etching. Some manufacturers prefer to use the pattern-plating

method for this purpose. Very few microvia board manufacturers use direct metallization methods for metallizing holes prior to galvanic plating. Several Japanese manufacturers use electroless copper all the way to the desired thickness in panel plating and use a positive electrodeposited (ED) system to achieve fine lines and very small annular rings. One important step in microvia hole board fabrication when resin is the dielectric choice, whether the process is photovia or laser via, is the removal of residual catalysts (normally palladium) entrapped in a microporous surface that can cause migration. The process used in this step is normally a trade secret.

Photovia processing is now used primarily to fabricate semiconductor chip package sub- strates because a large number of holes can be formed in one photoexposure and development step. However, as mentioned previously, photovia processing suffers more from material shrinkage than laser via processing after full cure, and hole locations tend to move randomly, which makes subsequent registration for patterning difficult. Because of this problem, photovia users limit the size of the panel to be much smaller than the usual panel size prevalent in motherboard fabrication to about 400 × 400 mm. Small hole formation is also difficult with the photovia process. As a result, even makers of package substrates are now resorting more to laser via processes as the laser-drilling speed is being improved. Photovia process users engaged in mass production are found only in Japan today. All photodielectric processes have certain characteristics in general. Table 25.11 lists the typical processing factors. A standard photovia process sequence is described in Fig. 25.18*a*.

TABLE 25.11 Four Typical Photodielectrics (Three Epoxy and One Polyimide) and the Processing Parameters for Coating, Exposure, Developing, Desmears, and Metallization

	Product A	Product B	Product C	Product D
Product	L-PID, negative	L-PID, negative	L-PID, negative	DF-PID, negative
Material	Epoxy	Epoxy	Polyimide	Epoxy
Preclean	Chemical clean	Pumice jet	Br. oxide	Chemical clean
Apply PID	Curtain coat 150–400 cps	Curtain coat 200–600 cps	Extrusion coat 12,000–25,000 cps	Vac, lam. 60 s @ 65°C
Thickness	50 µm	50 µm	37 µm	63 µm
Drying	15 h @ 90°C	6 h @ 25/40°C 3 h @ 140°C	5 h @ 25°C 15 h @ 125°C	N/A
Exposure	800–1200 mJ/cm^2	800–1600 mJ/cm^2	2000–3000 mJ/cm^2	700–1200 mJ/cm^2
Heat bump	15 h @ 90°C	12 h @ 125°C	N.R.	20 h @ 85°C
Development	Aqueous proprietary 75 min @ 35°C	Organic GBL 60 min @ 30°C	Organic proprietary 150 min @ 30°C	Aqueous proprietary 60 min @ 35°C
Final cure	UV: 1.0 J/cm^2 + 60 h @ 145°C	60 h @ 150°C	120 h @ 175°C	UV: 2 J/cm^2 + 60 h @ 150°C
Roughen				
Swell	4 h @ 65°C	4 h @ 75°C	2 h @ 65°C	5 h @ 60°C
Etch	4 h @ 80°C	8 h @ 75°C	1 h @ 75°C	10 h @ 75°C
Neutralize	6 h @ 50°C	6 h @ 50°C	3 h @ 45°C	3 h @ 25°C
Metallize: electroless Cu	0.3–0.5 µm	0.7–1.0 µm	0.3–0.5 µm	0.4 µm
Bake	20 h @ 90°C	60 h @ 150°C	60 h @ 150°C	15 h @ 90°C
Electroplate				


1st coating of dielectric and scrubbing
2nd coating
Dry-film photoresist
UV light exposure
Negative artwork
After development and curing
Permanganate roughing, catalyzing, and plating
Final pattern formation
(a)
Pattern
Copper foil
RCC
Nonreinforced resin dielectric
Base core
Window by etching
Plasma etching of dielectric
Copper overhang
Copper etch-down to remove overhang
Final pattern formation after plating
(b)

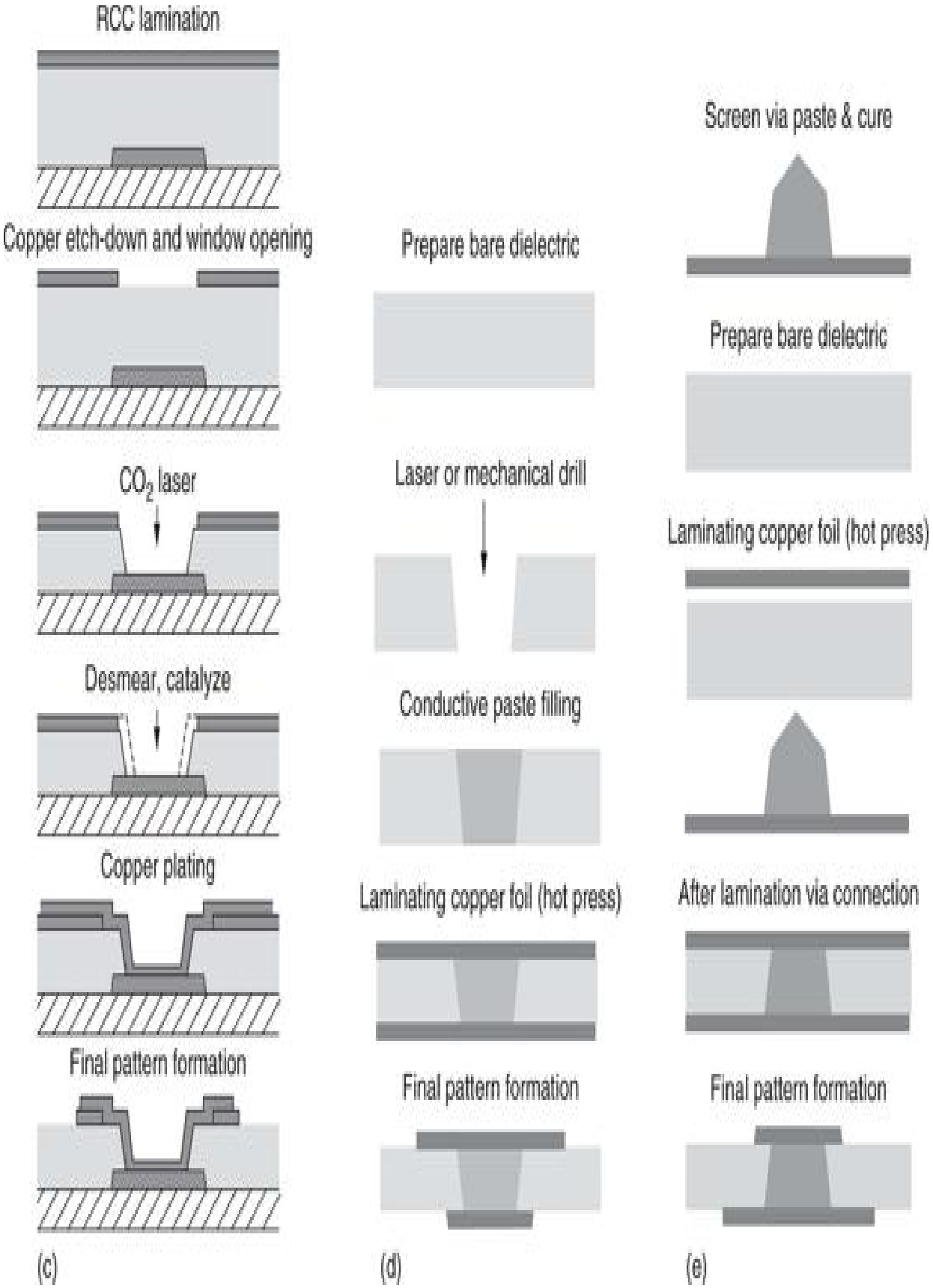

RCC lamination
Copper etch-down and window opening
CO_2 laser
Desmear, catalyze
Copper plating
Final pattern formation
(c)
Prepare bare dielectric
Laser or mechanical drill
Conductive paste filling
Laminating copper foil (hot press)
Final pattern formation
(d)
Screen via paste & cure
Prepare bare dielectric
Laminating copper foil (hot press)
After lamination via connection
Final pattern formation
(e)

FIGURE 25.18 Standard HDI manufacturing processes: (*a*) a typical photovia process with liquid resin dielectric; (*b*) the standard plasma via process with RCC; (*c*) the semiconformal laser via process; (*d*) the standard conductive (paste) solid via process; (*e*) the insulation displacement via formation process.

25.6.2 Plasma Via Process

Plasma via processing was developed by a Swiss PWB maker, Dyconex. Products made with the plasma via process are called DYCOstrate.

There are many variations to the plasma via process, one of which is illustrated in Fig. 25.18*b*. Today, it is mainly used to fabricate sophisticated flex and flex-rigid wiring boards in small quantities.

First, an opening or window is made through copper foil by a normal etching process. When plasma etching is applied through this window, the shape of holes tends to be like a bowl (as shown in Fig. 25.28*b*), which is not suitable for reliable plating (although new plasma- etching equipment claims to have solved this problem).[7,8] Another problem is related to how the microvia hole is formed. The copper edge of the window hangs out over the hole, which results in poor reliability after panel plating. Therefore, to ensure reliable plated holes, a secondary etching is necessary to remove this copper overhang. One good thing results from this secondary etching, however. Since surface copper is thinned, formation of finer conductors is made easier. Nevertheless, by the time the panel is ready for plating for subsequent conductor pattern formation, it takes several times longer than other processes in a mass-production environment.

Plasma via processing is effective for forming through holes on flexible materials since holes are formed by plasma etching from both sides of the film and the bowl effect is minimized.

Plasma via etching evolved from the traditional process of plasma desmearing of through holes. Different gas,

magnetrons, and equipment fixturing are employed by current plasma via-etching equipment. The plasma is generated in a partial vacuum filled with a mixture of oxygen, nitrogen, and chlorofluoro (CF4) gasses. Microwave magnetrons create the plasma field and special low-frequency kilowave units help provide rapid etching of organics.

25.6.3 Laser Via Process

Laser via processing is by far the most popular microvia hole formation process. But it is not the fastest via formation process. In Fig. 25.19, the chemical etching of small vias is the fastest, with an estimated rate of 40,000 to 50,000 vias per second. This is also true of plasma via formation and photovia formation. These are all *mass-via-formation* processes. Laser drilling is one of the oldest microvia generation techniques.[9] The wavelengths for laser energy are in the infrared and ultraviolet region. Figure 25.20 shows the five major wavelengths used in current laser drills. The absorption curves of many organic dielectrics epoxy, polyimide, matte copper, and glass fibers are shown in Fig. 25.21. Laser drilling requires programming the beam fluence size and energy. High-fluence beams can cut metal and glass, whereas low-fluence beams cleanly remove organics but leave metals undamaged. A beam spot size as small as approximately 20 microns (<1 mil) is used for high-fluence beams and about 100 microns (4 mil) to 350 microns (14 mil) for low-fluence beams.[10,11]

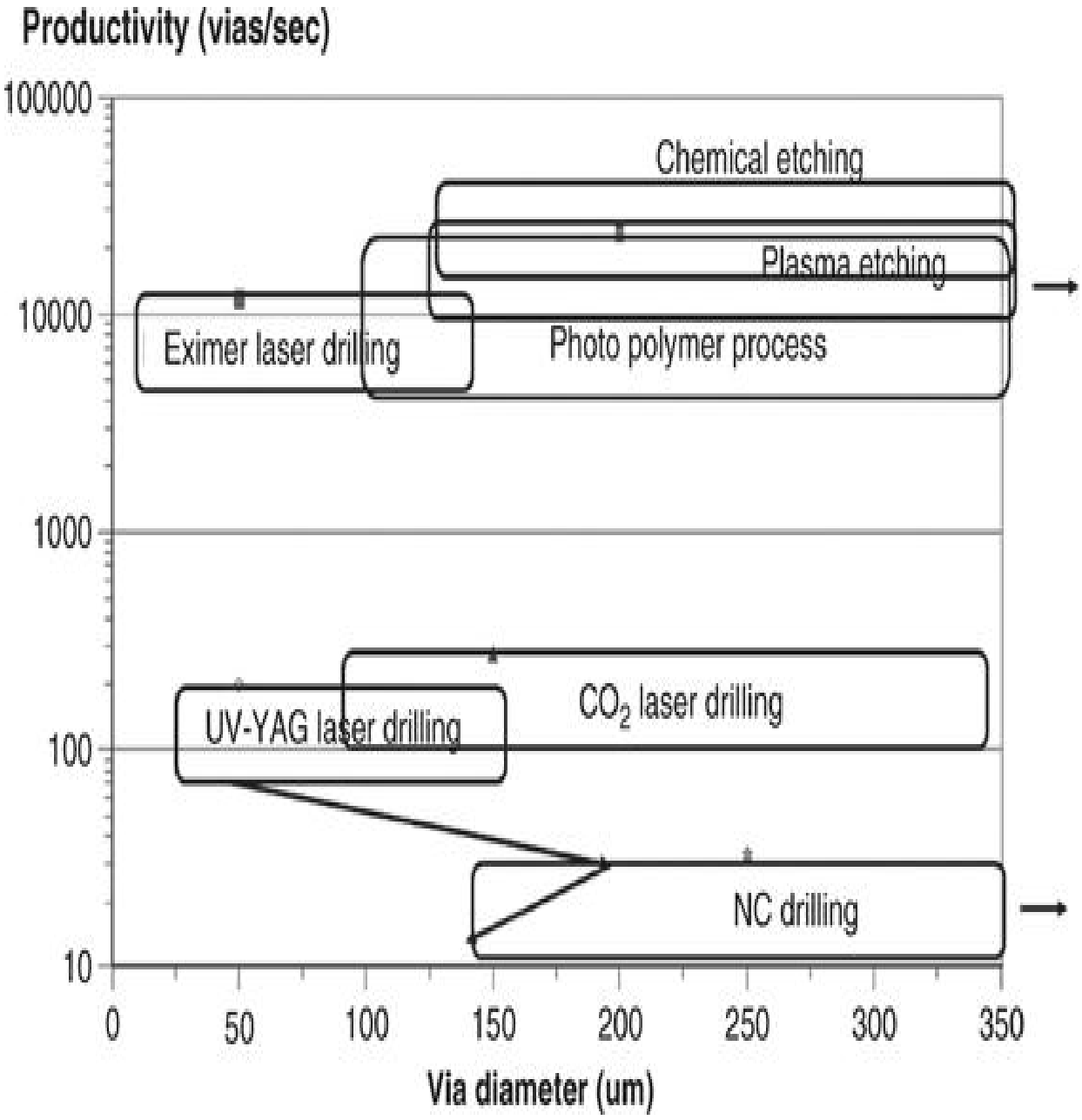


FIGURE 25.19 The various rates of via formation based on diameter and method of via ablation, from chemical, plasma, photo and laser techniques.

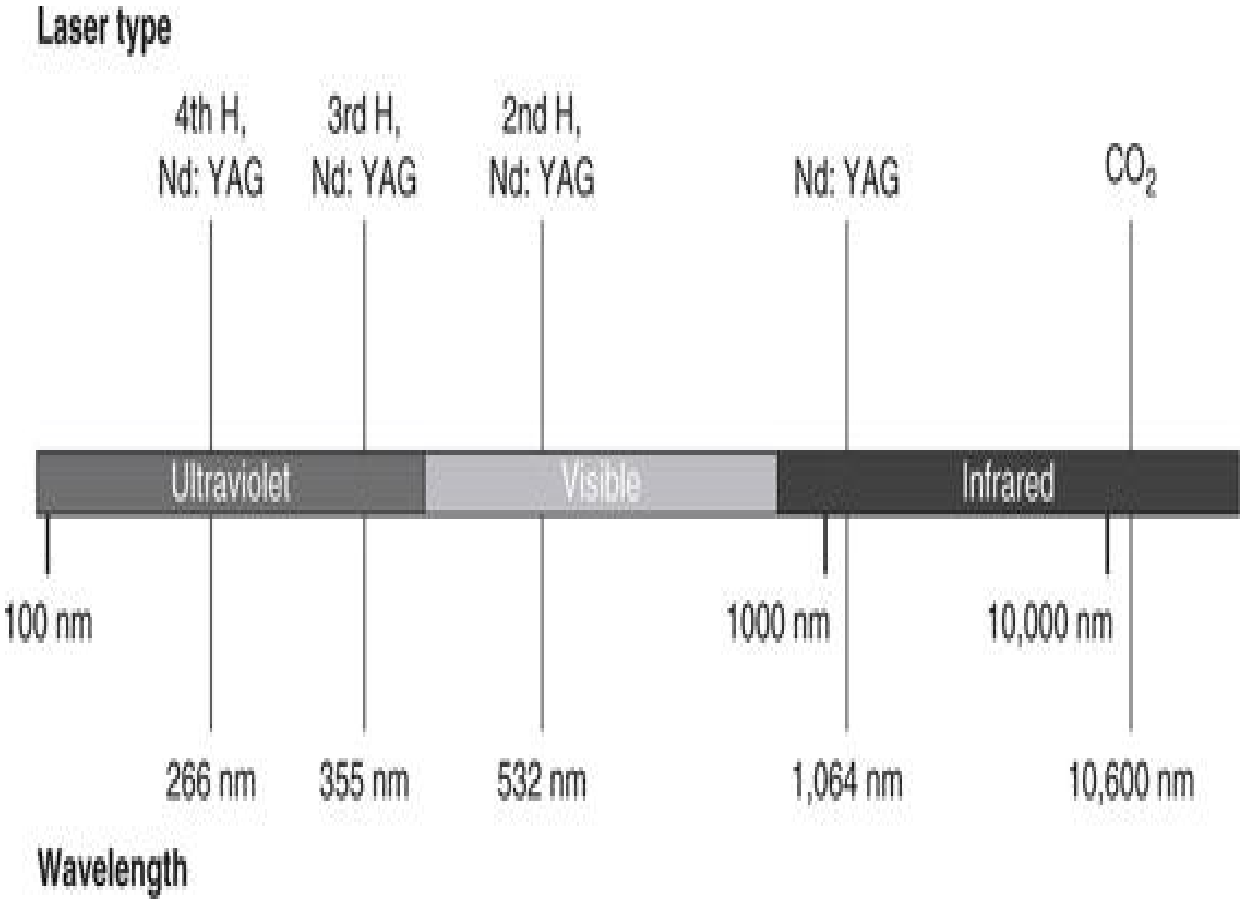


FIGURE 25.20 The wavelengths used by laser via drilling from infrared to ultraviolet region, including the harmonics of Nd:YAG lasers.

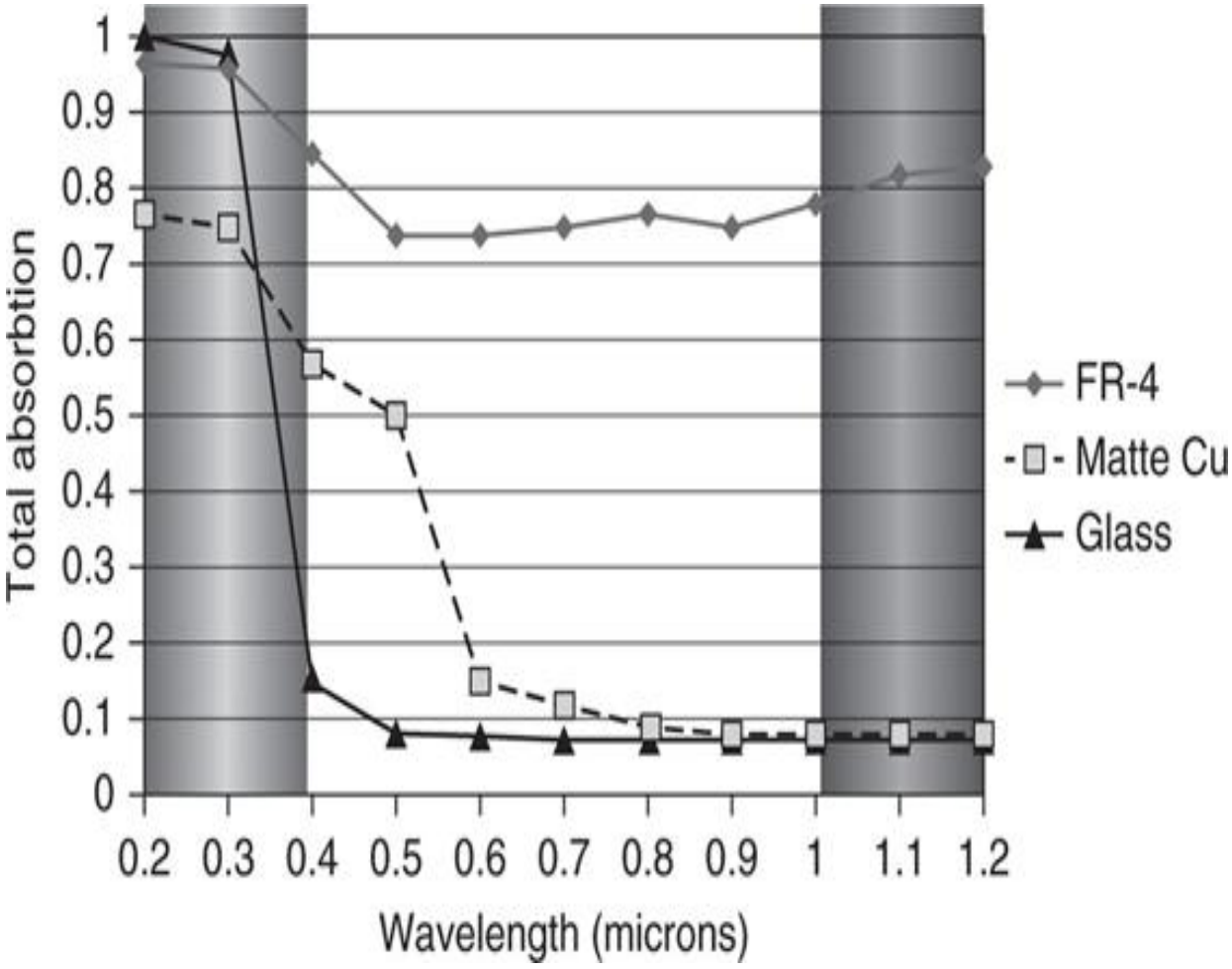


FIGURE 25.21 The absorption wavelength of different materials respond to different wavelength of laser energy. Epoxy, copper and glass of laminate are ablated by the UV wavelength but only the resin is ablated by the CO_2 wavelengths.

However, there are many variations. For the purpose of drilling microvia holes, there are four laser systems: UV/Yag laser, CO_2 laser, Yag/CO_2, and CO_2/CO_2 combinations. Then there are three dielectric materials: RCC, resin only (dry-film or liquid resin), and reinforced prepreg. Therefore, the number of ways to make microvia holes by laser systems is driven by the permutation of four laser systems and these three dielectric materials.

There are several factors to observe in laser via processing: position accuracy of lased holes (microvia holes), uneven diameters of holes, dimensional change of the panel

after curing dielectric, dimensional change of the panel due to temperature and humidity variations, alignment accuracy of the photoexposure machine, unstable nature of negative artwork, and so on. These should be carefully monitored and are important for all microvia hole processes.

25.6.3.1 UV/Yag Laser. A Yag laser can penetrate copper; therefore, it is not necessary to pre-etch the window when the choice of dielectric is RCC or a copper-foil/prepreg combination. Positioning accuracy in relation to the capture pad is good, but there are weaknesses associated with the Yag laser. The speed of drilling (ablation) is slower than the CO_2 laser, particularly when a hole diameter is equal to or larger than 125 µm, because the laser beam is very small. Therefore, it is necessary to do trepanning (spiral drilling pattern), which results in longer drilling time. Another weakness is the Yag laser's sensitivity to the thickness of dielectric material. If the thickness of the RCC's resin is not even, the Yag laser beam, the power of which is adjusted to remove the thicker part of the resin, may damage the capture pad. If adjusted to the thinner part, it may not reach the capture pad.

Although the Yag laser can penetrate copper and glass-reinforced prepreg, the situation is worse in this material than with RCC. The laser power must be adjusted to penetrate through the crossover part of woven glass. Then, when the laser beam hits the part of prepreg where there is now a glass bundle (opening), the beam can really damage the capture pad. To avoid this problem, the operator must reduce the laser power and apply laser ablation for a longer duration, which increases drilling time considerably. Depending on the construction of the dielectric layer through which the Yag laser beam must penetrate, the drilling speed must be adjusted to about 3 to 50 holes per second when glass-reinforced dielectric is used.

When the dielectric is RCC, the speed of the currently available UV/Yag laser is somewhere around 100 to 300 holes per second.

When the dielectric is resin without copper foil, a CO_2 laser is the best since a CO_2 laser can offer much faster drilling speed (a single-head CO_2 laser can drill as many as 25,000 holes per minute, including overhead such as loading a panel onto the drilling table and registering the panel).

The best feature of the UV/Yag laser drilling machine is its ability to drill a very small hole (down to 20 to 30 μm, whereas the smallest hole a CO_2 laser can drill is 50 μm in a mass-production environment) and its superior position accuracy through RCC.

For higher-speed drilling, even Yag laser users are now etching copper foil down to 6 to 9 μm, the process more frequently seen in CO_2 drilling.

25.6.3.2 CO_2 and Twin CO_2. A CO_2 laser beam cannot penetrate copper foil unless the foil is very thin, less than 5 μm, and the surface is treated to be dark to absorb the CO_2 laser beam (this process is called CO_2 laser direct drilling and will be treated later).

When the surface is resin only, a single-headed CO_2 laser machine can drill holes at the rate of 20,000 to 25,000 per minute depending on hole density and distribution. The drilling speed continues to increase. The denser the hole, the faster the drilling speed because time lost by table motion is minimized. A dual-head CO_2 machine can boost drilling productivity by about 70 percent compared to a single-head machine.

Manufacturers of dielectric resins mix fillers in the resins to enhance peel strength. Some fillers can slow down the drilling speed of a CO_2 laser beam (beam absorption is weaker in this case). For example, when the required

dielectric thickness is 60 µm, resin is coated twice, which is a frequent practice to produce a thick coating. The first coating is made with resin without filler (40 µm), and the second coating (20 µm) is resin with filler. Since the laser beam goes through a thin layer of filled resin, the speed degradation is minimized.

The most desirable shape of drilled microvia holes is tapered, which is accomplished by pulse drilling. Normally, two to three pulses are used. When three pulses are applied on the same spot continuously, the capture pad may be overheated and excessive epoxy smear may result. Therefore, when three pulses are to be applied, the entire panel is drilled first by two pulses and then the third pulse is once again applied to all holes. This way, the quality of the holes is ensured, although it takes longer to drill.

When the choice of dielectric is RCC, the opening or window must be formed first on copper foil, as in the case of plasma via. Prior to window formation, an etching process thins the surface copper, usually down to 6 to 7. This process is sometimes called *half-etching*.

Half-etching yields a few benefits. Window formation is made easier, and formation of fine-line conductors is also made easier. H_2O_2/H_2SO_4 etchant is often used for this purpose for even thickness. As mentioned previously, this half-etching procedure is also becoming common for Yag laser users.

There are two variations to CO_2 laser drilling through a window opening. One is called *conformal* and the other *semiconformal* (see Fig. 25.18*c*).

In the conformal method, a laser beam with a diameter larger than the window opening is used. Straight ablation of dielectric results in a bowl-shaped hole, as in the case of plasma via. Therefore, improved systems use laser beam diameters slightly larger than the window opening, and beams are pulsed to minimize the bowl effect.

In the semiconformal method, a laser beam with a diameter slightly smaller than the window opening is used. This results in a slight step when plated afterward, as shown in Fig. 25.18*c*. To minimize this step, half-etching is important in semiconformal drilling.

Some manufacturers using CO_2 drilling etch down copper completely after RCC lamination. The dielectric surface below copper is already microporous, which generates good adhesion except prior to the RCC stage. Therefore, some special treatment is applied to the resin surface, such as electrolessly plated nickel layer, prior to copper plating, but such treatment is kept secret. The RCC approach suffers from misregistration of window opening to capture pad when the surface and capture pad diameter becomes less than 250 μm, which causes serious defects (see Fig. 25.22). Laser via process practitioners have several solutions to this problem. They can use liquid resin or resort to a Yag or Yag/CO_2 laser. Since a Yag laser can break through copper foil, the beam can be directed to the capture pad position accurately. Another choice is to use laser direct imaging (LDI) for window etching in order to benefit from the speed of the CO_2 laser.

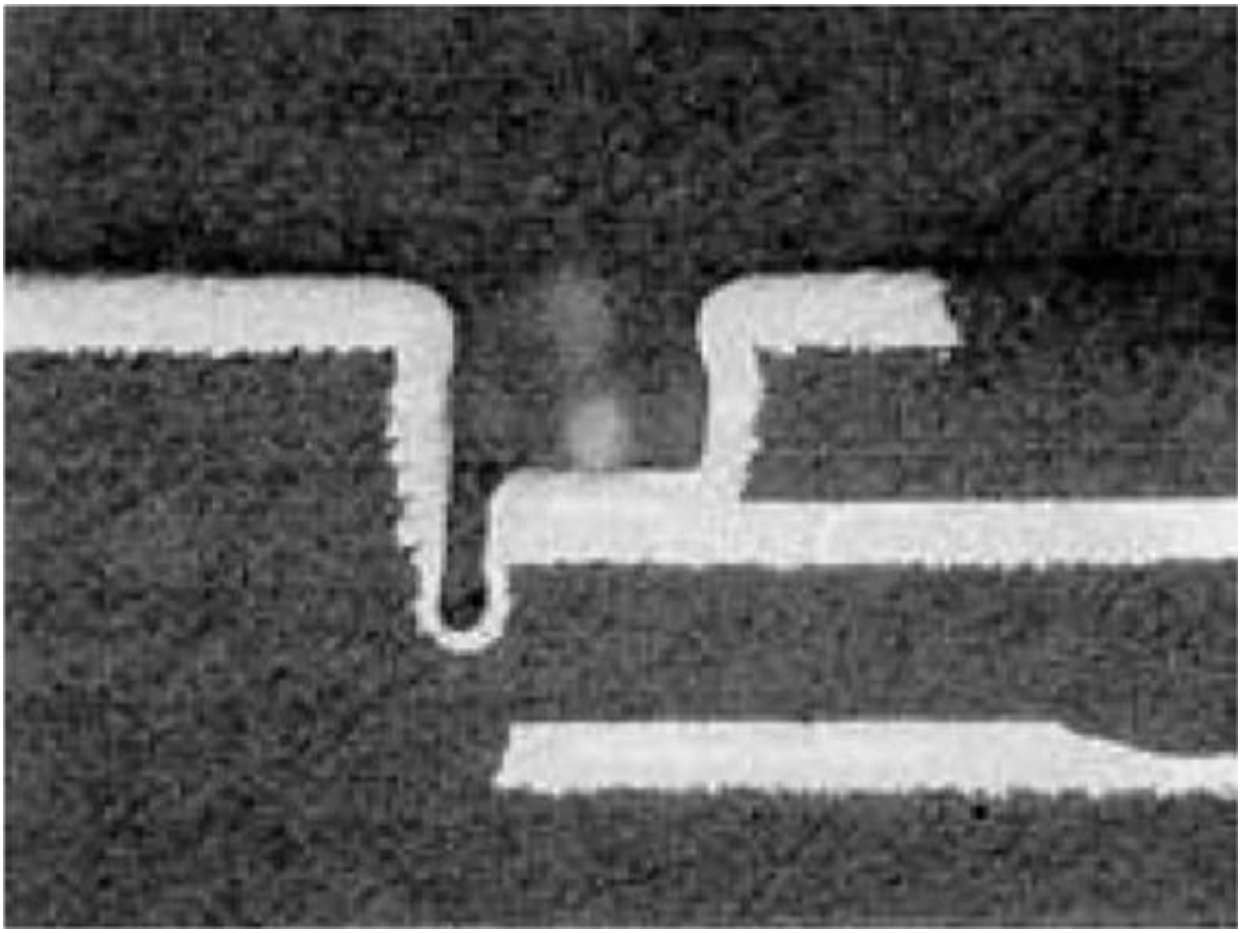


FIGURE 25.22 Misregistration of laser hole to capture pad. (*Courtesy of Ibiden*.)

Another solution is to use CO_2 laser direct drilling. The advantage of using RCC is the pre-established peel strength. Manufacturers go through delicate steps to establish the appropriate peel strength when using liquid resin. The degree of resin cure, permanganate etching, control, and regeneration of the permanganate solution affects the resultant peel strength as well as cost.

In this laser direct drilling method, copper foil is etched down to about 5 μm and its surface goes through oxide treatments such as black oxide or other methods, typically as alternatives to oxide treatment, which is normally an etching process. The copper thickness is further reduced by 1 μm, and the surface color becomes dark, allowing the CO_2 beam to penetrate.

Alternatively, ultrathin copper RCC may be used. Carrier foil, usually copper foil of 70 µm thickness (2 oz), is coated with a very thin layer (10 to 20 µm) of current conductive release film, and a thin foil of 3 to 5 µm is plated. After such RCC is laminated to the core, the carrier film is peeled off and the surface condition is the same as etched-down copper. Drilling speed in this direct CO_2 laser drilling method is degraded by 30 to 40 percent compared to that of straight resin drilling, but the registration to the capture pad is ensured.

25.6.3.3 Yag/CO_2. This combination is particularly useful for a copper/prepreg structure. The Yag laser offers good position accuracy and cuts through copper, but it tends to leave glass fibers sticking out in the hole after prepreg drilling. And as mentioned before, it is sensitive to dielectric thickness variation. The CO_2 laser beam cuts through glass fiber more cleanly than the Yag. In this combination laser drilling, the power of the Yag laser beam is adjusted to cut through copper and remove a portion of glass fiber and leaves the finishing to the CO_2 laser. The speed of drilling is governed by the speed of the Yag laser and is therefore slower than a pure CO_2 laser. However, this is the preferred laser-drilling machine for fabricating infrastructure types of PWBs, such as ones used for servers, network routers, and base stations that typically have copper/prepreg surface structures. The size of the panels used to fabricate such boards is usually large; therefore, the positioning accuracy of the Yag laser is preferred. Microvia hole boards used by the automotive industry also have this copper/prepreg structure.

The speed of drilling by a Yag/CO_2 machine is much slower than that of a CO_2 laser. However, the number of microvia holes to be drilled for infrastructure boards is normally one magnitude less than that seen in cell phone applications, in which the number of microvia holes can reach as many as

650,000 to 700,000 per m^2 Furthermore, the price of infrastructure boards is much more than that of mass-produced cellular phone motherboards. Therefore, slower speed of drilling, which means higher drilling cost, does not affect the total cost of manufacturing.

Residual glass fibers in the hole that can affect reliability may be removed chemically or mechanically. Mechanical removal is preferred. Blasting with aluminum oxide (about 20 µm diameter particles) is commonly used to remove glass fibers and smears as well. An excimer laser is also used to remove smears in the hole by a sweeping motion through the copper opening. In both cases, it takes about 30 seconds to desmear one side of the panel.

25.6.4 Dry Metallization (Conductive Inks, Conductive Paste, and Insulation Displacement)

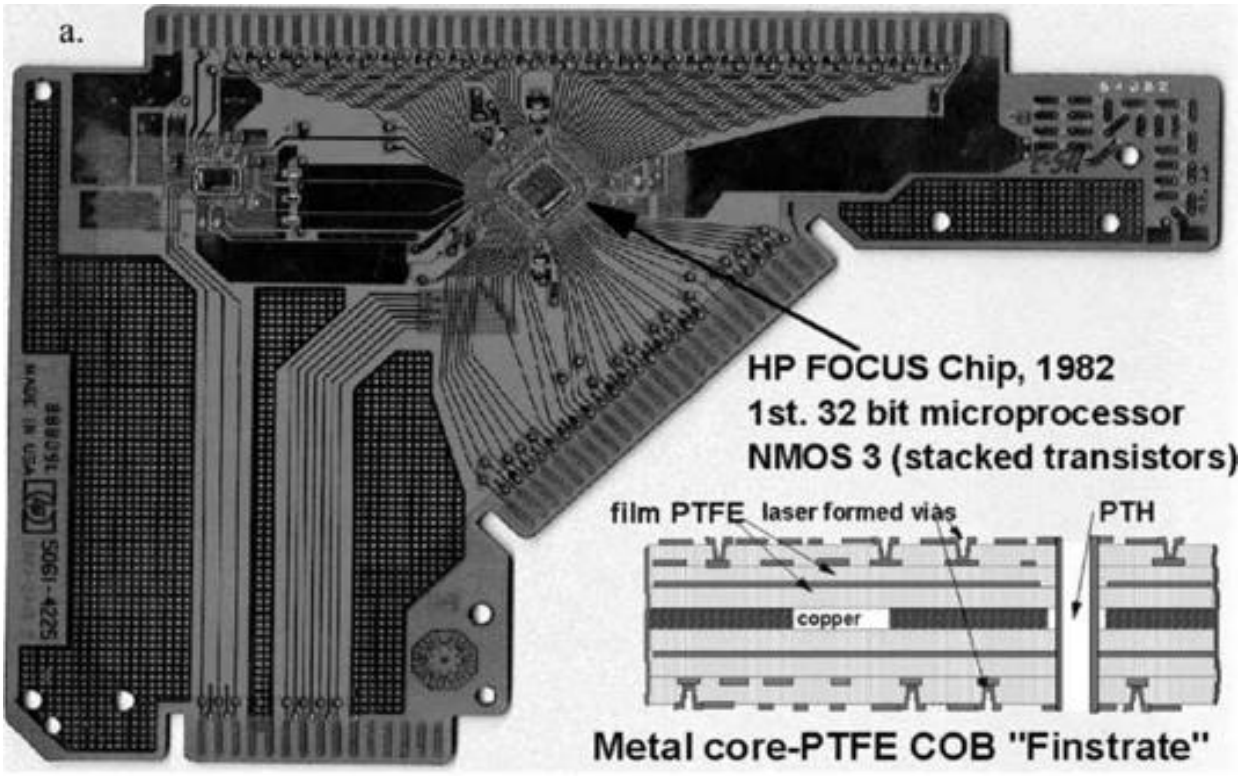
Three types of dry metallization are covered: conductive ink, conductive paste, and insulation displacement. Conductive ink describes a single-layer dielectric with microvias formed by photoimaging, laser, or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished either by laminating copper foil onto the dielectric surface or by chemical deposition. This process is shown in Fig. 25.18*d*.

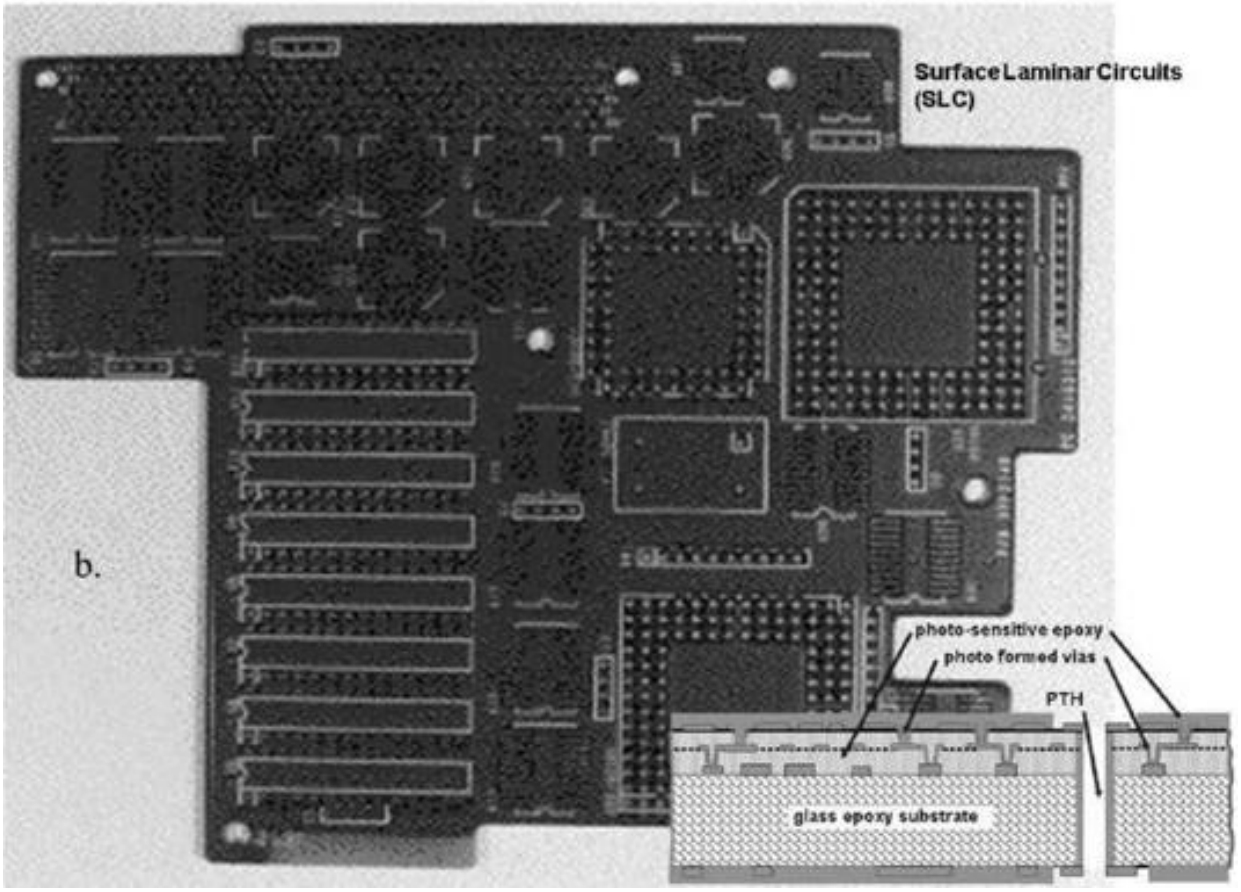
Insulation displacement is a unique process in that the silver conductive paste is screened on copper foil and cured. The conductive paste forms a “pointed” via that penetrates conventional prepregs during lamination and adheres to the copper foil on the reverse side, forming a via. Figure 25.18*e* shows this via formation process.

Standard activities concentrate on the use of photoimaging and screen printing while overcoming the limitations and expense associated with processes such as plating and etching. The concept is built on the use of a photoimageable dielectric to produce both vias and circuit channels that are then filled with a conductive ink. These approaches eliminate the need for a separate dielectric and clad-metal layer that requires either etching or a combination of plating and etching to produce a circuit. They also eliminate the resist deposition and stripping previously required to define that circuit. The conductive ink technique of metallization virtually eliminates the generation of metal waste streams.

Conventional multilayer printed wiring boards must be subjected to drilling and through- hole plating to create interconnections. These holes represent inefficient use of PWB area. In addition, to connect the printed wiring with part connection lands, some through holes must be provided in areas other than where the lands are located.

25.7 APPENDIX


a.
HP FOCUS Chip, 1982
1st. 32 bit microprocessor
NMOS 3 (stacked transistors)
film PTFE
laser formed vias
PTH
copper
Metal core-PTFE COB "Finstrate"


Surface Laminar Circuits
(SLC)
b.
photo-sensitive epoxy
photo formed vias
PTH
glass epoxy substrate

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Sutherland, I.E., and Oestreicher, D., “How Big Should a Printed-Circuit Board Be?” *IEEE Transactions on Computers*, Vol. C-22, No. 5, May 1973, pp. 5323–5542.

CHAPTER 26

ADVANCED HIGH-DENSITY INTERCONNECTION TECHNOLOGIES

Happy T. Holden

Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

26.1 INTRODUCTION

Since the introduction of HDI in the mid-1980s [HP-Finstrate, Siemens's MicroWiring, and IBM's Surface Laminar Circuit (SLC) technology; see Figs. 22.1, 22.2, and 22.3 in the 6th edition of this book], many variations of making high-density interconnect (HDI) wiring boards have been developed and implemented for mass production. However, if one technology is to be judged in terms of volume produced and picked as a winner, laser-drilling technology is the one. Other methods are still used by a number of printed wiring board (PWB) manufacturers, but on a much smaller scale.

The purpose of this chapter is to examine a variety of HDI fabrication processes as seen in Fig. 26.1. However, a

greater emphasis will be placed on the laser-drilling process (hereinafter *laservia*) since it is the most popular process today and it seems its popularity will grow in the future. It must be understood that interconnect via hole (IVH) formation is just one element of fabricating HDI wiring boards. The other two important factors are the various dielectric materials and the methods of metallization. Fabrication of HDI wiring boards with microvia holes involves many new processes not common to conventional board fabrication. Therefore, additional emphasis will be placed upon these new fabrication processes that are common to other microvia technologies.

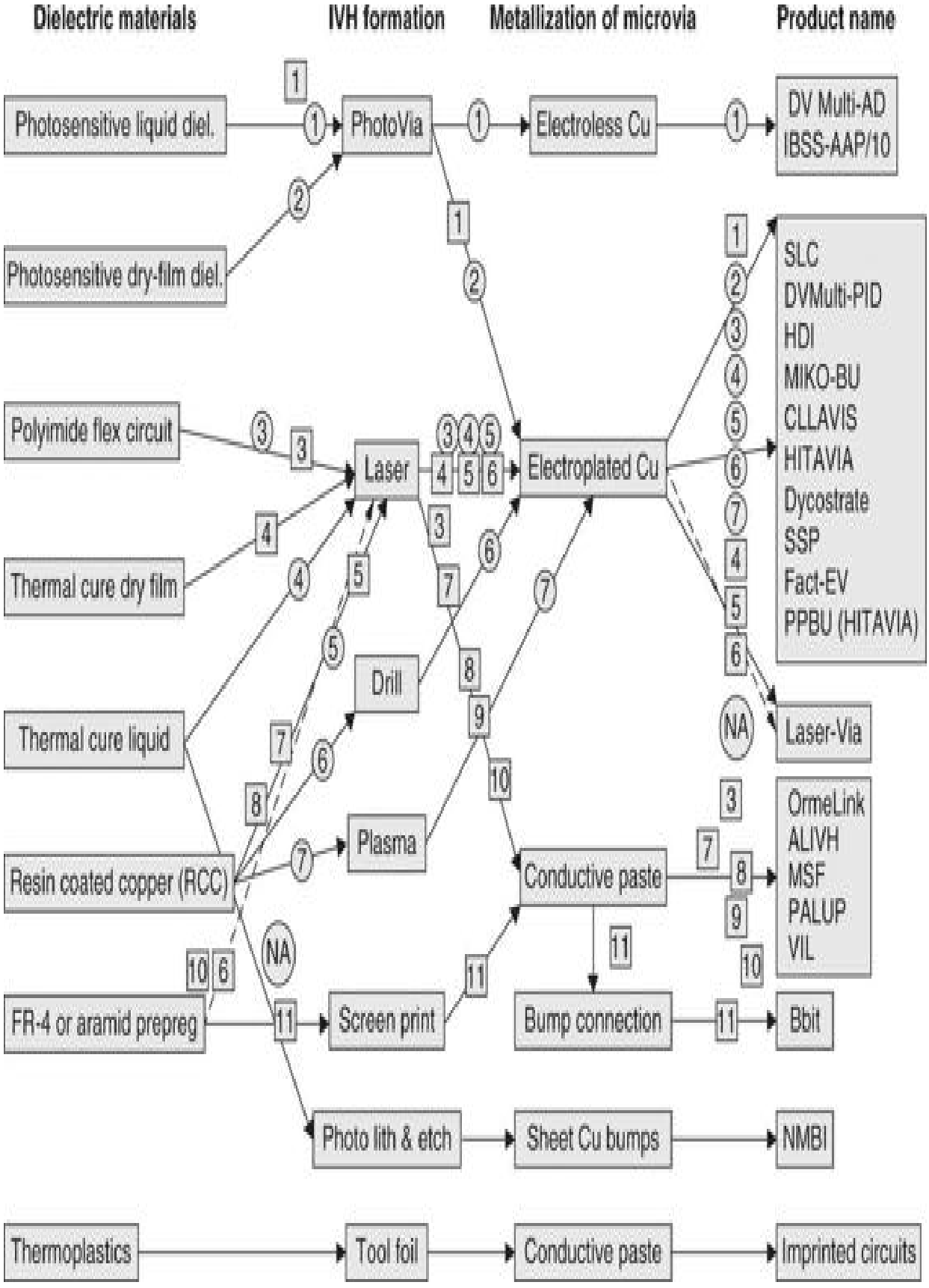

Dielectric materials
IVH formation
Metallization of microvia
Product name
Photosensitive liquid diel.
Photosensitive dry-film diel.
Polyimide flex circuit
Thermal cure dry film
Thermal cure liquid
Resin coated copper (RCC)
FR-4 or aramid prepreg
Thermoplastics
PhotoVia
Laser
Drill
Plasma
Screen print
Photo lith & etch
Tool foil
Electroless Cu
Electroplated Cu
Conductive paste
Bump connection
Sheet Cu bumps
Conductive paste
DV Multi-AD
IBSS-AAP/10
SLC
DVMulti-PID
HDI
MIKO-BU
CLLAVIS
HITAVIA
Dycostrate
SSP
Fact-EV
PPBU (HITAVIA)
Laser-Via
OrmeLink
ALIVH
MSF
PALUP
VIL
Bbit
NMBI
Imprinted circuits
NA

FIGURE 26.1 The HDI technologies in use today are made up of three factors: the dielectric materials, the methods of IVH formation, and the method of metallization of those z axis via connections. In recent years up until now, 21 different HDI processes have been used.

Additional advanced HDI applications will be introduced in the form of *embedded optical waveguides*, a next generation use of printed circuits.

26.2 DEFINITIONS OF HDI PROCESS FACTORS

The 21 different HDI processes shown in Fig. 26.1 have three basic fabrication factors in their process makeup:

1. Dielectric materials
2. IVH formation
3. Methods of metallization

26.2.1 Dielectric Materials

Eight different general dielectric materials have been used in the current or past HDI processes. IPC slash sheets such as IPC-4101B and IPC-4104 cover many of these, but many are not yet specified by IPC standards. The materials are

1. Photosensitive liquid dielectrics
2. Photosensitive dry-film dielectrics
3. Polyimide flexible film
4. Thermally cured dry films
5. Thermally cured liquid dielectrics
6. Resin-coated copper (RCC) foil
7. Conventional FR-4 cores and prepregs
8. Thermoplastics

26.2.2 Interconnect via Hole Formation

Seven different methods of forming the IVHs have been used in current or past HDI processes. Laser drilling is the most prominent, but the other six come into use also. The methods are as follows:

1. Photo processes to define vias in photodielectrics
2. Various laser-drilling methods, including UV-Yag, UV-Eximer, and CO_2
3. Mechanical drilling
4. Plasma drilling
5. Screen printing of via pastes
6. Photo and etch of solid vias
7. Toolfoil

26.2.3 Method of Metallization

Four different methods of metallizing the IVHs have been used in the current or past HDI processes. The methods are as follows:

1. Fully additive electroless copper
2. Conventional electroless and electroplating copper
3. Conductive pastes
4. Fabricating solid metal vias

26.3 HDI FABRICATION PROCESSES

The three basic and original HDI processes are laser drilling laminate (Finstrate) and flexible materials (microwiring), photo dielectrics with SLC and plasma-etching polyimide

(Dycostrate). These and the other 18 HDI processes have been integrated into standard printed circuit manufacturing flows. There is no standard way to organize these processes, but the method of IVH formulation is the most unique characteristic of each process and will be used for this purpose.

26.3.1 Photo-Via Technologies[1,2]

26.3.1.1 IBSS-AAP10 System. The Interpenetrating Polymer Network Build-Up Structure System (IBSS) is a new photodielectric. This photoimageable dielectric (PID) is a proprietary photodielectric developed by Ibiden of Japan. It complements Ibiden's older epoxy type of photo-redistribution layer technology, IP-10.

26.3.1.1.1 Structure. IBSS is specifically formulated for integrated circuit and flip-chip packages and has a high T_g and flexibility. The bismalene-triazine (BT) core also provides high-temperature resistance.

26.3.1.1.2 Manufacturing Process. IBSS is a liquid system applied by roller coater to a rigid core, typically BT. The coating is cured and photodeveloping creates the vias. The IBSS requires an aggressive swell-and-etch because of the higher-temperature nature of the photodielectric (PD). The metallization is fully additive copper, also proprietary to Ibiden.

The imaging for additive metalization uses a permanent dry-film photoresist. For additional layers of dielectric, an adhesion promoter is applied to the surface copper.

26.3.1.2 Surface Laminar Circuits. SLC technology was the first of the PID microvia, build-up technologies to reach the interconnect market in high volume. Development of SLC technology began during the late 1980s at IBM (Yasu,

Japan), and the first product was introduced in 1990.[1] The first flip-chip, direct-chip-attach (FC/DCA) product employing SLC technology was shipped from Yasu in 1992, and in 1995 IBM Endicott, New York, shipped its first printed wiring boards that utilized SLC technology.[2] Used by many original equipment manufacturers (OEMs) in Japan, the SLC process provided the high-density interconnect technology for Sony's first digital Camcorder, the DCR-PC7, seen in Fig. 26.2. This eight-layer build-up structure had two SLC layers on each side of a four-layer core. The assembly density of this was over 612 pins per sq. in due to the wall-to-wall 0.5 mm pitch chip scale package (CSP) used.[3]

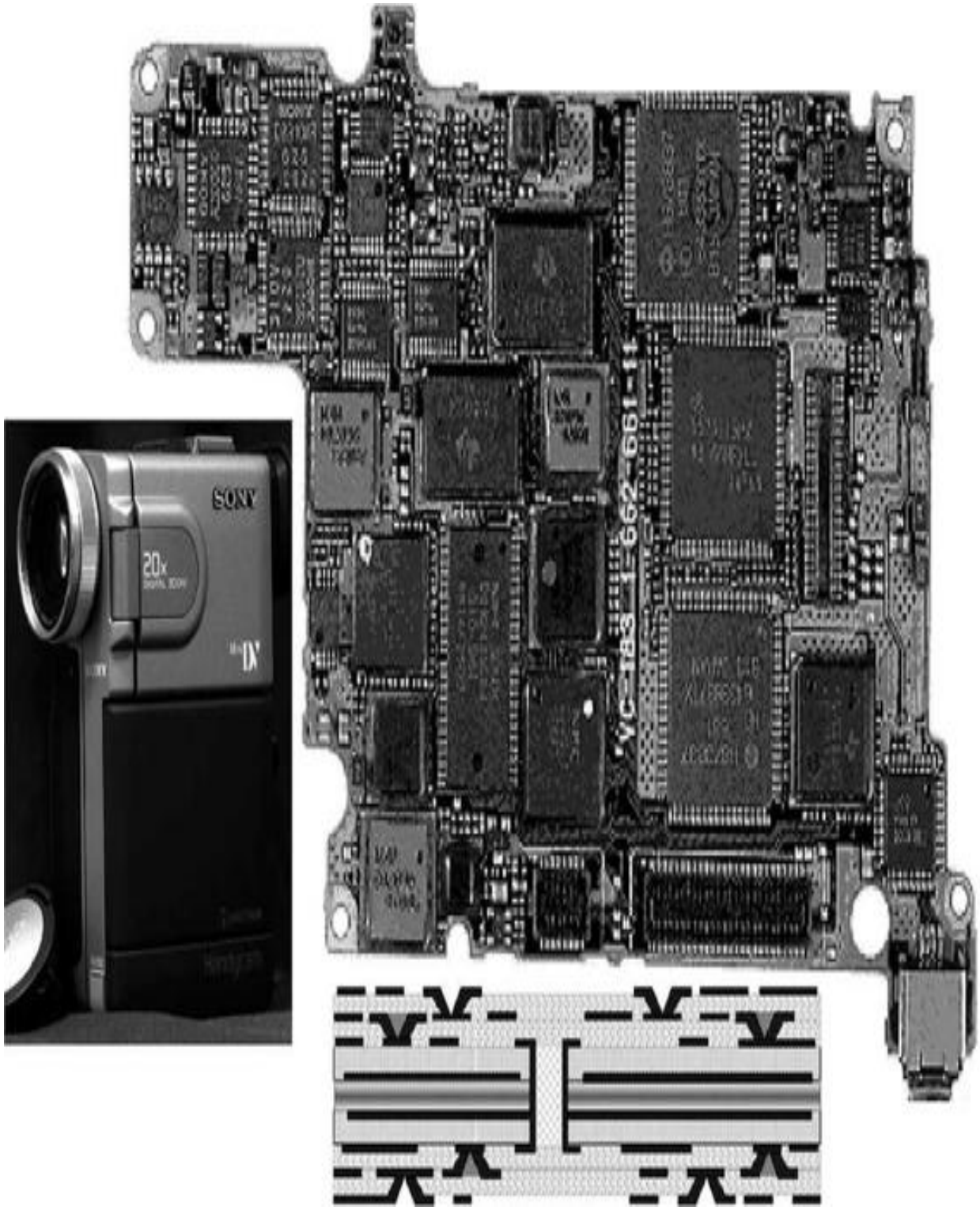


FIGURE 26.2 The Sony DCR-PC7 digital camcorder utilized the SLC process for the 2+4+2 build-up structure and 0.5 mm CSPs to achieve over 600 connections (pins) per sq. in.

The most suitable photosensitive dielectric was the photoimageable solder masks, due to their proven compatibility with printed circuit assembly processes, ability to withstand exposure to service environments, and possession of the necessary via-imaging characteristics. SLC technology was originally developed and implemented with a liquid PID solder mask applied by curtain coating. In 1995, it was also qualified with a dry-film PID with virtually identical electrical properties. The dry-film version did not require the extensive surface grinding processes that the liquid PID process required.

PID technology is based on photoimageable polymeric systems to form blind microvias in dielectric material between layers of circuitry. The use of PIDs allows all microvias on a panel to be formed simultaneously, with no incremental-per-via cost. Its use is particularly advantageous on applications with high densities of vias (e.g., more than 50,000 on an 18 × 24 in panel).

26.3.1.2.1 Liquid versus Dry PID. A typical flowchart of the PID technology fabrication process, including options for multiple build-up layers and a multilayer core, is shown in Fig. 26.5. At this level in the process, PID technology is the same whether a liquid or dry-film PID is used.

Liquid and dry-film PIDs do provide slightly different via wall profiles. The liquid PID has tapered via walls, whereas the dry-film PID has essentially vertical via walls. The tapered via walls provide good plating coverage on the via walls and base. Vertical walls allow for a smaller via top opening, and correspondingly smaller capture land for a given via bottom diameter.[4,5]

26.3.1.2.2 Tools. The use of a liquid PID requires two unique pieces of equipment: a coater of some variety, either curtain, slot, roller coater or screen printer (with associated drying ovens), and a leveling tool (surface sander). A leveling tool is required to planarize the surface of the cured liquid

PID to accommodate fine-line photolithography on the surface. Liquid PID provides a conformal coating over underlying circuit features, producing nonuniform planarity. The leveling operation also removes a lip of exposed PID that overhangs the via openings in these processes. Many liquid PIDs have a self-leveling characteristic and do not require any other leveling.

The use of a dry-film PID requires only one unique piece of equipment: a vacuum laminator. Vacuum laminators are common at printed circuit fabrication shops; in addition, the capital to obtain one is significantly less than for a curtain or slot coater. The dry-film PID has excellent planarization and does not require a leveling process due to the film's low solvent content, low shrinkage, and vacuum lamination process.[6,7]

PID technologies were originally conceived as an alternative to multilayer lamination as a way to make multilayer PWBs. PID technology builds up each surface signal layer on top of the previous layers in a sequential fashion. The base under all of the outer build-up layers is a conventional double-sided or multilayer circuit board containing voltage, ground planes, and even signal layers. Mechanically drilled and plated holes are used only in the core layers, to make connections to the backside of the laminate base and accommodate mounting pinned components. There is greater wiring density to use plated through holes (PTHs), which extend only through the base printed circuit structure and not through the build-up layers, especially when two or more build-up layers are used. Figure 26.3 provides additional details of the SLC manufacturing process of multilayer printed circuit boards.[8,9]

Circuitize Inner Layer Cores
Laminate Sub-Composite
Coat & Dry Liquid PID (1st side)
Expose & Develop PID (1st side)
Partial Cure PID (1st side)
Coat & Dry Liquid PID (2nd side)
Expose & Develop PID (2nd side)
Full Cure PID (both sides)
Level PID Surfaces
Inspect & Repair (optional) PID
Liquid PID
Vacuum Laminate PID (2 sides)
Pre-Bake PID
Expose PID (2 sides)
Post Expose Bake PID
Develop PID
UV Flood and Cure PID
Inspect & Repair (optional) PID
Dry Film PID

FIGURE 26.3 The manufacturing flows for the two major SLC manufacturing processes.

26.3.1.3 DV Mult-PID. DV Mult-PID is from NEC. This structure uses a PID primarily as an integrated circuit (IC) substrate and for high-density electronic products. It is capable of three build-up layers per side. The use of a dry-film PID requires only one unique piece of equipment: a vacuum laminator. Vacuum laminators are common at printed circuit fabrication shops; in addition, they cost much less than a curtain or slot coater. The dry-film PID has excellent planarization, does not require a leveling process due to the film's low solvent content, low shrinkage, and vacuum lamination. The modified structure of DV Multi-AD uses laminates and RCC for the build-up layers and fully additive electroless plating.

26.3.2 Laser Via Technologies[3–5,3–6,7–10]

Circled processes 3, 4, and 5, as well as squared 3 through 10 in Fig. 26.1, utilize a laser drill via generation technique. This process was first used in the late 1970s to drill small holes in G-10 laminate for buried vias in mainframe computer boards by IBM for its 3081 system and by Burroughs. (Attempts to find pictures of these products proved unfruitful.) The Hewlett Packard laser-drilled Finstrate family of boards, first produced in 1983, is shown in Chap. 22 of the previous edition. Siemens' laser-drilled microwiring was produced since 1987.

26.3.2.1 High-Density Interconnect (HDI). The HDI process developed by General Electric and now owned by Lockheed Martin is the one most similar to IC processes. This process is what is called a "chips first," as the assembly is

done before the substrate is completed and the IC bonding is direct to the substrate. It does not use flip-chip or wire bonding, but can utilize unmodified chips directly. A number of build-up layers and very fine geometry are possible. There are obvious advantages in making multichip modules and in using standard chips. The materials and bonding technologies have proven to be very reliable and suitable for military applications. The disadvantage is the maximum panel that can be sputtered. Future use of PVD/CVD metallization may make this process more cost-effective.

26.3.2.1.1 Structure. The circuit structure of HDI consists essentially of common conventional flex circuits or more advanced microvia flex structures. These are purchased for this process. The polyimide film is usually 25- or 50-micron adhesiveness. The laser ablates away the polyimide to produce blind and through vias. The through vias are stopped by the aluminum bonding pads of the integrated circuits. By doing this, integrated circuits designed for wire bonding can be directly attached.

26.3.2.1.2 Manufacturing Process. The process starts with a finished single-sided, double-sided, or multilayer polyimide flex circuit. An adhesive is applied to the flex circuit. All the ICs and components are bonded to the polyimide film layer pair flex circuitry and cured. The assembly is turned over and a laser drills down through the flex circuitry to make blind and through vias including opening up the bonding pads on the IC chip. Gold, underbump metallurgy, or C4 bumps are not required. The panel goes through tungsten sputtering to metalize the vias and seed the top layer. Circuit pattern can be applied, plated, and then etched to complete the circuit.[10,11]

26.3.2.2 Meiko-BU. Meiko Circuits of Japan takes a photoresist and coats it onto a stainless steel panel. This starts the process to produce high-density interconnect structures (HDIS) in a remarkable way. The advantages of

this process is that surface geometries are not determined by etching or full additive metallization, the vias are under the surface lands, and the circuits are all flush with the dielectric, permitting the elimination of solder masks. On the negative side, this is a more expensive process that involves carriers.

26.3.2.2.1 Structure. Figure 26.11 shows the structure of Meiko's build-up circuits. These are called carrier-formed because a stainless steel carrier serves as the base for the photodielectric even though they are laser-drilled to form the vias. The resulting structure is similar to other HDIs. The core is still a rigid board and the build-up layers are PID.

26.3.2.2.2 Manufacturing Process. The manufacturing process starts by taking a photoresist and coating it onto a stainless steel panel. The surface pattern is exposed and developed in the photoresist. First gold is plated, then nickel, and finally copper is plated on the panel. When the resist is stripped, the PID is applied over the entire panel and via holes are laser-drilled in the dielectric. Once metalized and plated, photoresists can define the circuitry by etching. The process can be repeated until the circuitry is complete or it can be laminated to FR-4 materials as rigidizers.[12,13]

26.3.2.3 CLLAVIS. The CLLAVIS build-up technology is marketed by CMK of Japan. This laser-drilled microvia technology is the most common of HDI processes. The construction is based on a filled buried vias in the multilayer core, as well as the optional filled microvias that can be stacked. This structure is also available with the simpler, unfilled staggered microvias.

26.3.2.4 SSP. The SSP technology was developed by Ibiden of Japan. It used standard FR-4, copper plating, and laser drilling. The additional step is the application of a thin adhesive to each finished single-sided, pump-plated core. The process sequence is as follows:

1. Start with single-sided copper-clad laminate.
2. Laser drill from the noncopper side.
3. Desmear laser holes and run through the electroless copper process.
4. Plate up bumps on the clad side.
5. Image and circuitize the copper side.
6. Apply a thin adhesive to the unclad side.

Repeat steps 1 to 6 for the remaining cores of the multilayer:

7. Lay up the finished cores with copper foil.
8. Vacuum laminate the finished layers.
9. Image and circuitize the outer layers
10. Coat the solder mask and finish.

26.3.2.5 FACT-EV. FACT-EV (Fujikiko Advanced Chemical Technology-Etched Via Post) is from Fujikiko of Japan. As with the SSP process, the via is a solid-plated copper post. In this case, the process uses standard dry-film photoresist to define the posts and a thin-liquid dielectric to coat the plated posts. Unlike SSP, however, the process is sequential and each two sets of layers are processed on the prior layers.

26.3.2.6 PPBU. The PPBU (Prepreg Build-Up), from CMK, is a standard sequential lamination process using laser-drilled vias similar to the CLLAVIS process.

26.3.2.7 Solid Conductive Via Fill. The next group of HDI technologies all utilize metal-particle pastes or a solid sheet of metal to form the via connections. Table 26.1 presents these alternatives to copper plating for forming IVH connections.

TABLE 26.1 Alternative HDI Technologies

Fabricator	Trade Name	IVH Process	Metallization
Dyconex	DYCOre	Copper etching	Etched copper bumps
Ormet	OrmeLink	Laser, plasma, or photodielectric	Cu/Sn organo-metallic
Matsushita Comp.	ALIVH	Laser	Copper particles in epoxy
Toshiba	Bbit	Insulation displacement	Silver/epoxy paste
Parelec	PARMOD	Drill, laser, or photodielectric	Metallo-organic decomposition, Cu or Ag
Namics	Unimec	Punch, drill	Silver, palladium, and copper particle pastes
North Corp.	NMBI NMTI (Neo-Manhattan)	Image and etch	Etched copper bump
Denso	PALUP	Laser	Cu organo-metallic
Ibiden	SSP	Laser	Plated copper bumps
Fujikiko	Fact-Ev	Photoprocessing	Plated copper posts

26.3.2.8 OrmeLink. CTS's colamination process and Ormet's transient liquid phase sintering (TLPS) process (OrmaLink) are similar to the ALIVH process conductive paste in that it is a via paste copper-tin organometallic matrix that sinters into a solid metallurgical via.

CTS's process is called ViaPly. Past users, in addition to Sheldahl (now Multek), included Litronics, now called Allied-Signal Substrates, in Costa Mesa, California. Up to four layer pairs have been connected (eight metal layers) using OrmeLink.

26.3.2.8.1 Structure. The Ormet structure is made up of polyimide or FR-4 layer pairs. Different materials can be mixed if a rigid core or heat spreader is required. The conductive paste is a TLPS ink of copper-tin. The structure is shown in Fig. 26.4. Figure 26.5 shows the cross-sections of two finished circuits with lasered-via polyimide layer pairs, with TLPS solid metallurgical vias connecting the layer pairs and FR-4 innerlayer cores with buried TLPS vias.

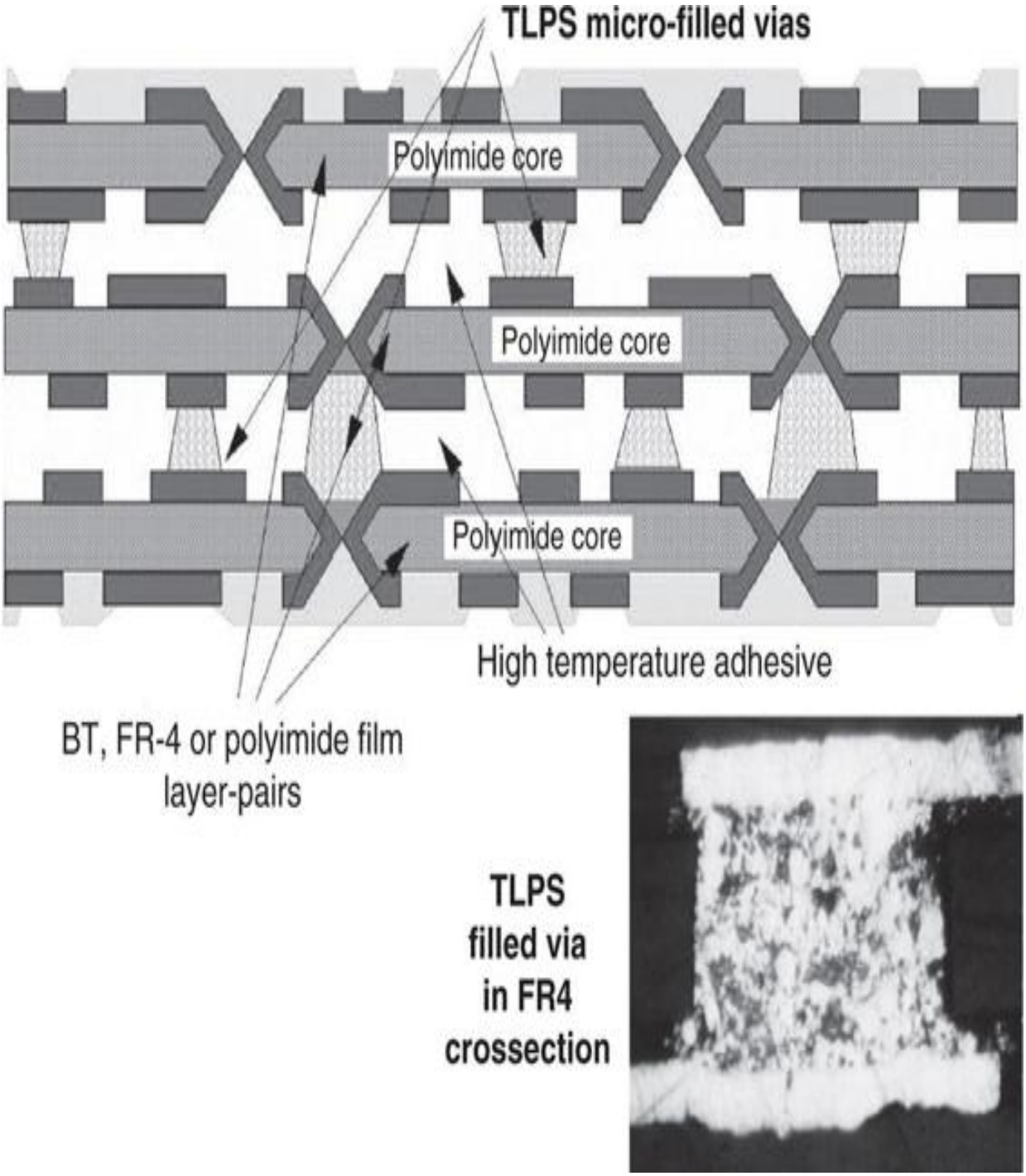
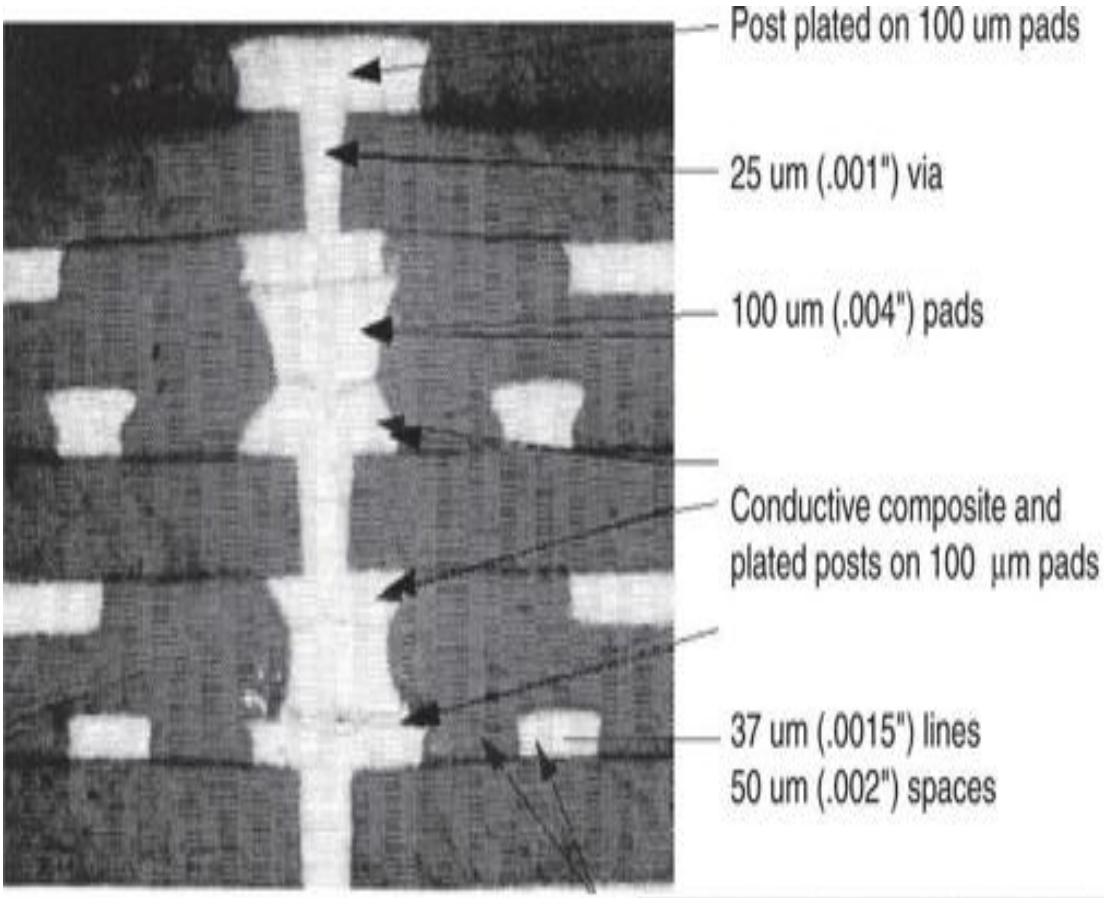


FIGURE 26.4 The colamination (OrmeLink) multilayer structure.



Double-sided flex circuit with 25 µm via

OrmeLink® 100 µm solid TLPS via

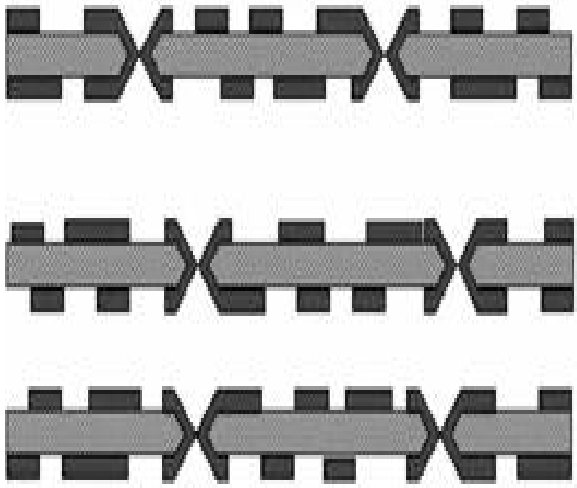
Perforated bond-ply dielectic

Photos courtesy Ormet Technology

FIGURE 26.5 Examples of TLPS cross-sections of three layer pairs with lasered-vias filled with TLPS paste vias and buried vias for FR-4 innerlayers.

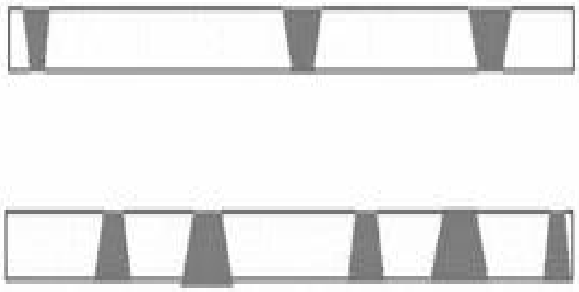
26.3.2.8.2 Manufacturing Process. The manufacturing process is shown in Fig. 26.6. The microvias are lasered or punched in the polymide adhesive and then filled with the TLPS paste. The structure can now take layer pairs from any other HDIS process (such as Sheldahl's) and turn them into a multilayer structure through sintering. The conductive pastes have to be sintered in a condensing vapor of fluorocarbon at 215°C for 2 min. The structure is then postcured by baking for 40 min. at 175°C. Table 26.2 details the process.

1. Acquire layer-pairs

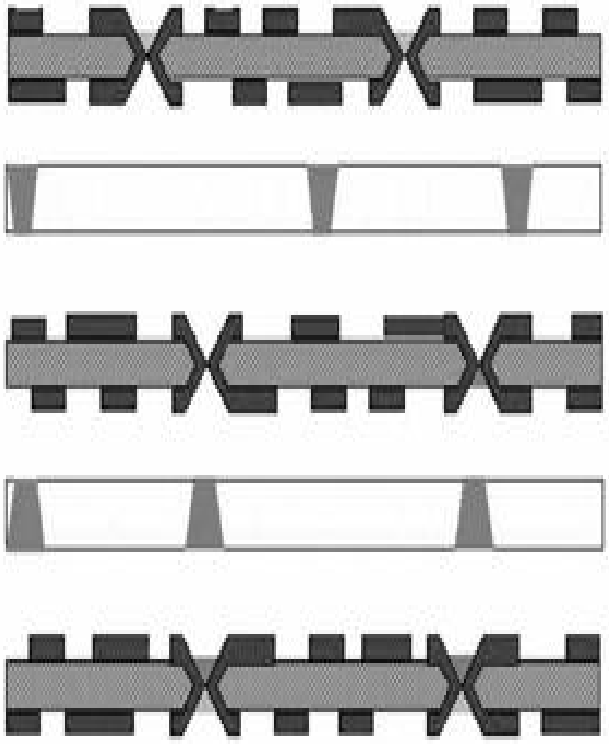


2. Generate vias in adhesive

3. Fill adhesive with TLPS metal paste



4. Lamination with paste filled adhesive



5. Sinter TLPS paste & Coat solder mask

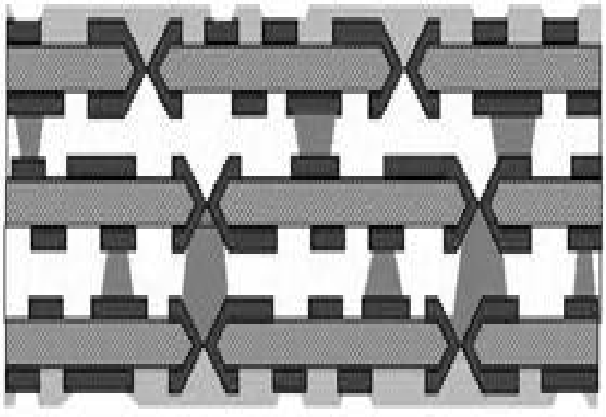


FIGURE 26.6 The OrmaLink multilayer substrate fabrication process.

TABLE 26.2 Properties and Curing Processes for the Ormet Type of TLPS Conductive Pastes

Property	Curing Process
Ormet 2005 series ink	Specification and processing parameter
Electrical conductivity	Bulk 4.0×10^{-3} Ω-cm Sheet resistance 10.0×10^{-3} Ω/sq. in
Adhesion (Tensile Pull) on Various Materials	
FR-4 (T_g = 125°C)	1300 psi (minimum)
Copper	2921 psi (average)
Printability	With 230 stainless steel wire mesh and emulsion thickness of 7.5 µm Sintered thickness 28–38 µm 200 µm traces on 400 µm pitch
Cure cycle	30 min drying at 85°C 2 min vapor cure at 215°C 40 min postcure at 175°C

26.3.2.9 ALIVH. The ALIVH (Any Layer Interstitial Via Hole) process has been in development for many years by Matsushita Components of Osaka, Japan. The novel process eliminates additive metallization and plating, but defines all features by subtractive etching of the copper foil. The build-up process is not sequential, though; it uses layer pairs and aramid-epoxy prepreg with copper-paste vias that can be laminated at one time into a three-dimensional structure. CMK (the second largest PCB maker in the world) and other Japanese firms have licensed the process. Six to 10 layers have been laminated in this way.

26.3.2.9.1 Structure. Figure 26.7 shows the structure and cross-sections for an ALIVH product. The PCB consists of laser-produced blind vias. The core material is an epoxy-aramid laminate. The man-made aramid filaments are ideal to be cut with a CO_2 or UV laser. If the DuPont Kevlar filaments are added, then the resulting material will have a very low coefficient of thermal expansion (CTE). This is useful for mounting ceramic packages and for direct attachment of flip-chip integrated circuits. The structure can be as simple as a two-sided PCB or as complex as a many-layered PCB. The vias consist of a copper-epoxy paste that connects the top and bottom copper foil. If used as a prepreg layer without copper, the vias connect the various ALIVH layer pairs into a multilayer structure. This is not a sequential build-up process, but rather a parallel build-up process.

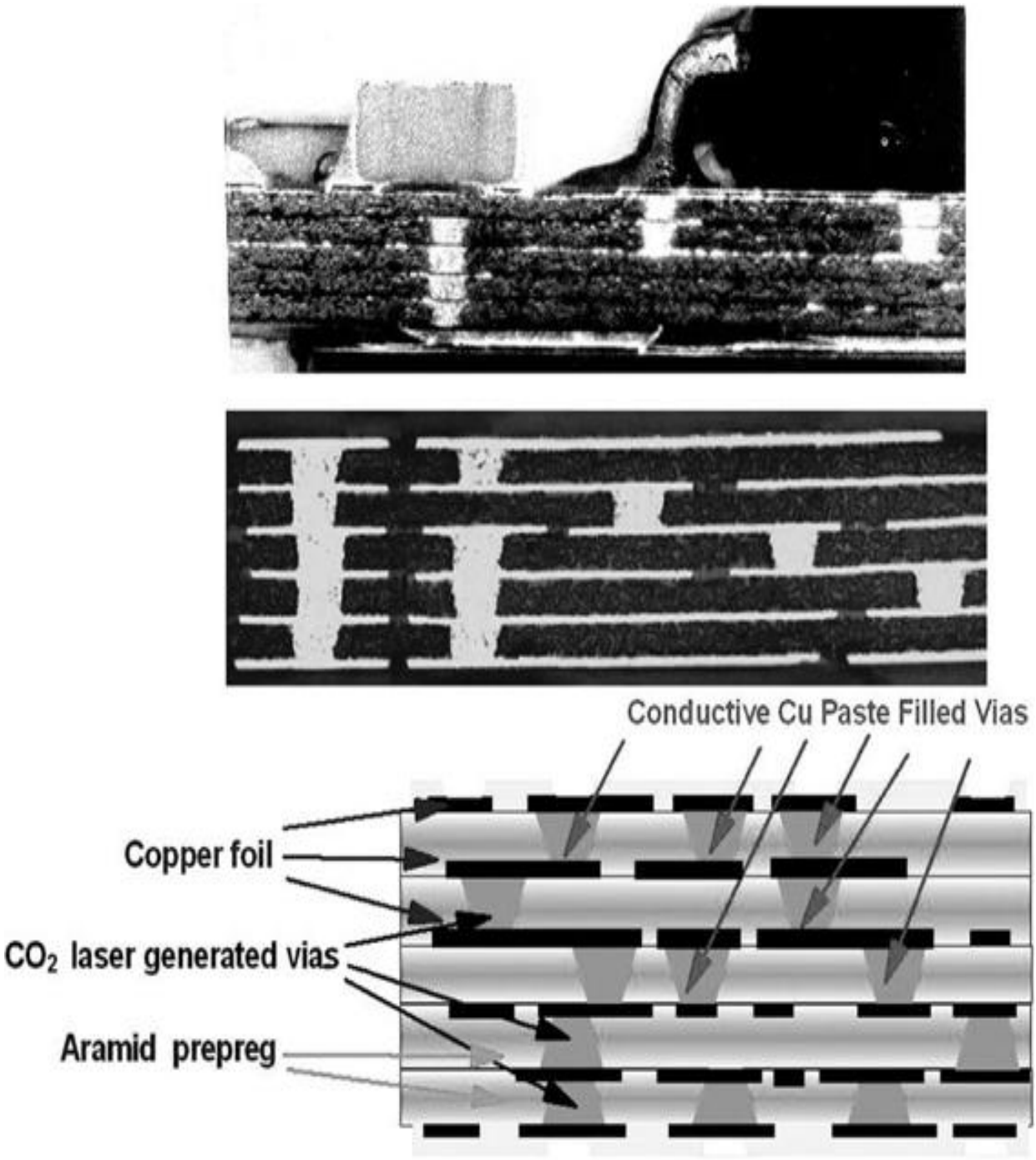


FIGURE 26.7 The parallel-bonded solid via structure of the ALIVH multilayer with cross-sections of examples.

26.3.2.9.2 Manufacturing Process. The ALIVH process is shown in Fig. 26.8. The process starts with an epoxy-aramid B-stage prepreg. The laser cutting of holes can proceed very rapidly. The material is then printed with a conductive paste

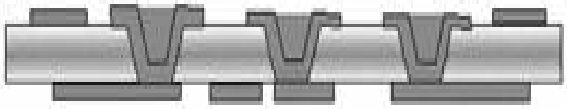
of copper and epoxy to fill these holes. Copper foil is applied and the structure is laminated to attach the foil and cure the prepreg and conductive pastes that serve as vias. The sheet of material is imaged and etched to provide the various circuits. Registration is less critical because the vias are now under the surface lands. Several of these two-sided layer pairs can be produced, inspected, and tested. The two-sided structures can then have additional single layers of B-stage/conductive paste layers with foil laminated to one or both sides, or the B-stage/conductive paste layer can be used to attach a number of layer pairs in one parallel lamination. The outside is imaged, etched, and completed as a normal PCB.

1. Laser drill prepreg 1

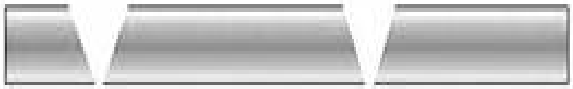
2. Fill prepreg with conductive paste 1

3. Laminate with copper foil 1

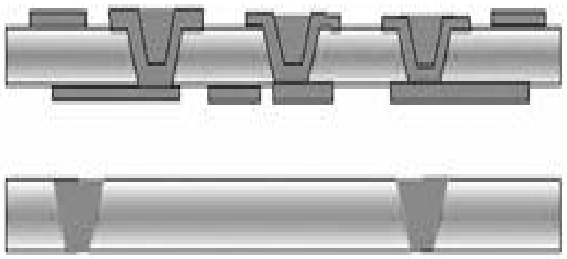
4. Circuitize 1 to N

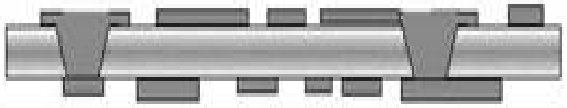


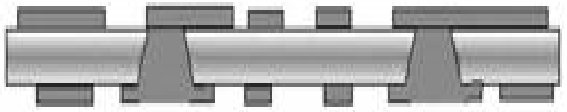
5. Laser drill prepreg 2



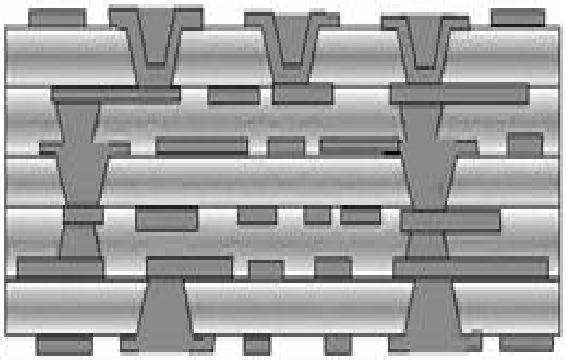
6. Fill prepreg with conductive paste 2







7.Co- Laminate with finished layer pairs 2



8. Coat solder mask & finish

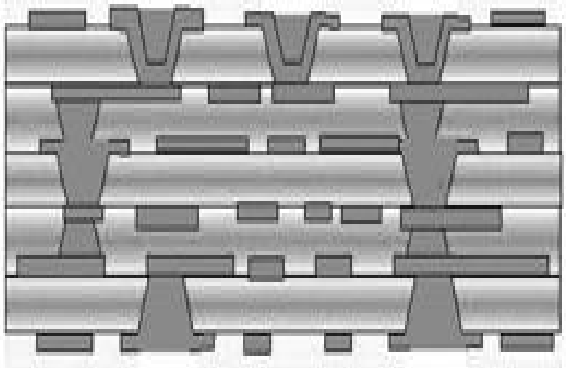


FIGURE 26.8 The ALIVH manufacturing sequence for a multilayer substrate.

An advanced manufacturing process results in a product known as ALIVH-FB. This product has a fine-line, tight via structure suitable for wire-bonding and flip-chip substrates, as shown in Fig. 26.9. The manufacturing process for each microvia technology begins with a base core, which may be a simple double-sided board carrying power and ground planes or a multilayer board carrying some signal pattern in addition to power and ground planes. The core usually has PTHs, which become blind via holes (BVHs). Such a core is often called an *active core*.

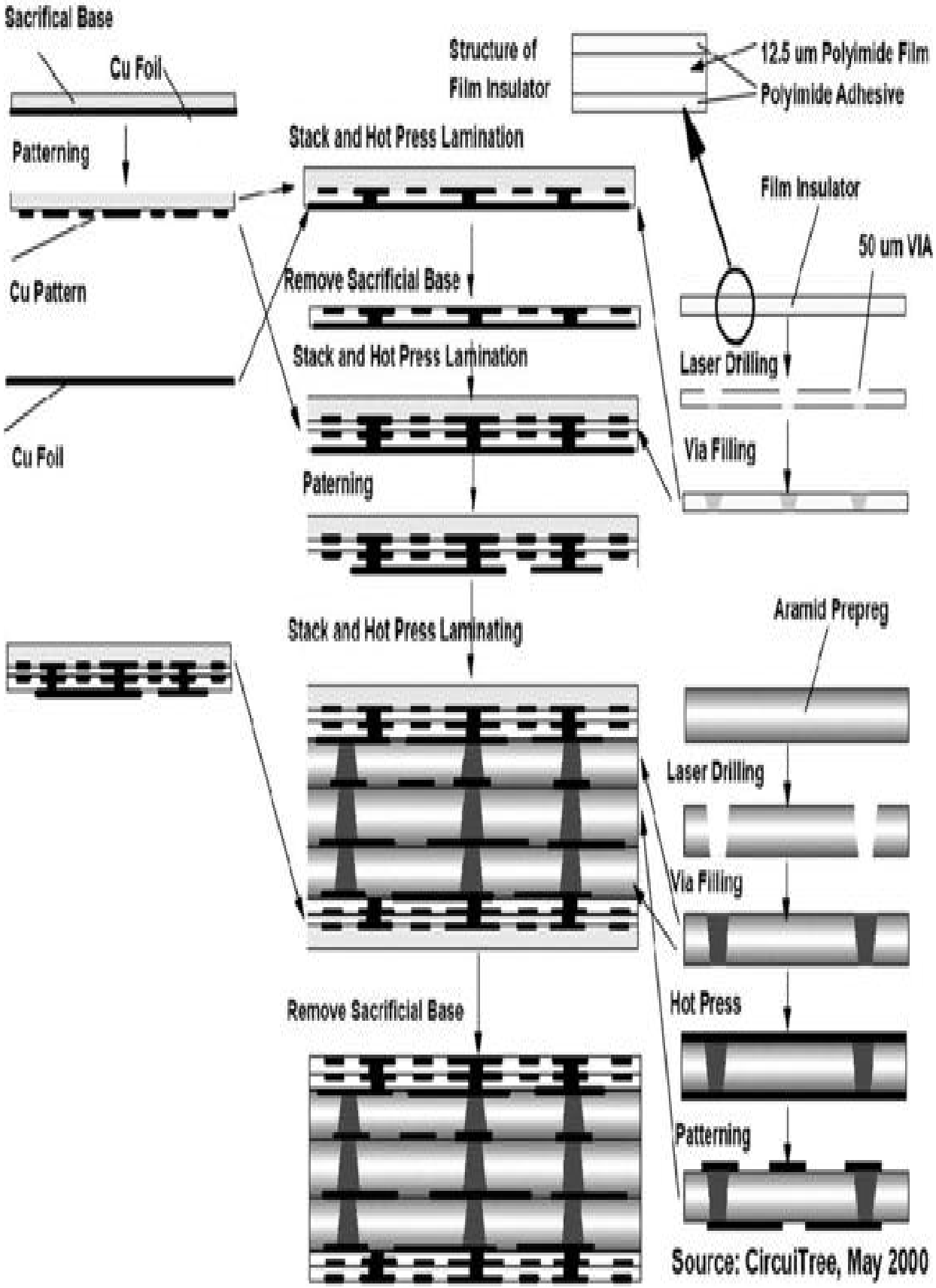

Sacrifical Base
Cu Foil
Patterning
Cu Pattern
Cu Foil
Structure of
Film Insulator
12.5 um Polyimide Film
Polyimide Adhesive
Stack and Hot Press Lamination
Film Insulator
50 um VIA
Remove Sacrificial Base
Stack and Hot Press Lamination
Laser Drilling
Via Filling
Paterning
Stack and Hot Press Laminating
Aramid Prepreg
Laser Drilling
Via Filling
Hot Press
Remove Sacrificial Base
Patterning
Source: CircuiTree, May 2000

FIGURE 26.9 The ALIVH-FB manufacturing process for a multilayer substrate. (*Illustration Courtesy of CircuiTree*.)

In fabricating a base core with a pattern, manufacturers usually panel-plate the core panel and create the pattern through a dry-film tenting process. Some makers seem to prefer pattern plating, however. The choice depends on the fabricator's familiarity with these processes. After the pattern is formed, dielectric material is laminated over the core (in the case of prepreg, with copper foil) and the holes can be filled with resins, depending on the plated hole diameter and the thickness of the core. It is generally agreed that when the diameter of plated holes is equal to or less than 0.3 mm and the core thickness is equal to 0.6 mm or less, these holes can be filled effectively by the lamination process (although the resin thickness of 80 µm is preferred in the case of RCC).

When the diameter and thickness conditions are not met, it is necessary to fill the holes by a separate process. A screening process does this from one side of the panel with a polyester screen that has an oversized hole pattern. After filling the holes the resin is cured completely.

26.3.2.10 MSF. Shinko of Japan developed the MSF HDI technology. It utilizes laser-drilled RCC materials and vias filled with a conductive paste. After testing, these are laminated into the parallel build-up structure.

26.3.2.11 PALAP. PALAP (Patterned Prepreg Layup Process) is a process that was developed by a consortium consisting of the Japanese firms Denso, Wako Corporation, Airex, Kyosha, Noda Screen, and O.K. Print. Originally, the process started with copper-clad laminates (CCL), but now utilizes thermoplastics like PEEK resins (polyether-ether ketone) or a new plastic called PAL-CLAD. PAL-CLAD is characterized by the electrical properties and heat resistance

of BIAC, a recyclable thermoplastic resin film produced by Japan Gore-Tex, Inc.

The single-lamination process compares favorably to conventional PCB processing, where lamination, curing, and wiring patterning are repeated layer after layer. PALUP boards can be multilayered by pressing together all thermoplastic resin layers, each having wiring patterns. This significantly improves quality, lowers costs, and shortens delivery times. PALAP boards also offer high-interconnecting reliability by adopting metallic paste for filling vias, and have excellent high-frequency properties due to a low dielectric constant.

PALAP boards also give due consideration to the environment, one of the major issues requiring action in the area of electronics products, including those used in information technology and automobiles. Because PALAP boards use thermoplastic resin as their base material, they enable material recycling in which only the resin is separated and reused.

26.3.2.12 VIL. The VIL (Victor Interconnected Layers) HDI technology was developed by Victor of Japan. It utilizes FR-4 prepreg materials that are laser-drilled and sequentially laminated after the vias are filled with a conductive paste.

26.3.3 Mechanical Drill-Via Technologies

Hitachi HITAVIA is an example of the mechanical drill-via technologies available.

26.3.3.1 HITAVIA. The Hitachi HITAVIA technology is the only HDI process developed for use with conventional mechanical drilling. It utilizes RCC or prepreg materials that are mechanically drilled and sequentially laminated after the

vias are filled with a conventional electroless copper and copper plating. The typical manufacturing sequence for this HDI technology is similar to that of previously described HDI processes such as CLLAVIS and PPBU.

26.3.4 Plasma-Via Technologies

Plasma-via technologies include DYCOstrate, plasma micromilling, and plasma-etched redistribution layers (PERL).

26.3.4.1 DYCOstrate. Starting in 1989, Dr. Walter Schmidt of Contraves in Switzerland developed the plasma-etching process for microvias. Evolving from the traditional plasma desmear process, the plasma etcher for vias was jointly developed by Dyconex (successor to Contraves) and Technic Plasma of Germany. Dyconex trademarked and patented its via-generation process as DYCOstrate. Hewlett Packard licensed the technology in 1993 and developed it for mass, low-cost production. The low-cost production process of Hewlett Packard is called PERL (for plasma-etched redistribution layers).

DYCOstrate, along with SLC and Finstrate, is among the most enduring production processes for microvias generation. The DYCOstrate process was first employed for high-reliability military, aerospace, medical, and IC packaging starting in 1991. Since that time, Dyconex has used the process to produce hundreds of different printed boards both in polyimide film and with the new laminates called FR-4 RCC. This Dyconex called DYCOstrate-C.

26.3.4.1.1 Structure. Figure 26.10 shows the structure of DYCOstrate. The core material can be polyimide film with plasma-etched holes, drilled epoxy fiberglass, or other plasma-etchable materials such as liquid crystal polymers. Multiple layers can be built up to increase density with the resulting buried and blind vias, but two-sided DYCOstrate

structures are also used in products because of the very high density that 0.075 mm through holes allow.

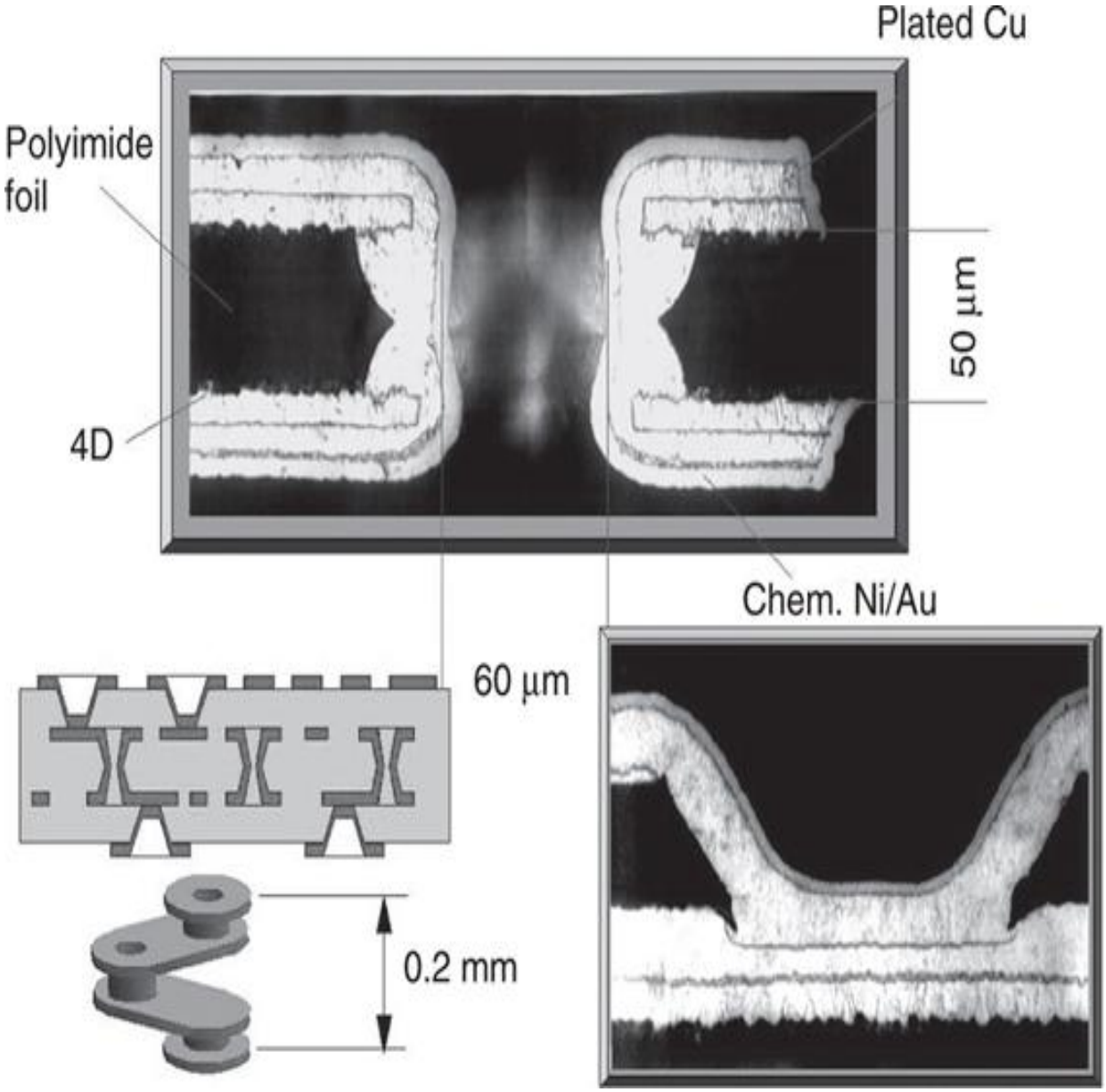


FIGURE 26.10 The DYCOstrate multilayer structure and cross-sections of through and blind vias.

26.3.4.1.2 Manufacturing Process. The manufacturing process for a DYCOstrate substrate utilizes common printed circuit board techniques. Only the via-generation process is different. To produce a plasma-etched via hole,

manufacturers use two or three process steps that replace the conventional mechanical drilling-debur-desmear steps:

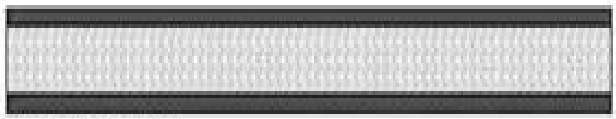
1. Define photographically the location and geometry of the via holes.
2. Etch an opening in the copper foil that will serve as the resist mask.
3. For blind vias, reduce the copper-foil thickness to eliminate the copper overhang.

Figure 26.10 shows microsections of a plated through hole and a blind via in polyimide film. The plasma-etch procedure is basically an isotropic process, as indicated by the undercut seen on the through hole; considering the actual dimensions, however, this undercut is too small to cause any plating problems.

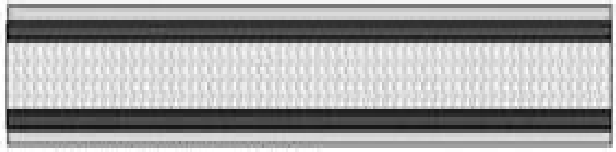
When the etching depth is increased, as in the case of a blind via, the resulting undercut is generally too big to allow reliable plating. To overcome this problem, the manufacturer can reduce copper use by etching the copper foil, eliminating the copper overhang, and providing a thinner copper foil for fine-line resolution.

Figure 26.12a shows two common products made with the Dycostrate process [a four-layer flex-multilayer chip-on-board (COB) for a hearing aid] and the PERL process (a six-layer FR-4 COB for a networking module).

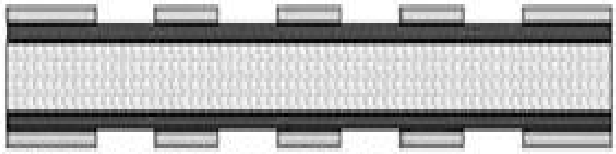
The manufacturing process for a DYCOstrate substrate with a standard four-layer build-up is shown in Fig. 26.11. Starting with a prefabricated double-sided DYCOstrate foil, the manufacturer bonds two single-sided copper clad foils to the center-core foil using standard lamination techniques of mass-lam-like process. The resulting four-layer structure is then processed and structured analog to the two-layer foil, producing blind vias instead of through holes.



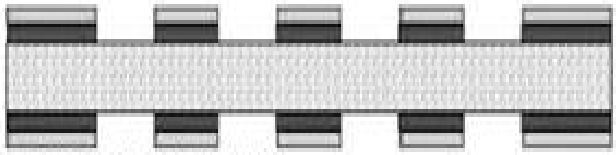
BASE MATERIAL



FOIL COATED WITH RESIST

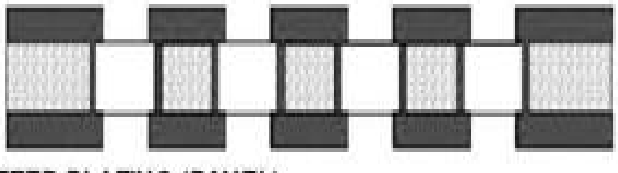


RESIST EXPOSED AND DEVELOPED



AFTER COPPER ETCHING

AFTER PLASMA ETCHING

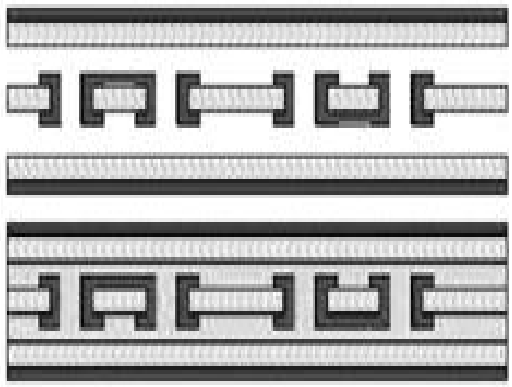


AFTER PLATING (PANEL)

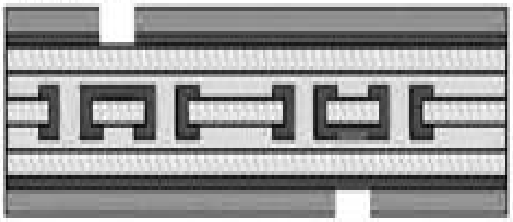
SS-FLEX MATERIAL

DS-DYCOstrate

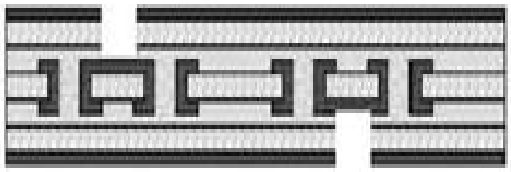
SS-FLEX MATERIAL



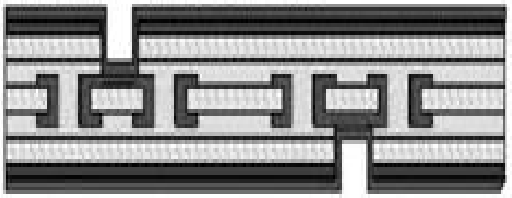
1. LAMINATION



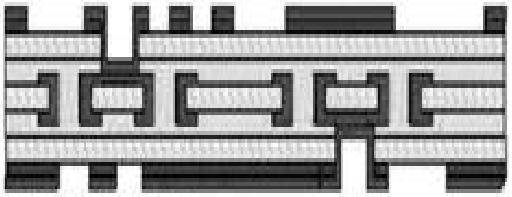
2. PHOTODEFINITION OF VIAS



3. PLASMA ETCHING OF VIAS



4. PLATING (PANEL)



5. CIRCUITIZATION

FIGURE 26.11 The DYCOstrate multilayer manufacturing sequence for a four-layer substrate.

Further refinements in magnetrons for IC manufacturing provide the opportunity for finer plasma-etched vias. Additionally, Dyconex has demonstrated landless vias to be simple and reliable, offering much higher densities at lower cost and simplifying fabrication registration.

26.3.4.2 Plasma Micromilling. The drilling of simple holes is not the only process in which plasma etching is used. Plasma can be also be used to sculpture the surface of the substrate or to fabricate slots, grooves, stepped windows, and more. Even angled vias or tubular systems can be formed. This is useful since cavities can be formed for wire bonding or recessed mounting of components. A simple definition of the periphery outline by artwork can provide extremely accurate final fabrication, or windows in the final etch step can define areas that will flex.

26.3.4.3 Plasma-Etched Redistribution Layers. The plasma-etched redistribution layer (PERL) process was developed by Hewlett Packard to produce microblind and buried vias using the DYCOstrate plasma via process. The materials used are the FR-4 epoxy-coated copper foils (RCC) to replace epoxy-glass prepregs in normal multilayer production. These are copper foils coated with a B-stage epoxy or dual C-stage/B-stage epoxy films.

26.3.4.3.1 Structure. The structure of DYCOstrate PERL is shown in Fig. 26.11. The core material can be standard FR-4 multilayer innerlayers or a through-hole-plated two-sided or multilayer board. Multiple layers can be built up to increase density with the resulting buried and blind vias. Current production ranges from 4 layers to 12 layers with various buried board and buried via constructions. As with DYCOstrate, many materials are plasma-etchable and the resin butter-coated copper foils come in many thicknesses

and resin types, such as BT, cyanate ester, and polyphenelene-ether (PPE).

26.3.4.3.2 Manufacturing Process. The manufacturing process for a DYCOstrate PERL substrate utilizes common printed circuit board techniques. Only the via-generation process is different. To produce a plasma-etched via hole requires only two or three process steps that replace the conventional mechanical drilling-debur-desmear steps:

1. Define photographically the location and geometry of the via holes.
2. Etch an opening in the copper foil that will serve as the resist mask.
3. For blind vias, reduce the copper-foil thickness to eliminate the copper overhang.

The manufacturing process for a DYCOstrate PERL substrate with a standard four-layer build-up starts with FR-4 innerlayers or a prefabricated double-sided or multilayer board. Two single-sided copper foils with resin coatings are bonded to the center-core foil using standard lamination techniques. This structure could also be procured through standard masslam channels. The resulting four-layer structure is then processed and structured analog to the two-layer DYCOstrate foil, producing blind vias. Through holes can be added or they can be in the preexisting buried board.

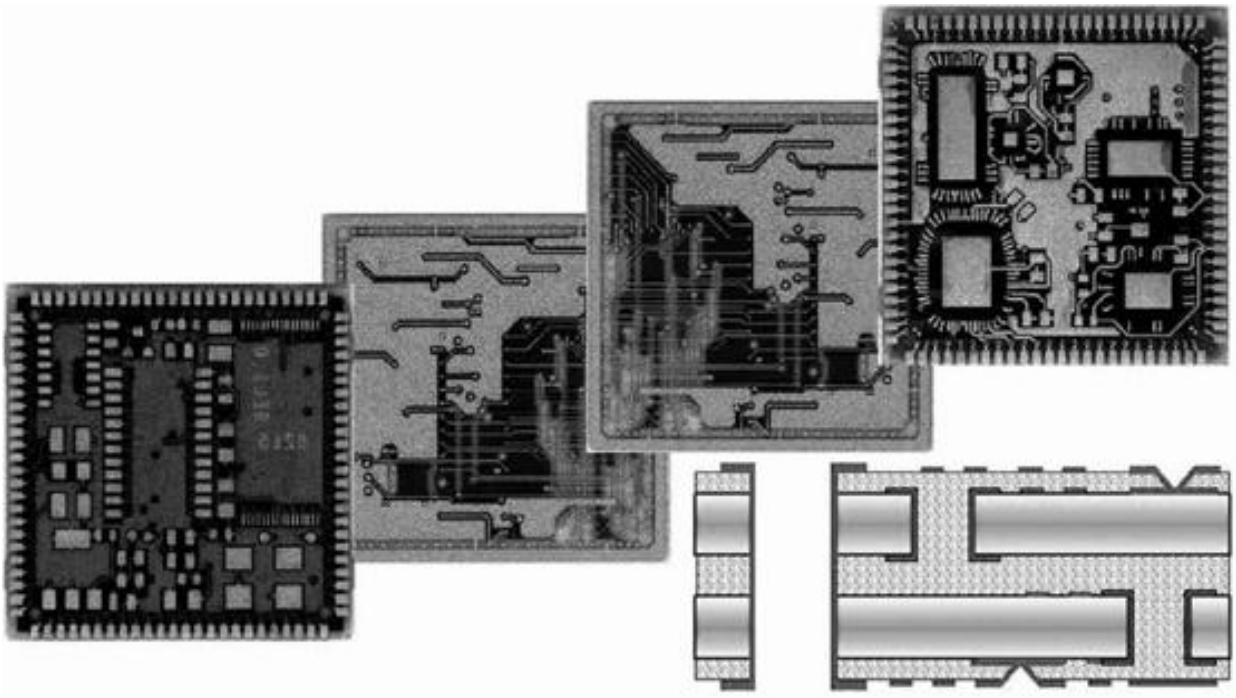
26.3.5 Screen-Printed Via Technologies[11]

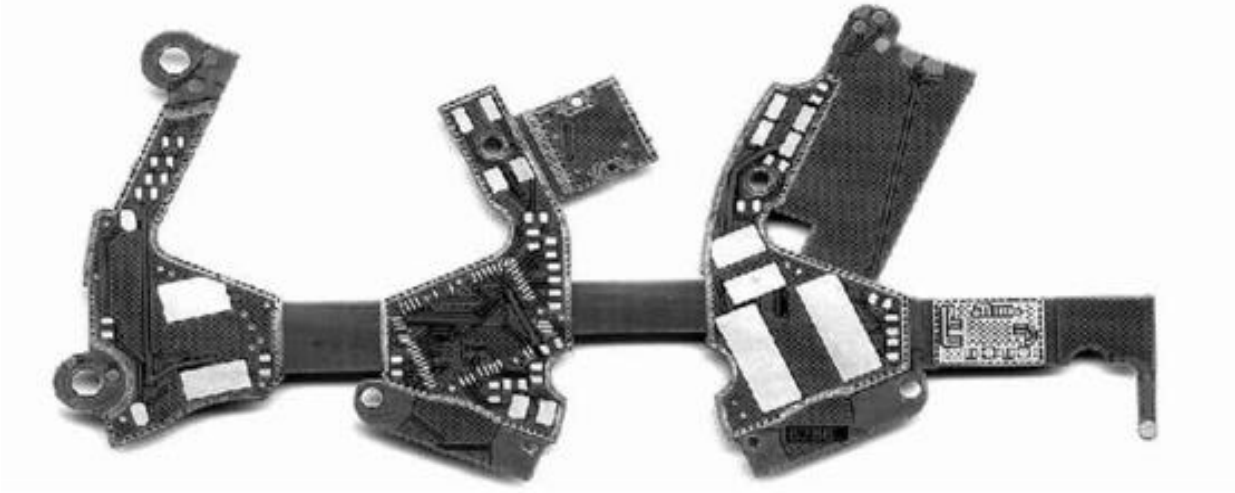
Toshiba's new Buried Bump Interconnect Technology is a new screen-printed via process.

26.3.5.1 Buried Bump Interconnect Technology (BBIT). Toshiba has developed a new process referred to as

BBIT (Buried Bump Interconnection Technology). With this process, a conductive paste is employed to replace via drilling, additive metallization, and via plating. The process has the advantage that hole-producing equipment is not required. Instead, a screened silver-epoxy paste is cured to be pointed like a thumbtack. This paste displaces the glass and epoxy during lamination to connect to the copper on the opposite side of the prepreg. The mass via-generation techniques, the simplification of metallization, and the fact that no drilling equipment is required make this new technique potentially very inexpensive. Currently, the design rules and features are for consumer products, but future uses are for simple plastic ball grid arrays (PBGAs).

26.3.5.1.1 Structure. The BBIT structure appears similar to that of other PCBs employing conductive paste vias. As shown in Fig. 26.12b, the structure is similar to ALIVH. The difference is that the BBIT structure uses standard FR-4 materials and a novel way to produce a via.





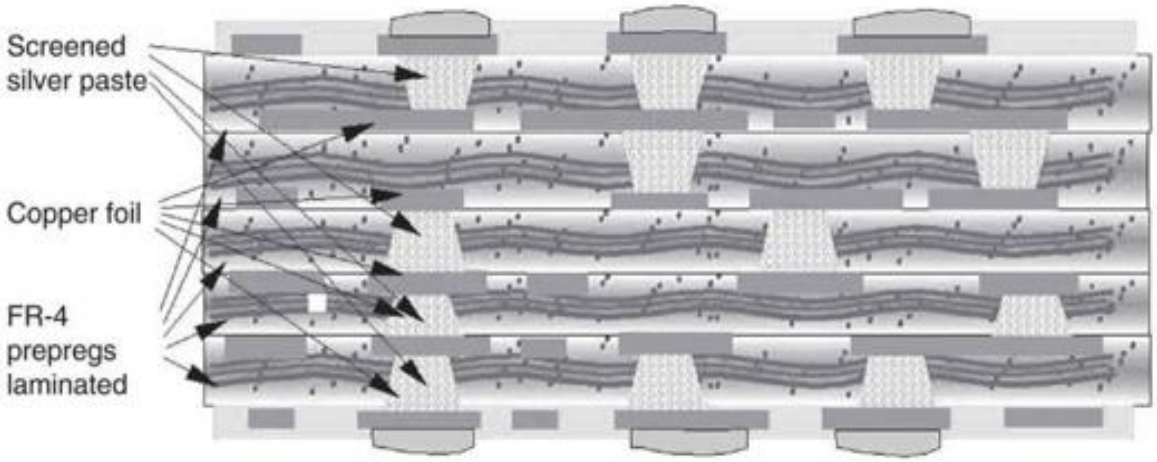
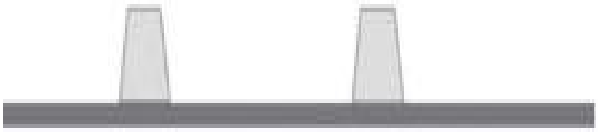

Screened
silver paste
Copper foil
FR-4
prepregs
laminated

FIGURE 26.12 (*a*) DYCOstrate and PERL multilayer examples; (*b*) structure of the BBIT substrate.

26.3.5.1.2 Manufacturing Process. A silver ink is screened on copper foil in the locations where vias are required. This copper is used in the manufacture of standard FR-4 laminate. The silver paste thumbtack-like obstruction forces itself through the glass cloth during lamination to connect itself to the copper foil on the other side of the laminate and to cure the prepreg. The sheet of material is imaged and etched to provide the various circuits. Registration is less critical because the vias are now under the surface lands. Several of these two-sided layer pairs can be produced, inspected, and tested. The two-sided structures can then have additional single layers of B-stage/conductive paste layers with foil laminated to one or both sides, or the B-stage/conductive paste layer can be used to attach a number of layer pairs in one parallel lamination. The outside is imaged, etched, and completed as a normal PCB. This process is seen in Fig. 26.13.

1. Screen silver paste on copper foil

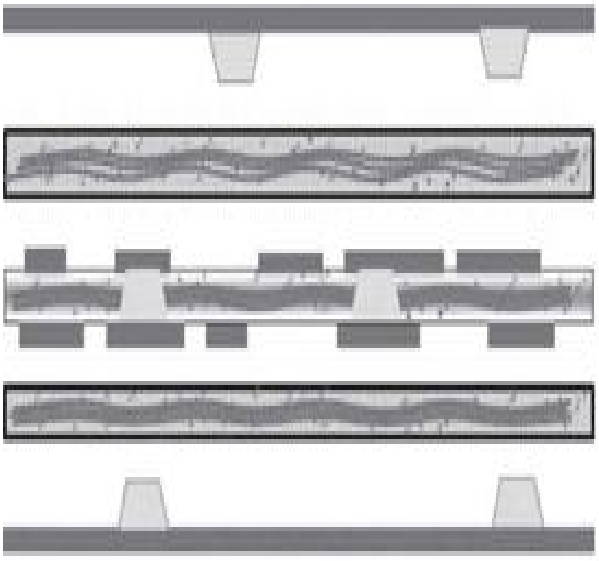


2. Cure screened bumps

3. Laminate with bumped copper foil 1, prepreg & foil

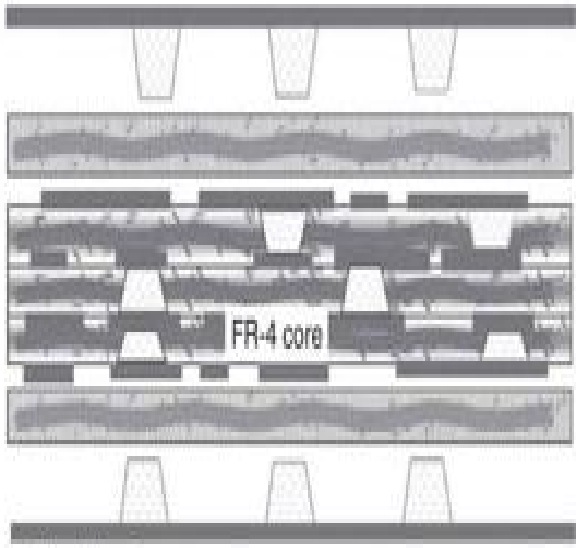
4. Circuitize 1

5. Laminate with bumped copper foil 2 & prepreg

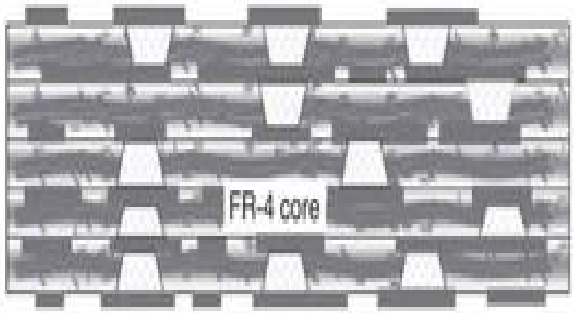


6. Circuitize 2

7. Lamination with bumped copper foils 3 & prepreg



8. Circuitize 3



9. Coat solder mask

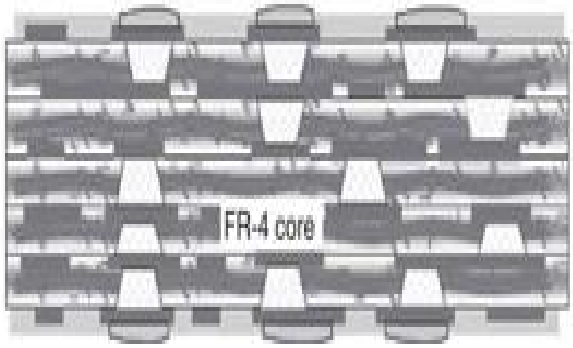
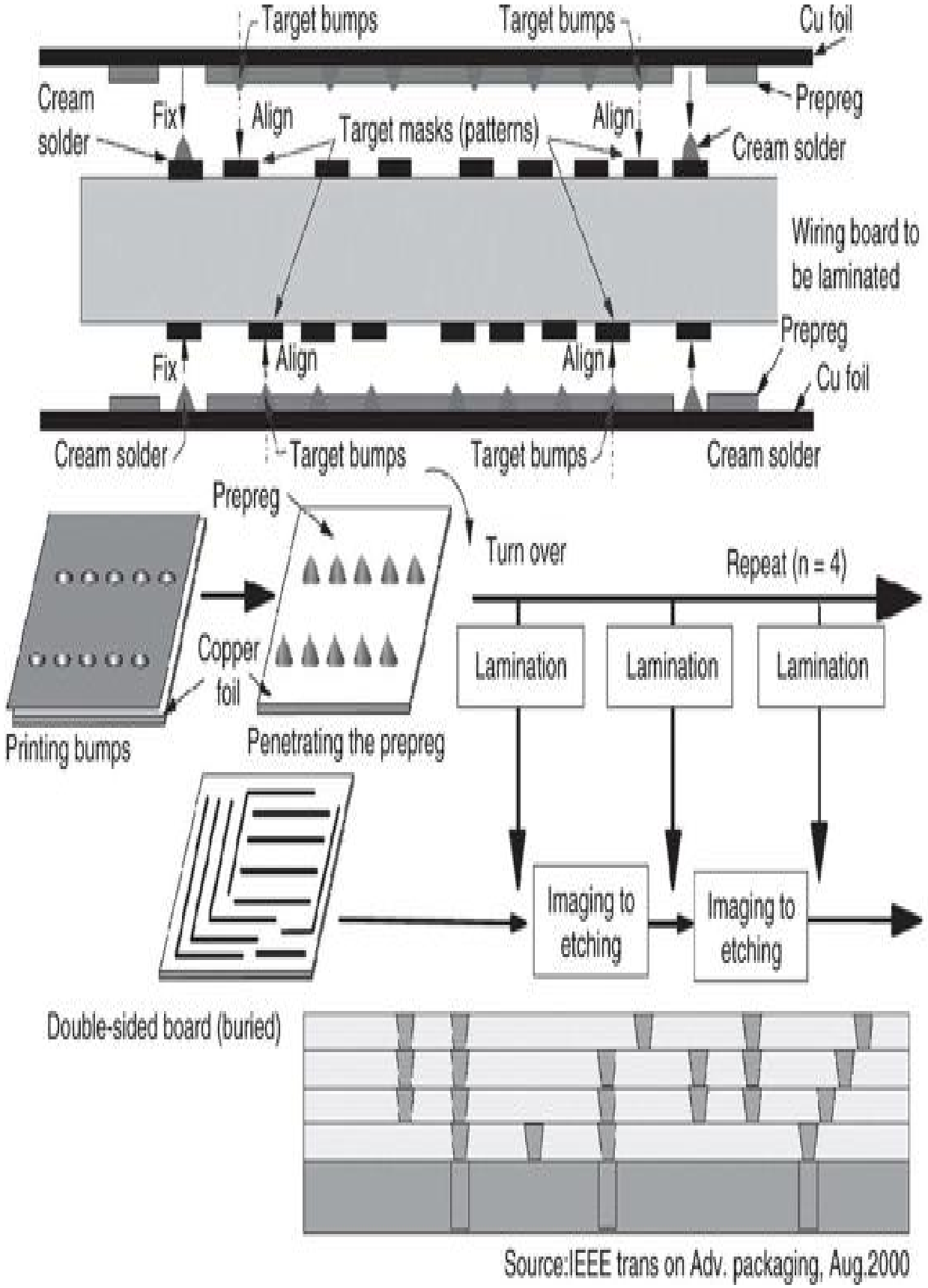


FIGURE 26.13 The manufacturing process for BBIT boards.

A newer BBIT process has been defined to manufacture wire-bonding and flip-chip substrates. In this BBIT process (shown in Fig. 26.14), the prepreg is laser-drilled so that smaller cream Ag solder can be used to bond to the copper.



Source:IEEE trans on Adv. packaging, Aug.2000

FIGURE 26.14 The manufacturing process for the fine-pitch BBIT substrates.

26.3.6 Photo-Defined/Etched-Via Technologies

Neo-Manhattan Bump Interconnect is an example of the photo-defined and etched-via technologies available.

26.3.6.1 Neo-Manhattan Bump Interconnect (NMBI). The NMBI technology is one of the newest of the Japanese HDI technologies. It might be considered a "third-generation" HDI technology after technologies as ALIVH is considered a second-generation HDI technology. NMBI was pioneered by North Corporation of Japan.

26.3.6.1.1 Structure. Figure 26.15 shows the structure of an NMBI substrate. Also in this figure is a scanning electron microscope (SEM) of the etched-metal bumps that make up NMBI's via interconnects.

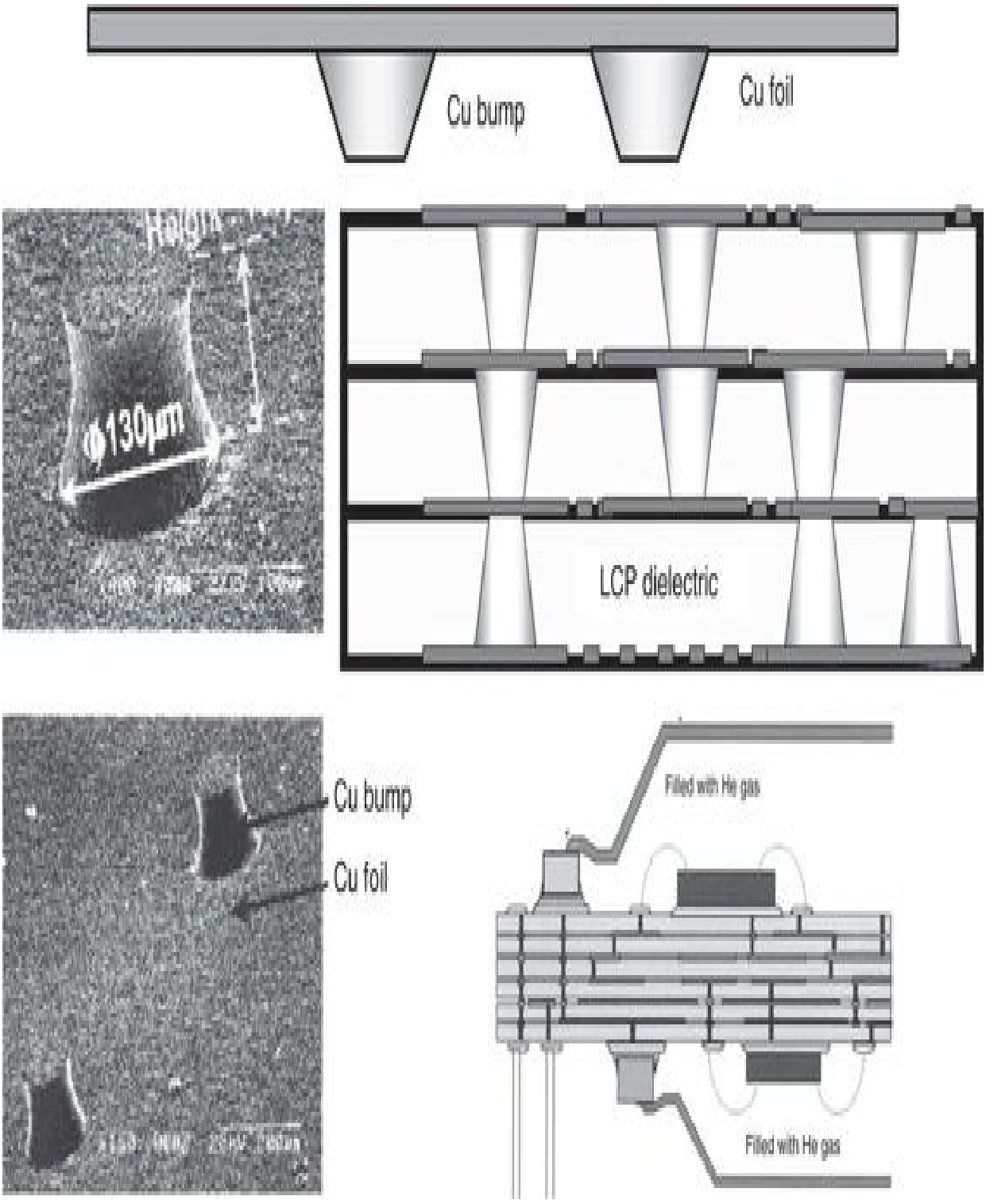


FIGURE 26.15 The neo-Manhattan bump interconnect structure.

26.3.6.1.2 Manufacturing Process. The manufacturing process for NMBI is unusual in that it does not drill the via

connections. Instead, a new material is employed that consists of two different coppers (one thicker than the other) that are bonded together. The thicker copper is imaged and etched to form the interconnect vias. This structure is then filled with a film or liquid dielectric. It is bonded to copper foil and both are cured. These copper foils are then imaged and etched to circuitize the layer pair. The layer pairs can be tested and later be stacked with uncured NMBI structures to form the final multilayer. Like the second-generation ALIVH HDI structure, an NMBI structure allows the connection of any layer to any other layer. This manufacturing process is shown in Fig. 26.16.

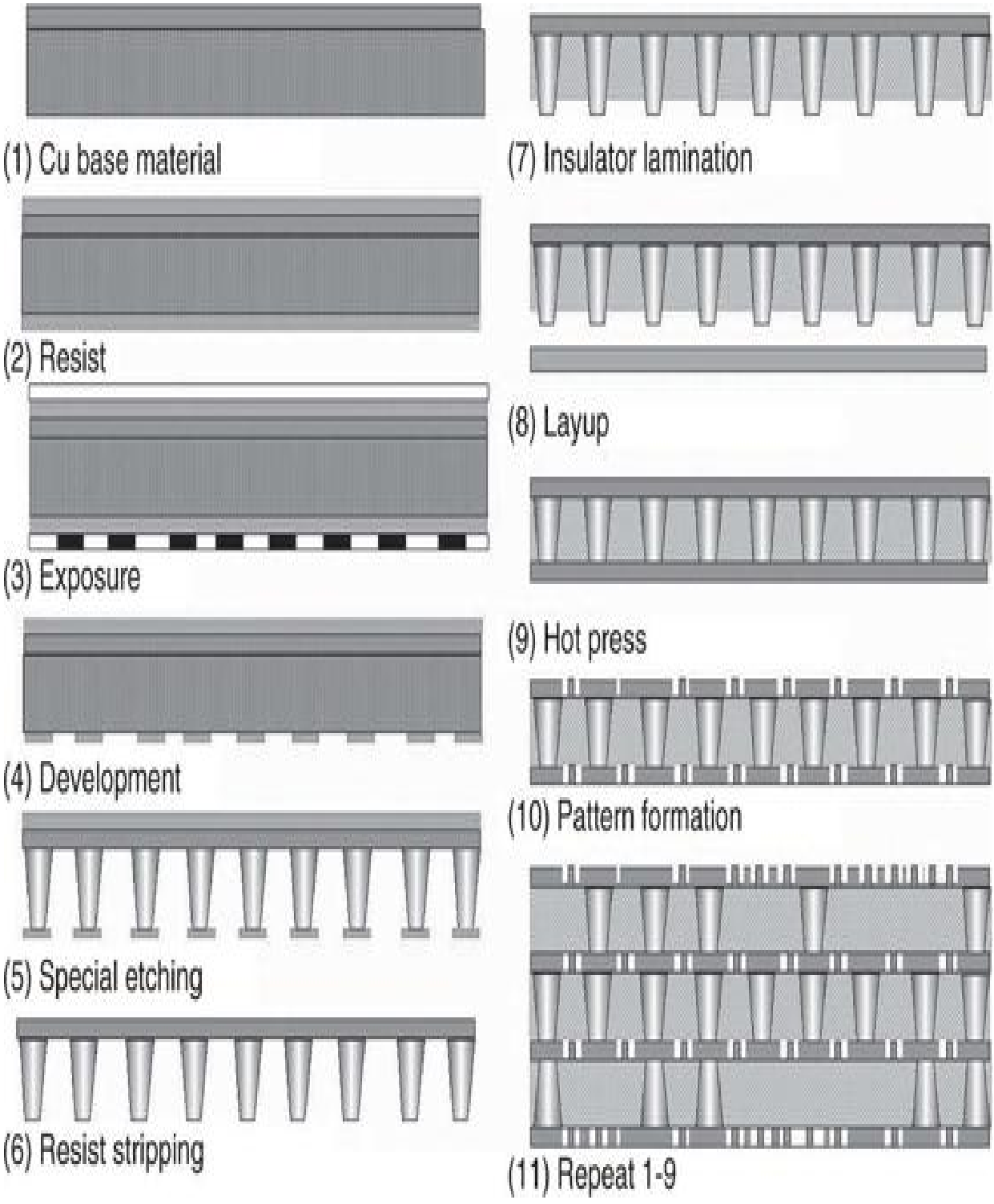


FIGURE 26.16 The manufacturing process for the NMBI substrates.

26.3.7 ToolFoil Technologies

Imprinted circuits are an example of a ToolFoil technology.

26.3.7.1 Imprinted Circuits. Imprint pattering is a similar technique used to manufacture compact discs (CDs). No photoresist, registration, or conventional techniques are employed.

Every substrate is a copy of the mold (or ToolFoil, in this case), and each can be done in sequence to make a build-up substrate. The unique characteristic of CDs and DVDs is the millions of 0.5 micron pits or vias. A typical CD includes over 3 km of these. The simple manufacturing process and perfect reproduction of the master tool creates inexpensive and accurate substrates. The patented process is a lab process; actual complexity is still under evaluation.

26.3.7.1.1 Structure. Figure 26.17 shows a diagram of the imprinted circuit structure, whereas Fig. 26.18 shows SEMs of an imprint-patterned circuit. The unique characteristic of this structure is that all features are embedded in the substrate. The critical dielectric is the part that is imprinted or molded. A long fiber molding compound, such as that used on components' overmolding, is best suited for this task. Such a compound can be used with or without an FR-4 backing. The cross section of an imprint circuit shows the features similar to a CD or DVD, that is, the various impressions. All are metallized but the vias are deeper. This allows the vias to contact the next layer of imprinted circuits.

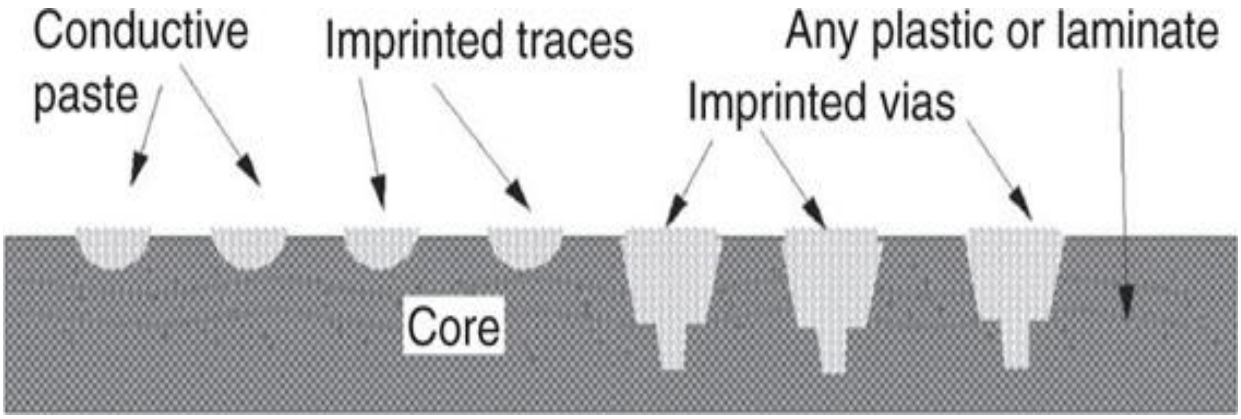
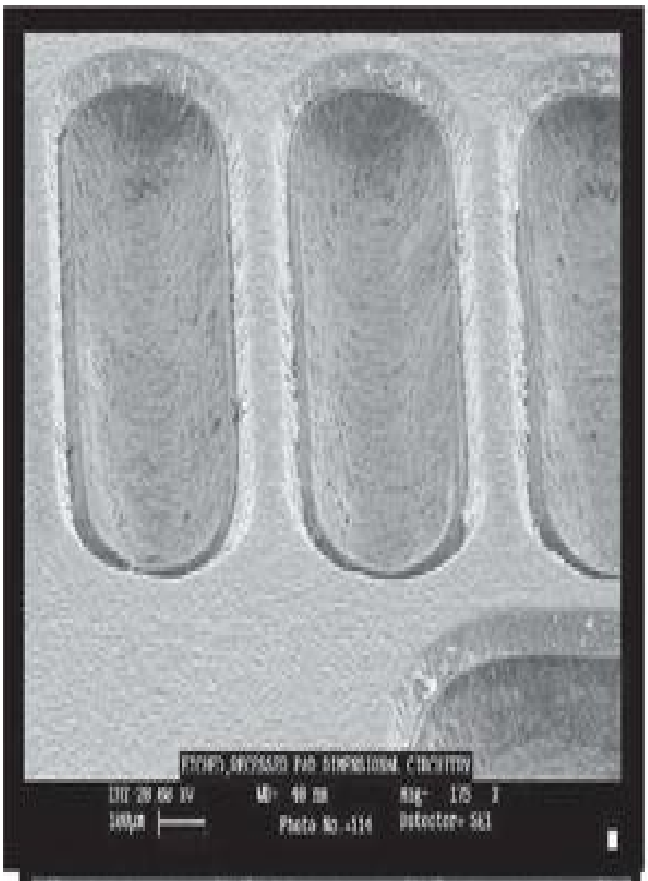
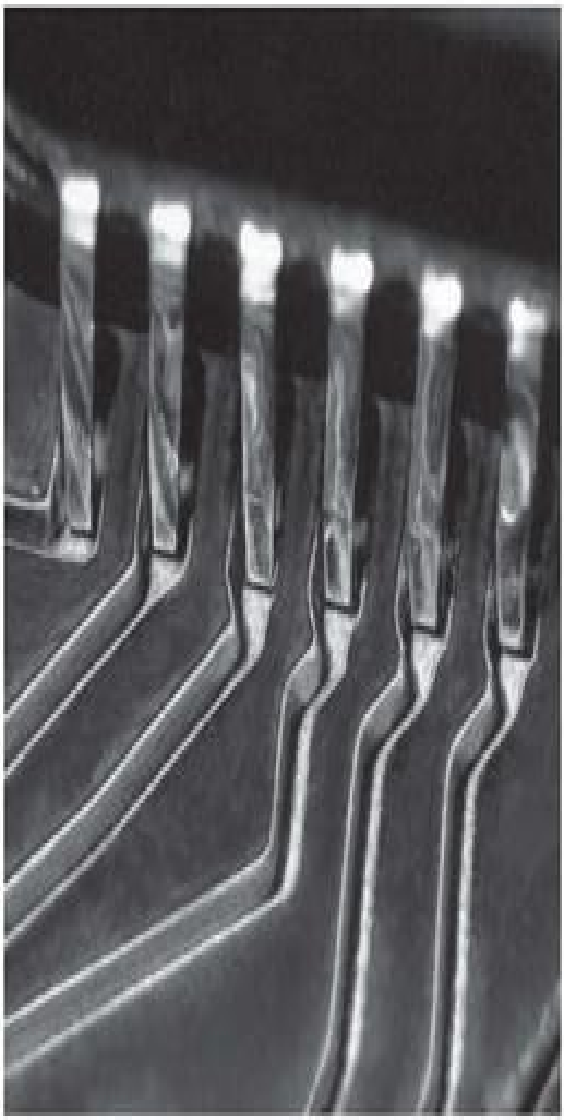


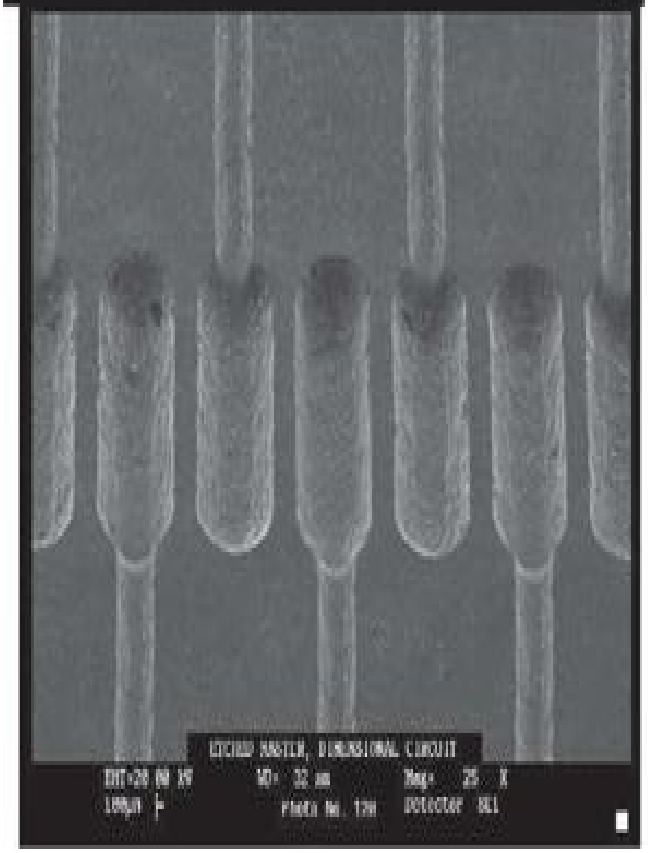
FIGURE 26.17 A simplified diagram of the imprinted printed circuit structure.



12 mil SMT land with ~ 17 microns of copper

30 mil pitch SMT without the solder paste





25 mil pitch SMT lands with 4 mil traces

FIGURE 26.18 Various views of SEMs of imprinted circuit liquids and traces. (*Courtesy of Dimensional Circuits*.)

26.3.7.1.2 Manufacturing Process. A master of the substrate is machined in copper by a UV laser or by photochemical machining. The vias are deep, and the circuits and pads are shallow. Since only one master tool, called a ToolFoil, is required, time can be taken to make sure the master is perfect. With a laser, it is possible to have perfect registration of lands to via holes or even landless vias. This master is electroformed with nickel and back-filled to make a master tool. A sample ToolFoil is shown in Fig. 26.19.

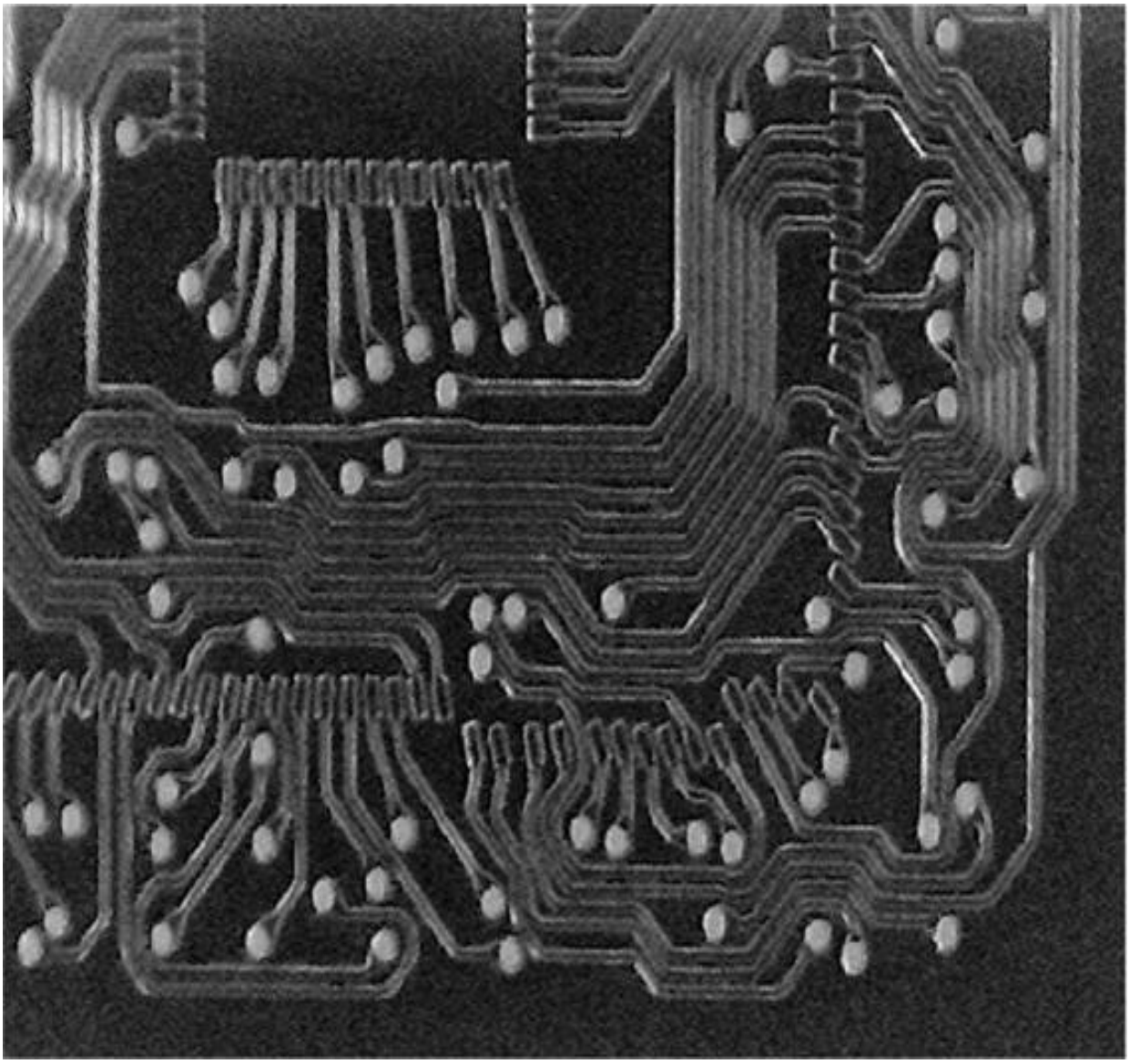


FIGURE 26.19 Example of a ToolFoil for imprinting. (*Courtesy of Dimensional Circuits*.)

For production, the mold is filled with a thermoset or thermoplastic resin and then cured. The substrate is additive or semi-additive metallized, and plated thicker with copper. The recesses are filled with an etch resist, and the surface resist is removed to expose the copper surface by polishing or by using an abrasive agent. The exposed copper is etched away and the etch resist is dissolved. The entire manufacturing process does not employ photoresists,

exposure, or registration. Because of this, the yield is expected to be very high.

26.4 NEXT-GENERATION HDI PROCESSES

HDI and microvias provide a big boost in density due to miniaturization. These technologies will continue to evolve and become smaller, following integrated circuit cell geometries. So the next revolution will be in optical wiring. Currently, optical networking ties together continents and cities, providing the backbone of modern worldwide networking. The fiercely competitive market is what technology will provide “the last mile” on connectivity? Optical wiring is competing for that market.

26.4.1 Embedded Optical Waveguides

Although electrical signals can be multiplexed on a single 100 micron wire or trace, many individual laser wavelengths can each carry many multiplexed signals on a single 100 micron wide waveguide. This results in a 10,000× increase in information handling while not being influenced by magnetic and electrical fields such as electronic signals. These optical conduits can now be mass produced on a printed circuits as polymer optical waveguides, as shown in Fig. 26.20 [12]. Much like when the industry transitioned from single-point soldering by individual wires to printed circuits, single-point fiber-optical cabling can now have low-cost printed waveguides.

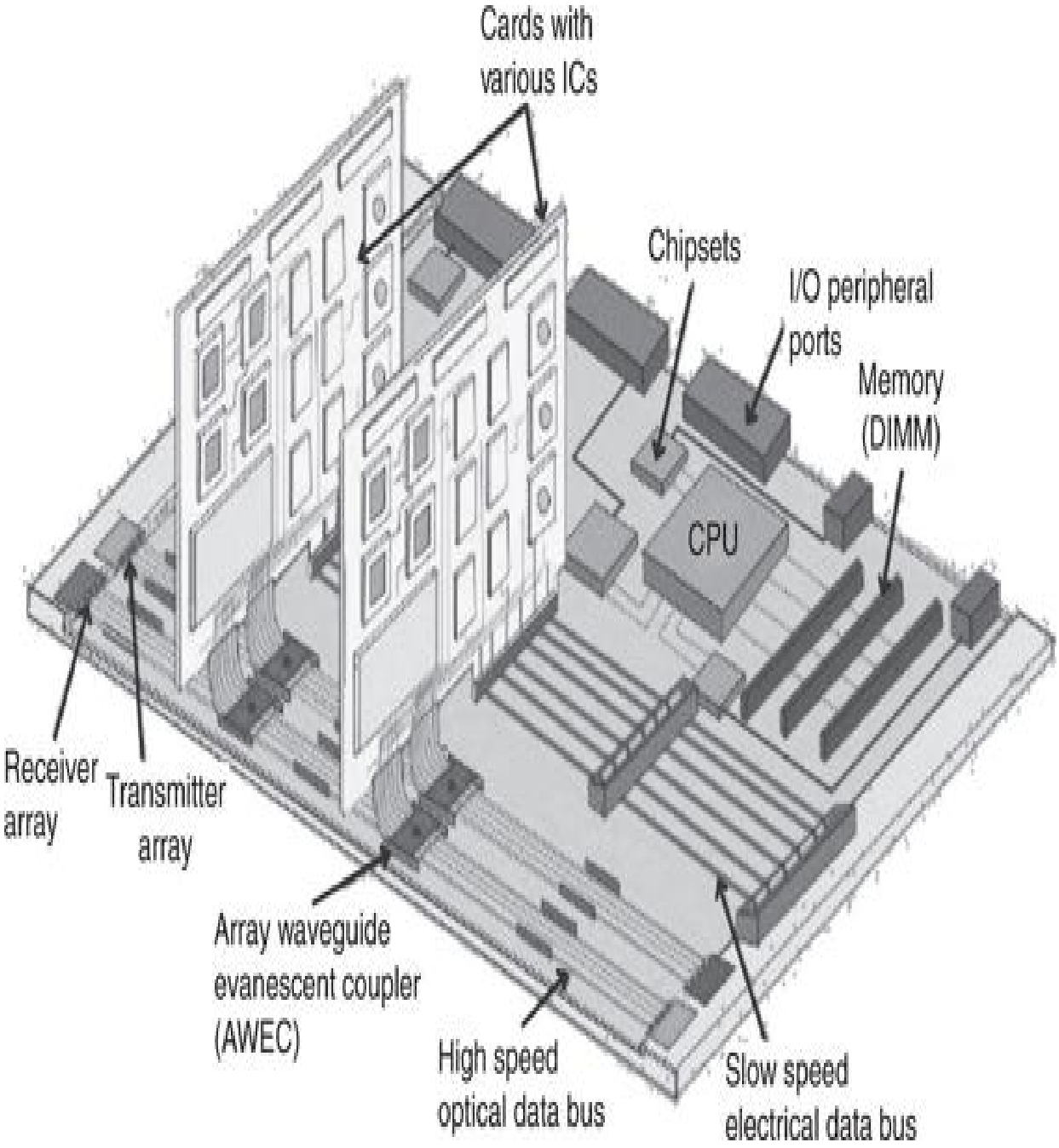


FIGURE 26.20 Board-to-board optical and electrical interconnections. (*Source: 3M.*)

Optical interconnections have major advantages over electrical signals: individual optical cables are 10× smaller than comparable high-speed shielded cables; optical bussing is 20× smaller than comparable electrical bussing; optical connectors are 7× smaller than electrical controlled

impedance cables while being 20 to 40 percent faster; and embedded optical waveguides are 8× smaller than differential striplines in PCBs. While optical bussing has many advantages, it will coexist with electrical bussing for the future as seen in Fig. 26.20.

26.4.1.1 Structures. The optical waveguide structures are shown in Fig. 26.21.[13,14,15] The transmitter package provides the multiplexed laser signal sources, through vertical cavity surface emitting laser (VCSEL) arrays into mirrors at the optical polymer waveguide level. At the receiver package, mirrors direct the laser signal up into photodiode arrays.

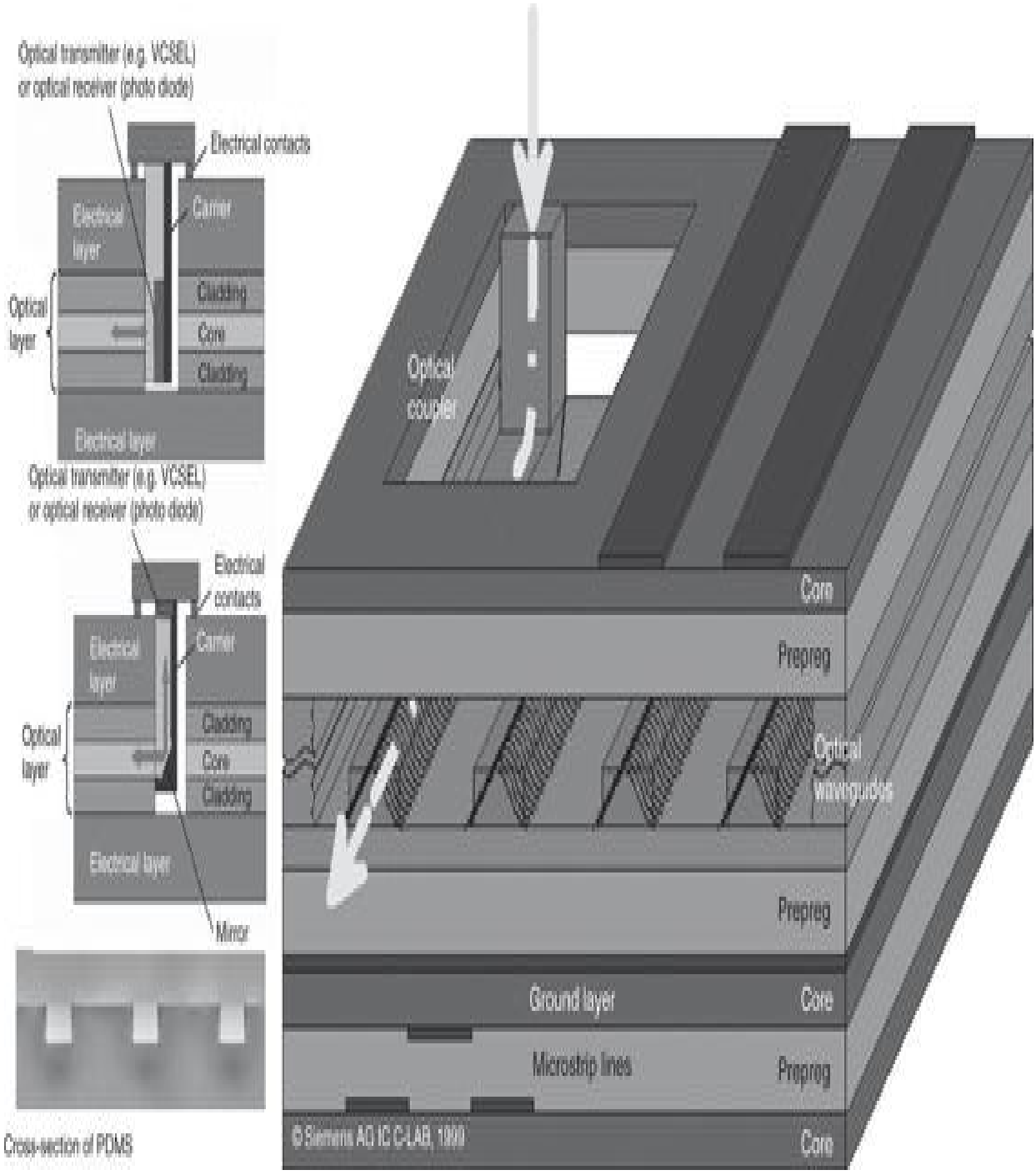


FIGURE 26.21 Structure of a printed optical waveguide. (*Courtesy of Siemens C-Lab*.)

26.4.1.2 Components. Figure 26.22[16] shows what the transmitter and receiver BGA packages will look like,

whereas Fig. 26.23[17] shows what the micro-mirrors, VCSEL, and photoreceptor sensors may look like.

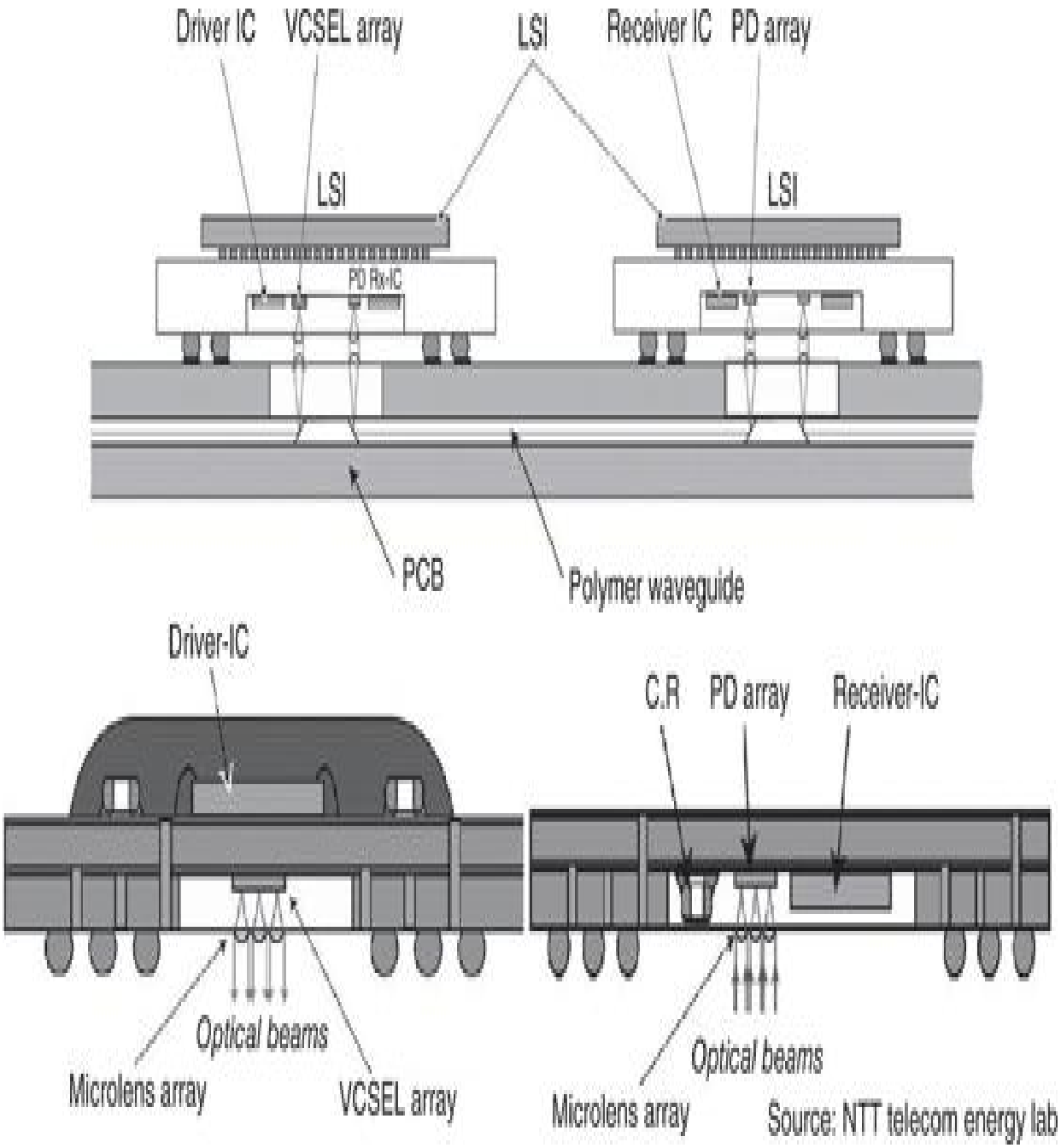
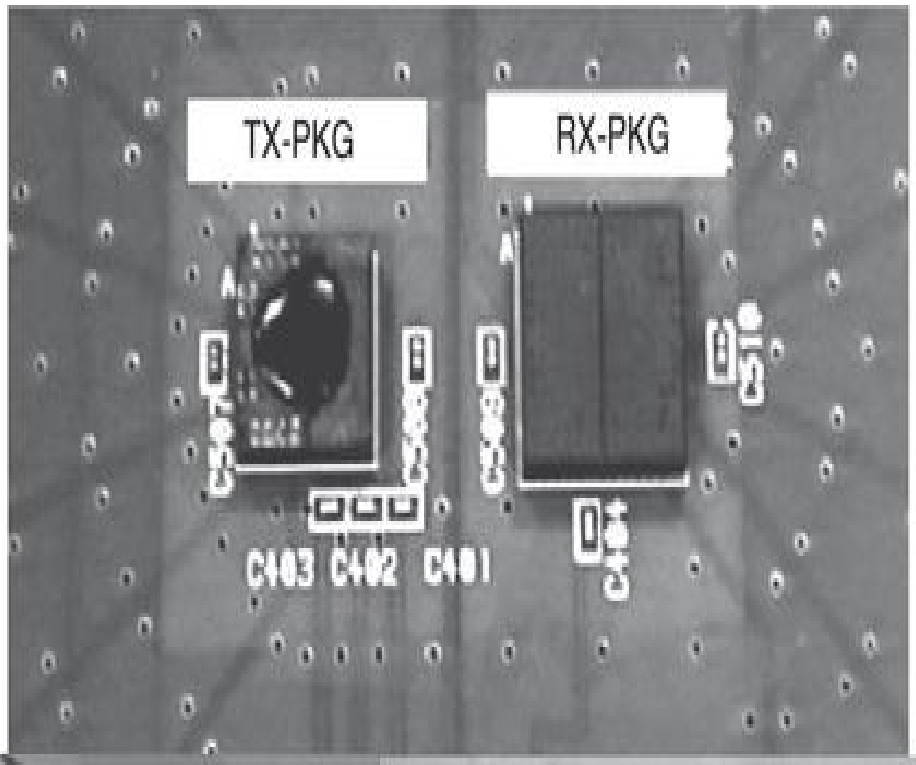
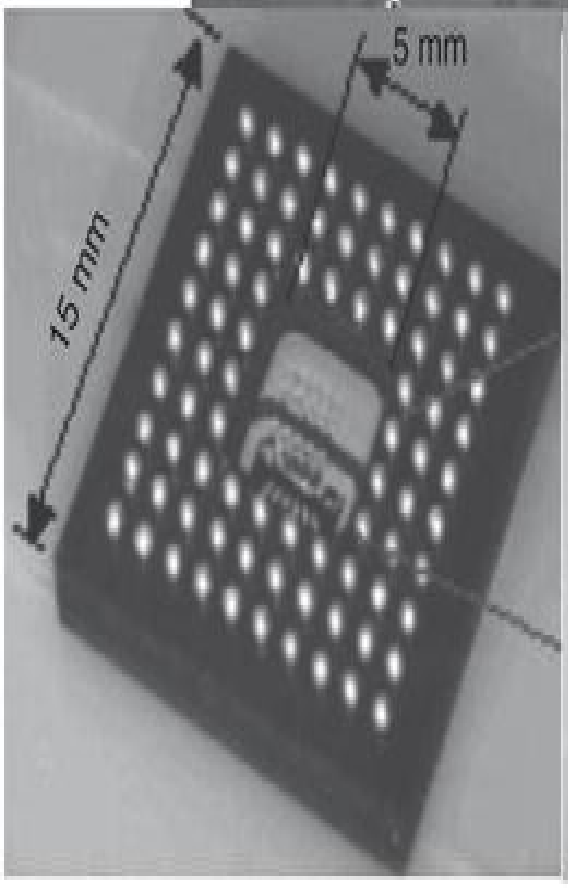
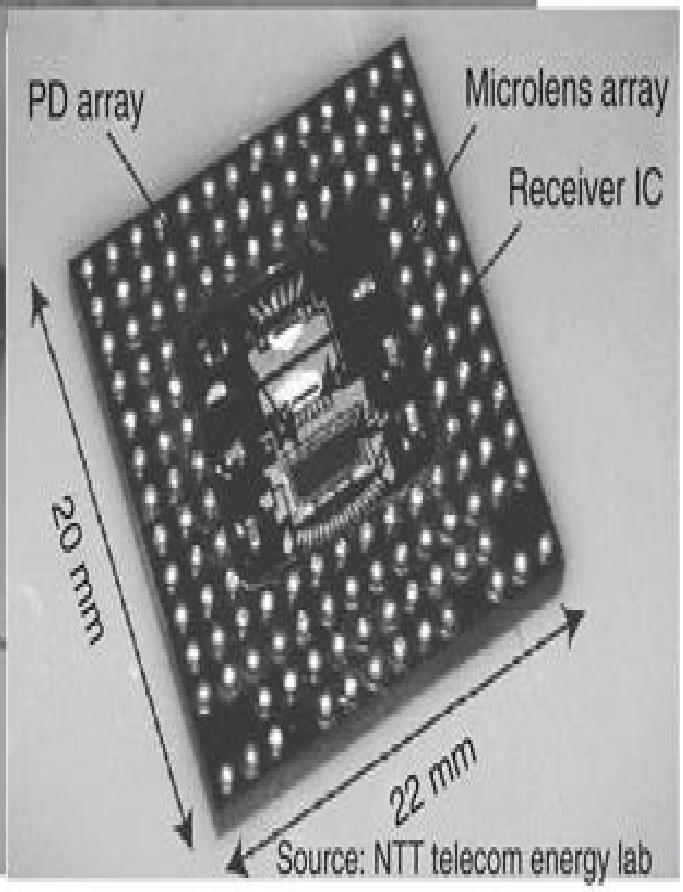


FIGURE 26.22 NTT waveguide-on-board concept with OptoBump packages. (*Courtesy of NTT-Lab*.)







Tx: 15 mm SQ., 84 pin @1.27 mm

Rx: 20 mm SQ., 134 pin @1.27 mm

FIGURE 26.23 NTT chip-to-chip optical interconnection, Tx and Rx. (*Courtesy of NTT-Lab*.)

26.4.1.3 Optical Waveguide Materials. The optical materials being considered for integrated waveguides are currently polymers. Polymers have a number of advantages:

- *Stability*. Such materials offer high thermal stability and long-term photostability. Bellcore Telecordia compliance (i.e., 1209, 1221) tested for less than 600 hr. at 85°C/85 relative humidity (RH), solder temperature >230°C, and degradation temperature >350°C.
- *Well established*. A huge body of data has been gathered over the last 100 years on polymers including all the popular photoresists.
- *Useful*. Polymers have unique properties (such as bend radius, modulators, and index tuning) that you cannot get anywhere else. These properties include unique processing options [photolithographic, reactive ion etching (RIE), direct laser writing, molding, and printing].

They also have a number of disadvantages:

- *Unstable*. Many have low thermal stability (POF below 80°C) with photodegration (laser dyes < days) and are sensitive to delamination, moisture, and chemicals.
- *Unknown*. New materials require new processes, equipment, and experience.
- *Useless*. Some polymers have losses of POF of 20 dB/km, whereas optical glass is <0.1 dB/km. The packaging cost of polymers is 80 percent of the cost in devices.

Candidate materials are acrylates, halogenated acrylates, cyclobutenes, polyimides, and polysiloxane. Table 26.3 lists many of the most popular materials. The optical losses of the polymers (dB/cm) are in the lower wavelengths near 840 nm.

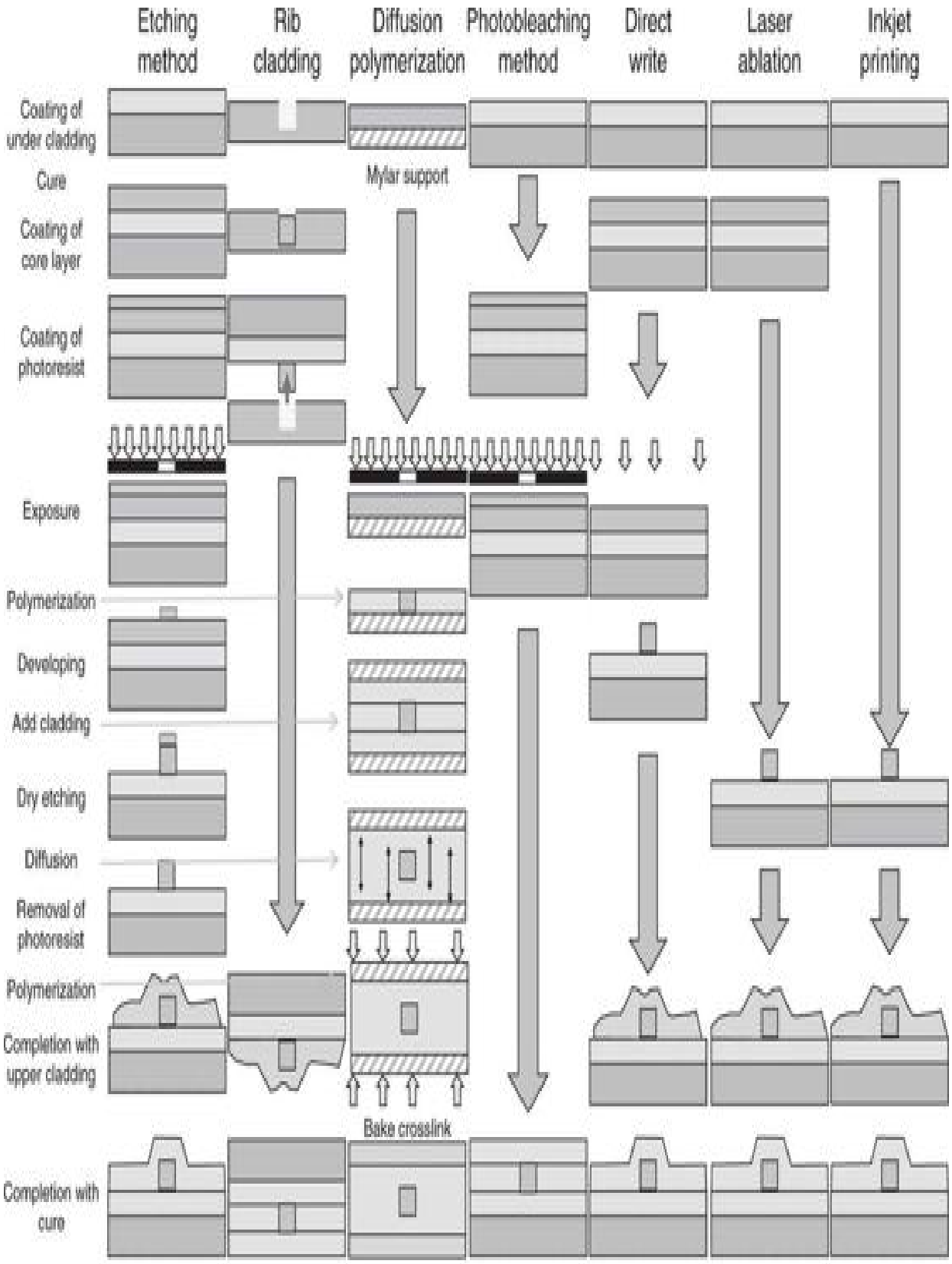
TABLE 26.3 Polymers for Optical Waveguides and Candidate Materials

			Waveguide Optical Losses (dB/cm)		
Manufacturer	Polymer Type	Patterning Techniques	840 nm	1300 nm	1550 nm
Allied Signal	Halogenated Acrylate	Lithography, RIE	0.01	0.03	0.07
	Acrylate	Laser	0.02	0.2	0.5
Amoco	Fluorinated polyimide	Lithography	–	0.4	1.0
Asahi	Epoxy-NanoSU-8-50	RIE	–	0.3	–
BF Goodrich	Polynorbornenes	RIE, Laser	0.18	–	–
Dow Chemical	Benzocyclobutene	RIE	0.8	1.5	–
	Silesquioxane	Lithography, Laser	0.031	0.05	0.5
Dow Corning	Siloxane	Lithography, Laser	0.02	0.4	–
DuPont	Teflon AF	RIE	–	0.4	–
Exxelis	Halo-Polyacrylate	Lithography, Laser	0.025	0.4	0.8
Fujitsu	Polysiloxane	RIE	0.17	0.43	–
General Electric	Polyetherimide	RIE, Laser	0.24	–	–
Hitachi/NTT	Halogenated Acrylate	RIE	0.02	0.07	1.7
ILFA/Wacker	Polydimethylsiloxane	Lithography	0.023~.027	0.3	–
JDSU/R&H	Acrylate	RIE	0.015	0.110	0.6
Nippon Paint	Polysilane film	Lithography bleaching	0.02	0.1	<1.0
Optical interLink	Acrylate Monomers	Lithography	–	0.6	–

RIE= Reactive Ion Etching

Source: Alcatel/Lucent Technologies, Loughborough University

26.4.1.4 Manufacturing Process. The manufacturing process for polymer optical waveguides is much like using a liquid photoresist. Roller coating or meniscus coating of the liquid polymer is all that is required to apply the optical polymer on a standard multilayer innerlayer. After drying, the optical polymer is exposed through standard photo masks and developed. After a final curing, they are laminated into standard multilayers with prepregs. Figure 26.24 shows the seven fabrication techniques experimented on. These are then fabricated into a standard multilayer, as seen in Fig. 26.25.[18]



Process for defining polymer optical waveguides

FIGURE 26.24 Seven processes for defining polymer optical waveguides.

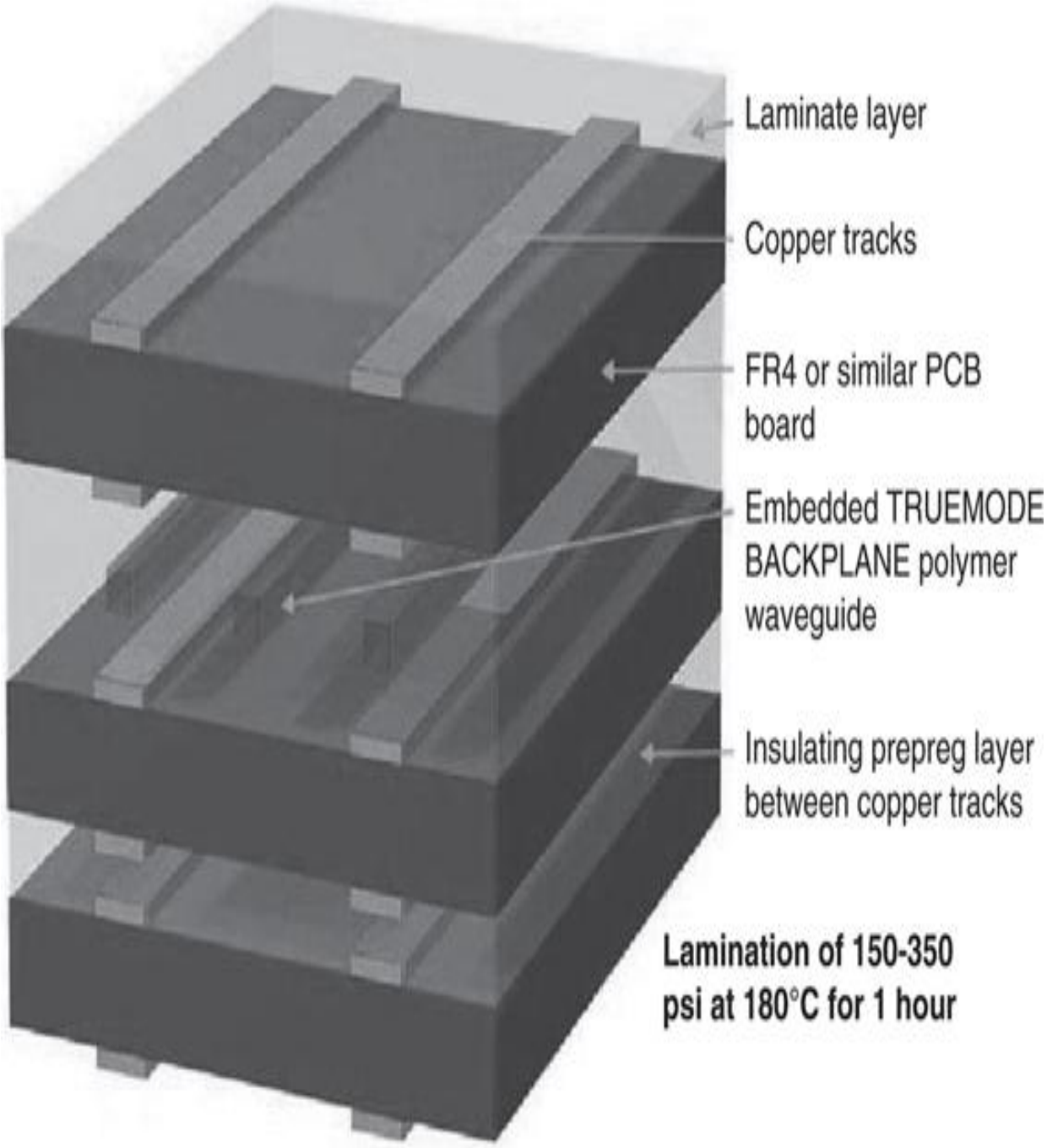


FIGURE 26.25 Optical waveguide stack-up in a conventional multilayer prior to lamination. (*Courtesy of Terahertz Corporation*.)

26.4.2 Current Research Globally Into Optical Waveguides in PCBs

Current optical waveguide research is being conducted all over the globe, with three programs of special note:

- EU's Electrical/Optical Circuit Board (EOBC) and OptoSys
- UK's Optical PCB (OPCB)
- US/DARPA/IBM Terabus Optocard

EOBC: This work is part of the German projects 'Electrical/Optical Circuit Board' and 'OptoSys,' which are supported by the German government's Department of Education and Research (BMBF) under grants 16SV802/6 and 01BP801/01. (Dortmund, Ulm and the Fraunhafer Institute for Applied Solid-State-Physics in Freiburg are participating on a suborder basis.)[19, 20, 21]

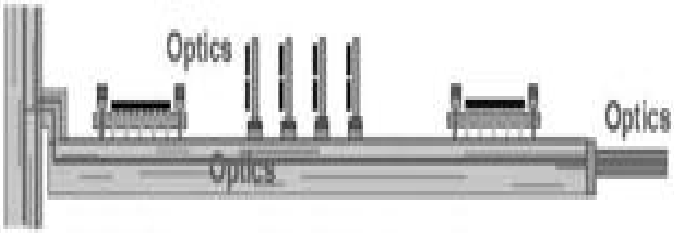
The progress in Germany is typical of that in the United Kingdom and United States, moving from the laboratory at universities to industrial companies building prototypes and the infrastructure. The EOCB (Electrical Optical Circuit Board) typified by C-Lab of Siemens in the last update is now replaced by commercial firms like VarioOptics AG of Villingen, Switzerland (spin-off of Varioprint AG of Heiden, Switzerland), and tested/qualified by Microtec GmbH laboratorie. Microtec tested and reported on the EOCB performance along with failure mechanisms and failure predictions. This provided new information for standards and pre-qualification actions.

OPCB: In the UK, a large team of university and industrial companies collaborated under EPSRC's leMRC, and OPCB: University College London, (UCL) Instigator, Principal Investigator and Technical Project Leader; the School of Engineering and Physical Sciences, Heriot-Watt University, Edinburgh; and the Wolfson School of Mechanical and Manufacturing Engineering, Loughborough University—

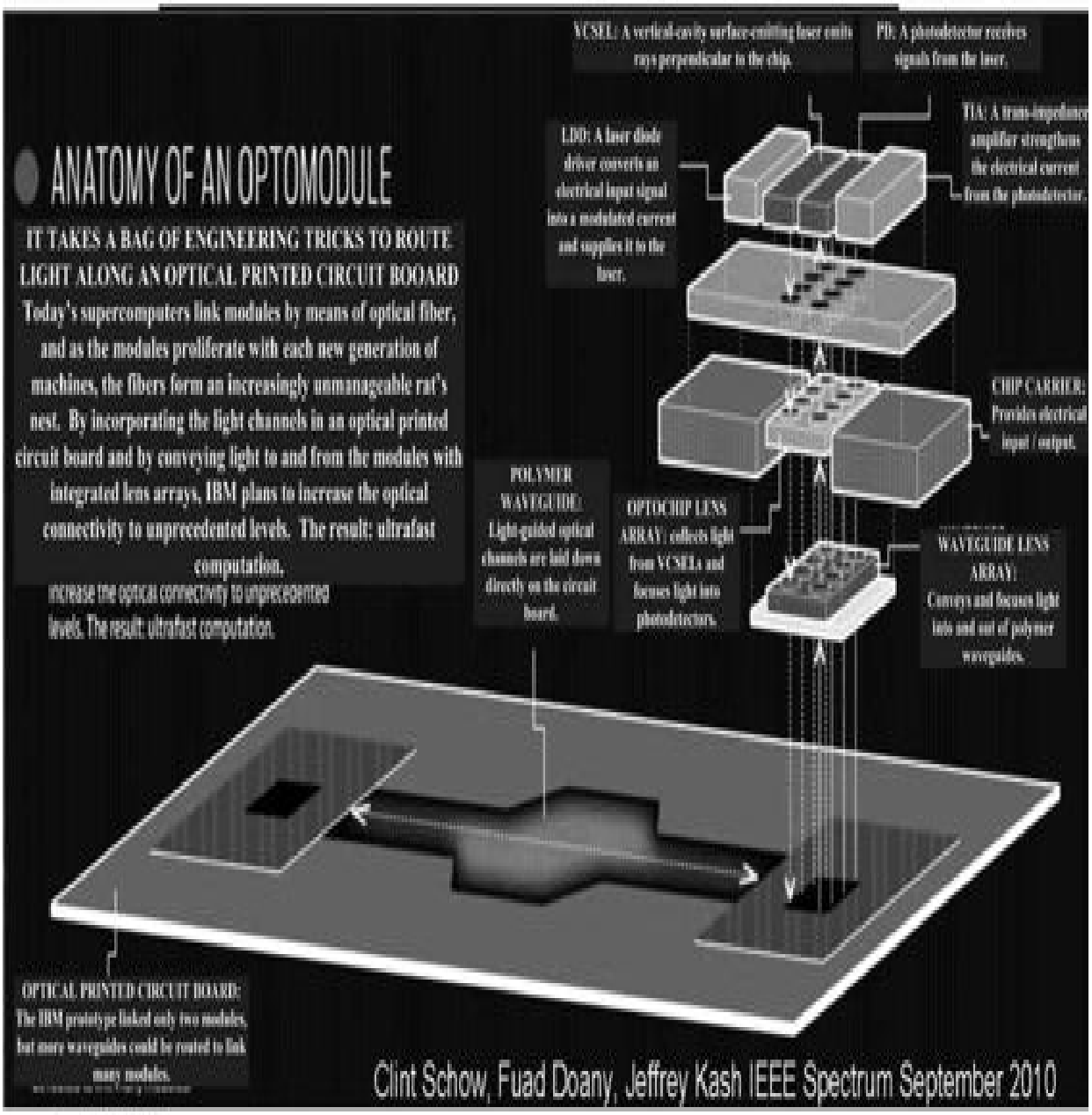
together with eight companies: Xyratex Technology (Project Manager and manufacturer of petabyte data storage systems), BAE Systems (global aerospace, security and defense company), Renishaw, Dow Corning USA (polymer supplier), Exxelis (polymer supplier), Stevenage Circuits Ltd. (PCB manufacturer), Cadence Design Systems (PCB layout software supplier) and National Physical Laboratory (national standards laboratory).[22, 23]

TERABUS: IBM Research and Agilent Corp. have invested heavily in the past 5 years in optical printed circuit board technology and connectors based on multimode polymer waveguides. This is now referred to as Optocard. This research was partially funded by the U.S. government as the Terabus Program.[24, 25, 26] IBM believes this technology will be needed to provide the bandwidth for future server generations (clouds), allowing highly integrated electrical-optical links of waveguides, flex and fiber between systems, modules, boards and chips. Their 2015 Project Milestone is seen in Fig. 26.26, the Anatomy of an Optomodule.

~2015



Optical waveguides in/on boards



- METRICS
  - Capacity: 360 Gbps
  - Reach: 0.15m
  - Energy: 6.5pj/bit
  - Density: 9 GBps/mm2
  - Cost: ?/Gbps

Source: IBM

FIGURE 26.26 The details of the optical system IBM is working on: Optochip, Optomodule, and Optocard connected by the polymer waveguides.[20]

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PART 6

FABRICATION

CHAPTER 27

CAM TOOLING FOR FAB AND ASSEMBLY

Happy T. Holden

Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

27.1 INTRODUCTION

The manufacturing of printed circuit boards (PCBs) and assemblies (PCAs) begins with the soft-tooling process. This process is the transformation of customer computer-aided design (CAD) data and specifications into the necessary tools required for manufacturing the bare PCB and populating the assembly. The typical tools required for manufacturing PCBs include artwork for photoprinting of inner conductive layers, outer conductive layers, and solder mask patterns. Artwork is also created for screen-printing patterns for nomenclature and via-plugging layers. Additional tools required include drill and routing numerical controlled (NC) programs, electrical testing netlists and fixtures, and CAD reference soft-tools.

The tooling process for assembly requires assembly drawings, bills of materials (BOM), and schematic or logic diagrams, and includes the solder-paste stencil design,

assembly array layout, and the resulting computer numeric control (CNC) programs for component placement, in-circuit test program creations, and possibly the creation of a functional test program. Many of these procedures will be covered in subsequent chapters in the Part 8 of this handbook (assembly).

During the tooling process, the customer part numbers are analyzed to determine the compatibility of the design features with the manufacturing process capabilities. Additionally, attempts to optimize the manufacturing of the product at the lowest cost are a primary goal. However, the majority of the costs have been defined before the design is transmitted to the manufacturing site by the PCB designer. An early investment in time by the PCB design team and the manufacturing tooling team can result in the most significant savings in overall product cost.

This chapter describes the PCB tooling process, as defined in Fig. 27.1, including the transfer of information, design reviews, optimization of materials, definition of BOM and routings, tool creation, and additional processes that are required.

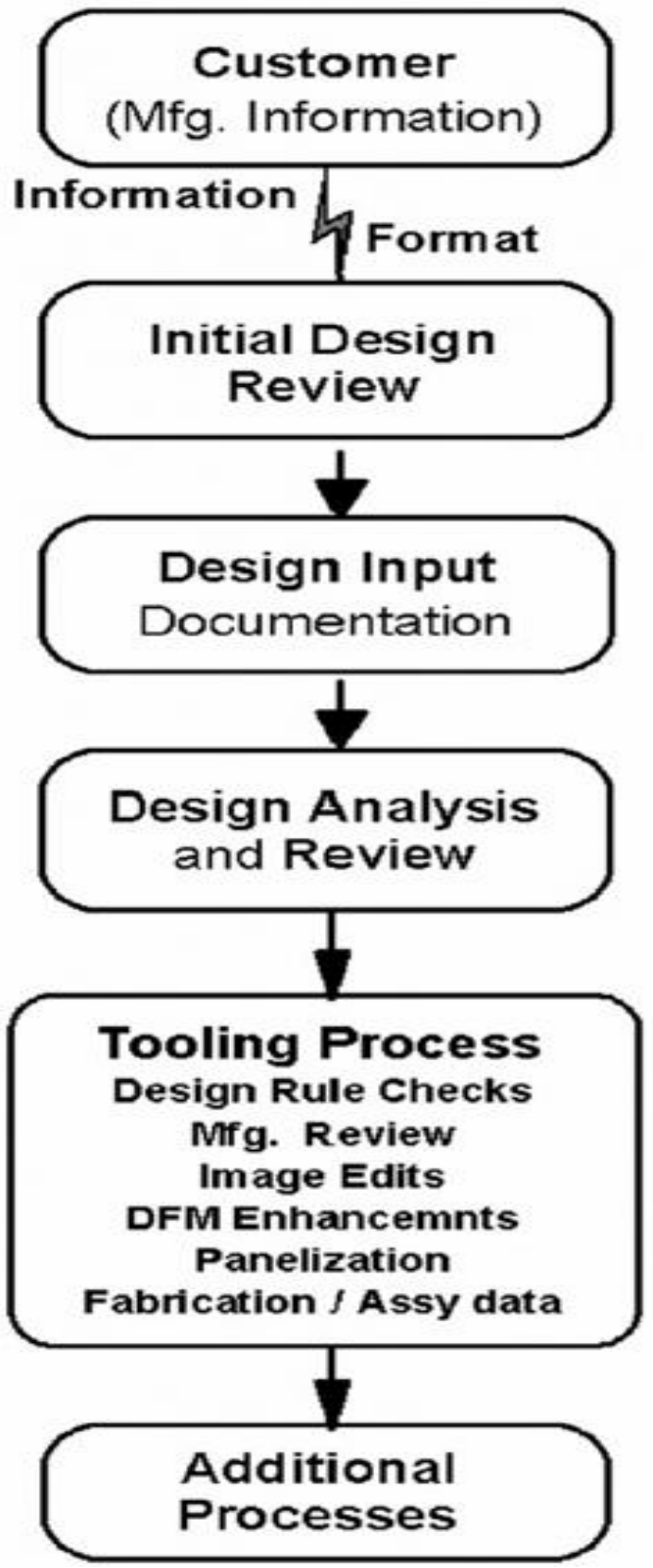

Customer
(Mfg. Information)
Information
Format
Initial Design
Review
Design Input
Documentation
Design Analysis
and Review
Tooling Process
Design Rule Checks
Mfg. Review
Image Edits
DFM Enhancemnts
Panelization
Fabrication / Assy data
Additional
Processes

FIGURE 27.1 The soft-tooling process [computer-aided manufacturing (CAM)] for PCB fabrication and assembly.

27.2 MANUFACTURING INFORMATION

The tooling process begins with the receipt of information from the customer. Unfortunately, although the time required to send information to the manufacturer has decreased to minutes or hours from day(s), a significant issue with the provision of packages to manufacturers is the completeness of the information provided. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has a new document, IPC-2610, that defines a complete documentation package, including the following:

- IPC-2611, “Generic Requirements for Electronic Product Documentation”
- IPC-2612, “Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)”
- IPC-2613, “Sectional Requirements for Assembly Documentation (Electronic Printed Board and Module Assembly Descriptions)”
- IPC-2614, “Sectional Requirements for Board Fabrication Documentation (Printed Circuit Board Description Including Embedded Passives)”
- IPC-2615, “Sectional Requirements for Dimensions and Tolerances”
- IPC-2616, “Sectional Requirements for Electrical and Mechanical Part Descriptions (Specification and Source Control Part Descriptions)”
- IPC-2617, “Sectional Requirements for Discrete Wiring Documentation (Wire Harness, Point to Point and Flexible Cable Descriptions)”

- IPC-2618, “Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, and Procurement Documents)”

Timely tooling of a part number depends on having the correct information. All features required to exist on the PCB must be defined for the manufacturer. The information is defined via design data, drawings, and textual information. Automated data are encouraged whenever possible.

27.2.1 Required Information

The information and common data formats required to permit the tooling of the PCB include the following (details are found in Sec. 5.2.1 and 5.3):

- Part number information
- Fabrication drawing
- Drill drawing
- Subpanel drawing
- Manufacturing notes
  - Board details: The type, size, and shape of the printed board, bow and twist allowances, overall board thickness requirements including tolerances, tooling hole information, special markings, and specific manufacturing processes and tolerances.
  - *Materials:* Type class and grade of materials, including color if applicable. Plating and coating material(s), type, thickness, and tolerances. Solder mask and marking inks type, minimum thickness, and permanency.
  - *Conductors:* Shape and arrangement of both conductors and nonconductor patterns, thickness, dimensions, and tolerances, including conductor width and spacing allowances.

- *Acceptability:* Location of quality conformance coupons or circuitry, control documents for acceptability, X-OUTs accepted and assembly-panel concerns.
- *Format:* Common formats for drawings are Adobe PDF, HP-GL, HP-GL-II, and Post- Script.
- Artwork data
- Aperture list files
- Drill data
- Drill tool files
- Special requirements information
- Netlist data

27.3 DESIGN ANALYSIS AND REVIEW

Design analysis and review is a refinement of the initial design review performed earlier but is the first step in the CAM (soft-tooling) process. This step focuses on the actual design data submitted for fabrication and assembly. The design analysis and review step consists of the following tasks:

- Design rule checking
- Manufacturability analysis
- Single-image edits
- DFM enhancements
- Panelization
- Fabrication parameters extraction

These tasks provide the final checking of the PCB design requirements against the capabilities of the PCB manufacturer and preparation of the design for manufacturing.

Most fabrication problems occur or are discovered during the initial tooling (CAM) phase. The following are among the causes of such problems:

- Poorly documented designs
- Improperly formatted drill files
- Use of 274-D Gerber with separate aperture tables
- Lack of proper clearance on solder mask openings
- Inadequate drill-to-copper clearance
- Misaligned layers
- Inadequate manufacturing clearances
- Lack of an IPC-D-356 netlist
- Use of positive plane layers instead of negative ones
- Minimal communication between the designer and the fabricator

The best advice for these problems is to fix them during the design phase. Consider the following precautions and considerations:

- Try not to use 274-D with separate aperture tables.
- Because there are no standards for aperture tables, the fabricator must do extra work to accommodate the tables, with increased opportunity for error.
- Use 274-X whenever possible. The apertures are embedded and files are easier for the fabricator to work with. This provides better support for special aperture shapes.
- Better yet, if possible, use “intelligent” formats like GenCAM, DirectCAM, or ODB++. These formats should enable the fabricator to better understand your design. Also, such formats have the netlist information embedded.
- Design rules can be embedded in some formats.

27.4 THE CAM-TOOLING PROCESS

27.4.1 Design Rule Checking

Design systems lay out circuits to defined rules; however, these systems may fail to adhere to these rules, because of either system failure or manual intervention. The purpose of reviewing the data package, in addition to reviewing the documented design constraints, is to confirm that the product can be produced at the manufacturing site and to the expected manufacturing yields. The analysis of the data describing the circuitry of the PCB to the manufacturing facility's production capabilities is critical to the success of the product.

Table 27.1 defines typical design rule checking that is performed, the reasons for checking, and the method of checking.

TABLE 27.1 Design Rule Checking

DRC Item	Purpose of Checking	Method of Checking
Drill layer duplicate coordinates	Duplicate drill holes consume manufacturing capacity and may result in broken drill bits.	Most PCB CAM systems have an explicit check for this problem, provided a given radius of tolerance.
Minimum drill hole-to- hole spacing	Drill holes too close together may result in broken material between the holes.	Most PCB CAM systems have an explicit feature spacing check.
NPTH-to-board edge minimum spacing	Drill holes too close to the board edge may result in broken material at the board edge.	Merge the routing profile onto a copy of the NPTH layer and execute a spacing check of the pad to trace (the route layer would appear as a trace).
Missing drill holes	Missing holes may result in nonfunctional designs or products that cannot be used due to missing mounting or tooling holes.	Check the pad registration against a circuit reference layer, and verify pads without PTH holes.
Extra drill holes	Extra drill holes could result in nonfunctional designs due to cutting of traces or shorts (if the holes become plated).	Check the pad registration against a circuit reference layer, and verify PTH holes without pads.
Board edge-to-board edge minimum spacing	Routing cuts leaving minimal material may result in fractured or broken material between routing.	Check the feature spacing of the routing layer as a design layer, without considering electrical connectivity.
Copper-to-board edge minimum spacing	Tolerances of the routing operation may result in copper exposed at the edges of the product.	Check the feature spacing of the routing layer as a design layer against the circuitry layer.
Minimum annular ring	Most customer specifications define the minimum acceptable annular ring on PCB products. Annular ring is dependent on the design and the registration tolerances of the manufacturing processes.	Most PCB CAM systems have an explicit annular ring check.

Minimum pad-to-pad spacing	In addition to feature spacing and potential shorts, pad spacing affects the capability to test products electrically.	Most PCB CAM systems have an explicit feature-to-feature spacing check.
Minimum pad-to-track spacing	Feature spacing below manufacturing capabilities could result in shorts and poor product yields.	Most PCB CAM systems have an explicit feature-to-feature spacing check.
Minimum track-to-track spacing	Feature spacing below manufacturing capabilities could result in shorts and poor product yields.	Most PCB CAM systems have an explicit feature-to-feature spacing check.
Copper-to-NPTH minimum spacing	NPTH locations too close together may prevent proper tenting of holes and require secondary drilling operations. NPTH too close together may result in damaged features (e.g., cut traces).	Check the feature minimum spacing against a copy of the design layer merged with the NPTH layers.
Minimum line width	Line widths below manufacturing capabilities could result in poor product yields.	Some PCB CAM systems have an explicit check for this problem; others may require review of the apertures used and highlighting of the apertures for visual inspection.
Track termination without pad	Although this may be the design's intent, missing pads may be the result of poor design information or loading failures. These problems can result in nonfunctional designs.	Most PCB CAM systems have an explicit check for this problem.
Padstack alignment	Misaligned padstacks may result in unpredictable annular ring results, incorrect compensations of registration, and product scrap.	Most PCB CAM systems have an explicit pad registration check.
Minimum solder mask pad clearance	Solder mask pad clearances below manufacturing capabilities could result in solder mask on the pads and poor product yields.	Check the solder mask layer (as a circuit layer) against the circuitry layer using an annular ring check.

Minimum solder mask edge-to-feature spacing	Solder mask edge to feature spacing below manufacturing capabilities could result in exposed features and poor product yields.	Check the feature minimum spacing against a copy of the design layer merged with the solder mask layer.
Minimum solder mask annular ring for NPTH	NPTH solder mask clearances may need to be larger to prevent ghosting of the solder mask from light diffraction through the product mask.	Check the solder mask layer (as a circuit layer) against the NPTH layer, and verify that there are no matches of the NPTH to the solder mask layer.
Solder-mask-to-board edge minimum clearance	PCB edge clearances may need to be larger to prevent ghosting of the solder mask from light diffraction through the product.	Check the feature minimum spacing against a negative copy of the solder mask layer merged with the routing layer.
Solder mask minimum web	Solder mask webs below manufacturing capabilities could result in solder mask breakdown and poor product yields. This problem could result in a PCB assembler with solder bridging defects.	Use minimum feature-to-feature spacing on the solder mask layer.
Plane-to-board-edge minimum clearance	Spacing below the tolerances of the routing operation may result in exposure of copper at the edges of the product.	Check the feature spacing of the routing layer as a design layer against the plane.
Minimum plane layer annular ring	An annular ring below manufacturing registration and tolerance capabilities could result in open connections and poor product yields.	Most PCB CAM systems have an explicit annular ring check.
Minimum plane layer clearance	Plane clearances below manufacturing registration and tolerance capabilities could result in shorts and poor product yields	Most PCB CAM systems have an explicit annular ring check.

Plane-to-plane isolation	Plane layer isolation typically results from either incorrect designs or interpretation of aperture lists; the result is a nonfunctional product.	Most PCB CAM systems have an explicit layer-to-layer isolation check.
Nomenclature-to-NPTH minimum spacing	Nomenclature spacing below manufacturing capabilities may result in nomenclature in the hole, due to misregistration or bleeding of the nomenclature ink.	Check the feature minimum spacing against a copy of the nomenclature layer merged with the NPTH layers.
Nomenclature-to-solder mask minimum spacing	Nomenclature spacing below manufacturing capabilities may result in nomenclature on product features, due to misregistration or bleeding of the nomenclature ink.	Check the feature minimum spacing against a copy of the nomenclature layer merged with each solder mask layer.
Nomenclature-to-feature minimum spacing	Nomenclature spacing below manufacturing capabilities may result in nomenclature on product features, due to misregistration, bleeding of the nomenclature ink, or skipping of the screen over features, resulting in illegible markings.	Check the feature minimum spacing against a copy of the design layer merged with the nomenclature layer.
Nomenclature minimum feature sizes	Nomenclature sizes below manufacturing capabilities could result in illegible nomenclature and poor product yields.	Some PCB CAM systems have an explicit check for minimum line width; others may require review of the apertures used and highlighting of the apertures for visual inspection

27.4.2 Manufacturability Review

The design rule checking results are reviewed against the PCB manufacturing capability matrix, with dispositions being made

to the acceptability of violations. The PCB customer may be contacted regarding design violations, to correct and retransmit the design or to permit design changes to be performed by the PCB manufacturer.

Additionally, the factors reviewed during the initial design review are revisited to confirm the results based on design actuals. If differences are noted, product yields and/or cost predictions may need to be altered. During this step of tooling, several concerns are uppermost in the fabricator's mind: Does the board meet the intent of the design? Can it be built? Will it function as planned? Does it pass a master rule set? Can it be improved, that is, be made cheaper or better? Is there component interconnectivity? Does the IPC-D-356 netlist show any shorted nets or broken nets? Were any multiple plane ties not happening? Did a design work-around fool the system—or allow intentional errors to slip through?

27.4.2.1 Bare-Board Analysis. Several physical artwork problems are not discovered by design rule checking and are not strictly speaking the result of design rule violations. Nonetheless, these problems can affect the manufacturability of a board and its yield. Table 27.2 describes some of these issues.

TABLE 27.2 Physical Artwork Issues

Physical Artwork Issue	Description of Issue	Illustration
Acid traps (photo-resist slivers)	Small pieces of photo-resist that have minimum adhesion and can break off, resulting in plating or redeposits	Figure 27.2*a*
Pin holes	Small openings in planes or pours that can result in loss of adhesion	Figure 27.2*b*
Copper slivers	Small features that may lose adhesion and break off	Figure. 27.2*c*
Starved/isolated thermals	Copper legs for thermals that are cut off from the rest of the plane	Figure 27.2*d*
Soldermask(S/M) slivers (web)	Small S/M features too tiny to image and adhere properly	Figure 27.2*e*
S/M to trace spacing	Small spacings that create S/M slivers	Figure 27.2*f*
S/M coverage	Features left open that could result in solder bridging	Figure 27.2*g*
Solder bridging	Small gaps between soldered features without S/M that could bridge solder	Figure 27.2*h*
Legend on pads	Silkscreen or legend on surface mount technology (SMT) lands	Figure 27.2*i*

Figure 27.2 shows examples of many of these problems. Most modern CAM-tooling systems can correct these manufacturability issues. Thus the manufacturing notes on the fabrication drawings should acknowledge this and allow for the fabricator to implement corrections. Other, less frequent, artwork errors discovered include

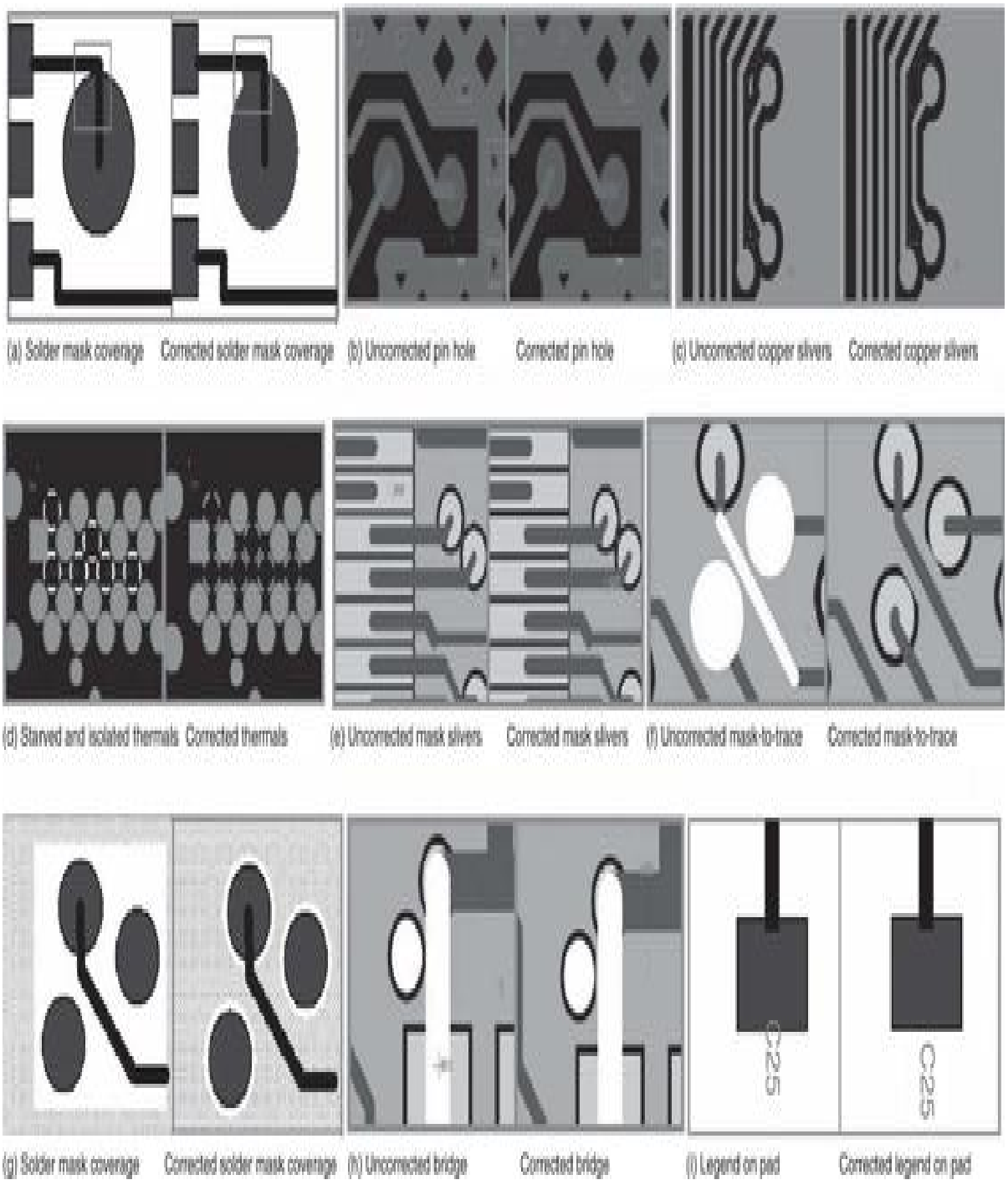


FIGURE 27.2 Typical producibility problems created in design (physical artwork).

- Signal integrity and performance issues
- Verification of last-minute changes [life savers and engineering change orders (ECO)]
- “Made in XX” and revision controls

27.4.2.2 Printed Circuit Assembly. In a similar situation, assembly tooling requires the checks and analysis of supplied BOM, machine files, and artwork for the assembly process. These actions are specifically designed to locate potential manufacturability problems during board assembly and to collect design statistical data for quoting, planning, and allocating resources. Each action covers a specific aspect of board assembly, including component location, fiducial coverage, and testability issues. These include but are not limited to the following:

Fiducial analysis: SMT component placement needs to align the machine to the individual board. By analyzing global and fine-pitch fiducials, you can identify and correct potential problems. Table 27.3, col. A, shows the checklist of a typical analysis.

TABLE 27.3 Checklist of Various Assembly and Test Analyses That Need to Be Performed in Tooling

A. Fiducial Analysis	B. Component Analysis	C. Padstack Analysis	D.Testpoint Analysis	E.Solder Paste Analysis
Global fiducial summary	Comp. max height	Toeprint to toeprint	Toeprint testpoints	Solder paste not on SMD pad
Local fiducial summary	Comp. pitch	Extra solder mask web	Via testpoints	SMD pad without solder paste
Non uniform local fiducial	Comp. rotation	No solder mask web	Other testpoints	Solder paste outside copper
Fiducial to copper	Comp. length Min	Special toeprints	Testpoint to rout	Solder paste not exposed by solder mask
Fiducial to hole	Comp. length max	Via to via center	Testpoint to NPTH	Solder paste to solder mask
Close fiducials	Comp. Spacing	Via to via edge	Testpoint to testpoint	Toe distance min (rect. pins)
Far fiducials	Comp. to toeprint	Via in SMD	Testpoint to toeprint	Heel distance min (rect. pins)
Fiducial to like pad	Rout spacing	Via to toeprint	Testpoint to capped via	Left Distance min (rect. pins)
Fiducial close to rout	Carrier wall spacing	No thieving pad	Testpoint wrong shape	Right distance min (rect. pins)

Fiducial far from rout	PTH to carrier wall	Toeprint to plane	Testpoint to THMT toeprint	Toe distance max (rect. pins)
Fiducial to background	NPTH to carrier wall	Toeprint annular ring	Testpoint to tooling hole	Heel distance max (rect. pins)
Fiducial to solder mask	Via to carrier wall	Toeprint SM clearance	Testpoint to uncapped via	Left distance max (rect. pins)
Fiducial to solder paste	Label to component	Toeprint to rout	Testpoint to exposed copper	Right distance max (rect. pins)
Fiducials to silk screen	Assembled board thickness	Hole in SMD	Testpoint to unexposed copper	Pin area/pad area min
Fiducial to conveyed edge	Comp. touch silkscreen	Flow solder orientation	Testpoint under component	Large pin area/pad area min
Component center fiducial	Component to conveyed edge	Gold fingers to capped via	Testpoint to component	Pin area/pad area max
Component covers fiducial	SMT component to conveyed edge	Gold fingers to thru TP	Testpoint to component angle	Large pin area/pad area max
Component local fiducial	Other side area keepout	Gold fingers to surface TP	Testpoint to solder mask	Pin width/pad pitch
Component global fiducial	Other Side pins keepout	Gold Fingers to uncapped via	Capped testpoint vias	Pin Pitch/pad pitch
Course-pitch component global fiducial	Comp. to gold fingers	Shadowing of inline components	Nets with one testpoint	Direct connection to plane
Fine-pitch component global fiducial	Component to tooling hole	Shadowing of staggered components	Nets without testpoints	No clearance in plane

Component to mounting hole

Hole under component

Uncapped via under component

No orientation indication

Component uncommon orientation

Wrong orientation indication

No square pad on THMT pin #1

Chip edge protection missing

Chip corner protection missing

Comp. outside keep-in area

Comp. within keep-out area

Comp. exceed max height

Comp. under min height

Component to exposed via

Trace under component

Toeprint to V-cut rout

Toeprint to conveyed edge

Toeprint to conveyed edge

Toeprint to conveyed edge

Toeprint to break tab rout

Exposed Via to exposed toeprint

Irregular exposed toeprint

Via to toeprint masked trace

Testpoints/via Clusters

Nonuniform SMD pads size

Nets with multiple testpoints

Via capped on both sides

Uncapped nontestpoint vias

Testpoint to conveyed edge

Testpoints outside keep-in area

Testpoint to silkscreen

Testpoints within keep-out area

Nets with missing testpoints

Nets with necessary testpoints

Nets with extra testpoints

Net testpoint summary

Net testpoint count report

ET pin without PTH

MP pin on PTH

Edge to edge

Missing hole

Extra holes

Pin too large

Pin too small

Pin touching

No pad for pin

Multiple pads for pin

Pin center to pad heel

Pin center to pad toe min

Pin center to pad heel min

Pin center to pad toe max

Pin diameter vs. hole diameter

Comp. to reference designator	Large pin right distance max (rect. pins)
Comp. without reference designator	Large pin toe distance vs. heel distance (rect. pins)
Misplaced reference designator	Large pin left distance vs. right distance (rect. pins)
Wave solder component orientation	Pin diameter/pad diameter min (%)
Component relative orientation	Pin diameter/pad diameter min (abs)
	Large pin diameter/pad diameter min (%)
	Large pin diameter/pad diameter min (abs)
	Pin diameter/pad diameter max (%)
	Pin diameter/pad diameter max (abs)
	Large pin diameter/pad diameter max (%)
	Large pin diameter/pad diameter max (abs)
	Max pin width/pad width min (%) (rect. pins)

(*Source:* Valor Computerized Systems.)

Component analysis: SMT components can have a multitude of missing, incorrect, or incomplete characteristics or properties. Component analysis looks for these potential problems, such as one component extending under another component. Table 27.3, col. B, provides a typical checklist for such an analysis.

Padstack analysis: SMT components have critical toeprints (TPs) and need to be checked with respect to vias, planes, solder mask, fabrication edges, and gold fingers. Table 27.3, col. C, shows a checklist for a typical analysis.

Testpoint analysis: SMT components need to be tested by in-circuit test (ICT). These analysis check testpoints to vias, surface features, tooling holes, and electrical nets. See Table 27.3, col. D, for a typical checklist for testpoint analysis.

Solder paste analysis: SMT components have to be soldered correctly. This is the second most important aspect of assembly, just behind placing the right part in the right place. Many checks are necessary to ensure manufacturability, as seen in Table 27.3, col. E.

The benefits of performing a comprehensive and thorough assembly analysis include the following:

- Estimation of cost can be derived from the results of the analysis.
- Manufacturing defects can be identified and corrected prior to construction on the assembly line.
- Such analysis can help detect potential problems so that any necessary reworking can be implemented early in the design process. Each analysis category is governed by a set of engineering reference file (ERF) values, usually unique to each production facility, thereby supporting full job portability between different assembly sites.
- The design rule checking results are reviewed against the PCB or assembly manufacturing capability matrix, with dispositions being made to the acceptability of violations.

The PCB and assembly customer may be contacted regarding design violations; the designer may need to send corrected designs or to allow design changes to be performed by the PCB manufacturer or assembler.

- Additionally, the factors reviewed during the initial design review are revisited to confirm the results based on design actuals. If differences are noted, product yields and/or cost predictions may need to be altered.
- When issues are addressed during the fabrication or assembly stage, the design database may not get updated to reflect vital changes, thus compromising the integrity of the design. If the design is respun in the future, this issue might be overlooked, resulting in scrap, or worse, faulty boards.

27.4.3 Single-Image Edits

Almost all designs include information that must be removed before they can be manufactured. Most of these items of information are used as references during the PCB layout phase to assist the designer in understanding the available real estate. However, these references must be removed or modified in order to manufacture the board to design intent. Among these typical items are the following:

Item	Impact if not removed/modified
NPTH pads on outerlayers	Plated holes
Routing crop marks	Copper at board edge
Direct contact plane markings of drilled holes	Open circuits
Clip nomenclature with solder mask data	Nomenclature on pads or in holes
Scaling and compensation	Finished traces or geometries that are the wrong size

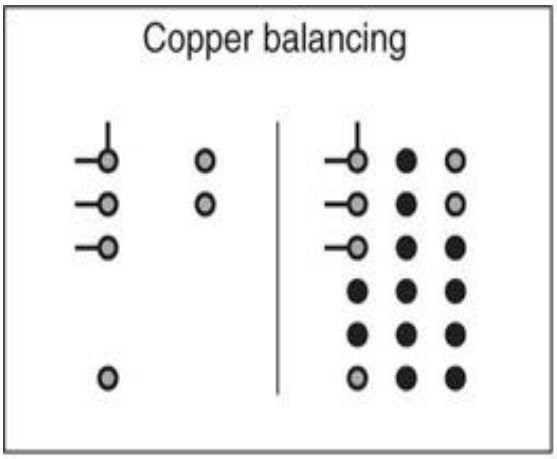
27.4.4 DFM Enhancements

The manufacturability of the PCB can be improved through design enhancements. Many of the enhancements can be performed on CAD systems (or through specialized post-CAD software); other enhancements can be performed at the manufacturing site.

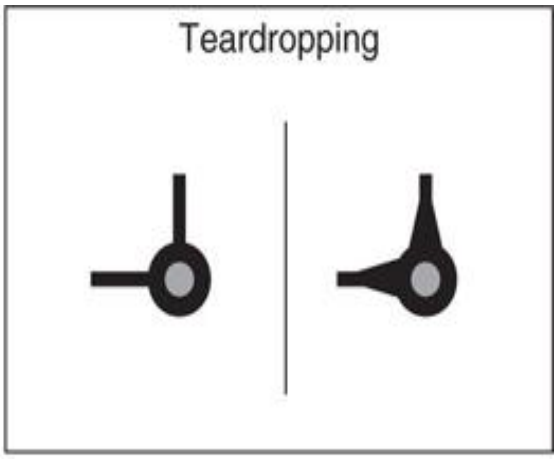
Ideally, all design enhancements would be performed at the design site to maintain the consistency of products from multiple manufacturers; however, some of the DFM enhancements can impact the CAD system's capability to provide further design changes. Specifically, the optimization of track-to-feature spacing could result in blocked routing channels, preventing an autorouter from performing. The following are typical DFM enhancements (see Fig. 27.3):

Item	Result from enhancement
Copper balancing	The balancing of copper on the surface of the design will improve the distribution of plating (in the pattern-plating process), preventing areas of overplating due to the isolation of features. This improvement enables the manufacturer to control the plated hole diameters to tolerances and reduce plating heights, which impact solder mask coverage. (See Fig. 27.3*a*.)
Teardropping	As annular rings decrease due to tighter design specifications, the probability of defects occurring due to registration/annular ring failures increases. The addition of teardropping increases the pad-to-trace junction size, improving the reliability of the connection and improving product yields. (See Fig. 27.3*b*.)
Removal of nonfunctional pads on innerlayers	Innerlayer shorts result from several factors, among them the proximity of circuitry to other circuitry.

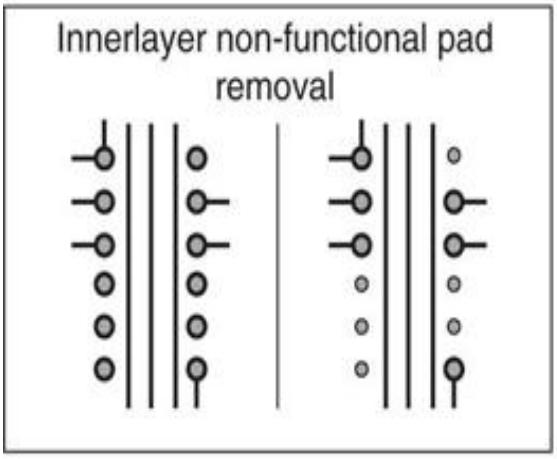
	The occurrence of shorts can be correlated to the running length of the circuitry versus the running length at some minimum spacing between circuitry (at the process capability of the operation). Reducing the total distance at minimum spacing will reduce the probability of shorts, resulting in improved yields. (See Fig. 27.3*c*.)
Optimization of track-to-feature spacing	As described in the nonfunctional pads discussion, the occurrence of shorts can be correlated to the running length of the circuitry versus the running length at some minimum spacing between circuitry (at the process capability of the operation). Reducing the total distance at minimum spacing will reduce the probability of shorts, resulting in improved yields. (See Fig. 27.3*d*.)
Track width optimization	The occurrence of opens can be correlated to the running length of the circuitry versus the running length at minimum track width (at the process capability of the operation). Reducing the total distance at minimum track width will reduce the probability of opens, resulting in improved yields. (See Fig. 27.3*e*.)



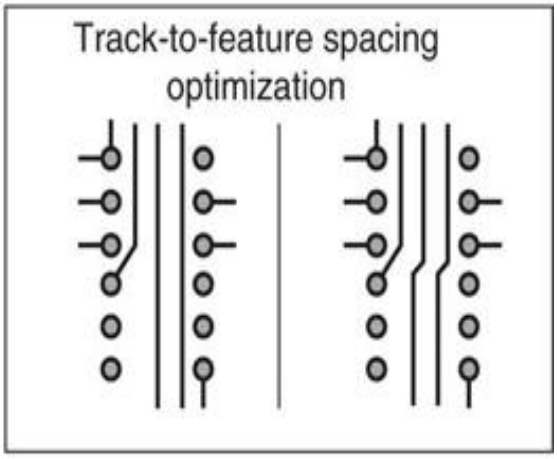
(a)



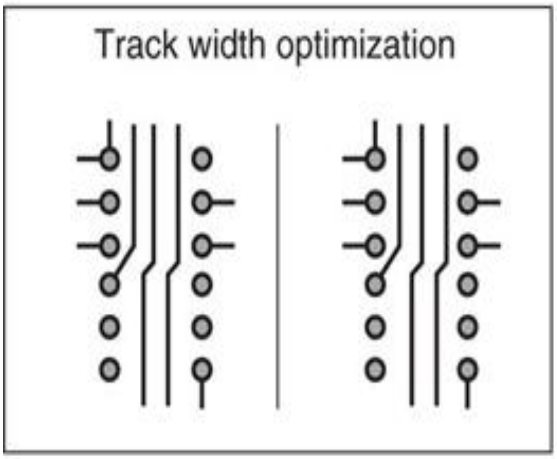
(b)



(c)



(d)



(e)

FIGURE 27.3 Typical producibility problems created in design.

27.4.5 Panelization

In the panelization process, the PCB single images are placed in the locations defined in the panelization definition step of the initial design review. In addition, the following features may be added to the panel for manufacturing:

Item	Purpose
Customer coupons	These coupons are provided to the customers for their inspection of the PCB product. These coupons are typically treated as separate PCB single images.
Internal coupons	During the manufacturing process, destructive testing may be required to confirm product quality. These coupons are typically treated as separate PCB single images.
Tooling holes	Holes used for registration of manufacturing panels to artwork, drilling, or routing operations are added to the panel borders.
Outerlayer thieving patterns	Plating thieving patterns are sometimes needed to balance the platable area across the panel.
Innerlayer venting patterns	The addition of copper to innerlayers outside the PCB single image provides more consistency in the lamination process.
Textual markings	Operator aides may be provided outside the PCB single image to improve manufacturing quality.

27.4.6 Fabrication and Assembly Parameter Extraction

Additional manufacturing information must be extracted or calculated from the design file before fabrication or assembly can begin. This information is loaded and stored in several files and databases used to run various fabrication and assembly equipment. In addition to requiring the basic tooling steps already defined, most PCB manufacturing sites also require the designer to provide the following information:

- Raw materials shearing and labeling instructions
- Copper foil thicknesses and etch rates
- Automatic optical inspection files
- Lamination lay-up BOM and order/stack height
- Lamination press cycles, heat input, and pressure settings
- Drill-file location and revision levels
- Plating area calculations and current density settings
- Copper foil thicknesses and etch rates
- Router-file location and revision levels
- Electrical test programs
- Quality control procedures and coupon disposition
- Final packing and shipping instructions

27.4.6.1 AOI Files. The CAD reference files, if required, are generally created at the PCB manufacturing site. These files prepare automated optical inspection (AOI) systems with data that confirm that manufactured pieces match, within tolerances, the PCB design.

27.4.6.2 Lamination Parameters. Each multilayer stack-up and material may require specific lamination processes. Modern multilayer presses have microprocessor-controlled time, temperature, and pressure. These parameters require selection in the tooling process.

27.4.6.3 Drill Files. Drill files and the respective drill bit tools must be archived and available for download to the appropriate drilling machine when production needs them. Drill

bit preparation precedes the actual drilling operation in order to create the drill cassette.

27.4.6.4 Plating Coefficients. Plating requires specific direct currents (DC) to be applied to this part. The current density of the appropriate plating bath is multiplied by the plated area on each production rack. After the first actual run, direct measurement of the plated metals is used to adjust the plated area to achieve the correct thicknesses.

27.4.6.5 Routing Files. Router files and the respective router cutting tools have to be archived and available for download to the appropriate routing machine when production needs them. Router tool preparation precedes the actual routing or secondary drilling operation in order to create the final fabrication cassette.

27.4.6.6 Electrical Test Programs and Fixture Creation. An electrical test netlist file may be either created internally from the artwork or prepared from a supplied IPC-D-356 file. This test file has to be compared to the netlist extracted from the artwork supplied. Any difference must be resolved before the actual electrical test file is finalized. In addition, the electrical test fixture must be constructed or sent to an outside contractor to prepare.

27.4.6.7 CAD to Assembly Processes. The assembly tooling operations include CAD interfacing to component data and BOM. These operations include the generation of manufacturing documentation (see Fig. 27.4) and assembly engineering for component machine management, program optimization, and line balancing (see Fig. 27.5).

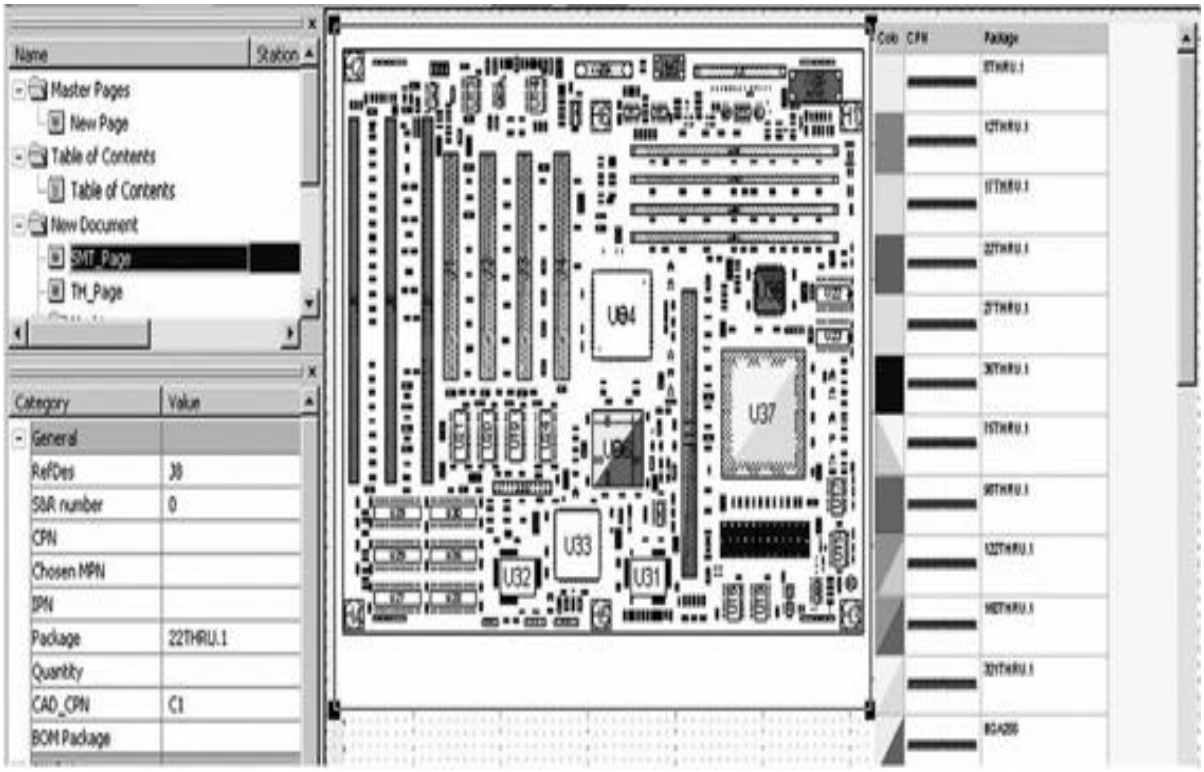


FIGURE 27.4 Assembly manufacturing documentation and instructions creation.

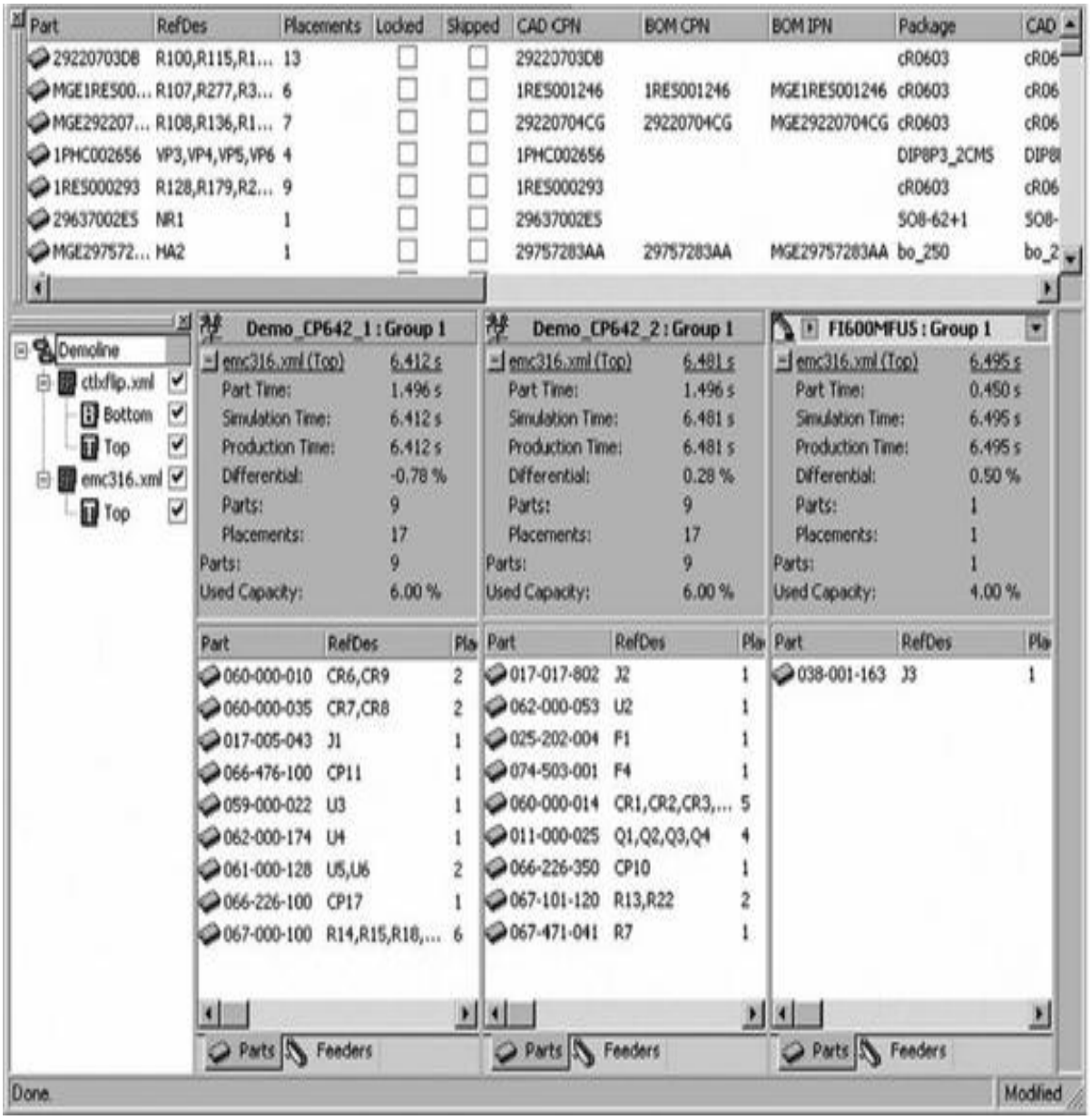


FIGURE 27.5 An assembly BOM control optimizing mixed vendors lines with line balancing.

27.5 ADDITIONAL PROCESSES

Because of variations in the PCB manufacturing process, additional CAM-tooling operations may be required. Variations in manufacturing that may call for additional tooling include the following:

- Rivet lamination versus pin lamination
- Laser drilling
- Multiple panel sizes
- Very large lamination presses (48 × 48 in)
- A very high degree of automation

New processes or PCB product features that may require additional tooling processes include the following:

- Embedded passives
- Embedded waveguides

Embedded passives and embedded waveguides are complicated to implement in production. Alignment and overlap are critical. Proper scaling for the particular embedded materials is especially important, depending on whether the materials are additive or subtractive. Figure 27.6 shows some of the critical tooling dimensions.

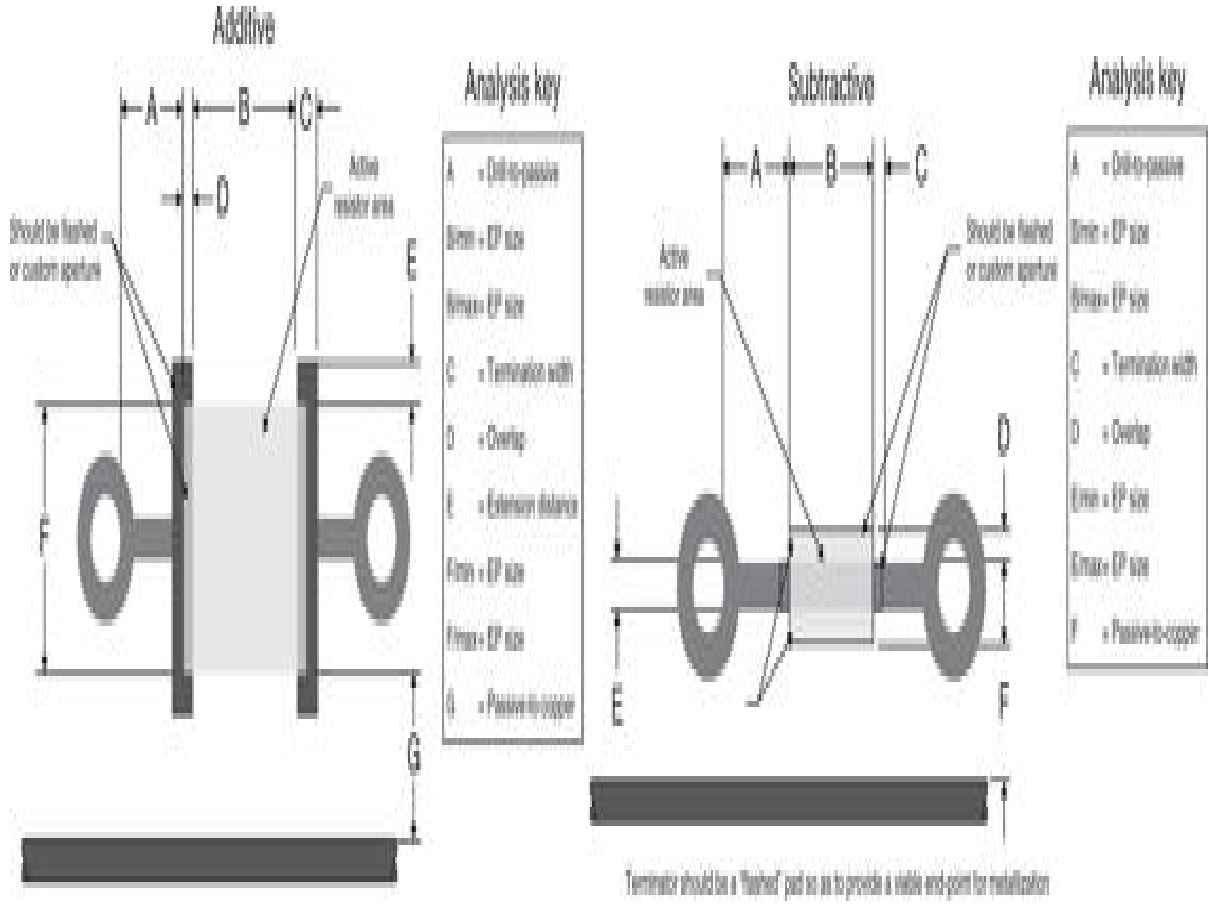


FIGURE 27.6 Critical tooling data for embedded passives.

An important step in all the processes already defined is the necessity for proper information management. Archival of PCB customer-supplied information and the files generated from the tooling process are critical for disaster recovery. Archiving systems available on the market also provide for centralized data management and distribution of the information to the various departments within an organization.

27.5.1 Macros

Macros (or scripts, as they are sometimes called) are used to automate tooling operations. Most modern CAM systems come with the facility to create, edit, debug, and exercise macros. One example of a macro was shown in Sec. 5.5.6.1 and in figure 5.27. This macro automatically scans all the CAM

information (artwork and NC files) and reports minimum, maximum, and critical geometries.

27.5.2 Design-to-Fab and Assembly Automation

Although a vast number of sophisticated CAD and CAM software packages are available today, experienced operators are still needed to exercise this software. During the era of captive printed circuit manufacturing by original equipment manufacturers (OEMs), internally developed software tools were created that actually automated the entire CAM tooling process. This level of automation was made possible through the development of software that automatically created drill, rout, fabrication, and panel drawings and manufacturing notes from the CAD database. In doing all this, the software captured in a digital header file all the pertinent information on the drawings. The header file could then automatically supply macros that would complete all the tooling. Although this software was never extended to the commercial market, today new automatic blueprint creation software is available that works off of the CAD database.

27.6 ACKNOWLEDGMENTS

I would like to thank Jeff Miller, WISE Software Solutions (www.wssi.com); DownStream Technologies (www.downstreamtech.com); and Julian Coates of Valor, Inc. (www.valor.com) for their invaluable contributions to this chapter.

CHAPTER 28

DRILLING PROCESSES[a]

Matthias Stickel
KSG Leiterplatten GmbH, Gornsdorf, Germany

28.1 INTRODUCTION

The purpose of through-hole drilling printed circuit boards (PCBs) is twofold: (1) to produce an opening through the board that will permit a subsequent process to form an electrical connection between top, bottom, and internal conductor pathways, and (2) to permit through-the-board component mounting with structural integrity and precision of location.

The quality of a hole drilled through a PCB is measured by its ability to interface with the following processes: plating, soldering, and forming a highly reliable, nondegrading electrical and mechanical connection.

As with any process, the elements of the drilling process are as follows:

- Materials
- Machines

- Methods
- Workers

When workers are properly trained and educated so that they possess a sound understanding of the other three elements, it is possible to drill holes meeting the aforementioned requirements with high productivity, consistency, and yield. The goals of this chapter are as follows:

- Understanding the drilling process thoroughly
- Recognizing what might go wrong
- Locating where problems could occur
- Detecting whether problems do occur
- Finding root causes of problems
- Correcting undesirable conditions
- Striving for zero discrepancies
- Making improvement a team effort

28.2 MATERIALS

Materials that affect the drilling process are as follows and as shown in the fishbone diagram of Fig. 28.1.

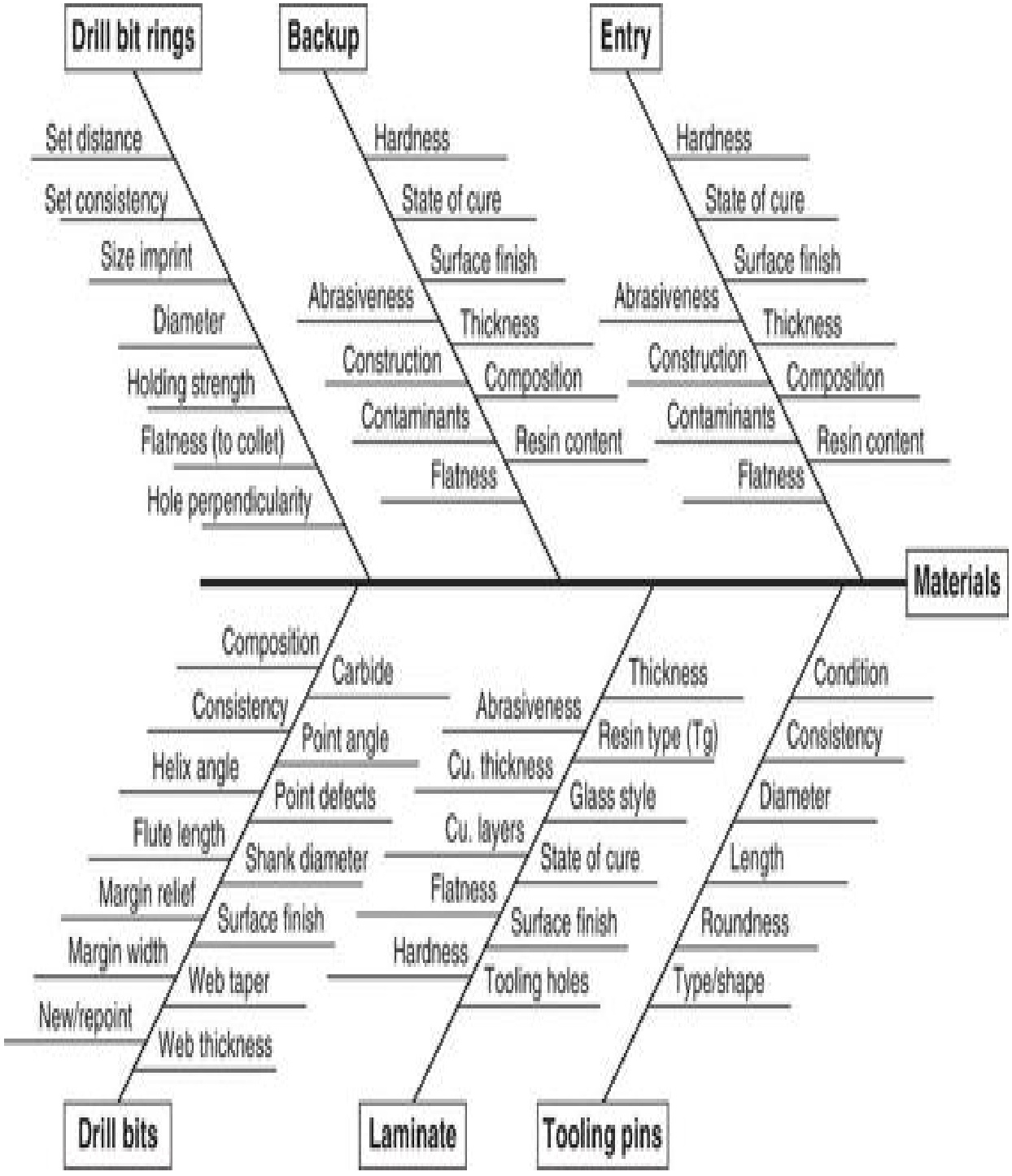


FIGURE 28.1 Materials used in the drilling process, with major variables and special considerations identified.

- Laminate material
- Drill bits

- Drill bit rings
- Entry material
- Backup material
- Tooling pins

28.2.1 Laminate Material

A typical circuit board laminate panel consists of three basic components:

1. Supporting fibers
2. Resin
3. Copper layers

The laminate substrate material is constructed of supporting fibers (most commonly a glass fiber weave) and a resin (most commonly an epoxy compound). Finished board thickness may range from 0.010 to 0.300 in or thicker, with the most common panel thickness ranging around $^{1}/_{16}$ (0.0625 in).

28.2.1.1 Supporting Fibers. Generally, the larger the glass fibers in the weave, the lower the cost of the base material. However, larger fibers are less desirable from a drilling point of view because they are more likely to cause the drill bit to deflect, resulting in decreased hole registration accuracy. In addition, larger fibers adversely affect drilled hole wall quality because they create larger (drilling) voids, defined as tear-out of supporting fibers. In simple terms: the larger the glass fibers, the larger the chunks torn out during drilling and thus the greater the hole wall roughness.

28.2.1.2 Resin. A common resin system is FR-4 epoxy. However, general drilling considerations (see Fig. 28.1) are the same for all resin systems. The glass transition (Tg)

rating of a material is defined as the temperature at which fully cured resin starts to soften. The Tg of “standard FR-4” is typically around 130°C, of “middle Tg FR-4” is around 150°C and of “high Tg FR-4” is around 170°C. Some materials include inorganic fillers resulting in a lowered z-axis expansion rate and making the material more stable under increased thermal environments like “lead-free assembly”. The compromise of a higher-Tg product which includes fillers is that the material is more brittle and more abrasive to the drill, resulting in increased tool wear and hole wall roughness. This increased abrasiveness to the drill bit may be offset by reducing the surface speed to reduce the spindle speed, resulting in less frictional heat being generated. Lowering drilling heat reduces drill wear.

28.2.1.3 Copper Layers. Outer and inner copper layers may be of various thicknesses, the most common being what is referred to as ½ oz and 1 oz copper. One ounce copper equates to a thickness of approximately 1.4 mils (0.0014 in). The more copper layers within a laminate, the more balanced the panel from a drilling point of view, meaning reduced occurrences or extents of drilled hole defects such as voids (torn-out fiber bundles). However, in order to compensate for a greater number of copper layers, the chip load (advance per revolution) that determines the infeed rate usually needs to be adjusted to control nail-heading. Increasing the chip load reduces the amount of nail-heading. In addition, more copper layers wear the drill bit at a faster rate and may require lowering the maximum hit count per drill bit.

28.2.2 Drill Bits

28.2.2.1 Materials. Drill bits are made of tungsten carbide because its wear resistance (and relatively low cost)

make it the most ideal material for cutting the very abrasive circuit board laminate materials. The binding agent for the tungsten carbide (>90 percent by weight) is cobalt (6 to 8 percent by weight). Other elements that can be added are titanium carbide, tantalum carbide, or other carbides (1 to 2 percent by weight). The carbides are categorized by their grain size into “ultrafine: (>0.5 μm), “extra-fine” (>0.05 to 0.09 μm) and “fine” (1 to 1.5 μm) with the smaller the diameter the smaller the selected grain size. The compromise of this very hard (carbide) material is that it is also brittle and subject to damage in the form of chips if not handled carefully and correctly.

28.2.2.2 Handling and Inspection. When handling drill bits, do not permit the bits to come in contact with one another and be careful not to touch them to the sides of the tool pods. Modern drilling machines utilize drill cassettes to reduce time per load by eliminating manual tool changes. These cassettes may accommodate 120 or more drill bits and reduce drill bit handling damage. If drill bits are measured to verify diameter using a contact-type measuring device (such as a contact micrometer), take the measurement away from the point to prevent chipping of the cutting corners. Following diameter measurement, inspect the drill bit for damage using a microscope. After use, again use care when removing drill bits from the tool pods or cassettes and remember, if they are intended for repointing, to use the same careful handling practices as when they were new.

28.2.2.3 Geometric Attributes. The geometry of a drill bit very much affects the way it behaves during drilling. (See Fig. 28.2 for attribute nomenclatures.) The land is the area remaining after fluting. In order to reduce the amount of land that creates friction with the hole wall (thus generating heat), drill bits are margin relieved. The amount of land

remaining in contact with the hole wall during drilling is referred to as the margin. The wider the margin, the greater the friction area and the higher the drilling temperature, resulting in higher extents of heat-related hole quality defects such as resin smear and plowing (defined as furrows in the resin).

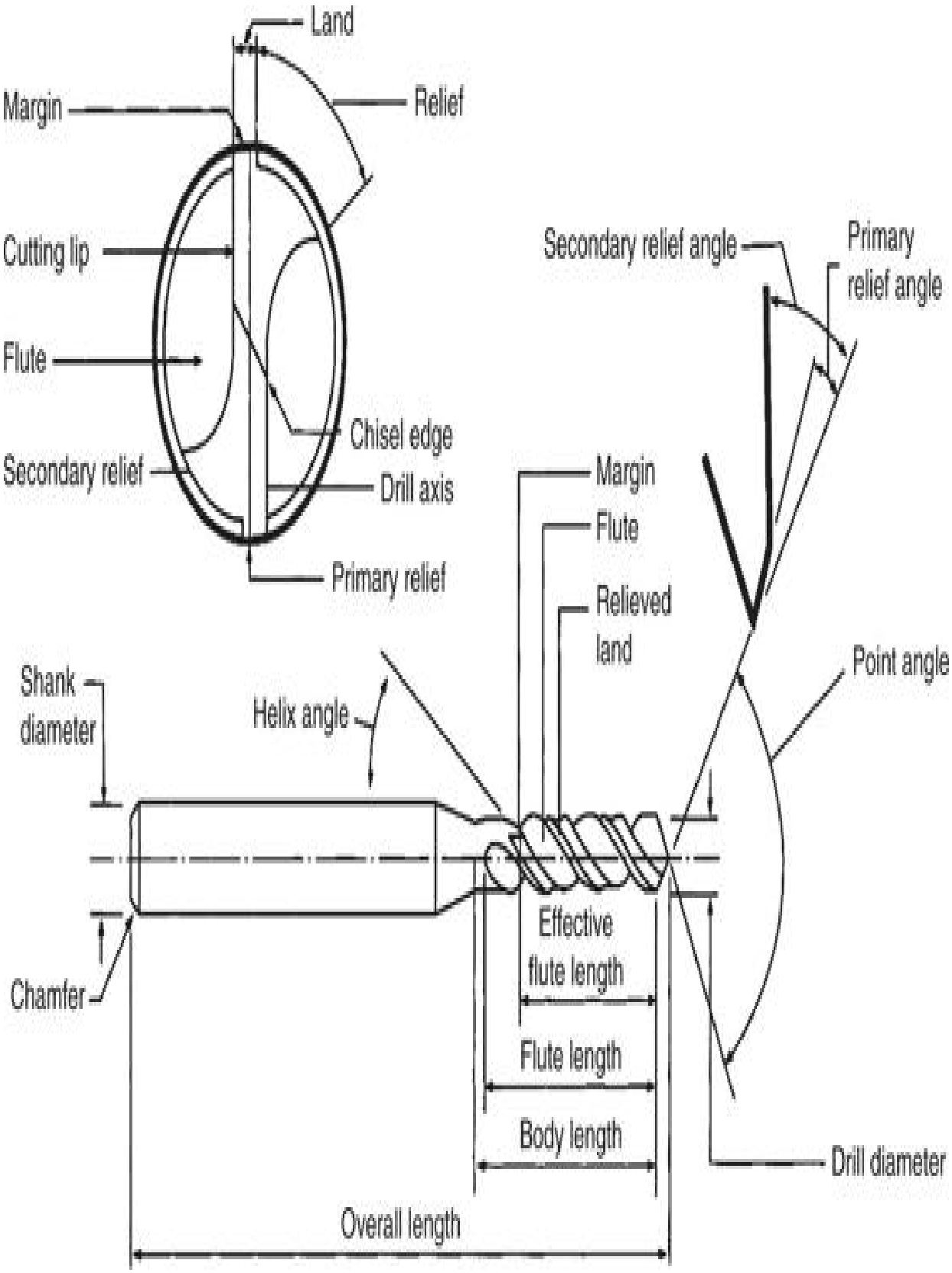


FIGURE 28.2 Drill bit geometry.

The result of increasing the land mass and the web is a smaller flute area. Less flute space implies reduced amounts of available area to remove drilling debris, which again raises the drilling temperature. It is important to understand that some drill designs that are meant to increase strength (particularly in smaller-diameter drill bits, with the intent to reduce breakage) may include what are referred to as partial margin reliefs (see Fig. 28.3). What this means is that when the drill bit is viewed from the point, a relieved margin is seen. However, viewing this type of design drill bit from the side reveals that the relief extends only part of the way, typically about one-fifth of the total flute length. The major drawback of this particular design is that it increases drilling temperatures (documented to be as much as 25 percent or more), resulting in increased heat-related drilled hole defects (such as smear) and drill breakage due to packed margins.

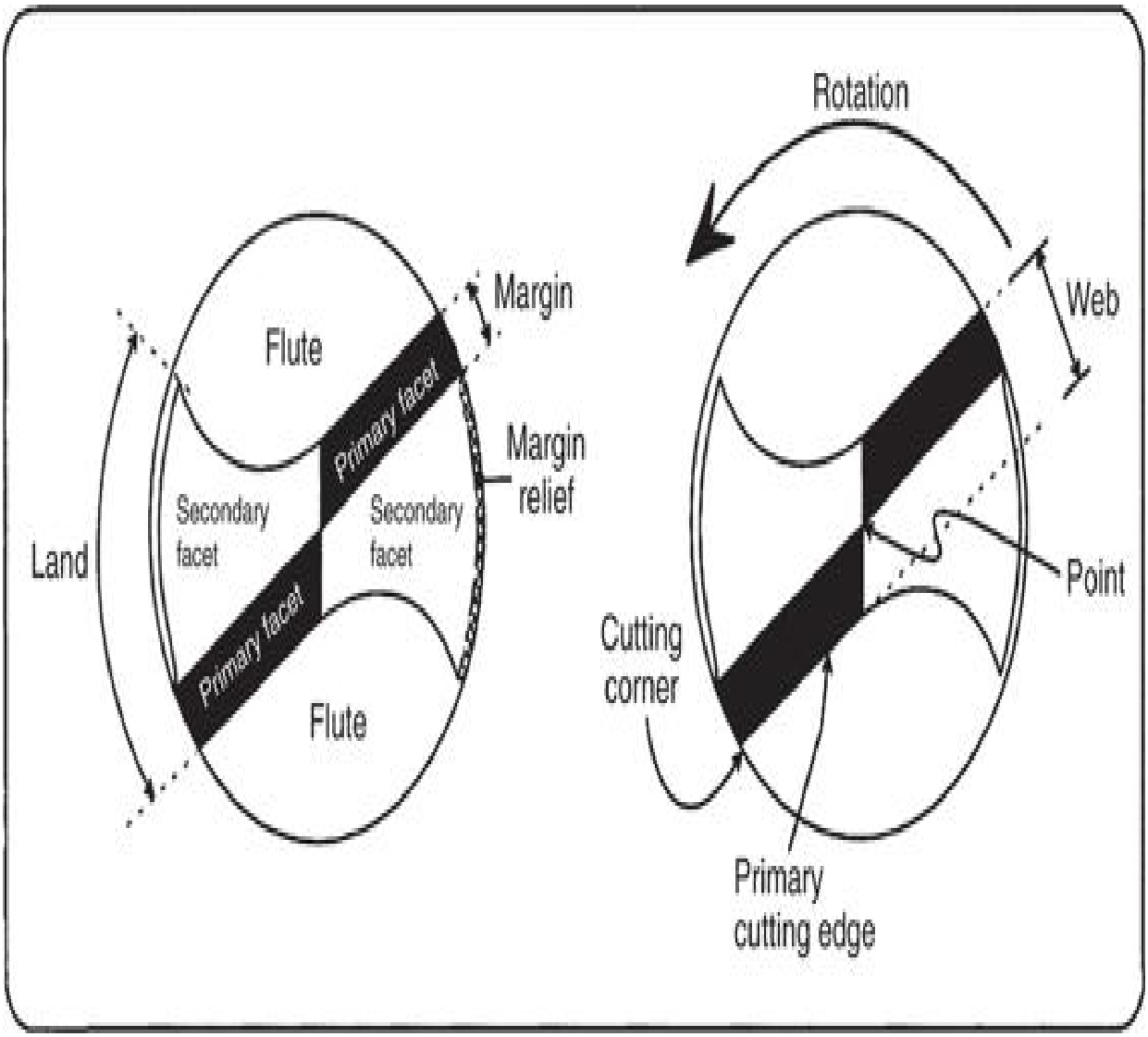
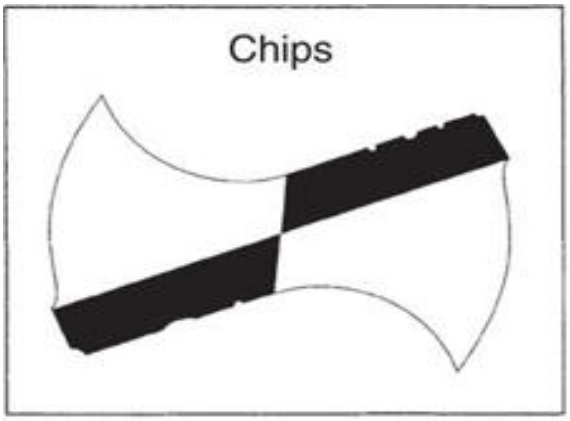
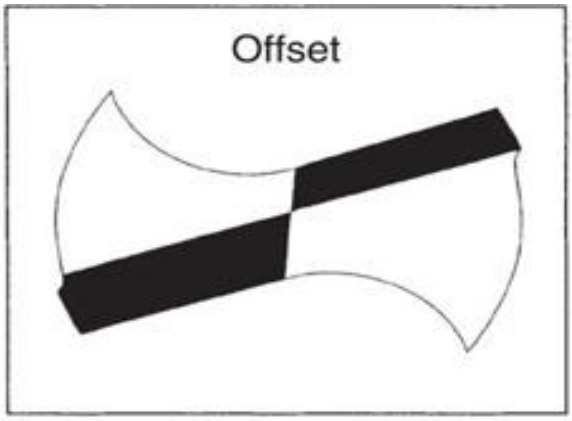


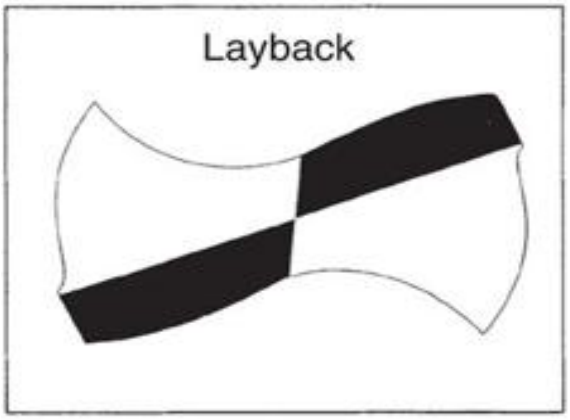
FIGURE 28.3 Drill tip attribute nomenclatures.

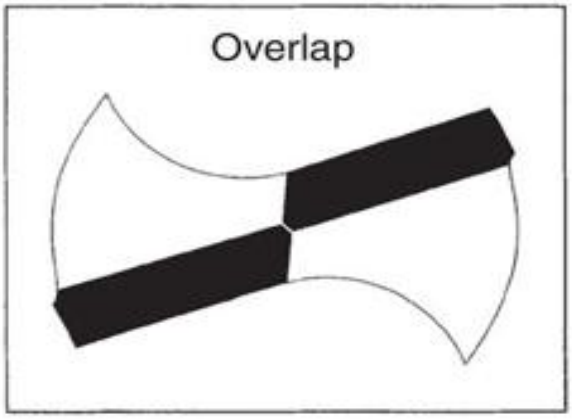
28.2.2.4 Flute Length. Minimum flute length must equal total drilled depth (total laminate thickness + entry thickness + backup penetration depth) plus at least 0.050 in of unused drill flute remaining above the stack at the bottom of the drill stroke to allow debris to be removed by the vacuum system. If debris cannot be removed from the drill flutes during and between drill strokes, the results are extensive hole quality defects and drill breakage.

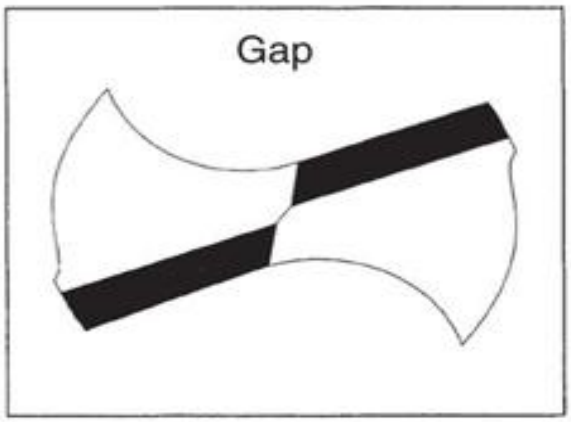
28.2.2.5 New Drill Bits. It is not necessary to inspect incoming orders of drill bits 100 percent. A procedure proved to be effective is to inspect drill bits according to an acceptable quality level (AQL) method (such as MIL-STD-105). This type of sampling plan allows the user to determine the percentage of drill bits that are inspected to judge an entire lot of drill bits to a predetermined quality level. Using this method, finding a defined quantity of drill bits that do not meet the specification is cause to return all received drill bits to the vendor; if the selected quantity of inspected drill bits meets specification, the entire lot of drill bits is accepted. Inspection criteria might include point geometry defects (refer to Fig. 28.4), damage (chips), diameter (drill and shank), and flute length, as well as correct ring set distance and size imprint (matching both the actual diameter and that labeled on the box).

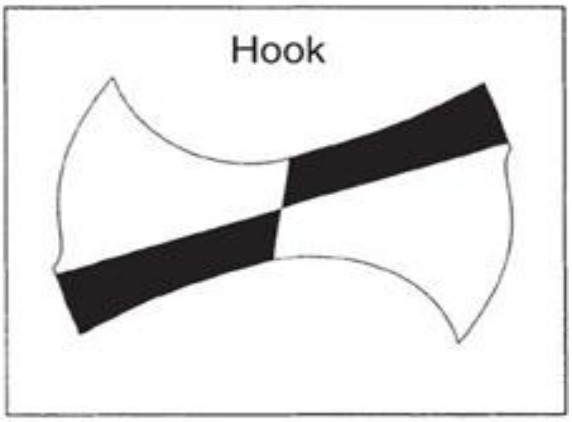

Chips

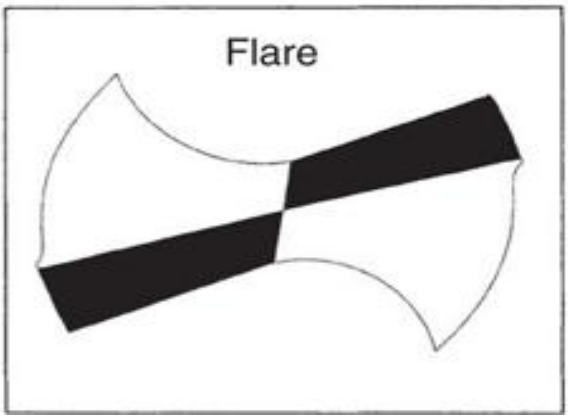

Offset


Layback


Overlap


Gap


Hook


Flare

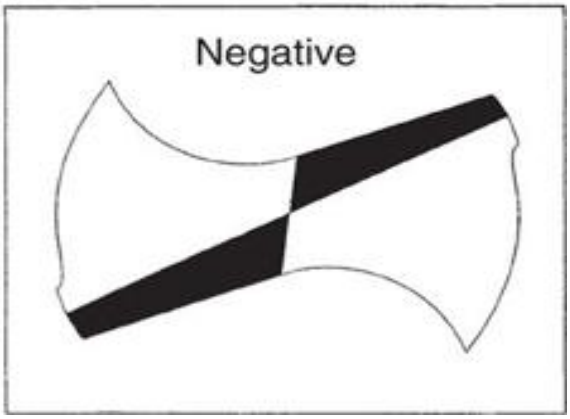

Negative

FIGURE 28.4 Drill point defect illustrations. (*Courtesy of LCOA Technical Center*.)

28.2.2.6 Repointed Drill Bits. Drill bits are typically repointed for reasons of economics. The cost of repointing a tool may be as low as 15 percent of the cost of a new tool. The number of times a drill is repointed varies anywhere from 1 to as many as 10 times or more and typically depends on the drill diameter. The smaller the drill, the fewer times it is normally repointed. The reason is that smaller-diameter holes are more critical and require better hole quality.

There are two methods used to repoint tools:

1. The first is to specify a certain number of times the tool is to be repointed before being discarded. This number typically varies between one to three for smaller-diameter tools depending on hole quality experienced after repointing.
2. The second is to specify a minimum overall length of the tool at which it is discarded. Minimum overall length is determined by calculation based on minimum remaining flute length required to drill the required total drilling depth. This method does not allow determination of how many times a drill is actually repointed because stock removal during each regrind may vary from 0.002 to 0.005 in or more.

Repointed drill bits cannot be expected to perform as well as new drill bits because only the points are refurbished to a quality that may be as good as a new drill bit while the rest of the drill bit, including the critical margin, is not. The condition of the margin is very important because it is the part of the drill bit that finishes the hole wall. A rough margin results in a rough hole wall surface. When inspecting repointed drill bits, examine the sides of the drills for margin damage and/or fused or packed drilling debris remaining

from previous use. These drill bits contaminate holes from the very first one drilled and may cause run-out due to an imbalanced condition of the drill bit resulting from the buildup. Drill bits must be repointed to the same point geometry specifications as those that apply to new drill bits. Point inspection criteria, therefore, is the same for repointed drill bits as for new drill bits.

28.2.3 Drill Bit Rings

Drill bit rings are set to a common distance from the point to the back of the ring, thereby allowing a controlled drilling depth on machines lacking other options for applications requiring this. The quality of these rings is as critical as the consistency of drill bit attributes because they can equally affect drill bit performance. Rings that fit loosely on the drill shank have been known to move during tool changes, resulting in insufficient drilling depth. Rings that fit too tightly may crack. Rings that have protruding material (“flash”) on the inside diameter may cause improper seating of the drill bit in the collet (of the spindle) or may prevent the drill bit from being properly inserted into the tool pod or cassette, resulting in destructive tool change problems.

Rings have specific color codes assigned to each size and are commonly imprinted with size, diameter, and design or series number. Rings may be either machined or mold-injected. While machined rings are superior because of their consistency and quality, their cost is prohibitive for many drill bit manufacturers. Some of the drawbacks of mold-injected rings that must be monitored are inside diameter, affecting how well the ring fits on the drill shank, and remaining flash.

28.2.4 Entry Material

28.2.4.1 Purpose. The purpose of the entry material is fivefold:

- Centers the drill
- Prevents drill breakage
- Prevents copper burrs
- Avoids contamination of the hole or drill bit
- Prevents pressure foot marks

28.2.4.2 Types. There are many different available types (constructions) of materials used as entry material for PCB drilling, although few are specifically designed and engineered for this purpose. Engineered products are designed to improve hole registration accuracy and reduce drill breakage. The performance qualifications of the most popular materials are discussed in the next section.

Commonly available entry materials, listed in order of performance quality with respect to the five characteristics listed in the preceding section, are

- Aluminum-clad cellulose core composite
- Solid aluminum (various alloys and thicknesses)
- Solid or melamine-clad phenolic
- Aluminum-clad phenolic

28.2.4.3 Performance. The right entry material will improve drilled hole registration and lower the risk of drill bit breakage by minimizing drill deflection upon contact with the stack. In order for the entry material to function properly, it must be flat and free of pits, dents, and scratches. Warped or twisted material will result in increased extents of entry burrs and drill bit breakage. Surface imperfections and materials that are too hard contribute to drill deflection, resulting in decreased hole registration accuracy and breakage of small-diameter drills.

Phenolic materials or phenolic composites (i.e., aluminum-clad phenolic) often warp and under most drilling conditions contaminate the hole wall, which results in problems with adherence of the plating because desmearing chemicals are not designed to remove phenolic resin. Solid aluminum materials of the correct composition and hardness that are not of an excessive thickness, yet are not too thin, may work satisfactorily with larger-diameter drill bits. However, drilling with solid aluminum materials (0.008 in and thicker) may increase the risk of breakage of smaller-diameter drills. Aluminum-clad cellulose core materials provide a hard surface to prevent burrs yet minimize drill deflection and breakage associated with solid aluminum.

28.2.5 Backup Material

28.2.5.1 Purpose. The purpose of backup material is defined by the following criteria. An ideal backup material will

- Provide a safe medium for drill stroke termination
- Prevent copper burrs
- Not contaminate the hole or drill bit
- Minimize drilling temperatures
- Improve hole quality

28.2.5.2 Types. Numerous materials are available that are sold as backup material. Few of the materials used as backup materials are actually specifically engineered for circuit board drilling. Many of the popular backup products are composites with a variety of surface coatings or skins bonded to several different core materials. Available backup products include the following:

- Epoxy-paper-clad, wood-core composite utilizing a bonding agent with lubricating properties
- Aluminum-clad, wood-core composite
- Epoxy-paper-clad, wood-core composite
- Melamine-clad, wood-core composite
- Urethane-clad, wood-core composite
- Solid phenolic
- Aluminum-clad phenolic composite
- Plain wood
- Hardboard

28.2.5.3 Performance. Desired qualities in a backup material are minimal thickness variations, flatness (no bow, warp, or twist), no abrasives or contaminants, a smooth surface, low cutting energy (minimizing drilling temperatures), and a surface hardness that supports the laminate copper surface (to prevent burrs) yet does not cause damage or extensive wear to the drill bit.

Backup materials with lubricating properties have been proven to significantly reduce drilling temperatures by as much as 50 percent or more, often resulting in temperatures below the T_g of the laminate product being drilled. This advantage greatly reduces hole wall defects such as roughness, smear, and nail-heading and often allows increased drill stack heights and/or greatly increased drill bit maximum hit counts. The importance of these benefits is significant reduction in drilling cost per hole and improved productivity and yield.

Remember that drilled backup debris exits the stacks by passing through the holes in the laminate material and that therefore contamination (from the backup material) is of great concern. Materials containing phenolic, or composed of solid phenolic, are not suitable for circuit board drilling. Phenolic materials or phenolic composites (i.e., aluminum-

clad phenolic) often warp and under most drilling conditions contaminate the hole wall, which results in problems with adherence of the plating because desmearing chemicals are not designed to remove phenolic resin. Hardboard types of materials cannot be maintained to thickness variation tolerances acceptable for circuit board drilling and are a source for a great variety of contaminants (e.g., oils crystallized on the surface for hardening purposes).

28.2.6 Tooling Pins

Seldom is any due attention given to the tooling pins. They come in many shapes and sizes and their cost, with respect to how much they add to the cost of fabricating a circuit board, is insignificant. Yet, quite often, tooling pins are found to be damaged or deformed (e.g., “mushroomed” from being hammered into the stack) or do not fit snugly. Tooling pins that do not hold the stack tightly in place or that allow the stack to move create a large variety of problems from burrs and other hole defects to poor registration or drill bit breakage. These unnecessary problems may be prevented by simply replacing tooling pins when they start to show signs of wear or damage. Use tooling pins that are hardened to minimize wear and deformation, and (ideally) $^{3}/_{16}$ in. in diameter. Pins that are less than $^{3}/_{16}$ in. in diameter (i.e., ⅛ in) do not hold the stack firmly in place during drilling and may result in stack movement.

28.3 MACHINES

Machine variables that affect the drilling process are as follows and as shown in the fishbone diagram of Fig. 28.5.

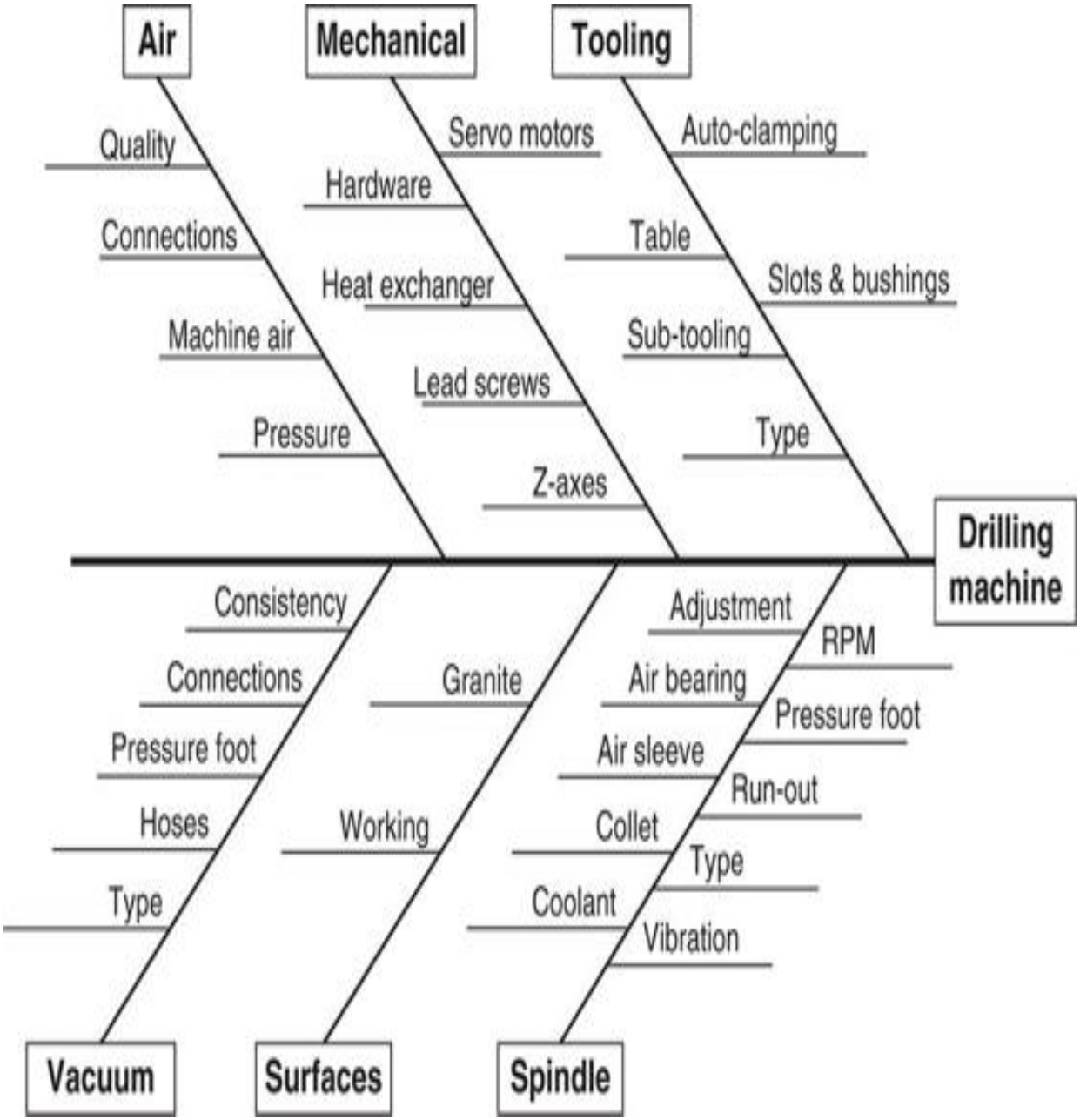


FIGURE 28.5 Drilling machine elements, with major issues and special considerations identified.

28.3.1 Air

28.3.1.1 Quality. Maintaining high levels of air quality is important. Air supplied to the machine and the spindle assemblies needs to be clean and dry. This is accomplished

by filters that remove dirt and moisture from the air. In areas where the relative humidity is high, or when using air-bearing-type spindles, an inline air drying and filtering system may be necessary to control air moisture levels and dirt. Moist air causes corrosion of air surfaces (such as the spindle sleeve and other spindle components operating on air) and reduces the life of these components, resulting in increased repair costs. Dirty air affects operation of components relying on air by clogging the channels that supply the air (e.g., to the spindle sleeves and table air shoes). In addition, dirt serves as an abrasive that causes faster wear of machine components, resulting in reduced life cycles between repairs, again increasing downtime and repair costs. Cleaning the machine air filters and purging air compressors and lines on a routine basis may minimize problems resulting from dirt or moisture.

28.3.1.2 Connections and Pressure. Check connections, gauges, hoses, and switches for leaks and wear. Air hoses connected to the pressure foot pistons often crack near the piston connector; by simply bending the hoses in these areas it can be determined whether they are leaking. Other locations that commonly have poor connections and air leaks are the collet air connector on top of the spindle and the air manifold on the side of the spindle sleeve housing that supplies air to the collet and the spindle sleeve. Sufficient air pressure to both the collet and the spindle sleeve is critical and must be maintained adequately for proper operation. The tool table is designed to ride on a bearing of air supplied through the table air shoes. Verify proper operation of the air shoes by slightly rotating them back and forth; the shoes should move freely. If the shoes do not move with ease or do not move at all, the most likely reason is that the air channels are blocked due to trapped drilling debris, meaning the shoes need to be cleaned or replaced. Check the pressure foot air gauges for the correct

air pressure; equal pressure must be supplied to each of the spindle stations. Insufficient or unequal air pressure results in burrs and increases the possibility of drill bit breakage.

28.3.2 Vacuum

Effective vacuum is absolutely essential because it greatly affects the resulting drilled hole quality. Heat (drilling temperature) seen by the hole walls depends on how effectively hot drilling chips are removed. Excessive temperature due to inefficient removal of drilling debris causes heat-related hole defects such as smearing and plowing, increases the opportunity for plugged holes, and is a major contributor to drill wear. Check hoses for proper connections, wear, and restrictions and examine the inside of the pressure foot for holes worn inside the connector attaching the vacuum hose.

28.3.3 Tooling

28.3.3.1 Bushings and Slots. Maintain tight tolerances on tool table bushings and slots and replace bushings that are sunken below the tool table surfaces or are worn. Bushings and slots that do not hold tooling pins snugly and allow stack movement during the drill stroke cause burrs, registration problems, and drill breakage.

28.3.3.2 Subtooling. Avoid subtooling plates that overlap across individual tool table stations and fasten the plates securely to the base plates with no separation or gaps. Ensure the subtooling is not warped, does not vary significantly in thickness, and has no surface protrusions (such as broken drill bits) to allow stacks to lay flat and to minimize variation in drill bit penetration depth into the backup material. If your subtooling is other than metal,

watch for potential shrinkage or expansion problems indicated by difficulties in fitting the pinned stacks to the existing pinning holes in the plates. If this problem occurs, the results are the same as those caused by bushings and slots that allow stack movement.

28.3.4 Spindles

Spindle assemblies are one of the single most important components of the drilling machine. Proper operation is essential and requires maintenance (e.g., collet and collet seat cleaning) and verification on a regular basis.

28.3.4.1 Collet Maintenance. For mechanical (ball) bearing spindles, cleaning of the collet and the collet seat (inside the spindle) needs to be performed a minimum of once per shift; dirty collets increase drill run-out. When processing certain laminate materials that create greater amounts of drilling dust, and depending on your vacuum system efficiency, a higher cleaning frequency may be necessary to maintain acceptable levels of drill run-out. It is recommended that after cleaning the collets be returned to the same spindle from which they were removed because collets tend to adjust to the respective collet seats. For air-bearing spindles, most manufacturers recommend cleaning the collets only when the run-out measures excessive.

28.3.4.2 Run-Out Measurement. Drill/collet concentricity, or total indicated run-out (TIR), is a measure that indicates how true the assembly rotates. It can be determined while the spindle is running at various speeds (rpm), which is referred to as a dynamic form of measurement. Another method is performed while the spindle is not running and is called a static measurement. Static TIR is determined by rotating a ⅛-in (0.1250-in)-diameter pin installed into the collet by hand while reading

movement on a dial indicator placed against the pin at a distance of approximately 0.800 in (simulating the distance of the drill point) from the collet nose (refer to Fig. 28.6). Of course, the pin used to measure TIR must itself be concentric.

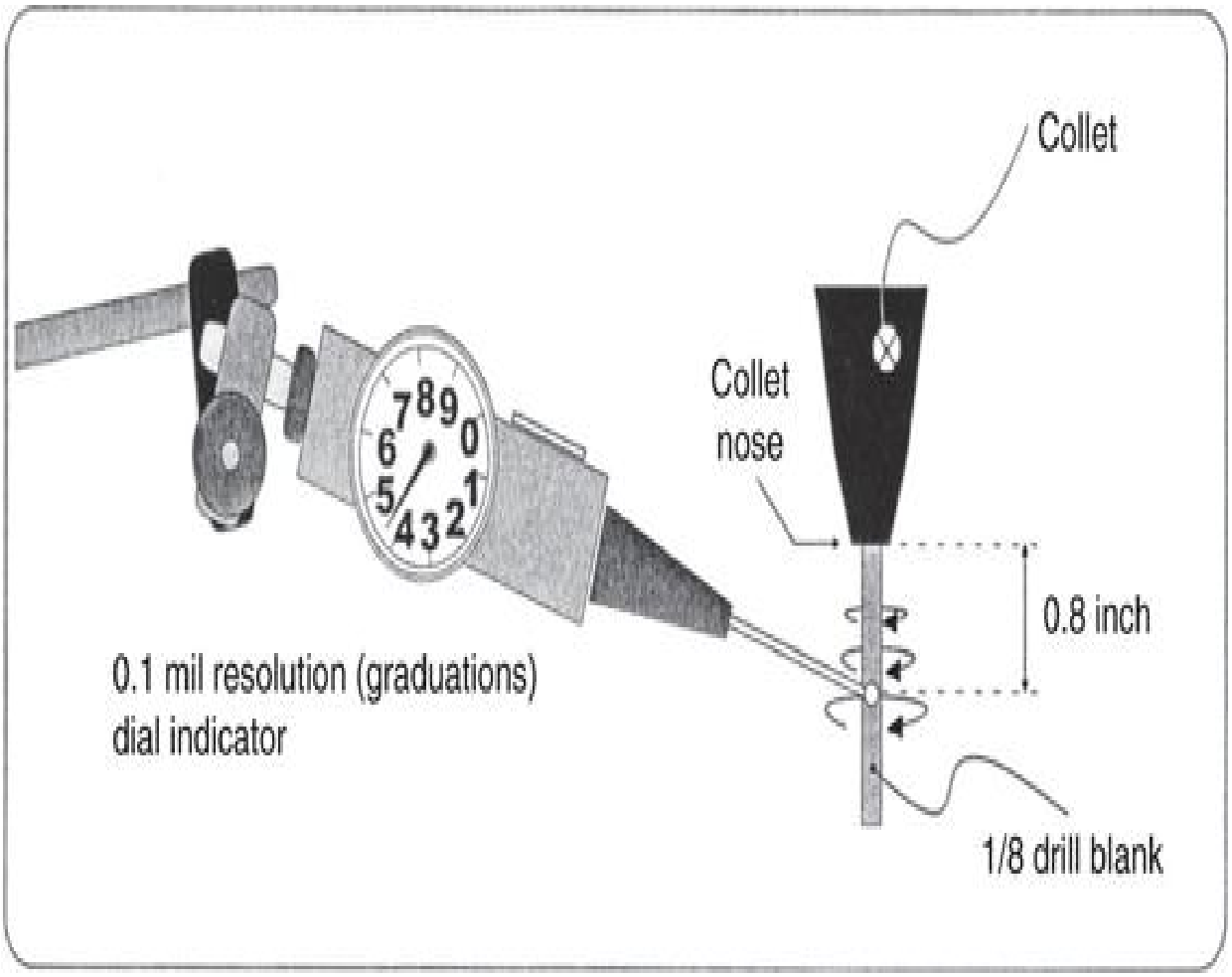


FIGURE 28.6 TIR measurement (static).

Maximum acceptable TIR for drills greater than 0.0200 in. in diameter is 0.5 mil (0.0005 in). When using drills 0.0200 in or less in diameter, the maximum TIR needs to be maintained within 0.2 mil (0.0002 in) to prevent drill breakage. If excessive TIR is noted, it is wise to replace the pin and again measure the run-out. Drill bit blanks make ideal pins for measuring TIR and may be acquired from drill

bit suppliers. Excessive spindle run-out results in drill breakage, causes burrs and other drilled hole defects, and adversely affects hole registration accuracy. Excessive TIR may often be corrected by simply cleaning the collet and the collet seat or by replacing a worn collet. Measure the run-out of spindles of each machine at a minimum frequency of once per week.

28.3.4.3 Spindle Speed. Maintaining correctly adjusted spindle speed is important because spindles running at speeds other than those displayed on the monitor imply that drill bits are rotating at surface speeds other than those that are desired. When actual rpm is higher than the displayed rpm, it implies higher surface speeds (refer to Sec. 28.4), and vice versa. Higher surface speeds cause greater frictional drill heat, resulting in faster drill wear and greater extents of heat-related hole defects such as smearing and plowing. Noncontact-type tachometers able to measure up to 150,000 rpm or more are available for around $300 (a lot less than the cost of rebuilding just one spindle) and allow measurement of actual spindle rpm in a matter of minutes. Verifying spindle speeds once every 6 months is usually sufficient.

28.3.4.4 Pressure Foot. The pressure foot insert lead distance to the point of the drill bit is set at approximately 0.050 in to give the pressure foot sufficient time to hold the stack flat before the drill bit contacts and enters the stack. If the lead distance is significantly less than the specified distance or if the drill bit point protrudes from the pressure foot, drill bits will break. To ensure the pressure foot assemblies function properly, check pressure foot inserts for wear or damage daily and verify that the pistons and guide rods are not bent and move smoothly.

28.3.4.5 Adjustment. When adjusting the physical *z*-axis height of the spindle, for instance to accommodate a thicker subtooling plate, care must be taken to also adjust the pressure foot so its height remains identical relative to the spindle. The pressure foot adjustment is independent from the spindle and, if not performed correctly, may result in a gap between the bottom of the spindle casing and the top of the pressure foot window. This gap is noticed only while the spindle is engaged and will draw most of the vacuum air, effectively cutting off the vacuum from the pressure foot insert, resulting in a great variety of hole defects and drill bit breakage. If a gap is present, it is usually accompanied by great amounts of drilling debris spewed across the stacks and drilling machine.

28.3.5 Mechanical Factors

28.3.5.1 Heat (Coolant) Exchanger. Drill motor temperatures are reduced by exchanging a fluid through the spindles. The fluid is processed through a heat exchanger that works much like a car radiator. As with a car, it is important to maintain the recommended coolant mixture, proper fill level, and flow rate indicated by the flowmeter. Check the operation of the fan and minimize coolant flow restriction (due to algae buildup) by cleaning filters regularly. Algae growth is promoted through exposure to ultraviolet light and may be controlled by using black hoses instead of clear ones in addition to adding growth inhibitors to the coolant mixture.

28.3.5.2 Hardware. Although simple to perform, checking mechanical connections for loose or worn parts (i.e., causing travel slop of pressure foot assembly movement) is often neglected. It may be accomplished by

observing the machine while it is running or checking by hand while the machine is idle.

28.3.5.3 Lead Screws and Servos. The environment and cleanliness of the drill room determine how often lead screws need to be cleaned and lubricated to ensure smooth operation and minimize wear. Most machine manufacturers recommend performing this type of maintenance every 6 months. When lubricating the lead screws, only a light coat of the appropriate grease needs to be applied. Excessive amounts of grease on the lead screws defeat the purpose, as this causes more dirt to be attracted, resulting in faster wear. Constant searching for programmed *x*-*y* locations indicates problems with the servo motors or lead screws. If this occurs, the displayed *x* or *y* (actual) location displayed on the controller will change continuously while the machine is stopped.

28.3.5.4 z-Axis Stroke. Because machines may have as many as six mechanical connections in the *z* axis, travel slop during the drill stroke or retraction may occur, causing chip loads to vary during the stroke, which results in burrs and other hole defects and drill breakage. Check connections by hand for slop while the machine is idle and observe and listen for improper operation while the machine is running.

28.3.6 Surfaces

A clean drilling room decreases repair costs and the possibility of improper operation of the drilling machines. Wipe surfaces clean using a lint-free cloth or use a vacuum to remove debris.

Never use compressed air to clean the drilling machine because debris will be blown into areas that need to be kept clean (e.g., lead screws).

28.3.6.1 Granite. Granite provides a stable platform that absorbs unwanted vibration. It also offers a smooth and level surface to support the movement of the table. Keep granite surfaces clean to prevent tool table air shoes from becoming clogged and to minimize collection of dirt on the lead screws.

28.3.6.2 Working Surfaces. Maintain clean working surfaces, such as the tool table, to minimize the possibility of dirt particles getting trapped between the stacked laminate, entry, and backup panels, causing stack separation that may result in burrs and possible drill bit breakage.

28.4 METHODS

Drilling parameter variables that affect the drilling process are as follows and as shown in the fishbone diagram of Fig. 28.7.

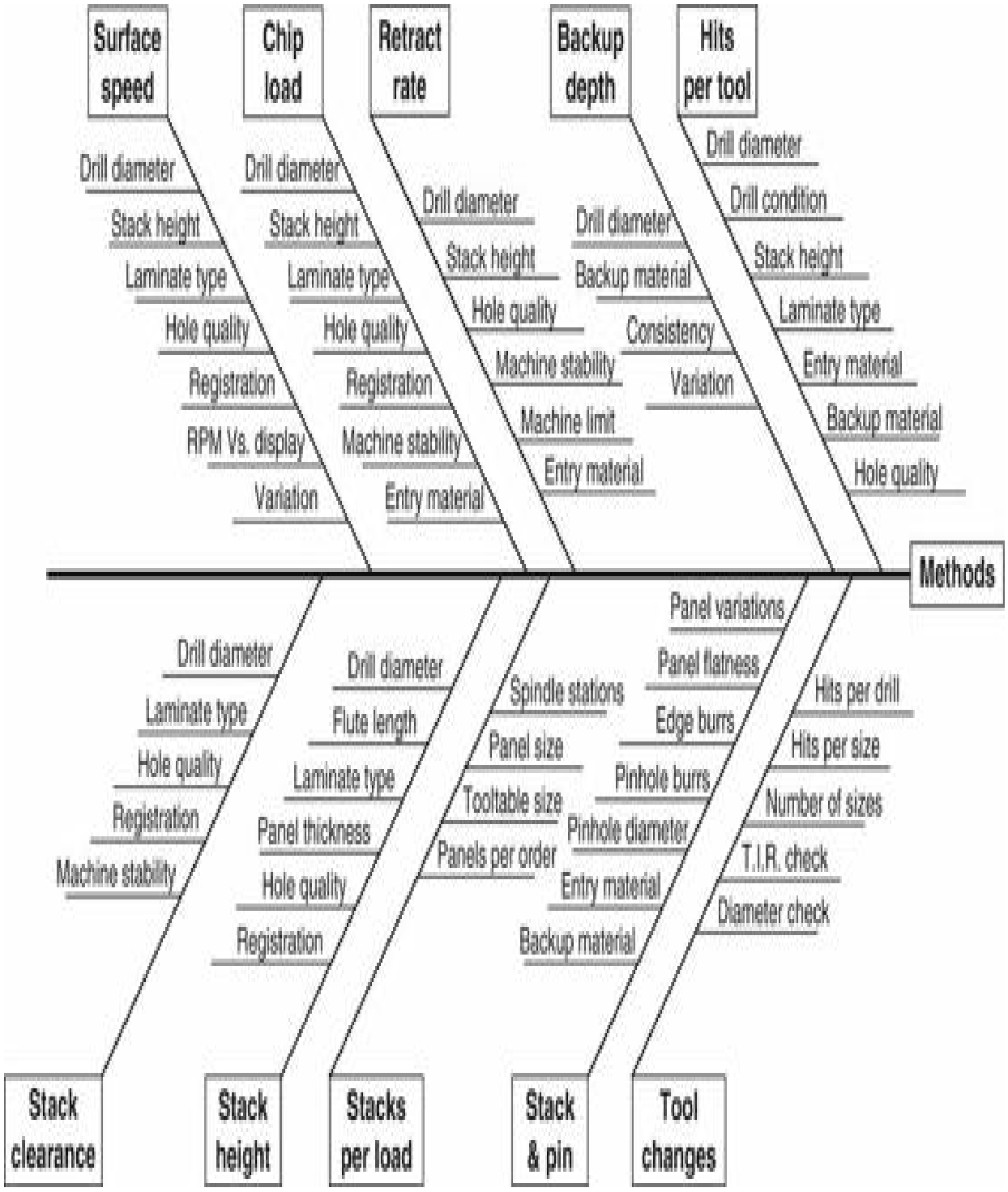


FIGURE 28.7 Methods used in the drilling process, with major variables and special considerations identified.

28.4.1 Surface Speed and Spindle Speed

As holes are getting smaller, higher spindle speeds are required to achieve the desired surface speed that determines throughput. However, higher surface speeds result in higher drilling temperatures that may increase heat-related hole defects such as smearing and plowing.

28.4.1.1 Definition. Surface speed is a measure of how much distance is covered by the drill's diameter while it is rotated by the spindle and is expressed in surface feet per minute (sfm). It is used to calculate spindle speed (rpm) for a given drill diameter. The formula to calculate spindle speed using the desired surface speed is shown in Eq. (28.1).

$$\text{spindle speed (rpm)} = \frac{\text{sfm} \times 12}{\pi \times \text{diam.}} \tag{28.1}$$

$$\text{where diam.} = \text{drill diameter (in)}$$

$$\pi = 3.1415$$

$$\text{cutting speed} = \pi \times \text{d}/1000 \times \text{spindle speed}$$

28.4.1.2 Effects. The higher the surface speed, the higher the spindle speed, and subsequently the higher the frictional heat that is generated, translating into greater extents of heat-related hole defects and drill wear. Conversely, lower surface speeds imply lower spindle speeds and less frictional heat. When more abrasive materials (e.g., materials with higher T_g such as multifunctional FR-4, polyimide, or cyanate ester) are processed or drilled stack height is increased, drilling temperatures increase. To offset the resulting increase in temperature under such conditions or when excessive extents of heat-related hole defects are

apparent, decrease the surface speed to lower the spindle speed.

28.4.2 Chip Load and Infeed Rate

28.4.2.1 Definition. Chip load is defined as advance per revolution and is usually expressed in mils [1 mil equals $^{1}/_{1000}$ of an inch (0.001 in)]. It implies the distance the drill travels during the drill stroke per each full revolution of the drill bit. Chip load is used to calculate the infeed rate in inches per minute (ipm).

$$\text{infeed rate (ipm)} = \text{chip load (mils/revolution)} \times \text{rpm} \qquad (28.2)$$

28.4.2.2 Effects. Higher chip loads result in greater throughput. However, chip load and infeed rate affect hole registration accuracy, drill breakage, burrs, and mechanical types of drilled hole defects such as voids (tear-out of the supporting fibers) and nail-heading. Faster infeed rates translate into higher (top laminate) entry burrs, lower extents of nail-heading defects and (bottom laminate) exit burrs, increased occurrences of drill bit breakage, and higher extents of drilling voids. Lower infeed rates result in exactly the opposite but lower throughput.

28.4.3 Retract Rate

28.4.3.1 Definition. Retract rate is the speed at which the drill bit exits the stack following the drill stroke and is expressed in inches per minute (ipm). Machine default (maximum) settings vary between manufacturers and may range anywhere from 500 to 1000 ipm.

28.4.3.2 Effects. Higher retract rates imply lower processing times per load. While the maximum retract rate

setting may be fine for larger-diameter drill bits, when using drill bits in the diameter range of 0.0250 in (size #72) to 0.0135 in (size #80), retract rates may have to be reduced to 500 ipm or lower to prevent drill breakage. When drilling with sizes smaller than 0.0135 in. in diameter, retract rates may have to be reduced even further. The maximum retract rate that may be used with any given drill diameter without causing drill breakage greatly depends on the stability and vacuum system efficiency of the drilling machine as well as the drilled stack height, laminate construction and thickness, type of entry material, use of proper stacking and pinning procedures, and the design characteristics of the drill bit such as flute length, web thickness, and web taper.

28.4.4 Z Compensation/Individual Z/Point Length

28.4.4.1 Definition. The z compensation or “individual z” refers to geometric aspects at the tip of a drill bit. It describes the length of the tip which varies with the point angle and the drill bit diameter (see Figs. 28.8 and 28.9).

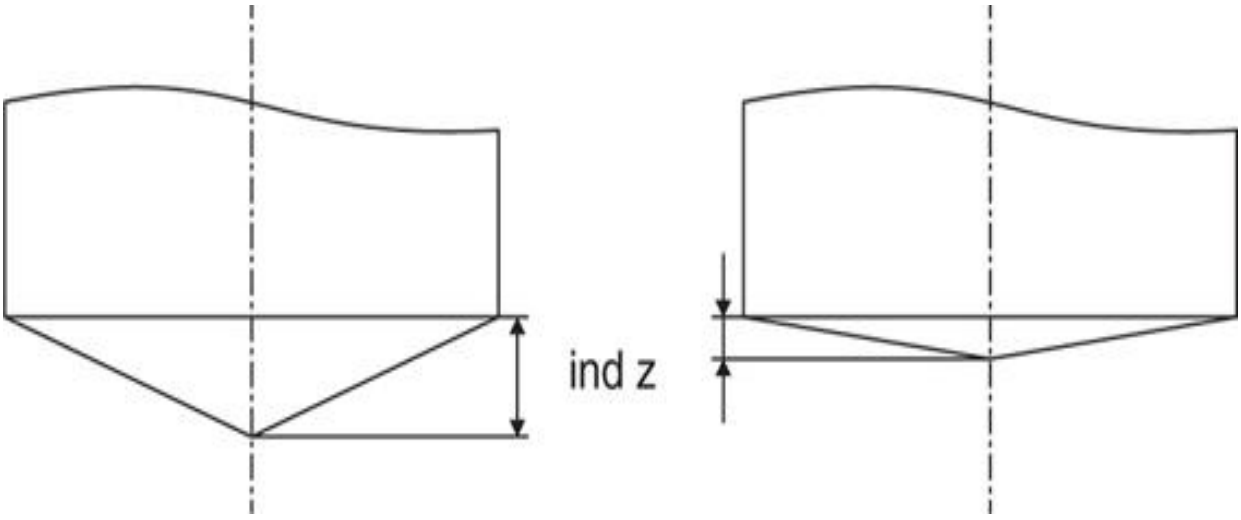


FIGURE 28.8 Individual z on bits with different point angles.

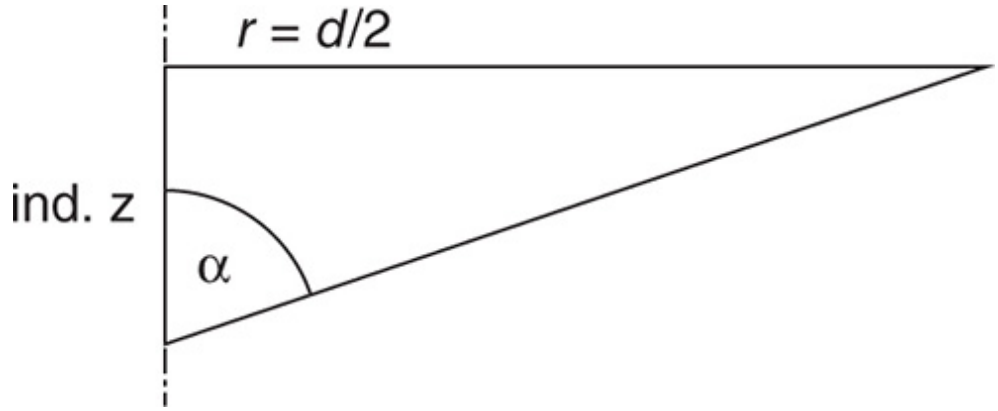


FIGURE 28.9 Geometrical aspects of the individual z.

28.4.4.2 Effects. The z compensation has an influence on the drilling depth. This is why it needs to considered in the drilling depth into the backup material ("backup penetration") and for any "depth controlled" drilling operations (blind vias, back drilling). As it depends on the drill bit diameter and the point angle, it is typically part of the parameter file.

$$\tan a = r/\text{ind. z} \qquad r = \text{radius [mm]}, d = \text{diameter [mm]}, a = \text{point angle/2 [°]}$$

$$\text{ind. z} = r/\tan \alpha$$

$$\text{ind. z} = d/2 \times \tan \alpha$$

28.4.5 Backup Penetration Depth

28.4.5.1 Definition. Backup depth is the distance a drill bit penetrates the backup material at the bottom of the drill stroke. The minimum backup penetration depth setting varies depending on drill diameter and is determined by calculating the drill bit point length (see Fig. 28.10) and adding approximately 0.010 in. As a rule of thumb, backup penetration depth may be set to a distance equal to the drill diameter or 0.040 in, whichever is less.

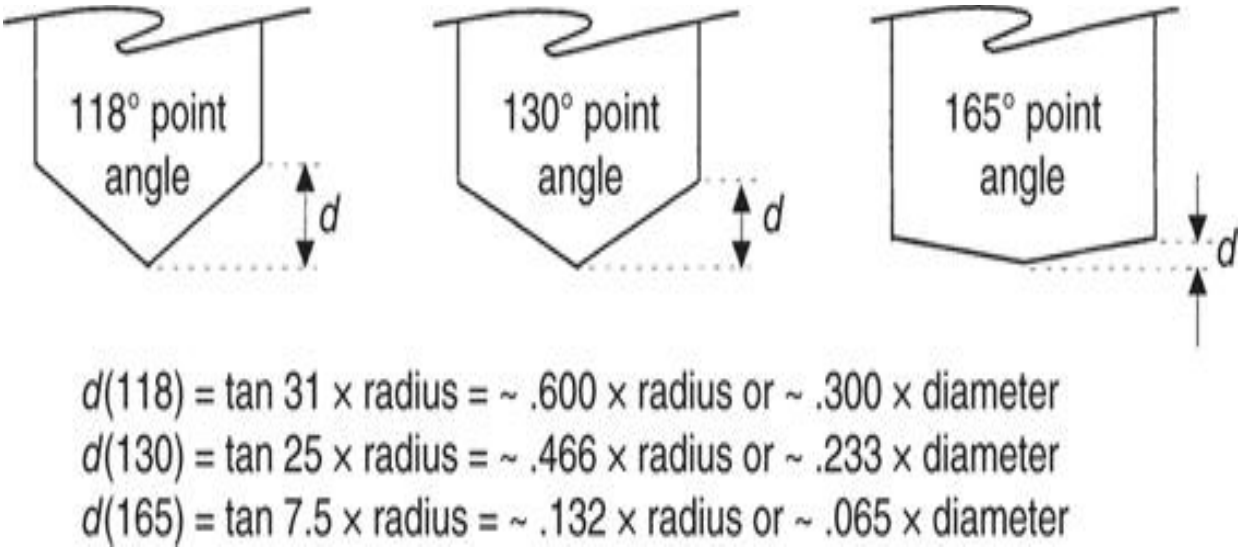


FIGURE 28.10 Point length calculation.

28.4.5.2 Effects. Excessive backup penetration depth increases drill wear and the occurrence of breakage of small-diameter drill bits, adversely affects hole quality, and increases process time per load. Insufficient backup penetration depth results in incompletely drilled holes. This implies that thickness variations of the backup material are very important, meaning that minimal variations are a much desired characteristic of the backup and need to be considered when choosing a material suitable for your application.

28.4.6 Hits per Tool

28.4.6.1 Definition. The maximum hits per tool specified for any given drill size implies the number of drill strokes a drill bit is used for until its expected effective life is expired. Maximum hit count per tool is product and process specific and is affected by laminate material construction, panel thickness, drilled stack height, surface speed, and the type of entry and backup material used. Additionally are there different quality specification levels that can be

applied. Therefore no specific number of hits per tool can be arbitrarily specified.

28.4.6.2 Effects. Excessive drill wear caused by excessive maximum hit count increases drilled hole defects and may prevent proper repointing. Conservative maximum hit counts greatly impact drilling cost per hole and increase time per load because of increased numbers of tool changes.

28.4.6.3 Parameter Example.

Diameter [mm]	Speed/RPM [rev/min]	Cutting-Speed [m/min]	In-Feed [m/min]	Chip-Load [mm/rev]	Retract-Rate [m/min]	Ind-z [mm]	Hit Count [#hits]
0,10	125000	39	0,8	0,006	2	0,030	500
0,15	125000	59	1,3	0,010	3	0,045	600
0,20	125000	79	1,8	0,014	4	0,060	800
0,25	125000	98	2,4	0,019	5	0,065	1000
0,30	125000	118	2,9	0,023	6	0,070	1200
0,35	125000	137	3,2	0,026	7	0,082	1300
0,40	119000	150	3,5	0,029	8	0,093	1500
....	....	....	....	....	....	....	....
2,20	22000	152	2	0,091	25	0,513	1000
2,30	21000	152	1,9	0,090	25	0,536	1000
2,40	20000	151	1,8	0,090	25	0,560	1000
2,50	20000	157	1,8	0,090	25	0,583	1000
....	....	....	....	....	....	....	....
3,10	20000	195	1,8	0,090	25	0,723	800
3,175	20000	199	1,8	0,090	25	0,740	800
3,20	20000	201	0,9	0,045	25	0,211	500
3,30	20000	207	0,9	0,045	25	0,217	500
....	....	....	....	....	....	....	....

The example in Fig. 28.10 shows selected diameters to highlight some general items in a parameter table:

- The maximum spindle speed is 1,250,000 rpm. This max rpm is already required at a drilling diameter of 0.35 mm,

resulting in a cutting speed of 137 m/min and with that deviating from the targeted 150 m/min for this and smaller diameters. If a spindle with a max rpm of 160,000 was used, the targeted cutting speed of 150 m/min would be achieved until 0.3 mm.

- The minimum spindle speed is 20,000 rpm. This min rpm is already reached at a drilling diameter of 2.4 mm, resulting in a cutting speed deviation from the targeted 150 m/min for bigger diameters.
- The fact that for diameters bigger than the shank diameter (3.175 mm) the point angle changes from 130 to 165° (also visible on the individual z), requires a reduced infeed.
- The inconsistency of the cutting speed in the diameter range 2.2 to 2.4 mm is due to the fact that the rpm's are rounded (up or down) to thousands.

28.4.7 Stack Clearance Height

28.4.7.1 Definition. Stack clearance height is the distance between the point of the drill and the surface of the stack at the top of the drill stroke. Maintain a minimum stack clearance distance of ⅛ in (0.125 in), which implies a space between the bottom of the pressure foot and the top of the stack of 0.075 in, assuming the pressure foot lead distance to the point of the drill is correctly set at 0.050 in. Stack clearance may be adjusted for each load by simply sliding a 0.075-in shim between the pressure foot and the stack and adjusting the upper limit until the pressure foot touches the shim.

28.4.7.2 Effects. The less the stack clearance distance between the drill point and the top of the stack, the shorter the drill stroke and therefore the shorter the processing time per load. Increasing the stack clearance distance allows

more time between drill strokes and gives the tool table more time to settle, which may improve hole registration accuracy and prevent small-diameter drill bit breakage. In addition, the greater the time between drill strokes, the more likely drilling debris will be removed from the drill flutes and, consequently, the lower the drilling temperatures, which results in reduced occurrences of drill breakage and lower extents of drilled hole quality defects. On some machine controls can different heights be defined. This is done based on the location of the hole (to avoid damage of the spindle, when passing alignment pins). With that can the retraction height be very small for economic drilling and only selectively be increased to avoid damage.

28.4.8 Drilled Stack Height

Material construction (panel thickness, number of copper layers, laminate type, etc.), drill bit diameter, and flute length, as well as hole quality and registration accuracy requirements, all are factors that need to be considered when deciding on appropriate drilled stack heights. A greater number of panels in the drilled stack means higher drilling temperatures, accelerated drill wear, and greater drill deflection, affecting the resulting hole quality and registration accuracy. When using smaller-diameter drill bits, stack heights need to be reduced to prevent drill breakage and to accommodate the shorter flute lengths. As a rule of thumb, the maximum total drilled depth (number of panels × panel thickness + entry thickness + backup penetration depth) that can safely be handled by the drill bit without breakage is approximately 17 times its diameter. When the stack height is determined, an additional “safety” in the flute length should be considered to allow debris removal during and in between the strokes (see Fig. 28.11).

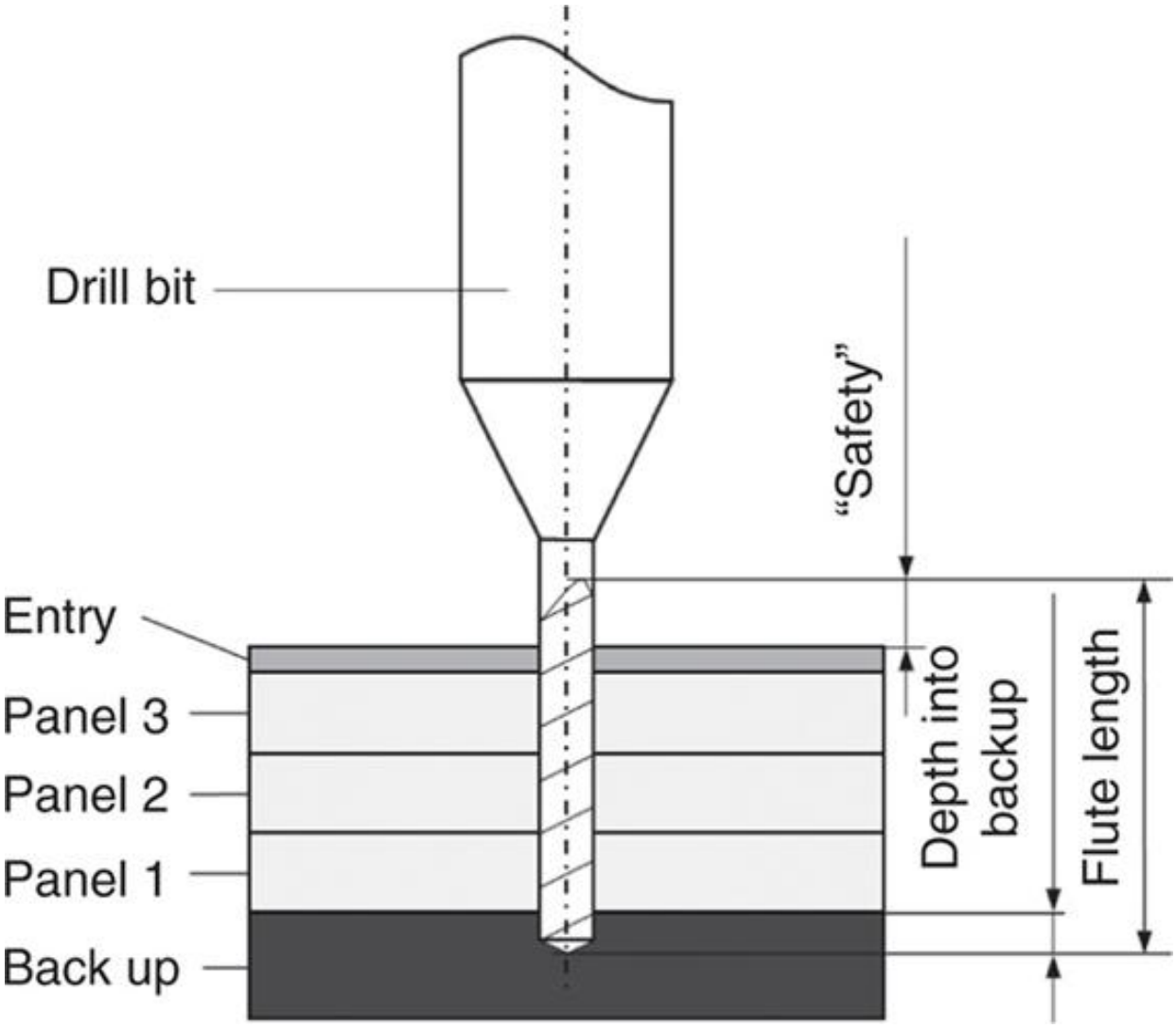


FIGURE 28.11 Drill stack.

28.4.9 Stacking and Pinning

***28.4.9.1 Building the Stack*.** Inspect all laminate panels and the entry and backup materials for surface damage and remove burrs from the panel edges as well as from the pinning holes. Even though the registration tooling holes on the laminate material may not be used to pin the stacked panels together, it is important to remove any resin buildup remaining around these holes after lamination (a common occurrence). Burrs and raised surface areas do not permit

the panels to lay flat, causing gaps resulting in drilled hole registration problems, burrs, hole quality defects, and drill breakage. Reject entry and backup materials with excessive nicks, scratches, and other surface defects as well as those that are warped or twisted.

28.4.9.2 Pinning Procedures. Wipe the surfaces of all laminate panels and the backup material using a lint-free cloth to remove any debris before stacking the panels (allowing intimate contact between the stacked panels). Verify that the pinning holes and pin insertion are perpendicular to the stack and avoid using pins that are damaged or deformed.

28.4.9.3 Installation. Before placing the pinned stacks onto the drilling machine tool table, inspect the surface for burrs or broken drill bits protruding from the table that may prevent the stacks from lying flat. Do not continue if the pin bushings of the tool table are sunken or worn to the point that they do not hold the stack firmly in place. Loose or sunken tooling pin bushings cause movement of the stack during drilling and result in a variety of hole defects, registration problems, and drill breakage, yet are simple to replace at a minimum cost. After stacks are put in place, again wipe the surface of the top laminate material as well as the entry material. Place the entry material on top of the stack and tape it in place. The entry material size should be such that it clears the pins and does not extend beyond the stack edges. Pinning the entry material to the stack is not recommended because it tends to constrict the movement of the material, causing separation between it and the stack and resulting in entry burrs and possible drill breakage.

28.4.10 Backdrilling

29.4.10.1 Definition. Back drilling is an additional blind via drilling step to improve the electrical signal of the circuits at high frequencies, by removing that part of the copper barrel which is irrelevant for the electrical functionality. The fact that this blind via drilling step initially was performed from the bottom side or back side of the board gave this operation the name. Meanwhile it's misleading as back drilling is also performed from the top or front side.

28.4.10.2 Effects. For example (see Fig. 28.12), a product with 10 layers of copper with areas on which the signal travels in the hole only from layer 1 to layer 4. In this case is the barrel between layer 5 to 10 electrically irrelevant or unused and basically only required to achieve the minimum thickness of plated copper in the hole (as the aspect ratio for such a blind via is too high). If this part of the barrel is not removed, reflections and interactions with pulled back copper layers (parasitic capacitances) distort the signal causing losses at high frequencies. The challenge for this drilling step is to come as close as possible to the layer carrying the signal (in the example layer 4), but without violating it. This layer is also referred to as "must-not-cut-layer" in specifications. The distance of the remaining copper barrel to the "must-not-cut-layer" is called "stub." Even though the machine drilling capability in the *z* axis is within a couple of µm is it required to consider several product and process tolerances of the PCB increasing the stub in cases where all tolerances add up. Typically also a minimum drilling depth is specified in relation to a copper layer. This layer is called the "must-cut-layer."

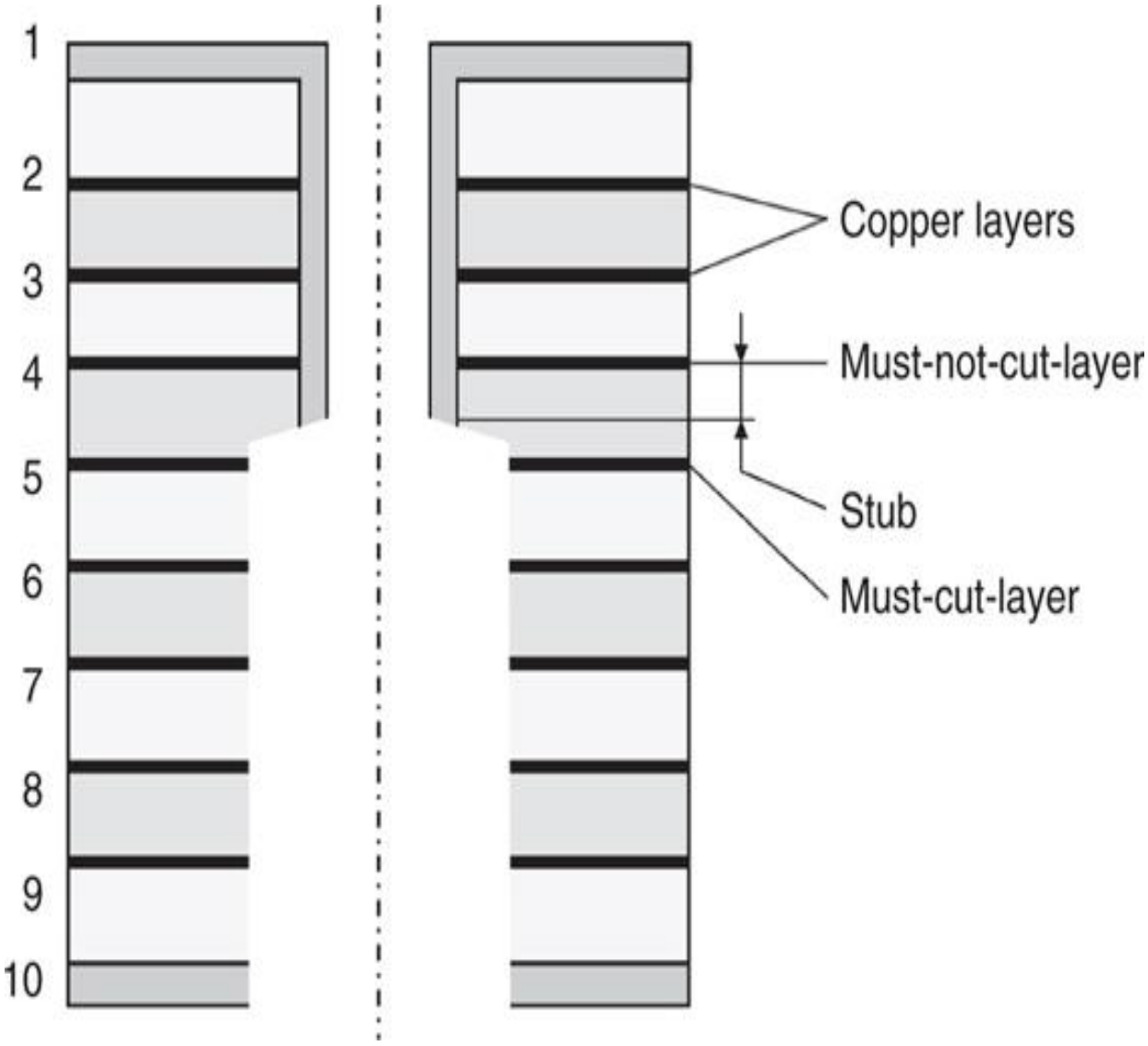


FIGURE 28.12 Back drilling from layer 10 to layer 4 (must-not-cut).

28.5 HOLE QUALITY

28.5.1 Definition of Terms

The terms in Tables 28.1 and 28.2 are commonly used to describe drilled hole defects observed on copper and substrate surfaces. It is important to be able to identify these defects specifically rather than in general terms. Using a general term such as *roughness* may imply voids or plowing.

While voids are a mechanical type of defect, plowing is a heat-related type of defect. Therefore, excessive voids would lead one to examine the chip load (infeed rate) used; plowing would lead one to look at surface speed (spindle speed).

TABLE 28.1 Copper Defects

Defect	Definition	Type
Burr	Ridge left on external surface	Mechanical
Debris	Drilling residues	Mechanical
Delamination	Separation of the copper from the substrate	Mechanical/heat-related
Nail-heading	Burr on internal copper layer	Mechanical/heat-related
Smearing	Thermomechanically bonded resin deposit	Heat-related

TABLE 28.2 Substrate Defects

Defect	Definition	Type
Debris pack	Drilling residues packed into voids	Mechanical
Delamination	Separation of the substrate layers	Mechanical/heat-related
Loose fibers	Unsupported fibers in the hole wall	Mechanical
Plowing	Furrows in the resin	Heat-related
Smear	Thermomechanically bonded resin deposit	Heat-related
Voids	Cavities due to torn-out supporting fibers	Mechanical

28.5.2 Examples of Drilled Hole Defects

Examples of typical drilled hole wall defects are shown in Figs. 28.13 and 28.14.

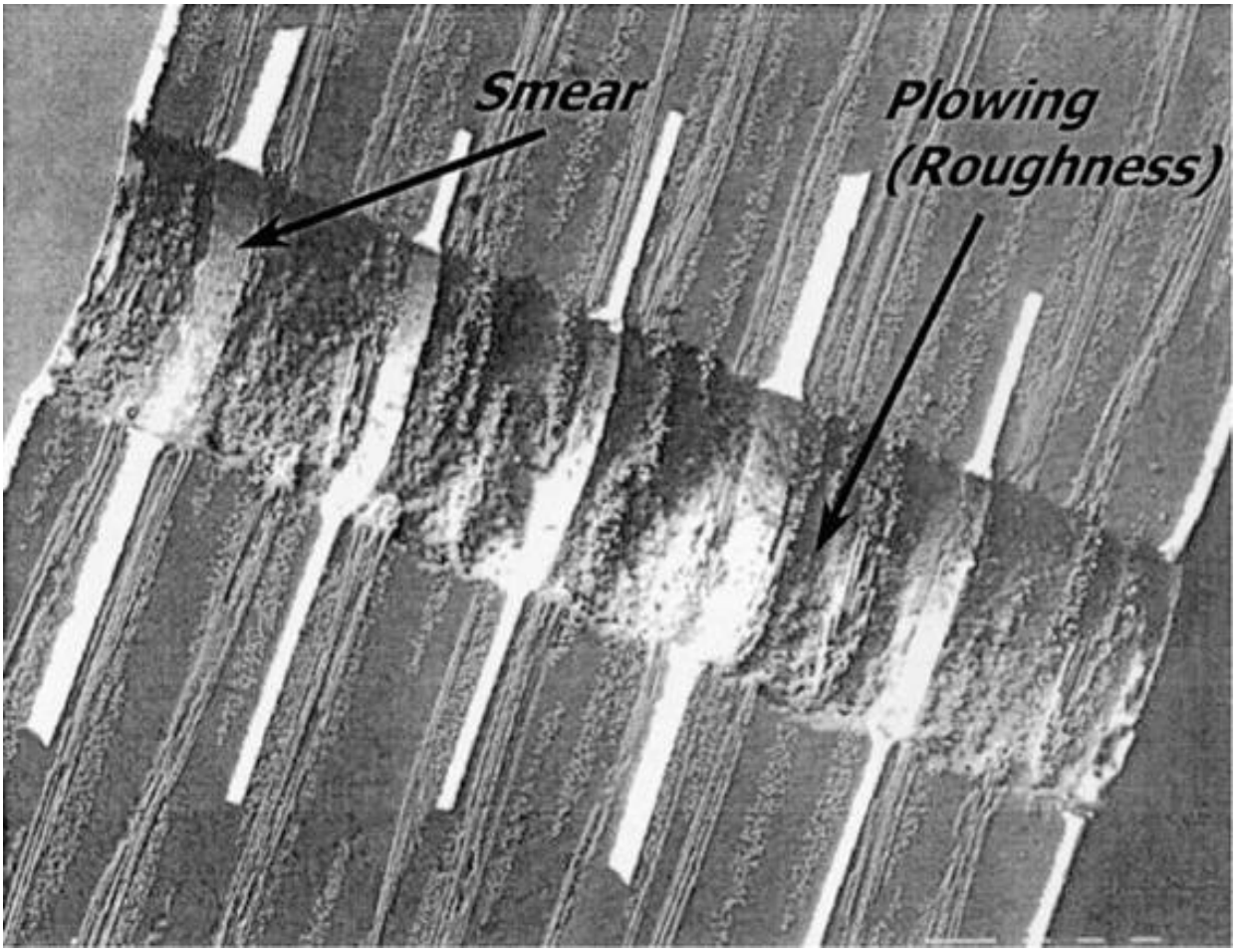


FIGURE 28.13 Cross-section of drilled hole showing.

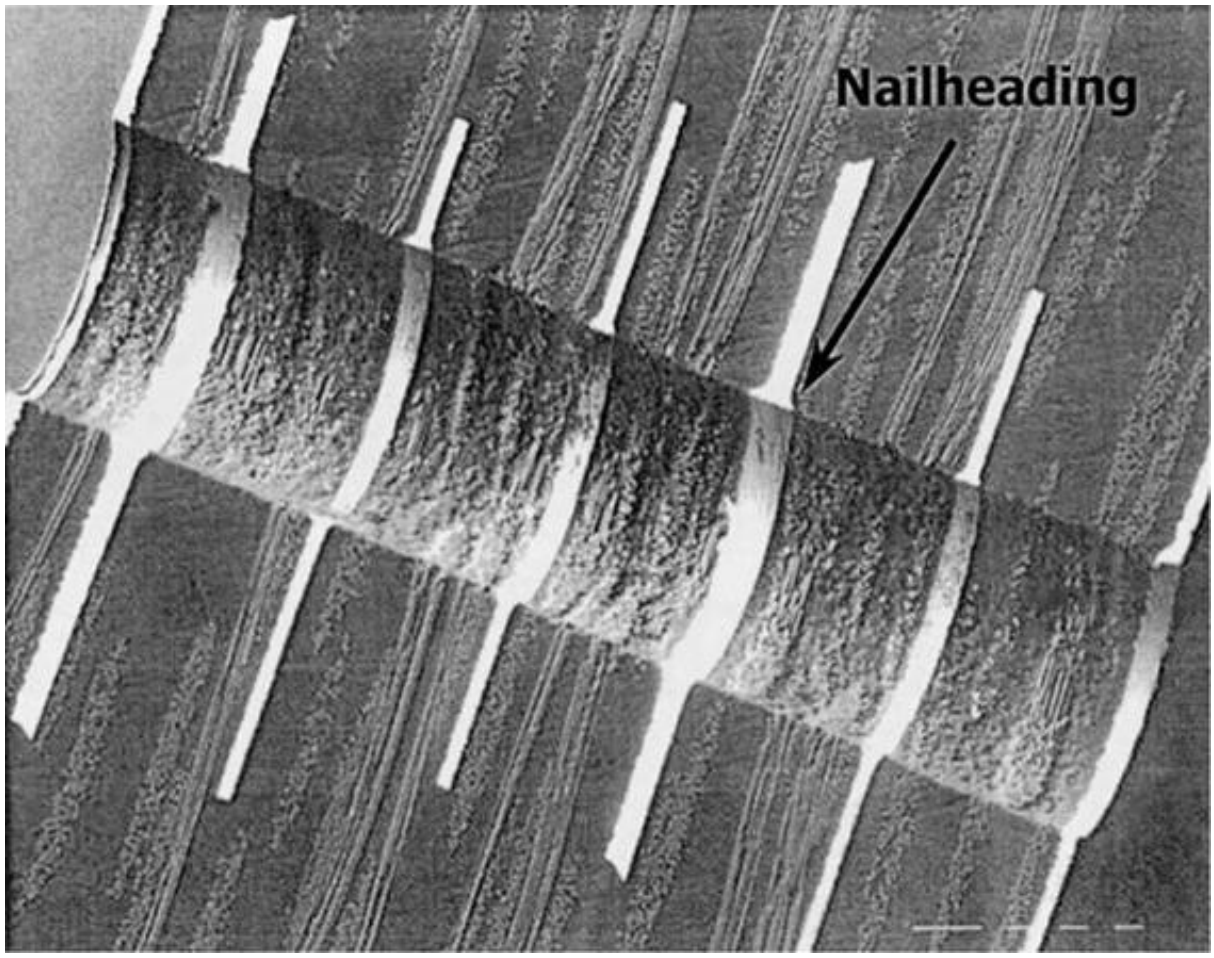
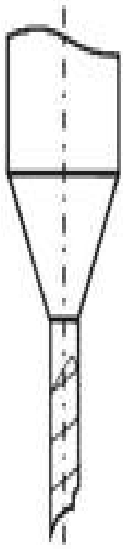


FIGURE 28.14 Cross-section of drilled hole show examples of smearing and plowing of nail-heading.

28.6 TROUBLESHOOTING

Drill bit breakage/ broken drill bits



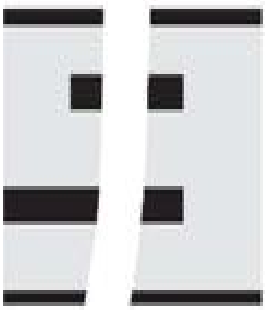
Insufficient flute length:
- Stack too high/flute length too short
- Drilling depth into backup too deep

Wrong drilling parameters/cutting pressure too high:
- Spindle speed/cutting speed too low
- Infeed rate too high
- Retract rate too high

Pressure foot:
- Pressure too low
- Wrong timing between pressure foot and vacuum (down too late/up too early)

Excessive wear:
- Hit count too high
- Damaged/chipped edges
- Spindle run out (tolerance too high)

Drill wander/drill bit deflection



Poor entry material quality
- Inclusions
- Scratches
- Burr on pressure foot => indentions/scratches

Excessive wear:
- Hit count too high
- Damaged/chipped edges

Flute length too long

Spindle run out (tolerance too high)

Debris between entry material and top panel

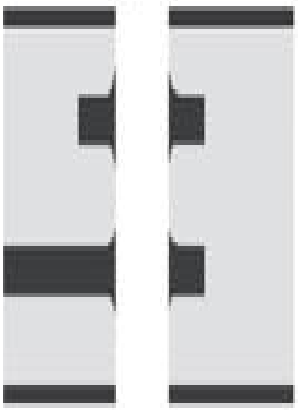
Pressure foot
- Pressure too low
- Wrong timing between vacuum and pressure foot (down too late/up too early)

Misregistration[1]

Alignment system:

- Alignment holes offset, holes too big
- Pins: improper insertion, pins too small
- Improper clamping system

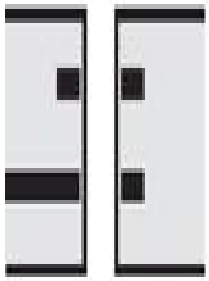
Nail heading



Excessive wear:

- Hit count too high
- Damaged/chipped edges
- Drilling depth into backup too deep
- Spindle speed too high

Smear



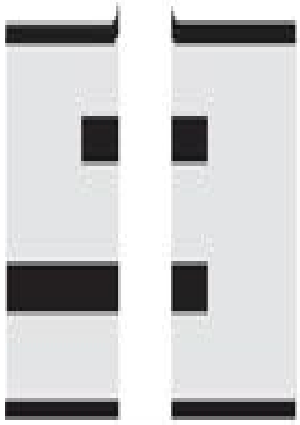
Excessive heat generation:

- Spindle/cutting speed too high
- Infeed too low
- Chip load too low

Material/prepregs not properly cured

(Inefficient desmearing process; depending on if the smear is detected prior or after the desmearing process.)

Burr (entry side)



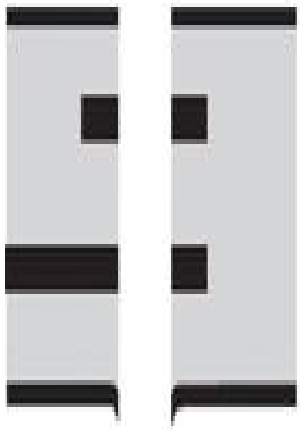
Excessive infeed rate or retract rate

No entry material or entry material too soft

Pressure foot:

- Pressure too low
- Defect

Burr (exit side)



Excessive infeed rate or retract rate

Excessive wear:

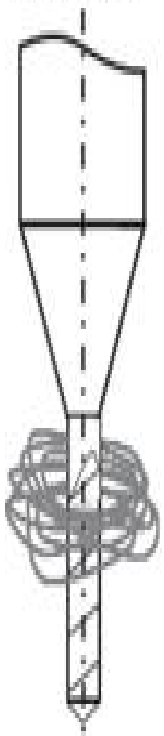
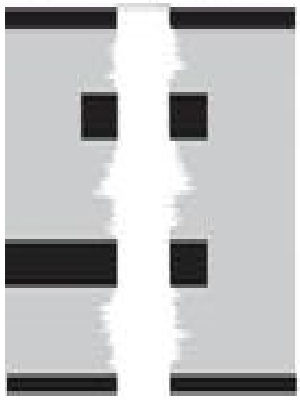
- Hit count too high
- Damaged/chipped edges

Warped panels

Pressure of pressure foot too low

Backup material:

- Too soft
- Off contact: debris between panels and backup

Bird nesting 	Chip load too low: • Infeed too low • Spindle speed/cutting speed too high No chip breakers tools (for big diameters) No step drilling/pulse drilling for "high copper" products
Hole wall roughness 	Excessive wear: • Hit count too high • Damaged/chipped edges Chip load too high: • Spindle speed/cutting speed too low • Infeed too high
Haloing (delaminations/cracks in resin on exit side)	See burr on exit side No contact between exit side and backup material, e.g., when drilling after etching or at "routing"/cut out process step

[1]Detected at the drilling department; at AOI are additional influences like misregistration of the imaging process and "overetching" reducing the annular ring and making any drill wonder/deflection or misalignment appear worse than it actually is.

28.7 POSTDRILLING INSPECTION

A wealth of information is available by simply examining the materials from the drilled stack and the drill bits. For instance, inspecting the drill bits will allow one to determine if wear occurs at consistent rates (for drills of same diameter) or will reveal whether hit count maximums are excessive and the type of drilled hole wall defects to expect. Bonded debris and/or extensive wear to the drill corners imply high drilling temperatures (resulting in greater extents of defects such as smearing and plowing) or materials that are not fully cured and point to a problem with the materials (laminate, entry, or backup) or may suggest an excessive surface speed.

Extensive primary cutting edge wear indicates abrasive materials and may require lowering stack heights, reducing hit counts, or replacing entry or backup materials.

Burrs on the surfaces within the stack mean that there is a problem with the way panels are assembled and pinned or may be the result of warped panels. Entry or exit burrs on the outer laminates should cause one to question the entry and backup materials or the infeed rate.

The point of a postdrilling inspection process is that if one takes the time on a regular basis, to examine materials and drill bits after drilling, many drilling problems would be solved before they get out of hand.

28.8 DRILLING COST PER HOLE

Material and processing costs, as well as the resulting total drilling cost, may be determined by using an analysis matrix such as a cost model specifically designed for this purpose and generated with the use of a computer spreadsheet

program. The advantage of using a spreadsheet is that it allows changes to be made in, for instance, specific material prices and processing times or parameters, and allows instantaneous viewing of the resulting effects on the total drilling costs, the cost per panel, and the average cost per hole. Knowing the cost per hole is important because it allows comparing different jobs or processing situations. Following is a step-by-step description of how to construct a drilling cost analysis matrix such as the one shown in Fig. 28.15. The Table demonstrates the different aspects that need to be considered and is just an example in which the actual numbers have to be entered.

TABLE A Machine Time

a	b	c	d	e	f	g	h	i	j	k
Drill bit size	Number of holes per panel	Number of drilled panels	Total number of drilled holes	Panels per drilled stack	Total number of drilled hits	Total number of drilled stacks	Stacks per machine load	Number of machine loads	Drill time per load (h)	Total machine time
0.0135	7,000	120	840,000	2	420,000	60	4	15.0	1.12	16.80
0.0160	5,000	120	600,000	2	300,000	60	4	15.0	0.80	12.00
0.0225	3,125	120	375,000	2	187,500	60	4	15.0	0.48	7.20
0.0350	1,500	120	180,000	2	90,000	60	4	15.0	0.19	2.85
0.0520	800	120	96,000	2	48,000	60	4	15.0	0.10	1.50
0.0700	250	120	30,000	2	15,000	60	4	15.0	0.04	0.60
	17,675		2,121,000						2.73	40.95

TABLE B Drill Bits

l	m	n	o	p	q	r	s	t	u	v
Drill bit size	Cost per new tool	Cost per repoint	Number of repoints per tool	Total cost per drill bit life	Number of uses per drill bit life	Average cost per drill bit use	Total number of drilled hits	Number of hits per drill bit use	Total number of drill bit uses	Total drill bit cost
0.0135	$1.25	$0.25	2	$1.75	3	$0.58	420,000	1,000	420.0	$245.00
0.0160	$1.20	$0.25	2	$1.70	3	$0.57	300,000	1,000	300.0	$170.00
0.0225	$1.15	$0.25	3	$1.90	4	$0.48	187,500	1,250	150.0	$71.25
0.0350	$1.15	$0.25	3	$1.90	4	$0.48	90,000	1,500	60.0	$28.50
0.0520	$1.15	$0.25	4	$2.15	5	$0.43	48,000	2,000	28.0	$10.32
0.0700	$1.30	$0.25	4	$2.30	5	$0.46	15,000	2,500	6.0	$2.76
										$527.83

TABLE C Entry and Backup Material

	w	x	y	z	aa
Material type	Cost per ft^2	Stack size ft^2	Cost per stack*	Total number of drilled stacks	Total material cost
Entry material	$0.53	3.00	$1.59	60	$95.40
Backup material	$0.65	3.00	$0.98	60	$58.50
					$153.90

* Backup material = cost/2 (uses per panel)

TABLE D Labor and Burden

	ab	ac
	Cost per hour	Cost total
Labor	$15.00	$614.25
Burden	$10.00	$409.50
		$1,023.75

TABLE E Total Costs

Cost variable	Cost per panel	Total cost	% of total
Drill bits	$4.40	$527.83	30.9%
Entry material	$0.80	$95.40	5.6%
Backup material	$0.49	$58.50	3.4%
Labor	$5.12	$614.25	36.0%
Burden	$3.41	$409.50	28.0%
Total drilling cost	$14.21	$1,705.48	100.0%

TABLE F Drilling Costs

Drilling cost per panel	$14.21
Average cost per 1000 holes	$0.804

FIGURE 28.15 Drilling cost analysis matrix. (*Courtesy of LCOA Technical Center.*)

28.8.1 Machine Time

Table A in the drilling cost analysis matrix is used to calculate the total time that is required to complete the job. First, the different drill sizes (a) and their respective total drilled holes per panel (b) as well as the total number of panels (c) to be drilled are determined and entered in the spreadsheet; this allows the spreadsheet to calculate the total number of holes for each size to complete the job (d).

Second, using the appropriate drilled stack height (e), the total number of drilled stacks (g) and the total number of drilled hits per drill size (f) can be calculated. The total number of drilled hits (drill strokes) is the total number of drilled holes per panel (b) divided by the number of panels per drilled stack (e).

Third, the number of total drilled stacks (g) is divided by the number of stations per machine [stacks per load (h)] to calculate the number of machine loads (i).

Fourth, the total drill time per load required per drill size (j) is entered to calculate the total machine time for each drill size (k).

Fifth, the total times of each of the drill sizes are simply added up to arrive at the total time required to finish the job.

An option is to enter the total drill time per load instead of entering the time for each of the drill sizes and multiplying the total drill time per load by the number of machine loads to determine total machine time.

28.8.2 Drill Bits

The cost of the drill bits needed to complete the job may be determined after the average cost per drill bit use has been

calculated. To find the average cost per drill bit use, the typical number of repoints for the particular size (*o*) is multiplied by the cost of each repointing (*n*). The resulting cost, added to the new drill bit price (*m*), is the cost per drill bit life (*p*). By dividing the cost per life by the number of uses (*q*) per life (the number of times the bit is repointed + 1), you arrive at the average cost per drill bit use (*r*). Next, by dividing the total number of hits per drill size (*s*) by the number of maximum hits per drill bit use (*t*), the number of required drill bit uses (*u*) for each size may be determined. Then calculate the total cost per drill bit size (*v*) by multiplying the number of uses (*u*) by the average cost per use (*r*). The sum of the total costs of each of the drill bit sizes (*v*) brings you to the total cost of drill bits needed for the job. This cost, of course, is true only with the assumption of no drill bit breakage.

28.8.3 Entry and Backup Materials

Entry and backup material cost per stack (*y*) is determined by multiplying the stack size [square foot per panel (*x*)] by the cost per square foot. Remember to divide the backup cost by 2 since each backup panel may be used twice. Total material cost (*aa*) is calculated by multiplying cost per stack (*y*) by total number of drilled stacks (*z*).

28.8.4 Burden and Labor

Using typical burden and labor rates per hour (ab), these values are multiplied by the number of hours to complete the job (determined in Table A) in order to calculate the total burden and labor costs (ac).

28.8.5 Total Drilling Cost and Cost per Hole

After entering the required data in Tables A through D of Fig. 28.15, the total drilling cost and the cost distribution (see Table E) as well as the drilling cost per panel and the cost per hole (see Table F) can be calculated. Because the cost per hole typically ranges around 1/10 of a cent, a more accurate and easier way to comprehend this value is by showing the average cost per 1000 holes, as is done in the cost model.

28.9 ACKNOWLEDGMENT

Portions of this chapter were taken from Chap. 24, “Drilling Processes,” written by Hans Vandervelde, Laminating Company of America, for Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

[a] Significant portions of this chapter are based on “Drilling Processes,” by Hans Vandervelde, Chap. 24 in *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

CHAPTER 29
PRECISION INTERCONNECT AND LASER DRILLING[a]

Matthias Stickel
KSG Leiterplatten GmbH, Gornsdorf, Germany

29.1 INTRODUCTION

As circuit density continues to increase along with the demand for higher and higher accuracy in hole location, the drilling machines and the environment in which the machines operate must be tightly controlled to achieve success in the drilling operation.

High-density interconnect (HDI) has been defined as referring to holes with diameters of 0.006 in or less. HDI holes were generally expected to be made by nonmechanical means, such as lasers, plasma, or photoimaging. However, most holes continue to be created by mechanical means, and as the hole size approaches or in some cases decreases to less than 0.004 in, special challenges face the mechanical drilling process. With the density increase, innerlayer registration is of utmost importance. Artwork generation and fabrication processes can introduce layer shift. This shift is

particularly troublesome in high-layer-count printed circuit boards (PCBs). This chapter addresses these issues of small-hole drilling as well as laser drilling.

In this chapter, holes created by traditional mechanical drilling methods are referred to as “drilled,” and the process is referred to as “drilling.” Holes created by laser, plasma, or photoimaging are not really drilled, even though the term is often used to describe them. When this chapter references nonmechanical via-hole creation processes, these are referred to by their specific type.

29.2 FACTORS AFFECTING HIGH-DENSITY DRILLING

PCB technology requires holes as small as 0.002 in (0.05 mm) to be drilled with extremely high accuracy, particularly when drilling dense hole patterns. The processes and machines used to drill these holes now constitute a highly developed science.

As the drilling process approaches these HDI dimensions, numerous factors become increasingly critical, such as:

- Hole location
- Predrilling process issues
- Drill room temperature/relative humidity
- Vacuum
- Drill bit condition
- Dynamic spindle run-out
- Backup and entry material (type and thickness)
- Maximum spindle speed
- Depth control

29.3 LASER VERSUS MECHANICAL

Although it is somewhat subjective, the decision to drill with mechanical or laser systems can be influenced by the following considerations:

- *Aspect ratio determination:* If the via to be formed is more than 0.016 in (6.3 mm) deep, it is better to use a mechanical drilling process.
- *Material type:* Materials that tend to have excess smearing that clogs the flutes in a mechanical system are usually better on a hybrid laser system.
- *Size of holes:* If the hole to be drilled is larger than 0.012 in, then use a mechanical system for speed and hole wall quality.

29.3.1 Other Advantages and Benefits to Use Lasers for the Via Formation

- Very fast [>500 holes/s (up to 1000 holes/s) compared to 200 holes/min for the mechanical process]
- No “safety” required, reducing the dielectric thickness under the landing pad; while for mechanical blind vias, thickness variations have to be considered with an increased drilling depth, which requires also a greater distance under the target layer, can the parameters for CO_2 lasers be set in a way to mitigate these variations (with extra energy) because the landing copper will not be damaged, due to the fact that copper reflects certain wavelengths to a great extend
- Easy alignment to the landing IL copper on the laser machine/in the same operation

- Ability to form dual-diameter holes (“telescope vias”) when going through multiple layers

29.3.2 Lasers for PCB Processing

Several types of lasers can be used to fabricate PCBs (solid state and gas), including:

- Infrared (IR) (CO_2) lasers (9.4 to 10.6 µm)
- Ultraviolet (UV) lasers for PCB (solid-state)
  - Nd:YAG (Neodymium-doped Yttrium-Aluminum-Garnet)
  - Yb:YAG (Ytterbium-doped Yttrium-Aluminum-Garnet)
  - Nd:YVO_4 (Neodymium-doped Yttrium-Vanadate)
  - Nd:YLF (Neodymium-doped Yttrium-Lithium-Fluoride)

In solid-state lasers is the beam delivery from the source to the working optics done with optical waveguides or with mirrors. The (fundamental) wavelength is typically in a range of 1030 to 1070 nm.

See Fig. 29.1 for diagram of laser wavelengths by type.

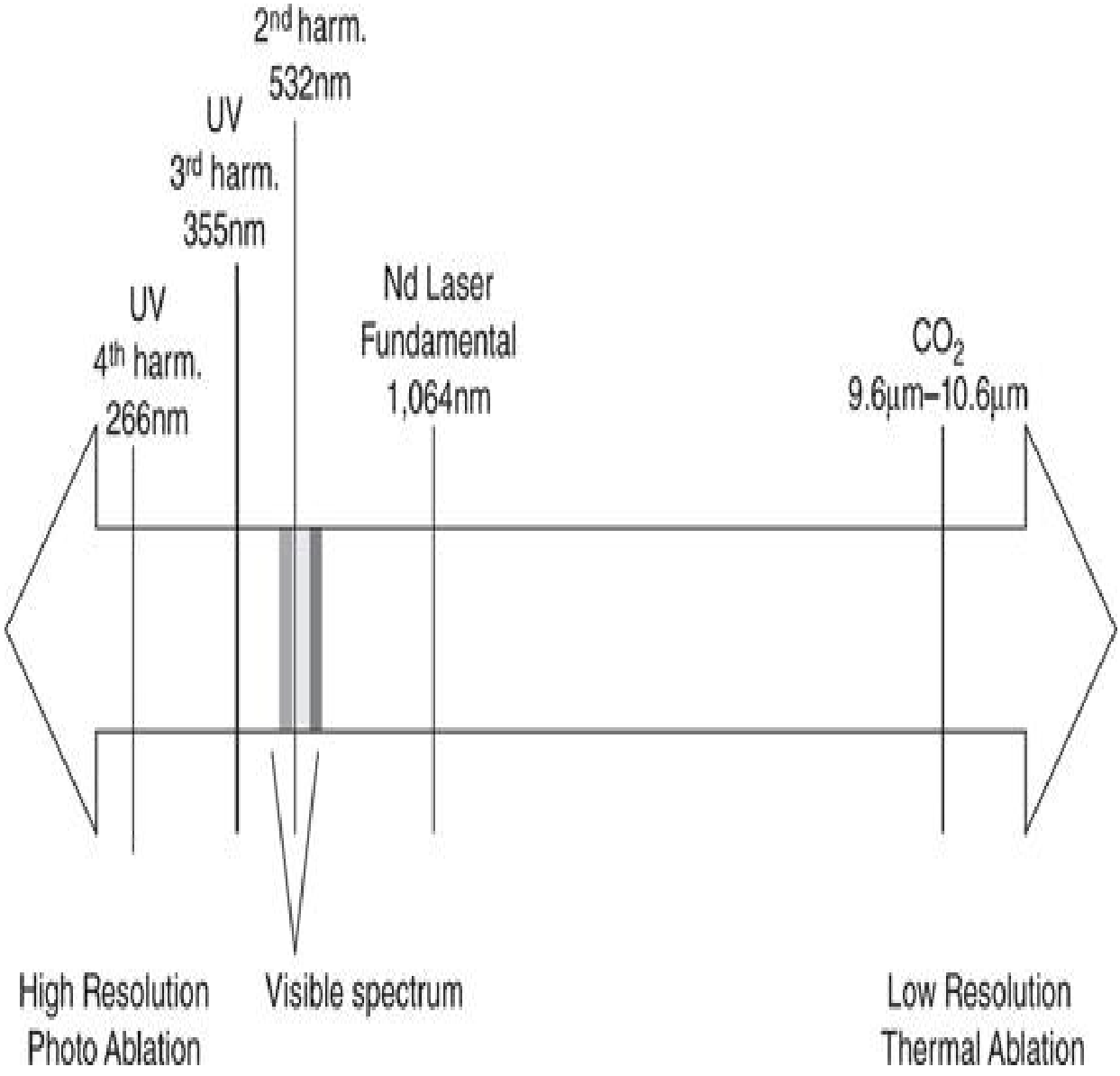


FIGURE 29.1 Laser wavelength by type.

29.3.3 Beam Delivery

Laser source outputs a collimated beam. Turning mirrors (see Fig. 29.2) guide the beam to the scanners. The attenuator is used to control UV beam power. Scanners move the beam on the worktable. The lens focuses the beam to the worktable.

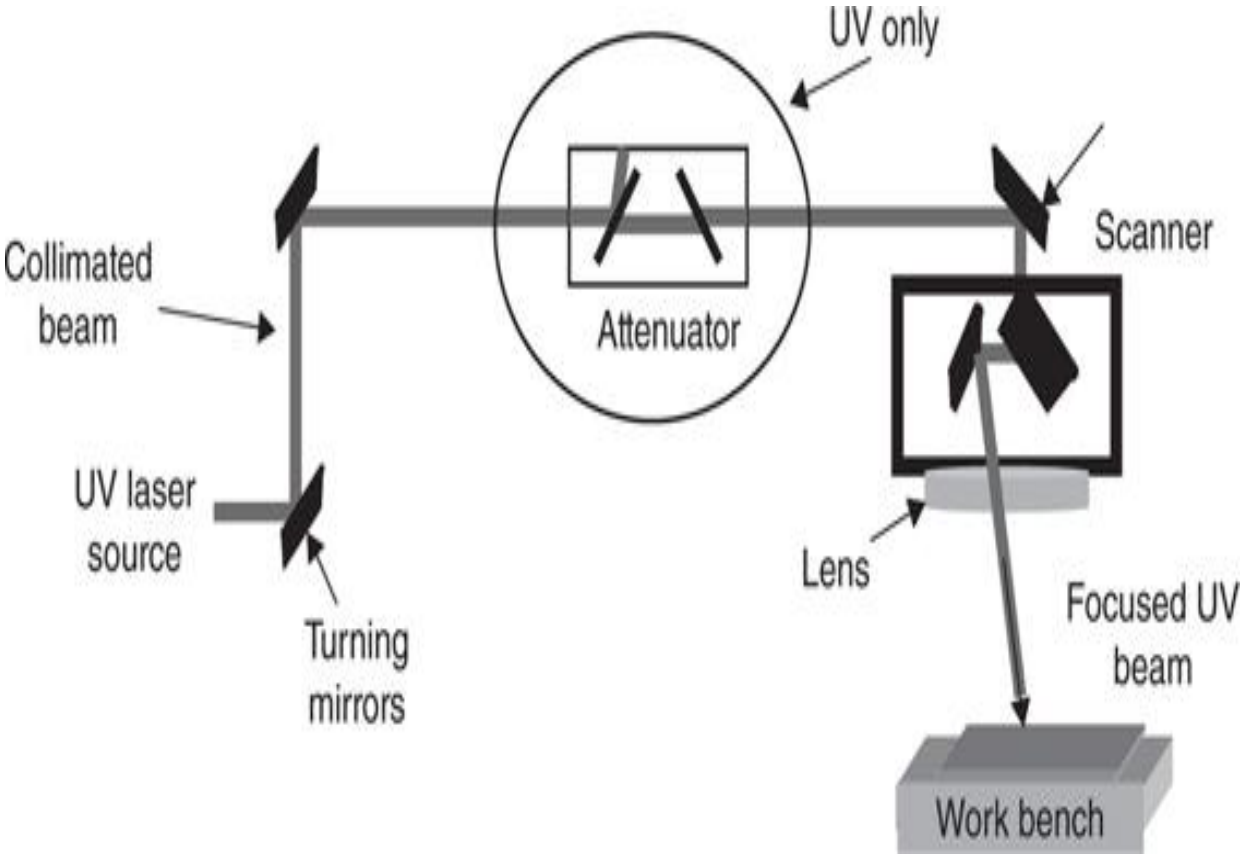


FIGURE 29.2 Laser beam delivery.

29.3.4 IR (CO_2) Drilling

IR drilling requires the following:

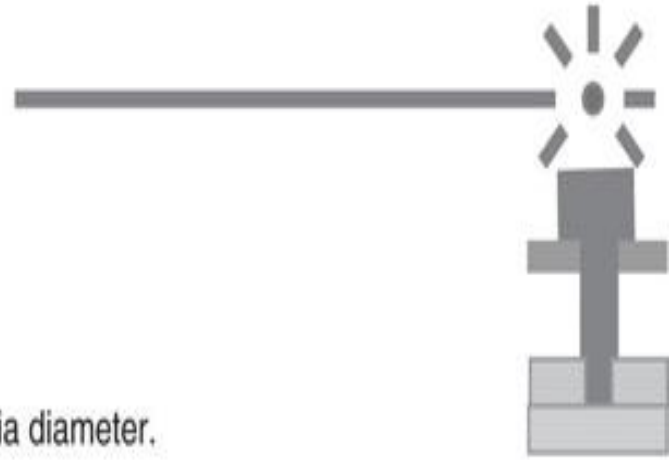
- *Thermal ablation*: This ablation requires heating, melting, and vaporizing. CO_2 IR wavelengths are reflected by copper.
- *Large focus diameter:* The focus should be ~200 mm.
- *Larger beam size*: The beam is adjustable through defocusing or apertures.
- *Percussion drilling:* Each pulse removes a portion of dielectric material.
- *High dielectric removal rate:* Scanner speed limits throughput.

- *Postprocess clean:* A desmear process is required.

See Fig. 29.3 for an overview of the CO_2 process.

Conformal mask processing

A mask of holes made by drilling, etching, or laser-ablating the top layer of copper. CO_2 is used for dielectric removal and a high ablation rate.



Direct dielectric drilling

No copper layer is required.
The mask in the laser beam defines the via diameter.

Via formation with CO_2 only

The copper layer is etched and oxidized.
CO_2 is used for copper and dielectric.

FIGURE 29.3 CO_2 process overview.

29.3.5 UV Drilling

UV drilling requires the following:

- *Photo ablation:* This process breaks molecular bonds. Minimal heat damage is inflicted on the surrounding area.
- *Precise cutting:* The small focus diameter should be ~20 mm.
- *Percussion drilling:* The hole diameter must be the same as the focus diameter.
- *Trepanned drilling:* The hole diameter must be greater than the focus diameter.

UV light is absorbed well by most PCB materials, but each material absorbs at a different rate.

29.3.6 Creating Board Elements with Lasers

Vias are created by having the laser beam make concentric circles or spiraled cuts. Laser pulse trains can be used to create vias or lines. Hole desmear can also be done by laser.

29.3.7 UV Lasers

29.3.7.1 Yitrium-Aluminum-Garnet

- The output pulse is ~120 ns.
- Yitrium-Aluminum-Garnet (YAG) was first used for laser PCB drilling.
- It provides high-pulse energy.

29.3.7.2 Yitrium-Vanadate

- Yitrium-Vanadate's (YVO_4) output pulse is ~20 ns.
- Its repetition rate is ~100 kHz.
- Currently YVO_4 is most commonly used for PCB drilling.

29.3.7.3 Yitrium-Lithium-Fluoride

- The output pulse is ~50 ns.
- Yitrium-Lithium-Fluoride (YFL) is more efficient, providing five times the absorption coefficient of YAG at the pump wavelength.

29.3.8 Hybrid Lasers (UV and CO_2)

Figure 29.4 shows a flow of the use of hybrid lasers for via formation. This hybrid is the combined use of CO_2 and UV laser technology.

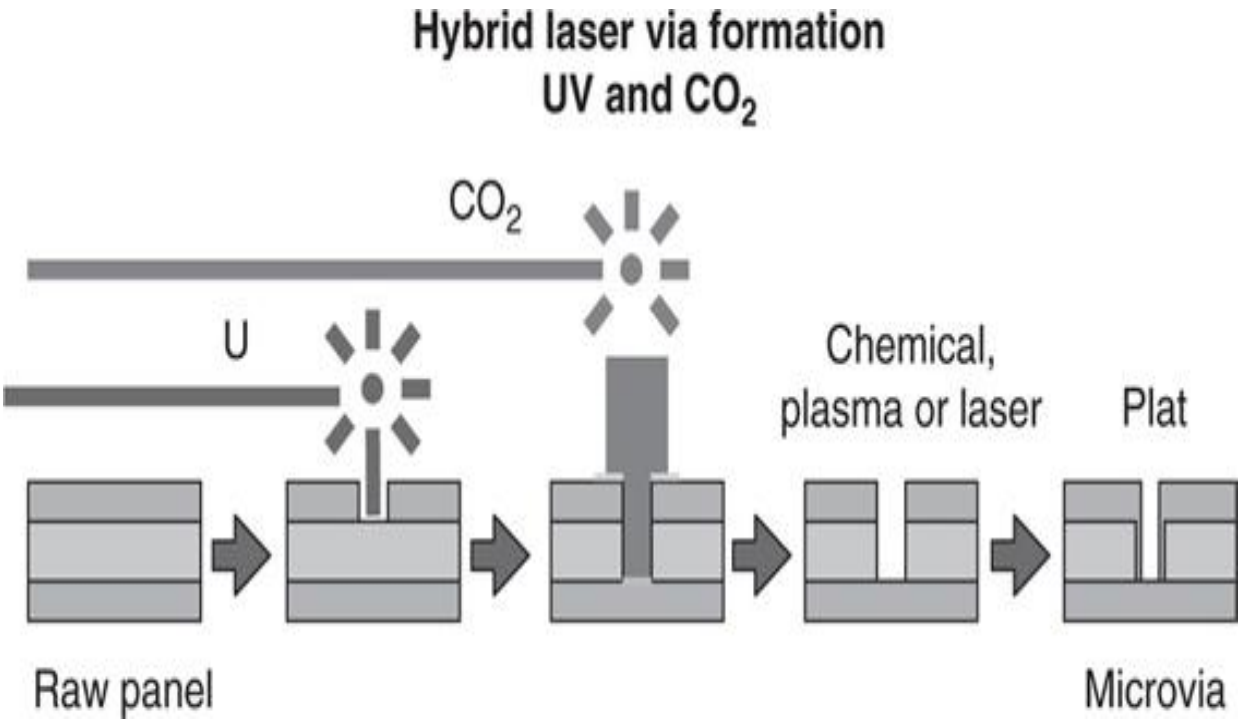


FIGURE 29.4 Hybrid laser via formation using UV and CO_2 lasers.

29.4 FACTORS AFFECTING HIGH-DENSITY MECHANICAL DRILLING

The following are factors to be considered regarding mechanical drilling.

29.4.1 Positioning/Hole Location

The positioning system for conventional drilling machines consists of *x, y*, and *z* axes. The *x* and *y* axes refer to the position of the circuit board under the drill spindle, and the *z* axis to the plunging and retracting motions that allow the drill spindle to feed the drill bit into the substrate material. Machine accuracy is defined by the machine's ability to position the table under the spindles to the desired programmed *x* and *y* values. All process variables, such as tool design, stack height, feeds and speeds, and tooling methods, must be eliminated to evaluate machine accuracy.

The stability of the machine is critical when microdrilling dense drill patterns. When the drilling system is designed, stability is one of the most important factors taken into consideration. The foundation or base of the machine is usually constructed of granite or similar material. Granite is typically used because of its mass and low coefficient of thermal expansion (CTE) to temperature fluctuation. The upper structure of the machine is designed with a high natural frequency, which allows the structure to stabilize quickly, reducing the time the machine must pause before making a rapid movement to the next hole location.

Vibration caused by forces such as punch presses, drilling machines operating in close proximity, or any other type of

equipment capable of causing severe vibration can have a detrimental effect on HDI drilling, such as drill bit breakage and hole mislocation. Each drilling machine should be isolated from these forces as thoroughly as possible. The ideal solution is to have each drill machine placed on its own isolated pad made of reinforced concrete. This setup serves to isolate the drill machine from a large percentage of the vibration transmitted through the shop floor.

29.4.2 Drill Room Temperature and Relative Humidity

All materials have coefficients that, because of the precision required, are critically important to the operation of drilling machines. Temperature has a profound impact on the accuracy of the drilling machines. With changes in ambient temperature, the materials used to build the machines may expand or contract, changing the position of the drilled hole in the PCB.

Keeping a consistent room temperature is essential for maintaining accurate positioning of the machine. A stable temperature throughout the PCB process assists in decreasing the amount of potential growth and contraction of the substrate materials. The drill room should be kept at a constant temperature and humidity, typically 72 ± 2°F (22 ± 1.1°C) and 45 to 60 percent humidity.

29.4.3 Vacuum

Sufficient vacuum flow is imperative when drilling high-aspect-ratio holes in tightly drilled grids. The vacuum system serves two main purposes:

1. To extract debris from the drilling surface

2. To keep the tool cool by removing the debris, thus decreasing the amount of friction in the hole wall

Insufficient vacuum flow leads to hole wall quality problems such as gouging, nail heading, and excessive smearing

There are numerous applications such as high-aspect-ratio drilling that require an increased amount of vacuum pressure to remove debris sufficiently, and the equipment manufacturer can provide specific guidelines for special situations. Increasing the *z*-stroke distance between the pressure foot insert and the top of the drilled stack also assists in cooling the drill bit.

29.4.4 Drill Bit

Drill bits (called *tools*) are critical in the drilling process. A wide variety of tools are available and your tool vendor can be very helpful with selecting feeds and speeds. Be sure to try several vendors to find the best tools for your particular process.

29.4.5 Drill Bit Condition

The condition of the used drill bit is a key indicator of the control and capability of the drilling process and provides an indication of the condition of the drilled hole wall. A wealth of process information can be extracted from the used drill bit. Examining drills before the repointing process can be a warning indicator of drilling problems in a real-time mode soon after the process has been affected.

Drill machine operators and drill bit resharpeners should regularly evaluate the condition of used drill bits and report the findings to the process engineers. The areas of greatest concern when evaluating the condition of used drill bits are

- Excessive margin wear
- Large amounts of burned substrate material attached to the relief areas
- Chips in the primary cutting edges of the tools

When tracked over time, this information can help alert the engineering team of any sudden changes in the drilling process. Although the used drill bit condition information is subjective, with properly trained personnel it can serve as a key indicator of the level of hole wall quality.

29.4.6 Dynamic Spindle Run-Out

The spindle houses the collet, which holds the drill bit that produces the hole in the PCB. Modern spindles are capable of running at a wide range of rpm (15,000 to 300,000) with a power rating near one horsepower (1 hp). Due to the accuracy required when drilling with small drill bits, the drill bit must run true in the spindle. Excessive spindle run-out causes the drill bit to rotate eccentrically, which leads to inaccurate hole location, drill bit breakage, and hole wall quality problems.

The spindle run-out must not exceed 0.002 in (0.005 mm) total indicated run-out (TIR) in a static situation. This trueness is achieved by using electrically powered spindles that rotate by the means of air bearings rather than mechanical ball bearings.

Other factors, such as poor collet condition and adjustment, can also lead to excessive run-out. Frequent collet cleaning and adjustment are necessary to ensure accurate mechanical hole location. Some modern drill machines are equipped with a tool metrology gauge (TMG). This feature measures the run-out for each drill bit during the tool change process, and if the run-out value measures over the predefined range, the tool is rejected. TMGs can help

increase productivity and quality by identifying potential problems before they occur.

29.4.7 Spindle Speed

As via holes get smaller and smaller, maintaining an adequate cutting speed is essential, particularly with chip loads exceeding 0.001 in per revolution. Increased spindle speed also allows for higher productivity because it corresponds to maintaining consistent chip load values while increasing *z*-axis feed rates. Spindle speed settings control the rotation of the drill bit during the drilling cycle. Measured in revolutions per minute, speed impacts hole wall quality as well as the condition of the drill bit's cutting edge. Excessive spindle speeds can result in premature wear on the cutting edges of the drill bit and may clog the margin relief area of the tool with burnt substrate (see Table 29.1). Spindle speeds are dependent on the process and the application. The maximum spindle speed capability is a factor when microdrilling, particularly when the desired surface foot per minute (sfm) values are above 300. Note the maximum achievable sfm for the microdrilling diameter range when utilizing the 180,000 rpm parameters for FR-4 material listed in Table 29.1. When the maximum allowable spindle speed is increased to 180,000 rpm, the 300 sfm value can be achieved when microdrilling, as shown in Table 29.1. As the table indicates, the upper spindle speed range accommodates microdiameter drill bits. Table 29.2 shows spindle parameters for FR-4 materials at various spindle speeds.

TABLE 29.1 Spindle Parameters for FR-4 Materials at 180,000 rpm

Spindle Speed 180,000 rpm Desired Cutting Speed: 500 sfm				
Tool Size (inch)	Infeed Rate (in/min)	Spindle speed (rpm)	Chip Load	sfm
.0071	077	180,000	.00043	334
.0080	094	180,000	.00052	377
.0100	130	180,000	.00072	471
.0120	134	159,200	.00084	500
.0145	137	131,700	.00104	500

TABLE 29.2 Spindle Parameters for FR-4 Materials at Various Spindle Speeds

Spindle Speed 125,000 rpm Desired Cutting Speed: 500 sfm				
Tool Size (inch)	Infeed Rate (in/min)	Spindle Speed (rpm)	Chip Load	sfm
.0071	054	125,000.0	.00043	232
.0080	065	125,000.0	.00052	262
.0100	090	125,000.0	.00072	327
.0120	105	125,000.0	.00084	393
.0145	130	125,000.0	.00104	474

29.4.8 Chip Load

Chip load is calculated by dividing the feed rate by the spindle speed. The term identifies the amount of penetration the drill bit completes per revolution. As commonly used, the chip load accurately describes the proper cutting action needed to drill certain applications successfully.

29.4.9 Surface Speed

The surface speed in sfm is described as the distance that the drill bit's outermost cutting edge travels in 1 min. Cutting speed is frequently used in the metal-cutting industry, and the meaning is the same in the PCB drilling process. Particular substrate materials drill and fabricate favorably at certain cutting speeds. Cutting speed should remain consistent throughout the drill range (except when limited by spindle speed capability). For general guidelines, see Table 29.3.

TABLE 29.3 General Guidelines for Cutting Speed

Cutting Speed, sfm	Material Type
200	Plastics, acrylics, soft materials
300	Teflon, Kapton
400	Polyimide, cyanate ester, BT epoxy, high-T_g laminates
500	FR-4, tetrafunctional, multifunctional multilayers
600	FR-4, difunctional rigid, double-sided

29.4.10 Retraction Rate

The *z*-axis return stroke can be programmed as well. This rate, known as *retraction*, should be set to the value that will minimize the time that the drill bit spends inside the drilled hole. The *z*-axis stability and drill bit diameter often influence the optimum retract values. An unstable or worn *z* axis can lead to poor depth control, poor hole wall quality, and high levels of drill bit breakage. Another advantage of high retraction rates is the speed of the drill stroke.

Increasing production in this case through faster drill stroking is a high priority for the PCB manufacturer. Machine technology allows the user to set retraction rates upward to 1400 in/min (35,560 mm/min).

29.5 DEPTH-CONTROLLED DRILLING METHODS

There are three common methods of depth control used in the drilling process:

- Manual through-hole drilling
- Machine depth-controlled drilling
- Controlled-penetration drilling

29.5.1 Manual Through-Hole Drilling

Manual through-hole drilling utilizes a down limit value to determine the bottom of the *z*-axis stroke. This method does not utilize the top of the stack or the top of the backing material as a reference point. Careful consideration should be given when a down limit is set. The operator needs to ensure that the drill bit is penetrating all the way through the

stack of laminated panels. Shallow penetration or incomplete holes can result in drilling scrap. Excessively deep penetration leads to increased drill bit cutting edge wear, excess debris to be removed, higher drilling temperatures, and drill bit breakage. The down limit should be set at a value that enables the drill bit to clear the point and also avoids drilling too deeply into the backing material.

29.5.2 Machine Depth-Controlled Drilling

Depth-controlled drilling utilizes the top of the drilled stack as its reference point. Before this depth-control method can be utilized mechanically, the machine needs to know what the distance is from the pressure foot insert to the tip of the drill bit.

To determine this distance, the manufacturer performs a TMG check using standard measuring devices. Once this distance is established, any negative (−) values entered into the depth box will cause the *z* axis to stop at the desired depth measured from the top of the stack.

29.5.3 Controlled-Penetration Drilling

Controlled-penetration drilling is utilized for drilling applications where the depth is referenced from the top of the backing material. This mode of depth control is not affected by stack height. The specified depth value or *z*-axis offset is treated as the desired amount of penetration relative to the top of the backing material. For the machine to be run in mode 3 depth control, a process called *mapping* must be performed prior to drilling any panels. During the

mapping cycle, the machine touches down on the surface of the backing in 2-in increments.

At each touchdown point, the thickness value of the backing is recorded. Once the mapping procedure is complete, the *z*-axis zero is established. Any negative values entered into the offset box represent the drill depth into the backing material. Controlling the penetration of the drill bit into the backing material assists in decreasing heat generation, improving hole wall quality by limiting the amount of debris, and decreasing drill bit breakage due to excessive depth.

29.6 CONTROLLED DEPTH VIA DRILLING

29.6.1 Blind Vias

29.6.1.1 Definition. Blind Vias are mechanically drilled holes which are not drilled all the way through the PCB, but only partially from one side (top or bot) to a specific innerlayer. It must be considered that the aspect ratio (ratio of the drilling diameter to the drilling depth) must be within the capability of the metallization processes. Another critical factor is that a minimum distance to the next (conductive) innerlayer under the target layer must be available to allow processing tolerances.

29.6.1.2 Effects. There are several approaches to realize blind vias:

The precision of “referencing to the table” relies on the knowledge of the location of the drill tip. This approach is mainly selected on machines using drill bits with rings, as the rings on the drill bit are set to a defined location and

with that help to reduce the tolerance given when the drill bit is picked up and set in the collet.

“Depth-controlled drilling with mechanical contact” utilizes the top of the drilled stack as its reference point. Before this depth-control method can be utilized mechanically, the machine needs to know what the distance is from the pressure foot insert to the tip of the drill bit. To determine this distance, the manufacturer performs a TMG check using standard measuring devices. Once this distance is established, any negative (−) values entered into the depth box will cause the *z* axis to stop at the desired depth measured from the top of the stack.

“Depth-controlled drilling with electrical contact” utilizes the “electrical broken drill bit detection” in which the surface of the PCB is detected with the help of an electrical signal generated when the drill bit touches the surface. A secondary measurement system is started, enabling a relative movement to the “new zero.” Especially with the introduction of linear *z* stages are very small tolerances in relation to the surface achievable, also on machines with multiple stations.

Controlled-penetration drilling is utilized for drilling applications where the depth is referenced from the top of the backing material. This mode of depth control is not affected by stack height. The specified depth value or *z*-axis offset is treated as the desired amount of penetration relative to the top of the backing material. For the machine to be run in mode 3 depth control, a process called mapping must be performed prior to drilling any panels. During the mapping cycle, the machine touches down on the surface of the backing in predefined increments. At each touchdown point, the thickness value of the backing is recorded. Once the mapping procedure is complete, the *z*-axis zero is established. Any negative values entered into the offset box represent the drill depth into the backing

material. Controlling the penetration of the drill bit into the backing material assists in decreasing heat generation, improving hole wall quality by limiting the amount of debris, and decreasing drill bit breakage due to excessive depth.

29.6.2 Peck Drilling

29.6.2.1 Definition. Peck-drilling refers to a drilling operation simulating the movement of a woodpecker, in which the hole is not drilled entirely in one step, but incrementally. The drill bit is retracted completely in between the increments, removing material in each step. This option is comparable to the generation of multiple blind vias with different levels of depth in the same location. The depth of each increment can be chosen individually, so that product or stack up specific aspects like copper weights can be considered.

29.6.2.2 Effects. The advantages of peck drilling are as follows:

- Decreased drill bit breakage
- Lower aspect-ratio values
- Improved positional accuracy/reduced deflection
- Decreased bottom-panel burring

There are different approaches for the selection of the size of the increments: linear (all the same size), progressive (getting bigger with each increment) or declining (getting smaller with each increment). Quite common is to set a small first increment, acting like predrilling and centering the drill bit for the next steps, with a total number of 3 to 5 increments. Peck drilling is typically applied when the construction of the PCB leads to an increased amount of

broken drill bits. A negative aspect (on top of longer cycle time) is that the multiple passes of drill bit on the same location of a via can lead to temperature related problems like excessive smear. The primary accomplishment of peck drilling is the decrease in effective aspect ratio value. Whereas aspect ratio is defined as the thickness of the board divided by the hole diameter, effective aspect ratio is defined as the total *z* stroke divided by the smallest drill bit diameter. For example, if the total *z* stroke equals 0.209 in (the total thickness of the board) and the smallest diameter is 0.025 in, the aspect ratio and the effective aspect ratio would have the same value of 8.36. By taking a total *z* stroke of 0.209 in and dividing it into four pecks, the aspect ratio is decreased from 8.36 to 2.08. In general terms, an aspect ratio scale of 1 through 15 is commonly used, 1 being conservative and 15 being on the aggressive side of the scale. See Fig. 29.5.

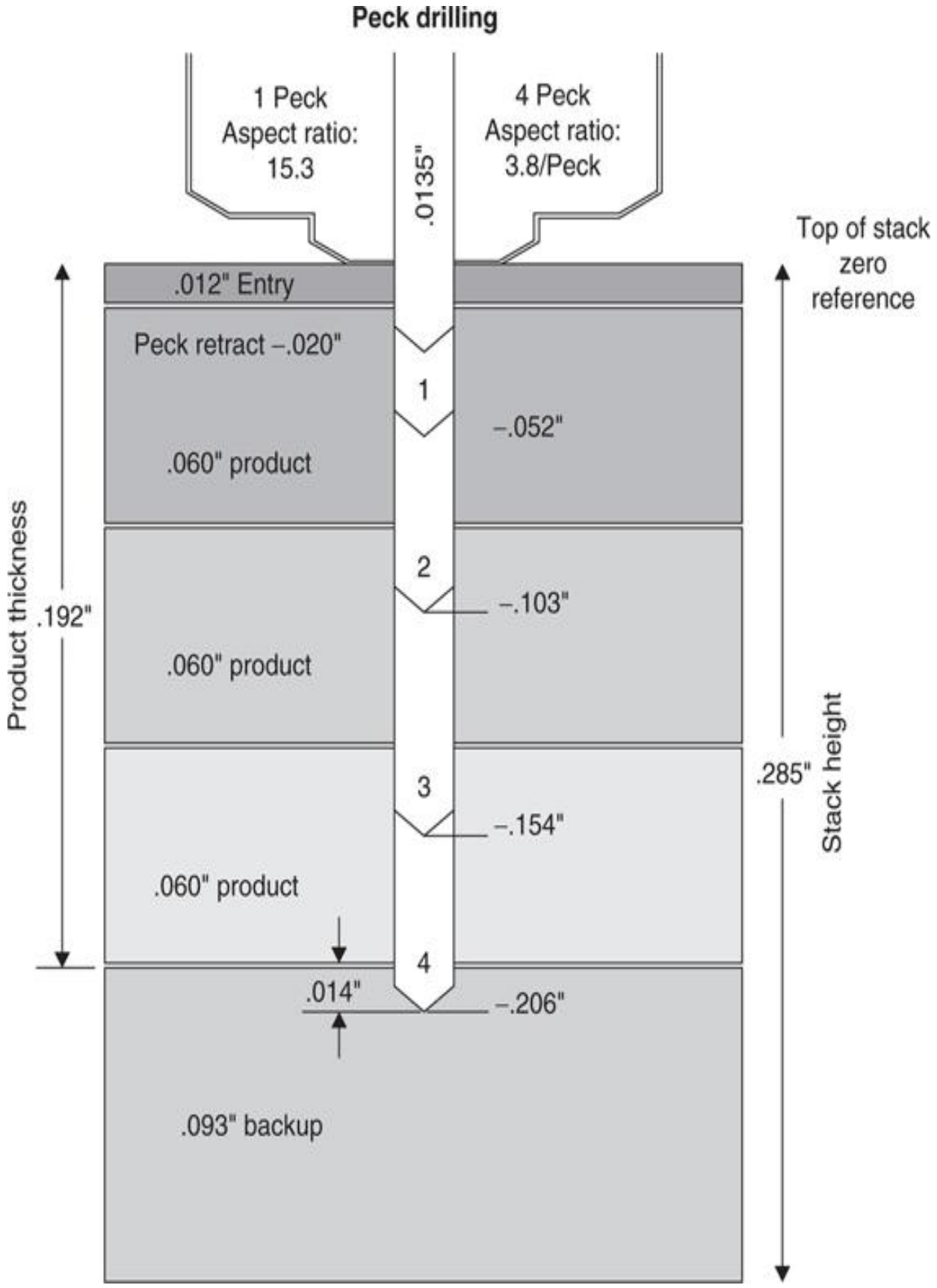

Peck drilling
1 Peck
Aspect ratio:
15.3
4 Peck
Aspect ratio:
3.8/Peck
.0135"
Top of stack
zero
reference
.012" Entry
Peck retract –.020"
1
–.052"
.060" product
Product thickness
.192"
2
–.103"
.060" product
3
–.154"
.285"
Stack height
.060" product
4
.014"
–.206"
.093" backup

FIGURE 29.5 An example of through-hole peck drilling, showing a stack of three boards with entry and backup material creating a stack height of 0.285 in and a total *z*-axis drill stroke of 0.206 in. The effective aspect ratio of 15.3 is reduced to 3.8 per peck when four pecks are made to complete the hole.

If the *z* stroke is reduced, the drill bit has less debris to extract per revolution, decreasing the chances of clogged flutes, which can cause the drill bit to seize in the hole and break.

Hole location improvement Another benefit of peck drilling is an improvement in hole location. Once a drill bit is deflected, it will continue at that deflection angle as it drills through the stack. Essentially, hole location is worse at the exit point than at the entrance point, particularly when drilling through thick panels with small-diameter tools (high aspect-ratio drilling). Peck drilling can assist in achieving better hole location by lessening the effects of deflection by dividing up the total drill stroke, therefore decreasing the effective aspect ratio value.

Bottom-panel burring Peck drilling can assist in decreasing the amount of bottom-panel burring by reducing the drilling temperatures resulting from drilling thick panels with small drill bits. Plowing, voids, and debris pack are reduced by peck drilling due to the decrease in the amount of debris the tool must extract per *z*-axis stroke.

Drill bit cooling when peck drilling, each individual stroke increment returns to the upper limit value.

The disadvantages of peck drilling are as follows:

- Increased nail heading
- Increased smearing
- Hole wall roughness
- Increased cycle times

Peck drilling increases the overall cycle time due to the greater number of *z* strokes necessary to complete one drilled hole. Nail-heading values tend to be worse for peck drilling due to the certainty that some copper pads will make contact with the drill bit several times as opposed to making only one contact when using a single drill stroke. Hole wall smearing can also be a problem when peck drilling. The increase in heat caused by drilling the same hole several times can cause the substrate material to become heated to its melting point, which can lead to deposits of resin along the hole wall. A similar effect on hole wall roughness.

Methods for reducing the negative effects on the hole wall caused by peck drilling include the following: Increasing the feed rate decreases the amount of time the drill bit spends in the hole. Minimizing the number of pecks also decreases heat generation and reduces overall drilling cycle time. The design of the tool has a major effect on hole wall quality when peck drilling. To decrease heat generation in the hole wall, the manufacturer must reduce the amount of friction caused by the drill bit making contact with the hole wall. To accomplish this reduced friction, the manufacturer can use an undercut tool design, sometimes referred to as a headed drill bit. The undercut tool design decreases the amount of contact by reducing the diameter of the tool, which creates a larger clearance area, consequently decreasing the amount of flute making contact with the hole wall. The undercut tool design reduces the amount of nail heading and smearing caused by peck drilling.

29.6.3 Slot Drilling

29.6.3.1 Definition. Slots can be realized on drilling machines without routing spindles or routing options, by placing multiple holes in the same area forming the final shape of a slot.

29.6.3.2 Effects. There are two ways to “slot drill.” The first one is setting one hole in a predefined overlapping distance to the next one. This method is predominantly used for small slots (<2 to 3× tool diameter). For larger slots an alternating method is used. The first holes are the two holes defining the slot width and are comparable to entry and the exit hole on a routing operation. From then on are holes always placed in between two holes (dividing the hole-to-hole distance by two). The advantage is that the drill bit always enters solid material (as long as possible) improving the precision by reducing the chance for deflections.

29.6.4 Predrilling

29.6.4.1 Definition. Pre drilling is an additional drilling step before the “main” drilling operation is performed and is typically applied for bigger diameters.

29.6.4.2 Effects. As the cutting conditions generally get worse going from the going along the primary cutting edge from the outside towards the center of the drill bit tip, in combination with the inability to have sufficient space to remove all material due to the remaining land or core of the drill bit, an additional drilling step upfront is made for diameters being equal or greater 0.157 in or 4.0 mm. This “predrilling” step removes a first volume of material and also centers the main drill bit. The size of this primary drill is chosen to be 15 to 35 percent of the main diameter.

“Predrilling” can also be applied for high aspect ratio holes for small diameters. In this case is the reduced diameter optional. The intention is more to use a drill bit with a very short flute length being more stable and having a smaller hole-to-hole tolerance and to perform a blind via centering the drill bit in the “main run.”

29.6.5 Pulse Drilling

29.6.5.1 Definition. Pulse drilling, also called step-drilling, is an incremental drilling step (like peck drilling), without retracting the drill bit out of the hole in between the drilling steps, but only pausing for a short period of time or number of revolutions, before continuing the stroke.

29.6.5.2 Effects. Especially on big diameters or counter sink holes is there a high risk for a continuous chip getting caught around the shank especially on high aspect ratio holes or heavy copper applications. This phenomena, also called “bird nesting” due to the visual similarity, is especially critical when operating with “contact drilling” as this chip can contact the surface of the stack before the drill bit, initiating the relative drilling operation “too early,” leading to a wrong depth or even missing holes. As an alternative to sole pausing in between the increments is the drill sometimes retracted to a very small extend. This is why some machine controls don’t differentiate between “peck drilling” and “step drilling” as they basically only differ by the amount the drill is retracted.

29.7 INNERLAYER REGISTRATION OF MULTILAYER BOARDS

Innerlayers of multilayer boards can shift during fabrication processes and create poor layer-to-layer alignment. During the artwork exposure or fabrication of the multilayer boards, the position of the copper shifts relative to the nominal stacked position. This can create breakout or missing of the copper pads when drilling the interconnection holes.

Two methods of inspecting the innerlayers of multilayer panels exist. One that has been used for several years is x-

ray. This technology has progressed significantly and is widely used.

29.7.1 X-Ray

X-ray technology is used to inspect the innerlayers of multilayer PCBs and to verify that the drill pads are located properly. Innerlayer shift is identified easily in an x-ray image, and a simple technique can be used to measure the misalignment accurately. In developing the PCB artwork, a set of stacked pads are located in the coupon area. These are inspected and a “bestfit” centering is calculated.

X-ray inspection also is used to determine movement of each individual layer. In this case, a locating pad with a corresponding layer pad is on each individual layer. The system can measure the distance from the locating to layer pad and determine movement of each layer due to the location of the layer pads. PCBs can be inspected after tooling holes are drilled to verify that they are in the proper locations. In addition, x-ray inspection can be performed after final drilling to verify that the holes are centered within the pads.

29.8 LASER DRILLING

The laser drilling operation can be split into data preparation, alignment, drilling (types), via formation, tool types.

29.8.1 Data Preparation

Similar to the conventional mechanical drilling operation, contain the data packages of a printed circuit boards the coordinates or locations of the laser vias and the diameter

information. As there are multiple methods or ways to generate the holes, there are several things that need to be defined in advance to enable the laser operation comparable to the selection of the drill bit geometry and the parameters. These parameters need to be set for different copper thicknesses, glass styles and resin (including the fillers) systems. But prior the parameter or tool definition, is the selection of the laser system and laser source.

29.8.2 Alignment

Before the laser operation can be started is it required to align the laser to the PCB. Usually is the laser operation immediately before or after the mechanical drilling process, avoiding an extra cleaning or desmearing operation. The alignment can be done:

1. To x-ray drilled holes (which are typically generated in relation to all inner layers)
2. To conventionally drilled holes
3. To the next inner layers

or to combinations of the three.

To enable an alignment to the inner layers is an additional process step called “skiving” required. In this process is all material above the target/landing layer removed with the laser in a square shape, clearing up alignment features (crosses, circles, …), to which the camera alignment can be done.

29.8.3 UV-Drilling

The most common lasers for UV drilling in PCB applications are the ND:YAG lasers. The generated (fundamental) wavelength is 1064 µm. However, for most systems is the

generated frequency doubled or tripled with optical elements (special crystals) leading to a harmonic of the fundamental frequency and with that to a shorter wavelength. The 2nd harmonic of Nd:YAG has a wavelength of 532 nm and the 3rd harmonic of 355 nm.

Configurations of conventional, pulsed, UV laser applications are average powers of 6 to 28 W, max. Repetition Rates of 40 to 300 kHz and pulse durations of 20 to 120 ns. The main parameters that can be set are for the via formation are: Drill type (spiral, trepan, punch, …), bite size, velocity, repetition rate, effective spot size, inner diameter, revolutions, radial pitch, entry angle (see also Sec. 29.6).

29.8.4 IR-Drilling

The most common lasers used for IR-drilling are CO_2 lasers. There are systems with different wavelengths available which are in the range of 9,400 to 10,600 nm or 9,4–10,6 µm.

Configurations of conventional, pulsed, CO_2/IR-laser applications for PCBs are average powers of 6 to 250 W, max. Repetition rates of 2 to 300 kHz and pulse durations of 1 to 100 ms. The main parameters for pulsed IR-drilling in addition to the diameter are: pulse period, pulse width, Z-focus offset.

The beam delivery from the resonator to the working area is done with mirrors.

29.8.5 Combination of UV—and IR-Drilling

To combine the advantages of UV drilling and IR drilling are systems with two different laser sources available. So that it

is possible to open the copper with the UV laser and remove the dielectric with the IR laser without additional alignment or setup times.

29.8.6 Short Pulse and Ultrashort Pulse Lasers

In addition to the wavelength which generally determines the type of ablation, is the “impact time” of the emission another important figure. For the laser drilling of blind vias are mainly “pulse lasers” used in which the light is emitted in portions or pulses. The length of the pulse is described in the duration in which the light is emitted.

For “short pulse lasers” is this time in the range of nano (10^{-9}) seconds. The energy impact causes a temperature exchange between electrons and between atoms. The material heats up until it exceeds the melting point and finally vaporizes.

“Ultrashort pulse lasers” have an even shorter pulse length in the range of pico (10^{-12}) seconds or even femto (10^{-15}) seconds. The material vaporizes directly without spreading much heat to the surrounding material. This is how carbonation of micro vias can be be minimized or even totally avoided.[3]

Configurations of conventional Ultra short pulse lasers are average powers of 6 to 50 W, max. Repetition rates of 400 to 1000 kHz and pulse durations of 0.3 to 20 ps.

29.9 LASER VIA FORMATION

The generation of laser (blind) vias is typically done in two steps to be most efficient and to assure a reliable process. In a first step is the surface copper removed and the via

“opened.” In the second step is the dielectric material removed all the way down to the landing copper. Both steps can be achieved in different ways (see Table 29.4).

TABLE 29.4 Steps for the Formation of a Blind Via with a Laser

Step#	Removal of	Laser Drilling Type 1	Laser Drilling Type 2	Alternatives
1	Copper	UV-drilling	Oxidation of copper + IR-drilling	Imaging + etching of Cu
2	Dielectric	UV-drilling	IR-drilling	Mechanical drilling

Removing the copper with a conventional imaging process (dry film lamination, exposure, Develop-Etch-Strip) is typically only practiced when there’s only an IR-Laser and no UV-laser available and the “work around” of oxidizing the copper to increase the absorption of the IR does not fulfill the quality requirements.

In case the “opening” of the via in step 1 is done with UV-drilling, some dielectric will be removed in addition to the copper. In the second step it’s necessary to adjust for UV-drilling the energy in such a way that the landing copper is not removed excessively. A minor removal of the outer diameter on the landing pad as indicated in Fig. 29.6 is quite common as the quality of cutting the glass in the dielectric needs to be compromised with the penetration of the landing Cu.

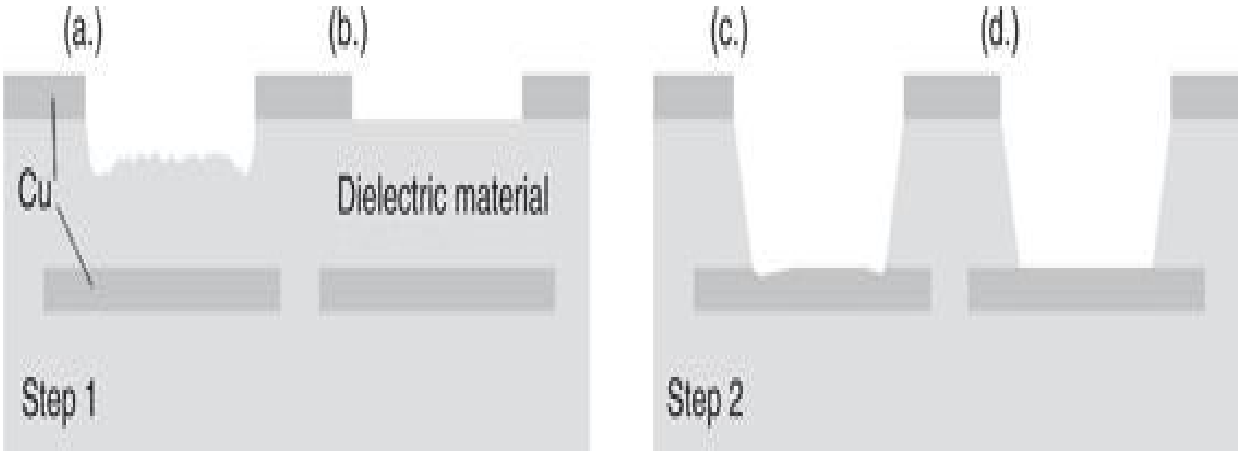


FIGURE 29.6 Removing the surface Cu with UV: (*a*) or etching (*b*). Removing the dielectric with UV, (*c*) or IR (*d*).

29.10 LASER TOOL TYPES

The two steps of generating the laser blind vias need to be set and adjusted for each diameter and material construction. For step one is the main driver the copper thickness. For step two are the key differentiators the type and amount of glass weave and the type and amount of filler elements in the dielectric. It’s possible to predefine different settings of the via formation with the selection and adjustment of different tool types.

29.10.1 Punching and Percussion Drilling

In this process is the materials removed with short pulses. In case of one single pulse this is called “single-shot” operation. In case of multiple pulses on the same location this process is called “percussion drilling” or “burst drilling.”

29.10.2 Trepan/Trepanning

This process describes a percussion mode, while moving the beam along a circular profile at a constant velocity. The distance from one pulse to the next is also called “bite size”. Some machine controls start at the center, going radially to the outer diameter, making the circular movement including some overlap and going back to the center. Others start with a center or pilot hole generated in percussion mode; this hole is then enlarged in a series of increasingly larger circles.

29.10.3 Spiraling

This process describes a percussion mode, while moving the beam from the center of a hole in a spiral path to the circumference. This spiral can be rotated and repeated, for example, to achieve the target depth of a blind via.

29.10.4 Helical Drilling

This process is used to generate through holes and describes percussion drilling in multiple circles of the same diameter at constant velocity. The laser starts removing material on the outside diameter (without starting from the center) in circles leading to a downward spiral. Once the laser has pierced through the material, additional revolutions help to improve the exit side of the hole.

29.10.5 Profile

This process describes a percussion mode, while moving the beam along a defined path at constant velocity to generate or cut any shape.

29.11 ACKNOWLEDGMENT

Portions of this chapter were taken from Chap. 24, “Drilling Processes,” written by Hans Vandervelde, Laminating Company of America, for Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

29.12 FURTHER READING

Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

Helmbrecht Bauer, *Lasertechnik*, 1st ed., Vogel, 1991, p. 88.

www.schmoll-laser.de/en/applications/pcb.html

[a] Significant parts of this chapter are based on “Precision Interconnect Drilling,” by Terry Haney, Chap. 25 in *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

CHAPTER 30

IMAGING AND AUTOMATED OPTICAL INSPECTION

Gareth Parry
Draig Technologies Inc., Stouffville, Ontario, Canada

30.1 INTRODUCTION

Imaging is the process that patterns the metal conductor to form the circuit. This process involves a multistep integration of imaging materials, imaging equipment, and processing conditions with the metallization process to reproduce the master pattern on a substrate. Large features (200 µm and greater) can be very economically formed by screen printing. Feature sizes smaller than 200 µm, however, are formed using a photolithographic process, which is the main discussion of this chapter. As circuit densities have increased over the years, the imaging process has continually evolved to enable commercial production of finer features. This need for high-density interconnect (HDI) is driving the industry to feature sizes of 10 µm or lower. Imaging equipment and materials have been developed to meet this challenge.

To achieve a reproducible high-yield/low-cost imaging process for a given feature size, various factors must be carefully balanced. This chapter outlines the chemistry and equ ipment options for the photolithographic imaging process, highlighting trade-offs that must be considered so that process engineers, designers, and procurers of printed wiring boards (PWBs) and HDI structures have an overview of the process considerations that can enable a manufacturable product.

Printing is an alternate process for imaging. Screen printing is used to print resist on foil and silver inks on polyester. Ink jet printing has been used to pattern resist, legend, and silver conductors. A number of ink jet systems have been introduced that prints a UV-curable resists or a catalyst layer to electroless plate copper at thicknesses of 0.05 to 5 μm.[1] Significant development work is underway on organic transistors patterned by ink jet and other printing methods. These PCB ink jet techniques are covered later in this chapter.

The photolithographic process sequence for imaging is given in Fig. 30.1. Basically the process involves applying a light-sensitive polymeric material (photoresist) onto the substrate of interest, exposing this photoresist to light with the desired pattern, and developing the exposed pattern. This developed pattern is used for either subtractive (etching) or additive (plating) metal pattern transfer. Details of these metallization processes are given in subsequent chapters. After metallization, the photoresist is stripped from the surface and the panel is ready for further processing.

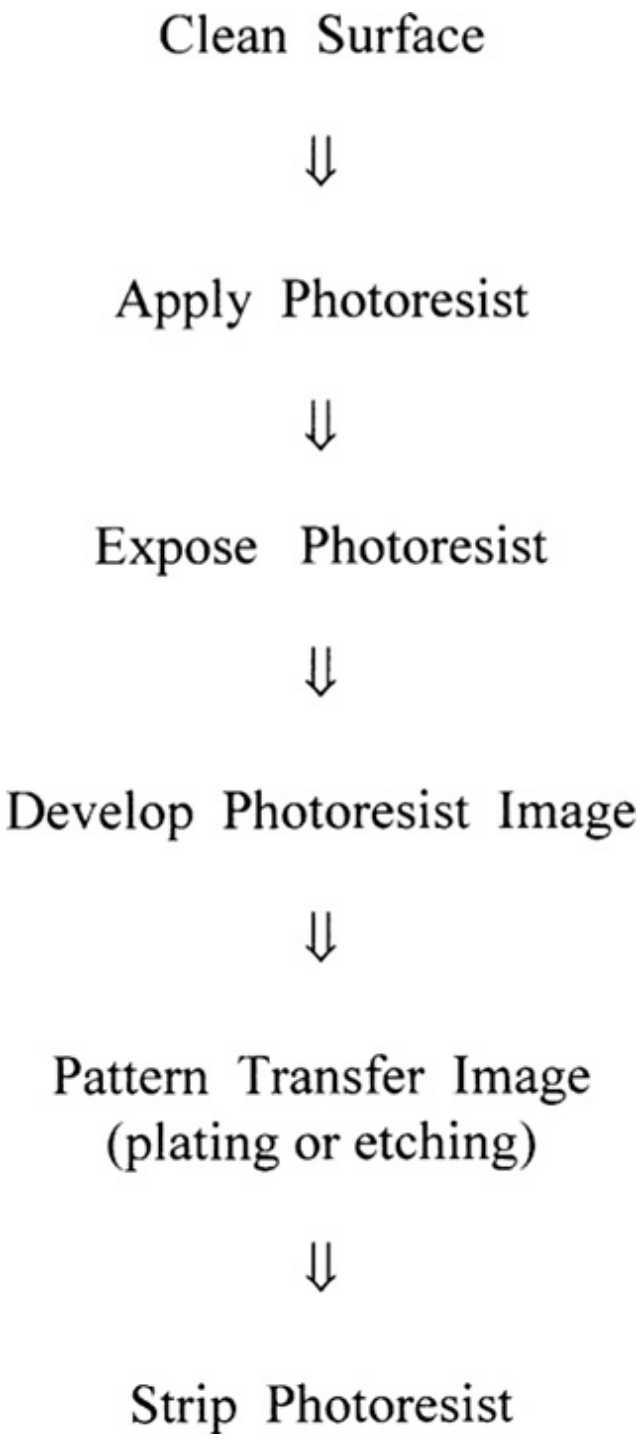


FIGURE 30.1 The photolithographic process sequence.

30.2 PHOTOSENSITIVE MATERIALS

The photosensitive polymeric systems used as photoresists in the interconnect industry are either liquids or dry films formed from a liquid solution. Dry-film photoresists are the industry standard, but liquid photoresists have become widely used, particularly for fine-feature circuits. Liquid resists come in both positive and negative acting, in neutral and electrolytic acting. Both types of photoresist can be used for a variety of processing requirements.

30.2.1 Positive- and Negative-Acting Systems

Photoresists may function in a photographic sense in either a positive or negative tone. The difference, illustrated in Fig. 30.2, is a result of the specific chemical reactions that occur on exposure to light. For the common negative-acting systems, exposure initiates cross-linking between one or more of the components in the polymeric matrix, reducing the photoresist's solubility in the developing solution. The exposed regions remain after development of the image. For positive-acting photoresists, the chemistry is often the novalac resin-based materials utilized by the semiconductor industry. Upon exposure, an acid-catalyzed reaction occurs that increases the solubility of the photoresist in the developer solution. In this case, it is these exposed regions that are removed in the developer solution.

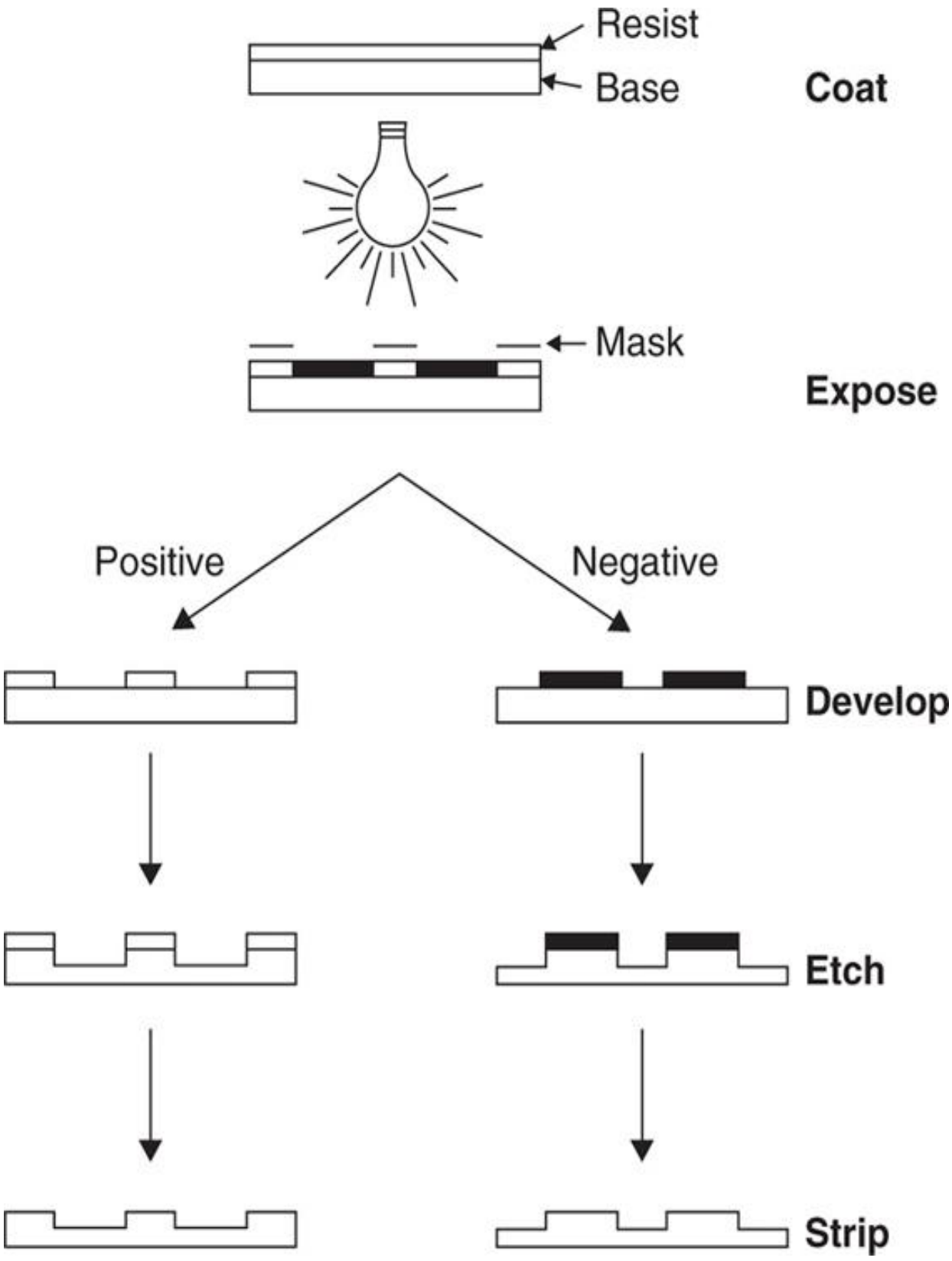

Resist
Base
Coat
Mask
Expose
Positive
Negative
Develop
Etch
Strip

FIGURE 30.2 The photolithographic process sequence for positive and negative tone photoresists. (*Reprinted by permission of C.G. Willson*, Introduction to Microlithography, Theory, Materials and Processing, *ACS Symposium Series 219, Washington, D.C., 1983, p. 89*.)

Photographic tone can have an effect on product yield caused by contamination between the phototool with the master image and the photoresist. For a negative-acting photoresist, contamination blocks the light and prevents cross-linking, leading to a mousebite (partial reduction in line width) or an open circuit in the conductor after etching. For a positive-acting photoresist, contamination blocks the light and prevents the acid-catalyzed solubilization, leaving excess metal and a possible short after etching, assuming the resist is utilized in a print and etch process. Since circuit patterns often have a greater area of spaces than lines, there is a lower probability of a contaminant causing an actual defect with the positive-acting photoresist. Defect can be short or open, depending if print and etch or plate and etch. However, negative-acting photoresists are the most widely used since many other factors impact yield and contamination must be minimized in any photolithographic process.

30.2.2 Decision Factors

The large variety of commercially available photoresists makes it a challenge to determine which one is likely to perform best for a given application. Key technical and economic factors that must be considered are summarized in Fig. 30.3. The primary consideration is the end use of the pattern.

Key Considerations in Photoresist Selection

Metallization Process

- Etching
  - –Acid
  - –Akaline
- Plating
  - –Copper
  - –Tin
  - –Tin/Lead
  - –Gold
  - –Nickel
  - –Full-Build Electroless Copper

Imaging Process
- Standard UV
- LDI
- DDI

Panel Design
- Substrate Topography
- Required Copper Thickness
- Number and Size of Holes
- Minimum Feature Sizes

Economic Factors
- Compatibility with Existing Application and Exposure Equipment
- New Capital Equipment Investment Required
- Productivity
- Process Latitude for High Yield
- Material Cost

FIGURE 30.3 Criteria for selection of photoresist materials.

The photoresist must be chemically compatible with the subsequent pattern transfer steps (i.e., can withstand the chemical environment such as the solution pH) for it to function as an accurate mask for pattern transfer.

The nature of the substrate itself in terms of topography and surface features must also be considered. Is the photoresist required to cover or tent plated through holes or tooling features, and must it conform to existing circuitry? This consideration will dictate if dry-film or liquid photoresists are appropriate and, in some instances, the required tone.

The required product feature dimensions are equally important. They are usually specified in terms of line width and spacing with a given allowable variation. Since these product specifications are for the final conductor features, the impact of photoresist processing on the critical dimensions must be established. Each photoresist has an inherent contrast (i.e., the rate of change of solubility on exposure to light). This contrast, combined with the resist thickness, phototool, light source used for exposure, and developing conditions, determines the finest feature that can be imaged. For photoresists used in the PWB industry, the minimum line width achievable in production is usually 10 to 25 μm greater than the photoresist thickness. Novel process sequences have demonstrated it is possible to overcome this traditional barrier.[2]

The adhesion of the photoresist is another key attribute. The chosen photoresist must have good adhesion to the underlying substrate during pattern transfer but must also be able to release cleanly from the substrate during stripping.

Key consideration that can effect resist selection is UV versus laser direct imaging (LDI).

30.3 DRY-FILM RESISTS

Dry-film photoresists are generally used for pattern formation prior to both plating and etching.

These films have a three-layer structure, with the photosensitive material sandwiched between a polyester coversheet and a polyethylene separator sheet (see Fig. 30.4). The photoresist thickness is typically 25 to 50 μm, but thinner and thicker films are used for special applications. The photoresist is applied to the PWB substrate using lamination: The polyethylene separator is removed, and the photoresist flows under the heat and pressure from the laminating rolls to adhere to the substrate. The polyester coversheet performs several key functions. It protects the photoresist during handling, prevents sticking to the phototool during contact printing, and acts as an oxygen barrier during exposure. The optical properties of this polyester coversheet are important, especially for producing features less than 100 μm.

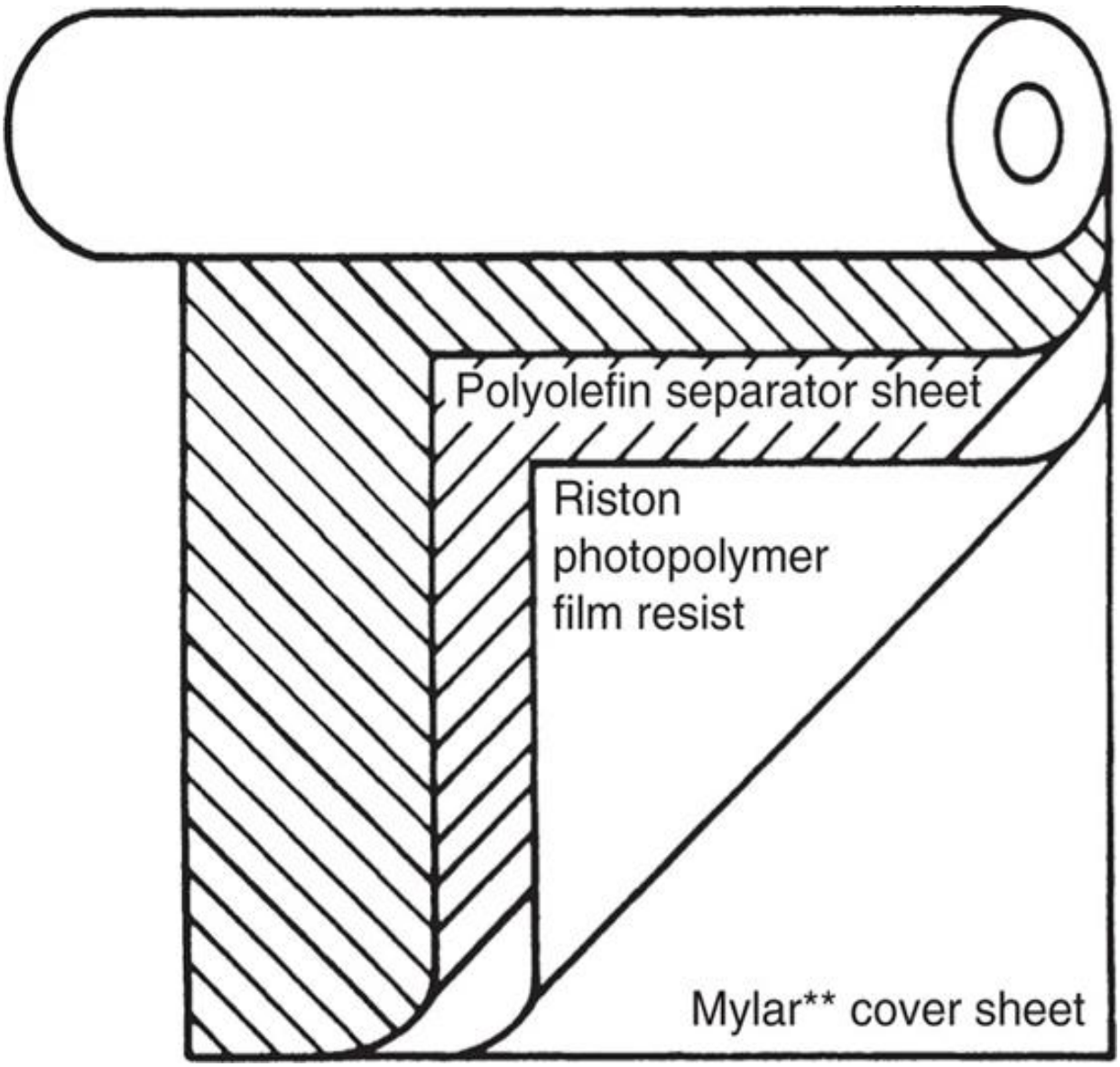


FIGURE 30.4 Dry-film photoresist components. (*Reprinted with permission of DuPont Electronics, DuPont Technical Literature*.)

Dry-film manufacturers have increased the optical clarity and reduced the thickness of the polyester sheet to achieve the required image quality. Thin dry films of 25 μm thickness and less generally use this high-quality coversheet.

The chemical and mechanical properties of dry-film photoresists have been tailored to withstand various plating solutions and acid or ammoniacal-etching solutions. They

can be grouped in terms of the processing chemistry used to develop the image:

- *Aqueous-developable:* This group is the industry standard.
- *Semiaqueous-developable:* These are used in special applications.
- *Solvent-developable:* This is the original system (see Table 30.1). Since solvent development used chlorinated hydrocarbons, use of the solvent-developable photoresists has generally been abandoned.

TABLE 30.1 Summary for Dry-Film Photoresist Types and Chemistries

Photoresist Type	Develop Solution	Strip Solution	Application
Aqueous-processable	Sodium/potassium carbonate	Sodium/potassium hydroxide	Acidic solution: etching, plating Limited alkaline solutions: alkaline etch
Semiaqueous-processable	Sodium tetraborate/ Butyl cellosolve	Ethanolamine or Butyl carbitol/Butyl cellosolve	Alkaline solutions: etching, precious metal plating
Solvent-processable	(Methyl chloroform) Alternate to CFCs	(Methylene chloride) Alternate to CFCs	Strong alkaline: full-build electroless Cu plating

30.3.1 Chemical Composition Overview

Dry-film photoresists vary in their exact chemical compositions, but all contain the following components[3]:

- Polymer backbone
- Photoactive compound
- Monomer
- Dye
- Additives: The polymer backbone sets the fundamental solubility and chemical resistance of the system.

On exposure, the photoactive compound absorbs light of the appropriate wavelength and subsequently reacts with the monomer to alter the solubility of the film in exposed areas. The dye changes color on exposure to provide a visible latent image of the master pattern in the film, referred to as the printout image. Although the printout image decreases the efficiency of the desired photoreaction by consuming a portion of the exposed photoactive compound, it has proven to be a valuable manufacturing aid and is used in almost all dry-film photoresists.

Additives include adhesion promoters, flexibilizers, and other compounds that can improve a desirable property. All the ingredients function together to provide the process latitude needed for the photoresist’s specific range of applications.

30.3.2 Aqueous-Processable Dry Films

The majority of materials used are based on an acrylic polymer with various forms of photoreaction initiation. The initiator’s absorption is designed to coincide with the major emission wave- length of the mercury arc lamps in the ultraviolet region of the spectrum at 365 nm.

Many are based on the use of Michler’s ketone and its subsequent sensitization of a triplet state promoted radical chain polymerization. This also explains the material’s

sensitivity to oxygen, an efficient triplet quencher. These materials are also very efficient at converting light energy into a chemical reaction due to the radical chain reactions; absorption of one photon of light results in many cross-links in the polymer matrix. Usual exposure doses measured as the irradiance from 330 to 405 nm to cross-link these materials functionally vary from 25 to 90 mJ/cm^2 depending on the exact chemistry used and the thickness of the materials, which compares favorably to positive-acting materials used for optical lithography in semiconductor integrated circuit (IC) production, where doses of 200 to 500 mJ/cm^2 are common.

The images in these materials are developed in alkaline solutions of 1 percent or less by weight of sodium or potassium carbonate. The complete removal of the photoresist after pattern transfer is accomplished in 1M or greater solutions of sodium or potassium hydroxide at elevated temperatures, often with an antitarnishing additive to limit oxidation of the copper. Thus, in general, these materials exhibit excellent stability in acidic solution, but they do have varying stability to more strongly acid and alkaline solutions. In fact, there are three subclasses of materials: for acid etching of copper, for acid plating of copper, and for alkaline (ammoniacal usual) etching of copper. Increased acid stability is required for use in acid copper plating, in which the pHs of the solutions often are below 1. For ammoniacal copper etching at pH 8 to 9, increased alkaline stability is required. This latter capability illustrates the flexibility in tailoring these materials to their end use since these materials are imaged using similar alkaline chemicals: develop at pH 10.3 and strip at pH 13. Often these alkaline-stable materials are developed at high temperatures.

In the past, several photoresists were formulated for exposure at a visible wavelength, 450 nm, using specialized exposure equipment—visible lasers or magnified projection

printing. Laser direct imaging (LDI) based on the Ar^+ laser output clustered around 360 nm has been commercialized and is becoming more popular for fine line processing and complex designs that require enhanced registration protocols. Direct digital imaging (DDI) is now also being used, based on Texas Instrument's proprietary DLP™ technology of digital micromirror devices (DMD). Conventional photoresists can be exposed on LDI and DDI equipment, but higher photospeed has been key to the productivity and economics of LDI/DDI.

Photoresists requiring only 10 mJ/cm^2 are commercially available for the major applications. In general, these high-speed photoresist processes are similar to conventional ones, but improvements include photospeed, sensitivity to yellow safelights, and postlamination hold.[4]

Novel aqueous-developable photoresists have been formulated to process in dilute acidic media. A dry film based on electrophoretic depositable (ED) materials was shown to have excellent stability in strong alkaline solutions, potentially useful for etching polyimides or for full-build electroless copper plating.[5]

30.3.3 Semiaqueous- and Solvent-Developable Dry Films

Semiaqueous-developable photoresists are used when increased resistance to chemical attack is required, such as the highly alkaline solutions used in polyimide etching or gold and precious metal plating applications. Their composition is similar to the aqueous-developable photoresists, but the polymer backbone is less alkaline-soluble. This increased chemical stability provides accurate image transfer by maintaining the integrity of the surface and sidewalls and minimizing underplating. Semiaqueous-

developer chemistry is slightly alkaline (sodium tetraborate) and contains an organic assist, typically butyl cellosolve. Process control for this mixture is more complicated than that used for aqueous development.

Solvent-developable dry-film photoresists were the first to be commercially produced. Since they are the only materials that can withstand the harsh conditions in some chemical processing sequences, they still have some interest. They are based on methyl methacrylate polymers and a Michler's ketone initiation system similar to that used for aqueous-developable photoresists. Although they can have very high contrast, they are prone to scumming, leaving residue in the spaces between exposed photoresist features after development. Slight etching of the underlying substrate is often required to have a clean image-transfer step, especially for pattern-plating applications. Traditionally these materials were developed in trichloroethane and stripped in methylene chloride. However, as the hazards associated with chlorinated hydrocarbons were recognized, use of these solvents has been practically eliminated. This has forced the use of alternative develop and strip chemistries for solvent development.[6]

30.4 LIQUID PHOTORESISTS

Liquid photoresists come in a variety of chemistries.[7] Many are simply coatable forms of the dry-film materials. They have been used primarily for patterning innerlayers and are applied to the substrate by roller, spray, curtain, or electrostatic coating techniques. These methods are discussed later in the chapter (with equipment). Applied thickness is typically 6 to 15 µm, giving superior resolution compared to dry-film resists that are generally thicker. Since resolution is approximated by the thickness, they have the

ability to resolve features less than 25 µm. Conformation of liquid photoresist to the copper substrate is generally very good, and it is possible to achieve high yield at 50 µm features and less.[8] However, cleanliness of the substrate and the coating and drying operation is critical. Liquid photoresists are dried to allow for hard contact with the phototool during exposure, maximizing resolution. If soft or off contact is used, resolution and yield decrease, especially for features 100 µm or less. For the majority of liquid photoresists, the developing and stripping conditions are similar to those for aqueous-developable dry films: mild alkaline sodium carbonate and strong alkaline sodium hydroxide. Exceptions are positive-acting novolac-based photoresists, thermal photoresists,[9] and negative-acting acid-developable photoresists.

30.4.1 Negative-Acting Liquid Photoresists

The chemistry of the typical materials is similar to that of the aqueous-developable dry films. They depend on a radical chain reaction to promote cross-linking in the acrylic polymer. Their sensitivities differ depending on the initiator system chosen. Materials are available with minimal solvent content, and a few are diluted with water.[10,11] This reduces the emissions from coating and drying that must be contained and treated.

Acid-developable photoresists mentioned in the dry-film aqueous section can also be formulated as electrophoretic-depositable liquids. These materials have high contrast, good resolution, and chemical stability in strongly alkaline solutions since they are developed in aqueous acid solutions.

30.4.2 Positive-Acting Liquid Photoresists

The other alternative is a positive tone novolac resin-based system that finds its application most usually in the semiconductor industry for imaging integrated circuits. It has excellent resolution and chemical stability in acid and a large number of basic solutions (precious metal plating). The chemistry involves the conversion of a base-insoluble diazonaphthoquinone to the base-soluble indene acid. Thus, this photo-driven conversion alters the solubility of the base material in alkaline solutions, allowing for image formation (see Fig. 30.5).

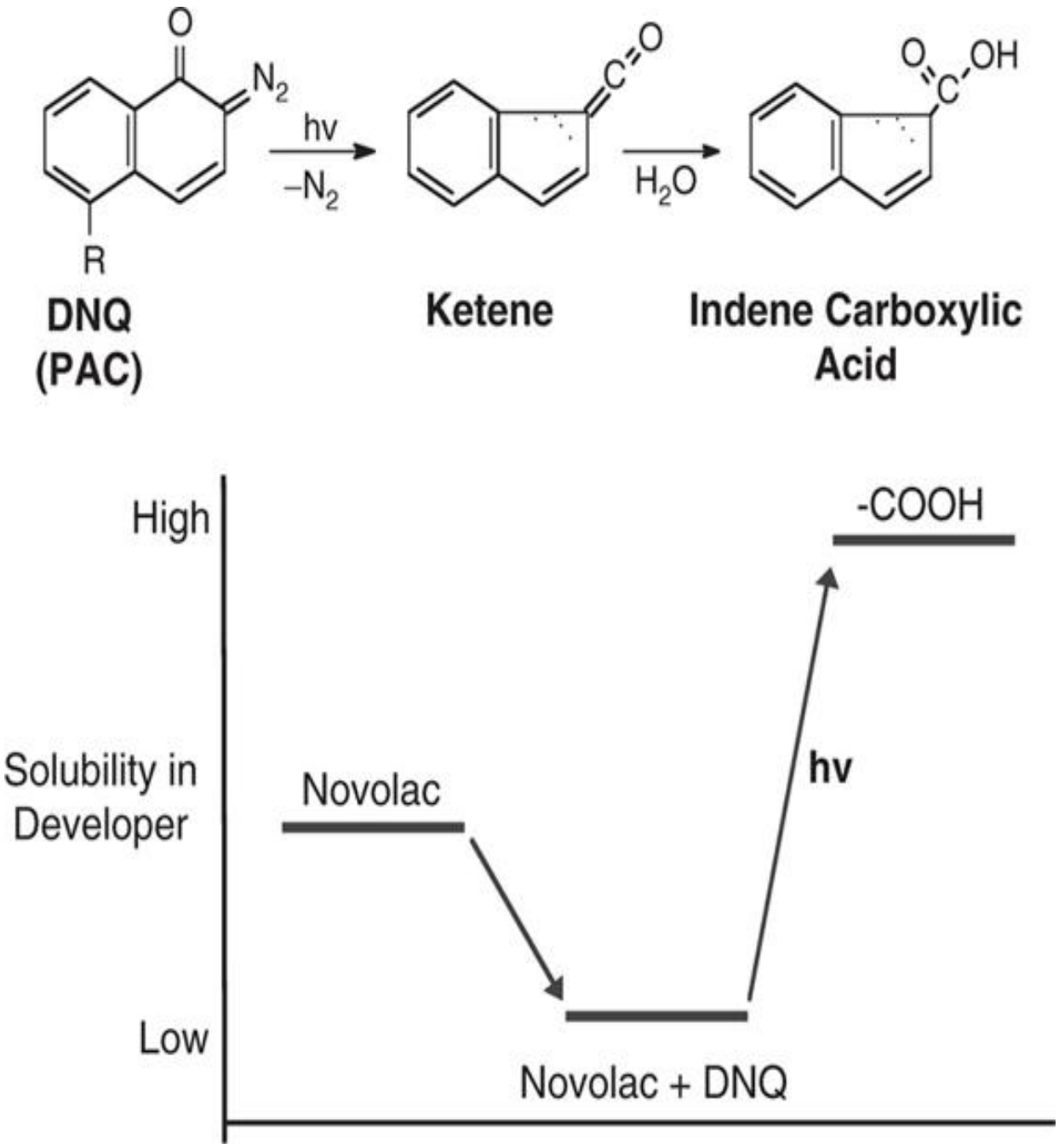


FIGURE 30.5 Chemistry mechanism of positive-acting liquid photoresists.

30.5 ELECTROPHORETIC DEPOSITABLE PHOTORESISTS

Electrophoretic depositable (ED) photoresists[12,13] were introduced in the late 1980s with expectations of broad adoption by the interconnect industry. The early materials were modifications of those used for coating automobiles and appliances. These fast-coating processes provide a defect-free film of high durability on conductive substrates and are well suited to large-volume production. Anodically and cathodically deposited materials that are both positive and negative acting have been introduced but have achieved limited market penetration in the interconnect industry. Advances in dry-film photoresists and liquid photoresists reduced the interest in implementing a new photoresist process. (A detailed discussion of electrophoretic depositable photoresists is included in Sec. 17.1.6 of the fourth edition of this handbook.)

30.6 RESIST PROCESSING

Imaging is a sequential process, and the various steps are very interdependent. Equipment and processing conditions play a large role in the image quality, yield, and productivity that can be achieved. The choice among the numerous options for each step depends on the type of substrate to be imaged, the feature sizes to be produced, the existing equipment, the type of photoresist, and the productivity and economics of the production line. Alternatives for each process step are described and compared.

30.6.1 Cleanliness Considerations

Cleanliness is an issue throughout the entire photolithography process, including yellow room contamination level (cleanliness class), solution filtration, equipment cleanliness class, and product handling. Its

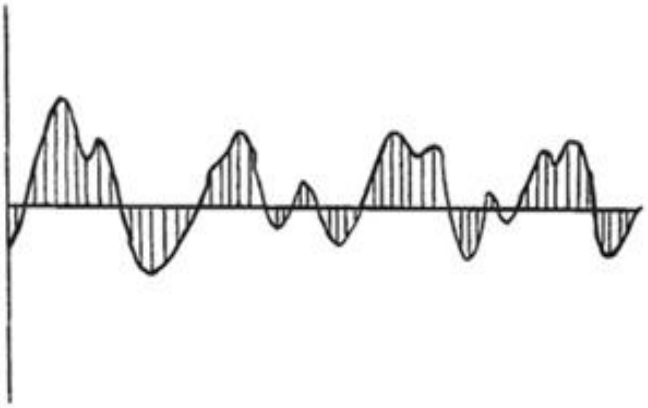
importance increases as feature size decreases. The level of cleanliness needed to give acceptable yield for the finest features must be established and maintained.

Sticky rollers, either as free-standing equipment or as handheld items, are one type of equipment used to remove contamination from flat surfaces, either panels or equipment.

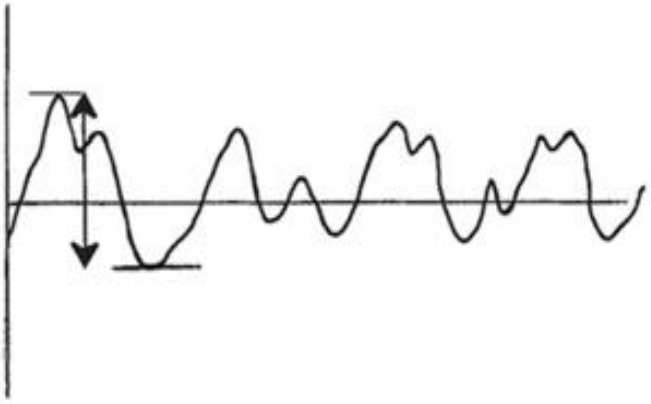
30.6.2 Surface Preparation

Good adhesion between the photoresist and the substrate is essential for the remainder of the process to be successful. All laminates arrive at the imaging area, dirty, and the exact process sequence for surface preparation is chosen based on the nature of the contamination. Epoxy dust generated during trimming and processing of the laminate is removed by mechanical cleaning. The copper surface is either foil or foil with electroless or electroplated copper. Foil typically has an antitarnishing agent of chromium and zinc that must be removed for reproducible imaging results. During cleaning, the texture or surface roughness of the copper is altered, promoting mechanical adhesion between the copper and the photoresist. The extent of this texturing is measured by the usual parameters for surface roughness, the height and spacing of the topography measured by profilometry (see Fig. 30.6).

R_a Arithmetic mean of all departures from the mean line



R_{max} Maximum peak to valley height within sampling area



R_m Mean spacing between peak measured at the mean line

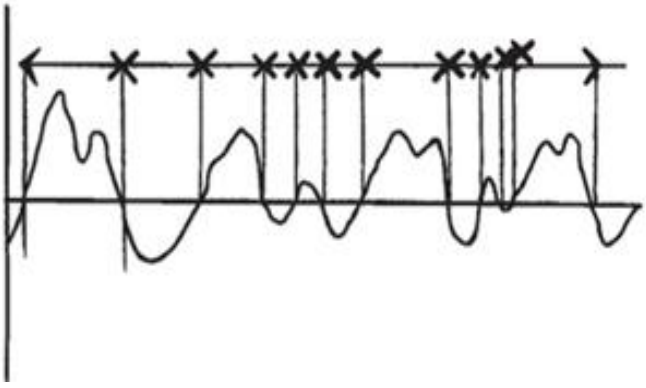


FIGURE 30.6 Surface roughness parameters.

Chemical cleanliness can be determined in a variety of ways. Wetting is often tested using a *water break test* or

more analytically in terms of contact angle, with a low value being desirable.

In addition, analytical techniques (Auger and x-ray photoelectron spectroscopies) can be used to evaluate the chemical composition of the surface (see Table 30.2).[14]

TABLE 30.2 Copper Surface Chemical Composition as Measured by X-Ray Photoelectron Spectroscopy (XPS)

Sample	% Cu	% O	% C	% N	% Zn	% Cr
Initial		46	24		16	12
Preclean 1	12	19	68			
Preclean 2	6	10	70	14		

30.6.2.1 Mechanical Cleaning. Most mechanical cleaning equipment physically abrades the copper surface using a pumice or aluminum oxide slurry either directly (scrubbing or vapor blasting) or impregnated into brushes. Scrubbing provides an even final surface texture, whereas brushing creates grooves (see Fig. 30.7). The copper thickness must be sufficient to provide the desired final conductor height after cleaning. Mechanical cleaning is more difficult for very thin flexible panel and should only be used on cores>0.020 in. (0.52mm)due to registration issues caused by mechanical distortion of the cores.

FIGURE 30.7 Comparison of the pumice cleaned (*a*) and mechanically abraded copper surfaces (*b*), 1200×. (*Reprinted with permission of D. P. Seraphim, R. C. Lasky, and C-Y Li*, Principles of Electronic Packaging, *McGraw-Hill, 1989, p. 383*.)

The texture of the mechanically cleaned surface affects the adhesion between the photoresist and the copper. The resist should conform to the topography, and thus, the extent and type of texture must be tailored to the type of photoresist. If

the gouges are too deep, a dry film applied with traditional lamination will have difficulty conforming to the surface and create defects: near or full opens after etching, and underplating or shorts after pattern plating. Thus, the cleaning process, photoresist type, and application method must be matched to image at high yields.

Conveyorized equipment is used that passes the panels through the brushes or slurry and then to rinse chambers before exiting through a dryer section. If rinsing is insufficient, residual pumice can remain on the copper surface. Maintaining proper functioning of the mechanical parts that contact the product is essential since brushes and slurry deteriorate with use. Equipment designs that isolate the abrasive from the majority of the tool are more durable. Conveyorized equipment that utilize brushes can distort thin panels and cause registration concerns of the build-up circuitry.

30.6.2.2 Chemical Cleaning. Chemical cleaning includes a variety of solutions since the solubility of contaminants can be quite different (see Table 30.3). Grease and fingerprints require a soap solution or solvent to dissolve them. Antitarnish treatment removal and copper roughening is done with mild etchants for the copper, such as ammonium persulfate, sodium persulfate, or peroxide/sulfuric acid. Depending on the oxidation level and the amount of antitarnish treatment, there is often an induction time for copper removal. Solutions used can be common chemicals or proprietary mixtures in which surfactants and other additives have been included. Alternatively, the oxide and antitarnish treatment can be removed initially, followed by a surface roughening. In this case, the oxide removal is accomplished with mild acidic cleaning solutions such as sulfuric acid spray followed by adhesion promoter.

TABLE 30.3 Cleaning Solutions Used to Remove Various Contaminants

Cleaning Technique	Process Chemistry	Contaminant Removed
Abrasion	Pumice, Aloxide	All
Plasma	CF_4/O_2, O_2/H_2O	Organic
Chemical solutions (aqueous etchants)	H_2SO_4, HCl, etc.	Inorganic
Chemical solutions (nonaqueous)	Alcohols, etc.	Organic
Thermal	N_2	H_2O

Source: Adapted from *Introduction to Microlithography,* 1st ed., L. F. Thompson and M. J. Bowden, American Chemical Society Symposium Series 219, Washington, D.C., 1983, p. 184.

The selection of the cleaning solution also depends on the copper thickness. Thin “seed” layers used for electrolytic pattern plating can tolerate very little etching, and extremely dilute solutions or dry methods are used. Thus, chemical adhesion can be more important than mechanical.[15] Selection of the proper process chemicals and sequence depends on the overall conductor formation process and the photoresist to be used.

Chemical cleaning sequences are often contained in conveyorized spray equipment with rinsing between each step. Batch processing in a tank system is also used, with a hoist for basket movement between solutions. Uniformity of the etching of panels within a basket must be measured, but is generally quite good and reproducible as long as the immersion time is short and the bath’s chemical composition is consistent.

Reverse treated foil (RTF) or drum side treated foil (DSTF) have a textured copper tooth topography designed for resist

adhesion. Further chemical roughening can effectively smooth out the copper surface. As such, no chemical etching is required on RTF/DSTF copper. A mild cleaner may be utilized to remove grease and fingerprints, and antitarnish coating. Several manufacturers find acceptable yields by not pre-cleaning RTF/DSTF foil and go straight into the resist application process.

30.6.2.3 Electrolytic Cleaning. A unique inline conveyorized tool built by a equipment supplier uses electrolytic cleaning.[16,17] The antitarnish is removed electrolytically along with oils and fingerprints in a uniform process with very little copper removal. The surface texture is then altered by microetching and passivated prior to dry-film photoresist lamination or other coatings.

30.6.3 Photoresist Application

The technique used to apply the photoresist to the substrate depends on the type of photoresist selected. The various techniques used with dry-film and liquid photoresists are discussed. For any of these techniques, the cleanliness of the operation—both the equipment and the room—and the handling of the product are critically important, especially for high density. It is also advisable to minimize handling at this stage by using automated inline equipment for the preclean step and automatic loading and unloading.

30.6.3.1 Dry-Film Hot Roll Lamination. In this process, both temperature and pressure are used to laminate the dry-film photoresist to the panels. After stripping off the polyethylene separator sheet, the photoresist is contacted to the substrate in a nip between two heated rolls. Heat reduces the viscosity of the photoresist and pressure causes

it to flow, conforming to the irregularities of the copper surface.

The weave of the laminate affects the topography of the substrate and how much flow is required to achieve good conformation, an essential condition for high yield. Dry-film photoresists are tailored to have rheology that maximizes flow during lamination while preventing flow in the roll prior to lamination, which could cause edge fusion. Panels are often heated with heated rolls and infrared heaters prior to lamination to improve photoresist conformation. The key process parameters affecting conformation are laminator speed, laminating roll temperature, and rigidity of the rolls with respect to the core material and rubber durometer. Typical rubber durometer is 40 to 50 on the Shore A hardness scale. Durometers of 55 to 65 can be used where extra conformance of the resist to the panel surface is required. For aqueous-developable materials, wet lamination has proven to be effective in improving conformation and yield for innerlayers. By using a water-alcohol mixture, wet lamination can also be applied to tent and etch inner via holes to minimize the land diameter.[18]

Both automatic and manual tools are available for film lamination (see Fig. 30.8). With manual tools, the panel is placed in the nip and pulled through by the rotation of the rollers.

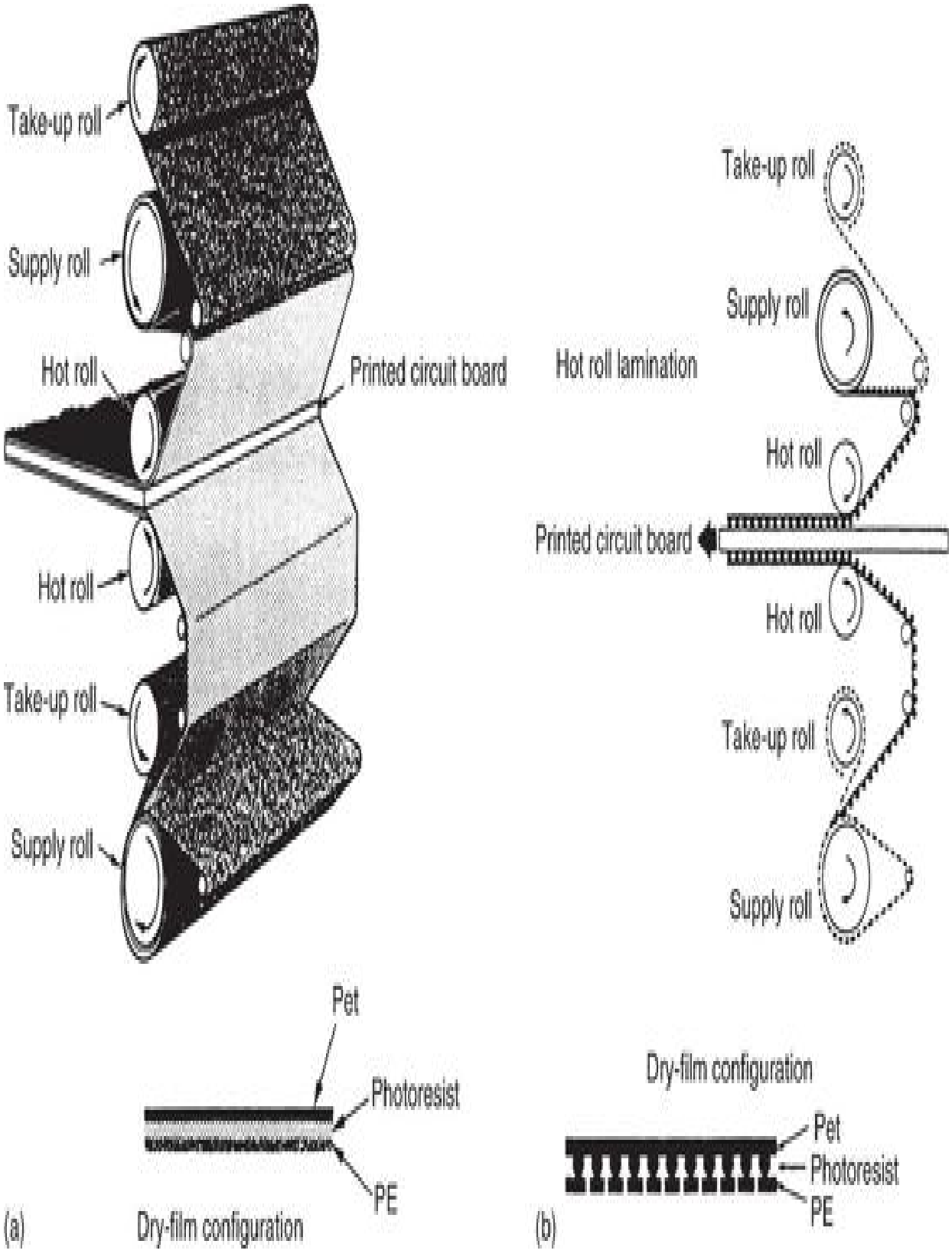


FIGURE 30.8 Configuration of a hot roll laminator: (*a*) three-dimensional schematic, (*b*) two-dimensional schematic. (*Reprinted with permission of E.S.W.*

Kong, Polymers for High Technology, *ACS Symposium Series 346, Washington, D.C., 1987, p. 280*.)

The continuous film of photoresist must be trimmed for each panel on at least two sides. This technique is labor-intensive and extremely dirty due to the chips of resist generated by trimming. However, it is useful for very thin materials and nonstandard-size panels in small lot sizes.

With automatic equipment, the basics are the same but the panel enters from an automatic loader or a conveyorized preclean tool directly into and through the dry-film laminator.

This is a relatively clean operation with little handling of the panels since the photoresist is automatically trimmed to the appropriate size and placed 1 to 4 mm within the board edge. Equipment is available to convey even very thin panels. Panels are often heated, wetted (wet lamination), or cleaned before the actual lamination.

30.6.3.2 Dry-Film Vacuum Lamination. This method is similar to hot roll lamination but the temperature and pressure used to adhere the photoresist to the substrate is applied by a heated vacuum platen instead of laminating rolls. Vacuum lamination is useful for products with tall or closely spaced features that make it difficult for the photoresist to conform. The vacuum removes the air that would be trapped and pulls the photoresist into tight spaces, providing conformal coverage. This equipment is also used for material that will deform nonuniformly under the pressure of laminating rolls, such as thin unreinforced polyimides. With vacuum lamination, the pressure is evenly distributed over the panel, improving dimensional stability control.

30.6.3.3 Liquid Coating. A great variety of methods are used to apply liquid photoresist to panels. Roller, spray, electrostatic, and electrophoretic coating provide double-sided application and are well suited to high-volume manufacturing. Curtain coating is single-sided, requiring

either two passes of the panel through the equipment with slight drying between coatings or an inline equipment layout with two coating and drying units. This causes a difference in the solvent content of the two sides. Screen-coating equipment is available for either single-side or double-side coating. In all instances, the cleanliness of the surroundings, equipment, and solutions is essential for high-yield processing. Most equipment is designed to minimize material consumption by collecting and filtering excess liquid so it can be recycled to the feed tank.

30.6.3.4 Roller Coating. This method places liquid photoresist on the board by transferring the liquid from one set of rollers to another (see Fig. 30.9). The exact number, physical configuration, and surface of the rollers vary, as well as how the material is metered. Often, gravure roller coating is used. Grooves or crosshatches in the rollers that contact the panel determine the amount of liquid deposited on the substrate and are set with a measured overlap or interference so that the board is squeezed between the rollers.19 Photoresist viscosity also influences the coating thickness applied. Improvements in panel handling and in confining the solution to the center of the panel allow for simultaneous two-sided “postage stamp” coverage similar to that obtained with dry-film photoresists, leaving the tooling and location holes clear of material. In commercial systems, the coater is conveyorized, with panels entering a clean oven immediately after coating. The throughput of these systems can be as high as 240 panels per hour.

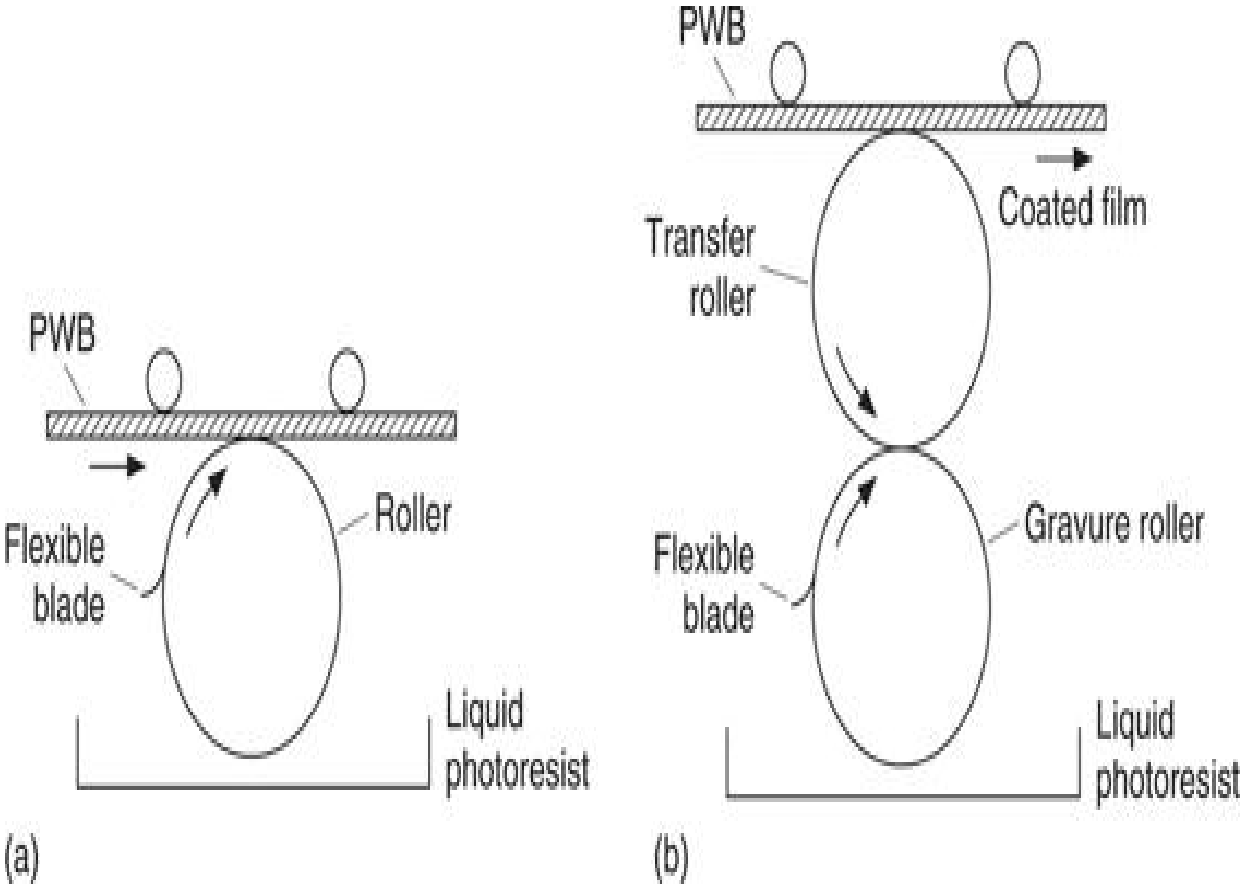


FIGURE 30.9 Configuration of a roll coater: (*a*) direct coating, (*b*) indirect coating.

30.6.3.5 Spray Coating. Although very thin and uniform coatings are possible with this method, its use in resist imaging has been limited due to concerns about waste caused by overspray.

The spray head traverses a larger area than the substrate to be coated, and the amount of liquid photoresist that becomes overspray can be significant. Exact characteristics of the coating in terms of thickness and topographical coverage depend on spray-head configuration, nozzle backpressure, droplet size, and conveyor speed.[20]

30.6.3.6 Electrostatic Coating. This method is similar to spray coating except that the rotation spray head is charged and the panel is grounded. Since the atomized

photoresist is attracted to the substrate, there is less material waste than with spray coating.[21] Electrostatic coating is used for solder mask since it provides good coverage of conductor sidewalls. However, its use with photoresist is limited to innerlayers. It is unsuitable for outerlayers because it deposits a thicker coating on the rim of a plated through hole while leaving its interior uncoated.

30.6.3.7 Electrophoretic Coating. This method requires materials specially formulated for anodic or cathodic deposition. The equipment schematic in Fig. 30.10 illustrates the process sequence: preclean, coat, permeate rinse, rinse, and dry.[22] Panels are placed in the photoresist solution wet or are often sprayed with solution to ensure wetting, especially if the parts have blind or through vias. Voltage is applied, and within 20 s to 3 min an insulating film forms.

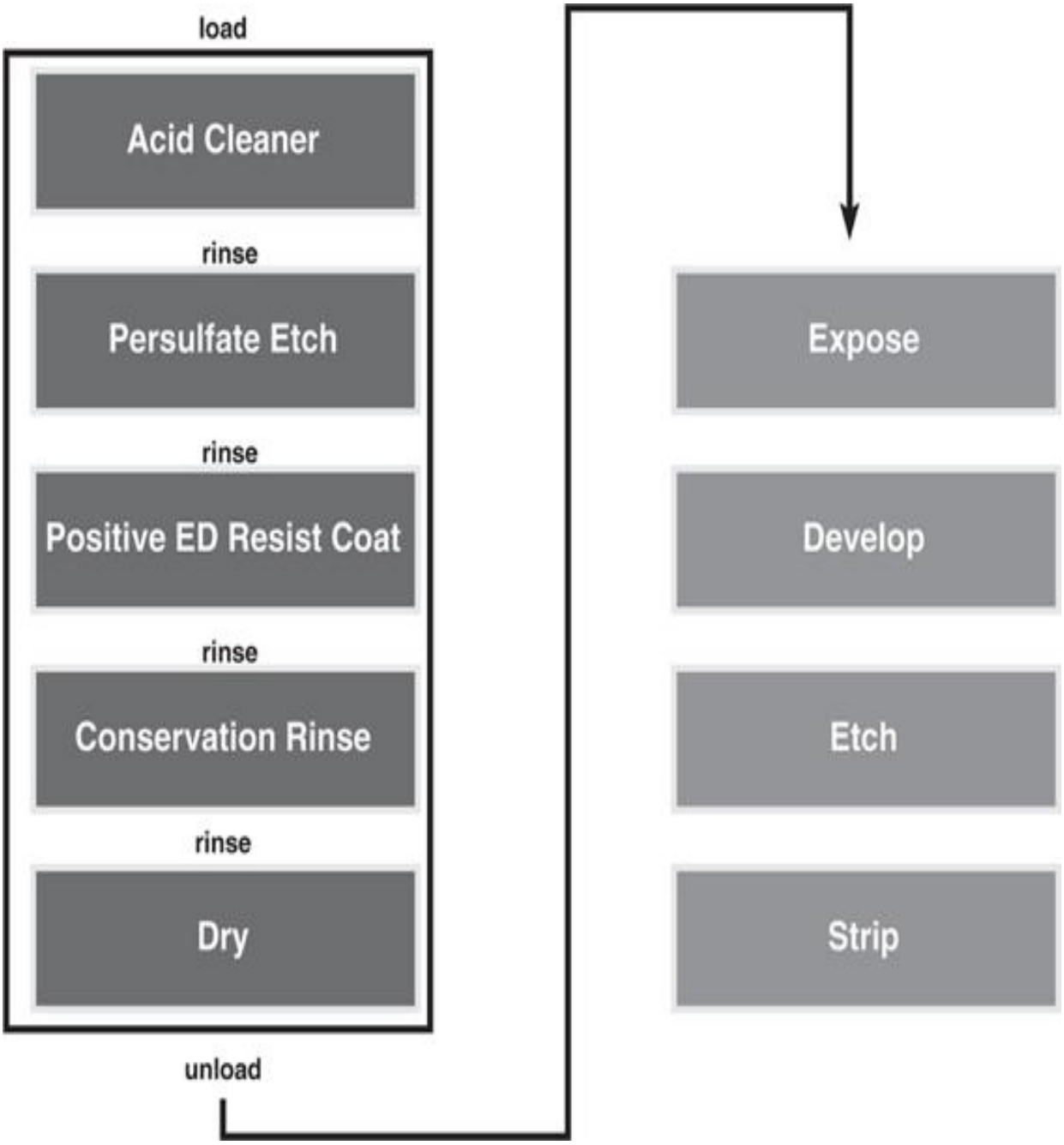


FIGURE 30.10 Configuration of an electrophoretic photoresist coater. *(Reprinted with permission of J. Dubrava et al., "Development of a Novel Positive-Working Electrodeposited Photo Resist Process for the Production of High Density PWB Outerlayers," presentation at the IPC Conference, San Diego, California, Spring 1995.)*

Rinsing removes loosely bound material that is returned to the plating cell after ultrafiltration to separate the

photoresist and the counterion. This aids in maintaining the ionic balance.

After a final water rinse, the panel is dried to remove water and consolidate the film. The film is now tack-free and can be imaged.

The chemical composition of the photoresist determines whether the equipment components are made from polyvinyl chloride (PVC), polypropylene, or polyethylene. Electrodes are made of stainless steel and encased in an ion-selective membrane that is flushed to prevent the build-up of counterion migrating there during deposition. The permeate and ultrafiltration unit is important for long-term stability of the coating solution. The coating unit is often enclosed in a clean environment to reduce the amount of particles found in solution or resting on the panel as the process proceeds.

30.6.3.8 Curtain Coating. This method is commonly used to coat liquid solder mask materials. The panel is conveyed at high speed through a vertically falling curtain of the liquid photoresist. The coating width can be adjusted so that the edges are not covered. Temperature and viscosity are controlled for reproducible coatings, and coating thickness is determined by the conveyor speed and the solution flow rate.[23] Material in the curtain is returned to the sump and reused, giving very efficient material utilization. This method is one-sided, and the first-side photoresist coating must be partially dried before coating the reverse side. Due to the extra handling required to coat one side at a time and the inability to convey very thin panels through the curtain at high velocity, this method has seen only limited use with photoresist.

30.6.3.9 Screen Coating. Another common method for coating solder mask with either a pattern or flood coverage is screen coating. The screen mesh size and the liquid solution viscosity set the wet coating thickness. The screen

is placed above the panel to be coated, and the material is forced through the openings in the screen onto the panel surface, where it forms a film.

Equipment is available for either single-side or double-side coating. With single-sided screen printers, special standoff are used on the screen bed to allow the panel to be flipped and coated on the reverse side. Without these standoffs the coating must be partially dried before the reverse side is coated. This causes a difference in the solvent content between the two sides that would result in nonuniformity for very precise lithography. In addition, the sequential nature of the coating allows debris and contaminants to be embedded into the first coating. Double-sided screen printers eliminate a drying step and minimize panel handling. The advantages of screen coating are that the equipment is relatively inexpensive to purchase and operate, “postage stamp” (small embedded areas) coating is possible, and waste is minimized.

30.6.4 Expose

Expose is the actual imaging step, reproducing the master pattern in the photoresist. The relief image is created after subsequent development. The expose process elements are phototool generation, registration of the phototool to the panel, and exposure through the phototool by the light source. Light-source alternatives include contact printing, either collimated or uncollimated; proximity printing; projection printing; and direct digital imaging (DDI) and laser direct imaging (LDI). The noncontact methods separate the phototool from the substrate, reducing yield losses caused by contamination between the phototool and photoresist. With laser direct imaging (LDI) and DDI, there is no phototool and the design data file of the master pattern drives the laser beam or quartz/LEDs to expose the photoresist.

Phototools are generated on either film or glass substrates, depending on the feature sizes that are being patterned and the durability required. The panel is either mechanically aligned, with pins holding the phototool with respect to the product, or optically aligned, with alignment features dictating the movement of the phototool and product. The alignment requirements are interrelated to those achieved at composite lamination and drilling. The registration scheme is contained within the exposure equipment.

30.6.4.1 Conventional Imaging

30.6.4.1.1 Artwork Generation. Polyester and glass are the substrates used for phototools. They differ in optical properties, dimensional stability, and durability. Silver halide on polyester is used to create first-generation phototools on a laser plotter. This image is often contact printed onto diazo on polyester to make the copies used in production. Optical absorbance of the different phototool materials versus wavelength is plotted in Fig. 30.11.

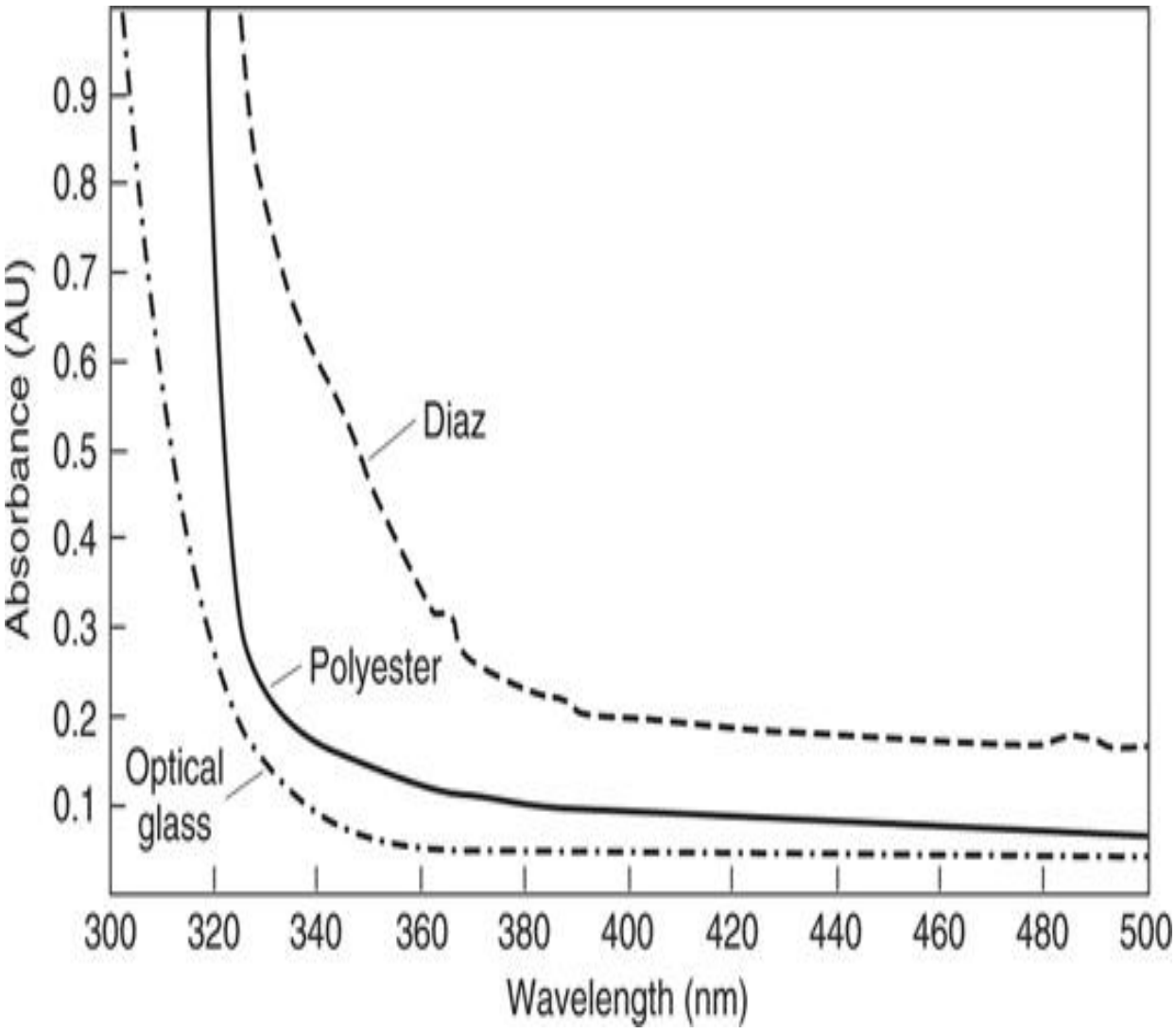


FIGURE 30.11 Optical absorbance of common phototool materials in the spectral region of PWB photoresist exposure.

Diazo phototools are the least expensive, and glass is the most expensive. Although the less-expensive materials have poorer transmission, this property is generally not limiting, except for applications requiring high intensity. Table 30.4 illustrates the impact on exposure time. Edge definition is a major difference among the options, as shown in Fig. 30.12. The photos illustrate that chromium on glass gives the sharpest edge definition. Edge definition is also affected by the pixel size of the phototool plotter and the spot's addressability (see the section on LDI). For applications that

use a low-contrast photoresist and poor light collimation, these differences are not measurable on the printed photoresist image or in the patterned conductor. However, for high-density imaging, edge definition is important, as is the dimensional stability of the phototool.

TABLE 30.4 Comparison of the Optical Transmission of Various Phototool Materials

Property	Diazo	Polyester	Glass
Absorbance at 365 nm	0.271	0.107	0.047
Transmission at 365 nm	54%	54%	90%
% increase in exposure time vs. glass	40	13	0

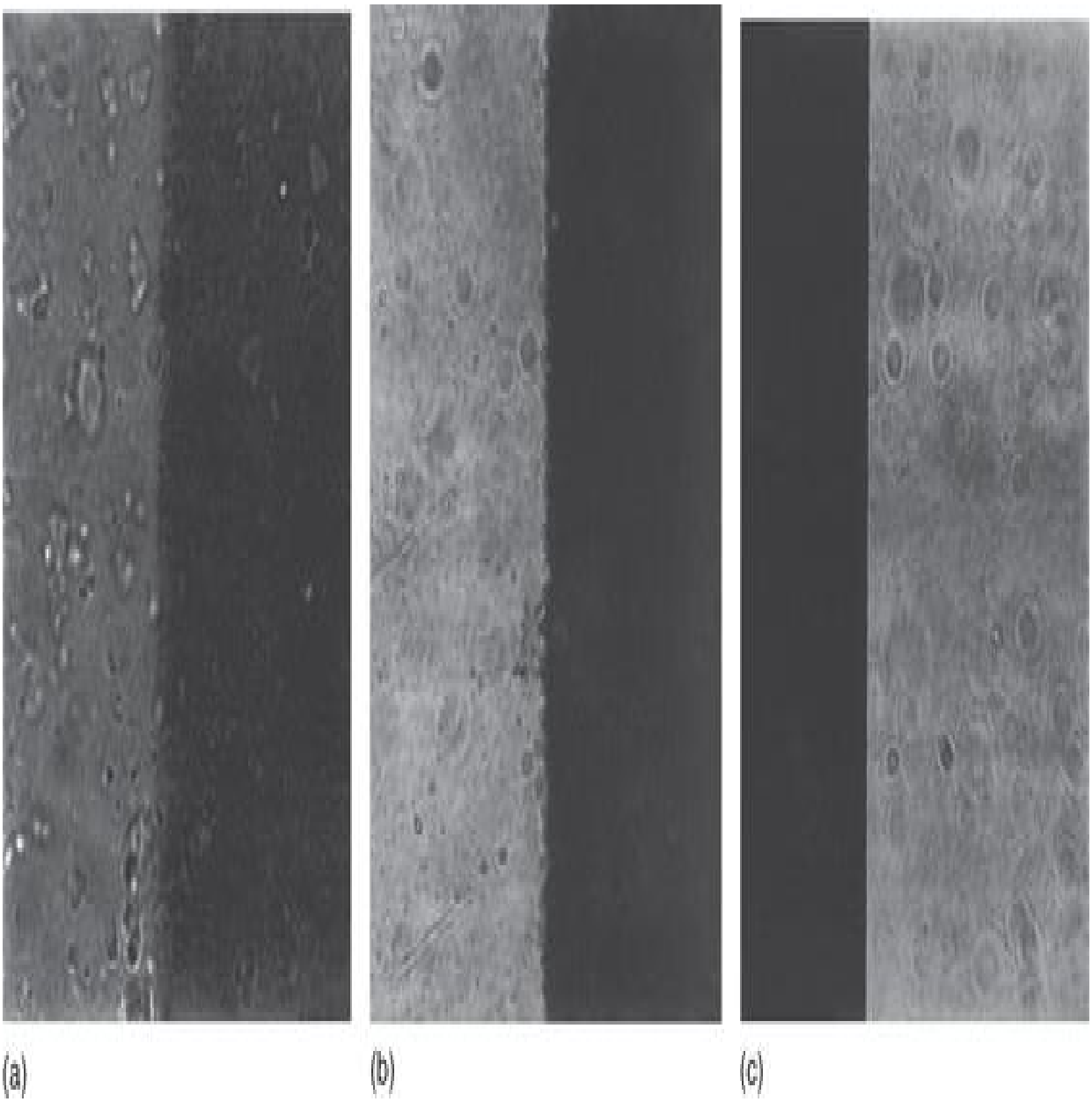


FIGURE 30.12 Optical micrograph of the image edge of common phototool materials, 1600×: (*a*) diazo on polyester, (*b*) silver on polyester, (*c*) Cr on glass.

Film dimensions change more rapidly with temperature than glass and are also affected by humidity. Careful control of both temperature and humidity is required throughout the life of a phototool (see Table 30.5).

TABLE 30.5 Dimensional Stability of Phototool Substrate Materials with Respect to Temperature and Relative Humidity

Substrate	Expansion Coefficient, ppm/°C	Expansion Coefficient, %RH/°C
Soda lime glass	9.2	0
Low-expansion glass	3.7	0
Pyrex	3.2	0
Quartz	0.5	0
Polyester	18	9

Source: Kodak Technical Literature (ACCUMAX 2000) for polyester film; *Tables of Physical and Chemical Constants,* Longman, London, 1973, p. 254; H. J. Fischbeck and K.H. Fischbeck, *Formulas, Facts and Constants,* Springer-Verlag, Berlin, 1987, for glass data.

The durability of the phototool is also important, especially for use in a manual contact printer. Damage depends on phototool handling, the exposure tool, the cleanliness level of the operation, and the surface of the product being contacted. Commonly, glass artwork is usable for 100 to 400 contacts with repair, while film artwork is usable for 20 to 50. For large numbers of the same part, number cost per contact may actually be lower with glass artwork, while for prototype parts, film artwork is ideal. However, the majority of production panels are exposed with film artwork. High-density applications such as chip scale packaging and multichip modules using laminate (MCM-L) may require glass artwork. The requirements of the product determine the type of phototool that should be used.

30.6.4.1.2 Registration. The image is placed on the panel with respect to a point of reference so that the image is well aligned to previous and future features. In multilayer construction, the innerlayer images are aligned front to back for successful lamination and drilling of the plated through holes (PTHs). The outerlayer image is then aligned to the

drilled holes. The same considerations are relevant for single-layer boards. Thus, accurate alignment is clearly part of the imaging process and also depends on knowledge and control of the dimensional stability of the product. The image must be scaled to match the dimension of the board at the exposure step; for multilayer structures with several photolithographic steps, a series of dimensional measurements are required prior to product manufacture.

Mechanical registration entails the use of fixed pins or other mechanical devices to hold the phototool and the panel in place during exposure. The actual configuration of the pins and their shape varies. Both two- and three-point systems are used. The three-point systems well define the center location since they are located at the extremes of the area to be patterned.

The shapes of the pins are either round or elongated with one flat side. In the latter case, the flat side defines the edge, while round pins center within the hole in the panel and phototool.

Film artwork alignment holes are punched with respect to the product pattern by plotting alignment targets as part of the product pattern and optically aligning and punching a slot or hole. The edges of the punched feature wear, and registration will deteriorate with use. For glass artwork, the glass is drilled at the alignment locations and a bushing is placed at the center of the hole. The pin is then inserted through the bushings in top and bottom artwork and through the panel. With use, the bushings do move and must be reset for maximum reproducibility.

LDI and DDI systems print a target on the reverse side of the undrilled panels to allow for front to back registration. For drilled panels, with multiple drill operations, a complex target is drilled to allow the LDI registration system to consider all the drill files. Some DDI systems can memorize the locations of *ALL* the holes (front and back) and can

manipulate the artwork in real time to have “perfect” registration.

30.6.4.1.3 Exposure Control and Measurement. The role of exposure is to change chemically the photoresist and its solubility in the developer solution. The appropriate energy dose is determined experimentally by measuring the combination of dose and development that is needed to produce features with straight sidewalls. The photoresist is coated on an optically clear substrate and exposed from the backside. Contrast curves, plots of the log of the exposure dose versus the thickness of the film remaining, are used to identify the functional cure point—for example, the dose that loses thickness less than 10 percent (see Fig. 30.13).

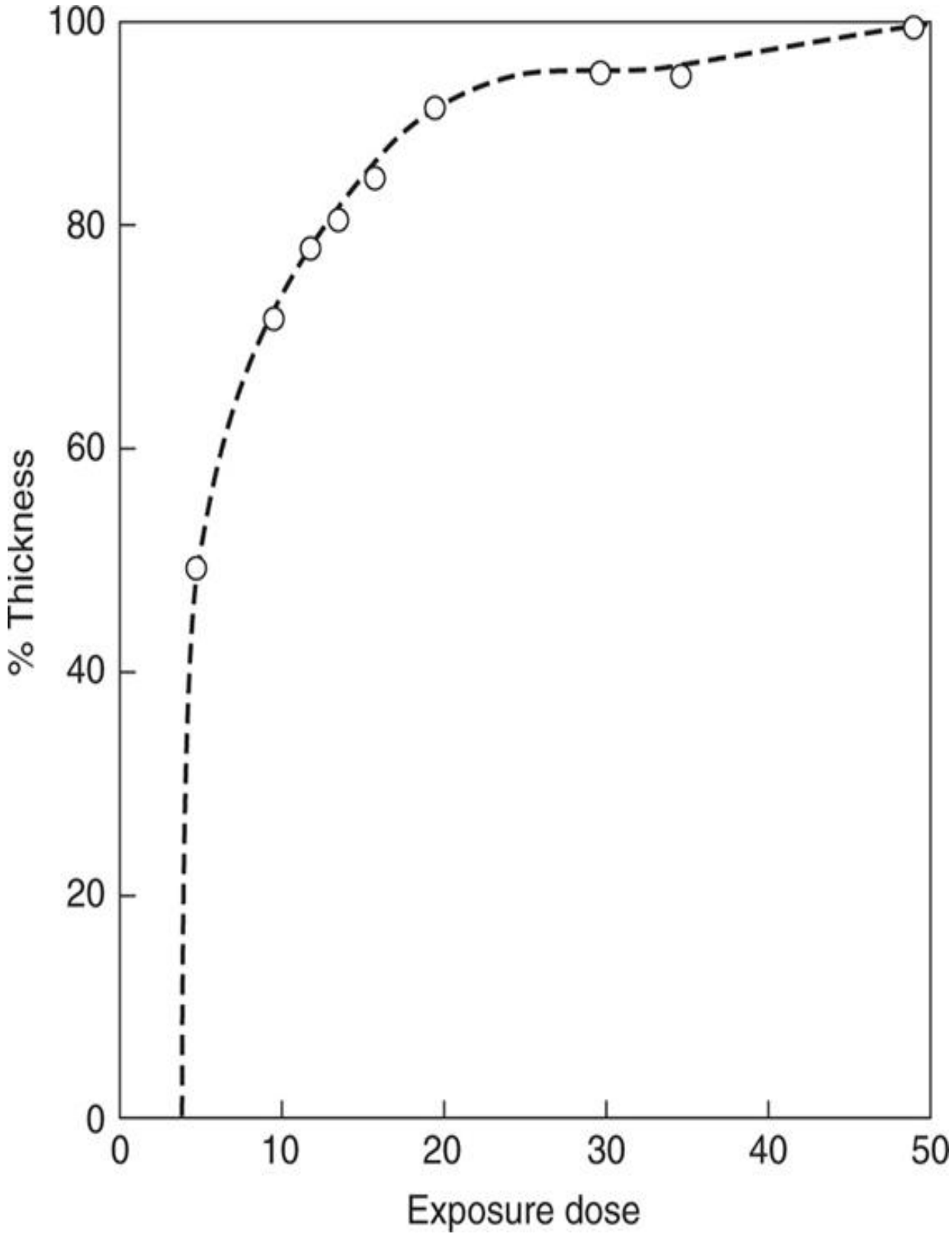


FIGURE 30.13 Contrast curve for a negative-acting dry-film photoresist, percent film thickness remaining versus exposure dose (mJ/cm^2).

Exposure in the region of stability ensures that the base of the material has reacted. Step wedges, film strips with a series of neutral density filters, are also used to determine appropriate exposure doses. The dose is varied to obtain photoresist residue on the area with the manufacturer's recommended step value. This technique depends on appropriate and consistent developer conditions.

Step wedges are often used to control the expose or expose-and-develop processes.

The energy incident on the photoresist is the product of the lamp intensity and the time of exposure:

$$\text{Energy} = \text{intensity} \times \text{time} \tag{30.1}$$

Thus, the exposure dose can either be measured directly by using an integrating radiometer or indirectly by measuring exposure time and light intensity with a radiometer. The radiometer response must be matched to the spectral output of the light used so that representative measurements are made (see Fig. 30.14). Most exposure equipment provides the option of using either direct energy or time measurement. With a stable light source, both approaches are equally reproducible.

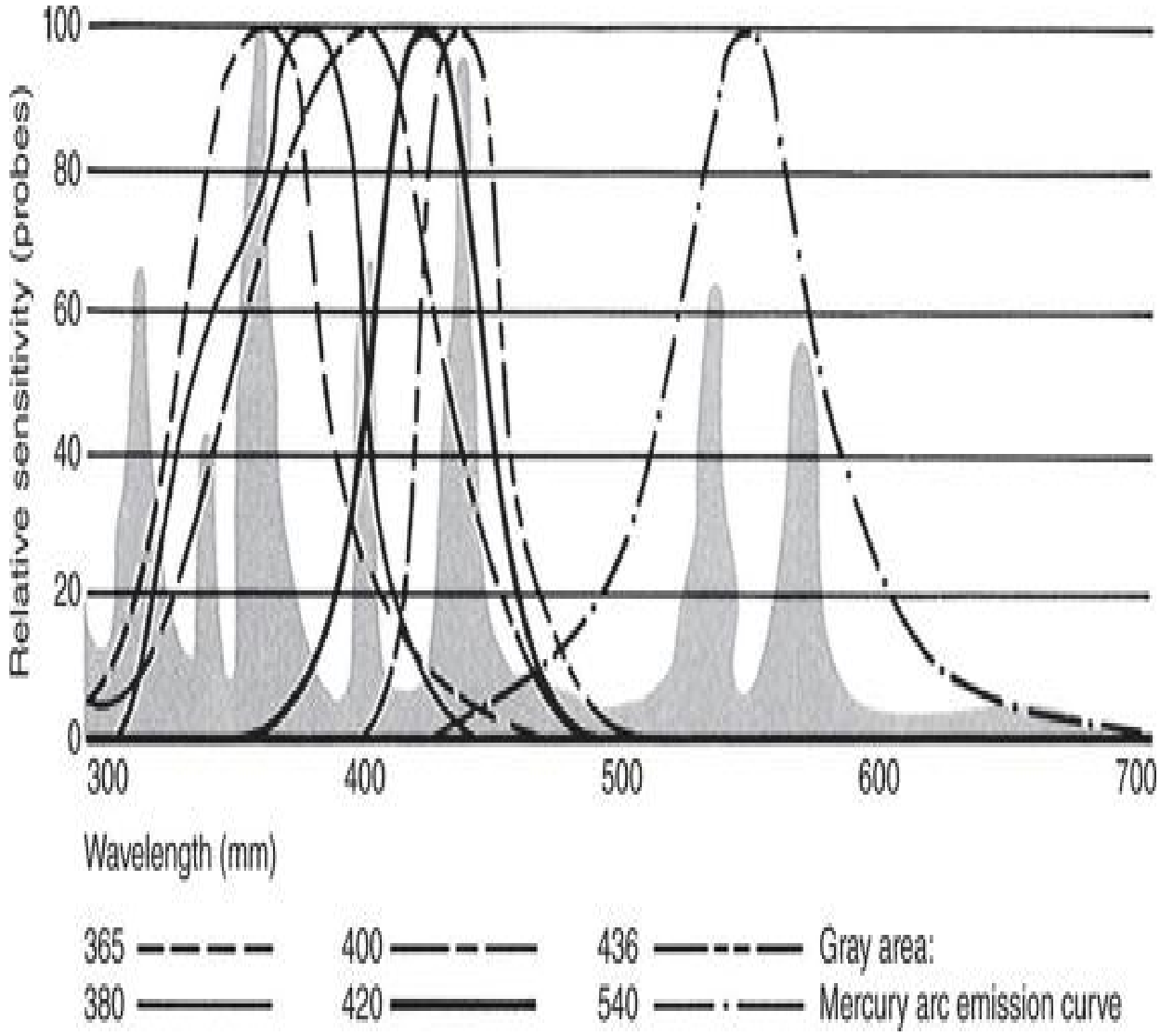


FIGURE 30.14 Output of Hg/Xe light source and radiometers. (*Reprinted with permission of Optical Associates, Inc., Milpitas, California, Technical Literature*.)

30.6.4.1.4 Contact Exposure Tools. This equipment places the phototool and the panel in direct contact and draws a vacuum between the pieces for hard contact. A range of light wavelengths is used, often from a mercury or mercury/xenon light source, which is stable and has a high intensity output at ultraviolet and visible (UV/Vs) wavelengths (see Fig. 30.14). The light is distributed over the area to be exposed by placing the board at a distance from the source, either noncollimated or collimated by the use of optical elements, as shown in Fig. 30.15. Collimation refers

to the angle of incidence of the light onto the photoresist, and it is critically important for fine-line images. Defining fine spaces is the challenge for both additive and subtractive conductor formation, and exposure under the opaque areas cannot be tolerated. The lamp intensity for noncollimated sources is greater, and therefore less time is required to expose the panel. Process throughput is noticeably enhanced for photoresists requiring a large dose.

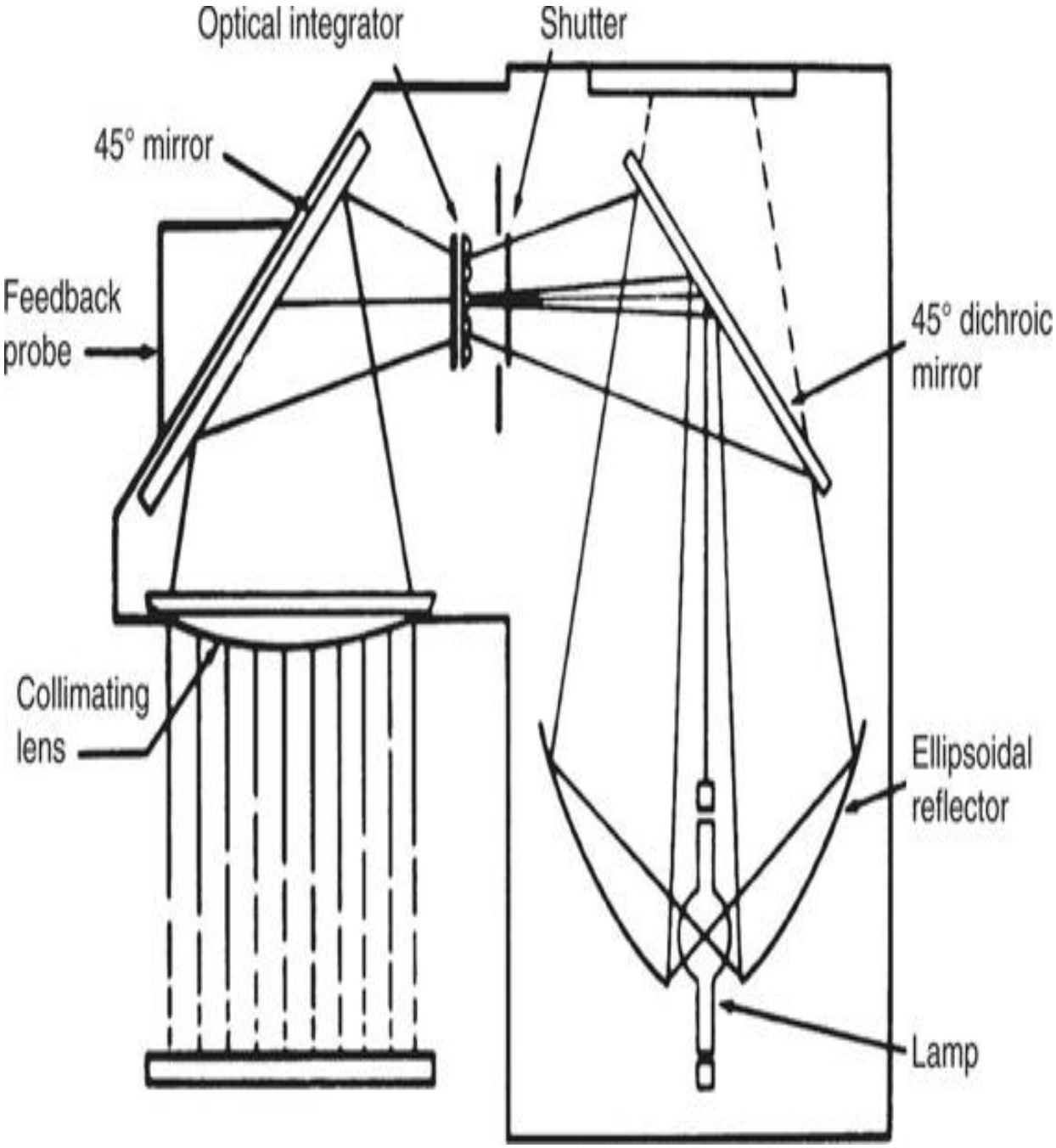


FIGURE 30.15 Configuration of lamp and optics for a collimated contact printer. A noncollimated source is identical except for the collimation lens in the lower left. (*Reprinted with permission of Optical Associates, Inc., Milpitas, California, Technical Literature*.)

In addition to collimation, good contact between the phototool and the panel is the most important factor to control in fine-line formation. Any gap will allow exposure

under the opaque, resulting in poor linewidth control and reduced resolution. The sensitivity to off-contact exposure varies among photoresists, and newer resists are formulated with increased off-contact latitude.[24] Since the lamp's spectral output degrades over time, the lamp must be routinely replaced to maintain a stable photoprocess. The exact frequency for replacement depends on the line and space definition required, but the lamp life is typically 1000 h.

Failure to replace a lamp can result in it exploding and damaging the optical elements in the exposure unit, which is far more costly than routine maintenance.

30.6.4.1.5 Noncontact Exposure Equipment. Semiconductor imaging demonstrated the yield limitations in using contact-exposure equipment. Noncontact methods had to be developed to achieve acceptable conductor yield as critical dimensions decreased to 0.18 µm and below.

The PWB industry is following this evolution, driven by the increased demand for products with fine features of 25 µm and less. Semiconductor tool concepts cannot be used directly due to important differences between IC and PWB products, namely the physical size of the substrate and features to be imaged and the flatness of the substrate. The key to noncontact methods is the use of appropriate optics for clear image placement in the photoresist (Fig. 30.16), even if the image transfer function has degraded. For PWB applications, this includes the depth of focus to allow for panel warpage and the resolving power, given the contrast of the resist. The following approaches address these concerns and are viable alternatives to contact printing.

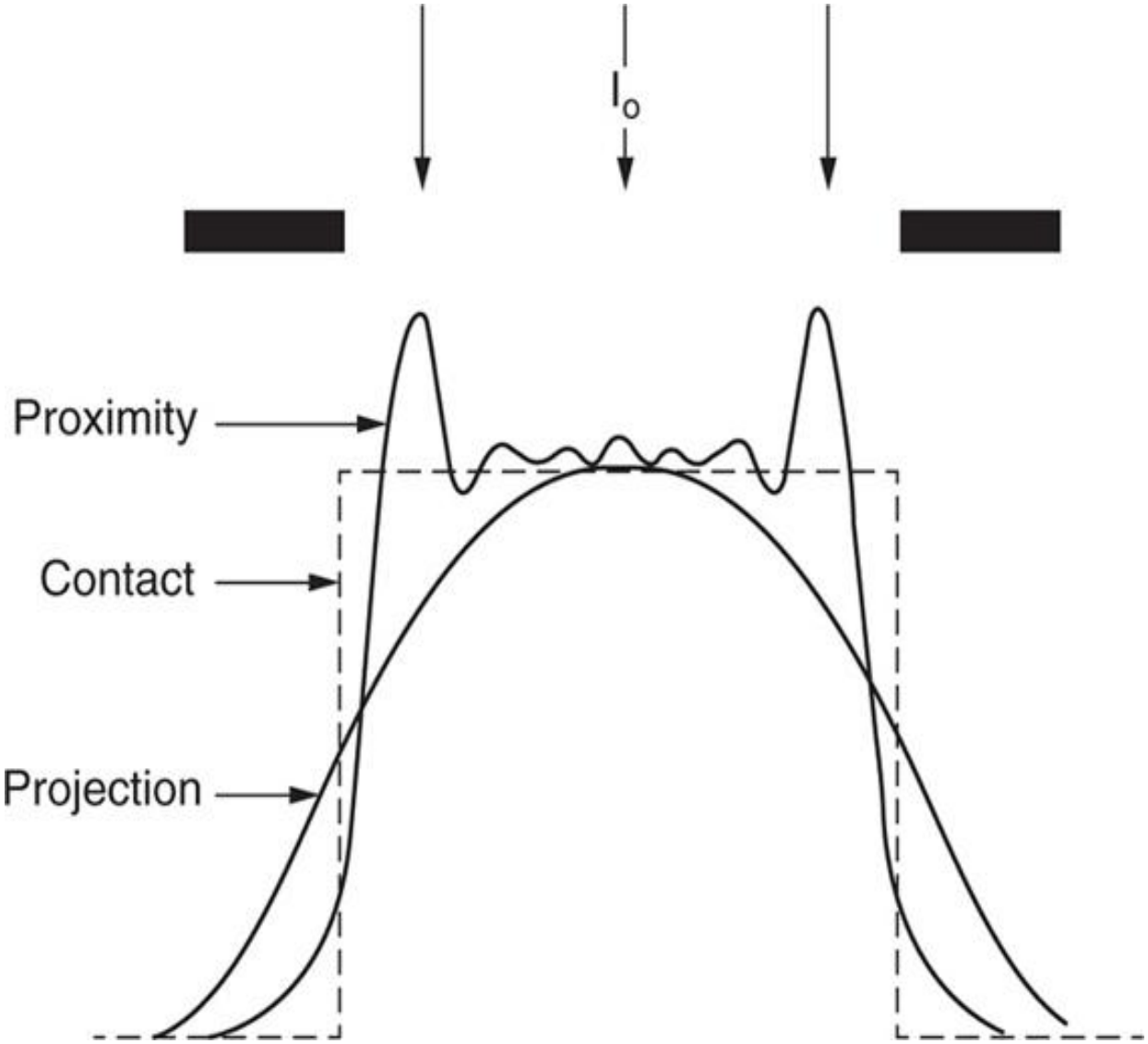
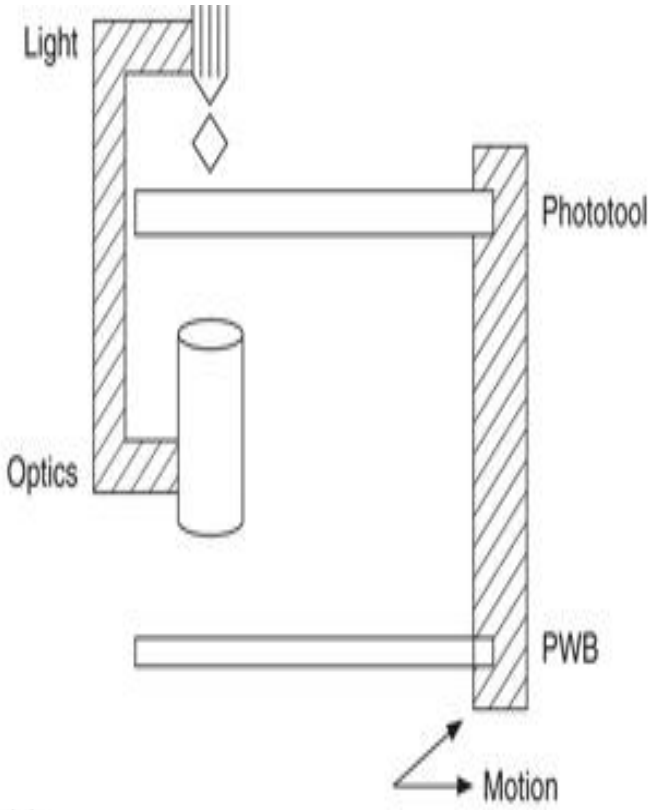


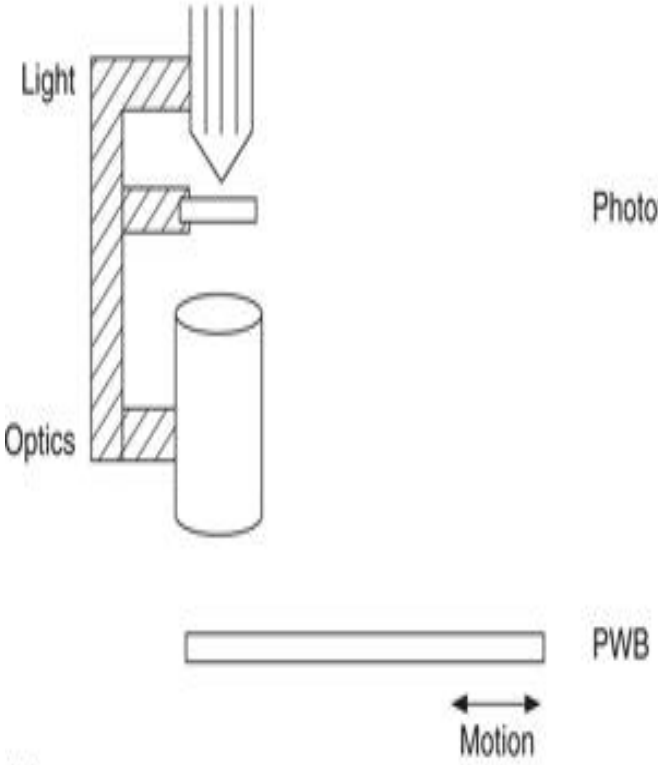
FIGURE 30.16 Image transfer for contact, proximity, and projection printing.

30.6.4.1.6 Proximity Printing. This is the oldest method for off-contact printing and requires no modification to the equipment optics. The phototool is held out of contact from 125 to 500 µm. The image in the photoresist suffers since the distance between the phototool and the part allows exposure under the opaque area and imaging of debris on the phototool. Nevertheless, resolution as fine as 75 µm has been reported for proximity printing with thin coatings of liquid resist.[25]

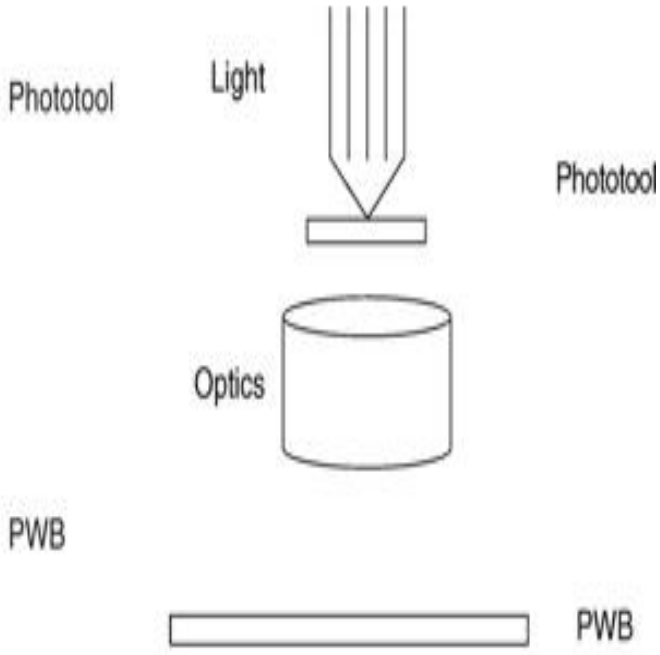
30.6.4.1.7 Projection Printing. Three approaches are possible for this technique: scanning, stitching, and magnified projection printing. Scanning and stitching evolved from semiconductor and MCM-D thin-film technology, where smaller, flatter substrates are used. They require movement of the phototool and/or the substrate during exposure. Magnified projection imaging is unique to the PWB application and has no moving optical components. A schematic of all three systems is given in Fig. 30.17.


Light
Phototool
Optics
PWB
Motion

(a)


Light
Optics
PWB
Motion

(b)


Phototool
Light
Phototool
Optics
PWB

(c)

FIGURE 30.17 Configuration for projection imaging equipment: (*a*) scanning, (*b*) stitching, and (*c*) magnified.

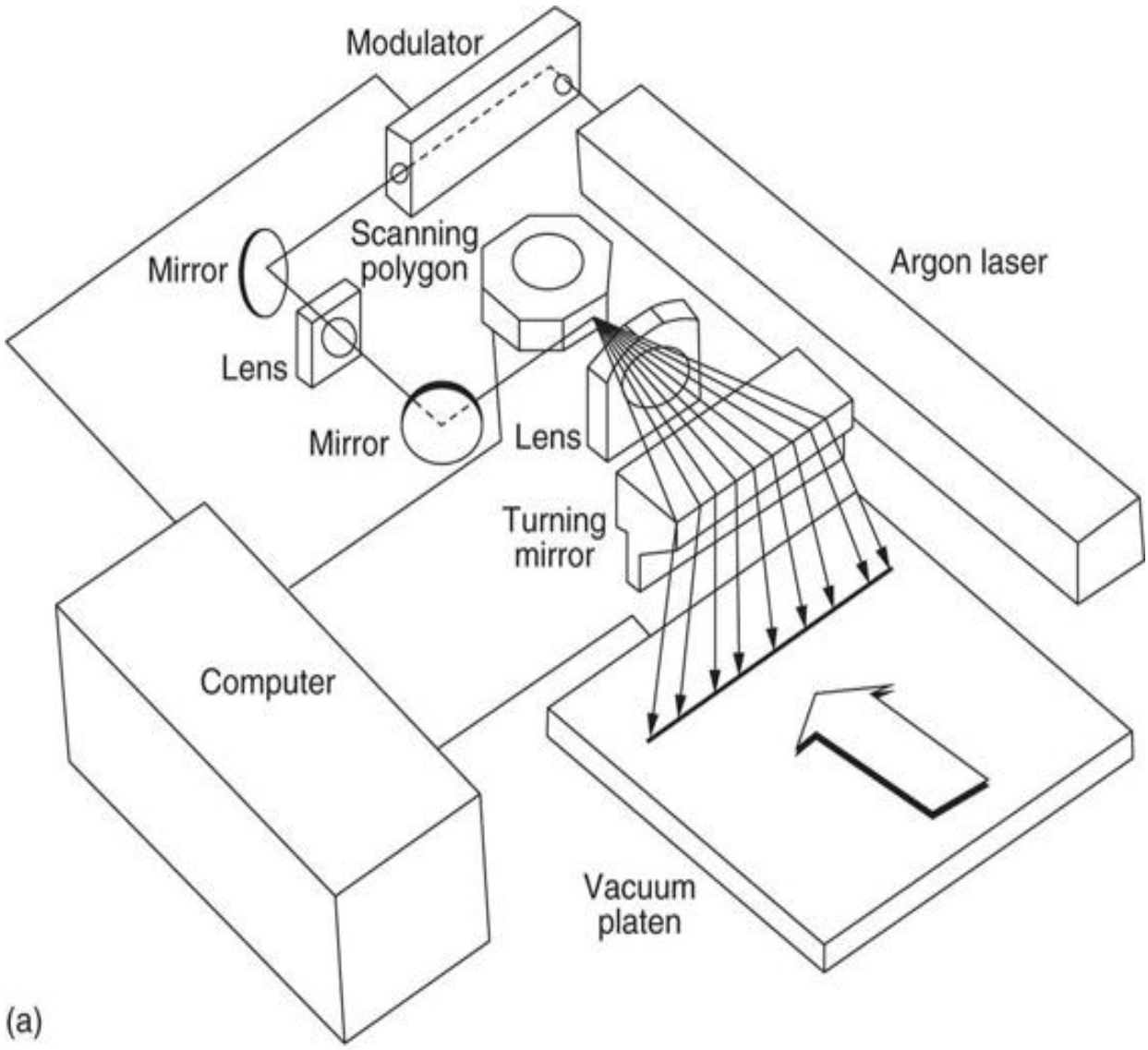
- The scanning printer requires the synchronized movement of the part and the phototool during exposure. Precise alignment of the two pieces must be maintained during the motion. Periodic adjustment for flatness is usually required since this equipment has a small depth of focus. For typical PWB formats, a large phototool is needed, requiring expensive glass phototools for their flatness, rigidity, and sharp line definition. This exposure technique has demonstrated high resolution over a large, relatively flat area using a high-contrast resist.[26] Few PWB applications exist, but the technique is useful for flat panel display manufacture.
- Stitcher projection printers are step-and-repeat tools that use a repeating image or "stitch" together several images. The artwork generation and management in the equipment are complicated, which has hampered these printers widespread use for large panels. The usual active area size as defined by the optics is approximately 6 × 6 in. Thus, for a standard 18 × 24 in panel, 12 artwork changes are required to expose one side. These systems have very high resolving capability and large depth of focus. Again, glass artwork is used, but these smaller plates are easier to generate and use than in a scanning projection printer.
- The magnified projection imaging concept was first demonstrated in the late 1980s with the SeriFLASH exposure tool, utilizing 436 nm illumination and a 5 × 5-in liquid crystal display as the phototool. The image was magnified six times to expose an 18 × 24-in panel, but demonstrated photoresist definition was limited to 125 μm since the liquid crystal features were one-sixth of the final conductor width. The equipment was subsequently modified for 365 nm exposure with a glass phototool to

improve resolution. Fifty-µm line and 63 µm space resolution has been demonstrated.[27] The exposure time required is similar to that of contact exposure equipment. With optimized optics, this may become a high-resolution tool that utilizes conventional photoresist and phototools.

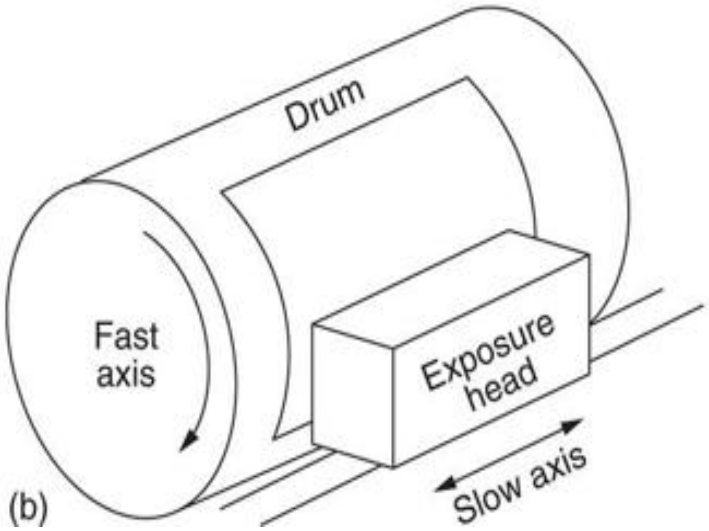
30.6.4.2 Laser Direct Imaging. The LDI method of exposure provides the ultimate in flexibility for customized pattern compensation factors and for engineering changes to the product design since it does not require a phototool. Systems introduced in the 1980s used an Ar^+ laser with visible optics, requiring specialized photoresists that were sensitive to visible light. Improved Ar^+ systems relied on the UV wavelengths, making it compatible with conventional photoresists. However, high-speed photoresists were needed to achieve the productivity for high-volume production. Concerns about the lifetime (3000 to 5000 h) and power consumption (60 to 80 kW) of gas lasers led to development of solid-state laser systems at various wavelengths.[28,29,30] The initial solid-state laser systems used 355 nm with a polygon mirror to scan the panel. LDI systems have used digital mirror devices (DMD) instead of polygon mirrors and image at a wavelength of 405 nm. Filters are used to block 355 nm light, extending the lifetime of the DMD device. Due to the small size of the individual mirrors, about 1.5 µm, DMD technology provides better resolution than an 8000 dpi polygon mirror system. However, the area coverage is smaller and several DMDs working in parallel are needed to expose a PWB panel. Systems have also been introduced that use no photoresist at all, laser ablating either tin for use as an etch resist or physical vapor deposition (PVD) copper on polyimide for use as a plating base.[31,32] In addition to varying in laser type and wavelength, specific equipment designs differ in optics, either single- or multiple-beam operation; platen design; single- or double-side exposure; pixel shape; and spot size and resolution.

Multiple-beam operation increases exposure productivity, a key requirement for economic feasibility in large-volume manufacturing. Target production rates for the various systems ranged from 60 to 180 panels per hour (18 × 24 in with 50 μm features). Initially, LDI systems have been used primarily for prototype and small-lot, quick-turn production of high-density boards. For these applications, savings are achieved due to artwork elimination and reduced setup time. For volume production of medium- to high-technology boards, it is possible to achieve an economic return through yield savings and the ability to produce designs that had not been technically or economically possible with conventional imaging.[33] LDI technology makes it possible to scale the electronic data and compensate for dimensional changes in sequential build-up (SBU) structures. Although the UV systems can expose conventional photoresist, use of high-speed photoresist is needed to maximize tool throughput. Most LDI systems use a flatbed platen design and can image both innerlayers and outerlayers.

Systems with an external drum architecture, similar in design to laser photo plotters, are limited to innerlayers because the panel must have sufficient flexibility to conform to the drum (Fig. 30.18). The pixel shape can be either square or gaussian. Square pixels are made up of many point sources of light and can theoretically achieve perfect stitching. However, in real systems there is intensity variation due to mechanical vibration and edge rounding. Gaussian pixels use a single-point source and may have less intensity variation. Due to the diffraction-limited nature of light, greater depth of focus can be achieved.[34] Figure 30.19 illustrates that imaging with a smaller laser spot size gives steeper aerial image sidewalls, increasing process latitude.[35] In addition to spot size, addressability of the beam is important in determining the system resolution, as shown in Fig. 30.20.


Modulator
Scanning polygon
Mirror
Argon laser
Lens
Mirror
Lens
Turning mirror
Computer
Vacuum platen

(a)


Drum
Fast axis
Exposure head
Slow axis

(b)

FIGURE 30.18 Schematics of laser direct imaging equipment: (*a*) flatbed platen, (*b*) external drum.

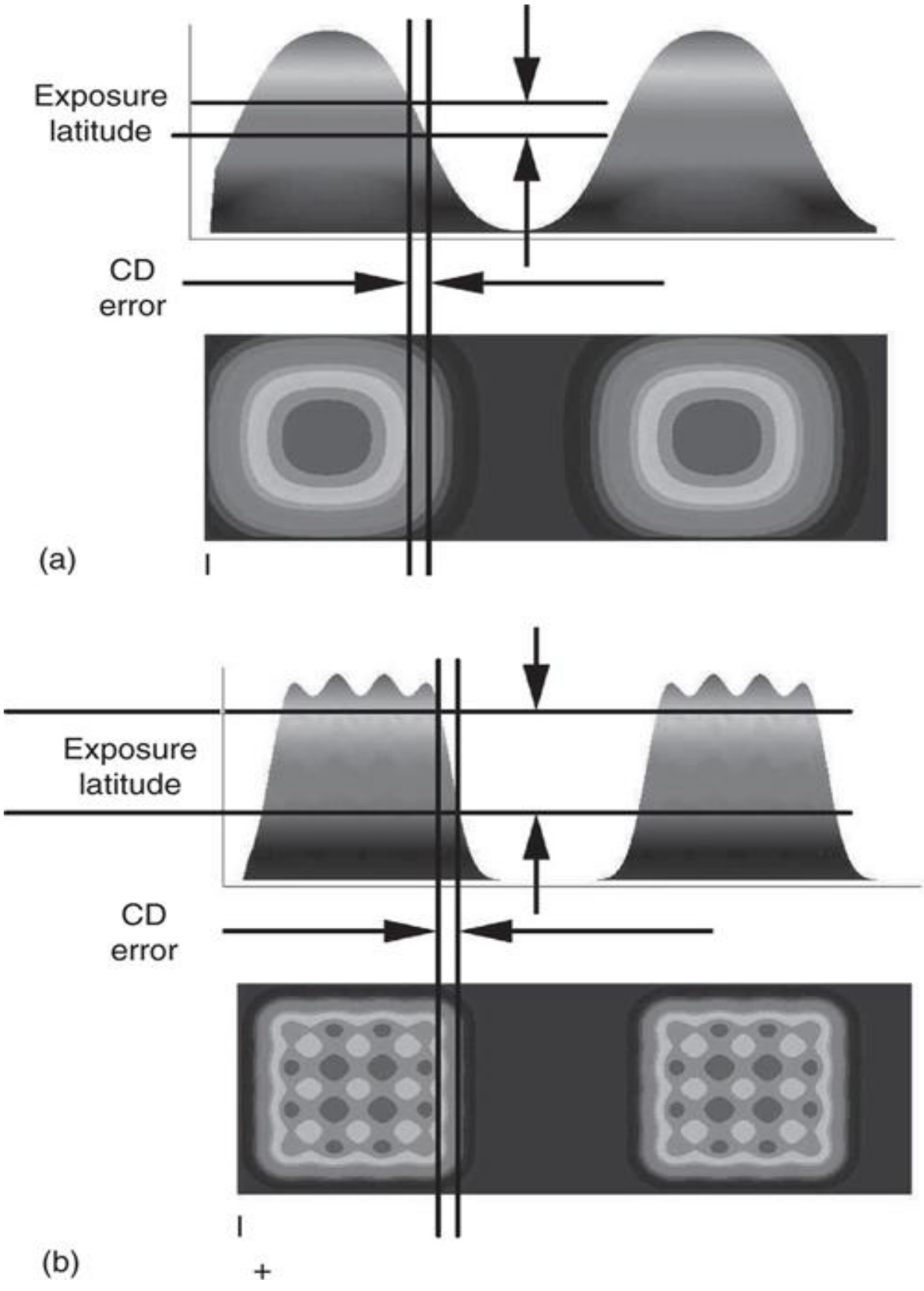

Exposure
latitude
CD
error
(a)
I
Exposure
latitude
CD
error
I
(b)
+

FIGURE 30.19 Computer simulation of aerial image for a 25-μm feature: (*a*) four 12.5-μm laser spots on 6.25-μm pixel spacing, (*b*) four 6.25-μm laser spots on 6.25-μm pixel spacing.

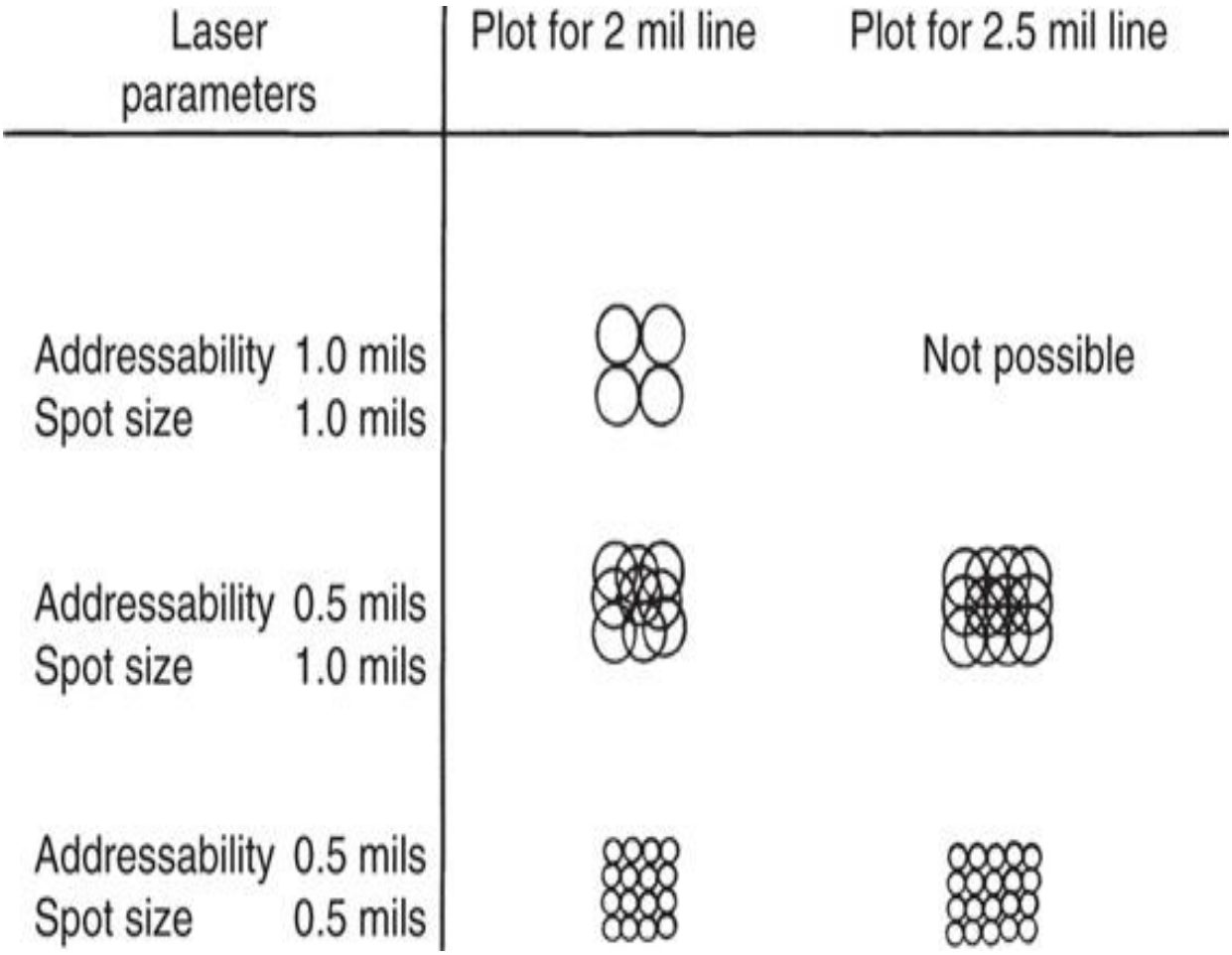


FIGURE 30.20 Final image dimension as governed by spot size and addressability of a laser plotter or laser direct exposure tool.

In selecting an LDI system, you must consider both the capital cost and operating cost. However, the critical factor is that the equipment combined with the photoresist material is capable of achieving both the resolution needed for the product mix and the productivity needed for the production volume. Photoresists for LDI are available that are compatible with the various metallization processes.[36]

30.6.4.3 Direct Digital Imaging. Very fine line imaging (<10 µm lines/spaces) has the growing need for

- High through-put using conventional photoresists
- "True position" imaging of small features over large formats
- Improved layer-to-layer registration
- Incremental-expandable image resolution and size
- The "scaling" of an image, i.e., changing the image dimensions and/or shifting the image for best-fit registration to a shifted or distorted reference image, on group or individual board basis
- Lower cost of ownership for an direct imaging system

These needs are now met through improved capabilities of the direct digital imager, with longer life and lower power consumption of conventional or "improved" UV lamps, LEDs or lasers and compatible with the vast majority of photoresists for primary imaging as well as soldermasks with reasonable photospeed.

Some attempts to introduce UV- LDI exposure machines (Etec DigiRite 2000, Automa-Tech DI2700, Barco Gemini) were abandoned but others are still being actively sold by Pentax' DI-2080, Hitachi DE-F, ORC, Fuji Film INPREX and notably Orbotech's solid state Paragon™-Xpress9 imager. The DDI units come from Maskless Technologies, Dainippon Screen Mercurex LI-9500, KIWO Screen Setter and Hitachi DE-S and DE-H series.

A typical DDI unit using high-pressure mercury UV light (as seen in Fig. 30.21) will have typical characteristics of

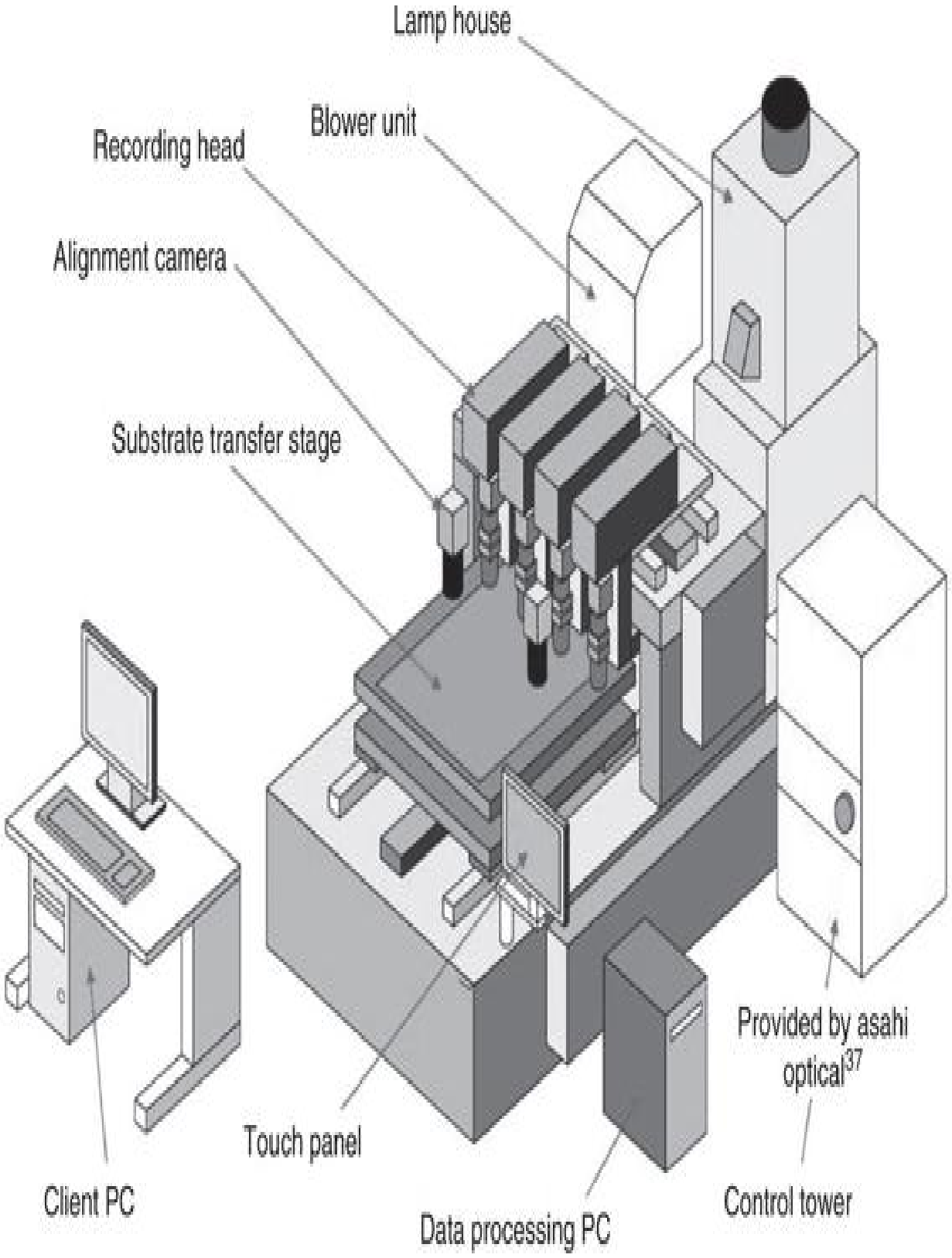
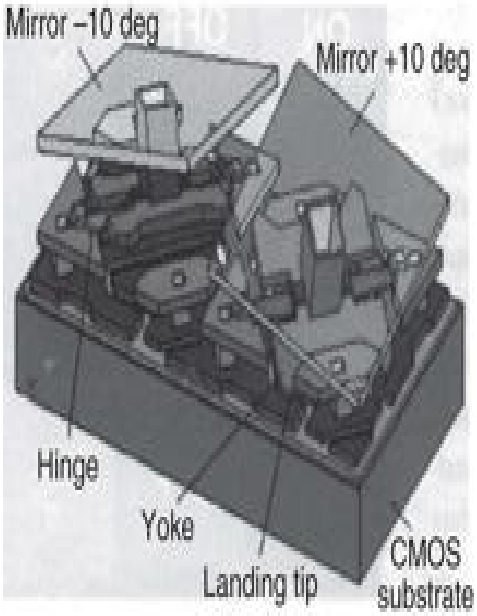


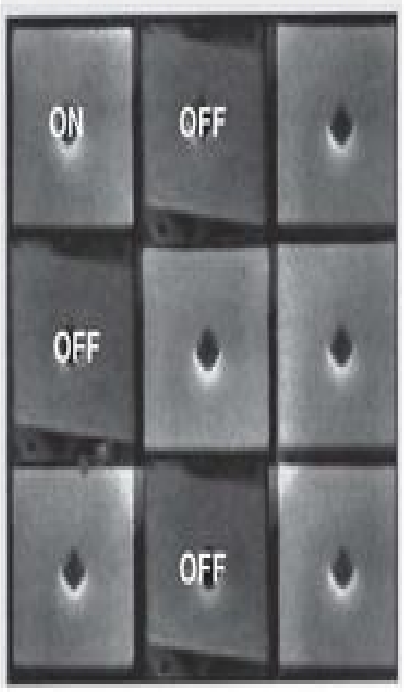
FIGURE 30.21 Next generation digital direct imaging (DDI) uses various light sources and the ubiquitous TI DMD mem-micromirror system to direct the rich UV

light.

- Dot positioning: DLP^{TM} (digital micromirror device in Fig. 30.22)

DMD


Mirror −10 deg
Mirror +10 deg
Hinge
Yoke
Landing tip
CMOS substrate


ON
OFF
OFF
OFF

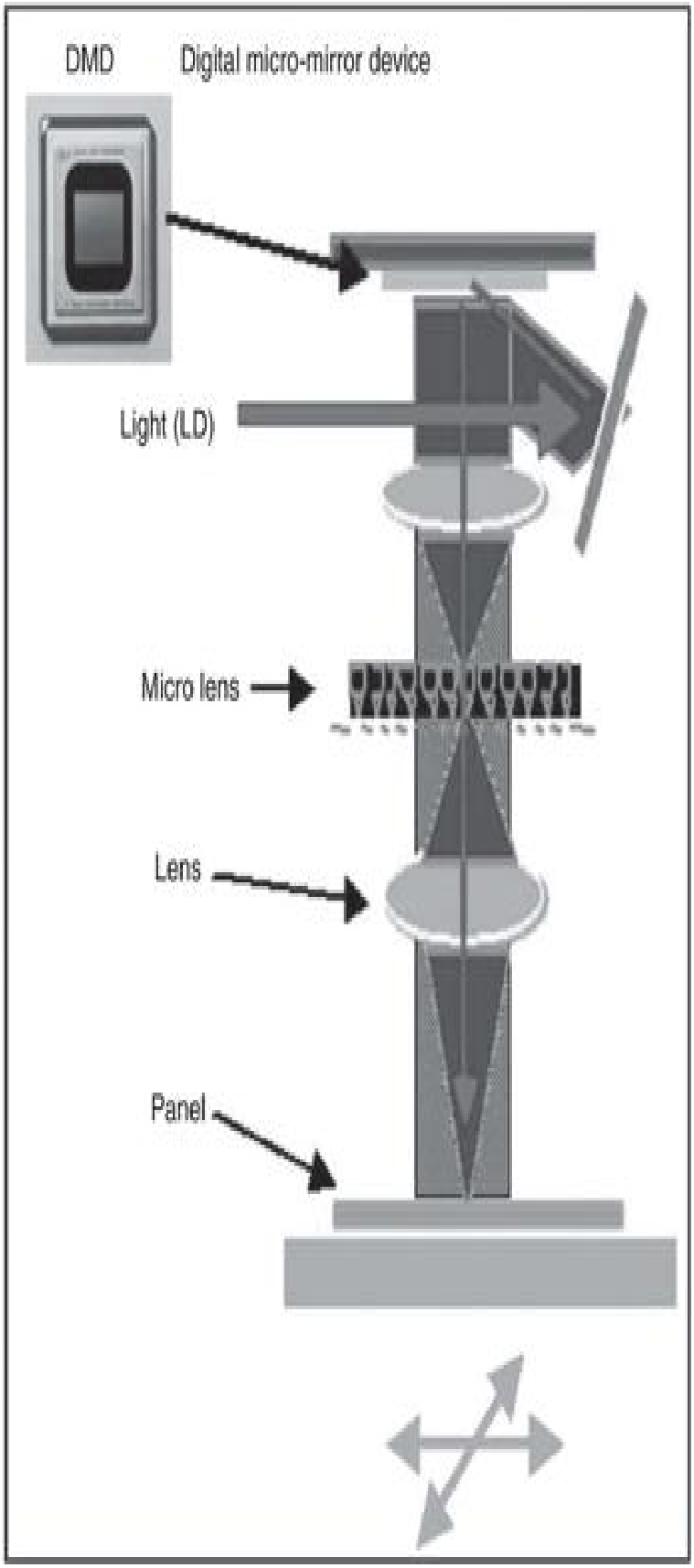

DMD
Digital micro-mirror device
Light (LD)
Micro lens
Lens
Panel

FIGURE 30.22 All have in common a way of directing the UV light thru the DLP/DMDs down onto the panel surface.

- Minimum feature size: 15 µm L&S
- Edge roughness (line width variation): ±1 µm
- Position accuracy (repeatability): ±1.0 µm
- Side-to-side registration: ±10 µm (3 sigma)
- Exposure time: 20 s for 530 × 650 mm
- Source wavelength: 350 to 425 nm (i-line to h-line)
- Source life: >3 years
- Other features: auto scaling/auto numbering/automatic loader + unloader

In their various configurations, they can be customized for (1) high output (up to 5000 panels per day), (2) fine-pitch (down to 8 µm L/S), or (3) combination of fine L/S and high-output (20 mm L/S and 2 panels per minute).

30.6.5 Develop

In this process step, the solubility difference between the exposed and unexposed areas of the photoresist creates a relief image of the master pattern. The panel is immersed in an appropriate solvent, and the process conditions are adjusted to control the clearing time for dissolving the unexposed areas for negative photoresists or exposed areas for positive ones. Total dwell time is set to approximately double the time to clear, commonly called a 50 percent breakpoint. Solution concentration, temperature, and agitation are key variables. The resulting photoresist images should be distinct, with vertical sidewalls. Failure to achieve this indicates that one of the previous steps requires adjustment. For images larger than the phototool dimension, the cause is either incomplete development, overexposure, or poor contact during exposure. For images that are smaller

than expected, either the exposure dose is too low or development is too aggressive. Distorted images can be caused by problems with preclean, application, or exposure. The common equipment for developing is spray conveyorized, either horizontally or vertically.

Additives are used in the developer solution to prevent foaming. The solution is filtered to remove resist particles and either replenished with fresh solution to maintain a consistent dissolved resist content and solution concentration or operated continuously for a certain amount of product and then replaced. Waste-developer solution is treated (aqueous and semiaqueous) or distilled and reused (solvent). Rinsing is important in stopping the dissolution and, for aqueous photoresists, water with a high-mineral content often improves the resist image and the conductor yield. Tank systems can also be used with photoresists that have a wide-process latitude. Ultrasonic agitation was formerly used to aid in the dissolution.

There are additional steps that improve the resist removal in the line channels and the conductor formation yield. Plasma treatment has been used effectively to improve product yield, especially with respect to shorts in a print-and-etch process. In addition, for some aqueous-developable dry films, a heat treatment after exposure has improved the space definition, and spaces equal to or smaller than the resist height have been resolved. Thus, these process steps ensure that tight resolution requirements can be met.

30.6.6 Strip

After the pattern transfer has been completed, the photoresist is removed from the substrate using equipment similar to that used for development. The stripping solution swells and dissolves the photoresist, stripping it either in sheets or as small particles. The equipment design must

effectively remove and separate the skins. Brushes and ultrasonic agitation are added to aid in the resist removal. As with developing, filtration is important to keep the spray nozzles clean and keep fresh solution reaching the panel. For stripper chemistries that oxidize the copper, an antitarnishing agent is often added either to the stripping solution or as part of the rinsing.

30.7 DESIGN FOR MANUFACTURING

As design features are continually reduced to produce higher-density interconnects, tighter control of every step in the conductor formation process is required to achieve high yield. The maximum possible yield with an etching or plating process depends on the conductor dimensions such as the conductor pitch in terms of line and space, the conductor thickness, and the size and shape of the capture pads around plated through-holes (PTH) and vias.

30.7.1 Process Sequence: Etching versus Plating Considerations

For a specific circuit design, there is often a question of the appropriate process sequence. Although the capabilities of imaging and the pattern transfer step dictate the overall limitations, the decision depends on the unique capabilities of the manufacturing line to be used. Some general considerations can clarify the true issues for most production situations.

Photoresist patterning has different constraints for etching and plating. For etching, a thin photoresist is desirable to maximize the etchants' attack in the channel developed in the photoresist. Resolution does not limit the process, since

very small spaces can be resolved in either liquid or thin dry-film photoresists. The etching process itself is key to conductor formation.

Etching the copper from the channel becomes increasingly difficult as feature size is reduced, particularly for thicker metal layers. Therefore, the key criteria defining the capabilities of the print-and-etch process is the minimum space cleared, constrained by the final conductor height and the etchant chemistry and equipment.

For pattern plating, the photoresist thickness must be greater than or equal to the maximum final plated thickness of the copper on the base copper, and it must be possible to develop a photoresist channel equal to the final conductor width. As conductor thickness increases, it becomes more challenging to produce channels with a higher aspect ratio. Since photoresist resolution is on the order of its thickness, it would be difficult to resolve smaller than a 38 µm photoresist channel for 25 µm thick plating, irrespective of the final conductor spacing. Thus, the challenge for pattern plating is to resolve and develop fine channels in thicker photoresist materials and then ensure that the plating solution wets the bottom of the narrow photoresist channels.

Thus, in choosing the conductor formation process, the thickness of the conductor and the linewidth and spacing are the key parameters. A generalized relationship between them is found in Fig. 30.23. It is important that this type of plot is known for the production area before the process sequence is determined.

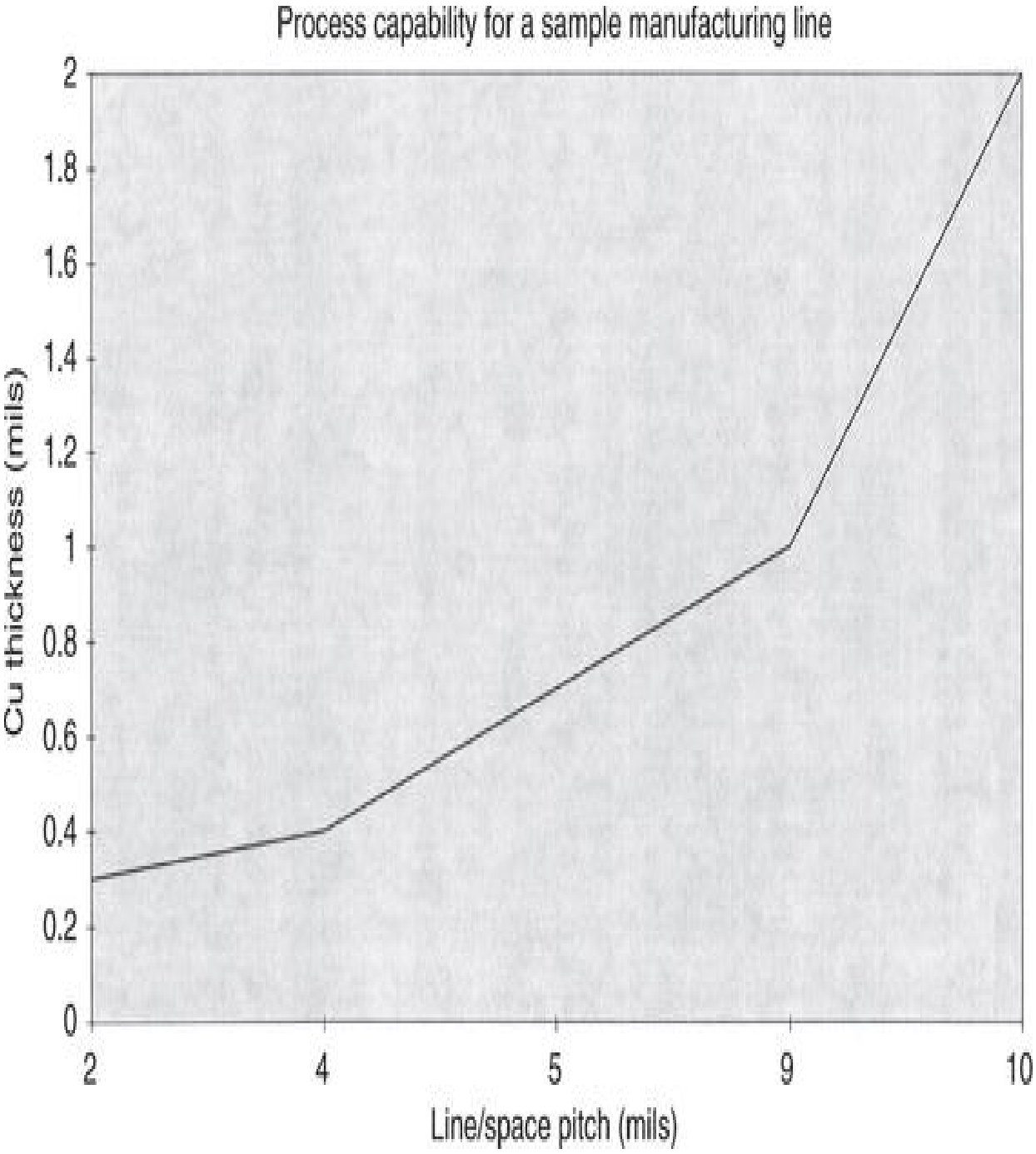


FIGURE 30.23 Sample plot of manufacturing line process capability to aid in processing sequence decisions.

30.7.2 Line and Space Division for a Fixed Pitch

It is common for product designs to have a fixed pitch, whether it refers to the I/Os for direct chip or packaging attachment or to the spacing between PTHs. This space is often divided equally between conductors and spacing. For etching or pattern-plating processes, avoiding their respective resolution limitations can increase the pattern transfer yield.

In etching, the etchant undercuts the photoresist and an etch factor is used to obtain straighter sidewalls and improved linewidth control. If lines and spaces are equally allocated in the circuit design, then the photoresist must resolve a smaller space than a line. This is difficult for fine features, except for very thin photoresists. For fine pitch, having a larger space than line will give higher yield. For pattern plating, the spacing in the photoresist is the limiting factor. After pattern transfer, this will become the line. In this instance, equal line and space is more acceptable, but based on the photoresist concerns, a wider final line than space is preferred. At the same time, it is desirable to increase the spacing for reduced incidence of line shorting, which translates to a wider “line” in the photoresist. The former is usually more important. Therefore, for both processes there is preferably balance between linewidth and spacing.

30.7.3 PTH Capture Pad Size and Shape for Optimum Line Formation

Just as the conductor line and spacing can be optimized, the PTH capture pad shape and size can also be altered to increase the yield. The absolute dimension of the feature is dictated by the placement accuracy of the drilling process and the overall dimensional stability of the product. The feature is sized to ensure that the PTH and conductor are connected. There are varying specifications as to the extent of capture that is required.

Feature dimensions above the line would be processed with pattern plating, and those below the line with print and etch.

Depending on the direction and magnitude of the dimensional stability and the drill wander and accuracy, the shape required to capture the PTH can be changed. This would reduce the size of this feature in at least one direction. In consequence, the spacing between the line and pad increases. Since this location is a change to the nominal line-to-line spacing, the narrowing of the channel results in shorting between the features in both a print-and-etch process and additive processes. In the former case, it is more difficult to clear the space, and in the latter, the narrower resist width is often underplated. Thus, when possible, an elongated pad will benefit the final conductor yield.

30.8 INKJET IMAGING

An *inkjet printer* is a type of computer printer that creates a digital image by propelling droplets of ink onto paper, films or in our application, printed circuit laminate. Inkjet printers are the most commonly used type of printer and range from small inexpensive consumer models to very large professional machines that can cost up to thousands of dollars. Direct printing of the resist, legend or solder mask can save many processing steps in fabrication.

Thermal-inkjet heads use a thin-film resistor to heat and “volatilize” a “portion” of the ink to produce a bubble that will drive the ink out through its nozzle. The figure below (Fig. 30.24) shows this process, as compared to the piezo effect. Piezo printheads are made by Xaar, Trident, Seiko-Epson, Kyocera, Konica-Minolta, Dimatrix, and Ricoh.

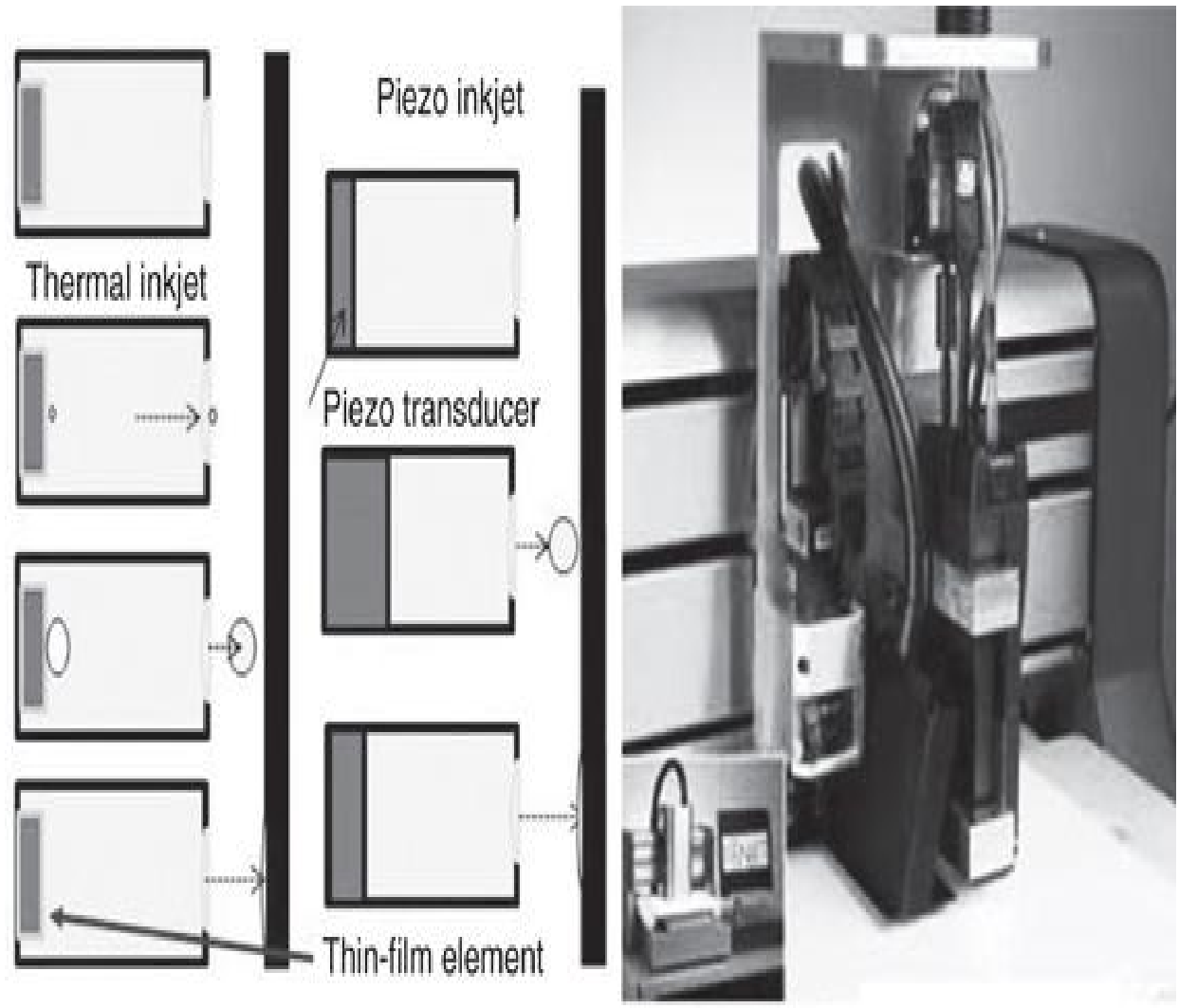


FIGURE 30.24 Thermal and piezo inkjet printing elements. Typical large format inkjet printers for legend, solder mask, print-and-etch innerlayers or plating resist.

Inkjet printers, especially models produced by Dimatix (now part of Fujifilm), JetXpert, Xennia Technology and Pixdro, are in common use in many labs around the world for developing alternative deposition methods that reduce consumption of expensive, rare, or problematic materials. These printers have been used in the printing of polymer, macromolecular, quantum dot, metallic nanoparticles, carbon nanotubes, human proteins, etc.

The emerging ink jet material deposition market also uses inkjet technologies, typically printheads using piezoelectric

crystals, to deposit materials directly on substrates. Dimatix, Orbotech, OCE, and MicroCraft utilize the MEMS and Piezo printheads for printing legend, soldermask and etch-resist ink for PCB and FPC. From single print heads to up to five 128-jets, 1 or 10-picoliter MEMS-based printheads and up to five different fluids for sequential production printing. Using a large 500 × 500 mm printable area with positional accuracy and repeatability of ±5 µm and ±1 µm, respectively. They can print with 1.5 mm depth-of-focus (DOF) for uniform printing over thick traces. Most printers are equipped with a drop watcher, fiducial camera, heated vacuum platen, ink drying either by UV or infrared, automated printhead maintenance and cleaning, PC, monitor and easy to use software.

30.9 AUTOMATIC OPTICAL INSPECTION

After imaging of any nature, comes inspection. Automatic optical inspection (AOI) replaces manual inspection and has become essential for high-density printed circuits fabrication and SMT assembly. For a bare PCB board AOI inspection may detect these features:

- Line width violations
- Spacing violation
- Excess copper
- Missing pad, i.e., a feature that should be on the board is missing
- Slivers
- Thin resist or scumming
- Trace shorts and dust/debris
- Cuts

- Hole breakage, i.e., a drilled hole (via) is outside of its *landing pad*

After a board scan, the defects report may be either rule based (e.g., no lines on the board should be smaller than 150 μm) or CAD based, in which the board is locally compared with the intended design via its artwork.

AOI inspection is much more reliable and repeatable than manual visual inspection and is used extensively in printed circuit fabrication world-wide. Units can have multiple illumination sources, including laser and multiple optical detection sensors, along with multiple-scan techniques to make false detection a rarity. A majority of the AOI units in production come from Israel, Japan, USA, and S. Korea. China is hoping to produce units in the future.

For SMT assembly, smaller circuit board designs are driving up the demand for AOI versus in-circuit test. Figure 30.25 shows a typical bare PCB scanning unit and a “repair and verification” unit.

FIGURE 30.25 A typical automatic optical inspection station for bare printed circuits with a “repair and verification” station interconnected by its CAM

network.

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CHAPTER 31

MULTILAYER MATERIALS AND PROCESSING

C. D. (Don) Dupriest

Lockheed Martin Missiles and Fire Control, Dallas, Texas

Happy T. Holden

Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

31.1 INTRODUCTION

Printed circuit board (PCB) structures and processes continue to be driven by device miniaturization, functional densification, and speed. The choice of components, actives and passives, and connectors are primary determinants of layer count and layer options, such as copper foil weights. Reductions in chip voltages are matched by an increase in current demand; this in turn causes increases in the number and thickness of the plane layers. More device leads combined with decreasing pitch increases the number of vias and interconnecting layers, while miniaturization and weight

reduction at the product level forces reduction in the physical package for the product.

New structures or advancements on existing structures are then needed to make these interconnections. These structures—such as blind and buried vias, multi-lamination (sublaminations), and build-up technologies—directly impact multilayer processing. Deeper blind vias and buried vias have caused a major increase in the demand for reliable via filling materials and methods. Relatively new materials, equipment, and processes have and are being developed to address this need. A new section in this chapter, “Filled Via Processing and Sequential Lamination,” addresses filled vias internal to the PCB.

Ever increasing frequencies continue to shift demand to materials with lower attenuation and propagation delay. To guarantee the electrical performance requirements of this product type and to benefit from the increased raw material and processing costs, the industry is specifying each element in the construction more so than in the past, and with less latitude. For instance, requirements for post-pressed thickness tolerance on a prepreg fill section, or surface roughness of the treatment side of the copper foil, or percent resin of the prepreg or core are much more likely to find their way onto fabrication prints.

Globalization of sourcing for PCBs continues to have a major impact on the physical design or the fabrication processes for the PCB construction. Mass lamination techniques have scaled to higher layer counts, and alternate tooling methods and panelization approaches have contributed to increases in material utilization and throughput. These technologies increase production volumes and reduce costs and are discussed in this chapter in Secs. 31.4.4 and 31.4.6.

The continued challenge to the physical PCB is coming from regulatory bodies and consumers who demand products that are less damaging to the environment.

Materials developed to meet these demands are known colloquially as either lead-free or RoHS-compliant (i.e., in accordance with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Directive). This chapter will not deal at length in the specific requirements of this directive, but will address the major impacts to the PCB materials and subsequent processing (see Secs. 31.5.5 and 31.6.2).

Lead-free joints, which have no appreciable lead content (for what "appreciable" means in this context, refer to the appropriate directive; see also Chap. 13 reflow at temperatures 30 to 40°C higher than the melt point of eutectic solder. These temperature increases have necessitated the development of newer resins or blends, different curing agents, and fillers to provide a laminate system that can survive and remain reliable after these elevated heat excursions. The changes to the laminates themselves are covered elsewhere in more detail (see Chaps. 9 through 15), but those properties directly applicable to the performance of the PCB are discussed in this chapter in Sec. 31.2.2.

In some market segments, particularly the consumer market, "green" technology is an important product differentiator or even a market requirement.

31.1.1 Relevant Specifications, Standards, and Test Methods

Industry standards groups such as the IPC have defined properties requirements and performance specifications to facilitate the choice of laminates. Design standards are available to inform the material selection process to achieve a desirable form, fit, or function. Standardized property tests have been developed to provide a common method to test

for property values and to interpret results. Some of the most commonly used are

- IPC-2221, “Generic Standard on Printed Board Design”
- IPC-4101, “Specification for Base Materials for Rigid and Multilayer Printed Boards”
- IPC-4104, “Specification for High Density Interconnect (HDI) and Microvia Materials”
- IPC-4652, “Metal Foil for Printed Wiring Applications”
- IPC-TM-650, “Test Methods Manual”

Table 31.1 lists some laminate tests covered in IPC-TM-650.

TABLE 31.1 IPC-TM-650 Laminate Tests

Test Method #	Title
2.4.24 C	“Glass transition temperature and Z-axis thermal expansion by TMA”
2.4.24.1	“Time to delamination (TMA method)”
2.4.24.2	“Glass transition temperature of organic films—DMA method”
2.4.24.3	“Glass transition temperature of organic films—MA method”
2.4.24.4	“Glass Transition and Modulus of Materials Used in High Density interconnection (HDI) and microvias—DMA method”
2.4.24.5	“Glass transition temperature and thermal expansion of materials used in high density interconnection (HDI) and microvias—TMA method”
2.4.24.6	“Decomposition temperature (T_d) of laminate material using TGA”
2.4.25C	“Glass transition temperature and cure factor by DSC”
2.6.25	“Conductive anodic filament (CAF) resistance test: X-Y axis”

31.2 MULTILAYER CONSTRUCTION TYPES

The construction of the rigid multilayer ML-PWB can take on many variations. To help categorize the various constructions, the IPC has developed industry PWB design specifications, defining them by class and type. Grouping the ML-PWB into categories facilitates the ability of designers and fabricators to communicate using a common format.

31.2.1 IPC Classifications

IPC classifications specify generic PCB design and rigid organic printed board structure.

31.2.1.1 IPC-2221: Generic Standard on Printed Board Design. There are many ML-PWB structures. This section discusses the methods and materials for the basic and several of the advanced structures. The IPC has two comprehensive standards for the design of rigid printed circuits, IPC-2222 and IPC-2226. The classification system within these standards for the ML-PWB by structure is shown. The distinction between the two is the focus on microvias in the later standard.

31.2.1.2 IPC-2222: Rigid Organic Printed Board Structure Design. This standard covers products with conventional feature sizes:

- *Type 3:* Multilayer board without blind or buried vias (see Fig. 31.1).

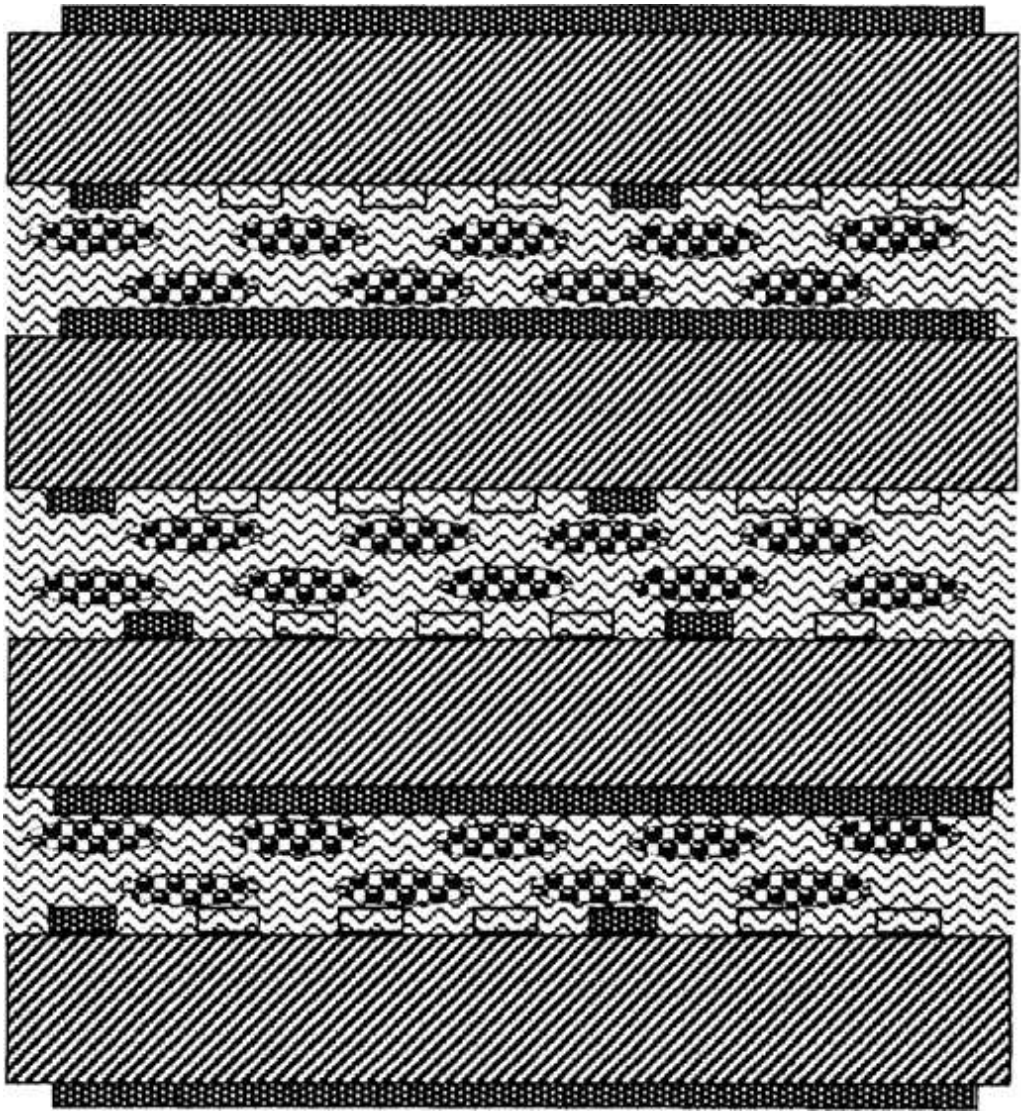

FIGURE 31.1 Type 3 (eight-layer ML-PWB) multilayer board without blind or buried vias.

- *Type 4:* Multilayer board with blind and/or buried vias (buried is shown in Fig. 31.2).

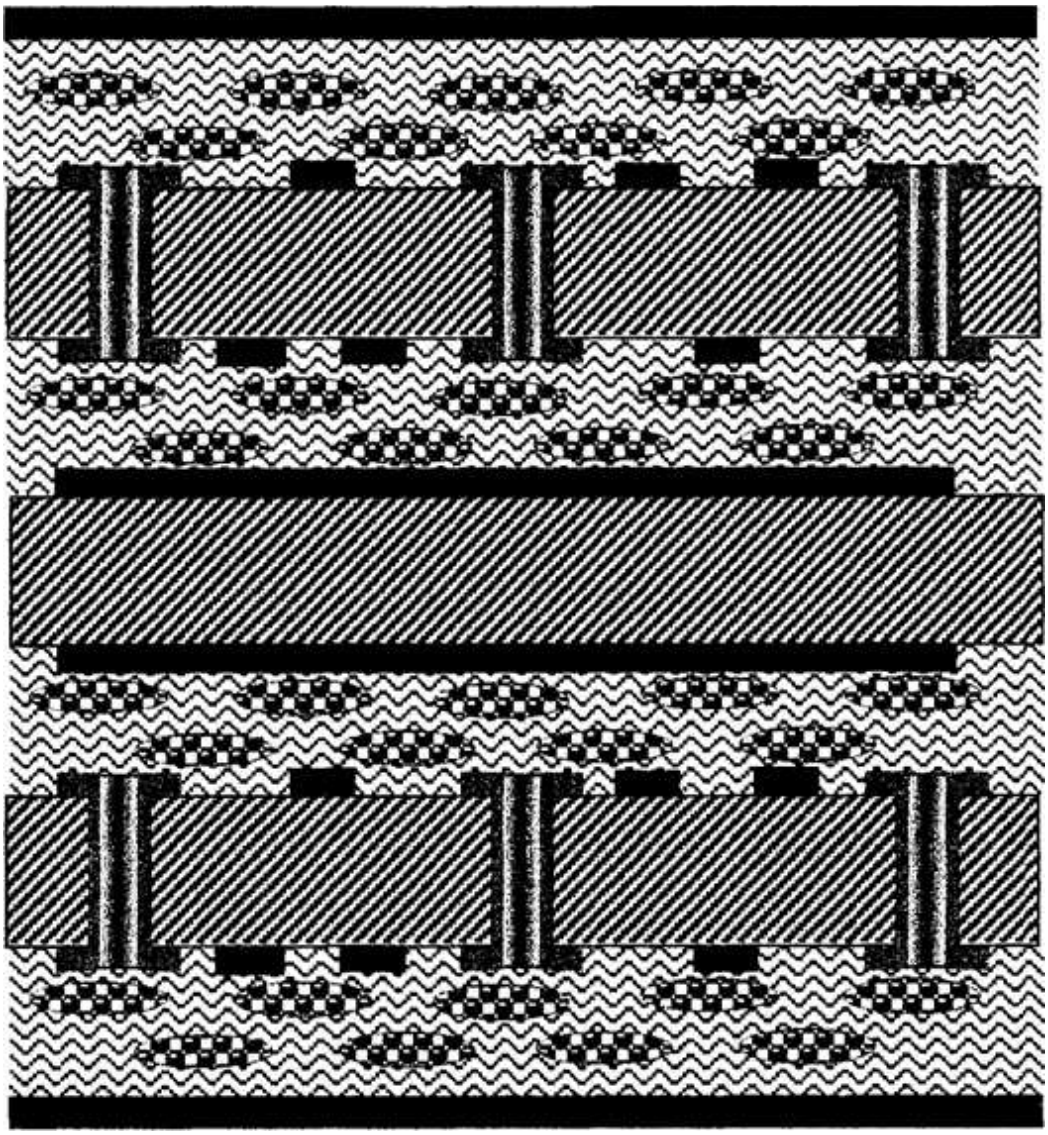

FIGURE 31.2 Type 4 (eight-layer-B/V MLPWB) multilayer board with buried vias.

31.2.1.3 IPC-2226: Design Standard for High-Density Interconnect (HDI) Printed Boards. This covers products with high-density feature sizes:

- *Type I:* 1[C]0 or 1[C]1 has through vias connecting the outerlayers (see Fig. 31.3).

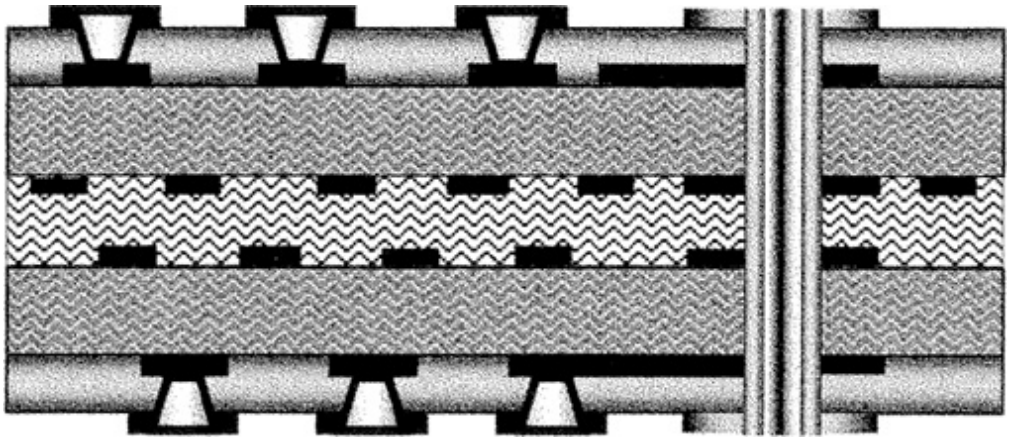

FIGURE 31.3 Type I (six-layer HDI MLPWB) high-density multilayer board with blind vias from top and bottom layers and through vias connecting the outerlayers.

- *Type II:* 1[C]0 or 1[C]1 has buried vias in the core and may have through vias connecting the outerlayers (see Fig. 31.4).

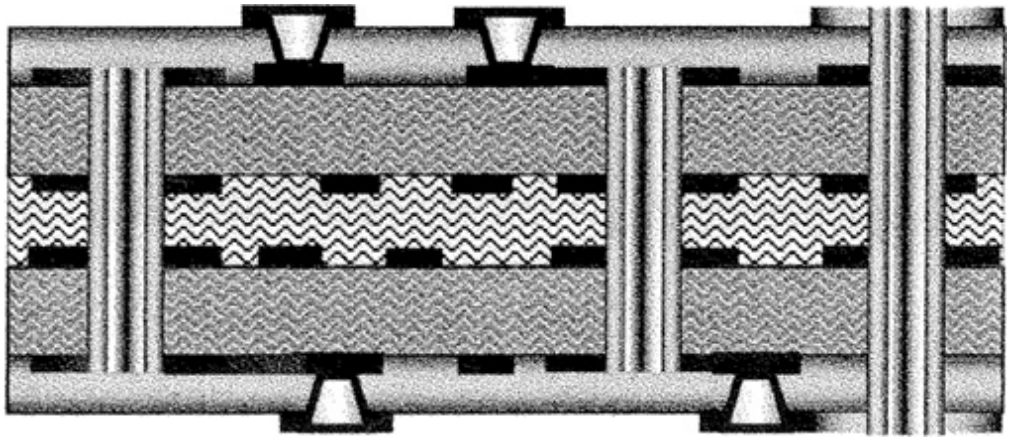

FIGURE 31.4 Type II (six-layer HDI MLPWB) high-density multilayer board with vias as well as buried vias in the core and through-vias connecting the outerlayers.

- *Type III:* >2[C]>0 may have buried vias in the core and may have through vias connecting the outerlayers (see Fig. 31.5).

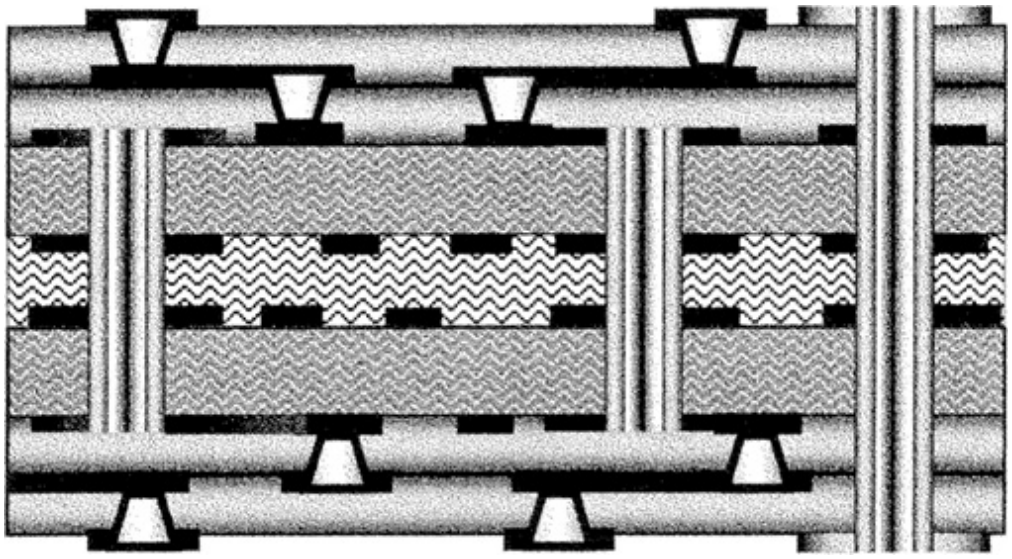

FIGURE 31.5 Type III (eight-layer HDI MLPWB) high-density multilayer board with blind vias as well as buried vias in the core and through vias connecting the outerlayers.

31.2.2 Basic Type 3 ML-PWB Stack-Ups

The type 3 construction can be said to be the most basic of PWB multilayer technologies. An ML-PWB is fabricated by the bonding (laminating) of copper-clad details consisting of imaged and etched laminates (typically double-sided). The bonding medium, known as prepreg, is a B-staged (partially cured) reinforced resin. The imaged details consist of C-staged (fully cured) laminate. These material components are arranged by layering according to the design documentation. This layering method in fabrication, known as the stack-up, follows the layer numbering order of the design. The stack-up formation method is often loosely defined in the design documentation; therefore, a good understanding of the lamination options is necessary. The lamination options described in this discussion refer to methods used to form the outerlayers and to form layer pairs. The material resin system should be defined on the

design documentation. Refer to IPC-2221/2222 for minimum suggested design documentation requirements.

The basic ML-PWB stack-up can be constructed with two options to produce the outerlayers and to form layer pairs. A third option that employs single-sided “capped” clads is rarely used and is not discussed. Often, in the case of designs having an odd number of layers, a combination of these methods is employed. The following three-layer stack-up methods are discussed:

- *Foil outerlayer construction (foil outer):* In this stack-up, the outerlayers are formed by using a sheet of copper foil per side.
- *Clad outerlayer construction (clad outer):* A clad detail provides the copper for the outerlayer.
- *Odd-layer construction:* This stack-up method balances a construction consisting of an odd number of layers.

31.2.2.1 Foil Outer Stack-Up. A board produced with copper foil outers is fabricated from one or more patterned innerlayer details and two copper sheets. The copper sheets form the outerlayers of the fabricated ML-PWB. This stack-up is the least expensive way to fabricate an ML-PWB and is by far the most popular design option. Figure 31.6 shows a typical stack-up for a foil outer board consisting of eight layers.

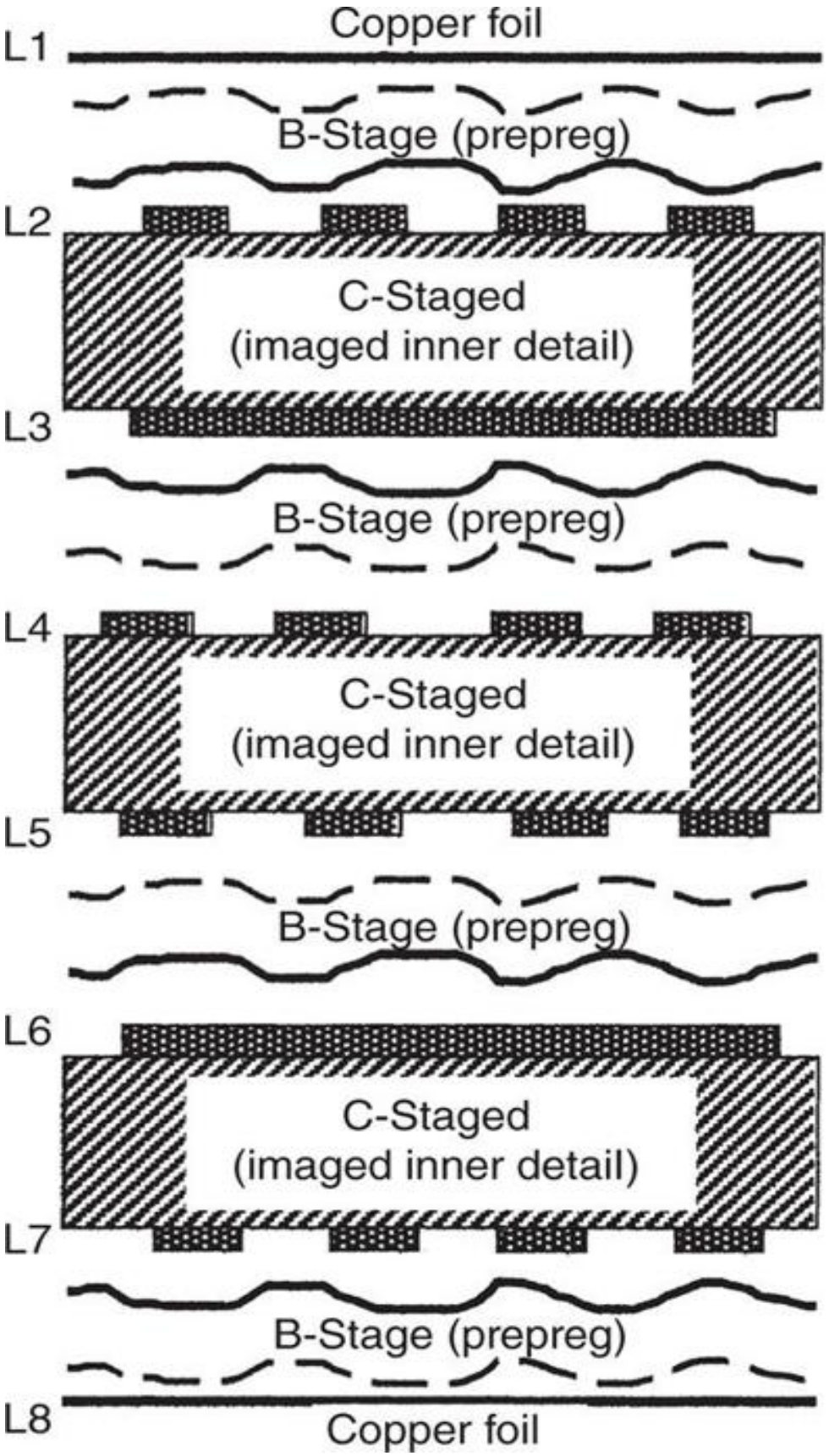
Copper foil
L1
B-Stage (prepreg)
L2
C-Staged
(imaged inner detail)
L3
B-Stage (prepreg)
L4
C-Staged
(imaged inner detail)
L5
B-Stage (prepreg)
L6
C-Staged
(imaged inner detail)
L7
B-Stage (prepreg)
L8
Copper foil

FIGURE 31.6 Foil outer stack-up (eight-layer ML-PWB), a typical stack-up for a foil board.

The stack-up shown contains three imaged clad details bonded with two sheets of prepreg at each opening and having two sheets of copper foil on the outside. When possible, the higher resin content prepreg ply should face the signal layer side. This is especially important when the signal is a heavyweight copper (2 oz or more). The copper layers, numbered from L1 to L8, begin with the top foil layer (typically called the primary side). In the design pictured, the layers L2, L4, L5, and L7 represent signal layers. Layers L3 and L6 represent power/ground layers. When the final imaged patterned is produced, it can provide another signal layer pair or a set of ground layers, or a "pads-only" pattern to support vias and component holes, as well as the device footprints of the electrical components and their associated fan-out patterns. Some of the advantages of this bonding method are

- *Lower raw material cost:* Loose sheet copper foil and prepreg sheets are more economical than clad laminate.
- *Lower consumable material cost:* The reduction in imaging resist and chemistry results in a cost savings.
- *Lower labor cost:* The reductions in material handling and in the processes of imaging and pre-lamination result in less total labor.

31.2.2.2 Clad Outer Stack-Up. Figure 31.7 depicts the same eight-layer design as Fig. 31.6, except the outerlayers are formed with a clad laminate. This stack-up arrangement requires four clad details, as compared to only three for the foil-stacked board shown in Fig. 31.6. This makes the clad outer board more expensive than the more commonly used foil outer construction.

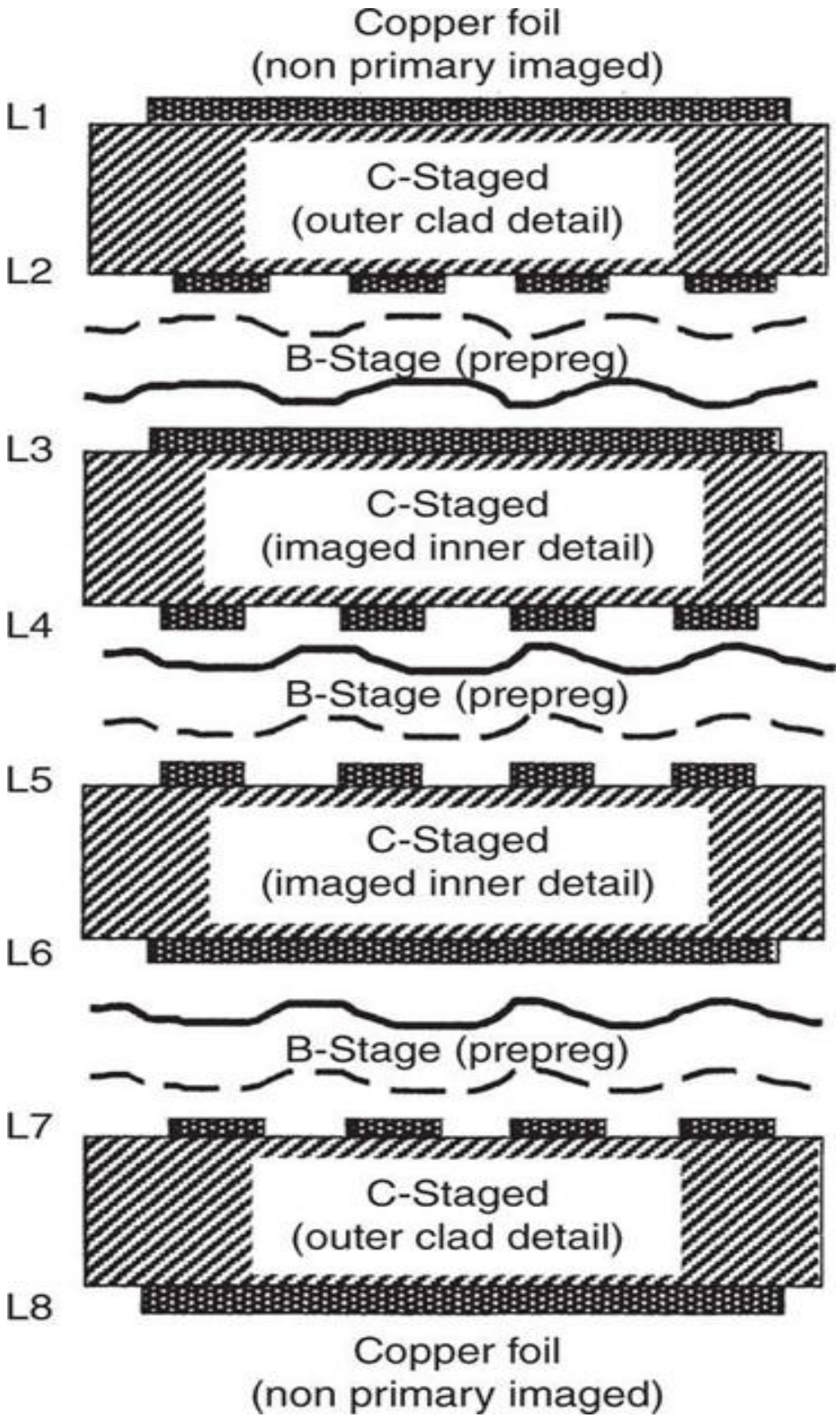
Copper foil
(non primary imaged)
L1
C-Staged
(outer clad detail)
L2
B-Stage (prepreg)
L3
C-Staged
(imaged inner detail)
L4
B-Stage (prepreg)
L5
C-Staged
(imaged inner detail)
L6
B-Stage (prepreg)
L7
C-Staged
(outer clad detail)
L8
Copper foil
(non primary imaged)

FIGURE 31.7 Clad outer stack-up (eight-layer ML-PWB) multilayer board design with the outerlayers formed with a clad laminate.

However, the clad outer design has one less B-stage opening and no loose individual copper foil. In addition, the clad outer boards are patterned on only one side prior to lamination. These factors partially offset the higher cost of this design. In Fig. 31.7, notice how the layer pairs have changed position placement. Layers L3 and L6 are now paired with a signal layer, which may be advantageous for controlling the dielectric thickness. Some of the advantages of using the clad outer bonding method include:

- *Improved surface topography:* When surface flatness is critical, the clad outer construction provides a smoother surface. When a signal layer of heavyweight copper is the first layer down, it is possible for weave texture imprinting to occur. This topography condition, sometimes referred to as “telegraphing,” can sometimes imprint the circuit pattern when using a foil build-up.
- *Improved handling:* Depending on the layer pairing, sometimes additional copper can be retained, as in a case where a signal-to-signal imaged detail can be avoided. This is mostly the case when the layer pair details are being produced on very thin core laminate.
- *Improved dielectric thickness control:* Sometimes, it is necessary to control the thickness at a specific layer pair tightly. This could be due to high-voltage considerations or to aid in the precision spacing of a signal plane to a ground plane where controlled impedance is necessary. This is possible because the C-staged (fully cured) clad laminate typically has an improved thickness tolerance.

The chief disadvantage with a clad outer layer design is in the potential for lower yield. This is because the external copper foil must be protected by the image mask during all the internal layer image, etch, strip, and oxide processing

steps; then the mask must be removed at a later point in the process so that the external details can be fabricated. The potential exists to scratch the photomask during all the handling steps, which will result in shorts or opens (depending at which point in the process the scratch occurs).

31.2.2.3 Odd-Layer Stack-Up. Sometimes, due to signal routing or the need to have a greater dielectric space, an odd-layer circuit is formed. Similar in characteristics to the clad stack-up, the odd-layer construction technique employs a nonimaged single-sided clad laminate. Material can be procured with a single side, but a warning is associated with its use due to a lack of bondability. When this material is manufactured at the laminator supplier with only copper on one side, a release sheet is used against the noncopper side. The release sheet produces a slick, smooth surface. The non-copper surface thus requires an aggressive surface preparation to promote bondability. One alternative to gain the same benefit of the single-sided clad is to etch the copper off one side of a double-sided clad. The etched side becomes the bond surface, which has greater adhesion due to the copper tooth imprint left behind. See Fig. 31.8 for an example of a balanced odd-layer construction.

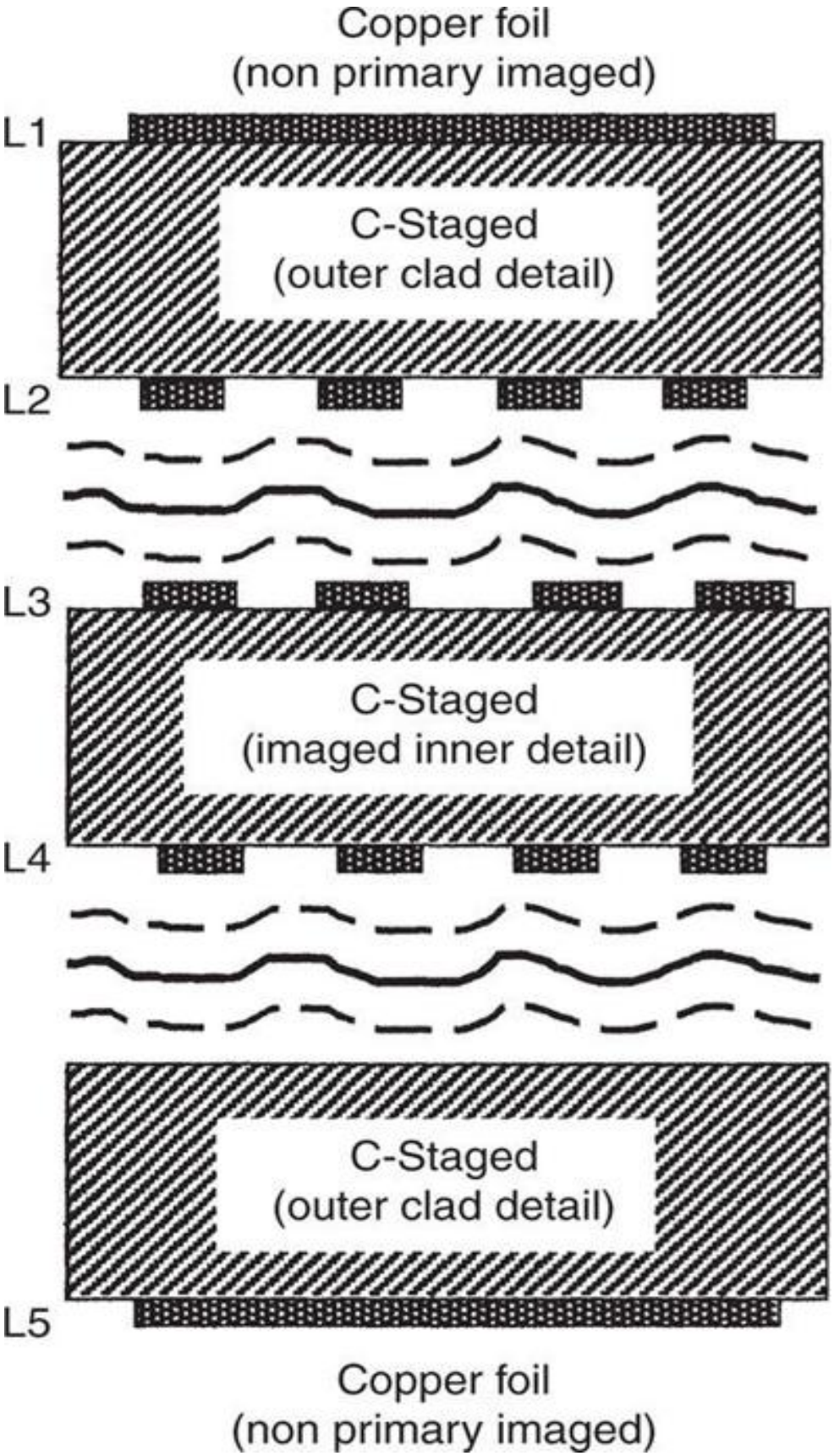
Copper foil
(non primary imaged)
L1
C-Staged
(outer clad detail)
L2
L3
C-Staged
(imaged inner detail)
L4
C-Staged
(outer clad detail)
L5
Copper foil
(non primary imaged)

FIGURE 31.8 Odd-layer clad stack-up (five-layer ML-PWB), an example of a balanced odd-layer construction.

Some of the uses of the single-sided odd-layer stack-up are

- *Odd-layer construction option:* The single-sided construction technique allows an opportunity to supply a layer for circuit designs having an odd layer count.
- *Odd-layer core balance:* One of the problems associated with a build-up of odd-layer circuits is the ability to maintain a balanced construction of the cores. Depending on the overall design thickness and layer count, this can become a major concern to reduce warping. Figure 31.8 depicts an example of an odd-layer stack-up with three equal core thicknesses.

31.2.3 Sequential Laminations

When a design includes buried and/or blind vias, it typically requires a set of sequential lamination and plating cycles. These technologies are defined in the industry design standard IPC-2221/2222 and are known as Type 4 ML-PWBs. These build types, when employing industry standard feature sizes, are mature in the industry. Complementing technologies, employing use of sequential processes for ML-PWB designs containing microvias less than 0.15 mm, are considered as build-up technologies. The terminology of build-up technologies encompasses many design stack-up variations; they can take on many forms and employ a multitude of methods. The build-up technologies defined in IPC-2315 and IPC-2221/2226 include categories named Type I, II, III, IV, V, and VI. The advanced build-up technologies use the materials found in IPC-4104. These include materials for layer forming, dielectric insulation, and interconnectivity. Included are photoimageable and non-photo-imageable materials (liquid, paste, or dry-film nonreinforced dielectric);

adhesive-coated dielectrics (reinforced and nonreinforced); and conductive foils and paste (coated and non-coated, photoimageable). For a detailed discussion of these processes, see Chaps. 25 and 26. This discussion will limit itself to addressing processes for standard technology Type 4 and advanced technology build-up Types I, II, and III, which can be manufactured with conventional processes.

31.2.3.1 The Buried Via Stack-Up. To avoid hopelessly complex routing, each signal net is generally routed using only one pair of layers with what is called *Manhattan geometry*. This means that diagonal routing is avoided and all signal lines run in a horizontal or a vertical direction. To avoid blockage and side-to-side cross-talk problems, horizontal lines are run on one layer and vertical lines on the other. This means that, in addition to a via at each end of the net (I/O via), most nets need one or two additional vias (routing vias) to change direction from horizontal to vertical. Figure 31.9 shows an example of Manhattan geometry.

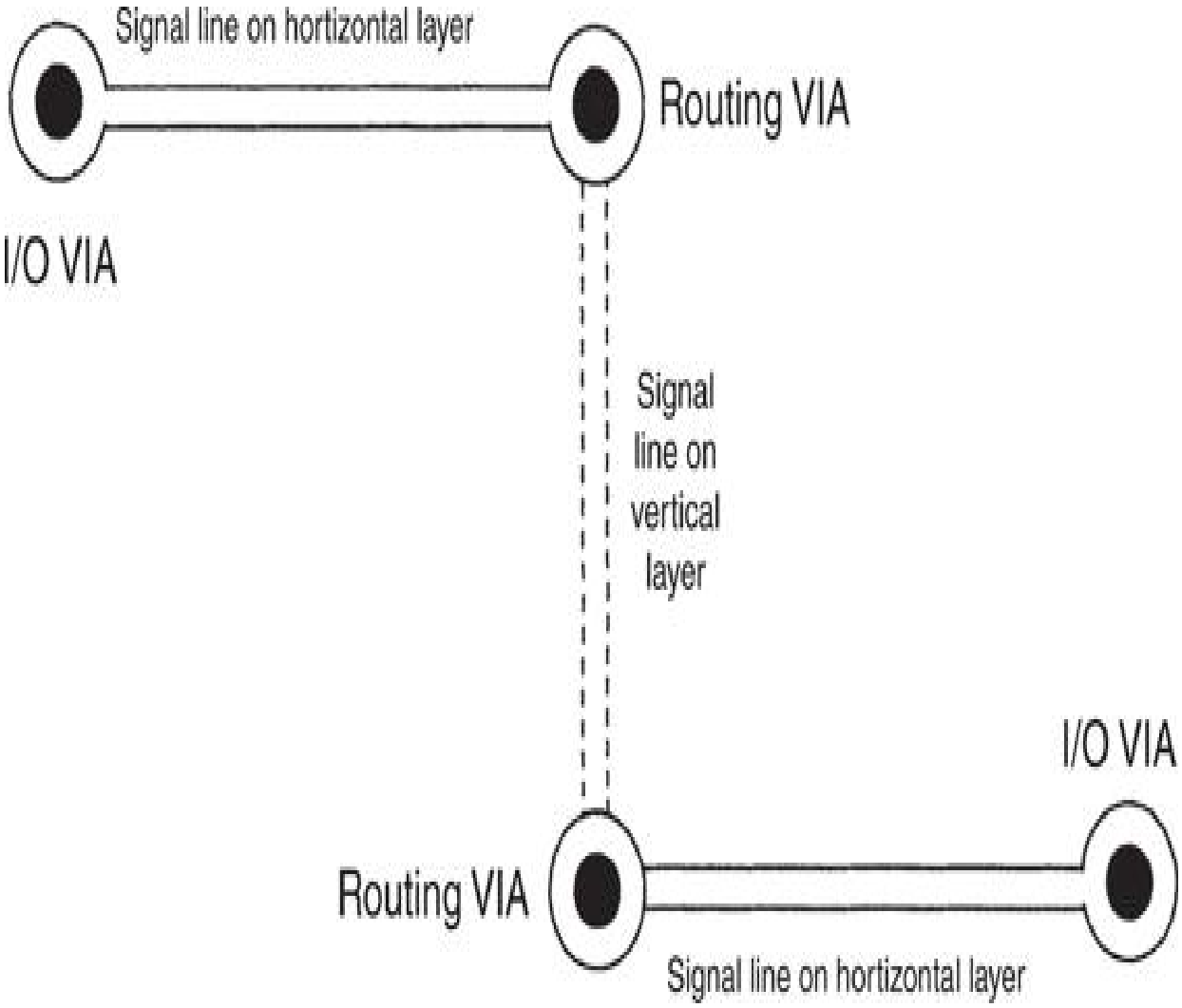

FIGURE 31.9 An example of a net routing using Manhattan geometry.

The net shown in Fig. 31.9 has two I/O vias and two routing vias. The I/O vias connect the signal lines to the board surface, where the net connects to an input or output point of an active circuit. The routing vias are used to change directions from horizontal to vertical. With through-hole vias, the routing vias pass through all layers, consuming valuable routing space. A high-layer-count board with many signal layer pairs can run out of via sites. In this case, additional layers will not improve routing completion and the board is said to be via-starved. One solution to a via-starved board is to use buried vias. The buried via connects two adjacent signal layers and provides routing vias without affecting

routing on other layers. Figure 31.10 shows an eight-layer board with two buried via layers.

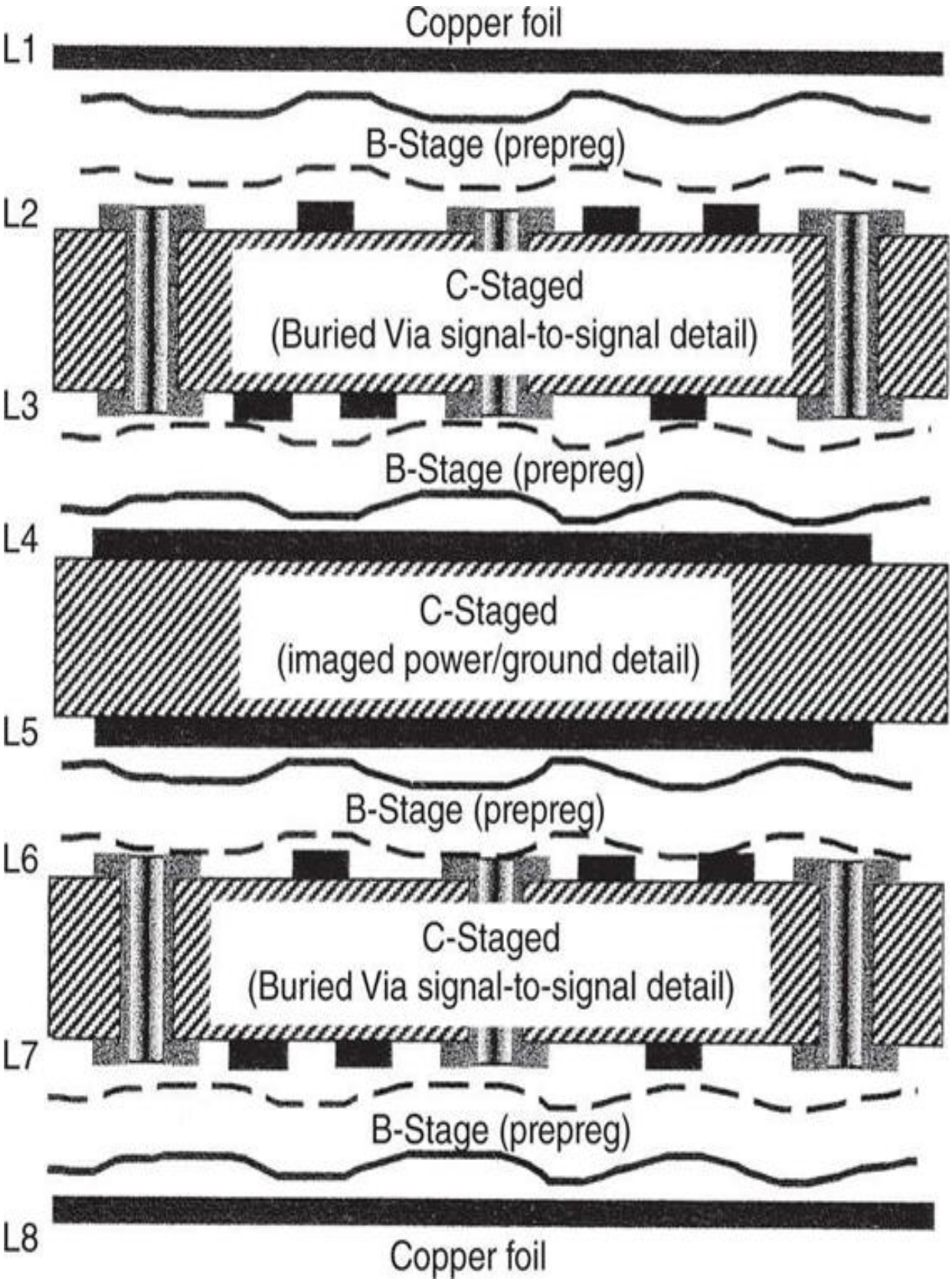
Copper foil
L1
B-Stage (prepreg)
L2
C-Staged
(Buried Via signal-to-signal detail)
L3
B-Stage (prepreg)
L4
C-Staged
(imaged power/ground detail)
L5
B-Stage (prepreg)
L6
C-Staged
(Buried Via signal-to-signal detail)
L7
B-Stage (prepreg)
L8
Copper foil

FIGURE 31.10 Type 4 (eight-layer B/V ML-PWB), an eight-layer board with two buried via layers.

Buried vias do not pass through the board, so they do not congest the routing on other layers. In addition, the same via site can be used simultaneously on different layer pairs. Since buried vias are drilled and plated in the thin laminate prior to lamination, they can be very small and positioned very accurately, saving additional routing space. In some applications, buried vias are placed where needed with no reference to a predetermined grid. This gridless routing approach gives very high computer-aided design (CAD) autoroute completion.

To benefit from buried vias, signal layer pairs must be routed on opposite sides of the same C-stage component. In Fig. 31.10, L4 and L5 are not buried via candidates. In Fig. 31.7, no signal layers can benefit from buried vias. The design shown in Fig. 31.10 is able to use buried vias on two layer pairs because a power/ground layer pair separates them. In nonburied via designs, it is best to use one power/ground plane between each signal layer pair. This gives cross-talk isolation and impedance reference. A buried via design uses a second redundant layer to force the next signal layer pair onto the same imaged detail. In other words, for a high-layer-count design to use buried vias on all signal layer pairs, power/ground plane pairs must be inserted between each signal layer pair. This increases the number of layers in the board and increases cost. Another disadvantage of buried vias is the cost associated with the extra drilling and plating operations.

31.2.3.2 The Blind Via Stack-Up. Another via option is the blind via, which connects the surface layer to one or more internal layers but does not go through the board to the opposite outside layer. Figure 31.11 shows an example of an eight-layer ML-PWB with both blind and buried vias. The design shown in Fig. 31.11 contains buried vias connecting

L5 and L6. Blind vias connect layers L1 and L2. The buried vias can be fabricated in layer details as described earlier or can be fabricated by blind drilling. Blind vias may become very important in very dense double-sided surface-mount designs that have interference between I/O vias from opposite sides on the board. If this is particularly troublesome, a via-in-pad (VIP) approach or dog-bone escape pattern is used. The VIP approach places a blind hole directly in the device I/O pad and typically plated shut (filled). The dog-bone approach places a blind hole in an adjacent pad next to the solderable land. A second application for buried vias is to ensure complete side-to-side electrical isolation.

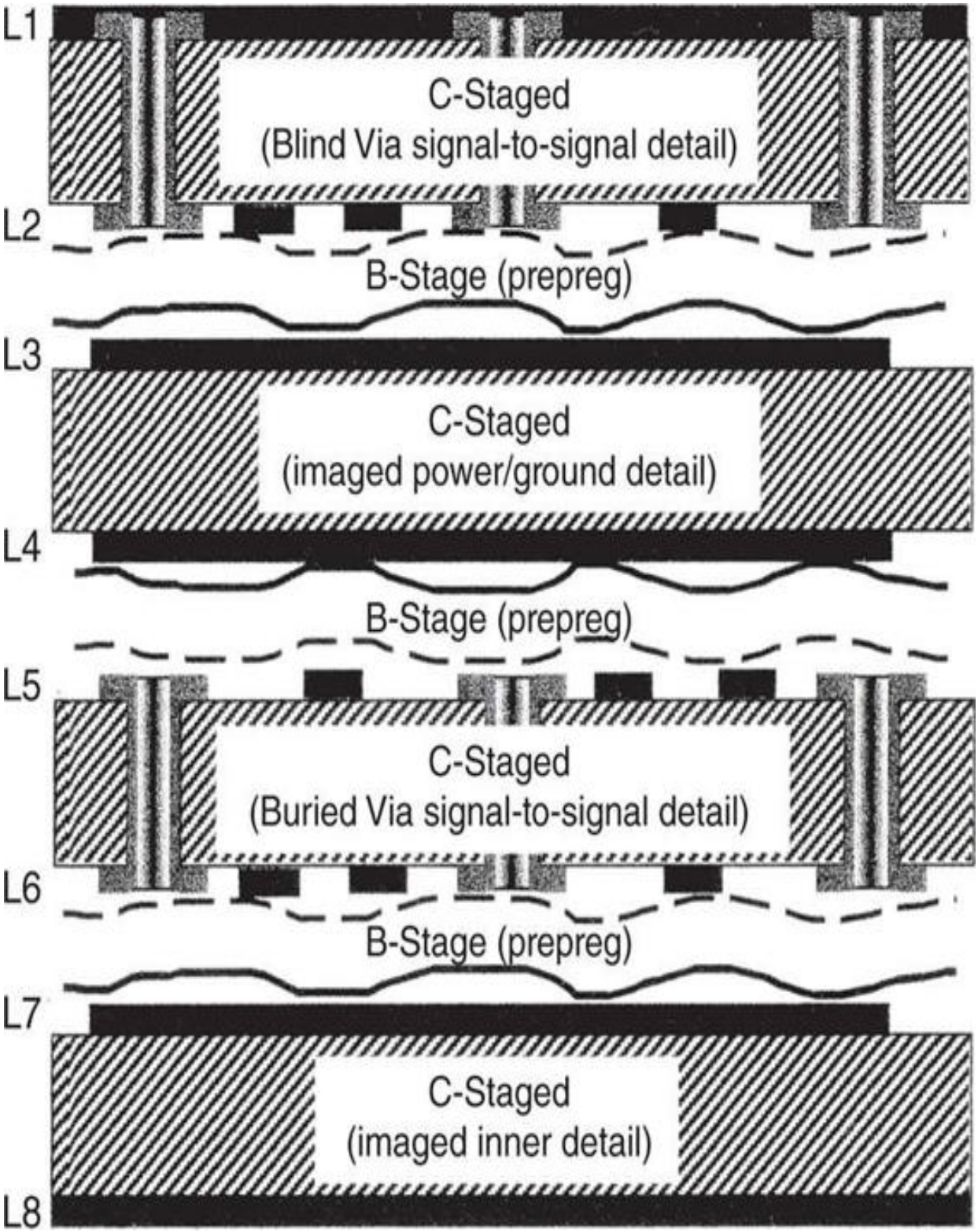

FIGURE 31.11 Type 4 (eight-layer blind and buried via ML-PWB). The design contains buried vias connecting L5 and L6. Blind vias connect layers L1 and L2.

This is particularly important in wireless designs where the RF circuits must be shielded from other circuits. Through vias allow RF electric fields to escape from a shielded region. A blind via eliminates this problem and allows RF functions to be combined with logic and control functions on the same board.

The ultimate use of blind vias is effectively to convert a dense double-sided surface-mount design to a pair of less-dense single-sided surface-mount designs. To see how this is possible, visualize an ML-PWB with fine-pitch SMDs on both sides as two separate boards with some level of side-to-side interconnection. If the board is manufactured as two separate subassemblies, the I/O connections on one side will not interfere with the I/O connections on the opposite side. For example, consider a 16-layer board fabricated as two 8-layer subassemblies. The subassemblies are laminated, drilled, plated, and patterned like a standard ML-PWB, with the exception that the sides that will become the board exterior are blanket-metallized. After patterning, the two subassemblies are laminated together and then processed as a standard ML-PWB. This process is another form of sequential lamination. The only through holes required in this design are the relatively few that provide side-to-side interconnection. Since each via site is used twice, a 100-mil grid may replace a 50-mil grid, providing a significant increase in innerlayer routing resources. This type of ML-PWB structure is very costly and has mostly been replaced with the routing features of the high-density design.

31.2.3.3 The High-Density Stack-Up. The buried via stack-up design came about for a solution to gain signal routability when CAD routing solutions were pressed to the limit. Early on, Type 4 designs were considered specialty products and utilized standard-feature-size characteristics. With the advent of more sophisticated CAD routing tools, it became possible to autoroute with greater efficiency,

sometimes avoiding the necessity and cost of buried vias. Soon high-I/O, full array components created new interconnectivity demands. Today buried via sections defined as cores in IPC-2221/2226 are used for the central starting point of manufacture, and then build-up layers are applied to complete the design as an HDI structure. As noted earlier, the common discriminator that separates the high-density design from a conventional Type 4 is mainly the feature size. For example, the HDI Type II, as shown in Fig. 31.4, uses a conventionally processed ML-PWB Type 3 board as the core (L2 to L5) and the PTHs become buried after the high-density features of L1 and L6 are added. Microvias are used to form a connection to L2 and L5; then through holes are formed to tie L1 through L6. The microvias and holes are now metallized in one cycle. The build-up layers in the example use thin dielectrics to provide a close proximity to the adjacent layer. This is required to accommodate the microvia connection and maintain producibility for metallization.

Figures 31.12 to 31.14 show a comparison of the HDI build-ups for Types I, II, and III. In each case, complexity is added by building add-on layers sequentially. The build-up layers are typically for signal routing and contain low copper weight. Dielectric-coated (nonreinforced) microfoils (as thin as 9 to 12 µm) are employed to provide a low-profile thickness after copper plating. This is needed to facilitate the image of fine-line widths typically associated with HDI. These styles of circuits offer some economy through use of a variety of dielectrics. The use and style of construction type must be matched with the product's expected application environment and operating life. Often the need for CTE match of area array components compels the application of a nonwoven aramid layer at the surface. The resin system selection should be based on the expected CTE mismatch concerns, such as when a ceramic device is surface-mounted to the assembly. Thermal cycling of power on and off can cause earlier failure when a large mismatch is present.

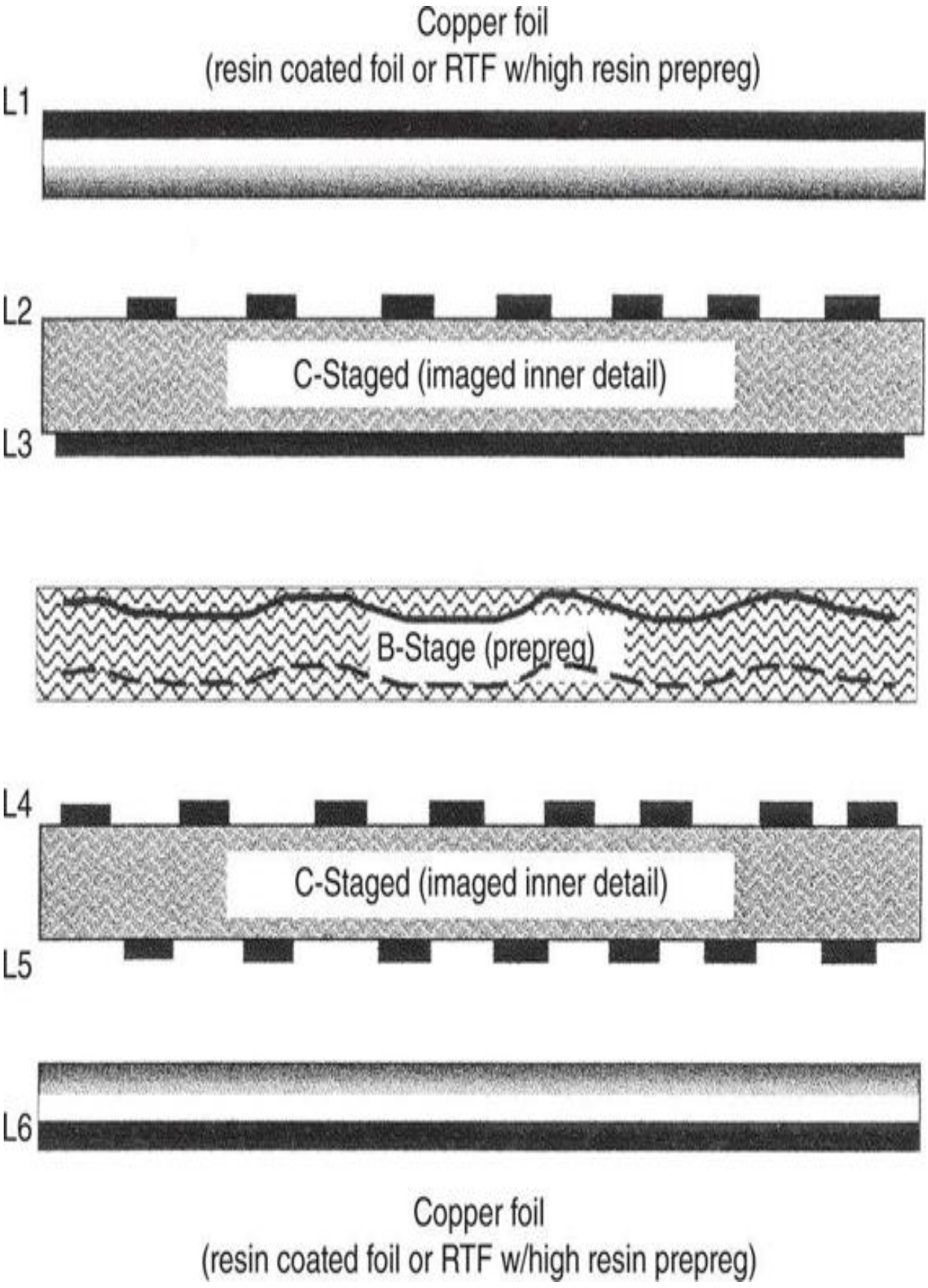
Copper foil
(resin coated foil or RTF w/high resin prepreg)
L1
L2
C-Staged (imaged inner detail)
L3
B-Stage (prepreg)
L4
C-Staged (imaged inner detail)
L5
L6
Copper foil
(resin coated foil or RTF w/high resin prepreg)

FIGURE 31.12 Type I (six-layer HDI stack-up) shows one example of how to stack up an ML-PWB with HDI features.

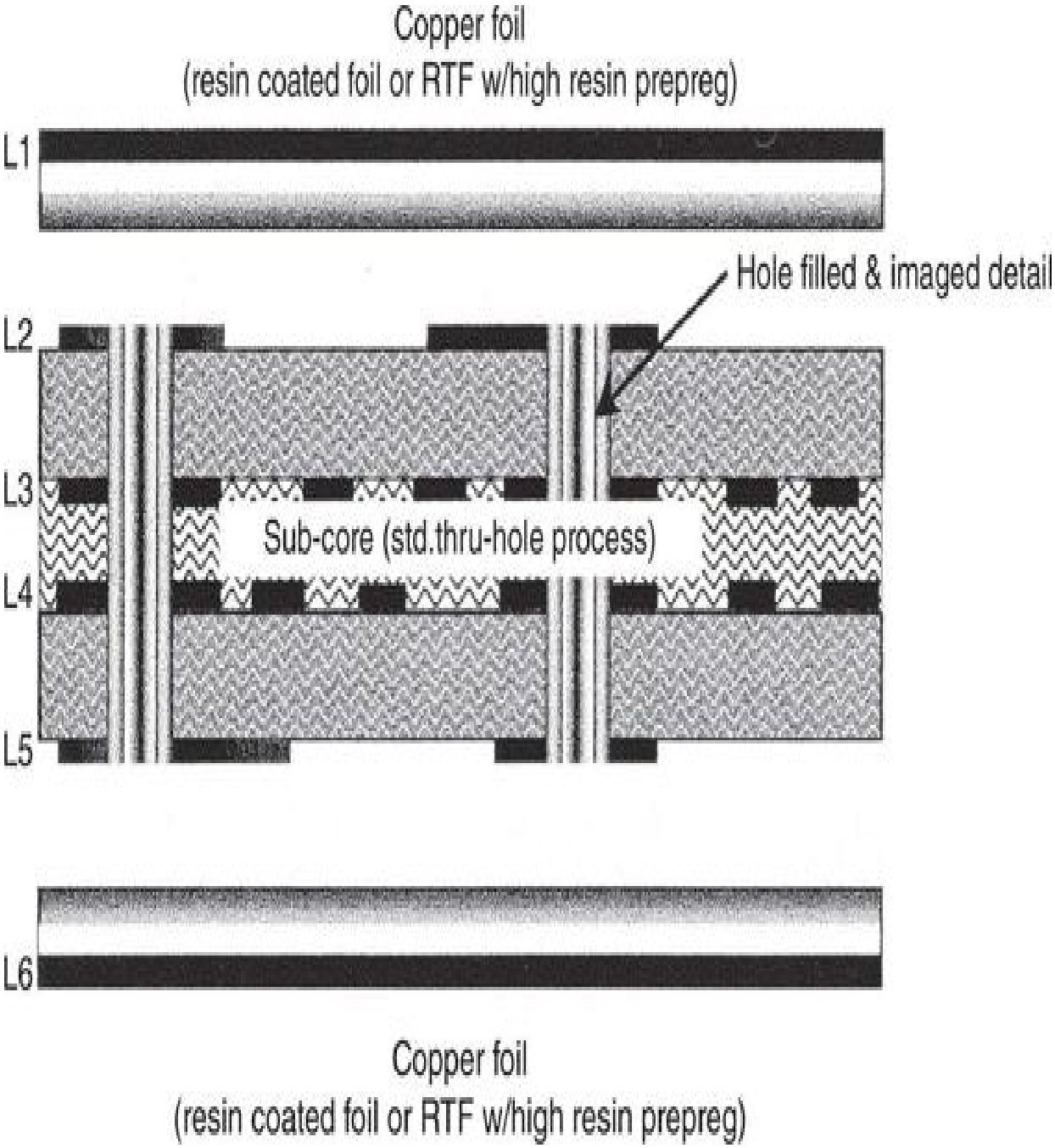

FIGURE 31.13 Type II six-layer stack-up having at its core a four-layer board with through holes, which later become buried.

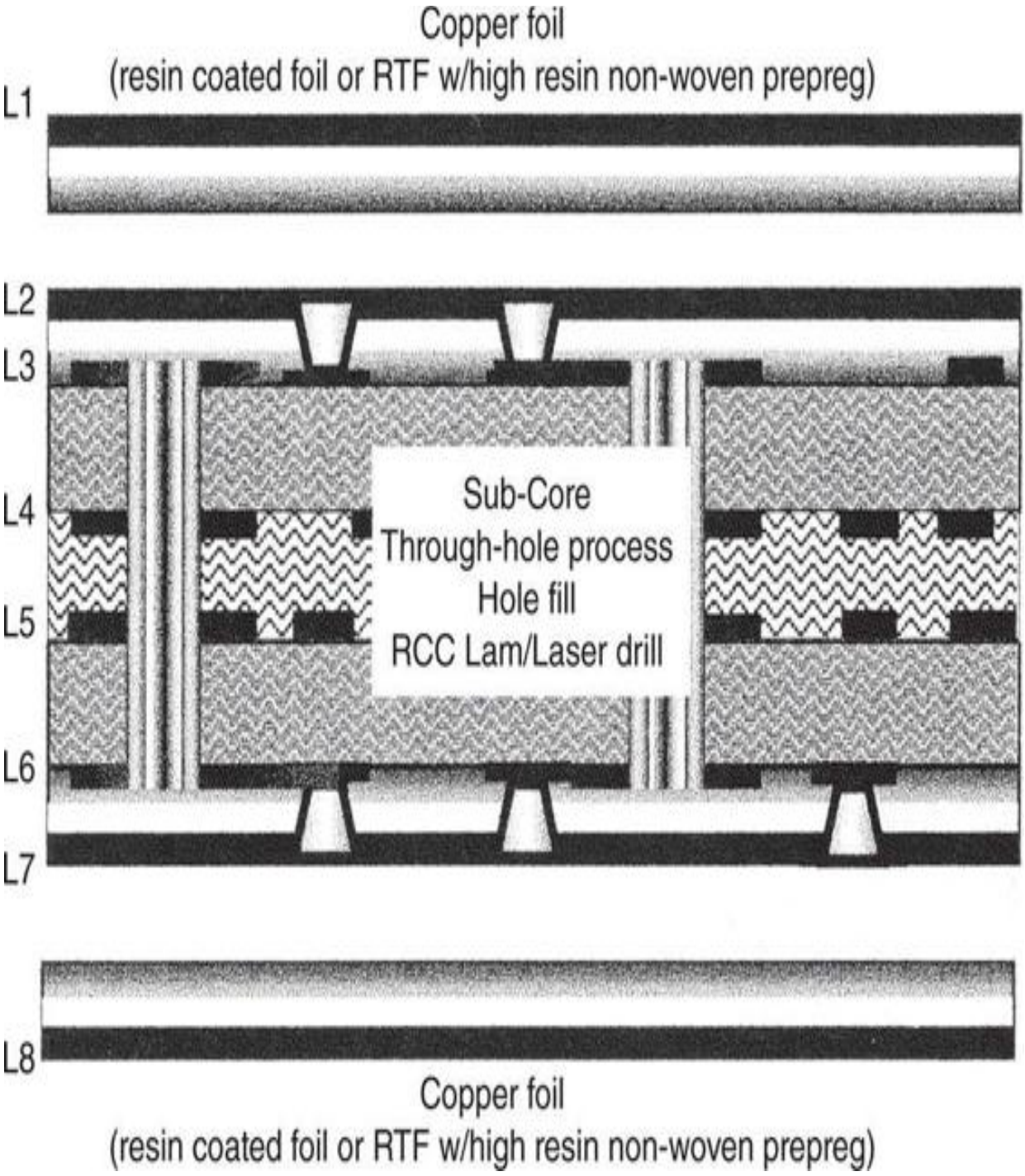

FIGURE 31.14 Diagram showing how an HDI Type III (eight-layer HDI stack-up) might be produced employing conventional lamination techniques.

Manufacturing capability becomes critical when targeting HDI features. The IPC-9151 Process Capability, Quality, and Relative Reliability (PCQR2) Benchmark Test Standard and

Database has taken the responsibility of developing industry standards to assist in benchmarking and quantifying capability limits. Manufacturing features such as imaging, etching, hole formation, plating, and lamination registration are all strained and must be optimized. Other processes that are equally challenged are the end-product continuity testing to access the high-density features.

31.2.3.3.1 HDI Type I Stack-Up. Figure 31.12 shows one example of how to stack up an ML-PWB with HDI features. The economies of this design are obvious because it requires only one lamination cycle. The density push in this level of HDI focuses on imaging and microvia routing. By routing at a high circuit density, the surface area of the board is better utilized. The outerlayers are typically formed with a low height dielectric. When utilizing conventional lamination, this is usually a resin-coated foil or a microfoil bonded with a high-flow nonwoven aramid prepreg. Special nonwoven series of aramid fiber laminates have been developed to yield an equivalent dielectric thickness of 1.9 mil.

Special handling is required for the microfoils, which are usually 9 to 12 μ m thick. To facilitate handling, a sacrificial carrier foil is sometimes cohered to the microfoil externally for added stiffness. After lamination, one option is to process the microvias through laser drilling and conventional through-hole drilling. Sometimes a clad outer construction may be best, depending on the laser technology chosen. For example, infrared (IR) (CO_2) laser ablation using an etched mask (small etched openings the size of the via) in the outer copper can be performed at primary print. This process helps reduce possible misregistration error. One metallization cycle is required to tie in all vias electrically. This reduces costs compared to sequential cycles. (See Chap. 29.)

31.2.3.3.2 HDI Type II Stack-Up. Density demands, when not met by the single lamination approach of Type I, must then address the use of sequential processing when

employing standard ML-PWB techniques. The Type II stack-up shown in Fig. 31.13 has at its core a four-layer board with through holes, which later become buried.

31.2.3.3.3 HDI Type III Stack-Up. The use of a Type III structure may be employed when routing densities are greatly pressed. At this point of complexity and above, alternative HDI approaches should be investigated because of the extra cost associated with performing repetitive cycles with conventional ML-PWB processes. Alternatives to lamination provide build-up of the dielectric and conductive layering through other means. These should be discussed with the manufacturer prior to selection. It is important to remember that the manufacturing method related to fabrication can have a great impact on the design rules chosen at CAD layout. Figure 31.14 represents how an HDI Type III might be produced employing conventional lamination techniques. Here, the core substrate is a four-layer ML-PWB detail similar to the Type II starting construction discussed earlier. Processing for the first pair of build-up layers follows the processing analogy of the Type II structure. Here, as in other foil laminated build-ups, the starting copper thickness should be kept to a minimum. Plating uniformity becomes critical when attempting to image/etch high-density features. After L2 and L7 have been defined, the final copper layer pair (L1 and L8) is laminated. At this final build-up, since no through holes are present, the flow of the resin-coated foil or prepreg should be sufficient to fill the microvias and flush the circuits. Once the additional layer is laminated, another level of microvias may be produced.

31.2.4 Filled-Via Processing and Sequential Laminations

The requirement to fill vias is driven most often by routing density. When high-density-area array components are utilized, the quantity of vias per square inch greatly increases in the local area under the device. Buried vias or blind vias are frequently the solutions to through-via starvation.

Buried vias, unless otherwise prefilled, will fill with resin during final lamination. The volume of resin necessary to fill the buried vias is dependent on the diameter, length, and total quantity. Buried vias might straddle a single core, or might interconnect several cores and dielectric separations in a sublamination section. If there is insufficient resin in the prepreg to fill the buried vias, those vias can starve bonding resin from the local area where they are concentrated. To prevent the prepreg resin from entering the buried hole, the fabricator often is required to prefill the vias prior to a build-up lamination with a resin or paste formulation. Other design constructions require blind vias that are planar and within the land pattern at the surface mount attachment locations. These VIP structures free up real estate on the component attachment surfaces and provide enhanced signal integrity at high frequencies. Prefilling internal buried vias or blind VIPs with a hole-fill resin can provide a more robust interconnect structure, improved lamination integrity, and a planar surface in the case of the blind vias.

31.2.4.1 Fill Materials. Since the fill material is an additional fabrication material that becomes a part of the design construction, procurement documentation is required to specify a fill material type and thereby implement the via fill process. The selection and documentation of the fill material require the same consideration as the base laminate preference. This is especially critical when targeting a lead-free-compatible process. Currently, an industry-based material specification for via fill material does not exist. Therefore, specific fill-material brands may be named on the

drawing, or some other form of user/supplier agreement must be established. The fabricator has preferences for the type of material used for via fill. Just as suppliers often have preferences for a specific solder mask brand, they also often prefer to use of a specific via fill material around which they have developed their principal processes. Supplier preferences can be driven by specific via fill material characteristics, such as accessibility, equipment compatibility, process supportability, plateability, and/or shelf/pot life. This may complicate source selection, or it might influence the use of a dedicated service center for the hole-fill process. The fabricator may not always know the reliability of its preferred material for a given via structure or end-use environment.

Determining the properties of the various fill materials may be difficult for the user. Obtaining properties from the material suppliers' data sheets may be possible for some properties, whereas others are more difficult to obtain; for example, many manufacturers' data sheets omit the modulus. Table 31.2 provides a cross-reference for some of the more common material types with properties available. Additional properties and performance data may also be found at the specific manufacturer Web page.

TABLE 31.2 Common Via Fill Manufacturers and Material Properties

Mgf. (Link)	Type	Material[2] (part number)	Pencil Hardness	Color & Plateability	Thermal conductivity (W/m/K)	T_g °C	CTE under T_g (ppm)	CTE over T_g (ppm)
Peters	Nonconductive (ceramic filler)	PP 2795	9H	White and light gray[1]	N/A	140	40	150
Peters	Nonconductive (ceramic filler)	PP 2794[1]	N/A	White[1]	N/A	115	40	105
SAN-EI	Nonconductive	PHP-900 IR-10F[3]	N/A	White[1]	N/A	160	32	83
Taiyo	Nonconductive	TCHP-200 DB4 (2 part)	8H	Green[1]	N/A	130	24	78
DuPont	Conductive	CB-100 Copper /Silver	4H	Silver[2]	3.5	115	35	47
Tatsuta	Conductive	AE 3030 Copper/Silver[3]	N/A	Silver[2]	7.8	171	40	86
Taiyo	Conductive	SCHP-7901 Silver	4H	Silver[2]	6.7	110	45	120

Notes: Some via fill materials are not typically compatible with permanganate chemical processing. Confirm with the specific supplier before using. The denotation of N/A indicates that the data were not readily available.

[1]Compatible with Plasma desmear, requires electroless followed by electrolytic processing.

[2]Compatible with Plasma desmear, conventional electroless recommended but may be use direct electrolytic processing.

[3]Capability with a lead-free profile should be verified; typically the higher T_g materials with a lower ppm above T_g will be more compatible.

31.2.4.2 Concerns and Common Defects. Concerns associated with filled-via structures have mostly been eliminated with process maturity today yet potential impact on reliability still exist. Some concerns include plating

adhesion, air entrapment (voids) created during the filling operation, CTE mismatch with the bulk resin, and the risk of overplanarization to remove excess resin. Entrapped voids are suspected to have an effect on hole wall integrity due to outgassing; CTE expansion mismatch could have an adverse interaction with the material and copper CTE properties. Overplanarization can grind down the plated hole wall knee, weakening the interconnect at the barrel plate. This is commonly called a reduction in wrap copper. A lack of wrap copper will leave a butt joint at the interconnect that is vulnerable to pad rotation (lift) knee crack. Reliability data within the industry for these structures suggest higher risk exist when wrap plating is less than 5 um (0.0002 inches). Some performance criteria for the via fill method has been quantified in industry standards today. To specify the most cost-effective via fill method with confidence, the designer must know the method's compatibility with the assembly process and targeted mission criteria. Qualification testing to the end-use environment with a preproduction build is recommended.

Designers need to be aware of potential processing issues associated with specifying via fill. Although the risks are well known, the manufacturing issues are often still difficult to detect from standard coupon analysis. Construction integrity weaknesses often are not found until latent defects occur or become revealed by aggressive thermal stress screening. Figure 31.15 is an example of a design employing conductive via fill within two via structures (blind and through holes) sharing a common surface layer. It should be noted conductive fill materials are very costly and difficult to process. This example is free of plating interconnect defects; the buried structures are fabricated without an internal cap plate; the voids in the conductive fill are typical for this type of material. Figure 31.16 is a nonconductive fill with a close-up view of a micrograph illustrating the plating integrity and surface planarization that has maintained the wrap copper

requirement. In this example, the full plating requirement was deposited without a separate button plate cycle. The wrap copper demarcation is noted and no separation has occurred at the cap plate. Some common failure mechanisms, which illustrate the risk associated with fill technology, are shown in Fig. 31.17. Here, micrographs show a via fill with a lack of plating adhesion and wrap copper, allowing interconnect separation.

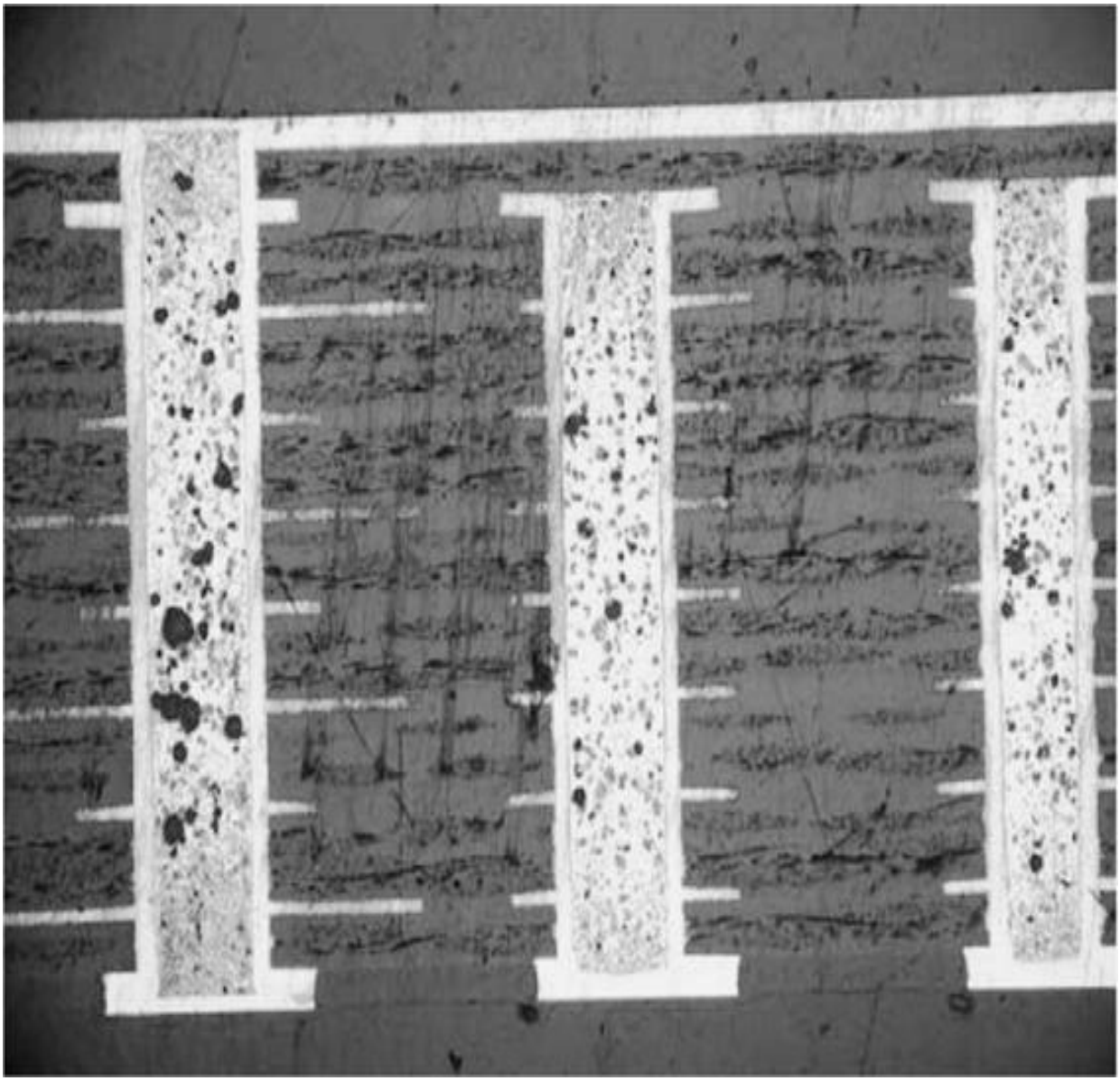

FIGURE 31.15 Micrograph of conductive via fill.

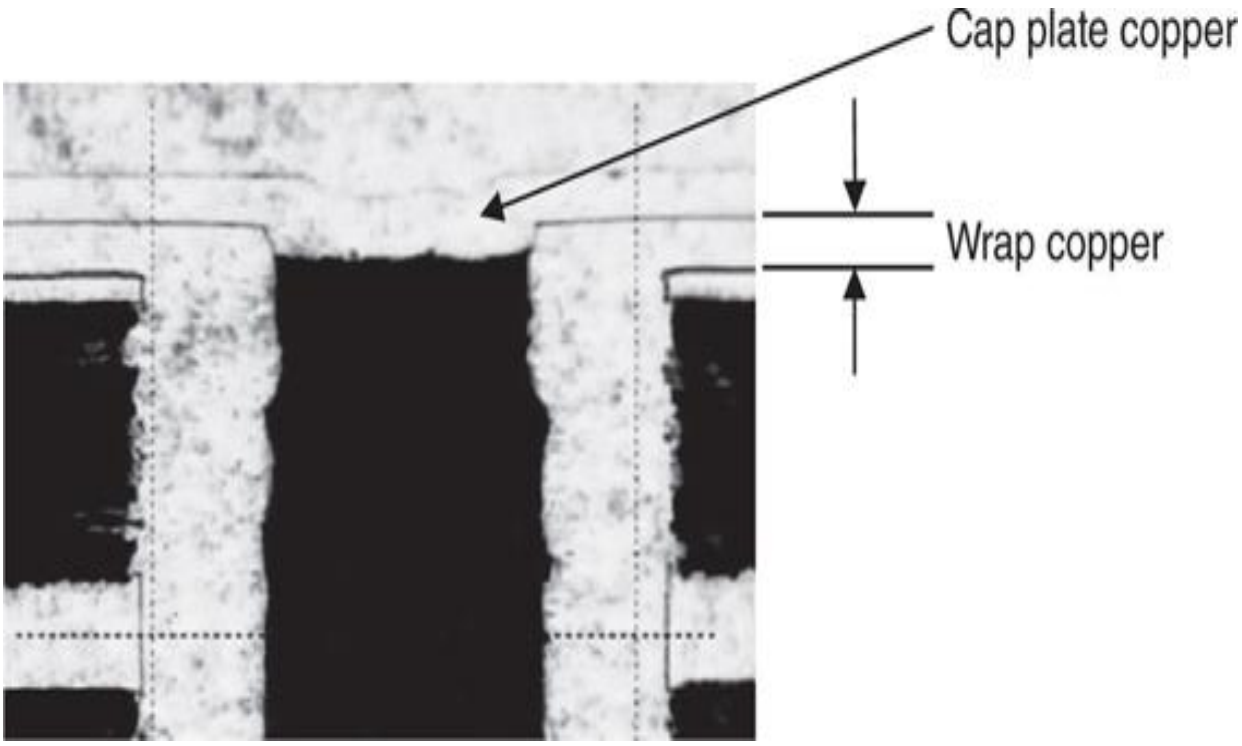

FIGURE 31.16 Micrograph of a nonconductive via fill with good plating features.

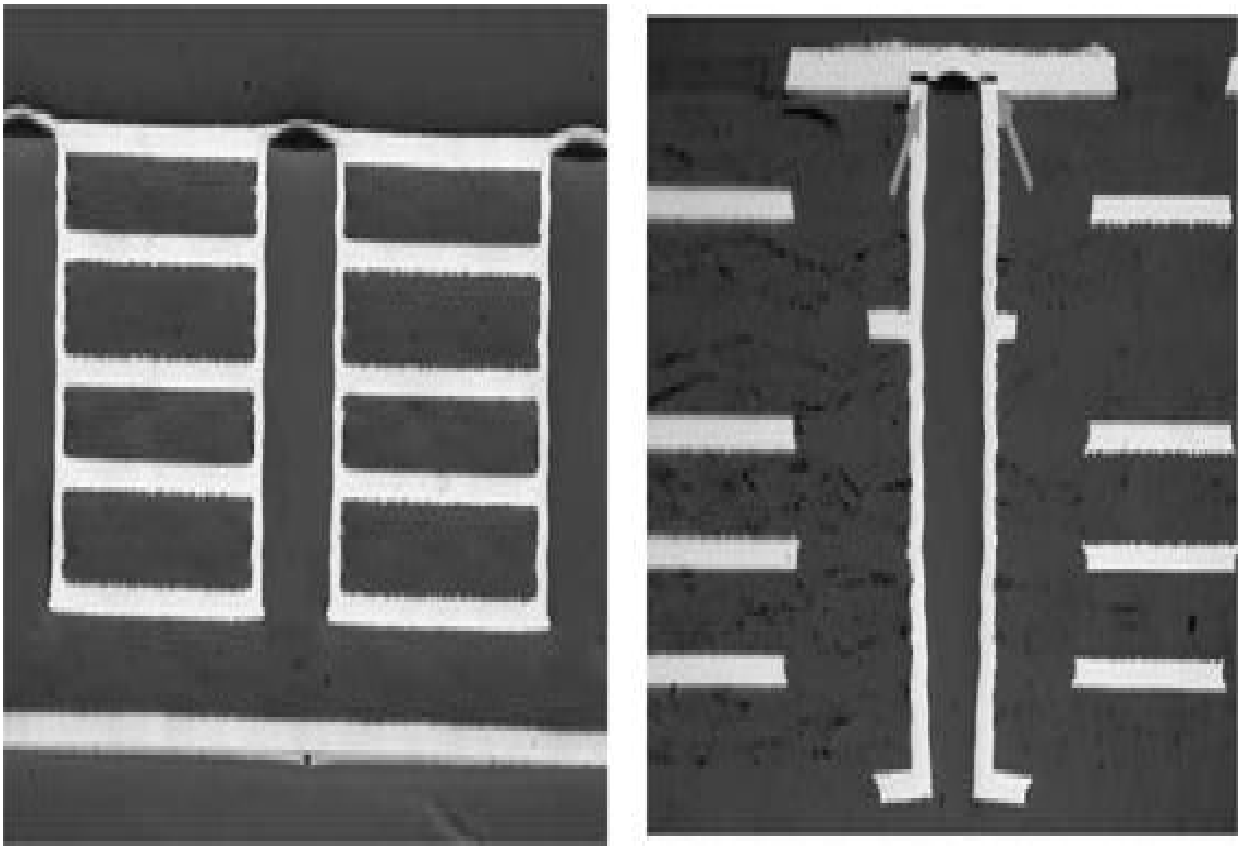

FIGURE 31.17 Micrograph of a nonconductive via fill with defective features.

31.2.4.3 Via Fill Processing and Flow. A via fill process flowchart can be used to communicate the modified steps of a typical manufacturing flow. Two process maps are shown to illustrate two typical process flow variables of a plated-cap versus non-plated-cap via fill process. Reliability testing to segregate the performance of via fill materials with the cap-plate and non-cap-plate features in the selected application should be performed prior to selecting this design feature.

When a plated-over via is required, plateability of the fill material should be a chief consideration. Fabricators should screen for this compatibility across the various via fill materials within their plating process to determine the integrity of the metalization. The flowcharts illustrate the fabrication methods employing a panel plate scheme. The flow could also be modified for a pattern plate methodology.

The two process flows are illustrated in Figs. 31.18 and 31.19. The key via fill process steps are highlighted for clarity.

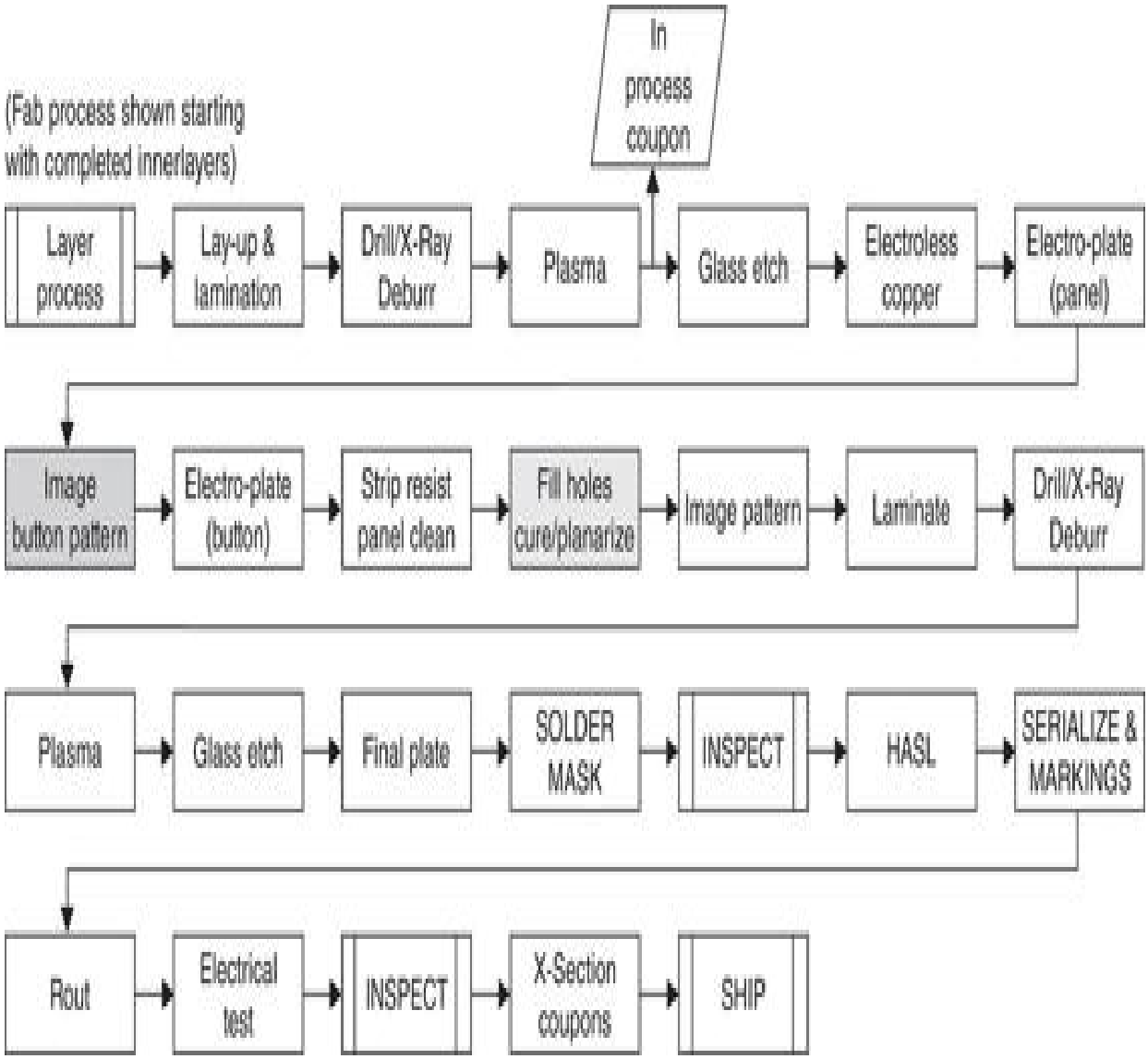

FIGURE 31.18 Via fill flow in a noncap plate process (panel plate/button plate).

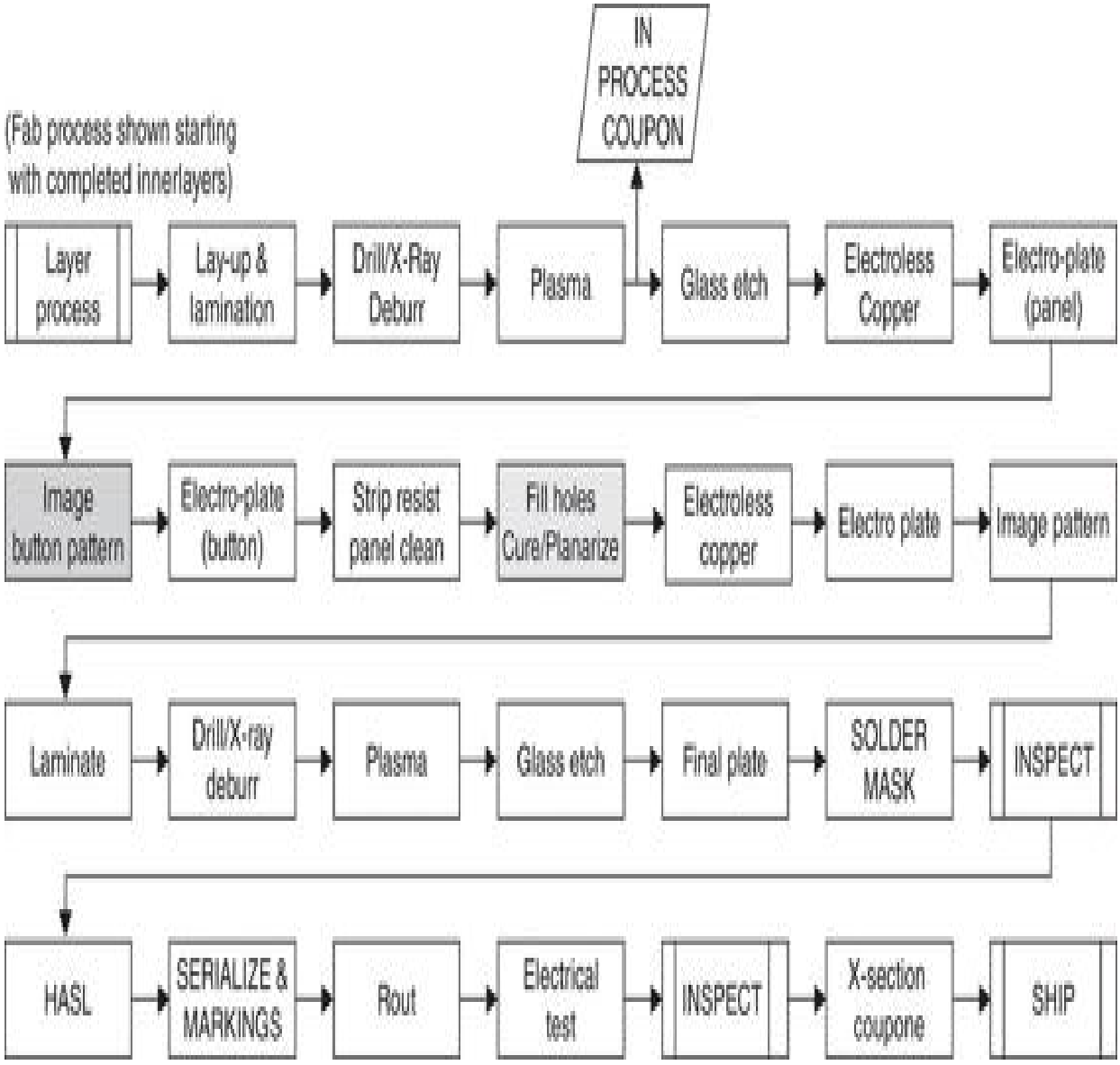

FIGURE 31.19 Via fill flow in a cap-plate process (button plate/panel plate).

31.2.4.3.1 Pre-Via-Fill Processing (Plating Variables). The plateability of via fill material is an important feature to understand due to industry trends that have shown that plated caps may be problematic in some design constructions. Outgassing of the fill material may separate the metallization during sequential lamination or thermal stress. Poor adhesion can also contribute to a separation but typically can be screened with standard tape testing. Figure 31.20 illustrates a cap-plated buried structure

and a micrograph showing a cap-plated via with separation occurring.

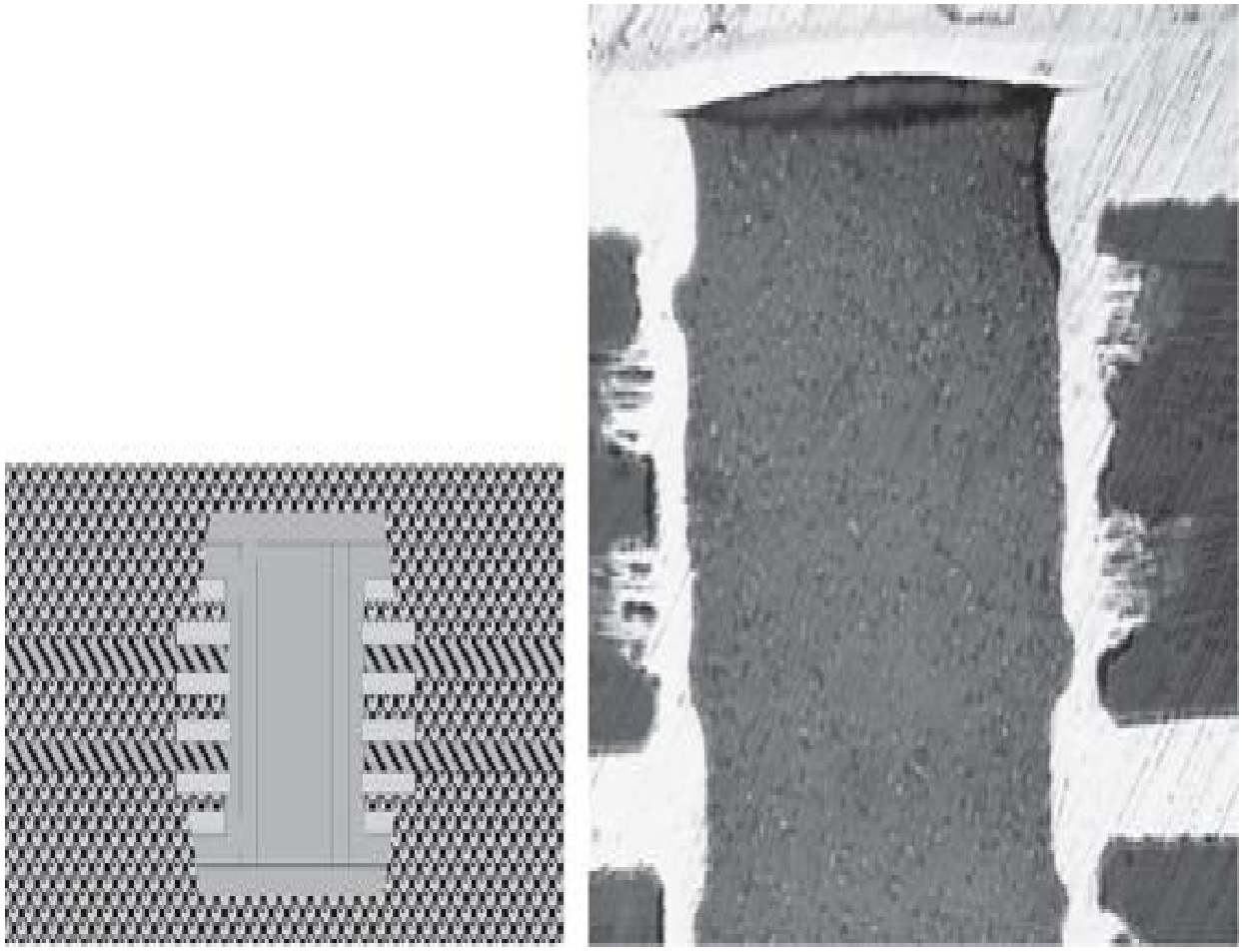

FIGURE 31.20 Cap-plated filled structure.

When the main design attribute is to limit resin from flowing into holes at sequential, lamination, the plating over the filled structure may not be required. Here, the filled panel after planarization can be staged for lamination. Figure 31.21 illustrates a non-cap-plated buried structure, and the micrograph shows a non-cap-plated via with lamination separation occurring.

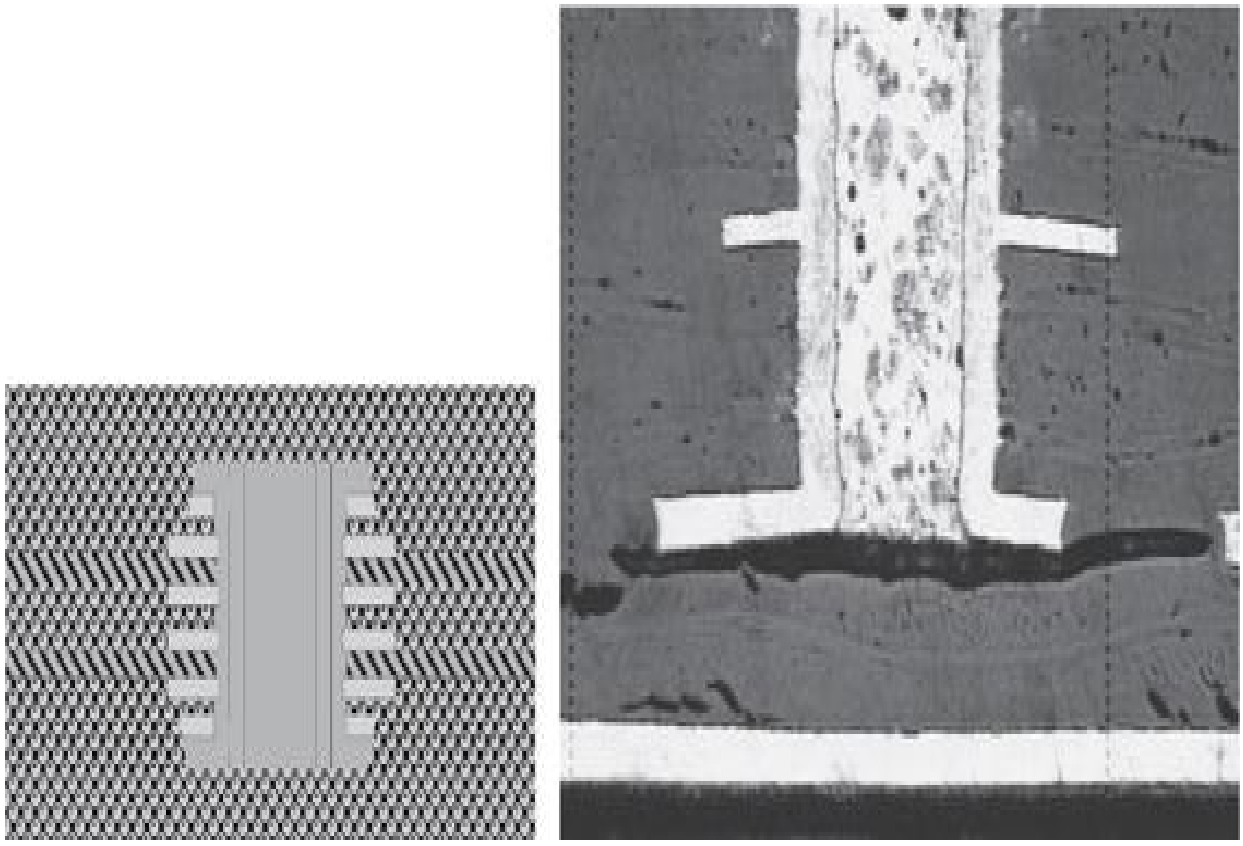

FIGURE 31.21 Noncap-plated filled structure.

Each of these techniques requires the fabricator to understand the fill material compatibility with their base laminate system and plating processes. Typically, process compatibility can be screened with a simple solder-float thermal stress analysis and cross section.

Prior to plating, the fabricator must understand the ability of the fill material to accept the electrolytic process. Some via fill materials have been reported to not be compatible with permanganate chemistry commonly found in electroless copper lines. Some cases of early failure of the via fill cap-plating integrity have been traced to this process. Elimination of the programming step to process the board through permanganate will avoid this incompatibility. Plasma desmear is the generally recommended preplating preparation step. Some resin chemistries that are loaded with ceramic are susceptible to excessive surface

roughening if the plasma is too aggressive as is typical in a full etchback cycle. This becomes problematic when secondary nonfilled plated vias are required and are processed with a full etchback cycle. In this instance, it is best to choose a nonceramic filled material or modify the drill sequence so they are protected. Typically, the conductive fill materials may be electroplated directly, omitting the electroless process. If the final surface plate has secondary drilled holes that require metallization, all features may be exposed to the electroless process anyway. If directly plating the material, the fabricator should characterize the material to confirm peel strength because some cases of plating separation have been traced to poor adhesion in direct plate applications. Therefore, when choosing a via fill material, it is best to develop a process map of the required via structure processing and understand the process sequence of when drilling, filling, and plating occur.

Figure 31.22 illustrates a typical manufacturing process targeting plating allowances for the successive plating steps prior to via filling. The first plating step establishes the minimum wrap plating requirement, and deposit thickness should be adjusted for the procurement specification and the balance of final plating. Here the substrate has a panel plate followed by a button plate. One advantage of the button plate is that it serves as a visual guide for the planarization removal process. Acting as a gauge, the button, when completely sanded off, indicates any additional sanding can be assumed to reduce the wrap plating.

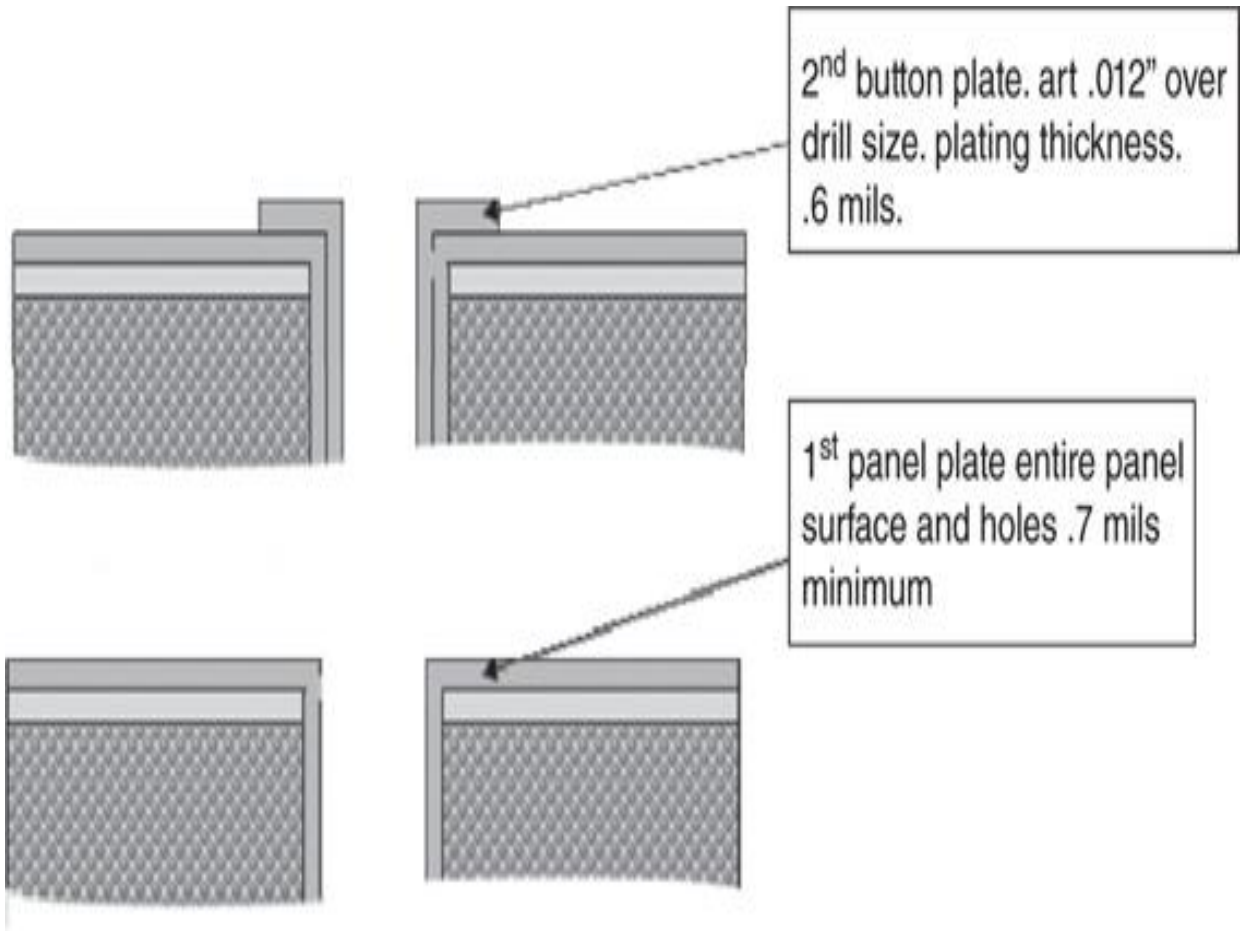

FIGURE 31.22 Pre-hole-fill plating.

31.2.4.3.2 Hole-Fill Process. Once the prefill-plating process is complete, the next major step is the actual hole-fill process. The fill materials can be divided into two major categories: conductive and nonconductive. A generic hole-fill process flow is shown in Fig. 31.23. The specific equipment and technique can vary by the material type used. The method chosen to apply the material in the holes can be influenced by many variables such as material cost, pot life, viscosity, equipment resources, and the quantity of panels to be processed. Some hole-fill materials lend themselves to a variety of fill methods. Some of the common hole-fill application methods are noted in the flowchart in Fig. 31.23. Application guideline parameters should be followed as noted in the respective material supplier data sheets. Via-

hole filling may be considered a mature process since process sensitivity has been reduced with advent of equipment designed to perform the process. Each application methods each have advantages and disadvantages associated with the technique employed.

PWB via fill application
(Generic flow)

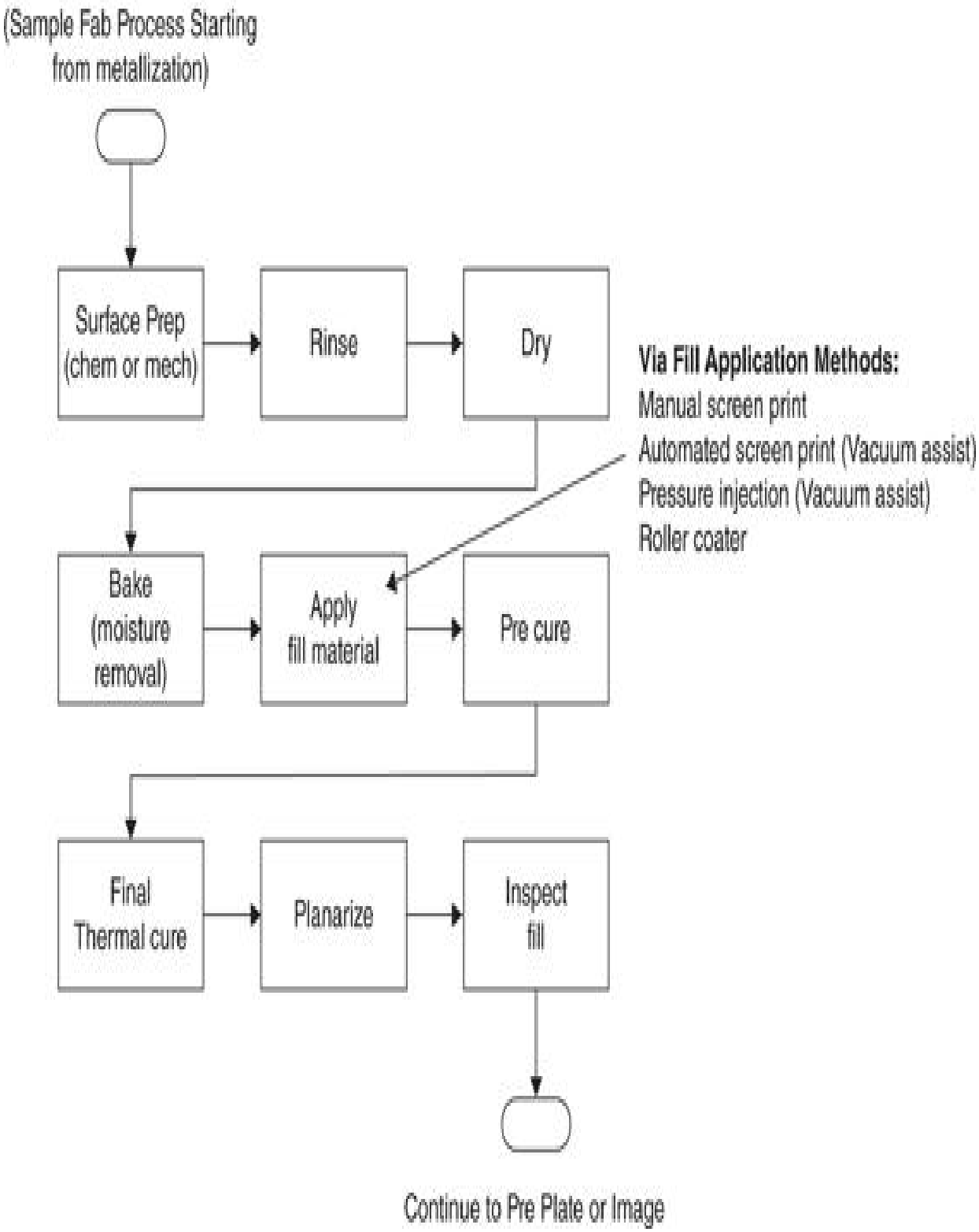

FIGURE 31.23 Generic via fill application flow.

Manual methods can be problematic. Such as when a fabricator uses screen printing, with a mask sized just over the hole size keeps excess material from being applied to the surface. Screen printing with a dot mask using a back side receiving template with open holes sized just over the plated hole diameter yields a domed fill bump. These bumps can act as a visual indicator similar to a button plate pad to indicate when the planarization is flush to the surface. Other methods include roller coating modified to squeegee excess material off the surface of the panel. Fewer problems exist with commercially available equipment designed specifically to apply fill material. One such machine uses a pressure-assisted injection method to force material into the holes under a vacuum. The principal advantage of this technique is the ability to reduce the opportunity for void entrapment.

Figure 31.24 illustrates an example of how the filled structure forms with successive steps for a non-cap-plated fill process. Note in this example how the surface button plating is mostly removed at the planarization step. Process development should be performed to target the optimum plating build-up method in regard to the process control of available planarization equipment. This means that whatever plating method is employed, both the deposit thickness across the panel and the net removal of deposit thickness as a result of planarization must be understood. Simple eddy current measurements of multiple locations across the panel are recommended prior to and after planarization sanding passes.

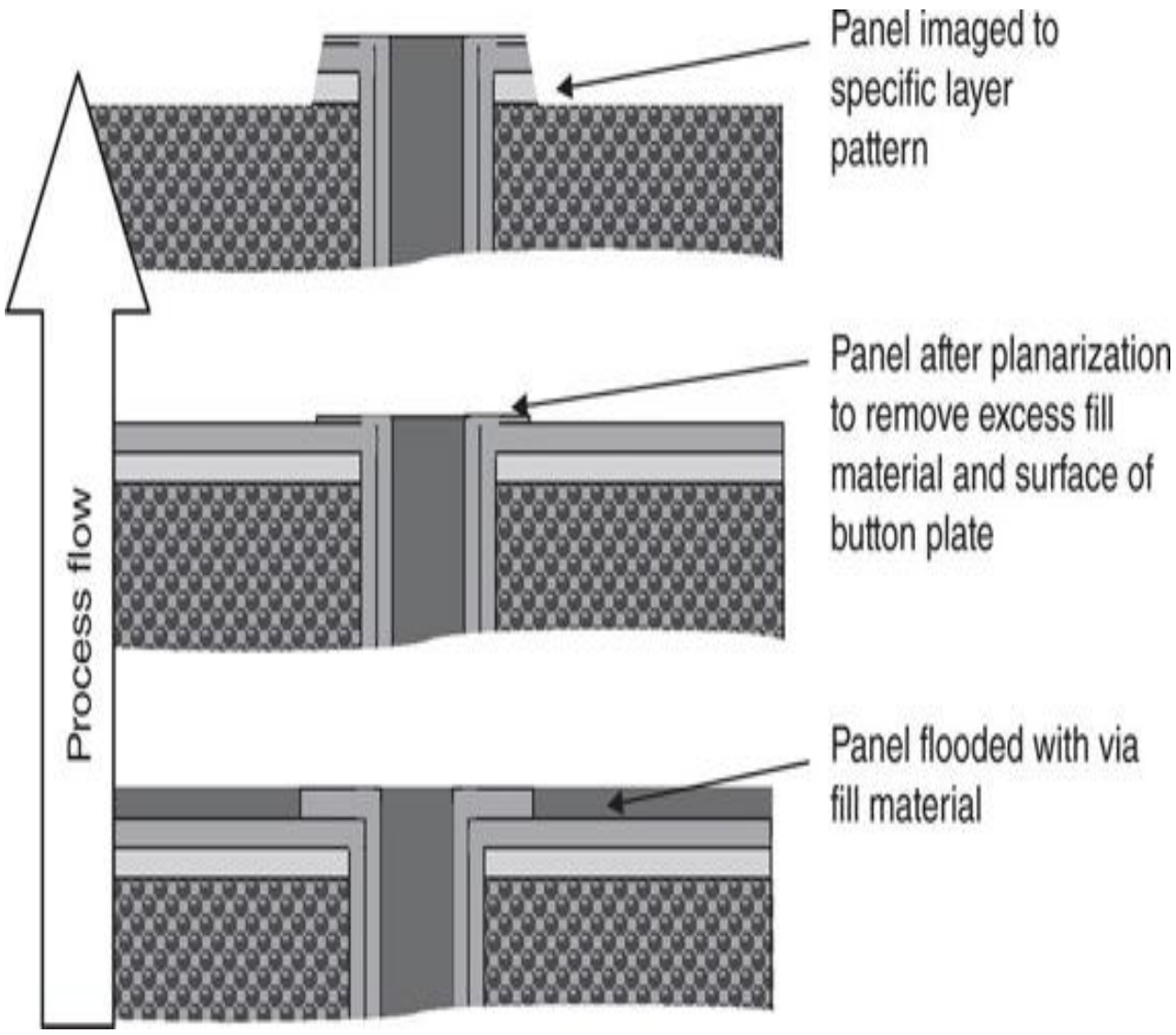

FIGURE 31.24 Non-cap-plated fill and planarization.

Once the planarization is complete, the panels are ready for imaging and etching to allow typical process flow, depending on construction type. The plating method chosen should take into account the surface pattern and construction level of difficulty. Multiple plating cycles are often required if multiple filled structures occur on the same surface plane. Excessive copper plating complicates the imaging, so the starting foil thickness should be kept to a minimum. Figure 31.25 illustrates how the fill method forms from use of a method employing cap plating over the fill material. It should be noted how the copper thickness

requiring etch can quickly build up, making pattern definition difficult.

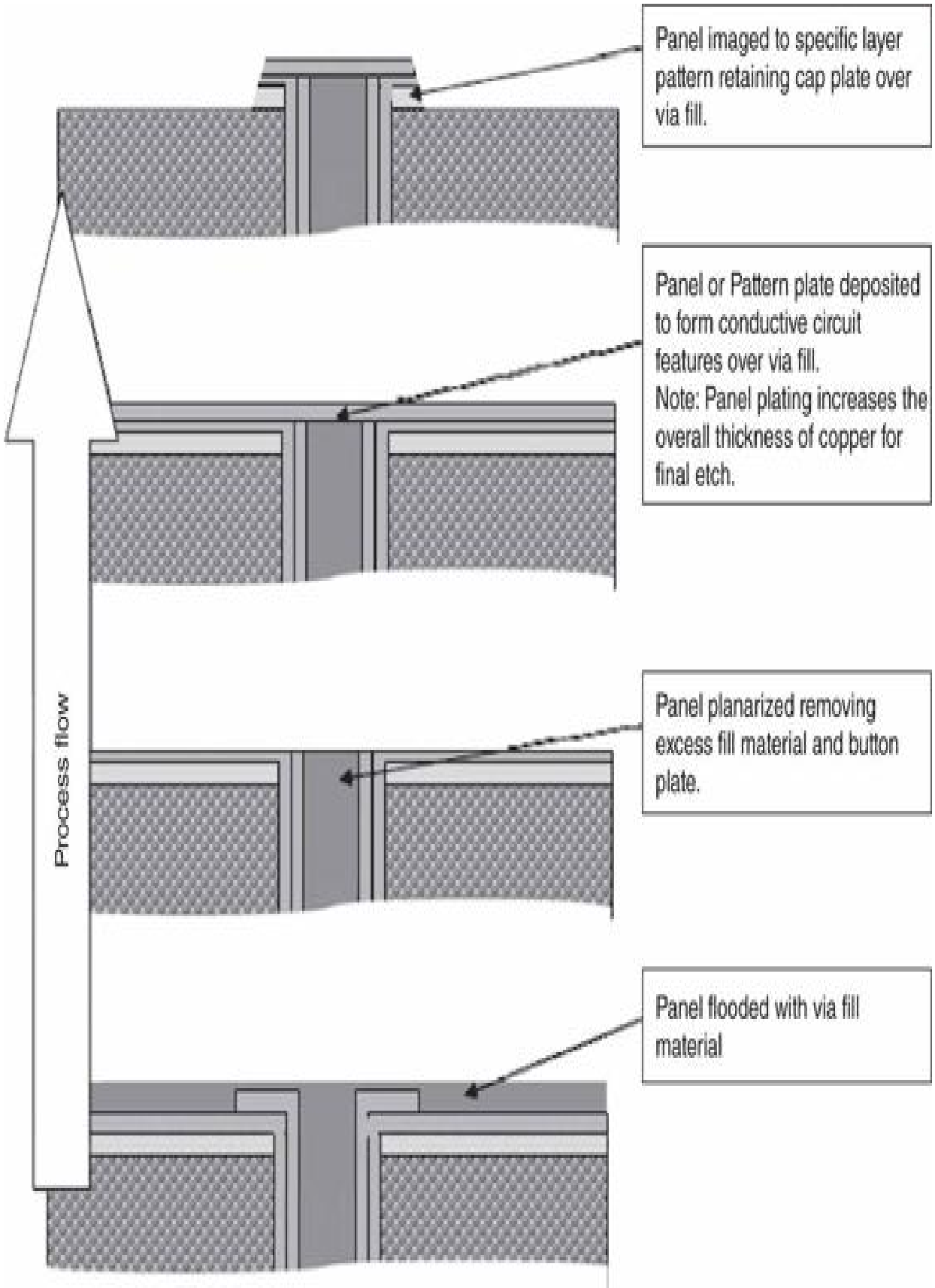
Panel imaged to specific layer pattern retaining cap plate over via fill.
Panel or Pattern plate deposited to form conductive circuit features over via fill.
Note: Panel plating increases the overall thickness of copper for final etch.
Panel planarized removing excess fill material and button plate.
Panel flooded with via fill material
Process flow

FIGURE 31.25 Cap-plated fill and planarization.

31.2.4.3.3 Specifications. The industry has released a design guideline document outlining via protection classifications, including the hole fill as described in this chapter. The IPC-4761, “Design Guide for Protection of Printed Board Via Structures,” has established via-protection techniques, creating specific types identified as Types I through VII. IPC-4761 contains many combinations of techniques where an added material is utilized to plug, tent, cover, or fill a via structure. Many of the techniques established are used in Class 1 and 2 hardware or where circuit card assembly consideration is the primary focus. Many of the 4761 via-protection types are of lower cost and lesser complexity than are those used for hole fills. The designer is encouraged to consult the application guide included in Table 5-1 of IPC 4761 to narrow the selection prior to layout and specifying a method. The via fills described in this chapter fall under the Type V and VII classifications. These types are maturely developed performance-based requirements for use in Class 3 hardware.

IPC-6012 and other IPC-6010 series specifications control minimum wrap copper. The specification limit remains at 127um (0.0005-inch) minimum wrap as verified by cross-section for Class 3 product. This is considered a conservative value resulting from the nonuniformity of the process. Correlation data is difficult and costly to verify coupons on the panel perimeter match that of the actual product. Maintaining uniformity of the planarization across the entire panel is difficult, so a conservative value at cross section was established to ensure that the part maintains wrap copper. The reliability data gathered support this value due to the additional manufacturing risk that can occur from the added fabrication steps. However, some data collected in MRB (Material Review Board) action and assessment indicate that

wrap copper as low as 0.0002 in is acceptable for some end-use environments; i.e., Class 2. Revisions of IPC 6012 continue to review the wrap requirement as the industry matures in regard to controlling the planarization process and additional reliability data become available. Additionally, some suppliers today have proprietary processes developed to lower risk associated with reduced wrap plating.

31.2.4.4 Via Fill Summary and Additional Considerations. The manufacturing of reliably filled vias should not be underestimated. Considerable process development is required to optimize the interaction of maintaining plating wrap to lower the risk associated with via fill planarization. The nature of reported failures due to compromised interconnect integrity have ranged from infant mortality at assembly to latent field failures. These failure mechanisms are very difficult to screen with standard performance verification methods. Even postassembly environmental stress screening (ESS) may not exercise sufficient stress levels to screen out marginal product effectively. This has directed some users to specify thermal shock temperature cycling at the bare-board production lot level for acceptance testing. This level of lot acceptance becomes more critical for lead-free assembly thermal stress environments, requiring the user to be more cognizant of the fill material selection.

A number of commercially available material choices exist with a wide variety of physical properties. Matching a material to a design type is necessary prior to specifying it on a drawing. Industry dialogue indicates the desire eventually to establish a material performance specification for fill materials similar to the IPC SM 840 for solder mask. The absence of a material specification requires the user to specify the brand(s) of acceptable fill materials through a user/supplier agreement. The process of specifying a hole-fill material can add cost to the PWB manufacturing process.

The process labor cost is relatively flat to apply a material with automated equipment application methods; the most significant cost variable being the material type. Some of the silver-filled conductive materials are roughly twice the cost of nonconductive materials. The process time and material cost can be roughly estimated at $25 to $50 per panel not including setup fees or minimum lot charges.

The impact to reliability is judged to be weighted more toward the suppliers' ability to successfully process the panels without degrading plated interconnects rather than the fill material type. This is followed by the ability of the manufacturer to metallize a specific fill material. The greatest number of failures reported in industry have historically been related to the planarization process. To this end, commercially available planarization equipment is now common place in the marketplace. Even with automatic planarization equipment, careful consideration should be given when specifying via fill for designs with heavy-weight copper or rigid flex constructions. Any construction that lends itself to circuit pattern imprint at the surface will have difficulty in the planarization process. Panel thickness at via structures can often be several mils thicker than open circuit areas. This change in height is not easily recognized and is problematic for producing a uniform sanding surface. Additionally, some softer materials or non-glass-reinforced materials may not be able to be planarized without distortion or gouging.

With more designs migrating to higher-density layout schemes via fill is common. The process of via fill has matured for Class 3 hardware as well. Many end users who learned difficult lessons quickly introduced their user-defined specifications for hole fill. User- defined specifications often do not lend themselves to producible limits, so consideration for via fill should be part of the DFM dialogue during the design layout cycle. The user and supplier must work closely

together to understand the impact of specifying hole fill for each design construction method employed.

31.3 ML-PWB PROCESSING AND FLOWS

31.3.1 Process Flowcharts

Attempting to visualize the process flow of the manufacture of multilayer printed wiring products can be overwhelming. One way to help picture the multiple paths a board travels is through the use of flowcharts. The flowchart in Fig. 31.26*a* is a typical process flow for the beginning innerlayer process identified as 1 through 4. Figure 31.26*b* is a typical finish board flow process after lamination and drill. Three additional diagrams are provided in Fig. 31.27 that represent possible sequential flows for HDI products. They are identified as processes 5, and 6 referring to how the different HDI types might flow. It should be noted that alternative flows and methods are possible in HDI. This discussion is limited to mostly conventional processing. Major aspects of these processes are discussed in detail in the following sections.

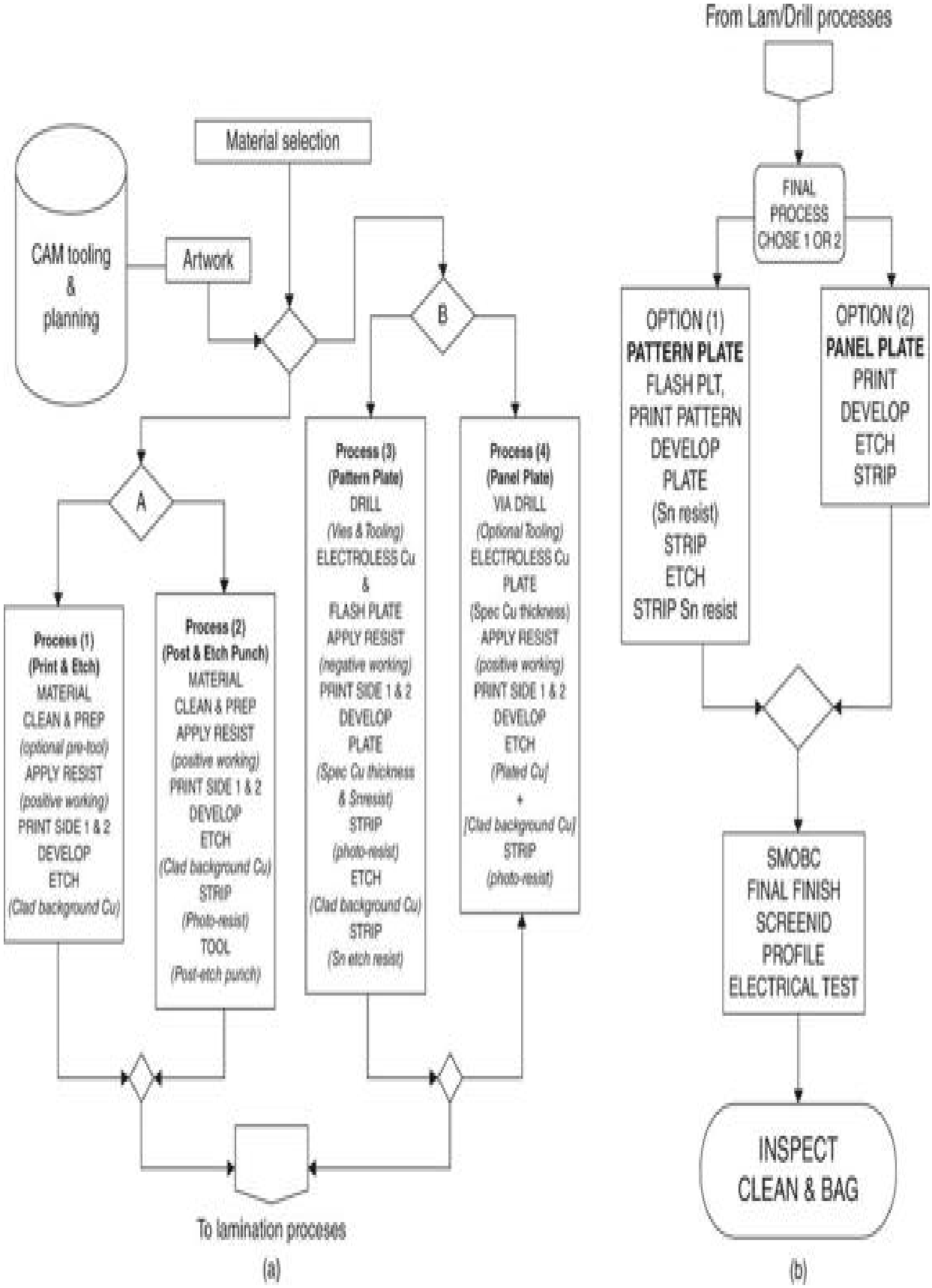
Material selection
CAM tooling & planning
Artwork
A
B
Process (1) (Print & Etch)
MATERIAL
CLEAN & PREP
(optional pre-tool)
APPLY RESIST
(positive working)
PRINT SIDE 1 & 2
DEVELOP
ETCH
(Clad background Cu)
Process (2) (Post & Etch Punch)
MATERIAL
CLEAN & PREP
APPLY RESIST
(positive working)
PRINT SIDE 1 & 2
DEVELOP
ETCH
(Clad background Cu)
STRIP
(Photo-resist)
TOOL
(Post-etch punch)
Process (3) (Pattern Plate)
DRILL
(Vias & Tooling)
ELECTROLESS Cu
&
FLASH PLATE
APPLY RESIST
(negative working)
PRINT SIDE 1 & 2
DEVELOP
PLATE
(Spec Cu thickness & Snresist)
STRIP
(photo-resist)
ETCH
(Clad background Cu)
STRIP
(Sn etch resist)
Process (4) (Panel Plate)
VIA DRILL
(Optional Tooling)
ELECTROLESS Cu
PLATE
(Spec Cu thickness)
APPLY RESIST
(positive working)
PRINT SIDE 1 & 2
DEVELOP
ETCH
(Plated Cu)
+
(Clad background Cu)
STRIP
(photo-resist)
To lamination processes
(a)
From Lam/Drill processes
FINAL PROCESS CHOSE 1 OR 2
OPTION (1) PATTERN PLATE
FLASH PLT,
PRINT PATTERN
DEVELOP
PLATE
(Sn resist)
STRIP
ETCH
STRIP Sn resist
OPTION (2) PANEL PLATE
PRINT
DEVELOP
ETCH
STRIP
SMOBC
FINAL FINISH
SCREENID
PROFILE
ELECTRICAL TEST
INSPECT
CLEAN & BAG
(b)

FIGURE 31.26 Process flowcharts: (*a*) a typical process flow for the beginning innerlayer processes identified as 1 through 4; (*b*) a typical finished board flow process after lamination and drill.

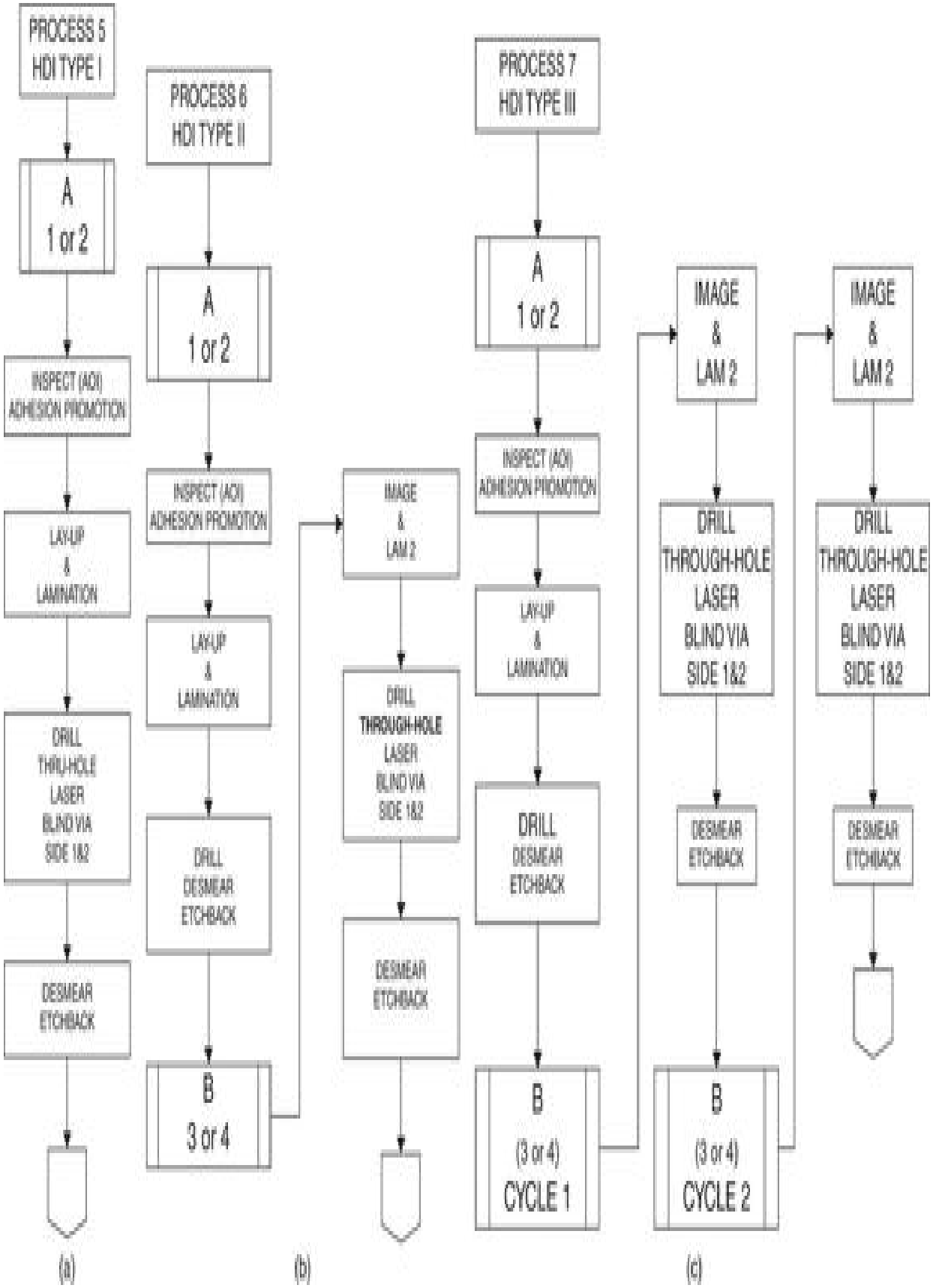
PROCESS 5
HDI TYPE I
A
1 or 2
INSPECT (AOI)
ADHESION PROMOTION
LAY-UP
&
LAMINATION
DRILL
THRU-HOLE
LASER
BLIND VIA
SIDE 1&2
DESMEAR
ETCHBACK
PROCESS 6
HDI TYPE II
A
1 or 2
INSPECT (AOI)
ADHESION PROMOTION
LAY-UP
&
LAMINATION
DRILL
DESMEAR
ETCHBACK
B
3 or 4
IMAGE
&
LAM 2
DRILL
THROUGH-HOLE
LASER
BLIND VIA
SIDE 1&2
DESMEAR
ETCHBACK
PROCESS 7
HDI TYPE III
A
1 or 2
INSPECT (AOI)
ADHESION PROMOTION
LAY-UP
&
LAMINATION
DRILL
DESMEAR
ETCHBACK
B
(3 or 4)
CYCLE 1
IMAGE
&
LAM 2
DRILL
THROUGH-HOLE
LASER
BLIND VIA
SIDE 1&2
DESMEAR
ETCHBACK
B
(3 or 4)
CYCLE 2
IMAGE
&
LAM 2
DRILL
THROUGH-HOLE
LASER
BLIND VIA
SIDE 1&2
DESMEAR
ETCHBACK
(a)
(b)
(c)

FIGURE 31.27 Diagrams representing possible sequential flows for HDI products. They are identified as processes 5, 6, and 7, referring to how the different HDI types mentioned in the text might flow.

31.3.2 Innerlayer Materials

The multilayer process begins with the accumulation of the innerlayer clad dielectric laminate.

31.3.2.1 Documentation and Specifications. The ML-PWB design documentation should specify the specific material system to be used in the fabrication. Typically materials are identified by IPC-4101 callout or slash sheet designation, for example, IPC-4101/24. Copper weights as well will be specified within the drawing documentation. The specification IPC-4562, "Metal Foil for Printed Wiring Applications," provides reference to the various weights of copper foils along with an applications use guide. The common terminology refers to foils less than oz/ft^2 as a metric thickness of micrometers.

31.3.2.2 Copper Foil. High-current applications use heavier (thicker) copper of 2 oz or above. With copper weights above 3 oz, processing difficulty is increased. High-density circuit designs that have low voltage and that are mainly concerned with passing signals may use thinner copper weight foils, such as 18 µm or less. When sequentially processing clads as buried via pairs, the fabricator must use thin starting foil to promote line definition and image integrity and, where necessary, impedance-controlled tracks. Copper foil is fabricated in an electroplating process on a rotating drum that produces a coarse-grained columnar copper. The economy of the foil process always yields copper at the minimum thickness tolerance. Due to the speed of the foil process, often a course grain structure can yield poor elongation. Elongation

is a property of major importance in reducing trace fracturing. Standard copper foils typically fail at elongations around 3 percent. IPC-4562/3 high-temperature elongation (HTE) provides a slight, but important, improvement in elongation from 5 to 8 percent. High-ductility electrodeposited foil, called HD-Type E (IPC-4562/2), is specified to withstand an elongation of 10 percent minimum. Foil vendors also sell special fine- grain-structure, annealed, or wrought foils. The foils with higher elongation are advertised to have superior etch performance for fine-line densities.

Standard foils have a rough surface called *tooth* on one side (drum side out) and a smooth or shiny surface on the opposite side (drum side). The rough side, treated with an adhesion promoter, is laminated against the C-stage dielectric to ensure good adhesion. Since the shiny side of the copper has poor adhesion characteristics, the ML-PWB fabricator must include adhesion promotion steps prior to resist lamination and prior to final board lamination. Double-treated copper foil has an adhesion promoter applied to both sides and is attractive in high-volume applications. Although double-treated foil requires no further adhesion promoting treatments, it has several process disadvantages to overcome:

- Cleanliness and material handling sensitivity is more critical.
- The cost often offsets the savings from the eliminated processes.
- It is somewhat fragile, so it is difficult to rework.
- Complete resist development is difficult, leading to a high incidence of shorts.
- It is not compatible with the plating processes used to make buried and blind vias.

Another foil type offered by laminate suppliers, reverse-treated foil (RTF), offers an advantage for producing fine lines. The RTF copper has adhesion promoter applied to both sides and is classified by 4562 as code R (reverse-treated bond enhancement [cathode side] stain-proofing on both sides). This approach provides advantages to imaging fine lines. When the copper tooth is reversed, the fabricator can improve line definition by allowing the etch chemistry process to stop sooner at the surface of the laminate.

31.3.3 ML-PWB Tooling

The tooling system employed for ML-PWB fabrication is one of the most critical aspects of the process and requires much forethought. The investment in tooling is significant and not easily changed. Planning is required to determine the degree of flexibility that is needed in a tooling system based on the types of ML-PWBs that will be produced in that facility. The ML-PWB tooling system can be broken down into four aspects: the panel size scheme, the front-end tooling, the method of generating tooling holes, and the hard tooling (plates).

31.3.3.1 Panel Size Scheme. The first decision is to choose from essentially three broad approaches to panel size: full sheet, or mass-lamination; standard panel sizes based on cuts from a full sheet; or customized (flexible) panel sizes based on cuts from a full sheet. Any particular facility may also employ more than one approach.

31.3.3.1.1 Mass-Lamination. Sheet sizes can be 24 × 48 in; 36 × 48 in; 48 × 52 in; 1.5 × 2 m; or other similar large formats. This approach is well suited to medium or mainstream technology requirements in lines and spaces, and hole-to-pad ratio. It works best with larger sized PWBs since too many small PWBs leave too much blank space

between the circuits, wasting the principal advantage of full-sheet lamination. Typically, the copper foils are standard weights. The cores are 0.004 in (1.0 mm) or thicker, although some mass laminators are capable at 0.002 in (0.05 mm); and the lamination is a single-resin system, not a mixed dielectric build. The most common construction is from epoxy resin, since most of the enhanced electrical or thermomechanical resin systems are not available in large sheet sizes.

31.3.3.1.2 Standardized Size Cut Panels. This approach is dominant in high-end technology PCBs. Some very common panel sizes are 18 × 24 in and 20 or 21 × 27 in. The facility strives to have the fewest number of standardized panels that will accommodate the majority of the MLB sizes typical of their customer base. Tooling is then either fully fixed or modular based on those panel sizes, but other new panel sizes are not possible without new hard tooling and die. Having four to eight panel sizes is common. These sizes are based on full yield cuts from the laminator's full sheets; for example, the laminator might offer a 36 × 48 or 42 × 54-in sheet and the fabricator orders (or cuts from full sheets) 14 × 18, 12 × 24, 18 × 24, and 21 × 27-in panels. This system standardizes tooling into the fewest number of different sizes of hard tooling (e.g., caul plates and separator plates; see Sec. 31.5.1.1). This approach is also best suited to advanced feature sizes, where limiting the panel size to just over the MLB size has the advantage of reducing some degrees of difficulty such as the registration requirement over a larger area. Fixed panel sizes work well for mixed dielectric builds and sequential laminations. Very large cut panel sizes such as 24 × 36 in, approaching mass lamination size, are uncommon but available in very high-volume or backplane fabrication specialty facilities.

31.3.3.1.3 Custom-Cut Panels. Asian fabricators have pioneered flexible custom-cut panel sizes to maximize material utilization further and so reduce costs. The

difference between standard and flexible cut panels is that standard-cut panels have a limited number of predetermined sizes and consequent hard-tooling configurations, while the flexible cut panels afford a continuous range of size because the tooling isn't fixed but highly configurable. Flexible cut panels are often paired with riveting instead of pinning to hold the details, prepreg, and foil together for lamination. Many Asian facilities will offer both approaches, selecting the best suited to the job at hand.

31.3.3.2 Front-End Tooling. The first aspect of the ML-PWB tooling is commonly called front-end tooling or simply computer-automated manufacturing (CAM) tooling. (Current data transfer XML schema is migrating to IPC-2581 to replace Gerber.) The front end is where manufacturing personnel using a CAM software package generate all phototools or output directly to Laser Direct Imaging (LDI), the associated computer numerical control (CNC) electronic files (used by equipment such as drillers and routers), the construction stack-up, and the part manufacturing instructions, or "work order," also called the "traveler." The CAM station mirrors the tooling method chosen for the shop and the job's work order. The CAM software overlays the tooling pattern on each circuit layer to produce the master pattern alignment. The master artwork pattern is then photo-plotted to reproduce the artwork film tools for the imaging operations. Several important manufacturing functions fall within the bounds of the front-end tooling responsibility.

31.3.3.2.1 Design Rule Check (DRC). Design rule check (DRC) is where the electronic design data are analyzed against a specific set of fabrication rules, a virtual simulation of the design for manufacturing (DFM). The capabilities and attributes of these rules are based on sound, industry-proven values that match the technology targeted for construction. The default values embedded into the CAM are input by the manufacturer as technology files. These files should reflect

the capability of the fabricator’s equipment and processes in light of how they are utilized against the ML-PWB type being produced.

31.3.3.2.2 Panelization. To gain economies in the manufacturing process, the individual board design is stepped and repeated within the artwork tooling. Panelization is the term used to describe this method. Here the elemental goal is to yield as many parts on one process panel as possible. The CAM software allows manipulation of the single design pattern to place or nest multiples within the confines of the chosen panel dimensions.

31.3.3.2.3 Artwork Generation (Photo-Plotting). Once the design has been formatted into the desired panelization, it is ready to be made into a working phototool or LDI data format. The CAM data are output to a server that converts the data into a language recognizable by the plotting/LDI equipment. The plotter exposes the circuit pattern on the film tool or direct writes it to the resist coated panel. Typically, the film tool is polyester-based with a silver emulsion and is exposed by means of a laser or fiber-optic light source. The resolution of the light source directly affects the ability to image the technology type. Note that when the technology type approaches the feature size of HDI, the use of an alternative approach to phototooling are commonly employed. This is known as laser direct imaging, and, as the name implies, the image is directly exposed onto the production innerlayer, thereby eliminating the use of a phototool.

31.3.3.2.4 CNC Drilling Routing Tools. The machine communication method commonly employed in the automation of the drilling and routing process is output from the CAM tooling as CNC programs (from the earliest computer numerical control machines, as differentiated from manual or template positioning systems). The front-end tooling software facilitates the organization and optimization of the CNC routine. The routine must match the flow of the

technology process steps being produced. When sequential processing is required, the drilling routing data must be broken out into separate routines. When the technology type involves HDI features that require laser drilling, specific tooling accommodations have to be considered to match the discipline of the laser equipment—for example, the use of special imaged fiducial targets or a special etched dot mask aligned to the drill locations.

31.3.3.2.5 Automatic Optical Inspection. Another aspect of the tooling set is the data configuration to support the automated optical inspection (AOI) process. AOI is considered part of the detailed inspection process. When the AOI equipment supports what is known as CAD reference, the original design data are now output as a configured file to compare the imaged circuit layer to the original designed circuit (see Chap. 53 for a complete discussion of inspection).

31.3.3.2.6 Electrical Testing. The final aspect of the tooling set is preparation of the electrical design data to support an electrical testing routine. The purpose of the electrical testing within the ML-PWB production process is to verify the integrity of circuit continuity. The electrical data required for the test must be extracted from the circuit pattern unless a separate net list is provided that contains the connectivity. The standard data format for electrical testing is IPC-356.

Electrical testers can take on many forms, but are generally divided into two major categories, the bed-of-nails and the flying probe. Tooling for a bed-of-nails tester consists of outputting data to manufacture a fixture to accommodate the pins, which make contact with the circuit nets. When a flying probe tester is employed, the net data are fed into the machine, which uses its own software to configure the routine to probe continuity and perform isolation. (See IPC-9252 for standard industry test parameters)

The chosen method of test tooling requires an examination of the economics based on the volume and technology of the ML-PWB. For small prototype lots required in short cycle times, flying probe may be more suitable than bed-of-nails testing. Although the throughput of a flying probe unit is less than that of a bed-of-nails tester, the flying probe does not require expensive, and time consuming to construct, fixtures. When the technology type involves HDI features, the only alternative is to use a flying probe due to the limitation of the grid spacing in a bed-of-nails tester. High-density test requirements continue to drive flying probe technology. (See Chaps. 39 to 42 for a complete discussion of electrical testing.)

31.3.4 Tooling Hole Formation

The shape, size, and location of tooling holes or slots are dependent on the investment tooling system determined by manufacturing engineering for a given facility, and there a variety of methods to form them. The tooling holes range in size and shape from 0.125 to 0.250-in diameter to a slotted hole of 0.187 × 0.250 in. The common methods used to produce the mechanical alignment in innerlayers are punch and die or drilling, but the point in the process where they are formed can vary depending on the total tooling scheme. New tooling schemes are coming to the marketplace that eliminate dependence on tooling holes described below. This new method inductively bonds layers together prior to lamination eliminating the tooling pins/holes.

31.3.4.1 Prepunch. The oldest method, fixed punch and die set are used to generate tooling holes/slots prior to imaging/etching. To avoid having to cut away the photoresist material over the tooling hole, fabricators sometimes perform the punching after resist lamination. In this case,

cleanliness has to be significantly refined. If a cut sheet resist laminator is used, it can be adjusted so the resist falls inside the boundary of the tooling locations. The punching occurs in a hydraulic punch press, where alignment is ensured by means of an edge stop on two axes of the panel to square the alignment. The die set penetrates the laminate in one stroke, punching all holes at one time while holding the material flat. Material is punched one piece at a time, yet high throughput can be achieved by this method. Punching of multiple laminates at once is not recommended because the quality and size of the tooling hole/slot are affected. Additionally, thicker laminates (greater than 0.032 in) require the punch and die set to have a slightly larger tolerance to accommodate the spring-back of the hole within the composite material. Overall, the prepunch method is very accurate and repeatable. Materials with a high degree of movement (low-dimensional stability) are at a significant disadvantage in this method due to the drift of the tooling location after innerlayer processing.

31.3.4.2 Post-Etch Punch. A more popular method uses an optically aligned punch to generate holes/slots after imaging/etching. The fully processed innerlayers are edge-aligned into the punch; a pair of video cameras locates on a diagonal pair of printed fiducials; a servo-system aligns the panel, minimizing alignment errors due to panel distortion; and tooling holes are punched. This process punches an optimized set of tooling holes/slots in the layer just prior to lamination. Post-etch punch can be automated so it has high productivity, but it is slower than a simple punch and die. However, the productivity gain achieved by printing without tooling reduces some of the productivity loss from using post-etch punch.

31.3.4.3 Drilled Tooling. When processing follows the process sequence 3 and 4 described earlier, tooling locations

may be drilled by X-Ray location of buried fiducials. This allows the tooling locations to be formed prior to the via-drill cycle. This accommodates the effects of final registration accuracy by optimizing for scaling of the pattern. i Scaling helps minimize the dimensional effect that processing has on the true positions of the holes. Alternatively, extra sets of tooling holes may be produced just for the imaging process, followed by a post-etch punch operation to optimize the lamination registration.

31.3.5 Tooling System

There are numerous rationales for innerlayer tooling schemes, and this has resulted in a wide assortment of tooling systems being used across fabricators. Over the years, many tooling systems have evolved, ranging from full-perimeter distribution of holes to as few as four holes located on the midaxis. One low-cost tooling system comprises use of rivets in a flexible layout scheme. The tooling system comprises a substantial investment and therefore merits considerable engineering conceptual judgment. Many shops become trapped with poorly conceived tooling schemes that are difficult to migrate from due to the cost of converting earlier designs. Therefore, careful analysis should be given to the product mix and technology types to be manufactured prior to choosing a scheme.

The primary purpose of the tooling system in ML-PWB manufacturing is to facilitate layer-to-layer alignment during the lamination cycle while maintaining a positional reference for subsequent processing. The tooling hole arrangement is mirrored within the front-end tooling routines mentioned earlier. The master alignment of each part keys off the tooling scheme. The primary tooling locations may be used at all process steps or sometimes used to introduce secondary reference holes.

Figure 31.28 shows three different tooling schemes. Figure 31.28*a* shows a system known as four-slot tooling. This is an excellent system, because the use of four slots allows for growth and shrinkage of the layers during processing. The four slots may be used for printing, inspecting, and lamination, or, if post-etch punch is used, they are used for inspection and lamination only. Figure 31.28*b* shows a system known as four-slot/four-hole. This is common in a pre-punched system where the slots are used for image printing and the extra holes are engaged at lamination. Alternatively, punched slots can be used for innerlayer image and lamination, while post-lamination holes are drilled for plated holes' drilling and outerlayer imaging. In this method, targets imaged in the details under the outerlayers are exposed by controlled depth boring; a camera then locates the targets and a spindle drills the locating holes for the secondary operations. Figure 31.28*c* shows a tooling system with a full perimeter of holes placed. This style would be considered overdetermined. It has a disadvantage at lamination because imaged panels typically have to be stretched over the alignment pins. A fourth tooling system not shown uses low-profile rivets to align layers. The rivets can be arranged outside the pattern area and do not penetrate into the caul plate. Rivet height is chosen based on the appropriate panel thickness. Alternative to rivets a newer process inductively bonds layers together in place of rivets.

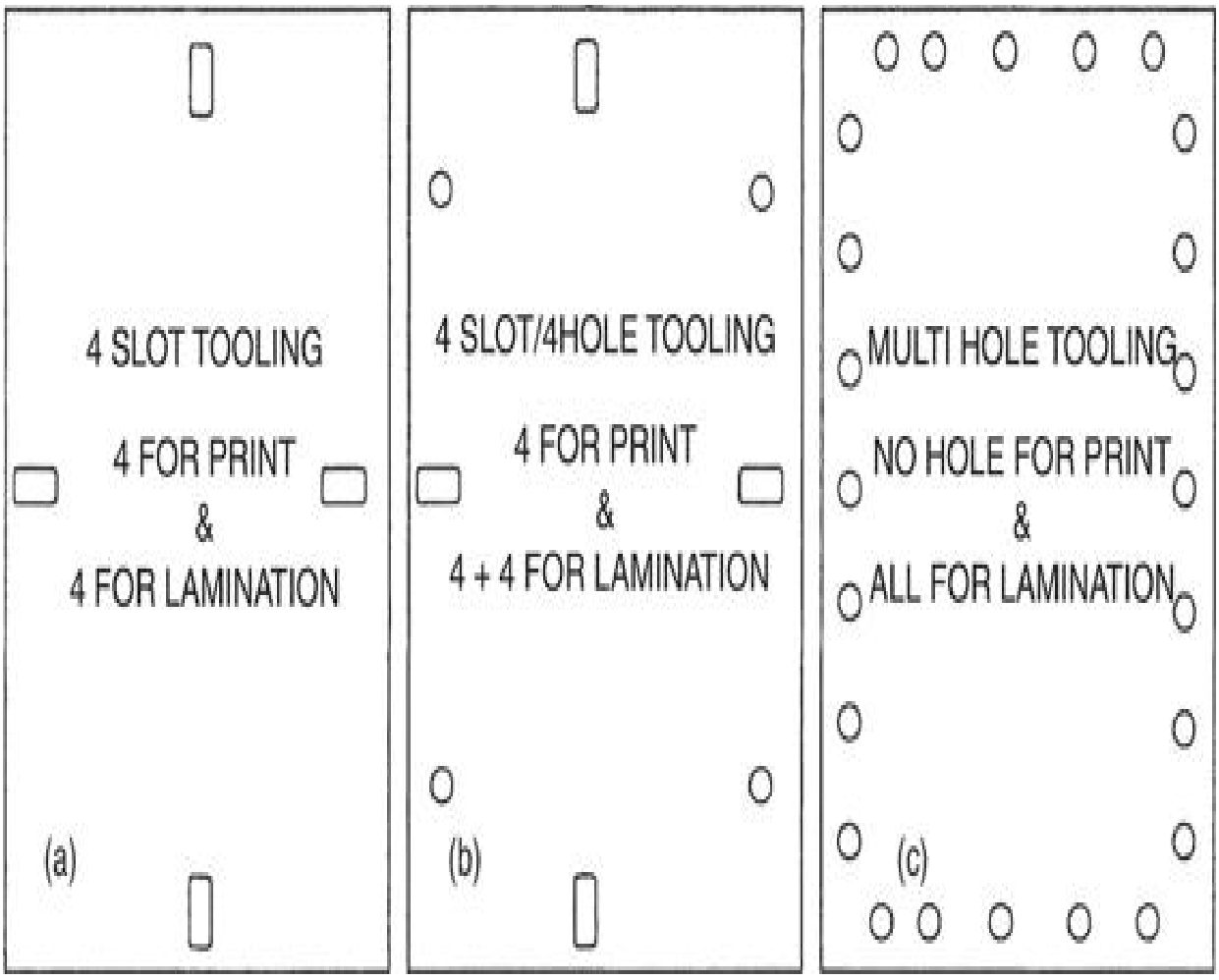

FIGURE 31.28 Three different tooling schemes: (*a*) four-slot tooling, (*b*) four-slot/four-hole; (*c*) a tooling system with a full perimeter of holes placed.

31.4 LAMINATION PROCESS

The lamination process is an essential step in the fabrication of an ML-PWB. The process is also one of the longest cycle time operations. Therefore, when the process method calls for repeat cycles, or what is called sequential laminations, it can be a significant cost driver. (*Note:* Sequential lamination is often paired with distinct, separate drill and plate processes for the subcore that further ratchets up pricing, as they are also time-intensive operations.) The lamination

process involves two distinct yet linked operations: lay-up and laminating.

31.4.1 Lay-Up and Materials

Lay-up occurs in a clean and controlled room environment. The level of environmental control depends on the circuit feature technology being fabricated. The lay-up process for standard multilayer processing is relatively forgiving. However, working with material that is hygroscopic will require additional measures. The innerlayer details require a bake cycle (typically 105 to 110°C for 1 h minimum) to remove moisture. A reduced bake cycle duration is indicated when certain oxide reduction chemistries are employed. Once layers are readied for lay-up, they should be processed as soon as possible. Should extended hold times become necessary, storage in a nitrogen-purged dry box is recommended.

The lay-up operation is often referred to as “building up a book.” The operation follows a guide, often referred to as a stack-up sheet. The guide sheet, which depicts the engineering design of the ML-PWB, is highly recommended to minimize error. The written and illustrated guide to the book build-up process is made a part of the job planning/traveler. Due to the complexity of some products, the operator follows this guide in a recipe-type manner to perform the systematic construction. The lay-up may consist of some four or more PWB material components or other subassemblies. The lay-up operation produces a large assembly when complete that consists of the tooling plates, consumable press materials, and the ML-PWB detail. Refer to Figs. 31.29 and 31.30 for illustrations of the following.

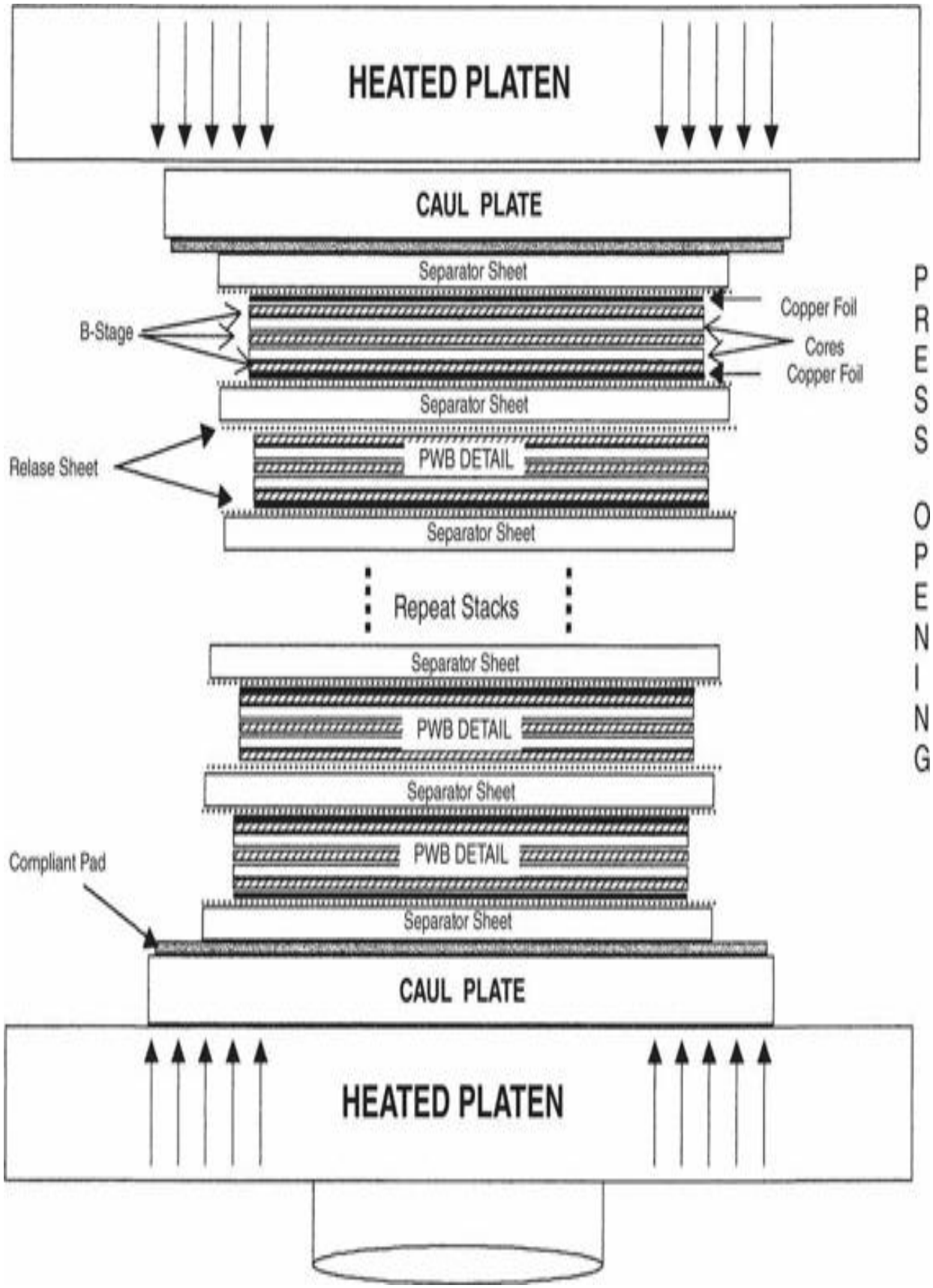
HEATED PLATEN
CAUL PLATE
Separator Sheet
Copper Foil
B-Stage
Cores
Copper Foil
Separator Sheet
Relase Sheet
PWB DETAIL
Separator Sheet
Repeat Stacks
Separator Sheet
PWB DETAIL
Separator Sheet
PWB DETAIL
Compliant Pad
Separator Sheet
CAUL PLATE
HEATED PLATEN
PRESS OPENING

FIGURE 31.29 Typical ML-PWB stack-up for hydraulic lamination.

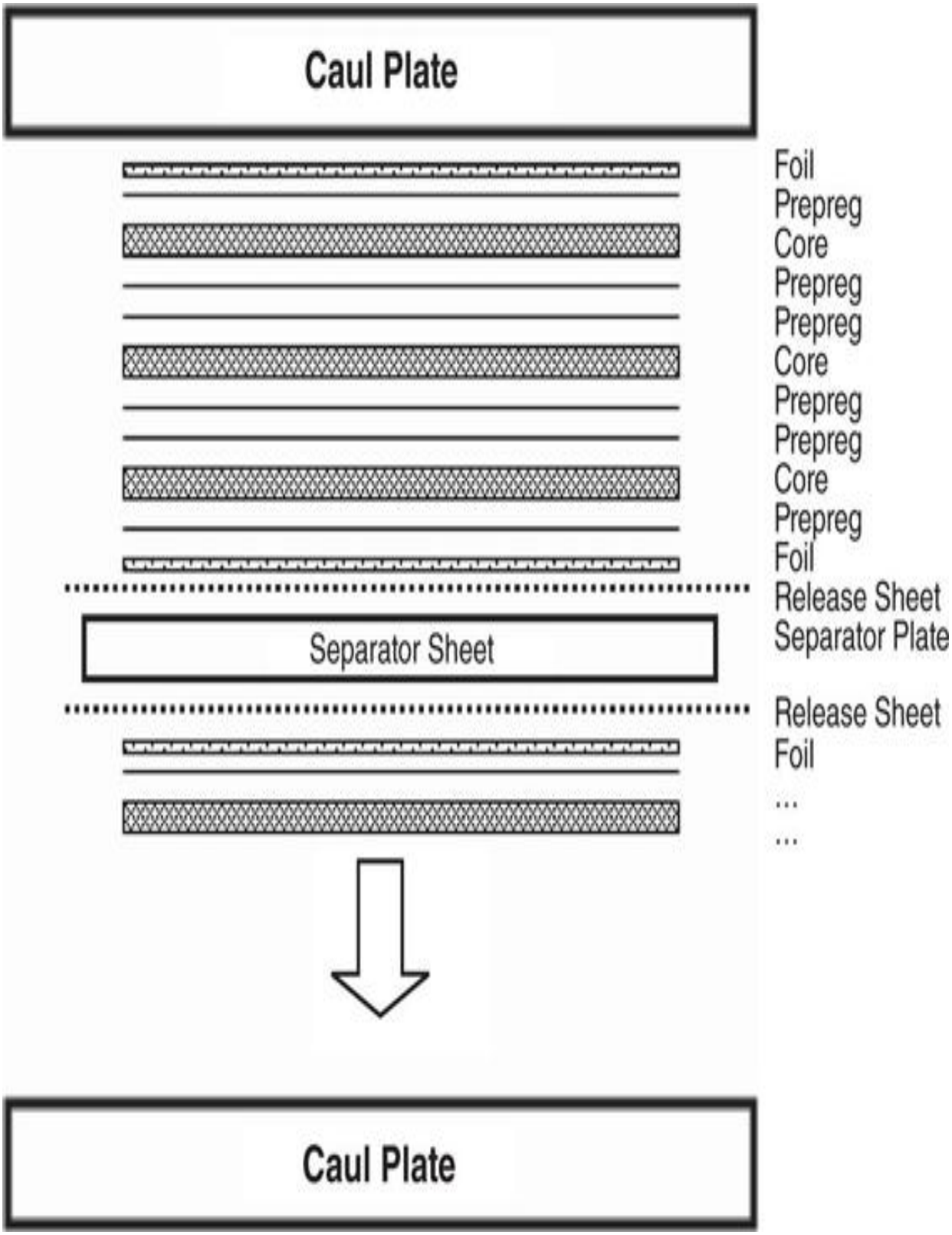

FIGURE 31.30 Press stack-up using release sheets and a separator plate.

31.4.1.1 Tooling Plates. The outermost item in the stack is termed a caul plate or carrier plate. These are thick, oversized metal plates, generally made of ⅜ in (9.525 mm/0.375 in) thick steel. The 4130 alloy of steel is often chosen due to its precision machining capability for placement of the holing holes. Sometimes a hardened aluminum alloy is chosen, but is not highly recommended due to its high in-plane expansion. The purpose of the caul plate is to provide a stable base to transport the ML-PWB stack.

31.4.1.2 Separator Plates. The multilayer boards in the stack are isolated from each other by metal separator plates. The separator plates provide a mold surface for the laminated ML-PWB. It is extremely important that the separator plates be clean and free of debris. Both aluminum and steel separator plates are used. Separator plates should be cleaned regularly. The surface finish of the plates becomes very critical when laminating against microfoils that will be printed with fine lines. The most common type of steel is one of the 400 series stainless steels that have a very durable surface. Hardened 300 series steels are also occasionally used. Separator plate thicknesses range from as thin as 0.015 in to as thick as 0.062 in. The thicker plates are more rigid and resist the tendency of internal layer features to print through from one ML-PWB to another. Thin aluminum plates have the advantage of being disposable, eliminating the need for cleaning.

31.4.1.3 Consumable Press Materials. The purposes of consumable press materials placed between the tooling plate and the top layer are to ensure that pressure is applied uniformly and to provide thermal lagging to correct heat rise. The purposes of consumable release sheets placed in contact with the foils are to protect the outerlayer foils,

keeping them resin-free, and to allow easy separation of the foil from the separator sheet.

Among the materials used to provide for pressure and temperature uniformity are multiple sheets of Kraft paper, silicone rubber pads, expanded mat paper, and composite board. Kraft paper and composite board have the advantage of low cost, but produce an odor that some press operators find objectionable. Silicone rubber pads have the advantage of being reusable, but are limited by the number of heat cycles they can withstand. Silicone rubber pads, when close to the end of their life, go through reversion and leach out silicone oil, which can become a source of contamination. They also have limited success in controlling edge voids. Excellent results are reported with expanded paper mat products that are commercially available. Mat paper press pad materials come in different thicknesses. Some are even produced with a sandwich layer of release material cohered. Other products exist that flow and thus act as a stop for resin during lamination of subcores with predrilled blind vias.

Some form of release material is required against the outer foil surface of the ML-PWB. The release material acts as a nonstick slip sheet to keep the copper surface smooth, minimize the plate cleanup, and catch the resin run-out. Figure 31.30 shows the location of the release sheets. Alternatively, oversized foil can be used to catch the resin run-out. Or, a product called C-A-C (for copper-aluminum-copper) is used that consists of two sheets of foil laminated to either side of an aluminum carrier sheet. In this configuration, the one sheet of C-A-C is between two PCBs with the bottom copper foil over prepreg to form the top side of the bottom PCB, and the top copper foil under prepreg to form the bottom side of the top PCB. Figure 31.31 shows the location of the C-A-C sheet. The aluminum serves to replace the steel or aluminum separator plates and has the added benefits of reducing the stack height (which can sometimes translate to increased productivity by enabling another board

to be made in the “book”) and providing excellent protection to the surface of the outerlayer foils. Since they are not handled as foils but as a more rigid composite, there is no propensity to wrinkle, and since they are covered for the entire book-building operation, they are not subject to scratching or having errant debris introduction cause a pit during lamination. Finally, when the book is broken down, the aluminum between the ML-PWBs is easily separated from the foils, leaving the distinct ML-PWBs. The aluminum itself is sometimes sent to the drilling department to be used as an entry material, and then sent to reclamation.

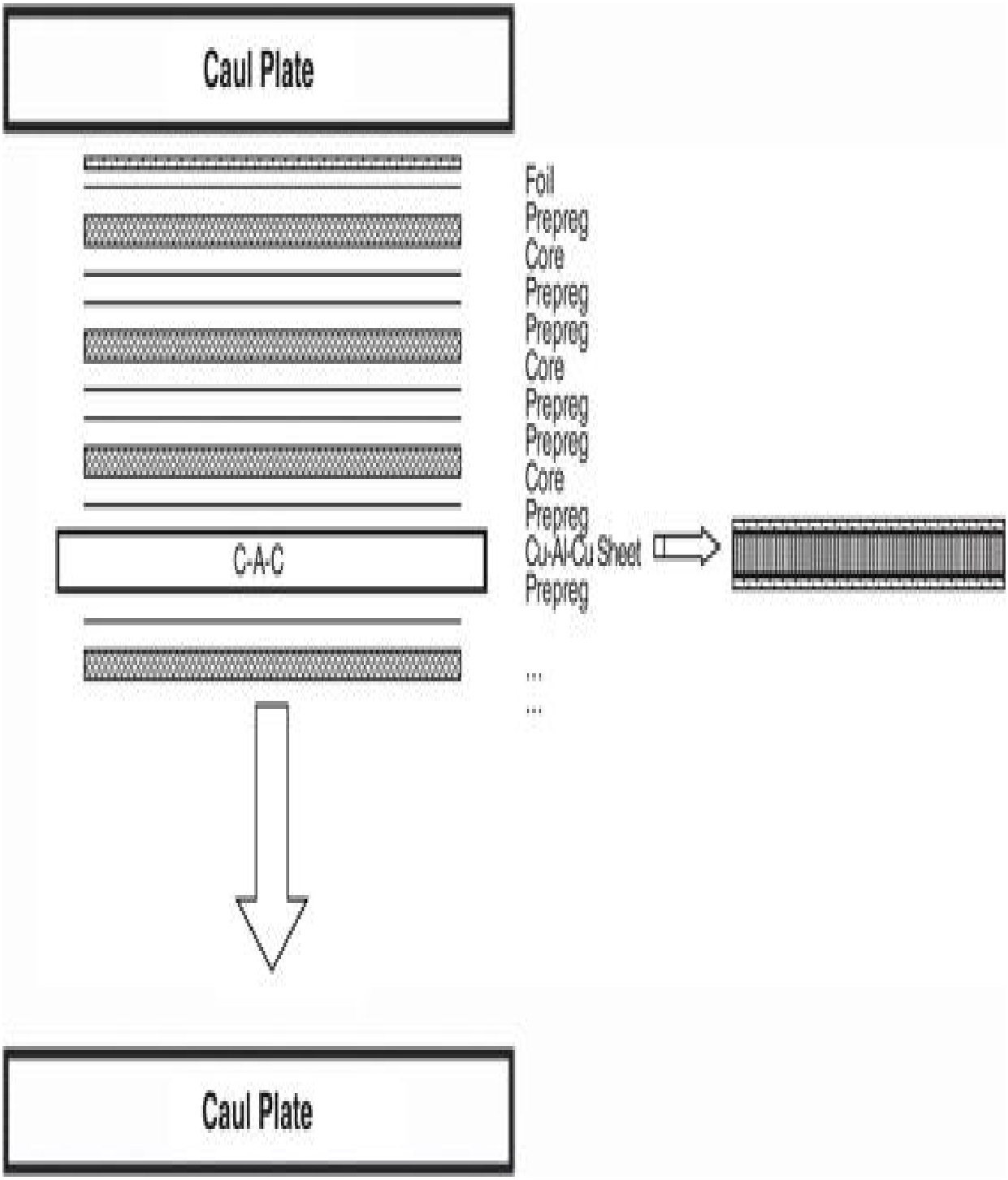

FIGURE 31.31 Press stack-up using one sheet of C-A-C to replace two sheets of foil, two release sheets, and one separator plate.

31.4.2 Lamination Stack-Up

The lamination process is key to building a reliable ML-PWB. In the lamination process, the board is subjected to heat and pressure that melts the B stage (bonding sheets) and causes it to flow. This encapsulates the circuits and fills any buried vias. The B stage then cures, establishing a good mechanical bond to the inner detail layers. A variety of materials can be utilized in standard laminating press cycles. (Refer to Sec. 31.3.5 for a detailed discussion of the materials and prefill process.) A typical ML-PWB stack-up is shown in Fig. 31.30. For productivity reasons, multiple stack heights are repeated within each opening of the press. The various components and their placement within the book are shown.

A standard lamination uses tooling pins that go from caul plate to caul plate, passing through each board and all of the separator sheets. Since the CTE of stainless steel roughly matches the in-plane CTE of a multilayer board, a tight fit to the pin is possible. Aluminum has a much higher CTE, so if aluminum is used, a loose fit to the tooling pin is required. Some fabricators use as few as four tooling pins. Others may use 20 or more. In addition to easy stacking, the four-slotted pin system minimizes problems arising from material growth and shrinkage in an overdetermined tooling system. On the other hand, users of systems with a large number of pins believe that firmly anchoring the ML-PWB to stainless steel obtains better dimensional stability.

31.4.3 Lamination Breakdown

Once the ML-PWB is fully cured and then cooled to room temperature per the manufacturer’s guidelines, the book is taken apart; this process is called “breakdown.” This is usually a manual process which consists of de-pinning the book, then separating the individual ML-PWBs from each other at the separator sheets or C-A-C boundary as shown in Fig. 31.31. The panels are sent to an automatic thickness

checker to ensure compliance with requirements, then on to an edge-finishing machine. The edge finisher removes the rough cured prepreg from the edges (called “ooze out”) and any copper foil overhang by routing the four sides to reduce imaging defects. The machine will then bevel and polish the edges so that they are not sharp and there are no protruding glass fibers or copper slivers. The finishing process might also include a bore to remove surface epoxy from around the tooling holes or slots.

31.4.4 Lamination Process Methods

31.4.4.1 Standard Hydraulic Lamination. A standard hydraulic press generally has a top or bottom ram and several floating platens that create multiple press openings. Typical presses have four to eight openings. The output of the press is based on the stack height in each opening. Low-layer-count designs can yield as many as 96 panels per press cycle based on a stack height of 12 by 8 openings. High-layer-count and thick laminated boards have the stack height reduced to ensure uniform heat rate from the outside to innermost stack. Steam, hot oil, or electrical resistance heaters may heat hydraulic-style presses. The steam and hot oil presses have the advantage of a fast heating rate, but the temperature of the heating fluid limits their maximum temperature. For steam, this is generally below the lamination temperature needed for high-temperature materials. If a steam press must be used, polyimide, PPO, and cyanate esters can be oven-baked to complete their cure. However, the thermal plastic adhesive layers used with Teflon are not compatible with a steam press.

31.4.4.2 Vacuum-Assisted Hydraulic Lamination. Many hydraulic presses use a vacuum to eliminate volatiles. Users of vacuum presses report a

reduction of edge voiding and the ability to laminate at a lower pressure. Almost all hydraulic presses sold since 1990 are equipped with a vacuum chamber. In a typical process, the ML-PWB caul plate is loaded onto a carrier sheet, where a spring-loaded rail holds it off the press platen and limits the heat transfer to the ML-PWB stack. Next, the vacuum chamber is closed and a vacuum is drawn and held. A typical vacuum cycle may be from 15 to 60 min, depending on the nature of the materials being laminated. This gives the vacuum time to pull air, moisture, and other volatiles out of the ML-PWB stack. At the completion of this prevacuum process, the press is closed, compressing the spring-loaded rails and establishing good thermal contact with the press platens.

31.4.4.3 Autoclave. The autoclave is a popular tool in the composites industry and has found limited use by board fabricators. The autoclave is a sealed cylindrical chamber that subjects the ML-PWB stack to a high-pressure heated gas. The ML-PWB stack is sealed in a vacuum bag, and the hydrostatic pressure from the gas produces the force necessary for lamination. In principle, the autoclave is an excellent machine for producing a void-free lamination. Since the pressure is hydrostatic, it eliminates the problem of low pressure at the panel edge. This results in void-free panel borders and increases the usable area on a panel. In practice, an autoclave requires a long prevacuum cycle and has a slow heatup rate. It is also vulnerable to problems with vacuum bag failures. The result is that autoclaves have not found broad acceptance among rigid board manufacturers.

31.4.4.4 Direct Current or Continuous Foil Manufacturing. The continuous foil method of lamination is covered in Chapter/Section 9.7.4.

31.4.5 Critical Lamination Variables

Since hydraulic presses are by far the most common type of press, the following discussion focuses on that process. The quality of the ML-PWB lamination is affected by both the pressure ramp and the temperature ramp. There are almost as many unique cycles (also known as press recipes) as there are fabricators. However, in general the lamination cycle can be divided into four regions: B-stage melt; B-stage flow; B-stage cure; and cooldown. Figure 31.32 shows a typical lamination cycle with these critical variables identified.

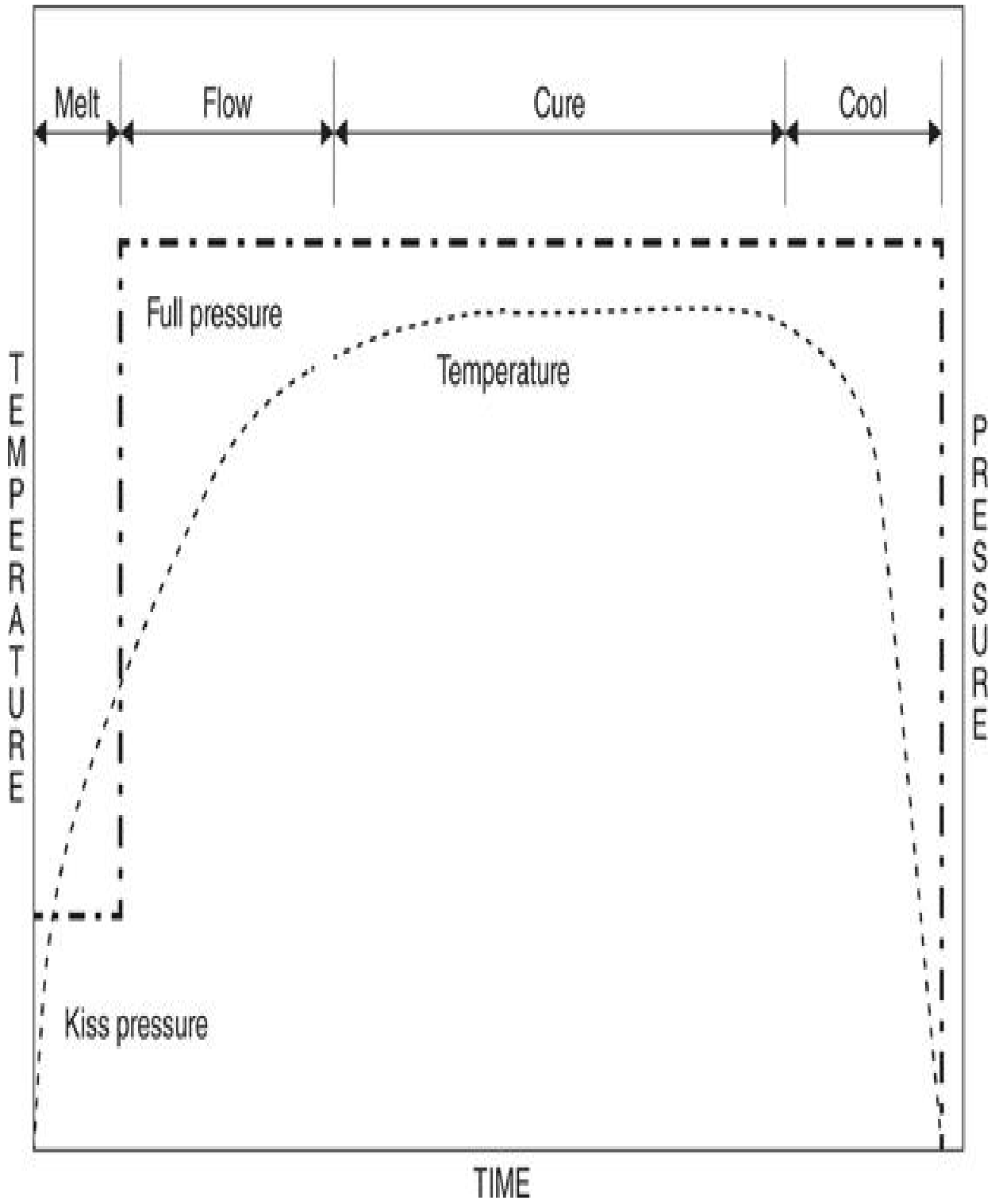

FIGURE 31.32 Typical temperature and pressure cycle for hydraulic lamination.

31.4.5.1 B-Stage Melt. During the melt cycle, the B stage is solid and the pressure should be low. Excessive

pressure during this portion of the cycle will damage the glass cloth and exaggerate problems with image print-through, also known as “telegraphing.” Most press cycles start with a low pressure known as a kiss pressure. The kiss pressure is high enough to ensure good thermal contact without damaging the ML-PWB. The length of the kiss cycle depends on the heating rates and the cure kinetics of the B stage. In a hot press cycle, the ML-PWB stack is loaded into a preheated press, and the heating rate may approach 20°C/min. In a hot press, the kiss cycle should be limited to a few minutes, or the B stage will begin to cure before flow is complete. At the opposite extreme, the press is loaded cold, and the heating rate is determined by the heating ramp of the press. For a slow heating rate of 5°C/min., a kiss cycle of 15 min. is appropriate. Consult the Technical Data Sheet for specific prepreg rise time flow characteristics.

Some LFAC laminates, however, have process guidelines where a best practice is to have a kiss cycle with 0 psi with a slow heat rise on the order of not more than 15°C/min until approximately a 90°C internal temperature. This step is held for 30 to 40 min to drive out moisture before pressure is applied and the flow stage initiates.

31.4.5.2 B-Stage Flow. The second portion of the cycle begins when the B stage liquefies, but before its viscosity begins to rise due to curing. In this region of the cycle, the liquid B-stage flows and encapsulates the circuitry. As long as the internal features are surrounded by liquid B stage, print-through is not an issue. The key to good results is to select a pressure that will allow reproducible resin flow but that does not squeeze out all available resin before the progressing cure stops the flow. Once again, the exact pressure depends on the temperature cycle, the B-stage viscosity characteristics, and the B-stage cure kinetics. For a fast-curing B stage and a fast temperature ramp, pressures as high as 600 psi may be needed to ensure complete circuit

encapsulation. On the other hand, with a slow ramp and a long B-stage working time, high pressures give excessive flow and best results are obtained at 200 psi. Improper melt staging can result in “footballing,” a term used to describe a panel whose center is significantly thicker than its outside. To determine proper melt, it is recommended to install a thermocouple in the center stack edge to chart the actual heat rise through the flow.

A typical dicy-cured FR-4 multifunctional epoxy has a flow range, called the critical range, at the temperatures between 70 and 130°C. HF and LFAC laminates have a critical range typically between 80 and 140°C. During the critical range, the heat rate input and pressure are critical variables. A typical dicy-cured FR-4 press recipe would be 4 to 8°C/min rise at 200 to 300 psi pressure. HF and LFAC laminates’ recipes are usually lower in the rate of rise and higher in pressure, such as 2 to 4°C /min and 225 to 360 psi pressure.

Table 31.3 shows some press recipes from the processing guidelines posted on the laminators’ webpages. This table is intended to illustrate that moving from standard FR-4 to other HF or LFAC laminates will require the development of new press recipes.

TABLE 31.3 Press Recipes for Selected Materials

	T_g °C, DSC	Rise, °C/min	Critical Range, °C	Pressure, psi	Cure Time, min/temp (°C)
Standard dicycured FR-4	175	4–7	70–130	200–300	60/182
Nondicy FR-4 laminate	155	2–4	80–140	275–360	90/193
HF laminate	160	2.3–5.6	>100	380	90/200
LFAC laminate A	185	4.4–7	70–130	200–300	75/185
LFAC laminate B	190	2.3–5.6	83–139	225–325	75/193
LFAC laminate C	210	2–4	80–140	275–360	90/193
LFAC laminate D	190	2–4.5	80–135	200–300	120/200
LFAC laminate E	215	2	80–135	300	120/200
Polyimide	250	2–4	80–138	225–275	200/218

31.4.5.3 B-Stage Cure. In the third part of the cycle, flow has stopped and the resin cure is proceeding. The temperature is held at its maximum value to minimize the time to obtain full cure. For a typical epoxy system, this usually is approximately 180°C for 60 min LFAC laminates, however, tend to require longer and hotter cure stages: up to 200°C internal temperature for 120 min, and longer for thicker boards. Some materials, such as polyimide, require a significantly higher cure temperature for even longer.

31.4.5.4 Cooldown. The last part of the cycle is the cooldown cycle. In Fig. 31.32, it is suggested that the pressure is released after some cooling has occurred, but before the stack reaches room temperature. In many modern systems, the ML-PWB stack is transferred hot to a low-pressure cooling press. It is important to control the cooling rate to minimize warpage. It is generally desirable to cool through T_g in a stress-free state without any significant

thermal gradients present. A properly designed cooling press will meet these conditions.

31.4.6 Critical B-Stage Variables

During a typical lamination cycle, the B stage undergoes several significant changes. At the beginning of the cycle, the B stage is a solid with a low cross-link density and a melt temperature near 90°C. As the temperature rises, the B stage melts and becomes a high-viscosity liquid. As the press heats further, the viscosity of the liquid drops. When the B stage begins to cure, viscosity reaches a minimum and begins to rise. The region around the viscosity minimum is called the region of maximum flow. The wider this region and the lower the minimum viscosity, the more flow occurs. Figure 31.33 shows a schematic viscosity curve for a typical cure cycle. In a high-flow B stage, the initial cure level is low. This results in a longer time at temperature before the B-stage viscosity rises due to cure. This is often described as a long gel time. In terms of Fig. 31.33, a high-flow B stage has a low minimum viscosity and a wide region of maximum flow. A low-flow B stage has a higher degree of initial cure and may include flow restrictors to increase the minimum viscosity. High-flow B stages are useful in presses with a high-heating rate where the resin may begin to cure before flow is complete. They give excessive flow if used in a press cycle with a very slow heating rate.

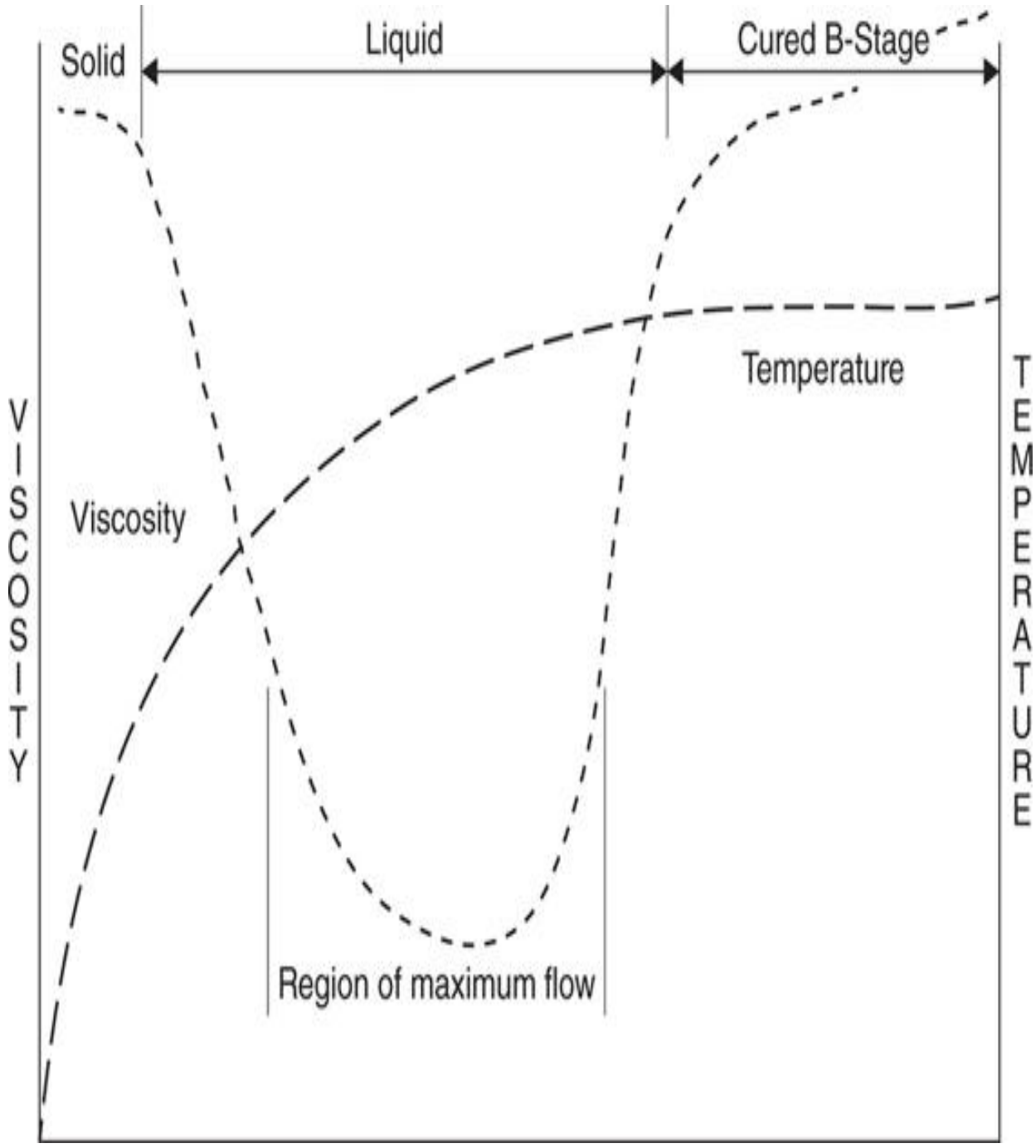

FIGURE 31.33 Typical viscosity curve for B stage during lamination.

31.4.7 Single-Ply versus Multiple-Ply B-Stage Fill Considerations

For dielectric separations that could be filled by either one “thick” ply of B stage—for instance, style 7628—or by two thinner plies of B stage—for instance, style 1080—the fabricator and engineer need to determine which approach is best on a product-by-product basis. Building ML-PCBs with single-ply B-stage fill is common for HDI and has the following advantages:

- Costs are reduced significantly when sheets of prepreg are eliminated—the main advantage.
- *Z*-axis expansion is easier to control since there is usually less resin with a thicker style.
- Overall thickness has less variation since there are fewer elements in the construction.
- Single-ply fill allows for overall thickness reduction when two plies of any style are replaced by one ply of the same style or thinner.

Building with two plies is usually either preferred or required with the following conditions:

- The separation to be filled is between two planes generating a large voltage bias and additional dielectric separation is required to minimize the potential of dielectric withstanding breakdown.
- The separation to be filled is between two layers having thicker (70 µm) copper foil. In this case, there is frequently insufficient resin in a single ply to encapsulate the features and prevent air bubbles in etched-out regions.

31.5 LAMINATION PROCESS CONTROL AND TROUBLESHOOTING

A good lamination cycle produces a flat ML-PWB that is free of moisture or voids and has a fully cured substrate. All layers must be well registered. The ML-PWB must be free of warp and the thickness must be within the specification. Any controlled impedance layers must have the correct pressed dielectric separations above and below the signal layer. Each of these requirements puts special demands on the lamination process. To assist in setting control measures, the following process indicators (see Table 31.4) should be monitored with a Statistical Process Control (SPC) method.

TABLE 31.4 Process Variables and Limits

Process Indicator	Specification Limit	Gauge Type or Method
Thickness control	Per engineering drawing or internal spec requirement	Over-arm micrometer
Heat rise °C/min through melt	Per resin system requirement	Chart recorder
Cure	T_g of resin system	TMA
Post cure	Dwell time/temp per resin system requirement	Chart recorder
Registration	Per engineering drawing or internal spec requirement	Appropriate coupons or x-ray inspection equipment
Dielectric separation	Per engineering drawing	Cross-section

31.5.1 Common Problems

31.5.1.1 Voids and Moisture. Substrate voids are a serious problem in many lamination processes. One source of these problems is moisture. B stage is very hygroscopic and must be stored in a low-humidity environment to

preclude serious void problems. C-stage components also have a tendency to absorb water, and many fabricators use a bake to dry layers prior to lamination. However, for a fast innerlayer line with a good dryer in the oxide line, an innerlayer bake may not be necessary. Voids generally cluster in the low-pressure regions near the edge of the panel. This effect is minimized by the use of vacuum lamination. Increasing the lamination pressure can also reduce voids. However, the use of high pressures with high-flow materials can result in excessive flow, which leads to other substrate flaws such as resin starvation.

31.5.1.2 Blisters and Delamination. Blisters and delamination are also caused by trapped volatiles that collect in the low-pressure regions associated with print-through. If a board has wide copper borders on every layer, blisters are often found in the lower-pressure circuit areas adjacent to the borders. The best solution to this problem is to avoid areas of heavy copper adjacent to low-density circuit areas by replacing solid borders with a dot or stripe pattern. Also, the glass style and resin content of the prepreg should be matched to the weight of copper thickness adjacent to the prepreg.

31.5.1.3 Under Cure. The requirement of full cure is relatively easy to obtain if proper cure time and temperature are used. One measure of the cure level is T_g. Periodic measurements of T_g are an excellent check for material and process consistency. Another way to check cure is to make two consecutive measurements of T_g: If the epoxy is only partially cured, it will continue to cure during the first measurement and a higher T_g will be detected on the second measurement. A shift in T_g of more than 5°C is an indication of under cure. This measurement is typically performed on a

TMA. Figure 31.34 shows an example of an epoxy TMA run; note that the second TMA run has a delta of 3°C.

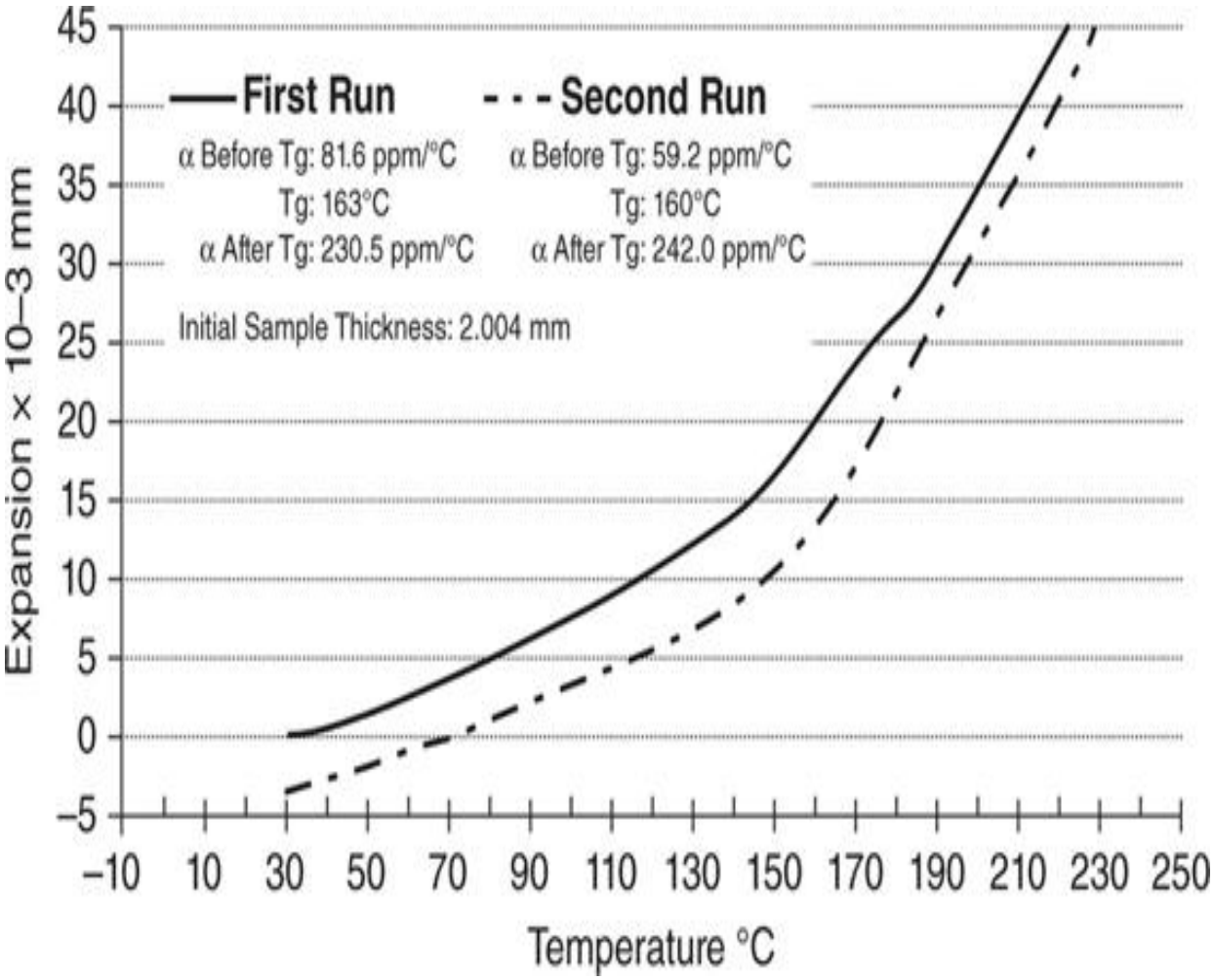

FIGURE 31.34 TMA analysis of epoxy with woven fiberglass. (*Courtesy of Microtek Labs, Anaheim, CA*.)

31.5.1.4 Post-Lamination Bake. Many fabricators bake the ML-PWB at 150°C for up to 4 h after lamination. One purpose of this baking is to ensure a complete cure. Although a bake will advance the cure, it is unnecessary if a proper lamination cycle is used (although polyimide is an exception; check the recommended processing guidelines). As discussed earlier, this can be verified by T_g

measurements. However, additional baking beyond full cure degrades the material and reduces T_g.

A second purpose of the bake is to reduce the warpage often seen in the outer boards of a stack-up. Although a post-lamination bake will flatten the boards, it is more of a repair than a root solution. If the panels are cured in the press in a way that ensures they go through T_g in an isothermal stress-free state, warpage should not occur. The warpage seen in the outer boards of a stack is generally a symptom of nonuniform cooling.

The third purpose of a bake is to relax internal stress and improve registration. Internal stresses are a symptom of an overdetermined tooling system. If such a system is used, a bake may improve registration. If the more popular four-pin system is used, a bake is unnecessary. Always confirm the need of a post cure with the recommendations of the material supplier.

31.5.2 Special Consideration for Nondicy, Nonbromine, and LFAC Laminates

For decades, the majority of PCBs have been built with epoxy resins, dicy-cured, and with bromine flame retardant. The industry has developed around this paradigm. Drills and drilling, chemistry, lamination, and circuit card assembly are all well understood with reference to standard FR-4. Although there are fabricators with processes developed to manufacture PCBs using laminates other than standard FR-4, this knowledgebase is not distributed industrywide. Especially problematic is the intersection of requirements for HF and/or LFAC with high thermal resistance and improved electrical characteristics, such as low attenuation in the material. Many laminators recognized that the heart of their

product line would need to be revamped from the entry-level cost-conscious material all the way through to the highest performance material. This was a large undertaking, requiring many different trials to find the right ingredients, in the right combinations, with the desired properties, especially the response to the new elevated reflow temperatures. As is frequently the case, there are trade-offs. For instance, reducing CTE by increasing filler is desirable to a point; the increase of filler increases the dielectric constant and loss tangent properties of the material, making it less suitable for high-speed digital products. The line-up from the bottom to the top of the performance ladder, with and without bromine, capable of withstanding high-temperature reflow, isn’t complete in all cases.

The major processes that need to be developed and optimized specifically for nonstandard FR-4 laminates are innerlayer adhesion promotion, lamination, drilling, and hole wall preparation. The fabricator must work closely with its laminate and chemistry providers to develop the specific process parameters that will work with their lamination equipment and chemistries.

Early problems have been delamination (both adhesive and cohesive failures), voiding, and hole wall pull-away. Some of these quality problems can be discovered prior to shipment by cross-section analyses, but some do not manifest until after high-temperature reflow. Since laminators test laminates rather than finished PCBs, and fabrication and design features both effect the final product, a cautious fabricator will test completed PCB parts for quality and reliability, simulating the intended assembly soldering profile. Accordingly, submitting an actual final ML-PWB to multiple cycles through a production reflow oven with a lead-free soldering profile can be advantageous. After reflow exposure, the parts are visually inspected for blisters, then cross sections are taken at both high and low hole density areas to look for internal delamination or laminate cracks,

voiding, and hole wall pull-away. Figures 31.35 through 31.38 show examples of these defects.

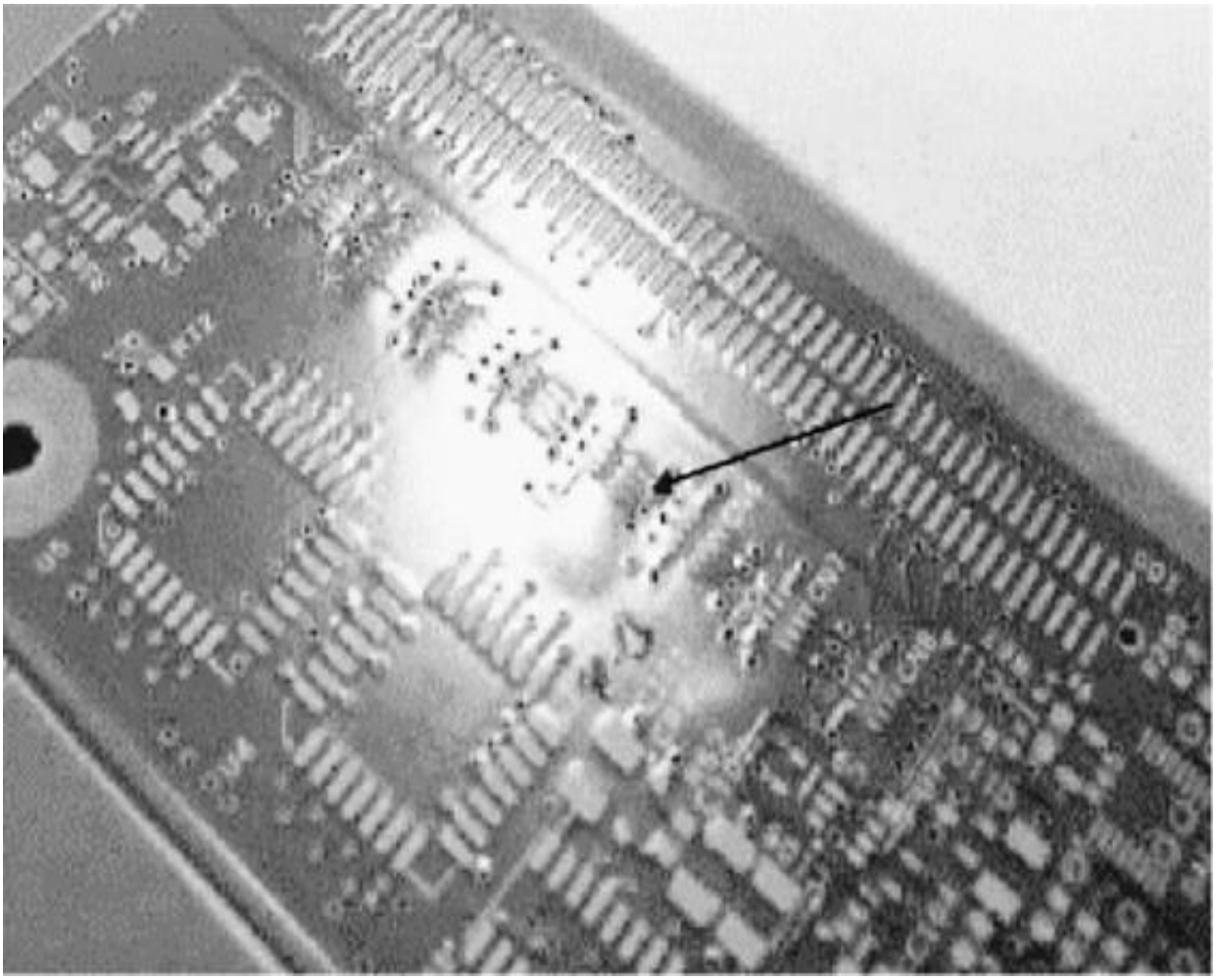

FIGURE 31.35 Blistering.

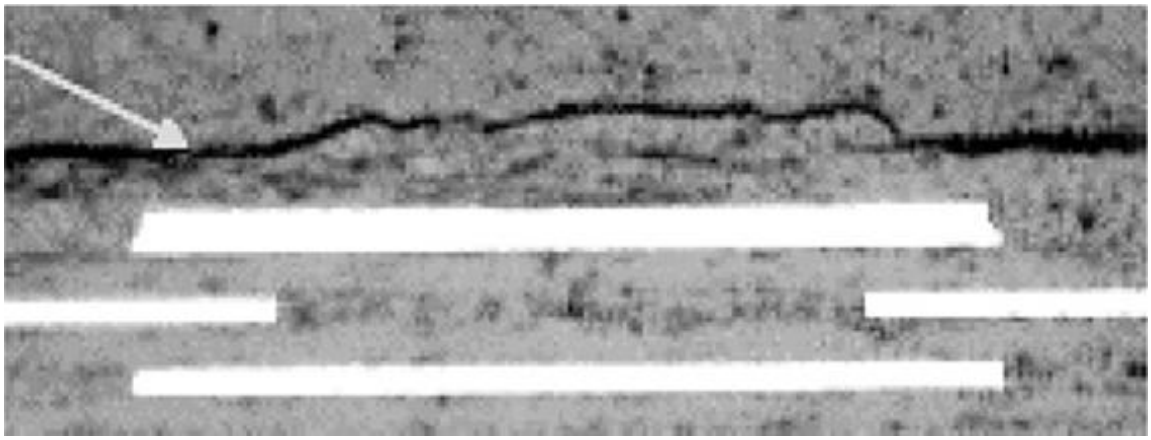

FIGURE 31.36 Laminate crack.

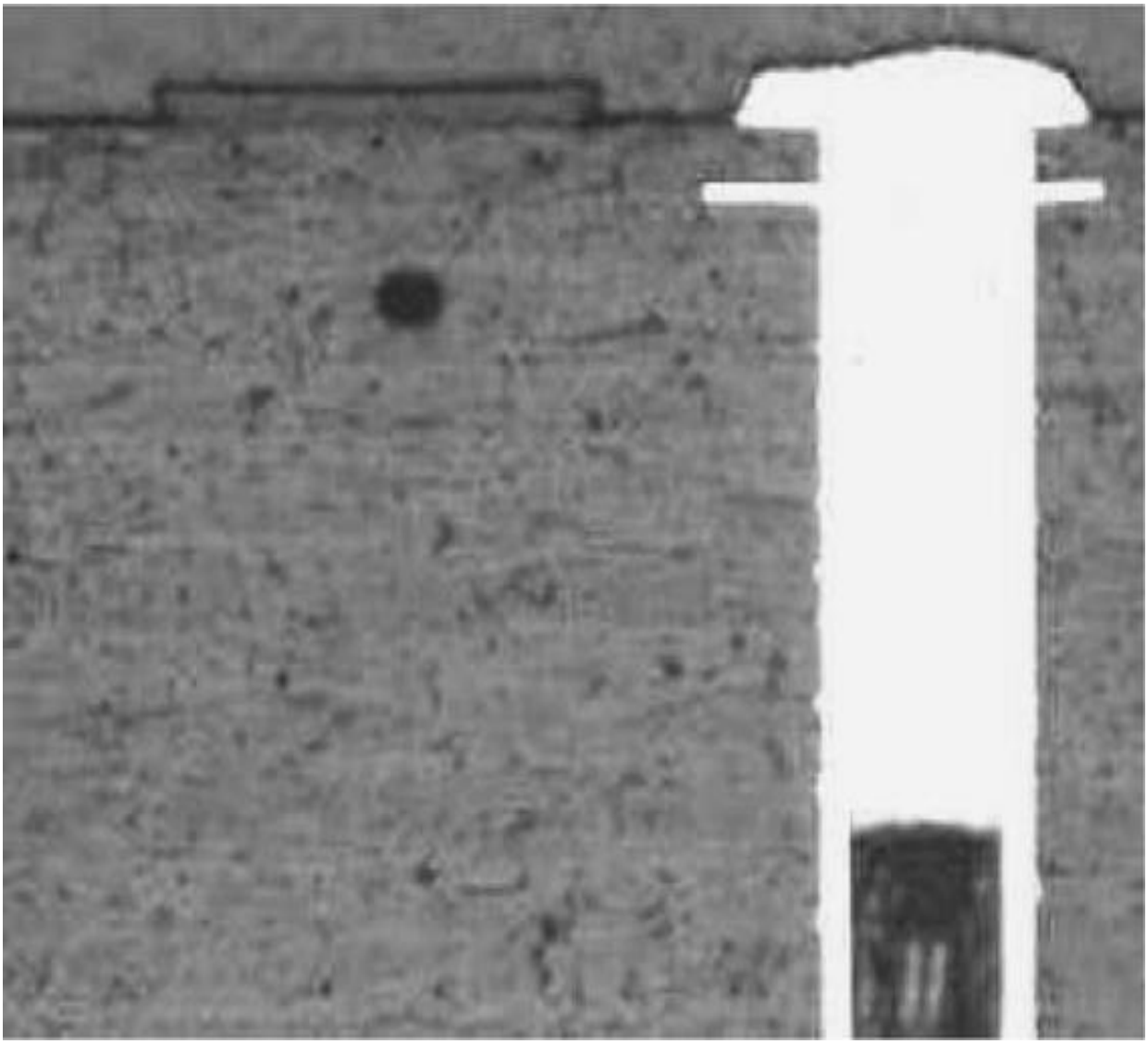

FIGURE 31.37 Void.

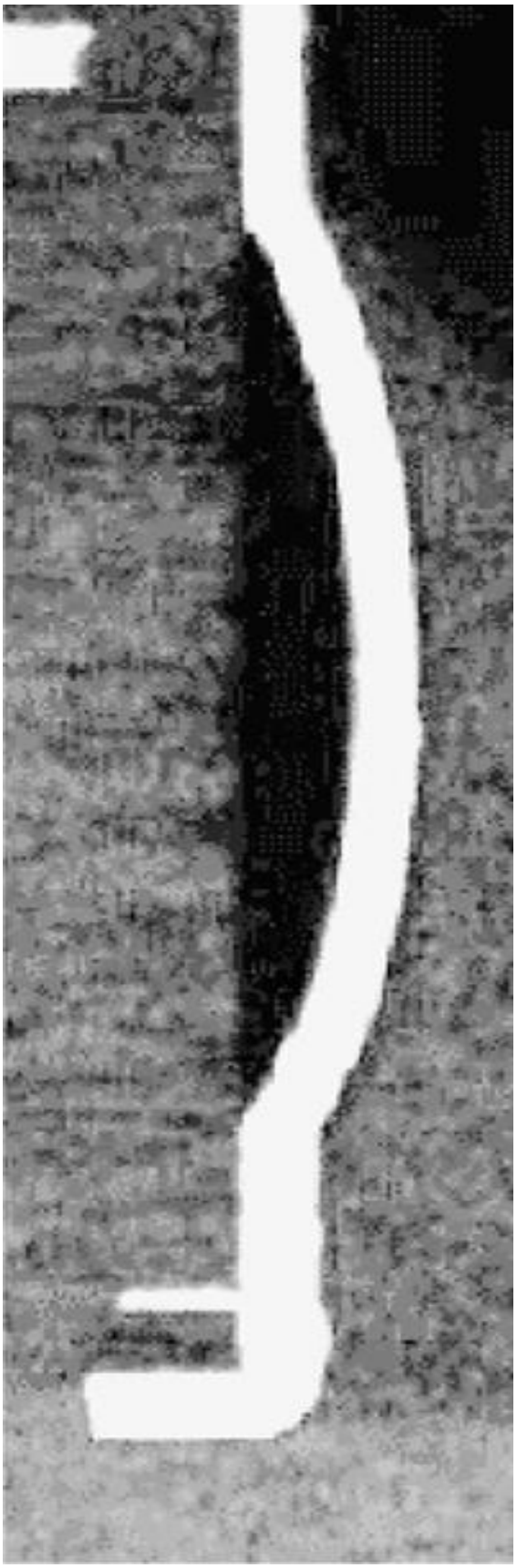

FIGURE 31.38 Hole wall pull-away.

31.6 LAMINATION OVERVIEW

The standard hydraulic vacuum press cycle is flexible and has very high output. Through the use of multiple openings and stacked lamination, high productivity is obtainable. Hydraulic lamination works effectively with all modern materials systems.

ML-PWB fabricators use many different laminate systems, press cycles, and B-stage formulations. The most significant differences among press cycles are in the heating rate, cure temperature, and cure time. At one extreme, the ML-PWBs are loaded into a cold press. This gives a very slow heating rate, and a B stage with a low flow is needed to avoid excessive flow. This material works well at low pressures, minimizing print-through and innerlayer distortion. A vacuum cycle is recommended to minimize voiding in low-pressure regions near the panel edge. The other extreme is a hot-loaded press with a very fast temperature rise. This cycle needs a high-flow material a high pressure to complete the resin flow cycle before the onset of cure. Although a vacuum is less important with this cycle, it will minimize edge voids. Some materials require a moisture drive-off prior to heat using a 0 psi low temperature hold.

Some fabricators use bakes both before and after lamination. The bake before lamination is designed to ensure moisture removal from cores after the application of the adhesion promotion chemistry; follow the recommendations of the laminate manufacturer carefully. The bake is also needed if innerlayers are stored at high humidity prior to lamination, or as a standard process for hygroscopic materials such as some of the LFAC laminates or polyimide. Other fabricators use a bake after lamination to complete the

cure, reduce warp, and relieve stress. Although a post bake will achieve these goals, it is usually unnecessary in a controlled lamination process. In the case of high-temperature materials such as polyimide, cyanate ester, and PPO, a post bake is a useful way to achieve a full cure in a process where the maximum press temperature is limited.

31.7 ML-PWB SUMMARY

The printed wiring board manufacturing industry continues to be challenged with a high rate of change. Today's global market and added environmental considerations are driving investments and innovation in research and development of integrated components (e.g., laminates), subcomponents (e.g., resins and glass), and process consumables (e.g., oxide chemistry) for PCB fabrication. The manufacturing flow has only a backbone of standard methodologies, with many optional branches and staging through some process sequences multiple times (as in sequential lamination and HDI technologies). PCB fabrication has become much more complex, interactions between processes and components are compounded, and the user requirements are more formidable. A successful implementation of any of the high-density constructs or high-temperature-resistant materials should always be complemented with sound statistical process verification and testing appropriate to the end use.

31.8 ACKNOWLEDGMENT

Parts of this chapter were written by Valerie A. St. Cyr of Teradyne, Inc., Semiconductor Test Division, North Reading, Massachusetts, for Clyde F. Coombs, Jr. (ed.), *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

31.9 FURTHER READING

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CHAPTER 32

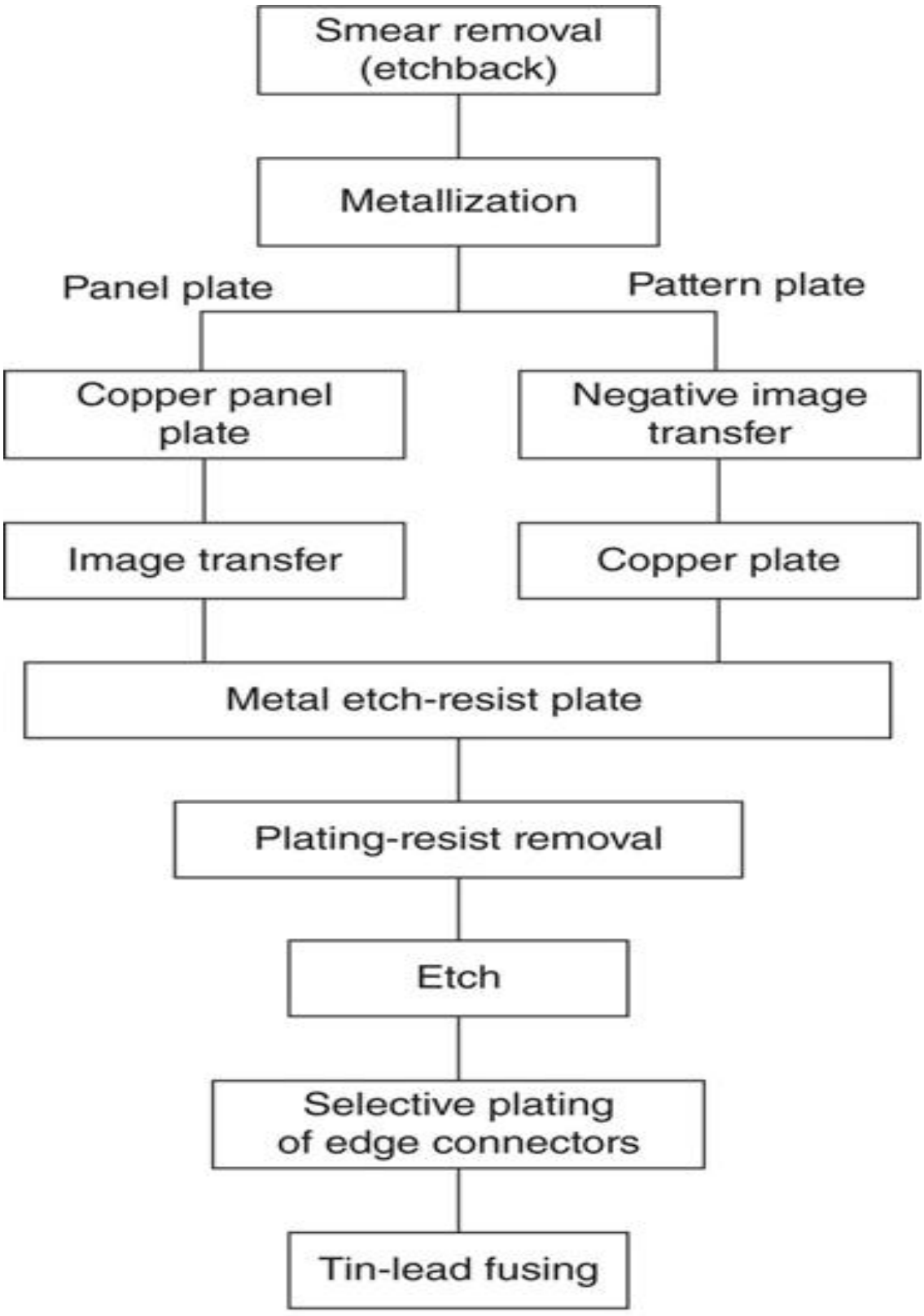
PREPARING BOARDS FOR PLATING

Michael Carano

Technologist and Chemical Consultant, Maple Plain, Minnesota

32.1 INTRODUCTION

A major part of manufacturing printed circuit boards (PCBs) involves *wet process* chemistry. The plating aspects of wet chemistry include deposition of metals by electroless (metallization) and electrolytic (electroplating) processes. Topics to be described here are multilayer processing, electroless copper, direct metallization, electroplating of copper and resist metals, nickel and gold for edge connector (tips), tin-lead fusing, and alternative coatings. Specific operating conditions, process controls, and problems in each area will be reviewed in detail. The effects of plating on image transfer, strip, and etching are also described in this chapter. See the printed circuit plating flowchart in Fig. 32.1.



Direct metallization technology (DMT)

FIGURE 32.1 Printed wiring board plating flowchart.

Two driving forces have had major influence on plating practices: the precise technical requirements of electronic products and the demands of environmental and safety compliance.

Recent technical achievements in plating are evident in the capability to produce complex, high-resolution multilayer boards. These boards show narrow lines (3 to 6 mils), small holes (12 mils), surface-mount density, and high reliability. In plating, such precision has been made possible by the use of improved automatic, computer-controlled plating machines, instrumental techniques for analysis of organic and metallic additives, and the availability of controllable chemical processes. Military-specification-quality boards are produced when the procedures given here are closely followed.

32.2 PROCESS DECISIONS

Process and equipment needs dictate the physical aspect of the facility and the character of the process, and vice versa. Some important items to consider are the following.

32.2.1 Facility Considerations

1. *Multilayer and two-sided product mix:* Lamination presses and innerlayer processes are required.
2. *Circuit complexity:* Dry film, photoimageable resist, and a clean room are needed.
3. *Level of reliability (application of product):* Extra controls and testing are required.
4. *Volume output:* Equipment sizing and building space are needed.

5. *Use of automatic versus manual line:* Productivity, consistency, and a workforce are required.
6. *Wastewater treatment system:* Water and process control capability must be available.[1]
7. *Environmental and personnel safety; compliance with laws*.
8. *Costs*.

32.2.2 Process Considerations

1. *Material:* The principal printed board material discussed will be NEMA grade FR-4 or G-10, that is, epoxy fiberglass clad with 1.2-, 1-, or 2-oz copper. Other materials will be briefly mentioned because they can significantly alter plating and related processes.
2. *Standard:* Plated through hole (PTH) is the current standard of the industry. The following purposes, objectives, and requirements apply to both multilayer and two-sided boards:
   a. *Purposes:* Circuit density; double-sided circuitry
   b. *Objectives:* Side-to-side electrical connection; ease of component attachment; high reliability
   c. *Requirements:* Complete coverage; even thickness; a hole-to-surface ratio of 0.001 in minimum; no cracks; no voids, nodules, or inclusions; no pull-away; no epoxy smear; minor resin recession; optimum metallurgical structure; M/L compatibility
3. *Image transfer:* Photoimageable, dry film, or screening of plating resists will depend on board complexity, volume, and labor skills.
4. *Electroless copper:* The type chosen will depend on the method of image transfer as well as on the need for panel plating. These processes are readily automated. The largest percentage (estimates are as high as 95 percent)

of PCB manufacturers worldwide rely on the electroless copper method for hole metallization.

5. *Direct metallization technology (DMT):* Some of the remaining PCB manufacturers have eliminated the electroless copper step and converted to DMT.

Developed in the 1980s, DMT methods produce a conductive surface on the nonconductive through-hole surfaces (see Chap. 30 for a detailed discussion). Electroless copper baths contain formaldehyde and chelators. In addition, the baths use large volumes of water, are difficult to control, and make it difficult to treat waste. DMT claims include increased productivity, ease of control, and lower hazardous material involvement. Because of these characteristics, DMT will probably gain significant acceptance as a primary hole metallization method.[2] Acceptance of the DMT process has been delayed by the high cost of conveyorized equipment and chemicals.

DMT primary technologies include:

- Palladium
- Carbon-graphite
- Conductive polymer
- Other methods (see Chap. 30 for further information)
- *Electroplating processes:* Deposit requirements are as follows:
  - Electrical conductivity
  - Mechanical strength
  - Ductility and elongation
  - Solderability
  - Tarnish and corrosion resistance
  - Etchant resistance
  - Compliance with military specification (mil-spec)

Details emphasizing operation, control, and mil-spec plating practices are given elsewhere. Metal-plated structures of completed PC boards are as follows:

- Copper/tin-lead alloy
- Copper/tin (SMOBC)
- Copper/tin-nickel (nickel)/tin-lead
- Copper/nickel/tin-nickel/silver

- *Strip, etching, and tin-lead fusing:* Methods required by these steps are determined by the preceding processes and by the need for automation.

32.3 PROCESS FEEDWATER

32.3.1 Water Supply

PCB fabrication and electronic processes require process feedwater with low levels of impurities. Large volumes of raw water must be readily available, either of suitable quality or treatable at reasonable cost. New facilities must consider water at an early stage of the site selection and planning process. Zero discharge, although a desirable goal, is very costly and difficult to achieve.

32.3.2 Water Quality

Highly variable mineral content causes board rejects and equipment downtime, as well as reduced bath life, burdened waste treatment, and difficult rinse water recovery. Many water supplies contain high levels of dissolved ionic minerals and possible colloidals that can cause rejects in board production. Some of these impurities are calcium, silica, magnesium, iron, and chloride. Typical problems caused by these impurities are copper oxidation, residues in the PTH,

copper-copper peelers, staining, roughness, and ionic contamination. Problems in the equipment include water- and spray-line clogging, corrosion, and breakdown. The best plating practices suggest good-quality water for high yields. The need for water low in total dissolved solids (TDS), calcium hardness, and conductivity is well known. Good water eliminates the concern that the water supply may be responsible for rejects. Although water quality is not well defined for plating and PC board manufacturing, for general usage, some guidelines can be assigned as follows. Where high-purity water is required, see Sec. 32.3.3. Typical quantities are

TDS:	4 to 20 ppm
Conductivity:	8 to 30 μS/cm
Specific resistance:	0.12 to 0.03 M
Carbonate hardness ($CaCO_3$):	3 to 15 ppm

Somewhat higher values are acceptable for less-critical processes and rinses.

32.3.3 Water Purification

Two processes widely used for water purification are reverse osmosis and ion exchange. In the reverse osmosis technique, raw water under pressure (1.4 to 4.2 MPa or 200 to 600 lb/in^2) is forced through a semipermeable membrane. The membrane has a controlled porosity that allows rejection of dissolved salts, organic matter, and particulate matter, while allowing the passage of water through the membrane. When pure water and a saline solution are on opposite sides of a semipermeable membrane, pure water diffuses through the membrane and dilutes the saline water on the other side

(osmosis). The effective driving force of the saline solution is called its *osmotic pressure*. In contrast, if pressure is exerted on the saline solution, the osmosis process can be reversed. This is called the *reverse osmosis* (RO) process, and involves applying pressure to the saline solution in excess of its osmotic pressure. Fresh water permeates the membrane and collects on the opposite side, where it is drawn off as product.

Reverse osmosis removes 90 to 98 percent of dissolved minerals and 100 percent of organics with molecular weights over 200, as shown in Table 32.1.

TABLE 32.1 Purified Water Supply Values
Typical in/out RO values

TDS, ppm	SiO_2, ppm	Conductivity, µS	Hardness-$CaCO_3$, ppm
170/4	30/1	130/8	24/1
240/7	45/2	200/14	35/2
300/10	60/2	250/20	45/3

A small quantity of dissolved substances also facilitates deionized (DI) water production, wastewater treatment, and process rinse water recovery, since it makes recycling less costly and more feasible. An RO system will result in lower costs for DI water preparation and for process water recycling. The setup for recycling requires additional equipment for polymer addition, filtration, and activated carbon treatment.

DI water purification is used when high-purity water is required, for example, in bath makeups, rinses before plating steps, and final rinses necessary to maintain low ionic residues on board surfaces. Mil-spec PC boards must pass

the MIL-P-28809 test for ionic cleanliness. This is done by final rinsing in DI water. Deionized water is made by the ion exchange technique. This involves passing water containing dissolved ionics through a bed of solid organic resins. These convert the ionic water contents to H^+ and OH^-. Deionized water systems are more practical when using feedwater low in ionic and organic content. Other requirements are as follows:

- pH: 6.5–8.0
- Total organic carbon: 2.0 ppm
- Turbidity: 1.0 NTU
- Chloride: 2.0 ppm

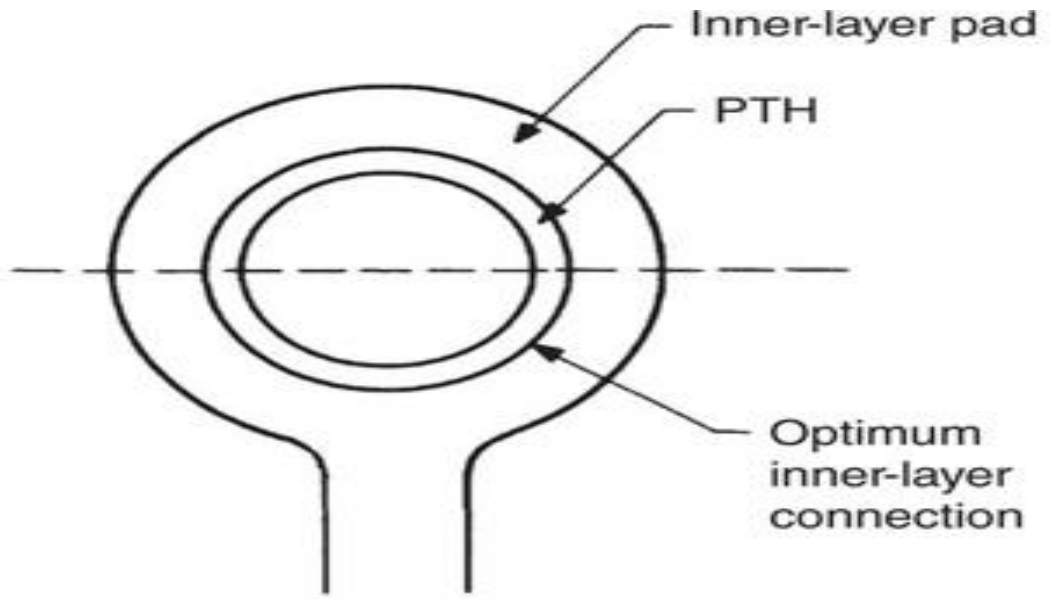
32.4 MULTILAYER PTH PREPROCESSING

Two-sided PCBs are usually processed by first drilling and deburring, then metallizing the through hole. Multilayers require treatment prior to any metallization process. Resin smear must be removed from the innerlayers, and texturing of the epoxy surface enhances hole wall adhesion. The preprocessing can be categorized as either smear removal or etchback.

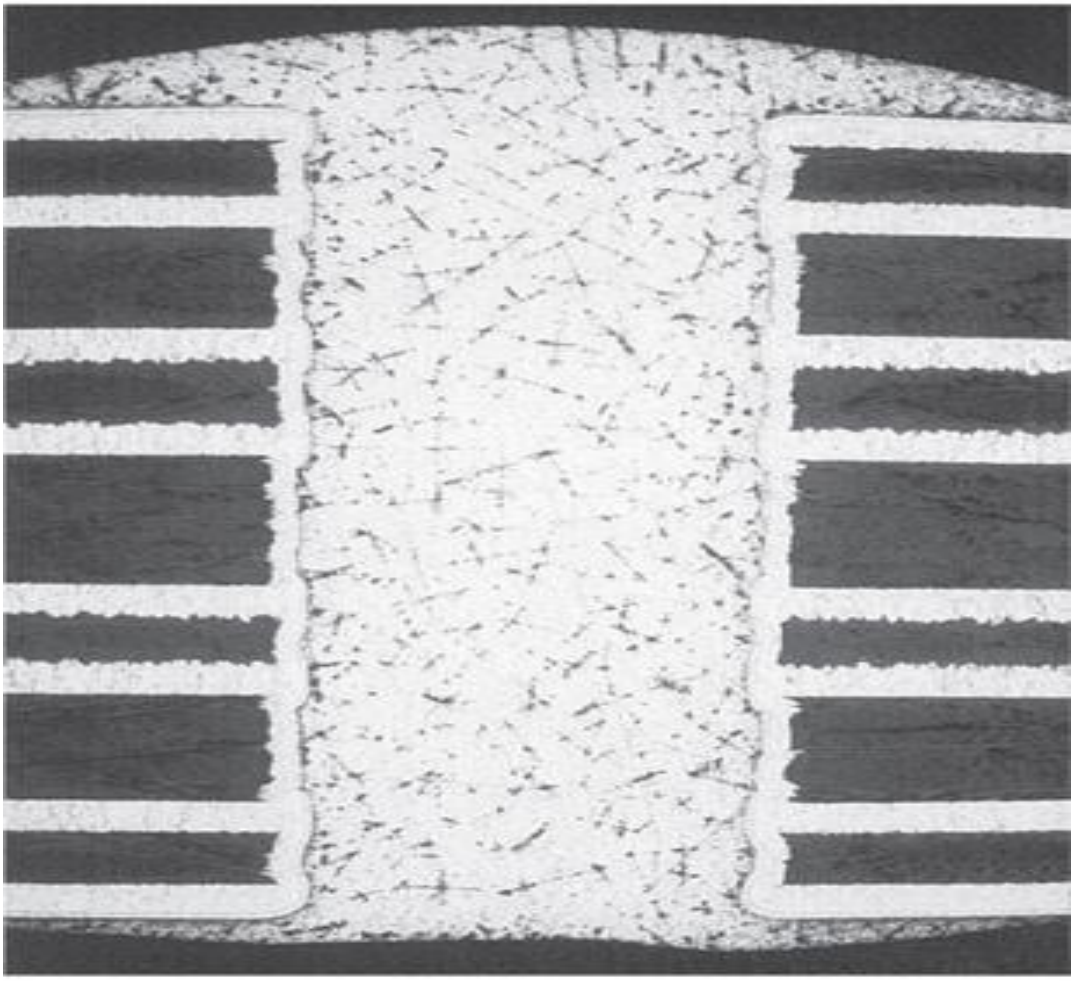
Fresh solution replenishment is crucial for effectively attacking smear and achieving uniformity through the holes. Circulation pumps and 90°C work piece movement are required to prevent temperature stratification of the heated baths as well as assist in forcing fresh chemistry through the holes. Higher aspect-ratio holes may require vibration to dislodge air bubbles from the holes and enhance uniformity of attack (see Chap. 29).

32.4.1 Smear Removal

High-speed drilling machines are used to drill holes into the PWB dielectric. During the drilling operation, sufficient heat is generated, causing the epoxy to melt. As the drill is withdrawn, the melted epoxy smears across and coats the innerlayer copper surfaces, causing a condition commonly known as *drill smear* (see Figs. 32.2 to 32.6).



(a)



(b)

FIGURE 32.2 PTH vertical and horizontal cross-sections illustrating optimum innerlayer connection and smear removal.

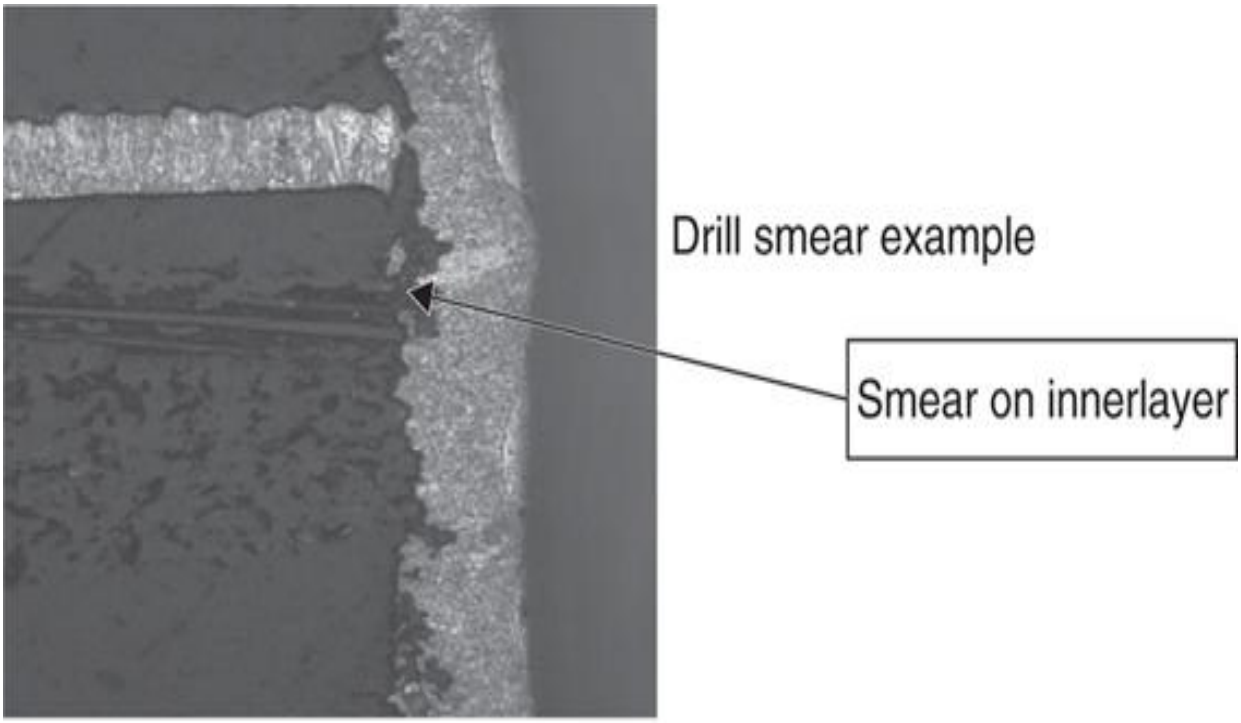


FIGURE 32.3 Drill smear example (note smear on the innerlayer).

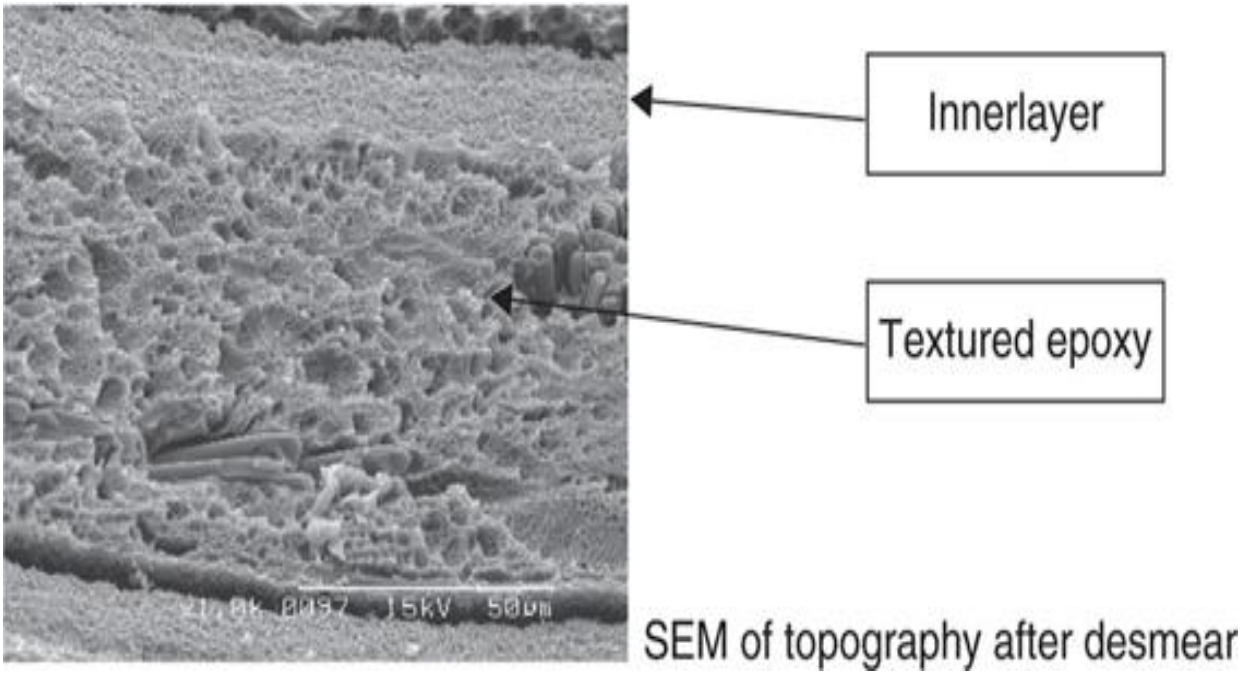


FIGURE 32.4 Scanning electron microscope (SEM) view of topography after desmear.

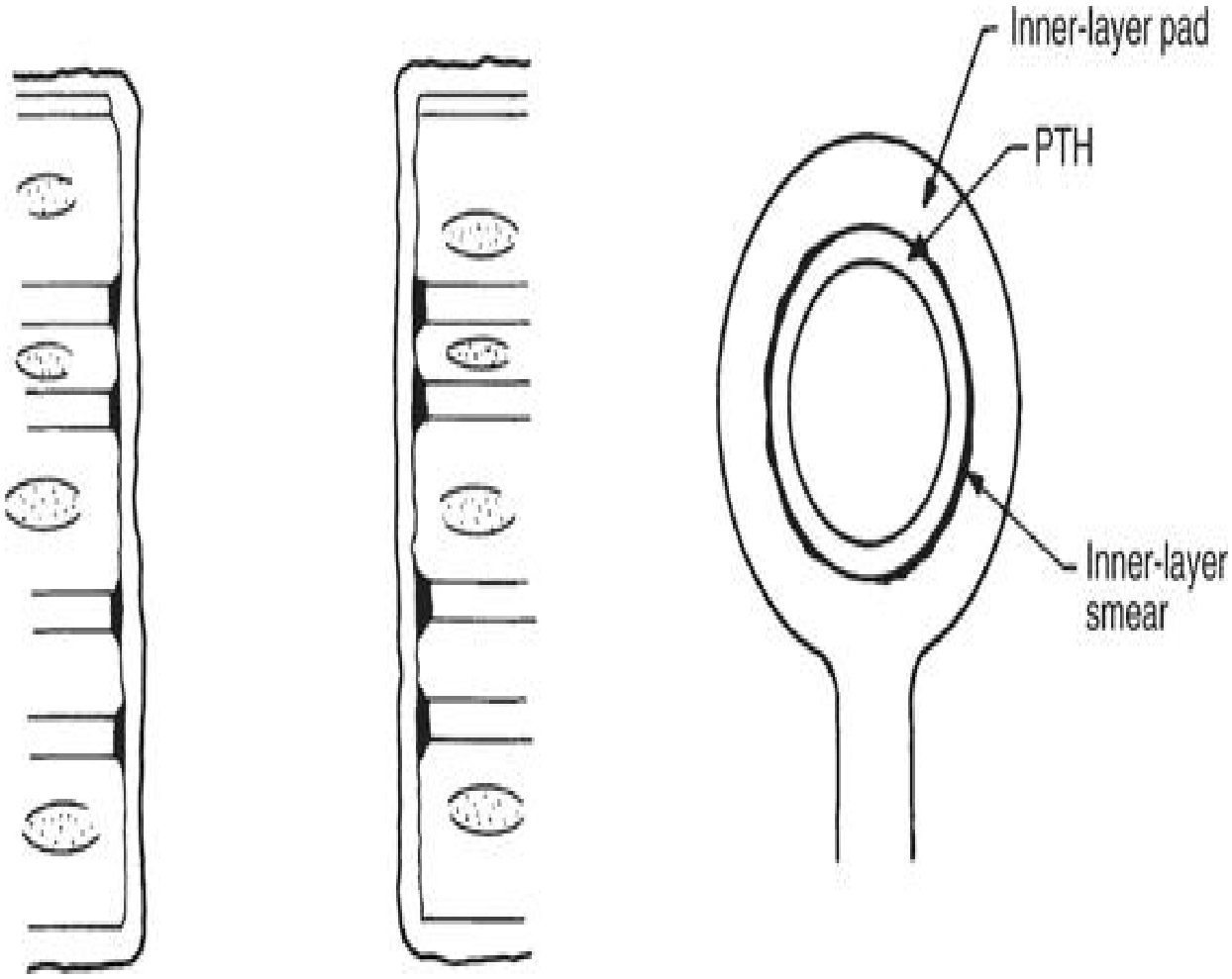


FIGURE 32.5 PTH vertical and horizontal cross-sections illustrating innerlayer smear.

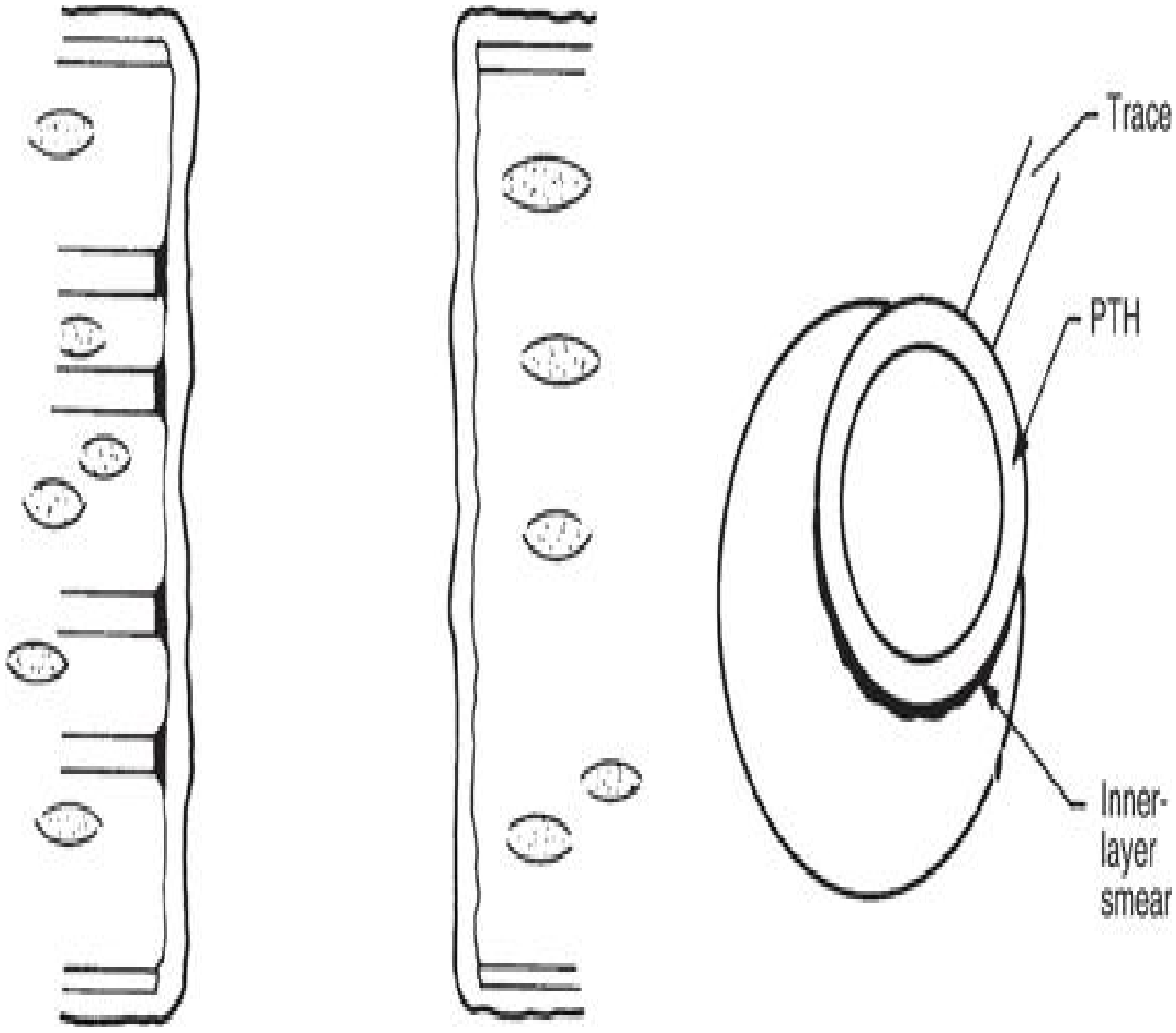


FIGURE 32.6 PTH vertical and horizontal cross-sections illustrating innerlayer smear and misregistration.

32.4.2 Etchback

Etchback refers to the aggressive removal of the epoxy and glass that results in the protrusion of the innerlayer copper. When two surfaces of the innerlayer are exposed, it is referred as two-point connection, and when three surfaces of the innerlayer are exposed, it is referred as three-point connection. Physically, the innerlayer copper will protrude from the drilled-hole three-point connection for copper

bonding, which is required on some mil-spec boards (see Fig. 32.7).

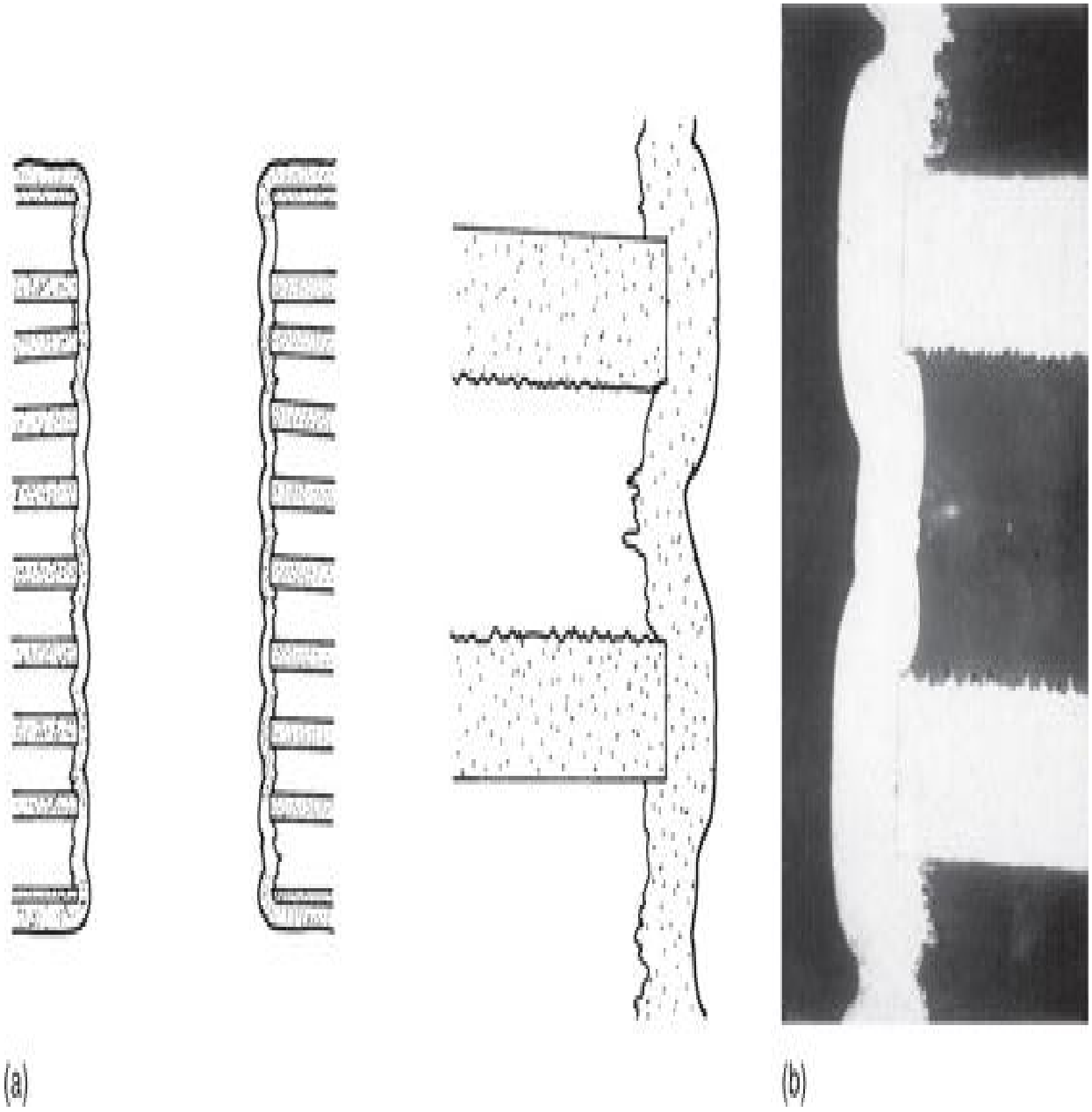


FIGURE 32.7 PTH vertical cross-section illustrating optimum connection and etchback: (*a*) shows a drawing of expected cross section; (*b*) shows an actual cross section with expected results.

32.4.3 Smear Removal/Etchback Methods

The four methods commonly used utilize hole wall epoxy or dielectric oxidation, neutralization-reduction, and glass etching. Three of the four common methods employ technology that oxidizes resin or dielectric, followed by a neutralization-reduction step. The fourth method—sulfuric acid—solvates or dissolves resin or dielectric. All methods remove smear, but the resultant surface of the epoxy affects hole wall pull-away and adhesion.

32.4.3.1 Sulfuric Acid. This process has been used extensively for many years because of its ease of operation and reliability of results. Disadvantages are lack of control, inability to attack certain resin systems, and the inability to create significant topography resulting in poor hole wall adhesion. Operator safety is crucial since concentrated sulfuric must be used. However, due to the significant changes and improvements in resin systems these last several years, sulfuric acid as a desmear method has fallen out of favor.

32.4.3.2 Chromic Acid. Chromic acid is a more controllable method that imparts some topography for enhanced hole wall adhesion and has a longer bath life. However, insufficient neutralization of the Cr^{+6} leads to copper voids. The line cost of using chromic acid is appealing. However, the Restriction of Hazardous Substances (RoHS) and waste treatment regulations of chromic acid add substantial costs that make this method a nonviable option. Etchback is possible by double processing.

32.4.3.3 Permanganate. Permanganate is the most widely used and preferred method in the industry. This easy-to-control process incorporates electrolytic regeneration,

which adds to consistency and increases bath lives. Permanganate effectively removes drill smear from most materials and imparts some texturing to the resin that increases hole wall adhesion.[3] See Fig. 32.3 for an example of hole wall topography after etchback. Problems result from lack of chemical control or inconsistent cure of the multilayer package.

Permanganate is also used as a second step in conjunction with the other methods to enhance hole quality.[4]

32.4.3.4 Plasma. Plasma utilizes electrical current to generate a plasma from fluorocarbon gases. This plasma oxidizes the epoxy resin and removes drill smear. Longer cycles or double cycling will generate etchback. Plasma works on any material and is especially effective when processing polytetrafluoroethylene (PTFE)-based dielectrics. This process has few steps and does not require the use of large quantities of chemicals. Disadvantages of plasma are nonuniformity of the treatment across the batch and across the panel. The texture generated on the epoxy is minimal, and an ash is commonly left behind that leads to poorer hole wall adhesion. A secondary cleanup, such as permanganate, is commonly used after plasma to remove the ash. The cost of the equipment and its maintenance is high. Controls must be provided to prevent air pollution.

32.4.4 Process Outline: Smear Removal and Etchback

The four common methods for smear removal and etchback are given in Table 32.2. Combinations of these methods are also in use because of added reliability they offer to both process and product.

TABLE 32.2 Smear Removal and Etchback Processes*

Sulfuric Acid	Chromic Acid
Rack panels	Rack panels
Sulfuric acid, 96%	Chromic acid 20-s dwell, 15-s drain, 3 min, 140°F room temperature
Neutralizer 8 min, 125°F	Reducer 3 min, room temperature
Ammonium bifluoride 3 min, room temperature	Ammonium bifluoride 3 min, room temperature
Unrack panels	Unrack panels
High-pressure hole cleaning	High-pressure hole cleaning
Release to electroless copper/DM	Release to electroless copper/DM
Permanganate	**Plasma Etch**
Solvent conditioner 90°F, 5 min	Plasma Oxyget, CF_4, 30 min
Alkaline permanganate 170°F, 10 min	Glass etch (optional)
Neutralizer-120°F, 5 min	High-pressure hole cleaning
Glass etch, 4 min, room temperature	Release to electroless copper/DM
High-pressure hole cleaning (optional)	
Release to electroless copper/DM	

*Water rinses after each step are not shown.

Polyimide and polyimide-acrylic systems are processed in chromic acid or plasma. Teflon, and R T Duroid materials are treated (before operations) in sodium-naphthalene mixtures to yield void-free, high-bond-strength copper in the PTH. The introduction of lead-free material and halogen-free material has challenged the desmear processes. The new materials

are more chemically resistant, and thus more aggressive desmear cycles are required to remove any smear. These more chemically resistant resin systems are more difficult to texture. Alternative solvents, higher temperatures, and cycle optimization may be required to process these newer materials effectively.

32.5 ELECTROLESS COPPER[5–10]

32.5.1 Purpose

This second series of chemical steps (after smear removal) is used to make panel side-to-side and innerlayer connections by metallizing with copper. The process steps required include racking, cleaning, copper microetching, and hole and surface catalyzing with palladium and electroless copper. Typical steps are as follows:

1. *Cleaner-conditioner:* Alkaline cleaning is used to remove soils and condition holes.
2. *Microetch:* This slow acid etching is used for removal of copper surface pretreatments, oxidation, and presentation of uniformly active copper. Persulfates and sulfuric acid hydrogen peroxide solutions are commonly used.
3. *Sulfuric acid:* This acid removes persulfate residues.
4. *Predip:* This process maintains the balance of the next step.
5. *Catalyst (activator):* Neutral or acid solutions of palladium and tin are used to deposit a thin layer of the catalytic metal on the nonconductive surfaces. Some palladium is unintentionally absorbed onto the foil surface and innerlayers.
6. *Accelerator (postactivator):* This process removes colloidal tin on board surfaces and holes or change the

charge of the palladium tin colloid.

7. *Electroless copper:* This alkaline-chelated copper-reducing solution deposits thin copper in the holes (20 to 100 µin) and surfaces.
8. *Antitarnish:* This neutral solution prevents oxidation of active copper surfaces by forming a copper conversion coating.

32.5.2 Mechanism

Equations (32.1) and (32.2) illustrate the process.

$$Pd^{+2} + Sn^{+2} \rightarrow Pd + Sn^{+4} \qquad (32.1)$$

$$CuSO_4 + 2HCHO + 4NaOH \xrightarrow{Pd} Cu + 2HCO_2Na + H_2 + 2H_2O + Na_2SO_4 \qquad (32.2)$$

However, Eq. (32.2) is an old two-step catalyzation sequence that is no longer in use in the industry.

32.5.3 Electroless Copper Processes

New materials and increased reliability criteria have precipitated a newer generation of electroless copper baths. Lead-free assembly forces the PWB to undergo higher thermal excursions, thus increasing the stress on the plated through holes. Proprietary additives (which are not listed in Table 32.3) affect the integrity of the electroless copper-plated deposit. Selection from the several types available depends on the type of image transfer desired. Operation and control of three bath types and the function of constituents are given in Tables 32.3 and 32.4. The problems encountered with this system are as follows:

TABLE 32.3 Electroless Copper Processes
Operation and control

	Low Deposition	Medium Deposition	Heavy Deposition
Copper	3 g/L	2.8 g/L	2.0 g/L
HCHO	6–9 g/L	3.5 g/L	3.3 g/L
NaOH	6–9 g/L	10–11 g/L	8 g/L
Temperature	65–85°F	115 ± 5°F	115 ± 5°F
Air agitation	Mild	Mild/moderate	Moderate
Filtration	Periodic	Continuous	Continuous
Tank design	Static	Overflow, separate sump	Overflow, separate sump
Heater	Teflon	Teflon	Teflon
Panel loading	0.25–1.5 ft^2/gal	0.1–2.0 ft^2/gal	0.1–2.0 ft^2/gal
Replenish mode	Manual	Manual or continuous	Automatic
Idle time, control	70–85%	Turn off heat	Turn off heat
Deposition time	20 min	20 min	20–30 min
Thickness	20 µin	40–60 µin	60–100 µin

TABLE 32.4 Electroless Copper
Function of constituents

Constituent		Function
Copper salt	$CuSO_4 \cdot 5\,H_2O$	Supplies copper
Reducing agent	HCHO	$Cu^{+2} + 2e \rightarrow Cu^0$
Complexer	EDTA, tartrates, Rochelle salts	Holds Cu^{+2} in solution at high pH; controls rate
pH controller	NaOH	Controls pH (rate) 11.5–12.5 optimum for HCHO reduction
Additives	NaCN, metals, S, N, CN organics	Stabilize, brighten, speed rate, strengthen

1. *Uncoppered holes or voids:* Voided holes appear as black or dark color in the holes. Corrective actions: Ensure that the process is functioning correctly by verifying the times, temperatures and concentrations of all preceding process tanks, including the desmear process as specified. The electroless copper bath components should be verified as well as the dwell time. Low loading factor, low temperature, or high air agitation lead to low bath activity and poor plating characteristics. Voids may also be caused by an overaggressive electrolytic preclean line.
2. *Hole wall pull-away:* This is the separation of the copper pulling away from the dielectric. The defect is usually detected during the cross-sectioning inspection. If the hole wall pull-away is severe, large blisters can be seen in the hole with the naked eye. Hole wall pull-away can be caused by insufficient texturing of the epoxy dielectric during the desmear process, overconditioning, overcatalyzation, or insufficient acceleration. The electroless copper bath may become overactive and plate a stressed deposit. Ensuring that the process is functioning as specified with regard to dwell times, chemical concentrations, and bath temperature are the corrective actions.

3. *Bath decomposition:* This is rapid plating out of the copper. Common causes are bath imbalance, overloading, overheating, lack of use, tank wall initiation, by-product build-up and contamination.
4. *Electroless copper–to-copper-clad bond failure:* Copper-to-copper adhesion failures can occur on the surface or on the innerlayers. Surface copper adhesion failures arise from unclean copper. Dry-film and/or developing residues, overconditioning, insufficient rinsing, insufficient microetch, and overcatalyization are common causes. Innerlayer copper-to-copper adhesion failures, commonly referred as ICD, may be due to all the items mentioned. Further causes may be related to the electroless copper bath itself. A stressed deposit due to high bath activity or decomposition has poor integrity and may fail under reliability testing. Specific additives in supplier formulations may contribute to ICDs as well.
5. *Staining:* Copper oxidation is due to moisture or contamination on the copper surface. Corrective action involves dipping boards in antitarnish or hard rinsing in DI water.

32.5.4 Process Outline

This outline presents the typical steps in an electroless copper process:

1. Rack
2. Clean and condition
3. Water rinse
4. Surface copper etch (microtech)
5. Water rinse
6. Sulfuric acid (optional)
7. Water rinse

8. Preactivator
9. Activator (catalyst)
10. Water rinse
11. Postactivator (accelerator)
12. Water rinse
13. Electroless copper
14. Rinse
15. Sulfuric acid or antitarnish
16. Rinse
17. Scrub (optional)
18. Rinse
19. Copper flash plate (optional)
20. Dry
21. Release to image transfer

32.6 ACKNOWLEDGMENTS

Significant portions of this chapter are drawn from Edward F. Duffek, “Preparing Boards for Plating,” in *Printed Circuits Handbook*, 5th ed., edited by Clyde F. Coombs, Jr., 2001, and Jim Watkowski, “Preparing Boards for Plating,” in *Printed Circuits Handbook*, 6th ed., edited by Clyde F. Coombs, Jr., 2008.

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CHAPTER 33
ELECTROPLATING

George Milad
Uyemura International Corporation, Southington, Connecticut

33.1 INTRODUCTION

The reality in printed circuit board (PCB) evolution is that the parts are continuing to increase in degree of difficulty and complexity. A new genre of high-density interconnect (HDI) boards is making the transition from leading edge to mainstream. These boards are characterized by a combination of complex features that include buried and blind vias, high-aspect ratio plating, small-hole plating, and fine lines and spaces side by side with ground plane areas of different sizes.

The industry, however, still has a need to produce simpler products, such as single-sided and double-sided boards; these are still in demand. Multilayer boards with lower layer counts (four to eight) fall in this category also.

This chapter focuses on different aspects of electroplating. Emphasis will be on acid copper. Acid copper electroplating is the process that forms the traces and the through-hole

connectivity that conveys the signal from end to end of the final device. Tin, tin-lead, nickel, and gold electroplating will also be covered.

33.2 ELECTROPLATING BASICS

Electroplating is the production of adherent deposition of conductive surfaces by the passage of electric current through a conductive metal-bearing solution. The rate of plating depends on current and time and is expressed by Faraday's law [Eq. (33.1)]:

$$W = (ItA)/(n\mathrm{F}) \tag{33.1}$$

where W = metal, grams
I = current, amperes
t = time, seconds
A = atomic weight of the metal
n = number of electrons involved in metal ion reduction
F = Faraday's constant (96,485 C/mol)

Plating occurs at the cathode (the negative electrode). Accordingly, deposition thickness is determined by the time and the current that is impressed on the surface being plated; for example, by using the preceding formula, one can readily calculate the weight of the deposited metal. The weight can then be converted to a specific thickness over a known area. To plate 1.0 mil of copper, one would need 17.8 amperes per square foot (ASF) or 1.88 amperes per decimeter (ASD) for 1 h (60 min). The rate of deposition of the most common metals is shown in Table 33.1.

TABLE 33.1 Rate of Deposition of the Most Common Metals Grams

Metal	Grams Deposited per amph	Amp. h. per sq.ft to Deposit 0.001 in	Amp. h. per sq.dm. to Deposit 25 µm
Copper	1.186	17.8	1.88
Tin	2.214	7.8	0.82
Lead	3.865	6.9	0.73
Nickel	1.095	19.0	2.00
Gold	7.348	6.2	0.65

Table 33.2 shows the properties of common electrodeposits.

TABLE 33.2 Properties of Electrodeposits

Property	Cu	Ni	Au	SnPb	Sn
Melting point, °F	1980	2600	1945	361	450
CTE X 10^{-6}/°F	9.4	8.0	8.2	12.2	12.8
Conductivity, %IACS	101	25	73	11.9	15.6
Electrical resistivity, µΩ/cm	1.67	6.8	2.19	14.5	11.1
Thermal conductivity, CGS°C	0.97	0.25	0.71	0.12	0.15

33.3 ACID COPPER ELECTROPLATING

Acid copper plating for PCB application must meet two challenges:

1. Thickness distribution/uniformity of the plated copper
2. Physical/metallurgical properties of the deposit

33.3.1 Thickness Distribution

The biggest challenge facing copper electroplating is the thickness uniformity of the deposit on the different features of the PCB. This is becoming more critical as demands for speed and impedance control continue to increase. On the surface, patterns have extremes of isolated small traces and pads as well as ground plane areas, the isolated traces are of low resistivity and attract more current than the ground plane areas; giving rise to big differences in plating thickness. The through hole offers its own challenges, particularly holes with a high aspect ratio (hole diameter to board thickness ratio). The knee of the hole is a sharp edge that attracts more current and tends to over-plate (dog bone effect) while the middle of the hole may lag behind in thickness.

33.3.1.1 Panel and Pattern Plating. Surface copper can be plated uniformly if the pattern is eliminated as in the case of “panel plating.” With panel plate the surface and the thru hole are plated first. The pattern definition is achieved by subsequent imaging and etching. Here the definition of fine traces is going to be as good as the imaging and the etching capabilities of the manufacturing site. Panel plating is wasteful as a large area of the panel is etched away. It also becomes challenging when the pattern involves small lines and traces, the etching process has to clear the trenches between the traces. In contrast “pattern plate” plates less copper and only etches the laminate copper (Fig. 33.1).

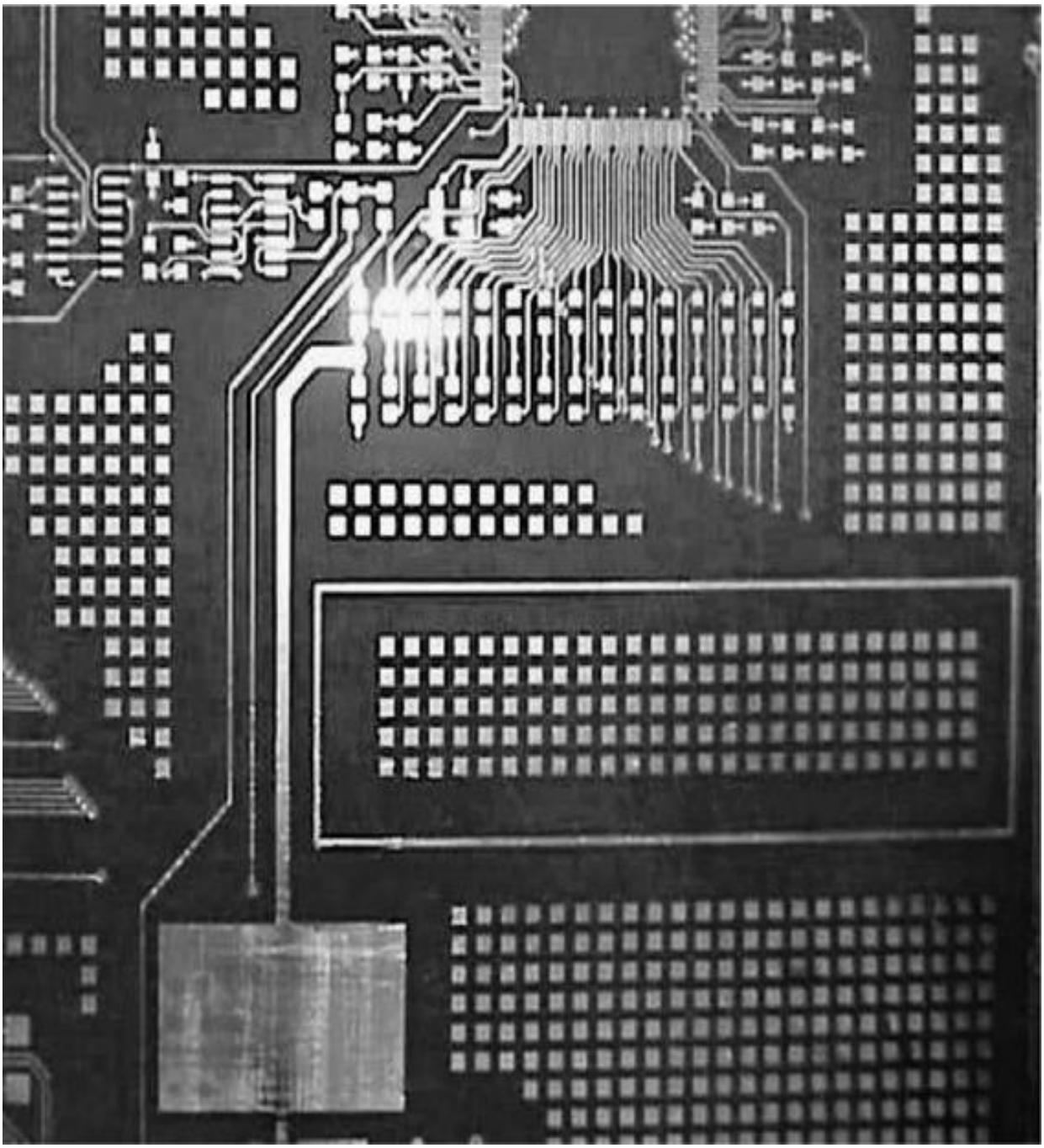

FIGURE 33.1 Example of isolated traces versus ground plane areas.

33.3.1.2 Throwing Power. High aspect thru holes will over plate the knee of the hole and depending on the throwing power (TP; the ratio of the plated thickness in the middle of the hole compared with the thickness at the entrance of the hole) of the plating solution will plate less in

the middle of the hole. The throwing power of the bath is a function of the aspect ratio; meaning the thickness of the plated copper in the middle of the hole may be equal to the thickness on the surface (100 percent TP) for a 3:1 aspect ratio hole and may be only 1/3 of the thickness on the surface (33 percent TP) for a 15:1 aspect ratio hole. In the latter case to achieve a thickness of 1.0 mil in the middle of the hole would result in plating 3.0 mils on the surface (Fig. 33.2).

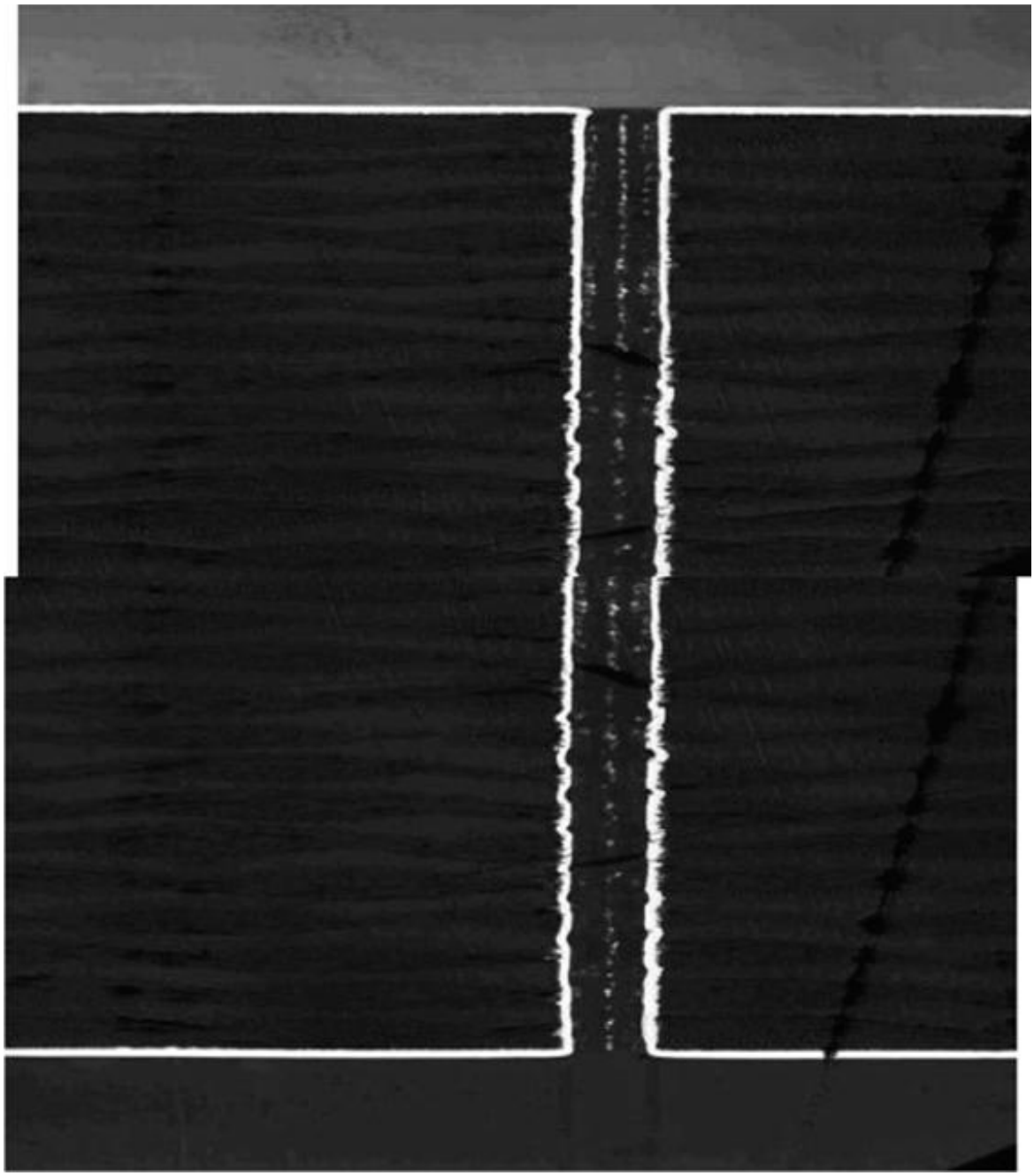

FIGURE 33.2 15:1 aspect ratio plated at 8 ASF in DC mode with greater than 85% TP.

33.3.2 Metallurgical Properties

Another challenge is to ensure that the deposit has the desired metallurgical properties, namely tensile strength and

elongation (T&E). Tensile strength in excess of 35,000 PSI and elongation in excess of 15 percent are desirable properties, to ensure that the plated copper can withstand the thermal excursions during manufacturing and assembly of the plated parts. T&E are directly affected by the crystal structure of the deposit. A fine-grained equiaxed (nondirectional) structure gives the highest T&E values.

33.3.3 PLATING PROCESS

The plating system, or process, should be designed to minimize thickness disparity and to deliver the desired physical properties of the plated copper, with minimum impact on productivity. All aspects of the plating process must be optimized toward that goal, these include:

- The plating solution
  - Inorganic plating chemicals
  - Organic additives
- Tank design
  - The plating tank, weir
  - Anode/type and placement
  - Cathode racking
  - Solution agitation
  - Part agitation
  - Filtration
  - Temperature
- Horizontal plating equipment
- Rectification
  - DC
  - Pulse

33.3.3.1 The Plating Solution. The plating solution is composed of both inorganic and organic chemicals. The chemicals in the bath have to be optimized for the intended use. The supplier should be able to guide the manufacturing site to the best chemical setup for their specific application.

33.3.3.1.1 Inorganic Chemicals. These consist of copper sulfate (g/L), sulfuric acid (g/L) and chloride ion (ppm). The copper sulfate contains the copper ion to be plated, the sulfuric acid supplies conductivity to the solution and the chloride ion serves a dual function: it plays a part in the corrosion of the anode and also in the adsorption/suppression of the carrier molecule.

The ratio of copper to acid varies based on the plating current density (CD). A low CD bath would use low copper concentration with high acid and the reverse is true for a high CD bath. A low CD bath uses longer plating times and does not require high copper ion concentration as the copper ion in the vicinity of the cathode is not readily depleted during plating; the high sulfuric, increases the conductivity needed for low current density plating.

The table below lists the inorganic ratios needed for different current densities of plating:

Component	Low CD Plating 5–20 ASF (0.5–2.0 A/dm)	Conventional Plating 20–40 ASF (2.0–4.0 A/dm)	High Speed Plating 40–150 ASF (4.0–15.0 A/dm)
Cu	1–2 oz/g (7–15 g/L)	2–3 oz/g (15–22 g/L)	7–8 oz/g (50–55 g/L)
$CuSO_4 \cdot 5H_2O$	4–8 oz/g (30–60 g/L)	8–12 oz/g (60–90 g/L)	28–32 oz/g (210–250 g/L)
H_2SO_4	20–32 oz/g (150–250 g/L)	12–20 oz/g (90–150 g/L)	7–10 oz/g (50–75 g/L)
Cl ion	40–80 ppm	40–80 ppm	40–80 ppm

33.3.3.1.2 Organic Additives. Ideally the organic additives should be continuously dosed into the plating solution based on ampere hours of plating. The dosing

pumps would be calibrated to deliver the desired volume of each component at specific ampere hour intervals. Organic additives are composed of

- Carriers
- Brighteners
- Levelers

Carriers increase the polarization resistance and are current suppressors. The suppression is a result of the carrier being adsorbed to the surface of the cathode; this results in increasing the effective thickness of the diffusion layer. The result is better organization. This gives rise to a deposit with a tighter grain structure. The carrier modified diffusion layer also improves plating distribution without burning the deposit.

The brightener is a grain refiner. Its random adsorption may produce a film that will suppress crystallographic differences. Alternatively brighteners may be adsorbed preferentially on particular active sites such as lattice kinks, growth steps, or tops of cones, or surface projections in general; growths at these locations are then blocked. The brightener produces a fine grained non directional (equiaxed) grain structure. It is the additive that directly affects the tensile strength and elongation properties of the deposit.

Levelers are small molecules that carry a partial charge that are attracted preferentially to the higher current density areas on the platting surface. Levelers, or leveling agents, are selective inhibitors present at low concentrations in the electrolyte as compared to the depositing metal. In case of a micro profile the diffusion layer does not follow the profile contour, but is maximum at the valleys and minimum at the peaks. Consequently, in absence of a leveling agent, depositing ions diffuse more rapidly to the peaks than to the valleys, and deposits grow more rapidly on the peaks,

resulting in an exaggerated profile. With good solution agitation, the leveler will accumulate more rapidly and readily at the peaks and it will inhibit growth or deposition. This allows the valleys to catch up to the peak, thus creating leveling.

33.3.3.2 Tank Design. Tank design is critical to the success of achieving the goals of thickness distribution and the physical properties of the deposit.

The tank material should be inert and nonconductive like polypropylene or PVC. The overall dimensions are based on the number of panels to be plated at any one time. The simplest plating bath would be a single plating cell with a single panel on a centrally located cathode bar with two anode bars one on either side of it. The length of the tank should be the panel width plus 12 to 16 in plus 8 to 12 in for the weir. The length may be expanded to allow for more panels to be racked on the cathode bar. The breadth—determines the anode to cathode distance—should be 18 to 30 in. 18 in will give 6 in between the anode basket and the panel and 30 in will give 12 in. The depth should be the depth of the panel plus 8 to 10 in from the top of the weir. This allows for better uniformity of solution agitation that is initiated from the bottom of the tank. The tank or bath may contain multiple plating cells (Fig. 33.3).

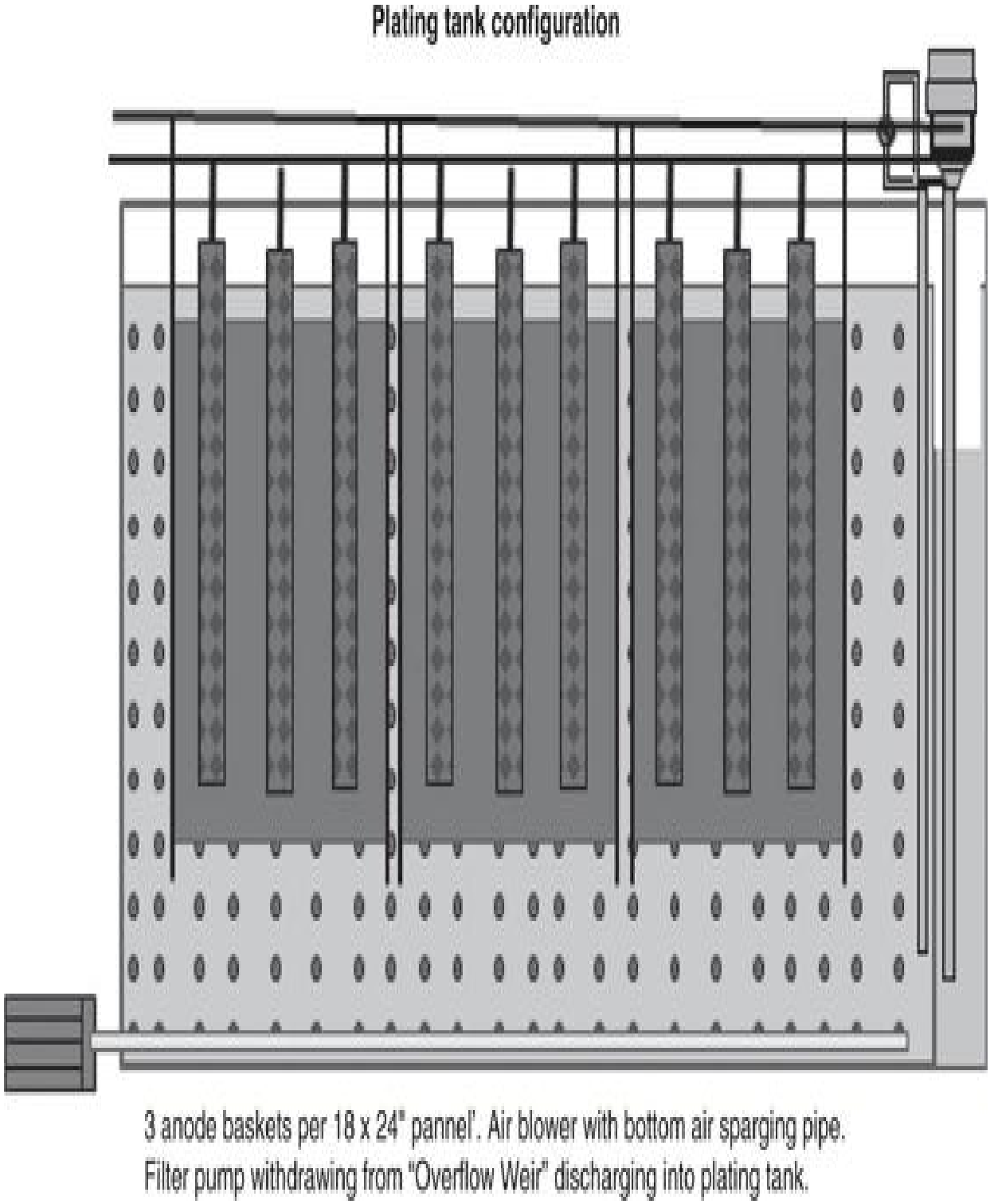

FIGURE 33.3 Tank configuration.

The weir should be located at the shorter end of the tank. It should create an 8 to 12-in well behind it; the height of the

weir should be 5 to 8 in below the surface of tank. The filtering pump should draw solution from the bottom of the weir well and return the solution to the plating area of the tank that in turn would overflow back into the well. The weir holds the solution level constant and allows suspended particulates to be forced thru the filtration system. In addition the overflow causes a certain amount of aeration which is beneficial in airless sparging systems.

33.3.3.3 Plating Materials and Equipment

33.3.3.3.1 The Anode. Anode types: Anodes may be one of two main categories: soluble anode or insoluble anode.

The soluble anode has been the staple of the industry. The anode is made of copper. Upon rectification the copper metal is oxidized to the copper ion and goes into solution. The copper ion is reduced to copper metal at the cathode where the plating occurs. Other than the source of copper the anode is positively charged when the rectifier is turned on and its location relative to the cathode has a direct impact on thickness distribution of the plated copper. For proper functioning the copper anodes must form an oxide film on the surface that helps the dissolution of the anode. New copper anodes must be filmed before utilization. This is accomplished by dummy plating at low CD for an extended time, per supplier recommendations.

One form of copper anode is a slab of copper (Fig. 33.4) with fixed starting dimensions. As the anode is used it dissolves and its dimension are reduced, and this would have an adverse effect on the plating thickness distribution. The reduced anodes will need to be replaced with new slabs. Replacing the anode is wasteful and not replacing it gives poor results. The alternative, which prevails in the industry, is to use a titanium basket (Fig. 33.5) with round or rectangular cross-section, full of copper balls. As the balls are used up the basket is replenished maintaining a constant area for the anode. The only downside to the balls is that

over time the balls at the bottom of the basket are reduced in size while the top has the full dimension of the copper ball. Anode maintenance would need to be performed periodically to remove the small balls. This is necessary as the small balls get buried in sludge, which is a natural byproduct of the dissolution of the anode. To prevent the sludge from getting into the plating solution all anodes are contained in a polypropylene anode bag. The bag should be loose, not napped and 2 to 3 in longer than the basket. The bags should be replaced periodically depending on usage.

FIGURE 33.4 Slab copper anodes.

FIGURE 33.5 Titanium anode baskets.

The alternative to a soluble copper anode is an insoluble anode. This anode serves the function of being positively charged and it will repel the copper ions toward the negatively charged cathode, and its location in respect to the cathode has a direct impact on thickness distribution, but it is not a source of copper ions. The common form of the anode is an expanded titanium mesh that is coated with what is referred to as mixed metal oxide coating (MMO) (Fig. 33.6). The primary component of the MMO is iridium oxide. These anodes produce oxygen gas during operation. If, MMO/Ti anodes are used, a source of copper must be added to the system. The most common source is CuO. CuO is dissolved external to the plating cell and is added based on ampere hours of plating. The MMO/Ti anode offers a constant area and does not require anode maintenance, in addition it does not require an anode film and eliminates the need for dummy plating.

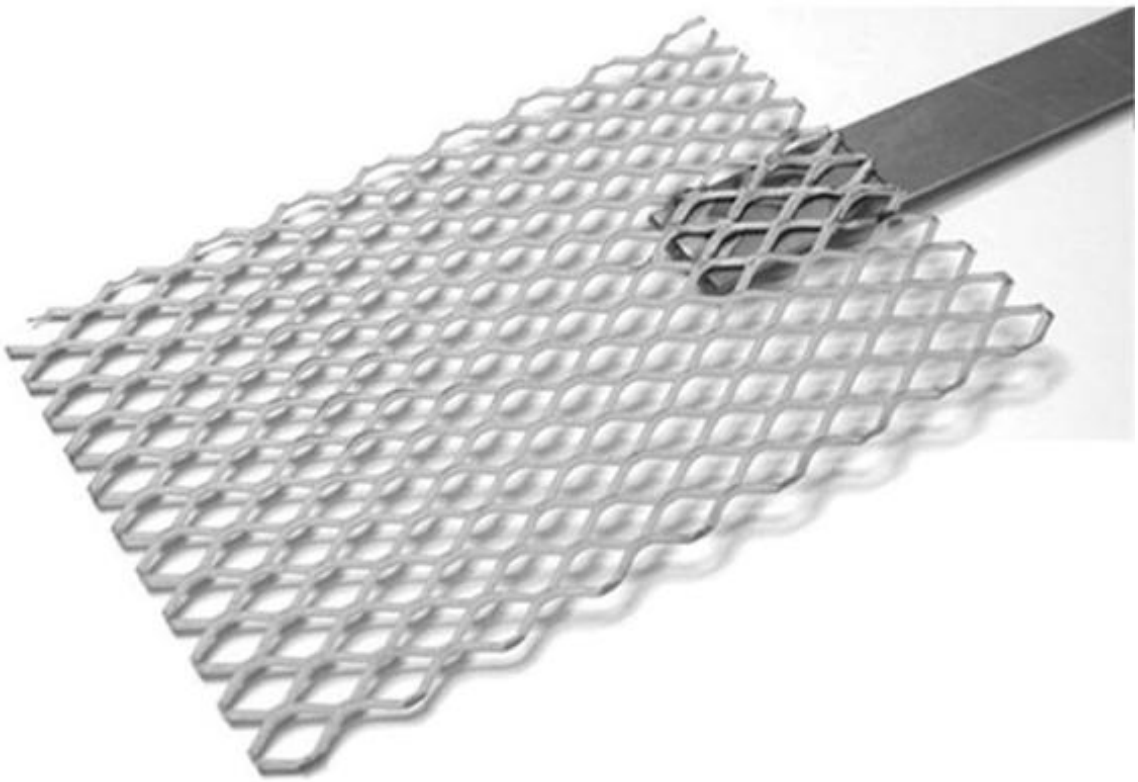

FIGURE 33.6 Insoluble anode.

MMO/Ti anodes have been adapted successfully in conventional plating; however, their primary utilization is in both vertical and horizontal conveyorized plating equipment.

Anode placement: The current initiates at the anode and is pulled in by the cathode. Areas of the cathodes that are closer to the anode source will plate more than areas further out. Accordingly the number of anode sources (baskets) and their distribution play an important role in the degree of thickness uniformity. The number of anodes should be adjusted to the plating current load, this is a function of CD and platable area. The higher the load; example panel plating, would require more anode baskets; example would be 3 to 4 round baskets (2.5- to 3.5-in diameter) per 18 × 24-in panel. For reduced platable areas; example pattern plate, 2 to 3 baskets would be adequate (Fig. 33.7).

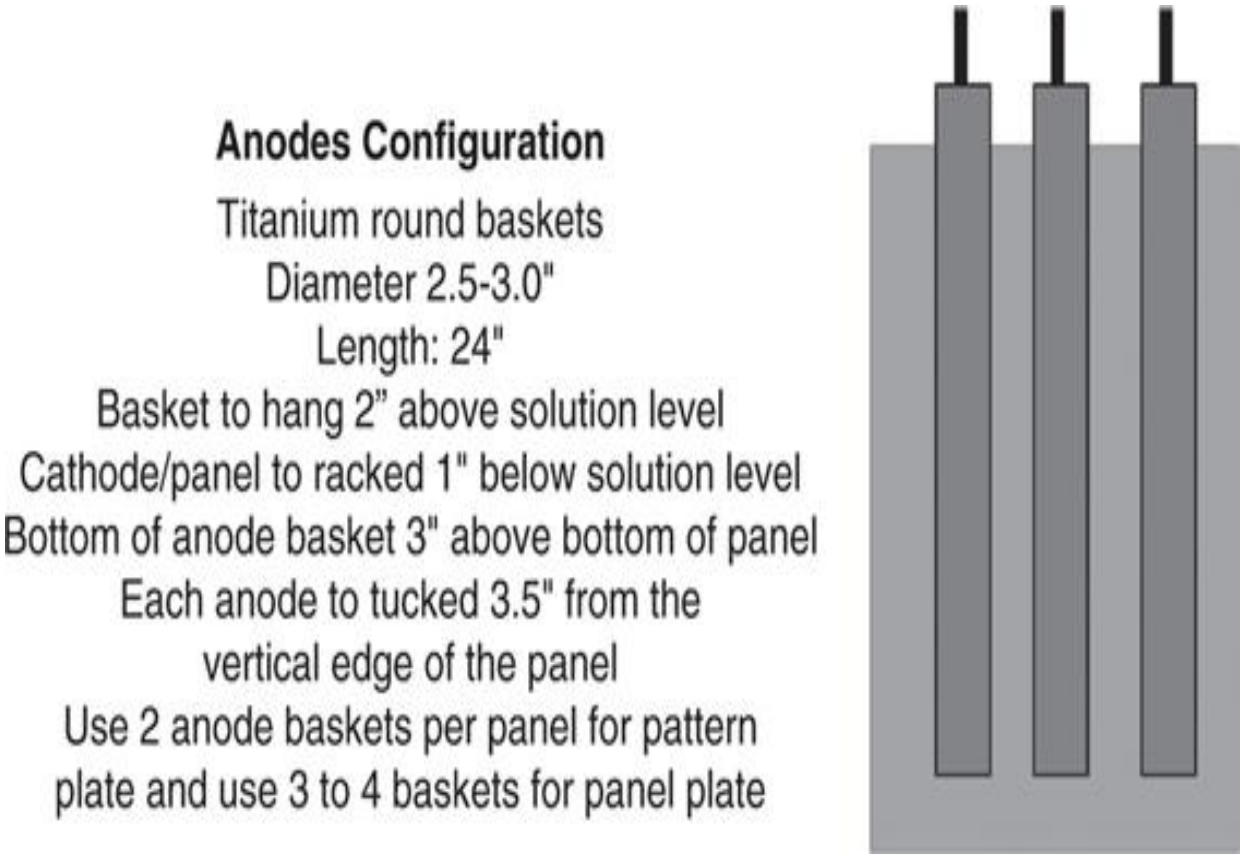

FIGURE 33.7 Anode placement.

Anodes should be evenly distributed throughout the anode bar. The anode should be 3 to 4 in shorter than the cathode and should be tucked into the cathode window by 3 to 4 in. This will reduce overplating at the bottom of the panel and at the vertical outside edges.

33.3.3.3.2 The Cathode. The cathode is composed of the panels to be plated on the cathode bar. The cathode bar, or the sum total of its agitation, should be equidistant from the front and back anode bars. Ideally the cathode window should be consistent commensurate with the anode configuration. The panels should be racked as close to each other as possible and should be racked within 1.0 in of the surface of the plating solution. Racking below solution level >1.0 will allow increased plating on the top edge. The cathode bar should be racked full with no gaps. If gaps are inevitable an appropriate dummy strip should be added to

protect the edges at the gap from overplating. Another approach would be to isolate any anodes that do not have complimentary cathodes across from them.

33.3.3.3.3 Cathodic Agitation. Cathodic agitation is recommended (1 to 3 in, through hole at 10 to 20 strokes per minute). The agitation offsets the solution flow rate front and back allowing for enhanced mass transfer thru the holes, like in getting alternately closer and further to the source of air sparging or e-ductor plume.

33.3.3.3.4 Solution Agitation. Solution agitation plays four important roles in plating:

1. It replenishes the copper ion in the immediate vicinity of the plating site (the diffusion layer). The primary source of replenishment of copper is “diffusion” which occurs naturally. When the rate of deposition is greater than the rate of diffusion, solution agitation must be implemented. It is more critical in baths with low copper concentrations. In absence of good copper ion replenishment the deposit would burn (not adherent and rough deposit).
2. Depending on the presence and the type of leveling component in the plating solution, agitation would sweep the leveler molecule across the surface of the panel where it is preferentially adsorbed to the high CD areas suppressing the plating thus creating leveling. This is particularly important in filling blind vias, by suppressing surface plating at the knee of the via and allowing the bottom of the via to plate faster and create filling.
3. In conjunction with cathodic agitation, solution agitation improves mass transfer thru the holes, a critical function when plating high aspect ratio holes.
4. The air maintains an oxidative environment in the solution and will oxidize any cuprous ion (Cu^{+}) to the desired cupric ion (Cu^{++}).

There are two common ways to agitate an acid copper plating solution, namely; air agitation and e-ductor agitation. The key is to produce uniform agitation at the cathode with the desired degree of turbulence/replenishment.

Air agitation is based on sparge pipes (Fig. 33.8) laid along the bottom of the tank below the cathode, in some instances a single pipe is used, with the cathodic agitation offsetting the flow front and back. In other cases two pipes are used one forcing air in front of the cathode and one forcing air behind the cathode. The source of air is an air blower; it should be sized to produce uniform air across the length of the cathode and to produce the desired degree of turbulence. In instances where transporting the leveling molecule is critical air agitation should be vigorous.

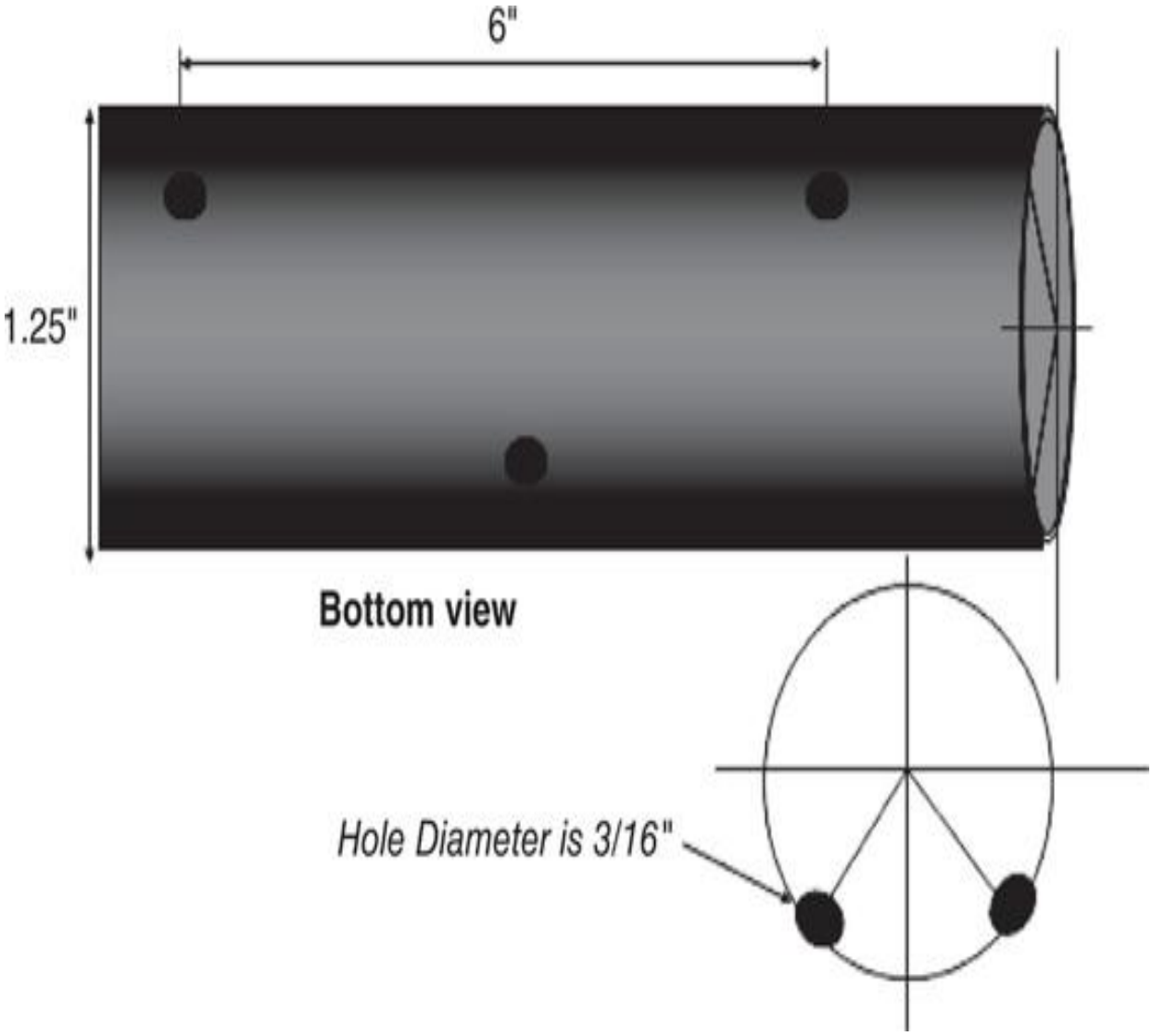

FIGURE 33.8 Forced-air sparger pipe details.

E-ductor agitation is based on the use of e-ductor nozzles (Fig. 33.9) spaced across a bottom manifold. The location and the spacing should be such that they produce uniform parallel flow (laminar) across the surface of the panel. Again here one may use a single manifold under the cathode or use dual manifolds one in front and one in the back of the cathode. Dual manifolds is the preferred arrangement. The location of the nozzles across each manifold should be such that nozzles on the one pipe are not directly across the nozzles on the opposing pipe.

FIGURE 33.9 Four inch- and 2.75-in e-ductor nozzles.

If e-ductors are used the depth of tank should allow for that; meaning the top of the e-ductor nozzle should be approximately 6 in below the bottom of the panel to be plated. In addition if the turbulence is inadequate to

minimize the cuprous ion; gentle air bubbling may be introduced in the weir or in a corner of the tank.

33.3.3.3.5 Part Agitation. Part agitation or cathodic agitation may be one of 2 types: “through-hole” agitation or “knife edge.” The more common “through hole” part agitation helps in solution exchange in the holes, particularly for higher aspect ratio holes. Getting copper ions to the plating sight or “mass transfer” is critical to the thickness distribution of the plated copper. Thru hole agitation does not alter the anode to cathode relative locations, it only alters the solution flow front and back by bring the cathode closer or further to the source of solution agitation.

Knife edge agitation helps in surface solution replenishment and in diffusing the lines of flux emanating from the anode toward the cathode. Increasing the anode to cathode distance preempts the need for knife edge agitation.

33.3.3.3.6 Filtration. Solid particulates in the electrolyte may be one of two types, inert or conductive. The inert particulates winding on the surface of the cathode would inhibit plating causing pitting. Conductive particulates at the cathode become nucleation sites and cause nodulation. Particle removal is a critical part of the plating system setup. It is achieved by continuous filtration through a polypropylene filter cartridge (polyspun) with 5 to 10 µm rating. The filtration intake is from behind the weir and returns into the main tank through a pipe running across the bottom of the tank centered under the cathode. The filter pump should be sized for 2 to 4 solution turnovers per hour STO/h.

33.3.3.3.7 Temperature. Temperature is a critical parameter for PCB plating; refer to vendor recommendations. Electrolytes operate in a relatively narrow range of temperature; example is 70 to 80°F. Maintaining the temperature within the specified limits has a direct impact on the quality of the deposit. If solution agitation is based on e-ductor flow; the temperature of the bath will rise from the

continuous pumping. Cooling will become the dominant temperature controlling factor. This is usually achieved utilizing a titanium cooling coil, connected to a chiller and appropriately located in the tank.

33.3.3.4 Rectification. Two main types of rectifiers are in use for copper plating namely direct current of DC rectifiers and periodic pulse PP rectifiers.

33.3.3.4.1 DC Rectifiers. Direct current rectifiers are the staple of the industry. The rectifier should be sized to supply the desired output, example if the platable area is limited a smaller rectifier would be the right choice, it is not advised to use a 200-A rectifier to plate at 10 to 20 A. Ripple (% AC; alternating current) should be less than 5 percent to ensure the deposit is fine grained adherent and equiaxed. High ripple would have an adverse effect on the physical properties of the deposit. The control accuracy or resolution should be 1 to 2 percent to ensure consistency of output. DC rectifiers use standard cable connections.

When plating with DC rectification the plater needs only to set the plating current density or amperes and plating time; with that he can readily calculate the amount of copper that will be plated.

33.3.3.4.2 Pulse Rectification. Here the current is supplied in pulses or burst. The rectifier is switched on and off in a controlled fashion in millisecond intervals. This pulsing has an effect on the diffusion layer and additive adsorption. The additives are desorbed in the off or reverse mode and readsorbed when the forward current is back on. The adsorption and desorption are not even everywhere. In the high-current density areas this process takes longer than the areas of lower CD. This helps even out the plating thickness between areas of varying CD on the part. Pulse rectifiers are connected to the plating cell with coaxial cables.

Pulse rectifiers also known as switch mode rectifiers produce a pulse wave. An example of a periodic pulse reverse (PPR) wave, would be to set the switch mode rectifier to the equivalent of 20 ASF in the positive mode for 10 to 20 ms and then to switch to a reverse at 3× or 60 ASF for 0.5 to 1.0 ms, respectively. For best results the switching should be instantaneous resulting in a square wave.

When using PPR the plater must set a program for the forward current and the reverse current, the forward millisecond time and the reverse time; he must also verify the shape of the wave. These are a lot of parameters to set up and will take a learning curve until a successful recipe is achieved for the product being plated. Changes in the product type may require a different wave setup.

Pulse plating produces a different crystal structure; it does not produce the same fine grained equiaxed structure that DC produces. The finished surface appears duller than DC. Attention must be paid to achieve the desired physical properties of T&E for the deposit. When properly set up PPR plating has a positive effect on thickness distribution; different switching programs may be needed for different plating configurations.

An optimized electrolyte in an optimized plating cell is the key to producing the desired copper physical properties and thickness distribution, in general the lower the CD of plating the better the thickness distribution of the deposit. Of course this would imply that the electrolyte used should be able to support the choice. This approach has a direct impact on productivity of the plating line and may not be a viable option.

The organic additive system must be chosen based on the type of work anticipated. Most suppliers offer more than one additive system geared toward meeting specific plating configurations.

33.3.3.5 Conveyorized Plating. Here, the panel is transported in a horizontal mode through the plating equipment with stationary anodes below and above it. The panel continues to plate as it travels, interfacing with one anode after the other. The panel comes off the end of the line plated.

Horizontal processing is suitable for high productivity manufacturing sites where large numbers of the same part are a common daily requirement.

The plating thickness is a function of time and current density. The dwell time is determined by the length of the plating module and the conveyor speed. Plating at 20 ASF for 60 min. in horizontal equipment running at 1 m/min. would require a plating module that is 60 m long. This length is not practical. Current density has to be increased to 40, 60, 80, and higher ASF. At 80 ASF, the equipment length needs to be only 15 m.

New chemical additives were formulated to accommodate high-current-density plating.

However, this current density offered new challenges: at high-current densities, most plating solutions lose throwing power. Another problem that was encountered early on was that the anode film particulates would land on the top side of the panel and eventually create nodulation. This did not occur on the bottom side.

Nodulation was resolved by taking the copper dissolution out of the module and replacing the standard anode with an inert or insoluble anode. Copper dissolution or oxidation was achieved by different means, such as the dissolution of copper oxide, or the use of external rectification.

33.3.3.5.1 Horizontal Processing Advantages. Advantages of horizontal plating: The most dramatic advantage of horizontal plating is the uniformity from panel to panel. All panels go through the equipment in an identical fashion. They all see the entire bank of anodes,

and they are in a single plating solution. All panels coming off a horizontal line are alike. If for some reason one edge of the panel has higher plating, then all panels will have the same edge equally high. In vertical plating, different panels are plated in different parts of the cell, in different positions in the rack, and even in different tanks or baths. Although vertically plated panels may all be within specifications, there will always be inherent variability that the shop has to contend with in downstream processing beyond the plating line.

Horizontal plating machines can be easily automated. Loaders and unloaders are usually integrated in the system. Automation of chemical analysis and dosing is incorporated with minimum cost increase. The equipment is easily linked to pre- and postprocesses. Horizontal processing lends itself well to continuous production flow and reduced cycle time.

Anode uniformity is a major advantage in horizontal plating. The size and geometry of an insoluble inert anode do not change. Anode variability and maintenance are eliminated. The latter is a very labor-intensive and hazardous activity is associated with vertical plating.

Horizontal equipment is completely enclosed. This minimizes the operator and shop personnel’s exposure to acid and chemical fumes and creates a better and safer working environment.

Horizontal plating gives superior surface thickness distribution. Variation of less than 10 percent across a panel-plated surface is normal. This is due to the anode’s close proximity to the cathode; usually, the anode-to-cathode spacing is between 8 and 10 mm, or 0.3 and 0.4 in.

33.3.3.5.2 Drawbacks of Horizontal Processing

1. The equipment requires a substantial investment and is a major deviation from standard vertical processing.
2. Panels processed must have one common dimension commensurate with the width of the conveyor.

3. If the equipment is used for pattern plating each order must clear the equipment before the next order with a different platable area can be introduced.
4. If soluble anodes are used; nodules on the top surface are a problem.
5. If insoluble anodes are used, allowance for anode gassing must be implemented.
6. The equipment must be operated at relatively high CD which reduces throwing power in the hole.
7. There is both a learning curve and engineering know-how that will be needed to run this equipment smoothly.
8. It requires a large parts inventory and trained equipment maintenance crew to ensure uninterrupted operation.
9. The equipment is integrated, and either it all works or it all doesn't.

33.3.3.6 High Aspect Ratio Plating

33.3.3.6.1 High Aspect Ratio Drilled Hole Issues. Pattern plating application pose a challenge to the electroplating process. Plating is accomplished using lower current densities (5 to 20 ASF) for extended plating times. It is a balance between the organic (with leveling component) and inorganic components (low copper high acid formulation) of the electrolyte coupled with the cell configuration where the cathode and anode are located to yield the best uniformity of flux lines and the solution and part agitation are designed for electrolyte replenishment and allow for maximum mass transfer thru the holes.

33.3.3.6.2 Blind Via Hole Fill. Blind vias that connect layer 1 to layer 2 or to layer 3 are an enabling technology for HDI (high-density interconnect) type boards. This activity started by conformal plating of the via (Fig. 33.10) and eventually developed into "via fill" (Fig. 33.11). Via fill makes for a robust connection with no chance of any voids during assembly. Vias with 1:1 aspect ratio are common, it is

possible to plate vias that are deeper than the diameter of the via up to 1.2:1.

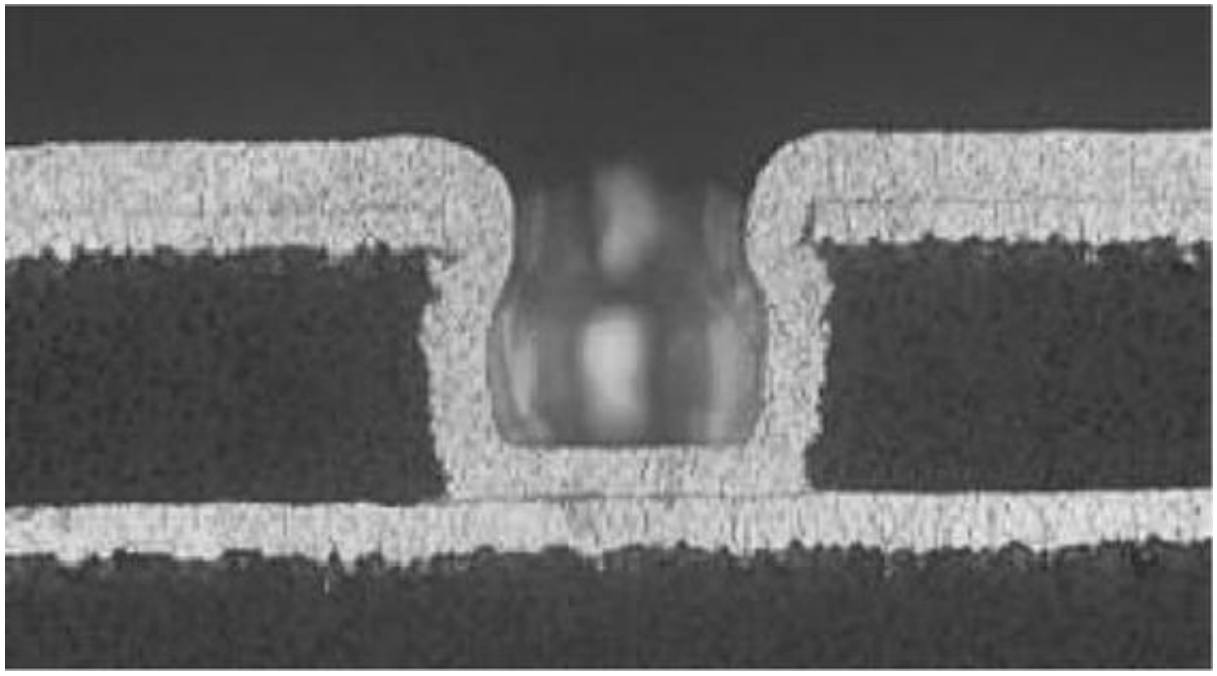

FIGURE 33.10 Blind via plating.

Successful via fill plating requires a specific electrolyte; the copper concentration is as high 50 to 60 g/L copper with low sulfuric acid at 30 to 60 g/L. This is combined with a unique organic additive combination with a prominent leveling component. The leveling component acts predominantly on the surface and suppresses the surface plating allowing the brightener and carrier combination to plate up from the bottom of the via, for filling to occur. Ideally the solution movement must be vigorous and parallel to the surface (laminar flow); this ensures adequate leveler replenishment at the surface of the via. Inadequate solution flow across the surface will produce conformal plating with no filling (Fig. 33.11).

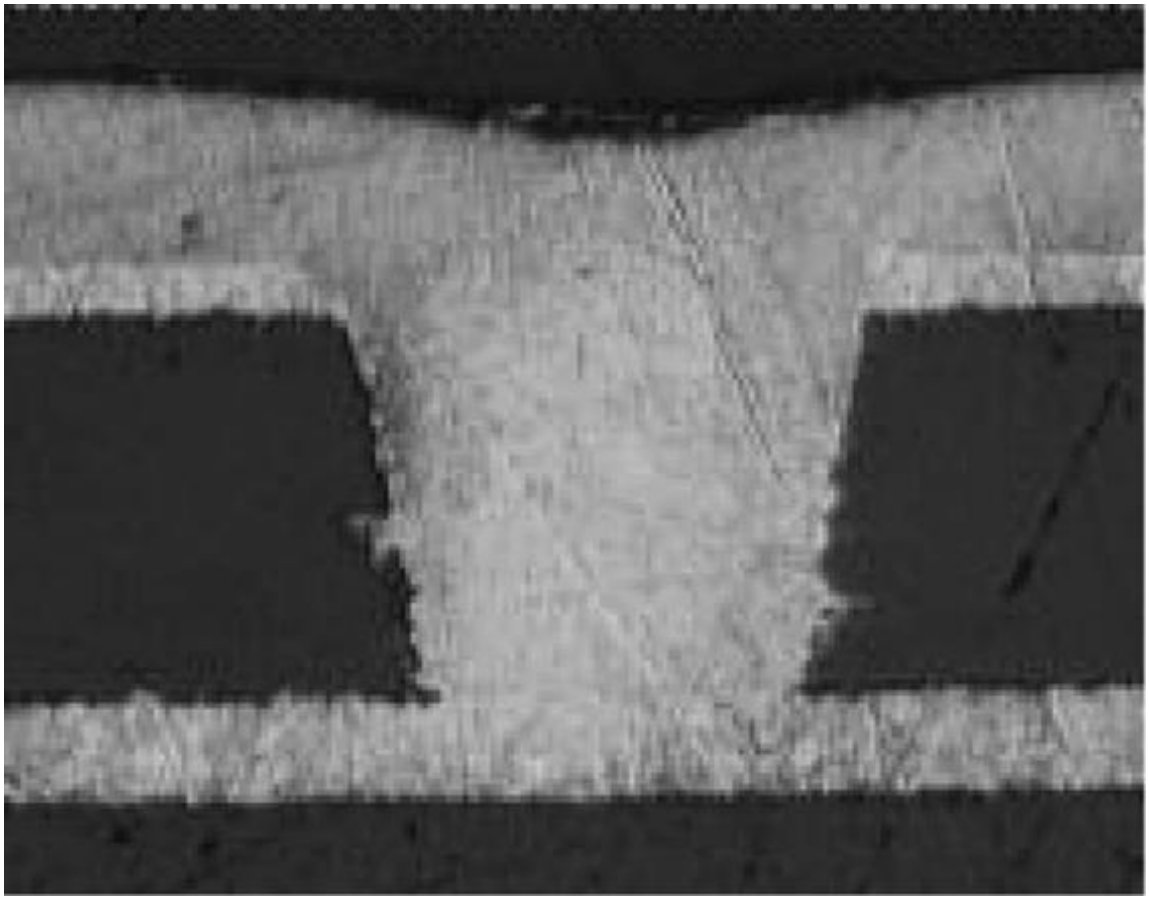

FIGURE 33.11 Blind via filling.

Blind via plating is presently done using both pattern (dot pattern) and full panel plating. Plating CD varies from 10 to 25 ASF, using a single setting example 12 ASF for 90 min, or a series of step up CDs, example 10 ASF for 30 min followed by 15 ASF for 20 min followed by 20 ASF for 20 min. The plating cycle should be optimized for the product and the equipment capabilities.

In the case of pattern plate, planarization after resist stripping is necessary to reduce the thickness of the copper on the surface above the via.

33.3.3.7 Bath Management and Control. With attention to solution management and control the electrolyte performance may be maintained for years. This may be divided into three areas:

1. Inorganic chemical control
2. Organic additives control
3. Contamination control

33.3.3.7.1 Inorganic Chemical Control. This involves the chemical analysis and control of the following:

- Copper sulfate
- Sulfuric acid
- Chloride ion

Titration methods are readily available for these analyses.

Copper sulfate concentration in baths that use soluble copper anodes will grow over time. Based on the operating range, the copper sulfate must be partially dumped to bring the copper sulfate in range. Insoluble anodes (Ti/MMO) have been used to plate out excess copper in the electrolyte. This method produces plated copper and avoids the generation of disposal waste.

In general the sulfuric acid and the chloride concentrations values remain consistent over time. The analysis is important during setup. It is also a way to ensure no extraneous chloride is being introduced into the bath.

33.3.3.7.2 Organic Additives Control. This involves the analysis and control of the following:

- Brightener
- Carrier
- Leveler

The organic additives have a direct impact on the physical properties and thickness distribution of the deposited copper.

Traditionally the hull cell was used to give an indication on the effect of brightener on the plated brass panel. A matte panel indicated no brightener and a fully bright panel

indicated adequate or excess brightener. For simpler additive systems (premixed carrier leveler and brightener), and with experience, this method can be effective.

With a better understanding of the role of each component and the availability of the additives in separate containers for the more sophisticated systems; a better method was needed. Cyclic voltammetric stripping (CVS) is now the method of choice for assessing the effective concentrations of the different additive components. CVS methods for analysis of each component are available and in use.

33.3.3.7.3 Organic Contamination. Sources of organic contaminants:

- Additive break down products particularly the carrier or suppressor.
- Extraneous organics brought into the bath such as the leaching of dry film components into the bath

The most practical way to get a handle on organic build up in the bath is to run a total organic carbon (TOC) analysis. For TOC values to be useful, a baseline needs to be established. The base line should be a fresh makeup simulation. Here the entire value (1×) comes from the additive contribution alone.

The upper limit for TOC should be established for each individual production environment, type of bath, bath loading, plating current density, type of product, etc. A good starting point is when the TOC value approaches 4× the original makeup value, a carbon treatment should be conducted. However, if there is an observed deterioration in the quality of the deposit the 4× value may be reduced to 3×, and so on.

The treatment is deemed successful if the TOC numbers drop to approximately 70 percent of the starting high TOC value. Once that is established then the shop will need to maintain the carbon-treat schedule.

Example: If the starting point the 1× is 300 ppm and the bath survives without adverse effects up to 4× (1200 ppm), and is then C-treated down to 70 percent (~850 ppm), these become the upper and lower limits that have to be maintained and the bath must be run between 850 and 1200 ppm.

In absence of TOC analytical capability, carbon-treatment based on electrolyte utilization can be set up. An example would be 100 to 120 Ah/L of bath for electrolytes using dry film pattern plate.

33.3.3.7.4 Carbon Treatment. C-treat can be conducted at two different levels:

1. Carbon treatment with no oxidant (C-polish)
2. Carbon Treatment with oxidant (C-treat)

Carbon polish involves circulating the bath through a bed of activated carbon in a carbolator, or an activated carbon filter at bath or room temperature. Carbon treatment involves the use of oxidants like hydrogen peroxide to break down the organic contaminants. This is usually done in a separate tank equipped with heating and mixing capabilities. The equivalent of 0.5 percent by volume of 35 percent hydrogen peroxide and activated carbon at ~2 g/L are added, with continuous solution agitation and heated at 120 to 140°F. Maintain temperature and mixing for approximately 4 h before cooling the bath. The cooled down bath is transferred back to the plating tank through a filter. The quantity of carbon and solution contact time, have to be established with the initial treatment. Once established the process is to be duplicated for every treatment thereafter.

33.3.3.8 Trouble Shooting Acid Copper

33.3.3.8.1 Corner Cracking. This occurs at the knee of the hole and is seen in cross-section after thermal shock. It indicates inferior crystal structure like coarse columnar

plating versus fine equiaxed crystals. It could also be the result of reduced plating at the knee of the hole due to over leveling. Both causes are corrected by adjusting the components of the organic additives.

33.3.3.8.2 Columnar Deposit. Insufficient brightener. Check and adjust additive concentrations and ratios.

33.3.3.8.3 Voiding in the Hole. Voids occur from one of the following:

- *Voids in the original metallization:* This needs to be fixed at the metallization process.
- *Voids due to air entrapment in the bore of a small hole:* This is resolved in the pretreatment “cleaner” step. The cleaner removes soils and oxidation and has an important function of wetting the hole. Vibration may be needed in the cleaner to ensure good wetting in the hole and to eliminate any entrapped air.
- *Voids from etch out due to voids in the tin (etch resist) plate:* Correction is to increase the thickness of the tin plate.

33.3.3.8.4 Roughness or Nodules. Nodules result from conductive particulates like anode sludge creating nucleation sites at the surface during the plating cycle. Corrective action; ensure the filtration system is operating properly. Check that no anode bags are torn or that the solution level is below the top of the bag.

33.3.3.8.5 Burning in the High CD Area. This is due to insufficient replenishment of copper ions. The easiest thing is to reduce the CD of plating, or to use an electrolyte with higher copper content that supports the desired CD of plating.

33.3.3.8.6 Poor Throwing Power in the Hole. The CD of plating is too high for the specific aspect ratio. Make sure that the electrolyte is designed to support good throw in the target aspect ratio, and CD range.

33.3.3.8.7 Poor Leveling. First ensure that the electrolyte used has leveling capabilities. Leveling on the surface is a function of solution replenishment/movement. More flow produces better leveling. Excessive leveling activity may cause step plating.

33.3.3.8.8 Inferior Thickness Distribution on the Surface. This can occur in pattern plate and to a lesser extent in panel plate. Thickness distribution can be enhanced by optimizing the cell geometry anode and cathode placement and solution and part agitation. Lower CD of plating reduces thickness variation. Electrolytes with the proper ratio of suppressor and leveling agents will give better thickness distribution.

33.3.3.8.9 T&E below Specified Values. The best values for tensile strength and elongation are achieved with a fine grained equiaxed crystal structure. This is achieved when the additives are operating in the optimum operating ranges. The brightener is the grain refiner. Other things that could impact T&E values is organic contamination and rectifier ripple (<10 percent). Contamination can be fixed by C-treating the electrolyte.

***33.3.3.9 Preplate Treatment*.** The pretreatment is composed of three steps: (1) the cleaner, (2) the microetch, and (3) the predip. The combined effect of the pretreatment is paramount to the success of the plating.

There is no room for compromise in these steps

33.3.3.9.1 The Cleaner Step. The cleaner is composed of a solvent, an acid and a surfactant. The solvent removes organic surface residues by dissolution. The acid removes oxidation and the surfactant wets the surface. The wetting is very important when plating small high aspect ratio holes or blind vias; a well wetted surface will not trap air. Intermittent vibration in this step is helpful to ensure that all air is dislodged from tight spaces. Follow vendor’s recommendations of concentration, temperature, dwell time

and dump and remake schedule to ensure the cleaner functions as intended. Good two-step rinsing is important after the cleaner as its components in trace amounts, if dragged down the line may adversely affect the plating.

33.3.3.9.2 The Microetch Step. The microetch is made up with a strong oxidant like sodium persulfate or hydrogen peroxide in a sulfuric acid medium. The microetch oxidizes the surface copper and literally etches it away exposing a fresh copper surface for plating. If the metallization used is electroless copper; the concentration and dwell time should be controlled to ensure that the electroless copper is not etched away. In addition the microetch can undercut minute stubborn residues that the cleaner did not remove. Concentration, temperature, dwell time and dump and remake schedule must be adhered to. The panels are double rinsed after the microetch.

33.3.3.9.3 The Predip Step. The predip is made up with sulfuric acid at 5 to 10 percent. This step ensures that the surface is oxidation free and is acidic to match the acidity of the electrolyte. There is no rinse between the predip and the acid copper bath.

33.4 TIN ELECTROPLATING

The primary use of tin electroplating in printed wiring board (PWB) manufacturing is as an etch resist after panel or pattern plating. The tin plate is the final step in pattern definition. The process starts with defining the pattern to be copper plated using a photoimageable resist. The plated copper pattern is then plated with a coating of tin. The panel is then resist stripped and the exposed laminate copper is then etched away, leaving the desired circuit with its tin coating. The final circuitization step is tin stripping.

33.4.1 Acid Tin Sulfate

This is the most widely used system. The key here is to ensure complete coverage; usually 0.3 mil (7.5 µm) of tin are deposited on the traces and the holes. This is a sacrificial layer that is not part of the finished PWB. After final etch the tin is stripped. Table 33.3 describes the operation and control of the tin sulfate bath.

TABLE 33.3 Acid Tin Sulfate
Operation and control

Operating conditions:	
Tin	2 oz/gal
Sulfuric acid	10–12% by volume
Carrier, additives	Replenish based on Ah usage or spectrophotometric analysis
Temperature	65–85°F
Cathode current density	10–30
Current efficiency	100%
Plating rates	7.8 Ah for 1.0 mil/ft^2
Anodes:	
Type	Bars
Composition	Pure tin
Bags	Polypropylene
Hooks	Monel or titanium
Length	Rack length minus 2–3 in
Current density	5–20 A/ft^2

33.4.1.1 Process Controls

33.4.1.1.1 Agitation. A filter pump circulates the solution without allowing air to be introduced. Cathode rod agitation is recommended for thru hole plating.

33.4.1.1.2 Filtration. A 3- to 10-µm polypropylene filter is needed to control excess cloudiness and sludge formation.

33.4.1.1.3 Temperature. Operate at the temperature recommended by the supplier.

33.4.1.1.4 Carbon Treatment. Continuous carbon filtration at room temperature is recommended to remove organic contaminants/buildup.

***33.4.1.2 Common Contaminants*.** These include three groups of contaminants.

- *Organic :* These come from additives and breakdown of resist. The solution may require carbon filtration or treatment; based on its carbon content.
- *Metal:* The effects of metallic contaminants on the plated deposits and the maximum levels allowable are as follows: copper darkness, 5 to 10 ppm; cadmium dullness, 50 ppm; zinc dullness, 50 ppm; nickel streaks, 50 ppm; iron dullness, 50 to 120 ppm; and chromium dullness, 5 ppm. Metallic contaminants may be removed by dummy plating at low current density (2 to 5 ASF).
- *Nonmetal:* The maximum allowable level for the chloride ion is 75 ppm.

33.4.1.3 Solution Controls

- Use electronic grade chemicals to avoid metallic impurities like Cd, Zn, or Fe.
- Maintain the appropriate levels for the organic additives.
- Ensure adequate rinsing after plating.
- Ensure the tin has a visual lustrous finish.

33.4.1.3.1 Bath Control. Stannous sulfate and sulfuric acid are maintained by chemical lab analysis. Additives may be controlled by spectrophotometric analysis, Ah usage, or hull cell.

33.4.1.4 Problems with Tin Electroplating

33.4.1.4.1 Dull Deposits. These are due to an out-of-balance condition of the main solution constituents, that is, low acid (<10 percent), high tin (>3 oz/gal), improper additive levels, contamination by metals or chlorides, or high temperatures (>65°F).

33.4.1.4.2 Peeling Tin. Tin peeling is attributed to low acid concentration (<10 percent) and or organic contamination.

33.4.1.4.3 Slivers. These are caused by overetching. A review of etching practice is indicated, as well as the use of reduced thickness copper foil.

33.4.1.4.4 Pitting. If the substrate is not the cause, check precleaning, solution balance and contaminants, current efficiency, and current densities. High-current densities may cause pitting.

33.5 NICKEL ELECTROPLATING

Nickel plating is used as an undercoat for precious and nonprecious metals. For surfaces such as contacts or tips that are normally subjected to heavy wear, the uses of nickel under a gold plate will greatly increase wear resistance. When used as a barrier layer, nickel is effective in preventing diffusion between copper and other plated metals. Nickel-gold combinations are frequently used as final finishes for soldering, contacting and wire bonding. MIL-STD-275 calls for a low-stress nickel with a minimum thickness of 0.0002 in. Low-stress nickel deposits are generally obtained using

nickel sulfamate baths in conjunction with wetting (antipit) agents. Additives are also used to reduce stress and to improve surface appearance.

33.5.1 Nickel Sulfamate

Nickel sulfamate is commonly used both as an undercoat for through-hole plating and on gold finger tabs.

Conditions given in Table 33.4 are applicable for through-hole and full-board plating.

TABLE 33.4 Nickel Sulfamate
Operation and control

Operating conditions:	
pH	3.5–4.5 (3.8)
Nickel	10–12 oz/gal
As nickel sulfamate	43 oz/gal
Nickel chloride	4 oz/gal
Boric acid	4–6 oz/gal
Additives:	
Brightener	As required
Antipit (Wetter)	As required
Temperature	130 ± 5°F
Cathode current density	20–40 ASF
Anodes:	
Type	Bars or chunks
Composition	Nickel
Purity	Rolled depolarized, cast, or electrolytic; SD chips in titanium basket
Hooks/baskets	Titanium
Bags	Polypro, or Dynel
Length	Rack length minus 3–4 in

33.5.1.1 Process Controls

33.5.1.1.1 pH. With normal operation, pH increases. To lower pH, use sulfamic acid (not sulfuric acid). A decrease in pH signals a problem; anodes should be checked.

33.5.1.1.2 Temperature. The preferred temperature is 125°F. Low temperature may cause stress and high current-density (CD) burning. Higher temperatures decrease the hardness of the nickel deposit.

33.5.1.1.3 Agitation. Solution circulation between panels is achieved through the filter pump and/or cathode rod agitation.

33.5.1.1.4 Filtration. This is done continuously through 5 to 10 µm polypro filter, which is changed periodically based on utilization.

33.5.1.1.5 Deposition Rate. For 0.5 mil, plate 25 to 30 min at 25 A/ft^2. For 0.2 to 0.3 mil, plate 15 min at 25 A/ft^2.

33.5.1.1.6 Common Contaminants

Metals: The following are the maximum allowable metal contaminants: iron, 250 ppm; copper, 10 ppm; chromium, 20 ppm; aluminum, 60 ppm; lead, 3 ppm; zinc, 10 ppm; tin, 10 ppm; and calcium, 0 ppm. These metal contaminants lower the deposition rates and cause nonuniform plating. Copper and lead cause dark, brittle deposits at low CD. Dummy-plate at 3 to 5 A/ft^2. Iron, tin, lead, and calcium cause deposit roughness and stress.

Organics: These cause pitting, brittleness, step plating, and lesser ductility.

Sulfates: These cause solution breakdown and should not be added.

33.5.1.1.7 Carbon Treatment. This process is used to reduce the organic contamination in the electrolyte.

Circulate through a carbon canister for 4 h (more than one canister may be required) or batch-treat to remove organics. The basic six steps to batch-carbon-treat are as follows:

1. Transfer to the treatment tank. Do not adjust pH.
2. Heat to 140°F.
3. Add 3 to 5 lb carbon per 100 gal of solution.
4. Stir 4 h at temperature.
5. Let the solution settle 1 to 2 h.
6. Filter the solution back to plating clean tank.

33.5.1.2 Common Problems. A Hull cell Plated at 2 A for 10 min. with gentle agitation is a useful tool for evaluating the deposit, the condition of the bath and contaminants.

33.5.1.2.1 Visual Observation. The plated metal has a matte, dull finish. Burned deposits are caused by low temperature, high-current density, bath imbalance, and poor agitation. Rough deposits are due to poor filtration, pH out of spec, contamination, or high-current density.

33.5.1.2.2 Pitting. This is caused by low antipit, poor agitation or circulation, boric acid imbalance, or the presence of organics. In testing for antipit, the solution should hold bubble for 5 s in a 3-in wire ring and for less than 5 s in a 5-in ring. In the case of severe pitting, cool to room temperature, add 1 pt/200 gal hydrogen peroxide (35 percent), bubble air, and reheat to 140°F. Carbon-treat the solution to remove additional organics. Adjust pH before restarting.

33.5.1.2.3 Stress. This refers to the cause of deposit cracking. Although low nickel chloride causes poor anode corrosion (a rapid decrease in nickel content), high chloride causes excess stress. To prevent this, maintain pH, current density, and boric acid for control below 10 kpsi.

33.5.1.2.4 Burns. A low concentration of nickel sulfamate causes high-current-density “burns.”

33.5.2 Nickel Sulfate

This is typically plated with an automatic edge connector (tab) plating machine. Table 33.5 gives the operating conditions that apply to these systems. For additional instruction, follow the details in nickel sulfamate section above.

TABLE 33.5 Nickel Sulfate
Operation and control

Operating conditions:	
pH	1.5–4.5
Nickel	15–17 oz/gal
Nickel chloride	2–4 oz/gal (with soluble anodes)
Boric acid	5–7 oz/gal
Stress reducer	As required
Antipit	As required
Temperature	130 ± 5°F
Cathode current density	100–600 A/ft^2
Current efficiency	65%
Anodes:	
Composition	Nickel or platinized titanium

Nickel anodes are preferred in tab plating equipment because the pH and the metal content remain stable. The pH will decrease rapidly when insoluble anodes are used. The pH should be maintained at 1.5 or higher with additions of nickel carbonate. Stress values are higher than in sulfamate baths, with values of about 20 kpsi.

33.6 GOLD ELECTROPLATE

Early PCB technology used gold extensively. In addition to being an excellent resist for etching, gold has good electrical conductivity, tarnish resistance, and solderability after

storage. Gold can produce contact surfaces with low electrical resistance. In spite of its continued advantages, the high cost of gold has restricted its major application to edge connectors (tabs) and selected areas, with occasional plating on pads, holes, and traces (full build). Both hard-alloy and soft, pure gold, are currently used. Plating solutions are acid (pH 3.5 to 5.0) and neutral (pH 6 to 8.5). Both automatic plating machines for edge connectors and manual lines are in use.

33.6.1 Acid Hard Gold

To a large extent, acidic gold solutions are used for compliance to MIL-STD-275, which states that gold shall be in accordance with MIL-G-45204, Type II, Class 1. The minimum thickness shall be 0.000050 in (50 µin); the maximum shall be 0.000100 in. Nonmilitary applications require 25 to 50 µin. A low-stress nickel shall be used between the deposited gold and copper substrate. Deposit hardness and wear resistance are made possible by adding complexes of cobalt, nickel, or iron to the bath makeup. Type II hard gold is not suited for wire bonding. These systems use potassium gold cyanide in an organic acid electrolyte. Automatic plating equipment are being used increasingly because of the enhanced thickness (distribution) control, efficient gold usage, productivity, and quality. A comparison of automatic versus manual plating methods for edge connectors is given in Table 33.6.

TABLE 33.6 Acid Gold-Cobalt Alloy
Operation and control

	Manual	Automatic
Gold content, troy oz/gal	0.9–1.1	1–3
pH	4.2–4.6	4.5–5.0
Cobalt content	800–1000 ppm	800–1200 ppm
Temperature	90–110°F	100–125°F
Solution density	8–15 Be°	12–18 Be°
Replenishment per troy oz gold	8 Ah	6.5 Ah
Current efficiency	50%	60%
Agitation	5 gal/min	50 gal/min
Anode-to-cathode distance	3–5 in	1.4 in
Anodes, composition	Platinized titanium	Platinized titanium
Cathode current density	1–10 A/ft^2	50–100 A/ft^2
Thickness	40 ± 10 µin	40 ± 2 µin
Deposition rate for 40 µin	3–6 min	0.3–0.6 min
Deposition composition	99.8% gold, 0.2% cobalt	99.8% gold, 0.2% cobalt
Hardness	150 Knoop	150 Knoop

Gold solution: Maximum allowed metal contaminants

Metal	Maximum ppm	Metal	Maximum ppm
Lead	10	Iron	100
Silver	5	Tin	300
Chromium	5	Nickel	300–3000
Copper	50		

33.6.1.1 Process Controls

33.6.1.1.1 Analysis. Gold content, pH, and density should be maintained at optimum values. Operation at very low gold content causes early bath breakdowns with loss of properties, less current efficiency, and less cost savings. The pH is raised by using potassium hydroxide and is lowered with acid salts. Solution conductivity is controlled by density, which is adjusted with conductivity salts. Hull cell is not recommended for this purpose.

33.6.1.1.2 Anodes. Platinized titanium should be replaced when operating voltages are excessive or when thick coatings develop on the anode surfaces.

33.6.1.1.3 Recovery. Plating solutions should be replaced when contaminated, when plating rates decrease, or after about 10 total gold content turnovers.

33.6.1.1.4 Problems. Difficulties can be controlled by proper gold bath and equipment maintenance. Some typical situations follow:

Discolored deposit: This may be due to low brightener; to metal contaminants such as lead, low pH, low density, or organic contaminations; or to leaking from tape. Gold plate is stripped to evaluate nickel. For these problems, first try to lower the pH, raise the density, or increase the brightener before replacing the bath or using decreased current densities.

Gold peeling from nickel: This is generally due to inadequate solder stripping, leaky tape, or poor nickel activation. Methods to increase nickel activation include increasing acid strength after nickel plating and using a fluoride activator, or the use of a gold strike. A gold strike that is compatible with gold plate and has low metal content and low pH is available. Its main purpose is to maintain adhesion to the nickel substrate.

Wide thickness range: To improve thickness distribution of the gold deposit; improve the solution movement between panels; clean, adjust, or replace anodes; and adjust or replace the solution.

Low deposition rate: This is characterized by excessive gassing and low efficiencies. To correct this condition, adjust solution parameters and check for contaminants such as chromium.

Pitting: Strip gold and evaluate the underlying nickel by cross-sectioning.

Resist breakdown: Low current efficiencies cause this condition. Use solvent-soluble screened or dry film for best results.

33.6.1.2 Pure 24-Karat Gold. High-purity 99.99 percent gold processes are used for boards designed for semiconductor chip (die) attachment, wire bonding, and plating solder (leaded) glass devices, for their solderability and weldability. These qualities comply with Types I and III of MIL-G-45204. The processes are neutral (pH 6 to 8.5) or acid (pH 3 to 6).

Table 33.7 gives typical conditions for a neutral bath.

TABLE 33.7 Neutral Pure Gold
Operation and control

Gold content	0.9–1.5 troy oz/gal
pH	6.0–7.0
Temperature	150°F
Agitation	Vigorous
Solution density	12–15 Be
Current efficient	90–95%
Cathode current density	1–10 A/ft^2
Deposition rate @5 ASF	100 µin in 8 min
Deposit composition	99.99% + gold
Hardness	60–90 Knoop

33.6.2 Alkaline, Noncyanide Gold

Various processes for alloy and pure gold deposits are available. Solutions are based on sulfite gold complexes and arsenic additives and operate at a pH of 8.5 to 10.0. A decision to use this process is based primarily on the need for uniformity (leveling), hardness (180 Knoop), purity, reflectivity, and ductility. PC board use is limited to body plating, since wear characteristics of the sulfite-gold are not suitable for edge connector applications. The microelectronics industry uses these processes for reasons of safety and gold purity. Semiconductor chip attachment, wire bonding, and gold plating on semiconductors are possible applications and are enhanced by using plating without metallic additives.

33.6.3 Gold Plate Tests

Several routine in-process and final quality control tests are performed on gold:

- *Thickness:* Techniques are based on beta-ray backscattering and x-ray fluorescence. Thickness and area sensitivity are as low as 1 µin with 5-mil pads.
- *Adhesion:* Standard testing involves a tape pull test.
- *Porosity:* Tests involve nitric acid vapor and electrographics.
- *Purity:* Lead is a common impurity that must be controlled to <0.1 percent. Other tests included discoloration by heating, electrical contact, and wear resistance.

CHAPTER 34
DIRECT PLATING

Hayao Nakahara
N.T. Information Ltd., Huntington, New York

34.1 DIRECT METALLIZATION TECHNOLOGY[a]

For 40 years the PTH process of choice has been palladium followed by electroless copper, but there have been at least 12 DMT processes challenging that established process, with several hundred installations, a significant percentage of the total number of PCB shops. The basic idea for the palladium systems dates back to the Radovsky patent of 1963,[1] which claimed a method of using an electrically nonconductive film of palladium in a semicolloidal form to directly metallize through holes in printed circuit boards. Radovsky's invention was never commercialized. The basic idea for the carbon/graphite systems dates back to the very early days of eyelet boards when Photocircuits was experimenting with graphite, silver, and other media to turn their single-sided PCBs into reliable double-sided boards.

34.1.1 Direct Metallization Technology Overview

From the many media and technical variations, some common elements have evolved.

34.1.1.1 DMT Common Elements. There are two elements common to all DMT:

1. Holes must be conditioned more specifically and thoroughly than for electroless copper.
2. Conductive media must be removed from the copper foil in a majority of the techniques (an exception is DMS-E).

It is understood that additional desmear steps are necessary or advisable when processing multilayer PCBs. Common elements to all horizontal conveyorized DMT systems are:

- Throughput is typically 6 to 15 min for a panel, with the next panel following 1 in behind
- Tremendous economies in rinse water use
- Lower consumption of chemicals
- Fewer steps than in its vertical mode
- Panel-to-panel uniformity

Many DMT processes work better than electroless copper on substrates with “difficult” resin systems such as PTFE, cyanate ester, or polyimide.

34.1.1.2 Direct Metallization Categories. DMT falls into four broad categories:

1. Palladium-based systems
2. Carbon or graphite systems
3. Conductive polymer systems

4. Other methods

34.1.2 Palladium-Based Systems

34.1.2.1 Palladium/Tin Activator with Flash Electoplating. EE-1,[2] the first commercialized direct metallization technique was invented in 1982 at Photocircuits and PCK. It uses a palladium/tin activator followed by mandatory flash electroplating. The flash-plating bath contains a polyoxyethylene compound to inhibit the deposition of copper on the foil surface without inhibiting deposition on palladium sites on nonconductive surfaces (holes, edges, substrate). Deposition occurs by propagation from the copper foil and grows epitaxially along the activated surface of the hole. Coverage takes about 5 to 6 min. This flash is pattern- or panel-plated subsequently to full thickness in any electroplating bath. Microetching is incorporated in the accelerator to remove palladium sites and nail heads from innerlayers. A special cleaner/conditioner is used. This process has never been adapted to horizontal equipment. (See Fig. 34.1.)

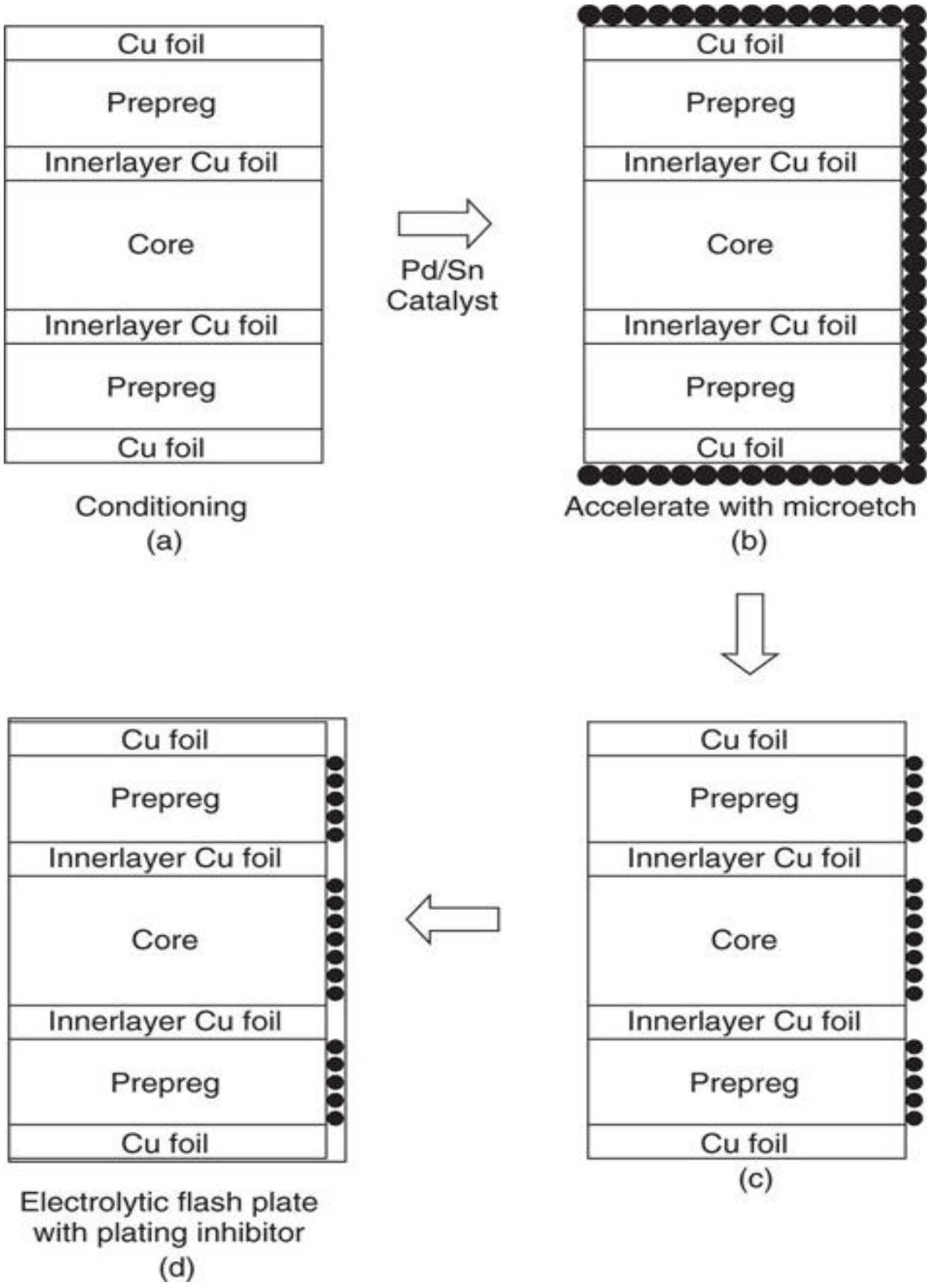
Cu foil
Prepreg
Innerlayer Cu foil
Core
Innerlayer Cu foil
Prepreg
Cu foil
Conditioning
(a)
Pd/Sn
Catalyst
Cu foil
Prepreg
Innerlayer Cu foil
Core
Innerlayer Cu foil
Prepreg
Cu foil
Accelerate with microetch
(b)
Cu foil
Prepreg
Innerlayer Cu foil
Core
Innerlayer Cu foil
Prepreg
Cu foil
(c)
Cu foil
Prepreg
Innerlayer Cu foil
Core
Innerlayer Cu foil
Prepreg
Cu foil
Electrolytic flash plate
with plating inhibitor
(d)

FIGURE 34.1 Principle of EE-1 process: (*a*) conditioning—making glass and epoxy surfaces receptive of Pd catalyst sites; (*b*) palladium catalyst sites; (*c*) acceleration removes excess tin and microetch removes catalysts from the surface of Cu foil; (*d*) flush Cu plate coppers enter surface in drilling hole walls.

34.1.2.2 Palladium/Tin Activator with Vanillin. DPS[3] was invented in Japan in the late ’80s. This method uses a palladium/tin activator with vanillin, followed by pattern or panel electroplating. It employs a special cleaner/conditioner and a carbonate accelerator. The three key solutions—cleaner/conditioner, activator, and accelerator—all operate at elevated temperatures. DPS has recently been adapted to horizontal equipment, but works well in the vertical mode, both manual and automatic. Following the last step, the *Setter*, DPS yields a stable, grayish conductive palladium film in the holes. It is believed that the cleaner/conditioner slightly solubilizes the activator, attracting it to the nonconductive surface, and that the vanillin lines up the palladium molecules, and directs them towards the work, hence giving lower electrical resistance and better adhesion to nonconductive surfaces. It is also claimed that there is little palladium/tin left on the copper foil, so it is easily soft-etched away in the normal electroplating preplate cycle. (See Fig. 34.2.) DPS was the first DMT process to suggest an Ω meter as the standard quality assurance (QA) tool.

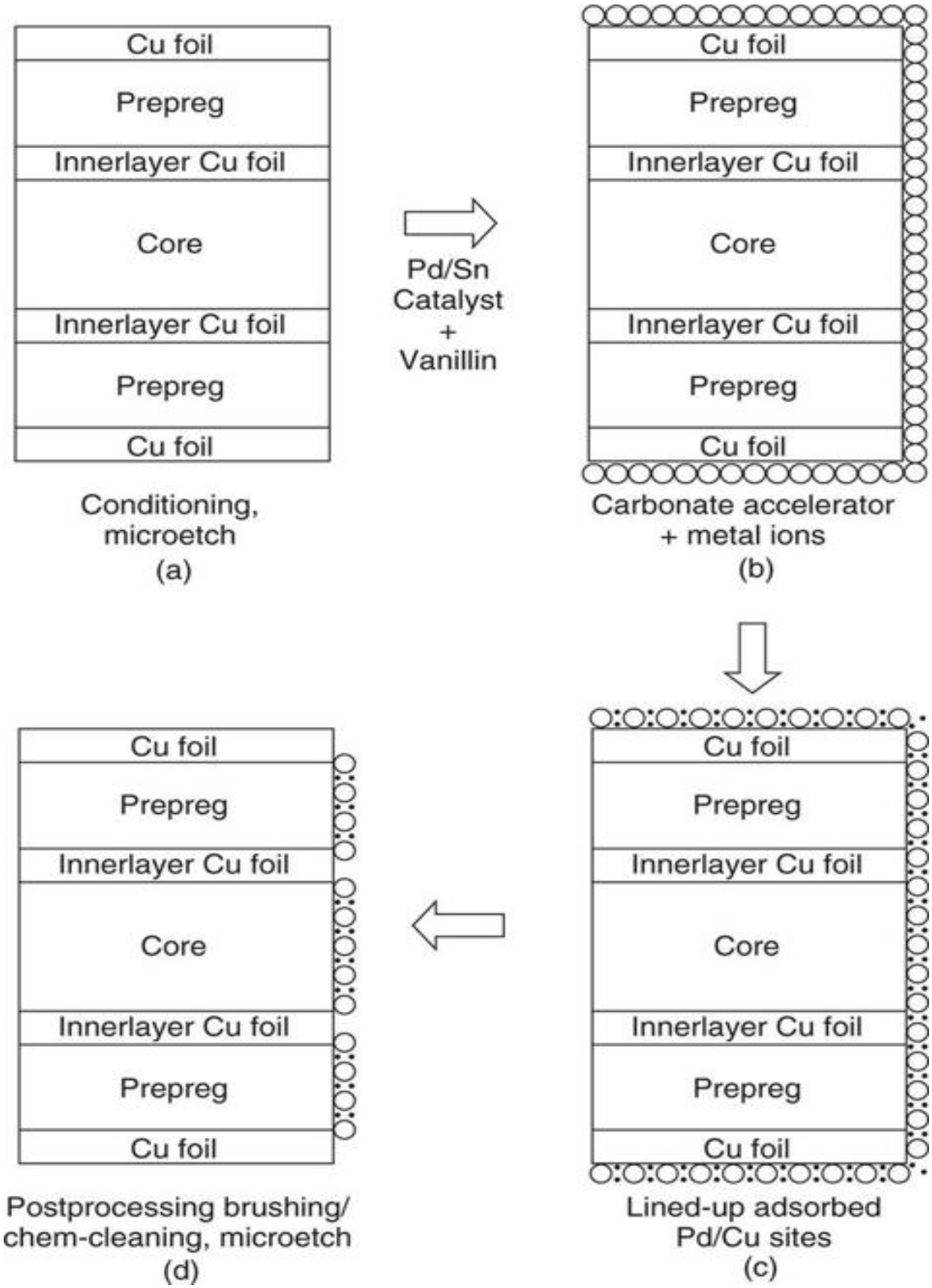
Cu foil
Prepreg
Innerlayer Cu foil
Core
Innerlayer Cu foil
Prepreg
Cu foil
Conditioning, microetch
(a)
Pd/Sn Catalyst + Vanillin
Carbonate accelerator + metal ions
(b)
Lined-up adsorbed Pd/Cu sites
(c)
Postprocessing brushing/ chem-cleaning, microetch
(d)

FIGURE 34.2 Principle of the DPS process: (*a*) conditioning for receptive surface; (*b*) catalysts adhering to the surface; (*c*) stronger adhesion; (*d*) ready to plate.

34.1.2.3 Converting Palladium to Palladium Sulfide.

Crimson,[4] invented by Shipley, employs a conversion step after the activator where palladium is changed to palladium sulfide, which is claimed to be more conductive for subsequent electrolytic copper plating. The *enhancer* stabilizes the conductive film so that it is chemically resistant to imaging steps. The *stabilizer* neutralizes residues from the enhancer, thereby preventing contamination of subsequent steps. The *microetch* selectively removes activator from copper surfaces to achieve optimum copper-to-copper bond and reliable dry film adhesion. The process works best in conveyorized horizontal equipment and can be followed by pattern or panel electroplating. (See Fig. 34.3.)

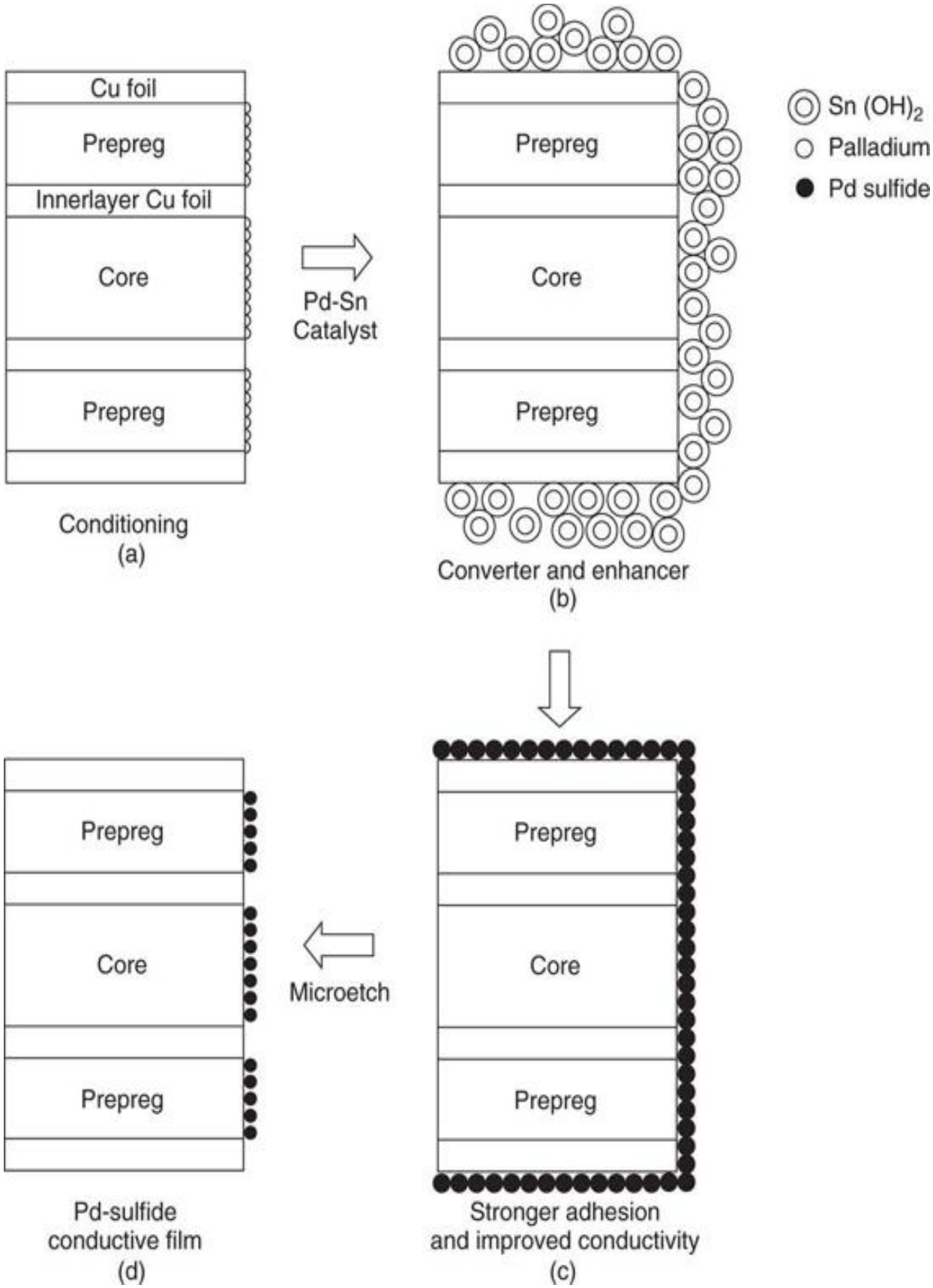
Cu foil
Prepreg
Innerlayer Cu foil
Core
Prepreg
Conditioning
(a)
Pd-Sn
Catalyst
Prepreg
Core
Prepreg
Converter and enhancer
(b)
Sn (OH)2
Palladium
Pd sulfide
Prepreg
Core
Prepreg
Stronger adhesion
and improved conductivity
(c)
Microetch
Prepreg
Core
Prepreg
Pd-sulfide
conductive film
(d)

FIGURE 34.3 Principle of Crimson process: (*a*) conditioning; (*b*) colloidal Pd sites adhered to the surface; (*c*) Pd-sulfide (stronger adhesion of Pd catalysts); (*d*) microetch to remove Pd from Cu surface for better Cu-Cu adhesion.

34.1.2.4 Process Variations. ABC,[5] invented in Israel by Holtzman et al., is similar to EE-1. It has been adapted to conveyorized horizontal equipment, but must be followed by a flash electroplating in a proprietary bath.

Conductron, from LeaRonal, is similar to DPS with the addition of a special cleaner/conditioner and a glass-etch step. It has been adapted to conveyorized horizontal equipment and can be followed by pattern or panel electroplating.

Envision DPS, from Enthone-OMI, and Connect, from M & T (now Atotech), are fairly similar to each other, and to DPS, though each has a specific cleaner/conditioner and modified accelerator. No adaptation has been made to horizontal processing. Both processes can be followed by pattern or panel electroplating.

Neopact,[6] from Atotech, uses a tin-free palladium activator in colloidal form. The subsequent postdip removes the protective organic polymer from the palladium, leaving it exposed and with increased conductivity. It has been adapted to conveyorized horizontal equipment, works well in vertical, and can be followed by pattern or panel electroplating. (See Fig. 34.4.)

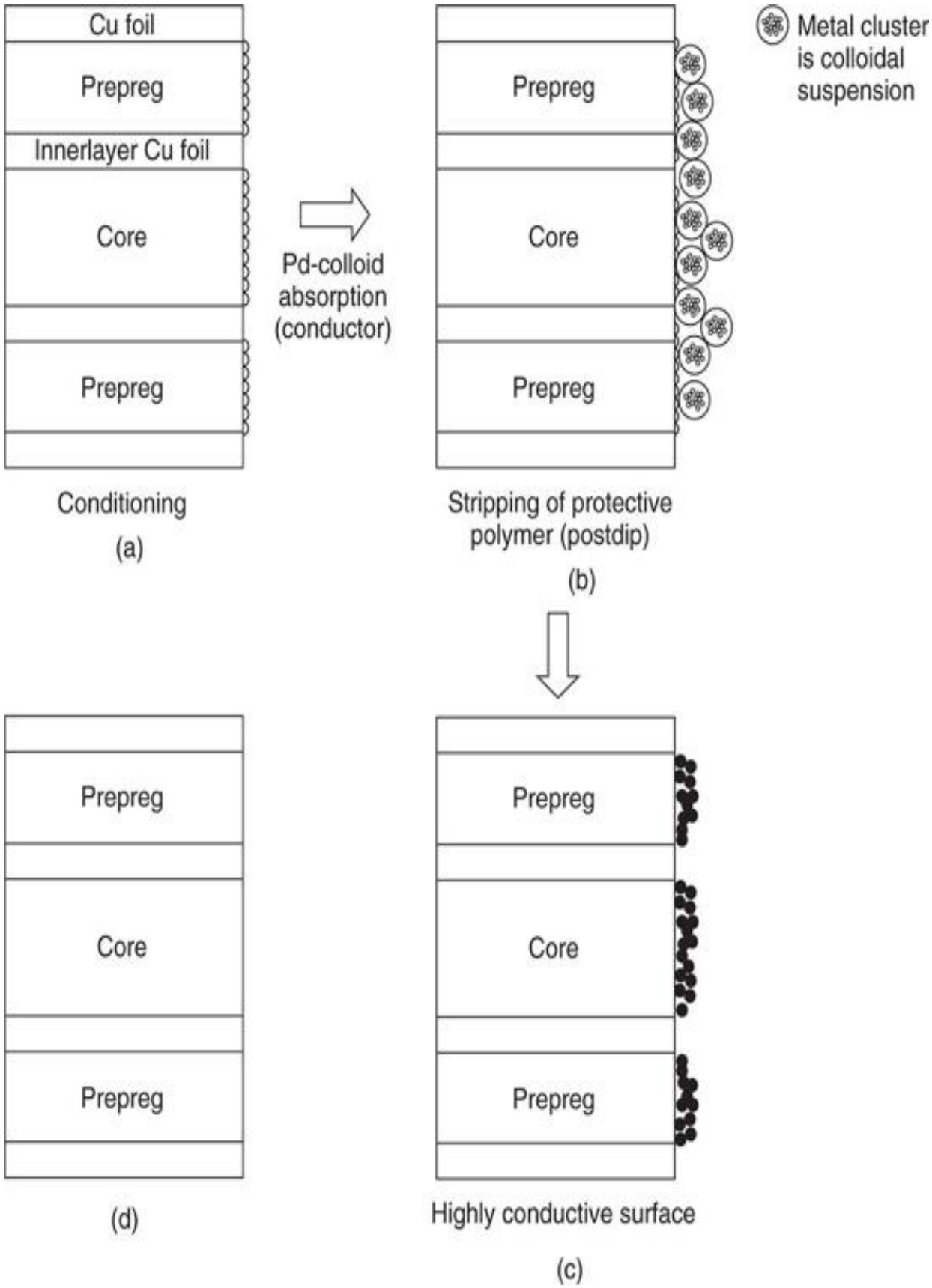
Cu foil
Prepreg
Innerlayer Cu foil
Core
Prepreg
Pd-colloid absorption (conductor)
Prepreg
Core
Prepreg
Metal cluster is colloidal suspension
Conditioning
(a)
Stripping of protective polymer (postdip)
(b)
Prepreg
Core
Prepreg
Highly conductive surface
(c)
Prepreg
Core
Prepreg
(d)

FIGURE 34.4 Principle of Neopact process: (*a*) conditioning surface; (*b*) metal cluster in colloidal suspension adhered to the hole wall; (*c*) stripped Pd adhering to the hole wall; (*d*) Cu reduced.

34.1.3 Carbon/Graphite Systems

34.1.3.1 Carbon Suspensions. Black Hole,[7] the second direct metallization technique, was patented by Dr. Carl Minten in 1988 and pioneered by Olin Hunt, who sold their technology to MacDermid in 1991. MacDermid improved the process considerably and called it Black Hole II. Instead of palladium activator, Black Hole II uses carbon suspensions as its conductive medium. Polyelectrolyte conditioned nonconductive surfaces absorb carbon sites, and they "line up" after heating. To ensure sufficient conductivity, the carbon treatment is performed twice. Residues of carbon sites must be removed from the copper foil surface by a microcleaning step. Black Hole II has been well adapted to conveyorized horizontal equipment and can be followed by pattern or panel electroplating. (See Fig. 34.5.)

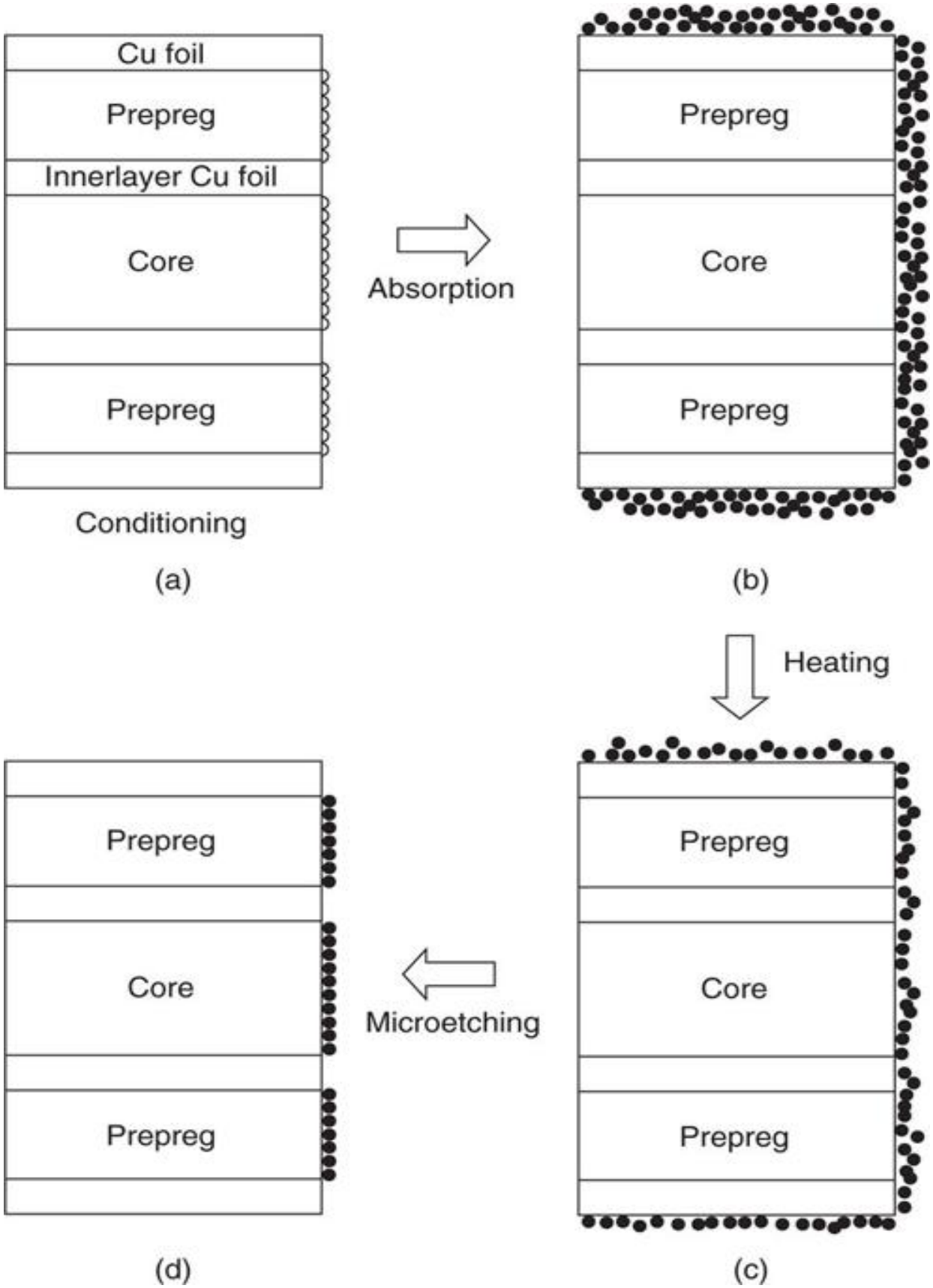
Cu foil
Prepreg
Innerlayer Cu foil
Core
Prepreg
Conditioning
(a)
Absorption
Prepreg
Core
Prepreg
(b)
Heating
Prepreg
Core
Prepreg
(c)
Microetching
Prepreg
Core
Prepreg
(d)

FIGURE 34.5 Principle of carbon/graphite process: (*a*) conditioning; (*b*) carbon particles adhered to the surface; (*c*) dense more conductive carbon conducting film; (*d*) removal of conduction film from Cu surface resulting in stronger Cu-Cu interface.

34.1.3.2 Graphite. Shadow[8] is from Electrochemicals (division of LaPorte Industries, UK, then OMG and now Platform Speciality) and uses graphite as its conductive medium. The process sequence of Shadow is very simple and involves fewer steps than most DMT. Electrochemicals and one of their fabricators, Eidschun Engineering, made the breakthrough in inexpensive, compact, conveyorized horizontal equipment, and the Shadow process is well adapted to this mode. It can be followed by pattern or panel electroplating.

34.1.4 Conductive Polymer Systems

34.1.4.1 DMS-E. DMS-E[9] from Blasberg is a second-generation DMS-2 process with which they pioneered in this field. DMS-1 was similar to EE-1. After microetch and conditioning, a potassium permanganate solution forms a manganese dioxide coating in the holes which acts as an oxidizing agent during subsequent synthesis reaction. In the catalyzing step, an EDT[b] monomer bath wets the manganese dioxide surfaces especially well. During the sulfuric acid fixation step, a spontaneous oxidative polarization takes place, forming a black conductive poly-EDT film on the nonconductive areas of the PCB. This technique is very suitable for use in conveyorized, horizontal equipment, since the oxidative conditioning step is very hot (80 to 90°C), and there are solvents involved. It can be followed by pattern or panel electroplating. (See Fig. 34.6.)

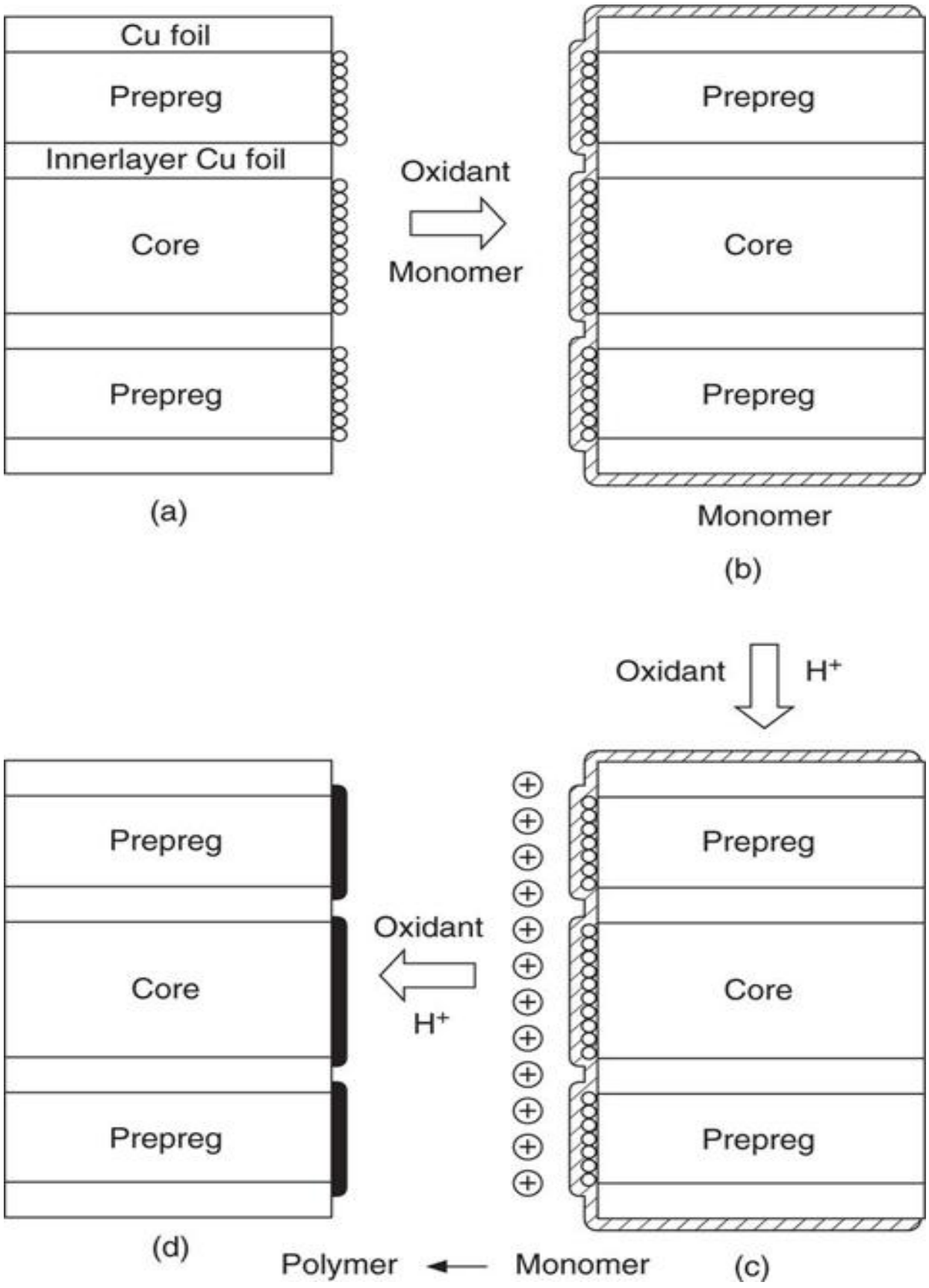
Cu foil
Prepreg
Innerlayer Cu foil
Core
Prepreg
(a)
Oxidant
Monomer
Prepreg
Core
Prepreg
Monomer
(b)
Oxidant
H+
Prepreg
Core
Prepreg
Oxidant
H+
Prepreg
Core
Prepreg
(d)
Polymer
Monomer
(c)

FIGURE 34.6 Principle of conductive polymer process: (*a*) conditioning; (*b*) monomer created on the surface; (*c*) oxidant reduces monomer to polymer yielding highly conductive surface; (*d*) further improved conductive surface.

34.1.4.2 Compact CP. Compact CP[10] was developed by Atotech in 1987 and is essentially similar to DMS-E, except that it combines the catalyzing and fixation steps, it uses an acid permanganate, and the conductive film is a polypyrrole. The technique is very suitable for use in conveyorized, horizontal equipment. It can be followed by pattern or panel electroplating.

34.1.5 Other Methods

There are several other novel ways to metallize holes in PCBs, such as Phoenix and EBP from MacDermid, Schlötoposit from Schlötter. There are conductive ink and laser scribing/filling techniques; there are sputtering and sequential plating, to name a few, but they do not fall within the scope of this chapter.

34.1.6 Comparative Steps of DMT Process

34.1.6.1 DMT.1: Palladium-Based Systems. All vertical modes only, for comparison purposes, are shown in Table 34.1.

TABLE 34.1 DMT.
Palladium-based systems—all vertical mode only

EE-1	DPS	Crimson	ABC	Conductron	Envision DPS	Neopact
Cleaner conditioner	Cleaner conditioner	Cleaner conditioner	Cleaner conditioner etch	Glass conditioner	Conditioner	Etch cleaner
Rinse	Rinse	Rinse	Rinse	Rinse	Rinse	Rinse
Microetch	Microetch	Predip	Activator	Cleaner conditioner	Carrier	Conditioner
Rinse	Rinse	Activator	Rinse	Rinse	Activator	Rinse
Predip	Predip	Rinse	Salt remover	Microetch	Rinse	Predip
Activator	Activator	Accelerator	Rinse	Rinse	Generator	Conductor
Rinse	Rinse	Rinse	Dry	Predip	Rinse	Rinse
Accelerator	Accelerator	Enhancer	Microetch	Activator	Stabilizer	Postdip
Rinse	Rinse	Rinse	Rinse	Rinse	Rinse	Rinse
EE-1 electrolytic flash	Setter	Microetch	Reactivator	Accelerator	Microetch	Dry
Rinse	Rinse	Rinse	Rinse	Rinse	Rinse	
Dry	Dry	Dry	ABC electrolytic flash	Acid Dip	Dry	
			Rinse	Rinse		
			Dry	Dry		

34.1.6.2 DMT.2: Carbon/Graphite Systems—Conveyorized Horizontal.

Conveyorized horizontal systems are shown in Table 34.2.

TABLE 34.2 DMT.2
Carbon/graphite systems—conveyorized horizontal

Black Hole II	Shadow
Cleaner	Cleaner conditioner
Rinse	Rinse
Black Hole I	Shadow bath
Dry	Heated dry
Rinse	Inspection chamber
Condition	Microetch
Rinse	Rinse
Black Hole II	Antitarnish
Heated dry	Dry
Microclean	
Rinse	
Antitarnish	
Rinse	
Dry	

34.1.6.3 DMT.3: Conductive Polymer Systems.

Conveyorized, horizontal systems with optional electrolytic flash are shown in Table 34.3.

TABLE 34.3 DMT.3
Conductive polymer systems—conveyorized, horizontal, shown with optional electrolytic flash

DMS-E	Compact CP
Microetch	Microetch
Rinse	Rinse
Conditioner	Cleaner/conditioner
Rinse	Rinse
Oxidative conditioning	Permanganate
Rinse	Rinse
Catalyzing	Polyconductor
Fixation	Rinse
Rinse	Soft-etch
Acid dip	Rinse
Electrolytic copper	Acid dip
Rinse	Electrolytic copper
Dry	Rinse
	Dry

34.1.7 Horizontal Process Equipment for DMT

Although many DMTs fit easily into existing electroless copper lines, whether manual or automatic, and perform well in a vertical mode, DMT is becoming inextricably linked to horizontal processing in a conveyorized machine. Like so many inventions, necessity was its mother. Certain DMT processes are marginal in the vertical/basket mode, and handling each panel individually was the only solution. The advent of compact and inexpensive horizontal DMT equipment has been a catalyst. Although Atotech pioneered horizontal electroplating equipment with their Uniplate system, until the development of horizontal DMT machines it was not feasible to engineer a horizontal PTH machine. Now, however, for those who want only flash plating, or even full electroplating, the entire process—both PTH and galvanic—may be horizontal, conveyorized, and automated with the advantages of reduced chemical consumption; radically reduced use of rinse water; panel-to-panel uniformity, reliability, and quality; reduction in operating personnel; reduction of handling; a fully enclosed operating environment; and JIT delivery. Stackers/accumulators further minimize handling and optimize efficiency.

34.1.8 DMT Process Issues

Anything brand new experiences some “teething problems” at the beginning, and DMT is no different. But most of the processes referred to in this chapter are in at least their second generation and some are already in their third, so there are no serious contraindications to the use of DMT. However, there are a few caveats:

1. Esoteric base material does not run well with all DMT.
2. Not all DMT performs as well in the vertical mode as in the horizontal.
3. Certain DMT is better suited to the rigors of multilayer production.

4. Some perform better than others with very small holes.
5. Some processes are cleaner than others.
6. Certain DMT is more sensitive than electroless copper to organic contamination in electrolytic copper plating.
7. Rinsing is important, and some DMT needs special rinsing.
8. Rework is simple in most DMT, but it can be abused, i.e., it changes the cost structure.
9. Quality assurance tools for DMT (how do you know that holes will plate void-free?) are being developed, but at the moment, the only absolutely certain method is to flash electroplate, because, unlike electroless copper, there is not much to see in the hole after DMT.
10. Some DMT analyses and operating controls are rudimentary.

34.1.9 DMT Process Summary

Strong ecological and health reasons will drive the use of DMT for the manufacture of PTH boards. Since the cost of PTH metallization constitutes only 2 to 3 percent, at most, of the total process cost of a PCB, the direct saving resulting from DMT is very small. However, the fringe benefits of this technology are rather significant: water conservation, no noxious chemicals, minimal panel handling, reduced waste treatment, lower labor costs, fewer rejects, etc.

34.2 REFERENCES

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6. Stamp, et al. (Atotech), PCT WO 93/17153, September 1993.
7. Minten, et al. (MacDermid), U.S. Patent 4,724,005, February 1988.
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10. Bressel, et al., U.S. Patent 5,183,552, 1993.

[a] All proprietary names are trademarked by their respective owners.

[b] EDT = 3,4 Ethylendioxythiophene.

CHAPTER 35

PRINTED CIRCUIT BOARD SURFACE FINISHES

George Milad

Uyemura International Corporation, Southington, Connecticut

35.1 INTRODUCTION

35.1.1 Purpose and Functions of Surface Finishes

The printed circuit board (PCB) conductor surface finish is a critical element in the formation of the interface between the component and the interconnection circuitry. As its most essential function, the final finish process is intended to provide exposed copper circuitry with a protective coating in order to preserve solderability. In addition certain surface finishes provide a suitable wire bonding surface as well as an electrical contacting surface. Perhaps no other step in the PCB manufacturing process has undergone more change in the era of surface mount manufacturing than the final finish chemical process. A wide variety of functional,

environmental, engineering, cost, and productivity have contributed to this frequent change.

35.1.2 The Impact of Lead-Free Manufacturing

The impact of lead-free manufacturing, as a result of the Waste Electrical and Electronic Equipment (WEEE) directive and Restriction on Hazardous Substances (RoHS), has changed surface finish specifications for PCBs and the soldering of those surfaces at assembly. Lead-free assembly has changed just about every aspect of the surface finish technology. The elimination of lead (Pb) in most designs has rendered the standard surface finish hot air solder level (HASL) increasingly obsolete. At assembly, the use of new solder alloys affects the compatibility of the finishes with the metallurgy of the final solder joint. Many of the assembly issues related to surface finishes, such as surface-mount technology (SMT) pad wettability, plated through hole (PTH) fill, and voiding are exacerbated by the Pb-free assembly process. Finally, the higher temperature of Pb-free soldering has a major impact on the shelf-life and solderability of the Pb-free finishes.

35.1.3 Technology Drivers

Each company in the manufacturing supply chain has needs specific to its manufacturing step. The methods used to achieve these goals have evolved with developments in PCB technology. Historically, technicians were able to solder components directly to copper using very active fluxes. When PCBs were first made in large production quantities, chemists devised ways to protect the copper using metal or organic coatings. Electroplated tin-lead became a popular

coating as a metallic layer that could be subsequently reflowed. Design changes forced the era of solder mask over bare copper (SMOBC). With SMOBC, reflowed plated tin-lead was no longer possible because the tin-lead liquefies under the soldermask during the soldering process. HASL, the successor to plated tin-lead, became the surface finish of choice worldwide.

Increasing PCB circuit density and the need for co-planarity, inspired the reemergence of organic coatings, such as organic solderability preservatives (OSPs) and metallic layers such as electroless nickel/immersion gold (ENIG), immersion silver and immersion tin. For the highest functionality electroless nickel electroless palladium and immersion gold ENEPIG offers an even better alternative.

The environmental initiative to eliminate ozone-depleting chemicals led to the next change in surface finish preference. Use of no-clean assembly operations prompted a decline in OSP and an increase in metallic finishes.

35.1.4 Fabrication Requirements

The company producing the bare printed circuit board––that is, the PCB fabricator––has needs that are specific to that business, as follows:

- Inexpensive processing equipment and high throughput
- Electrically testable surface
- No attack on the soldermask
- No toxic chemicals (waste should be easily treated)
- Availability of technical service from supplier
- Reworkability
- Measurable performance
- No sensitivity to poor handling
- Long shelf-life

- Specified by most original equipment manufacturer (OEM) customers

35.1.5 Assembly Requirements

The assembly engineers, whether contract Electronics Manufacturing Services (EMS) provider, or independent original design manufacturer (ODM), have requirements that are very different from those of the PWB fabrication customer:

- Flat surface for stenciling paste
- Low contact resistance for in-circuit test (ICT)
- Tolerance for paste misprint cleaning
- Long incoming shelf-life (more than 1 year)
- Long mid-assembly shelf-life (more than 2 weeks)
- Compatibility with all pastes and fluxes
- Capability of bonding with Al and/or Au wire
- The ability to be visually inspected
- Ease of handling
- Excellent and predictable wettability
- Fiducial recognition
- No warp and twist of the PCB
- Good compliant pin and connector contacts
- Good Pb-free soldering with no need for nitrogen
- No solder bridging or plugged holes

35.1.6 OEM Requirements

The original equipment manufacturer has the following additional requirements:

- Best solder joint reliability; strong intermetallic

- Minimum impact on cost of bare board
- Corrosion resistance in uncontrolled field environments
- Usefulness as an electrical test point and EMI shield
- Functionality as a touchpad/keypad contact
- Good electrical performance of high-speed signals
- Adherence to industry specifications
- Complete documentation from the chemical supplier
- Established supply base of installed fabricators
- Audited fabricators

35.2 PWB SURFACE FINISHES

35.2.1 Surface Finishes Available in the PCB Industry

- HASL
- Reflowed tin-lead
- ENIG
- ENEPIG
- OSP
- Immersion silver
- Immersion tin
- Electroless palladium (Pd)
- Electrolytic nickel/electrolytic gold
- Electroless gold
- Direct immersion gold

Table 35.1 shows the common finishes and their typical thicknesses.

TABLE 35.1 Common Surface Finish Options with Typical Thickness

PCB Surface Finish		Typical Thickness
Hot air solder level		2–40 µm (80–1600 µin)
Organic solderability preservative (OSP)		0.1–0.6 µm (4–24 µin)
Electroless nickel/immersion gold (ENIG)	Nickel:	3–6 µm (120–240 µin)
	Gold:	0.04–0.12 µm (1–3 µin)
Electroless Ni/electroless Pd/immersion gold (ENEPIG)	Nickel:	3–6 µm (120–240 µin)
	Palladium:	0.08–0.3 µm (2 – 12µin)
	Gold:	0.04–0.12 µm (1–3 µin)
Immersion silver		0.1–0.4 µm (4–16 µin)
Immersion tin		0.6–1.2 µm (24–48 µin)

35.3 HOT AIR SOLDER LEVEL

Hot air solder level (HASL or HAL) is the process of immersing a circuit board into molten solder, immediately followed by blowing the excess molten solder out of the holes using hot air under high pressure. For the vast majority of HASL applications, the solder alloy is tin-lead. For Pb-free applications, the main alloys include tin-copper, tin-silver-copper, tin-copper-nickel, and tin-copper-nickel-germanium alloys. The thickness and texture of the HASL surface result from the surface tension of molten solder. As such, the thickness varies from 2 to 20 µm or more.

HASL boards demonstrate excellent shelf life, solderability protection, and resistance to poor handling, but they do tend to have higher levels of residual ions left over from fluxing. The HASL operation forms an intermetallic with copper circuitry at the PCB shop.

This extra thermal step, with the associated loss in copper, is a concern for Pb-free assemblies. Expansion of the PCB substrate at high temperatures can warp and/or twist the board. The dimensional movement, along with uneven pad flatness and plugged vias, makes assembling dense circuitry (less than 0.5 mm pitch) difficult or impossible. The worldwide decline of HASL is partly due to assembly concerns and partly due to Pb restrictions.

35.3.1 Fabrication Process

HASL can be applied in vertical or horizontal equipment. As a pretreatment, the copper is cleaned, microetched, and fluxed. It is common for the HASL pretreatment steps to be carried out in conveyorized equipment, and then the panel to be transferred to a vertical machine that dips the individual panel into molten solder. As the panel is raised, air knives blow off excess solder. Surface finishing engineers must be aware of safety concerns, such as exposure to Pb and the possibility of equipment fires. Newer horizontal conveyorized equipment provide a safer environment as well as a more planar surface.

To handle the very high temperatures of the molten alloy, equipment is manufactured from stainless steel, titanium, and other alloys. Aggressive rinsing is needed to remove flux residues, as the HASL process uses aggressive acid fluxes as compared to no clean fluxes used in other surface finish processes.

35.3.2 Benefits and Limitations

Benefits

- Inexpensive as compared to other finishes
- Forms the more reliable Cu/Sn intermetallic solder joint

- Widely available

Limitations

- It is a nonplanar finish
- Increases the overall thickness of the IMC
- May form solder bridging (fine pitch)
- High temperature immersion may damage the PWB

35.4 ELECTROLESS NICKEL IMMERSION GOLD

Electroless nickel immersion gold (ENIG) is an electroless nickel layer capped with a thin layer of immersion gold. It is a multifunctional surface finish, applicable to soldering, aluminum and copper wedge wire bonding, press fit connections, and as a contact surface. The immersion gold protects the underlying nickel from oxidation/passivation over its intended life.

The nickel layer forms a diffusion barrier preventing the diffusion of the underlying copper into the gold overcoat. The nickel also strengthens the thru hole by acting as a rivet. In addition the nickel protects the copper from dissolution into molten solder at assembly.

Chemically, gold is the ideal element for the external coating of PCBs. Gold does not form an oxide, so it is virtually unaffected by temperature and storage conditions that might reduce the shelf-life of other finishes. In addition, gold dissolves readily into solder, promoting superior wettability to the nickel substrate.

35.4.1 IPC-4552 ENIG Specification (2002)

The ENIG IPC-4552 Specification was issued in 2002, at that time the idea of lead free (LF) had not taken hold in the industry and tin lead was the dominant assembly solder in use.

For thickness IPC-4552 stated:

> The electroless nickel thickness shall be 3 to 6 µm [118.1 to 236.2 µin].
>
> The minimum immersion gold thickness shall be 0.05 [1.97 µin] at four sigma (standard deviation) below the mean; the typical range is 0.075 to 0.125 µm [2.955 to 4.925 µin]. There was no upper limit set.

No thickness upper limit was set for the immersion gold. The stated “typical range” was erroneously interpreted as the upper and lower limits of the specification.

The IPC ENIG Specification 4552 is presently under revision. The reason for the revision is related to present practices that expect immersion gold thickness in excess of 3 µin. IPC 4552 Rev A is presently in its final draft format awaiting peer review before issuance. The IPC4552 Rev A draft sets limits for immersion gold with a minimum of 1.6 µins to a maximum of 4.0 µins. The revision also contains a nickel corrosion (Black Pad) chart. The chart shows examples of acceptable corrosion, debatable corrosion and rejectable corrosion.

35.4.2 Chemical Definitions

35.4.2.1 Electroless Process. This chemical process promotes sustained deposition of a metal or metal alloy onto the PCB surface through an oxidation-reduction chemical reaction, without the application of an external electrical potential. Reducing agents, such as sodium hypophosphite or sodium formate, react at catalytic surfaces to release

electrons, which immediately reduce the positively charged metal ions (e.g., nickel ions in ENIG and ENEPIG and palladium ions in ENEPIG), promoting their deposition onto the PCB.

This type of reaction is described as “autocatalytic,” as the deposition process will continue even after the substrate is completely covered by a continuous layer of the plated deposit. The deposit thickness will therefore continue to rise in the presence of source metal ions and a reducing agent, until the board is removed from the plating bath. The thickness of plated deposits will vary depending on the bath temperature, chemical parameters (such as solution pH) and the amount of time spent in the plating bath.

35.4.2.2 Immersion Process. This chemical process uses a chemical displacement reaction to deposit a layer of a second metal onto a base metal surface. In this reaction, the base metal dissolves, releasing the electrons that reduce the positively charged ions of the second metal present in solution. Driven by the electrochemical potential difference, the metal ions in solution (e.g., gold ions in ENIG or ENEPIG process) are deposited onto the surface of the board, simultaneously displacing ions of the surface metal into solution.

This type of reaction will continue as long as the base metal is available to supply electrons to the displacement reaction.

35.4.3 ENIG Fabrication Process Sequence

1. *Cleaner:* The purpose of this step is to clean the copper surface in preparation for processing. The cleaner removes oxides and light surface contaminants, and ensures that the surface will be in a condition allowing it

to be uniformly microetched. Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.

2. *Microetch:* The purpose of this step is to produce a surface that may be uniformly catalyzed and plated with good deposit adhesion by removing some copper from the surface. A variety of different etchant types may be used (e.g., sodium persulfate, peroxide/sulfuric). Vendor specifications for temperature, dwell time, agitation and bath chemical control should be followed.
3. *Catalyst:* The purpose of this step is to deposit a material that is catalytic to electroless nickel plating on the copper surface. The catalyst lowers the activation energy for nickel deposition and allows plating to initiate on the copper surface. Examples of metal catalysts include palladium and ruthenium (deposited by an immersion reaction with the copper surface). Vendor specifications for temperature, dwell time, agitation, and bath chemical control should be followed.
4. *Electroless nickel:* The purpose of this bath is to deposit the required thickness of electroless nickel on the catalyzed copper surface. The nickel thickness should be adequate to cover the copper with a substantially pore-free coating, to create a diffusion barrier to copper migration, and also serve as a solderable surface, depending on the intended application.

   The nickel bath has a relatively high deposition rate and its active chemical components must be maintained in balance on a continuous basis, by addition of appropriate replenishment components. Electroless nickel baths typically run at high temperatures and extended dwell times to achieve the required deposit thickness. It is therefore important to ensure that compatible PCB substrate and solder mask materials are used. Vendor

specifications for temperature, dwell time, agitation, and bath chemical control should be followed.

5. *Immersion gold:* The purpose of this step is to deposit a thin, continuous layer of immersion gold. The gold protects the underlying electroless nickel layers from oxidation or passivation, and also serves as a contact surface, depending on the intended application. This bath runs at relatively high temperatures and dwell times. Vendor specifications for temperature, dwell time, agitation, and bath chemical control should be followed.
   - *Rinsing:* The purpose of these steps is to remove residual process chemicals from the PCB surface after each chemical processing step. This may be achieved in either a single step or with multiple rinses. In some instances, predip and/or postdip process steps may also be required for optimum process performance. Vendor specifications for temperature, dwell time, agitation, and turnover rate should be followed.
   - *Drying:* The purpose of this step is to ensure the boards are completely dry. This may be achieved by use of either in-line vertical, or off-line horizontal drying. Off-line horizontal drying should be preceded by a horizontal rinsing step and should be dedicated to the boards from the ENIG processes. The time and temperature should be optimized to suit the type of product.

Due to the long dwell times, high operating temperatures, the ENIG process is always conducted in vertical tanks. To achieve the throughput required in production, many ENIG systems make use of two electroless nickel (EN) tanks, which allows for heating new baths or nickel stripping. Using two active EN tanks greatly improves throughput.

In addition to the normal plastic materials used in tank construction, stainless steel can be used for EN tanks. This is possible only with the use of anodic passivation, which

employs an electrical bias applied to the steel to prevent reduction of nickel ions on the steel. By using steel tanks, fabricators avoid the frequent stripping of plastic tanks required due to the slow plate-out of nickel on rough surfaces and localized hot spots.

35.4.4 Benefits and Limitations of ENIG Surface Finish

Benefits

- Flat co-planar surface, ideally suited for fine pitch surface mount applications
- Solderable surface forms a Ni/Sn intermetallic
- Aluminum and copper wire bondable
- Excellent contacting surface
- Shelf life exceeds 12 months
- Strengthens the PTH
- Protects the underlying copper from dissolution in the solder
- Does not require connectivity during the deposition process, like electrolytic Ni/Au
- Widely available

Limitations

- Complex process requiring good engineering and lab support
- Thicker nickel deposits may interfere with high frequency signal propagation
- Difficult to rework
- More costly compared to other finishes
- Susceptible to “nickel corrosion” or black pad*.

The term “black pad” (BP) occasionally referred to as “black nickle” describes a very specific phenomenon that

may occur in ENIG finished boards. It describes a corroded nickel surface under the immersion gold. If this corrosion is *excessive*, soldering fails (poor wetting, and poor solder joint strength). If a solder ball soldered to a highly corroded Ni surface is subjected to a pull force it would come apart at the Ni solder interface leaving behind a pad with a darker almost black Ni surface.

The BP occurs with an extended dwell time in an aggressive gold bath depositing on a compromised nickel surface. An aggressive gold bath is one where the plating parameters particularly the concentration of the gold is below the recommended supplier operating range. A compromised nickel deposit is uneven and has deep crevices, mostly a result of uneven catalyzation/initiation of nickel deposition. It can also be the result of running the bath outside the recommended ranges.

Following supplier's specification a pristine copper pad would be evenly catalyzed, the nickel will initiate uniformly and will produce a flat crevice free deposit. Under these conditions running the gold bath within its operating range will never produce BP or nickel corrosion.

35.5 NICKEL PALLADIUM GOLD

Electroless nickel/electroless palladium immersion gold (ENEPIG) is sometimes referred to as the "universal" finish, because of the versatility of its applications. ENEPIG is suitable for soldering, gold wire bonding, aluminum wire bonding, and contact resistance. ENEPIG is formed by the sequential deposition of electroless Ni (120 to 240 µin) followed by 2 to 12 µin of electroless Pd with an immersion gold flash (1 to 2 µin) on top. It is a multifunctional surface finish, applicable to soldering and to gold, aluminum and copper wire bonding. In addition, it is also suitable as the

mating surface for soft membrane and steel dome contacts, “low insertion force” (LIF) and “zero insertion force” (ZIF) edge connectors and for press-fit applications.

ENEPIG has the advantage over ENIG of being a gold wire bondable surface. ENIG is not an ideal gold wire bonding surface because over time the electroless nickel will diffuse thru to the surface along the crystal boundaries of the immersion gold and the bonding would fail. ENEPIG’s palladium layer is a diffusion barrier to the nickel, the gold remains unadulterated and is bondable with gold thickness as low as 1.2 µin or 0.03 µm.

A thicker gold coating as thick as 0.1 to 0.2 µm or 4 to 8 µin would open the wire bonding operating window. Thicker gold is beyond the capability of standard immersion gold. If a thicker gold is specified then a modified immersion gold like a “reduction assisted immersion gold” would be the preferred choice.

The electroless palladium requires a reducing agent. The most commonly used reducing agent is sodium hypophosphite, this produces a phosphorus palladium deposit with 4 to 5 percent phosphorous in the deposit. The presence of phosphorous renders the palladium deposit amorphous (noncrystalline), making it the ideal diffusion barrier. Other reducing agents may produce a nonphosphorus palladium which tends to be crystalline in structure.

35.5.1 The ENEPIG IPC-4556 Specification 2013

For thickness IPC-4556 stated:

The thickness specification for ENEPIG states:

Nickel: 3 to 6 µm [118.1 to 236.2 µin] at ± 4 sigma (standard deviations) from the mean. Palladium: 0.05 to 0.15

µm [2 to 12 µin] at ± 4 sigma (standard deviations) from the mean.

Gold: 0.025 µm *[1.2 µin] at −4 sigma (standard deviations) below the mean*.

All measurements to be taken on a nominal pad size of 1.5 mm × 1.5 mm [0.060 in × 0.060 in] or equivalent area.

An amendment is presently in final draft for peer review. The amendment is setting an upper limit for gold thickness for ENEPIG at 2.8 µin (0.7 µm). The amendment was necessary because too many designers were specifying a much higher immersion gold value. The higher thickness involved increased dwell time in the gold bath resulting in nickel corrosion under the palladium layer.

35.5.2 Process Sequence

The ENEPIG process sequence differs from the ENIG sequence only in the addition of the electroless palladium and its subsequent rinses between the electroless nickel and the immersion gold process steps.

35.5.3 ENEPIG Specific Attributes

ENEPIG has specific attributes that are attractive to designers that call out PWB surface finishes:

35.5.3.1 Soldering. ENEPIG forms the most robust solder joint with SAC type lead free solder. The copper and the palladium are incorporated in the intermetallic (IMC) Ni/Sn layer (Sn tin, Ag silver Cu copper). This limits the propagation of the IMC with thermal stressing or extended shelf life, resulting in a solder joint of superior strength.

35.5.3.2 Wire Bonding. ENEPIG is a gold wire bondable surface in spite of the reduced immersion gold thickness. The palladium layer is a diffusion barrier to the nickel, resulting in an unadulterated gold surface layer for bonding.

35.5.4 Benefits and Limitations of ENEPIG Surface Finish

Benefits

- Gold wire bondable
- Aluminum and copper wire bondable
- Solderable surface forms a Ni/Sn intermetallic
- Produces the most robust solder joint with lead free SAC type alloys
- Ideally suited for fine pitch surface mount applications
- Excellent contacting surface
- Shelf life exceeds 12 months
- Strengthens the PTH
- Protects the underlying copper from dissolution in the solder
- Does not require electrical connectivity like electrolytic Ni/Au

Limitations

- Complex process requiring good engineering and lab support
- Thicker nickel deposits may interfere with high frequency propagation
- Difficult and costly to rework
- More costly compared to other finishes

35.6 ORGANIC SOLDERABILITY PRESERVATIVES

As the name implies, organic solderability preservatives (OSPs) are very thin organic coatings used to preserve the solderability of PCB surface copper. OSPs form a complex organo-metallic compound with the copper surface of the PCB. The primary function of OSP is to provide a solderable surface finish, suitable for all surface mount and through-hole assembly applications and with an appropriate shelf life. The coating has demonstrated the ability to meet category 3 coating durability (shelf life of 12 months per J-STD-003 and industry data), when produced per the required vendor specifications. Some OSP coatings, may not necessarily meet this requirement, but may meet category 2 or 1 coating durability. In spite of OSPs being limited to solderability preservation, OSPs are widely used worldwide on products that are not fine pitched or with high aspect ratios holes.

There is a wide variety of OSPs that have evolved with the increasing complexity of the PCB. OSP products include benzotriazoles, imidazoles, benzimidazoles, and phenyl benzimidazoles (see Fig. 35.1). Initially all that was required was a single thermal excursion for soldering leads into component holes, Then came surface mount that required at least two thermal excursions (one per side), This later evolved into surface mount with through hole, and eventually to high aspect through holes in multilayer boards with heavy ground planes that act as heat sinks. Add on top of that the need to hand solder an occasionally rework.

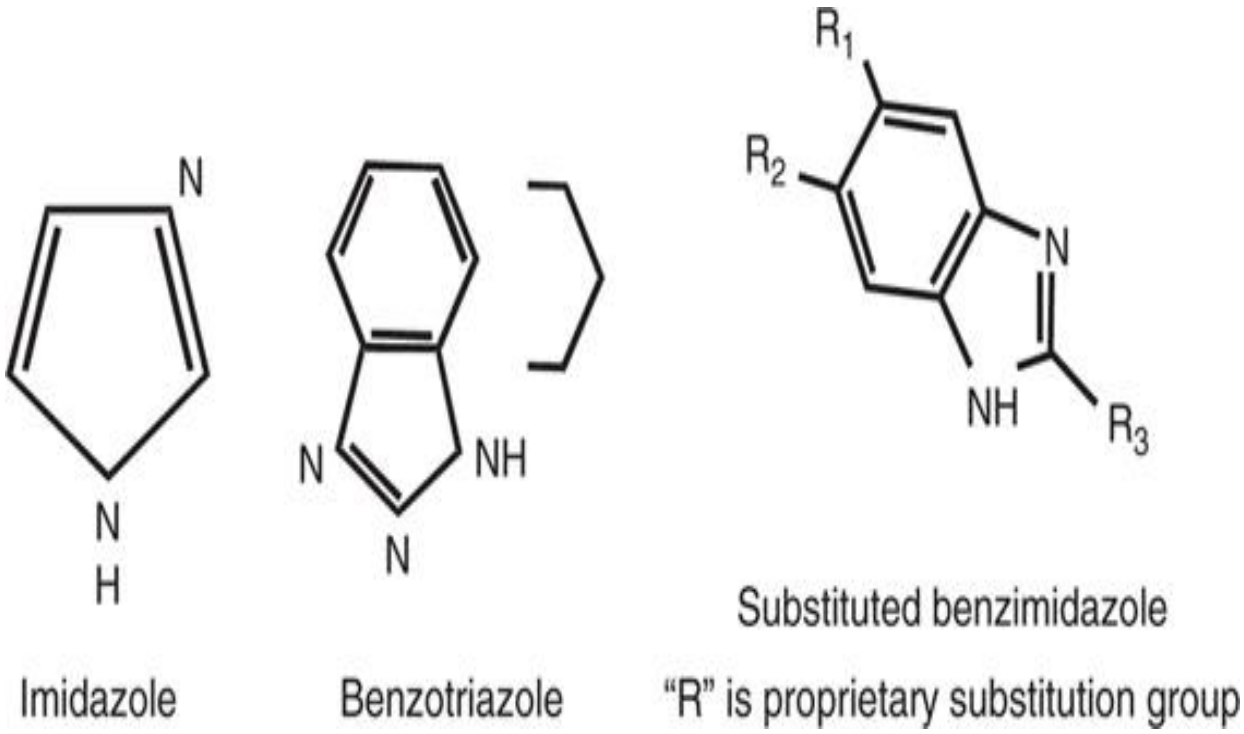

FIGURE 35.1 OSP molecule types.

The biggest relevant evolution is "lead free" (LF) assembly. LF assembly temperatures at 260°C are 35°C higher than eutectic soldering at 225°C. The more thermally robust coatings have significantly higher decomposition temperatures than the peak reflow temperature. They require contact with appropriate flux and or molten solder to penetrate the coating. They have longer shelf life, survive multiple reflow cycles and are more lead-free assembly compatible. Some of the newer OSPs have additives occasionally referred to as "oxygen scavengers." These additives can "open" the performance window of the specific OSP.

A newer generation of OSPs is designed to survive exposure to multiple high-temperature soldering operations. These chemicals are normally based on benzimidazole with attached functional groups to add molecular weight and thermal resistance. Substituted phenylimidazole and OSP systems with metal co-deposits have been used as well. The

intent of the new generation of OSP is to withstand Pb-free soldering temperatures. These “high-temperature” OSP coatings, made for use with Pb-free alloys and the associated fluxes, can be deposited at higher thicknesses and may be measured as high as 1.0 µm.

35.6.1 Fabrication Process

Table 35.2 shows the fabrication process for OSP, including chemicals and dwell times.

TABLE 35.2 Process Flow for Organic Solderability Preservative

Process	Chemicals	Time, min
Cleaner	Aqueous solvents, acids, and surfactant. The solvent removes organic residues. The acid removes oxidation and the surfactant wets the surface.	1–4
Microetch	1–2 µm of Cu is oxidized to Cu^{++} and dissolved.	1.0
Predip	Normally, the predip employs ingredients of the OSP bath without the OSP chemical itself.	0.5
OSP	OSP, acetic or formic acid, source of copper or other metals.	0.5–1.0

OSP is usually applied using conveyorized equipment. The cleaner and microetch may use flood or spray application, but OSP is applied using only a flood module. Rinsing is very important to ensure that contamination from all prior fabrication steps is removed. Often, OSP is applied when the PCB is in individual circuit form after the PWB has been electrical tested, routed, and depanelized. This is to preserve the fragile OSP surface, which is sensitive to handling,

contamination, and fingerprints. The OSP parts should stabilize at room temperature and controlled humidity before packaging, as any moisture in the package can cause different levels of discoloration.

OSP thickness is normally determined by indirect sampling. A sample coupon is processed along with the production parts. The coupon is immersed in an acid/solvent solution that dissolves the coating. The thickness of OSP is calculated by comparing the degree of UV light absorbance of the sample against a standard of known concentration using a spectrophotometer. That measurement is used as a quality control for the production boards.

Another method relies on “optical reflectivity” and resolves thin-film thickness by analysis of spectral interference observed by reflecting light over a range of optical wavelengths from layered samples. For OSP on PCBs, light reflected from the air/OSP interface and the OSP/Cu interface exhibits phase differences that create intensity oscillations across the wavelength range. The intensity oscillation is dependent upon the wavelength of the light, OSP thickness, and the physical properties of the coating. By analyzing the frequency and amplitude of these intensity oscillations, the thickness of the OSP coating can be determined.

35.6.2 Benefits and Limitations of OSP

Benefits

- Simple process
- Flat planar surface
- Widely available
- Forms a Cu/Sn intermetallic
- Easy to rework
- Cost effective

- High productivity at Fabrication

Limitations

- Handling sensitive
- Only applicable as a soldering finish
- Limited shelf life
- Exposed copper after final assembly
- Not easy to inspect or verify thickness
- Problematic for paste misprints
- A nonconductive surface

35.7 IMMERSION SILVER

Immersion silver (IAg) forms a thin immersion deposit over copper. It is a multifunctional surface finish, applicable to soldering, press fit connections and as a contact surface. It has the potential to be suitable for aluminum wire bonding. The immersion silver protects the underlying copper from oxidation over its intended shelf life.

Immersion silver is a galvanic displacement process with a typical thickness range of 0.1 to 0.4 µm. The fabrication process is easy, but the coating can suffer from tarnish when left exposed after assembly in field use. Heavy tarnish can be a predictor for corrosion and functional loss.

Thickness Specification of Immersion Silver IPC-4553 A (2009) states:

The thickness of the immersion silver deposit should be 0.12 µm [5 µin] minimum to 0.4 µm [16 µin] maximum at ± 4σ from process mean as measured on a pad of area 2.25 mm^2 or 1.5 mm × 1.5 mm [approximately 0.0036 in^2 or 0.060 in × 0.060 in]; typical value between 0.2 µm [8 µin] to 0.3 µm [12 µin].

Note: The original IPC-4553 silver specification issued in 2005 is outdated and should not be called out.

Chemical Coating

The PCB copper is prepared using separate cleaning and micro etch steps. Over time, these steps can be taken for granted, but improper use can cause many defects. The predip bath removes excess acidity from the PCB and prevents chlorides from entering the silver bath, where silver chloride would quickly precipitate. The silver bath relies on the galvanic displacement of less noble copper with two atoms of more noble silver. Proper rinsing and drying is essential.

35.7.1 Fabrication Process

Table 35.3 shows the fabrication process for immersion silver surface finish, including the chemicals used and dwell times.

TABLE 35.3 Process Flow for Immersion Silver

Process	Chemicals	Time, min
Cleaner	Aqueous solvents, acids, and surfactant. The solvent removes organic residues. The acid removes oxidation and the surfactant wets the surface.	1–4
Microetch	1–2 µm of Cu is oxidized to Cu^{++} and dissolved.	0.5–1.0
Predip	Normally, the ingredients of the silver bath without the silver metal itself.	0.5
Silver	Silver, acid, grain refiners, chelating agents $Ag^{+} + Cu(0) \rightarrow Ag(0) + Cu^{++}$	0.5–3.0
Postdip (optional)	Can be an antitarnish or an extra cleaner for demanding ionic cleanliness applications.	

Most immersion silver in large production is applied in conveyorized equipment. The cleaner and micro etch may use flood or spray application, but the silver solution is applied using flood. Rinsing is very important to ensure that contamination from all prior fabrication steps is removed. In smaller-scale production and prototype manufacturing, silver can be applied in vertical process tanks. Often, silver is deposited on individual circuits, after the PCB has been routed, depanelized, and electrically tested. This is to preserve the silver surface, which can be sensitive to handling, contamination, and fingerprints.

35.7.2 Benefits and Limitations

Benefits

- Planar surface finish suitable for fine pitch assembly
- Relatively simple process, with high productivity at fabrication
- Forms a Cu/Sn solder joint
- Suitable for use as a contacting surface
- Compatible with lead free soldering
- Widely available

Limitations

- The surface will tarnish over time
- Handling sensitive
- Exposed silver after assembly can exhibit creep corrosion
- May attack the soldermask interface during deposition
- Requires special packaging for extended (12 months) shelf life

Design considerations for IAg:

The following should be part of the original design for immersion silver surface finish:

- Use anti-tarnish overlay
- Eliminate soldermask defines pads (SMD) pads
- Filled vias must be completely filled
- At assembly, print paste to cover entire pad
- Keep test pads apart (min 80 mils)
- Paste and reflow test pads

35.8 IMMERSION TIN

Immersion tin is a thin coating of pure tin, typically 0.6 to 1.2 µm thick, which protects the underlying copper from oxidation and provides a highly solderable surface. Tin is deposited using a galvanic displacement process and can be applied in vertical or conveyorized equipment. Tin boards are used primarily for solderability and have very good compliant pin connector functionality.

IPC-4554 Immersion Tin Specification 2007

For immersion tin the committee only specified a lower limit for thickness. The relatively thick value of 1 µm was chosen to ensure that enough virgin tin would be available at the surface for soldering after storage. It is well understood that tin forms an intermetallic (IMC) layer with the underlying copper, and that this layer continues to grow in thickness over time.

The immersion tin thickness will be:

1.0 µm (40 µ”) minimum at –4σ from process mean as measured on a pad of area 2.25² µm (3600² mils). Typical value of 1.15 µm ((46 µ”) to 1.3 µm (52 µ”).

The immersion tin Specification IPC-4554 was amended in 2011. The amendment addressed solderability testing and specified the allowed stress testing conditions for the deposit and the type of fluxes to be used for both tin/lead and LF testing.

35.8.1 Immersion Tin Deposit

As with all immersion metal systems, the copper needs to be perfectly clean and textured before the tin plating step. A predip is used to maintain proper chemical balance in the tin bath and prevent contamination. The tin deposition is not a direct galvanic displacement, since tin is more electronegative than copper. Thiourea is used in tin chemical formulation to create a copper-thiourea complex on the surface. This complex becomes more electronegative than tin, and can be displaced in the immersion reaction. Because of the need to drive the reaction, the tin bath contains relatively high concentrations of chemicals, which must be thoroughly rinsed. Allowance must be made at waste treatment for the presence of thiourea.

35.8.2 Fabrication Process

Table 35.4 shows the fabrication process for the immersion tin surface process, including chemicals used and dwell times.

TABLE 35.4 Process Flow for Immersion Tin

Process	Chemicals	Time, min
Cleaner	Aqueous solvents, acids, and surfactant. The solvent removes organic residues. The acid removes oxidation and the surfactant wets the surface.	1–4
Microetch	1–2 µm of Cu is oxidized to Cu^{++} and dissolved.	0.5–1.0
Predip	Normally, the ingredients of the tin bath without the tin metal.	1.0
Tin	Tin, thiourea, acids, whisker inhibiting trace metals, chelating agents.	4.0–12.0
Postdip (optional)	Can be an extra cleaner for demanding ionic cleanliness applications.	

Some production installations use immersion tin in horizontal conveyorized applications. Conveyorized lines are long and therefore expensive and are only used in high productivity fabrication sites. The use of vertical tanks carrying baskets of panels for immersion tin plating makes better use of production floor space. Due to the high sulfur reactivity of the thiourea ingredient, tin lines should be dedicated to the tin process only and not mixed in with OSP, silver, or ENIG lines where sulfur can harm the surfaces.

35.8.3 Benefits and Limitations

Benefits

- Planar surface finish suitable for fine pitch assembly
- Relatively simple process, with high productivity at fabrication
- Forms a Cu/Sn solder joint
- Excellent compliant tin functionality
- Compatible with lead free soldering
- Reworkable
- Widely available

Limitations

- The surface will oxidize with exposure to moisture and air
- Susceptible to whisker formation
- Handling sensitive, a soft metal
- May attack the soldermask interface during deposition
- Cu/Sn intermetallic (IMC) is formed after deposition and continues to grow with time and temperature
- The IMC may interfere with accurate thickness determination

35.9 OTHER SURFACE FINISHES

Other surface finishes include reflowed tin-lead, electrolytic nickel/electrolytic gold, electroless palladium, electroless gold, direct immersion gold,

35.9.1 Reflowed Tin-Lead

Before the widespread use of solder mask, a primary method for protecting copper circuitry was to electroplate a coating of tin or tin-lead on the copper. After component insertion, the tin plating could be liquefied with oven or vapor-phase reflow to form solder joints. The use of solder mask over bare copper to take advantage of surface mount, wave soldering, and mixed assembly restricted the use of tin plate finishing. For simple technology product, tin or tin-lead plate and reflow remains a viable fabrication and assembly method.

35.9.2 Electrolytic Nickel/Electrolytic Gold

The electrolytic nickel-gold process employs galvanic electroplating. The circuit board is placed on a rack and electrically connected to a power supply (rectifier). When immersed in a solution of metal ions, the metals are reduced as a metal coating on the PCB by the supply of electrons. The metal thickness grows in a very predictable way depending on the time, current, area plated, and efficiency of the reaction. More frequently, the coating is applied selectively in combination with another finish such as OSP.

Electrolytic nickel gold is commonly used on features requiring high-force physical connections or gold wire-bonding. Several micrometers of nickel are deposited, and 0.50 to 1.5 µm of gold as the final mating surface. It is not a recommended soldering surface as the thicker gold will create embrittlement within the intermetallic phase of the solder joint.

If the surface is designed as a contacting surface with multiple insertions hard gold must be used. Gold is hardened by alloying the deposit with ~3 percent of nickel, chromium, or iron. For a large number of PCBs that employ edge tab connection, the PCB is electroplated in a special plating line where only the exposed edge features are immersed into the plating cell.

If the application is gold wire bonding, only soft gold (99.99) must be used. For gold wire bonding a thick gold layer ensures that the underlying nickel will not defuse all the way to the surface where it would have an adverse effect on the bonding process.

35.9.3 Electroless Palladium

As a precious metal palladium is resistant to oxidation, and can offer a good physically strong deposit for electrical contacts and soldering. A thin coating of 0.1 µm or 4.0 µin was successfully utilized as a solderable and contacting

surface in the mid to late 1990s. As the price of palladium soared, it became less attractive and for this application immersion silver was a more attractive alternative.

35.9.4 Electroless Palladium/Immersion Gold

As electroless palladium/immersion gold (EPIG) begins to get a foothold in the industry as a surface finish with unique attributes; the question was what about very fine pitch applications where the thickness of the nickel may reduce the spacing between the pads? And what about high-frequency signal propagation where the thicker nickel layer “skin effect” may create a degree of signal loss? These have led to the emergence of EPIG, as a surface finish that could resolve these issues. It is a solderable contacting surface that is also gold wire bondable.

Suppliers who offer this finish have specific recommendation for the thickness of the palladium and the gold depending on the intended use. No IPC specification for this finish exists as yet.

35.9.5 Electroless Gold

Gold can protect copper and resist oxidation like no other metal. Electroless nickel with a cover layer of electroless gold is a viable surface finish and has been in use as a gold wire bondable surface. For this specific application the electroless gold is deposited on a layer of immersion gold. Both gold layers are soft/pure gold (99.99 pure). As with ENIG, electroless nickel under layer is needed as a barrier layer to prevent copper to gold interdiffusion. Electroless gold can achieve a sufficient thickness to allow gold wirebonding and some physical connection functions. It also deposits much

more uniform thickness than electrolytic gold. Better thickness control allows somewhat thinner coatings, so gold embrittlement can be prevented, if the finish doubles as a soldering surface. Cost and process control considerations prevent more widespread use as a PCB finish.

35.9.6 Direct Immersion Gold

Because electroless nickel is the cause for many of the disadvantages of ENIG, some designers have considered the use of immersion or electroless gold directly on top of underlying copper. This process works for boards that are assembled without a long shelf life and do not require multiple thermal excursions. Without the barrier coating of nickel, however, the copper and gold soon dissolve into each other creating a discolored gold finish. The solderability of the finish, however, is unaffected by this discoloration. The finish remained solderable after 3+ years in an ambient environment.

Printed circuit board designers have at their disposal a large variety of surface finishes. Each surface finish is unique in some aspect like cost, material compatibility, signal integrity, assembly attributes, intended use, life expectancy, environment of use, reliability, and the list goes on.

Newer designs like continuous miniaturization and high frequency signal propagation, are creating opportunities for supplier’s R&D departments to seek innovative surface finish solutions to meet the continuous evolution of the electronics industry.

CHAPTER 36
SOLDER MASK

David A. Vaughan
Taiyo America, Inc., Carson City, Nevada

36.1 INTRODUCTION

36.1.1 Definition and Terminology

The term *solder mask*, as used in this chapter, is the same as the terms *mask, soldermask*, or *solder resist*, which are frequently used interchangeably in the printed circuit board (PCB) fabrication industry. The Association of Connecting Industries (IPC) has standardized on the use of *solder mask*, since that is the term most widely used in the industry. The existing definition for “Solder Resist” from IPC-T-50 is, “A heat-resistant coating material applied to selected areas to prevent the deposition of solder upon those areas during subsequent soldering.” With the evolution of PCB technology, solder mask coatings are now asked to provide much more functionality than simply a soldering aid.

36.1.2 Purpose

When solder masks were first used, their purpose was to protect the circuitry of the PCB from solder during the assembly operation. Eliminating short circuits was the main objective. As the use of solder mask became more prevalent and the material properties improved, solder mask was used for other functions, such as to provide environmental protection to the assembled board, and to serve as a plating resist for final finishes, dielectric protection, and other functions that take advantage of the properties of the cured mask.

36.1.3 History

Solder mask began with the use of two-part epoxy, thermally curable inks that were an offshoot of inks that were used in the printing industry. These inks were applied by screen printing with the use of a patterned screen, since these materials were not photoimageable. One-part inks that were ultraviolet (UV) curable were available soon after, but these also had to be applied by a patterned screen because they could not be imaged and developed.

Photoimageable solder masks were developed in the mid-1970s and were offshoots of photoresist materials used for patterning the circuitry. Photoimageable solder masks were developed in both liquid (LPI) and dry film (DFSM) and both were used widely. Today, more than 98 percent of the solder mask used is applied in liquid form, and most is photoimageable.

36.2 TRENDS AND CHALLENGES FOR SOLDER MASK

The use of solder mask continues to evolve with the technology. This section discusses some of the issues involved.

36.2.1 Circuit Density

Since the development of circuit boards, the dimensions of the holes and features have been decreasing. Smaller component attachment dimensions require corresponding decreases in solder mask features that challenge the solder mask materials and processes.

36.2.1.1 Feature Size. Smaller solder mask features have eliminated non-photoimageable solder masks from all but the lowest technology designs, and continue to require ongoing improvements in resolution and image reproduction. A very high percentage of solder mask being used is photoimageable.

36.2.1.2 Hole Size. Holes in boards that have been coated with LPI solder mask will have some solder mask material in the holes after application. Typically this material must be removed in the development process. There are very significant differences in how easily different solder mask materials develop from holes. There is also a difference in the amount of solder mask material that is in the holes between application methods, with spray and curtain coating leaving less material than screen printing.

36.2.2 Component Attachment in a Lead-Free Environment

As many PCB fabricators and assemblers transition to lead-free processing, they are faced with solder alloys that have

an operating temperature up to 30°C (54°F) hotter than the traditional eutectic tin-lead solders. These increased soldering temperatures raise concerns about the ability of the solder mask (as well as all other materials) to resist embrittlement, discoloration, loss of adhesion, and cracking with repeated exposures to the higher temperatures. Some existing products may not be acceptable for lead-free processing.

36.2.3 High-Density Interconnection

High-Density Interconnection (HDI) technology creates small blind microvias that are plated to provide interconnects to buried layers of circuitry. These small holes can either be coated with solder mask or filled and plated over so that the real estate of the hole can be utilized for a circuit or a component mounting pad (via-in-pad).

If the hole is simply coated with solder mask and the solder mask is not developed from the hole, the air trapped in these small holes may expand and create a bubble or blister, or may erupt, exposing the copper in the hole to potentially corrosive chemistries. These holes should be developed cleanly so that they receive the final finish, should be protected before solder mask application with an inert final finish or be completely plugged.

Plating over microvias requires that they are totally filled, planarized, roughened, and catalyzed before the plating process. If a conductive plugging material is used, the catalysis step typically can be eliminated. Material selection for this application is particularly important because not many materials can withstand the roughening and plating and still maintain good adhesion of the copper to the plugging material after exposure to soldering temperatures. If the via is in a component mounting pad (via-in-pad), the plugging material must not shrink and cause a significant

depression (dimple) in the pad. This is especially true for wire bonding applications that require a very flat planar surface.

36.2.4 Environmental

The Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC places restrictions upon specific materials that may be included in PCB fabrication materials, including solder masks. These requirements may require some products to be reformulated. Some products and/or markets may require low-halogen materials to comply with company or industry specifications. Again, these requirements have required some solder masks to be reformulated or new products to be developed.

Many localities have strict air emissions regulations that limit the materials and the amount that may be exhausted to the atmosphere. Individual processes or pieces of equipment may require a permit to exhaust any volatile materials. Hazardous air pollutants (HAPs) and volatile organic components (VOCs) are of particular concern. Limits on these parameters can limit mask selection and application processes. For example, curtain coating and spray mask application are not viable in some areas due to the higher percentage of solvent needed for proper application. Screening utilizes solder mask at a much higher percent solids (less dilution), so air emissions may be only half that of other methods.

36.2.5 Technical Service and Troubleshooting

The solder mask process is quite complex. It relies upon all PCB fabrication processes that preceded it and plays a key

role in all processes after it has been applied, through assembly and the life of the PCB. As a result, it is recommended that the specifying authority choose companies that can provide technical expertise and troubleshooting assistance. Companies that offer service and experienced engineering personnel in the PCB fabricators are becoming scarcer, making the supplier's ability to provide service a key issue in solder mask selection.

36.3 TYPES OF SOLDER MASK

36.3.1 Non-Imageable

Early solder masks could not be photoimaged—that is, placed in its exact location with a photographic process. They could not be hardened selectively in one area and then be removed from other areas. These masks had to be applied in the final pattern desired, typically through a patterned screen. The "silk screening" process (the screens are actually nylon) is limited in that it can neither resolve the fine features nor meet the registration requirements and tolerances needed for today's PCB designs. The use of these materials is limited to lower technology products.

36.3.2 Imageable

Higher-density circuitry, with its close tolerances and image reproduction requirements, has mandated the use of photoimageable solder mask. Assemblers need fine dams (or "webs") of solder mask between fine-pitch component leads (see Fig. 36.1) to enable assembly with low defect rates. These webs are frequently as narrow as 0.003 in. and can be as narrow as 0.001 in. A photoimageable mask is required to meet these needs.

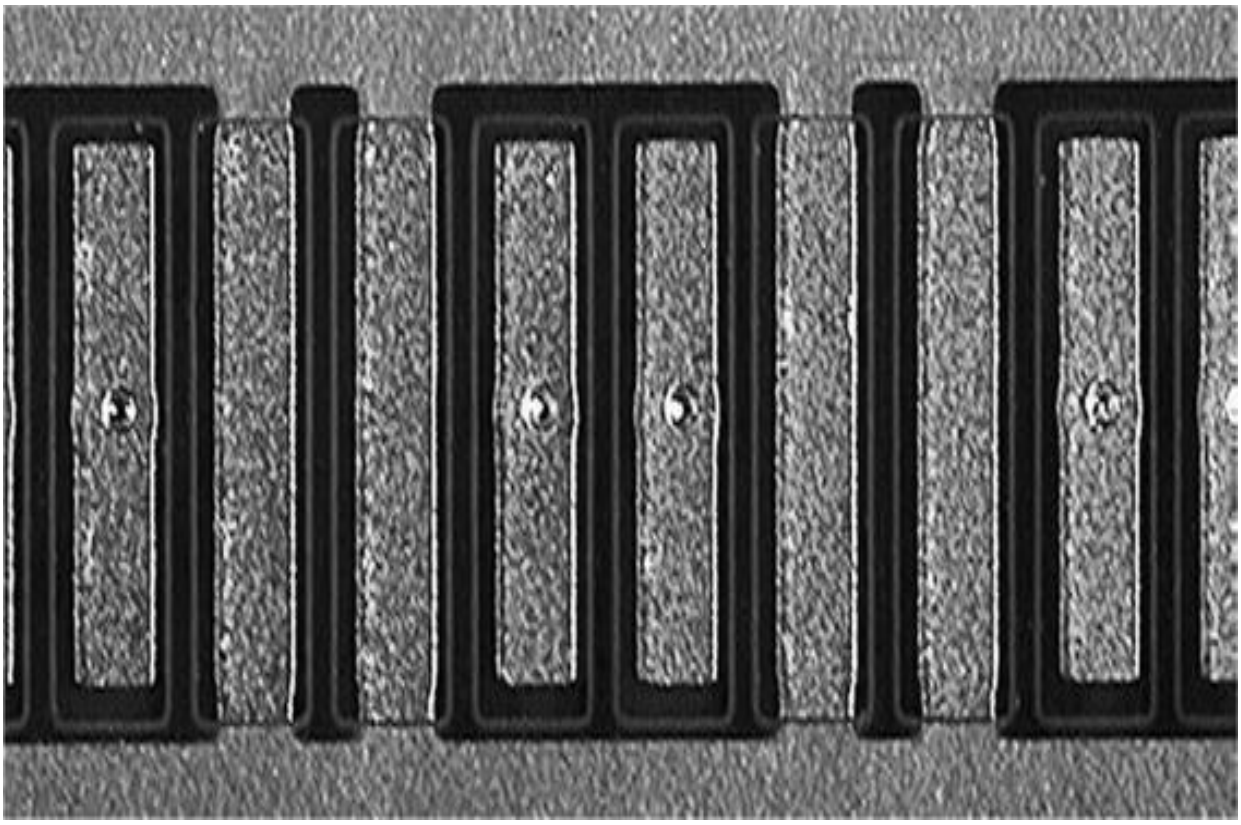

FIGURE 36.1 An example of fine solder dams, or “webs,” imaged between fine pitch SMT pads.

Photoimageable masks are available in either liquid or dry-film forms. Liquids account for more than 98 percent of the products used, due to their lower cost, greater availability, ease of use, and acceptability in assembly processing. Dry-film masks require special application equipment, are expensive, are often not robust when used as a resist for final finishes such as ENIG or immersion tin, and are too thick for use in some assembly processes.

36.3.3 Temporary

A number of temporary masks are used in PCB fabrication and assembly processing. The properties of these masks vary considerably depending upon the purpose for which they have been used. The typical application for these masks

is to protect circuitry from plating and/or soldering. Various products can be removed mechanically by peeling (“peelable mask”) or by dissolving in cleaning chemistry. Since they do not become a permanent part of the finished assembly, there are no industry standards for these products. PCB fabricators and assemblers should be careful to verify the compatibility of any temporary mask with their solder mask(s) to avoid problems such as swelling, blistering, and so on.

36.4 SOLDER MASK SELECTION

36.4.1 Availability and Consistency

There are ongoing changes in the makeup of the supplier base of electronic materials, including solder mask. Many acquisitions have taken place and several products eliminated in the recent past, so users must have confidence that they will have a continued source of supply of solder mask that is the same lot to lot for the future. International Organization for Standardization (ISO) qualification for the manufacturing operation as well as for environmental considerations are good indicators of a supplier with a long-term view.

36.4.2 Performance Specifications

36.4.2.1 IPC-SM-840. This is the predominant solder mask material specification used globally. Most manufacturers test their products to verify that their products are capable of meeting the requirements of this document. The SM-840 includes physical, chemical, thermal, and electrical requirements for two classes of application.

36.4.2.2 Underwriters Laboratories UL94. This specification defines the degree of flammability of a material. Solder mask suppliers generally test their products for flammability according to UL94. The solder mask is applied to a specific type of base material or construction before burn testing. The main variables in this test are the specific base material and construction, the mask type, and the thickness of each. Since most solder mask has no flame retardant, thinner mask and thicker base material will give better results.

36.4.2.3 Telcordia GR-78-CORE. This specification, from Telcordia, is commonly referred to by its previous name, BellCore. With the introduction of the C Revision to IPC-SM-840, the Class T requirements were accepted by the BellCore as equivalent to meeting the GR-78-CORE specification. This specification is still available as part of a package of documents from Telcordia that is quite expensive. However, since Telcordia recognizes the IPC-SM-840 Class T specification for solder mask, it is typically not necessary to purchase a copy of the GR-78 specification.

36.4.2.4 Military Applications. The military specification that applies to solder mask is MIL-P-55110. Since the mid-1990s, the revisions of this document refer to the IPC-SM-840 specification for solder mask requirements.

36.4.2.5 NASA Outgassing. Materials that will be used in space applications are tested under extremely high vacuum conditions. To be acceptable, they must exhibit a maximum total mass loss (TML) of 1.0 percent and have a maximum collected volatile condensable material (CVCM) of 0.10 percent. A list of tested products is available from the NASA website at http://outgassing.nasa.gov. This site features “Outgassing Data for Selecting Spacecraft Materials,” which lists products that the Goddard Space

Center has tested (and the tests' results). Not all materials tested have passed the TML and CVCM specifications. Independent test labs can also be used to test for this property.

36.4.2.6 Other Customer Industry Application Specifications (AABUS). Often PCB customers have special requirements for their solder mask. These can be a modification of the IPC criteria or some additional requirement not included in the SM-840 document. There is a term used to describe these requirements: as agreed between user and supplier (AABUS). The key word here is "agreed," since both parties must be completely aware of the requirement and what it takes to achieve the required result.

36.4.3 Environmental and Health Considerations

36.4.3.1 RoHS Compliance. Most PCB fabricators now insist that any solder mask products they use be compliant with Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment, the RoHS directive, and Directive 2003/11/EC, the 24th amendment to Council Directive 76/769/EEC. This directive places requirements on specific materials and amounts of each that may be included in a formulation. Meeting this criterion is essential for most printed wiring board (PWB) fabricators.

36.4.3.2 Lead-Free. One of the materials eliminated with RoHS compliance is lead. The largest impact of eliminating lead is the higher soldering temperatures required for lead-free solders. Soldering temperatures for

these alloys are typically 10 to 20°C hotter than for eutectic tin-lead solders. For example, one of the current alloys of choice is SAC-305 (tin-silver-copper solder) has a melting point 34°C higher than eutectic solder. Higher temperatures place additional stress upon the solder mask and could potentially lead to adhesion loss, color change, embrittlement, or cracking.

Organization	Spec-test Method	Chlorine	Bromine	Total Halogen
JPCA	JPCA-ES-01-1999	<900 ppm	<900 ppm	
IEC	IEC 61249	<900 ppm	<900 ppm	<1,500 ppm

36.4.3.3 Low Halogen. The low-halogen requirement came about due to concerns about incineration of scrap PCBs generating dioxins under some conditions, and originally centered on some brominated flame retardants used in base laminates. It progressed from that into an additional concern over the chlorine content. This requirement is sometimes referred to as “halogen-free,” but in reality, the true requirements place a limit on the amount of bromine, chlorine, and their sum in the content of the material. Current low-halogen requirements on the cured solder mask are as follows:

Although solder masks do not typically contain flame retardants, and hence no bromine, they often contain chlorine. The chlorine generally comes from pigments that give the mask its desired color, and also from residual catalyst from the resin (solder mask raw material) manufacturing process. A number of manufacturers offer low-halogen solder mask materials that meet the specified criteria.

36.4.4 Circuit Density Issues

As the pitch of circuitry and packages has decreased, it has also generated the demand for smaller holes and finer solder mask features.

36.4.4.1 Hole Size. As mentioned in Sec. 36.2.1.2, small hole sizes are a significant challenge for the solder mask process. All application processes introduce some solder mask into the holes, and this material must be removed (developed) from the holes before curing. There are two primary considerations in achieving finished PCBs with no mask in the holes. First, it is easier to achieve mask-free holes when less solder mask is introduced into the holes during the application process. In general, spray applications put the least mask into holes, and single-sided screening introduces the most. Curtain coating and simultaneous double-sided screen printing produce more moderate levels of solder mask in holes.

The ability to remove all solder mask from the holes is dependent upon the solder mask material itself, the tack drying, and the developing processes. Some solder masks inherently develop faster than others, so the choice of products has a significant impact on development. If the solder mask is subjected to an overly aggressive (too hot and/or too long) tack drying process, the mask may not develop at its optimum speed. The developing equipment and process should be set up according to the solder mask manufacturer's recommendations. This includes the chemistry, pressures, flow rates, nozzle type(s), process cycle times, and so on.

36.4.4.2 Solder Dams ("Webs"). To reduce soldering defects in assembly, designers have placed fine solder dams, or "webs," between attachment pads. The width of these dams is frequently in the 2.5 to 3.0 mil range, with some

designs requiring dams as narrow as 1.0 to 1.5 mils wide. Producing features this fine is not possible with all solder mask materials, and the imaging process for very fine features will typically be modified from normal production with wider dams.

36.4.5 Assembly Considerations

36.4.5.1 Thickness. When PCBs had all through hole components, solder mask thickness was not of much concern. However, with the advent of surface-mount technology in the 1980s, excessive solder mask thickness caused assembly problems, including:

- Tombstoning of discrete devices in reflow soldering
- Excessive opens with discrete devices in wave soldering
- Solder paste printing problems (excessive paste, solder balls, paste on back of stencil, etc.)

Flip-chip assembly, with its finer pitch, has placed further restrictions on the maximum mask thickness. These thickness restrictions effectively eliminated dry film solder mask in most applications and relegated it to a specialty product for special applications.

36.4.5.2 Cleanliness. After PCBs have been assembled, they must meet specific ionic and visible cleanliness requirements. It is important that PCBs produced with the specific solder mask through the normal process be qualified through the assembly process to ascertain whether the production parts will meet expectations. Each solder mask and flux combination throughout the assembly process may give a different cleanliness result.

36.4.5.3 Solder Balls. Some assembly processes are more prone to generate solder balls than others.

Prequalification of the solder mask with the assembly chemistries and processes is essential to predict production performance. If solder balls occur during assembly, in some cases they can be reduced by using a mask with a different surface finish. Satin or matte products sometimes have less of a tendency to have solder balls. Modifying the solder mask cure can have an effect on the level of solder balls also—consult with the solder mask supplier before deviating from its recommended cure process.

36.4.5.4 Assembly Material and Process Compatibility. When qualifying a new solder mask or new PCB supplier, it is critical that all existing materials and processes be evaluated for compatibility before production is scaled up. This should help avoid major issues where there is a large quantity of PCBs awaiting assembly that cannot be assembled with the existing assembly materials and processes. Care should be taken to include evaluation of:

- Soldering fluxes and pastes
- Cleaning agents
- Multiple heat exposures
- Adhesives
- Underfills
- Temporary solder masks
- Tapes
- Anything else in assembly that depends upon the surface of the solder mask

36.4.5.5 Conformal Coating Compatibility. Again, qualification of the solder mask, through all of the fabrication processes, is required to ensure that no problems with production boards arise. Since conformal coating is applied after assembly, a significant amount of processing and exposure to other chemistries will have happened since the

solder mask has been applied. The conformal coating compatibility testing should be done on a board that has been through all of the assembly processing. The cleanliness of the PCB surface after the final assembly process has a great impact upon the adhesion of the conformal coating. One cannot expect conformal coating to adhere well to a dirty board. These coatings were not meant to be applied over a no-clean flux, but over a clean substrate.

36.4.6 Application Method for Installed Equipment

Choose solder mask that is compatible with the existing or proposed application method. Not all solder masks can be screen printed, sprayed, and curtain-coated. Consult with the solder mask supplier for the appropriate solder mask for your application method.

36.4.7 Gloss

Solder masks are available in different levels of gloss. Typical terminology for finishes includes gloss, semigloss, satin or semimatte, and matte. These finishes represent a certain level of reflectivity of light and microroughness. Gloss level is generally specified by end users for assembly or cosmetic reasons.

36.4.8 Color

Likewise, different levels of color may be available. Most solder mask is green, but many other colors, such as red, blue, black, yellow, and white, are often specified. Some solder masks are specified to be clear.

36.4.9 Packaging versus PCB

When solder mask is used on substrates that will become part of a semiconductor package. The JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council) specifications apply in addition to the IPC specifications. JEDEC specifications include additional, more aggressive testing that generally requires a more robust solder mask. Low moisture absorption is important for a mask used in packaging applications.

36.4.10 Surface Finish Compatibility

The choice of the final surface finish for the copper has an effect upon how the solder mask performs. And, with the elimination of lead in solder, the compatibility of new final finishes needs to be confirmed before their implementation. Most of these finishes are applied after the solder mask so the process for mask application can have a significant impact upon final quality of the PCB:

- *Hot air solder leveling (HASL)* This has been the most common final finish, utilizing 63/37 eutectic or 60/40 tin/lead (Sn/Pb) alloys. The PCB is coated with flux, immersed into molten solder, and withdrawn through air knives to remove excess solder. Lead-free solders are expected to require solder temperatures significantly hotter than what has been required for eutectic solder. The higher temperatures are expected to place higher stress on the solder mask and may also present more difficult post-HASL cleaning challenges.
- *Electroless nickel/immersion gold (ENIG)* ENIG is typically applied to the metal surfaces of the PCB after the solder mask process. Each plating chemistry supplier has its own ENIG bath, and each has a different level of

aggressiveness to the solder mask. Consequently, the solder mask and ENIG chemistry must be qualified together to avoid breakdown of the solder mask over circuits or around openings on metal. A thicker coating of solder mask may alleviate solder mask breakdown problems. Excessive microetching before plating can undermine the solder mask and induce tape test failure as the overhanging mask is broken off.

- *Immersion tin* The same comments from ENIG also apply to immersion tin.
- *Immersion silver* Immersion silver is relatively benign to the solder mask, and few, if any, issues are known as of the writing of this book.
- *Organic solderability preservative (OSP)* This is another process and chemistry that has little impact on the solder mask.

36.5 SOLDER MASK APPLICATION AND PROCESSING

36.5.1 Surface Preparation

Solder mask should be applied to a clean, dry surface. The cleaning step should remove all particulates, oils and greases, and unwanted oxides. In the case of bare copper, this step should provide some “tooth” to the copper to enhance the mechanical bond of the mask to the copper. The cleaning step is followed by a rinse and drying step that leaves the panels ready for coating with mask. The surface preparation technology chosen is dependent upon the metallization of the circuitry and, to a lesser extent, the base laminate material.

36.5.1.1 Copper Circuitry. A large majority of panels produced have solder mask coated over bare copper (SMOBC). The goals of the surface preparation process are to remove all unwanted oxides and contaminants from the copper and to impart a microroughness or “tooth” to the surface, and to leave a clean, dry surface for coating.

36.5.1.1.1 Incoming Copper. The quality of the surface of the copper is very important for achieving good solder mask adhesion. All traces of the etch resist metallization, typically tin or solder, must be removed prior to the solder mask surface preparation process. Solder mask does not adhere well to tin or solder residues or tin-copper intermetallic surfaces.

36.5.1.1.2 Preparation Methods. The most common surface preparation method is pumice scrubbing with either a silica or aluminum oxide media. Most equipment in use is brush pumice, but jet pumice may be used also. With this method, the main considerations are keeping the pumice concentration within recommended levels, periodic changing of the media, and good equipment maintenance. A prepared surface from a proper pumice cleaning will have a uniform rosy pink, matted surface that is free from stains. Considerations in pumice-based preparation techniques include the following:

- *Brush pumice versus jet pumice* Both techniques utilize a slurry of pumice in water. With brush pumice the slurry is pumped onto the panel surface under low pressure, and rotating brushes scrub the pumice against the panel surface to clean and roughen it. With jet pumice, the slurry is sprayed through nozzles at high pressure onto the panel surface; the impact of the particles against the panel surface provides the cleaning and roughening.
- *Silica versus aluminum oxide* The media used in pumice scrubbing degrades with usage. Silica pumice is softer than aluminum oxide and must be changed more

frequently, but it is much less expensive; thus relative cost differences in operation may not be significant. Silica pumice particles degrade by fracturing into smaller pieces and not providing the needed impact to roughen the surface. Aluminum oxide particles become rounded with age and will “peen” the surface instead of roughening it. Both conditions lead to a less than optimum solder mask adhesion.

Chemical cleaning, usually in the form of a microetch, may be used to prepare the copper surface. Not all microetch chemistries will provide the proper tooth for best adhesion, so a product should be selected that provides some tooth (a matte surface is a good indicator) instead of a bright shiny surface. Good rinsing and drying, and possibly a passivation chemistry, are important to avoid rapid staining of the copper since it is very active after chemical cleaning.

Abrasive brush or compressed pad technology is generally acceptable for solder leveled panels, but if other final finishes such as ENIG or immersion tin are used, it may not provide sufficient adhesion. The abrasive in the brushes leaves directional scratches in the copper that can lead to the wicking of plating chemistries under the mask that will cause loss of adhesion around mask openings on copper. If this method is to be used, it should be followed by a chemical cleaning that will provide the microroughness needed for good adhesion.

A very good alternative to abrasive or chemical cleaning is to impart an oxide to the copper surface. If the copper has not been cleaned or if there are residual etch resist metals on the surface, the copper will not oxidize. The oxide provides a fine structure and microroughness for very good adhesion. When using this technique, the fabricator should use a “reduced oxide” so that cleaning chemistries in subsequent processes will not attack the oxide layer and cause adhesion loss at the mask-copper interface.

36.5.1.1.3 Rinsing and Drying. After the cleaning step, the panel surfaces must be thoroughly rinsed with good quality water. City or well water is often inadequate due to high levels of minerals, particulates, and other contaminants. Poor water quality can lead to blistering of the mask and/or discoloration of the copper under the solder mask. Deionized (DI) water is the best rinsing agent, but reverse osmosis (RO)-treated water is also used effectively.

After the panels have been rinsed, the drying step should remove the water from the panels—both from the surface and from the holes. Air knives should be incorporated to blow out the holes and sweep the water from the surface. It is undesirable to dry water on the boards since any droplets that are dried will leave behind any dissolved minerals and other contaminants that had been in the water.

36.5.1.2 Other Metals

36.5.1.2.1 Gold, Tin, or Solder. If the gold-plated surface is perfectly clean, no surface preparation is required. However, if there is any question about cleanliness, or if the panels have been exposed to any chemical vapors or particulates, or have been awaiting solder mask for any appreciable time, they should be cleaned. Depending upon the extent of surface contamination, the panels can be only rinsed and dried, or may be cleaned in a mild detergent solution before rinsing and drying. Abrasive cleaning is not recommended.

36.5.1.2.2 Mixed Metals. Two good examples of the use of mixed metals are for panels that have been selectively solder-stripped and for panels that have had fingers or contacts plated with gold before the solder mask process. The surface preparation process must be selected based upon the most delicate of the metals on the panel.

36.5.2 Solder Mask Application

36.5.2.1 Liquid Masks. Solder masks applied in liquid form can be either photoimageable or not. Most solder mask in use today is photoimageable, meaning that after application it will be patterned in a photolithographic process. A non-imageable product must be applied only to those areas to be coated, and areas where metal or base material must be exposed cannot be coated.

36.5.2.1.1 Application—Liquid Photoimageable (LPI) Solder Mask. LPI solder masks are applied typically by screen printing, spray, or curtain coating. Although each method has pros and cons, all are used successfully in the industry.

Screen printing is the most common technique of applying solder mask. This technique utilizes a non-imaged, tightly stretched screen of precise construction and a squeegee to apply the solder mask through the screen onto the panel. The screening technology includes a wide range of equipment and techniques, from single-sided hand screening to fully automated double-sided equipment:

- *Single-sided coating (hand or flat bed)* In this application, each side of the panel is fully coated (except for a border on each side) with solder mask, one side at a time. The panel may be tack dried between coating the two sides, or the second side may be coated immediately using a dimple plate to protect the coating on the first side. It is advantageous to coat both sides of the panel before tack drying so that both sides see the same tack-drying cycle. One concern about this technique is the amount of solder mask that is pushed into the holes. Since this is a single-sided process, there is nothing to restrain the amount of mask that gets pushed into the holes, so it may be more difficult to develop all of the mask out of the holes.

- *Double-Sided Coating* Vertical double-sided screen printing applies solder mask to both sides of the panel or panels simultaneously. The screening units used are available in various levels of automation, up to fully automated screening units that are integrated with tack drying ovens. Because they apply mask to both sides at the same time, the units put less mask into holes, making it easier to develop mask out of holes—a particularly important consideration when working with small holes that must be free of solder mask. Front-to-back squeegee alignment is critical for putting the least amount of solder mask into the holes.

A key variable in screen printing is the screen mesh. Most applications utilize a non-calendared, nylon mesh material. These products are designated with the number of threads per inch and the diameter of the threads in microns. Typical examples of commonly used mesh counts are 86-120, 83-100, 86-100, 92-100 or 110-80. Supplier literature will provide a theoretical ink volume for each type that can be used to determine the relative difference in coating weight to be applied to the panel.

Table 36.1 provides an overview of the screen process key variables and the effect of operating a process at the extreme of that variable.

TABLE 36.1 Screening Process Variables and Effect Operating at the Extremes

Process Variable	Effect of Low	Effect of High
Mesh Tension	Mesh sticking to screen Poor quality printing Low coating thickness	Nonuniform coating across panel
Squeegee Pressure	Skips (areas with no solder mask)	Low coverage over circuits
Squeegee Speed	Lower circuit coverage	Higher coverage
Squeegee Shape	Very sharp edge, lower coverage	Slightly rounded edge, higher coverage
Squeegee Angle (from panel surface)	Lower coverage, Less ink in holes	Higher coverage, More ink in holes
Snap-off	Screen sticking to panels	Skips or difficult printing
Ink Viscosity	Lower coverage, More flow or sagging if too low	Higher coverage, Bubbles if too high

Spray coating accounts for a limited percentage of the solder mask coating. There is renewed interest in spray coating since it can allow more latitude in removing solder mask from holes. As the holes become smaller, some solder masks and processes have difficulty achieving clean holes after development. At the same time, because the solder mask is sprayed at reduced viscosity, the amount of solvent (VOCs) that is exhausted to the environment is significantly higher than for screen printing, the use of spraying may be limited in some localities.

Two basic types of spray equipment have been used for spray coating PCBs with solder mask, HVLP (high volume, low pressure), and electrostatic. HVLP spray systems are most common. Single- and double-sided spray units are available.

The solder mask is sprayed at a reduced percent solids compared to screen printing, so circuit coverage and tack

drying can be more of a problem, especially if the ink and/or spray guns are not heated. Heating of the ink allows more solvent to evaporate between the nozzle and the panel, resulting in a higher viscosity liquid on the panel. The higher viscosity theoretically allows greater circuit coverage with less ink.

The conventional HVLP spray process utilizes a low pressure stream of solder mask liquid that is atomized by a high volume stream of air. The atomized solder mask is directed to the PCB surface in a specific pattern so that as either the panel or the spray head(s) move, a uniform coating is applied to the panel. In some systems, the ink is heated just before spraying to lower its viscosity and aid in the evaporation of solvent between the spray nozzle and the panel. Typical process variables for HVLP spray include ink viscosity, ink (pot) pressure, atomization air pressure, conveyor speed, and ink and atomization air temperatures.

In a typical electrostatic spray application, the ink is atomized and given an electrostatic charge while the PCB panel is grounded to attract the ink particles. The intent is to limit the amount of overspray and provide a more even coating. In reality, with the infinitely variable PCB designs to be coated, there are often many ongoing adjustments required to minimize Faraday effects that cause uneven distribution of the spray. Often solder mask formulations need to be modified for effective use in electrostatic spray applications. The main process variables in electrostatic spraying are solder mask temperature and viscosity (dilution), bell speed and voltage, back plane voltage, and shaping air pressures. These variables are adjusted to provide a uniform coating of the desired thickness or weight.

Table 36.2 lists the process variables and the effect of operating at the extremes of that variable.

TABLE 36.2 Key Variables for Spray Coating and Effect of Low and High Levels for Each Variable

Process Variable	Effect of Low	Effect of High
Ink Viscosity	Low circuit coverage, Tack drying difficulties	Mottled or "orange peel" coating, excessive atomization, and overspray
Ink Temperature	Low circuit coverage	Possible clogging of lines or nozzle
Ink (Pot) Pressure	Thin coating, low coverage	Thick coating, drying problems
Atomization Air Pressure	Mottled surface	Excessive overspray
Wet Weight or Wet Film Thickness	Low circuit coverage	Thick coating, insufficient drying, and/or bubbling

Curtain coating is an application method where the panel to be coated is rapidly passed through a continuous falling "curtain" of solder mask. The curtain is created by pumping the solder mask through a die with a slot of controlled opening. The curtain falls vertically through an opening between two conveyors that carry the panels horizontally through the curtain, thus coating the panel on its upper side. Solder mask that is not coated onto the circuit board panels falls into a trough between the conveyors and is recirculated. The pump and conveyor speeds and the gap in the die control the coating thickness. Solder mask used in curtain coating applications must be coated at reduced viscosity or percent solids (as in spray applications), so the increased VOCs emitted to the atmosphere may limit curtain coating's acceptability in some localities.

Curtain coating is a highly productive process that gives uniform coating across panels. It has good flexibility for coating panels of different sizes (above a minimum) and gives very high material utilization.

The quality of the coating from this process is highly dependent upon the ability to maintain a uniform, stable

curtain of solder mask. The solder mask must be maintained at the specified temperature and viscosity to avoid coatings that are too thick or thin, streaks, skips, or breaks in the curtain that cause no coating in localized areas, commonly referred to as “blips.” Curtain coating is sensitive to circuit height and typically requires process changes as height increases to avoid skips in the coating. Thin panels may become airborne at high conveyor speeds, and thick panels may slip on the conveyor and not accelerate to proper coating speed.

Typical process variables for curtain coating include solder mask viscosity and temperature, pump pressure, die (gap) opening, conveyor speed, and air flow. Table 36.3 lists the key variables for curtain coating and the effect of operating the process at the extremes of each variable.

TABLE 36.3 Key Variables for Curtain Coating Solder Mask Application and the Effect If the Process is Operated at the Extremes of That Variable

Process Variable	Effect of Low	Effect of High
Ink Viscosity	Low circuit coverage, dewetting, Streaks or breaks in the curtain ("blips"), Sagging of the coating	Unstable curtain, streaks, improper leveling, skips
Ink Temperature	Coat at incorrect percent solids, Sagging of the coating, Thin coverage	Unstable viscosity, high solvent evaporation, Inconsistent leveling
Pump Pressure	Thin coating, low coverage	Thick coating, drying problems
Conveyor Speed	Excessive coating	Insufficient coating, Ink in holes, Teardropping on bottom side
Wet weight or wet film thickness	Low circuit coverage	Thick coating, Insufficient drying and/or bubbling, Sagging of coating
Air flow around the curtain	None	Unstable curtain, "blips," Nonuniform coating

36.5.2.1.2 Tack Drying—Photoimageable Solder Mask. LPI solder mask inks received from the supplier contain solvents to control the viscosity in the correct range for their intended application process. These solvents must be removed to harden the surface of the coating so that it may be handled and processed through the exposure step. Because the coated solder mask is wet and tacky, tack drying should closely follow the mask-coating process to reduce the possibility of handling damage and airborne debris becoming embedded in the wet ink. Care must be taken that panels do not touch each other in tack drying because they will mark each other and will not dry properly due to localized inadequate air flow across the panel surface. (Dry film, UV, and thermally cured solder masks do not require tack drying.)

Panels that have had insufficient tack drying will be sticky (phototools will stick to the solder mask); they may also exhibit “artwork marking,” where the pressure from the exposure process causes the mask surface to be smoothed, changing the cosmetic appearance of the surface. If solder mask has excessive tack curing, it will become difficult or impossible to develop—a condition called “lock-in.”

Oven types used for tack drying include batch ovens, tunnel ovens, and infrared (IR) ovens.

Batch ovens can be as small as a bench-top unit where panels may be inserted individually or as large as a walk-in oven that may be loaded with many panels in racks or carts. The wet panels are loaded through a door or doors that are gasketed or sealed to the operating area so that the vapors emitted are not exhausted into the work environment.

Total tack drying time in a batch oven is the sum of the ramp-up time plus the desired time at temperature. Ramp-up time of the panels is dependent upon the initial temperature of the oven, the heating capacity of the oven, the amount of makeup or purge air, and the loading (thermal mass) of the panels, racks, and carts placed in the oven at start-up.

Cure times are generally specified to be a specific time at temperature. Once the ramp-up time has been determined for the specific temperature and worst-case loading (generally a full oven load), the total time for the cure process is the ramp-up time plus the cure time. Oven doors should not be opened during a cure cycle because cure volatiles may escape into the environment and temperature will be lost and potentially cause incomplete curing.

Pros of using batch ovens include the ability to load large quantities of panels of any thickness or design at one time with minimal labor. Cons include having to wait for the oven to be empty before starting a new cycle. Opening of doors causes significant drop in temperature and may cause under

curing if the time is not adjusted for the time below curing temperature.

In conveyorized *tunnel ovens*, panels are generally placed in slots in the conveyor or in racks that ride on the conveyor. The main controls are temperature and conveyor speed. Exhaust from the oven serves the same purpose as purge air and should be regulated per the oven manufacturer's specification. Curing is typically uniform and is independent of panel design and construction.

With IR ovens, panels typically lay flat and are processed one at a time, and cure times are very rapid. Multiple cure recipes are usually needed to compensate for differences in panel design, materials, and construction. Proper handling of the exhaust is important, as with all curing ovens.

Several issues must be considered in the tack drying process:

- *Time at temperature* Proper curing requires specified time at temperature. Ovens should be set up with a profiler to ensure that variables such as oven loading, heating capacity, ramp-up time, and so on, compensated for when establishing process conditions.
- *Air flow* Air flow in ovens must be parallel to the panel surface so that there is uniform temperature across the panels and the solvent is swept away from the coated surface.
- *Debubbling time* With some solder mask applications, it is important to have some time (usually 5–10 min. maximum) for the coating to debubble before the tack drying occurs. This allows time for the bubbles to break and for the coating to heal itself.
- *Purge air* All ovens need fresh air to be drawn into the oven to replace solvent-laden air that is exhausted. Without sufficient purge, air panels will not dry properly.

- *Condensate* Volatiles from the solder mask can condense on cool surfaces of the oven and ductwork. This material must be cleaned periodically so that it does not plug air passages. Proper safety equipment should be worn during cleaning.

See Table 36.4 for a list of oven types and their advantages and disadvantages.

TABLE 36.4 Solder Mask Drying Ovens and Their Associated Advantages and Disadvantages

Oven Type	Pros	Cons
Batch	Productivity—large quantities with minimal manpower	Potential for nonuniform temperature
	Low investment	Opening oven doors causes temperature to drop
	Not dependent on panel design, materials, or construction	Cure time may be oven-loading dependent
	Consistency	
Tunnel	Consistency	More handling
	Uniformity	Higher investment
	Not dependent on panel design, materials, or construction	Thin panels may need a fixture to prevent them from bending
Infrared (IR)	Very fast cycle time	Multiple recipes usually required to compensate for different materials, designs, and constructions
	Productivity	Cannot cure every PCB design/construction
		Requires automation or extra handling
		High investment

36.5.2.1.3 Exposure. Exposing photoimageable solder mask requires equipment that provides the needed intensity of light of the proper wavelength to expose the solder mask to an extent that the exposed mask will withstand the developing process without washing away, lifting, or getting surface attack.

Exposure equipment must provide a means of holding a phototool in intimate contact with the surface of the panel being exposed and provide the required amount of light (millijoules/cm^2) of the needed wavelength distribution (which may depend on the solder mask) at the appropriate intensity (mW/cm^2). Unfortunately, many exposure devices that are used for exposing solder mask are substandard, including many units that were designed many years ago for exposing primary imaging photoresist. Modern units have high-intensity lamps (7 kW or higher) and sufficient lamp and exposure frame cooling to provide a high-quality image very quickly.

Lamp intensity and energy output should be monitored routinely with a radiometer sensitive to the appropriate wavelength to verify that the lamps are performing as expected. Intensity will decrease with lamp hours, making exposure times become longer. At the same time, the infrared output will increase, potentially causing frame cooling issues. Hot exposure frames cause artwork to stick to the mask, resulting in artwork marking or mask to transfer to the phototool.

Laser units are available for exposing photoresist that have been used for exposing solder mask. These solder masks may be specially formulated to be sensitive to the laser wavelength. Laser imaging eliminates solder mask registration problems, but is not as productive as conventional exposure. Equipment cost is very high compared to conventional lamp exposure equipment.

Underexposure will result is insufficient polymerization to withstand the development process properly without damage to the solder mask. Typical symptoms may include a dull or chalky surface, lifting of small features (e.g., solder dams), excessively undercut sidewalls, or lifted mask.

Overexposure causes image growth where the exposed feature is larger than on the artwork and openings in the solder mask will be smaller. If the growth is excessive, the mask may grow onto the pads.

36.5.2.1.4 Development. Development of the unexposed solder mask material must be sufficient to clean out completely the smallest holes that must be free of mask.

Photoimageable solder masks may be developed in either aqueous or solvent chemistries. The developer chemistry needed depends on the mask formulation. In the development process, solder mask that has not been exposed to UV light and polymerized is washed away, or developed, from the PCB panel to reveal the desired pattern of solder mask.

For aqueous development, the chemistry is a warm, mildly alkaline (pH 10.6–11.3) solution of sodium carbonate (Na_2CO_3) or potassium carbonate (K_2CO_3). Proprietary chemistries are also available. Antifoam is generally used to control foaming as the development solution loads with developed mask.

Solvent-developing chemistry typically uses gamma-butyrolactone (also known as “GBL” or butyrolactone) or butyl carbitol (2-(2-Butoxyethoxy)ethanol) solvent.

The development process must be set up to ensure that the smallest holes are free of undeveloped solder mask. This is very different from photoresist because the breakpoint will often be 10 to 15 percent of the development chamber instead of nearly 50 percent with photoresist.

Key process variables for the development process are the time in the developer and rinse sections; solution

temperature, pressure, and nozzle type; flow rate; and configuration.

It is very important to have an inspection step immediately after development to check for registration, mask in holes, feature resolution, dam retention, lifting, and so on. Once the panels have been cured. it is significantly more difficult to strip and rework the solder mask, and the rework process is more likely to cause the panels to be scrapped.

36.5.2.2 Dry-Film Solder Mask (DFSM) Application.

The process for DFSM differs from LPI solder mask only in the application step. Surface preparation, exposure development, and cure are the same as for LPI solder masks.

36.5.2.2.1 Application with Vacuum Lamination. DFSMs typically have no solvent in them to enable them to conform to circuits without entrapping significant amounts of air along or between circuit traces. To apply these films to circuit topography, a laminator must be able to laminate panels in a vacuum chamber. The predominant type of vacuum laminator has heated upper and lower platens. The panel or boards to be coated will have DFSM gently applied (without any pressure) to one or both sides and are placed into the vacuum chamber formed between the upper and lower platens. The platens are closed together and a seal is formed. Vacuum is drawn in the chamber. When a specified time has been reached (determined by the board type and thermal mass, DFSM type and thickness, and board/panel plated circuit height), the flexible diaphragm on the upper platen (which had been held tightly against the upper platen surface by vacuum) is released to slap down onto the panel surface. The heat will have made the DFSM plastic so that it will conform to the circuits, and the vacuum prevents poor lamination along circuits. The lamination is completed when the platens separate and atmospheric pressure forces the DFSM into all voids.

36.5.2.2.2 Roll Lamination. Lamination of DFSM with a standard hot roll laminator is unacceptable for all except the least demanding applications. It is impossible to laminate a flat film of solder mask to PCB topography without trapping air along circuits. There are vacuum hot roll laminators that will work satisfactorily, but these are not widely available.

36.5.2.3 Non-Imageable

36.5.2.3.1 UV and Thermally Curable Solder Masks. Because these products are not photoimageable, they must be applied with patterned screen printing in the exact pattern that is needed on the finished PCB. After their application, they are cured by the appropriate cure recipe as dictated by the supplier. There is no opportunity to develop off solder mask from areas where it is unwanted, so registration of the screen to the panel is very important.

36.5.2.3.2 Ink Jet Application. This technique utilizes digital data and ink jet technology to coat solder mask only in areas where it is wanted. This eliminates the photoimaging steps and should reduce or eliminate registration problems. Several machines are now being used in production and the application is growing. Most are UV-cured machines are being used in production for solder mask application.

36.5.3 Curing

36.5.3.1 Cure Purpose. All solder mask products require a cure step or process for the solder mask to achieve the desired material properties. Curing typically increases hardness and the thermal and chemical resistance. The desired curing process is determined by the specific solder mask used. Consult the technical data sheet for the product and follow the supplier’s recommendations for the appropriate cure.

36.5.3.2 Types of Cure—UV, Thermal, IR.

36.5.3.2.1 Thermal Cure. Nearly all solder masks require a thermal cure. It is generally specified as a specific time at temperature. When calculating the correct time, the fabricator must add the temperature ramp-up time to the required time at temperature to arrive at the total time in the oven. For a conveyorized oven, a thermal profile will show the time above the minimum temperature.

If the thermal cure is to be accomplished with an infrared oven, the time will be much shorter but temperatures will be far greater than for a convection oven. Also, a number of recipes are usually needed to compensate for materials with different IR absorbance and panels with different thermal mass or thickness.

36.5.3.2.2 UV Cure. Some solder masks require high-intensity UV light to cure. This is typically applied in a conveyorized UV curing unit. Calibration of the curing unit is important to ensure the solder mask is cured properly.

36.5.3.3 Effects of Undercure and Overcure.

Improperly cured solder mask can exhibit poor properties that will become apparent in subsequent processing. Care must be taken to ensure that the solder mask is cured according to the supplier’s recommendations. The following are some of the potential problems caused by improperly cured solder mask.

Undercure problems include:

- Blistering or adhesion loss in final finish or assembly
- High ionic contamination
- Residues from assembly soldering
- Solder balling
- Handling damage and soft coating

Overcure problems include:

- Embrittlement and cracking
- Adhesion loss

36.5.4 Stripping Solder Mask

Stripping of solder mask is something to be avoided, but at times is required due to problems such as misregistration, incorrect or wrong sized artwork, handling damage, and so on. It is important to recognize problems as early in the process as possible since the stripping process must be more aggressive after each process step.

36.5.4.1 Stripping after Coating. At this stage, the solder mask may be removed easily. An LPI solder mask can simply be developed off. (*Note:* The mask should be tack dried first to avoid contaminating the developer with wet mask and/or solvent.). UV and thermal mask must be removed manually with an appropriate solvent.

36.5.4.2 Stripping after Photoimaging. The stripping task becomes more difficult. Aggressive chemistries, typically highly caustic and at high temperature, are required. These chemistries are aggressive and the process, if not controlled, can damage the butter coat of the laminate and render the panel scrap. Small holes filled with solder mask may not be able to be cleaned out in the stripping operation without damaging the panel.

36.5.4.3 Stripping after Cure. Stripping solder masks is most difficult at this stage, and doing so in fact may be impossible for some solder masks. The time required to strip the solder mask may allow exposed portions of the laminate to become damaged and cause the panel to be scrapped. Every effort should be made to identify panels needing stripping before curing.

36.6 VIA PROTECTION

Via protection is an increasingly complex issue for PCB designers and fabricators. There are multiple options for protection—organic and conductive, platable or not, before or after final finish, and more. The materials and processes for each type are not the same, so there is no single answer, and few answers that are easily performed with high productivity. Inks for plugging come in a variety of processing types, including thermal cure, UV cure, photoimageable, conductive, platable, and so on. The panel design will narrow the choice for the specific application.

36.6.1 IPC-4761, "Design Guide for Protection of Printed Board Via Structures"

IPC-4761, published in July 2006, gives excellent guidance for how best to protect vias and what not to do. It does not give specifications for the plugging materials themselves, but a future document is expected to do so. This document calls out a number of classes of via protection that can be used by designers and fabricators.

One very important message from this document is that vias should be protected from both sides, not only one side. If single-sided protection is used before an "inert" final finish, a ring void of copper results at the barrel-plug interface that is subject to corrosion due to entrapped microetch, flux, or other corrosive chemistry. Also, some of these materials leach out in subsequent processes and can kill plating baths, cause high ionics, induce electrochemical migration, or present other long-term reliability concerns.

36.6.2 Material Specifications

Although there are no “official” specifications for the materials used for plugging, there are some specifications that apply to solder mask that should be considered when using a material other than solder mask to protect vias. UL94 flammability and IPC-SM-840 tests—including especially resistance to solvents and cleaning agents, as well as non-nutrient testing—may be necessary. Dependent upon the specific circuitry design, other specific tests from IPC-SM-840 or other specifications may be appropriate.

36.6.3 Material Selection Considerations—Solder Mask versus Specialty Inks

36.6.3.1 Shrinkage—Percent Solids. LPI solder masks have solvent in the formulation to control viscosity and tackiness. Drying the solvent causes the plug of mask in the via to shrink, typically causing a dimple and some thinning of the coverage on the knee of the hole. This may not be a problem if the plug is covered with another coating of solder mask or if the annular ring of the via does not pick up solder or other final finish. Specialty hole plugging inks are available that are very high in solids and shrink very little, as are 100 percent solid inks that eliminate this concern.

36.6.3.2 Platability—Cu Adhesion. More frequently, designers are specifying that the material used to plug the hole be platable so the real estate can be reclaimed as in via-in-pad designs or in subcomposite structures. Such applications require a material that can be roughened, catalyzed, and plated with good copper adhesion.

36.6.3.3 Image Definition. If the vias to be filled are in very close proximity to areas that must be solderable (e.g., surface-mount technology [SMT] pads) it may be desirable or, mandatory to utilize a plugging product that is photoimageable to ensure the ink does not encroach upon solderable surfaces.

36.6.3.4 Other Properties. One property important for vias needed to conduct thermal energy is thermal conductivity. Products used to fill such vias are generally highly loaded with a material with good conductivity such as silver or copper. Some designers believe that boards that must operate at high temperatures should have plugging materials with low coefficient of thermal expansion (CTE) and high glass transition temperature (T_g), but there is little data to substantiate benefits of such materials.

36.7 SOLDER MASK FINAL PROPERTIES

Final properties are often characterized into physical, electrical, mechanical, and chemical properties. Most people who specify solder mask utilize the criteria in the IPC-SM-840 document when specifying desired mask performance. There are other industry and regional specifications but the IPC specification is recognized worldwide.

36.8 LEGEND AND MARKING (NOMENCLATURE)

Many boards still require legend and marking to identify part numbers and component locations, for company logos, date

codes, and a multitude of other reasons. These can be etched into the copper or, more typically, added in a separate process after solder mask. For good legibility, materials are of a color that contrasts with the solder mask color.

36.8.1 Types

36.8.1.1 UV. These materials are not photoimageable, but are applied in the specific desired pattern through a patterned screen and then are cured with high-intensity UV light.

36.8.1.2 Thermal. These materials are not photoimageable, but are applied in the specific pattern desired through a patterned screen and then are thermally cured, generally in a batch or conveyorized oven.

36.8.1.3 Photoimageable. These inks are applied to large areas of panels or over complete panels, as with an LPI solder mask. They are tack dried, imaged, developed, and cured, often at the same time as the solder mask is cured. The advantages of these products are that they eliminate expensive screen making and achieve excellent resolution, even over the topography of circuits.

Special inks have been formulated for LPI legend applications that have higher pigment loading. The advantage of these inks is that they can be coated much thinner while achieving good color contrast. This increases the productivity through the tack and developing processes and gives a more robust finished product since it is thinner and less likely to be chipped. Standard solder masks of contrasting color may be used but they will have to be coated thicker to achieve similar contrast. The higher

sidewall thickness makes the legend more susceptible to chipping.

36.8.1.4 Ink Jet. These are actually UV and/or thermal inks that are applied with an ink jet. A limited number of these machines are in production as of early 2007. Initial equipment cost is very high, as is the price of ink, and progress in productivity is expected in the future.

36.8.2 Legend Specifications

36.8.2.1 IPC. No approved IPC specification exists for legend inks. A committee is drafting a specification, IPC-4781, that should be issued in 2008.

36.8.2.2 Military. The military has an obsolete specification that was written years ago around a two-part epoxy ink that most MIL applications still specify. Many of the criteria (such as shelf life, pot life, composition, etc.) in this specification are irrelevant to the final legend performance, but they are still enforced as long as the specification is used. More recently the specification for legend ink called out for many military applications is CID A-A-56032D, entitled “Commercial Item Description—Ink, Marking, Epoxy Base.” Although military specifications call out epoxy-based marking inks, a number of fabricators have had other inks approved on a waiver basis for military applications.

36.8.2.3 UL94. When areas of legend ink on the board are larger than a UL flame strip (½ × 5 in.), it is treated as if the legend is another coating that needs UL qualification. If all areas are smaller than the flame strip dimension, no separate UL qualification is needed.

36.8.3 Legend Performance

36.8.3.1 Legibility and Resolution. The legend must be readable to be useful. As circuitry becomes more dense, the feature sizes needed for legend become smaller also, causing processes to be reestablished to give the desired quality. Some fabricators have switched to a photoimageable (LPI) legend to give the desired resolution for the legend on high-density circuitry.

36.8.3.2 Adhesion. The legend must be applied to a clean, dry surface and be properly cured to achieve optimum adhesion. This can be a challenge when legend is applied after HASL or other final finish that could leave a residue (such as HASL flux) on the surface. Legend adhesion must be evaluated in combination with the solder mask and its processing. Different legend materials have different adhesion to different solder masks.

36.8.3.3 Final Finish Compatibility. Like solder mask, legend materials that are applied before the final finish must survive the final finish processes and chemistries. Not all legend materials will survive all finishes and these must be qualified together, the same as with solder mask.

CHAPTER 37
ETCHING PROCESS AND TECHNOLOGIES[a]

Gareth Parry
Draig Technologies Inc., Stouffville, Ontario, Canada

37.1 INTRODUCTION

One of the major steps in the chemical processing of subtractive printed boards is *etching*, or removal of copper, to achieve the desired circuit patterns. Etching is also used for surface preparation with minimal metal removal (microetching) during innerlayer oxide coating and electroless or electrolytic plating. Technical, economic, and environmental needs for practical process control have brought about major improvements in etching techniques. Batch-type operations, with their variable etching rates and long downtimes, have been replaced completely with continuous, constant-etch-rate processes. In addition, the need for continuous processing has led to extensive automation along with complete, integrated systems.

The most common etching systems are based on alkaline ammonia and cupric chloride. Other systems include peroxide–

sulfuric acid, persulfates, and ferric chloride. Process steps include resist stripping, precleaning, etching, neutralizing, water rinsing, and drying. This chapter describes the technology for etching high-quality, fine-line (0.0015- to 0.003-in) circuits in high volume at a practical cost, as well as continuous processing, constant-etch rates, and control at high dissolved copper capacities. Increasingly, the production of uniform and constant feature geometries calls for precision and statistically robust control of the circuitization processes and materials.

There remains the ever increasing need to balance the process selection according to the factors of cost, environmental and regulatory compliance, stable factory productivity, low worker intervention requirements, compatibility with board design, and construction innovations. It is significant that environmental concern has eliminated the use of chromic–sulfuric acid and ammonium persulfate etchants and chlorinated solvents. Limitations on chlorine gas and volatile organic emissions loom as a significant factor in determining future process choices, and pressure to eliminate brominated compounds and lead content may have consequences for processing mandated by material developments. More than ever, the simplification of process selection and vendor support appear to drive process selection in the industry.

Typical procedures are given for etching organic (i.e., dry film) and metal-resist boards, and for innerlayers. Strippers and procedures for resist removal are described based on resist selection, cost, and pollution problems. The properties of available etchants are also described in terms of resist compatibility, control methods, ease of control, and equipment maintenance. Other considerations include chemical and etchant effects on dielectric laminates, etching of thin-clad copper and semiadditive boards, solder mask on bare copper (SMOBC), equipment selection techniques, production capabilities, quality attained, and facilities.

37.2 GENERAL ETCHING CONSIDERATIONS AND PROCEDURES

Good etching results depend on proper image formation in both organic innerlayer print-and-etch and plated-metal etch resists. Etch personnel must be familiar with screened, photosensitive, and plated resists commonly used. The etching of printed boards must begin with suitable cleaning, inspection, and preetch steps to ensure acceptable products. Increasingly, metal foil or plating uniformity in structure thickness and freedom from coatings and defects must be maintained to achieve uniform small-feature definition. Plated boards also require careful and complete resist removal. The steps after etching are important because they remove surface contamination and yield sound surfaces. This discussion considers the various types of resists and outlines typical procedures used to etch printed boards using organic and plated resist patterns.

37.2.1 Screened Resists

Screen printing is a common method for producing standard copper-printed circuitry on metal-clad dielectric and other substrates. The etch-resist material is printed with a positive pattern (circuitry only) for copper etch-only boards or with a negative image (field only) when plated through-holes and metal resist are present.

The type of resist material used must meet the requirements for proper image transfer demanded by the printer and for stripping chemistry compatibility. From the metal etcher’s point of view, the material needs to provide good adhesion and etch-solution resistance; be free of pinholes, oil, or resin bleed-out; and be readily removable without damage to substrate or circuitry.

Typical problems are excessive undercutting, slivers, unetched areas, and innerlayer shorts in multilayer boards. In addition, conductor line lifting may occur when the copper-to-laminate peel strength (or surface contamination) is below specification.

37.2.2 Hole Plugging

Plugged-hole, copper-only boards use alkaline-soluble screen resists in a unique manner. The technique, called *hole plugging*, makes the SMOBC board possible. This technique can be used with screened images and to augment *tent-and-etch* processing for small annular ring structures.

37.2.3 UV-Cured Screen Resists

Ultraviolet-cured solventless systems are available for print-and-etch and plating applications. These products are resistant to commonly used acidic plating and etching solutions. Stripping must be evaluated carefully.

37.2.4 Photoresists

Dry-film and liquid photoresist materials are capable of yielding the fine-line (0.0015 to 0.003 in) circuits needed for production of surface-mount circuit boards. Like screened resists, photo-sensitive resists can be used to print either negative or positive patterns on the metal-clad laminate. Although dry-film and liquid materials differ in both physical and chemical properties, they are considered together for our purpose.

In general, both positive- and negative-acting resists offer better protection in acidic rather than alkaline solutions; however, negative-acting types are more tolerant of alkaline solutions. Negative resists, once exposed and developed, are

no longer light sensitive and can be processed and stored in normal white light. The positive resists remain light sensitive even after developing and must therefore be protected from white light. Liquid photoresists, although less durable, are capable of finer line definition and resolution.

Positive-acting resists are subject to the same problems as are negative-acting resists, although they may be easier to remove cleanly, after exposure, from areas to be etched or plated. Problems related to plating photoresist-coated boards are reviewed in Chap. 33.

37.2.5 Plated Etch Resists

At present, the most extensive use of metal-plated resists is found in the production of double-sided and multilayer plated-through-hole circuit boards. The most commonly used resists are tin (matte and bright surface). Solder plate (60 percent Sn, 40 percent Pb) continues to be used on some reflow-treated solderable coating situations, but it is not favored for a sacrificial resist that is to be removed for SMOBC processing. Nickel, tin/nickel, and gold are occasionally used. Silver is used to some extent for light-emitting and liquid crystal applications. Details concerning the deposition of these metals are given in Chap. 35. The use of these resists is described in the following paragraphs.

37.2.5.1 Tin Plating. Thin tin deposits (0.0002 in) are used to make SMOBC boards where the tin etch resist is stripped after etching. Alkaline ammonia etchants are usually favored. Other etchants, such as sulfuric acid–hydrogen peroxide and ammonium persulfate–phosphoric acid, have been especially formulated for bright tin. Tin plating (directly over barrier layers of nickel or tin/nickel) has been used because of its optimum solderability. Cupric and ferric chloride etchants attack tin and are not used.

37.2.5.2 Solder Plate. Tin/lead solder (0.0003 to 0.001 in thick) is the plated etch resist for “fusing” into a solderable finish. The 60Sn/40Pb alloy offers good etchant resistance with few problems but must be treated with a brightening solution to retain solderability. Increased reliability may be achieved by the use of solder plate over tin/nickel.[1] Thin solder deposits (0.0002 in) can be used for the SMOBC process but have no benefit over tin plating for this purpose. The most suitable etchants are alkaline ammonia and sulfuric acid–hydrogen peroxide. Ferric and cupric chloride acid etchants cannot be used because of solder plate attack. Postetch neutralization rinses are needed, especially with alkaline systems, to rinse away etchant residues and to maintain optimum surface properties.

37.2.5.3 Tin/Nickel and Nickel. Tin/nickel alloy (65 percent Sn, 35 percent Ni) and nickel plate, used as is or overplated with gold, solder, or tin, are also capable metal resists for etching copper in alkaline ammonia, sulfuric acid–hydrogen peroxide, and persulfates.

37.2.5.4 Gold. With an underplate of nickel or tin/nickel, gold provides excellent resistance to all the common copper etchants. Some etchants have a slight dissolving effect on gold.

37.2.5.5 Precious Metals and Alloys. Rhodium has been described as being a suitable resist for edge connectors on boards; however, the plating process is difficult to control. When plated over nickel, rhodium tends to be thin and porous and to lift during etching. Because of varying surface properties, 18-karat alloy gold and nickel/palladium must be evaluated carefully when used as substitutes for pure gold systems.

37.2.5.6 Silver. Although silver is not used on most printed boards (MIL-STD-275 states that it shall not be used), it has found some applications for camera, light-emitting, and liquid

crystal devices. Copper etching using silver as resist can be done with alkaline ammonia solutions. Silver loss is about 0.0001 in/mm.

37.2.5.7 Etching Procedures for Plated-Metal Resists. Etching of the metal-resist-plated boards begins with removal of the plating resist using commercial strippers. The stripping process must be sufficient to remove resist trapped under plating edges. Gold, solder, and tin resists must be handled carefully because they scratch very easily. Tin/nickel alloy and nickel plate, however, are very hard and resistant to abrasion.

The procedure after etching includes thorough water rinsing and acid neutralizing to ensure removal of etchant residue on the board surface and under the traces. Alkaline etchants are followed by treatment with proprietary ammonium chloride acidic solutions, ferric and cupric chloride with solutions of hydrochloric or oxalic acid, and ammonium persulfate with sulfuric acid. Alkaline cleaning is used for tin/lead boards etched in chromic–sulfuric acid. Etchant residue not removed before drying or reflow results in lowered electrical resistance of the dielectric substrate and in poor electrical contact and soldering on the conductive surfaces.[2] Care must be taken to minimize undercutting and overplating to eliminate slivers of plating breaking off and bridging circuitry.

A problem common to etching printed boards is not having the entire area etch clean at the same time. This occurs when etch action is more rapid at the edges of printed areas than in a broad expanse of copper. If very fine patterns and lines are required, the result can be loss of the pattern due to undercutting, especially when the board is left in the etcher until all the field copper has etched away. Modern etchers with reduced pooling of etchant have reduced this problem.

Fine-line boards in high-volume production may require special fine-line etchants, high-resolution photoresists, thin-clad laminates, controlled plating distribution, and thin base foil processing. Care must be taken to balance etching and

thickness factors. In some cases, fine-line etchant additives have actually made cleanout more difficult in spaces of 0.003 in and narrower.

37.3 RESIST REMOVAL

The method used for resist stripping must be carefully evaluated when a resist is selected. The effect on board materials, cost and production requirements, and compliance with safety and pollution standards must be taken into account. Solvent-based stripping solutions are under significant environmental pressure. Chlorinated solvents and cyclic compounds (toluene, xylenes, etc.) have been banned, and many glycol ethers are restricted. In spray applications, care must be taken to capture or eliminate VOC emissions. For these reasons, aqueous or primarily aqueous stripping systems are necessarily widely used.

37.3.1 Screen Resist Removal

Alkali-soluble resist inks are generally preferred. Stripping in the case of thermal and UV-curable resists is accomplished in 2 percent sodium hydroxide or in proprietary solutions. The resist is loosened and rinsed off with a water spray. Adequate safety precautions must be taken, since caustics are harmful.

Conveyorized resist-stripping and etching machines use high-pressure pumping systems that spray hot alkaline solutions on both sides of the boards. Certain laminate materials such as the polyimides may be attached by alkaline strippers. Measling, staining, or other degradation is noted when strippers attack epoxy or other substrates. Control of concentration, temperature, and dwell time usually can prevent serious problems.

Screened vinyl-based resists are removed by a dissolving action in solutions of chlorinated, petroleum, or glycol ether

solvents. Methylene chloride and toluene (both currently not usable) were used extensively in cold stripper formulations. The most common strippers are acidic formulations that contain copper brighteners and swelling, dissolution, and water-rinsing agents. The usual procedure for static tank stripping involves soaking the coated boards in at least two tanks of stripper. Excessive time in strippers is to be avoided because of attack on the butter (top epoxy) coat, especially on print-and-etch or single-sided boards. Water is a contaminant in most cold strippers.

37.3.2 Photoresist Removal

37.3.2.1 Dry Film. Dry-film resists have been formulated for ease of removal in aqueous alkaline solutions. Strippers are available for both static tank and conveyorized systems, although conveyorized systems are preferred because the spray action aids in separating the resist from the copper surfaces and washing it off the panel. Prompt processing after etching avoids resist adhesion “lock-in,” which can make removal difficult. Aqueous-alkaline stripping results in partially undissolved residues of softened resist films. These residues are captured in a filter system and disposed of in accordance with waste-disposal requirements. Design and availability of specific filters to match the character of the “skins” can be a significant factor in the selection of the proper resist. Environmental caution must be taken to properly evaluate and dispose of resist residues. Metal content (particularly lead) may lead to classification of these residues as toxic waste.

37.3.2.2 Negative-Acting Liquid Photoresist Removal. Negative-acting, liquid-applied photoresist can be readily removed from printed boards that have not been baked excessively. Baking is critical to removal because it relates to the degree of polymerization. Since overbaking is also damaging to the insulating substrates, processes should stress minimal baking—only enough to withstand the operations

involved. The negative-acting resists are removed by using solvents and commercial strippers. In this case, the resist may not dissolve; instead, it softens and swells, breaking the adhesive bond to the substrate. Once that has taken place over the entire coated area, a water spray is used to flush away the film.

37.3.2.3 Positive-Acting Photoresist Removal. Positive-acting photoresists are removed in commercial organic and inorganic strippers if baking has not been excessive. Removal by exposure to UV light and subsequent dipping in sodium hydroxide, TSP, or other strong alkaline solutions is also effective. Overbaking makes removal difficult. Machine stripping is done in a solution of 0.5*N* sodium hydroxide, nonionic surfactants, and defoamers.

37.3.3 Tin and Tin/Lead Resist Removal

In SMOBC processing, the metal-plated resist is removed to present a flat, clean copper surface for solder mask definition. Tin/lead alloys can be stripped in oxidizing fluoride solutions such as fluoboric acid and hydrogen peroxide or ammonium bifluoride with hydrogen peroxide or nitric acid. (Caution: machine construction must be made compatible with fluorides by elimination of titanium and glass components.) Commercial formulations are available to be used inline after the etch machine rinses. Accumulations of spent solution or filtered lead fluoride deposits must be treated as hazardous waste and have been accepted by solution vendors for treatment and disposal costs. Modern applications usually use lead-free tin plating resists, which can be fluoride containing as previously discussed, or compounds of ferric chloride followed by nitric acid. In either case, feed-and-bleed solution management with filtration and periodic chamber cleanout has been successful.

37.4 ETCHING SOLUTIONS

This section is a survey of the technology and chemistry of the copper etching systems in common use. Selection of practically available etchants has been limited by economic, operational, and (environmental) regulatory concerns. Fabricators have been forced into practical trade-off decisions to suit situations. Two etchants in particular, chromic–sulfuric acid and ammonium persulfate, are no longer practical considerations due to environmental pressures. Other formulations and choices have been modified to suit these pressures.

There are two basic etchant needs to be met. The first is traditional foil etching for print-and-etch, plate/tent and etch, and pattern plate and etch. Virtually all processes use constant-rate systems for alkaline ammonia or cupric chloride etchants for this purpose or ferric chloride. The second need is developing technology for specific precision very fine-line etching—including foil thinning and thin metallization clearout for HDI constructions and fine features. (See Sec. 37.7 for additional discussion and mention of additional chemistries that may be useful for these applications.)

Continuous constant-rate systems with process automation represent current practice in production etching. These systems feature feed and bleed of replenishment chemicals under control of process instrumentation that monitors and responds to real-time changes in properties of the working solution. The “bleed” stream of the working composition etchant is usually returned to suppliers for copper reclamation and chemical recycle. The resulting degree of constant etching rate allows for stable and repeatable performance to achieve practical manufacturing processes. However, as demands for higher precision increase, further sophistication in controls will be necessary.

Key factors for selecting an etching chemistry include

- Board design requirements
- High yield
- Compatibility with resist
- Etch rate (speed)
- Difference of speeds and sidewall topography with respect to ammonia/cupric/ferric etchants
- Equipment required for process control of etch rate, regeneration, and replenishment
- Ease of equipment maintenance
- By-products disposal and pollution control
- Operator and environmental protection

The preceding factors serve to evaluate copper etchants to be used. Introduction, chemistry, properties, and problems are given in this section, along with suggestions for selection and control.

37.4.1 Alkaline Ammonia

Alkaline etching with ammonium hydroxide complexing is increasingly used because of its continuous operation, compatibility with most metallic and organic resists, high capacity for dissolved copper, and fast etch rates. Continuous (open-loop) spray machine chemical control systems are universally used. This operation provides constant etch rates, high work output, ease of control and replenishment, and improved pollution control. However, rinsing after etching is critical, and the ammonium ion introduced to the rinses presents a waste-treatment problem. On-site closed-loop regeneration with chemical recycling is commercially available but not routinely practiced because of facility requirements, capital cost, fluctuating economics depending on copper commodity pricing, and worker requirements. The general economical and environmentally appropriate operating strategy is to recycle the by-product etchant products under

contract to a supplier who reclaims or reconstitutes the copper contained and regenerates the ammoniacal constituents into a reformulated replenisher solution for return to fabricators.

37.4.1.1 Chemistry. The main chemical constituents function as follows:

1. Ammonium hydroxide (NH_4OH) acts as a complexing agent and holds copper in solution.
2. Ammonium chloride (NH_4Cl) increases etch rate, copper-holding capacity, and solution stability.
3. Copper ion (Cu^{2+}) is an oxidizing agent that reacts with and dissolves metallic copper.
4. Ammonium bicarbonate (NH_4HCO_3) is a buffer and as such retains clean solder holes and surface.
5. Ammonium phosphate [$(NH_4)_3PO_4$] retains clean solder and plated through-holes.
6. Ammonium nitrate (NH_4NO_3) increases etch rate and retains clean solder.
7. Additional additives are included in most formulations to enhance speed and/or sidewall protection. Thiourea or its derivatives are often used, although a newer thiourea-free formulation with improved undercut protection is available.
8. Continuous operations consist of single-solution makeup buffered to a pH of 7.5 to 9.5.

Alkaline etching solutions dissolve exposed field copper on printed boards by a chemical process of oxidation, solubilizing, and complexing. Ammonium hydroxide and ammonium salts combine with copper ions to form cupric ammonium complex ions [$Cu(NH_3)_4^{2+}$], which hold the etched and dissolved copper in solution at 18 to 30 oz/gal.

Typical oxidation reactions for closed-loop systems are shown by the reaction of cupric ion on copper, and air (O_2) oxidation of the cuprous complex ion:

$$Cu + Cu(NH_3)_4^{2+} \rightarrow 2Cu(NH_3)_2^{+} \quad (37.1)$$

$$2Cu(NH_3)_2^{+} + 2NH_4^{+} + 2NH_3 + \tfrac{1}{2}O_2 \rightarrow 2Cu(NH_3)_4^{2+} + H_2O \quad (37.2)$$

There is strong evidence that the etching rate is dependent on the diffusion of $Cu(NH_3)_2^{+}$ from the copper surface [Eq. (37.1)] into the bulk of the active solution, where oxidation per Eq. (37.2) occurs.[3] Etching can be continued with the formation of $Cu(NH_3)_4^{2+}$ oxidizer from air during spray etching and as long as the copper-holding capacity supported by Cl^- ions is not exceeded.

37.4.1.2 Properties and Control. Early versions of alkaline etchants were batch operated. They had a low copper capacity, and the etch rates dropped off rapidly as copper content increased.[4–6] It was found to be necessary to add controlled amounts of dissolved oxidizing agents to speed up the rate and increase copper capacity at a constant temperature. Batch operation is no longer supported by commercial suppliers.

Etching solutions are operated at 120 to 130°F and are well suited to spray etching. Efficient exhaust systems are required because ammonia fumes are released during operation.[7] Etching machines must have a slight negative pressure and moderate exhausting to retain the ammonia necessary for holding dissolved copper in solution. Care must be taken that sufficient fresh air to supply needed O_2 is introduced to balance the extraction. Currently available solutions offer constant etching of 1 oz (35 µm) copper in 1 min or less, with a dissolved copper content of 18 to 24 oz/gal.

37.4.1.3 Continuous Systems. A practical method of maintaining a constant etch rate with minimal pollution uses automatic feeding controlled by specific gravity or density.[6] The process, which is generally referred to as *bleed and feed*, is illustrated in Fig. 37.1. As the printed boards are etched,

copper is dissolved, and the density of the etching solution increases. The density of the etchant in the etcher sump is sensed to determine the amount of copper in solution. When the density sensor records an upper limit, a switch activates a pump that automatically feeds replenishing solution to the etcher and simultaneously removes etchant until a lower density is reached. An elegant by-product of this technique is the introduction of the replenisher into the first rinse stage following the etcher. The rinse captures the copper from the panel and reintroduces it to the etcher, where it is eventually eliminated to the by-product tank with the rest of the copper. When used with aqueous processing photoresists, it has been found that low pH (7.9 to 8.1) aids etch reliability. However, maintaining this pH by adjustment of exhaust extraction has been difficult. Measurement of pH and controlled addition of anhydrous ammonia into the etchant has improved consistency. It has been established that control of free ammonia as well as ammonium chloride and oxygen levels are needed to stabilize etching rates. Direct injection of oxygen has also been attempted to stabilize the etching rates between low and high copper etching demand process utilization periods. Typical operating conditions are as follows:[b]

Temperature	120 to 130°F (49 to 50°C)
pH	8.0 to 8.8
Specific gravity at 120°F (49°C)	1.207 to 1.227
Baumé, Be°	25 to 27
Copper concentration, oz/gal	20 to 22
Etch rate, 0.001 in/mm	1.4 to 2.0
Chloride level	4.9 to 5.7 mol/L

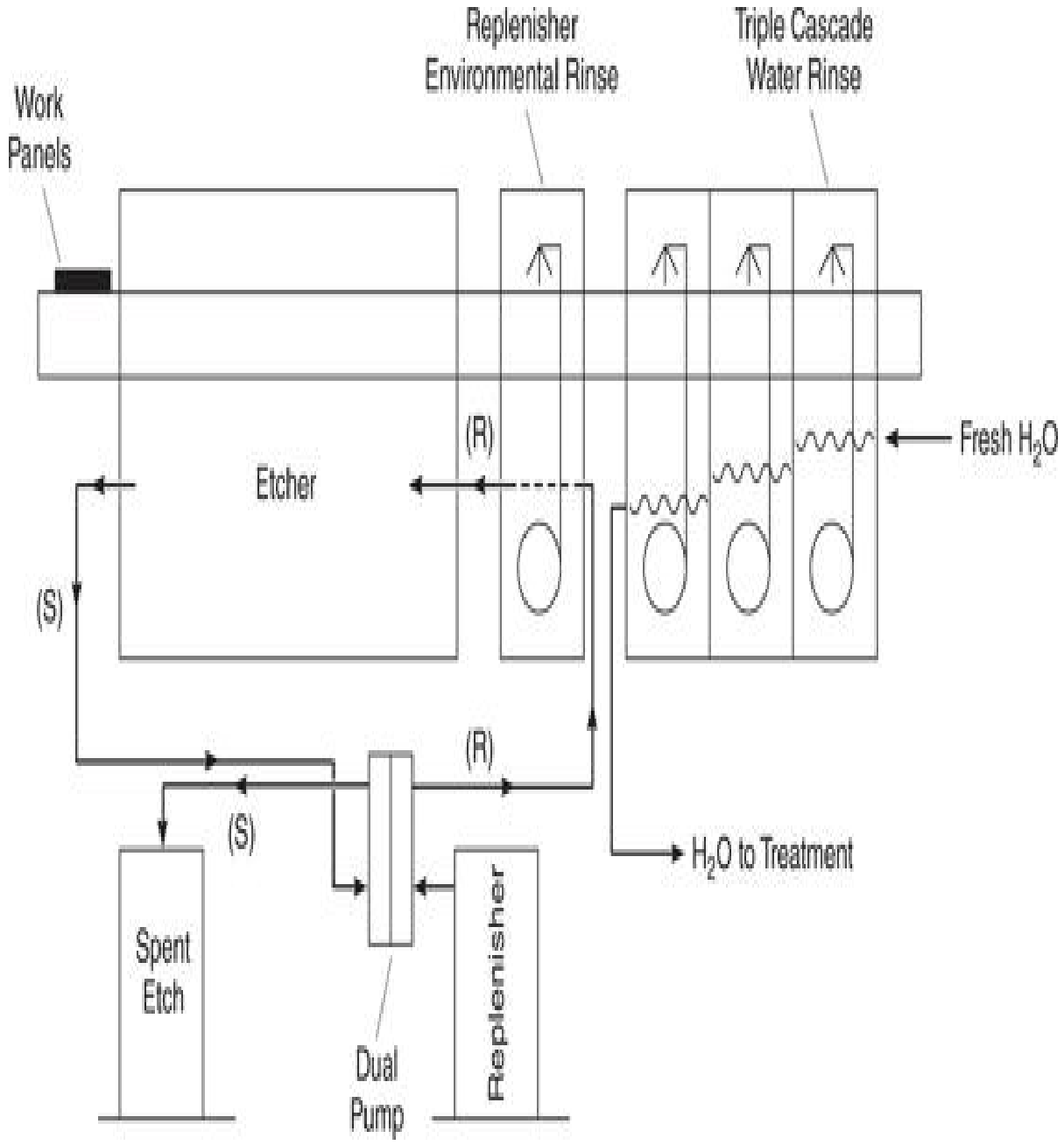

FIGURE 37.1 Automated flow-through alkaline etching system.

A study of the etching rate versus dissolved copper content shows the following effects:

0 to 11 oz/gal	Long etching times
11 to 16 oz/gal	Lower etch times but solution control difficult
18 to 22 oz/gal	Etch rates high and solution stable
22 to 30 oz/gal	Solution unstable and tends toward sludging

All work must be thoroughly rinsed immediately upon leaving the etching chamber. Techniques such as replenisher rinsing and multiple cascade water rinsing assist in thorough rinsing with controlled effluent and limited water use.[8] Do not allow the boards to dry before rinsing. Typical plated resist is tin. On occasion, tin/lead solder resist is plated for fused tin/lead applications. Etched circuitry with plated tin/lead solder resist also requires an acid application of solder brightener for reflow of the coating. Thiourea-containing brighteners have largely been eliminated due to use of sacrificial plating resist (SMOBC) and environmental pressures. Rinsing must be sufficient to remove etchant from under circuit edges and to completely clean the circuit surfaces and plated through-holes.[8] Multiple-stage cascading water rinsing and air knife drying result in clean, stain-free surfaces (see Fig. 37.1). Modern processes often follow the etching rinse with metal-resist stripping and rinsing chambers before exiting the machine conveyor.

37.4.1.4 Closed-Loop Regeneration. True regeneration requires the following:

1. Removal of portions of the spent etching solution from the etcher sump under controlled conditions, according to the amount of copper added to the etch bath.
2. Chemical restoration of spent etchant (i.e., removal of excess by-products and adjustment of solution parameters for reuse).
3. Replenishing of etchant in the etching machine, balancing the actual production use demands. Constant etching conditions are achieved when regeneration is continuous. Regeneration by these methods is expensive and is thus

limited to large printed-circuit facilities. The principal methods of regeneration are crystallization, liquid–liquid extraction, and electrolytic recovery.

- Crystallization reduces the copper level in the etchant by chilling and filtering precipitated salts. This is followed by refortification and adjustment of operating conditions.
- Liquid–liquid extraction[9,10] is gaining acceptance because of its continuous and generally safe nature. The process involves mixing spent etchant with an organic solvent (i.e., hydroxy oximes) capable of extracting copper. The organic layer containing copper is subsequently mixed with aqueous sulfuric acid, which extracts copper to form copper sulfate. The copper-free etchant is restored, and the copper sulfate is available for acid copper electrowinning. Closed-loop regeneration systems reduce chemical costs, sewer contamination, and production downtime, but require floor space, resources, and technical attention. Economics are directly affected by copper market prices.
- Electrolytic recovery of copper directly and through membrane cells from an ammonia-complexed copper sulfate etchant yields possible benefits such as reduced waste shipments and cost savings.[11,12]
- These processes are usually employed by the large-scale vendor/recycling plants that offer a spent removal and replenisher replacement service as part of the product contract. This practice allows for economies of scale and environmental responsibility to be removed from the fabrication plant site.

37.4.1.5 Special Problems Encountered during Etching[13]

1. *Low etch rate with low pH, <8.0*. This is caused by excessive ventilation, heating, downtime, and spraying when the solution is hot, under conditions of adequate replenishment or low ammonia. The pH must be raised with

anhydrous ammonia. Automatic replenishment equipment must be checked.

2. *Low etch rate with high pH, >8.8*. This is caused by high copper content, water in etchant, or underventilation.
3. *Low etch rate with optimum pH*. This is due to error of copper thickness, oxygen starvation in the etcher, or contamination of the etchant.
4. *Solder attack*. This is caused by excess chloride in the etchant, improper tin/lead deposits, or insufficient phosphate content.
5. *Residue on solder plate, holes, and traces*. These may be caused by etchant solution imbalance or by spent finisher.
6. *Under- or overetching*. This may be due to improper pH or equipment adjustments.
7. *Sludging of etch chamber with low pH, <8.0*. See special problem 1. Sludge will be gritty and dark blue. This may be corrected by the addition of anhydrous ammonia.
8. *Sludging of etch chamber with high pH, >8.8*. See special problem 2. Sludge will be light blue and fluffy. This may be due to the copper concentration exceeding the capacity of the chloride concentration. It may be corrected by adding ammonium chloride. It may also be due to water added to the etchant.
9. *Presence of ammonia fumes*. The cause of this is leaks in the etcher. Ventilate for operator safety.
10. *Pollution*. This results when water coming from the etchers contains dissolved copper. If so, it must be chemically treated and separated from ammonia-bearing rinses. Thin-clad copper laminates present a further problem because their faster movement through the etcher increases the transport of etchant into the rinses. Evaluate isolation roller placement and cleanliness, internal etcher overspray, and proper chemical and water rinsing.

37.4.2 Cupric Chloride

Cupric chloride is the second mainstream etchant of choice. (See Table 37.1 for characteristic cupric chloride solutions.) It is more compatible with photopolymer resists and is the etchant of choice for precision etching of small features. Because the cuprous ion buildup renders the etchant impractically slow, this etchant must always be used as a regenerative system with continuous oxidizer management and control. These systems have been the subject of many innovations to achieve continuous regeneration, lower costs, and a constant, predictable etch rate. Steady-state etching with acidic cupric chloride permits high throughput, material recovery, and reduced pollution. Regeneration in this case is somewhat complex but is readily maintained. Dissolved copper capacity is high compared with that of batch operation. Cupric chloride solutions are used mainly for fine-line multilayer inner details, print-and-etch boards, and panel-plate/tent-and-etch boards.[14] In addition to photoresists, screened inks, gold, and tin-nickel have been used. Solder and tin resists are not compatible with cupric chloride etchant.

TABLE 37.1 Characteristic Cupric Chloride Etching Solutions

Component	Solution 1[15]	Solution 2[16]	Solution 3[17]	Solution 4[18]
$CuCl_2\ 2H_2O$	1.42 lb	2.2 *M*	2.2 *M*	0.5–2.5 *M*
HCl (20° Be)	0.6 gal	30 mL/gal	0.5 *N*	0.2–0.6 *M*
NaCl		4 *M*	3 *M*	
NH_4Cl				2.4–0.5 *M*
H_2O	*	*	*	*

*Add water to make up 1 gal.

37.4.2.1 Chemistry. The etching reaction is as follows:

$$Cu + CuCl_2 \rightarrow Cu_2Cl_2 \quad (37.3)$$

Chloride ions, when added in excess as hydrochloric acid, sodium chloride, or ammonium chloride, act to solubilize the relatively insoluble cuprous chloride and thereby maintain stable etch rates. The complex ion formation can be shown as

$$CuCl + 2Cl^- \rightarrow CuCl_3^- \quad (37.4)$$

The formation and diffusion of this chloro-complex form of the Cu(I) ion determine the etching rate for cupric chloride. Thus, the rate is affected by chloride ion concentration as well as the typical diffusion concentration and film thickness variables.

The etchant is regenerated by reoxidizing the cuprous chloride to cupric chloride by several chemical choices as illustrated by the following equations:

$$Air\ 2Cu_2Cl_2 + 4HCl + O_2 \rightarrow 4CuCl_2 + 2H_2O \quad (37.5)$$

This method of regeneration is not used because the oxygen reaction rate in acids is slow and the solubility of oxygen in hot solution is low (4 to 8 ppm). Spray etching induces air oxidation, but is not sufficiently reactive to support practical etching rates. An additional option of using ozone can accelerate the rate of this process, but ozone concentrations in an oxygen stream are difficult to maintain at above 3 percent, thus limiting utility.

Direct chlorination

$$Cu_2Cl_2 + Cl_2 \rightarrow 2CuCl_2 \quad (37.6)$$

As the traditional regeneration choice, the chlorine reaction is rapid, positive, and easily controlled. Liquefied chlorine gas has been generally available, and standardized commercial addition systems have been available. Recently, pressure on chlorine distribution and use due to safety and environmental regulations have made availability and implementation more

expensive and difficult. It is significant that the reaction simplicity indicates that all etched copper is converted directly to cupric chloride [combination of Eqs. (37.3) and (37.6)]. Thus, there is no effect on water or acid balances from the etching reaction itself.

Hydrogen peroxide

$$Cu_2Cl_2 + 2H_2O_2 + 2HCl \rightarrow 2CuCl_2 + 2H_2O \qquad (37.7)$$

This process is more complicated because both hydrogen peroxide and hydrochloric acid add water in the reaction process. Since hydrogen peroxide is unsafe to store and handle in concentrations above 35 percent, there is considerable water added with both the oxidizer and the hydrochloric acid. The result limits the copper-holding capacity of the etchant. The addition is reasonably and simply controlled as a direct ratio of HCl, and peroxide is added to the bath to maintain the copper oxidation. This formulation has been favored in Europe and to some extent in Asia.

Sodium chlorate

$$3Cu_2Cl_2 + NaClO_3 + 6HCl \rightarrow 6CuCl_2 + NaCl + 3H_2O \qquad (37.8)$$

Sodium chlorate has become one of the most widely used formulations. The oxidizer solutions can be mixed from powder and are also commercially supplied as 45 percent solutions. The water balance must also be carefully controlled with this oxidizing plan, and the amount of sodium chloride in the working bath can be boosted by addition with the oxidizer. This can be a rate enhancer by supplying chloride ions needed by Eq. (37.6), and since the chloride ion is separately added from the hydrochloric acid, the free acid can be maintained at very low levels (<0.1 normal).

Electrolytic

$$\text{(Cathode)} \qquad Cu^+ + e^- \rightarrow Cu \qquad (37.9)$$

$$\text{(Anode)} \qquad Cu^{+} \rightarrow Cu^{2+} + e^{-} \qquad (37.10)$$

Electrolytic systems of direct and membrane cell design have been employed. However, this technology is not a major factor in current manufacturing practice.

37.4.2.2 Properties and Control. Early cupric chloride formations had slow etch rates and low copper capacity and were limited to batch operation.[15–21] Regenerated continuous operation using modified formulations has brought useful improvements. Etch rates as high as 55 s for 1 oz copper are obtained from cupric chloride–sodium chloride–HCl systems operated at 130°F with conventional spray-etching equipment. Copper capacities are maintained at 20 oz/ gal and above. However, more recently, higher copper contents and adjusted chemistries at 125°F typically etch at 75 to 90 s for 1 oz copper.

37.4.2.3 Continuous Etching and Regeneration. Systems in use include chlorination, sodium chlorate, hydrogen peroxide, and electrolysis.

37.4.2.3.1 Chlorination. Direct chlorination has been the preferred technique for regeneration of cupric etchant because of its historically low cost, high rate, efficiency in recovery of copper, and pollution control. The cupric chloride–sodium chloride system (Table 37.1, no. 3) is suitable. Figure 37.2 shows a generalized process.[17] Chlorine, hydrochloric acid, and sodium chloride solutions are automatically fed into the system as required. Sensing devices include oxidation-reduction instruments (Cu oxidation state), density (Cu concentration), level sensors, and thermostats. Chlorination is reliable and controllable. Other factors are safety and solution control. Optical colorimetric sensors can be used to detect Cu(I) levels. However, these cells are subject to fogging by organic contamination and crystalline buildup with the hazardous defect of continuing to add chemicals past the proper control points and liberating chlorine into the work area.

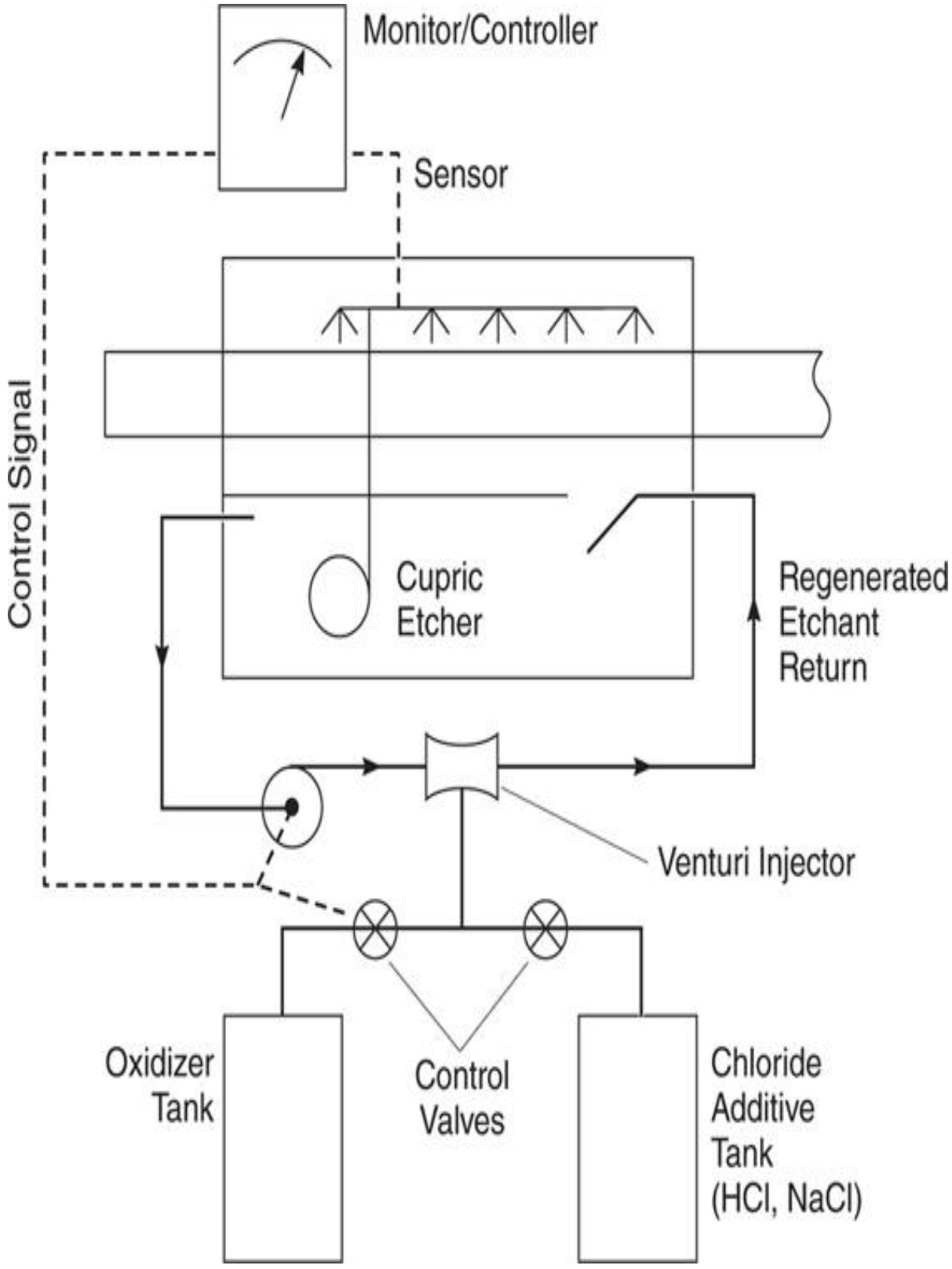

FIGURE 37.2 Cupric chloride chlorination regeneration system.

1. *Safety:* Use of chlorine gas requires adequate ventilation, tank and cylinder storage, leak-detection equipment, emergency protocols, personal protective equipment, operator training, and fire department approval and inspection of installations.
2. *Solution control:* An increase in pH will cause the copper colorimeter to give erroneous readings caused by turbidity in the solution. Organic deposits can also foul controls. Excess NaCl at 18 to 20 oz/gal copper causes coprecipitation of salts when the solution is cooled. Solution filtration and etch tank cleanliness must be maintained. Replacement of electrodes, instruments, and metering devices should be scheduled regularly.

37.4.2.3.2 Chlorate Regeneration. This method, currently widely supported, uses sodium chlorate, sodium chloride, and hydrochloric acid and is an alternate method similar to chlorination. A control sequence similar to the one shown in Fig. 37.2 may be used. Sodium chlorate is available in commercial solutions of several strengths with some degree of formulated agents (usually sodium chloride) added to the mixture. These solutions are added with hydrochloric acid either as a coordinated addition or in a special control logic sequence that allows very low free acid. This control system uses a multiple sensor color or turbidimetric optical system. The addition of one component (e.g., oxidizer) to a flowing sample cell occurs when the primary cell senses are triggered. A second cell allows this addition so long as there is a change from the first cell input. When there is no longer a change response and the first cell is still in “triggered” condition, the second component (e.g., HCl) is added. The logic continues to flip-flop until the first cell is satisfied. The etch sump conditions seem to have a partially delayed response to the chemical addition reaction such that oxidizing seems to occur over a longer period. Therefore, proper addition and mixing in the sump must be considered for stable control operation.

1. *Safety:* Sodium chlorate is a potent oxidizing agent that can support combustion. It is necessary to ensure that solution spills are completely cleaned up and that the rags or other materials are not allowed to dry out. Excess addition of reagents above amounts to support the actual copper etched may form chlorine gas that will be liberated into the etch machine and environment. Proper instrumentation and training for this eventuality must be implemented.
2. *Solution control:* If there is insufficient free acid content in the etch sump to react with the oxidizer and copper [Eq. (37.8)], a dangerous imbalance can occur. First, the instruments and controls may not respond properly, and the etch reaction may slow down. Second, any subsequent addition of acid or mixing with acid-containing wastes can liberate chlorine gas in an uncontrolled and dangerous manner. Proper chemical balance is another issue. Water is added in all of the chemical streams and is produced in the chemical reaction. Therefore, any excess chemical addition can dilute the chemistry and change the copper-holding ability of the etchant.

37.4.2.3.3 Hydrogen Peroxide Regeneration. Hydrogen peroxide uses a two-part chemistry much like sodium chlorate. ORP instrumentation is identical in the control of adding proportional amounts of oxidizer and hydrochloric acid. Peroxide tends to decompose on sitting so that the spills are not as dangerous. Older application of colorimetric cells for the control of dosing has largely been eliminated.

1. *Safety:* Hydrogen peroxide solutions can become unstable and disassociate into oxygen and water with the liberation of heat. This can occur with explosive force in a confined vessel such as a drum stored in sunlight or heat. It can also occur in plumbing with closed valving. The decomposition is catalyzed by many metals, including Cu, Ni, and Fe. If traces of metal or metal salts are allowed to contaminate

piping runs, the piping may also rupture explosively. Facilities should be constructed with pressure relief capabilities.

37.4.2.3.4 Electrolytic Regeneration. The electrochemical reversal of the etching of copper shown in Eq. (37.9) and (37.10) is claimed to be effective and economical. Descriptions of this system are given in the literature.[15] On a large scale, electrolytic regeneration requires a high investment in equipment and materials, as well as high power consumption. The chemical formulation is relatively high in acid content and low in copper, a condition not optimized for etching effectiveness or plating efficiency.

The etchant is a solution of cupric chloride and hydrochloric acid (Table 37.1, no. 1). Etchant flows continuously between spray-etching machines and a plating tank. In the plating machine, two processes take place simultaneously: copper is plated at the cathode, and regeneration of the spent etchant occurs at the anodes. Copper recovery may not return copper value and may be expensive, inconvenient, and cause difficulty with recycling.

37.4.2.4 Problems with Cupric Chloride Systems

1. *Slow etch rate:* Depending on chemical formulation, cupric chloride is inherently slower than ammonia and must be properly evaluated before production expectations are established. Check to ensure no resist residues or chromate coatings remain on the panel surface before etching. A slower than usual rate is frequently due to low temperatures, insufficient sump mixing, or poor solution chemical control. If temperature and agitation are under control, slow etching with a dark green solution may result from a low cupric ion content, indicating insufficient oxidizer. Acid must also be added to clarify cloudy solutions. (Before acid addition, make sure excess oxidizer is not present.) In regenerative systems, the source of oxidation

may be depleted. It is advisable to analyze specific gravity, free acid, and total chloride on a regular schedule and maintain control charts to ensure that bath controllers are consistent and operating properly.

2. *Sludging:* This occurs if acid is low or if water dilution occurs.
3. *Etcher goop:* This is a common floating accumulation of photoresist compounds leached into and precipitated from etch baths. Accumulations appear to increase with higher acid formulations. Formation can be limited by proper exposure of photoresists and continuous recirculation of the etch bath through carbon filtration. Periodic, complete drain-down of the etching machinery and thorough mechanical and chemical equipment cleaning with a sulfamic acid–type commercial cleaner can minimize problems.
4. *Yellow or white residues on copper surface:* Yellow residue is usually cuprous hydroxide. It is water insoluble and is left when boards are etched and alkali-cleaned. A white precipitate will probably be cuprous chloride, which can remain after etching in solutions that are low in chloride ion and acid. To eliminate both conditions, the solution in which the board is rinsed just before final water-spray rinsing should be 5 percent by volume hydrochloric acid.
5. *Waste disposal:* Spent or by-product etchant is usually sent off-site for copper reclamation. There is usually a fee for this service depending on copper content and distance to the reclamation facility. The solutions must be free of unreacted oxidizer (see previous chlorate system discussion). Etchant can contain traces of zinc, chromium, and arsenic from the foil treatments.

37.4.3 Sulfuric Acid–Hydrogen Peroxide

Sulfuric-peroxide systems are used extensively for copper surface preparation by microetching the surface to provide texture and active surfaces. These formulations have been used in the past for primary circuitization etching but are no longer favored because of slow etch rate and needs for accompanying control of exotherm and copper crystallization. However, the increasing need for fine-line etching has renewed use possibilities for this and other etchants (see Sec. 37.7.4). In essence, these call for etching foils thinner than ½ oz and the control precision offered by slower etchants. They are compatible with metal resists and many organics.

37.4.3.1 Chemistry. Typical constituents of both immersion and spray etchants and their functions are as follows:

1. Hydrogen peroxide is an oxidizing agent that reacts with and dissolves metallic copper.
2. Sulfuric acid makes copper soluble and holds copper sulfate in solution.
3. Copper sulfate helps to stabilize etch and recovery rates.
4. Molybdenum ion is an oxidizing agent and rate exaltant.[22]
5. Aryl sulfonic acids are peroxide stabilizers.[23]
6. Thiosulfates are rate exaltants and chloride ion controllers that permit lower peroxide content.[24]
7. Phosphoric acid retains clean solder traces and plated through-holes.[25,26]

The etching reaction is as follows:

$$Cu + H_2O_2 + H_2SO_4 \Rightarrow CuSO_4 + 2H_2O \qquad (37.11)$$

37.4.3.2 Properties and Control. The earlier technical problems of slow etch rates, peroxide decomposition, and foaming in spray systems have been solved, but critical concerns still remain. Among these are process overheating, etchant composition balance with by-product recovery, etchant

contamination, and the dangers of handling concentrated peroxide solutions. The specific problem of decomposition of peroxide during idle hours has caused disastrous equipment meltdowns, and thus requires thermal management while equipment is otherwise not in operation.

37.4.3.3 Closed-Loop Systems. Production facilities require continuous recirculation of the etchant through the etching tank or machine and the copper sulfate recovery operation. Etchant replenishment is controlled by chemical analysis and by additions of concentrates.

Copper sulfate recovery is based on lowering the solubility of $CuSO_4$ $5H_2O$ by decreasing the etchant temperature to 50 to 70°F. Crystallizer equipment and conveyorized discharge has been available for this process.

37.4.3.4 Problems Encountered with Peroxide Systems

1. *Reduced etch rates:* This problem can be caused by operating conditions, solution imbalance, or chloride contamination.
2. *Under- and overetching:* A review of etching conditions, solution control, and the resist stripping process may show deviations from normal. In the case of immersion etching, the solution and panel agitation may need to be increased. When spray-etching, a check of nozzles and line clogging is indicated.
3. *Temperature changes:* Recirculating water rates and thermostats need to be examined regularly. Overheating may be due to high copper content, contamination, or rapid peroxide decomposition.
4. *Copper sulfate recovery stoppage:* Examine solution balance, heat exchanger, and other recovery equipment. Exit conveyor jamming difficulties from thermal excursions and varying crystal size and liquid content cause major shop floor problems.

37.4.4 Persulfates

Ammonium, sodium, and potassium persulfates modified by certain catalysts have been adopted for the etching of copper in PC manufacturing. Continuous regenerative systems and a batch system using ammonium persulfate are no longer used. Wide use is made of persulfates as a microetch for innerlayer oxide coating and copper electroless and plating processes. Persulfate solutions allow all common types of resists on boards including solder, tin, tin/nickel, screened inks, and photosensitive films. Formulations of ammonium persulfate catalyzed with mercuric chloride are no longer used, primarily because of environmental issues, costs, and improved alternatives. In general, persulfate etchants are unstable and will exhibit decomposition, lower etch rates vs. copper content, and lower useful copper capacity.

37.4.4.1 Chemistry. Ammonium, potassium, and persulfates are stable salts of persulfuric acid ($H_2S_2O_8$). When these salts are dissolved in water, the persulfate ion ($S_2O_8^{2-}$) is formed. It is the most powerful oxidant of the commonly used peroxy compounds. During copper etching, persulfate oxidizes metallic copper to cupric ion as shown:

$$Cu + Na_2S_2O_8 \rightarrow CuSO_4 + Na_2SO_4 \qquad (37.12)$$

Persulfate solutions hydrolyze to form peroxy monosulfate ion (HSO_4^{1-}) and, subsequently, hydrogen peroxide and oxygen. This hydrolysis is acid catalyzed and accounts for the instability of acidic persulfate etching solutions.

Ammonium persulfate solution, normally made up at 20 percent, is acidic. Hydrolysis reactions and etchant use cause a reduction of the pH from 4 to 2. The persulfate concentration is lowered, and hydrated cupric ammonium sulfate [$CuSO_4$ $(NH_4)_2SO_4$ $6H_2O$] is formed. This precipitate may interfere with etching.

Solid persulfate compounds are stable and do not deteriorate if stored dry in closed containers. Solution makeup composition includes various catalysts, including organic matter and transition metals (Fe, Cr, Cu, Pb, Ag, etc.). Materials for storage must be chosen carefully. Persulfates should not be mixed with reducing agents or oxidizable organics.

The useful capacity of the etchant is about 7 oz/gal copper at 100 to 130°F. Above 5 oz/gal of copper, it is necessary to keep the solutions at 130°F to prevent salt crystallization. The etch rate of a solution containing 7 oz/gal of dissolved copper is 0.00027 in/min at 118°F.

37.4.4.2 Batch Operation. Sodium persulfate is preferred because it has minimal disposal problems and somewhat higher copper capacity and etch rates. A composition of 3 lb/gal sodium persulfate with 15 ppm of $HgCl_2$, 1 gal of proprietary additive, and 57 ml/gal of H_3PO_4 has been successfully used for batch-type spray etching.[27] Etch rates vary throughout bath life and range from 0.0018 to 0.0006 in/min for copper content of 0 to 7 oz/gal. Prepared solutions must be aged for 16 to 72 h before etching when proprietary additives are used.

37.4.4.3 Problems with Persulfates

1. *Low etch rates:* Since the solution may decompose, it will be necessary to replace the bath. If solution is new, add more catalyst and check for iron contamination.
2. *Salt crystallization:* Salts crystallize on the board and cause streaks, damage the solder plate, and plug the spray nozzles or filters. When copper content is high, blue salts may precipitate.
3. *White films on solder surface:* This may occur normally or when the lead content in the solder plate is too high.
4. *Black film on solder:* This condition can result when the solder alloy is high in tin. If solder reflow or component soldering is to follow, activate by tin immersion or with

solder brighteners. Adjust phosphoric acid content in etchant and solder-plating conditions.

5. *Spontaneous decomposition of etch solution:* This breakdown is due to contaminated, overheated, or idle solutions. Ammonium persulfate etchants are unstable, especially at higher temperatures. At about 150°F, the solution decomposes quickly. Use it soon after mixing.
6. *Disposal:* The exhausted etchant consists mainly of ammonium or sodium and copper sulfate with a pH of about 2. Two methods for disposal are
   a. Electrolytic disposition of the copper on the surface of passivated 300 series stainless steel is one disposal method. The spent etchant is acidified with sulfuric acid prior to electrolysis. Once the copper has been removed, the remaining solution can be diluted, neutralized, checked, and discarded. The copper can be removed from the cathode. Spent sodium persulfate can be treated with caustic soda.
   b. Addition of aluminum or iron machine turnings to a slightly acidified solution is another practical but possibly more difficult means of removing the dissolved copper. The reaction, especially in the presence of chloride ions, will be violent, and considerable heat will be given off if the solutions are not diluted.

37.4.5 Ferric Chloride

Ferric chloride solutions are used as etchants for copper, copper alloys, Ni/Fe alloys, and steel in PC applications, electronics, photoengraving arts, and metal finishing. Current use of ferric chloride etchant in printed wiring fabrication is extremely limited in the United States because of costly disposal of the copper-containing etchant, and the much better commercial support for ammoniacal and cupric chloride etchants. There is still considerable use for alloy etching and photochemical machining applications.

Ferric chloride can be used with screen ink, photoresist, and gold patterns, but it cannot be used with tin or tin/lead resists. However, ferric chloride is an attractive spray etchant because of its ease of use, holding capacity for copper, and ability to be used on an infrequent batch application basis.

The composition of the etchant is mainly ferric chloride in water, with concentrations ranging from 28 to 42 percent by weight. Free acid is present because of the hydrolysis reaction and the need to maintain an acid environment. The natural acidity is usually supplemented by additional amounts of HCl (up to 5 percent) to prevent formation of insoluble precipitates of ferric hydroxide. Commercial formulations for copper alloy etching are usually 36 Be, or approximately 4.0 lb/gal $FeCl_3$, and may contain antifoam and wetting agents. Customary acid operating HCl content is 1.5 to 2.0 percent.

The effects of ferric chloride concentration, dissolved copper content, temperature, and agitation on the rate and quality of etching have been reported in the literature.[28,29]

37.4.6 Chromic-Sulfuric Acids

These etchants for solder- and tin-plated boards were preferred for many years. More recently, their use has been completely eliminated due to Cr(VI) listing as a critical environmental hazard. Other problems with chromic-sulfuric etchants are difficulty in regeneration, inconsistent etch rate, the low limit of dissolved copper (4 to 6 oz/gal), and dangerous degradation of PVC and polypropylene equipment. Chromic acid etchant is suitable for use with solder, tin/nickel, gold, screened vinyl lacquer, and dry or liquid film photoresists. Chromic-sulfuric mixtures etch copper slowly, and additives are needed to increase the etch rate. For example, sodium sulfate and iodine have been used for rate increase. Alkaline etchants have become so well controlled that there is no justification for the risks and costs of chromic acid formulations.

The following listing demonstrates some of the operational difficulties with chromic-sulfuric etchants.

1. *Solder attack:* The protective value of solder depends on the formation of insoluble compounds on the surface. Solder is attacked if the sulfate content of the bath becomes very low or contains chloride or nitrates. The solder plate composition can also cause etchant attack. When the lead content becomes low, the sulfate film protection is lowered, and protection is lost.
2. *Slow or no etching of copper:* This can be caused by low chromic content, low temperature, insufficient acid, or high copper content. The solution is maintained as close as possible to 30 Baumé (pH about 0.1, temperature 80 to 90°F) and should be discarded when copper metal content exceeds 5.5 oz/gal.
3. *Staining of board materials:* The surfaces of dielectric substrates such as paper-based phenolics are attacked by chromic acid etchants. Removal is difficult, and the boards are generally rejected.
4. *Disposal:* Spent chromic acid etchants present a serious disposal problem. Disposal must comply with pollution standards and approved practice.
5. *Safety hazards:* Chromic acid is an extremely strong oxidizing agent. It will attack clothing, rubber, plastics, and many metals. Safety measures require adequate ventilation to keep fumes out of room air, synthetic rubber gloves, aprons, face and eye shields, and storage away from combustible materials. Dermatitis and nasal membrane damage are possible dangers.[7]

37.4.7 Nitric Acid

Etchant systems based on nitric acid have not found extensive application in PC manufacture. Copper etching is very exothermic, which may lead to violent runaway reactions.

Problems with this system include solution control, attack on resists and substrates, and toxic gas fuming. However, nitric acid has certain advantages. These include rapid etching, high dissolved copper capacity, high solubility of nonsludging products, availability, and low cost.

37.4.7.1 Chemistry. Reaction in strong acids is shown by the following equation:

$$3Cu + 2NO_3^- + 4H^+ \rightarrow 3Cu^{2+} + 2NO_2 + 2H_2O \qquad (37.13)$$

Recent work shows that process improvements are possible.[30,31] Controlled etching has been attained in solutions containing 30 percent copper nitrate, water-soluble polymers, and surfactants. Dry-film resists work well in this etchant. An important finding was that straight wall trace edges were achieved using nitric acid. This could result in higher yields and density of fine-line boards. The major difficulty in obtaining the sidewall results is the requirement for specific crystollagraphic grain structure to the copper foil that has been difficult to reproduce in production quantities.

37.5 OTHER MATERIALS FOR BOARD CONSTRUCTION

Printed board laminates are usually composed of copper foils bonded to organic dielectric materials, ceramics, or other metals.

1. *Organic dielectrics:* These are thermosetting or thermoplastic resins usually combined with a selected reinforcing filler. Thermoset-reinforced materials used for rigid and flexible boards provide overall stability, chemical resistance, and good dielectric properties. Thermoplastic materials are also used for flexible circuit applications. A

factor in material selection is the effect of process solutions, etchants, and solvents on the material. In addition, the adhesives used in laminating metal to substrate can be softened, loosened, and attacked by some solutions. Flat-surface planarity is an aid to precision etching. This can be improved by selection of laminate with fine glass woven structures that do not express a waviness to the free copper foil surface.

2. *Thin-clad copper:* Etched printed boards with epoxy laminate of ¼ oz (9 µm) copper or less show minimal lateral etching, thus enabling higher fidelity to pattern-plated traces. The problem with very thin copper foils is pinhole density and fragility in the laminate manufacturing process. One method of avoiding these problems is to start with a more conventional ½-oz (18-µm) foil and reduce its thickness by etching to a thinner state (3 to 9 µm).[32] This technique depends on a uniform starting foil and a very well-controlled etching process. Although the particulars of the published process were not disclosed, cupric chloride and sodium persulfate formulations have been used for this process.
3. *Reverse foil laminate:* This construction is receiving attention for improving precision and control of etched lines. In order to achieve this foil structure, the *tooth* or crystalline roughness must also be controlled in the foil. The tooth side is usually placed on the dielectric interface of the laminate to increase peel strength and present a flat surface for processing. However, one variation is to place the *drum* or flat side of the laminate toward the dielectric and leave the tooth side upward. This forms a flat interface so that the etching stops at this surface, instead of the conventional extra etching to remove the teeth that are buried in dielectric.
4. *Semiadditive copper:* A copper thickness of 0.000050 to 0.000200 in with subsequent copper and resist metal plating shows no overhang or sliver formation. These layers must be of sufficient thickness and uniformity to withstand

the cleaning and preparation steps for plating the required conductors.

37.6 METALS OTHER THAN COPPER

37.6.1 Aluminum

Aluminum-clad flexible circuits find use in microwave stripline[33] and radiation-resistance applications. Aluminum and its alloys have good electrical conductivity, are lightweight, and can be plated, soldered, brazed, chem-milled, and anodized with good results. Laminate dielectrics include PPO,[33] polyimide,[37] epoxy-glass, and polyester.

Precleaning for resist application includes nonetch alkaline soak, water rinsing for 5 to 10 s in chromic-sulfuric acid, rinsing, and drying. Preferred etchants include ferric chloride (12 to 18° Baumé), sodium hydroxide (5 to 10 percent), inhibited hydrochloric acid, phosphoric acid mixtures, solutions of HCl and HF, and ferric chloride–hydrochloric acid mixture.

Screen-printed vinyl resists and dry-film photoresist are the most durable for deep etching or chem-milling. A dip in a 10 percent nitric or chromic acid solution will remove residues from the surface or edges of conductor lines that may be left on some alloys. Dilute chromic acid has also been used for this purpose. Spray rinse thoroughly with deionized water after etching.

37.6.2 Nickel and Nickel-Based Alloys

Nickel is increasingly used as a metal cladding, electroplated deposit, or electroformed structure for printed wiring because of its welding properties. Nichrome- and nickel-based magnetic alloys are other examples of materials requiring special etching techniques.

The methods previously described are adaptable to image transfer and etching of nickel-based materials. Etching uses ferric chloride (42° Baumé) at about 100°F. Other etchants include solutions made from one part nitric acid, one part hydrochloric acid, and three parts water, or one part nitric acid, four parts hydrochloric acid, and one part water.

37.6.3 Stainless Steel

Alloys of stainless steel are used for resistive elements or for materials with high tensile strength. Etching of the common 300 to 400 series can be done with the following solutions:

1. Ferric chloride (38 to 42° Baumé) with 3 percent HCl (optional).
2. One part HCl (37 percent) by volume, one part nitric acid (70 percent) by volume, one to three parts water by volume. Etch rate is about 0.003 in/min at 175°F, useful for high 300 to 400 series alloys.
3. Ferric chloride + nitric acid solutions.
4. One hundred parts HCl (37 percent) by weight, 6.5 parts nitric acid by weight, 100 parts water by weight.

37.6.4 Silver

Silver, the least expensive precious metal, has excellent properties, including superior electrical and thermal conductivity, ductility, visible-light reflectivity, high melting point, and adequate chemical resistance. As such, it is widely used throughout the electronics industry. Flexible circuit structures with silver are used in electronic cameras and LED products.

Standard image-transfer methods are suitable. Preetch cleaning should include a dip in dilute nitric acid. Mixtures of nitric and sulfuric acids are effective etchants. With silver on

brass or copper substrates, a mixture of 1 part nitric acid (70 percent) and 19 parts sulfuric acid (96 percent) will dissolve the silver without attacking the substrate. The solutions should be changed frequently to prevent water absorption and the formation of immersion silver on the copper.

Etching can be done with a solution containing 40 g chromic acid, 20 mL sulfuric acid (96 percent), and 2000 mL water.[35] This is followed by a rinse in 25 percent ammonium hydroxide. Thin films of silver are etched in 55 percent (by weight) ferric nitrate in water or ethylene glycol. Solutions of alkaline cyanide and hydrogen peroxide will also dissolve silver. Use extreme caution. Electrolytic etching is also possible with 15 percent nitric acid at 2 V and stainless-steel cathode.

37.7 BASICS OF ETCHED LINE FORMATION

The basic process of chemical etching to form features has been studied and modeled extensively. However, the best scientific knowledge can only proceed to an understanding of factors influencing the process. The practical execution of the process to manufacture useful circuits contains elements of experience in the best practice of several processes and choices in the selection of materials and process variations to achieve technically sound, cost-effective, and manufacturable results. In order to make fine-line circuit products, it is necessary to understand the process fundamentals so that the limitations may be understood and then overcome. The intent of this section is to briefly review the underlying science and discuss factors and practices for precision etching.

37.7.1 The Image

37.7.1.1 Phototools. It seems obvious that artwork is the first defining step of the image. If the phototool lacks definition, integrity, or dimensional stability, there is no possibility of improving the image in subsequent processing. The edge definition and contrast are particularly important. Images of multiple pulses or *spots* must be overlapped so that there is minimum waviness of edges. As the feature to be resolved becomes smaller, the image must have better and cleaner integrity. It is desired that the artwork be at least an order of magnitude (factor of 10) better than the final tolerance required for the final product. Therefore, if the line tolerance is 0.0001 in, then the artwork should be 0.00001 in.

37.7.1.2 Image Integrity. The effectiveness of the image translated from the artwork/ exposure process can be best achieved by optimization through all of the processing. Surface preparation, resist application, exposure, handling, development, and cleanliness must be maintained sufficiently to produce images with proper integrity. Image integrity may be gauged periodically with a resource such as the Conductor Analysis Technologies etch evaluation protocol. Defects such as shorts and opens have been determined to be related to resist integrity, and persistent linewidth repeating patterns may be image related. General concepts indicate that the thinner the resist, the shorter the light path; and the less optical interface layers between the light source and the copper surface, the better fidelity of the image to the phototool. However, constant improvement in film, exposure, and phototool products makes fine-image options dependent on proper optimization and constancy of technique and cleanliness as well as choice of technology.

37.7.2 Basics of Processing

37.7.2.1 Diffusion—The Controlling Mechanism. In Sec. 37.4, the chemical reactions of the etching process are discussed. In order to understand the formation of the actual

shapes of the foil cross section, the influences of diffusion and fluid flow must be understood.[32] As a result of the etching reaction at the reaction point on the copper surface, a complex ion concentration is built up and active etching chemicals are depleted. In order to complete the reaction, this complex ion must move through a static *boundary layer* into a place where there is fresh etchant supplied to complete the reaction and carry away the etched product (see Fig. 37.3). This boundary-layer shape is dependent on the specific shape of the resist and etching wall, the fluid flow over the surface, and the critical fluid flow in the channels formed by the resist and the etched side wall.

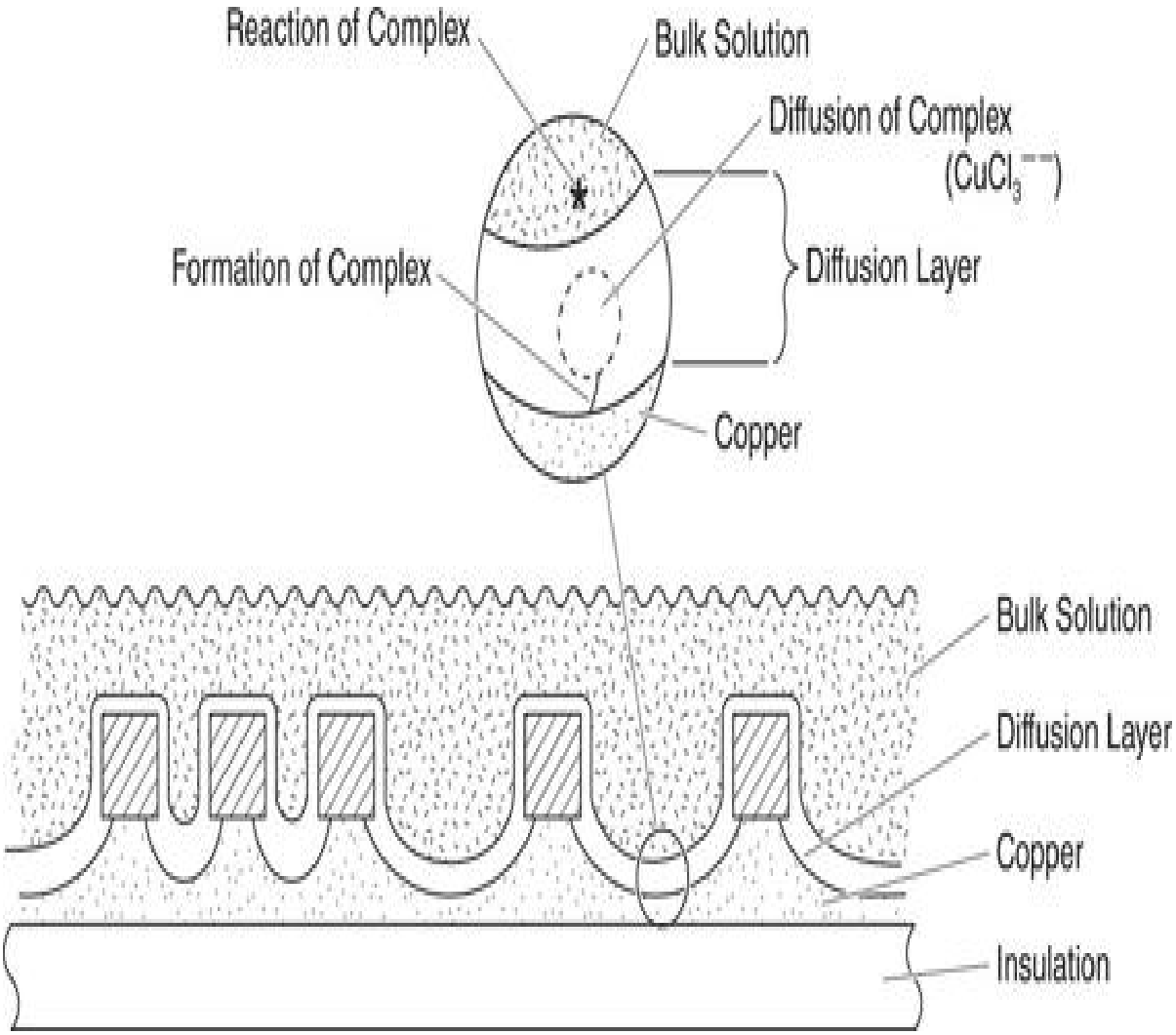

FIGURE 37.3 Etching dynamics for diffusion.

37.7.2.2 Fluid Flow Contribution. Examination of Fig. 37.3 shows that the contour of the boundary layer and its thickness vary with the shape and narrowness of the channel. If the surface is flat with no resist image, the boundary layer is thin and only dependent on the fluid properties and velocity across the surface. On the other hand, with resist images forming channels with depth, and the etched copper forming further channels, it is easy to see how the flow of fluid in the channel can be much different than the surface flow. In order to make matters even more confusing, the circuit traces and resist images form actual channels in the surface.

Much like a river bottom, the fluid flow in these individual channels is influenced by but different from the overall surface flow. In general, the narrower and deeper the channel, the slower the flow; and, critically, the diffusion boundary layer is more significant and etchant slows. In general terms, this is the reason that the middle section of a group of parallel, closely spaced lines etches slower than the outside lines. Similarly, this is the reason why a sharp 90° angle has a slower-etching section in the inside edge of the bend.

The concept of spray etching adds another dimension to the fluid dynamics. The surface of the panel is never really free of a liquid film. The top side of a panel has the etch liquid held up between delivery by the sprays and removal by flow off the edges. This flow is influenced by the number, flow, and pattern of the nozzles, the interaction of the flow between the sprays, the motion of the panels, and the effects of rollers and other contacting and shadowing objects. Even the bottom side retains fluid by surface tension and is influenced by the amount of liquid moving under the direction of the nozzles. The end result is complicated flow patterns that are the result of testing and optimization by the machine manufacturers.

37.7.3 Trace Shape Development

37.7.3.1 Etched Trace Shape Description. During etching, the gap between resist areas is removed evenly at first, and then progressively cup-shaped until the center area is broken through. After this, the area of exposed laminate opens progressively and the etching works on the side walls, etching in and under the resist as the side wall is relieved to expose more insulation and isolate the desired feature. (It has been noted that very little undercutting is apparent until the center is opened.) Figure 37.4 illustrates the attack with standard definitions for R (resist width), B (base of trace), T (top of trace), and t (foil thickness). There are two descriptive measures of the etching process—undercutting and etch factor—which are defined in Eqs. (37.14) and (37.15). These definitions are not universal, so it is necessary to clarify the definitions to correctly interpret discussions using these factors. Undercutting defines the average overhang of resist after top width reduction, and etch factor defines the average side wall inward taper of the etched feature per unit thickness. Occasionally, the etch factor is inverted or different measured values are used.

$$\text{Undercut:} \qquad U = (R - T)/2 \tag{37.14}$$

$$\text{Etch factor:} \qquad F = 2t/(B - T) \tag{37.15}$$

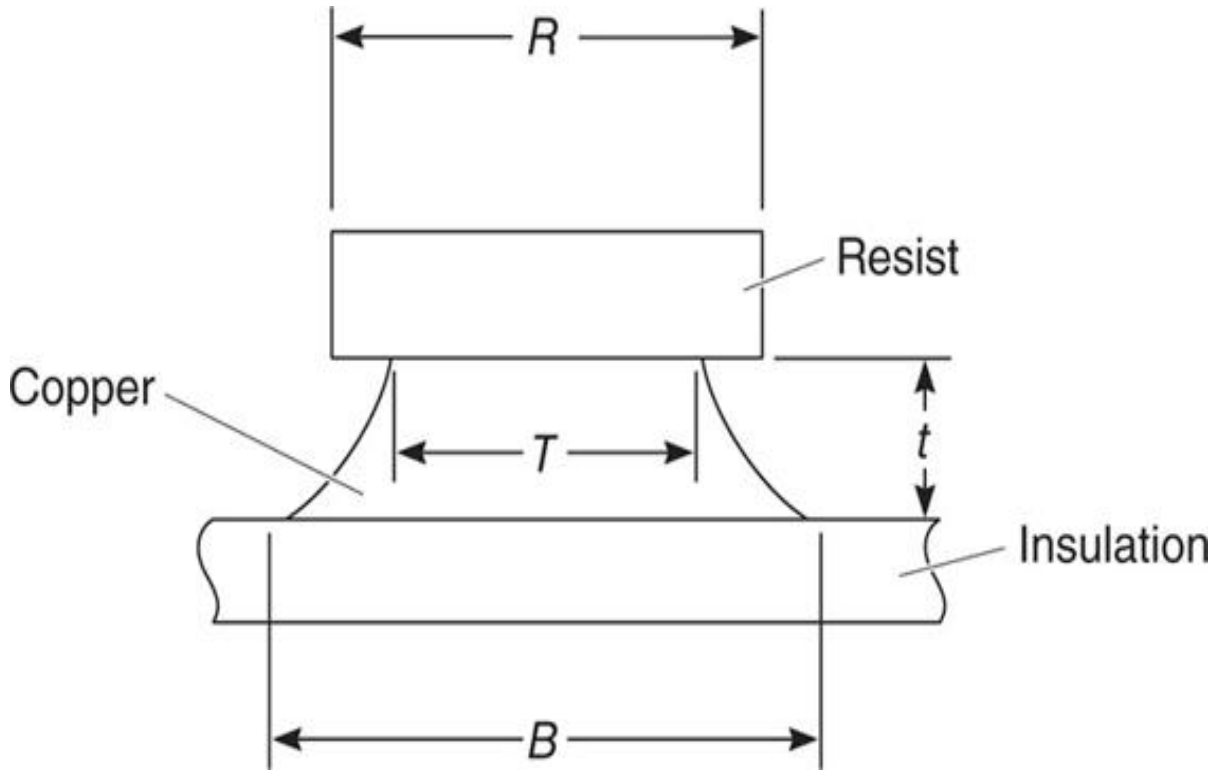

FIGURE 37.4 Trace cross-section measurement.

It is significant that these two units of measure are useful in describing the development of the shape of an etched part. It is desirable that *U* be minimized and *F* maximized for best feature definition.

37.7.3.2 Undercut and Etch Factor Development. The development of trace shapes has been studied by observing etched traces at progressive times.[36, 37] This allows one more parameter to be developed, the extent of etch, which is the ratio of *R/B*. This factor equals 1.0 when the bottom of the trace equals the resist width, one measure of ideal etching. Note that if $R < B$, this implies that the trace is underetched, and $R > B$ indicates overetching. The traces were etched in cupric chloride using 3.0-mil line and space patterns of 1.0-mil resist on 1-oz (1.4-mil) copper foil. The progression of etch values is found in Table 37.2 and Fig. 37.5.

TABLE 37.2 Etch Progression

Etch Time, s	Undercut, *U* mil	Etch Factor, *F*	Extent of Etch, *R/B*
90	0.05	0.90	0.5
110	0.30	1.75	0.75
125	0.45	2.33	1.1
140	0.525	2.67	1.0
165	0.75	3.11	1.25

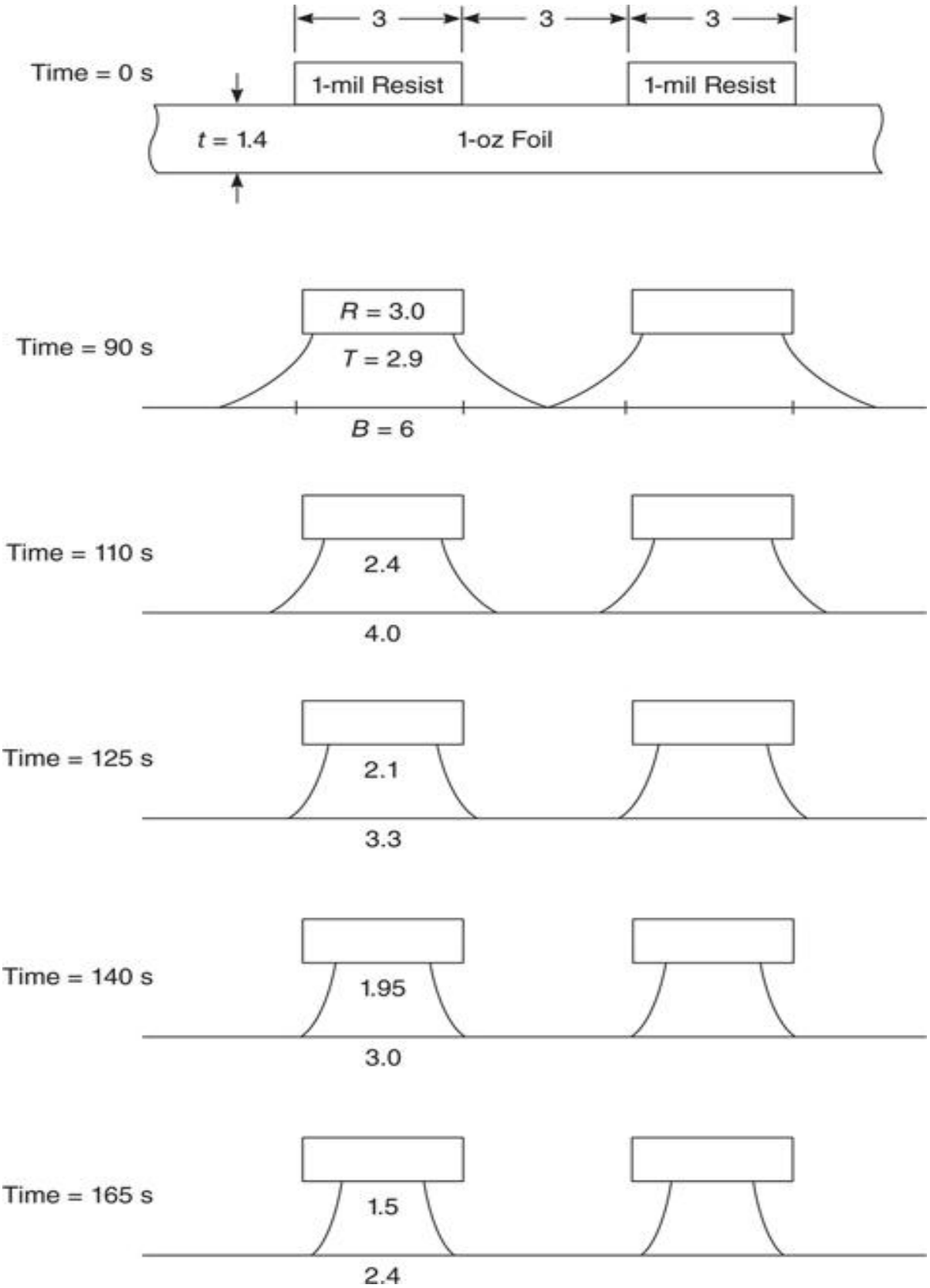

FIGURE 37.5 Line formation development.

There is an important conclusion to be drawn from these data. In order to compare or characterize an etch process (etcher to etcher, etchant to etchant, condition to condition, etc.), it is not sufficient to only use the undercut or etch factor alone. The data must be evaluated at a given *R/B* point for the same foil, resist, artwork, and panel size. If these factors are not held constant, the statement that "process A gives less undercut" has little meaning—additional etching gives more undercutting and straighter side walls.

37.7.3.3 Sensitivity Analysis. One of the extensions of the previous analysis is the ability to evaluate the sensitivity of the process. This is a study of the change in the result (*R/B*) due to the additional etching (relative time). Relative time is the ratio of the actual etching time to the nominal etch time taken to reach *R/B* of 1.0. In Table 37.2, it took 140 s to reach *R/B* = 1, but only 25 s (18 percent) more etching to achieve 25 percent overetching (*R/B* = 1.25). This sensitivity indicates that a small amount of overetch time could cause overetched 3-mil circuits. In this example, the etching process is slow enough to be controlled with the adjustment of the conveyor speed in the etcher. However, if the etchant were twice as fast (alkaline, for example) with the same sensitivity, it would be difficult to accurately "dial in" the proper result. Further evaluation of the cumulative variation from several variable properties on the overall product capability statistics can be found in the literature.[38]

37.7.3.4 Implication for Improved Processes. As a practical process application, it is often desirable to improve the etch factor to get a more square shape of the etched profile. One method for accomplishing this is to design the phototool for wider lines than desired, and then overetch to the desired endpoint. This practice increases *F* at the expense of also increasing *U*. However, as spaces get smaller, there is no space available for additional resist linewidth, because the fluid activity is restricted so that the etchant is stagnant

between the traces. Therefore, resist width near the final line specification and precise control of the etch process are required to obtain desired shape profiles within the $R/B = 1$ degree of etching. As feature specifications tighten, the process to do this may need to be altered. One patented approach is to finish the etch with a specific slower-speed fine-tune etching chemistry to be able to stop the etching process at precisely the correct point.[39]

37.7.4 Fine-Line Formation Etching Requirements

37.7.4.1 Fine-Line Definition. The term *fine line* is a relative one because the current state of processing by conventional available technology is constantly improving. Therefore, fine lines can be considered the next extension of capability that requires precision higher than that afforded by available technology. This is understood by means of statistics and standard gauging tools. The measure C_p (simple process capability) evaluates the variability of output results ($6s$, where s is the standard deviation of the linewidth distribution) to the specification limits of variation.[40] The data for the performance can be obtained by using a standardized test vehicle (IPC-9251) or a commercial testing program by CAT (see Chap. 36). In general, fine lines can then be defined as the linewidth point at which yield performance begins to drop below the run of production. Note that it is up to the customer and shop to determine what product line variation (usually a percent of line dimension) is allowed. It is apparent that this definition depends on the available technology and operation of the individual shop.

37.7.4.2 Limitations—Practical Rule of Thumb. It is useful to have a practical limit to express an understanding of where the technologies may limit performance. In the case of etched linewidth, it has been expressed that the total of the

resist thickness plus the etched foil thickness would limit the gap between the etched features. Therefore, for 1.2-mil dry-film resist over 1-oz copper foil, the total thickness is 2.6 mils. This could be used as a practical limit for both the trace and gap. Further limits can be determined by the undercut and etch factor experienced for the same type of etched features. Therefore, using the $R/B = 1$ data from Table 37.2 ($U = 0.525$ mil), a 2.6-mil resist line would be 2.6 mils at the trace bottom and would have a 1.5-mil etched top reduction, leaving only a 1.1-mil top surface. It must then be determined if these dimensions (with allowance for variations) are sufficient for the design functionality.

37.7.4.3 Thinner Is Better. In general, it follows that thinner foil and thinner resist allow for smaller features. However, if thin foil (9 µm, ¼ oz) is used, the traces may be plated to achieve better current capability. Thin resist may be used, but the image may be susceptible to handling damage or damage in the process equipment. However, for coated resists of 0.4 mil and ¼-oz foil (0.35 mil), the result could indicate a limit of 0.75 mil (19 µm). In fact, there has been a process using 3- and 5-µm foil to produce 30-µm line- and spacewidth patterns with 14 µm additional plated copper (total trace height of 17 and 19 µm). This method uses both panel and pattern plating.[41] The original foil was etched from thicker commercial foil laminate to the working thickness.

37.7.4.4 Changing the Microchannel Flow. As previously explained, the flow in the microchannels surrounding the features is critical in achieving uniform and accurate etching results. There is a unique process development using fibers to affect localized fluid mixing in these channels.[42] This approach requires specific patented equipment and processing methods.[43] Reported results down to 50-µm (2-mil) lines and spaces in 1-oz (37-µm) copper have been produced with 1.4-mil (37-µm)-thick resist. This is a very unique and important result because conventional foil and

resist technology can be used to make features significantly smaller than conventional capability through improved fluid application mechanics.

37.7.4.5 Beyond Fine? HDI Impacts. High density interconnect (HDI) technology involves several technology changes to form the circuitry. The highlight, as the name implies, is small via structures made in a layer-by-layer methodology with a built-up thin insulator and thin foil structure. To achieve the interconnection, thin and precisely controlled traces are required. The technologies, such as the two previous items, are becoming available to attack the needs of the products. As layer counts increase, the accumulating yield implications are significant, so that each process must produce minimum defects. For etching, one of the challenges is to make the resist conform to the surface—which forces the structural materials and processes to engage planarity of the end stage process as an issue. Etching capability requires improving the precision, stability, and capability of processing. The flowchart in Fig. 37.6 graphically illustrates the effects required for etching concerns and approaches to address these.[44] It is significant that there are no new concerns added to previous discussions.

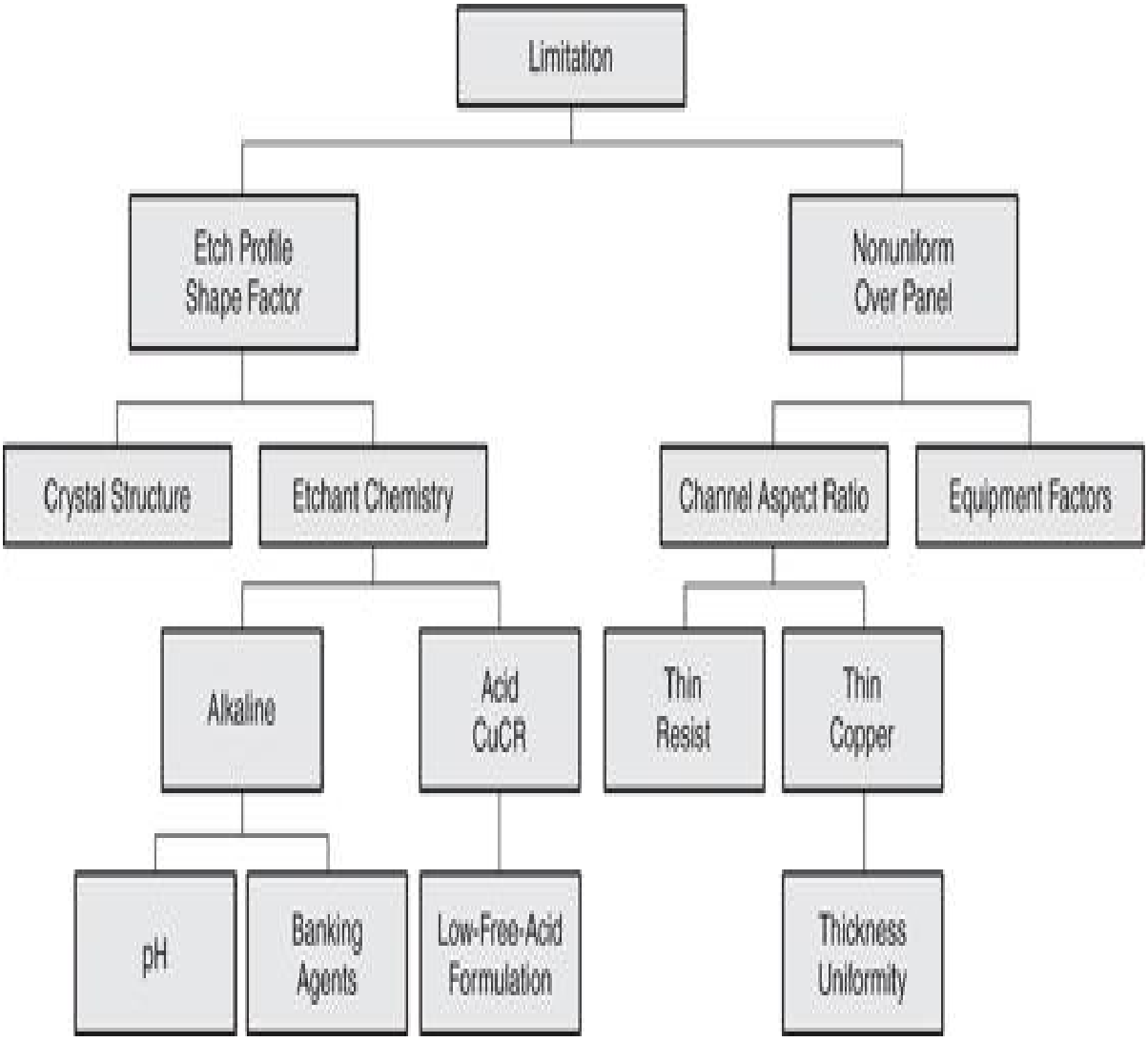

FIGURE 37.6 Flowchart for study of resolution of HDI etched product limitations. Profile and uniformity limitations may be studied for process improvement by progressing down the chart for contributing elements.

37.7.4.6 Stability and Control. It is important to measure and understand sources of variation in order to eliminate them. The gauging tools mentioned previously are very useful for collecting the data for analysis. One important feature is the positional and orientational variation in line geometry. Various conclusions can be taken from feature variation by location across the panel and orientation relative to the direction of motion. Repeating the gauging technique on a regular basis can allow observation of changing conditions within the process (such as plugged nozzles and other defects).

Another type of variation can be obtained by examining a series of gauge panels progressively processed with specific time-lag variations. If etching chemical controls are not adequate, the etch rate may vary in the sequence and therefore cause line variation with time. Usually, regeneration equipment can be adjusted or modified to minimize these variations, but the value of such instrument upgrades can be determined easily by data recorded about the type and extent of defects incurred.

37.8 EQUIPMENT AND TECHNIQUES

Etching equipment for circuit line formation has developed many variations on spray processing equipment. Often, as members of a coordinated automatic immersion plating process line, there are immersion etching tank varieties for microetching and surface preparation. However, for individual panels, conveyorized spray processing is clearly established because of efficient part handling and processing effectiveness.

37.8.1 Spray Equipment Basics

37.8.1.1 Construction. Etching equipment must be made from materials for long life, good dimensional stability, and resistance to chemicals and temperatures (130°F and higher). The basic construction includes rigid plastics (PVC, polypropylene, CPVC, and PVDF), metals (titanium, Hastalloy C), elastomers (vinyl, Viton A, Kel F, ethylene-propylene), specialized composites (epoxy-glass, graphite, and carbon-filled polymers, and other specialized formulations), and glass or clear and translucent polymers for visibility. The challenge is to select proper grades, compositions, and properties for mechanical strength, functionality, and durability. Equipment manufacturers perform these tasks in their design process.

37.8.1.2 Controls. Controls and electronics are significant because the increasing robustness and precision can have a large impact on cost. Therefore, the compromise on cost-effectiveness/technology trade-off often is made with a market-price primary goal. Therefore, cost-benefit analysis must be made by purchasers to evaluate available upgrades in instrumentation. The key controls are temperature, pressure, conveyor speed, and safety interlocks. Temperature is especially important because the etching reactions are usually exothermic and heat must be removed by cooling water coils to maintain stable rates. Conductivity, pH, density, ORP, and other process chemical control instruments may be added to monitor and control the processes. These instruments may be integrated into a PLC or computerized control system or may be individual control-panel stand-alone instrumentations. The wiring and the control cabinet itself must be suitably fume and hazard protected for water and chemical splashes as well as corrosive fumes. It is desired to have critical condition displays available to operators in the machine environment as well as some means of monitoring and recording process information.

37.8.1.3 Spray Strategies. Individual equipment designers have implemented very different types and mechanisms of spray attack on the panels. It is important to realize that the spray system design must be carefully integrated with the conveyor and mechanical design to minimize the effect of rods, wheels, panel control devices, and other mechanisms to achieve both uniformity and geometry of the features produced. It must be realized that the effect of the sprays is not merely the attack by droplets on the surface, but that the sprays are the prime drivers of the direction and effectiveness of the microchannel fluid flow on the panels. Therefore, separate controls and gauges must be provided for top and bottom spray arrays. For maximum precision, four quadrant controls are often beneficial. The mechanical spray arrays can be described as a variation of the following types.

37.8.1.3.1 Fixed Spray Array. This is a system of spray tubes containing multiple nozzles connected transversely across the conveyor to a header pipe on one or both sides. The spray nozzles are placed into the tubes in a pattern designed to optimize the effect. Care must be taken to install and orient the nozzles properly for designed effect. Mechanical intervention to selectively activate (or deactivate) portions of the design to effect the fluid dynamics of particular patterns should be included.

37.8.1.3.2 Oscillating Sprays. This system uses spray tubes that are connected generally to be aligned with the conveyor direction (often at a slight angle). The ends of the spray tubes are made with rotating seals so that the tubes can be moved back and forth by an oscillating crank or gearing mechanism. The nozzles move the liquid in a pattern generally across the conveyor travel. Individual spray tubes may be throttled and/or selectively activated.

37.8.1.3.3 Reciprocation. These nozzles are usually placed in an array similar to the fixed system, and the entire array is moved by a cranking mechanism in a direction across the conveyor. Maximum precision offerings include various patterns of nozzles that can be separately valved and selectively activated by computer controls.

37.8.1.3.4 Spray Nozzles. Spray nozzles are available in several types, sizes, and materials. For etching it has been established that PVDF nozzles are robust and consistent. The nozzle patterns are flat fan, full cone (round and squared), and open cone designs. Generally, flat fan nozzles have large openings and high impact for a given flow rate, while round cones have lower impact and orifice restrictions to ensure the pattern is filled. One of the principal failings of nozzles is simply clogging. The best array design can become dangerously nonuniform simply by plugging a small number of sprays. There is a commercially available nozzle that has a self-clearing fan design. Many are installed. For some applications, filtration between the pump and sprays has been installed to prevent plugging.

37.8.1.3.5 Selection. All of these combinations of nozzles, arrays, and mechanisms offer benefits and drawbacks that are often counterintuitive to the end user. It is necessary, therefore, to test and evaluate the performance of the spray systems for the work type and working environment. Testing of performance must be evaluated in a carefully controlled trial or by comparison with a standardized gauging tool.

37.8.2 Spray Equipment Options

37.8.2.1 Vertical Panel Orientation

37.8.2.1.1 Batch Operation. Some of the earliest equipment is still useful for prototype manufacture. This equipment holds a single panel on a workpiece that is generally rotated about an axis and sometimes oscillated as well. The sprays are addressed from one or both sides of the work and may be fixed or oscillating. This type of equipment usually is limited to small panels. The liquid all drains off the panel and falls into a collection sump. The panels must be removed after etching is complete and placed into a separate rinse vessel. (Some equipment has been designed to divert the drain and spray water onto the same work orientation.) This equipment is not capable of high capacity but has been able to etch high-quality work.

37.8.2.1.2 Conveyorized Operation. There are several versions of large machines that accept vertically oriented workpieces, convey them on a series of rollers from beneath the panel, and stabilize the work with rollers or wires. There are some machines that suspend the panels from the top surface. Vertically oriented nozzle arrays, either stationary or moving, spray the panel surfaces. These machines have been more successful in developing than etching because the depth of the image to be developed is formed by the exposure rather than completely depending on the etching fluid dynamics. All the liquid sprayed on the panels is removed by running downward off the bottom panel edge; therefore, the nozzles

must be specifically designed to offset the effects of higher amounts and speeds of down flowing etchant progressively toward the panel's lower edge. It is obvious that very thin workpieces can have difficulty being conveyed through this design.

37.8.2.2 Horizontal Panel Orientation

37.8.2.2.1 General Operation. The most widely used configuration of etching equipment handles the panels horizontally on a roller table support. The panels placed on the rollers move constantly through arrays of sprays above and below the work. One of the principal design challenges is the fluid flow control of the liquid pool that builds up on (and runs off) the top surface of the panel. The various designs of the spray system must allow equally good and equally fast etching beneath the panel as on top. In a well-conceived design, the simple adjustment of spray pressures can achieve this balance.

37.8.2.2.2 Conveyance. The conveyor design is particularly critical. Rollers must turn at constant speed to ensure that the surfaces are not rubbed and damaged. Chains and gear designs have been successfully used. The potential problem areas are the entrance and exit squeegee rollers and the changes from one machine drive section to another. The roller wheels themselves need to be made of compliant materials that have flat area contact with the panels (rounded contact areas allow points that can cause resist damage, especially if the rollers harden with age). The wheels must be spaced far enough apart to allow the bottom spray to hit the panel with minimum shadowing, but close together enough to convey thin work without sagging or deforming.

Thin panels (0.0015- to 0.003-in insulation core) are difficult to convey because the leading edges must feed consistently from one roller to the next in spite of the downward force of the fluid. In addition, the deflection of the panels between rollers due to fluid loading can cause lack of uniformity in etching. Often, special mechanical guides such as clips or wires are used to overcome these difficulties. Problems occur

when the guides stretch or are misplaced during production. If one panel jams, then the others behind it continue to jam and pile up, resulting in a major problem when discovered. The clearing of the jam often requires removal of rollers that are usually enmeshed in the mass of displaced guides and work. Not only are damaged panels costly, the downtime to renew the equipment and reestablish production causes significant production delay. One particular patented design features a combination of rollers and spray force that assures robust transport while simultaneously improving planarity for spray action.[45]

Truly flexible circuitry requires even more enhancements for reliable transport. Frames and screens have been used in the past, but these fixtures require extra handling and cause drag-over and cleaning problems. For sheet-cut panels, the best solution is a leading edge support attached to the panel by tape or mechanical clips. Usually these panels are attached and removed manually, but automatic systems could be provided. Flexible circuits can also be manufactured in continuous rolls that can be threaded through multiple processes. In addition to the previous difficulties with planarity and drag-over, the precise synchronization of roller speed throughout all the processes is mandatory. Therefore, machine and processing speeds must be carefully planned at original manufacture to allow proper dwell settings and latitudes. Rinsing and drag-over present problems.

37.8.3 Rinsing

Rinsing is a process technology that needs particular attention because of the multiple needs of uncontaminated panels, conservation of rinse waters, and environmental discharge limitations. It is no longer sufficient to flood the panel with large amounts of water that are then discharged to sewers. The capability of technical analysis of this process has been published.[46]

37.8.3.1 Cascade Rinsing. The principal tool to effect the required change is the concept of multiple-stage cascade rinsing. This process includes the concept that a robust flow recirculated on a panel can reduce the concentration to a level in equilibrium with a much lower circulated water stream. The lower stream passes through a series of chambers of increasing concentration, while the work passes through a series of chambers of increasing cleanliness (in reverse order from the water). The end result is a small use of water capturing a relatively high level of contamination. The contamination level is many times the discharge limit for direct environmental discharge. However, the fact that the stream is relatively small and highly concentrated allows for reasonable treatment and recovery of by-products by ion exchange, direct electrowinning, or membrane cell concentration. In certain circumstances, the waste stream may be comingled with a main process stream for recycling (see Fig. 37.1).

37.8.3.2 Drag-Over Minimization. All of the contamination that eventually ends up in the water stream is that introduced by drag-over from the process itself (or from a recirculated environmental rinse). Therefore, the first step in successful rinsing is the reduction or prevention of materials from the panel. The conventional means of attempting this is by a set of pinch or squeegee rollers at the output of the chemical module. These rollers may be increased in effectiveness by softness or by pressure. Often, rollers made of PVA foam have been employed effectively. However, these rollers must be kept clean and moist to be effective. Other methods include improved baffling, ensuring capture of overspray, and low-velocity air blow-off. Proper management of drag-over on conveyorized equipment has reduced residues by a factor of 10 or better. Thin panels cause difficulties because the compromise made between conveying reliability devices and planarity and contact of squeegee rollers and surface tension reduces effectiveness of retention. Thick panels (over 0.125 in) also cause problems because squeegee

rollers and baffles must lift to clear the panels, allowing gaps for solution escape. It is therefore a subject for engineering study and process management trade-off decisions that must be considered during the specification process.

37.9 ACKNOWLEDGMENT

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[b] PA Hunt Chemical Corporation, West Paterson, NJ.

CHAPTER 38
ROUTING AND V-SCORING

Matthias Stickel
KSG Leiterplatten GmbH, Gornsdorf, Germany

38.1 INTRODUCTION

The routing and v-scoring operations have predominantly the function to give the printed circuit board (PCB) the final outline dimensions or to transform the shape and size from the production format of the PCB manufacturer to the required shape and size of successive processes (e.g., assembly). Especially for small parts are there big advantages in handling, when the single PCB is not cut out entirely, but left in a “subpanel” together with other PCBs. In addition to the reduced amount of handling is the efficiency of several steps requiring “alignment” increased at the PCB manufacturer (e.g., electrical test) and at the assembly process. Pre-cuts with tabs or other break-away features enable an easy manual or tooled singulation at any stage. As the routed features have multiple requirements concerning the alignment (to drilled holes, to the image, to the inner layers), several functions were added to CNC machines over the years. Examples are

- Routing of plated slots (instead of slot drilling)

- Routing of big holes (instead of circular slot drilling)
- Routing of larger diameters for unplated through holes to avoid broken tents
- Routing with camera alignment for critical alignments to the outer layer image
- Depth controlled routing
  - To reduce the thickness on the board edges for insertion applications
  - For cavities
  - To break electrical connections
- Pre-cutting to enable break-out after assembly
- Routing with special tools (v-groove cutters, chamfering, counter sink vias)

38.2 THE ROUTING OPERATION

In opposite to the drilling operation, in which the main material removal is made in the *z* axis leading to an axial force onto the spindle, the main material removal in the routing operation is made in the *x* and *y* axis, leading to a radial force onto the spindles. This requires not only different bearings of the spindles, but also a different focus on the movements of the table and the traverse holding the spindle as they heavily contribute to the material removal and with that the achieved speeds and quality levels.

There are several key elements involved in a routing operation:

- Alignment
- Router/router tool
- Machine
- Product
- Program/coordinates/hole locations

- Parameters/cutting conditions
- Supporting materials

All of them will be covered in this chapter in detail.

38.2.1 The Basic Principle of Routing

Routing, as subtractive manufacturing operation, belongs to the group of “cutting with geometrically well-defined tool edges.”[1] A relative motion of a rotary cutting tool and the workpiece is required to remove material from the workpiece to bring it to a desired shape, where the feed of the cutting wedge parallel to the surface generates a chip.[2]

Goals of this operation are

- Smooth surface
- Low force
- Short time/fast processing
- Long tool life

These goals typically need to be compromised and can be influenced with the selection of different, dependent angles of the cutting tool and the parameters. The angles and geometries contributing to the material removal when the tool penetrates the workpiece can be seen in Fig. 38.1.

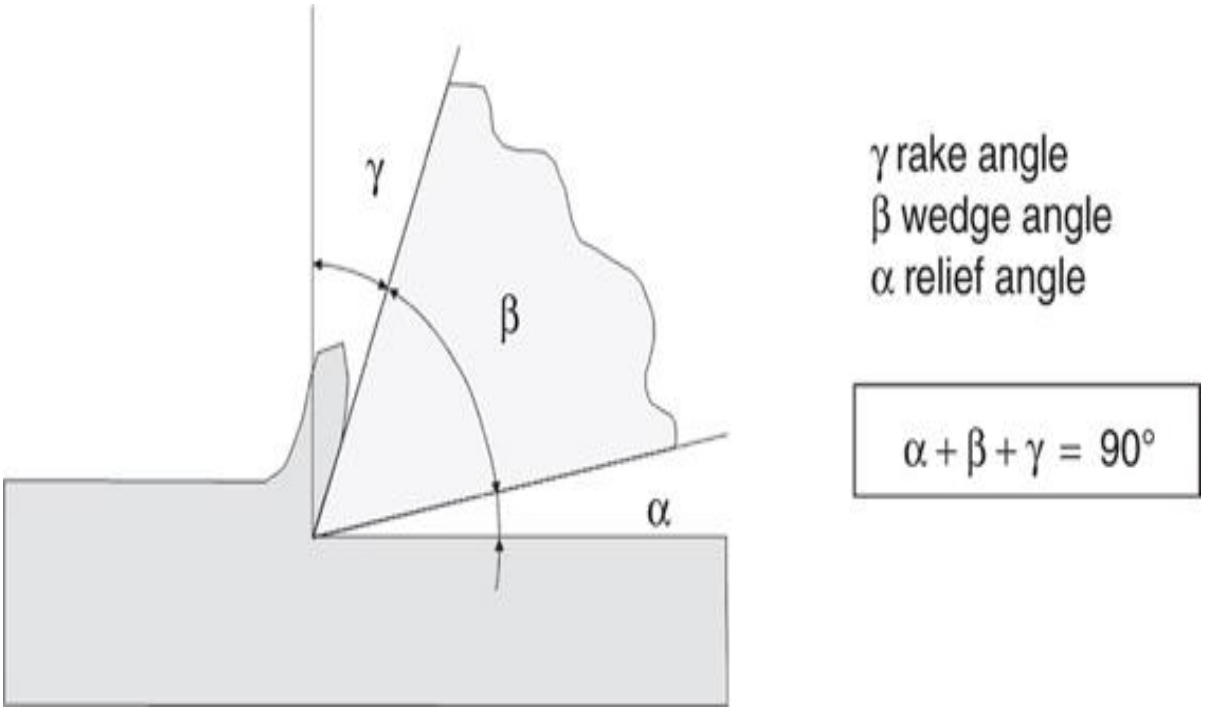

FIGURE 38.1 Geometries during a chip generation/formation.

Looking at the different angles are some general statements possible:

The smaller the wedge angle, the lower the required force to generate the chip. However, needs the wedge angle to be matched with the material that is to be removed. If it is too small for the selected application, the result is excessive wear or break outs of the cutting edge. The harder the material, the bigger needs the wedge angle to be. The relief angle determines the amount friction and generated heat. The softer the material, the bigger the relief angle needs to be, as soft materials generate more friction and heat. The rake angle determines and influences the type and size of the chip. Large rake angles can generate a continuous chip (depending on the material). A negative rake angle leads to scraping and a very small amount of material removal.

The quality of the routing operation is not only defined by the materials, the selected geometries and the cutting conditions, but also to a large extend by the selected method or for peripheral routing by the considered side, as the chip

formation is totally different for the sides. The basic cutting principals are shown in Fig. 38.2.

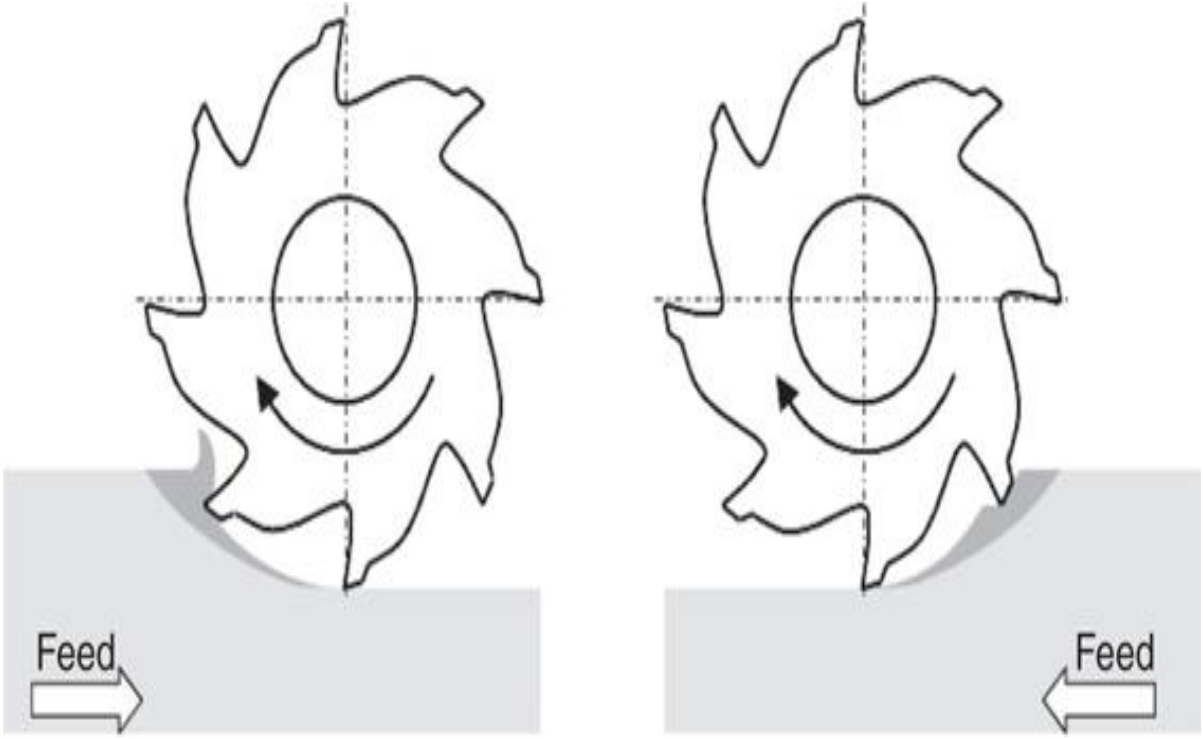

FIGURE 38.2 Routing operations: conventional milling (*left*) and climb milling (*right*).

While for “conventional” or “up” milling the chip starts at zero and ends at the maximum thickness, the chip formation for “climb” or “down” milling is in a way that it starts at the maximum thickness and ends at zero.

Looking at the routing operation in the PCB industry, where there is a relative movement between the rotating tool perpendicularly to solid material, both principles are present in the same operation. These different cutting conditions on both sides result in different quality levels and a “good” and a “bad” side. As the result the conventional or up milling leads to a better edge and can be considered as “good” or product side and the side with the “climb” milling as the “bad” or scrap side (Fig. 38.3).

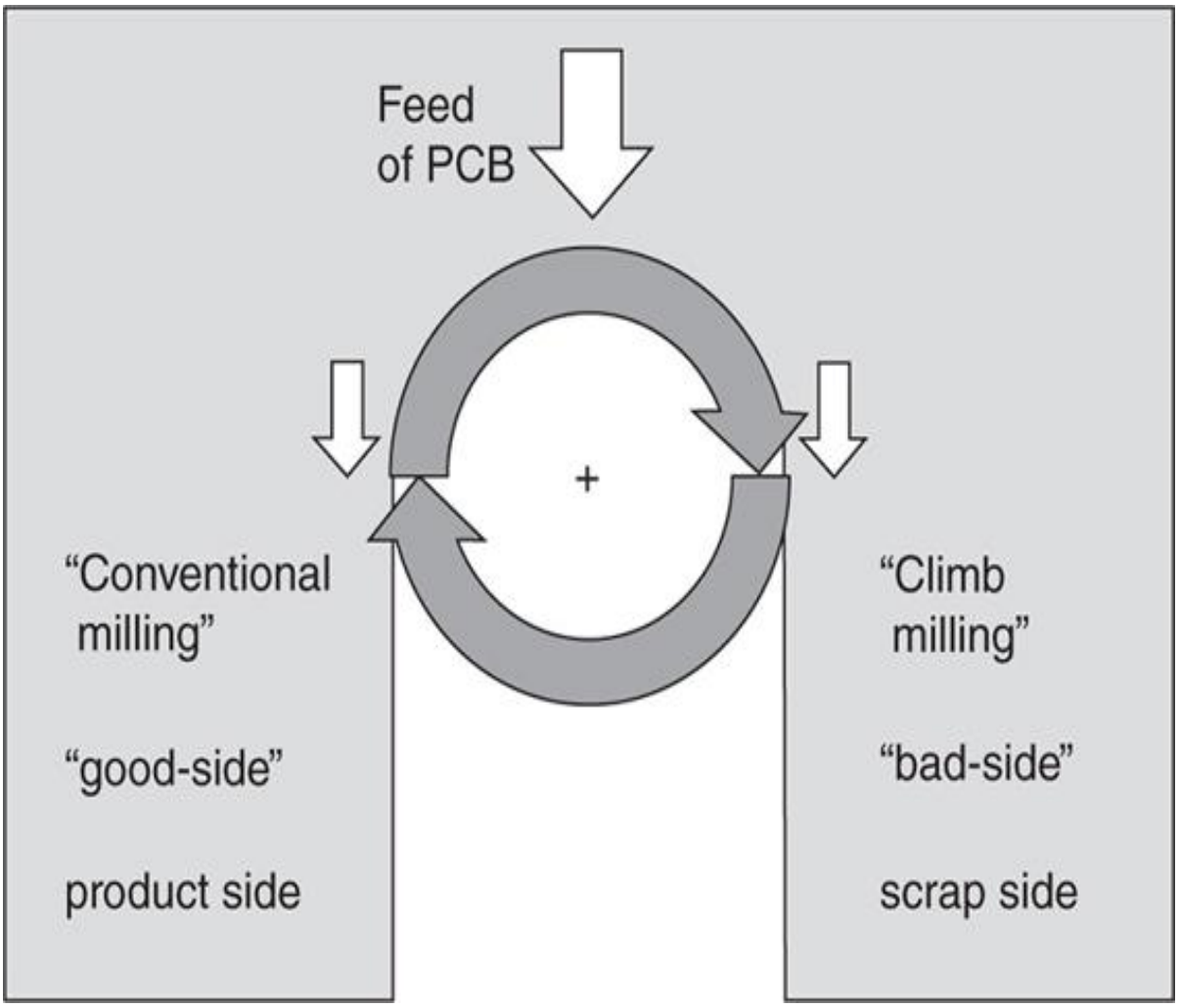

FIGURE 38.3 Cutting conditions routing into solid material.

This is the reason why the orientation of the motion of the tool to the PCB is performed counterclockwise for depanelization, singulation, profiling or outer contours of the PCB and clockwise for cutouts within a printed circuit board always leaving the side with "conventional" milling cutting conditions on the product.

Figure 38.4 also demonstrates another aspect which needs to be considered during the routing operation: the tooling or design data of a specific layout show the outline dimensions after processing. If this would be the path of the router, the PCB would turn out to be too small, as for each routed line additionally the radius (or half the diameter) would be taken away. Special machine commands compensate this defining if

the router tool is to the left or to the right of the structure. In doing so is the radius “compensated,” meaning that the center line of the tool is shifted accordingly by the radius to one side.

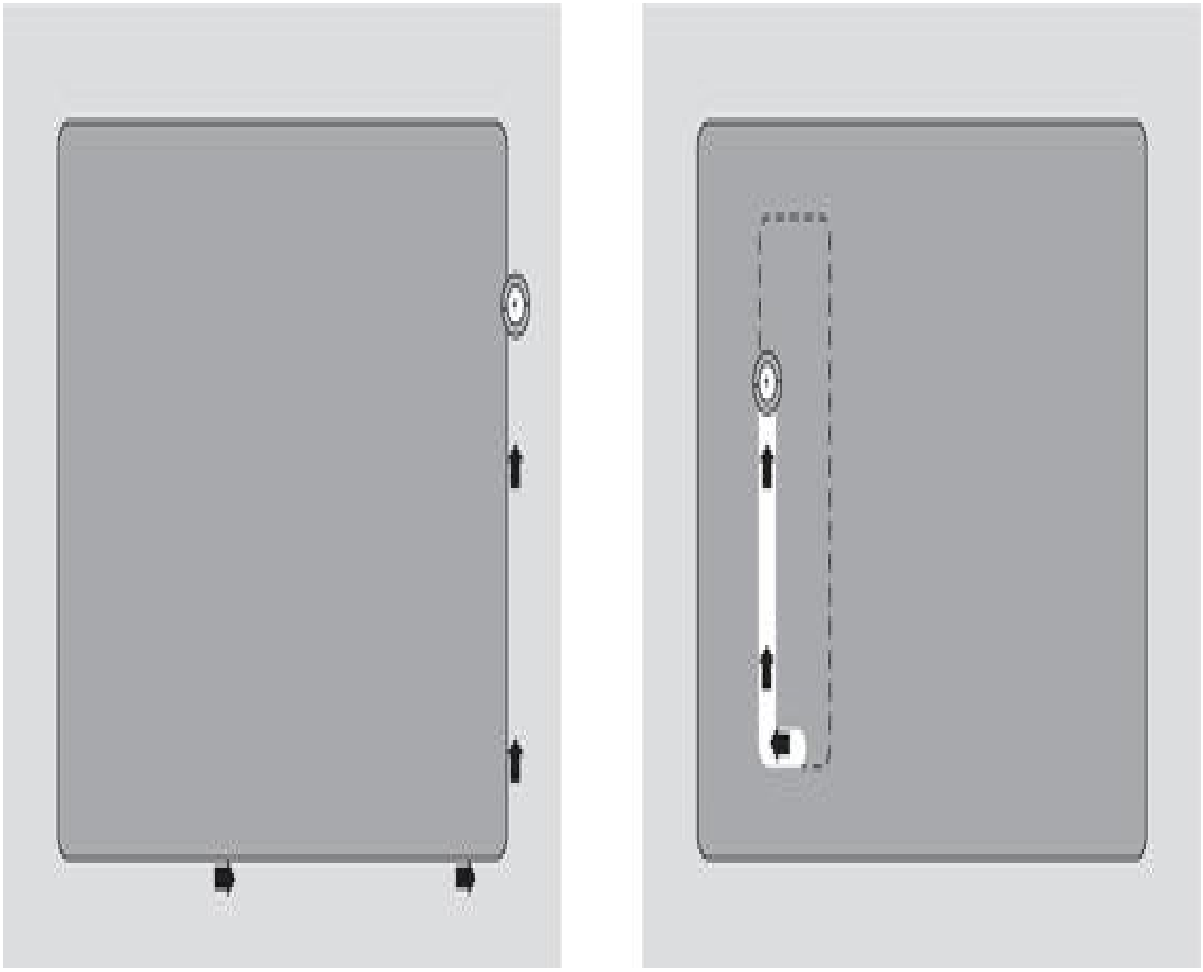

FIGURE 38.4 Selection of cutting orientations: counterclockwise (*left*) and clockwise (*right*).

In addition to the general compensation of the radius (also “cutter offset”) which is required due to geometrical aspects, is also a product and process related compensation required. Based on the combination of the table feed and the rotating tool is there an additional force to the side resulting in a deflection of the router. This deflection will change the effective dimensions and needs to be compensated (for inner and outer contours) as well. The amount depends on the tool (diameter, length, material, geometry), the stack (height,

material) and the selected cutting conditions (feed, speed) and with that is so individual, that it needs to be determined in a pre-run for every new product for best results.

38.2.2 Alignment/Stacking/Pinning

The alignment in the routing operation can be done in several ways. Selection criteria are the outline tolerances and the degree of automation which is practiced in the manufacturing shop. Considering manual loading and unloading are the production panels aligned with two pins (in the center of the short axes) or four pins (in the corners) in the area of the panel frame. With that, is the alignment done outside of the active area so that the panel frame, including the pins, remains fixed to the table, while the cutout boards which are loosely on the table can be removed from the machine after the program is run. The pins are either fixed into plastic inserts or fixtures on the table, so that the stack of multiple PCBs is generated manually by piling one panel after the other, after putting a backup material on the table.

Another option is to generate the stack in a separate operation by pinning the defined number panels together. This is done with two to eight pins. The entire stack is then aligned by inserting the pins into holes in subtooling plates manually on the table (with a backup material in between).

In an automated loading system for which the stacks are also generated in a separate operation, there is only an alignment with two pins possible. These pins need to be on one axis (typically in the center of the short axis) and are fixed with a prism slot clamping system. As the PCBs or subpanels are cut out of the panel frame is the unloading done manually.

Another option is to have multiple pins in a fixture, so that each board is aligned with pins when the stack is generated and not only each panel. The advantage is, that after the program is run, the boards are not loosely on the table, but stay fixed on their pins until they are removed. The

disadvantage is that this type of alignment requires product/layout specific fixtures which need to be generated in advance. This is the reason why especially for small volume productions usually the other alignment approaches are selected and in case of concerns the boards are additionally fixed with tape to prevent damage after being cut out.

38.2.3 Machine Preparation

Before the entire lot can be processed in the routing operation, the machine has to be set up by

- Loading the program (coordinates and diameter information)
- Loading the parameters or parameter files
- Loading (additional) tools
- Performing a first run
- Measuring the actual dimensions
- Doing additional RC (radius compensation) adjustments

The routing programs are generated with a CAD/CAM system, similar to the drilling programs, by adding board shop specific routines (pilot holes, definitions of the routing path, or tool direction, etc.), to the outline dimensions. The set up (loading the program and the tools, etc.) is also in the same way as for the drilling operation.

38.2.4 Loading/Stacking

For the peripheral routing, when the PCBs are cut into single pieces or subpanels, much bigger diameters are used compared to the drilling operation. This is why stacking, putting several PCBs on top of each other to cut them out simultaneously to increase efficiency, can be practiced in a greater extend. The stack height should not exceed 75 to 85

percent of the effective flute length or the flute length should be chosen accordingly whereas the depth in the backup material and the optional entry material needs to be considered part of the stack as well.

38.2.5 De-Stacking

After the program is run the singulated parts need to be taken out of the machine regardless, if the product is cut out into single pieces or in subpanels. Additionally need the panel frames to be taken out and the pins removed. The PCBs need to be checked for scratches, burrs, or tips.

38.3 MATERIALS

The materials involved in the routing operation are defined by the quality level that needs to be achieved. The main materials that can and need to be selected are

- Router
- Entry material
- Backup material
- Pins, tooling pins
- Soft tools

38.3.1 Entry Material

As there is much less movement in the *z* direction compared to the drilling operation there is no real need to center the router when it penetrates the stack or to clean the router when it leaves the stack. But there are other aspects that might require an entry material:

- To protect the metal surface during the routing operation

- To prevent burr on the entry side
- To transfer and spread heat off the router

Routing is one of the last manufacturing operation steps of a PCB and with that almost all value is added to the product at this stage. This typically also includes the final surface finish which can be sensitive for scratches. As the tool moves in *x* and *y* direction during the operation, the challenge for the pressure foot is to press the stack together, without damaging the surface. This is realized with circular or donut shaped brushes around the cutting tool. The brushes have to have a certain rigidity to press the stack together, but on the other hand they have to be flexible enough to accommodate/compensate changes in the topography due to the circuitry on the outside of the PCB. For sensitive surfaces or critical applications might an entry material be required, as already a small burr caught in the brush can lead to scratches and with that to violations of the acceptability.

The material can be a melamine phenolic. As an alternative are sometime laminates or cores used and the copper in an etching step removed, which makes this type of an entry a fully cured, glass reinforced epoxy material.

38.3.2 Backup Material

The backup materials main function is to protect the machine table from being damaged. Burr on the bottom side of the stack or where the tool exits the stack is also something that has to be paid attention to. But as this is most critical in the *z*-axis direction, conservative/moderate infeed rates can be chosen for the routers as the number of *z*-axis movements is rather low. The backup material is typically made of wood-chip composites. But in opposite to the drilling operation in which for every run a new backup side is used, are the backups in the routing operation used multiple times. This has not only economic advantages, but is also beneficial for the quality as

additional room for the swarf is available and together with a good vacuum reduces the heat generated during the operation. In cases in which there are product specific challenges with burr, regardless if in the area where the router enters the stack or along the routing path might unused backup material be required. This backup material should ideally be processed and structured with the same program before the stack is added and the program run a second time. The diameter for the prerouting of the backup material should be chosen smaller than the router of the conventional program, ensuring that the tools of the conventional always hit solid materials on the edges. In this case can the backup material be used only twice (once per side).

The routing depth into the backup material needs to be compromised between a maximum generating much room for the swarf and a minimum to reduce the additional heat generated on the router. Typical values are 1 to 2 mm, with smaller values for smaller diameters.

38.4 MACHINES

There are no major differences between the CNC routing machines and the drilling machines used in the PCB industry. The selection of different elements, options and components are enough to optimize a machine for routing applications. For example is the higher side or radial force something to consider in the section of the spindles. Since the tool diameter range is much smaller for the routing, including the much bigger minimum diameter, is the maximum spindle speed also not as relevant compared to drilling? The major elements are shown in Fig. 38.5.

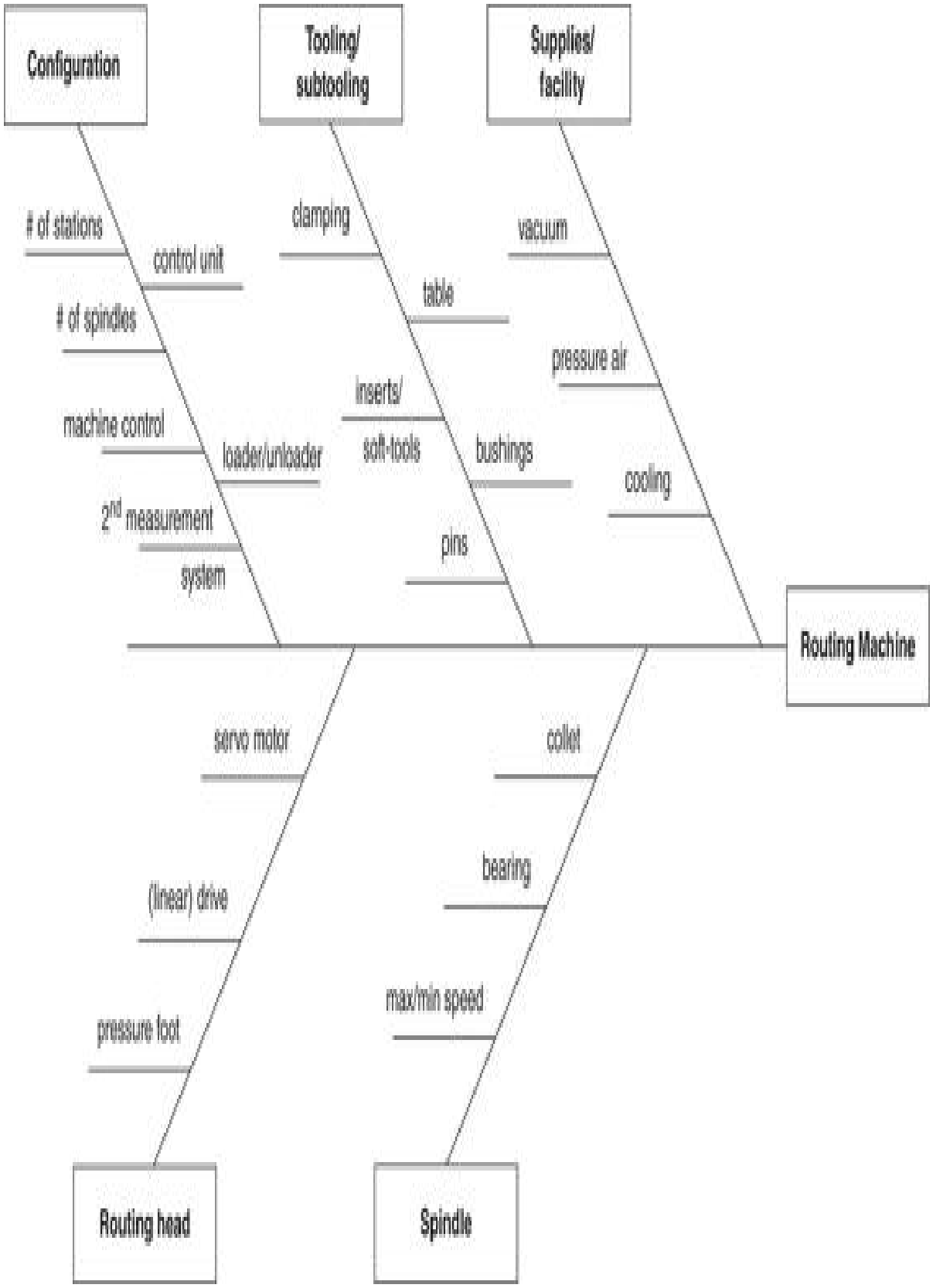
Configuration
Tooling/ subtooling
Supplies/ facility
# of stations
control unit
# of spindles
machine control
loader/unloader
2nd measurement system
clamping
table
inserts/ soft-tools
bushings
pins
vacuum
pressure air
cooling
Routing Machine
servo motor
(linear) drive
pressure foot
collet
bearing
max/min speed
Routing head
Spindle

FIGURE 38.5 Key elements of a routing machine.

The number of stations on which different stacks are routed at the same time defines the size and drives the weight. The range can be anywhere between 1 (for special applications, prototyping, etc.) and 6 stations (for mass production). The machine base and the traverse holding the routing heads are made of granite or mineral cast. The drives for the *x* direction (moving jointly all router heads) and the *y* direction (moving jointly all stacks) are linear. The *z* axes, moving the spindles up and down, either move jointly or independently from each other, depending on the configuration. The *z* axes can either be driven by ac motors with lead screws or linear drives.

Each station has a subtooling and up to three clamps on the long side (*y* direction) either fixing and holding each stack in place during operation or as additional clamping system for the subtooling plate in which the pins of the stack are inserted. The general alignment of each stack is done with pins. These can either be inserted into the subtooling (for example in interchangeable plastic inserts) for manual loading and stacking or are integrated in the stack, in case the stack is generated outside the machine in separate operation. In this case is there an integrated prism slot tooling in the table.

Each station is typically equipped with a laser measurement station controlling the tools prior and after use for length diameter and run out. In doing so, can tools with a wrong diameter or broken tools (after achieving the predefined maximum distance in the material) be detected. The tool storage is either done in cassettes or in a chain. Some PCB manufacturing shops still use routing machines using tools with plastic “rings” on the tool shank. These can define the distance in the backup and also protect the collet from swarf.

There are different types of pressure feet. On top the standard pressure foot, is one available especially developed for web and burr free routing. The function, also called “pressure foot routing,” can be activated with a special command in the program. Before the very last distance when a

PCB is singulated, the pressure foot remains in the same position and the router moves within the pressure foot. This enables a clean cut at the end. Without this function is there a chance the PCB moves slightly when it is separated from the frame leaving a small tip, which needs to removed manually. The last type of pressure foot is one with multiple functions. It has a special plastic or Teflon coating with which the surface can be detected very precisely (see mapping). For all applications (drilling, routing, mapping, “pressure foot routing”) should different pressures of the foot be selected, as the pressure can be of course higher when there’s no movement in *x* and *y*.

Special attention should be taken to the vacuum removing swarf and debris and with that contributing heavily to the resulting quality of the routing operation. Values of 80 to 120 mbar should be achieved to have good conditions. Additionally should the vacuum be shut off when the spindle moves from one PCB to the next to avoid that the cutout PCBs are dragged along. Small pieces which could clog the exhaustion need to be avoided by optimizing the routing path accordingly.

38.5 ROUTERS

38.5.1 Router Material

Similar to the drill bits used in the PCB industry are the routers predominantly made of solid tungsten carbide. To increase tool life are also routers with a diamond coating (PCD = **p**olycrystalline diamond) available.

38.5.2 Router Geometry

There are several basic types of routers for specific applications (Fig. 38.6).

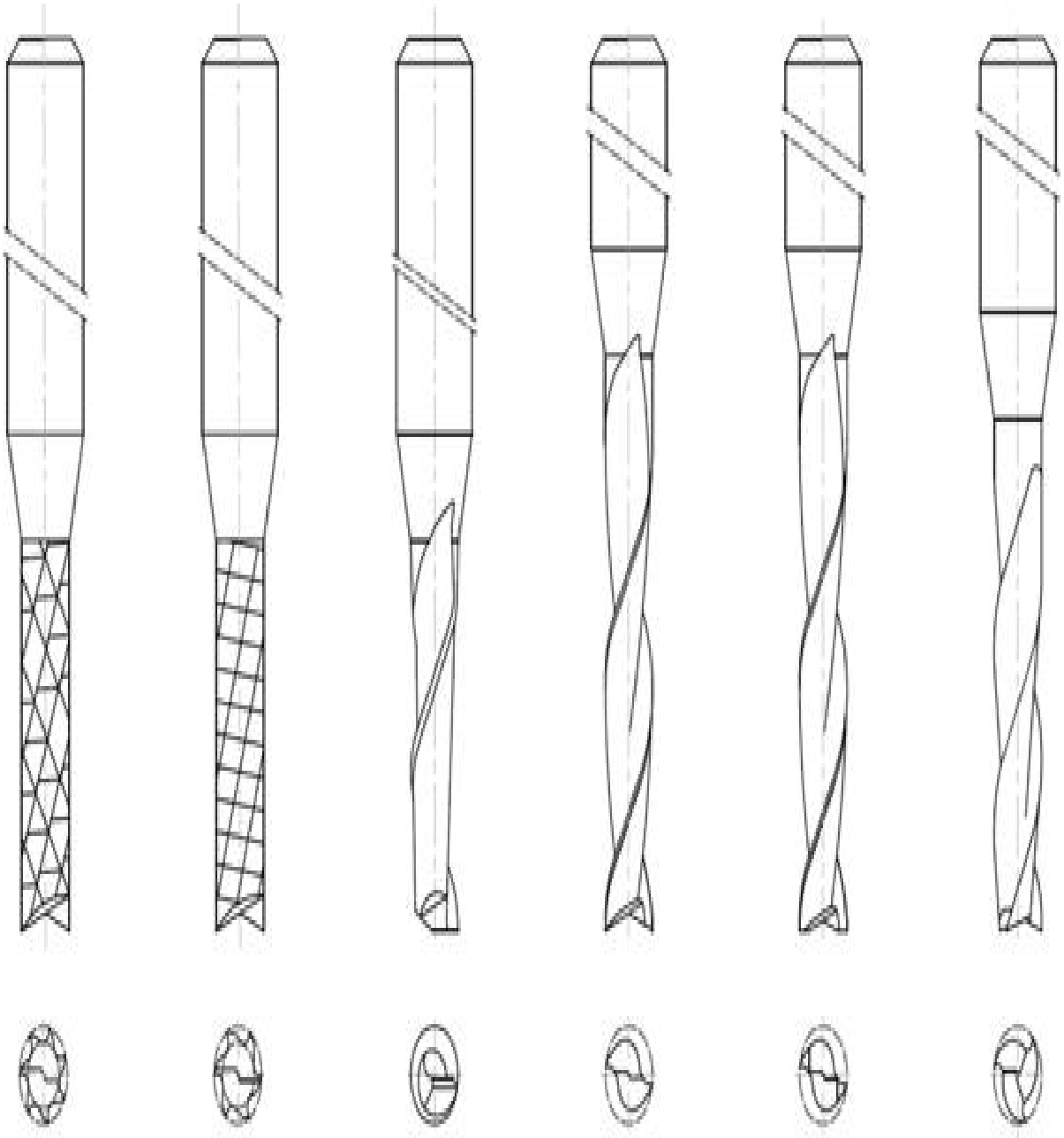

FIGURE 38.6 Router types (*left-to-right*): diamond cut, spiral cut, 1-flute, 2-flute, 2-flute, 3-flute. (Picture courtesy of HPTEC.)

- Diamond cut
- Spiral cut (with or without chip breakers)
- 1 flute
- 2 flute
- 3 flute

All of these tools are available with different orientations of the flute:

- Right-hand spiral/right-twisted flute: in case of conventional clockwise rotating spindles => up cut forcing the material upward out of the slot, toward the vacuum
- Left-hand spiral/left-twisted flute: in case of conventional clockwise rotating spindles => down cut forcing the material downward, pushing the stack together

In case the spindles are rotating counterclockwise is the effect in an opposite way:

- Left-hand spiral flute => up cut
- Right-hand spiral flute => down cut

Most router types are available with a variety of point geometries:

- Drill point
- Double drill point/M-cut
- Fishtail/fishtail with flat end
- Flat end

A special type of router is a v-groove cutter. This tool is not only used for conventional v grooves (v scores) for sophisticated patterns, but also to add chamfers (e.g., for connector insertions).

38.6 PARAMETERS

For the selection of the parameters is the main aspect on top economic considerations the quality level that needs to be fulfilled. Key drivers are the stack height and material that is to be routed along with the selected router (type and geometry). A big influence can be if a predrilling step in the area where

the router enters and exits the stack is done. This can improve the accuracy and due to the additional room for debris, also the quality level. A first starting point for the main parameters is typically provided by the router suppliers who develop general settings for their specific geometries.

Parameters

- Speed or RPM (revolutions per minute) n
- Infeed F_Z
- Table feed F_{XY}
- Chip load (XY) or depth of the cut
- Chip load (Z)
- Tool life

38.6.1 Speed

The cutting speed or surface speed is the speed of a point on the outside of the router. This speed is generally determined by the base material and if necessary adjusted for specific constructions or product groups. As this speed should be kept constant over the whole router bit diameter range, the spindle speeds need to be increased with reduced diameters and decreased for larger diameters.

Cutting speed	$V = n \times \pi \times d/1000$	V [m/min], n [rev/min], d [mm]
Spindle speed	$n = V \times 1000 / (\pi \times d)$	n [rev/min], V [m/min], d [mm]

38.6.2 Chip Load/Depth of Cut

The chip load or “depth of cut” as it is called for routing describes the feed or penetration of the router per revolution. As the routing operation can be performed in three axes in the material, there are two relevant chip loads and feeds (z axis; x

and *y* axis). The chip load is determined by the stack height, the materials that are to be routed and the router geometry (type, diameter, etc.) defining the material volume that can be removed per revolution. If the chip load is chosen too low and the teeth and cutting edges don’t penetrate enough, it leads to “scraping” and excessive generation of heat, influencing the result negatively. If the chip load is chosen too high it will lead to high(er) deflections and worst case to tool breakage.

Chip load (Z)	$f_z = F_z \times 1000/n$	f_z [mm/rev], F_z [m/min], n [rev/min]
Chip load (XY)	$f_{xy} = F_{xy} \times 1000/n$	f_{xy} [mm/rev], F_{xy} [m/min], n [rev/min]

38.6.3 Infeed

The infeed is the *z*-axis speed in which the router moves into/through the stack. The possible speeds depend on if “predrilling” is applied or not.

Infeed rate	$F_z = (f_z \times n)/1000$	F_z [m/min], f_z [mm/rev], n [rev/min]

38.6.4 Table Feed

The table feed is the speed in which the table and the traverse holding the spindles move in the *x* and *y* direction. It more results out of the cutting speed and the chip load.

Table feed	$F_{xy} = (f_{xy} \times n)/1000$	F_{xy} [m/min], f_{xy} [mm/rev], n [rev/min]

38.6.5 Tool Life / Router Life

Equivalent to the number of hits that a drill bit can perform is for routers the “distance in the material” defined and limited. As already mentioned above is the quality level that needs to

be achieved for the tool life the main driver. The wear, driving the quality, is in addition to the selected tool, heavily influenced by the cutting speed, the chip load/table speed, the vacuum and the product stack (materials, stack height, etc.). For standard FR-4 type materials is the maximum distance in the range of 40 to 60 m for a 2.0-mm diameter for a stack of 4.5 mm. For materials containing fillers is the distance reduced to 30 to 50 percent, depending on the type and amount of fillers.

38.6.6 Parameter Example

The example (Fig. 38.7) shows selected diameters to highlight some general items in a parameter table:

DRM [mm]	Speed / RPM [rev/min]	Cutting-Speed [m/min]	Table-Feed F_{XY} [m/min]	Chip-Load [mm/rev]	In-Feed Fz [m/min]
0,50	100000	157	0,3	0,002	0,1
0,60	100000	188	0,4	0,003	0,1
0,70	91000	200	0,4	0,004	0,1
0,80	80000	201	0,6	0,007	0,1
0,90	71000	201	0,7	0,009	0,1
1,0	64000	201	0,8	0,012	0,2
1,1	58000	200	0,9	0,015	0,2
1,2	54000	204	0,9	0,016	0,4
1,3	49000	200	1	0,020	0,4
1,4	46000	202	1	0,021	0,4
1,5	43000	203	1,1	0,025	0,6
1,6	40000	201	1,1	0,027	0,6
....	....	....	....		....
2,0	32000	201	1,1	0,034	0,6
....	....	....	....		....
2,5	26000	204	1,2	0,046	0,6
....	....	....	....		....
3,0	21000	198	1,2	0,057	0,6
3,175	20000	199	1,2	0,057	0,6

FIGURE 38.7 Example of a routing parameter file with a target cutting speed of V = 200 m/min.

- The maximum spindle speed is 100,000 RPM. This maximum RPM is required for diameters being smaller than 0.7 mm, resulting in a cutting speed deviating from the targeted 200 m/min for 0.6 mm smaller diameters.
- The minimum spindle speed is 20,000 RPM. This minimum RPM speed is required in the example at a diameter of 3.175 mm (which is equal to the shank diameter). If a smaller

cutting speed was chosen, the theoretically required minimum spindle speed would not be achievable with this spindle, resulting in a deviating from the ideal cutting conditions.

Properly chosen parameters not only avoid mechanical damage (on the tool or the product) but also have a big influence on the quality, where in most cases the quality level and economic aspects are compromised.

38.7 DEPTH CONTROLLED ROUTING

In addition to peripheral or contour routing are there more and more applications which require only partial removal of the material. Typical applications are areas of reduced board thickness along two sites supporting the insertion of the boards in rails. These features were realized in the past with conventional milling machines. Other applications are “cavities” in the PCB. These are areas where the all material above certain inner layer locations are removed, enabling direct access for the assembly of critical components and or simply reducing the overall height of the PCBA after assembly.

38.7.1 Mechanical Contact

One common approach for the routing in relation to the board surface is to detect the surface via mechanical contact or physical pressure. Required is the laser measurement station measuring the location of the tip of the router in relation to the pressure foot. When the spindle moves downward, the brush passes a physical pressure to the system. Once a certain level is reached is the surface determined. As the location of the tip has been logged, can the relative movement to the surface be started with a secondary measurement system.

38.7.2 Electrical Contact

Another approach is to detect the surface via electrical contact. This requires a conductive surface. It can be electrically detected when the router hits the surface and a relative movement to the “new zero” can be started with a secondary measurement system. The principle can also be applied for referencing to a copper inner layers. Additional holes and traces or bus bars to bring the connection from a conductive board or panel edge to the inner layer. The big advantage is that tolerances caused by thickness variations of the locally different resin flow of the pregregs in the lamination process become irrelevant.

38.7.3 Mapping

Another approach is to detect the surface of the board or the construction under the board physically at multiple predefined points. The relative *z* height is detected and put into a map and considered in the depth controlled routing program. In addition to the laser measurement station, the secondary measurement system and the mapping software option is a special pressure foot required to eliminate the additional tolerances of the brushes.

38.8 V-SCORING

V-scoring is a special form of routing, for the generation of breakaway areas as an alternative to conventional, peripheral routing with reduced requirements on the edge quality. The material is removed with cutting tools from the top and bottom side of the workpiece (PCB) simultaneously, leaving grooves with a v shape on both sides. The remaining material in between the grooves, the web, predominantly defines the force which is required to break the two pieces apart (see

Figure 38.8). The breaking or separation can be done manually in case of thin webs or with special separation tools for thicker webs. The latter is, for example, practiced when additional processing steps (during the manufacturing operation or at the assembly) between the cutting and the breaking are done, for which a certain stability of the production unit is required. A separation with machines improves the edge quality compared to manual breaking.

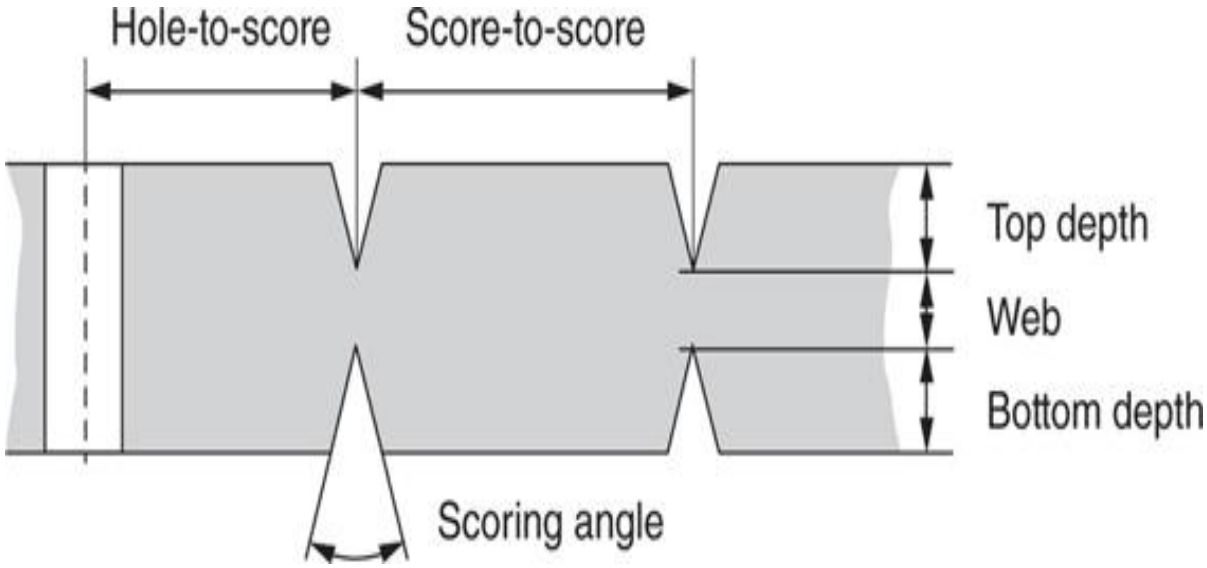

FIGURE 38.8 Key tolerances on products with v-scoring.

The v grooves can be generated parallel to the short and long production panel sides, requiring a 90° rotation during the operation if grooves in both directions are required. Interrupted grooves, so called jump-scores, can be generated as well. In case of round corners or other structures deviating from the orthogonal grooves are routing and scoring combined. Key tolerances are shown in Fig. 38.8.

38.8.1 Scoring Tools

The cutting tools, blades, or saws are available in solid carbide with or without coating and in PCD, with the PCD tools having typically 24 teeth and the solid carbide tools having 100 or 120

teeth (see also Fig. 38.9). The scoring angle (20° to 30°, 90°), defines the material volume which needs to be removed to achieve a certain depth. Additionally is also the groove width and with that, the minimum distance to the next feature defined by the angle. Tools with bigger scoring angles (100° to 140°) are also available if the application requires special geometries for edge beveling or chamfering.

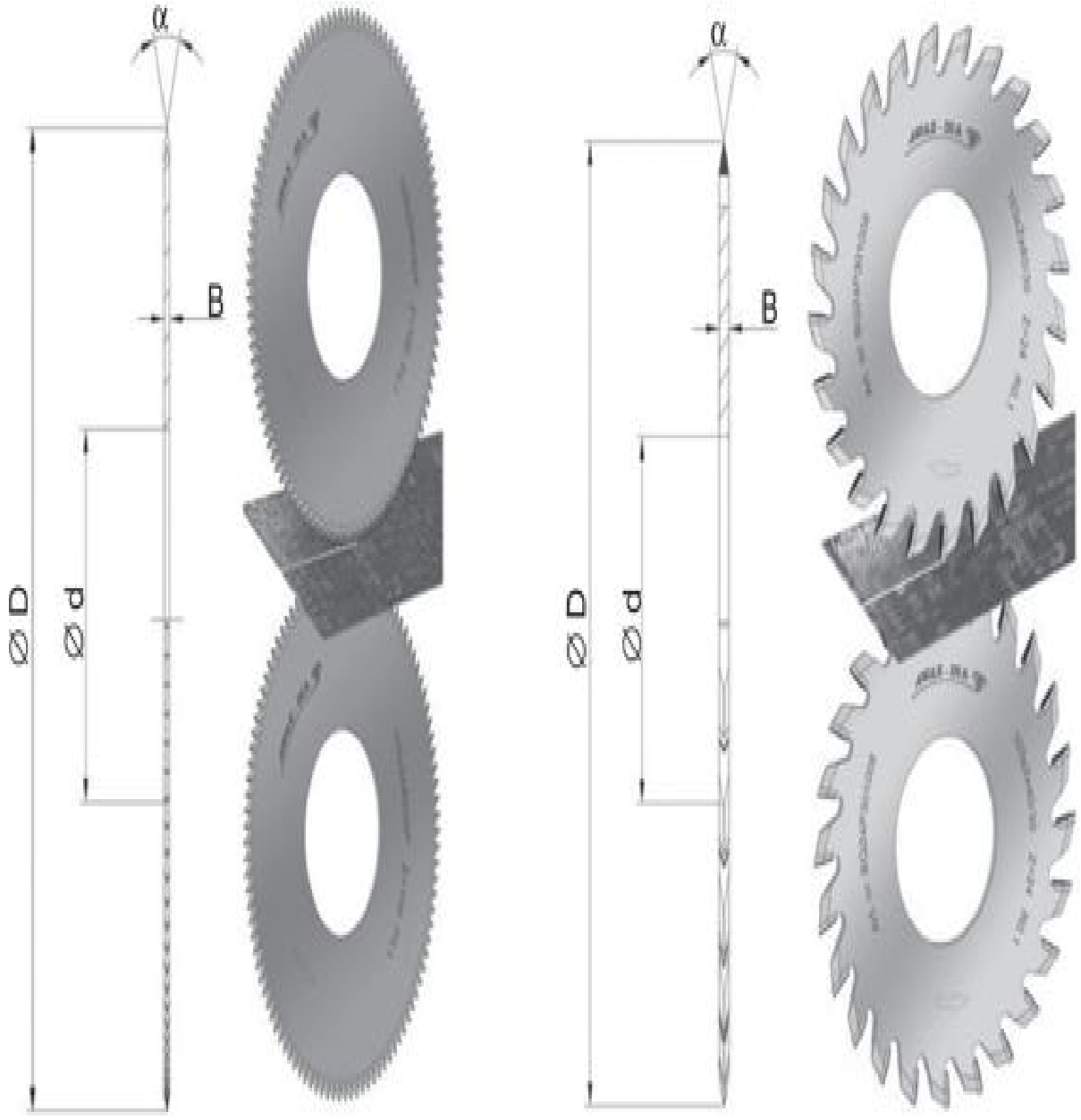

FIGURE 38.9 V-scoring with solid carbide blades (*left*) and PCD blades (*right*). (Pictures courtesy of Awax-Dia.)

To increase the tool life, defined by the distance in the material similar to conventional routing tools, is the tip intentionally removed to reduce wear and avoid fast breakage. For solid carbide tools is that achieved with a chamfer, whereas PCD-tools have a defined radius.

Blades can be repointed, similar to drill bits. However, it is the general wear during operation that needs to be monitored. As the main attribute in the production environment is the web or web thickness, the tool diameter which decreases with the wear, needs to be adjusted to keep the web constant. In this case is the cutting area of the blade penetrated deeper into the product increasing the width of the groove slightly.

The tool life or distance in the material, like in any mechanical subtractive machining operation, is dependent on the material and the cutting conditions. The number of revolutions of the blades is in ranges of 4000 to 8000 RPM. The relative motion of the cutting tools to the material is 20 to 40 m/min. With these settings can PCD tools achieve a distance in the material of up to 80,000 m but also be as low as 10,000 m for heavily filled base materials.

38.8.2 Alignment and Machine Types

There are different types of machines available, varying in the number of CNC axes and the type of alignment. The standard alignment in the v-scoring operation is a “pin-alignment” in which the position or location of the printed circuit board to the v-scoring machine is defined over two mechanically drilled holes in one axis of the board and a corresponding pair of pins in the machine. The PCB is then moved in a relative motion through the two cutting blades which are set in a defined distance resulting in the required web. An additional controlled axis is able to move the board to the location of the next groove. With that, all (parallel) grooves in one axis of the PCB can be generated. With another machine axis can the PCB be rotated 90° and all grooves in the other board axis can be

generated. The next higher level in automation also has a controlled *z* axis with which the distance of the tools (defining the web) can be set in the program. By moving the cutting tools so far apart that they leave the material, can interruptions of the grooves be generated. These technique or technology is also referred to as “jump scoring.”

Due to the increased requirements concerning the alignment of the grooves to the outer layer image can modern CNC v-scoring machines additionally be equipped with a camera system. This allows adjustments in the angle in which the score is generated and also in the positioning of the grooves to each other. After the camera measures metal features (fiducials) or holes in all four corners can the v-scoring pattern be stretched or shrunk to mitigate dimensional changes of the PCB. For the alignment to fiducials might multiple light sources be required as the different final surface finishes reflect the different wavelengths in a different way, giving alternatives for a good recognition of the fiducial enabling a perfect alignment.

38.8.3 Scoring

In a CNC scoring operation is the printed circuit board fed (manually or automated) into the v-scoring machine, after a program with the locations and depth of the grooves and if required the coordinates of the fiducials, is loaded and started. A first rough alignment of the PCB against a mechanical stop is followed by a clamping system which fixes the PCB and defines the location in relation to the machine. In case of “camera alignment” is the camera moved to detect the fiducials at predefined locations. Once the fiducials are detected, additional fine adjustments of the locations of the PCB can be performed. If necessary and defined in such way, is it also possible to stretch or shrink the distance of the v grooves to each other (based on the information gained during the measurement of the features) to compensate dimensional changes of the printed circuit board.

The two blades (one on the top side of the PCB one on the bottom side of the PCB) are accelerated to the defined cutting speed. A relative motion moves the blades across the PCB for the first groove. As the blades only move in one axis back and forth, is the PCB moved to the next groove location, so that the second groove is generated while the blades move back to their original location.

As the blades have cutting “teeth” for the material removal, are the cutting conditions similar to the conventional routing operation. If not defined differently, will one groove be generated in “conventional milling” and one in “climb milling” leading to different results concerning the edge quality of the groove. For critical applications can the direction of the movement of the blades be defined for each individual groove. It has to be considered that the choice of only one cutting direction will have a negative impact on the efficiency as the blade will need to be moved to the original position relative to the PCB after each groove. With that, material is only ablated in every pass.

38.8.4 Depaneling

The separation of the parts after the generation of the groove can either be done manually or with additional (cutting) tools. The parameters defining the force which is required for the manual separation are

1. The web or web thickness
2. The blade or scoring angle
3. The width of the separation partners

The angle and the width of the elements define the lever in which the separation can be done and with that another big element to the web, which defines the general force which is required to separate the elements.

Especially for the manual depanelization or singulation has to be considered that the parts turn out to be bigger than the inner edge of the material. This increase is caused by the broken web exposing glass fibers.

The separation can also be done with tools, in the simplest way a cutter knife looking like a pizza cutter. There are also depaneling machines available having blades, saws, round cutters or linear cutters on one or both sides (top and bottom) looking similar like the actual v-scoring machine. Common is also a single cutting blade (like a saw) with manual feeding of the pre-cut products. The grooves which are already in the product guide the operation and make an additional alignment obsolete.

Very effective can be to combine “routing” and “scoring” enabling complex structures and perfect edge quality (only) where needed and being cost effective and fast on the other areas (see Fig. 38.10).

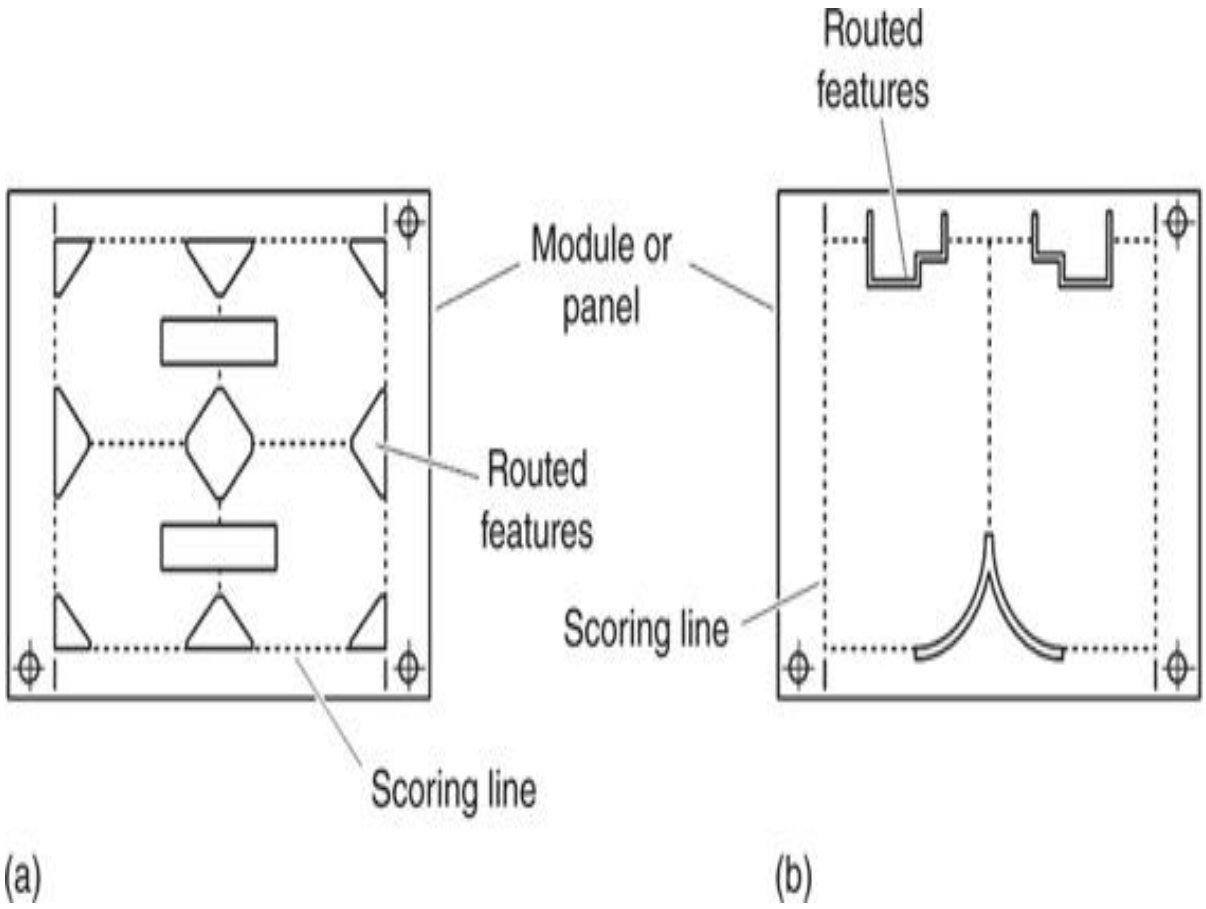

FIGURE 38.10 (*a*) Panel with typical scoring lines and routed corners; (*b*) scoring lines and routed complex features.[3]

38.8.5 Process Control

Controlling the v-scoring operation in a production environment can be manifold. Key elements are

- The edge quality of the groove, for proper parameters and tool life.
- The location of the groove, typically in relation to fiducials or other features on the board.
- The web or web thickness; this is a critical attribute especially if the separation is not done “in-house”. Measurements can either be done visually by looking at the

board edge or mechanically with a caliper gauge or combinations of the two.

- The outline dimensions after separation (visually or mechanically).

To reduce human errors in a manufacturing environment like skipping the entire v-scoring step or to double check the v-scoring machine itself for missing scoring lines, can small coupons in the shape of “I” or “U”-shaped copper traces with test points at both ends be added. These need to be cut once (I-shape) or at least once (U-shape) and can be included in the electrical test. In the example would the pass-criteria be an “open” and a fail-criteria be a “short” indicating that the entire process step or single lines were not performed and the copper traces in the coupon are not cut.

38.8.6 Trouble Shooting V-Scoring

The two main issues in the v-scoring operation are shown in Fig. 38.11. In this figure (1) shows a web which is off center, leading to a deeper and wider score on one side. Usually is the increased width the bigger problem, potentially violating a minimum distance to adjacent features. Root cause is a wrong thickness of the board or a mismatch of the actual or planned thickness. This thickness needs to be entered manually or is part of the NC program. On the other hand can a shape like that be achieved by purpose by entering a thickness deviating from the actual thickness.

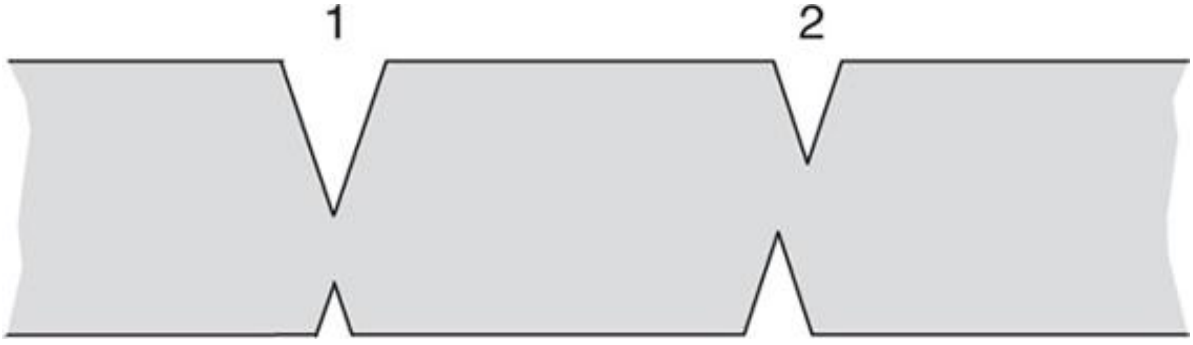

FIGURE 38.11 Issues around the v-scoring process; (1) web-off-center, (2) offset between top-and-bottom cutter tool.

Issue (2) shows an offset of the top cutter to the bottom cutter. Problems can occur in the separation process and the final edge quality. The offset needs to be adjusted in the machine as part of a process control.

38.9 REFERENCES

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PART 7

BARE BOARD TEST

CHAPTER 39

BARE BOARD TEST OBJECTIVES AND DEFINITIONS

David J. Wilkie

Everett Charles Technologies, Pomona, California

39.1 INTRODUCTION

Advances in packaging technology resulting in finer board geometry, including the various forms of high-density interconnection (HDI), have combined with increasing data rates to put significant pressure on the electrical test area. Fixture construction is more expensive and requires improved process control. Advanced test methods, such as radio frequency (RF) impedance testing, are more often required. Global price competition demands reduced costs. Meanwhile, original equipment manufacturers (OEMs) demand that board manufacturers accept increased liability for defective product—thereby demanding improved fault coverage. This chapter is devoted to the why, what, where, when, and how of current electrical test methods useful in meeting these requirements.

39.2 THE IMPACT OF HDI

Test engineers are currently confronting significant changes in test requirements that derive from changes in the product itself. Notable among these changes are those driven by the growth of various HDI technologies. Examples of common HDI applications are direct chip attach (DCA), high-density ball grid array (BGA), and variants of these often referred to as chip scale packaging (CSP). In addition, higher-density input/output (I/O) connectors are commonly applied. In addition to the changes in physical geometry, HDI also implies increasingly high data rates and clock speeds. Advanced means are being applied that verify not only the ability of the product to interconnect electronic components, but to do so in a manner that guarantees signal fidelity.

An analogy is possible comparing the impact of HDI on board technology with the impact of the sound barrier on aerodynamic flight. This analogy is readily applied to final electrical testing. It was popularly imagined that the sound barrier was impassible, or could be passed only by Buck Rogers in his silver rocket—that beyond the speed of sound was no place for an airplane to go. As it turned out, passing the sound barrier *was* difficult, and required rethinking many aerodynamic principles. But the resulting vehicles are still recognizable as aircraft. They have wings, they burn fuel. They meet all of the objectives of earlier craft, and do so in a superior manner. The test processes that are resulting from the impacts of HDI upon final electrical testing are similarly recognizable evolutions of previous methods, employing familiar base technologies, but in new combinations and with added features that actually improve test coverage rather than diminishing it.

Proposals have circulated for radical new measurement approaches to electrical testing. These have included the use of electron beams, laser-stimulated photoelectric

effects, and gas plasma techniques in configurations similar to existing flying probers. In each case, the board is scanned without use of a custom test fixture. To date, all of these methods involve compromise of fault coverage, or add little or no fine-pitch performance beyond conventional methods. Relaxation of test criteria is not a relief available to most users. HDI product types demand increased fine-pitch capability. These finer trace and via geometries increase the risk of latent defects and increase interest in measurement methods most sensitive to precursor symptoms of such defects. As a result, none of these approaches has seen widespread adoption.

Rather than witnessing radical breakthroughs, the market has seen a steady improvement in the availability of software and hardware tools that provide for the effective combination of the best features of conventional test systems and increased availability of test systems dedicated to specialty markets, in particular the small-format laminated chip carrier product type.

39.3 WHY TEST?

Why pay for testing? Why do we need to test? The answer has several components. The primary assumption is that not all boards produced are good. If we could look at the yields through the history of the industry in printed wiring boards using similar technology, we would see exponential reductions in the percentage of bad boards produced. Process improvements and a wide variety of quality improvement programs continue to make a difference. In spite of these improvements, the need for electrical testing remains.

39.3.1 The Rule of 10s

One reason to test is to block the addition of further value to defective product. Consider the printed wiring board as a component of a completed assembly. A commonly accepted relative measure of the cost of faults in a completed electronic assembly can be expressed by the rule of 10s (see Fig. 39.1). The idea is that the earlier a fault is caught, the less it will cost. An example might be an open in a bare board that is not found at bare board test. The faulty bare board is now loaded with the components, soldered, and tested. If the fault is found at the loaded board level, repair or scrapping of the assembled board is much more expensive than repair or scrapping at the bare board level. There are situations where the assembler of the board charges back to the manufacturer of the bare board some portion of the cost of the scrapped components, assembly labor, and/or production cost. This is increasingly true with the high-cost and high-capability integrated circuits (ICs) present in so many designs. A fault that passes a system-level test and makes it to the end user entails even higher cost. Some of these costs are very tangible in the form of field service labor, downtime, parts, and labor. Other costs are counted in lost business and reputation.

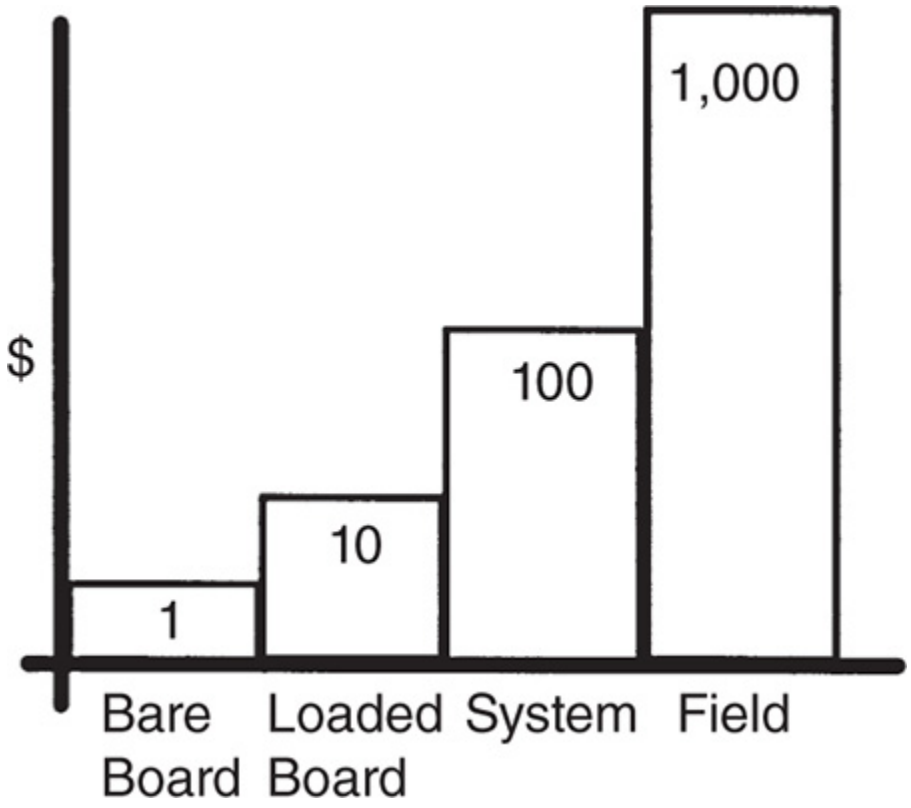


FIGURE 39.1 Rule of 10s: cost of a found fault.

39.3.2 Satisfying Customer Requirements

Where the rule of 10s is a logical big-picture approach to the necessity of testing, requirement from a customer is quite the opposite. The board user has already determined that electrical testing is appropriate and necessary and has made it a requirement as part of supplying the board. It is the obligation and responsibility of the bare board manufacturer to meet this requirement of purchase contracts. In practice, we find such customer requirements stated in various ways.

39.3.2.1 Generic or 100 Percent Board Test. Unfortunately, this requirement may be nothing more than the words “100 percent electrical test” appearing

somewhere in a purchase order or a larger package of documentation. Not only is such a specification relatively meaningless, but the issuer of such a requirement is led to believe that the boards will be tested to the most stringent requirements—that it will not be possible for a single bad board to be delivered. Nothing could be further from the truth. Such a specification fails to define what a 100 percent test consists of. The purchaser of the bare board will certainly be dissatisfied when he or she receives a bad board. Although the specific fault on the bare board in question may have a perfectly viable explanation (might not be detected electrically, or may be undetectable by the specific methods employed), the 100 percent test specification implies that no explanation is acceptable. In many cases, application of this general sort of specification is combined with a customer-imposed limitation on test cost, which in turn requires cost-driven limits on the thoroughness of electrical testing performed by the board manufacturer.

39.3.2.2 Written Test Specification. It is the responsibility of both the bare board manufacturer and the bare board purchaser to agree upon a test specification that is specific in terms of test thresholds and method of testing while keeping in mind the appropriateness to the application for the bare board design. Some limits on test thresholds and test methodology may be due to equipment and capabilities of the manufacturer. It is the responsibility of the bare board manufacturer to educate the end user as to the implications of test specifications in thoroughness and cost of testing. A matrix of test options, fault detection capabilities, escape risks, and associated costs should be presented to the end user. It is the responsibility of the end user to work with the bare board manufacturer to develop specifications appropriate to the bare board being produced and to accept and plan for any testing compromises

imposed by cost or specification limits. Areas that should be covered in the specification are:

- Data-driven testing, source of data, format, and integrity
- Test thresholds: maximum allowable for continuity verification
- Test thresholds: minimum allowable threshold and applied voltage for isolation verification
- Test fixture methods: single fixture with simultaneous access of all test points versus split-net fixtures versus flying probe
- Test point optimization
- Board marking indicating electrical test satisfaction
- Resolution of discrepancies in process (contacts and procedures)
- Requirements for special test methods (time domain reflectometry [TDR], embedded passives, etc.)
- Resolution of escapes

Such agreements make for good communication, clear understanding, happy customers, good reputation, and good business.

39.3.2.3 Using Available Standards. Industry standards or guideline documents such as IPC-9252, “Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards” (which replaces IPC-ET-652), are useful in developing agreed-upon written specifications for a particular product.

Standards documents must be applied in consideration of the target application. An excessively rigorous specification would result in unacceptable test cost with little quality improvement.

Arbitrarily high isolation voltages or continuity test currents can actually lead to product damage. Conversely,

relaxing isolation resistance specifications on boards containing sensitive amplifiers would be inappropriate. These are but a few examples. In IPC-9252, the IPC has made efforts to distinguish between general classes of board applications, suggesting specific electrical test requirements that attempt to recognize different levels of criticality in testing.

Final determination of the suitability of a given set of requirements must be made in cooperation with technical representatives of the bare board purchaser.

39.3.3 Electrical Testing as a Process Monitor

A third benefit of testing is the improvement of processes and the resultant reduction in costs. To raise yields, reduce scrap, or generally improve quality, there must be a system of measurements able to express results of changes. One of the best areas to collect data is electrical testing. This usually requires an integration of testing and repair data. While the test system can identify a bad board and the location of a fault, a repair operator can further classify the fault to associate it with a specific process (imaging, plating, etching, solder masking, etc.).

These data can be quantified and analyzed in a variety of ways, and corrective action may then be directed to one or more of the following levels.

39.3.3.1 Faults Specific to the Operation. Fault types may be detected that are not typical of the industry or competition. It can be difficult to assess this type of situation accurately because data commonly available from the customer, alternative vendor, or competitor are likely to be narrow or biased. It may be better to analyze fault types

specific to an operation in terms of cost or profitability. Are certain product types profitable to manufacture? What would be the cost to make them profitable?

39.3.3.2 Faults Specific to the Process. An analysis of fault data may lead to a specific process that regularly induces faults in a wide variety of part numbers, or in a variety of part numbers sharing key characteristics. This may point to requirements for new settings, procedures, materials, training, personnel, equipment, etc.

39.3.3.3 Faults Specific to a Part Number. Fault data on a specific part number are useful in correcting and optimizing processes for future runs of the same part number, and often for similar future part numbers. It may be possible to feed back electrical test data in real time using software systems, depending upon lot size, factory flow, and the type of test and repair analysis equipment available for use. In this situation, results from electrical testing may help drive some adjustments or quick changes in the process that will immediately improve the yield and reduce scrapping, repair, and retesting costs.

39.3.4 Quality System Improvement

Quality control analysis of fault data is only a piece of what needs to be in place already, that is, a quality control system or process. The value of electrical test (or other process) data for process monitoring is only as great as the quality control framework making use of it. It is possible for electrical test results to become a vehicle for improvements to a board manufacturer’s quality system.

39.4 CIRCUIT BOARD FAULTS

For electrical test purposes, faults may be defined as test system measurement results other than those programmed to be representative of a good board. The faults detected may or may not impact the functionality of the circuit board, though in most cases they will. Some guidelines may prove useful when more specific guidance from the original specifier or designer is lacking. Obviously, gross shorts and opens in a circuit are likely to cause problems. Will an electrical test system find all the faults? No. The definition of “all the faults” is too subjective.

The electrical test system will not detect all faults related to aesthetics, annular rings, layer-to-layer registration, etc., unless they present an effect measurable by the test system. Further, the electrical measurement employed, type of test fixture, test program generation method, and end-use requirements vary too widely to state broadly that electrical testing will find all the faults.

For purposes of the following discussion, it is worthwhile to clarify the distinction between a defect and a fault. A fault is a test system designation for an item that does not meet the expected criteria. A defect refers specifically to the board and a defect in its design, fabrication, appearance, etc. Not all defects can be detected by the test system.

39.4.1 Fault Types

Table 39.1 presents common fault types. For those fault types that are commonly detected, it is valuable to distinguish types of tests from types of faults. It may be preferable to refer to isolation testing or continuity testing rather than to shorts or opens testing, as the latter meaning is often confused Shorts and opens are results, not test types. Test methods themselves are discussed in detail elsewhere in this chapter.

TABLE 39.1 Test and Fault Types

Test type	Fault type identified by test
Continuity	Open
Isolation	Short and/or leakage
TDR or network analysis	RF impedance fault
Hi-pot	Voltage breakdown

39.4.1.1 Shorts. Shorts, hard shorts, or short circuits are defined here as erroneous (undesired and unexpected) low-resistance connections between two or more networks or isolated points, typically exhibiting a fairly low electrical resistance value. Shorts are reported as failures of the isolation test of the product. Shorts are produced in a variety of ways, including exposure problems, underetching, contaminated phototools, poor alignment of layers, defective raw material, and improper solder leveling.

39.4.1.2 Opens. Opens represent an absence of expected circuit continuity, or in other words, a missing connection. This divides a circuit network such that the network is split or divided into two or more pieces. Opens are reported as failures of the continuity testing of the product. Opens are produced in a variety of ways, including overetching, underplating, contaminated phototools, contaminated raw material, layer registration errors, and mechanical damage. A common problem during electrical testing is “false open” errors, typically the result of localized contamination on the product or test probe that prevents proper connection to the test system. Of particular concern in testing substrates employing microvias are latent defects

(those which may appear after test during subsequent substrate assembly processing). Examples are improperly formed conductors at stress points where cracks may form during thermal or mechanical stresses of assembly. Small HDI features are less tolerant of such defects. These may be completely undetectable at the time of test, or limited examples may be detected by especially sensitive ohmic measurements able to detect a limited conductor cross section where a future open circuit may occur. Frequent observation of such defects indicates the need for process changes if field failures are to be avoided.

39.4.1.3 Leakage. A leak or “leaking network” is essentially a type of short. Leaks are also referred to as high-resistance shorts, and differ from hard shorts in that they exhibit a higher resistance value. The precise division between the two types of error reports varies according to the type of equipment used, and some equipment does not attempt to distinguish them in fault reports. As in the case of hard shorts, leakage is a failure of the isolation testing of the product.

Common leakage causes are moisture, chemicals, or debris. Contamination can occur during innerlayer fabrication, lamination, plating, solder masking, or any stage due to handling. Chemical contaminants are often deposits of metal salts left as artifacts of the chemical processes used to manufacture the product. With sensitive test methods, even fingerprints can result in detectable leakage between networks. Such contaminants are often spread over an area of the board such that several networks become interconnected. Consideration of the potential for multiple network involvement is useful in selecting the particular isolation test algorithm or test method, as these methods differ in their sensitivity to this situation. Isolation test methods are discussed elsewhere in the chapter. Some circuits are not sensitive to the high-resistance loads

immediately presented by such contaminants. But it is important to note that, in the presence of time, electric fields, and moisture, it is possible for the resistance of a high-impedance short to decrease greatly. Contamination sites may facilitate the growth of metallic crystals that reach out as thin metal threads between networks, forming hard shorts.

Thus an area of the product exhibiting unusual leakage may, at some future time, exhibit hard shorts between networks. This amplifies the need for effective high-impedance testing of high-reliability product types as a means of preventing latent field failures. Note that the nature of board materials is such that they can absorb moisture relatively easily, and they do so over time. Thus even a fairly “dry” contamination providing a very weak electrical path may eventually result in sufficient metal migration during product operation to cause a serious field failure.

39.4.1.4 RF Impedance Fault. Many circuits produced today are required to operate at very wide bandwidths. Examples include fast microprocessors, fast general digital circuits, RF amplifiers in wireless devices, etc. Just as we must use a proper type of cable to connect a television antenna to a TV receiver, it is important for specific RF characteristics to be maintained in interconnections between components of fast electronic circuits on printed wiring boards. One parameter commonly specified and measured is the RF transmission line impedance of the signal traces. This parameter is strongly affected by the materials used in fabricating the board, the trace thickness and width, and the spacing from ground planes and adjacent signals. A common method of measuring RF impedance is to employ TDR.

The TDR measurement provides a statement of RF impedance as a function of distance along the trace.

(Distance and time are related here, as the electric signal flows through the board at velocities approaching the speed of light.) TDR testing is often performed on a test coupon attached to the product during manufacture and subsequently disconnected. TDR testing on actual product traces is also done on selected traces, but is complicated by the need for a trace length of several inches, uninterrupted by branches or other constructions. Common values for RF impedance on circuit boards range from the low tens of ohms to several hundred ohms.

RF impedance should not be confused with ordinary direct current (DC) resistance and cannot be measured with common ohmmeters, even though the same unit of measure—the ohm—is used.

RF parameters of interconnections can also be characterized in the frequency domain using instruments referred to as network analyzers, but this method is not common in bare board testing. Requirements for RF impedance testing are more commonly applied as signal frequencies exceed 100 MHz.

39.4.1.5 Hi-Pot Faults. Hi-pot or high–potential voltage breakdown testing is often confused with isolation testing. The tests are very similar, and, to the extent that high voltage is employed in an isolation test, they might achieve a similar result. But isolation testing of bare boards commonly occurs with 250 volts or less applied between networks, and hi-pot testing is often performed at values from 500 volts to several kilovolts. Hi-pot testing attempts to verify the strength of the insulating material between networks by subjecting it to so high a voltage that a catastrophic or avalanche-type voltage breakdown will occur if the insulator is subpar. In contrast, isolation testing on bare boards attempts to detect the small current flowing through contamination (or, for that matter, a hard short) before voltage breakdown occurs. Of course, if the insulator

is very weak, then avalanche failures can occur at almost any voltage. Hi-pot testers tend to be benchtop devices with a pair of test leads and no switch matrix, and hi-pot test requirements usually specify that the voltage be applied for a sustained period of time.

Hi-pot testing is valuable for inspection of very thin insulating core material, before circuits are etched. This can serve to detect z-axis faults or contamination in the material before value is added in subsequent processes. It can be impractical to perform hi-pot tests between all conductors of finished fine-pitch boards, as the atmospheric environment (air) between conductors will break down before high voltage is reached. The slow speed at very-high-voltage hi-pot testing and the costs of suitable fixtures and electronics present problems. For final product inspection, it is arguable that a very-high-impedance isolation test provides the superior solution.

CHAPTER 40
BARE BOARD TEST METHODS

David J. Wilkie
Everett Charles Technologies, Pomona, California

40.1 INTRODUCTION

Although the main bare board testing technology is electrical, it is important to consider that nonelectrical methods are also important in the acceptance or rejection of bare printed wiring boards (PWBs). This chapter therefore includes detailed descriptions of both electrical and nonelectrical testing methods.

40.2 NONELECTRICAL TESTING METHODS

There are two nonelectrical acceptance/rejection methods, both based on inspection processes:

- Visual inspection

- Automatic optical inspection

40.2.1 Visual Inspection

Visual inspection is a very manual approach in that it makes use of people, good lighting, some type of training defining what is acceptable and what is not, and good operator judgment.

Usually a comparison to a known good product or the artwork is made. If the operator has seen the board often, he or she becomes more skilled at finding faults and looking for faults in likely locations. As product complexity has increased, we find that many modern products are not suited to this method. Many innerlayer defects are completely undetectable, and even the external layer complexity is visually overwhelming. Visual inspection often remains appropriate for detecting cosmetic defects, such as poor solder masking or physical damage. Such defects generally fall outside the realm of electrical testing as they are not detected by electrical means.

40.2.2 Automatic Optical Inspection

There are computer-based visual inspection methods, referred to as automatic optical inspection (AOI). AOI equipment compares the board or its innerlayers to expected data and/or design rules that have been programmed into the controlling computer. These can be generally accepted parameters or design-rule-based parameters, or windows of acceptable dimensions for each specific feature on the board. As with manual visual inspection, faults found with this method can imply that there may be an impact on the board’s functionality, but the board’s functionality and interconnect are not directly tested. Distinctions between the

aesthetics of the board's features and its fitness for use are difficult to differentiate, and may result in false failures. Rather than being used in final testing, AOI is used for inspection of innerlayers prior to lamination, with the goal of increasing final yield by weeding out the majority of defective layers prior to the addition of further value. As such, AOI can achieve significant financial benefit. AOI can detect some defect types not readily detected by electrical means, particularly "mouse bites" (brief narrowing of the conductor cross section). AOI may also be used to inspect the outside layers after lamination, but is not generally accepted as a quality assurance substitute for final electrical testing.

40.3 BASIC ELECTRICAL TESTING METHODS

Electrical testing is the final test method frequently used to determine whether a board should be shipped. Electrical testing emulates the intended function of the board conductor and insulator patterns by passing currents through conductors and applying voltages across insulators. Such direct electrical measurement requires that the board come into physical contact with a measurement system. Two test types are almost universally performed: continuity and isolation testing. Some other tests may be applied selectively, depending upon the product and customer requirements.

Test order is usually such that the continuity test is performed first. This verifies that each network is intact within itself, and that contact is established between any test fixture and the product. The isolation test can then be performed using only a single test point per network. Some test methods attempt indirect inference of continuity and

isolation without making direct current (DC) measurements. These methods are commonly employed in flying probe systems.

40.3.1 DC Continuity Test Method

Continuity testing checks for the expected continuous path within each electrical network. This is done in a series of point-to-point measurements within each network. The resistance found in each measurement is compared to the selected continuity resistance threshold. If the measured value is higher than this threshold, then a fault report is generated. For complex networks, multiple measurements are required in order to ensure that all extremities of the network are interconnected. For example, the network with test points labeled A through D, shown in Fig. 40.1, could be tested in the sequence illustrated in Fig. 40.2. For a network with four test points, the minimum number of tests would be three to determine whether all points are connected. If a board contains a total of N isolated networks, and contains a total of X test points, we may calculate the number of continuity measurements C as $C = X - N$. In assigning test points, the software system often is programmed to delete those that are unnecessary. This is referred to as test point optimization. In Fig. 40.1, a test point located along the path between D and the branch to C would not be useful. Various optimization rules may be applied, but should be applied with care to ensure that adequate test coverage remains in place.

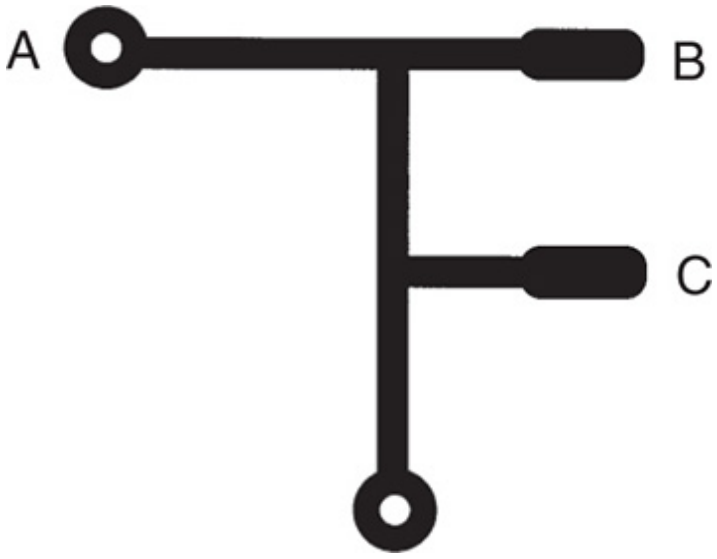


FIGURE 40.1 Sample network.

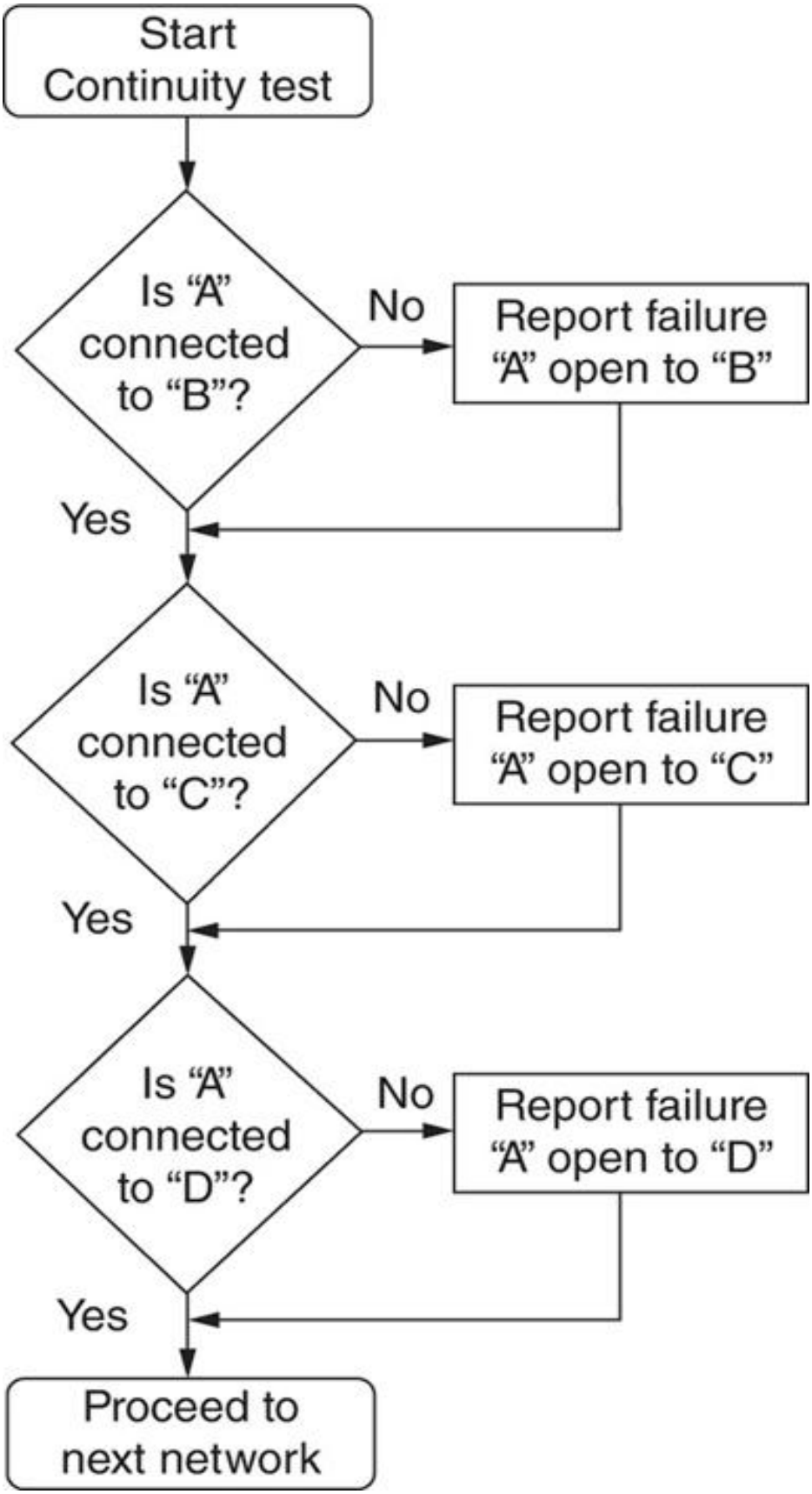

Start
Continuity test
Is "A"
connected
to "B"?
No
Report failure
"A" open to "B"
Yes
Is "A"
connected
to "C"?
No
Report failure
"A" open to "C"
Yes
Is "A"
connected
to "D"?
No
Report failure
"A" open to "D"
Yes
Proceed to
next network

FIGURE 40.2 Continuity test algorithm.

40.3.1.1 Continuity Test: Two-Wire versus Four-Wire Switching. Switch matrixes are constructed using either two-wire or four-wire circuits. A diagram comparing a single continuity measurement being performed on both two-wire and four-wire matrixes is shown in Fig. 40.3.

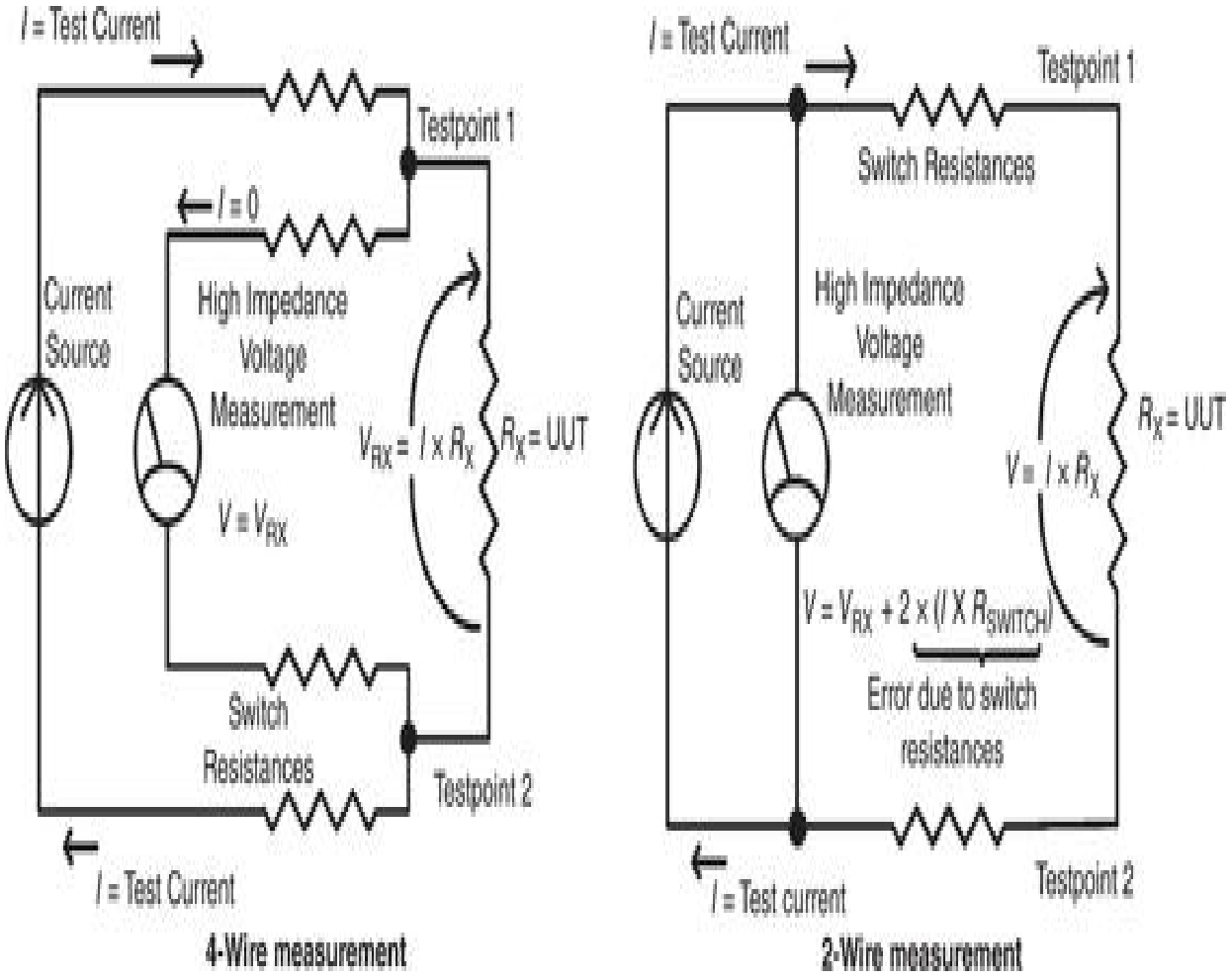


FIGURE 40.3 Continuity measurement circuits.

Grid test systems use solid-state switches to connect appropriate test points to an internal measurement system (which is effectively an ohmmeter). Current *I* is driven from the upper test point through the product network and returned to the measurement system through the lower test

point. The resultant voltage V across the network is measured. The continuity resistance R is then determined using the relationship $R = V/I$.

40.3.1.2 Two-Wire Switch Matrix Construction. The simplest, most affordable, and most common construction of the switch matrix is to have a pair of switches for each test point that can connect the test point to either the high side or low side of the ohmmeter. This technique is illustrated on the right side of Fig. 40.3. However, as the solid-state switches exhibit a certain amount of on-resistance, they contribute error to the measurement. The resistance of the switches is added to the resistance we measure, increasing the likelihood of failing the test. These errors can be reduced in various ways:

- Use switches with low on-state resistance (and thus a small amount of variation in on-resistance). This means using physically larger transistor dies. Such devices are not expensive, but are harder to integrate into integrated circuits. Thus, most two-wire designs rely upon discrete output transistors as switch elements.
- Use software to subtract the estimated typical on-resistance. As switch resistance effects vary from device to device, and change with temperature, some error remains.
- Make multiple measurements for each continuity to be inspected, and mathematically subtract most of the switch resistance. However, this slows the measurement process somewhat by requiring extra measurements and requires high-quality fixture construction such that contact resistances do not vary during the required multimeasurement sequence.
- Attempt to learn the resistance of each switch. Some systems require the operator to install a shorting plate over all test points, and the system then learns the sum of the switch resistances plus contact resistances to this

plate. Note that this technique can actually add error if a high contact resistance value is learned for a particular test point, perhaps due to dirt on a probe. The excessive resistance value learned is subtracted from all subsequent measurements made with that probe, masking some high product resistances. The net result is a slightly increased possibility of passing a board that should be failed.

40.3.1.3 Four-Wire Switch Matrix Construction. The left side of Fig. 40.3 represents a Kelvin or four-wire switch matrix construction. Notice that each test point will require four switches, so that any test point can be connected to the high-side current drive, high-side voltage sensor, low-side voltage sensor, or low-side current return via separate paths. Because the voltage-sensing portion of the measurement system has an extremely high input resistance, almost zero current flows through the extra pair of switches that connect the test points to this circuit. The result is that there is zero voltage drop across these sense switches, and the measurement unit sees exactly the voltage across the unknown load. Because the measurement system knows exactly the current flowing through the load, and exactly the voltage across it, it can calculate the load resistance accurately. The dominant error term in this situation is generally the contact resistances in the fixture and fixture-product interface. Also, the smaller transistors leak less current in the off state, thereby permitting isolation testing at higher thresholds with smaller errors. The continuity accuracy benefit of this technique is realized only if high-quality fixtures with low contact resistance are employed.

40.3.1.4 Continuity Threshold. The continuity resistance threshold parameter is usually specified in the range from a few ohms to 1,000. Several standards useful in suggesting continuity thresholds are summarized in Table 40.1. IPC-9252 has actually weakened the recommendations

of IPC-ET-652, which it replaces. As discussed earlier in the chapter, these must be applied with judgment. Generally, a lower continuity threshold provides a more stringent test of the board. Networks with resistances of 5, 10, or 25, although rare when using copper traces of moderate length, can significantly impact the functionality of precision measurement instruments or high-speed computer products. At the same time, it should be noted that there are practical and economic considerations in determining how low the continuity test threshold should be set. Part of the limitation comes from the test system's measurement and switch matrix capabilities and, to a greater part, from the type of test fixture used. At the time of this publication, a 10- continuity resistance test threshold is a common lower limit for production testing with good-quality systems and fixtures.

TABLE 40.1 Examples of Continuity Resistance Test Threshold Standards

IPC Board Class	IPC-9252	IPC-ET-652 (obsolete)	MIL-55110D (obsolete)
Class 1: General Electronic	< 50–100 Ohms	< 50 Ohms	< 10 Ohms
Class 2: Dedicated Service	< 50 Ohms	< 20 Ohms	< 10 Ohms
Class 3: High Reliability	< 50 Ohms	< 20 Ohms	< 10 Ohms

40.3.1.5 Continuity Test Current. Continuity test current is not addressed in IPC-9252 or in most other publications. Use of high current has been proposed as a means of burning out weak traces or mouse bites. But such currents may also damage good traces. If this occurs after the test system has already determined that there is a good connection, the result is a board that once tested as good but is now bad. It is preferred that the continuity test not be

invasive or destructive. Typical test currents today are in the range of 5 to 50 mA.

40.3.1.6 Continuity Test False Opens. A common problem with continuity testing is a high incidence of false failures due to fixture and product contamination, poor product registration, or fixture damage. Dramatic improvement is often possible with the addition of product and fixture cleaning methods. Separation of the board-testing environment from such dust-producing processes as drilling/routing can be invaluable in increasing throughput. High-voltage pulses are sometimes used to overcome thin-film contaminants or oxides coating the surface of the board and preventing good contact with the test probe. As no current is initially flowing through the oxide, some test systems offer a feature delivering a high-voltage pulse of strictly limited current and duration, and therefore limited total energy. While brief, the energy level is higher than for a normal continuity test and a small risk of damage at defect sites remains. Adding test time for automatic or manual retesting of the product yields additional boards, but this common approach becomes expensive when large numbers of false opens occur. It may be advisable to correct the root cause.

40.3.2 DC Isolation Test Method

Isolation testing verifies the presence of adequate electrical isolation between networks that are not intended to be connected to one another. Typically a resistance measurement is made from a given network to another net (or group of nets). If the measured value exceeds the specified isolation resistance threshold while the specified voltage is applied, then the measurement is considered to have passed. Otherwise, a fault report is generated. So long

as contact with the net has been ensured (during the continuity test), only a single test point per network is required to perform the isolation test. The actual number of isolation measurements required to test a given board can vary substantially with details of the algorithm employed, with subtle impacts upon fault coverage. These issues are discussed in a separate section.

40.3.2.1 Isolation Resistance and Voltage. As isolation testing is a means of evaluating the ability of product insulation to withstand voltage and prevent current flow, it is common for the isolation test specification to include not only a statement of minimum resistance, but also an applied voltage. This is the voltage that the insulator must withstand while exhibiting at least the minimum isolation resistance. Given the relationship $R = E/I$, increasing the applied voltage is also a means of increasing the measurement current level up out of the noise floor internal to the test system. Thus, high-voltage-capable bare board test systems usually are able to verify isolation at higher resistance levels and do so at reasonable speed. Typical values for isolation resistance can range widely, from as little as 1 k. to as much as 1000 M.Values of 2 to 10 M are common, but higher values are useful in detecting trace contamination. Excessive humidity in the test area may preclude the use of very high thresholds and may affect accuracy at lower thresholds. Values below 50 to 55 percent relative humidity are desirable. Common isolation test standards (see Table 40.2) have not always kept pace with the capabilities of new equipment to test at elevated and sensitive thresholds. In any event, assignment of specific test thresholds would ideally be based upon a competent analysis of the intended application of the specific circuits on the product to be tested.

TABLE 40.2 Examples of Isolation Resistance Test Threshold Standards

IPC Board Class	IPC-9252	IPC-ET-652 (obsolete)	MIL-55110D (obsolete)
Class 1: General Electronic	> 500 K Ohms	> 500K Ohms	> 2 M Ohms
Class 2: Dedicated Service	> 2 M Ohms	> 2 M Ohms	> 2 M Ohms
Class 3: High Reliability	> 10 M Ohms	> 2 M Ohms	> 2 M Ohms

There is somewhat less emphasis on test voltage than was true previously, probably as a result of increasingly fine geometry in the product. Older or simpler test systems may be limited to 10 to 40 volts, but most are able to apply 100 to 250 volts during the isolation test. A higher voltage increases the test current, providing a better signal-to-noise ratio and generally improving test speed at higher isolation thresholds. Excessive voltage is inappropriate for very fine-pitch substrates and may result in damage from arcing in normal environments (see Table 40.3). The insulating properties typical of modern board material suggest that it may be of little value in specifying elevated voltages while using low (relaxed) threshold resistances. Raise the resistance threshold first, then use enough voltage to get adequate speed and accuracy.

TABLE 40.3 Examples of Isolation Test Voltage Standards

	IPC-9252	IPC-ET-652 (obsolete)	MIL-55110D (obsolete)
Minimum isolation test voltage	High enough to provide sufficient current, but avoid arcover	High enough to provide sufficient current, but avoid arcover	All least 40 volts, or twice the rated voltage of the board, whichever is greater

40.3.2.2 True Isolation Test Method. Several different algorithms have been developed for sequencing the switching state during the isolation test, and the choice may affect test coverage. In the most rigorous method, each network is individually tested to determine the total parallel leakage resistance to all other networks on the product. This requires one measurement per network, as illustrated in Fig. 40.4 for a board with three networks. Each network is, in turn, given a chance to charge to an elevated voltage. All other networks are connected together and to 0 volts at this same moment. Notice that only one test point is needed per network.

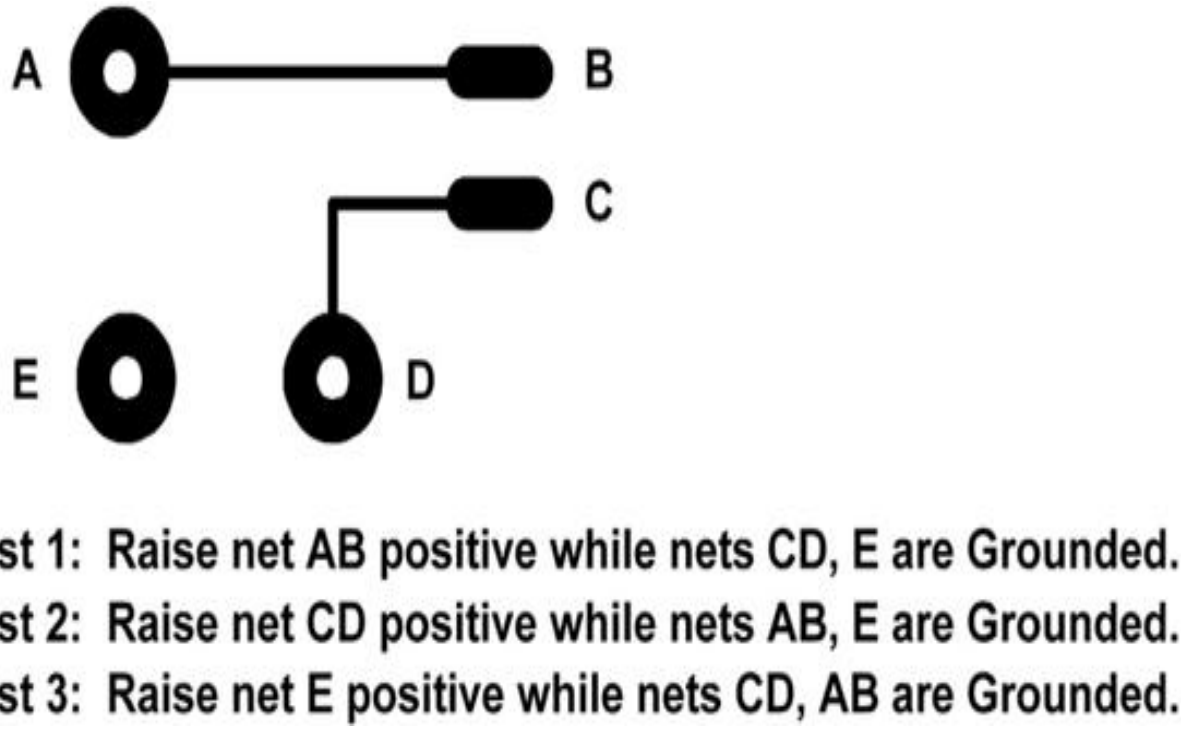
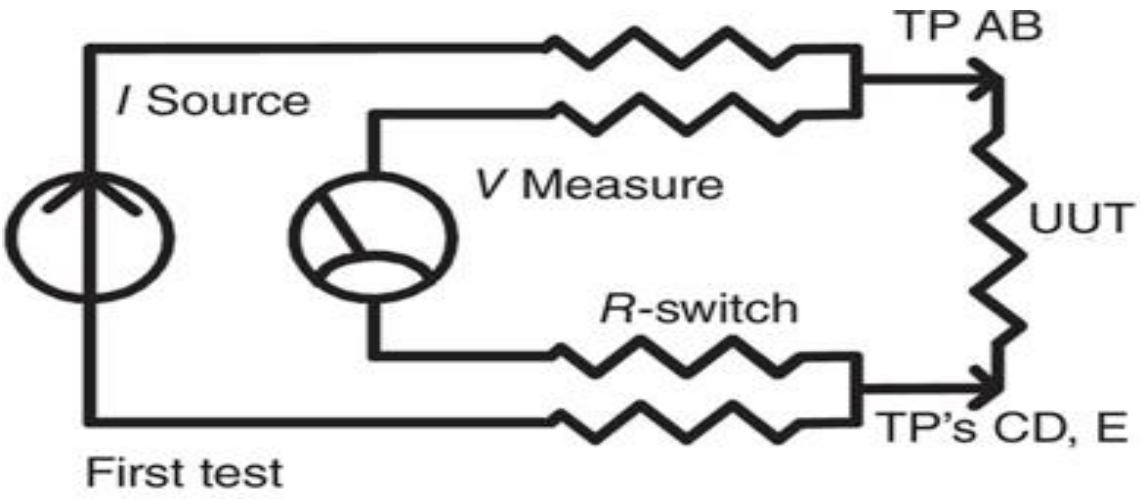


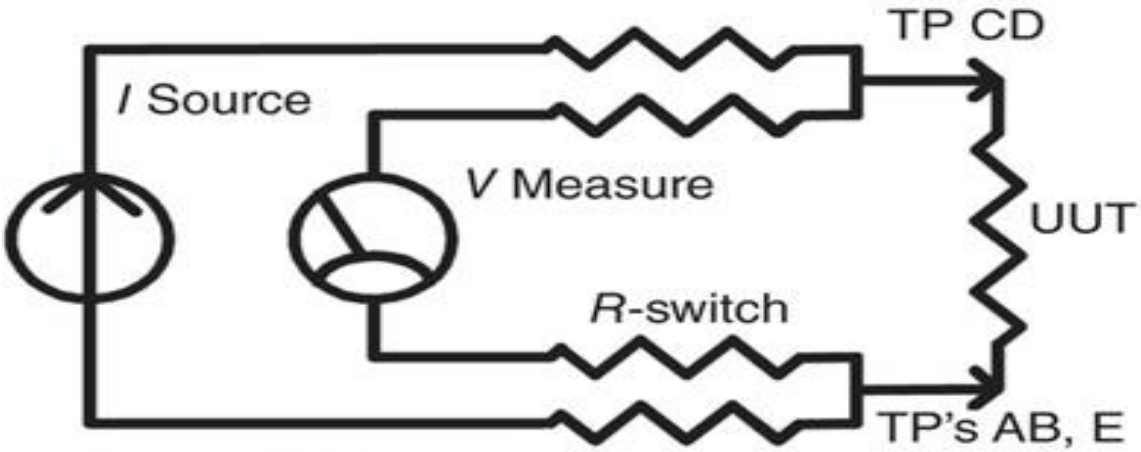
FIGURE 40.4 True isolation test of three-network board.

If the network under test is shorted or leaking to any of the other networks, or to any combination of them, it will fail to charge adequately and the test will fail. The pattern continues until each network has been tested.

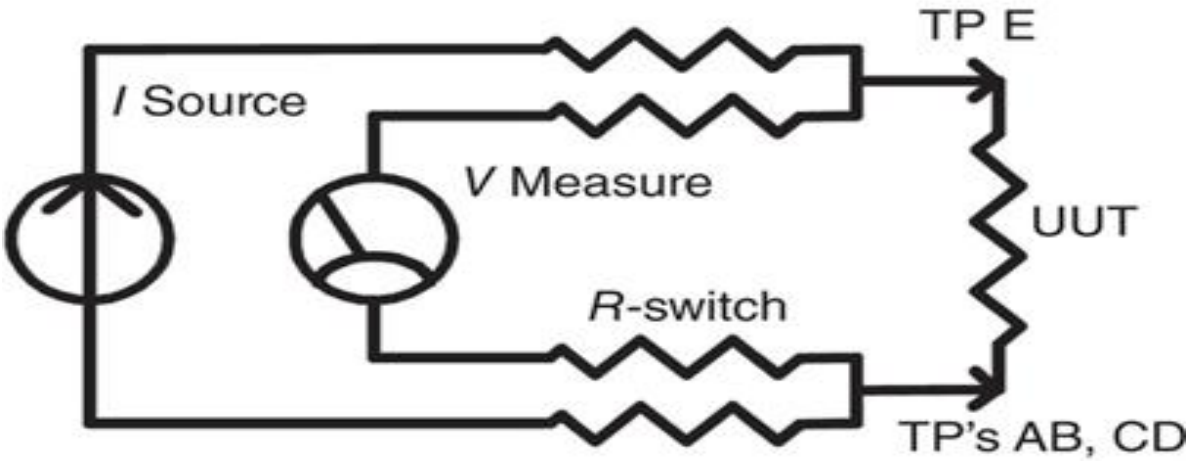
Figure 40.5 illustrates the status of the measurement system during the three tests. Notice that test points A and C are used to access their respective networks, and that test points B and D are not needed for the isolation test. These test point switches remain open through all measurements.



First test



Second test



Third test

FIGURE 40.5 Measurement sequence for three isolations.

A key feature of this method is the ability to answer the rigorous question: “How well isolated is this network from the rest of the board?” Consider the example illustrated in Fig. 40.6.

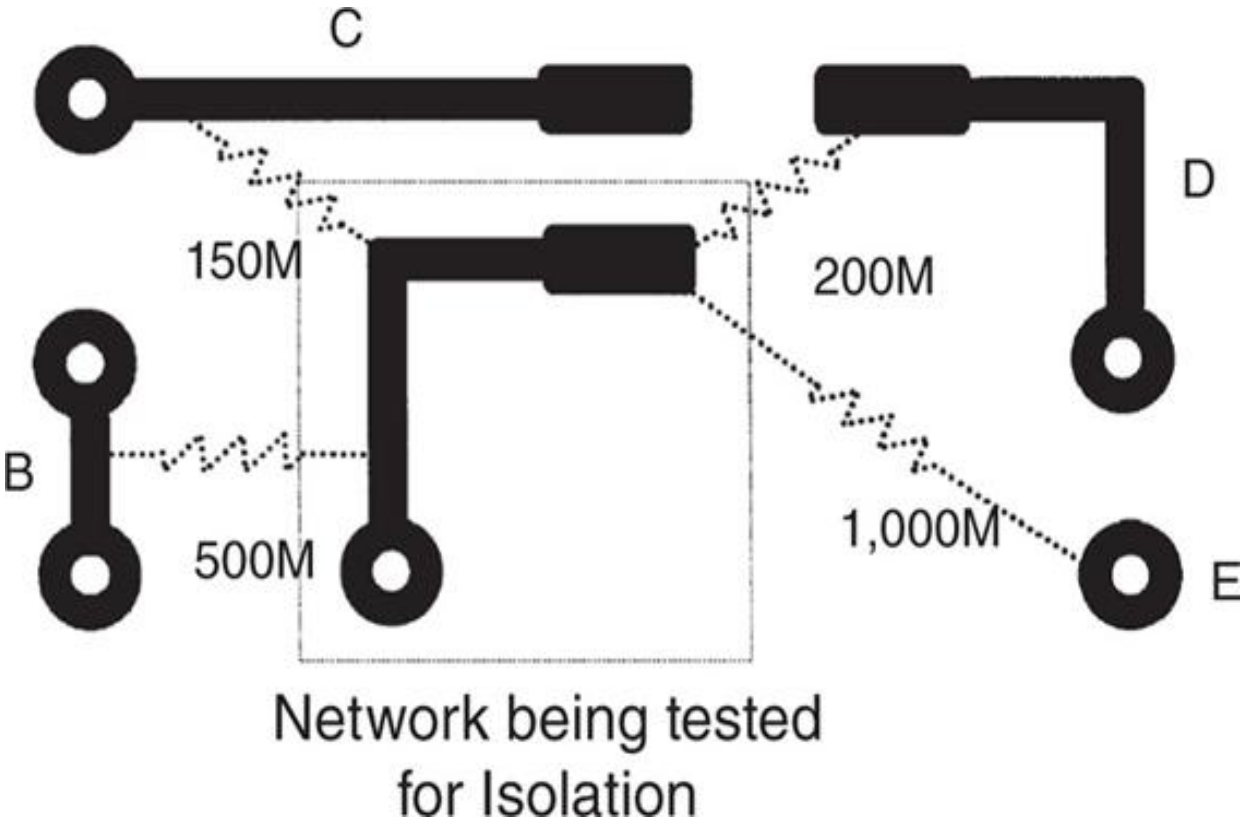


FIGURE 40.6 Parallel leakage detection.

Here the isolation threshold is 100 M. Four leakage paths exit network A, one each to networks B, C, D, and E. Each path, measured separately, is well above the 100-M. pass/fail threshold. But electrically we can only guarantee that network A is isolated by the parallel combination of these four resistances, given by:

$$RA = \frac{1}{(1/R_{AB})+(1/R_{AC})+(1/R_{AD})+(1/R_{AE})} = 68 \text{ Mohms}$$

Thus, the true isolation test method will correctly fail this measurement. A not unlikely real-world situation would be a smear of contamination that touched A, B, and C.

40.3.2.3 Log of (N) Isolation Test Method. Table 40.4 illustrates the log of *N* isolation test method, and compares it to the true isolation method described earlier. The log method offers the powerful advantage that only a small number of measurements are required to test a complex board. That number is given by log2(*N*) rounded up to the next whole number, where *N* is the number of networks.

TABLE 40.4 Isolation Methods Compared

	Network Name							
Measurement Number	A	B	C	D	E	F	G	H
Log method								
1	+	+	+	+	–	–	–	–
2	+	+	–	–	+	+	–	–
3	+	–	+	–	+	–	+	–
True method								
1	+	–	–	–	–	–	–	–
2	–	+	–	–	–	–	–	–
3	–	–	+	–	–	–	–	–
4	–	–	–	+	–	–	–	–
5	–	–	–	–	+	–	–	–
6	–	–	–	–	–	+	–	–
7	–	–	–	–	–	–	+	–
8	–	–	–	–	–	–	–	+

Thus, for a board with eight networks, we need only three measurements. The gain is even greater for large boards. For a realistic board with 4,000 networks, only 12 measurements would be needed.

This method involves a compromise of fault coverage for parallel leakage detection. Consider the example shown in Table 40.4. The top half of the table considers a very simple board with eight networks and illustrates the pattern of measurements required by the log method.

Networks noted with a + in a given measurement are connected to the upper side of the measurement system. Networks with a − are connected to the lower side. Notice that in each measurement, about half the networks are positive and half are negative.

A hard short between any two networks in Table 40.4 will be detected by either method. In at least one measurement, a + will be at one end of the short, and a – at the other. Both methods work well for hard shorts, and parallel resistance effects play no significant role. But consider the effect of two 15–M. leaks, one from network A to network B and the other from network A to network C. If the threshold is 10 M., this fault will not be detected by the log method, but the true method will fail test measurement #1. The log method is ineffective because there is no one measurement that has the + end of the measurement system on network A while the—end is connected to networks B and C simultaneously. (Were the A–B resistor moved to A–D, then we would detect an error on measurement #2 of the log method.)

The log method may fail to detect certain combinations of high parallel leakage. For product types where a low isolation resistance threshold is acceptable, this may not be a significant issue. Note that this risk may be reduced by substantially increasing the test threshold, such that a larger proportion of individual leaks are likely to trigger a fault report.

40.3.2.4 Isolation Failures: Distinguishing Shorts and Leaks.

Earlier discussion made a distinction between hard shorts and leakage failures, although both reports result from the isolation test. Consideration of either the true isolation test method or the log(*N*) method shows us that neither method immediately tells us the opposite end of the short or leak (refer again to Table 40.4). In the true isolation method, we know that the network under test is leaking or shorted to some other network, but we don't know which one. Initially the log(*N*) method tells us slightly less: We know only that the short is between that half of the networks switched positive and the half switched negative (or ground). Upon fault detection, either method must call a subroutine to search all network pairs systematically to localize the fault. Searching all networks in pairs for leakage can be slow as well as ambiguous. Therefore, some test systems allow the user to disable searching for leakage.

In the case of distributed leaks, a clear answer may be impractical because searching pairs of networks never connects all of the leakage paths in parallel. The effort to localize a high-resistance leakage may report the entire problem, part of the problem, or none of the problem. The exact result depends upon the actual leakage resistances present, the pattern of networks involved, and the isolation resistance threshold. Note that a flying probe system seeking to "verify" defects may be unable to detect some or all leakage for the same reason. It may be advisable to return such boards to a grid (or other fixtured tester) for final pass/fail.

40.4 SPECIALIZED ELECTRICAL TESTING METHODS

Certain special testing methods have evolved to provide for detection of defects more subtle than simple shorts, opens, or leaks. Additional methods have evolved as suitable to specific types of test equipment, notably the flying prober. These are discussed in the following text.

40.4.1 Hi-Pot Testing

Hi-pot or high-potential testing is very similar to isolation testing, but is commonly distinguished by the magnitude of the applied voltage and, to some extent, by the expected behavior of the detected failure. In the context of bare printed circuit boards, hi-pot testing usually refers to voltages over 250 volts, often 500 to 3,000 volts. The objective is to locate faults in the dielectric (insulating) layers of the board that may result in subsequent field failures at lower voltages.

When the dielectric is subjected to a voltage substantially in excess of the expected working voltage, certain types of material defects can result in an “avalanche” mode of failure of the insulation. Ionization of the intervening material or atmosphere occurs, resulting in a sudden increase in current flow to some relatively large value. Visible arcing and/or burning may result at the failure site. This contrasts somewhat with the isolation test, where a very subtle leakage current flow is usually detected using a somewhat lower voltage. Most often, the isolation test is less destructive as the total energy delivered is less. However, depending upon product conditions, arcing can occur at many voltages and in such cases an ordinary isolation test is essentially the same as a hi-pot test.

It is often impractical to perform hi-pot tests on finished products, except at limited numbers of test points. Equipment limitations are one factor, it being expensive to construct test equipment and fixtures capable of routing

such high-voltage signals to a large number of test points. However, the product itself is often a poor target for such tests when evaluated in finished form. Modern products are often constructed with relatively fine spaces between conductors.

On the surface layers of the board, the exposed component connection sites are usually too close together to withstand very high voltage stress without surface arcing. Such arcing is destructive to perfectly good product. The voltage at which such arcing will occur is a function of product geometry and atmospheric conditions.

In consideration of this, the most common practical application of hi-pot testing is to inspect raw material for defects before etching. For example, a thin FR-4 core, clad with copper on both sides, might be evaluated by placing a high voltage across the opposing sides. Any crack or other defect in the insulating material may ionize, resulting in a large current flow. Thus the defective material is rejected before substantial value is added in subsequent processing.

40.4.2 Embedded Component Tests

Methods of embedding certain electronic components *within* the board have been developed. The most common example is the embedded or “buried” resistor. Such resistors are constructed by embedding a layer of partially conductive material within the board. By selectively removing (or adding) material, the resistance value is adjusted. Accuracy ranging from a few percent to many tens of percentage points is realized. Typical resistance values range from a few ohms to thousands of ohms. The most common use of this technology is within high-speed digital circuit designs to replace large numbers of termination resistors with a resistance of 200 ohms and lower. Measuring these values accurately is challenging, requiring good fixture construction

and cleanliness. Another difficulty with testing of buried resistors is obtaining usable expected value data for the resistors. At the board shop, most resistors are specified as a shape and a type/thickness of resistance material rather than as a specific resistance value and tolerance.

It may be necessary to analyze the circuit pattern and compute the net resistance of series and parallel combinations, arriving at a measurable final resistance value for the tester.

Embedded capacitors may also be present. All boards exhibit capacitance between various traces, and especially between planes. The amount of capacitance is determined by the parallel surface area of the conductors, the thickness of the insulator between them, and the dielectric constant of the insulating material. Some product designs seek to maximize the desirable noise suppression benefits of capacitance between power and ground planes by making the intervening insulator thin. Some go further and use special insulating cores for these layers.

This is the common form of buried capacitance. Most bare board test systems are not well suited to measuring capacitance values, particularly small ones. In some cases, no measurement is specified and it is only important that the test system tolerate the presence of the capacitance. When measurements are specified, it is usually true that few test points are involved. It may be expedient to use benchtop equipment.

40.4.3 Time Domain Reflectometry

Time domain reflectometry (TDR) is a measurement method often used to verify the radio frequency (RF) impedance of a signal conductor on a circuit board. The RF impedance is important to the proper function of high-speed digital or RF applications. Examples include computer products, cellular

telephones, radios, etc. The RF impedance of a signal path should not be confused with the DC resistance, as verified during the continuity test. It is common for a trace with seriously errant RF impedance to demonstrate a very solid DC connection (i.e., low DC resistance). The RF impedance of the trace is most strongly affected by the trace's width, thickness, z-axis spacing from the ground plane, the location of adjacent traces, and the relative dielectric constant of the type of insulating core used to build the board. These parameters are usually rather constant within a particular panel, justifying use of coupons as a means of monitoring the delivered product. Standard bare board testing systems (other than flying probes) do not incorporate TDR capability, as the signal paths through the fixture will not pass the fast-risetime TDR signal. TDR is commonly conducted on a test bench manually.

TDR test systems inject a very fast-risetime voltage step into one end of the conductor. Discontinuities in the RF impedance level along the conductor result in reflected voltage waves being returned to the driving point, where they are collected by the same probe that injected the signal. The result is usually presented as a graph of RF impedance versus distance from the point of injection. Because of reflections and disturbance occurring at the point of injection, a minimum trace length is needed to get a meaningful measurement. Extremely short networks are not ideal candidates for TDR measurement. A trace 2 in. or more in length is generally required to obtain a useful reading. Longer traces may provide improved accuracy of the result. A branch-off to a second signal path along the measured length will disturb measurement badly; thus an undisturbed signal path provides the best measurement target.

A typical TDR result graph is illustrated in Fig. 40.7. This illustrates a region of approximately 50 ohms RF impedance, rising toward infinity as the trace ends in an open circuit at

the right, but falling between the upper and lower pass/fail bounds in the region of interest.

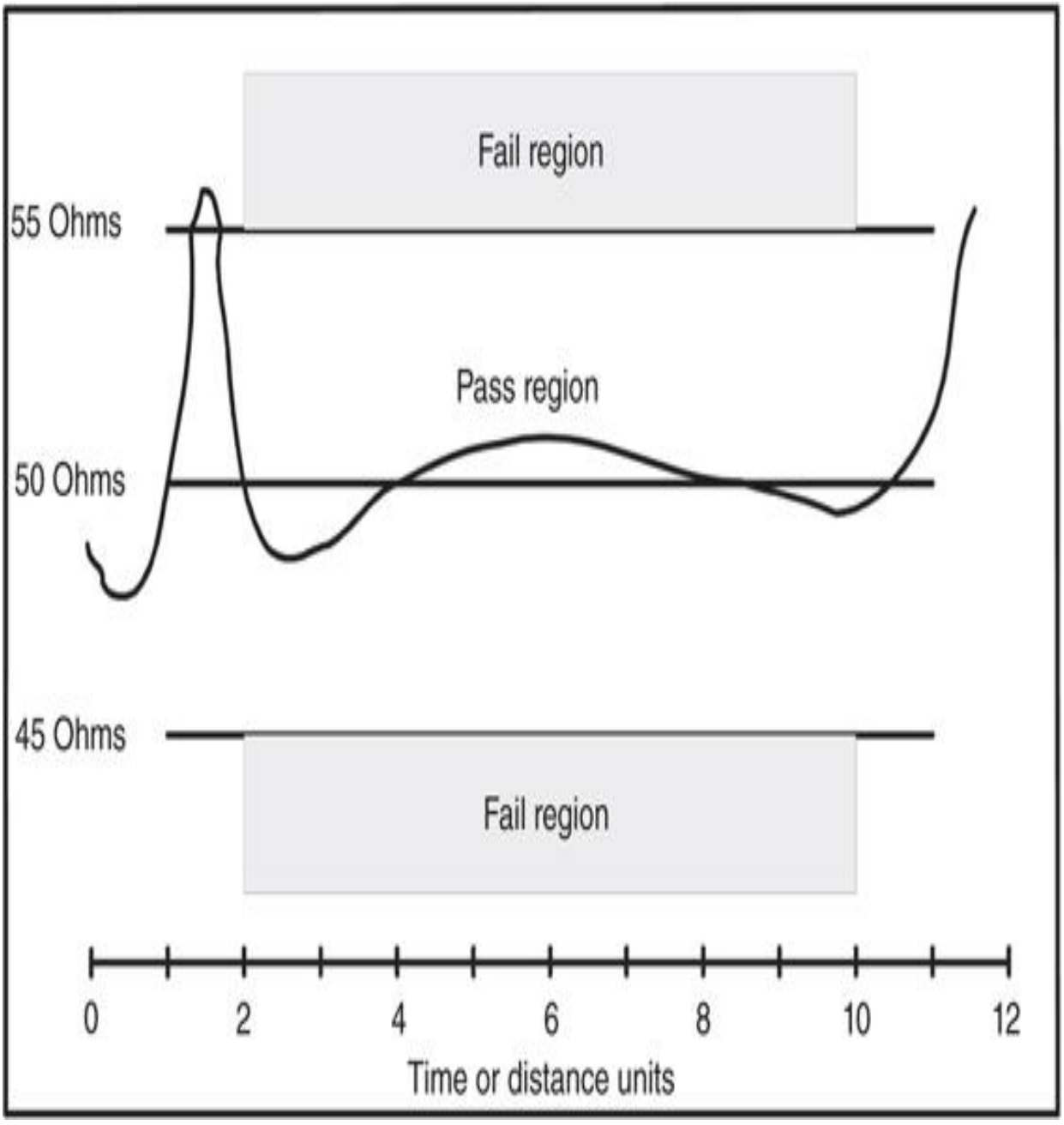


FIGURE 40.7 Typical TDR measurement.

Sample testing using handheld probes is popular and practical, but the influence of hand and body position on the measurement can be significant, reducing the repeatability

of the result. Several vendors offer flying probe solutions dedicated to TDR test. While requiring some additional setup they are faster at higher volumes and greatly improve repeatability.

40.4.4 Test Methods Unique to Flying Probe Systems

Because flying probe systems contact pairs (or other limited numbers) of points at any one time, they cannot directly perform precisely the same isolation measurements as can universal grid (and other fixtured) systems. DC isolation is performed between pairs of networks, with the number of measurements reduced by determining which networks are adjacent to the network being tested and therefore likely to cause isolation problems. Otherwise, flying probers are capable of ordinary DC continuity and isolation measurement, as discussed earlier. In addition, most flying probe vendors have developed alternative measurement methods that reduce the number of measurements and therefore reduce time lost to mechanical motion. These methods are discussed in the following text.

40.4.4.1 Indirect Measurement of Isolation or Continuity. Different vendors have developed various implementations of indirect measurement, but in general these methods share a general assumption that a given product network will display a certain amount of capacitive or other electromagnetic coupling to neighboring planes or traces. The amount of coupling is affected by the geometry of the traces involved. If a trace is broken, the remnant will display reduced coupling. Similarly, if a trace is shorted to another trace, the amount of coupling will increase substantially. If the test system measures the amount of coupling from each trace to a ground plane (or other

electrical environment), a degree of confidence can be obtained that all traces are intact. No direct measurement of isolation or continuity is necessarily made.

Instead, the coupling signature is used to imply the correctness of the configuration. As no direct measurement of isolation or continuity is made, we refer to these methods as indirect measurements.

Typically these methods are highly reliable in detecting hard shorts and opens, but may be less effective in detecting distributed contamination or high-resistance connections of several meg ohms or more. Specific methods include constant-current capacitance measurement (charging or discharging variations), voltage-source measurement of Resistance-Capacitance (RC) time constant, alternating current (AC) capacitance measurement, and measurement of the electromagnetic coupling of an AC signal between adjacent networks.

The capacitive techniques using constant currents are generally based upon the approximation:

$$C = i\frac{dt}{dv} \quad \text{or,} \; C = i\frac{\Delta t}{\Delta v}$$

where C is the network capacitance, i is the charge or discharge current, and v is the change in voltage that occurs during the measurement time t. Related, though more complex, behaviors occur for RC time constant and AC coupling measurements.

Using the preceding example, note that if two networks are shorted, the resulting capacitance is the sum of their individual capacitances. The larger capacitance causes a slower charge rate than is expected for either net individually. The system may note that these two networks are adjacent and displaying suspiciously similar charge time behavior. The system tags the networks as suspicious, and either fails them or verifies the presence of a short with a DC

measurement. Networks containing an open will have reduced capacitance and will charge or discharge too quickly. These conditions are illustrated in Fig. 40.8.

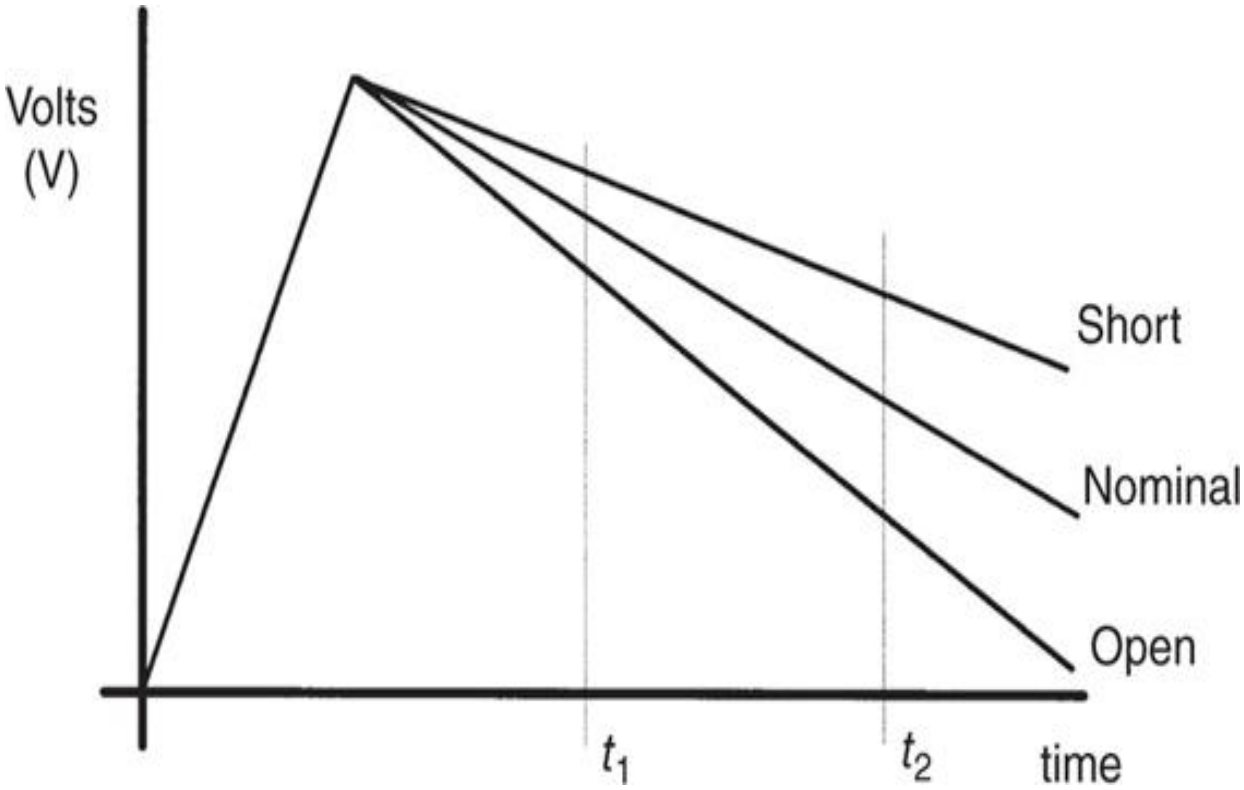


FIGURE 40.8 Indirect measurement: constant-current discharge.

To use these indirect methods, most systems require testing of a first article board using standard direct measurement methods for both continuity and isolation. Once the board is known to be good, the signal-coupling behavior is learned for each network on this board. The learned values are saved and compared to measured results from subsequent boards as described previously. Tremendous speed increases are obtained by eliminating repetitive probing of each network at multiple locations, particularly in the case of isolation testing. Some users combine a traditional DC continuity measurement with the indirect method as a substitute for isolation.

40.4.4.2 Adjacency Analysis: Isolation Testing on Flying Probe Systems. Adjacency analysis simplifies isolation testing on flying probers by reducing the number of measurements, even for direct measurement methods. In adjacency analysis, a database is prepared listing each network and all traces found to be immediately adjacent to that network according to a set of geometric criteria. Such locations are assumed to represent the sole opportunities for shorts and leaks. Isolation testing is then performed only between adjacent pairs, this measurement being well suited to the nature of the flying prober. It is important that attention be paid to whether such analysis is three-dimensional. Networks may cross over a network horizontally, but on a different layer of the board. A hole or defect in the intervening insulating layer may allow a short or leakage to occur.

In the example illustrated in Fig. 40.9, network A would probably be judged adjacent to B, but not to C. B would be considered adjacent to A and D. Assuming that the qualifying dimension was a bit smaller than the distance from E to either B or D, E might not be judged adjacent to either.

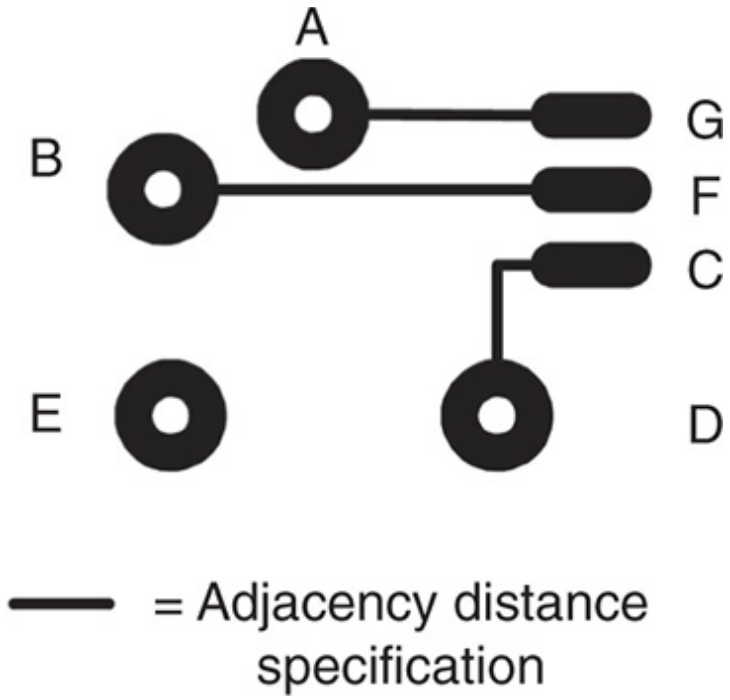


FIGURE 40.9 Network adjacency.

40.5 DATA AND FIXTURE PREPARATION

An essential element in any test operation is the means of generating test programs, and, in the case of fixtured tests, the design of an appropriate test fixture. There are several methods for deriving this program and fixture information.

These methods vary from simple to complex and from escape-prone to very sound. The most common terms used in the language of bare board testing for the test program development are self-learning and netlist testing. *Netlist testing* is a misnomer that confuses computer-aided design (CAD) output with test inputs and implies that there is not much in between. In this discussion, we will use the term *data-driven test program* to indicate the program to be loaded into the test system is derived from the board's design data (which may be provided in any of several

different forms). On the other hand, a self-learned program is derived by placing an assumed good board on the test system and causing the test system's internal computer to create a program automatically that can be used to compare other boards to the detected pattern. It is worth noting that the description "known good" is often used to describe this first board, when in fact our knowledge of its quality is often imperfect.

Flying probe test systems generally require no fixturing, except sometimes a frame to hold thin boards or to load multiple small boards simultaneously. Flying probers still require test program generation and optimization. Instead of a fixture, the product program contains probe position information for planned test. Data preparation processes are therefore similar to those of fixtured tests, but only test program data are output.

Note that the extractions of program and fixture information are quite naturally linked. In fact, the final test program cannot be created until the fixture is defined. The fixture determines how the individual test points of the test system are connected to specific product locations.

Knowledge of how the fixture has taken hold of the product is essential to determining which system test points to employ in performing specific measurements. Thus, the same software system generally outputs both the final test program and the fixture drilling/loading information.

40.5.1 Self-Learning

Self-learning has increasingly limited application and is subject to certain escape risks derived from assuming that the original circuit board is good. The self-learning method requires that a fixture be already available, as well as a known good board (preferably). A shorting plate is placed on the fixture in place of the product, and the test system uses

this to identify which test points are employed in the test fixture. (All test points found shorted to the plate are considered active. This eliminates test points of no interest, shortening the test program and saving considerable execution time during both learning and testing operations. This set of active points is sometimes referred to as a mask.) The known good board is then substituted for the shorting plate, and the pattern of product interconnections is learned and saved as a test program.

A few boards are tested, and, if results appear reasonable, the program is considered valid. The key drawback of the method is that self-learned test programs determine that all the boards are the same, not that they are good. Moreover, for economic fabrication of the test fixture, it is necessary to process product data anyway; thus we may as well have output a data-driven test program. With virtually 100 percent of board designs being CAD-driven, there is little motivation to use self-learning today.

40.5.2 Data-Driven Testing

The preferred method of deriving program and/or fixture data is data-driven programming (DDP), sometimes referred to as netlist testing. The basic idea of data-driven test programming is to test the board using the same database used to specify its manufacture—in other words, the original design database. The fixture and DDP development process can be divided into two stages:

- Input/extraction, the preparation and processing of the various possible input sources into a format usable by the second stage
- Fixture data, test program, and repair file output, and subsequent application of the data.

Factors such as data quality and completeness, the format of data available, and fixture design can significantly reduce or extend software processing and engineering time. Board technology, size, and complexity tend to increase time requirements. While software tools are not always the most immediately visible tools in the testing department, the completeness and automation of software tools can have a large impact upon whether you are able to set up and test boards quickly and efficiently rather than struggling to build fixtures quickly—while testing very few boards.

Ideal fixture software readily accepts the product data, analyzes the data, recommends an optimal fixture design including all fabrication details, and outputs computerized numerical control (CNC) files for fixture fabrication, material requirements, special procedures required, and a test program in the proper format for the selected test system(s).

40.5.2.1 Selecting Fixture Software. A complication arises due to the mechanical incompatibility of many types of test systems. If the available equipment includes something of a grab bag of different equipment types, the test manager's task is made considerably more difficult in several ways. Aside from the obvious problems of manufacturing different fixture types, the manager is also faced with difficult load-leveling tasks. In such circumstances, the test manager may be forced to select general-purpose fixture software packages. By virtue of offering many configuration options, these require additional operator training and present increased opportunity for error. If the testing equipment uses a shared fixture type, it becomes possible to standardize the software process (and raw material). Optimized configurations may be locked into the software, minimizing error opportunities.

40.5.2.2 Test Data Extraction Methods for Fixtures and Programs. The initial stages of processing include the

acceptance and inspection of the input data to ensure that they have been presented in a valid format. These data are then scanned to determine which sites on the board deserve test points, and what measurements are required among these test points in order to ensure proper continuity and isolation of the product. There are a variety of input sources, summarized in subsequent sections.

A usual goal of the extraction process is to eliminate unnecessary test points. According to predefined rules, the software identifies those end points of each network segment where test pins can and should be placed. For example, a T-shaped network probably requires three test points, located at the extreme extensions of each arm of the T. This provides sufficient connectivity to the product to permit a complete continuity test. One point per network is the minimum needed to attempt isolation testing, and two points per network make the isolation test more robust by permitting the tester to ensure that these points are in proper contact with the product.

The following is a generic description of the software process, where CAD or photoplot information is available.

- *Data orientation* The toughest side of the board in terms of test centers is usually oriented face down. It is often easier to manage a heavier, more complex fixture on the bottom side of the test system. This may require flipping or inverting the data.
- *Test site identification and optimization* Depending upon customer preference, it is often true that some test points can be deleted from the program. Figure 40.10 shows a network with a midpoint B that does not need to have a test point on it. The test points at A and C are all that are necessary to determine whether this network is isolated and contains no opens. Test point optimization can reduce the number of points in a fixture by 10 to 50 percent,

thereby reducing the cost of the fixture and the time needed to test the board.

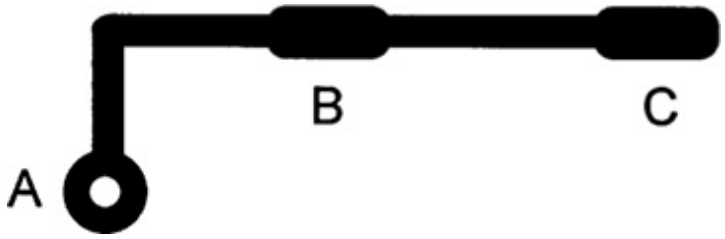


FIGURE 40.10 Optimizing a network.

Although optimization provides some economic and minor throughput benefits, this must be offset by any impact upon the repair process and by any fault coverage risk. Midpoints can provide failure data that help the repair station more easily pinpoint the actual fault site. Where an operator is required, or when flaws appear in the algorithm, the deletion of test points can add to the risk of test escape. Optimization is sometimes not performed, speeding data preparation and reducing escape risk but adding cost to the fixture.

- *Pin type assignment* Once the test sites have been identified, test pins can be assigned to the features to be tested. Different pin types may be required for different features. For example, a through hole might require a large head or larger-diameter pin than a surface-mount technology (SMT) pad on 0.025 in. centers. The software usually includes a table relating feature types to pin types.
- *Test system type identification* Mechanical details of the fixture must suit the target test system. The fixture in a universal grid system requires assignment to a grid of uniform centers. A more detailed description of fixture and system types is included elsewhere in this chapter, but obviously the fixture must be built in the correct size and grid density to match the specific test system to be employed. Figure 40.11 shows three of the most common grid configurations available. Single density (100 points

per sq. in., or a 0.100 in. grid) is the most common, with double-density systems being added as product technology demands.

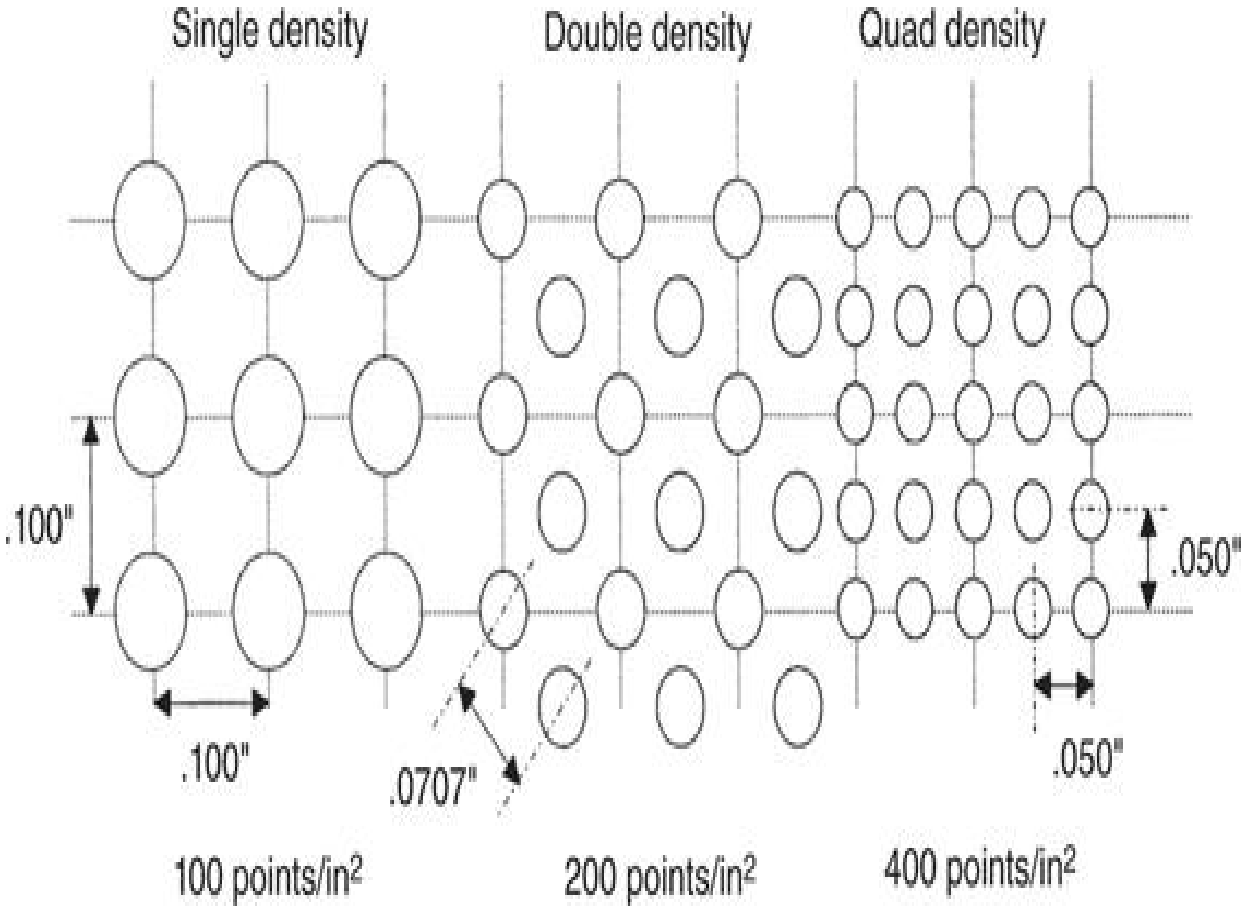


FIGURE 40.11 Single-, double-, and quad-density universal grid patterns.

Of course, a few systems still use wired fixtures, and here the output will be a set of drill files, a wire list, and the test program. The balance of this discussion focuses on tilt pin translator–equipped grid systems:

- *Grid pin mapping* The fixture software determines which system grid location will be mapped to each of the previously determined on-product test targets. Several factors are considered:

- No two targets can be assigned to the same grid location.
- No assignments can allow the pins to touch each other as they tilt through the fixture (cross pins).
- Drilled holes in fixture plates cannot break out into adjacent holes (adequate spacing on all plates).
- No assignment can require a pin to tilt beyond the predetermined deflection limit (determined by the fixture and pin design).
- Test sites that are very close together may require that on-product targets be staggered such that the test pins are more widely separated. (See Fig. 40.12.)

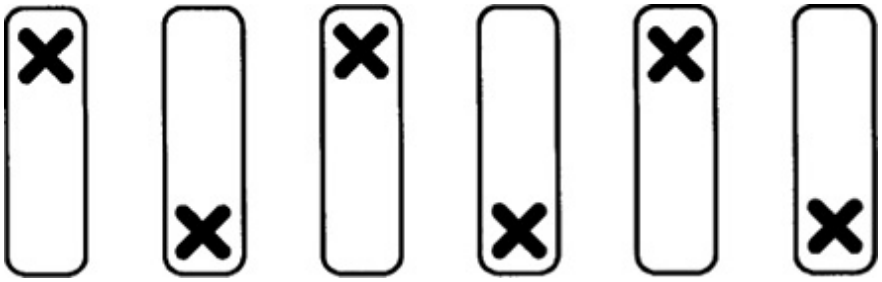


FIGURE 40.12 Test point staggering.

- Hole diameter and placement relative to the pin diameter and pin deflection must be optimized. A nearly vertical pin might be assigned a hole diameter just slightly greater than its shaft diameter. This clearance balances avoidance of friction against pointing accuracy during testing. Other pins of the same diameter that are highly tilted will require a slightly larger hole to avoid binding. The fixture adjusts drill sizes for each hole, depending on the amount the pin is deflected. This maintains pointing accuracy while eliminating pin binding. Hole locations may also be shifted slightly to compensate for the fact that the pin is pointed at an angle and that the point of contact will not be at the

center of the hole. The result is a more reliable test fixture.

- *Test program output* With all pins fully mapped to grid locations, the test program file can now be constructed and saved.
- *Tooling* The last step in data preparation requires the marrying of the job being processed with the tooling. The tooling includes tooling to the test system and tooling for the specific fixture design utilized.
- *Fixture file outputs* The completed CNC files for fixture drilling and fabrication can now be created and the test fixture prepared.

40.5.3 Data Formats

Modern circuit boards are designed using CAD systems. These systems output data files used by the board shop to generate phototools, drill files, routing patterns, and other tools used to fabricate the boards. While several standards have been developed for data outputs from this process that can provide useful data input to the final test process, adoption has not been universal. As a result, test engineers and software providers have developed means of hijacking and converting the photoplot data stream, and can use this to drive the test process with certain compromises and a degree of inconvenience. Both approaches are discussed in the following text.

40.5.3.1 Gerber Format Data Extraction. The primary example of “hijacked” photoplot data arrives in Gerber photoplotter format. Even here a standard was eventually developed. RS-274X is a standard that affords a degree of consistency to the photoplotter files. This data stream is a series of drawing commands that direct the photoplotter in drawing the copper patterns for each layer of the board. The

drawing is made with a selection of “apertures” that define different pen tip shapes and dimensions. Thus a fine line is drawn by choosing a small aperture, issuing a light-on command, and directing a move. These data are contained in a very large set of files, containing a picture of each layer of the board. Combined with a drill file and aperture definitions, the appropriate information for generation of fixture and test program files is present, but a considerable amount of processing is necessary to develop understanding of layer-to-layer connectivity and finally identify test targets.

Although the standardization of Gerber data has been improved with efforts such as RS-274X, it remains a data format originally optimized for the purpose of photoplotting and not for testing. CAD system developers and board designers have a great degree of freedom in how they design board features and in how these features are represented in Gerber. As a child will readily demonstrate, many different sequences can be used to draw even simple shapes. A rectangle might be created by “flashing” a square pattern, or might be created by an elaborate spiral using a much finer aperture, a zigzag pattern, or a sequence of overlapping flashes. This variety leads to occasional errors, because it is difficult for any Gerber extraction routine to be capable of handling all possible permutations. The software system must successfully interpret any of these examples (and many others) as defining the same intact square area of copper conductor pattern on the final product. Some methods result in huge file sizes.

Despite these problems, this method is far superior to self-learning, digitizing, or drill file extraction, and remains in common use in a variety of software packages. The data requirements to start from this format include:

- Photoplot files for each layer, solder mask layers, etc.
- Photoplot files for silk screen legend(s) (required for computer-aided repair)

- Aperture file
- Drill file
- Board outline

40.5.3.2 CAD/CAM Data Extraction Method.

Recognizing the problems inherent in photoplot extraction, system vendors have agreed to add support for test-oriented output formats, in particular IPC-D-356 and 356A. These formats provide data in a much more readily digested format, and eliminate most ambiguities in processing the data. These formats include the following data:

- Signal ID, network name, and/or network number
- Reference designator or PIN number (e.g., U14, 12, R11) for the related component on board
- X-y coordinate of pad center (minimum data set requirement if grouped as connected)
- Pad dimensions relative to the center, and size of the hole (if any)
- Resistor or other component values (if appropriate and not usual)
- Board side (top or bottom)
- Mid-network flag suggesting that test point placement may not be required.

Often this data set is converted to a standard such as IPC-D-356 from the CAD/CAM system's internal data formats by means of an intermediate converter. These software converters, although simple, are usually customized for each individual CAD system. A converter must be updated or modified with any output changes made by a CAD vendor due to a CAD system software update or new product introduction. The number of converters required by an independent PWB manufacturer could be quite high, as data

will likely be received from many different CAD system types. Fortunately, many of the CAD vendors now include direct output of IPC-D-356 data or readily provide converters. Acceptance of these standards is now such that in many cases even Gerber input data are first converted into IPC-D356 format prior to final processing.

40.5.4 Outputs from Data Extraction

Once all the preparation steps and processes have been performed, there are several outputs generated by the fixture software.

- *Test file* A data-driven test program is outputted in a format compatible with the test system type. This file informs the test system of the measurements expected and of pass/fail criteria. Some test system formats permit the data-driven test program to support a graphical representation of the fixture and/or board on the test system monitor, provided that sufficient data are included in the test program file. This graphical presentation is useful in fixture and/or program debugging.
- *Fixture fabrication files* Probably the most significant output—the drill files, one for each plate or pass required by the fixture design—is needed in drilling to start building the fixture. (In the case of wired fixtures, a wiring list is also required.)
- *Repair/verification files* Files can also be outputted that support the repair or verification function. These relate the graphical image of the board to the assigned test point locations in the program. Preparation often relies on inclusion of Gerber data in the input data stream to the software system. Extensions to IPC data formats are planned to better support the repair function without this recourse to photoplot data. Some test systems may carry

trace image information in the test program file as well, for enhanced debugging support on the test system.

40.5.5 Setting Up a Fixture

With the fixture assembled and CAD data–derived program prepared, the next step is to set up the fixture on the test system and validate the fixture and program. Details vary with the fixture and system used, but in general the following steps are taken:

- Program data are loaded into the test machine from the disk or network.
- Test thresholds are set to the desired continuity and isolation values.
- Compression settings on the test system are adjusted to the proper values for the fixture type. In some cases, these values may already be included in the test program file.
- The new (or recalled to duty) fixture is compressed with a nonconductive material of similar thickness to the board being tested.
- An all-isolations version of the test program is executed to verify that the fixture does not contain any internal shorts.
- The fixture is then compressed again with a conductive plate in place of the product, intentionally shorting all fixture test points together. Often this plate is a simple piece of copper-clad G-10. Copper oxidation can prevent reliable contact, and users sometimes wrap the plate in fresh aluminum foil or use a flash-gold-covered plate. In this step, an all-shorts version of the test program verifies that all expected test points are continuous through the fixture, up to the shorting plate. The intent is to verify that the number of test points is correct and that, under multiple compressions or closures, all points are present and remain in contact with the shorting plate.

- Assuming proper alignment and cleanliness, the product can then be tested with the final test program. If certain errors immediately repeat on all boards, then it is reasonable to suspect a pin-loading error or other error in the fixture, and investigation is warranted.

The basic techniques just described are generally applicable to all fixture types, whether tilt pin, wired-dedicated, or other specialized types.

Do not underestimate the value of removing dust and debris from the product and fixture, both during setup and occasionally during operation. Target sizes on modern products are not tolerant of debris, and false open circuit reports are an immediate result. Tacky roller-type cleaning systems may be helpful in periodically removing debris from test fixtures, system grids, and the products themselves. Follow the test equipment manufacturer’s recommendation regarding the use of electrostatic discharge (ESD)-safe cleaning materials near the test system.

Adjustment of fixture compression is also important, especially on press-type systems where the amount of compression stroke is controllable. (In vacuum fixtures, the dimensions of various fixture plates and components usually fix the amount of compression.) Undercompression usually leads to poor contact and false open results. Overcompression can cause excessive marking of the product by probe tips, probe damage, and fixture damage.

Overcompression is a very common problem, and, unfortunately, so is product damage in the form of excess probe marking. It seems intuitive to just press harder when you experience contact problems, and this is often the first step taken. But the actual change in force per spring probe is very small as it travels further, until the spring probe hits bottom—and at that point you begin damaging the product almost immediately. A typical spring probe in a grid system presents about 139 g of force when compressed 0.167 in.

(two-thirds of travel). At zero travel (uncompressed), the spring inside is already preloaded to about 55 g. The force increases at a spring rate of 503 g/in. Just before bottoming, the spring force peaks at about 180 g. Thus, there is only modest force gain possible before serious danger of bottoming the probe occurs. Consult the spring probe manufacturer for details, but most probes function well at about two-thirds of full travel. If contact problems remain at this level of compression, leave further compression adjustment as a last resort and look elsewhere. Generally, you should never cause the probes to hit bottom. (Some older vacuum fixture probes are a notable exception.)

40.6 COMBINED TESTING METHODS

As product density and geometry become more challenging, the cost of fixture construction increases. In a large number of cases, the most challenging test sites occur at only a few areas of the product. It is possible to combine test techniques such that less expensive means are used to test the majority of product features, while more advanced and costly techniques are reserved for the most challenging test sites. Some examples follow.

40.6.1 Split Net Testing

This is perhaps the oldest and most primitive example of a sequential or combinational test. When the product complexity exceeds the capacity of a fixture design to solve the test requirement with a single fixture, it is possible to divide the test responsibility among multiple fixtures. The flip test method of dual-side access described earlier is one example of this. More typically, the test department has

dual-side-access equipment, but the density of test sites exceeds the capability of the fixture and/or test system.

One way to split the responsibilities is to divide continuity and isolation between fixtures. For example, one fixture could be limited to two test points per network. These two would be checked for continuity with each other (to verify that there are no open pins in the fixture) and would then be used to perform a 100 percent isolation test of the product. A second fixture would complete the continuity test. In very difficult cases, multiple fixtures can be used.

Handling boards in this scenario is complicated. Boards that pass the first fixture must be stacked and prepared to run on the second fixture. But boards that fail the first fixture must be tagged with failures, and in many cases must be run through the repair process, retested, and combined with the boards being sent to fixture 2. Such failed boards must not be confused with any failed boards from fixture 2, which have already completed the first phase of testing.

Unless there is a large continuous flow of boards with two different test systems/fixtures set up, it is also likely that the two fixtures will have to be installed/removed from the test system a number of times.

40.6.2 Manual Combination of Methods

It is also possible to divide the test burden by testing the majority of ordinary test sites with a test fixture, followed by a flying probe system to test strictly limited portions of the product. Without special software, one has the same handling problems as in the split net case. But it is possible to automate the data handling between the two test systems using network resources, such that a single error tag results from both tests. All boards then flow through both test systems, and any rejects flow to repair. This flow is very

similar to that of ordinary testing, resulting in less confusion. An interesting additional benefit of this combination is that the flying prober not only can test those sites that you wish to avoid fixturing, but can also retest any of the failures noted by the universal grid. This can eliminate the majority of false open reports caused by stuck pins and contamination, improving the total first-pass yield.

CHAPTER 41
BARE BOARD TEST EQUIPMENT

David J. Wilkie
Everett Charles Technologies, Pomona, California

41.1 INTRODUCTION

The largest volumes of bare boards are tested on fixtured systems. However, for smaller volumes or special purposes, “flying probe” systems may be preferable. This chapter discusses them both to enable the user to make the most effective decision based on testing objectives and volumes.

41.2 SYSTEM ALTERNATIVES

41.2.1 Fixtured Systems

Each dedicated, or hard-wired, test system presents some sort of standardized interface pattern of test points. This may consist of a universal grid’s continuous array of points (bed of nails) or may be a connector pattern of some type. In the most primitive systems, a simple cable connector may be

presented. Each of these types of equipment uses one or more types of customized test fixtures to connect this standard electrical interface pattern to the unique contact pattern of a particular product to be tested.

Each fixtured system includes a measurement unit that can be connected to any of some thousands of test points by a solid-state switching matrix. A central computer controls the measurement unit and switching matrix. This computer also controls the press (or vacuum mechanism), which can compress the product against spring-loaded test points presented to the product by a customized test fixture.

To imagine the system's operation, first consider the measurement unit to be an ohmmeter. The computer commands the switch matrix to connect the red lead of the meter to, say, test point 17. It then connects the black lead of the meter to test point 1027. The measurement system can then be commanded to measure the resistance of the product under test between test points 17 and 1027. The test program dictates a long series of such measurements organized to test the product completely. Because the switching and measuring occur at the high speeds possible with modern electronics, a complex board can be tested in seconds.

41.2.2 Dedicated (Hard-Wired) Fixture Systems

Originally the most popular system type, dedicated systems are generally being displaced by systems employing less expensive and more accurate fixturing methods. The word "dedicated" refers to the fact that it is generally impossible to salvage very much material from these fixtures for reuse in other fixtures. The cost of these fixtures derives from this fact, and from the high labor and material costs involved in the original construction.

41.2.2.1 Advantages of Dedicated Fixture Systems.

A primary advantage of these systems is that, because each test point is routed within the fixture by a flexible wire, it is possible to position any test point at just about any location. If your product requires 8,000 active test points, then you need no more points than this in the test system. One hundred percent utilization of available test points is possible. This contrasts with the universal grid approach discussed later, wherein points can be shifted only a small distance from the original location on the grid. In that case, you must have enough electronic test points to cover the entire surface of the product at some constant density, and any given fixture will generally use only a portion of these points. Thus, the capital equipment cost of a dedicated system may be lower, but the ongoing fixture costs may be much higher. Dedicated systems are generally built with no more than about 10,000 test points, with smaller numbers common.

41.2.2.2 Construction of Dedicated Fixtures.

The test fixture for such systems generally consists of a rigid box structure with one side facing the product to be tested and some other side or surface presented to the interface pattern of the test system. The side facing the product includes the probe plate. This plate of insulating material is drilled to mount an array of spring-loaded pins able to make electrical contact with the product. The reverse side of these pins is connected within the box by physical wires to the system interface connector on the opposite side of the fixture.

Fabrication of the fixture involves the usual data-processing steps, followed by spring probe type selection, drilling of the probe plate, installation of spring probes, drilling of the interface plate, and installation of system mating contacts or connectors. Many spring probe tip styles are available to suit different diameters of target pads and holes (see Fig. 41.1). In most cases, the probe plate actually

carries a socket or receptacle into which a replaceable spring probe is inserted, simplifying service. The underside of the receptacle protrudes into the fixture box and carries a wire-wrap tail. Each of these receptacle tails must be wired to an individual system interface contact on the bottom of the fixture.

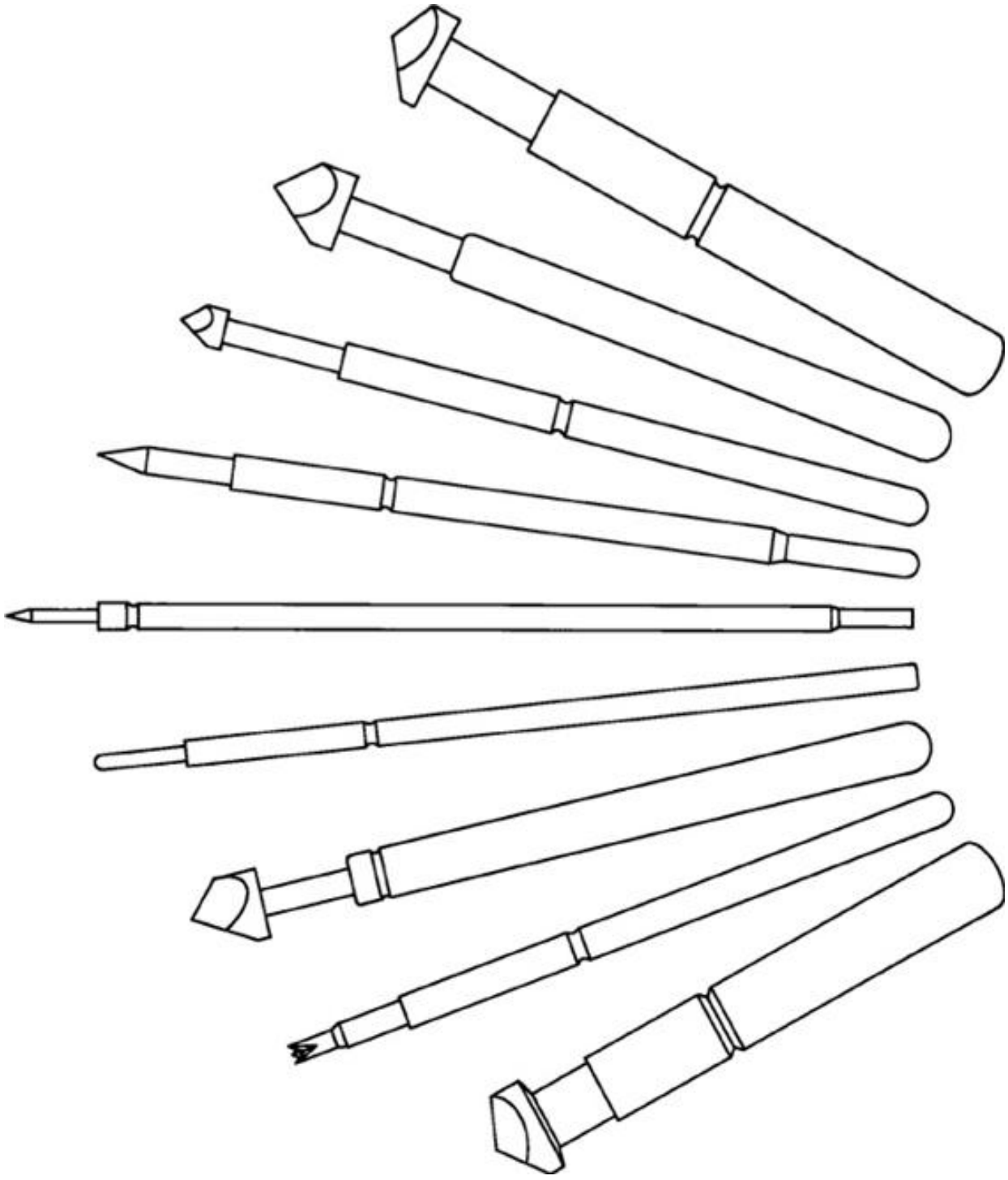


FIGURE 41.1 A variety of spring probes and receptacles. (*Courtesy of Everett Charles Technologies*.)

Compression of the product onto the fixture spring probes may be accomplished with electric drives, pneumatic air

cylinders, or vacuum (see Fig. 41.2). Vacuum compression can result in the lowest system cost, but adds cost to the fixture and limits the total number of probes that can be compressed.

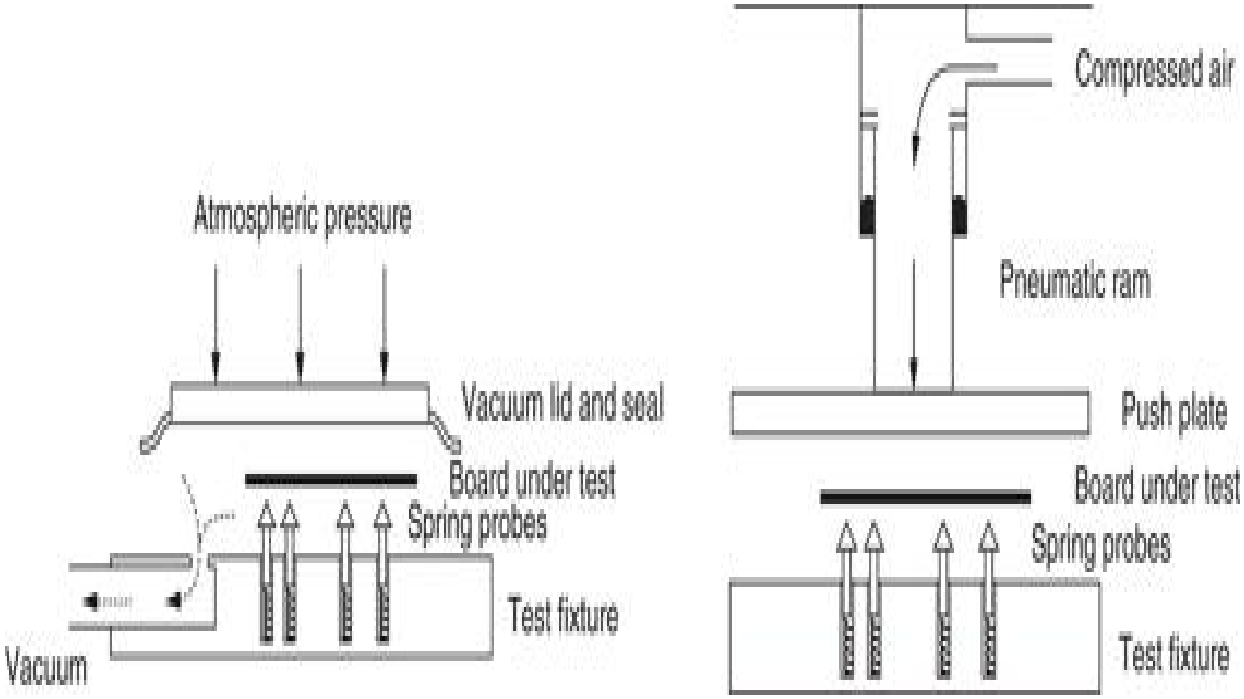


FIGURE 41.2 Vacuum versus pneumatic compression.

Many forms of fixture interfaces have been provided, with many appearing as small universal grid patterns. Some very simple test systems have been constructed with a large number of ribbon (or other) cable connectors presented as the only connection to the fixture. The matching wired fixture may be troublesome to connect (because of the large number of cables), but is left connected for days or weeks at a time to a single fixture type due to the quantities of boards being tested.

41.2.3 Flying Probe–Type Test Systems

Smaller volumes and specialty parts are tested on flying probe–type test systems. These consist of a small number of robotic probes with independent measurement abilities. These are moved among the various product test target locations, and a sequence of measurements is made. Such systems offer the powerful advantage that no fixture preparation is required (although data must still be processed to prepare the test program). The best of these systems are also able to provide extremely high probe placement accuracy, generally exceeding that of fixtured systems. The primary drawback of such systems is low throughput, as a result of the need to reposition the probes mechanically between measurements.

41.3 UNIVERSAL GRID SYSTEMS

The most flexible and widely used electrical test solution is the universal grid test system (see Fig. 41.3). Most systems now include upper and lower grids, permitting simultaneous dual-side access for test of surface-mount technology (SMT)–type products. Grids offer very high test speeds, and moderate the cost of test fixtures by permitting the reuse of many fixture components. Thus, today, the majority of product is tested on universal grid systems and fixtures.

FIGURE 41.3 Universal grid test system. (*Courtesy of Everett Charles Technologies*.)

41.3.1 Universal Grid Test System Design

The universal grid test system presents a rectangular array of equally spaced test points. Generally this is chosen to be large enough to cover the test area of the largest product type to be tested (see Fig. 41.4). It is common to speak of

the density of test points presented. A single-density system presents points spaced at 0.100 in. (10 per in.). Thus, there are 100 points per sq. in. Similarly, a double-density system has test points spaced at 0.0707 in. and provides 200 points per sq. in., and quad-density spacing is 0.050 in. for a density of 400 points per sq. in. As grid cost is largely a function of the number of test points, larger sizes and/or higher-density configurations become expensive. With modern grid designs, the test system grid size can be upgraded in the field by addition of electronic modules. With older designs that use wire between the grid and the electronics, upgrades may be less practical.

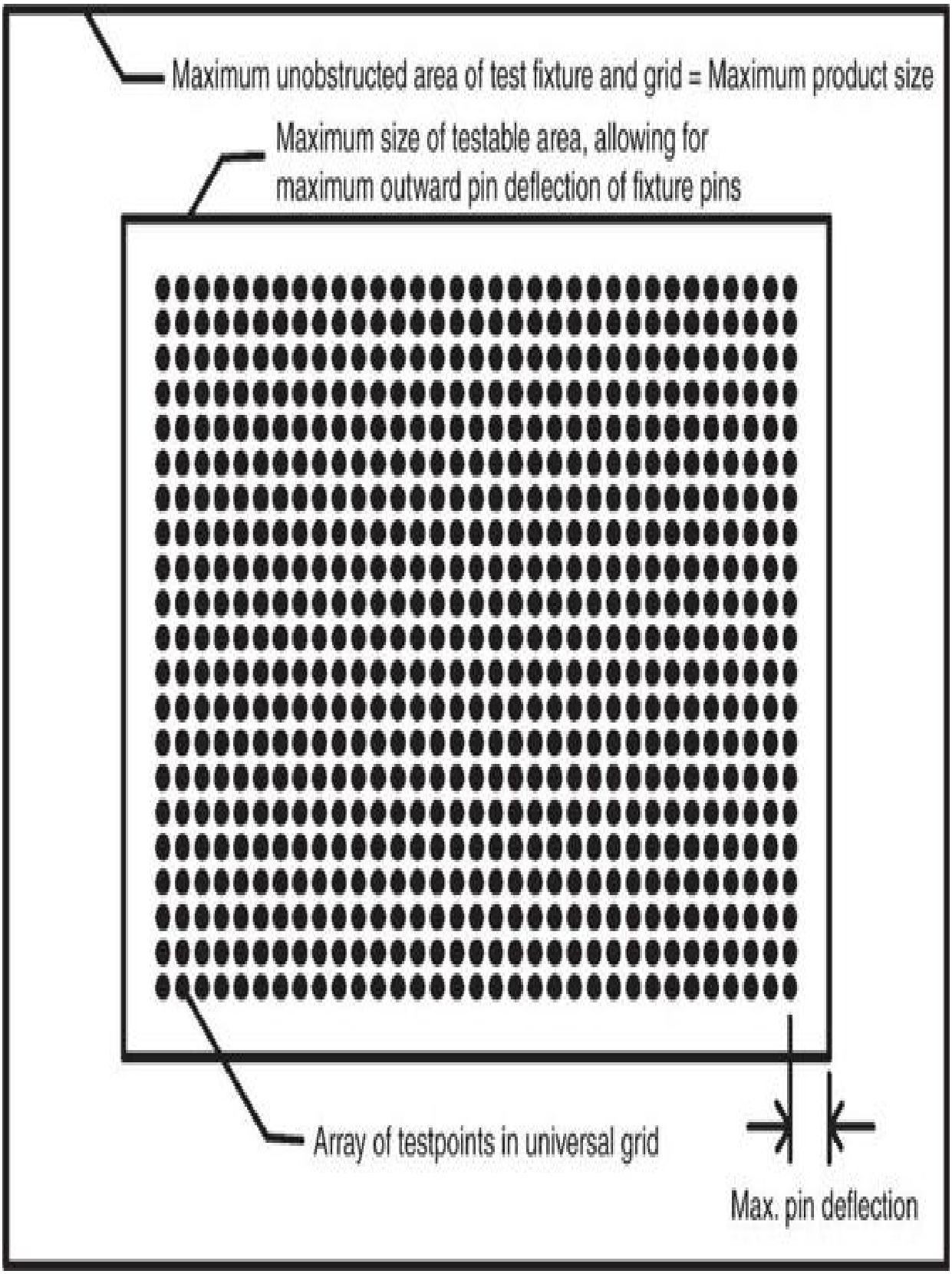


FIGURE 41.4 Universal grid testable area.

41.3.2 Exclusion Mask Fixtures for Universal Grid Systems

Occasionally, some applications involve product whose test-point spacing exactly matches the grid pattern. This situation may permit use of a very simple fixture referred to as an *exclusion mask*. This is composed of a thin glass-epoxy sheet, perhaps 0.030 in. thick, drilled at those locations where test probes are desired to pass through from the grid to make contact with the product. The exclusion mask (see Fig. 41.5) prevents unused grid probes from contacting the product unnecessarily, preventing erratic contacts and marking of the product. To use such a mask, it is necessary that the grid be constructed with a pointed or chisel-tip probe. Unfortunately, few products exist that are so simple to test.

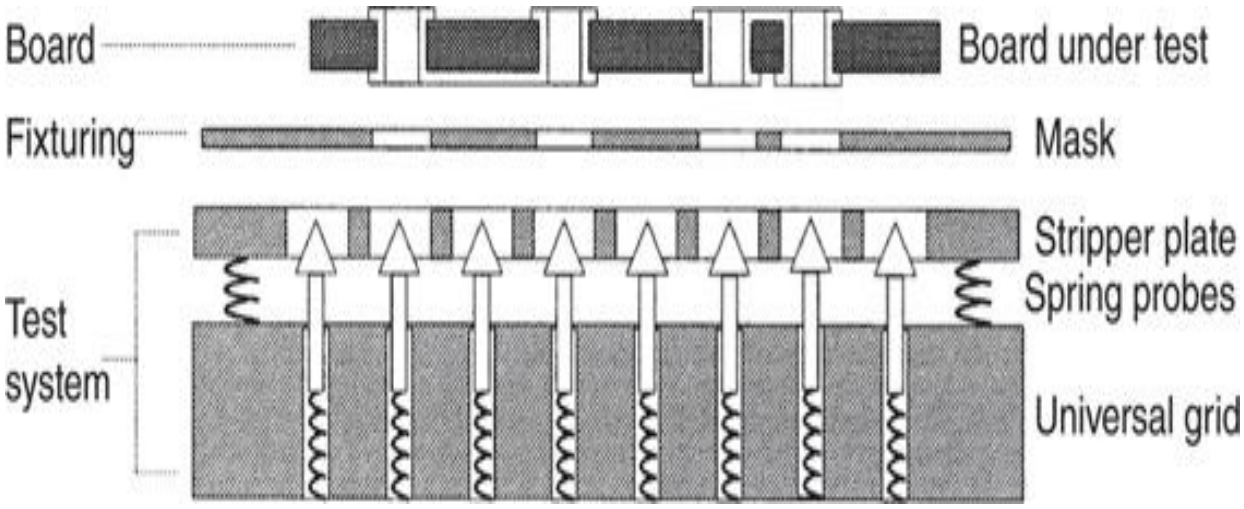


FIGURE 41.5 Exclusion mask fixture.

41.3.3 Pin Translator Fixtures for Universal Grid Systems

Most boards manufactured today are tested on universal grids through the use of pin translator fixtures. These fixtures are rapidly designed and produced using available software systems, and the most expensive material components (the contact pins and plate spacers) are generally reuseable. These fixtures are also referred to as *tilt-pin fixtures* or *grid fixtures*. Grid fixtures and related software remain the fastest-evolving area in electrical testing. Particular fabrication details will not remain current for long. Therefore, this discussion employs current practice only as means of illustrating key issues such as density and registration.

In a tilt-pin fixture, a rigid pin serves the dual roles of providing an electrical contact path from a grid test point to the product and translating the grid test-point location a small distance horizontally (in x- and y-coordinates) such that contact is made to the desired target on the product surface. Because the product targets are unlikely to be perfectly centered above grid test point locations, these pins are usually somewhat tilted from vertical. The amount of tilt or displacement varies according to the amount of x-y shift required. Several lightweight plates of plastic material support these pins. The individual hole locations in each plate are offset the amount required to achieve the desired pin tilt and spaced apart the required distances (see Fig. 41.6). These pins are variously referred to as *tilt pins, translator pins*, or *fixture pins*.

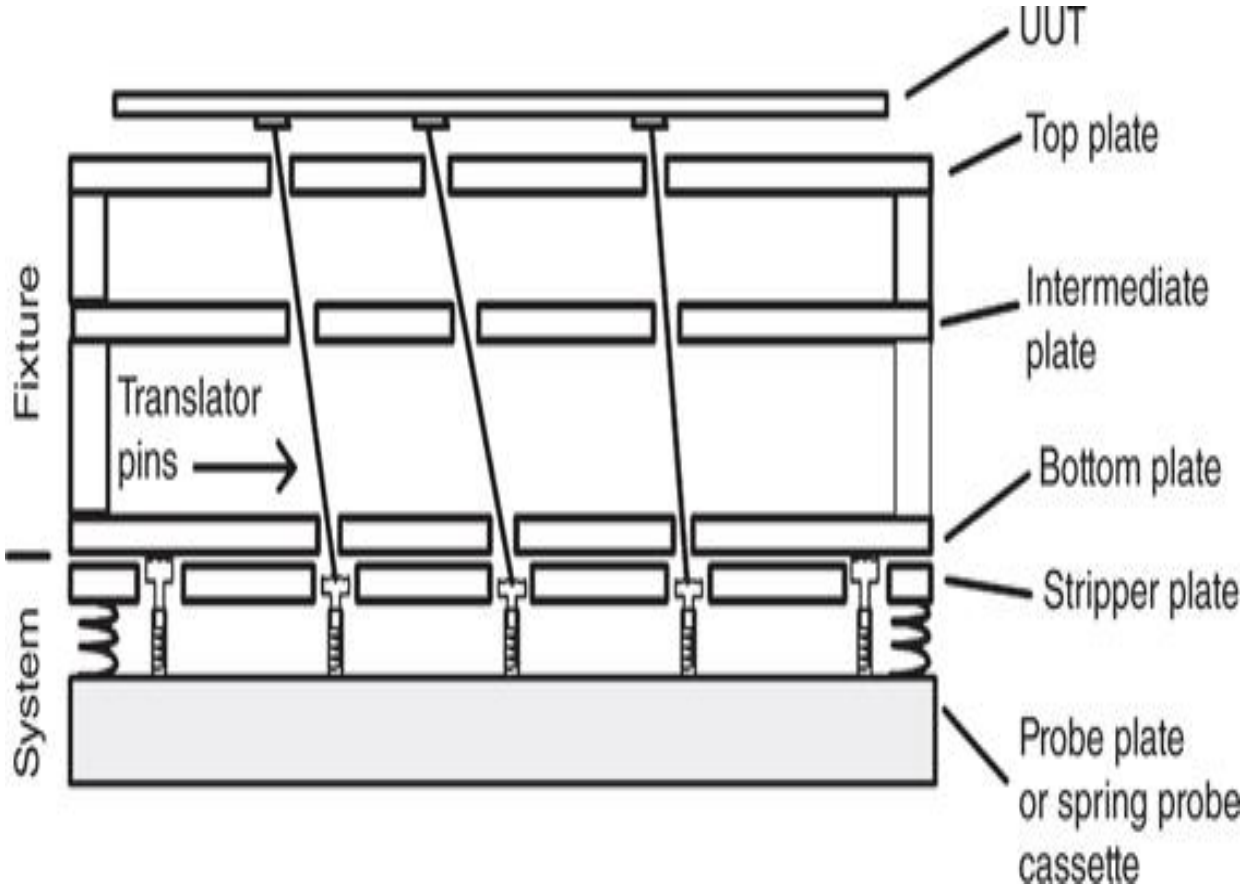


FIGURE 41.6 Single-side multiplate tilt-pin translator fixture.

To enable grid test points to be translated to exactly the correct target location on the product, it is important that each translator pin fall into the correct sequence of holes while the fixture is being assembled. If sufficient intermediate guide plates are employed, then the geometry of drilled holes can be so arranged that a virtual tunnel is created for each translator pin. It becomes impossible for a pin to fall into an incorrect sequence of holes. More plates are required when the maximum degree of pin tilt is increased. Calculation of plate count, position, and drill hole locations is a key function of the data extraction and fixture software, whose process is described elsewhere in this chapter.

41.3.3.1 Test Pins for Pin Translator Fixtures. A wide variety of pins are available for use with different system types and for different applications (see Fig. 41.7). These vary in length, tip style, material, cost, and thickness. For a given angle of tilt, a longer pin is generally able to translate the test point a larger horizontal distance (larger pin displacement). Pins with enlarged heads of various shapes are useful for probing large-diameter holes. Aggressive shapes such as chisels provide the pin with enhanced abilities for cutting through product contaminants, but may be unsuited to closely spaced test applications. At present, the vast majority of pins are headless music wire pins with lengths ranging from 2.5 to 3.75 in. When probing a large-diameter through hole, common practice now is to probe the annular ring around the hole rather than pay the penalty for an odd-headed pin type.

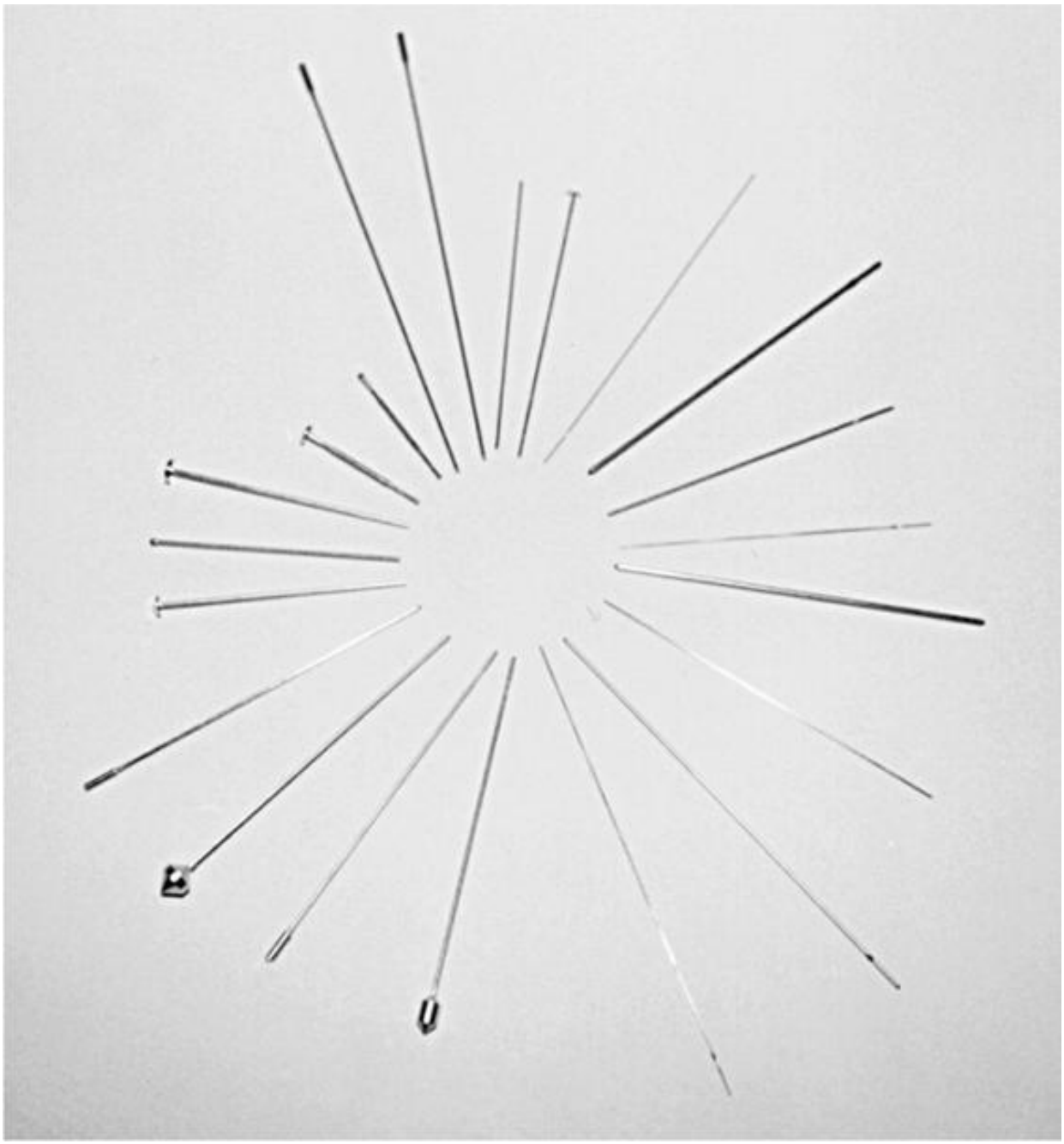


FIGURE 41.7 Examples of translator pins. (*Courtesy of Giese International*.)

41.3.3.2 Pin Displacement in Grid Fixtures. Pin displacement capability is one of the more significant performance measurements of a pin-fixture design combination. A larger displacement ability provides greater freedom in allocating test points, resulting in improved ability to fixture complex products on a test system of given

density. With an arbitrary fixed rule of thumb of 10° maximum tilt, we can see from Fig. 41.8 that the longer the pin, the further the pin can be displaced from its on-grid location to its on-product target location. The maximum pin displacement that can actually be obtained is a function not only of pin length, but also of fixture design and the resultant maximum tilt angle that can be tolerated in the design. The fixture software usually seeks to arrange pins such that the maximum tilt in the fixture is minimized. This decreases the number of guide plates required, minimizes the number of different hole sizes required in the plates, and tends to reduce friction and binding. Nonetheless, a design that permits a maximum tilt capability ultimately provides the greatest flexibility in assigning test points and generally permits the solving of denser products on grids of a given density.

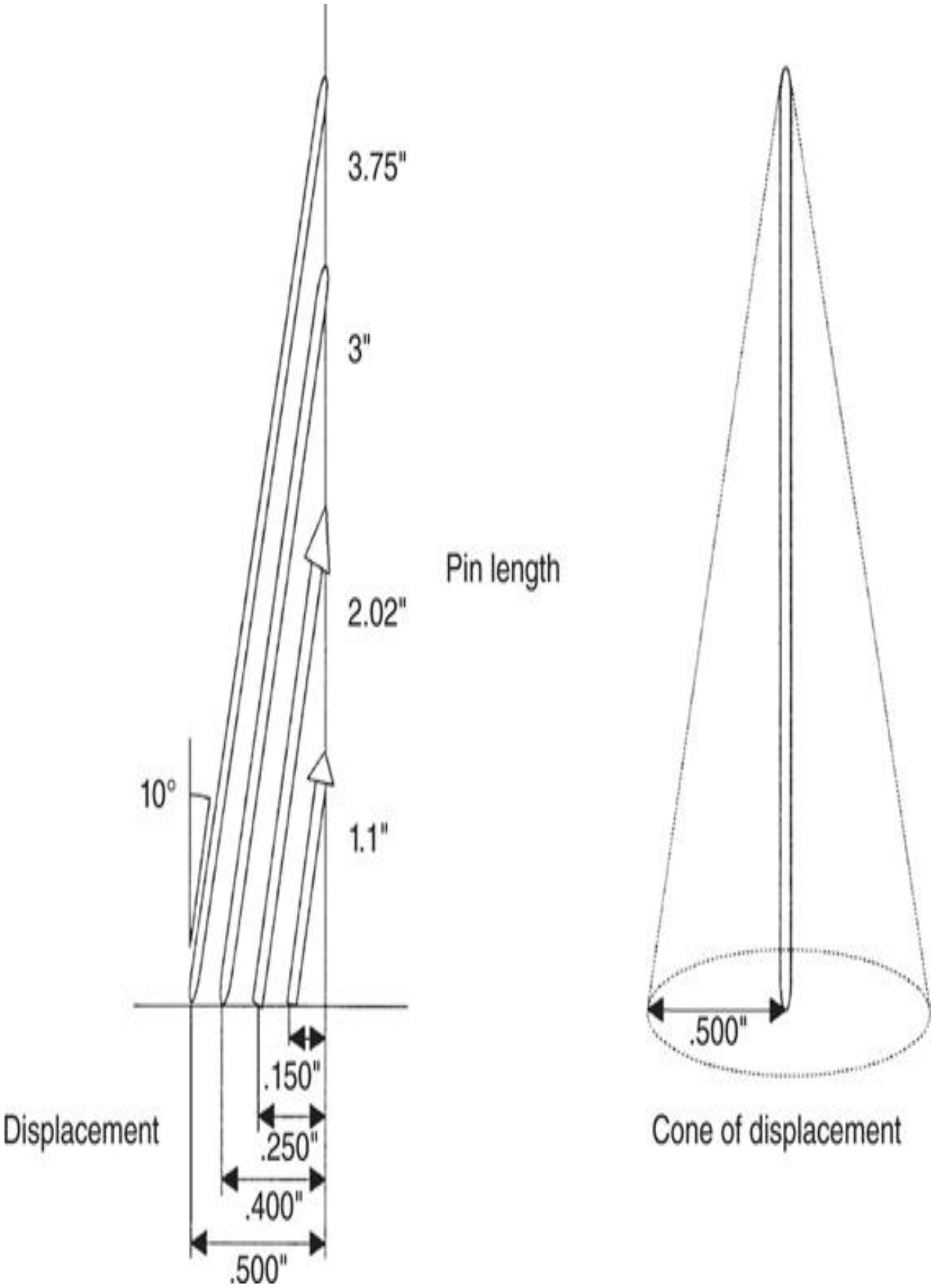

3.75"
3"
2.02"
1.1"
Pin length
10°
.150"
.250"
.400"
.500"
Displacement
.500"
Cone of displacement

FIGURE 41.8 Approximate pin displacement as a function of pin length.

41.3.3.3 Pin Binding and Friction in Grid Fixtures. As noted, the grid fixture pins must lean some distance to connect the grid to the on-product target location. Thus, the relationship between the plate thickness, hole diameter, and angle of displacement is critical. If the plates capture the pin too tightly, binding and friction can result. A pin that is held down below other pins in the fixture by binding will fail to make contact with the product (see Fig. 41.9).

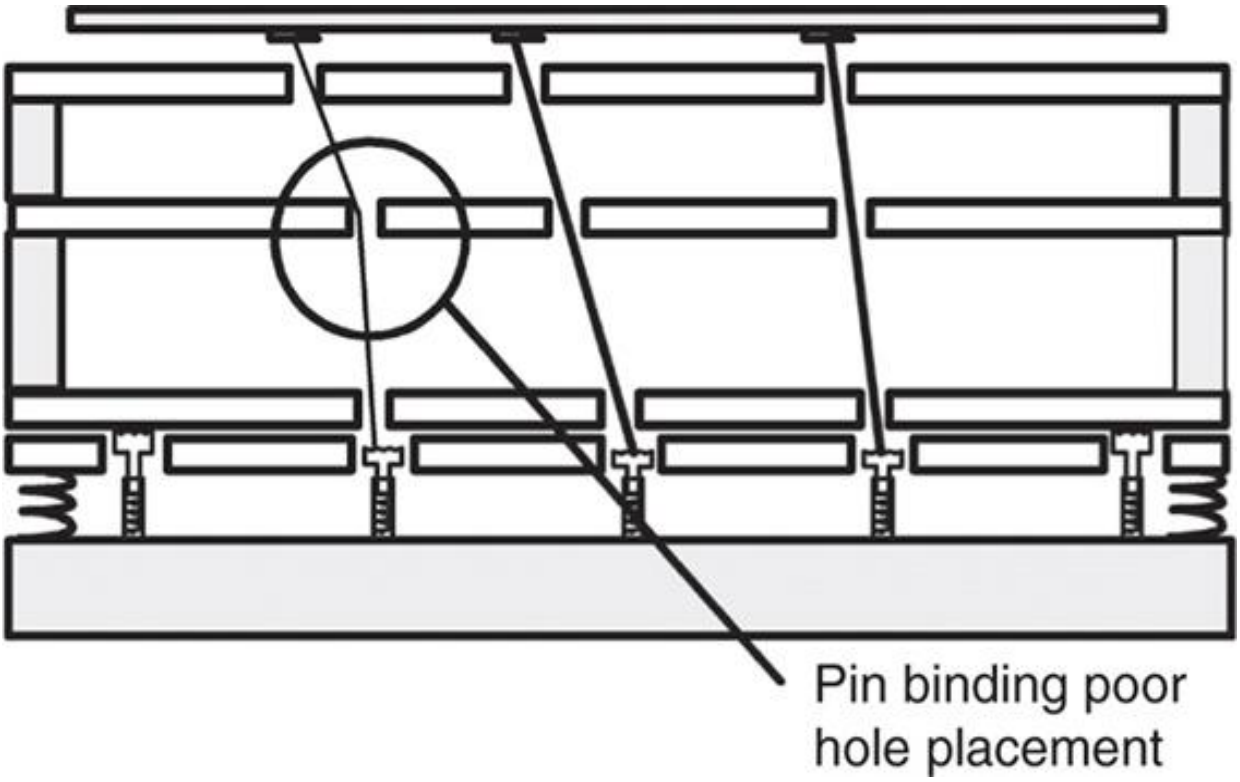


FIGURE 41.9 Pin binding in multiplate tilt-pin fixture.

The spring force of the spring probe in the universal grid is intended to supply the pressure that presses the tilt pin against the product. Every bit of friction in the tilt-pin motion subtracts some of this force. If the friction is great, not only may the pin fail to contact, but if the pin is stuck high (toward the product surface), the product may press on it with undue force in shoving it back into the fixture, resulting

in excess product marking. Binding can be caused within a single plate by hole diameters that are too small for the degree of pin tilt. Binding can result between plates if the plates are offset from one another, forcing the pin to bend as it snakes its way through the various plates. Binding can also result if the plate spacing is incorrect as compared to the design values.

41.3.3.4 Calculations for Tilt-Pin Fixtures. Modern fixture construction software should perform all of the necessary calculations automatically. Yet it is valuable to understand the basic decision processes.

41.3.3.4.1 Minimum Hole Diameter Calculation. The relationships between pin displacement, pin diameter, plate thickness, and drilled hole diameters are trigonometric. We calculate Eq. 41.1:

$$A = \sin^{-1}(PD/PL) \text{ and} \tag{41.1}$$

$$HS_{min} = [SD/\cos(A)] + [PT \times \tan(A)] + HT$$

where HS_{min} = minimum hole size in a particular fixture plate
PT = fixture plate thickness
SD = pin shaft diameter as it passes through the plate
PL = overall pin length
PD = horizontal displacement distance of the pin tail relative to the pin head location
A = angle of pin tilt expressed as degrees from vertical. (i.e., a vertical pin has a tilt of 0°)
HT = minimum acceptable tolerance to ensure that the pin slides freely in the hole

The first term in the equation derives from the effective increase in shaft diameter in the horizontal plane as the pin tilts (see Fig. 41.10). The second term derives from the horizontal distance that the center line of the pin travels as it

passes through the plate thickness. The third term, as mentioned earlier, is to provide a minimal clearance.

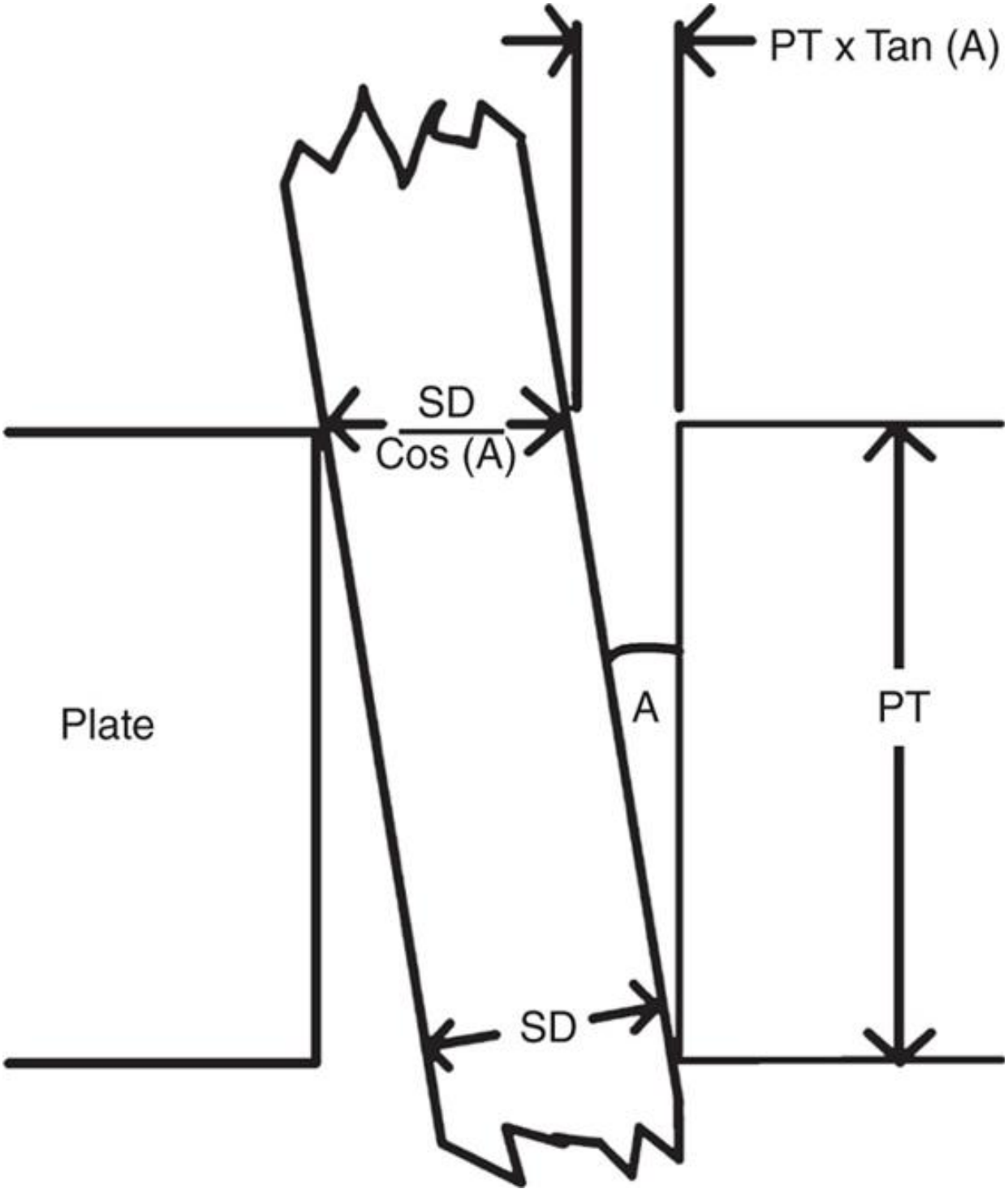


FIGURE 41.10 Illustration of hole diameter calculations for a tilt-pin fixture.

For angles of tilt below 15°, the value of the cosine is close to 1 (over 0.96), and for rough calculations the term may be omitted. (For a 20 mil diameter pin, the contribution of pin tilt to effective shaft diameter is less than 0.7 mil). Similarly, for the same small angles, the calculation of the tangent can be simplified to tan(A) ≈ PD/PL. The error incurred increases as the plate thickness increases. For a 0.1 in. thick plate, the error at 15° will again amount to something less than a 1 mil hole diameter.

With these simplifications, for low tilt angles and thin plates, the formula may be reduced to that shown in Eq. 41.2, with an extra mil or two added to the clearance.

$$HS_{\min} \approx SD + [PT \times (PD/PL)] + HT \qquad (41.2)$$

For the highest-accuracy applications, use the exact calculation.

41.3.3.4.2 Drill Bit Size Selection. Note that the minimum hole size calculated previously is often not the ideal drill size. The most common material used for grid fixtures is polycarbonate.

Polycarbonate tends to have a finished hole size that is about 0.001 in. smaller than the drill size for plate thicknesses typically employed in fixtures. Therefore, 0.001 in. should be included in the tolerance figure HT to permit accurate drill bit selection.

41.3.3.4.3 Pin Lean and Pointing Accuracy. *Pointing accuracy* is defined as the pin's ability to hit an intended target, usually described as a radial dimension (the distance from the intended target to the actual contact location). Because the pin is typically not perfectly vertical, there are several possible sources of error, depending upon the type of pin employed. With the older headed pin types, the head sat above the top plate of the fixture. With modern headless approaches, the pin tip is usually flush with the upper surface of the top plate while in contact with the product. As

the pin tip projects less (nearly zero) above the top plate surface, its tip position in x-y coordinates is better controlled by the hole in the top plate. For this reason, most modern fixture designs operate with the probe tips arriving flush with the top plate surface while the product and fixture are compressed.

It is also preferable that the pins remain approximately flush when compression is released. If they project above the top plate surface, the tip moves out of position in x-y coordinates, as illustrated in Fig. 41.11. When a product is placed on such a pin, the tip initially contacts an incorrect target location. During compression, the pin must drag across the product surface as the pin retracts into the flush position. Thus some spring mechanism, which supports the fixture and pins above the array of grid spring probes, is commonly employed. The fixture may rest on a spring-loaded stripper plate over the grid of spring pins, or the fixture may be designed with spring feet on its underside. In some designs. the fixture kit itself is compressed.

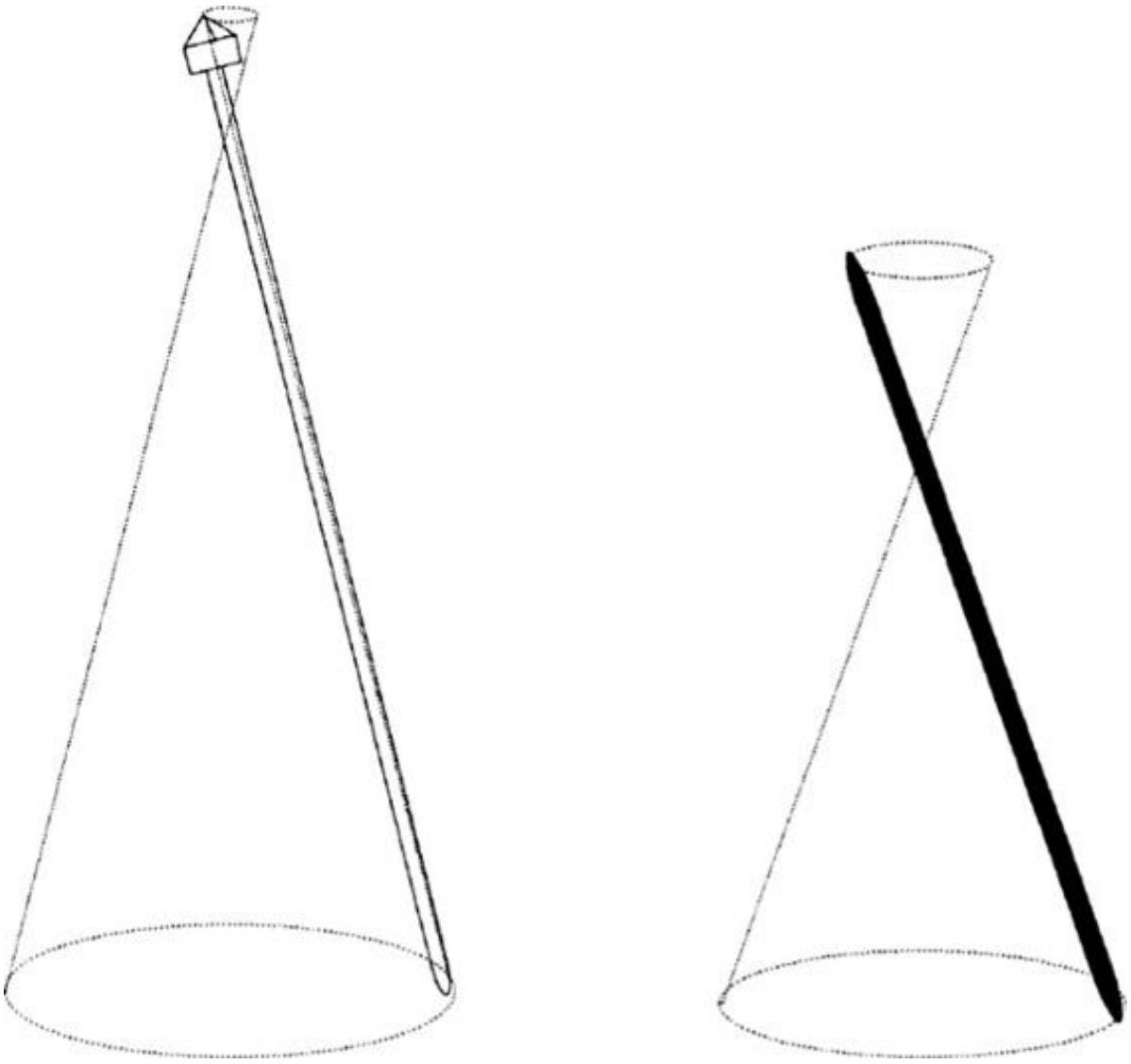


FIGURE 41.11 Pointing accuracy.

Some fixture designs have used bent or curved test pins. In such cases, the pin is bent by including additional fixture plates such that the tip of the pin as it comes through the top plate is perpendicular to the test pad. This allows the top plate holes to remain on the product and mirror the board under test and thus eliminates concerns about the effects of pin contact at an angle. Common examples of such fixtures were built as spring boxes, such that the overall thickness of the fixture decreases during compression. This eliminates the need for spring feet or a stripper plate, but complicates

friction and binding issues as the entire array of test pins must bend and flex during every compression. Contact reliability, product marking, and ease of pin loading all suffer.

41.3.3.4.4 Offset Error Compensation. Figure 41.12 represents the problem associated with the deflection of a pin retained in the top plate and its ability to hit the center of the pad or target. As described earlier, the hole diameter must be sufficiently oversized to allow the pin to pass through the hole at its angle of deflection without binding. Vertical force on the pin from the product above tends to press the pin against one side of the hole, as illustrated. (This has the curious effect that tilted pins can display more consistent targeting performance than do perfectly vertical pins.) As the pin tilts, the center line of the pin becomes substantially shifted from the center line of the hole (note the offset distance *OS* in the illustration). Finally, the conical tip associated with most modern pins has a certain finite radius—the pin is not infinitely sharp. Thus, in the illustration, the product will not contact the pin on its center line. As illustrated, contact will come at the highest point of the tip radius, slightly to the right of the center line. Thus, the theoretical contact point will be at neither the center line of the pin nor the center line of the hole. Probing targets only a few mil wide with probes two or three times as wide requires high-quality probes displaying consistent tip geometry, and software able to calculate the actual point of contact carefully.

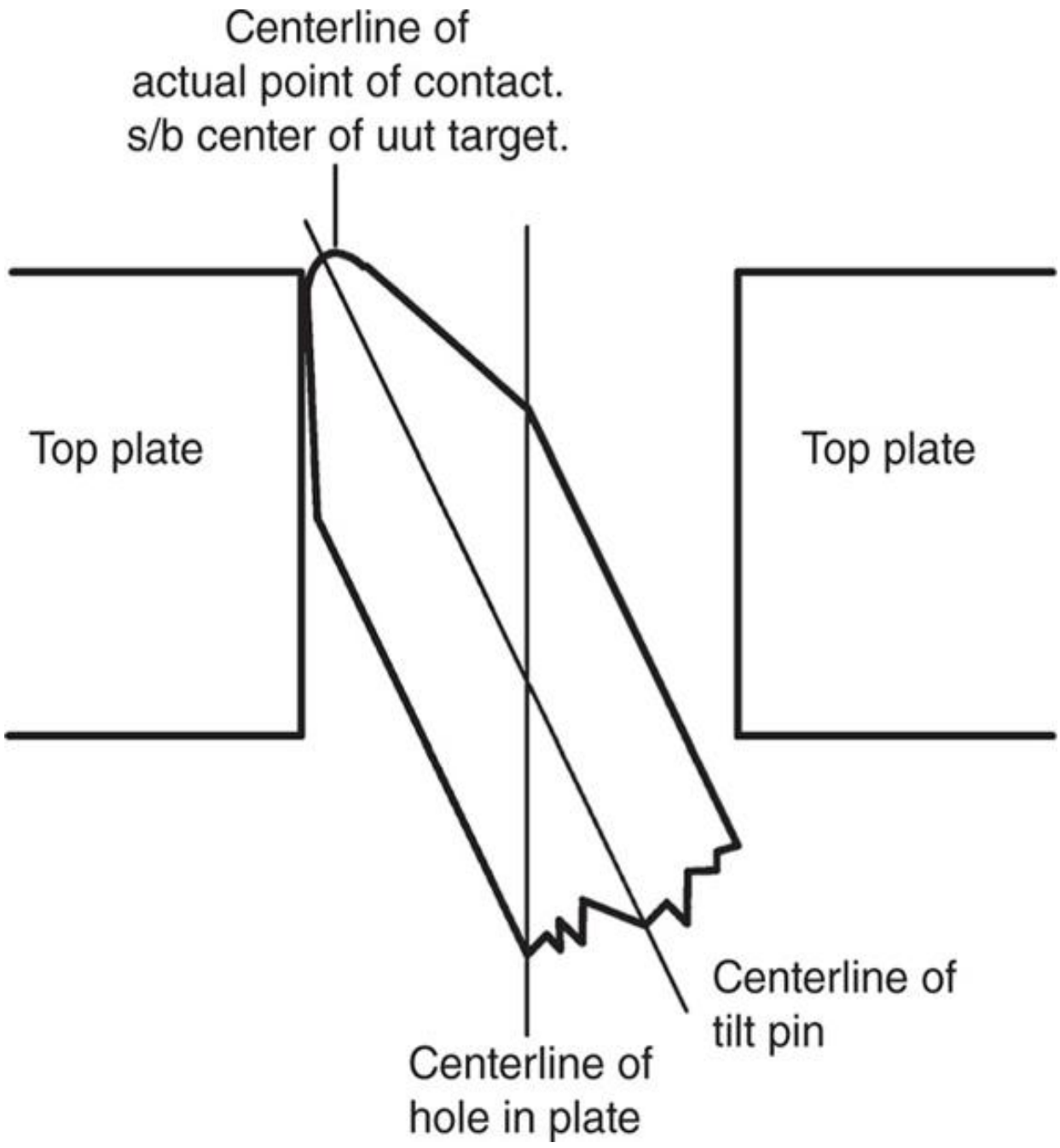


FIGURE 41.12 Pin tip offset error.

41.3.3.4.5 Countersink Drilling of Top Plate. The calculations and considerations just discussed illustrate that thicker plates and higher pin tilt present some interesting problems when combined. A highly tilted pin in a thick plate requires a substantially oversized hole if binding is to be prevented. Looking through the hole at a viewing angle

equivalent to the tilt of the pin, the hole will appear to be oval, with the narrow axis considerably shorter than the drill bit diameter. Of course, the pin is thereby allowed somewhat more freedom of movement along the major axis of the oval. This bit of looseness can be a problem with very fine-pitch products.

A better solution is to use a very thin plate for the upper fixture plate, backed up by a thicker plate drilled oversize. Alternately, a single plate can be countersunk. The effect is the same, as illustrated in Fig. 41.13.

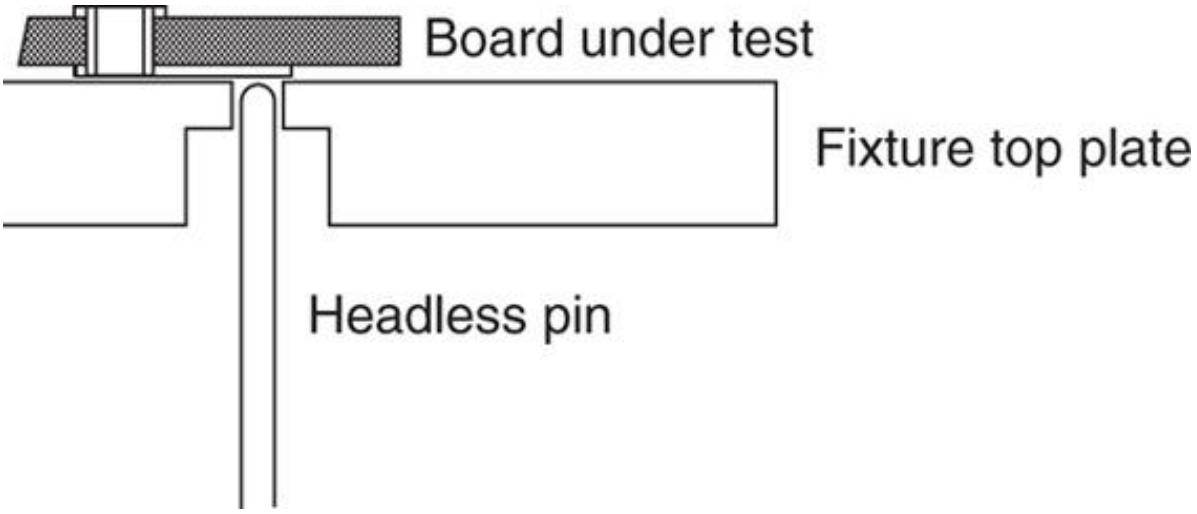


FIGURE 41.13 Countersink drilling of top plate to avoid binding or oversize holes.

41.3.3.5 Retaining Fixture Pins. It is necessary to retain the pins in a translator fixture such that they do not fall out of the fixture during ordinary use and handling. Older headed pin types were often used in single-sided fixtures. The oversized head protruded above the top fixture plate, and therefore the pin was unable to fall out the bottom of the fixture (although they fell out all too easily if one accidentally inverted the fixture). Early top-side fixtures attempted to duplicate this method for the upper fixture by employing a different pin in the upper fixture half, using an oversized "tail" on the fixture. However, the oversized geometry of the

heads is inappropriate for fine-pitch testing, and therefore the use of such pins has fallen out of favor.

The desire to use thin, headless music wire pins necessitated the invention of new means of pin retention (see Fig. 41.14). These have included:

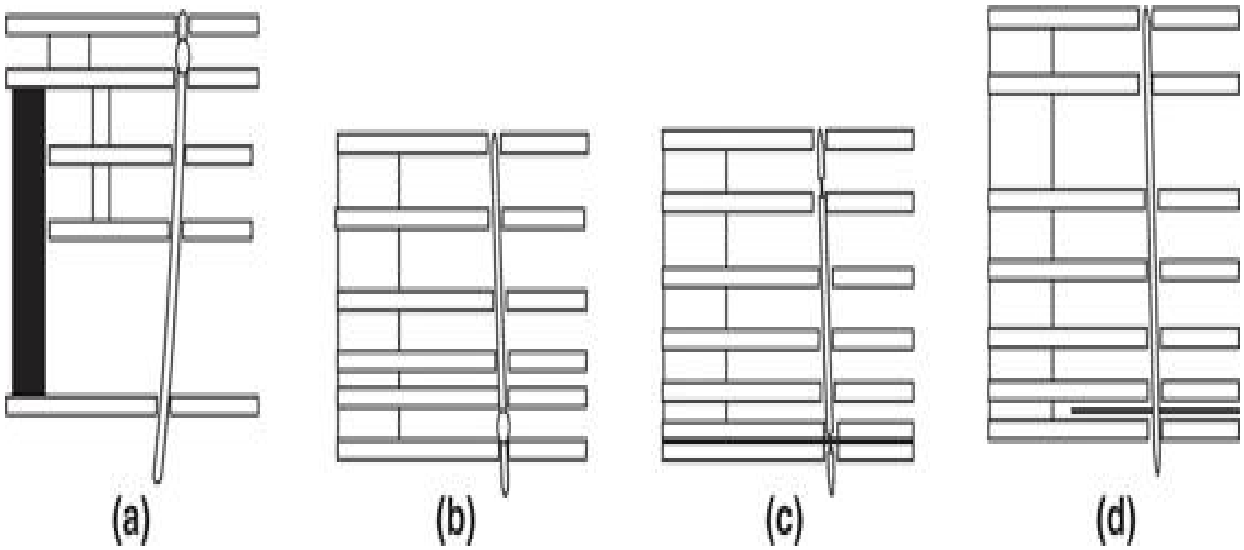


FIGURE 41.14 Alternative pin retention methods. (a) (b) (c) (d)

a. Crimping a wide flat into the pin, and trapping the oversize flat between two plates

b. Trapping the pin in a sheet of foam rubber such that friction retains the pins

c. Passing the pin through a sheet of spandex cloth that grips the pin

d. Passing the pin through a sheet of drilled latex rubber that grips the pin with flexible flaps

41.3.3.6 Examples of Real-World Fixture Designs. While many combinations of fixture techniques have been employed, it is worthwhile to compare several popular examples. No substantial discussion of older headed rigid pin types is included here, as their use is largely disappearing. Most fixtures today are built with headless pins that compress flush into the fixture without bottoming on the

spring probe below, such that the contact force is entirely controlled by the spring (excluding friction or binding effects).

Figure 41.14a represents a common bent or curved pin design using 3.75 in. music wire pins. The upper and lower fixture plates are held apart by a spring mounting, and the entire fixture compresses during actuation. The pins hit the intended target perpendicularly, because they bend toward vertical as they reach the product area. But extra force is required, increasing pad marking. Hole diameter in the top plate can be tightened to improve pointing accuracy because all pins pass through perpendicularly, and a fairly thick top plate is possible. For a given pin length, the maximum possible horizontal displacement is more limited than in straight pin designs, because all displacement must occur in the lower portion of the pin length. The hanging middle plates do not contribute to torsional stability of the fixture design, increasing distortion under compression. This in turn can increase pin binding as the pins try to bend and slide through the compressing fixture envelope. The pins usually used have a flattened crimp trapped between the upper two plates and must be loaded or serviced with the upper plate removed. Pin loading is therefore difficult. The increased diameter in the crimp region limits close spacing of the probe. Finally, the crimp cannot be employed on very fine-diameter pins, as they would weaken excessively.

Figure 41.14b illustrates a significant evolution from Fig. 41.14a. Here the pins are not bent or curved. Shorter pins (3 in.) are sometimes used, providing about the same horizontal translation as in Fig. 41.14a. Deleting the bend significantly reduces pin binding. A retention crimp similar to the previous example is used, relocated toward the bottom of the fixture where the pins are more widely spaced. Pins are loaded from the bottom side, with the lower plate removed. This design still requires disassembly of plates for pin servicing, but the bottom plate is somewhat easier to

reinstall due to the possibility of larger hole sizes. Fixtures are usually rigid as opposed to spring-loaded, reducing friction effects during compression.

Variations of the fixtures illustrated in Figs. 41.14a and 41.14b are produced using a foam-rubber pin retention method. In these versions, the crimp on the pin is deleted and a sheet of foam rubber material is sandwiched between the two lower plates. During loading, pins are forced through this foam, and friction holds them in place. This provides the important advantage that individual pins can be replaced without fixture disassembly. Unfortunately, high-density zones incorporating many pins stretch the foam rubber material. The stretched foam holds adjacent pins so tightly that a group of pins becomes reluctant to move except as an almost solid block. The resulting pin binding effect causes contact reliability and product marking problems. Also, the foam tends to deteriorate with time and/or heavy use. As densities have increased, this fixture has become difficult to use.

Figure 41.14c illustrates a retention technique employing a very thin sheet of drilled Mylar combined with a unique feature on the pin. The Mylar sheet is sandwiched between standard polycarbonate plates. The pins employed begin as straight-sided music wire pins 3 in. long. A grinding operation reduces the pin diameter in a short region (about 0.2 in.) of the pin length. The Mylar retaining sheet is drilled with a hole diameter that is slightly smaller than the original pin diameter. As the pin is inserted, it is forced through this undersized hole until the reduced-diameter zone reaches the Mylar sheet. At that point, the pin can slide freely over the 0.2 in. narrowed length. Only in this region are the pins able to move quite freely up and down. The height of the Mylar plate in the fixture is matched to the reduced-diameter portion of the pin, such that the pin is free to move a short distance up and down from its nominal position without falling out of the fixture. Pins are generally specified with the

grinding operation performed at locations near both ends of the pin, such that the pin is symmetrical and can be loaded without regard to orientation. This pin demonstrates low friction and good contact, but a few problems remain. The Mylar sheet is thin and fairly brittle. It is not uncommon for a particular hole to fracture when extracting or reinserting a pin, such that the damaged hole can no longer retain a pin. Replacing the Mylar sheet requires unloading all pins and removing one or more plates. Pins for this fixture are expensive, as the grinding operation is difficult. The requirement to grind the pin undersize along a portion of its length limits the minimum pin diameter which may be used without causing the pin to become excessively weak at the narrowed section. As product pitch and density demands have increased further, these issues have become significant limiting factors.

Figure 41.14d represents techniques employed in more recently developed fixtures. These fixtures include nonoriented, nonfeatured pin designs, usually 3.75 in. long. A key feature is retention via drilled latex rubber or undrilled spandex cloth. The drilled latex is not sandwiched but rather floats in a gap between two plates, amounting to 0.1 in. or so. Drilling tends to cut or tear a slit in the rubber rather than to cut a round hole. The result upon pin insertion is that the pin is gripped by a pair of tiny rubber flaps, allowing short motions of the pin to occur without actually rubbing the pin against the rubber. (The flaps are able to move short z-axis distances with the pin.) This provides essentially frictionless pin motion over the short range of travel needed to conform to surface irregularities on the product. Properly sized to match pin diameter, the presence of the holes or slits tends to relieve any accumulation of stress in the rubber sheet in high-density areas, providing good contact reliability under such conditions. The lack of motion against the rubber sheet also promotes long life of the fixture. The presence of the hole or slit provides stress relief in the rubber in high-density

situations. Molded one-piece plate spacers speed assembly and disassembly, lower cost, and provide accurate z-axis position control of the plates. Use of the longer 3.75 in. pin provides maximum pin displacement.

The featureless music wire pin is economical and widely available. A countersunk top plate hole or two-ply top plate is generally used for high-performance applications. Notice that no disassembly is required to service a pin.

A variation of this fixture employs a stretchable fabric web in place of the latex, generally referred to as *spandex*. Under close examination, this material appears as a very fine, stretchable net. The stretchable net requires no drilling operation—pins are just pressed through during the pin-loading operation. However, some stress accumulation is observed in very dense areas.

41.3.3.7 Intermediate Guide Plates in Fixtures. Early pin translator fixtures were constructed with only two plates, top and bottom. Modern fixtures add intermediate plates to speed fixture building, produce a more reliable fixture, and make the fixture determined. Determined fixtures ensure that a pin started into a fixture hole during pin loading is able to follow one and only one path through the fixture (without bending). This is required if data-driven test programs are to be used because the test program assumes a specific mapping of grid test points to product targets. The determined pin load must remain constant if the fixture is taken apart and later reloaded; otherwise, the test program will become invalid.

Intermediate plates simplify and shorten the pin-loading process because each pin must fall into the intended track. Assemblers do not have to pick between several possible holes or spend time checking for misloads and/or short circuits. Determined pin loads permit the fixture software to calculate the side loads imposed on fixture plates by the combination of tilted probes in each region of the fixture,

adjusting the pin-loading plan until these side loads are balanced. This prevents the fixture from collapsing sideways under compression. The intermediate plates also support finer-diameter pins, ensuring that they do not buckle under load.

As density increases, holes in the various plates become more closely spaced. At some point, for a given plate stack-up, there is the risk that some pair of holes on the next plate will become close enough that a pin being loaded might fall into the wrong hole. At that density, the fixture software must add an additional intermediate plate to the design. Thus, denser fixtures generally require more plates. Fixture software should analyze the requirements of each fixture and delete unneeded plates.

41.3.3.8 Fixture Plate Spacing Techniques. Errors in the vertical (z-axis) position of fixture plates can result in pin binding. As a tilted pin travels through the plate stack-up, the hole position in each plate shifts slightly in the x and y directions, according to the amount and direction of tilt. If a plate were to be mounted either too high or too low in the plate stack-up, the drilled hole would no longer be at the correct x-y position, forcing the pin to bend in order to pass through the hole. Pins would become difficult or impossible to load; binding and friction would occur during operation. Sensitivity to this problem increases as the amount of tilt increases.

Early multiplate fixtures used a plate-spacing technique referred to as *post and doughnut*, which had mediocre control of z-axis plate position. A long screw passed through a stack consisting of the fixture plates and thick plastic washers. The washers were drilled in the center, and the plates were drilled with corresponding mounting holes. The screw passed through all of these in turn. The thickness of a given washer determined the space between two plates. The problem was that the errors in washer and plate thickness

accumulated through the stack-up. At greater pin tilts, the result was binding. It turned out that the thickness of inexpensive fixture plate material was not terribly precise.

Alternative means of plate spacing have been devised in which a single molded (or machined) part is responsible for the entire fixture stack-up, and which eliminate intermediate plate thickness as an error contribution. One method is illustrated in Fig. 41.15.

FIGURE 41.15 Molded spacer prevents pin binding.

This molded spacer provides a series of flat surfaces upon which individual plates sit. In a top view, the shape of each surface is modified such that plates slip easily over the top of the spacer, but are locked into position when the spacer is rotated 90°. As long as the spacer is accurately molded, no cumulative plate spacing error results. For midfixture plate

supports, a similar part of smaller diameter is used. Short screws at the top and bottom plate secure the support in place. Alternative methods use machined bars around the periphery of the fixture. Either method results in accurate fixtures, reduced parts count, and ease of assembly.

41.3.3.9 Headed Music Wire Pins. For very large through-holes, the preferred probing method is to probe the annular ring of the plated through-hole. If, however, this ring is insufficient, a headed pin may be required. Such pins are manufactured with a machined tip attached to a standard music wire pin. Various head shapes are available. These headed music wire pins work in the fixture design much the same as the headless pin, that is, flush in the top plate (see Fig. 41.16), with the exception that the headed pin must be loaded from the top individually.

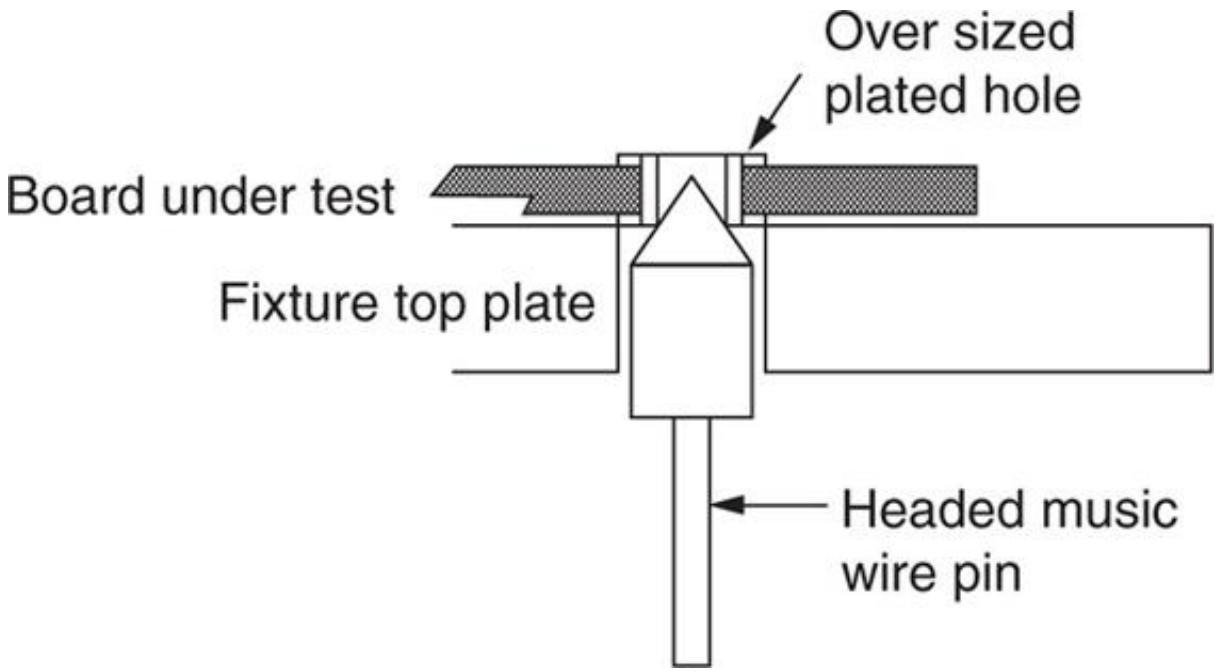


FIGURE 41.16 Headed pin in a tilt-pin fixture.

41.3.4 Dual-Side Testing Considerations

Modern SMT boards often have networks that terminate at component locations on both sides of the board. Continuity testing of such networks requires that the top and bottom terminations of such networks be probed simultaneously. There are three ways to test boards that require dual-side access:

1. Flip test
2. Clamshell upper fixture
3. Dual-side universal grid fixture

These methods vary in terms of test coverage, fixture cost, labor cost, risk of test escape, and required infrastructure. Each method is discussed in the following subsections.

41.3.4.1 Flip Testing. Flip testing is a last-resort method employed where up-to-date dual-side equipment is not available and compromising in test coverage is acceptable. The flip test method requires building either two fixtures, one with the top-side image and one with the bottom-side image, or one fixture with both images on it. The board is then tested one side at a time. Although this does provide partial fault coverage, it does not test those plated holes that link the top-side half of a network to the half on the bottom of the board. This poses a significant risk that bad boards will escape the test process. The problem only becomes worse if these interconnecting vias are tented (that is, if they have solder mask over them), preventing probing. In this case, the traces that run from the tented via to the first pad on the network that can be probed are also untested at both sides of the board.

Flip testing is expensive. Not only are two fixtures built, but also many test points are duplicated between the fixtures.

Much additional board handling and potential for confusion are involved. The cost and risk incurred would likely justify an equipment upgrade to dual-side test capability.

41.3.4.2 Clamshell Upper Fixture. Clamshell testing is another compromise method employed where dual-side equipment is not available. This method provides top-side access through the use of a wired (dedicated) top-side fixture. The method is superior to flip testing in that it can provide complete simultaneous access and full test coverage. However, fixture costs are quite high, especially for top-side test points. In this scenario, a more-or-less normal pin translator grid fixture is built for the bottom side of the board. The board should be oriented such that the busy side of the board faces down, as this minimizes the costly top-side fixture (see Fig. 41.17). Additional test points (called *transfer points*) are added outside the product area on both the top and bottom fixtures, conducting test points from the lower fixture and grid to the upper fixture assembly. Normal wired fixture construction methods are used within the upper fixture to relocate these points to desired top-side product target positions.

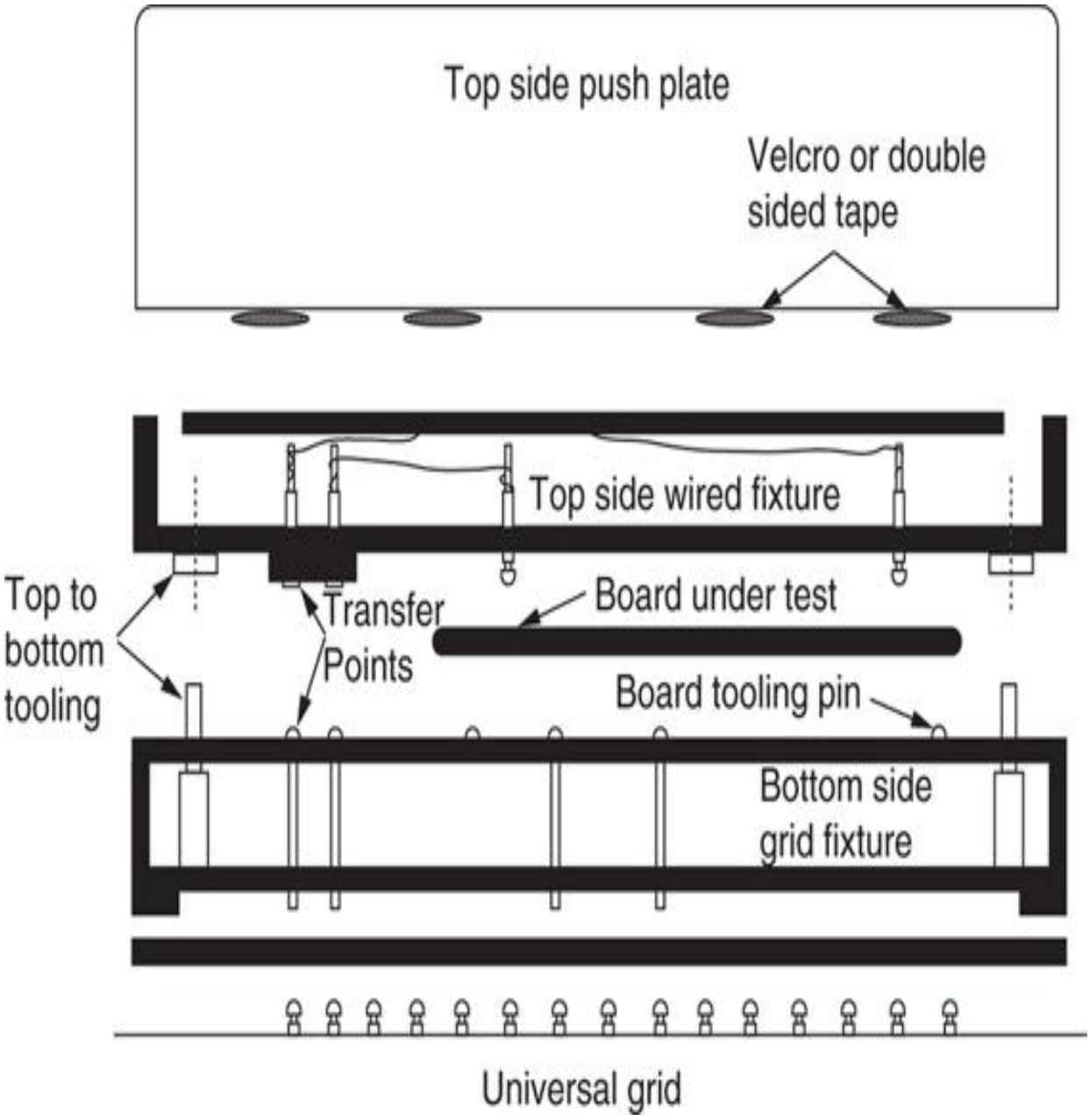


FIGURE 41.17 Transfer point clamshell fixture for dual-side access.

To use this method, it is necessary that the lower grid be larger than the product under test such that a number of transfer test points adequate to provide for the upper fixture can be placed outside the product area. Again, the cost of the extra contact points, spring probes, wiring, and other special material and labor processes associated with the topside fixture may well justify an equipment upgrade.

41.3.4.3 Dual-Side Access Universal Grid. The third and most widely accepted method of providing for volume testing of dual-side product is the double-sided universal grid. Such systems provide electronics and grid probe fields on both the top and bottom sides. Upper and lower translator fixtures are built for dual-side products using the standard techniques discussed earlier, providing economical fixtures, reusable pins and hardware, full fault coverage, excellent throughput, reliable contact, and accurate targeting.

41.3.5 Press Units

The major mechanical component of the grid is a press unit. The three major compression methods used to compress the product onto the fixture are hydraulic, pneumatic, and electric. The total force requirement can be quite large. The spring probes employed in grids usually require a force in the range of 4 to 10 oz. each. A large, complex board may have 20,000 active points per side. This amounts to 5,000 to 12,500 lb. of force, depending upon the probes used.

Hydraulic drive is probably the least used compression method. Although it provides tremendous power, it is difficult to maintain and fluid leakage is a problem. Pneumatic and electric compression are popular and successful. Electric drives are easy to control, but become expensive and/or slow when larger forces are required (as in the case of larger grids). Pneumatic systems are fast and powerful, but require a good supply of clean, dry, compressed air. With any method, accurate compression control is critical to reliable fixture performance.

As noted, universal grids present the test points as an array of spring-loaded contacts. A variety of contact tip shapes have been used, but most contacts used today offer waffle tips.

Waffle tips are nominally flat, but with an *H*-shaped pattern of grooves cut into the surface to provide a somewhat aggressive contact surface. Such a surface is better able to cut through thin contaminants on any surface it contacts.

41.4 FLYING-PROBE/MOVING-PROBE TEST SYSTEMS

Moving probe, flying probe, and x-y prober are all names for test systems that make use of two or more test points that can be accurately positioned anywhere on the board surface by means of a computer-controlled motion system (see Fig. 41.18). Probe tips can be retracted in a z-axis direction away from the board surface, then moved in the x and y directions to a new board location and extended again to make contact. Figure 41.19 shows two probe tips contacting board. Dual-side systems generally provide a minimum of two independently moving probes per side for a minimum total of four heads.

FIGURE 41.18 Flying-probe test system. (*Courtesy of atg Test Systems GmbH*.)

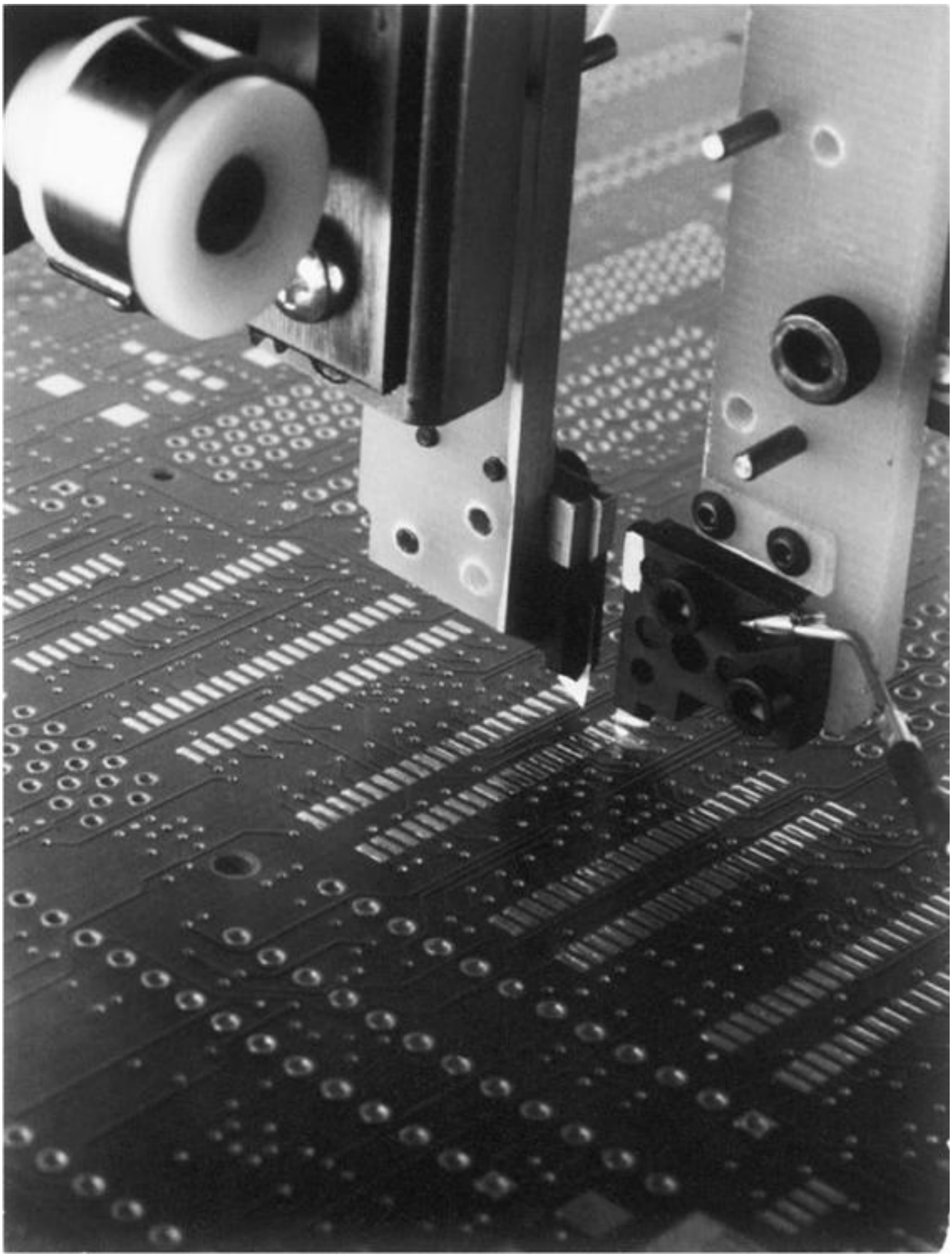


FIGURE 41.19 Two probe tips contacting board. (*Courtesy of Probe Inc*.)

41.4.1 Advantages of Flying-Probe Systems

The major advantage of these systems is elimination test fixtures, making these systems ideal for small-to-moderate volume production. Advanced flying-probe systems provide highly accurate probe placement, and contact the board with minimal force, leaving no discernable witness marks on most surfaces. They are very well suited to testing the finest pad sizes. Although not subject to limitations due to test-point density, these systems do slow down as additional test points are added.

Direct current (DC) continuity test measurements are accomplished by placing one probe tip at each end of the continuity to be verified and performing a measurement. The probes then retract, move to the next measurement site of interest, make contact, and make the next measurement. Similarly, it is possible to perform DC isolation testing of a network by placing one probe (probe A) on the network, while another (probe B) checks all other networks in sequence for the presence of a short or leak. Probe A can then be stepped to the next network to be tested and the process repeated. This continues until each network has been checked against all others.

This requires a huge number of measurements. For a board with N networks, the total number of measurements M required would be:

$$M = (N2 – N)/2$$

For example, a fairly ordinary board with 1,000 networks would require 499,500 measurements. Fortunately, several means of reducing the measurement burden have been developed.

The program preparation software can analyze the conductor pattern on the board and, noting that short

circuits should occur only between physically adjacent conductors, reduce the number of measurements required. This is termed *adjacency analysis*. To achieve further time savings, the testing department might use an indirect measurement method. Please refer to Sec. 41.4.4.

Some indirect methods require only a single probing action of each net, combining continuity and isolation testing with some extra probing to verify any suspect results. Theoretically, our example board with 1,000 networks might have isolation verified with only 1,000 probe placements.

41.4.2 Economics of Flying-Probe Systems

The primary limitation of flying-probe test systems is throughput. Although systems with up to 16 test heads are commonly available, these systems still lose a substantial fraction of the operating time due to mechanical positioning of the heads. Yet the cost savings derived from elimination of direct fixture costs, fixture support infrastructure, fixture debugging, and so on, are substantial.

Accurate comparison of the costs associated with grid and prober methods requires inclusion of all the costs associated with each approach. Common omissions include:

- Labor overhead
- Floor space allocated to fixture storage, materials, and assembly
- Costs outside the test department (such as drilling)
- Stranded investment in completed fixtures, pins, other fixture materials
- Stranded investment in drills and other equipment
- Lost throughput of test systems due to maintenance

- Lost throughput of fixtured systems during fixture setup, debugging, and maintenance
- Peak throughput demand

It is quite possible that, depending upon product mix, a testing department would be made more efficient with a larger investment in capital equipment (in the form of flying probe systems) and a smaller investment in fixtures. With smaller runs and/or smaller lots necessitating frequent fixture teardown/bring-up, this becomes more likely.

41.4.3 Flying-Probe Throughput Enhancement Systems

The tremendous advantages of flying probers for advanced substrates (such as the ability to hit the smallest targets even on large panels, the lack of fixture cost, witness mark reduction or elimination, and fractional ohm measurement) have traditionally been offset by the relatively slow speed of test compared to universal grid methods. As products have included increased amounts of high-density features, test managers find that flying probers are the solution that can reliably contact the smaller features without damaging them. This has provided tremendous motivation for flying-probe manufacturers to find ways to increase throughput.

Recognizing that many of the test targets are easily measured (only a fraction of the sites on most boards presents the majority of the challenge), one new approach uses an extra piece of equipment to prescreen the boards before they are placed on the flying prober, eliminating many of the measurements from the flying prober's task list. This approach is described in this section, with each of the two commercially available models summarized.

In the first case, a row of thousands of regularly spaced sliding contacts moves relative to the board surface,

scanning the surface electrically as a row of scan lines. The contacts are designed to be individually flexible and to apply minimum force, eliminating witness mark concerns for most surfaces. Adjacent to the row of contacts is a planar section of a pliant conductive surface. This surface electrically grounds all exposed conductors on the board that lie beneath any part of the planar area. This conductive plane is fixed in position relative to the row of scanning contacts and extends to within a fraction of an in. of the row of scanning contacts. The relationship is illustrated in Fig. 41.20.

ELIMINATOR
atg
E6

FIGURE 41.20 Flying-probe throughput enhancement system. (*Courtesy of Everett Charles Technologies*.)

As relative motion of the board to the scanning contacts/pliant conductive plane occurs, a high-speed measurement apparatus constantly makes measurements among the scanning contacts and between the scanning contacts and the pliant conductor. For example, if a scanning contact is at one moment making electrical contact at one point end of a network so that another end of the same network is being grounded by the compliant planar surface, then current injected into the scanning contact will fail to increase the voltage of (that is, fail to charge) the network. The pliant planar surface holds the network grounded. Similarly, if two adjacent networks are simultaneously contacted by different scanning contacts, and if at that moment no area of at least one of these networks is grounded by the compliant planar, then it will be observed that at least one of the two networks can be charged to a high voltage and that they must not be shorted together. Software in the prescreening system uses the real-time measurement results to “image” the board and constantly adapt to any shifts in geometry. Thus the system solution is useful for very-fine-pitch substrates appearing in large-panel form.

In a manner similar to the preceding examples, significant portions of most boards may be tested using this apparatus. Some portions of the board usually remain untested, and these measurements are reserved for the subsequent final test by the flying-probe test system. The flying prober also retests and verifies any failures reported by he prescreening system, effectively eliminating most false failures. The resultant speed increase of the combined systems is tremendous, so that true production volumes can be tested. It is important to note that no fixture is required and that both systems provide for true DC measurement of continuity

and isolation. Moreover, because high-density interconnect (HDI) features that are too fine for the scanning contacts of the prescreener are simply passed on to the prober, this solution seems to be appropriate for very advanced substrates.

A second commercially available pre-screening system is very similar, but uses a capacitive measurement made at each time of the finely spaced row of scanning contacts. The overall function is very similar to that just described, except that the alternative of a true DC measurement of continuity and isolation is not provided. For those customers that do not perform such tests with their existing flying probers, this may not prove a significant limitation. For high-reliability applications where DC continuity testing is required the utility of this method may be reduced.

41.5 VERIFICATION AND REPAIR

The test system identifies faults on the board. Assuming that repaired boards are acceptable to the end user and that it makes economic sense to repair boards, a repair process normally follows testing. Because fixture problems, contamination problems, product registration problems, and other issues often result in false error reports, a verification process usually is added between testing and repair. During verification, a technician reads the fault data and makes confirming measurements to determine whether the reported faults are genuine.

If verification of the fault finds that the fault report is valid, the board proceeds through the repair function. If the fault report is not valid, the board may be either retested or directly shipped, depending on customer requirements, in-house policy, etc.

When deciding on a ship-from-verification policy, be mindful of the possibility of multiple defects masking one another (an open hiding a short) or appearing only under the pressure of the fixture. If possible, it may be preferable to perform a complete retest.

In some cases, simple tabletop meter equipment is used for verification, and verification may actually be done at the repair station by the repair technician. More commonly, some form of computer-assisted search-and-display tool is employed. The computer has information concerning the product and test program available, and searches the artwork pattern for areas likely to contain the fault being considered. The resulting risk area is displayed to the operator or superimposed as a visual projection onto the suspect board, simplifying the task of placing meter leads.

Automatic verification may be accomplished by a flying-probe–type system. The flying probe performs a similar analysis, but does the retesting itself and displays a final result. Video camera systems may provide image capture of suspected fault sites, storing the image for subsequent recall at the repair station. Advanced systems may even suggest the repairability of particular fault sites according to user-defined rules.

Figure 41.21 shows an example of a fully automatic verification system and Computer Aided Repair (CAR) station. At the repair station, a display computer similar to that described for verification purposes is used to highlight the proposed repair site to the operator, who performs the appropriate cuts or welds.

FIGURE 41.21 Fully automatic verification system and CAR station. (*Courtesy of Everett Charles Technologies*.)

41.6 TEST DEPARTMENT PLANNING AND MANAGEMENT

In most cases, a new manager inherits a selection of existing equipment, processes, and personnel. Nonetheless, over a period of time, the manager has the same opportunity to shape the test floor operation as does the unlikely individual starting from a clean sheet of paper. To the extent that the past suggests the future, the new manager may expect increased density, finer pitch, higher total test-point counts, decreased tolerance for test escapes, shorter product delivery times, shorter product lifetimes, and larger numbers of smaller batches of boards for just-in-time delivery.

41.6.1 Equipment Selection

Most equipment being purchased for general bare board testing consists of universal grids and flying probers. The increased capabilities of flying probers and increased demand for small lot and prototype testing have increased the number of probers selected. This trend seems likely to continue, but each shop must determine its appropriate solution individually.

A first consideration in selecting equipment lies in recognition of the type of business you anticipate. For very-high-volume production of a variety of part numbers, the universal grid is a likely participant. For medium volumes, considerable savings may result from the elimination of test fixturing costs and delays that can be achieved by combining flying-probe test systems with throughput enhancement systems, as described in Sec. 41.4.3. For prototype or small lot production, a quantity of flying-probe systems may be the best alternative due to the elimination of fixture expense. Dedicated (wired) fixture–type equipment is rarely

demanded due to fixture cost, excepting very simple systems that remain devoted to an extremely high-volume run of a single product type for extended periods of time.

A further important concern is the level of technology that you anticipate. Verify that it does not outrun the capabilities of the fixture or test system types that you plan to use. Plan for change, as the equipment that you purchase must last for several years. Also consider the level of support available from the equipment vendor, including ordinary maintenance service, emergency service, employee training support, and applications support.

For high-volume operations, you can achieve substantial throughput and consistency of operation by adding automatic handling systems to a universal grid system configuration. For prototypes and moderate production volumes, the ability to place a stack of boards on a flying probe system and walk away for an hour or so, rather than wait for a board to come out every three minutes, can result in huge labor savings. Note that some very large, very thin, or very small product types may not be well suited to automatic handling without the use of special carriers or adapters. It may be best to size the automation equipment to handle the major portion of production and leave unusual product configurations on manually loaded equipment.

An often overlooked but practical consideration is maintaining some degree of commonality in equipment and fixtures. It is not uncommon for fixture problems to lead a test engineer to change equipment types several times, resulting in a motley assortment of incompatible (but expensive) test systems but failing to resolve the fundamental underlying issue. With data-driven test processes and automated fault data management in the mainstream, the ability of equipment to share data, fixtures, and operating procedures will decrease cost, increase throughput, simplify training, and enhance opportunities for combinational test solutions. This is harder to achieve with a

random mix of equipment. If this seems to state the obvious, try this experiment: Visit some shops, stopping in drill rooms and in the electrical testing area. Do you see a difference in the assortment of equipment? Department planning should include not only new equipment, but also an exit strategy for old and inefficient equipment that you wish to retire.

41.6.2 Fixtures: Build or Buy, and What Type?

If you plan to use fixtures, the selection of fixtures is probably more important than the choice of equipment on which you choose to run the fixtures. Certainly you must have equipment at least adequate to the fixture, and with sufficient test-point density for the product. This is where a careful evaluation of product technology is crucial.

If the product includes even fairly simple SMT boards, then you should plan immediately for a dual-side capability. If the product includes fine-pitch SMT, dense BGA patterns, and such, then you must consider higher-density universal grids and modern tilt-pin fixtures consistent with the test-site density on these products.

If you plan to build fixtures in-house, recognize that you are creating a complete manufacturing operation. Measurement of complete material, labor, inventory, and overhead costs as well as operating efficiency is critical to effective management of this operation. Don’t just measure how fast you build a fixture, but include measurement of the time it takes to get it running. Consider whether you would be better served by outsourcing fixture fabrication.

Avoid manufacturing multiple styles of fixtures. Ensure that you have an inventory management process that does not run out of pins at midnight, but does not have half a million dollars tied up in obsolete pin inventory. Consider outsourcing at least the more difficult fixtures to specialists.

You may save time, plus gain a partner who provides exposure to alternative techniques and materials.

41.6.3 Selecting Fixture Software

Today’s tilt-pin translator fixture is largely a software product. It should be possible for you to establish a flow of information from your computer-aided manufacturing (CAM) department to the front-end fixture software that automates the design of fixtures and the creation of test programs. (The same goal holds true for processing data to create flying-probe test programs.) A premium tool will pay for itself many times over in reduced fixture scrap, reduced late deliveries, and elimination of test escapes. If you can select a tool that is also used by several fixture outsourcing vendors, you will have a backup supply of fixtures in the event of equipment problems, personnel problems, or workload peaks. If you have special and specific demands for the fixture design, verify that the proposed software package readily supports your requirements. And, as in the case of the test system, evaluate the software vendor’s ability to sustain and support your operations.

CHAPTER 42

HDI BARE BOARD SPECIAL TESTING METHODS

David J. Wilkie
Everett Charles Technologies, Pomona, California

42.1 INTRODUCTION

Printed circuit technology is now being applied to high-density interconnection (HDI) applications that require consideration of new testing techniques. Notable examples include many types of advanced integrated circuit (IC) packaging introduced in recent years, such as area-array devices, ball grid arrays (BGAs), laminate chip carriers (LCCs), and circuit boards employing direct chip attach (DCA) or chip-scale packages (CSPs). In some of these cases, semiconductor dies are being directly attached to a printed circuit surface, and in the case of CSP, the package size is approximately the same as a raw die. Flip-chip die (or CSPs) may be attached to a circuit board by an array of solder balls. Other devices may attach with a peripheral array of wirebond pad sites just outboard of the die area. For

high-pin-count devices, this last example can produce the finest side-to-side test-point pitch as efforts are made to squeeze a large number of contacts onto the limited periphery of the die. The flip-chip or CSP bump array attachment parts generally produce the highest test-point density per unit area. The flip-chip or CSP approaches allow the designer to distribute the solder ball contacts over the full surface area of the die or package. For fixtured test systems, the ability of the tester to provide a sufficient density of test points and the ability of the fixture to achieve the needed pitch and accuracy must be considered.

The general goal of electrical testing for HDI substrates remains about the same—detection of opens, shorts, and leakage, although often with increased concern for latent defects, whose appearance can be made more likely by the fine geometry employed in traces and microvias. The measurement electronics are often the same, and are not further discussed here except for special cases. For some applications, time domain reflectometry (TDR) or other radio frequency (RF) tests are desired, but are complicated by the short signal runs on some of these substrates.

Sensitivity to pad marking is increased as there is not much pad area to mark. Marking that penetrates the metallization layers on the board can affect the chemistry of the solder joint, adversely impacting reliability. It is quite challenging to prepare test fixtures able to test such products on universal grids given the need to minimize witness marks, meet aggressive continuity test threshold expectations, and contact the finest geometries. When HDI parts are tested in panelized form, the very small target sizes combine with potential expansion/contraction issues in the panel construction to place a maximum demand upon test-point positional accuracy within the fixture. The ability of the latest camera-equipped flying-probe systems to locate these targets individually and probe them without

marking combines with the fixture cost savings to make this method of test very attractive, especially as new techniques improve throughput (see Sec. 42.4.3). Because of the high costs associated with HDI fixtures, some fixtured solutions compromise test coverage such that the fixture can be simplified to a practical degree.

42.2 FINE-PITCH TILT-PIN FIXTURES

Many HDI structures can be tested with advanced examples of tilt-pin fixtures. Using such techniques as test pins that taper (see Fig. 42.1) to a very fine diameter at one end, fixtures have been built for devices with pitch down to about 0.010 in., with research and development (R&D) examples at about 0.008 in. These fixtures contain additional plates to support the very thin pins (so they do not buckle under pressure or short to adjacent pins). Those fixture plates very close to the product must be fairly thin, or the closely spaced holes will break out into one another. Such fixtures increase the demand for higher grid densities. These fixtures and pins are moderately more expensive to prepare than standard fixtures, but use similar technologies and processes. Excellent process control is important, as is excellent pin tip symmetry.

FIGURE 42.1 Tapered pin for a fine-geometry fixture.

Areas of the product requiring large numbers of probes are subjected to considerable total force. If no equal and opposing force is applied on the opposite side of the product, bowing or “potato chipping” of the product will occur. Ultimately this can collapse the opposing test fixture, but long before this, the probing accuracy of a fine-pitch fixture will be affected because the product no longer lies in a flat horizontal plane. To avoid this, the fixture software can add support within the opposing fixture, directly opposite the densely probed site. This additional support can be accomplished with a spacer affixed between the top and bottom fixture plates or by using blind pins. Blind pins are ordinary test pins located in the opposing fixture at sites where the top (product side) plate of the probing fixture is not quite drilled all the way through. If a quantity of blind pins equal to the quantity of dense product site probes is employed, then the opposing forces are perfectly balanced in this region.

When dealing with fine-pitch fixtures, the problem of product and fixture registration must be considered. Even if the fixture is manufactured perfectly, the product may not align. Because the tooling features of the product (edge or tooling hole) are added in a process separate from the artwork production, the artwork and tooling features are usually misaligned. With HDI substrates, it doesn’t take much for this error to move pads completely away from the assigned test pins. To overcome this, a variety of test systems are available with optical and/or electrical means of sensing misregistration. Movable plates in the fixture are controlled by servomotors, which reposition the product through motion of the tooling pins. As the product grows in size, or as the manufacturing process deteriorates, the registration errors may not be sufficiently constant over the product area to permit the use of motorized alignment. In

this case, none of the probe-per-pad fixtured approaches may be effective.

42.3 BENDING BEAM FIXTURES

Bending beam fixtures are somewhat similar to tilt-pin fixtures, except that they use extremely thin test pins manufactured from a special alloy. As in the tapered pin fixture, a significant number of thin supports are required near the product, where the pin tends to be held fairly straight to avoid conflict with other nearby pins. These pins are not held rigid, but are expected to buckle under force. This buckling displaces the pin sideways. The buckled portion may be located at some distance from the product plane, where the probes can be more widely separated. Once the pin has buckled, the force applied to move through a substantial travel is constant. This is very different from the case for a spring probe, where the force increases at a constant rate determined by the spring constant. Bending beam fixtures provide good immunity to witness mark damage. The basic technique has been in use in specialty situations for many years.

At the interface side, these pins may mate to spring probes instead contacting a rigid contact surface. In some commercial examples, the pin continues away from the product as a piece of wire routed to widely spaced contacts on the interface portion of the fixture. These in turn interface with traditional spring probes. Within the fixture, the probe wire is bonded in place at some distance from the product, defining the separation between the probe and wiring portions of its overall length. Such fixtures are quite expensive, and replacing damaged probes can be challenging. Thus, this technique is usually restricted to small areas and limited test-point counts.

42.4 FLYING PROBE

The more precise examples of flying-probe systems are very well suited to HDI testing. With on-head optical pattern recognition guiding the probe tips, they can contact extremely small targets—even in the presence of significant product registration problems. They can probe small features without marking or disturbing the surface. These systems can be equipped with true Kelvin contact tips supporting effective single-measurement fractional ohm testing, well suited to the sort of fractional ohm continuity test that may be desirable in efforts to detect precursor phenomena to latent defects caused by cracks or other geometry problems. The principle drawback is, of course, test speed. Used alone, these systems are ideal for prototype or small volume production applications where fixture production would be quite expensive. Used with throughput enhancement systems as described in Sec. 42.4.3, these systems can accommodate moderate production volumes.

42.5 COUPLED PLATE

In a situation where most of the target product is relatively easy to fixture, but a DCA or CSP site is difficult, it may be possible to use coupled plate–type testing. A variety of proprietary products are available, but the basic technique is fairly similar. The primary assumption is that each signal network arriving at the DCA or CSP site is accessible by a traditional probe at some other site on the board. These probe sites are used to perform a normal isolation test of the product. Continuity testing of most of the board is performed in the usual manner also.

To verify the continuity of the signals to the DCA or CSP site, a small metal plate or antenna is suspended just over the site, perhaps insulated from the site only by a thin dielectric. One at a time, the standard probe sites are used to inject some sort of alternating current (AC) signal or pulse into each network in turn. If the network is properly continuous to the DCA or CSP site, then a signal of appropriate amplitude is detected at the antenna. Substantial deviation from the proper amplitude means that something is wrong. The different methods vary in terms of the applied signal, antenna characteristics, and so on.

This method eliminates the need for super-fine-pitch probing at the DCA or CSP site and also avoids marking of the product at this site. However, the test does not perform a true DC test of continuity and may miss high-resistance connections, which would be detected by a low-threshold DC continuity measurement. Signals that loop from one DCA or CSP pin to another and go nowhere else may be untestable as there is no outboard probe site at which to inject the test signal.

42.6 SHORTING PLATE

This method is employed in circumstances similar to the coupling plate method just described. In this case, however, the plate must be movable during the test. Generally, a pencil-sized pneumatic actuator is mounted within the test fixture to accomplish this motion. The plate employed here is a small flat metal plate that is the size of the DCA or CSP site and covered with an electrically conductive rubber (see Fig. 42.2). When pressed against the product, it shorts together all of the pads at the DCA or CSP site. Continuity testing is performed in this condition by using the outboard probe sites to confirm that all of these (otherwise isolated)

networks are shorted together via the path to the DCA or CSP site. All other networks are tested normally for continuity. Then the shorting plate is removed and a normal isolation test is performed. Key advantages of this method are the accomplishment of true DC measurements for both isolation and continuity and the use of standard bare board test systems.

FIGURE 42.2 Pneumatically actuated shorting plate.

In some applications, there is concern about any trace chemicals that may be left behind by the conductive rubber, although outright marking is minimal. Cleanliness of the product is critical, as the rubber or plate must be replaced

when excessive dirt is embedded. As with the coupled plate, certain signal topologies are untestable or difficult to test. Signals that loop from one DCA or CSP pin to another and go nowhere else are untestable, as there is no external probe site with which to verify either continuity (to the DCA or CSP shorting pad) or isolation. Any signal that connects two DCA or CSP pads on the same package may be partially untestable, even if the signal continues to an external probe site. In this case, it is possible to verify that the external signal arrives at the device, and it is possible to verify isolation of this segment. But there is no simple way to discern whether the two device pads are joined to each other. (If they are already shorted together on the board and engaging, the conductive rubber has no effect.) This latter case may sometimes be mitigated by segmenting the shorting pad, such that each of the target device pads is in a separate segment. Then, if the connection on the board is good, the halves will be joined through the board.

42.7 CONDUCTIVE RUBBER FIXTURES

Several designs for fixture systems employing conductive rubber as the basic probe element have been offered commercially. In some cases, the rubber is a specialized material in sheet form and is conductive only in the z-axis (through the thin sheet vertically, but not sideways across its surface). The fixture is itself made from a circuit board, with slightly raised pads to compress the rubber tightly against desired product sites. The fixture board connects to the grid electronics at its reverse side. Other designs have included various types of locally deposited rubber dots, usually of conductive rubber that is not sensitive to orientation. Again, a rubber probe is formed. Problems with

cost, complex manufacturing, complex repair, dirt sensitivity, and suitability to very small pad areas (which limit contact quality to the rubber) seem to have prevented widespread adoption.

42.8 OPTICAL INSPECTION

Optical inspection has been discussed elsewhere (Chap. 30). It is generally applied early in the fabrication process as a yield improvement and data collection tool, not as a means of final product qualification. However, with improvements in resolution, the type of defect that may escape undetected becomes somewhat more limited, and optical inspection is argued as a possible means of final testing.

With complex multilayer product, optical inspection will not be able to identify assembly/contamination-induced defects internal to the board in any case, and may still be limited in cases of contaminants or very fine-geometry shorts and opens on external layers. The equipment is somewhat slower than universal grid test systems, particularly when run at very high resolution. For such reasons, it is still not common practice to employ optical inspection (by itself) as a substitute for electrical testing. This may be a method that develops further in the future or that finds acceptance in special circumstances.

42.9 NONCONTACT TEST METHODS

Quite possibly the greatest daily irritant (and cost) in the operation of a typical test area today revolves around the cost of building test fixtures. Customers still hate to pay for them, and the creation of fixtures burdens the board shop

with an entire manufacturing process that seems to add no value and that distracts from the main productive purpose of the factory. The only fully effective commercially available systems that require no test fixtures are flying-probe test systems and the related throughput enhancement systems. In addition, extensive work has been done by several organizations to attempt to develop alternative noncontact means of fixtureless test. To date, no fully successful noncontact method has yet emerged with a capability for parametric measurement of the normal range of both continuity and isolation, yet some brief description of various techniques seems warranted.

42.9.1 Electron Beam Methods

When a test system contacts a product with an electromechanical contact, it uses this contact to inject or remove electrons. That is, current flows. The sort of electron beam common to the picture tube in a television might be used to do the same thing without contacting the product physically. Experimental systems have been built by several firms to date, but have shared some common problems. First and foremost, the amount of current delivered by the electron beam is so small that only a very poor continuity test is possible. Increased interest in fractional ohm and/or high-current testing to detect latent continuity defects runs counter to this limitation. Lab systems have been limited to continuity thresholds of 100,000 ohms or more, and this only very slowly. As most users wish to test at 10 to 100 ohms, this is a major compromise. (A smear of contaminant across an open circuit would appear to be a perfectly good conductor.)

Test speeds are affected by product capacitance, as a longer time is required for the limited current to achieve significant voltage effect in a highly capacitive environment.

Also, such systems must operate in an extremely high vacuum of laboratory grade. Expensive pumping systems are required. Costly air-lock systems with multiple stages and robotic product handling are probably required to keep any reasonable flow of material through the system. (Staging product in and out through a series of chambers avoids the time delay of constantly pumping down the main chamber when loading new product.) At the present time, flying-probe systems seem to offer superior test and measurement coverage at more practical operating costs.

42.9.2 Photoelectric Methods

Subjecting a metal surface to an intense beam of light, such as that from a laser, can cause electrons to be ejected from the metal. As in the case of the electron beam, a very small current flow can be induced. Again a vacuum is required (so that the ejected electrons can be measured before they collide with air molecules), though the vacuum requirement is less stringent than that for the electron beam technique. The resistance at which continuity measurements can be made is quite limited, as in the case of the electron beam. (See discussion of electron beam method in Sec. 42.9.1.) Again, test speed suffers due to product capacitance. No practical system has resulted from investigative work.

42.9.3 Gas Plasma Methods

Fluorescent light bulbs emit light because a gas is subjected to an electric field, which adds energy to the electrons orbiting the gas molecules until some break free. As they attempt to reattach themselves to the gas molecules, they eject their excess energy as photons (light). The plasma consists of a mixture of gas molecules, ionized gas

molecules (missing electrons), and free electrons. In this state, the gas can conduct an electric current. If a jet of plasma is directed from a small nozzle to the surface of a circuit board, the effect is that of building a “gas probe.” In broad terms, the gas probe can be used just as any other probe or test is completely possible.

Generally a noble gas such as argon is used. The gas residue is nontoxic, only a tiny amount of gas is consumed, and substantial current can flow to the product. Several companies have developed experimental systems in the form of flying-probe systems.

Although gas probes offer the benefit of little or no product marking, it is difficult to achieve one that is as fine as the best mechanical probes. Adjacent jets tend to combine, producing a short circuit just as if two mechanical flying-probe tips shorted while testing. Thus, the commercial system offered to date includes completely traditional mechanical probes as well, using these to probe closely adjacent (i.e., HDI) sites. As a flying-probe mechanism is still used, there is little speed advantage to date. Eventually some benefit may be obtained due to the elimination of any wait time for z-axis travel of the prober head, although this is already the fastest motion axis of most flying-probe systems. The cost of this technique is modestly higher than that of an ordinary flying prober.

42.10 COMBINATIONAL TEST METHODS

One technique that offers immediate practicality in resolving difficult testing situations for high-density product —often using existing equipment—is generally described as combinational testing or sequential testing. As the name

implies, this is testing in one or more stages, using a combination of test techniques. Combining techniques inevitably adds complication. The simplest example is the use of a universal grid to test the majority of a product, followed by a flying probe system to test HDI features and reverify the failures reported by the grid. Software tools have simplified the process of combining test methods.

PART 8

ASSEMBLY, SOLDERING MATERIALS, AND PROCESSES

CHAPTER 43

ASSEMBLY PROCESSES[a]

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

43.1 INTRODUCTION

The electronics “revolution” has been sustained through the development of products having increased miniaturization, enhanced functionality, improved reliability, and reduced costs of manufacturing. In fact, innovations in electronics assembly methodologies have kept manufacturing costs low with each new generation of product.

43.1.1 Feature Density

Product designers have been able to explore new packages, materials, etc., so as to increase functionality further while, at the same time, reducing the size and weight of both consumer as well as high-reliability military and space electronics. The result has been greater challenges for

process engineers. For example, there is a continued trend of decreasing component sizes. Leadless ceramic chip capacitors having sizes of 0804, 0603, and 0402 are commonplace, whereas smaller 0201 devices are being introduced into product lines, particularly handheld products. Manufacturing resources are now developing the means to tool up for 01005-size components. Fine-pitch and area-array packages—ball grid array (BGA), chip-scale packages (CSP), and flip-chip (FC) or direct-chip attach (DCA)—provide the means to increase device functionality significantly. Input/output (I/O) interconnections that are reaching several thousands on BGA packages require stringent solder paste printing, part placement, and reflow processes controls to minimize defects. At the same time, the need for more complex, multilayer substrates has also placed limitations on the process window so as to avoid damage to circuit board microvias and fine traces that are needed to support higher assembly densities. Lastly, these challenges are made more complicated by the use of Pb-free solders. Changing equipment parameters as well as alternative surface finishes impact solderability performance and thus process yields as well.

43.1.2 Printed Circuit Board Assembly Process

There are two basic steps in the assembly of a printed circuit board: (1) placement of the components (resistors, capacitors, etc.) on the substrate and (2) soldering those components into place. Although this is a fairly accurate description of a through-hole, hand-soldering operation, nearly all electronics assembly operations are, in fact, considerably more complex. Multiple-step assembly processes provide the versatility to incorporate different component package types and a wide variety of substrate

configurations and materials as well as to accommodate frequently changing production volumes in order to meet prescribed defect levels and reliability requirements. A more accurate, albeit still relatively general, listing of assembly process steps consists of the following:

- Preparation of the component and substrate surfaces to be soldered
- Application of the flux and solder
- Melting of the solder to complete the joint
- Postprocess cleaning of the soldered assembly
- Inspection and testing

Some of these steps may be either combined together or eliminated, depending on the particular product line.

It is important that the manufacturing engineer and operator understand the critical steps in the printed circuit board assembly process to ensure the manufacture of a cost-competitive, reliable product. That understanding includes both the general function of the equipment as well as the activity taking place *inside* the machines. The following sections of this chapter describe in detail the printed circuit board assembly processes.

43.1.3 Assembly Process Categories

Assembly processes can be placed into the following three categories, which are described by the types of circuit board components:

1. Through-hole technology
2. Surface-mount technology
3. Mixed technology, which is a combination of through-hole and surface-mount components on the same circuit board

Within each of these assembly technologies are different levels of automation that equipment resources offer. The degree of automation will be optimized, depending on the product design, bill of materials, capital equipment expenditures, and actual manufacturing costs.

It is important to remember that through-hole printed circuit boards and their assembly processes remain a critical technology in the electronics industry, albeit clearly not at the same production volumes as experienced before the advent of surface-mount technology (SMT). Through-hole technology may be used because it is the only format available for some components, particularly large devices such as transformers, filters, and high-power components, all of which require additional mechanical support that is offered by through-hole interconnections. A second reason for using through-hole technology is economics. It may simply be more cost-effective to use through-hole components, together with manual assembly (i.e., no automation) to produce an electronics assembly. Of course, through-hole technology is not limited to manual assembly. There are varying degrees of automation that can be used to assemble a through-hole circuit board.

43.1.4 Pb-Free Technology

The introduction of Pb-free technology has not changed, per se, available electronics assembly processes (reflow, wave, hand soldering, etc.). However, it has caused manufacturing engineers to reassess the parameters used in those processes because of two factors: (1) higher process temperatures required by Pb-free solders, and (2) the poorer solderability of these alloys (owing largely to the absence of Pb). With respect to the five general process steps noted previously, the use of Pb-free solders primarily affects steps 3, 4, and 5.

The need for higher processing temperatures limits the assembly “process window” of Pb-free solders. A higher *nominal* temperature is needed to accommodate the temperature variation at components across a circuit board to ensure melting of the solder and adequate wetting and spreading at each interconnection. On the other hand, the maximum temperature must be limited to prevent thermal damage to heat-sensitive devices and the circuit board.

The poorer solderability of the Pb-free solders presents several challenges as well. Although the longer time needed to heat the component lead or termination and circuit board is often cited as the underlying source of poor solderability for Pb-free solders, it is primarily the higher surface tension of the Sn-based alloys (in the absence of Pb) that restricts wetting and spreading behavior. The need for longer heatup times is a particular issue with “faster” assembly processes such as wave soldering and hand soldering. However, the intrinsically poorer solderability impacts all assembly processes because it can degrade the quality of hole fill and fillet development for both short and relatively long (e.g., reflow) assembly processes.

The intrinsic solderability performance of Pb-free solders is being improved by two means. First, new flux formulations are available that more effectively reduce the surface tension of the solder. Second, alternative surface finishes can be specified for the component I/Os and/or circuit boards that improve wetting and spreading activity exhibited by the Pb-free alloys.

Strictly from an assembly process point of view, the mixing of Pb-free and traditional Sn-Pb solder can be beneficial. The Sn-Pb solder can improve the wetting and spreading performance of the Pb-free solder by two phenomena. First, Pb contamination lowers the molten solder surface tension of the solder. Second, the Pb contamination reduces the melting temperature of the Pb-free alloy. However, concerns are raised by the mixing of Sn-Pb and Pb-free solders and its

effect on the long-term reliability of interconnections under thermal-mechanical fatigue environments.

Lastly, the use of Pb-free solders impacts the postassembly cleaning step (step 4) and the inspection step (step 5). The higher process temperatures can produce more tenacious flux residues that require more aggressive cleaning steps to ensure their removal. Also, the more tenacious residues affect the ability of test probes to contact test site pads on the circuit board. Poor contact can be responsible for detecting false opens on the assembly.

43.2 THROUGH-HOLE TECHNOLOGY

Through-hole technology refers to assemblies having components with leads that are inserted into holes in the circuit board and soldered into place. This technology has been used since the early days of electronics (the 1920s). The leap in automation came in the early 1960s with the advent of wave soldering. The particular drawback of through-hole printed circuit boards, which led to the introduction of surface-mount technology (see the next subsection), was low assembly densities. The relatively large devices, and the circuit board real estate required for holes, limited the density of components, which in turn restricted product functionality and further miniaturization. A photograph of a through-hole circuit board is shown in Fig. 43.1 along with an optical micrograph that shows the through-hole solder joint of the component lead extending through the circuit board.

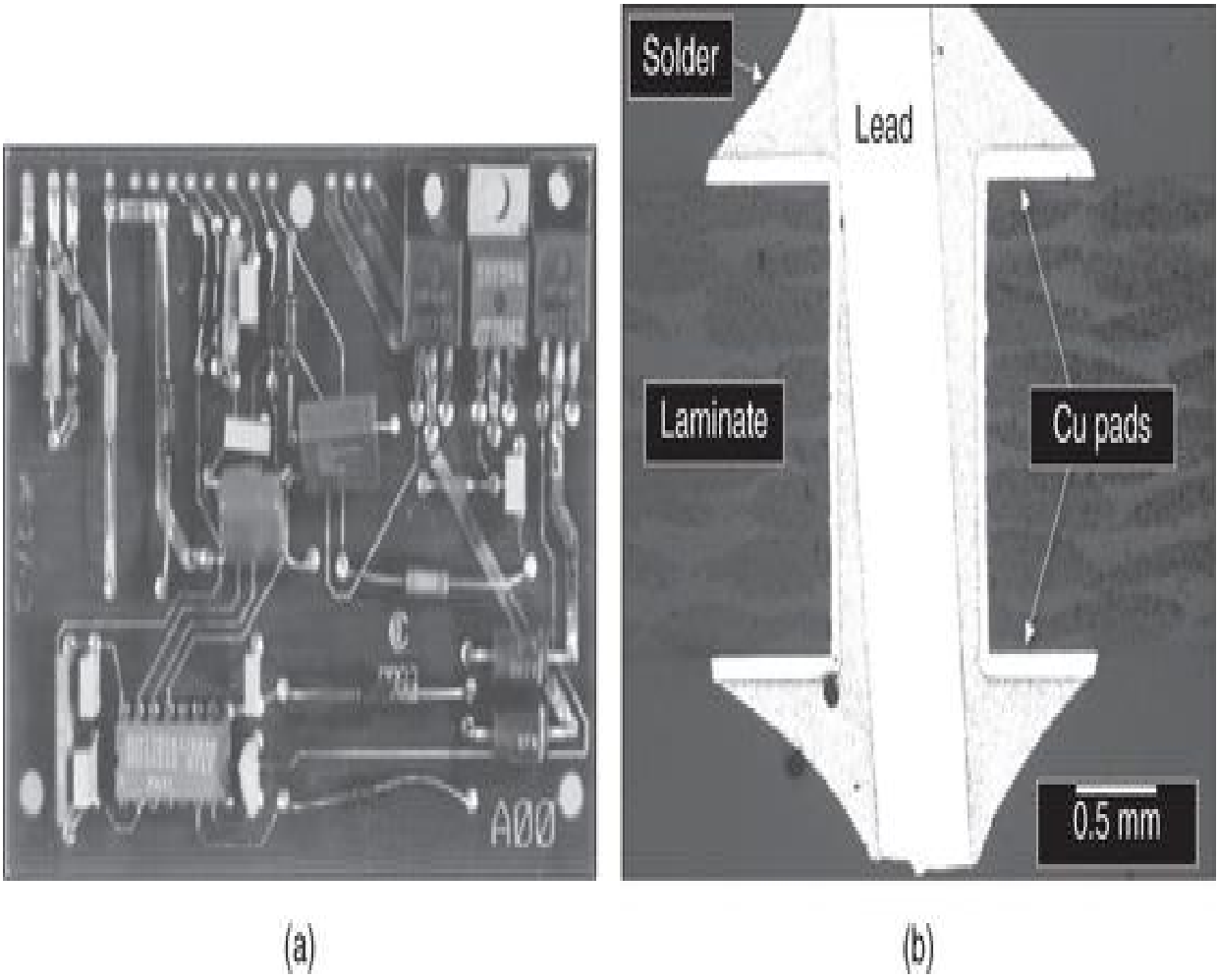


FIGURE 43.1 (*a*) Photograph of a through-hole printed circuit board; (*b*) optical micrograph of the component lead as it is soldered into the circuit board hole. (*Courtesy of Sandia National Laboratories*.)

An advantage of through-hole technology is reduced cost in some applications. That cost benefit may be realized by lower labor costs in some parts of the world that support hand assembly, which is relatively easy with the larger components and products, and lower board densities. Even when fully automated—either by wave soldering, selective soldering, or paste-in-hole/reflow—the capital equipment and manufacturing costs can still be lower than those required for surface-mount assembly.

43.2.1 Impact of Pb-Free Soldering on Through-Hole Technology

The change to Pb-free solders affects through-hole assembly technology. First, there is equipment selection. Manual assembly operations may require purchasing higher-temperature soldering irons. At the other end of the cost spectrum, there are the expenses to replace several hundreds of pounds of Sn-Pb solder with a Pb-free alternative in the pot of a wave-soldering machine. Alternatively, it may be advantageous simply to purchase an entirely new machine to avoid cross-contamination with legacy Sn-Pb operations and/or to have the latest technology that mitigates the higher erosion activity of Pb-free solders on machine components.

The use of Pb-free solders also requires a review of the process parameters. The specific aspects are the higher processing temperature required to use Pb-free alloys and the reduced solderability of these alloys. It has been fortuitous that Pb-free solders, when used in manual (soldering iron) and wave processes, have not required a very significant increase in soldering iron temperature as was first anticipated in the early stages of Pb-free technology development. The added temperature margin was of least concern with manual soldering processes because the localized heating limits thermal degradation to either the component or substrate. Some concern arose in the wave-soldering process because the substrate is exposed to the molten solder bath. On the other hand, paste-in-hole technology that uses a Pb-free reflow process subjects through-hole components and substrates to temperatures higher than those to which they are normally accustomed, thereby possibly degrading them.

The soldering of a through-hole interconnection is also susceptible to the intrinsically poorer solderability of Pb-free

alloys. The higher surface tension of these solders results in a slower flow of molten alloy between the pin and barrel, thereby potentially requiring a longer soldering time. Also, the poorer solderability can result in reduced wetting of the pad and limited fillet formation, particularly on the opposite side of the circuit board to which the joint is being soldered. Some of these solderability issues can be mitigated by changing flux and/or the use of alternative surface finishes (e.g., Au solderable finishes). Both options can reduce the solder surface tension as well as enhance the base material metallurgical reaction, thereby improving solderability.

43.2.2 Design Considerations

The design of a through-hole printed circuit board must necessarily consider currently available equipment and assembly practices as well as the potential for advances in future machines and processes. It is important that circuit board designs comply, as much as possible, with recommendations provided by industry standards, such as those of the IPC Association Connecting Electronics Industries (IPC) and the Joint Electron Device Engineering Council (JEDEC). These recommendations include hole diameters, trace dimensions, and feature spacing. The overriding document is the specific product drawing. Any design deviations from industry standards must be fully considered with regard to how such changes will affect the assembly (process).

The following are important design considerations regarding the assembly process for a through-hole printed circuit board products:

- Tooling requirements (holes, edge clearances, etc.)
- Registration holes (manual alignments or vision systems)
- Component lead-hole sizes

- Circuit board dimensions (length, width, and thickness)
- Size and density of components
- Pb-free solders

Three of these factors are discussed below because of their general role on all assembly processes.

43.2.2.1 Component Lead and Circuit Board Hole Sizes. Designing the correct component lead hole diameters begins by referring to the appropriated industry standard(s) [e.g., IPC, Electronic Industry Association (EIA), etc.]. Hole tolerances must take into account run-out by the drill, etch-back, barrel-plating thicknesses, and the need for a nominal gap of 0.07 to 0.15 mm between the pin and hole to support the capillary flow of the molten solder. In addition, there are added tolerance considerations due to the variation in component lead diameters as well as the positioning accuracy of the equipment.

43.2.2.2 Circuit Board Dimensions (Thickness). The thickness of the circuit board is typically governed by the product design and the number of layers required for signal routing. Thickness has minimal direct impact on the ability of automated machines to accept a circuit board physically. (The same is true of hand soldering.) However, the board thickness affects the soldering process. As thickness increases, it becomes more difficult to supply a sufficient amount of heat to the joint area that allows the molten solder to fill the through-hole completely prior to solidification. Copper layers contained within the laminate, which are used for signal transmission, ground planes, radio frequency (RF) shielding, and power sources as well as layers for thermal management, act as additional heat sinks that can impede the flow of molten solder into the hole.

43.2.2.3 Pb-Free Solders. Design rules and industry standards that have been established are based primarily on experiences with eutectic Sn-Pb solder. Studies are investigating through-hole processes for Pb-free solders. Part insertion, equipment tooling considerations, even paste placement for paste-in-hole technology will be largely unaffected by the change of solder alloy. As noted previously, in spite of the higher liquidus temperature, hand-soldering iron tips and wave-soldering pots will use similar temperatures. The design engineer will have to address the generally poorer solderability of Pb-free alloys, which arises from the higher surface tension of the solder. Flux selection and alternative surface finishes can mitigate this discrepancy to some degree. Other measures may be necessary. For example, the designer may be required to increase the spacing between components in order to avoid solder bridges that cause short circuits during wave and selective soldering. The high Sn content of Pb-free solders results in a greater degree of erosion of the Cu features on the circuit board. This phenomenon is particularly severe at the knee of the through hole when the molten solder is highly agitated such as in a wave-soldering or selective soldering machine. Therefore, it may be necessary to reduce the time that the joint is exposed to the molten solder or to select an alternative Pb-free alloy (Sn-Ag-Ni or Sn-Ag-Ni-Ge) that is less prone to Cu erosion.

43.2.3 Assembly Process

The through-hole printed circuit board can be a cost-effective technology for many applications. One determining factor is the level of automation used to make the product, which can range from hand assembly to fully automated processes (inline or batch). The specific assembly steps include component insertion (also referred to as “board stuffing”),

lead trimming, soldering, and postassembly cleaning. Labor costs, capital expenditures, board design, and production volumes are contributing factors toward determining the details of these steps.

There are two general formats for assembly processes: the cell or batch process and the line process. Both methods are discussed in the following subsections.

43.2.3.1 Cell (Batch) Process. The cell process routes the circuit boards in batches between the different steps. The cells or workstations are not always in immediate proximity to each another and can be entirely manual, semiautomated, or fully automated in terms of the actual process step. For example, component placement may be fully automated, but require several machines for inserting the different component types. Circuit boards are typically loaded and unloaded by hand between machines. Table 43.1 lists the advantages and disadvantages of the cell process. The cell or batch process is best suited for a facility that assembles a high mix of low production volume products (e.g., prototype development or high-reliability circuit boards) where flexibility is necessary on the factory floor.

TABLE 43.1 Advantages and Disadvantages of the Cell Process

Advantages	Disadvantages
• Single machine outage does not immediately stop the entire process line.	• Higher product flow time due to the transfer of parts between cells is unattractive for high volume applications.
• Adds greater flexibility to the process by creating alternative routes.	• Part transfer between cells increases the likelihood of handling damage workflow
• Attractive for high-mix, low volume applications that require frequent equipment change-outs and retooling.	• Difficult to predict product line throughput in a multicell assembly process.

43.2.3.2 Line Process. The second approach is the line process, where the different insertion machines, as well as the soldering process in some cases, are linked together with automatic board-handling equipment. Table 43.2 lists the advantages and disadvantages of the line process line. The line process is best suited for a factory floor where high production volumes (e.g., consumer electronics) and a low mix of product types are typical of the manufacturing operations. Less versatility is required by assembly processes, which justifies the capital equipment expense.

TABLE 43.2 Advantages and Disadvantages of the Line Process Line

Advantages	Disadvantages
• Improved manageability of material inventory, product flow, and operator resources is attractive for high volume, low mix applications.	• Failure or maintenance outage of a singe machine failure can potentially halt an entire assembly line.
• Shorter process times by eliminating the transfer of parts between machines	• Reduced equipment flexibility is unattractive for high mix assembly.
• Reduce the likelihood of handling damage to the assembled product.	• Capital equipment costs and fixed floor space requirements are critical considerations.

The configurations of most through-hole components fall into one of three geometries: axial leaded, radial leaded, and dual inline pin (DIP) packages. These traditional configurations are used for resistors, capacitors, transistors, crystals, and, in the case of active devices, the DIP package. There are also odd-form packages for devices such as transformers, switches, and relays. New package configurations such as the pin grid array (PGA) are being developed to accommodate the increased functionality and further miniaturization of active devices. Besides the actual

component body size, shape, and lead configuration, the other factor that can impact the through-hole assembly process is the lead finish. First of all, the finish can potentially add significantly to the diameter of the lead, which must be taken into account when considering the tolerance budget for the hole in the board design. Secondly, for hot solder dipped leads, the potential accumulation of solder at the end of the lead can interfere with part insertion.

The Pb-free alloys can impact the hand-soldering assembly process. First, the higher melting temperature of these alloys requires a slightly longer soldering time. In the case of hand soldering, tip temperatures designated for Sn-Pb process can be used for the Pb-free soldering of traditional through-hole designs. However, hotter tips and/or irons with a higher power rating may be required for “borderline” designs such as those having bigger component leads or thicker circuit boards. Secondly, the Pb-free solders have a higher surface tension that tends to slow wetting and spreading on surfaces as well as capillary flow into holes. For example, the Pb-free solder may not fully coat pad surfaces on the opposite side of the circuit board. Third, the high Sn content of the Pb-free solder increases the rate of erosion of the soldering iron tip, wave-soldering machine parts, and the Cu features on the circuit board.

43.2.4 Hand-Soldering Process

The sequence of steps used to hand solder a through-hole circuit board varies somewhat between different applications. First, there is part insertion. If the insertion operation is fully manual, the parts will be “kitted” into specific groups: The first group is inserted and then soldered; the second group is inserted and soldered; and so on. The order of the groups is determined so as to maximize throughput as well as to take into account human factors in

order to minimize part error, lead damage, and operator fatigue or inattention. In semiautomated processes, the operator may receive the circuit board for soldering that was partially or fully populated by machine.

Next, there is the soldering step. The location of the joint where soldering is performed depends on the architecture of the circuit board. For single-sided boards without a plated through-hole, soldering must be performed on the component side. On the other hand, in the case of double-sided and multilayer circuit boards with plated-through holes, soldering is typically performed on the bottom side in order to avoid potential heat damage to components by the soldering iron, particularly on densely populated circuit boards.

The hand-soldering process proceeds as follows:

1. The operator applies flux to the joint. The soldering iron tip is contacted to one side of the component lead (see Fig. 43.2). The tip should not contact the circuit board pad, if possible. It may be necessary to contact the pad of thicker circuit boards.

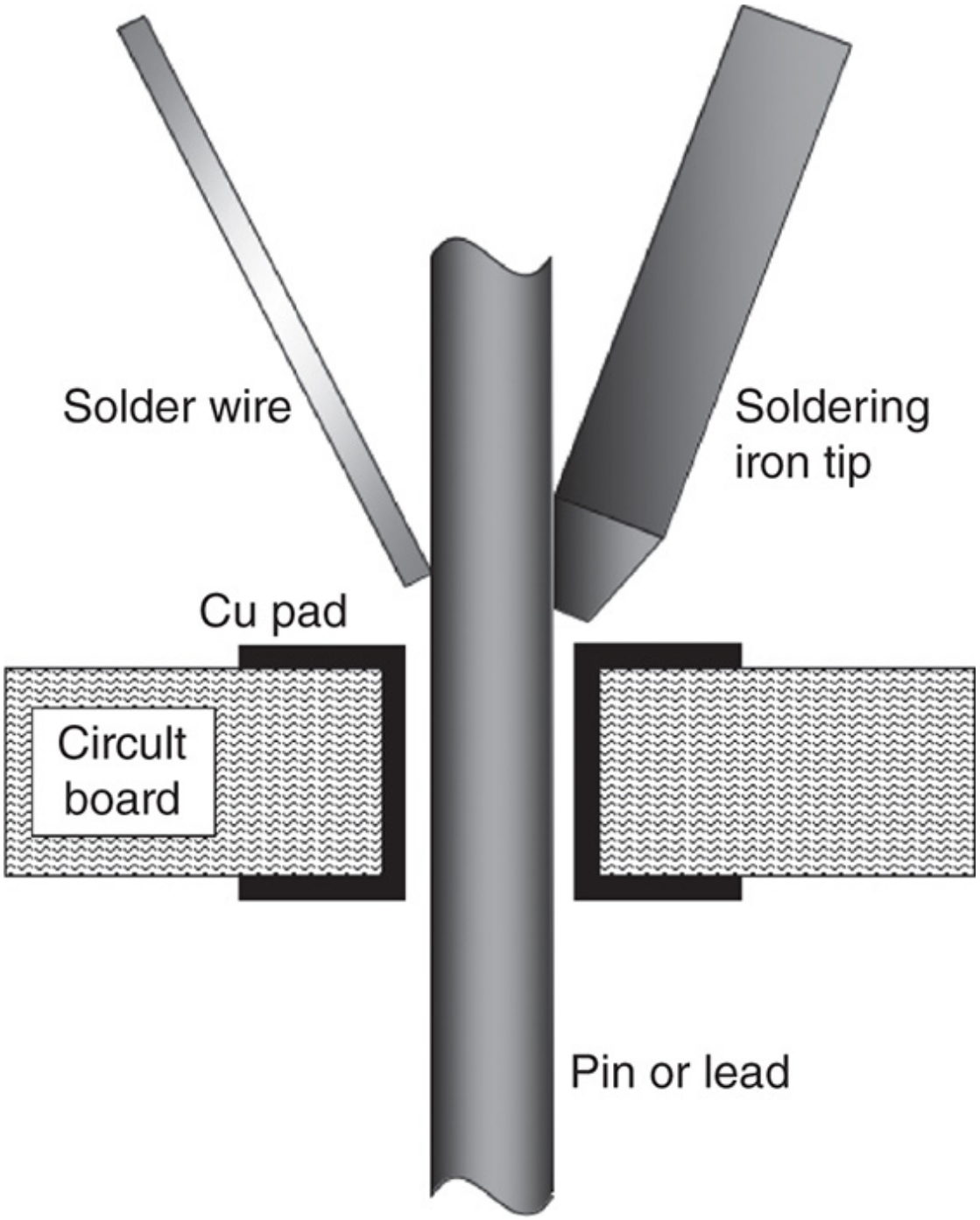


FIGURE 43.2 Diagram showing placement of the soldering iron tip for heating the lead and placement of the solder wire to complete the joint.

2. The solder wire is brought into contact at the side of the lead opposite to the soldering iron tip. The solder wire should not contact the tip in order to melt it. Once melting, the solder is allowed to wet and spread over the

surfaces as well as to flow through the hole. In the case of flux-cored wire, the flux application step is omitted. A properly designed process—that is, one having a soldering iron with adequate power as well as tip temperature and geometry—should complete the joint in approximately 3 to 7 s.

3. Once the soldering process is completed, the circuit board is cleaned of flux residues when required by the flux type or the product's long-term reliability requirements.

Hand soldering may be achieved in an assembly (or "slide") line process for larger volumes. In this case, each one of several operators solders only a few of the total components of the circuit board. In the case of single-person work cells, the operator may solder all of the components to the circuit board. Alternatively, the work cell may be used to add odd-form components as the final assembly step on a nearly complete circuit board.

43.2.5 Automated Soldering and Insertion Technology

In the case of automated assembly processes, the general sequence is part insertion followed by the soldering step. (Slightly different steps are used for the paste-in-hole process; that is, the paste may be applied before or after part insertion.)

43.2.5.1 Components. Part insertion is typically performed in the following order:

1. DIP package
2. Axial leaded components
3. Radial leaded components

4. Odd-form components

The following subsections provide a brief description of each of the component formats and the manner in which the insertion machine addresses those formats.

Choosing the appropriate insertion machine depends on production volume requirements and the mix of products (part density, board sizes, etc.) that must be assembled in the factory. These factors determine the machine's physical dimensions, placement speed, and part-handling (staging) features.

43.2.5.1.1 Dual Inline Pin (DIP) Package. The first autoinsertion process is placement of the DIP packages. The typical DIP package (see Fig. 43.3) is manufactured in one of two widths: 7.6 mm and 15.2 mm. Package lengths vary with the number of pins. For example, a 6-pin DIP package can have the same width and length of 7.6 mm. On the other hand, a 42-pin DIP package has a width of 15.2 mm and a length of 54.6 mm. The DIP packages are typically received in 61-cm-length plastic tubes. The insertion machine carries these tubes vertically in magazines. The part shuttle selects the appropriate package and carries it to the center of the machine for insertion into the circuit board. Tooling on the shuttle head holds the package by the leads during the insertion process. The tooling is simply scaled for different DIP package dimensions.

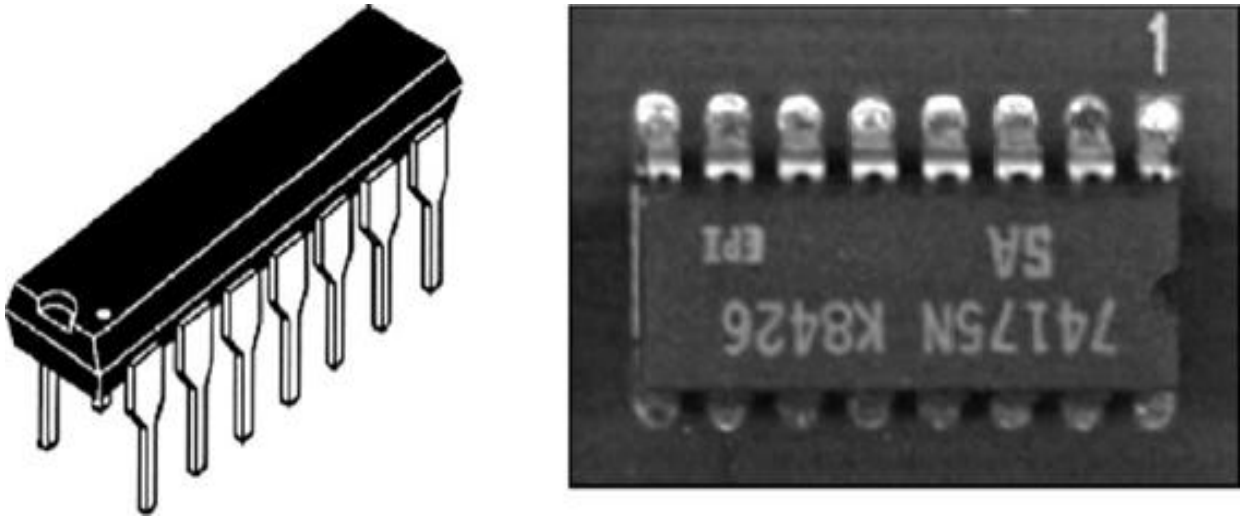
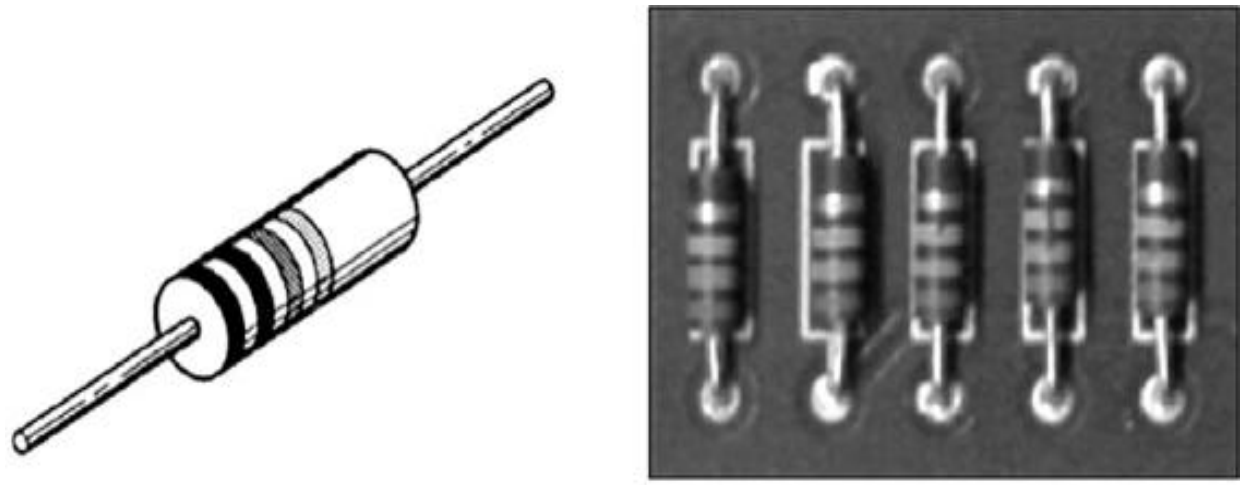


FIGURE 43.3 Dual inline package (DIP). (*Courtesy of Sandia National Laboratories*.)

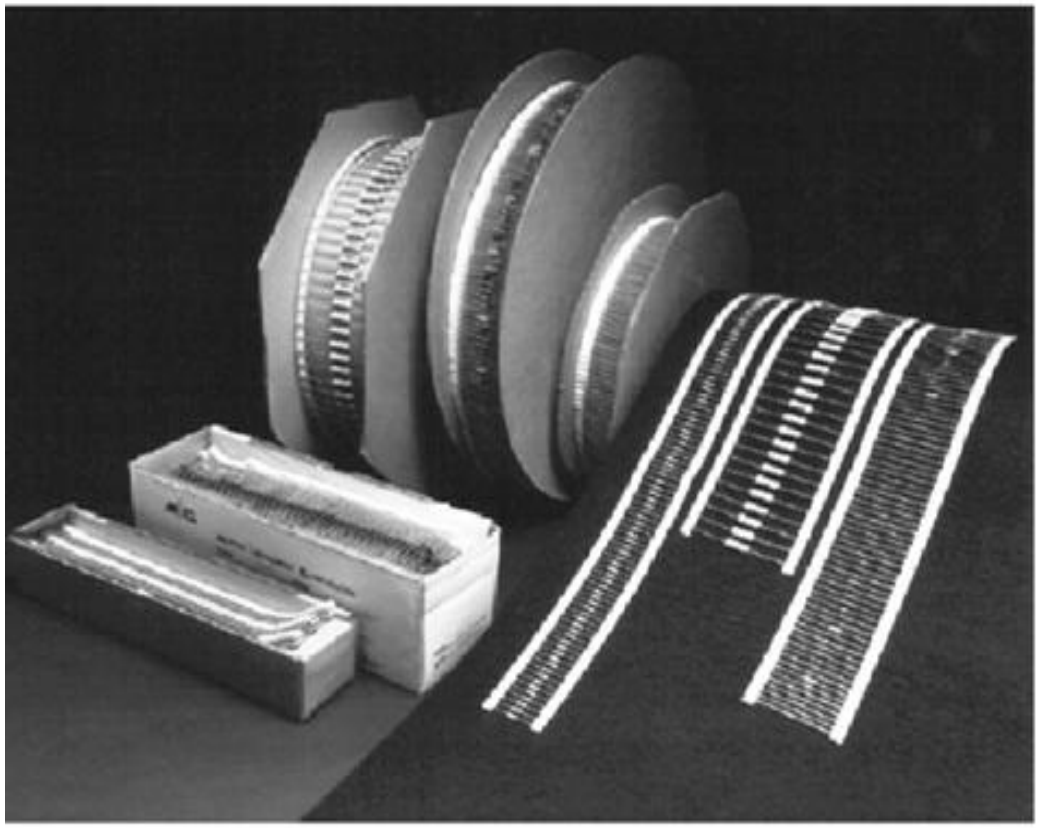
Dual inline packages are either molded plastic (PDIP) or ceramic (CerDIP, or just CDIP). The surface finishes on PDIP packages are typically electroplated layers of Ni (solderable layer) and Sn-Pb (protective finish) over a Cu lead frame. The Sn-Pb finish is being replaced with 100 percent Sn layers to meet environmental requirements. The CDIP package has low-expansion Fe-based alloy leads that are either electroplated with Cu finish for solderability or the alternative lead finish of Ni (the solderable layer) followed by Au (the protective layer). Although the DIP package is rarely received from the manufacturer with a hot-solder-dipped coatings, these coatings may be applied, after-market, to prevent Sn whiskers with 100 percent Sn finishes (PDIP) or Au embrittlement with Au finishes (CDIP). Aside from potential hole interference with a hot-solder-dip coating, there is also the need to unpackage and repackage the components, which can potentially damage the leads as well as add to the overall cost of the assembly process.

43.2.5.1.2 Axial Leaded Components. Following the DIP packages is insertion of the axial leaded components, which are taped together at the leads by the manufacturer to prevent damage. The taping of the leads conforms to EIA

specification number 296-E. Examples of axial leaded devices are shown in Fig. 43.4. During the insertion process, the machine cuts the axial components from their tape to ready them for sequencing into the shuttle head. The leads on axial devices are typically copper or a Cu-clad, Fe-based alloy material. Electroplated Sn-Pb or 100 percent Sn coatings are used to preserve lead solderability. Hot-solder-dipped coatings (Sn-Pb or Pb-free) may be increasingly encountered as a replacement for 100 percent Sn coatings, especially for high-reliability applications. The coating thicknesses must be considered when determining the tolerance stack-up between the hole and pin. Also, hot-solder-dipped coatings often lack uniformity, increasing in thickness near the end of the lead where molten solder accumulated prior to solidification.



(a)



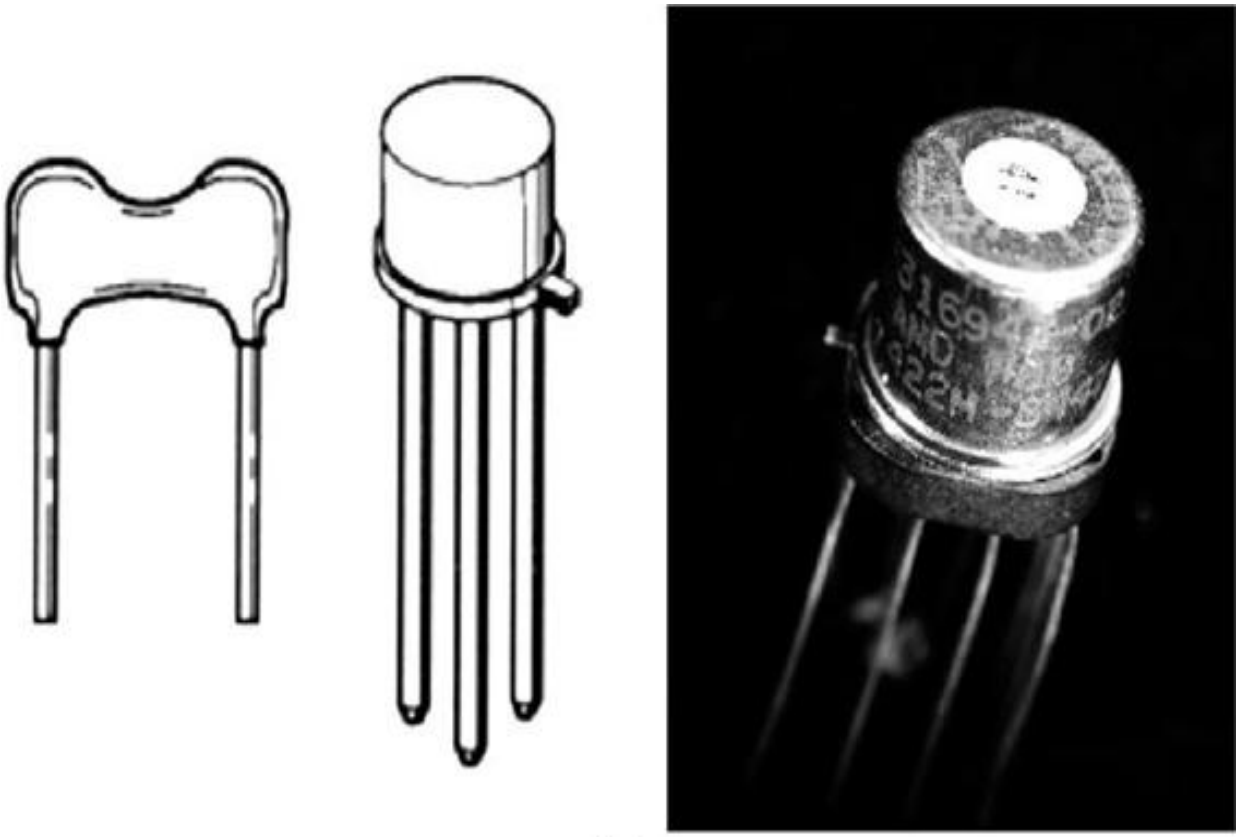
(b)

FIGURE 43.4 Examples of axial leaded devices: (*a*) axial leaded components; (*b*) axial leaded components in reels and boxes. (*Courtesy of Sandia National Laboratories*.)

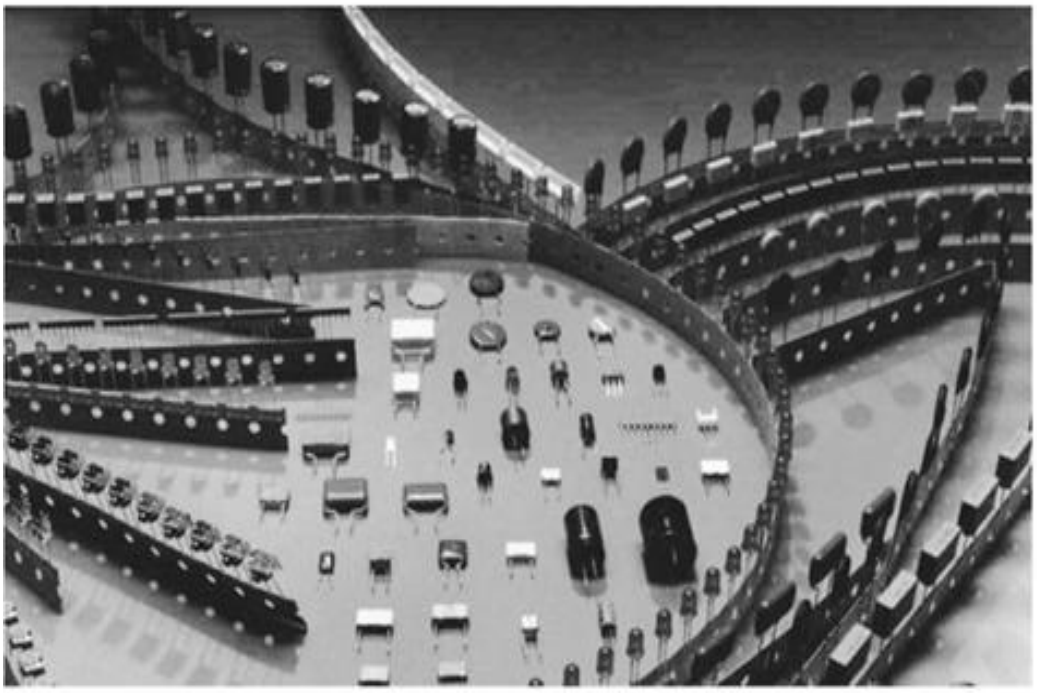
Choosing the appropriate insertion machine depends on production volume requirements and the mix of products (part density, board sizes, etc.) that must be assembled in the factory. These factors determine the machine's physical dimensions, placement speed, and part-handling (staging) features.

Axial leaded components are inserted before radial leaded components because, typically, axial components are smaller overall than radial components. Because the associated tooling size is also smaller, inserting axial components prior to the radial components facilitates the stuffing of higher-density circuit boards.

43.2.5.1.3 Radial Leaded Components. After DIP and axial leaded components, the radial components are inserted into the circuit board. Radial components can vary greatly in size, shape, height, and weight (see Fig. 43.5). The lead finishes—types and thicknesses—are identical to those of axial leaded components. The possible exceptions are hermetically sealed components, such as active Si chip devices in TO-5 cans, optoelectronic packages, and relays. Such devices typically have low-expansion, Fe-based alloy leads that allow for them to be sealed into the header with a glass-to-metal joint. Although some device manufacturers use a Sn-Pb or 100 percent Sn finish over an electroplated Ni (solderable) layer, other suppliers prefer an Au (protective) finish over the Ni (solderable) layer to provide adequate solderability. In such cases, the Au layer is removed by hot solder dipping in order to prevent Au embrittlement of the circuit board interconnection.



(a)



(b)

FIGURE 43.5 Radial leaded components: (*a*) individually; (*b*) in taped reels. (*Courtesy of Sandia National Laboratories and Universal Instruments*.)

Radial leaded components are taped together at the leads. Radial insertion machines remove the components from the tape and insert them in sequence on to the printed circuit board using a shuttle system similar to that used for other components. The insertion machine tooling for radial components is designed to avoid previously inserted DIP and axial components.

43.2.5.1.4 Odd-Form Components. The odd-form components are the last devices to be assembled on the circuit board. Odd-form components, by definition, are those packages that are not readily addressed by automated assembly because (a) they are used at insufficient volumes on the product to justify machine "space" or (b) they are of a geometry (shape or size) that lacks the customer demand to justify the machine manufacturer to provide off-the-shelf tooling for them.

High-power applications often require a variety of odd-form components, including simply oversized DIP, axial leaded packages, or radial leaded packages. Also, odd-form components include transformers, switches, relays, and connectors. Several of these packages are shown in Fig. 43.6. Unusual package sizes and geometries are often accompanied by unusual lead configurations and materials. It is not uncommon to have Cu- and Ni-based alloy leads, or even leads made of refractory materials such as Mo and Ni. The leads may be round, square, or in the form of ribbons. Irrespective of the lead material or nontypical geometry (which must have the hole geometry addressed at the circuit board design step), it is *always* required that the leads have adequate solderability. Leads are typically plated with solderable layers (Cu or Ni) and protective finishes (Au, Sn, Sn-Pb, etc.) very much like those used on traditional components to support the soldering process.

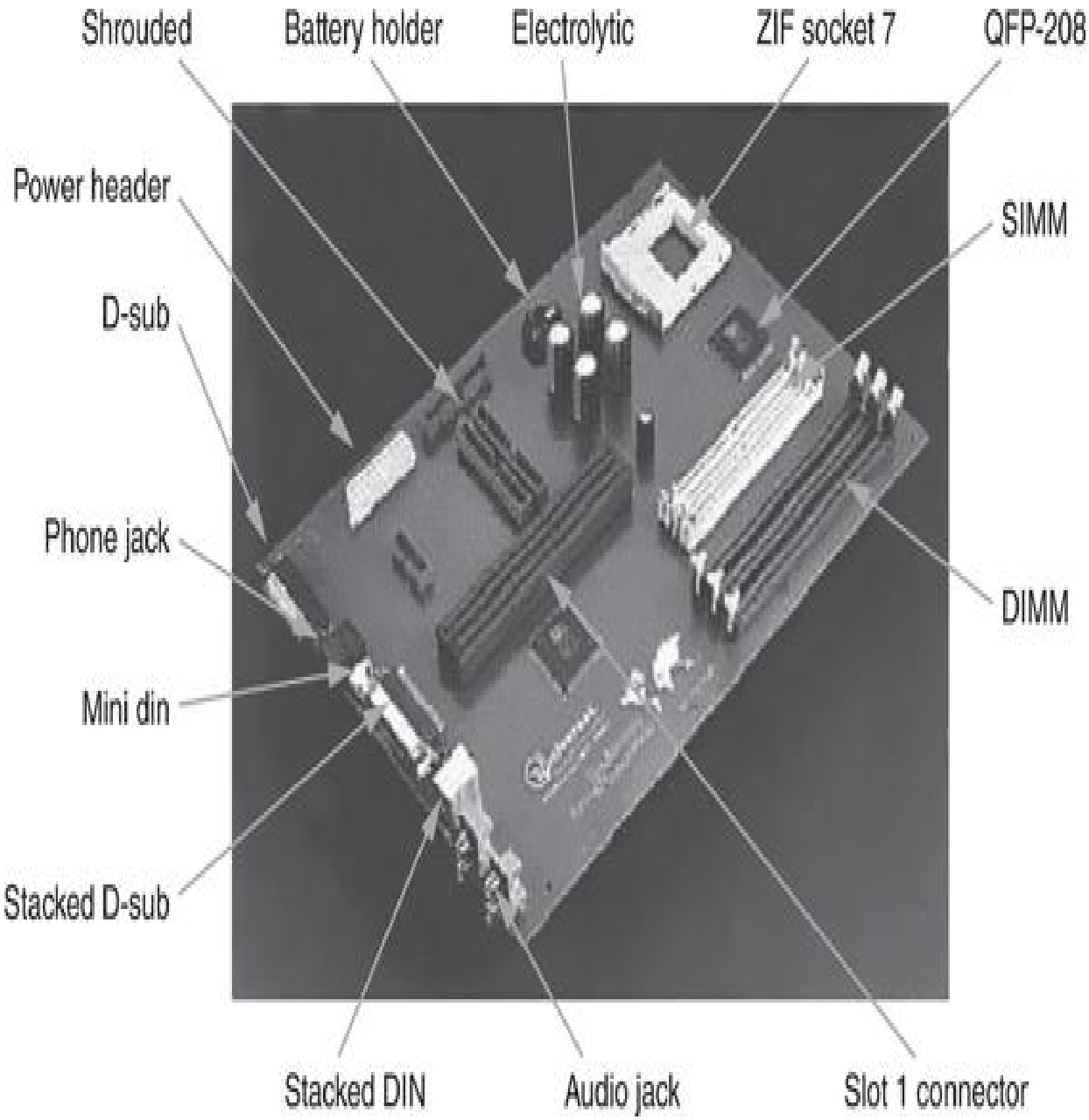


FIGURE 43.6 Examples of odd-form, through-hole components and a circuit board assembly. (*Courtesy of Universal Instruments*.)

43.2.5.2 Insertion Equipment. Because the demand for through-hole circuit boards has remained strong, insertion equipment capabilities have steadily improved. Brushless servo-motors and state-of-the-art motion controllers and sensors have replaced most pneumatic drive assemblies and bulky (and slow) mechanical switches and relays,

respectively. Some equipment options include the capability to test parts electrically prior to insertion. At insertion rates of up to 40,000 components per hour (CPH), defect rates are a couple of hundred parts per million or lower for the common axial and radial leaded packages. Interchangeable tooling has allowed the automated insertion of many odd-form components, as well. The change to Pb-free solders does not have a direct impact on insertion equipment technology.

43.2.6 Automated Soldering and Wave Soldering

The most commonly used process for the soldering of through-hole and mixed (through-hole and surface-mount) circuit boards is *wave soldering*. The wave-soldering process is shown schematically in Fig. 43.7. The populated (or “stuffed”) circuit board is secured to a conveyor belt. The conveyor belt carries the board through the fluxer, then the preheat stage, and lastly on to the molten solder wave.

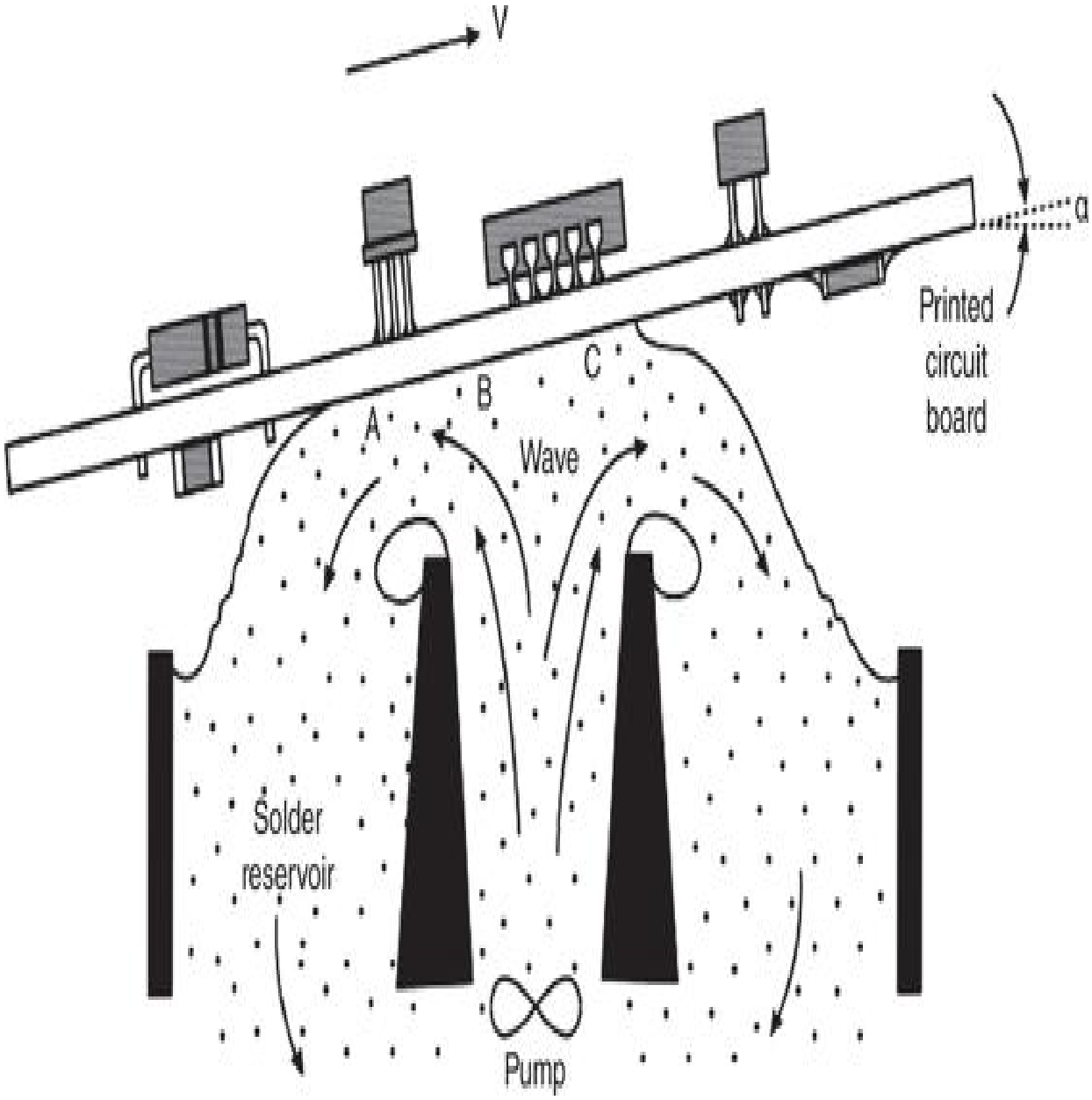


FIGURE 43.7 Schematic diagram showing the wave-soldering process.

Interestingly, one of the most critical steps in the wave-soldering process is the application of the flux. Manual fluxing has given way to more precise, automated equipment in order to improve yields. The advantage is better control of the *quantity* of flux on the circuit board as it enters the wave because the flux controls both the entry and exit geometries of the molten solder wave, which in turn are instrumental toward minimizing skips, bridges, or icicle

defects. Flux can be applied by spraying techniques or by passing the circuit board through the foam or “suds” of the flux. The latter technique is provided by the “foam fluxer.”

After the fluxing step, the circuit board passes through the preheat stage, which is comprised of a set of radiant heaters. As the circuit board is heated, this step evaporates volatiles from the flux coating (which if not adequately removed can lead to voids and blow holes) and activates the chemical reactions between the flux and oxides on the component lead or termination and the circuit board conductor.

The solder wave is created by pumping molten alloy upward through a nozzle, where it exits to a certain height and then falls back into the bath. The solder bath temperature is 260°C for eutectic Sn-Pb solder. The printed circuit board is carried by the conveyor so that is passes over the surface of the wave. The bottom side of the circuit board contacts the wave, allowing the molten solder to wet the exposed pads as well as to flow upward through the holes by capillary action. The speed of the conveyor and the take-off angle—that is, the angle at which the circuit board approaches the wave—are critical parameters for minimizing wave-soldering defects.

Another critical parameter of wave soldering is the wave geometry. The schematic diagram in Fig. 43.8 shows the commonly used dual wave. The first wave is turbulent so as to counteract the surface tension of the molten solder, thereby literally forcing the molten solder into confined geometries in order to initiate the wetting process. The second wave is smooth or laminar. The laminar wave is located at the exit point because its geometry reduces the propensity for bridges and icicle defects to form as the molten solder retracts itself from the circuit board. The photograph in Fig. 43.9 shows a circuit board entering the turbulent wave of a dual-wave soldering system.

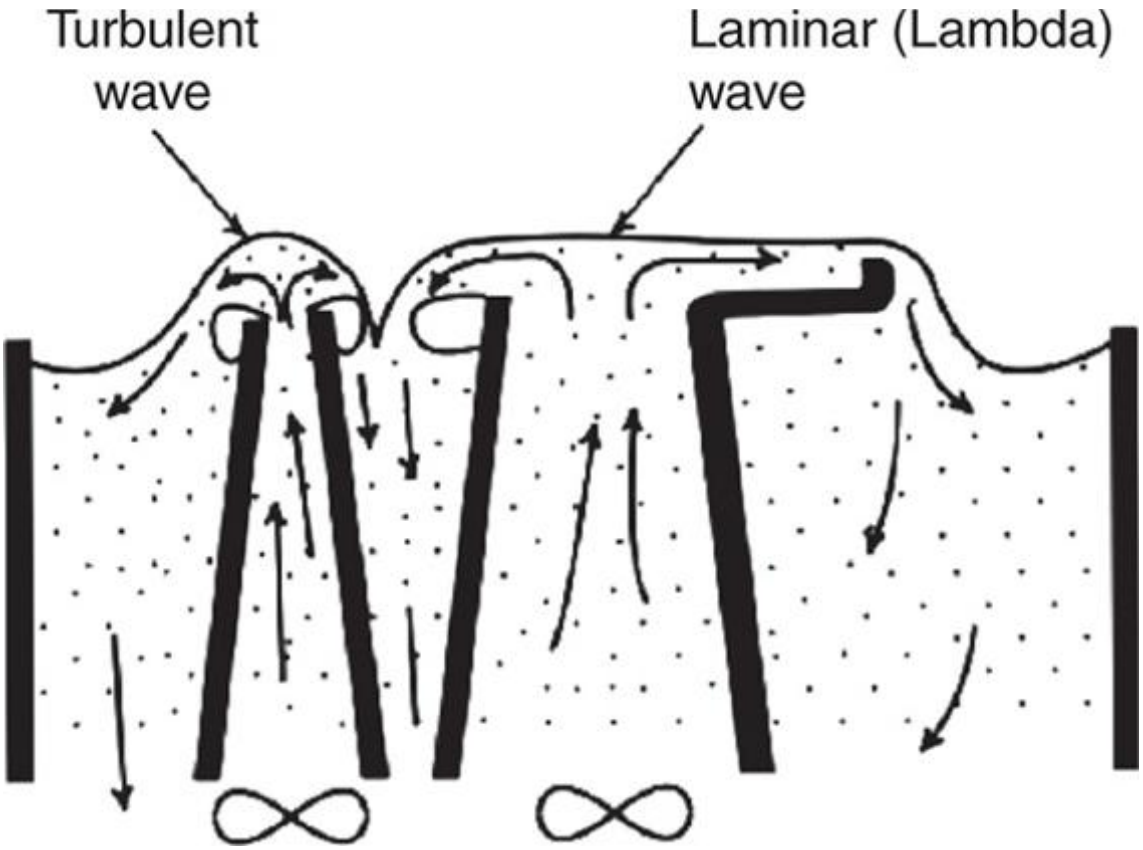


FIGURE 43.8 Schematic diagram of the dual solder wave configuration.

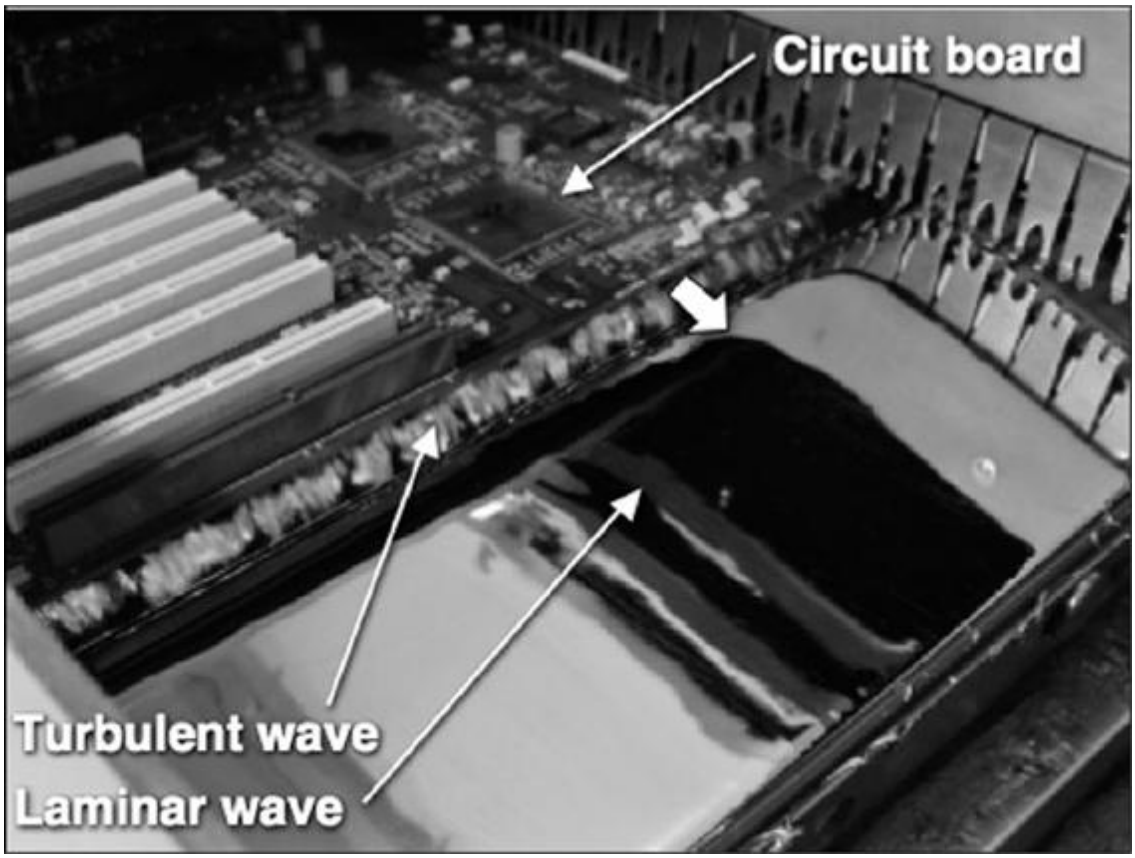


FIGURE 43.9 Photograph of the dual-wave configuration. (*Courtesy of Vitronics-Soltec*.)

A variation of wave soldering is the so-called selective soldering process. Instead of using a long wave to accommodate the dimensions of an entire circuit board, a small fountain is created of molten solder. The reduced geometry allows for the soldering of individual components or several components on only selected areas of the circuit board. A manual operation is used to apply flux and preheat the circuit board prior to the actual soldering process.

The change to Pb-free solders has affected the wave-soldering process. Fortunately, the 260°C bath temperature used with eutectic Sn-Pb solder has proven to be adequate for most applications using the 99.3Sn-0.7Cu (wt. percent) and Sn-Ag-Cu alloys. Some users have preferred to raise the pot temperature to 260 to 270°C. The elements Ni and Ge have been added to the Pb-free solders in order to provide

the shiny fillets that inspectors are accustomed to observing with Sn-Pb solders. The higher surface tension of the Sn-based, Pb-free solders increases the tendency for opens, bridges, and icicles to form as the circuit board exits the wave. A change of flux chemistry as well as adjustments to the take-off angle and conveyor speed have been used to minimize those defects. Lastly, a particular problem with Pb-free wave soldering is erosion of the machine parts by the high-Sn alloy compositions. Special coatings are put on the impeller, nozzles, baffles, and bath walls to mitigate the erosion process.

43.2.7 Paste-in-Hole (Pin-in-Paste) Soldering

Very rapid production volumes are realized with inline surface-mount assembly processes. In general, the surface-mount assembly process consists of three basic steps: (a) screen printing of solder paste, (b) pick and place of components, and (c) reflow of the solder paste. To obtain similar throughputs for through-hole circuit boards, paste-in-hole soldering is being investigated as an alternative to wave soldering. Solder is provided to the joint in the form of a paste, using screen or stencil printing, or dispensed from a needle. The component is then inserted into the hole. In some applications, the parts are inserted into the circuit board and subsequently the solder is dispensed at the hole using a needle and pump. Then the assembly is sent through the reflow furnace. The primary hurdle with paste-in-hole soldering is supplying a quantity of paste that is sufficient not only to develop a fillet on that side of the joint, but also to fill the hole and, optimistically, create a fillet on the bottom side of two-sided and multilayer circuit boards.

A second concern for paste-in-hole soldering is the temperature sensitivity of the through-hole components.

Recall that in wave, selective, or even hand soldering, the temperature rise is confined largely to the leads and circuit board. At worst, the component package materials experience only the preheat temperature environment. However, in paste-in-hole soldering, components must withstand the soldering temperatures within the reflow furnace. Therefore, a conversion to this solder process requires an in-depth review of the allowable temperature range for all of the components.

43.2.8 Cleaning

The final step in the soldering process is the removal of flux residues from the completed circuit board. No-clean fluxes, as the name implies, produce residues that need not be removed from the assembly after soldering. The corrosive activators are locked up in a hard, polymerized residue. However, no-clean flux residues can potentially interfere with in-circuit testing (probes) and inspection, degrade cosmetic appearance, inhibit rework activities, and lessen the adhesion of conformal coatings. In the event that any one of these factors becomes critical, it is best to switch to a cleanable flux than to develop a cleaning process for a no-clean flux.

Low-solids fluxes (which are not to be confused with no-clean fluxes) are simply formulated with reduced solids content so that very little residue is left on the circuit board. Low-solids flux can be successfully used in wave-soldering and paste-in-hole processes, thereby eliminating the need for a cleaning step. However, they are somewhat more difficult to use in hand-soldering processes because the higher temperature of the soldering iron tip can cause premature loss of the activating agent, resulting in poor solderability.

The cleaning step can be performed in either a batch or inline machine. The optimum equipment is determined by production volumes, floor space, and capital expenditure costs. Smaller, batch cleaning (or “dishwasher”) machines are very cost-effective for overall batch-type processes (e.g., hand soldering) as well as for circuit boards assembled in low production volumes. Inline cleaning equipment is placed at the end of the soldering assembly line to accommodate high production volumes. Whether batch or inline equipment is used, an equally important consideration is selecting the type of cleaning solution. Solvent-based, aqueous, and semiaqueous cleaning materials are commercially available that meet environmental regulations and provide adequate efficacy for the removal of flux residues.

The impact of Pb-free soldering on the cleaning step depends on the particular assembly process. By virtue that the same pot temperatures are used in Pb-free wave soldering as are specified for Sn-Pb solder, there is no added thermal degradation to the flux residues that would cause them to be more difficult to remove from the circuit board surfaces. Such degradation may be observed, albeit to a limited extent, with hand assembly due to slightly longer soldering times. Thermal effects are potentially most significant with paste-in-hole soldering because of the increased temperature settings of the reflow furnace required to melt Pb-free alloys.

43.3 SURFACE-MOUNT TECHNOLOGY

Surface-mount technology refers to assemblies that have components soldered to pads on the surfaces of the circuit board. Components may populate only one side (single-sided) or both sides (double-sided) of the circuit board. Surface-mount technology dates back to the 1960s, when it

was developed for hybrid microcircuit (HMC) assemblies for which it was difficult to put holes into the ceramic substrates. The advent of surface-mount technology for laminate substrates, though, is relatively recent (c. 1980). The advantages of surface-mount technology include smaller components and greater board densities. The large holes have been replaced by small vias for signal conduction between sides and internal layers. Finer traces and reduced component heights also contribute to increased circuit board miniaturization and functionality. Surface-mount circuit boards are shown in Fig. 43.10.

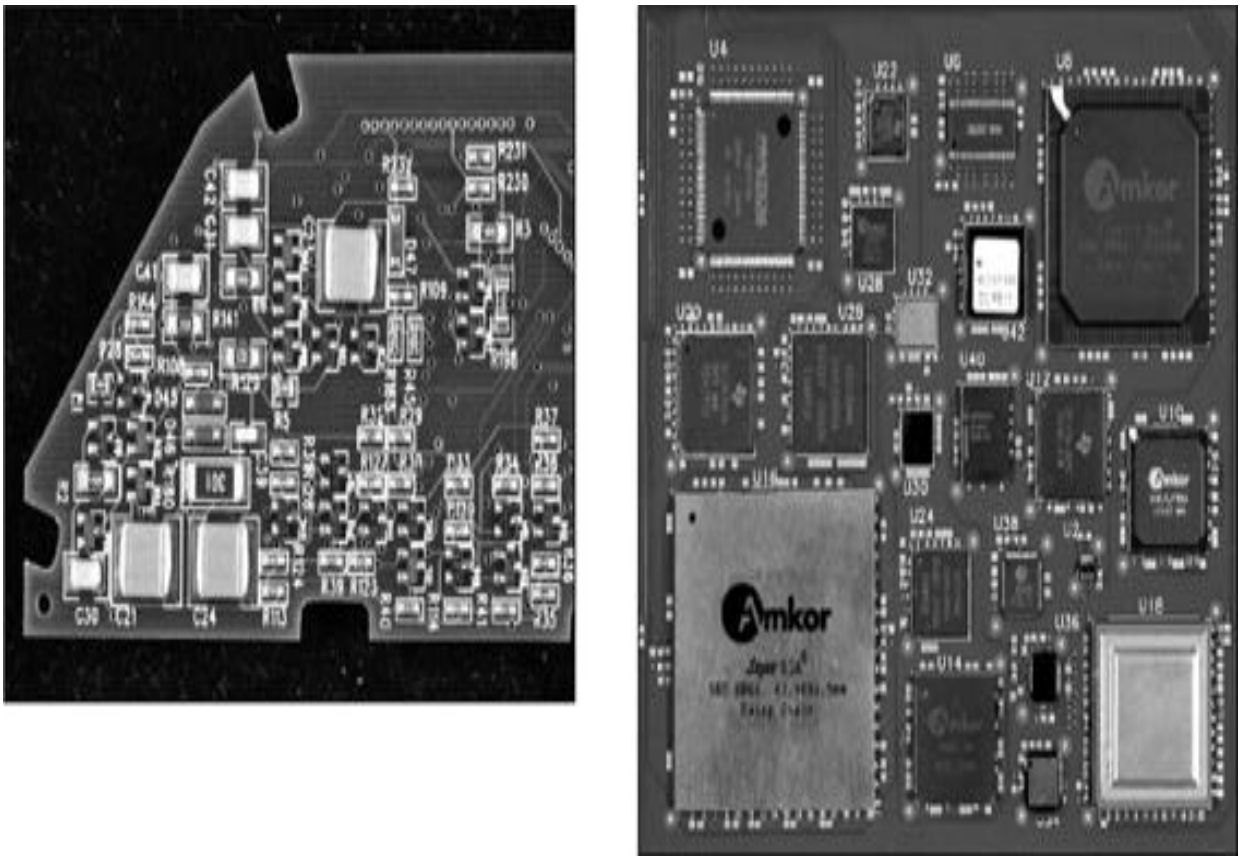


FIGURE 43.10 Surface-mount technology circuit boards showing the range of passive and active device sizes and geometries. (*Courtesy of Sandia National Laboratories and American Competitiveness Institute*.)

The trend in surface-mount technology is to use smaller passive devices such as capacitors, resistors, and inductors.

Also, there is the use of embedded passive devices, that is, resistors and capacitors that are located within the circuit board laminate. Embedded passive devices free up additional surface area for larger, active components.

Active devices are experiencing two opposing trends. On the one hand, memory components (RAM, SDRAM, etc.) are becoming smaller as more transistors are being packed on to the silicon chip. On the other hand, microprocessors and application-specific integrated circuits (ASICs) are becoming larger because of increased functionality on larger chips. Both trends have seen a shift away from peripherally leaded packages to area-array packages. Area-array packages include BGAs and the smaller counterparts, those being CSPs and DCA/FC technology. Examples of peripherally leaded and area-array packages are shown in Fig. 43.11. The advantages of the area-array technology include a reduction of the component footprint by eliminating the leads that extend from the package. Also, fewer assembly defects results from damage to the fragile leads during packaging, transportation, and part placement on the circuit board.

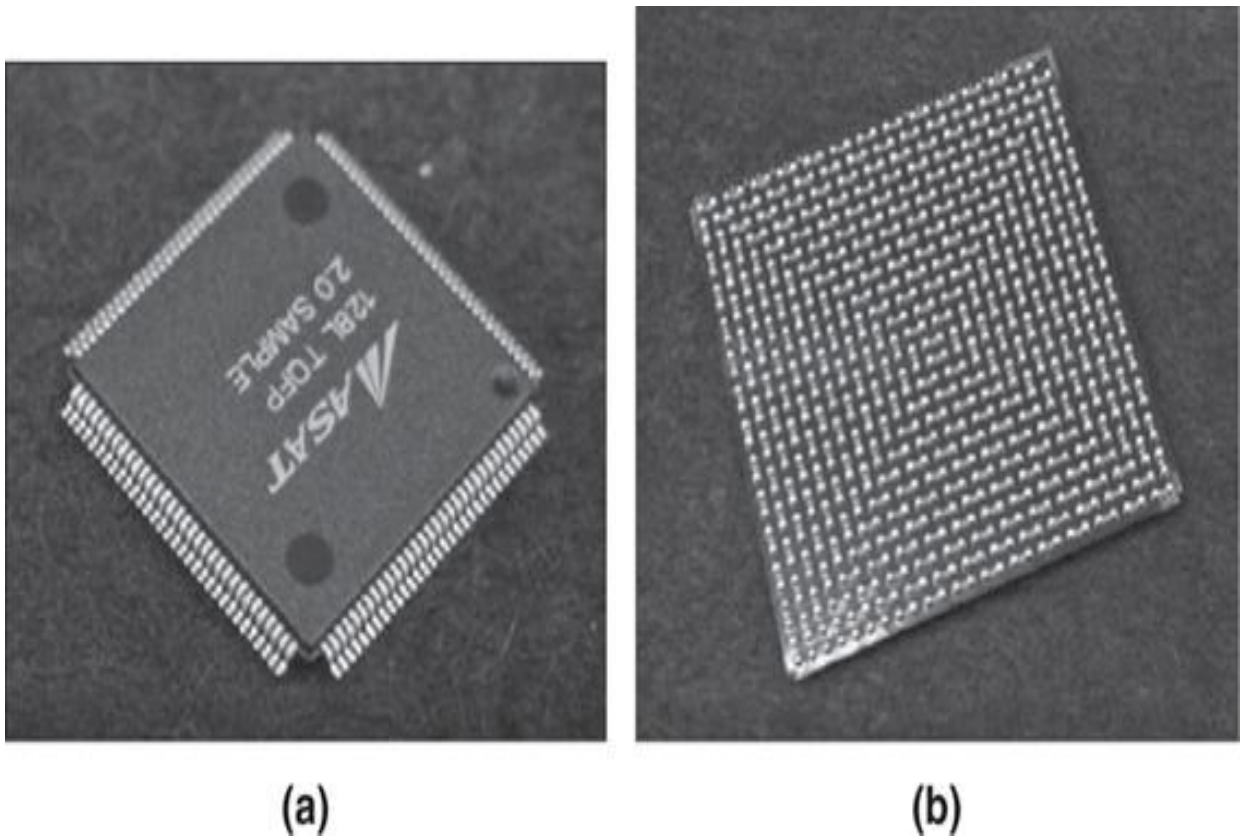


FIGURE 43.11 Photographs of (*a*) peripherally leaded and (*b*) area-array surface-mount packages. (*Courtesy of Sandia National Laboratories*.)

At the inception of area-array technology, the size and pitch of the I/Os were initially higher when compared to what was then 0.4 mm and 0.5 mm fine-pitch, peripherally leaded packages. However, as I/O counts have increased with the functionality of area-array packages, solder ball size and pitch have decreased significantly, particularly when taking into account DCA technology.

Increased device functionality and further miniaturization, which have resulted in higher board densities, are placing stricter requirements on circuit board technology. Increased internal conductor layer counts result in the need for thicker laminates. Whereas once the 1.58 mm board thickness was the norm, now 2.29 mm is commonplace, with many products requiring thicknesses greater than 2.54 mm. The internal conductor layers are being designed to carry not

only the electrical signal, but also contribute to thermal management by removing excess heat from active devices. Similarly, the vias within the laminate are used to transmit signals between layers and the surfaces as well as remove excess heat from large active components (e.g., microprocessors, ASICs, etc.). Vias are reaching aspect ratios (length/diameter) of 8:1 to 10:1, which is nearing the fabrication as well as reliability limits for these structures.

A particular advantage of surface-mount technology is the lower manufacturing cost resulting from automated assembly processes. Solder paste, which is the combination of solder metal powder, flux, and thixotropic agents, is applied in highly controlled amounts (thickness and area) using screen or stencil printing as well as dispensing techniques. Pick-and-place machines handle even the smallest components, locating them precisely on the solder paste deposits (or “bricks”). The tacky nature of the flux component in the paste keeps the components in place. The assembled (or “stuffed”) printed circuit board then passes through the convection/radiation reflow furnace or vapor phase (or condensation) reflow oven to melt the solder. The machines responsible for the steps—paste printing, component placement, and reflow—are connected by conveyor belts to create the inline process. In fact, the final step—cleaning the circuit board—may also be a part of the assembly process sequence.

Of course, various levels of automation may be considered, depending on production volumes and capital expenditure costs. However, with continued miniaturization of surface-mount products as well as the strict requirements for the repeatable placement of specific solder paste volumes and accurate placement of components, it will be a foregone necessity to assemble surface-mount technology with a fully automated assembly process.

Mixed technology refers to the combination of surface-mount and through-hole components on the same printed

circuit board. The lack of components in a surface-mount package is nearly always the reason for using a through-hole counterpart. In general, the surface-mount devices are soldered first to the top side of the circuit board using a convection/radiation reflow furnace or vapor-phase soldering machine process. (Surface-mount is performed first because the through-hole components would interfere with solder paste printing and pick-and-place steps.) The through-hole components are then soldered to the board. The actual soldering process is performed at the bottom side. For larger numbers of through-hole components, the board is wave-soldered. If there are surface-mount components located on the bottom side, they can likewise be wave-soldered; however, those components must first be secured in place by an adhesive. Hand soldering may be preferred if there are relatively few through-hole devices or if bottom-side surface-mount devices cannot be exposed to the solder wave.

43.3.1 Pb-Free Soldering

Pb-free soldering technology has affected surface-mount technology. Fortunately, the fallout has not included the need for new automation equipment. Lead-free solder paste behaves essentially the same as its Sn-Pb counterpart in the printing process. Slight modifications have been suggested for the screen and stencil apertures to accommodate the reduce solderability of Pb-free alloys once the paste enters the reflow furnace. Pick-and-place equipment can remain unchanged by a Pb-free soldering process. Reflow furnaces must be able to accommodate the higher process temperatures required by Pb-free solders. Vapor phase reflow machines are available with fluids that provide the higher process temperatures needed for Pb-free assembly. (As noted earlier, significant equipment costs are associated with altering a wave-soldering machine for the Pb-free

assembly, which would pertain to mixed-technology printed circuit boards. Those costs include the replacement of the solder as well as the replacement of some components that are susceptible to erosion by the high-Sn alloys.)

The most significant impact of Pb-free technology is in reflow process parameters, specifically the time-temperature profile. Longer times at higher reflow temperatures increase the likelihood of thermal damage to components and substrate materials. Also, in seeking to reach higher reflow temperatures, one must also consider the sensitivity of the solder paste to the temperature ramp-up rate. An incompatibility between the paste and time-temperature profile can lead to increased levels of defects such as voids, solder balls, short-circuits due to paste slump, etc. Similarly, excessively fast cooldown rates from the higher reflow temperatures can result in board warpage and cracked passive devices. The greater need to control the Pb-free time-temperature profile favors greater control capabilities for the reflow furnace.

The Pb-free solders have intrinsically poorer solderability performance than their Sn-Pb counterparts. The slower rate of wetting and spreading is not as critical of a factor in reflow surface-mount assembly as it is the faster wave- and hand-soldering processes. However, the higher surface tension of Pb-free alloys may limit the extent of solder spreading on a pad, particularly with bare Cu, leaving the corners uncoated by solder. The choice of flux and use of alternative surface finishes can mitigate this artifact in some cases. A high surface tension also increases the likelihood of *tombstoning* by passive devices particularly for the smaller chip resistors and capacitors. The degree of tombstoning can vary from the device having one termination just lifting from the pad to the component standing up completely on one end.

43.3.2 Design Considerations

The design of a surface-mount circuit board requires the consideration of three factors pertaining to the assembly process. First, there is a wide variety of solder-joint configurations for the different package types. Second, higher board densities can lead to upward of several tens of thousands of solder joints being fabricated at one time. Third, component miniaturization, as well as the unexposed solder joints of area-array packages, further diminishes the viability of performing repair or rework activities to correct solder-joint defects. A number of design rules are printed in documents (e.g., IPC SM-782 and D-330) that govern the size and location of bond pads. Surface-mount circuit boards are at least double-sided and, in most cases, multilayer, so that board design also must consider the interior of the laminate where vias are placed to conduct signals between the layers and surfaces.

Assembly requirements also place constraints on the circuit board layout. A very high part density requires a large number of apertures in the solder paste stencil, which can cause the stencil to become locally too flimsy to control the solder paste deposit. A surface-mount circuit board with a very wide range of component sizes and package configurations may require multi-thickness stencils to properly control the paste deposit. Solder paste printing quality is a determining factor in solder-joint defects observed after the reflow process.

The layout design of the surface-mount circuit board is a factor in the optimizing of the time-temperature profile used in the reflow process. Two important factors are overall thermal mass of the circuit board, determined primarily by the board thickness and number of internal layers as well as the variety package sizes and materials that can lead to temperature gradients as large as 20°C between the smallest passive devices and larger ball grid array packages over the board surface. Also, double-sided circuit boards require two reflow processes. Therefore, larger components

should be placed on the side of the circuit board that is soldered last. If placed on the first side to be soldered, large packages may fall off of the board when the circuit board is upside down for the second side’s soldering step, unless those devices are secured in place with an adhesive or “staking” compound.

The design of a printed circuit board for Pb-free assembly must consider the same points as are considered for Sn-Pb technology, but with a greater emphasis placed on the effects of higher process temperatures—for example, temperature gradients between components across the circuit board. Foremost, there are the enhanced temperature gradients that may be created across a large circuit board having a high mixture of different component sizes and shapes. In the case of a mixed-technology product, there may be limitations placed on the maximum substrate thickness due to the less-solderable Pb-free alloys. It may also be necessary to limit via aspect ratios (typically remaining less than 10:1) to prevent immediate damage (defects) by the reflow process or a loss of long-term reliability.

43.3.3 Assembly Processes

The basic assembly process sequence for surface-mount technology is (1) solder paste printing, (2) pick and place of components, and (3) reflow of the solder. The assembly process is complicated when through-hole components are combined with surface-mount devices on the same circuit board; this is the previously mentioned mixed technology. In general, hand assembly of surface-mount boards is not always practical given the small size of passive devices and hidden solder joints of area-array packages. The use of hand soldering for repair and rework activities is limited by these same factors.

This section lists the sequence of process steps for the different circuit board categories. The term *top side* has typically referred to the side with the greatest density of components and/or where the larger, active device packages are clustered together. As the functionality of printed circuit board products increases, these physical distinctions between the two sides have become less obvious. Therefore, the circuit board sides are simply given a designation: A or B.

Single-sided (top side), surface-mount only:

- Print paste
- Place components
- Reflow solder paste

Double-sided, surface-mount only:

- Bottom side, print paste
- Bottom side, dispense adhesive for larger components, if necessary
- Bottom side, place components
- Bottom side, reflow solder paste and cure adhesive

Flip the board over to the top side:

- Top side, print paste
- Top side, place components
- Top side, reflow solder paste

Double-sided, mixed technology (with bottom-side wave soldering):

- Bottom side, dispense adhesive for surface-mount components
- Bottom side, place surface-mount components
- Bottom side, cure adhesive

Flip the board over to the top side:

- Top side, print paste
- Top side, place components
- Top side, reflow solder paste
- Top side, insert through-hole components

Keep the top side facing up:

- Wave-solder the through-hole and the bottom-side surface-mount components

For mixed-technology products, there is some flexibility regarding the sequence of staking (gluing) of bottom-side components versus the topside soldering step, based largely upon the capabilities of the pick-and-place equipment.

In the case of area-array packaging technology having solder balls (BGA, CSP, and DCA), there is the option of *not* adding solder paste to the pads. Instead, only the flux is deposited on the pads, which serves to tack the package in place during transport of the board to the reflow oven. The solder balls provide the solder to complete the joint; however, the penalty is a reduced gap thickness that may affect self-alignment during soldering (as well as solder-joint reliability later on). Omitting the solder paste is most often considered for the DCA/FC assembly process because the solder balls, and the corresponding pads, are so small that it is not possible to print the acceptable quantity and dimensions of the paste consistently.

There is also the use of step-solder processes for double-sided, surface-mount-only circuit boards. A high-temperature solder, often the 96.5 Sn-3.5 Ag (Sn-Ag) alloy (Teutectic = 221°C), is used to attach the bottom-side components. These solder joints do not remelt when the topside joints are made using the Sn-Pb solder (Teutectic = 183°C). Somewhat tighter process control is required, since the 221°C Sn-Ag eutectic temperature is very near the optimum, peak process temperature for the Sn-Pb process (210 to 220°C). This

approach provides the option of placing larger passive and active components on both sides of the circuit board without the need for an adhesive dispensing and curing step. Unfortunately, the use of the higher melting temperature, Pb-free Sn-Ag-Cu solders all but eliminates this step-soldering approach without identifying a higher melting temperature solder for the first step.

The following sections examine each of the steps in a surface-mount assembly process, beginning with an examination of component types. The different dispensing technologies are reviewed, including those for solder paste and adhesives. Component placement machines are examined, followed by a description of the use of the various heat sources such as convection/radiation reflow ovens, wave-soldering equipment, condensation reflow apparatus, hand soldering, and conduction soldering. Lastly, cleaning processes are described.

43.3.3.1 Components. A wide variety of components are available for surface-mount printed circuit boards. The form, size, and materials used for these components change constantly as new offerings are made by suppliers to meet miniaturization, functionality, and reliability requirements. The most common surface-mount components are the passive or “chip” devices—the resistors, capacitors, and inductors. Chip capacitors and resistors are often referred to by a four-digit number, such as 1825, 1210, or 0804. The first two digits refer to the component body length, which is the distance between the terminations, and are in hundredths-of-inches (0.*xx*). The second two digits refer to the body width in hundreds-of-inches (0.*xx*). [For passive devices, a similar numeric designation is given that is based upon the metric system (mm). The actual values are very close to the English values and can be a source of confusion, especially when partnering with overseas companies.] Thus, an 1825 capacitor has a length of 0.18 in. and a width of

0.25 in. A stereo photograph appears in Fig. 43.12 that shows examples of passive components. Chip resistors tend to be very robust and thus relatively immune to damage during the assembly process. Multilayer chip capacitors are temperature-sensitive and therefore more prone to cracking during assembly, particularly under fast temperature ramp rates.

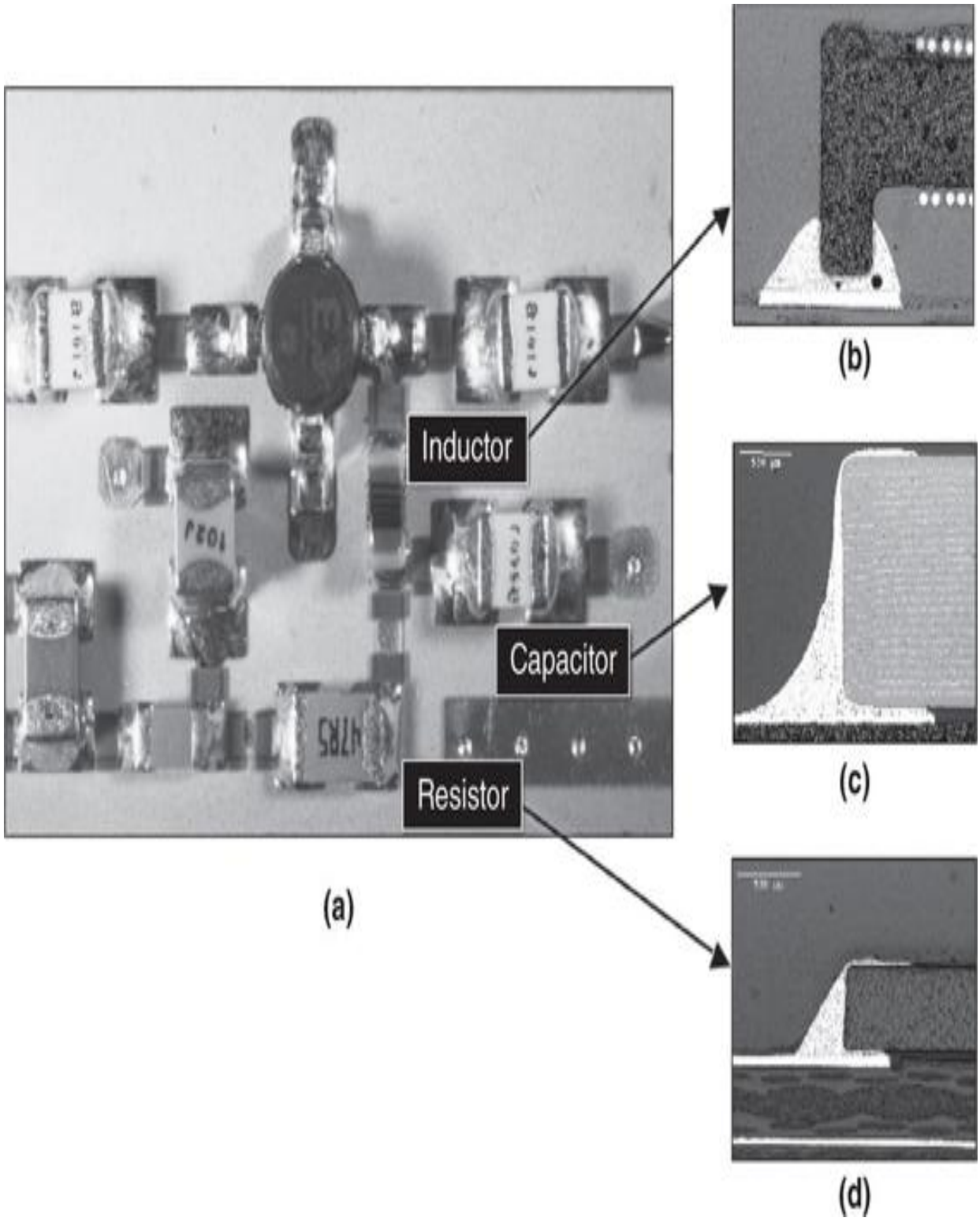


FIGURE 43.12 (*a*) Stereo photograph showing surface-mount passive (chip) devices: inductor, capacitor, and resistor; (*b–d*) cross-sections of their respective solder joints. (*Courtesy of Sandia National Laboratories*.)

The chip resistor is constructed of a piece of alumina ceramic on top of which is deposited a thin film that serves as the resistive element. Attached to the resistive element at the top, on the ends, and partially at the bottom are the termination structures to which the solder joint is made. The termination structures are comprised of a fired, Ag-based thick film; a Ni or Cu barrier layer; and lastly an electroplated finish of Sn, Sn-Pb, or Au.

Chip capacitors are constructed from a special oxide-based ceramic that is built up of alternating layers of ceramics and thin film layers that provide the device capacitance value. This capacitor is the multilayer thin film (MLTF) type. The second capacitor type has electrodes on the top and bottom surfaces of a homogenous “block” of ceramic. The ceramics used to make chip capacitors tend to be more fragile than the alumina body of a chip resistor. The built-up layer structure of MLTF capacitors causes them to be particularly susceptible to both mechanical and thermal shock. Chip capacitors use similar metal layers to build up the terminations that are soldered to the circuit board pad as were described previously for resistors.

Chip inductors are of two types as well. Coil inductors are comprised of a fine Cu wire wound around the alumina body. The body size and number of windings determine the part inductance. The second type is the thin-film inductor. The winding is fabricated from a patterned thin film, which is deposited upon a piece of alumina. (Although the latter are considerably easier to fabricate, they have a limited range of inductance values.)

As much as 40 percent of passive components on a surface-mount product are chip capacitors. The miniaturization of these devices is critical for reducing the size and weight of electronic products. For handheld electronics (such as cell-phones, PDAs, and pagers), common capacitor sizes are from 0603 down to 0402 and 0201.

Some diodes and all active devices come in a wide variety of peripheral lead and area-array packages. The diodes and transistors are typically used in small-outline (SO) packages; they are the small-outline diode (SOD) and small-outline transistor (SOT) packages. The package body is a plastic overmolding compound. There are two leads for the SOD and three for the SOT. The leads are very robust, have a gull-wing shape, and are formed from Cu or an Fe-based alloy. Larger active devices require more I/Os. These devices use the small-outline integrated circuit (SOIC) package with gull-wing leads protruding from the two sides of the long dimension. The gull-wing leads are very robust with a pitch of 1.27 mm (50 mils) or 0.635 mm (20 mils). Pitch is the distance between the centerlines of two neighboring leads.

A further increase in the number of I/Os was realized by placing leads around all four sides of the package; the leads can have the gull-wing geometry or have the J-lead geometry. The J-configuration reduces the bond pad area by bending the lead inward, under the package. Like the gull-wing, the J-lead geometries are robust at 1.27 mm (50 mils) and 0.635 mm (20 mils) pitches.

Pitches below 0.635 mm, beginning with 0.5 mm and 0.4 mm pitches, are called fine-pitch (package) technology. The smaller leads are considerably more fragile, causing them to be more susceptible to damage during handling and pick-and-place activities. Also, the fine-pitch packages have a more stringent coplanarity requirement for the leads. Coplanarity specifies the degree to which the lead bottoms must be at the same level around the periphery of the package. A non-coplanar lead—one that is lifted high—is more likely to generate an open because of the reduced amount of solder used for these smaller I/Os. A lead that is too low will be damaged during package placement and also displace the solder paste deposit, causing a defective joint or short circuit to a neighboring lead after the assembly step.

A second type of peripheral I/O package is the leadless ceramic chip carrier (LCCC). This package is made of ceramic material; the I/Os are castellations on all four sides of the package. Solderability of the castellations is obtained by a Ni finish over which is deposited an Au layer. The Ni and Au layers extend down the castellation and under the frame to form a pad. This package can be used only on so-called matched or low-expansion substrates, that is, circuit board substrates with a thermal expansion coefficient that matches that of the ceramic package. Otherwise, the solder joints are quickly degraded by thermal mechanical fatigue (TMF) when exposed to even modest cyclic temperature environments.

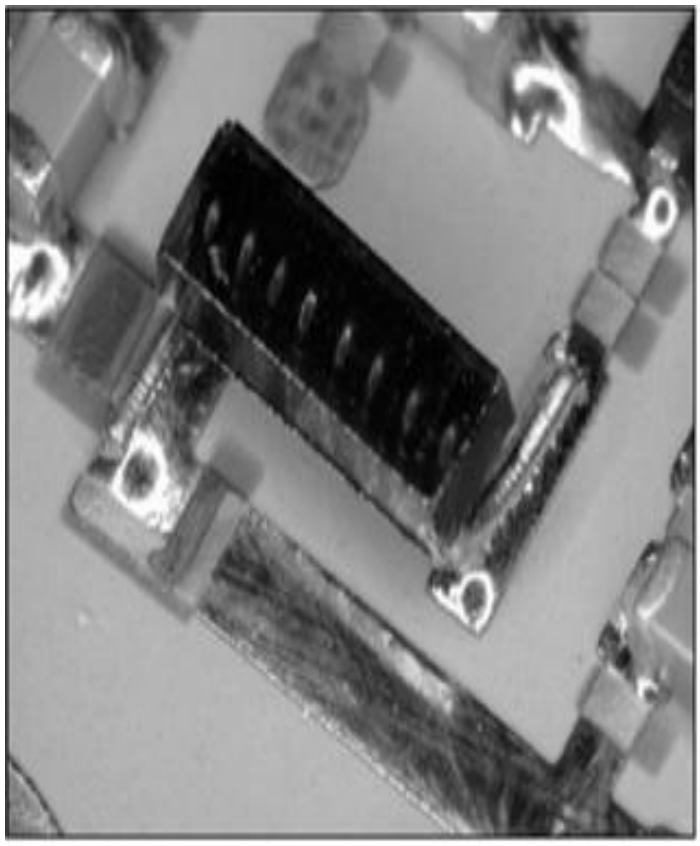
Area-array packages include the BGA, CSP, the land grid array (LGA), DCA/FC, and the ceramic column grid array (CCGA). The common characteristic of these packages is that the solder joint is made to an array of solderable pads on the bottom side of the package rather than to peripheral leads or castellations. The difference between a BGA package and a CSP package is that the latter is stipulated to have molding compound dimensions that are less than 1.2 times the corresponding die dimension. There are no specified limits on a BGA package size.

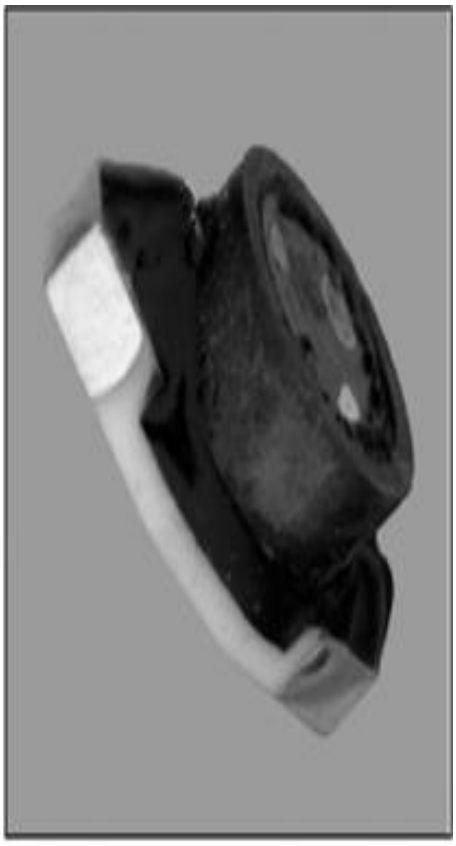
The typical pitch size is 1.27 mm and 1.0 mm for BGA and CSP packages. Here, the pitch is the distance between the center points of any two balls or lands. Therefore, alignment requirements are not very stringent for these area-array packages. Also, there is a sufficient quantity of solder to allow self-alignment between the package and circuit board pads by the surface tension of the molten solder. However, as ball counts reach several thousands, reduced ball sizes and pitches are required, which in turn necessitate closer tolerances on part placement. This is also the case of DCA, where the solder ball size and pitches tend to be as small as 0.10 mm and 0.25 mm, respectively.

The CCGA is a variant of the BGA in which the solder balls have been replaced with solder columns. The columns allow

the ceramic package to be assembled to an organic laminate circuit board of considerably larger thermal expansion coefficient by absorbing the higher strains created by the larger thermal expansion mismatch between the two materials. The columns are created from one of the high-melting-temperature, Pb-based alloys (e.g., 95Pb-5Sn or 90Pb-10Sn) that will not melt during a eutectic Sn-Pb reflow process. The columns may also have a Cu spiral wound around them to enhance durability as those columns are susceptible to damage during handling and part placement.

The accelerated development of surface mount components has generated packages and I/O configurations that have not yet been standardize, resulting in odd-form devices. Examples of odd-form components include surface mount switches and connectors as well as a variety of inductors, (Fig. 43.13) LEDs, and transformers. Typically, so-called surface-mount connectors may actually be mixed technology with through holes providing the mechanical strength needed for cable insertion and removal activities and surface-mount leads establishing the electrical connection. (The through-hole interconnections can be made by paste-in-hole techniques or be soldered manually.)





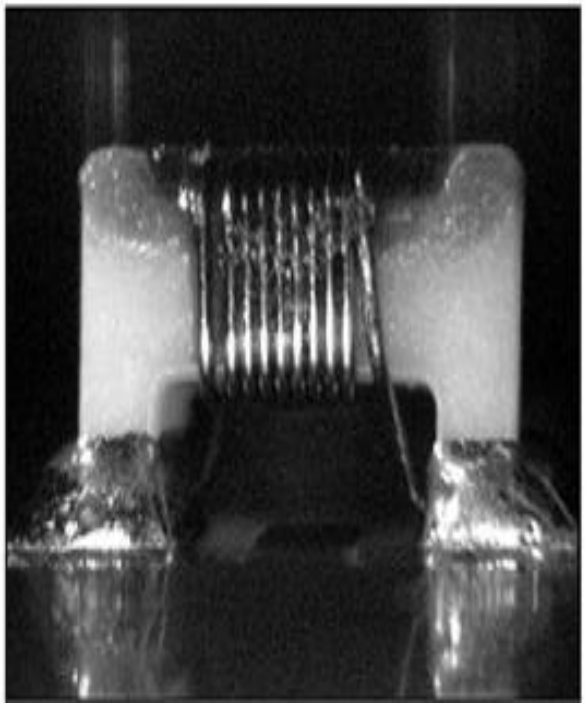


FIGURE 43.13 Odd-form components as exemplified by surface-mount inductors. (*Courtesy of Sandia National Laboratories*.)

A number of assembly-related issues must be addressed with odd-form components. First, it is necessary that correct pad dimensions be designed on the circuit board. Also, the stencil must have the correct aperture size to print an adequate quantity of solder paste. The pick-and-place machine may require custom tooling in order to handle these components. Lastly, odd-form parts are typically larger and heavier. Therefore, it is possible that they will not readily self-align while the solder is molten during the reflow process.

The conversion to Pb-free solders has significantly affected surface-mount components. In the case of leadless passive devices and peripherally leaded packages, the traditional electroplated Sn-Pb finish has been replaced with 100 percent Sn coatings. The Sn coatings have raised concerns regarding the development of Sn whiskers that can potentially short nearby conductors in service. The Sn-Pb solder balls of BGA, CSP, and DCA technologies, having a melting temperature of 183°C, are being replaced with Sn-Ag-Cu alloys with a melting temperature of 217°C. In the case of DCA/FC and CCGA applications, the high-Pb alloys used for the balls and columns, respectively, will not melt during a Sn-Ag-Cu solder process used to create the second-level interconnections.

43.3.3.2 Dispensing. In surface-mount technology, three classes of materials must be dispensed on to the circuit board: adhesives, fluxes, and solder pastes. Each of these three categories, which utilize very similar equipment options for the actual dispensing action, is discussed in the following subsections.

43.3.3.2.1 Adhesives. Adhesives are used to secure surface-mount devices to the circuit board. An adhesive may be required when, for example, exposing surface-mount

components to a wave-soldering process used to assemble a mixed technology circuit board. Also, larger components on double-sided circuit boards may be adhesively bonded in place to prevent them from falling off when the board is turned upside down for the second reflow step. Under these circumstances, the package weight exceeds the surface tension force of the molten solder that keeps smaller components on the board. The adhesive must be able to withstand the temperature conditions of the wave or reflow soldering process as well as the chemical activity of the flux. Adhesives may also be required to anchor larger surface-mount devices to the circuit board. This additional strength is needed for service specifications that include mechanical shock and vibration environments.

(Adhesives are typically not used for through-hole components because clinching the leads provides a sufficient anchor to keep the component on to the board prior to and during the soldering process. After soldering, through-hole solder joints are sufficiently robust to withstand heavy shock and vibration environments. Nevertheless, in very severe environments, adhesives may be used to anchor through-hole components to the substrate.)

It is important to control the quantity of dispensed adhesive since there must be sufficient material to perform the attachment function. On the other hand, too much adhesive can cause run-out onto the solder pad or component I/O, resulting in poor solderability. Some adhesives are prone to run-out or “bleeding” caused by their separation into individual liquid components that together comprise the adhesive material. When bleeding by a component liquid occurs beyond of the adhesive deposit, that bleeding liquid can contaminate nearby solderable surfaces. In the case of very dense circuit boards, excessive migration of the whole adhesive migration, or the bleeding of one of its components, can contaminate the pads of other components, affecting their placement and solderability.

Although the function of the adhesive is to anchor components in place for the soldering process, the adhesive deposit remains as a part of the assembly after soldering, and as such must not interfere with next-assembly steps or negatively impact the long-term reliability of the circuit board. For example, some epoxies readily absorb moisture or other organic compounds. Those absorbed materials may outgas during subsequent temperature excursions that could contaminate critical surfaces (e.g., sensors) when the product is in service. Therefore, it is important to select only adhesive materials that are qualified for a particular application.

Adhesives materials that are used in electronics assembly processes are typically based upon epoxies or silicones. Adhesives can also be described by the following four functional/materials categories: thermosetting adhesives, thermoplastic adhesives, elastomer adhesives, and toughened alloy adhesives. Each group differs in its compositions, the type of curing cycle, and its pre- and postcure material properties. The curing cycle, which typically requires an elevated temperature/time profile, must not degrade the components present on the board or the laminate itself. It is understood that the added step of a curing cycle slows the overall assembly process.

Thermosetting adhesives cure by heat or a catalytic reaction that cross-links the polymer chains. Once cured, these materials remain very strong and will not readily soften at elevated temperatures. Epoxies are one group of thermosetting adhesives, which are used widely in electronics assembly because they do not weaken at the high temperatures of wave and reflow soldering environments. Also, epoxies are resistant to attack by solvents and aqueous-based cleaning solutions. Epoxies can be one-part, in which the curing agent and resin are already mixed together, or two-part, in which the two chemistries are combined prior to application. Although the one-part epoxies

are convenient from the assembly standpoint, their storage and handling must be rigidly controlled to prevent curing prior to use. Both epoxies are cured by exposure to elevated temperatures, which can range from less than 100°C to as high as 125 to 150°C, for time periods of 1 to 4 h, depending on the specific product recommendations. There is very little outgassing associated with the curing of thermosetting adhesives. Higher residual stresses can be generated by these materials due to their rigidity at elevated temperatures when there is a significant thermal expansion mismatch among the package, the epoxy, and the circuit board substrate. The “permanency” of thermosetting adhesives complicates repair or rework functions. The removal of these adhesives usually requires mechanical scraping and abrasion that can damage the component and circuit board.

Thermoplastic adhesives soften when exposed to elevated temperatures. These adhesives are weaker than thermosetting epoxies. However, when tolerances are less restrictive, these materials may be preferred for assembly applications, particularly when excessive residual stresses are of concern during the soldering process temperature cycle. Thermoplastic materials are less resistant to solvents and aqueous-based materials. These adhesives tend to absorb these liquids more readily, resulting in dimensional changes (swelling) and more outgassing than is observed with thermosetting adhesives.

Thermoplastic materials have curing temperatures that are lower and time durations that are shorter than thermosetting materials. Some compositions will cure at room temperature, making them suitable for temperature-sensitive components or when thermal expansion mismatch, residual stresses are of concern. Another advantage of thermoplastic adhesives is that because they readily soften at elevated temperatures, they can be easily removed to allow for the rework of components.

Elastomeric adhesives are a subset of thermoplastic adhesives. These materials tend to be very tough, yet have a higher degree of elasticity. The silicone (rubber) adhesives are examples of this category. The lack of rigidity limits the application of these adhesives in the soldering assembly process. Curing temperatures are relatively low, as some compositions cure at room temperature. However, the curing cycle of some silicone adhesives include considerable outgassing and, moreover, the outgassing of vapors that can be corrosive to metal surfaces (e.g., acetic acid).

Toughened alloy adhesives are blends (or alloys) of elastomeric materials and epoxy resins that together form this special class of thermosetting-like adhesives. These adhesives are engineered to provide both high structural strength and sufficient toughness (ductility) to resist damage due to either thermal or mechanical shock. Examples of this type of material include epoxy-nylon adhesives.

All of these materials have been engineered to have properties that can accommodate one or more of the various dispensing techniques used in printed circuit board assembly (which are discussed later in this chapter). However, these properties do not remain optimal indefinitely. There are two stages of degradation. The first stage is the shelf-life of the material, which is the time frame during which the adhesive keeps its properties while the container remains unopened. Manufacturers date-code specify shelf-life based on changes to the mechanical properties (strength, ductility, etc.) and physical properties (glass transition, density, liquid viscosity, etc.) that occur to the adhesive. Density and viscosity directly impact dispensability.

The second stage of degradation occurs when the adhesive is removed from the container, mixed if required, and is loaded into the dispensing equipment. Exposure to air, even under room temperature conditions, causes the adhesive to begin curing on the assembly floor. The curing can alter density and viscosity and thus the dispensing

properties of the adhesive. Indications of a significantly cured adhesive include a clogged dispensing machine, run-out or bleeding of the deposit, and “stringers” of material created as the dispensing tool moves from one location to another spot.

43.3.3.2.2 Fluxes. The dispensing of fluxes has more limited applications in surface-mount technology (aside from mixed technology that includes a wave-soldering step). Flux dispensing is performed when solder is not simultaneously delivered to the joint—for example, the wave soldering of a mixed technology circuit board or the attachment of an area-array package for which the solder balls provide a sufficient quantity of alloy for the joint. In fact, flux dispensing is most widely used for DCA/FC applications. The DCA joints often require only a very small quantity of solder that would be difficult to control or to place accurately with typical printing equipment and stencils. Thus, the quantity of solder present in the ball forms the joint, and only flux must be added to the assembly.

Soldering fluxes are generally available only as a liquid for electronics applications. The low viscosity prevents the flux from being precisely located on the circuit board using stencil printing. Therefore, flux is usually dispensed by spraying techniques. However, once flux is sprayed on the surface, the circuit board must be soldered very quickly as volatiles and other components begin to evaporate from the flux coating.

In the case of DCA applications, the flux is applied directly to the component. The process is shown schematically in Fig. 43.14. The die is placed into a bath containing a very thin layer of flux. The thickness of the layer controls the quantity of flux taken by the die when it is withdrawn from the bath. The flux must be sufficiently tacky to anchor the die to the substrate for transport to the reflow step. Because of the large exposed surface area of the flux bath, the flux volatiles

readily evaporate so that the bath must be replenished on a regular basis.

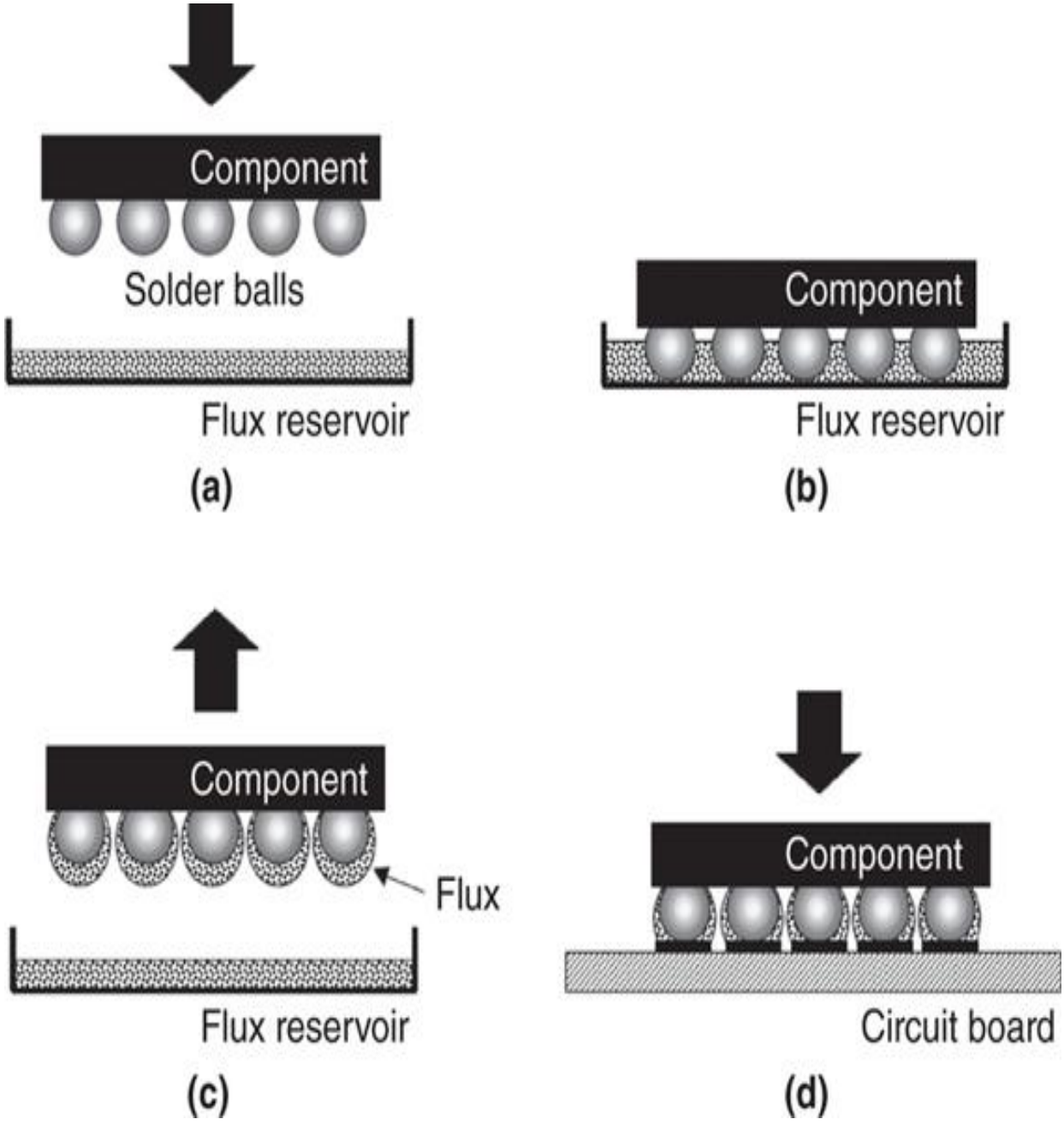


FIGURE 43.14 Flux dispensed on the balls of a flip-chip component: (*a, b*) the solder balls are immersed into the flux reservoir; (*c*) the component is removed from the reservoir with the solder balls coated with flux; (*d*) the component is placed on the circuit board.

43.3.3.2.3 Solder Paste. The dispensing of solder paste is the most widely used means of providing flux and solder metal to the joint for the reflow process. The primary components of the solder paste are the solder metal and the flux. The solder metal is typically 80 to 90 wt. percent of the paste. Aside from the In- and Zn-containing solders, there is very little sensitivity of the paste properties to the solder metal composition for Sn-based alloys. Important properties of the paste with respect to dispensing are the solder powder particle size and weight percent or “metal loading” of the paste.

The flux can be any one of the various compositions—rosin-based, no-clean, low solids, and water-soluble. The flux also provides the tack that keeps the components attached to the board prior to the reflow step. Other ingredients in the paste are the thixotropic agents. It is the thixotropic agents, together with the metal content and flux, that determine the viscosity of the paste.

Viscosity controls the dispensing properties of the paste, irrespective of the particular technique (needle, screen printing, etc.). The viscosity and hence the dispensability of the paste change with time, whether slowly in an unopened jar on the shelf or more quickly when the paste is exposed to air while awaiting the dispensing step. Care should be taken to monitor strictly the manufacturers’ recommendations for shelf-life and lifetime on the assembly floor. Poor solder paste dispensing accounts for the majority of solder-joint defects observed in surface-mount technology.

43.3.3.2.4 Dispensing Methods. There are five primary methods for dispensing adhesives, fluxes, and solder pastes:

1. Pin transfer
2. Screen or stencil printing
3. Time-pressure pump dispensing
4. Archimedes screw pump dispensing

5. Positive displacement pump dispensing

The latter three methods generally produce a single deposit per dispensing step. The first two methods enable the application of the material at multiple sites in a single step. Of course, the five techniques do not perform equally well for the three materials. This section discusses the advantages and disadvantages of each technique.

Pin transfer is the simplest technique for dispensing adhesives and flux. Although a single pin may be used to deposit material one location at a time, a matrix of pins can do so at multiple sites, the pin transfer process is illustrated in Fig. 43.15. This technique is suitable for adhesives and fluxes; it does not work as well with solder paste. A pin is dipped into a reservoir of the adhesive or flux. The length and diameter of the pin determine the quantity of material that is picked up upon its withdrawal from the reservoir. The pin is then lowered to a position just above the surface of the printed circuit board that allows the flux or adhesive to contact the circuit board. Surface tension causes a portion of the adhesive or flux to be deposited on the printed circuit board. It is very important that the pin does not touch the board because this will cause inconsistent dot sizes and shapes. This system requires the substrate to be relatively flat and free from distortion. The nature of the pin array can also allow for adhesive to be applied to the board even after through-hole parts have been put into place.

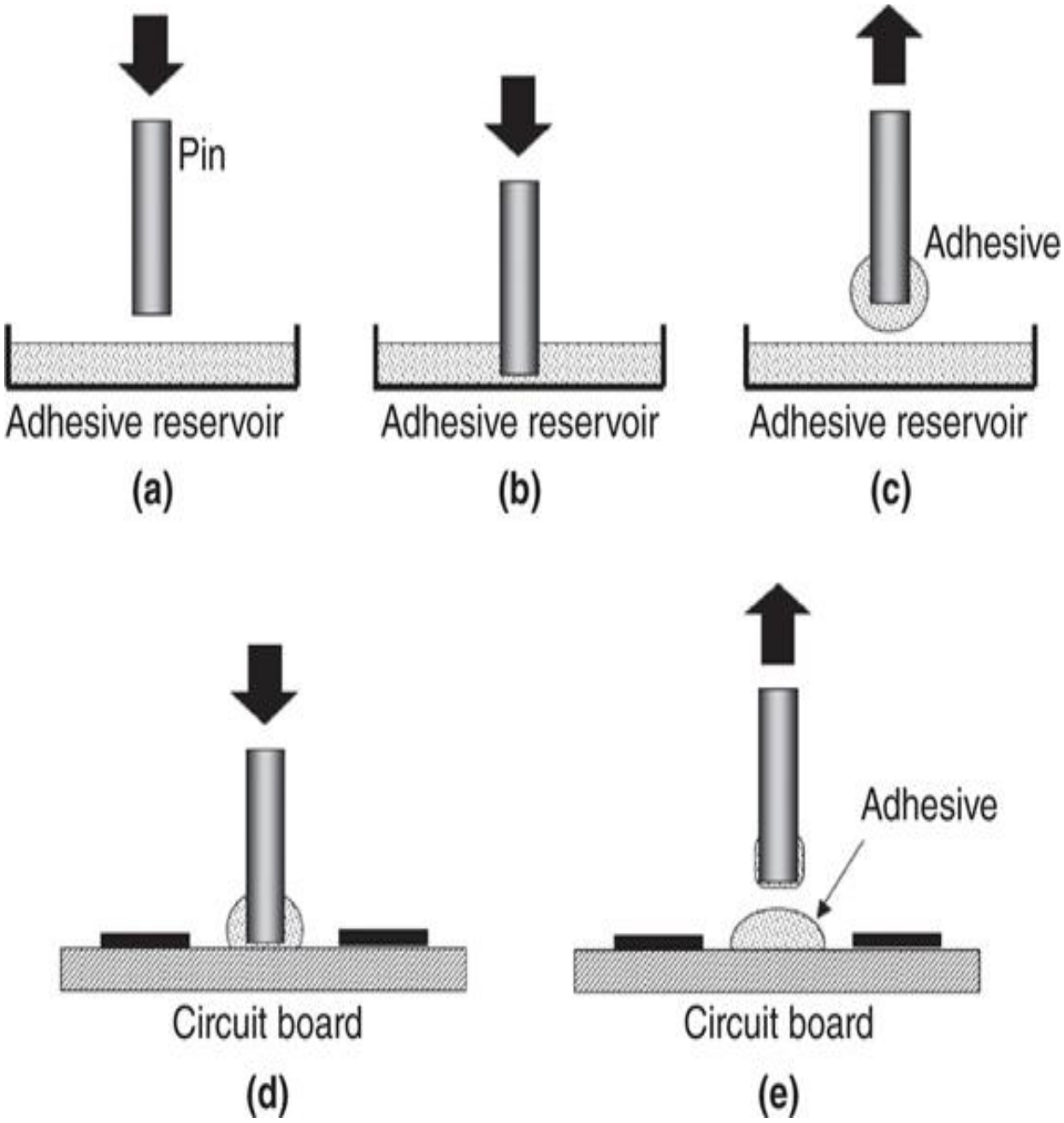


FIGURE 43.15 Pin transfer technique: (*a*) the pin is brought down to the adhesive reservoir; (*b*) the pin is immersed in the adhesive; (*c*) the pin is withdrawn from the reservoir with a repeatable quantity of adhesive; (*d*) the pin is positioned on the circuit board, allowing the adhesive to contact the surface; (*e*) the pin is withdrawn from the surface, leaving behind a well-controlled volume of adhesive.

A similar principle to pin transfer is used for the application of flux on the solder ball of FC components for DCA (see Fig.

43.14). The die is immersed into a thin film bath of flux. The flux depth allows only the balls to be coated so that, in effect, the solder balls become the pin, taking up the flux. The flux on the solder balls is transferred with the die to the circuit board, where it provides the tack function as well as fluxing action for the solder balls during the reflow step.

An important consideration about the pin transfer technique is that it requires an open bath of the adhesive or flux. Adhesives readily absorb water from the air. Fluxes lose vehicle (water or alcohol) and possibly other constituents through evaporation. By either mechanism, the material properties change, which affects the quantity of fluid retained on the pin and deposited at the site (including the flip-chip process previously described). Adhesives must have sufficient “wet strength,” and the fluxes must have enough tack to hold the component in place for the duration of component placement activity as well as subsequent handling of the circuit board on its way to the curing oven or reflow oven.

Screen or stencil printing can be used for adhesives as well as solder paste. The low viscosity of most flux solutions precludes their successful dispensing by this technique. The adhesive or solder paste is deposited through openings in the stencil or screen called *apertures*. The apertures are located over the locations on the circuit board where the adhesive or solder paste is required. The placement of material is performed by a squeegee pushing a quantity of adhesive or paste ahead of it, over the screen or stencil, as illustrated by Fig. 43.16*a*.

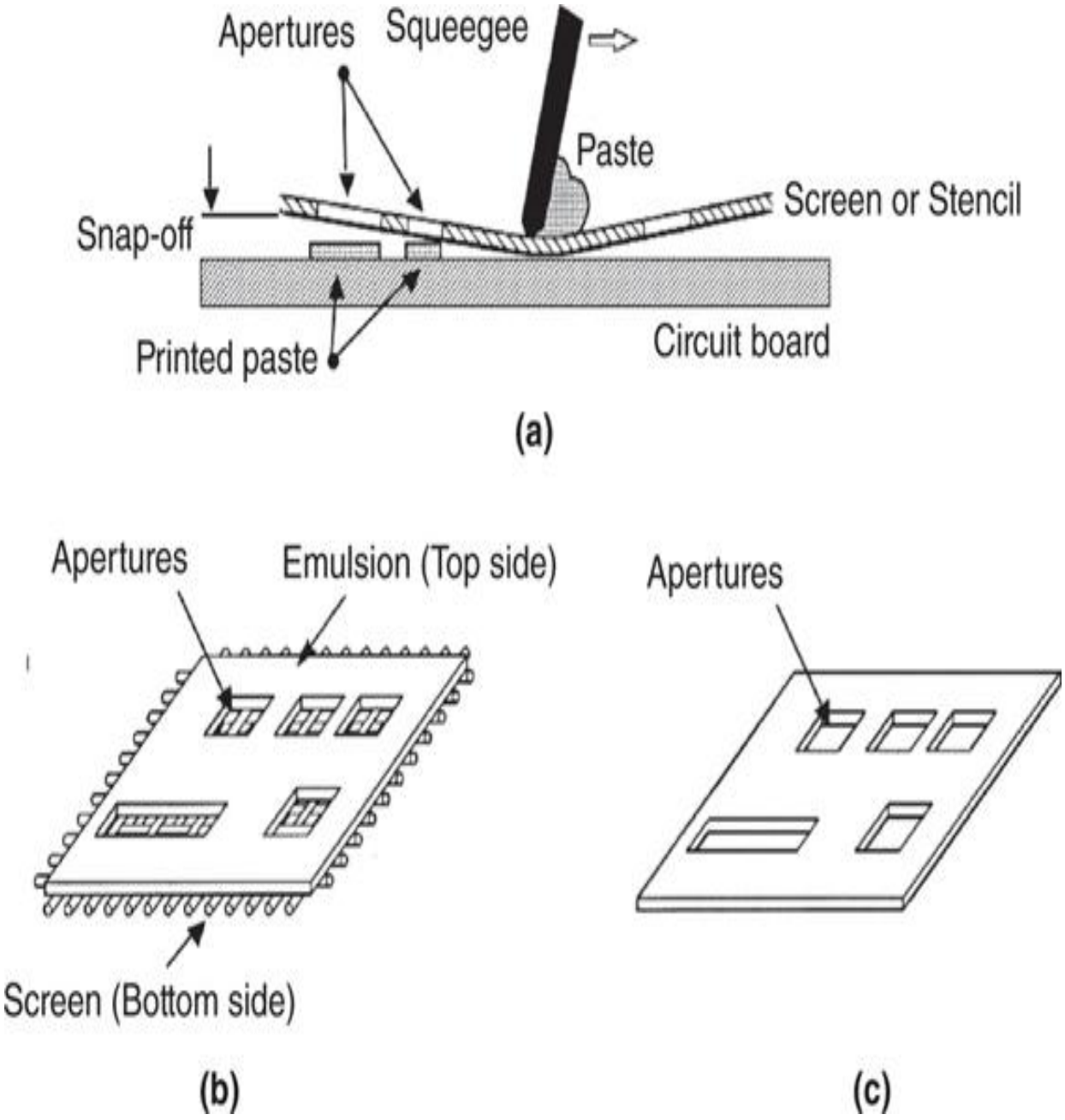


FIGURE 43.16 Screen and stencil printing: (*a*) the squeegee movement used to print adhesive or paste through a screen or stencil; the construction of a screen (*b*) and stencil (*c*) used for printing.

The difference between a screen and a stencil is in their respective structures, as shown in Fig. 43.16*b*, *c*. The screen is comprised of two layers: the emulsion layer and the actual screen that supports the emulsion layer. The apertures through which the adhesive or solder paste is deposited are

created in the emulsion by photoimaging techniques. The adhesive or solder paste simply flows past the screen cross-hatched wires.

The stencil is simply a sheet of metal or alloy (commonly Mo, Ni, brass, or stainless steel) having the apertures formed in them. The apertures can be created by one or a combination of the following techniques:

- Photoimaging (photoresist definition) combined with etching by wet chemistry
- Laser cutting
- Build-up technology by electroplating processes

The choice of fabrication technique depends on the required sizes and densities of the apertures. The stencil has replaced the screen in most surface-mount printing applications, not only because of its simpler construction, but also because it can accommodate finer, denser circuit board features.

The thickness of the screen or stencil and the size of the individual aperture openings are the parameters that control the *quantity* of adhesive or solder paste deposited on the circuit board. Secondary factors are the aperture wall quality, the material viscosity, the hardness of the squeegee, and the speed of the squeegee. In the case of solder paste, the quantity that is actually deposited is usually *less than* the volume of the aperture, which is the product of the width, length, and stencil thickness. The degree of that discrepancy is called the *transfer factor* or *transfer coefficient*. Values can range from 60 percent for very small apertures to nearly 100 percent for larger aperture openings.

Screen or stencil printing is the most widely used means for depositing solder paste on a surface-mount circuit board. The preferred paste viscosity for screen printing is 250 to 550 kcps (kilo-centipoises) for an 80-mesh screen. In the case of stencil printing, the desired viscosity is 400 to 800

kcps. The ability to print consistently upward of tens of thousands of paste deposits per circuit board has been critical to the realization of high-volume electronics production. This process is being developed for through-hole circuit boards and is referred to as *paste-in-hole* or *pin-in-paste* technology.

Solder paste printing technology includes stepped stencils. Stepped stencils are made with two different thicknesses and are used when a circuit board has such a wide range of device pitches and joint configurations that a single stencil cannot yield the optimum paste deposits for all the components. The thinner sections are used for the very-fine-pitch packages, whereas the thicker sections deposit paste for the larger-pitch components. These stencils are more expensive to fabricate than the single-thickness products.

The printing of adhesive or solder paste with a screen or stencil has several limitations. It can only be performed in a single pass; if there is a fault during that pass, the board must be removed and cleaned prior to a second attempt. Second, the circuit board surface must be flat and have no obstructions that will interfere with the stencil or screen surface “sealing” against the board surface as the adhesive or paste is pushed into the apertures by the squeegee. As such, it is important that the screen or stencil be thoroughly cleaned of paste residues prior to use in order to minimize printing defects, which can subsequently become solder joint defects if not caught prior to reflow. Third, stencils and screens wear with time, resulting in an increased number of printing defects. The harder the metal or alloy, the longer is the lifetime. For example, brass stencils, which are relatively inexpensive, have a short service life. Stainless steel stencils have a longer lifetime, but are also considerably more expensive.

Referring to the solder paste printing process with a stencil, Pb-free solder pastes behave very similar to the Sn-Pb pastes for leaded and area-array pitches of greater than

0.5 mm. At the smaller pitches that are characterized by smaller apertures, it has been observed that the Pb-free solders have a slightly reduced transfer coefficient. The likely cause is the reduced density of the Pb-free solder particles, which becomes a significant factor when so few particles are passed through the aperture. Therefore, it may be necessary to slightly open up the apertures to ensure a sufficient quantity of Pb-free solder at the joint.

Time-pressure pump dispensing is a method to deposit adhesive or solder paste by applying a pressure pulse for a specific time duration on a reservoir of material (see Fig. 43.17). A precisely controlled quantity of adhesive or solder paste emerges from the selected orifice size, which is deposited on the circuit board. Often, the material comes prepackaged in a syringe that is inserted into the machine.

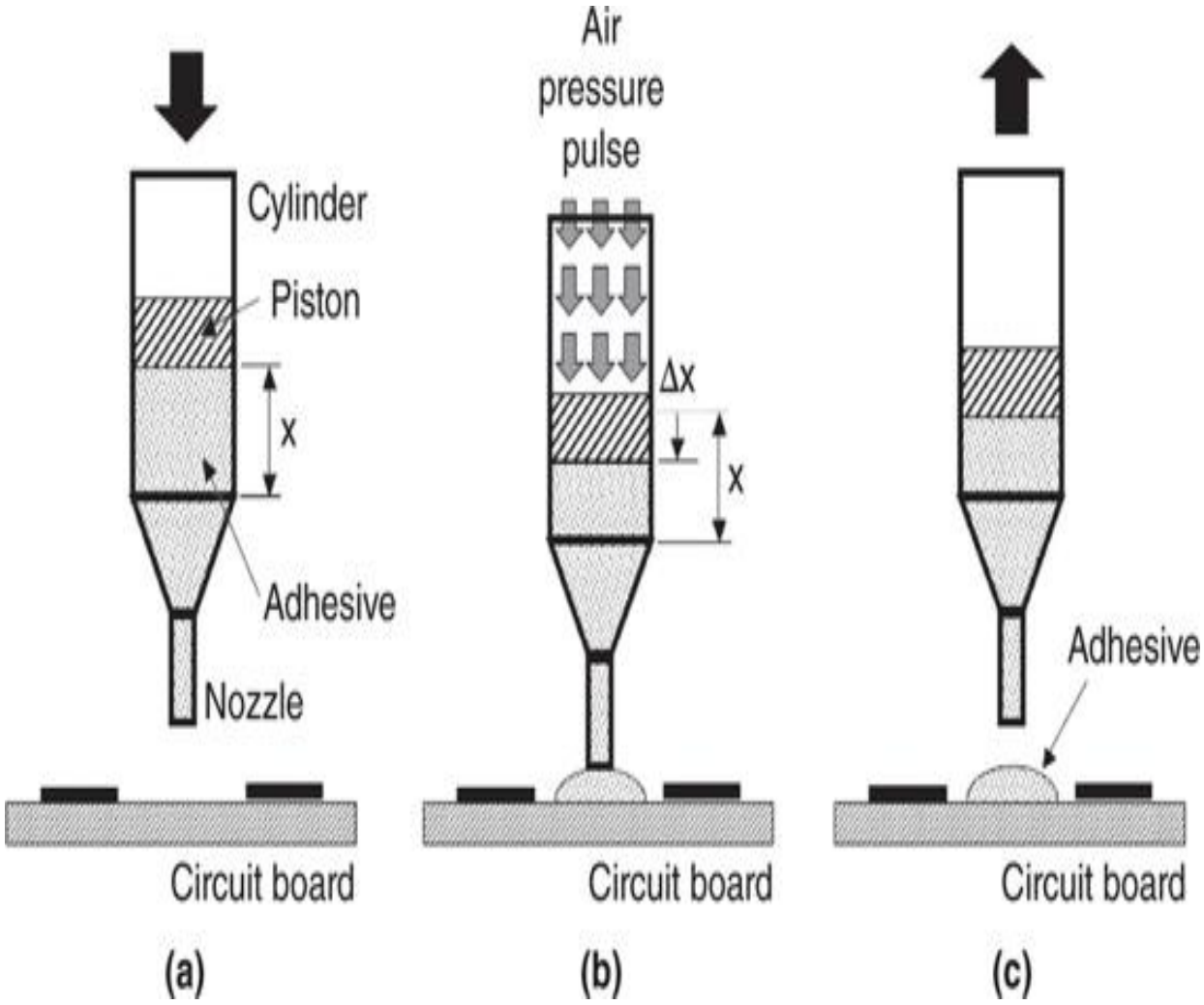


FIGURE 43.17 Time-pressure pump dispensing technique: (*a*) the dispenser is positioned at the circuit board site; (*b*) the dispenser is lowered to near the surface at which time, a pulse of air pushes the piston a distance Δx to dispense a set quantity of adhesive; (*c*) the dispenser is raised from the site, leaving the adhesive deposit.

As with all dispensing techniques, the flow properties of the adhesive or solder paste are important factors that determine the consistency of the deposit between the different sites. Shelf-life requirements should be strictly followed, particularly those pertaining to time allowed for the material to be present in the dispenser due to rapid degradation when open to the factory floor environment. The desired viscosity for pump dispensing through a nozzle is 100 to 400 kcps.

Machines utilizing the time-pressure dispensing technique can dispense different deposit sizes on a single board. One approach is to have multiple nozzles or syringes on a single head, using the same pulse profile. The second approach is to preprogram a different time-pressure pulse that alters the deposit quantity from a single orifice or syringe. This pump-dispensing technique (as well as those described in the following paragraphs) is slower than screen or stencil printing. However, it offers greater flexibility in terms of well-controlled deposit quantities and location.

Archimedes screw pump dispensing utilizes an Archimedes screw to push the adhesive or solder paste out of a nozzle (see Fig. 43.18). The speed and duration of a turn, as well as the size of the opening, determine the quantity of adhesive or paste deposited on the site. As in the case of the time-pressure technique, different deposit quantities can be realized by multiple spindle (heads) or a computer program that alters the screw speed or turn duration to change the amount of material dispensed from the same orifice. All other considerations with respect to the roles of adhesive or solder paste viscosity and shelf-life also apply to this technique.

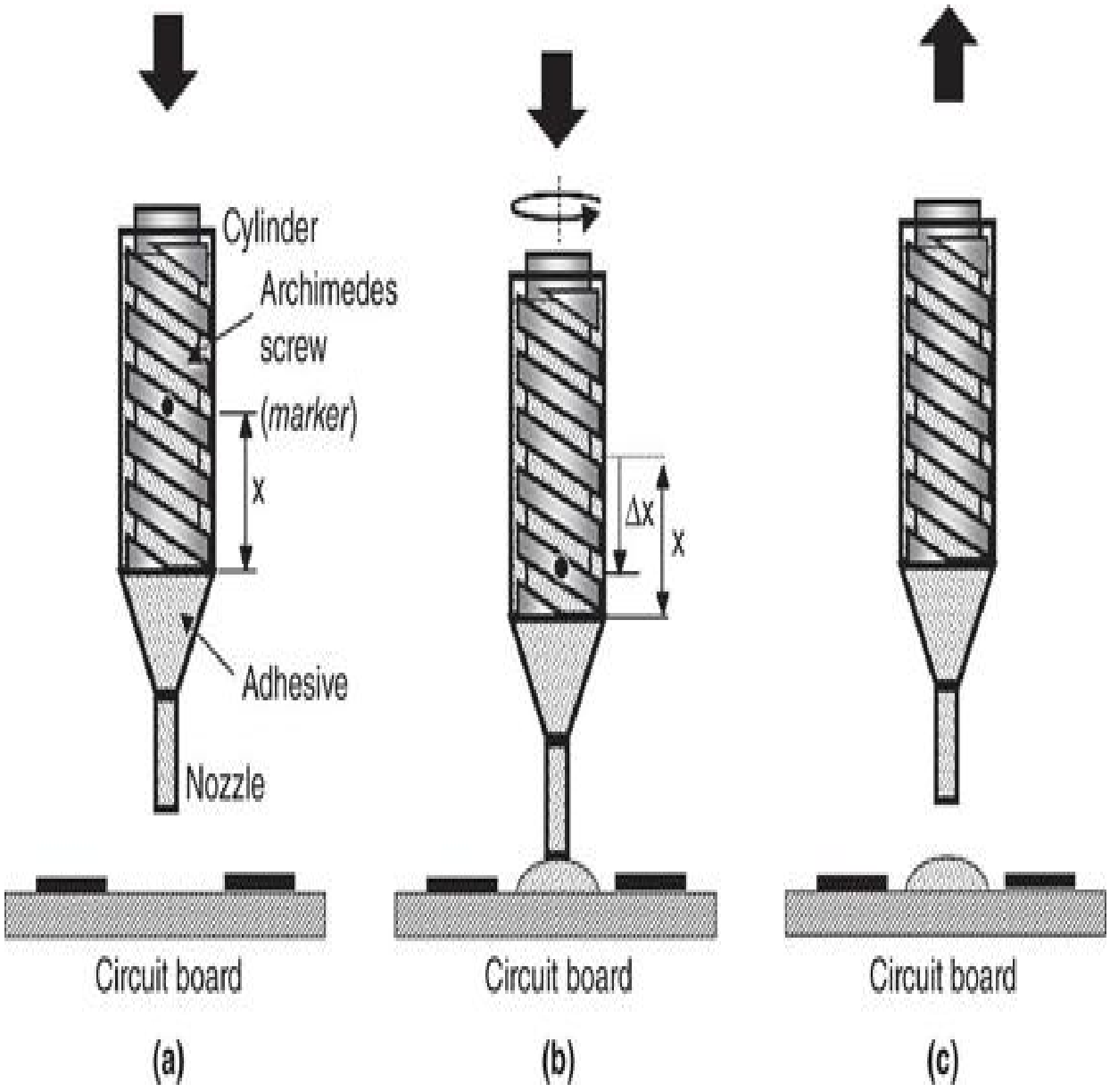
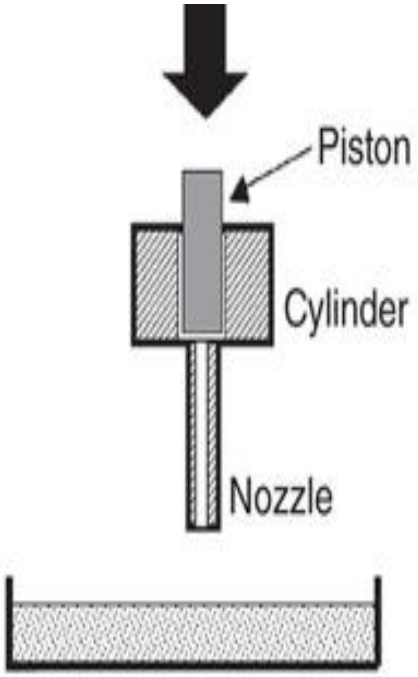


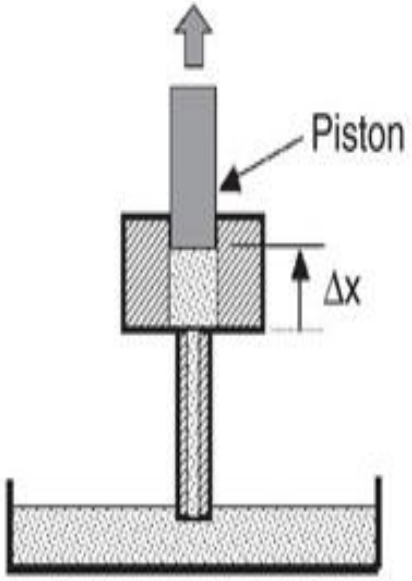
FIGURE 43.18 Archimedes screw pump dispensing technique: (*a*) the dispenser is lowered to above the circuit board surface; (*b*) the Archimedes screw is turned a set rotation (Δx), pushing adhesive out of the nozzle; (*c*) the dispenser is lifted from the circuit board.

Positive displacement pump dispensing uses a piston, rather than an air pressure pulse, to control the deposit quantity. This technique is used primarily to dispense adhesive (see Fig. 43.19). First, the nozzle is placed in a bath of adhesive, in which it retracts to draw a quantity of adhesive that fills the orifice and small cylinder at the top of

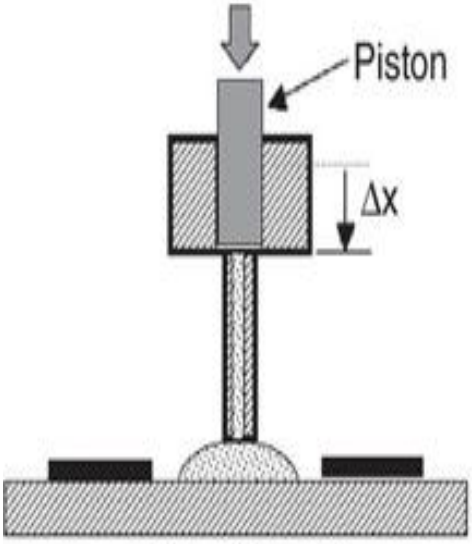
the orifice. This suction step works best with low-viscosity fluids. It is difficult to pull up relatively high-viscosity materials such as solder paste and some adhesives. Next, the piston moves downward into the cylinder, forcing an exact amount of adhesive out the nozzle and onto the printed circuit board. This technique consistently produces the same volume of material. Besides the dimensions of the cylinder as well as the speed that the piston displaces, the viscosity of the adhesive also affects the dispensed quantity. Shelf-life specifications should be strictly enforced.


Piston
Cylinder
Nozzle
Adhesive reservoir

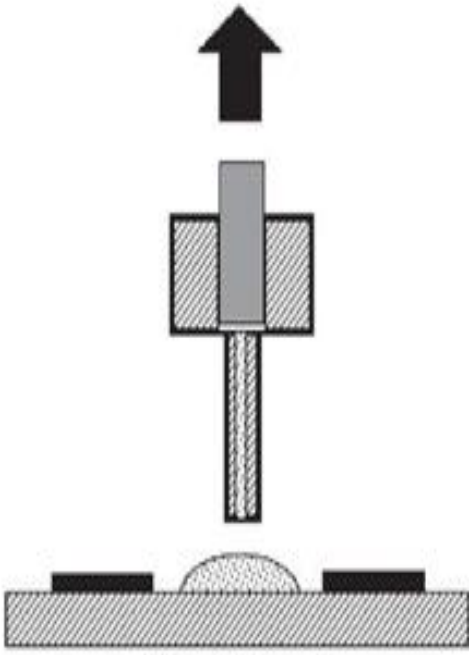
(a)


Piston
Δx
Adhesive reservoir

(b)


Piston
Δx
Circuit board

(c)


Circuit board

(b)

FIGURE 43.19 Positive displacement pump dispensing technique: (*a*) the dispenser is brought to the adhesive reservoir; (*b*) the nozzle is immersed into the adhesive and the piston withdrawn a distance Δx, resulting in a set quantity of material being pulled into the cylinder; (*c*) the dispenser is brought to just above the circuit board surface so that a reverse displacement of the piston pushes out a quantity of adhesive; (*d*) the dispenser is lifted from the circuit board.

The primary objective in each of the five dispensing techniques is to deposit *consistently* a *specific quantity* of adhesive or solder paste at each designated site. Too small of a quantity of adhesive, especially dot height, can fail to attach the part to the board. Too much adhesive causes it to run on to the solder pads, degrading solderability. In the case of solder paste, an insufficient quantity of paste will cause an incomplete joint or, in the worst case, an open circuit. An excess of solder paste results in a fillet that is difficult to inspect for solderability or risks formation of short circuits between neighboring interconnections.

43.3.3.3 Component Placement. The purpose of the component placement machine—also called the "pick-and-place" machine—is to select the proper component, orient it correctly, and then place it on the circuit board, all with degrees of accuracy and precision that minimize defects on the finished product. In addition, the component must be placed on the printed solder paste, the dispensed adhesive, or a combination of the two deposits with a controlled pressure or release distance that does not excessively spread out either material or damages the component package. Moreover, the placement machine must execute these tasks as quickly as possible in order to maximize the production volume. Lastly, the equipment must be sufficiently versatile to address continually changing electronic packages, specifically dimensions and I/O configurations.

The change to Pb-free solders does not have an explicit impact on component placement machine technology.

Indirectly, however, the need for alternative surface finishes on both the components and circuit board fiducials, which have different reflectance characteristics, can affect the performance of the vision systems used to locate accurately both the circuit board and the tooling that delivers the component to the board.

Several machine types are available. The turret-style chip shooter and the gantry-style or flexible fine-pitch (FFP) machines have both been used extensively in the assembly of consumer electronics, telecommunications, mainframe and server computers, as well as for lower volume, high-reliability electronic products. However, the demands for even higher production volumes as well as the flexibility to change product lines rapidly have caused manufacturers to consider alternative machine architectures that include high-speed stepper motors and optical sensors as well as highly parallel methodologies that place multiple components at the same time.

43.3.3.3.1 Turret Systems (Passive Devices). The basic turret or “chip shooter” has been used to place passive components (i.e., capacitors, resistors, etc.) since the early development of surface-mount technology. A photograph of the turret head and schematic diagram of its operation are shown in Fig. 43.20. Multiple heads are positioned around a stationary, horizontally rotating turret. A moving feeder carriage positions tape feeders that deliver a component to each head. After the part is located in the head, the turret rotates it to a vision processing station where a charge coupled device (CCD) camera acquires an image of the part. This image is processed so that the part will be precisely located over the circuit board location. As the turret continues rotating, a moving table positions the printed circuit board so that the target location is in position under the turret head to receive the component. The part is lowered to the circuit board and released. The head rotates to acquire another component, and the cycle repeats itself.

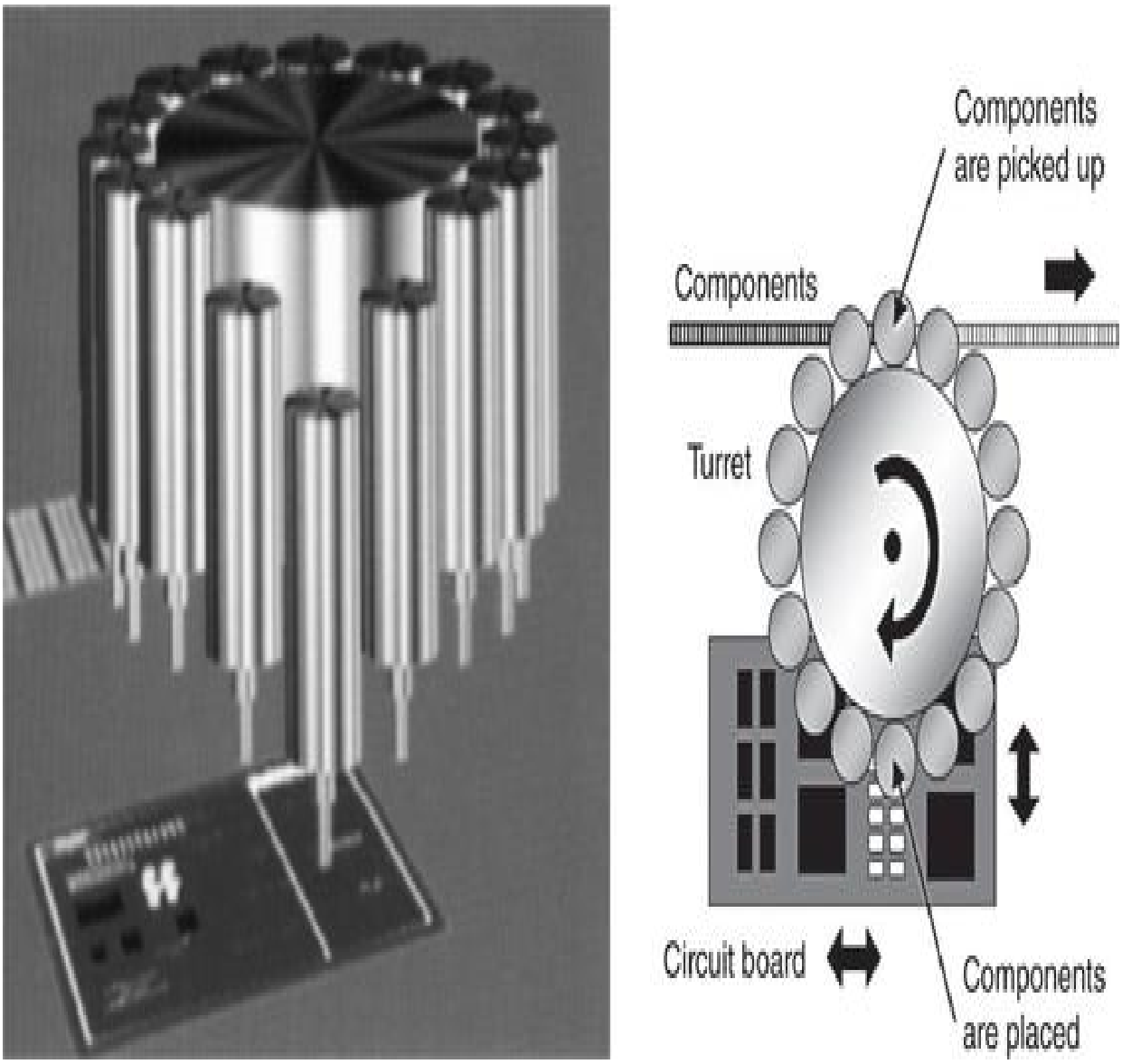


FIGURE 43.20 Turret head used to retrieve chip components from a tape and place them on the circuit board. (*Photo courtesy of Universal Instruments*.)

Listed in Table 43.3 are general performance characteristics for turret chip placement technology. This technology is constantly addressing smaller passive devices (0101 and 01005) as well as an increased demand for placing bare die (flip-chip) components on more densely populated circuit boards. Equipment manufacturers and users must continually address new package configurations with different I/O geometries.

TABLE 43.3 Capabilities of Turret Chip Placement Technology

Property	Range
Part range	0201 (English) passive chip devices to 10 mm area-array packages
Part capacity	Several hundreds
Placement speed	25,000–40,000 CPH*
Capabilities	1. Handle both chips and small area-array packages. 2. Moving turret and PCB to increase placement speed. 3. Flexibility of using either tape or bulk part supply.

*CPH = components per hour

43.3.3.3.2 Gantry Systems (Active Devices). The gantry-style architecture differs from the turret because the printed circuit board is fixed in place and the moving gantry locates the component over the correct position (see Fig. 43.21). The part feeder is stationary. The gantry method is typically used to place larger components (e.g., SOICs, PLCCs, etc.). Several attributes of gantry technology are listed in Table 43.4.

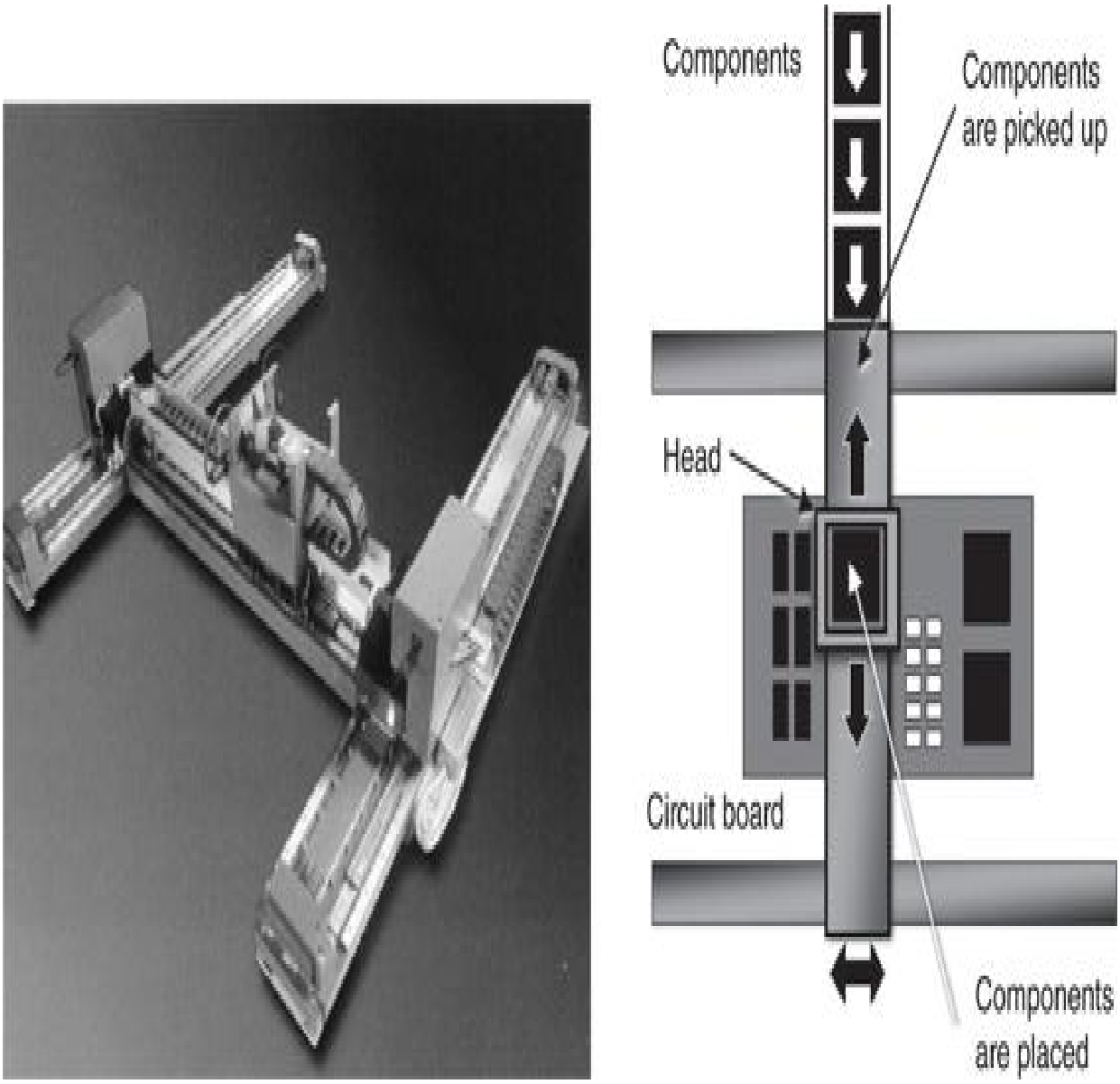


FIGURE 43.21 Gantry architecture used for placing larger components such as SOICs, PLCCs, and area-array packages. (*Photo courtesy of Universal Instruments*.)

TABLE 43.4 Capabilities of Gantry Technology

Property	Range
Part range	Full SMT (SOD, SOT, SOIC, PLCC, CCGA, BGA), direct-chip attach (DCA), and odd-form components.
Part capacity	Several hundreds
Placement speed	5,000–15,000 CPH*
Capabilities	1. Oversized and odd-form parts placed with very high accuracy. 2. Moving gantry, fixed PCB, and feeders. 3. Flexibility of using tape, tube, bulk, and tray part supplies.

*CPH = components per hour

Several equipment variations can be specified to increase the variety of parts placed on the circuit board. Each gantry is made to accommodate different parts when equipped with a multispindle placement head. The placement head is positioned at each feeder location to receive a part. Then, the head moves the component to the upward-looking vision station for inspection followed by its placement on the printed circuit board. A second option is a placement machine made with dual gantries, each placing a single component type or multiple components with the spindle head option.

Several features in gantry-style equipment allow component placement speeds to approach those of turret systems in “high-speed” models. See Table 43.5 for the performance of some dual-beam (gantry) equipment. Machine options that enhance placement speeds include tape splicing for uninterrupted machine operation and simpler bank-changing capability to allow for the rapid changeover of components between different product lines. Also, part inspection can be made using a head-mounted

camera while the gantry(ies) is (are) in motion, which eliminates the time interval required for part inspection with a stationary, upward-looking camera.

TABLE 43.5 Capabilities of High-Speed Gantry Technology

Property	Range
Part range	Full SMT (Passives, SOD, SOT, SOIC, PLCC, CCGA, BGA), direct-chip attach (DCA), and odd-form components.
Part capacity	Several hundreds
Placement speed	15,000–21,000 CPH*
Capabilities	1. Oversized and odd-form parts placed with very high accuracy. 2. Oversized board capacity. 3. High volumes of tape, tube, bulk, and tray part supplies.

*CPH = components per hour

Further enhancements in capabilities of component placement equipment can be realized in *massively parallel* architectures. The attributes of this approach are listed in Table 43.6. Multiple placement modules are capable of picking up, inspecting, and placing components at the appropriate location on the circuit board. The circuit board is stepped by an indexing conveyor to locate the placement site precisely under the overhead component.

TABLE 43.6 Capabilities of Massively Parallel Gantry Technology

Property	Range
Part range	0201 (English) passive chip devices to 25 mm area-array packages
Part capacity	Several hundreds
Placement speed	60,000–100,000 CPH*
Capabilities	1. Chips and small area-array packages.
	2. Large board size.
	3. Tape part supplies in multiple bans.

*CPH = components per hour

43.3.3.3.3 Machine Vision Technology. A brief which is description is provided of one of the most critical advancements in component placement *machine vision technology*. The earliest pick-and-place function relied on mechanical stops (*detents*), switches and precision tooling to ensure that components were placed at the correct locations and with the proper alignment of I/Os to pads. As both board densities and component varieties increased, this technology was too slow to meet the requirements for higher production volumes and reduced placement defects. A critical incentive to move away from mechanical registration toward vision-based placement came from smaller I/Os on components. DCA/FC uses die bump pitches as small as 0.1 mm. Passive device sizes are commonly 0402 and 0201. Fine-pitch, quad flat pack (QFP) components have lead pitches as small as 0.3 mm. Each of these cases underscores the need for very high placement precision that can be realized only with machine vision technology.

In addition, there has been a steady increase of odd-shaped devices that include inductors as well as LEDs, surface-mount connectors, etc. The result has been circuit

boards with a greater mix of package types and sizes. Consequently, it is considerably less expensive and time-consuming to reprogram a computer-based, machine vision system to recognize these components than it is to retool a machine based on mechanical relays, detents, and such for component placement.

Machine vision technology uses electronic cameras and optics together with specialized computer software to control the stepper motors responsible for positioning the component and the circuit board (site) relative to each other with the required accuracy and precision. To realize this objective, the placement machine must identify the component in the turret or gantry and establish the position of the turret or gantry. At the same time, the placement machine must know the position of the circuit board. The computer software ties these two requirements together by being programmed with the artwork (drawings) that identify the location of each component on the circuit board. Component recognition and circuit board recognition are discussed next, followed by comments regarding vision system limitations.

Component recognition is typically obtained from the configuration of the I/Os. The I/O configuration includes two attributes: the I/O's shape, whether it is a beam lead, gull-wing lead, or solder bump; and the I/O's layout, which may specify, for example, peripheral leads on two rather than four sides, or solder balls as full area-array packages rather than perimeter, area-array packages. Shown in Fig. 43.22*a* is the machine vision image of a flip-chip die with a perimeter array of solder bumps. The vision system determines the position of the package based upon the coordinates of the I/O locations, for example, two or four of the corner leads or solder bumps. Additional fiducials and/or nonsymmetries in the I/O layout (e.g., missing corner leads or bumps) are used to establish the rotational orientation of the component.

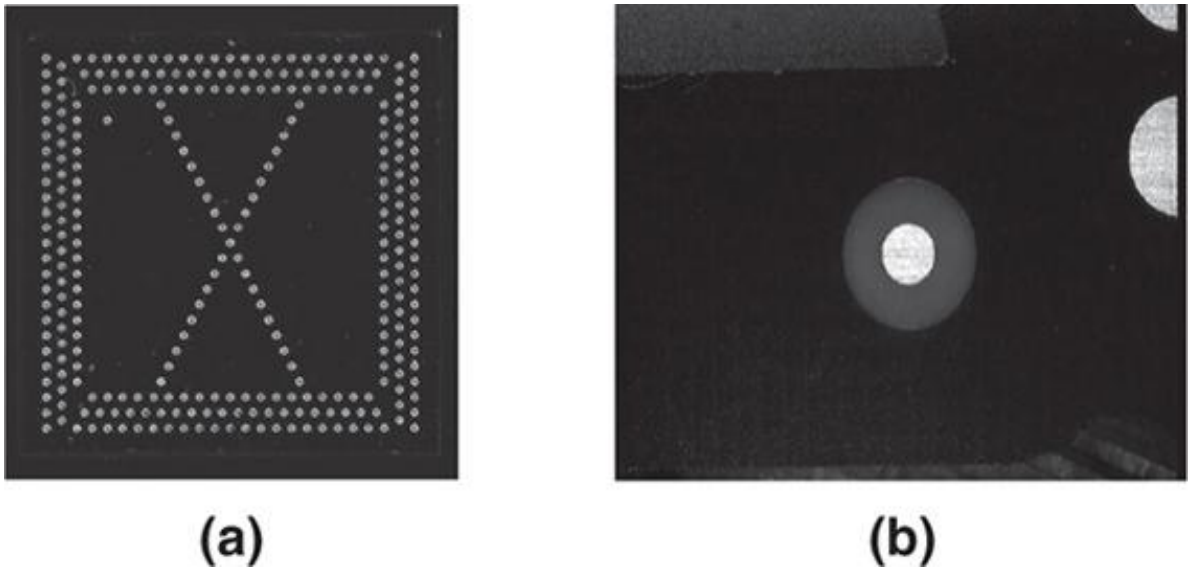


FIGURE 43.22 Vision system images: (*a*) a flip-chip component; (*b*) a printed circuit board fiducial. (*Courtesy of Universal Instruments*.)

Besides determining component type and orientation, vision systems have also been programmed to recognize damage to components. For example, fine-pitch quad flat packages are prone to bending of the very small leads, particularly at package corners, due to worn die sets or improper handling. In the case of area-array packages (BGAs, CSPs, and DCA die), there can be missing balls or solder bumps. The damaged component is rejected into the "scrap bin" and a new unit retrieved for placement. It should be noted that component recognition vision systems are designed primarily for part placement. Although defect recognition can be programmed into the software, increasing the degree of inspection function slows the placement process significantly. Therefore, the optimum approach is to allow the vision system to identify only gross component defects, targeting those defects that would occur between incoming inspection and the component placement step. Otherwise, full, incoming component inspection should be performed *before* the parts are loaded into the placement machine.

Circuit board recognition requires that the machine (computer) be able to locate the circuit board site precisely for the component. First, the circuit board is secured on the conveyor by mechanical clamps, vacuum chuck, or other technique. The circuit board is then positioned under a camera that identifies the registration marks or fiducials on the surface (see Fig. 43.22*b*).

This process is repeated for two to three other fiducials on the circuit board. At this point, the machine "knows" the location and orientation of the circuit board and thus, through the artwork design stored in the software, correlates the fiducial locations with the location of each component site. Subsequently, the software matches the coordinates of the circuit board site to those of the component positioned in the turret or gantry. Then the software instructs the stepper motors to position the component over that site and lower it on to the circuit board.

Some applications, such as those using ceramic substrates that are prone to inconsistent degrees of shrinkage during fabrication (e.g., low-temperature, cofired ceramic, or LTCC), may develop a discrepancy between the software design and the actual circuit board component positions (pads). In this case, the placement site of each component is determined directly using fiducials in close proximity to that component site. Although local fiducials may enhance component placement accuracy to some degree, especially when tolerance stack-up in the product causes it to deviate from the design files, this approach requires added processing time by the machine computer. The result is a decrease in placement speed that can develop into an appreciable process delay, particularly for large production volumes.

Vision system limitations are determined by the speed with which the computer can process information (e.g., circuit board coordinates, component geometries, defects). The more information to be processed, the slower is the component placement step. For products requiring the

placement of thousands of parts per circuit board, even an additional few tenths of a second per component can add up to a significant loss of production throughput.

Similarly, there are operational limitations on vision systems themselves (cameras and optics). The trade-off is between resolution and the range of processable part sizes. The underlying premise is pixel count. The vision system requires a minimum number of pixels to recognize a feature (lead, solder bump, fiducial, etc.). A very small feature (e.g., a flip-chip solder bump) requires both high magnification and high resolution (i.e., pixels/length or pixels/area) in order for the system to recognize the feature. However, using the same system to recognize a large BGA package would require a magnification that may well be outside the capability of those same optics. Moreover, even if the package could be brought into the field of view, using the same high resolution, which is now not necessary, will overload the computer memory and bog down the software processing step, resulting in a slowing of the placement process. And conversely, the same camera that can efficiently process a large, 32 mm QFP (208 I/O) in a single image would generally not have sufficient resolution to process a flip-chip solder bump of 0.1 mm diameter. Therefore, the choice of optics is critical to maximize the efficiency of the pick-and-place function for a particular product. For optimum efficiency, it may be necessary to place the two components on separate machines. Alternatively, multiple cameras and optics may be used on a single piece of equipment. Cost becomes a critical factor.

Once the components have been placed, the circuit board is soldered using one of the techniques briefly described in the following sections. The component placement step is synergistic with the soldering step and, in particular, reflow soldering. That synergism arises from the fact that placement inaccuracies can be compensated by the self-alignment of packages arising from the surface tension

(more accurately, the solder-flux interfacial tension) of the molten solder. This self-alignment phenomenon opens the placement window for passive devices larger than about 0603, smaller LCCCs, and 1.27 mm pitch area-array packages of up to several hundred balls. Unfortunately, for smaller passive devices and larger area-array packages, the self-alignment process becomes less capable of compensating for placement errors. In the case of smaller passive devices, there is the increased likelihood that an imbalance of surface tension forces can result in an asymmetric movement of the part, causing the tombstoning defect. In the case of larger area-array components, poor placement (which is becoming more critical with the finer pitches of smaller balls) cannot always be remedied by self-alignment simply because of the greater weight of the component.

The topic of soldering is described in greater detail in Chaps. 46 and 47. Therefore, this chapter offers only a brief overview of each approach, with the discussion limited to its relevance to the overall assembly process.

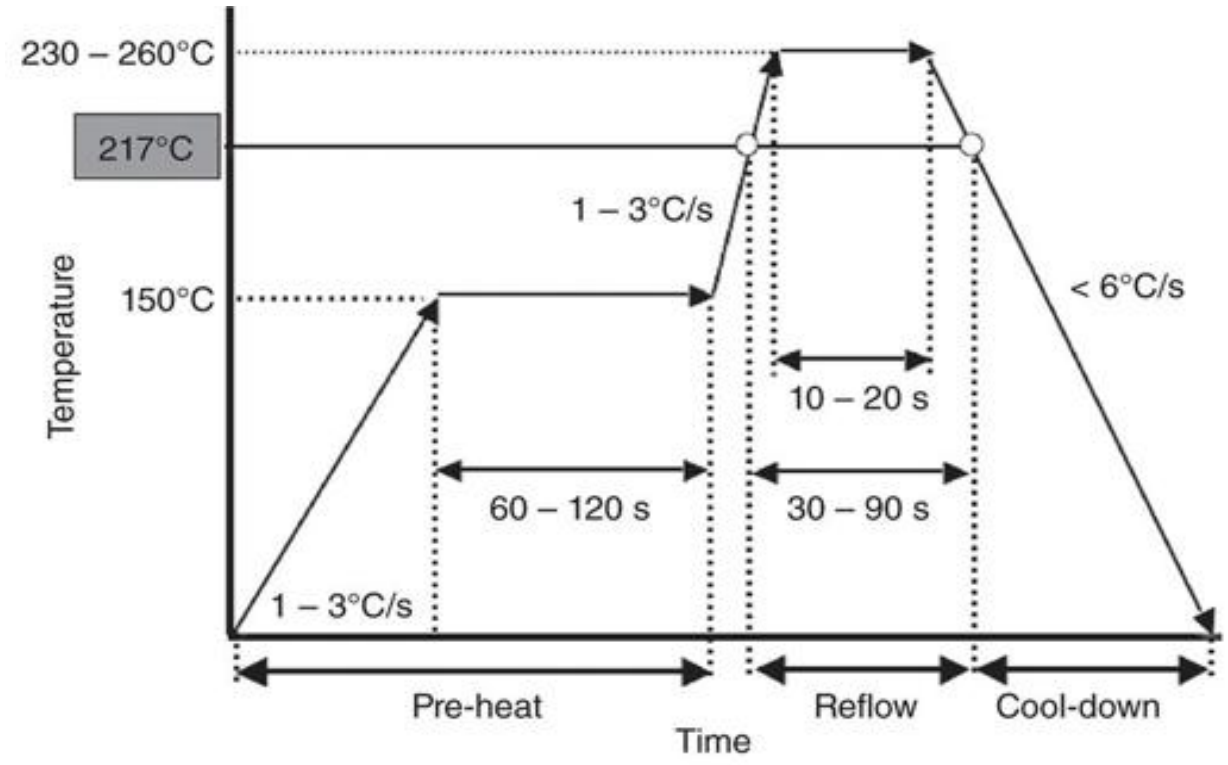
43.3.3.4 Reflow Soldering. Reflow soldering is the technique in which a circuit board, which has the components placed on the solder deposit (either as paste or preforms) is passed through a furnace (oven) in order to melt the solder and form the joints. The furnace may be a batch type in which the circuit boards must be loaded and unloaded, one group at a time. The operator inputs the batch furnace time-temperature profile into the controller that alters the power to a set of heating coils as a function of time. The atmosphere can be very well controlled, including the use of vacuum. The batch furnace is advantageous for small production lots, including development work or when the time-temperature profile and environment must be carefully controlled for the application.

The second furnace has an inline configuration. The circuit boards continuously enter one end unsoldered and exit the other end soldered. Therefore, the inline furnace can be part of an overall assembly line, receiving stuffed circuit boards from the component placement machine via a conveyor without operator intervention. The temperature of the different zones along the length of the furnace and the conveyor speed determine the time-temperature profile. More zones (five to seven are typical) provide for better control of the soldering profile. Inert atmospheres, typically nitrogen (N_2) to minimize cost, can be maintained to better than 20 ppm oxygen (O_2). However, control of both the time-temperature profile as well as atmosphere cannot match that of a batch furnace. Also, vacuum conditions are not possible with most inline equipment. Nevertheless, inline furnaces are well suited for high production volumes and are the most widely used furnace type for electronics assembly.

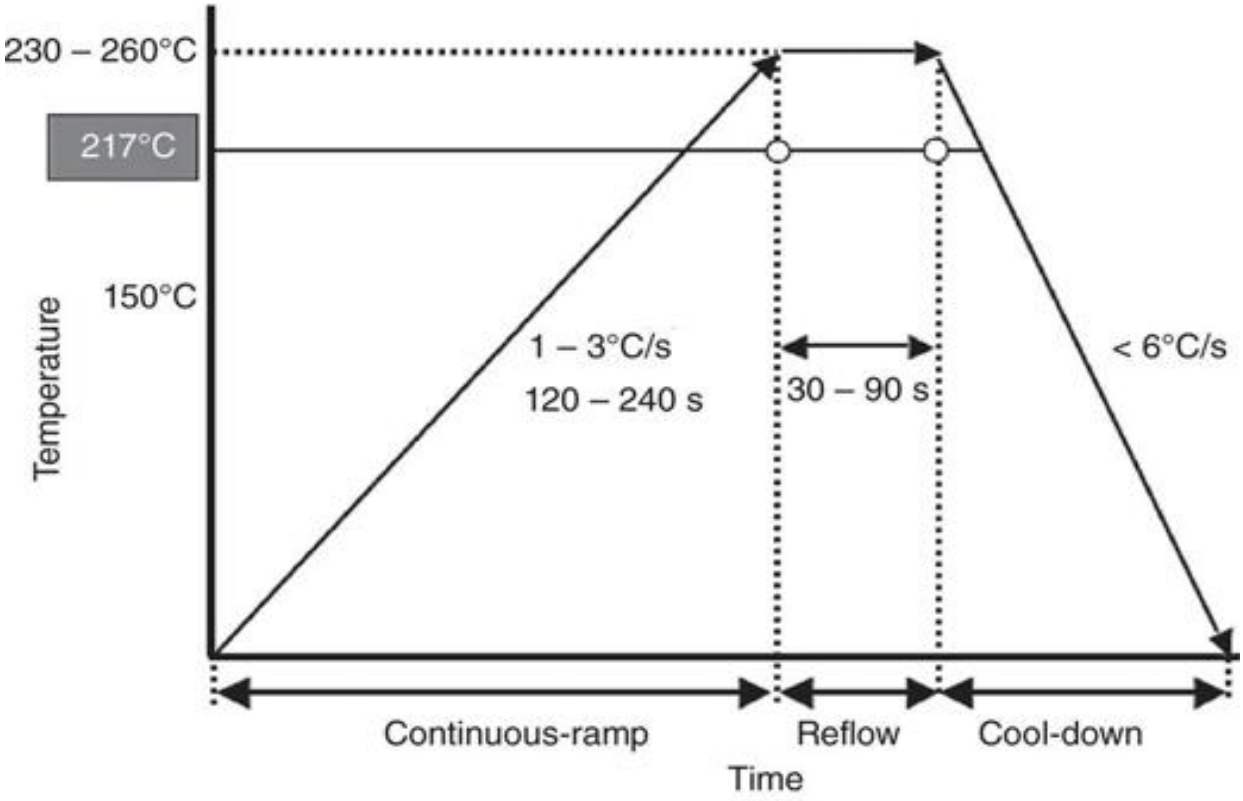
Whether batch or inline, furnace selection is based not only on throughput rates, but is also determined by the type of product being assembled. A greater complexity to the circuit board requires more control of the time-temperature profile to ensure that all of the solder joints are completed at minimum defect levels. In some applications, the extra furnace zones are used to control the cooling rate of the soldered circuit board to prevent thermal shock damage to sensitive components or substrates.

The introduction of Pb-free solders has impacted reflow soldering, less so in terms of actual equipment temperature capabilities than in the development of a suitable time-temperature profile. The heat source technology (infrared, convection, or mixed) can provide the higher reflow temperatures of the Sn-Ag-XCu alloys (T_{melt} = 217°C versus 183°C for the traditional Sn-Pb solder). Of course, higher energy usage and maintenance costs are likely. Two generalized reflow profiles are used for Pb-free soldering.

They are illustrated graphically in Fig. 43.23. The soak-reflow profile in Fig. 43.23*a* derives from the traditional Sn-Pb eutectic solder profile, but with the reflow “spike” increased for the higher melting Sn-Ag-Cu alloys. The soak step provides for activation of the flux as well as heatup of the circuit board and components. The continuous ramp or “hat” profile in Fig. 43.23*b* allows for a more rapid heatup rate, which reduces the time that heat-sensitive components and materials spend at elevated temperatures. On the other hand, the relatively faster heatup rate can increase the chances of thermal shock damage to some components—for example, larger plastic and ceramic devices—or to circuit board structures such as vias.


230 – 260°C
217°C
150°C
Temperature
1 – 3°C/s
< 6°C/s
10 – 20 s
60 – 120 s
30 – 90 s
1 – 3°C/s
Pre-heat
Reflow
Cool-down
Time

(a)


230 – 260°C
217°C
150°C
Temperature
1 – 3°C/s
120 – 240 s
30 – 90 s
< 6°C/s
Continuous-ramp
Reflow
Cool-down
Time

(b)

FIGURE 43.23 Generalized time-temperature profiles for Pb-free reflow soldering: (*a*) the soak-reflow profile; (*b*) the continuous ramp or "hat" profile. Peak temperatures will vary, depending on the particular circuit board product.

In terms of optimizing the time-temperature profile, a balance must be established between achieving sufficiently high temperatures that will reflow the solder of every component (size and shape) and preventing thermal damage to other components or the substrate. Therefore, the higher melting temperatures of Pb-free solders make it more challenging to develop a time-temperature profile that will successfully melt the solder paste of larger components without causing thermal damage to smaller devices or to the circuit board material.

Therefore, in the case of some very-high-mix products, it may be necessary to solder larger packages in a separate operation (e.g., hand soldering or selective soldering). Under this circumstance, the latter packages would be considered as odd-form components.

43.3.3.5 Wave Soldering. Wave soldering is used when surface-mount technology is mixed with through-hole components on the circuit board. (See Figs. 43.7 to 43.9 showing wave soldering as it is used for through-hole circuit boards.) Surface-mount devices that are present on the same side as the wave are soldered as well, being held in place by an adhesive. The surface-mount components must be resistant to thermal shock because of the temperature spike experienced upon entering *and* leaving the molten solder wave. The temperature on the topside surface of the circuit board typically remains well below the solder solidus temperature, thereby preventing the reflow of any solder joints present there.

Wave-soldering equipment can be used either in an inline or in a batch process since the equipment has generally the same construction. The inline approach is used to support high production volumes. Small systems that are used in a

batch-like mode include those used for *selective soldering*. This equipment includes miniwaves or solder fountains and are used to solder only localized areas of the circuit board, such as when attaching through-hole connectors, transformers, or switches. The advantage of selective (wave) soldering is that the entire circuit board need not be exposed to an elevated temperature.

An important consideration in wave soldering is the supporting fixtures that hold the circuit board on of the conveyor. In reflow soldering, the conveyor can support the entire bottom side of the circuit board. However, in wave soldering, the conveyor does not offer such support, as it must allow the wave to contact the circuit board bottom side. Therefore, it may be necessary to provide an additional fixture to prevent warpage and sagging of larger circuit boards.

The impact of Pb-free technology on wave soldering has largely occurred in the equipment performance. It has been determined that the same solder bath temperatures that are used for Sn-Pb processes (250 to 270°C) are suitable for the Sn-Ag-XCu Pb-free alloys. Therefore, excessive dross formation and flux residue removal have not become a significant problem during equipment operation. The lack of shiny fillets with the Sn-Ag-XCu alloys has been addressed by modified alloys having Ni and Ge additions that alter the solidification process, which leads to shinier fillet surfaces.

The Pb-free alloy compositions are more prone to erode the wave machine’s structures, such as the impeller, baffles, and pot walls. New wave-soldering machines address this problem through the use of alternative steel alloys and ceramic coatings.

43.3.3.6 Condensation (Vapor Phase) Soldering.

Condensation soldering, also referred to a vapor phase soldering, uses a working fluid’s heat of condensation to reflow the solder paste or solder preform to

make the joints. Because the condensation reflow process had its origins in the early days of surface-mount technology when production runs were more limited in volume, these machines were primarily batch-type units. Subsequently, inline equipment was developed to “attach” the vapor phase reflow machine to the back end of the placement equipment for higher production volumes. Two particular attributes of condensation soldering are (a) the temperature of the product cannot exceed the vaporization (or condensation) temperature of the working fluid, thereby preventing overheating of temperature-sensitive materials; and (b) the temperature is very uniform over all of the components and the substrate, thereby minimizing temperature gradients that could warp or crack component or laminate materials. This process fell out of favor in the early 1990s, for two reasons. First, the working fluid for Sn-Pb solder, Dupont’s Freon TMF, was categorized as an ozone-depleting substance (ODS). Its use was initially restricted and then prohibited by the Montreal Protocols. Second, the increasingly more complex circuit boards that were being designed with surface-mount technology required more precise control of the time-temperature profile, which lead to the development of multizone reflow furnaces having convective and infrared heating capabilities.

There has been a resurgence in the use of condensation soldering. Alternative working fluids have been developed for both Sn-Pb and Pb-free processing that are compatible with environmental regulations. Preheaters are added to reduce the thermal shock when parts entered the working fluid, thereby providing a more controlled time-temperature profile. Lower capital cost and properties of the condensation heat source previously noted cause condensation or vapor phase reflow to be well suited for prototype development programs and small production volumes.

43.3.3.7 Hand Soldering. As noted earlier, in the highly automated surface-mount assembly line having automated paste printing and component placement capabilities, hand soldering would not be particularly advantageous in terms of maximizing production volumes. However, in some applications, the assembly process includes a hand-soldering operation. For example, often odd-form components cannot be incorporated in a pick-and-place machine, or temperature-sensitive devices cannot be exposed to the reflow furnace environment. Under these circumstances, the hand-soldering step is performed *after* mass soldering (reflow, wave, etc.). The implication is that hand soldering is now being performed on what is potentially a very-high-valued circuit board. Therefore, factors such as handling damage, electrostatic discharge (ESD) damage, and thermal damage to nearby components by the soldering iron tip, as well as flux residue contamination, must be thoroughly addressed at the development stage of the hand-soldering process.

The use of Pb-free solders has not impacted the hand-soldering process itself. There is a slight lengthening of the soldering time, typically from 3 to 4 s to 5 to 7 s, due to the higher melting temperatures of the Pb-free solders. The same soldering iron equipment can provide the necessary tip temperatures. The high-Sn solder compositions, coupled with their higher melting temperatures, can more quickly degrade the tip. Lastly, the operator should not mistake a duller appearance to the fillet surface for a “cold” solder joint.

43.3.3.8 Conduction (Sikama) Soldering. Conduction soldering is the process in which heat arrives to the solder paste by means of conduction through the substrate. The process, which is illustrated in Fig. 43.24, is also termed Sikama soldering, being named after the primary equipment manufacturer. The equipment is set up to accommodate an

inline process, although it can be used in batch mode as well.

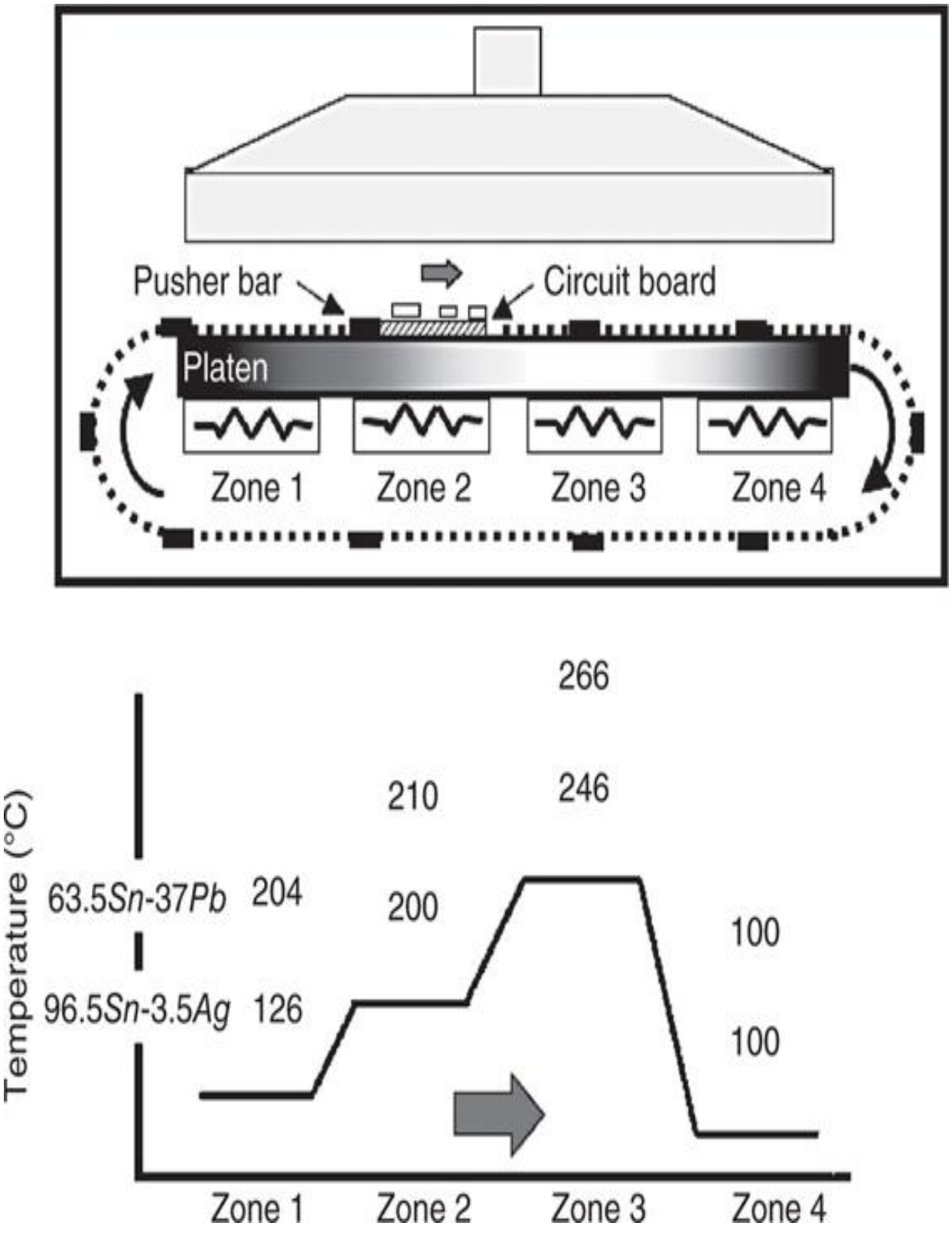


FIGURE 43.24 Schematic diagram depicting conduction soldering. The pusher bar presses the circuit board along the surface of platen. Heaters under the

platen determine the time-temperature profile.

The circuit board is pushed along on top of the heated platen by rods attached to a conveyor. Different sets of heating elements under the platen heat the latter locally to different temperatures along its length, creating heat zones such as those in a reflow furnace. The soldering process can be performed in air or using an inert atmosphere. The fact that the substrate is fully supported along its entire footprint (which is needed to maximize heat input) precludes excessive warpage.

The conduction heating process has been used almost exclusively for ceramic substrate because these materials do not degrade when exposed to the high platen temperatures. Thermal degradation would be more likely for organic laminates. Best results are realized when this process is used with relatively thin substrates (<1.0 mm).

43.3.3.9 Cleaning. Cleaning is typically the final step in the circuit board assembly process. There is a variety of cleaning equipment, from hand-loaded, batch-type "dishwasher" machines for smaller production volumes, up to larger inline units that are integrated into the back end of the assembly line for large production volumes. In response to environmental regulations, cleaning solutions have moved away from the once popular organic solvents to aqueous and semi-aqueous cleaners based on water- and water-alcohol-based compositions. Similarly, the handling of the waste stream is also important. Closed-loop systems are preferable to once-through cleaning process because of regulations governing the disposal of the waste stream. In the case of assemblies requiring multiple soldering steps, the cleaning portion of the prior soldering step does not leave a residue on the surface that degrades the solderability required for the follow-on process.

The use of a Pb-free process does not necessarily have a significant impact on the cleanability of circuit boards. At one time, it was believed that flux residues from Pb-free processes would be more difficult to remove, due to the higher soldering temperatures. Subsequently, it has been determined that thermal degradation of those residues is not as severe, so current cleaning processes appear to perform adequately.

43.3.3.10 Pb-Free Solders. The equipment types described in the preceding sections are often combined to form an electronics assembly line. The term “line” implies that the equipment is physically located end to end, thereby allowing for the movement of circuit boards between the different functions or stations. Although this scenario is, in fact, typically the case, it need not always be so. Under some circumstances, it may be advantageous to locate some stations a distance away others on the shop floor, thus requiring operators to move product between the two sites on wheeled racks. This is usually the case with inspection and repair/rework functions as well as for some cleaning processes due to health or safety concerns. The setup and hence the flow of a product assembly process are referred to as the (assembly) line architecture.

Numerous variables are considered when developing any assembly line architecture. The underlying consideration is optimizing the *level of automation*. Some of these variables include the following:

- Available floor space and facilities (electricity, exhaust, computer networks, etc.)
- Equipment footprint and cost of ownership or lease
- Labor costs
- Production volumes and product changeover flexibility

- Circuit board technology (through-hole, surface-mount, or mixed)
- Soldering technology: Sn-Pb versus Pb-free
- Inspection and quality requirements

It is important for the manufacturing engineer to consider not only each of these points individually, but to also apply the proper weighting factors of their importance when integrating them together to develop a process for the product(s).

The introduction of Pb-free solder technology does not, in and of itself, alter the previously described principles with regard to assembly-line architectures. The equipment is very similar and the factors that determine an optimum line configuration remain unchanged. Instead, consideration must be given to the cost/benefit of having an *entirely separate* assembly line that is dedicated to Pb-free products. In the case of wave soldering, the need for a second line is intuitive; it is simply not practical to empty and refill the solder pot with different alloys from both a process time-management point of view as well as the metallurgical-based concern of mixing the two alloys. An interim approach is to exchange only solder pots in the machine, ensuring that all residues of the previous solder have been removed from all equipment surfaces.

However, even in the case of solder paste printing and reflow soldering, many manufacturers have determined that two separate assembly lines are required, even to the extent of physically locating them at separate locations in the plant. There are simply too many risks associated with potentially mixing the two assembly technologies, particularly in high-volume operations where a significant quantity of product may be built before an error is recognized. The potential mix-ups include

- Use of the incorrect solder paste

- Placement of components with the incorrect surface finish—Pb-Sn (high-reliability electronics) versus 100 percent Sn (consumer electronics)
- Incompatible moisture sensitivity levels (MSLs) of plastic molded components
- Vision system settings for identifying fiducials of alternative surface finish
- Reflow furnace settings for the different time-temperature profiles

43.4 ODD-FORM COMPONENT ASSEMBLY

An accurate definition of an odd-form component is one that cannot be placed and/or soldered with equipment *available in the assembly line*. The likelihood of having to address an odd-form component is actually quite high. Because of the wide range of current component technologies as well as those expected in the future—whether through-hole or surface-mount—there is always the chance that a package cannot be placed or soldered in the assembly line. Certainly, if volumes warrant, new equipment can be purchased, or special tooling made, for adapting the placement and/or reflow equipment for odd-form components. However, there is a significant cost penalty to this approach, especially if it is performed for a variation of sizes and configurations. Each package variation would require separate tooling designs or equipment modifications. However, the advantages of automating odd-form assembly operations include a higher production volume as well as fewer defects resulting from the automated rather than manual operations. Therefore, it is not unusual for odd-form component assembly to be a mix of both manual practices as well as automated techniques.

Generally, the introduction of Pb-free soldering affects odd-form components in a manner not unlike that for other surface-mount and through-hole components. The two primary issues are I/O surface finishes and temperature sensitivity of each component's material set. High-reliability applications have to monitor components for 100 percent Sn finishes. Because odd-form components often fit this category due to a large size, hot Sn-Pb solder dipping is a more viable option to remove the 100 percent Sn finish. Otherwise, the tracking of incoming material and verification of the actual surface finish may be required.

Temperature sensitivity of devices will have to be documented in terms of surviving the Pb-free reflow profile. In fact, some devices that were previously processed on a Sn-Pb assembly line may have to be set aside as odd-form components because they cannot be exposed to the Pb-free process temperatures. Another risk of the higher-processing Pb-free reflow temperatures is the damage to moisture-sensitive components. The typical Pb-free time-temperature profile adds one or two MSLs to a component. Therefore, devices at MSL levels 5 or 6 per a Sn-Pb profile may have to be assembled to the circuit board in a separate operation to avoid damage, thus causing them to be odd-form components.

43.4.1 Components

Connectors comprise approximately 75 to 80 percent of odd-form components. See Fig. 43.6. For example, there are universal serial bus (USB) connectors, dual inline memory module (DIMM) connectors, phone jacks, and zero-insertion-force (ZIF) connectors, as well as a variety of surface-mount connectors. Other odd-form components include sockets, electrolytic capacitors, transformers or large inductors, LEDs, relays, switches, as well as speakers and vibrators for

handheld communications devices. In surface-mount technology, odd-form components are most often through-hole packages, including both passive and active devices as well as connectors. When addressing such odd-form components, the first step is to check the availability of an equivalent surface-mount version since there has been a shift toward surface-mount versions of many of these devices. Of course, the materials used to construct the surface-mount replacement must survive the reflow furnace environment, and especially the Pb-free reflow temperatures, particularly connectors because of their complex internal construction. In some cases, it has been possible to replace the through-hole connector with one of a variety of solderless products.

Also, it is not necessarily size or weight that causes a component to be identified as “odd-form” per the particular assembly line. Temperature-sensitive and moisture-sensitive devices may also be excluded from a reflow step of the assembly process to prevent damage to them. The latter scenario is of particular concern when converting from a Sn-Pb to a Pb-free process. DCA refers to the assembly of an *unpackaged* active semiconductor device directly onto the circuit board. The interconnections are made either by wirebonding or by solder bumps on the front side of the die. The latter application is referred to as FC attachment and can be implemented into a surface-mount assembly process as long as existing equipment can accommodate the placement accuracy required for the very small solder bumps and pads.

Otherwise, a dedicated cell may be required.

The DCA process, which uses wirebond interconnections, is based on the following steps. First, an adhesive is dispensed on the board and the die placed on it. The adhesive, which is often thermally conductive for heat management, is cured. The I/O pads on the die are wire-bonded to the appropriate pads on the circuit board. Then, the die and wire bonds are

encapsulated in an epoxy to prevent damage to them. The encapsulant, or “glob top,” is then cured. Critical to the glob top technology are the following factors: complete coverage of the die and wire bonds with minimal run-out beyond the circuit board pads; adequate adhesion between the die and circuit board; and good adhesion between the encapsulant and the circuit board beyond the perimeter of the die.

43.4.2 Manual Assembly

In the least complicated format, only an operator places the odd-form components on the circuit board. The soldering process is automated in that the operator picks components from bulk bins and repeatedly positions them onto the circuit board as it is carried along the conveyor line. For paste-in-hole assembly, the solder paste and other components (surface-mount or through-hole) may already be on the board, being held in place only by the tackiness of the paste. Therefore, the operator must not inadvertently displace other components off of their sites during handling.

Also, the operator must pay special attention to handling and ESD damage while placing components. Also, those components that incorporate snap-in features (e.g., connectors) can require that the operator exert relatively high forces on the circuit board. Thus, the operator must not damage either that component or other components and the circuit board. Often, special tooling is used to press snap-in components on the circuit board to prevent such damage.

A large number of applications require the operator to place and then manually solder the odd-form component into place, often after the other components have been soldered into place. The operator must be cognizant of handling and ESD damage as well as prevent thermal damage or the inadvertent reflow of solder joints for neighboring components. The impact of Pb-free soldering would be most

significant in this circumstance. It is necessary to verify that a longer hand-soldering time or a higher tip temperature does not cause thermal damage to the component in question or cause the reflow of nearby solder joints.

It should be noted that irrespective of whether manual assembly is performed on only stuffed boards that will be subsequently soldered or on circuit boards that have already been soldered, the units have a higher value to them because of this processing, which is performed beforehand. Therefore, *any* damage (handling, ESD, thermal, etc.) will result in a significantly higher yield loss to production volumes as well as higher costs associated with the repair or scrapping of damaged circuit boards. Therefore, manual assembly steps must be given due consideration during product design and process development activities.

43.4.3 Automated Assembly

The automated assembly of odd-form components uses the same placement equipment as is used for other components, but with special tooling or a dedicated machine (cell), which is already set up with the required tooling and component feeder systems, that can be introduced into the assembly process. The latter equipment typically places more than one type of odd-form component for increased versatility. For example, the close-up photograph in Fig. 43.25 shows the type of gripper tooling that can place different component packages (to within its design limits, of course). After accuracy and component-type requirements are met, speed is the critical performance metric for odd-form placement machines. Odd-form component placement is nearly always a bottleneck or slow point in the line; therefore, minimizing assembly time devoted to odd-form components will speed up the entire process flow.

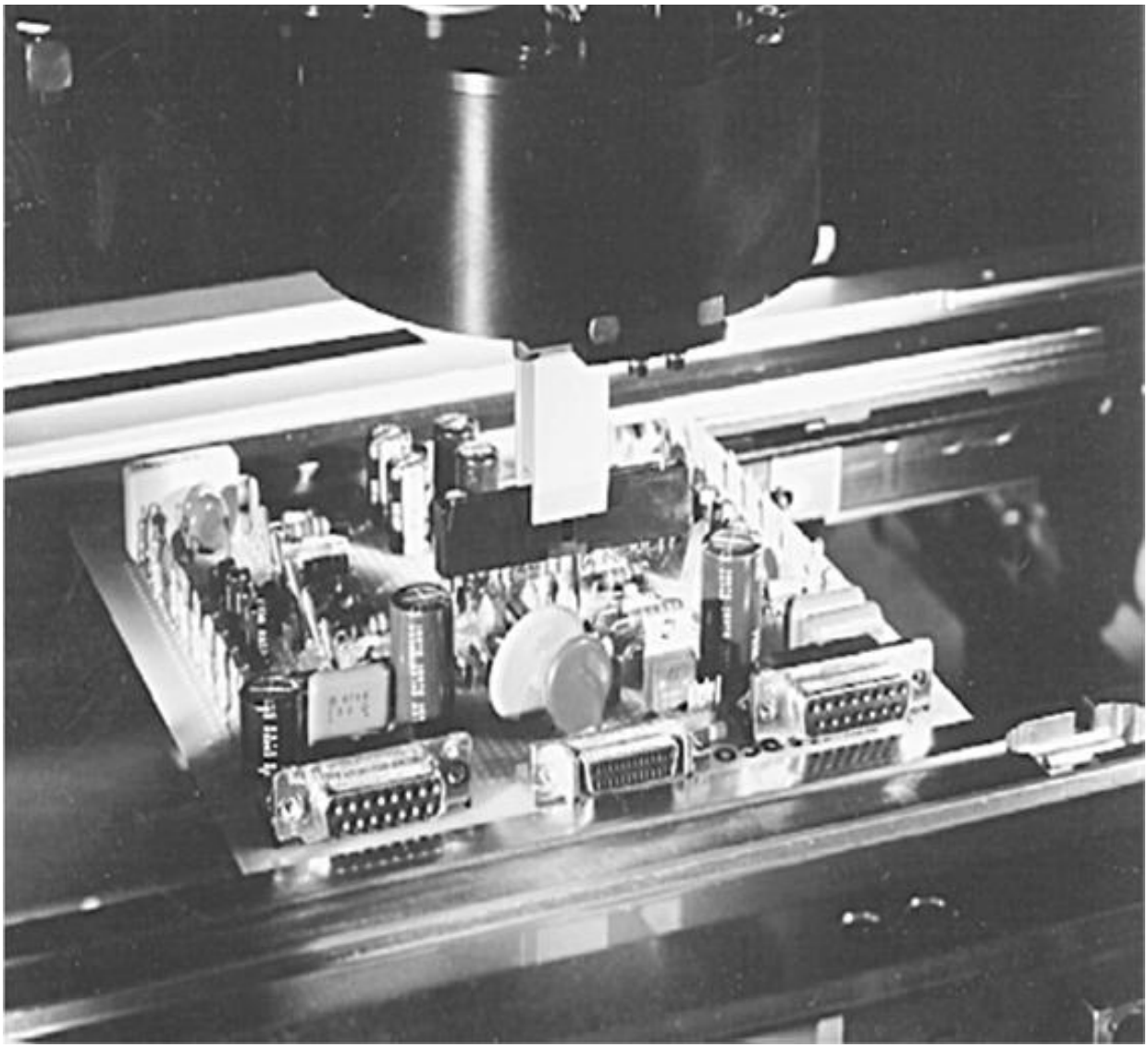


FIGURE 43.25 Odd-form component placement machine having a flexible servo-driven gripper tooling that can place a wide range of different component configurations. (*Courtesy of Universal Instruments*.)

There are both advantages and disadvantages to the automated assembly of odd-form components. Advantages include the following:

- consistent as well as higher quality and faster throughput result from eliminating manual processes.
- Automated assembly saves floor space, as machines typically take up less area than operator work benches.

- Solder dispensing is integrated into the placement process flow, minimizing related defects.
- Automated assembly complements an overall, computer-integrated manufacturing infrastructure already in place with the other assembly steps that, in turn, facilitate process flow, quality control, and product changeover.
- Automation eliminates operator-related health and safety issues (fumes, repetitive tasks, etc.).

The disadvantages of automation include the following:

- Capital equipment costs can be high for machines, dedicated tooling, and plant modifications.
- Prepackaging components are required for automated feeders.
- Equipment changeover for different product lines is somewhat slower due to the need for special component packaging and/or feeders.
- Higher production volumes can generate a greater quantity of defective product before a process problem is identified.

43.4.3.1 Component Packaging Formats. Odd-form components come in a variety of sizes, geometries, and I/O configurations that determine the ease with which the component can be “automated” into the assembly process line. Another important variable is the component placement machine. Typical component packaging formats for the placement machine include tape and reel (radial and axial leaded), extruded tube, tray, continuous strip, and bulk containers. Each of these formats has benefits and drawbacks, as noted in the following subsections. Industry specifications have standardized nearly all of these packaging schemes. For example, there is EIA-468-B for radial devices and EIA-296-E for axial components.

43.4.3.1.1 Tape and Reel. Tape and reel allows for the delivery of parts to the circuit board at very rapid rates. See Fig. 43.26. Tapes are available generally in three formats: flat-carrier tape, deep-pocket tape, and semi-deep-pocket tape. Flat-carrier tape is the traditional method of carrying both odd-form (as well as form-fit) radial and axial components. It is inexpensive and can provide a large quantity of parts for rapid placement rates. Deep-pocket and semi-deep-pocket tapes provide room for the larger component bodies. The packaging of multiple parts having a similar pitch is possible with semi-deep-pocket tape; the particular advantage is to conserve feeder space, particularly when only a few of each type of component are required on the circuit board.

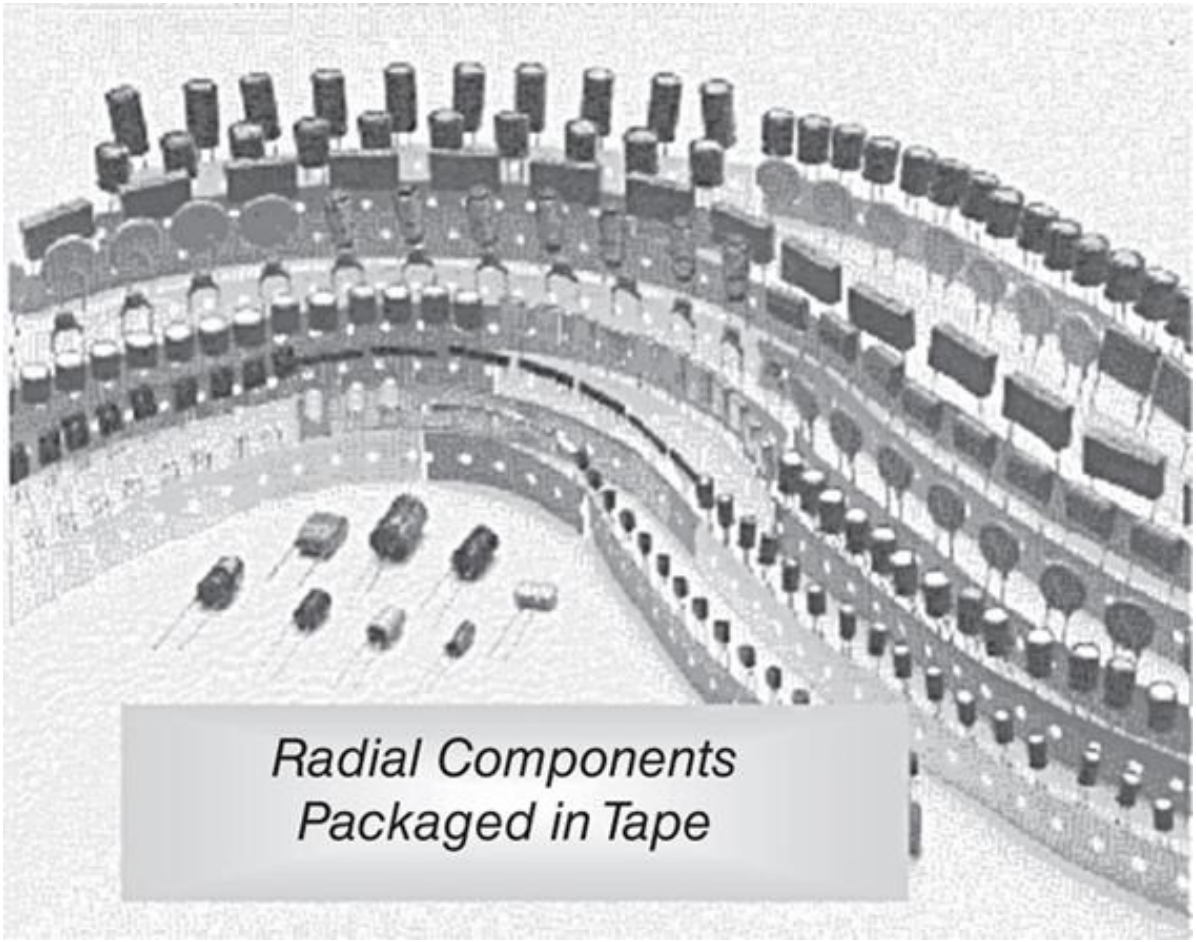


FIGURE 43.26 Radial components packaged in tapes that would come off of reels. (*Courtesy of Universal Instruments*.)

Several drawbacks are associated with tape carriers. For example, tall or heavy parts may change position or break the cover of deep-pocket tape carriers. The potential consequence is that the tape and/or components will jam or damage the feeder mechanism of the placement machine, thereby interrupting the assembly process.

43.4.3.1.2 Extruded Tube. Extruded tube is a commonly used format for odd-form components. See Fig. 43.27. Components such as D-Sub connectors, phone jacks, transformers, relays, and shrouded headers are typically supplied in tube packaging. Recently, component manufacturers have begun to supply long connectors such as single inline memory modules (SIMMs), DIMMs, and other designs of long-aspect ratios in edge-stacked tubes.

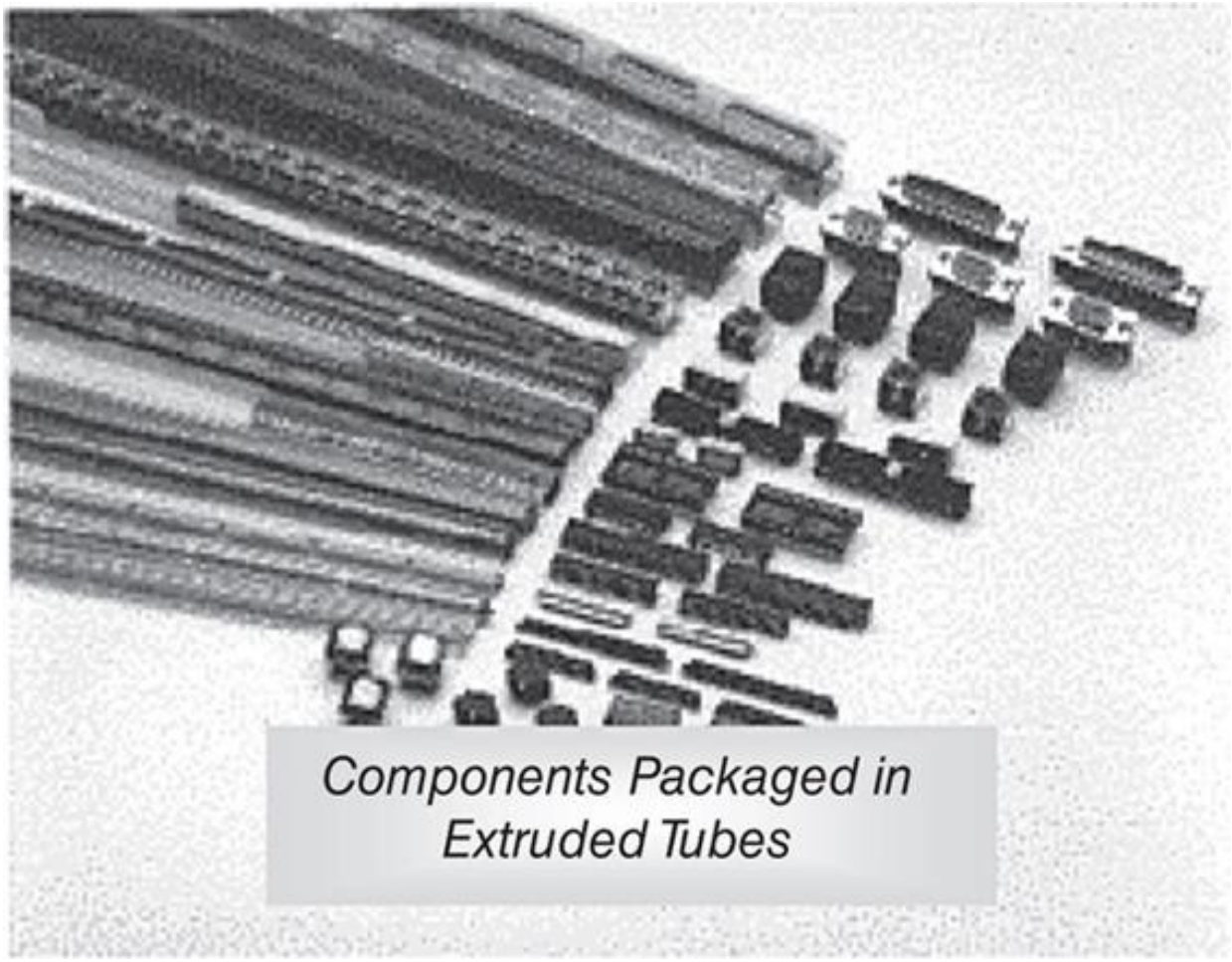


FIGURE 43.27 Components in tube packaging. (*Courtesy of Universal Instruments*.)

Tube packaging is particularly beneficial for protecting the component at a reasonable cost. Also, tubes are less likely than tape to cause problems feeding components into the placement machine. Of course, it is necessary to verify that the tube geometry is compatible with the feeder mechanism on the placement machine. The tube material should be sufficiently thick so as not to bend readily. Bending of tubes is the primary cause for the jamming of devices inside of them during the feeding process. Moreover, heavy components packaged in thin cross-sectional tubes may actually interfere with adjacent tubes when stacked in the automated feeder.

43.4.3.1.3 Matrix Trays. Matrix (or waffle) trays are an inexpensive means to supply components that are generally too large or heavy for tube or tape packaging and must be individually separated from one another. See Fig. 43.28. An important consideration is that the trays themselves may not be a suitable starting point for the automated placement processes especially for very small components. First of all, the components have too much room to move about in each bin to establish coordinates for initiating the pickup and insertion process. Also, component leads are not always oriented correctly in the insertion plane.

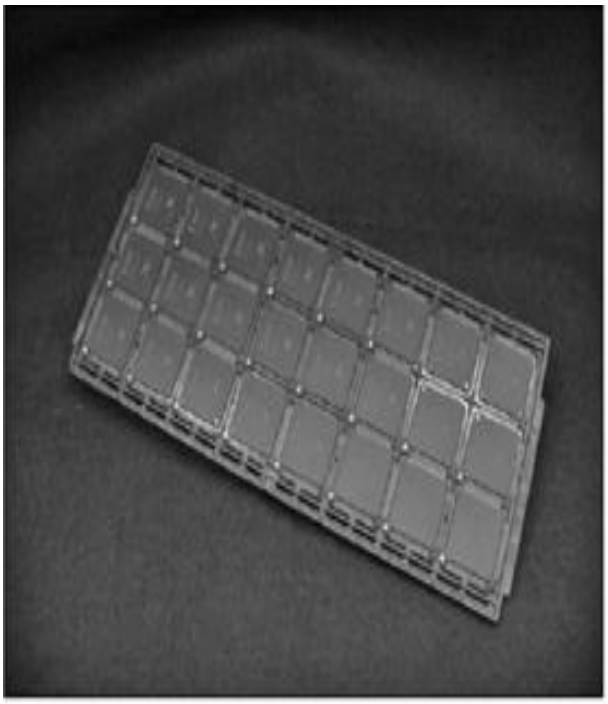


FIGURE 43.28 Components packaged in matrix trays. (*Courtesy of Sandia National Laboratories*.)

Several potential issues may need to be considered when choosing trays. Trays lack the rigidity required by many assembly machines for part pickup. Also, trays hold a more limited quantity of parts to the placement machine, and thus require more operator changeout during assembly. There are no standards for vacuum-formed trays that are used for odd-form components. Lastly, trays simply take up a greater amount of feeder space in a placement machine and on the floor.

43.4.3.1.4 Continuous Strip. Continuous strip packaging is designed for high-volume automation applications of odd-form components. This technique eliminates the need for separate component packaging formats because the individual parts are all attached in sequence to a single metal or plastic strip as part of the assembly process. The parts are located with a specified pitch that can be accommodated by the placement machine. Some components that are packaged in this manner include headers, battery clips, transformers, and motor brushes. Either the metallic part (e.g., brushes) or the leads that are part of the component can be stamped from a continuous strip of metal or thermosetting plastic. This type of packaging provides high levels of online parts inventory. However, such strips are application-specific and may carry a higher cost to automate due to the need for specially designed feed mechanisms.

43.4.3.1.5 Bulk. Bulk packaging eliminates the expense of component packaging altogether by simply placing the devices in a large container. A significant number of odd-form components are shipped in this format. Of course, the component manufacturer has likely established the cost/benefit of the fallout of parts due to handling and shipping damage versus the cost of added packaging by one

of the previously mentioned formats. On the other hand, the degree of part damage may not be acceptable to the circuit board assembly house because of increased downtime due to machine jams and part replacement.

Bulk packaging is the most difficult packaging format to automate for odd-form components. Generally, bulk components require a specially designed bowl feeder to supply parts to the machine with some degree of consistent orientation, which increases cost and process implementation lead times. Also, the unusual configuration of bowl feeders may require a dedicated placement machine (cell) that may have a significant idle time. The feeders usually take up considerable space and are not easily retooled for product changeover. The placement machine must have then the versatility to orient each part consistently from a haphazard “pile” of devices so that the pickup device can obtain each unit and correctly place it on the circuit board. In spite of these numerous drawbacks, bulk packaging is a cost-effective approach for odd-form components in numerous product applications.

43.4.3.2 Equipment. Advances continue to be made in the capabilities of odd-form assembly equipment. Early vintage, single-task robotic systems are giving way to machines that perform all of the alignment and functions of modern placement equipment, and which can be integrated into existing assembly lines. New machines are designed for speed and the flexibility to handle different odd-form component geometries as well as a variety of circuit board configurations.

Typically, automated odd-form component placement machines use an overhead gantry-style positioning system and vision and optics systems underneath the head. The emphasis is on placement accuracy given the high component density of surface-mount boards and, in some applications, the use of solder paste-in-hole printing methods

for a 100 percent reflow soldering process. The component must be placed accurately into the solder paste the first time so that the solder paste is not disturbed, which can result in potential defects. Interchangeable grippers and vacuum pickups as well as improved component feeding mechanisms provide greater flexibility for different product types, faster placement rates, and minimum equipment downtime.

43.4.4 Cleaning

The cleaning of assemblies having odd-form components, like the placement of those devices themselves, can occur at one of several points along the assembly process. If the components are placed prior to the principal soldering step, then they will be cleaned along with the rest of the circuit board. The higher temperatures of a Pb-free solder process can make this cleaning step somewhat more difficult, depending on the tenacity of the flux residues.

On the other hand, when the odd-form devices are soldered to the circuit board after the primary soldering process has taken place, the subsequent cleaning procedure must take into account the other components that are already on the circuit board, particularly potential handling damage. It may be preferred to use a no-clean or low-residue flux to minimize or eliminate the added cleaning step required for the later placement of odd-form components. Because odd-form components are often larger and/or have more complex constructions (geometry and materials), there is an increased likelihood of flux residues becoming trapped in confined areas. Therefore, the cleaning process must be sufficiently thorough to remove residues from those locations on the component. Similarly, it is necessary to verify that the cleaning solution has likewise been removed from those locations as part of the process.

43.4.5 Cleaning

The use of no-clean and low-solids fluxes has reduced the need to clean a greater number of circuit boards. Nevertheless, high-reliability electronics, as well as those used in harsh environments, may still require the removal of flux residues. The primary metric used to control the cleaning process is the quantity of residues that remain on the circuit board or components. Visual inspection (white light or ultraviolet light) and ionic testing are the two most commonly used methods to assess a cleaning step. In addition, in-circuit testing (ICT) provides a secondary means to indicate excessive residus presence. The residues prevent the electrical probe from reaching the conductor, which is registered as an “open” in the data collection routine. Unexpectedly large numbers of “open” defects may indicate excessive flux residues on the circuit boards as well as signify an actual electrical performance defect. Also, in the case of high-frequency circuit boards (radio frequency and microwave), ICT can identify flux residues as indicated by signal leakage and other parasitics when inspecting for electrical performance.

The cleaning step must be carefully considered for a Pb-free soldering process. The higher processing temperatures can increase the tenacity of residues, particularly those of fluxes designed for Sn-Pb processes. This point addresses fluxes used separately, as in manual or wave soldering, as well as the flux in solder pastes. The cleaning step may need to be enhanced to ensure that these residues are removed satisfactorily from the circuit board surface. On the other hand, flux formulations that have been developed specifically for the Pb-free soldering processes may create residues that are not compatible with cleaning processed developed specifically for Sn-Pb technology.

43.4.6 Network Communications

The generation, transmittal, and storage of process information is critical for real-time control of a circuit board assembly process, whether that process is for building consumer electronics in high volume or involves a low-volume assembly line for high-reliability military, space, or satellite electronics. The information that is generated by operators or automated machines on the shop floor typically includes commodity usage (i.e., circuit boards, components, etc.) as well as defects and machine malfunctions. Commodity usage information can then be made available to inventory control in the plant stockroom or even to the bill-of-material (BOM) suppliers across town and around the world, identifying the need for additional components, flux, and such at that particular site.

Process information is also accessed by the manufacturing engineer, who is monitoring the overall assembly flow, as well as by the process engineers or technicians who are directly responsible for equipment operations (e.g., furnace zone temperatures, flux levels, etc.). In addition, information may be shared between the different machines on an assembly line to prevent slowdowns in process flow due to equipment outage. Such slowdowns and stoppages can impact upstream steps. For example, there can be shelf-life issues with solder paste that is left out in a printer too long due to a stoppage created at a subsequent component placement machine or reflow oven.

It is often necessary to archive process-related information. Archived data are used to track defects as a means of process control. These data can assist in quickly determining the root cause of an out-of-control process. Process information can also be used to monitor long-term equipment performance, indicating the need for periodic preventive maintenance or machine replacement. Easy access to historical process information can also facilitate

the reintroduction of a particular product line with a minimum investment in process development efforts.

Finally, archived process data are useful in an investigation of field failures. The traceability of the troubled product to the exact process parameters used on the assembly line at that time, material lots, operators, and so on can be accessed; these data are invaluable for the follow-up root-cause analysis, particularly in the case of high-valued, high-consequence electronics systems (e.g., military equipment, space and satellite hardware, as well as medical and automotive electronics). Understanding the circumstances under which the defective product was made can also provide insight into implications regarding long-term reliability and specifically warranty costs versus liability and the need to implement a product recall.

The need to access information quickly as part of assembly operations extends beyond process and inventory control. Peripheral information such as equipment software and operations manuals must also be quickly accessible. The ready availability of boot-up software and instructions minimizes the downtime required to reestablish a product line or effect repairs on a malfunctioning machine.

Once the need for a network has been determined, the locations of terminals, servers, and information storage equipment must be established. Local area networks (LANs) and the World Wide Web (WWW, or Internet) can link access points located in adjacent rooms or halfway around the world. However, it is critical that the network uses consistent computer and data transmittal protocols in order to provide uninterrupted, information handling in an efficient manner. For example, serial communication via an RS-232 port is relatively common, but too slow for most machine applications. Ethernet communication via transmission control protocol/Internet protocol (TCP/IP) is a preferred method because most equipment suppliers offer this network option. The TCP/IP method allows computers to

share resources, no matter whether the operating system is for an Apple®, a version of the Microsoft® operating system for PCs, or the UNIX operating system. Also, the Semiconductor Equipment Communication Standard (SECS)/Generic Equipment Model (GEM) is widely used as the interface between the host computer and assembly machines.

Lastly, the need for efficient network communications is particularly acute with the advent of Pb-free solders. In the case where OEMs as well as contract manufacturing service (CMS) companies are assembling both Sn-Pb and Pb-free technologies, it is essential to control all aspects of the assembly process with precision. In fact, process control extends beyond simply certifying that the reflow, wave, or soldering iron correctly reflect the higher soldering temperatures. It must also make certain that components and circuit boards have been delivered to the appropriate process line having the correct surface finishes and/or MSLs. Also, process control must establish that other factors, such as flux type and cleaning procedures that may be unique to the Pb-free process, are being used on the appropriate product line.

43.5 PROCESS EQUIPMENT SELECTION

The selection of assembly process equipment is an extensive undertaking for the manufacturing engineer. The three principle variables are equipment utilization, costs, and physical plant requirements. These three areas are listed in order of consideration, not in the order of importance. The analysis behind equipment selection can be very complex, given the wide variety of product designs, potential automation options, and access to worldwide labor markets.

Unfortunately, the failure to consider thoroughly the details underlying any one of these three factors can result in a significant financial burden, lost time to market, and poor product quality/reliability for the OEM or CMS. The following sections provide relatively general discussions of these three areas. The reader is referred to many excellent texts on the topic of manufacturing engineering, as well as source books that specifically address assembly process equipment for electronics manufacturing.

43.5.1 Equipment Utilization

Equipment utilization refers to two aspects of the equipment. The first aspect is the operational time during which the machine is actually performing its intended function. The second aspect is production volume (expressed as parts or assemblies per unit time) provided by the machine while it is in operation. The consequences of operational time can be considered as follows: When the machine is performing its intended function, it is making product and as such is making a profit for the company. On the other hand, when a machine is idle, not only is it not making product (or profit), it may be losing money for the company. Those monetary losses result from wasted electricity and other utilities while the machine is on standby, labor costs for idle operating personnel, continued draw-down on the maintenance interval, and overall loss the equipment lifetime.

Next, equipment utilization is discussed in terms of throughput or product volume. It should be noted that the general approach is nearly the same for both Sn-Pb and Pb-free technologies. Only the specific cost factors may differ slightly between the two cases. A determination of equipment utilization requires that the appropriate metrics be defined that accurately reflect the machine activity. For example, in the case of component placement machines, the

utilization metric may be components placed per unit time or it may be the number of stuffed circuit boards that are completed per unit time. Printed circuit boards or finished assemblies per unit time are the typical metrics for paste printing and reflow furnaces, respectively. For example, component placement rates are expressed as, components per hour (CPH). Some manufacturing engineers prefer to analyze utilization in terms of time per product unit, which is the inverse of production rate. Such an approach would be exemplified by measuring the time required to print the paste on, or to stuff, a single circuit board.

It is important to select a metric that is most appropriate for the machine and the products that are processed in it. Moreover, the metric should allow the process development engineer to monitor the performance of the machine process accurately; it can also be used to compare specifications between different equipment brands for a procurement activity.

Different methodologies can be used to exercise an equipment utilization analysis. The details of these techniques are many and beyond the scope of this text. Nevertheless, it is important to be familiar with several key attributes that are used to make utilization assessments. Descriptive definitions of several attributes are shown below:

- *Theoretical throughput* is the output of a machine based upon its underlying design.
- *Actual throughput* is the output of the machine for the particular product line or application. This value is always less than the theoretical value.
- *Utilization or utilization efficiency* is the ratio of actual throughput to theoretical throughput.
- *Operation time* is the total time during which the equipment may be required to operate. For example, it

may be an 8-h shift or it may be 24 h if three shifts are running in the factory.

- *Equipment uptime* is the time that the machine is available to perform its task; it may not necessarily be performing the task. Therefore, this time period takes into account the various contributions to downtime, such as preventive maintenance, unexpected breakdowns, resupply of commodities, and so on.
- *Productive time* is the time during which the machine is actually performing its task.

These various attributes can be further broken down as the need arises; for example, several factors can account for loss of equipment uptime, including scheduled maintenance versus unexpected machine failures, commodity resupply, etc.

These attributes are reduced to mathematical variables that are used in equations to calculate the performance of a particular machine. However, the assembly process for electronic circuit boards is comprised of several machines or cells that are *in series*. Therefore, once the performance attributes are determined for a given machine, they must be integrated to predict the performance of the entire assembly line. For example, it is preferred that the throughputs of the individual machines be matched for the product application. A mismatch of machine capabilities can generate bottlenecks in the assembly process. The slowest machine or function then controls the production rate of the entire line. The obvious consequence of a bottleneck is an underutilization of the other equipment, which ultimately appears as an increase in manufacturing costs.

But there are also quality control reasons to smooth out the flow of bottlenecked assembly processes. For example, if the component placement machine has a throughput of 100 circuit boards per hour, but the reflow machine can only process 90 circuit boards per hour, then printed and stuffed

boards will spend time in the open factory air awaiting entry into the reflow step. The consequence is a degradation of paste properties, resulting in the increased likelihood of solderability defects and a drop in product yield. Such technical ramifications must also be addressed when considering equipment utilization for an assembly process.

43.5.2 Costs

There are several cost factors to consider when establishing an assembly line: the initial capital investment for the machine(s); depreciation and lifetime (obsolescence) of that equipment; operational costs such as labor rates, electricity, water, or the use of inert atmospheres; and maintenance support costs. Many of these cost factors are determined on a “per product unit” basis so that an estimate of potential production volumes is often required for their calculations. Many OEMs and CMS providers have had to establish their own cost models to take into account labor rates, energy costs, shipping costs, and tax structures that are specific to the assembly plant location—on-shore as well as overseas. Because of the cost variables just mentioned, it is difficult to establish a universal model for these calculations.

When addressing the implementation of Pb-free soldering technology, one must consider two aspects regarding equipment costs. First are the direct costs of purchasing and installing equipment that can provide a Pb-free assembly capability. Second is the cost of simply developing a Pb-free assembly line in the factory.

Regarding the first point, equipment capability vis-à-vis Pb-free solder pertains primarily to the soldering process, including the reflow furnace, wave-soldering machine, soldering irons, etc. Printing and placement equipment is largely unaffected by the Pb-free soldering technology. Most reflow equipment used for Sn-Pb soldering is nominally

capable of also supporting Pb-free soldering for moderately complex circuit boards. Changes are simply made to the time-temperature profile of a reflow furnace. On the other hand, for more highly complex products, a replacement reflow furnace may be required that has more than the typical five to seven zones. A larger number of zones allows more flexibility—and greater control—over the time-temperature profile. In the case of wave soldering, the exchange of Sn-Pb solder for a Pb-free alloy may also require the replacement of the pot, impeller, and baffles to prevent excess erosion by the higher Sn solders. Last, it is expected that erosion of soldering iron tips will be greater with the Pb-free solders. Tip technology has changed little from the Ni-coated or Fe-coated Cu core construction. Therefore, it may simply be a matter of stocking extra tips for those operators using Pb-free solders.

The second cost aspect addresses the manner in which a Pb-free capability is to be implemented on the factory floor. Specifically, the decision must be made whether to have separate Sn-Pb and Pb-free solder assembly lines or to mix the two technologies using the same assembly equipment. Critical factors include capital costs, factory floor space, infrastructure required to prevent inadvertent mixing of technologies, and projected product volumes. It is preferred to separate the two assembly capabilities physically. This separation is not limited to the actual machines, but also includes support functions such as solder material storage and component inventory control in order to prevent the use of the wrong solder or components and circuit boards with incorrect finishes. The extent of this separation of capabilities will determine the need for the capital investment in new machines as well as the cost of duplicating some support functions and personnel that are needed for adequate process control.

43.5.3 Physical Plant

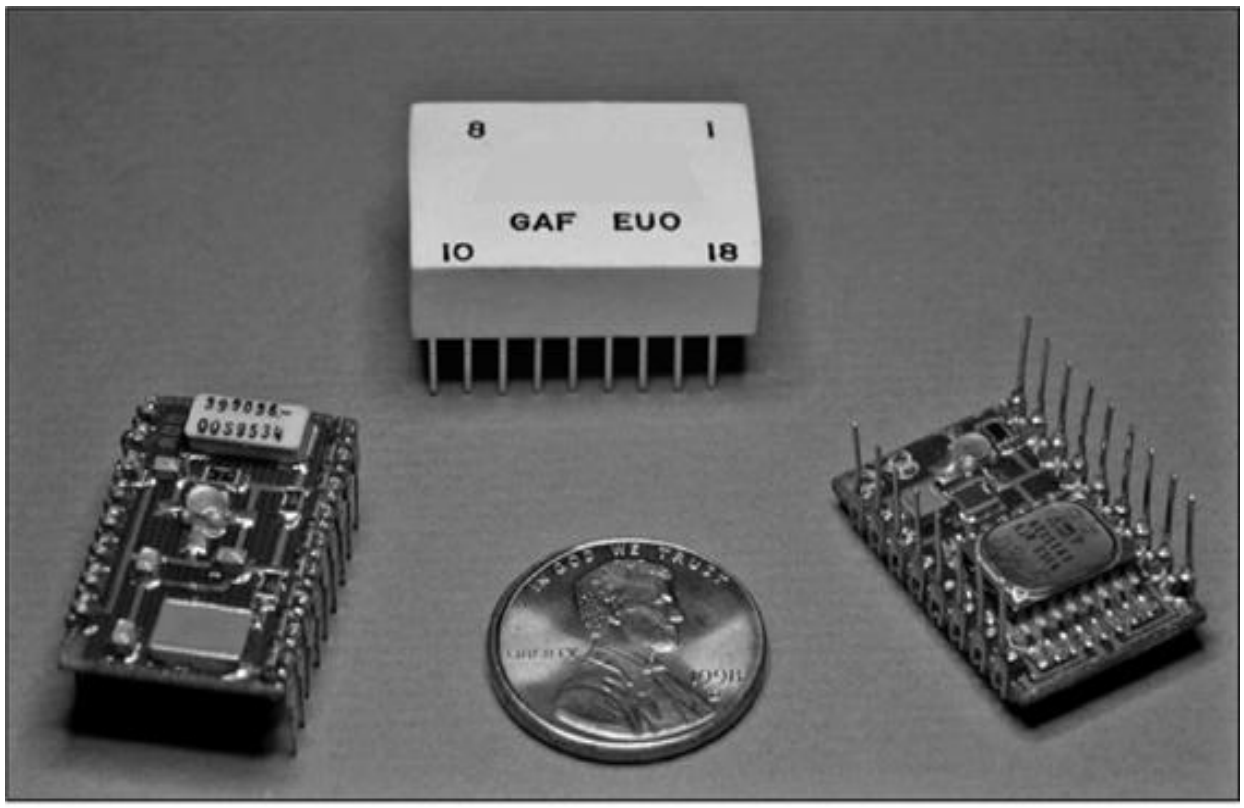
The cost of having a soldering process line extends beyond the capital costs of the equipment or even the labor costs for operators and process engineers. There are also the costs of operating the machines themselves. The factory must have adequate floor space for the assembly line footprint, as well as the access required to move parts and finished assemblies to and from the line. There are also space requirements to perform maintenance functions safely and make repairs to equipment. Finally, there are assembly costs arising from utility usage: electricity, compressed air (pneumatic actuators), and water (cleaning).

If the reflow or wave-soldering machine is to have an inert atmosphere—typically nitrogen is cheaper than argon—then it becomes necessary to select between the options for the gas source. Those alternatives are compressed gas tanks, a liquid nitrogen tank, or an onsite nitrogen generation facility. The compressed gas tanks are usually used only for short production runs. For most moderately sized electronics assembly factories, the most cost-effective option is to use one or more liquid nitrogen tanks, off of which is bled the nitrogen gas. Only for very-large-scale manufacturing facilities is an onsite generation plant the best option. Ancillary costs include the installation of pipe lines that transport the gas to the specific machine sites on the factory floor as well as the provision for adequate ventilation of the used gas from the machine to the external environment.

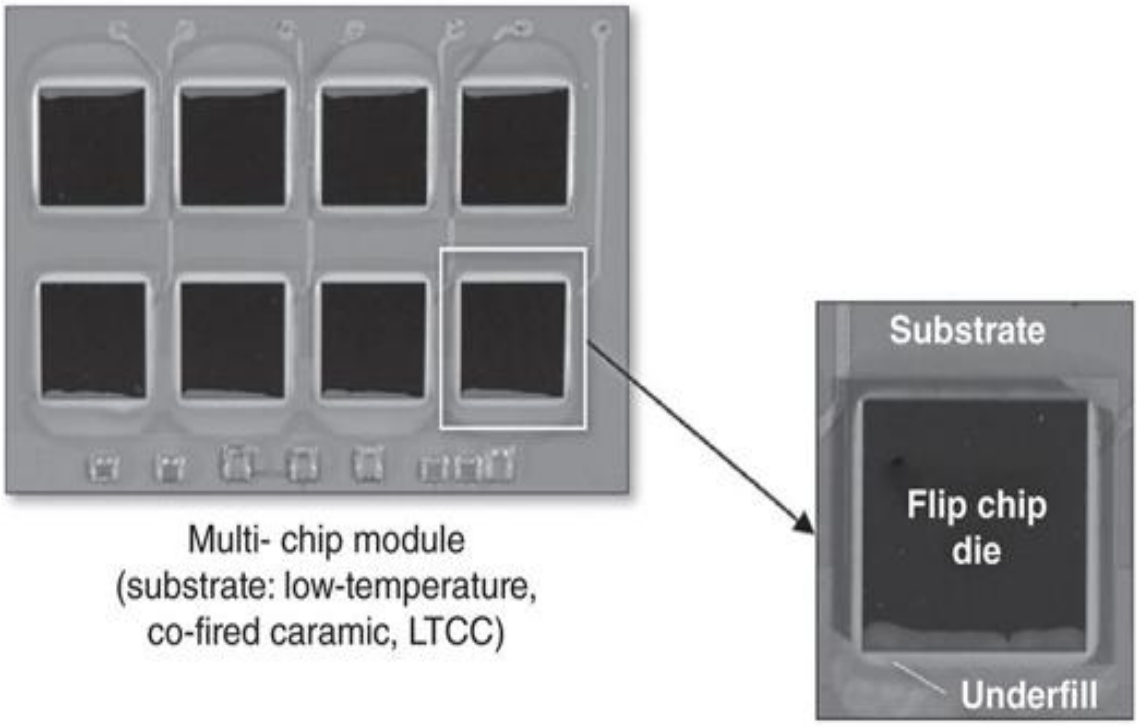
The physical plant costs are generally similar for both a Pb-free assembly process and a Sn-Pb line. The two possible differences would be electricity usage, which may be greater with the Pb-free line due to the higher soldering temperatures, particularly with respect to a reflow process, and the need for an inert atmosphere capability for the soldering machine.

43.6 CONFORMAL COATING, ENCAPSULATION, AND UNDERFILL MATERIALS

When required, the final steps in the assembly of a printed circuit board are the applications of conformal coatings, encapsulants, and underfill materials. Conformal-coated circuit boards are shown on the bottom of the stereo photograph in Fig. 43.29*a*; the same circuit board, encapsulated, is shown in at the top of the photograph. An example is shown in Fig. 43.29*b* of underfilled flip-chip devices.



(a)



Multi- chip module
(substrate: low-temperature,
co-fired caramic, LTCC)

(b)

FIGURE 43.29 Stereo photographs showing (*a*) conformal-coated (*bottom*) and encapsulated (*top*) versions of a surface-mount circuit board and (*b*) underfilled flip-chip components. (*Courtesy of Sandia National Laboratories*.)

The role of the conformal coating is to protect the circuit board and components against large-scale contamination from dirt, water, liquid chemicals, corrosive gases in air pollution, mold, and fungus. Because the layers are very thin (<0.25 to 0.50 mm) and relatively soft, they do not offer significant protection against handling damage or mechanical loads in shock-and-vibration environments. Protection against the latter conditions is obtained from encapsulants, also called *potting* materials, and underfill materials. Underfill materials perform a function similar to adhesives by securing the component to the circuit board. The difference is that the underfill material is applied after soldering and must fill the entire gap between the package and the circuit board. In the case DCA/FC, the underfill also improves the thermal mechanical fatigue reliability of the solder joints.

The details of these materials are discussed in other chapters. However, it is important to understand their role in the overall circuit board assembly process. First of all, the functions of these three materials require that they have good adhesion to all surfaces. Therefore, the printed wiring assembly must be cleaned of any flux residues as well as those residues left behind from the cleaning procedure.

Second, the application of conformal, encapsulant, and underfill materials must be tightly controlled in order for them to function properly. The nominal thickness and its uniformity are critical for conformal coatings. A coating that is too thin is a less effective barrier against harsh environments. Thickness and uniform coverage have become even more critical as many designers are relying on conformal coatings to mitigate the consequences of Sn whisker growth on 100 percent Sn coatings. On the other hand, a conformal coating that is too thick can interfere with

rework procedures as well as prevent fit-up of the circuit board into racks and backplane cabinets. In general, visual inspection is used as a nondestructive method to control the application processes.

In the case of encapsulant or potting materials, there must be complete filling of the mold, especially around the components, to prevent stress concentrations that can damage surface-mount solder joints. Potentially damaging stresses can also be generated when the density of the potting material varies excessively about the circuit board. The resulting variation of physical and mechanical properties of the foam encapsulant (thermal expansion coefficient, modulus, etc.) can lead to excessive board bending that damages solder interconnections, particularly those of large components (e.g., BGA devices). Therefore, it is necessary to control the encapsulant material itself as well as the "casting" process to prevent these defects.

Unfortunately, most nondestructive evaluation techniques are not effective at finding encapsulation defects. Voids and density variations are not readily detectable by visual inspection or by x-ray analysis. In the case of x-ray, the inherently low density of encapsulant foams limits the contrast between filled and unfilled (void) regions. Scanning acoustic microscopy (SAM) has had some limited success when the encapsulant layer is relatively thin, which is not often the case. Witness samples taken during the casting process are used to confirm foam density.

A number of studies have been performed that underscore the crucial requirement to control the underfill process used on flip-chip devices. Even small variations in underfill material properties (e.g., viscosity, percentage of filler, etc.) or the method for dispensing the underfill material between the die and substrate can significantly alter the long-term reliability of these interconnections.

The accepted method of nondestructive testing used to control the underfill process is SAM. The thin layer allows this

technique to detect voids in the underfill material, which when located near the solder interconnections can be responsible for a significant loss of thermal mechanical fatigue reliability. X-ray techniques can be used to monitor the density of the underfill material, specifically, the distribution of filler material within the layer under the die. Density variations can indicate a larger distribution of underfill mechanical and physical properties, which may affect long-term reliability performance of the solder joints. Quantitative image analysis can be coupled into SAM and x-ray analysis data to provide valuable process control tools for the factory floor.

43.7 ACKNOWLEDGMENTS

R. Boulanger is acknowledged for contributions to this chapter, which is based on “Assembly Processes,” *Printed Circuits Handbook*, 5th ed., Clyde F. Coombs, Jr. (ed.), 2001, Chap. 43. The author also wishes to thank M. Dvorack of Sandia National Laboratories for his careful review of the chapter.

[a] Paul T. Vianco, Sandia National Laboratories, Albuquerque, New Mexico, is acknowledged for contributions to this chapter, which is based on “Assembly Processes,” Chap. 40 in *Printed Circuits Handbook*, 6th ed. (McGraw-Hill, New York, 2008).

CHAPTER 44
CONFORMAL COATING

Jason Keeping
Celestica, Toronto, Ontario, Canada

44.1 INTRODUCTION

Once a circuit card assembly (CCA) has been fully assembled and tested, it often needs to be protected from the environments in which it will ultimately be used. Moisture, salt, dirt, fungus, and a variety of other contaminants as well as mechanical shock and vibration will cause failure on an unprotected assembly. The CCA's last line of defense against the elements is a thin layer of coating that conforms to the shape of all the part leads, solder joints, and other complex features on the completed CCA. This conformal coating (or flow coating) is applied as liquid, atomized material and/or vapor deposition to the fully assembled CCA, and is cured in place to form a protective layer of insulation for the assembly.

This chapter presents:

- An overview of the five basic conformal coating types

- Preparatory steps necessary to ensure a successful coating process
- Various methods of applying conformal coating
- Aspects for cure, inspection and demasking
- Repair and rework processes
- Design guidance on when and where coating is required, and which physical characteristics and properties are important to consider

44.1.1 Objectives and Applications for Conformal Coatings

Besides protecting the CCA from the elements, conformal coating also provides:

- Mechanical support for components during mild shock and vibration
- Electrical insulation for high-voltage components, especially at altitude
- Chemical resistance for various environment elements, especially harsh conditions
- Prevention of short circuits due to tin whisker growth from pure tin-plated part leads and cases[1]

Because of the extra cost involved with the cleaning, coating, curing, and touchup operations, conformal coating was usually reserved only for equipment that required high reliability, such as military and aerospace electronics, and equipment that needed to operate in severe environments. With the introduction of automated application robots, ultraviolet (UV) curable chemistries[2] and product migration from sterile to outdoor applications, conformal coating has become more common.

44.1.2 Overview of Types of Conformal Coatings

Conformal coating materials are available in five basic chemistries, each with multiple application methods and several drying/curing options. As such, no one material will fit every application, but the wide variety will allow the designer to select a material that meets most technical, budgetary, and manufacturing needs. The various coatings and their characteristics are summarized in Table 44.1.

TABLE 44.1 Conformal Coating Materials and Their Characteristics

	Material type	Urethane			Silicone			Epoxy				Acrylic			XY
	Cure methods	Solvent evap.	Heat cure	UV Cure	RTV	UV Cure	Catalyzed	Solvent evap.	Heat cure	UV Cure	Catalyzed	Solvent evap.	Heat cure	UV Cure	Vapor deposited
Application method	hand paint	x	x	x	x	x	x	x	x	x	x	x	x	x	
	dip	x				x		x				x			
	hand spray	x	x	x	x	x	x	x	x	x	x	x	x	x	
	automatic spray	x	x	x	x	x	x	x	x	x	x	x	x	x	
	selective coating	x	x	x	x	x	x	x		x	x	x	x	x	
	vapor deposited														x
Removal	Solvent	x	x	x	x	x	x	x				x	x		
	Thermal	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	Mechanical	x	x	x	x	x	x	x	x	x	x	x	x	x	x
	Plasma etch														x
Benefits	Easy to rework											x	x		
	moisture resistent	x	x	x	x	x	x					x	x	x	x
	simple cure											x	x	x	
	Biologically compatable														x
	High temperature use				x		x	x	x		x				
	Abrasion resistent	x	x	x				x	x	x	x				x
	Solvent Resistent		x	x					x	x	x				x
	Complete coverage														x
	Reversion resistent		x	x								x	x	x	x
	Cold temperature Use		x	x	x	x	x								x
Risks	High VOC	x	x					x				x			
	Requires strict viscosity control											x			
	flammable											x			
	aided by primer				x	x	x	x	x	x	x				x
	cure affected by thickness and mass		x						x				x		
	cure inhibition or reversion	x					x	x			x	x	x		
	High cure shrinkage								x				x		
	not for low temp	x						x	x				x		
	Incomplete cure in shadow			x		x				x				x	
	Has pungent odor			x		x				x	x			x	
	Brittle at high temp			x						x				x	
	rework difficult			x				x		x	x			x	x
	UV wavelength affects cure			x						x				x	
	potential for contamination							x							
	difficult process							x							x
	Poor edge cure								x						
	Short work life				x						x				
	Moisture affect cure	x													
	Long complete cure time	x													
	Health and safety concern	x													
	Violent reaction with water		x												
	Requires moisture for cure				x										
	Low abrasion resistance				x	x	x								
	High CTE				x										
	May contaminate other products				x	x	x								
	Intermittant solvent resistance				x	x	x								
	difficult adhesion						x								
	batch process														x
	Full masking required														x

The five basic chemistries are

1. *Urethane:* This coating has good moisture and chemical resistance and good electrical insulation.
2. *Silicone:* Being soft and having good adhesion, silicone is useful over a wide temperature range.
3. *Epoxy:* This coating is tough, durable, and very chemically resistant.
4. *Acrylic:* Acrylic is easy to apply and remove.
5. *Para-xylylene:* This very thin, pinhole-free coating is vapor deposited instead of being applied as a liquid.

More information on the less common types of conformal coating may be found in IPC-HDBK-830.[3]

Currently, there is a new coating type (type UT) that is within industry review for final publication and release. These coatings are labeled UT since their application thickness is much less than that of the current para-xylylenes (type XY) coatings. These coatings are within the nano-thickness ranges.

44.1.3 Environmental Issues

The predominant environmental issue with coatings was the use of solvent thinners to aid the application process. Most coatings are available in low-solvent or zero-solvent formulations, so that the emission of solvents can be reduced or eliminated. The change to lead-free solders and plating has produced an increase in the use of conformal coatings, since conformal coating has been shown to prevent tin whiskers (see Chap. 49 on tin plating) from causing short circuits, and is used for that purpose in types of products that have not been coated before. The higher-temperature lead-free soldering processes are irrelevant to the conformal

coating step, since the coating is applied after the soldering process.

44.2 TYPES OF CONFORMAL COATINGS

The most commonly used types of conformal coatings include

- Urethane (type UR)
- Silicone (type SR)
- Epoxy (type ER)
- Acrylics (type AR)
- Para-xylylenes (type XY)

44.2.1 Urethane (Type UR)

Urethanes are relatively easy to apply with dip, spray, or brush. Cure times (other than UV curable) range from a few hours for two-part heat curable, to several days for a single-part room temperature cure. Typical application is 0.001 to 0.005 in thick. They are often used for space applications due to their low outgassing characteristics.

44.2.1.1 Chemistry. Urethanes are based on a diisocyanate and polyol backbone. They are available in solvent evaporative cure, heat cure, and UV cure formulations.

44.2.1.2 Properties. Since urethanes are polymerized and cross-linked in place, they have excellent resistance to chemical, moisture and solvents. They are available in hardnesses ranging from tough, abrasion-resistant varieties

to low-modulus versions suitable for extreme temperature ranges (see Fig. 44.1).

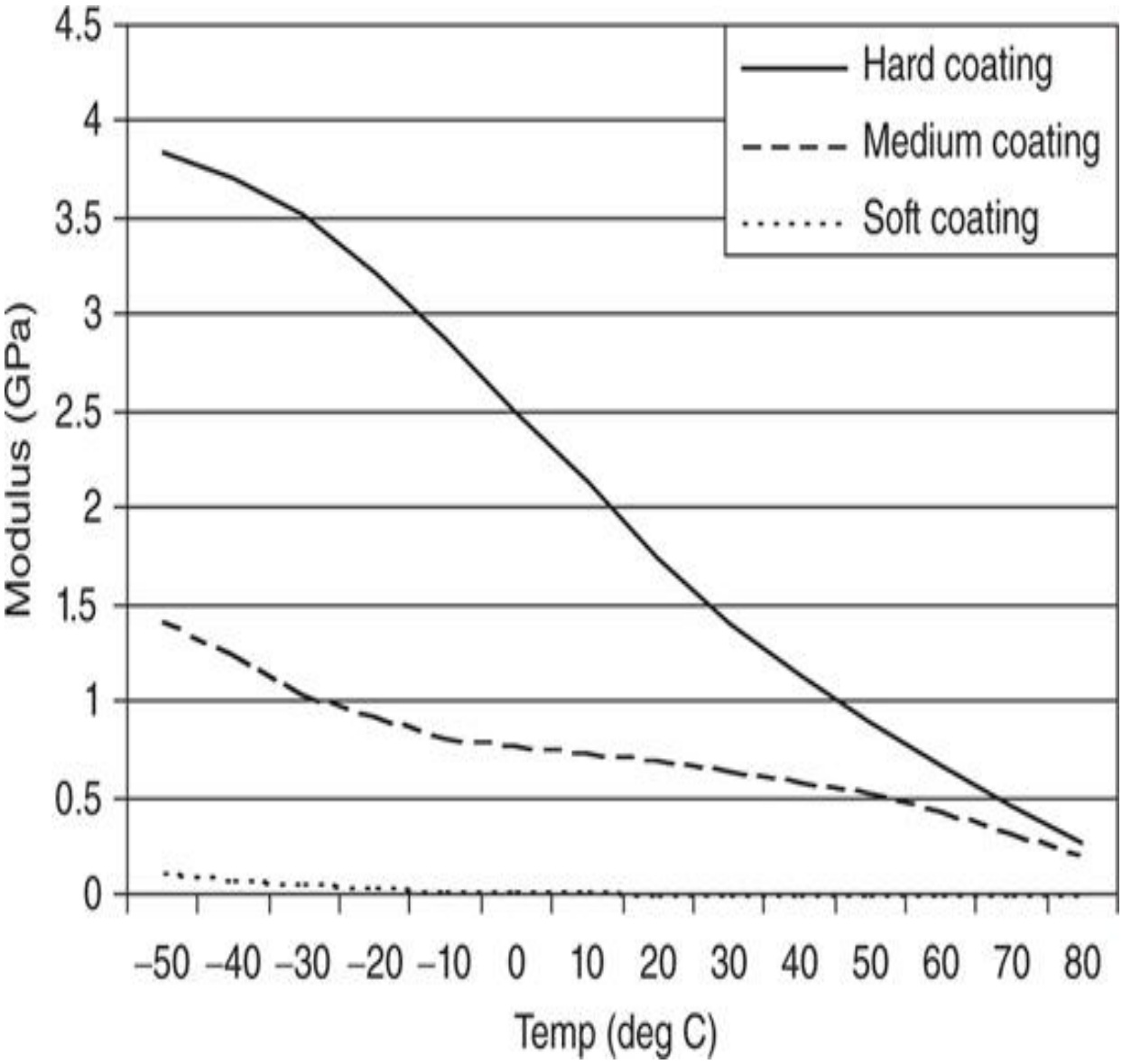


FIGURE 44.1 Elastic modulus versus temperature for three different type UR coatings.

44.2.1.3 Advantages and Disadvantages. Urethanes have good adhesion to most materials, including epoxy part bodies, metals, and ceramics. As such, the coating process is fairly robust. Since urethanes are chemically resistant, they are also difficult to remove except by thermal or mechanical

means. Urethanes can be soldered through, although this often results in a brownish discoloration that must then be removed.

44.2.2 Silicone (Type SR)

Silicones are very flexible, and stay that way over a wide range of temperatures. They have good adhesion to a variety of surfaces, but contaminate the surface and, once applied, prevent other materials from adhering. Typical application is 0.002 to 0.008 in thick. They are often used in automotive applications, where high temperature and moisture-resistance are needed.[4]

44.2.2.1 Chemistry. The silicone polymer chain is based on an alternating silicon-oxygen backbone. SR coatings are available in three types, room temperature vulcanizing (RTV), UV cure, and catalyzing (addition) cure.

44.2.2.2 Properties. Silicones have relatively stable properties from –55 to 200°C. Their coefficient of thermal expansion (CTE) is higher than that of urethanes, but this is mostly offset by their lower modulus, so that the level of stress exerted on parts is still relatively low. They have high resistance to moisture and humidity, as well as polar solvents.

44.2.2.3 Advantages and Disadvantages. Silicones are usable over a wide temperature range and are relatively easy to remove via mechanical or thermal means. If mishandled, silicones may contaminate the work area, causing adhesion problems on other CCAs. Careful process sequencing and process separation is necessary to prevent this.

44.2.3 Epoxy (Type ER)

Epoxies are chemically stable and very resistant to chemical attack. Typical application thicknesses are 0.001 to 0.005 in. Epoxies are useful in extreme environments where chemical vapors or high temperatures are present.

44.2.3.1 Chemistry. Epoxy coatings are based on epoxy resin systems and come in four types: solvent evaporation, heat curing, UV curing, and catalyzed.

44.2.3.2 Properties. Epoxies have a low CTE that matches well with printed wiring board (PWB) epoxy resin, since they share very similar chemistry. They have a higher T_g than most of the other coating materials. They are also very tough and abrasion resistant, so that rework is very difficult; epoxy coating can form the basis of an antitampering coating.

44.2.3.3 Advantages and Disadvantages. Epoxies are useful at moderately high temperatures, up to about 150°C. Because of their strength, they also provide mechanical support for components. The disadvantages of epoxy coatings are their usually pungent odor and the possibility of skin irritation. They are difficult to rework. Some formulations of epoxies are chemically delicate and do not cure properly in the presence of inhibiting compounds. Cure shrinkage is also of concern for fragile components; a softer buffer coating should be applied locally before the epoxy, particularly for assemblies that need to withstand wide swings in temperature.

44.2.4 Acrylics (Type AR)

Acrylic coatings are applied 0.001 to 0.005 in thick and are often used in military and consumer electronics.

44.2.4.1 Chemistry. Acrylic coatings are usually supplied as dissolved prepolymerized acrylic chains. The acrylic chemistry does not cure by polymerization and cross-linking as the other coating materials do, but instead hardens gradually as the solvent evaporates. Acrylics are also available in heat-curable and UV-cured formulations.

44.2.4.2 Properties. Acrylics are easy to apply, and are the easiest coating to remove, since relatively mild solvents soften and dissolve the acrylic coating while leaving the epoxy encapsulated parts and PWB unharmed. They can be cured quickly.

44.2.4.3 Advantages and Disadvantages. The greatest strengths of acrylic coating are the ease of rework and the fast room temperature cure. Acrylics provide good moisture resistance and fluoresce easily, aiding inspecting under UV lamps. Since they are so easy to rework, acrylics are also susceptible to inadvertent chemical attack from solvent splash during hand cleaning of solder joints elsewhere in the assembly. The high emission of solvent inherent in the acrylic process makes them less environmentally friendly than other materials. As the solvent evaporates, the coating shrinks and exerts stress on the components, so acrylics may not be suitable for all low-temperature applications.

44.2.5 Para-Xylylene (Type XY)

Para-xylylene coatings are unique, since they are applied by vapor deposition (see Sec. 44.4.6) rather than as a liquid. They are applied 0.0005 to 0.002 in thick. Para-xylylene coatings are often used in biomedical devices due to the inert character of the coating.

44.2.5.1 Chemistry. XY coating is supplied as a dimer, a polymer chain only two units long. During the vacuum deposition process, the dimer powder is gradually vaporized and is recondensed onto the CCA, polymerizing with the material already deposited. Typical application is 0.0005 to 0.002 in thick.

44.2.5.2 Properties. XY coating is chemically inert and moisture-resistant. Very thin, uniform layers are possible, with no pinholes or voids. XY coating also has very high dielectric strength. Due to the nature of the deposition process, no volatiles are generated.

44.2.5.3 Advantages and Disadvantages. XY coating is the highest performing coating in many regards. It has the highest dielectric strength, and is the lightest weight, lowest outgassing, mostly chemically inert, and most moisture-resistant. It provides the most uniform coating over, under, and inside parts where liquid coatings cannot be applied. The coating process must be performed in batch mode, using specialized coating equipment. It may be impossible to mask adjustable components such as potentiometers adequately. Rework is difficult; since the thin coating cannot be peeled, a microabrasion process is usually required to remove the coating. Additional staking or adhesive bonding of parts is required, since the thin coating provides little mechanical support.

44.3 PRODUCT PREPARATION

Most coating problems can be traced to improper preparation. The four preparation steps are

1. Cleaning to remove flux, oils, and contaminates
2. Masking to ensure coating is applied only where desired

3. Preparing the surface or priming to promote adhesion of the coating
4. Baking out to prevent moisture from being trapped under the coating

44.3.1 Cleaning

Thoroughly cleaning the CCA before conformal coating is the best way to ensure proper adhesion of the coating. The various cleaning chemistries and their effectiveness on different kinds of fluxes are treated in depth in Chap. 45, “Fluxes and Cleaning.” Besides removing flux, the cleaning process removes any contamination such as mold release agents on plastic part bodies, fingerprints, etc. No-clean fluxes reduce the need for waste water and waste solvent treatment. For boards that require conformal coating, the benefits of a no-clean system must be balanced with the risks of poor coating yields. A minor change in flux or coating chemistry could render the coating incompatible with the no-clean flux being used, causing delamination, cure inhibition, or other defects. In general, coating results are not as good with no-clean flux as with standard flux plus cleaning, yet in some cases may still be adequate to do the job.

44.3.2 Masking

To control the areas where coating is applied, some kind of masking is usually needed. Masking tapes or adhesive circles may be used to keep flat areas and holes free of coating. Since the tape needs to be removed completely after the coating operation, the tape adhesive must be capable of withstanding the cure temperature without peeling or becoming permanently bonded to the surface. To mask irregular surfaces, latex masking material is used. This

material is applied with automatic or manual dispensing equipment and is cured in an oven before the coating operation is performed. It then peels off easily after coating. For high-quantity production, boots or covers can be molded to fit over the areas that do not require coating. These are reusable, easy to install, and produce well-defined repeatable results. Rather than being masked, areas may be sealed with a permanent bead of a thixotropic (nonrunny) adhesive. This eliminates the demasking step, and is useful for complicated geometries such as the back of connectors and the perimeter of ball grid arrays (BGAs).

44.3.3 Priming and Other Surface Treatments

The adhesion of some coatings—notably epoxies, silicones, and para-xylylenes—will be improved if the CCA surface is primed before coating. Primers are applied as a very thin coat using dip or spray (generally the thinner the better) and oven-dried to drive any remaining solvent from crevices, vias, and such. If the primer fails to wet all areas of the board, the coating will not wet either but will easily delaminate instead. Such surfaces are not compatible with the primer, and an adjustment in primer chemistry is required. For difficult surfaces, such as large fluoropolymer parts or substrates, a more aggressive measure such as plasma-etch or mechanical abrasion may be needed to promote adhesion. Mechanical abrasion (grit blasting) may be used to roughen troublesome surfaces to promote coating adhesion. It may be easier to do this step as the parts are fabricated (in the case of mechanical parts) or as part of the make-ready process before assembly. Microabrasion can be used with proper care on the finished assembly as long as electrostatic discharge is controlled by the design and use of the abrasion equipment, and is monitored daily to ensure

that it is working properly. Microabrasion is also a viable method for removing coating (see Sec. 44.6.4).

Another aspect that can impact the ability of a coating to adhere to a substrate is the surface energy of the substrate. In general, a rough substrate, having high surface energy, will exhibit better wetting and coating adhesion than a smooth substrate, having low surface energy, all other factors being equal (which of course, seldom happens). A good example is comparing the adhesion of a conformal coating to the surface of a ceramic DIP component vs. a plastic bodied DIP of the same configuration. Smooth plastic surfaces, often compounded by the presence of fluorinated (e.g., Teflon™) or silicone mold release agents from the injection molding process, may show a higher incidence of coating delamination in thermal cycling due to surface energy conditions.

44.3.4 Measuring Surface Energy

There are a number of general methods for measuring or estimating the energy of a surface prior to coating application.

1. *Dyne pens:* These are liquid filled pens, similar to highlighting markers (see Fig. 44.2). Each pen body contains a solution with a calibrated surface tension. The most commonly available commercial sets start with 30 dynes/cm and end with 44 dynes/cm. In use, the marker tip is drawn across the substrate surface. If the solution does not immediately “bead up” or dewet, then the next higher pen is tried in an adjacent area. If a solution of 34 does not dewet and a solution of 36 does dewet, then the surface energy is judged to be 35 dynes/cm. This method is relatively inexpensive, very quick to use, but is variable and requires operator judgment.

FIGURE 44.2 Standard dyne pen samples.

These commercially available pens are very economical and it is often easier to purchase a set than to make your own solutions. However, if solutions are desired for measuring outside the range of 30 to 44 dynes/cm, individual solutions can be formulated using the information found in ASTM-D-2578, titled “Wetting Tension of Polyethylene and Polypropylene Films.” This test method focuses on measuring the surface energy of polyethylene and polypropylene films, but the test method includes the procedures on mixing the necessary solutions.

The methods in D-2578 use combinations of reagent grade formamide (HCONH2) and reagent grade ethyl cellosolve (CH3CH2OCH2CH2OH) to create solutions ranging from 30 to 56 dynes/cm. Be advised that both ethyl cellosolve and formamide are toxic and pose exposure risks.

General rule of thumb: When examining the surface energy of a substrate with dyne pens, the following general guidelines can be used (Table 44.2).

TABLE 44.2 General Guidelines When Using Dyne Pens

Surface Energy, dynes/cm	Expected Result
Above 40	Adhesion expected to be good
35–40	Adhesion generally good, with some intermittent delamination under severe conditions
30–35	Adhesion generally poorer, with increasing incidence of delamination under severe conditions
Below 30	Coating adhesion poor in any climatic testing

A great many factors affect coating adhesion, but all other factors being equal, this scale can be used to determine an overall degree of risk for coating delamination during environmental stress screening tests.

To show how surface energy can have an impact in production and reliability, the following illustrations are provided.

Illustration 1:

Company A used a solder mask coated coupon as part of its process control methodology for the conformal coating process. Each day, operators would coat the coupon using methods similar to those being used on production hardware. Following the standard cure methods, the coupons would be allowed to sit for one hour. The coupons would then have a 1″ × 1″ X scribed into the coating using a sharp razor blade. A standard tape was applied to the surface of the scribed coating and then pulled off. The coating was to have no loss of adhesion in the scribed area. While the company had numerous qualified solder masks, surface energy was never part of the qualification protocol, and the coupons were standardized on the most common solder mask used. Failures in the tape test were seldom encountered, but always passed in a subsequent

retest. All was well and good with the world, the workers were content, and the feudal lords of production smiled.

Then, during the same week, multiple failures began to occur in the process control coupons at multiple manufacturing sites. While processes between sites were similar, it was highly unusual for such failures to occur. The quality assurance policies of company A required that hardware be visually examined after product burn-in testing. No evidence of any coating delamination was found for the hundreds of complex assemblies examined. The loss in productivity and delays in shipment easily ran in the $250,000 to $500,000 range.

After extensive root cause analysis, it was found that the solder mask on the control coupons had been changed. The drawings allowed for any solder mask that was on the approved list, and only tribal knowledge was used in ordering the coupons. The mask was always assumed to be the same. The previous surface energy of the solder mask was in excess of 44 dynes/cm when using the dyne pens. The surface energy of the new solder mask was 30 dynes/cm. The inventory control system for the coupons was done in large lots to keep the per part prices low. The production problems began when the supply of the old coupons was exhausted and the supply of new coupons began.

Fearing that this meant a large scale quality problem, a sampling of unpopulated circuit boards was made for all vendors and all solder masks, again using the dyne pens. All bare boards were found to have surface energies in excess of 40 dynes/cm, which was deemed to be acceptable. Circuit boards go through a much wider range of chemical processes during board fabrication, such as plating and etching, and so have a higher surface energy as the mask surface is etched at the microscopic scale. In contrast, the coupon processing methods were very simple and did not have such exposure, creating the wide

disparity in surface energy between coupon and bare board, even for the same solder mask.

Illustration 2:
As noted, one of the elements which can impact the ability of a coating to adhere to a substrate is the surface energy of the substrate. In general, a rough coating, having high surface energy, will exhibit better coating adhesion than a smooth coating, having low surface energy, all other factors being equal.

To validate this surface energy adhesion, there are a couple methods, such as the IPC-TM-650(2.4.1.6) Adhesion test. This Adhesion test is a destructive test method that is completed by etching a cured conformal coated surface and placing a calibrate tape of adhesion strength and measuring the amount of material loss. Once this test is passed and there is no adhesion loss noticed, the assumption is that you have full adhesion with no potential for conformal coating peeling. However, this is not fully true. If the IPC Adhesion test is passed, however the surface energy below the conformal coating material is below 40 dynes/cm, there can still be a field failure for conformal coating adhesion as noted earlier within the table of surface energies for reference. This potential field failure aspect is only presented as a cured conformal coated material on an assembly is environmentally tested within a cycle consisting of high and low temperatures. In that, as the assembled is cycled the conformal coating material pulls away from the surface area during the heating process and starts to form aspects of a peeling/cracking within the coating area as cooled (see Fig. 44.3).

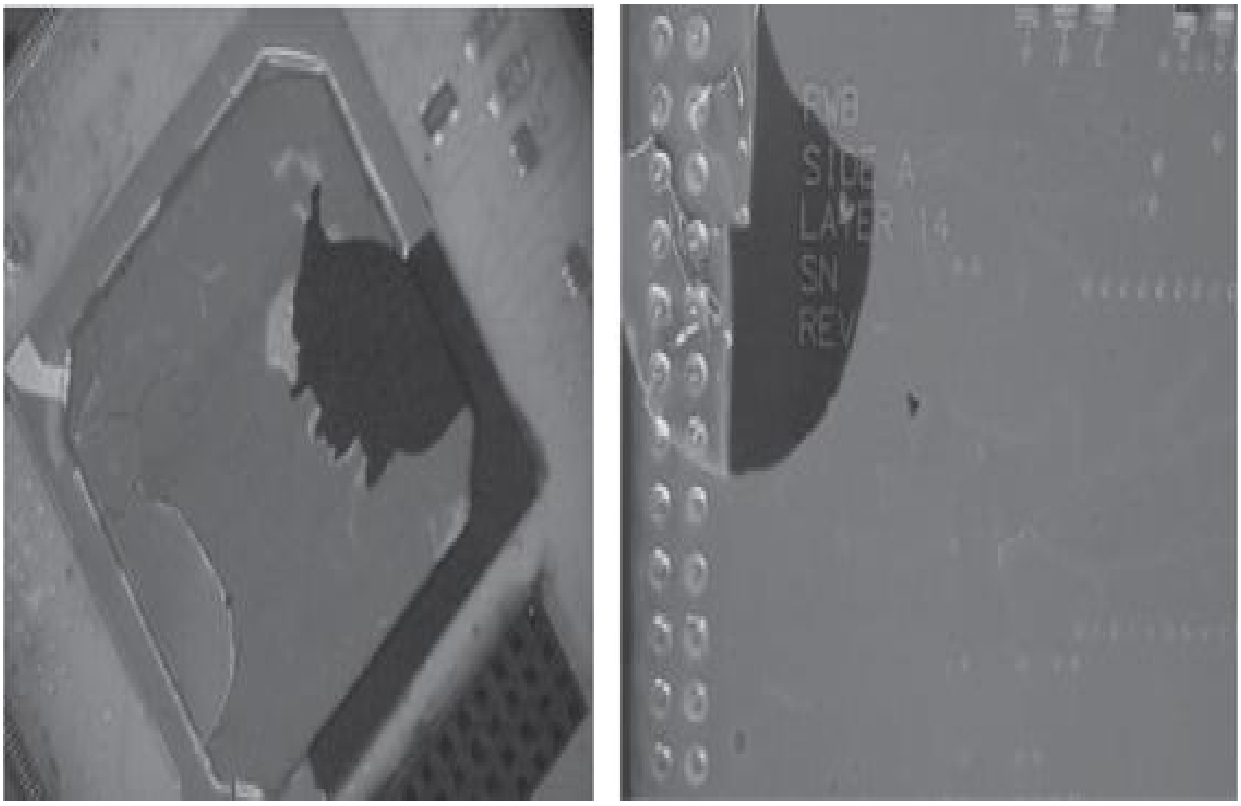


FIGURE 44.3 Cracked and peeling coated areas.

2. *Water break test:* One relatively inexpensive qualitative method for examining the surface energy of a substrate is a test commonly called a “water break” test. This test is common in the printed wiring board fabrication industry to examine the surface energy of a substrate prior to the application of solder mask. The test is also common prior to plating and anodizing operations.

The formal test method can be found in ASTM-F-22, titled “Standard Test Method for Hydrophobic Surface Films by the Water-Break Test.” This test method covers the detection of the presence of hydrophobic (nonwetting) films on surfaces and the presence of hydrophobic organic materials in processing ambients. When properly conducted, the test will enable detection of molecular layers of hydrophobic organic contaminants. On very rough or porous surfaces, the sensitivity of the test may be significantly decreased.

To paraphrase the test methodology:

- Take a cleaned and dried part and set it in a vertical position.
- Use a spray bottle containing distilled water.
- Spray the part two to three times from at least 6″ away.
- If the part is clean and free of oily residue, the water spray should sheet off.
- If some oily residue remains, the water will tend to adhere in droplets or patchy, nonuniform slicks.

Alternatively, apply several drops of distilled water to the cleaned surfaces. If the surface is inadequately cleaned, the spherical form of the drop is largely retained, and the surface must be cleaned once more. If the water runs on the treated surface, then wetting has been satisfactory and the part is ready for subsequent operations.

Caution: This test can be “fooled” by certain wetting agents, which will cause a continuous liquid film to spread over the metal surface even though the surface still has grease or oil on it.

This difficulty can be overcome in certain cases by dipping the parts in a dilute sulfuric or hydrochloric acid solution (the acid inhibits or destroys the “spreading power” of the wetting agent so a more truthful test result is obtained) and then rinsing again. Keep in mind that even with a good water-break test the surface still may contain soils.

3. Solder Mask Handbook—in Handbook can cut paste from existing document.

IPC-HDBK-840, titled “The Solder Mask Handbook,” discusses solder masks and surface energy.

A practical method for surface direct surface energy measurement and A to B comparison revolves around the simple concept of placing a known volume of a liquid on a surface and then just measuring the resulting drop

diameter. With a micro-liter pipette, it is fairly easy to place many small drops on a substrate and then measure the resulting drop diameter by any number of methods such as optically with a microscope, or mechanically with a caliper. If one desires to go through a very long geometric proof, the drop diameter can be directly related to the contact angle, which in turn can be related to the surface energy. Figure 44.4 shows this relationship for a 5 µL DI water droplet at 50 percent RH. So, it is fairly quick and low cost to place a number of 5 µL drops on a surface, measure the diameter and the relative humidity, convert drop diameter to surface energy and come up with a fairly accurate estimation of the substrate surface energy. The application of this test method isn’t limited to just DI water. Correlations for other fluids and/or curing materials can be obtained.

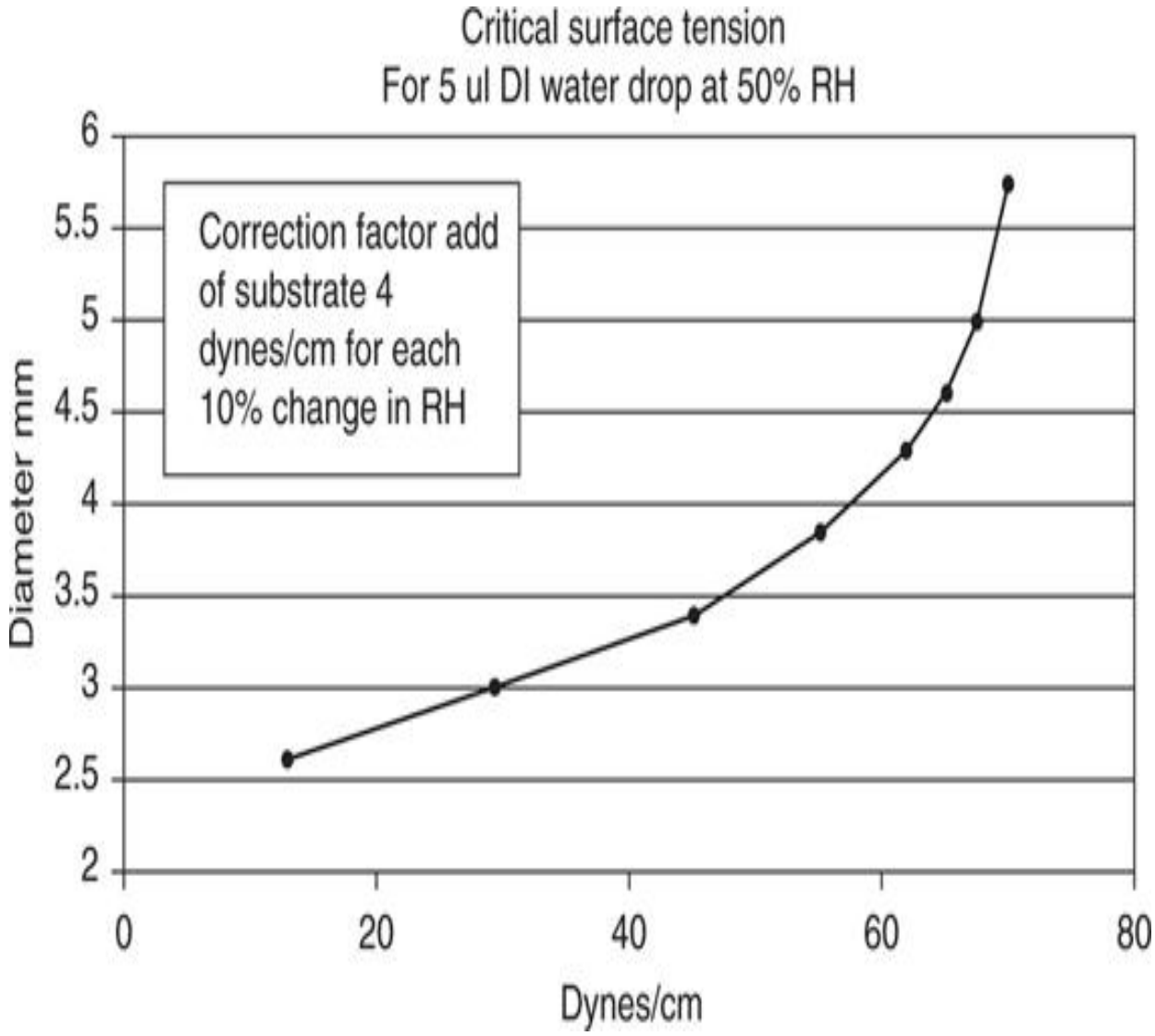


FIGURE 44.4 Critical surface tension for 5 uL of DI water drop at 50% RH.

Illustration 1:

The following example of applied surface energy shows how this test method may be applied to a silicone conformal coating. This example shows the interaction between materials (flux, solder mask)[5] and process (the wave soldering process). Just like the previous DI water example this example applies a known and controlled volume of a conformal coating and then measures the resulting drop diameter after the conformal coating cures.

A 5-µL drop of a conformal coating was applied to various substrates which were previously exposed to different fluxes (same basic flux formulation with different surfactants). This example shows that a no-clean flux formulation with a fluoro-surfactant had a major impact on the conformal coating wetting. The fluoro-surfactant significantly reduced wetting when compared to another potential flux ester based surfactant. Again, the amount of wetting directly corresponds to the relative drop diameters (i.e., a large drop diameter indicates improved wetting). In this example, to solve the coating wetting issue, the production wave soldering flux formulation was changed (see Fig. 44.5).

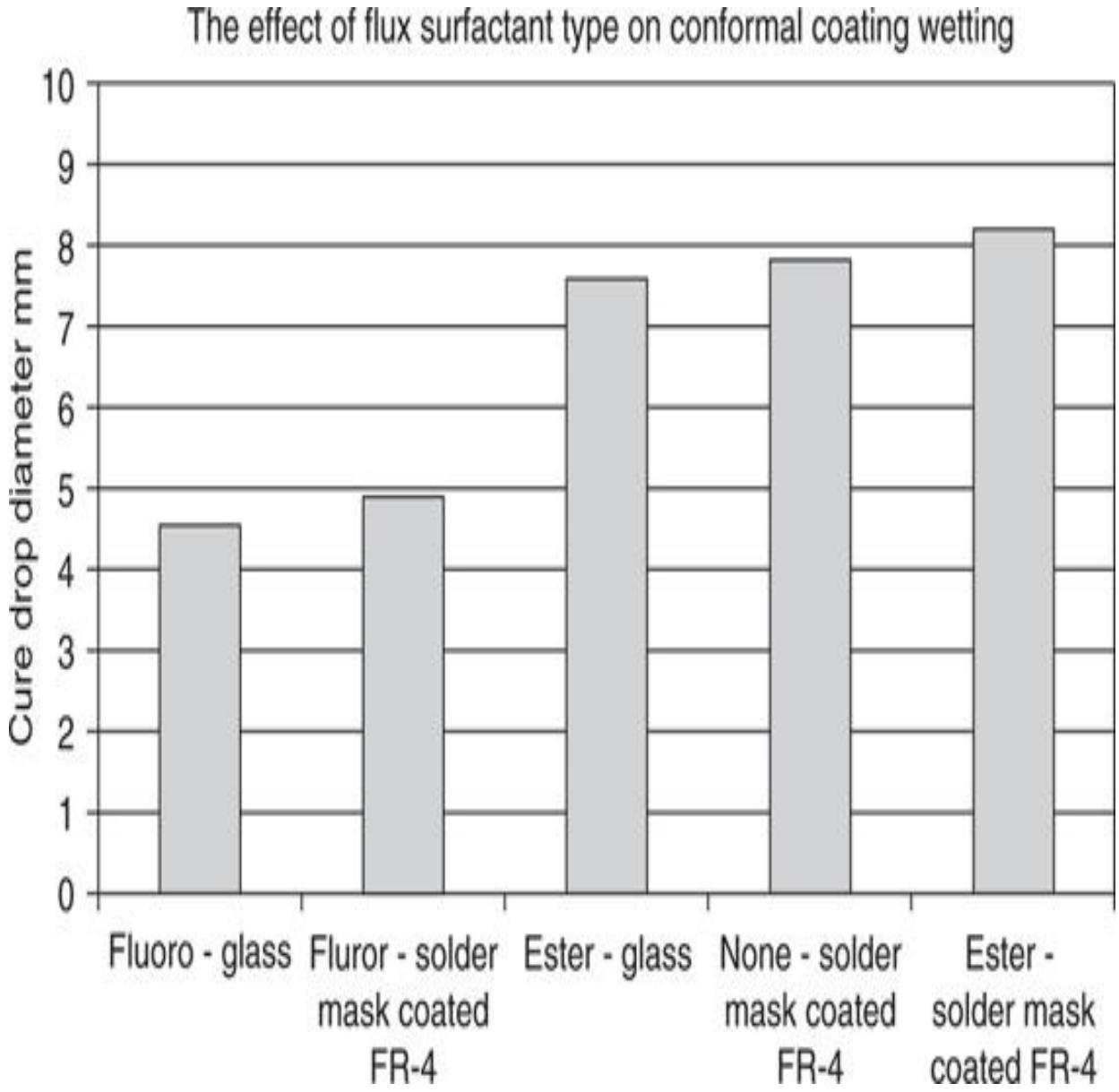


FIGURE 44.5 The effect of flux surfactant type on conformal coating wetting.

44.3.5 Water Drop Contact Angle

One quantitative test method for the determination of surface energy is to measure the contact angle of a droplet of distilled or deionized water on the substrate surface. A substrate with a high surface energy will have a large contact angle (water will bead up). A substrate with a low surface energy will have a low contact angel (water wets

out). This method is more quantitative and repeatable than the dyne pen method, but requires a greater capital investment.

ASTM-D-7334, titled “Standard Test Method for Measurement of the Surface Tension of Solid Coatings, Substrates and Pigments using Contact Angle Measurements,” outlines one method used to determine contact angle and a calculation of resulting surface energy.

ASTM-D-5725 titled “Standard Test Method for Surface Wettability and Absorbency of Sheeted Materials Using an Automated Contact Angle Tester,” shows an automated (though capital intensive) method of determining contact angle.

Figure 44.6 shows a diagram of the pertinent measurements for contact angle.

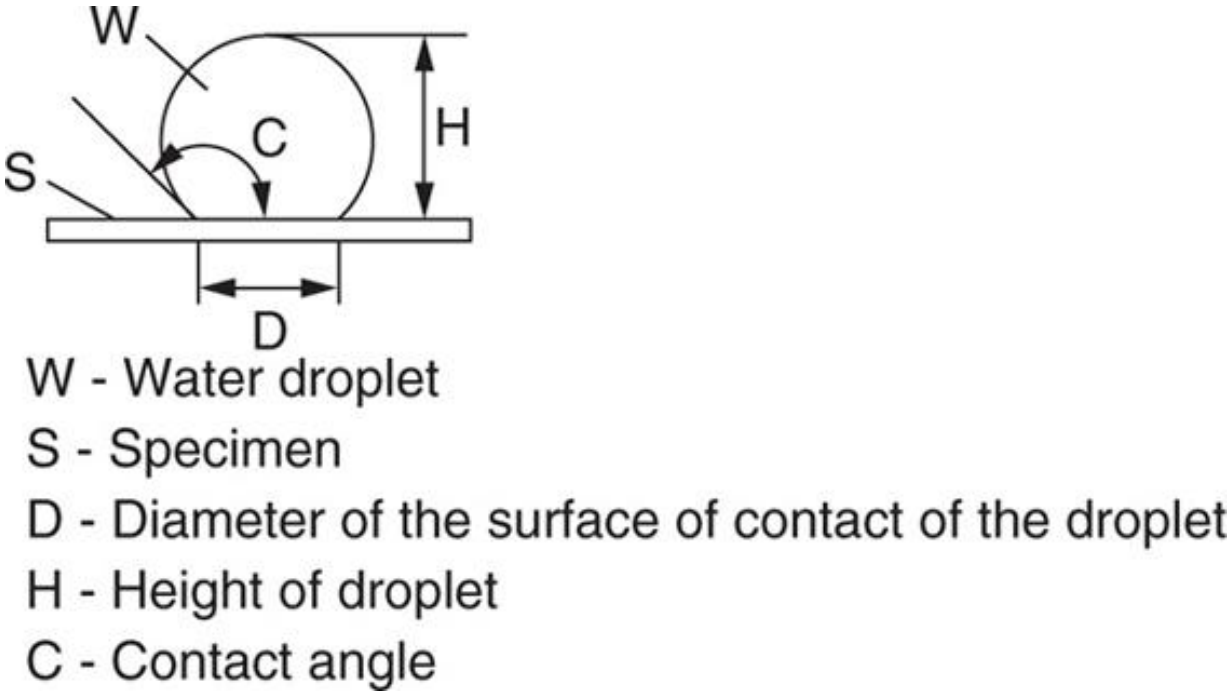


FIGURE 44.6 Measurements for contact angle.

A manual method of measurement makes use of a device called a goniometer. An example of such an instrument is shown in Fig. 44.7. A substrate is placed on the center

pedestal. A calibrated syringe is used to dispense a droplet of distilled/deionized water on the surface of the substrate. A light source behind the water droplet illuminates the water droplet. A front viewer is set level with the surface of the substrate. Reticules in the eyepiece are adjusted to measure the contact angle of the drop. A hydrophobic surface will have a high bulbous shape. A hydrophilic surface will have a flat and wide droplet shape.

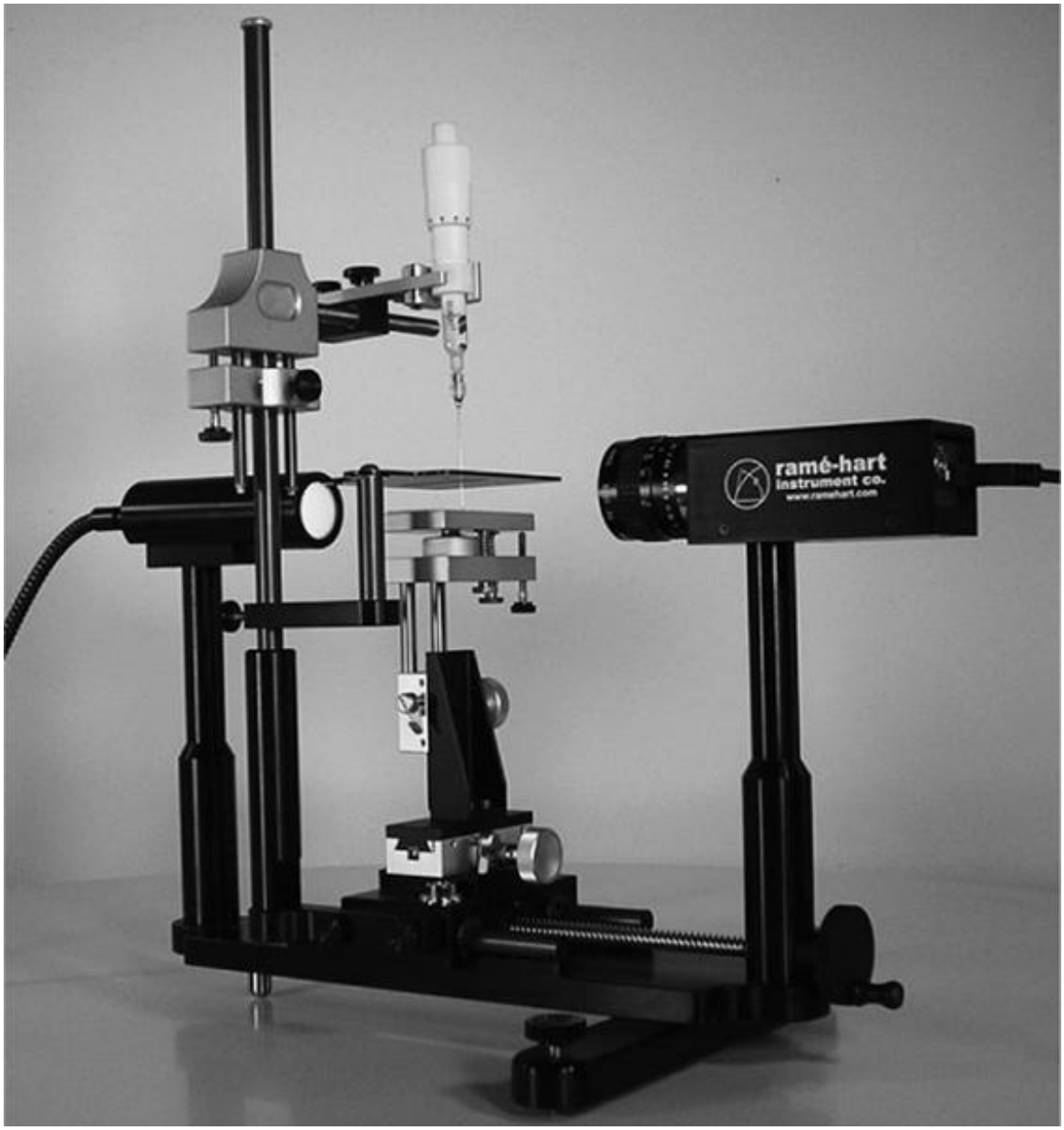


FIGURE 44.7 Goniometer (*Courtesy Rame' Hart Instrument Company*.)

44.3.6 Bake-Out

Since the coating is intended to be waterproof, it is imperative that all moisture be baked out before the coating is applied, especially for hydroscopic substrates such as GI polyimide. If moisture is left in place, it can cause corrosion of traces and/or parts and will promote dendritic growth between conductors, as well as enabling the growth of conductive anodic filaments (CAF) along the glass fibers in the weave of the PWB (see Chap. 59). A bake of 93°C for 4 h will be sufficient to drive out moisture from the CCA. With certain component designs, a lower temperature and different qualification time may be required.

44.4 APPLICATION PROCESSES

Conformal coatings can be applied by a variety of methods, including

- Hand painting the coating with a brush
- Dipping the board into the coating
- Hand spraying with an aerosol can or handheld spray gun
- Automatically spraying the board with coating as it passes by on a conveyor
- Selectively applying coating to certain areas of the board with a robotic nozzle
- Vapor depositing para-xylylene onto the board with specialized equipment

44.4.1 Hand Paint

Hand painting allows coating to be applied wherever desired with no setup time and low equipment cost. It is still the preferred method for touching up thin spots in a bulk applied coating and for coating replaced components. It can be used to reach areas where spray or automatic nozzles cannot reach, and works well for smaller, one-of-a-kind items. Hand painting is the most variable of all methods.

44.4.2 Dip

Dip coating works best for coatings that have a long pot life at room temperature, such as solvent evaporation cured coatings and one part materials. Since the unused coating remains in the dip tank, a long (or infinite) pot life keeps the waste down to a minimum. The viscosity of the material in the bath should be checked daily, using a flow cup viscosimeter or other method, and solvent added to keep the viscosity of the material within the acceptable range. For a given dip speed, a lower viscosity will produce a thinner coating. The dip machine (see Fig. 44.8) will have bars or hangars on which to hang the board to be coated. Insertion speed should be slow enough to prevent the formation of bubbles as the coating flows around and under surface mounted parts, etc. Withdrawal speed should range between 1 and 6 in/min and will dictate the finished coating thickness; a slower withdrawal will produce a thinner coating. Dip coating cannot be used multiple times to build up thicker layers of acrylic coating, since solvent in the bath will loosen or dissolve previously applied layers of acrylic. Any areas that are not to be coated must be completely masked before dipping. Assemblies can be partially dipped to leave the top edge of the board uncoated if the board is designed so that all components that need coating are below the level of the bath.

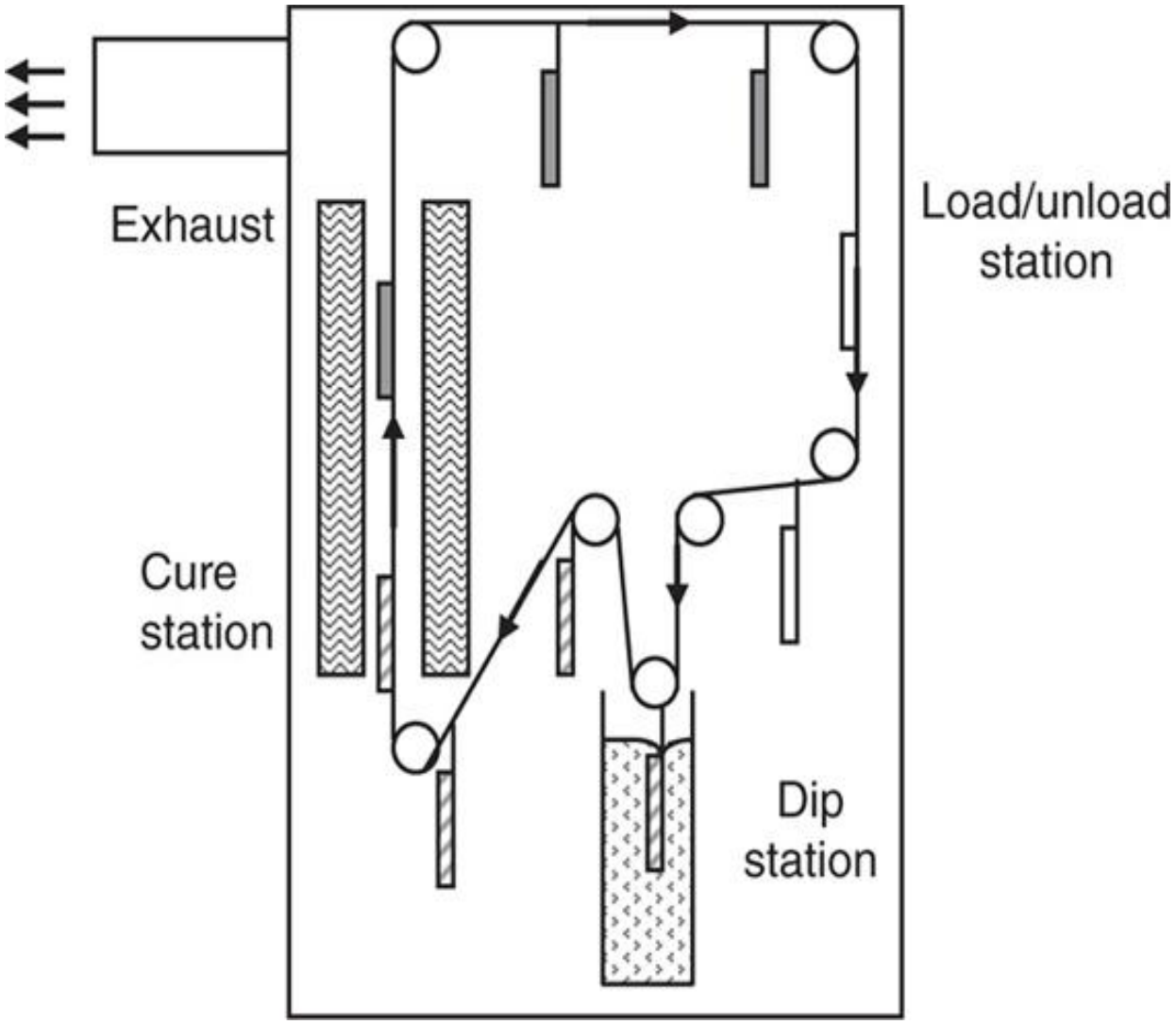


FIGURE 44.8 Dip coating machine.

44.4.3 Hand Spray

Hand spraying is used for all types of liquid coatings. The boards to be coated are sprayed several times; the angle is changed 90° each time so that complete coverage is achieved. Tall components may shadow or block the spray from lower profile components behind them, so care must be taken to ensure all areas of the board are fully coated. A witness strip is often sprayed at the same time for use in measuring the coating thickness. As with the dip method,

viscosity control is a key factor to reducing bubbles, cobwebs, and improper coating thickness. Two part materials are mixed immediately prior to filling the spray gun container, or are mixed in line if a continuously fed mixing gun is used. Solvents may also be used to modify the viscosity of the coating being applied. Single-part materials (particularly acrylics) are also available in aerosol cans, eliminating mixing altogether.

44.4.4 Automatic Spray

For high-volume coating application, a semiautomatic spray machine is used to eliminate the dependency on the operator and allow in-line coating. The boards enter the machine on a paper-covered conveyer and are sprayed by a rotating or reciprocating spray head. The motion of the spray head(s) is designed to cover a given width of the belt completely from all angles. Shadowing is of greater concern with semiautomatic spray equipment, since special treatment cannot be given to any one area of the board. Full masking is required to keep the coating out of areas that should not be coated. Once the board is coated on one side, it is partially cured (or fully cured), turned over, and coated on the other side.

44.4.5 Selective Coating

The selective coating process utilizes a robot similar to the automated pick-and-place machine to dispense coating only where it is needed. Four- or five-axis machines can be used to coat the sides of tall parts and around corners. The greatest benefit to selective coating is that it drastically reduces the amount of labor needed for masking and mask removal; areas that need to be free of coating simply have no coating applied there. Coating utilization is highest of all

methods, since almost no coating is lost in continuous production. Spray patterns may be either atomized, spraying droplets onto the board and providing a thinner coating (see Fig. 44.9), or continuous, applying a stream or sheet of liquid to the board (Fig. 44.10), producing a well-defined boundary between the coated and uncoated areas and eliminating the need for masking. In the same way as the semiautomatic sprayer, the board is tack-cured and then turned over and coated on the other side. An automated board flipper may be used to accomplish this to automate the entire coating process.

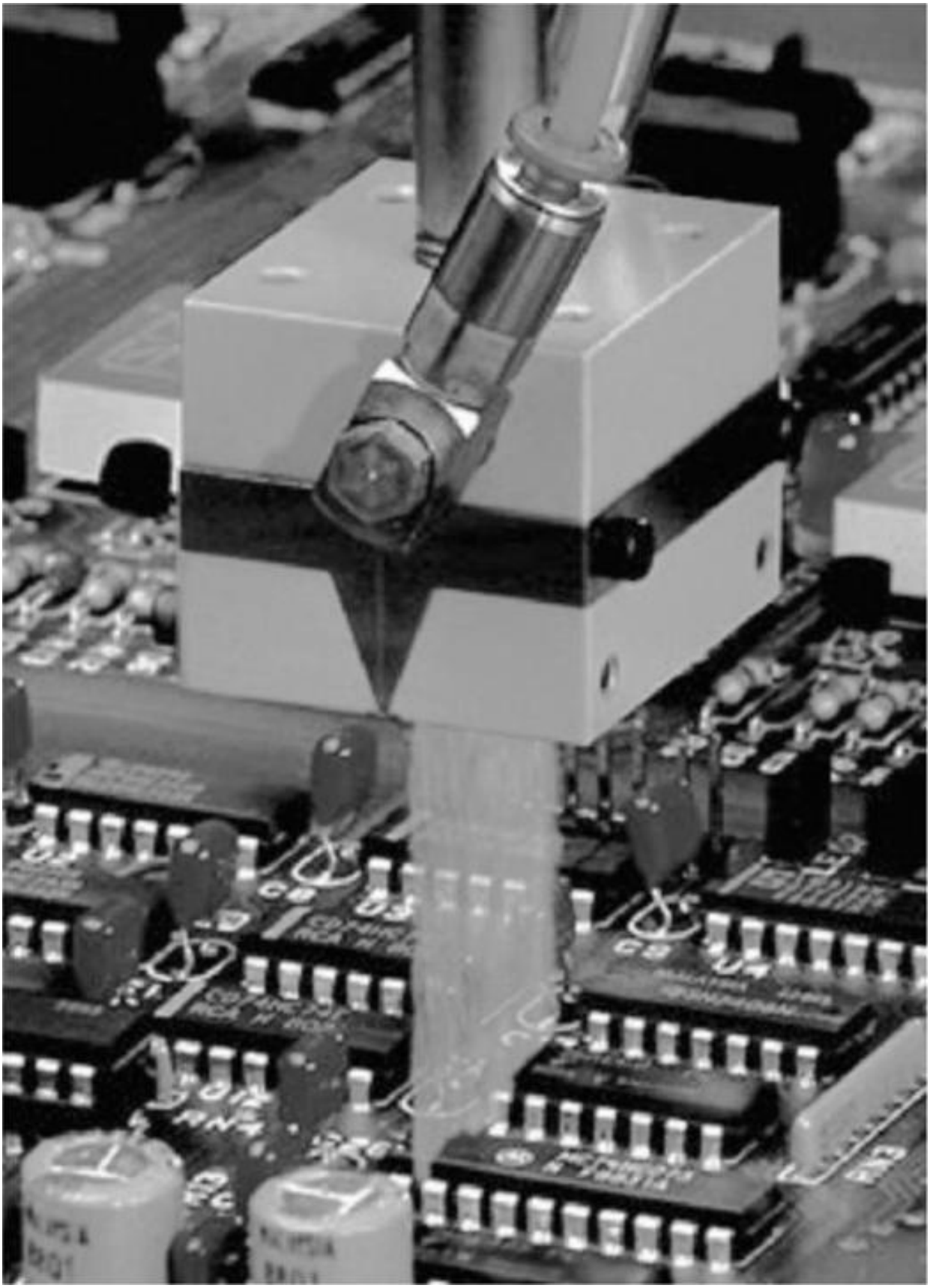


FIGURE 44.9 Selective coating using an atomizing nozzle. (*Courtesy of Asymtek*.)

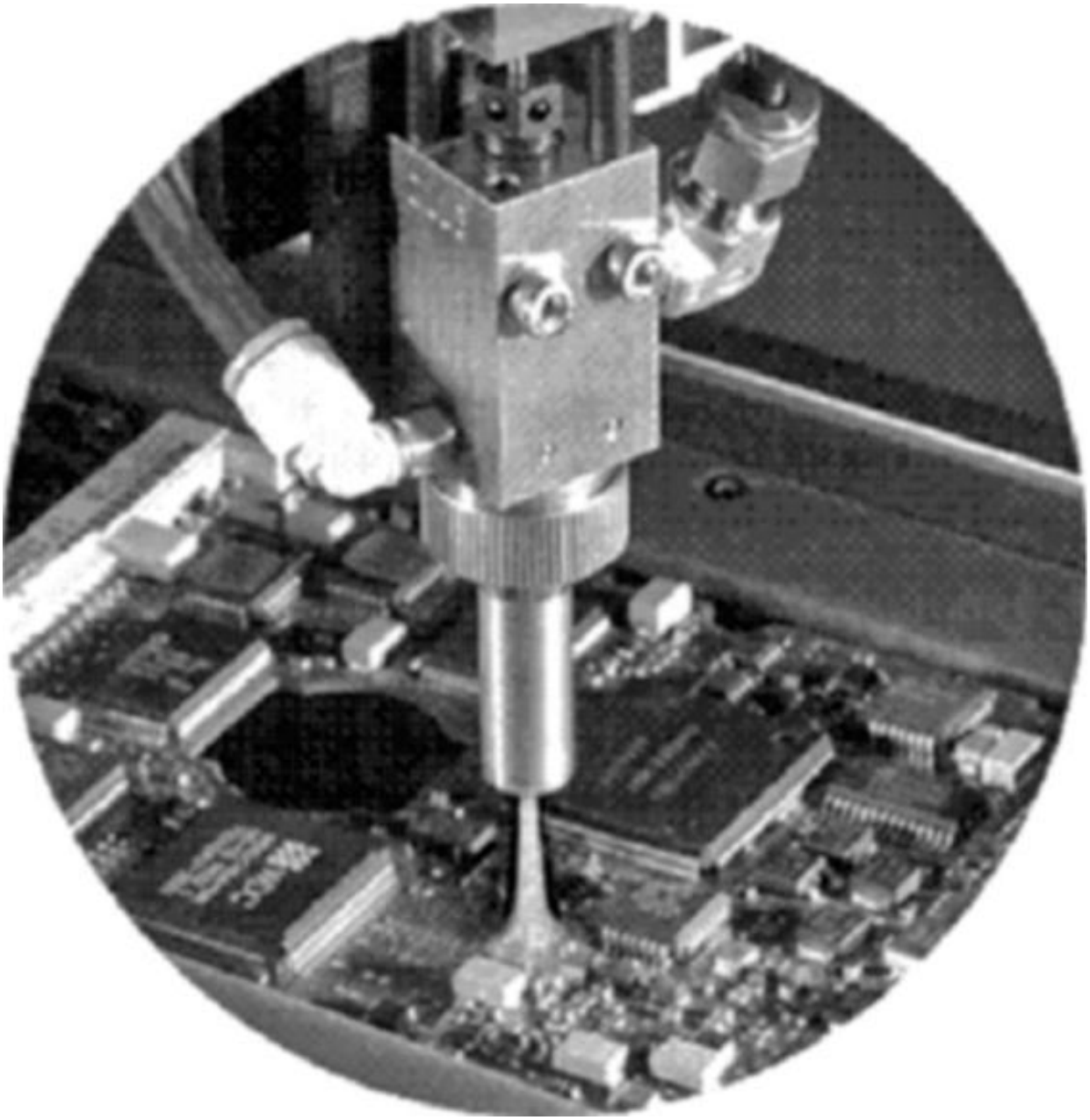


FIGURE 44.10 Selective coating using a continuous flow nozzle. (*Courtesy of Chipco, Inc*.)

44.4.6 Vapor Deposition

Vapor deposition is only used with XY coatings, and requires specialized coating equipment. In the evaporator, a measured amount of dimer is placed in a crucible. The coating cycle is then started, and the chamber is pumped down to an almost complete vacuum (see Fig. 44.11). During the deposition process, the dimer powder is vaporized and recondenses onto the batch of CCAs, forming a uniform coating covering all corners and edges evenly. The vapor deposition process drives the vapor into any crevices and openings. Vapor deposition has the most stringent masking requirements, since leaks in the maskant will still admit vapor that will contaminate the surface behind, and air pockets inside masking boots or tape may dislodge the boot in the vacuum and create leaks as the air escapes.

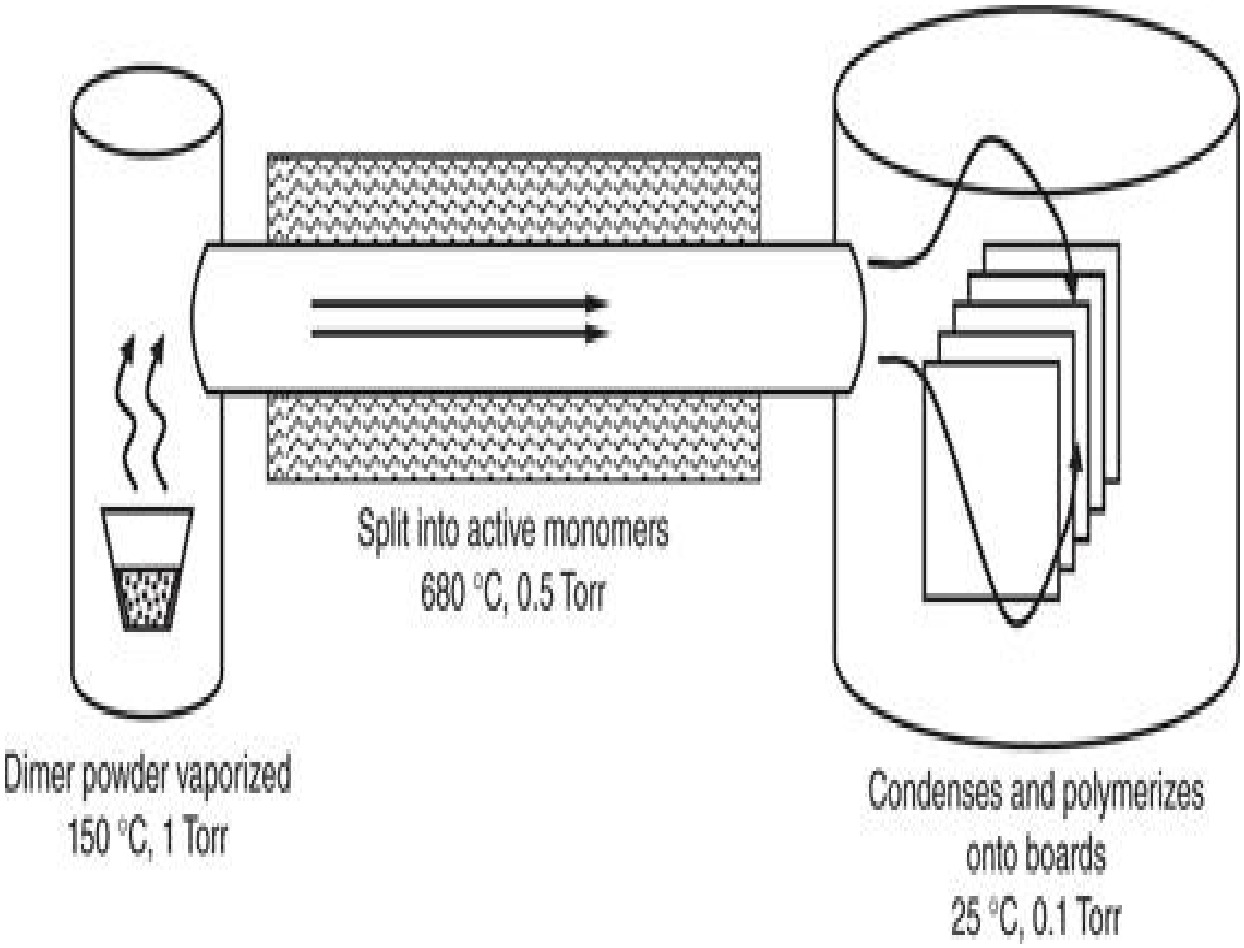


FIGURE 44.11 Para-xylylene vapor deposition process.

44.5 CURE, INSPECTION, AND DEMASKING

The finishing steps require most of the labor involved in conformal coating process. Three finishing operations are

- Curing the coating
- Inspecting under UV light to verify complete coverage and touch-up
- Removing mask materials

44.5.1 Cure

Each of the four liquid chemistries is available in a formulation offering different cure mechanisms, as shown in Table 44.1.

44.5.1.1 Solvent Evaporation. Systems that are cured by solvent evaporation can be air dried, or slightly heated to drive the solvent out faster. Care must be taken not to overheat the freshly coated assemblies; the coating will skin over and cause bubbles. Long-term exposure to the unevaporated solvents trapped in the coating may also be deleterious to the materials in the parts and PWB. Drying of solvent cure assemblies must be done under a ventilation hood or other properly ventilated area.

44.5.1.2 Room Temperature Vulcanization. Some silicone-based coatings use the room temperature vulcanization (RTV) cure process, which consumes moisture from the surrounding environment as part of the cure process. Some means of humidity control is required; if cure is attempted in a dry oven, the material will not cure properly, if at all.

44.5.1.3 Heat Cure. Oven-curable systems use an extended bake, ranging from 15 min to several hours or longer, for the material to cure fully. Thermally activated systems require the increased temperature to start the curing process, whereas thermally accelerated systems will cure eventually at room temperature but are baked to speed up the process and improve material properties. Generally, the hotter the oven, the quicker the cure, and the harder the finished material. However, care must be considered to ensure there are no thermally sensitive components that are added prior to the coating process when higher temperatures are used to expedite the cure.

44.5.1.4 UV Cure. For high-volume production, UV-curable materials are used. Immediately after the coating machine is a booth with high-intensity ultraviolet lamps to illuminate the assembly. After several seconds, the assembly has cured enough to be able to be handled at the next stage of assembly, such as coating the opposite side. UV-curable materials do not cure fully under components, where the coating is not illuminated. Therefore, most UV-curable materials also contain a secondary curing mechanism, such as heat or moisture cure, so that at the end of the line the CCA can be fully cured in a single baking or moisture step or naturally come to full cure in ambient conditions inside the finished product. Since different coatings are sensitive to different wavelengths of UV light, it is important to coordinate the purchase of the light source with the supplier of the coating.

44.5.1.5 Catalyzed. The catalyzed process involves mixing two parts together just before application, to initiate polymerization and cross-linking. This process occurs slowly at room temperature but may be accelerated by elevating the temperature in an oven. Catalyzed coatings may be affected by contaminates present in the PWB or parts being

coated, resulting in uncured areas or peeling coatings. Since the pot life of catalyzed materials tends to be short, it is imperative that the mixed material be cleaned from sprayers, tubing, and so on, before it thickens and hardens.

44.5.2 UV Inspection

Coatings contain a fluorescent dye that will glow under UV light and show where the coating has (or has not) been applied. Areas without coating can be touched up at this time. The areas most susceptible to insufficient coating are corners of parts, where the coating can flow away and leave little behind; the protruding ends of through-hole part leads; and shadowed areas under or behind larger components. If large flat areas are uncoated and show beads of coating, there is a wetting problem due to improper surface preparation or a material incompatibility. The coating should also be inspected for improper thickness, bubbles, trapped material or debris, and incomplete curing (see Fig. 44.12).

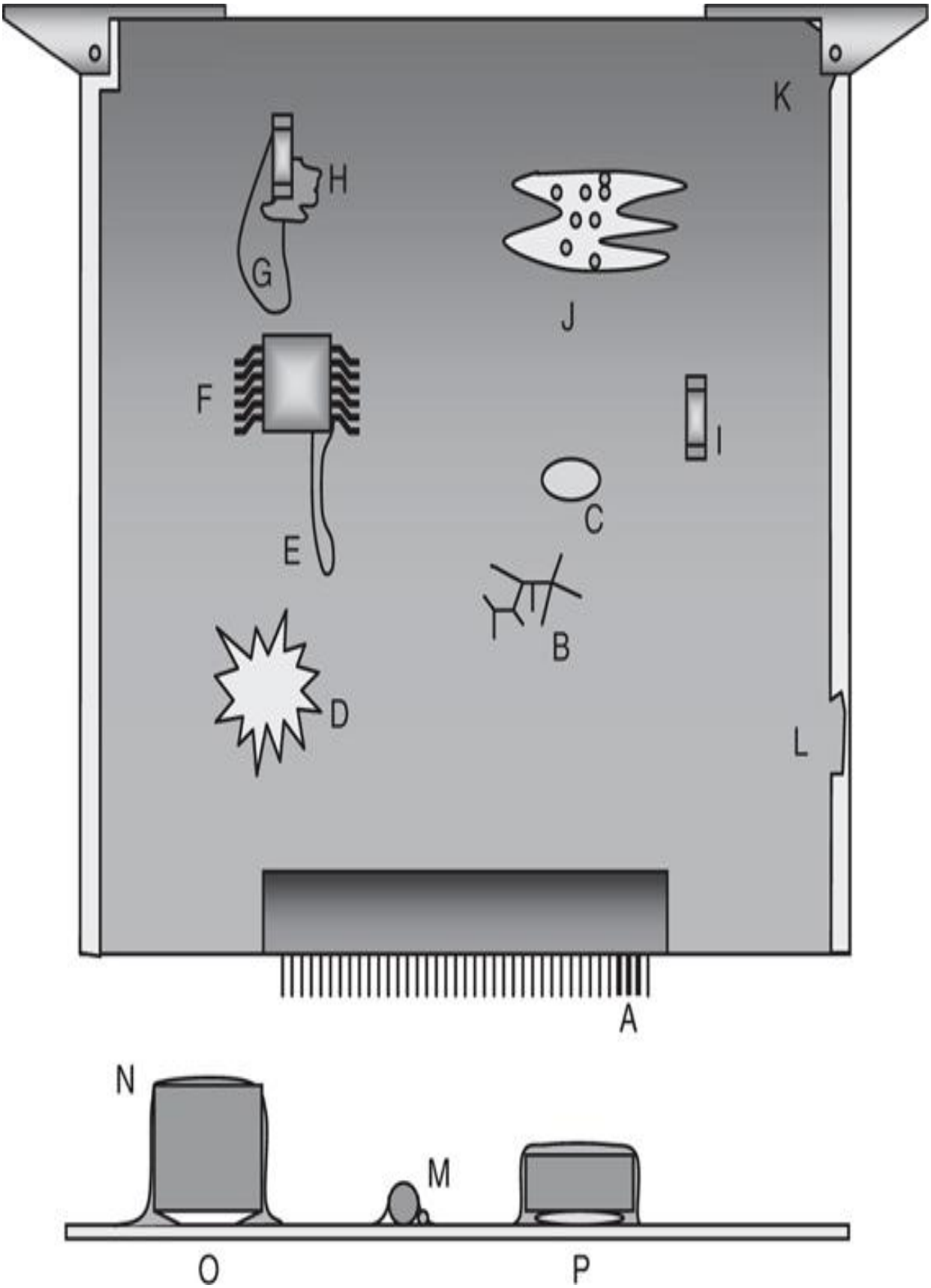

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FIGURE 44.12 Various conformal coating defects.

Recently, with the migration of conformal coating into new market segments, new suppliers have developed camera-based AOI systems that can measure the presence of the coating, detect defects such as insufficient coverage and voids and calculate the coating thickness of flat, unencumbered cured surface. Completely transparent coatings yield a low optical signature, the signal the AOI system detects under ambient lighting. The resolution of the AOI is frequently not high enough to see the clear film.

Fluorescent coatings provide an enhanced optical signature when illuminated, making AOI inspection easier. AOI systems utilize filters to eliminate background light not emanating from the fluorescent coating. This can be a fast solution for in-line verification of coverage.

44.5.3 Demasking

Mask materials should be removed carefully; to prevent peeling, it may be desirable to score or cut the coating at the edge of the mask so that the coating tears along the correct line. Ensure that the mask is removed entirely and that no residue has been left behind on the board. Latex mask that has been overheated will be sticky and difficult to remove completely, as will overheated masking tapes.

44.6 REPAIR METHODS

Since the different varieties of available coatings vary widely in their properties, removal methods must be evaluated and developed on practice boards first before being used on deliverable CCAs. The coating can then be removed as easily

as possible, with the least risk to the CCA. Several methods to remove conformal coating are

- Using a solvent to loosen or dissolve the coating
- Using a hot soldering iron or hot-air nozzle to solder through the coating while simultaneously removing the offending electrical part
- Mechanically cutting, abrading, or picking away the coating
- Etching the coating away using rarefied gas plasma (typically for XY coating only)

44.6.1 Solvent

The easiest coatings to remove are acrylics, since they do not react when they are applied. For local coating removal, the area to be repaired can be cotton swabbed several times with the proper solvent. Care must be taken to keep the solvent only in areas that are to have the coating removed. The entire board may be stripped of coating with a solvent soak. This is most useful on acrylic coatings, but is also possible for some urethanes and silicones, which swell and loosen when soaked. Note that this process may damage the components or solder joints on the board, which will be stressed as the expanding coating pushes up the components. The solvent may attack the components and PWB itself; epoxy coatings cannot be removed with solvent or chemical strippers, since many parts and the PWB are also made of epoxy.

44.6.2 Thermal

Thin coatings may be loosened from solder joints with a soldering iron or a hot-air reflow tool, while the faulty part is being desoldered. The area is then cleaned of charred and or

damaged coating, and the repair completed. Although this method is simple, it usually produces toxic gases, and must be performed with adequate ventilation. The decomposed coating is also difficult to clean off of the board and soldering iron.

44.6.3 Mechanical

Mechanical means such as scraping and picking are necessary to remove all coatings, even if the bulk has been removed via one of the preceding methods. Softer coatings such as UR or SR can be scraped away with a wood implement, so as not to cause damage. A soft rotary tool may be used for larger areas. The board may be heated slightly to make the job easier. For harder coatings, a hot knife is used to cut through the material.

44.6.4 Abrasion (Microabrasion)

The principle of micro abrasive blasting is based on projecting a small particle onto the coating surface with enough force to mechanically abrade the surface and eventually remove the coating. Balance must be achieved between the abrasion of the coating surface and abrasion of the printed wiring board surface beneath the coating.

This coating removal method uses a micro abrasive blasting system and a very fine soft abrasive powder. The powder is propelled through a small nozzle toward the area where the coating needs to be removed. The nozzle is positioned around the base of component leads to selectively remove the coating. This technique requires practice in order to not damage the substrate beneath the coating along with contamination by the abrasion media to the surrounding board areas.

Micro abrasive blasting will generate substantial static charges. Proper ESD measures need to be used in order to ensure that static charges are handled appropriately.

44.6.5 Plasma Etch

An extended plasma etch will remove XY coatings from large areas, since the plasma erodes the surface evenly. Since the plasma will chemically change the surface (leaving behind oxides, reduction products, and ash), compatibility of the plasma-stripped surface with the new coating must be verified.

44.7 DESIGN FOR CONFORMAL COATING

When designing a conformal coating system into the product, the designer needs to consider a number of questions:

- Is coating required for this product, or should it be omitted for cost savings or other reasons?
- What material properties are most important for this application, and which materials will provide the best balance?
- What areas should not be coated?

44.7.1 Is Conformal Coating Required?

One of the basic questions to consider is whether or not to coat the particular assembly. Generally this will be a trade-off

between reliability and cost.

44.7.1.1 Why Use It? Customers may flow down requirements for conformal coating for industries where it is commonly used such as military or aerospace electronics. The following are some of the reasons to consider the use of conformal coating:

- The end products are used in humid or condensing atmospheres, such as electronics boxes for military and shipboard applications. It should be noted that although conformal coatings are moisture resistant, they are not waterproof, and should not be used for items that will see extended or continuously wet conditions. For those applications, use a watertight enclosure and conformal coat the boards inside. Conformal coating will protect against condensation, such as when the product is brought from a cold environment into a warm humid one.
- Clean conformal coating does not support mold and fungus growth.
- The end products can become contaminated by dirt and debris. Conformal coating is especially useful in space applications, since loose debris will float readily from place to place inside the electronics box.
- Conformal coating greatly improves the board’s capability to withstand high voltage, especially at altitude or low pressure, since an electrical arc now has to travel through two layers of insulation rather than just jumping from one trace to its neighbor.
- Conformal coating protects against tin whiskers. Pure tin plating has the tendency to recrystallize and extrude long (>1 mm) whiskers of pure tin, which can short to neighboring part leads and cause short circuits. Conformal coating provides protection against short circuits caused by tin whiskers. Even if a tin whisker can force its way through a layer of coating on the way out, it cannot force

its way back through the coating on the neighboring lead without bending and buckling

- Conformal coating provides mechanical support for components during shock and vibration. Components weighing more than ¼ oz per lead should be supported by other means as well, such as staking with a bead of adhesive along the side.
- Lastly, conformal coating may be made opaque, and thus provide a level of security. A thick opaque epoxy coating will prevent the casual observer from determining what is under the coating.

44.7.1.2 Why Not Use Coating? Most of the reasons for not coating on an assembly stem from the recurring cost of cleaning, masking, demasking, touch-up, etc. The target cost of the product may not support the extra cost incurred by the coating, and if reduced reliability of the uncoated assembly is still acceptable, the rational decision is not to coat the assembly. Since the coating is a dielectric material, it changes the impedance of high-speed traces on the surface of the PWB. Boards with microstrip are usually not coated for this reason. Radio frequency (RF) PWBs for severe environments can still be coated if the traces are buried microstrip or stripline, which are unaffected by the additional coating on the board surface.

44.7.2 Desirable Material Properties

When selecting a coating, the entire suite of material properties must be considered in order to choose the best coating for the application. Unfortunately there is no “one size fits all” solution, but many different coatings, each suited to different applications, as shown in Table 44.1.

The following are some of the properties to consider:

- *Ease of application and producibility:* The intended production environment may determine the cure process and application process that is best for the job, and will narrow the field of alternatives.
- *Compatibility:* The coating must not be inhibited from curing by any material on the completed assembly. Often the best way to address this is to ask the manufacturer and try out the coating in question on a sample of the materials that you are going to use.
- *Moisture resistance: S*ometimes called moisture and insulation resistance (M&IR), is a measure of how well the insulation characteristics are maintained when exposed to elevated conditions of temperature and humidity. A material with a low M&IR value would be a poor choice to protect a circuit in a high humidity end-use environment.
- *Dielectric constant:* For RF and high-speed circuits, a material with a low dielectric constant will change circuit performance less than a material with a higher one.
- *Dielectric strength:* For high-voltage application, materials with a high dielectric strength should be used. For a valid comparison, tests must be performed on samples of equivalent thickness, since thin samples will break down at a higher volt/mil than thick samples of the same material.
- *Insulation resistance:* Also known as resistivity, insulation resistance is of concern in high-voltage or high-impedance circuits, where the resistance in the circuit is very high (>10 MΩ) and is significant compared to the resistance of the coating and PWB laminate. For these applications, choose a coating with high (>10^15 Ω-cm) resistivity and excellent moisture resistance.
- *Hardness:* For products that need to withstand cold temperatures <−10°C, a soft coating is recommended so that at cold temperatures the coating will not exert excessive force on fragile or beneath components (see Fig. 44.13). For products that need good abrasion resistance

and protection from external handling damage, a harder coating must be used.

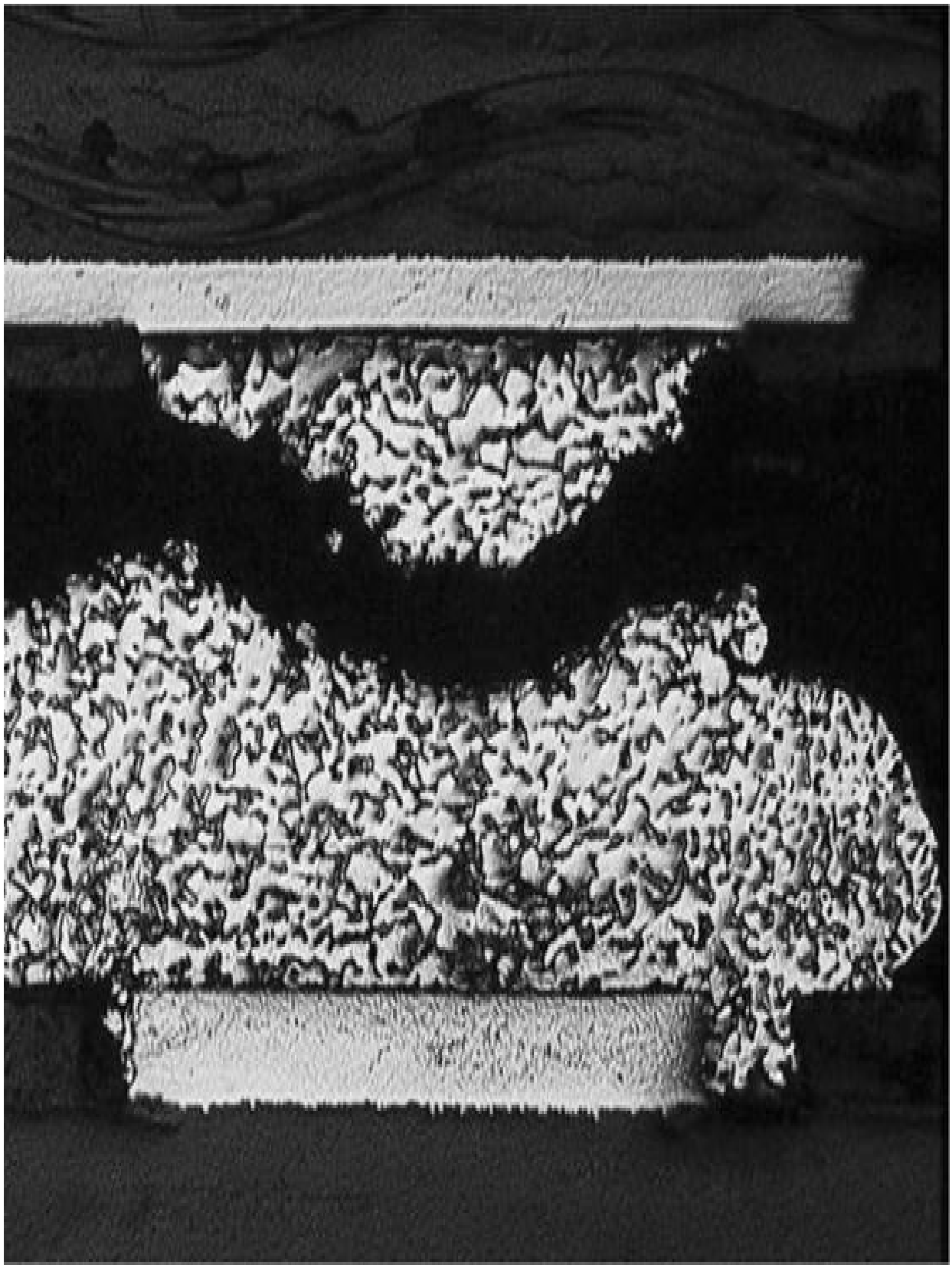

FIGURE 44.13 BGA ball cracked by high-modulus coating.

- *Glass transition temperature (T_g):* For assemblies that need to withstand cold environments, select a coating that either has a T_g below the coldest temperature required or a T_g of 25°C and above. Coatings that have a low T_g in the range of operation will suddenly get hard at cold temperatures and impose great stress on the surrounding components.
- *Elongation:* Materials with high elongation are resistant to cracking and abrasion.
- *Reworkability:* AR coatings are the easiest to rework, whereas XY and ER are the hardest.
- *Abrasion resistance:* This is ability of the coating to withstand damage from handling and later assembly operations, as well as in the field.
- *Flammability:* For assemblies that need to withstand prolonged exposure to sources of heat, select a coating that has the correct flammability standards that are published by Underwriters Laboratories may be a requirement. Coatings that do not have this certification, if used within this condition could fail and in danger the public.

44.7.3 Areas to Mask

During the design, the designer needs to consider all the areas and parts on the board that need to be uncoated and identify them on the assembly drawing, shop instructions, or other paperwork that the coating technician will use. Although it is obvious to the design engineer that an expensive infrared (IR) sensor element should not be coated, it may not be so obvious to the technician holding a drawing that says, “Coat entire board,” and nothing else. Being specific on the drawing clarifies what should be coated and how.

Consider the following areas:

- Coating on connector pins can cause open circuits, and may interfere with the full mating of the connector. It is necessary to mask the back of the open back connectors as well as the front, to keep the coating from flowing along the back of the pin into the active area. Also, pin alignment depends on a certain amount of looseness on the pins, and filling the connector shell with coating will defeat this feature.
- Coating should be kept from the edges of plug-in CCAs where the card guides travel. The coating will interfere with proper operation of the card guide and may prevent proper grounding of the card.
- Mounting holes for screws should be masked to keep the coating from filling or reducing the size of the hole and to ensure that the PWB is properly grounded.
- Test points should be masked so that they can be reliably accessed during testing.
- The adjustment screws of adjustable components. If the adjustable components have openings in them, the openings should be masked also.
- If the product contains sensors for air temperature, pressure, humidity, etc., the coating should not block the air from entering the sensor.
- Optical devices, light-emitting diodes (LEDs), infrared sensors, and light sensors may have their operation affected by the coating. This is especially true for UV and IR devices since the coating may be opaque to UV and IR wavelengths of light. The coating may also darken, cloud, or turn brown as it ages, eventually affecting the operation of the circuit. Connectors for fiber-optic cable should also remain clear of coating for the same reason.
- Components mounted in sockets should have the sockets masked and the components inserted after coating.

- Areas under BGA packages should not be underfilled with conformal coating but with an underfill adhesive particularly suited for that purpose. If no underfill is used, the edges of the BGA should be masked, or dammed with a permanent adhesive barrier to prevent the coating from entering under the BGA. Due to the shrinkage of conformal coating, during thermal cycling the balls will be crushed and the reliability of the BGA will be adversely affected.

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CHAPTER 45
FLUXES AND CLEANING

Gregory C. Munie

IPC—Association Connecting Electronics Industries, Bannockburn, Illinois

Laura J. Turbini

International Reliability Consultant, Waltham, Massachusetts

45.1 INTRODUCTION

Cell-phones, iPods, digitial cameras, laptops and desktop computers, DVDs, and indeed all electronic equipment in our world have one thing in common: They each contain an electronic assembly composed of integrated circuits and discrete components soldered to a printed wiring board (PWB) to create an electrically functional circuit.

In years gone by, printed circuit assemblies were made exclusively with through-hole components. Today's assemblies contain components that are both through-hole and surface-mount, and some contain unpackaged integrated circuits (ICs) attached directly to the PWB. Except

in the case of direct chip attachment by wirebonding or conductive adhesive, the use of a soldering flux to ensure good joining is almost universally practiced. Thus, soldering flux choice has become an important consideration in the manufacturing of electronic assemblies. As electronic product designs have moved to more densely packed PWBs with fine lines and spacing, double-sided surface-mount technology, fine-pitch components, ball grid arrays (BGAs), chip-scale packages (CSPs), stacked packages, etc., the role of the soldering flux has become a critical link in the chain of events required for a successful manufacturing process.

In the past, the soldering process was usually followed by a cleaning step to remove flux residues and to ensure the reliability of the assembly. This practice was challenged in the early 1990s by the elimination of a major class of cleaning materials, which had been used for flux residue removal. The targeted cleaning agents include chlorofluorocarbons (CFCs) and methyl chloroform (1,1,1—trichloroethane) that have been shown to destroy stratospheric ozone.[1] These were replaced by aqueous detergent cleaners and saponifying agents, and in some cases cleaning was eliminated by the use of low solids or no-clean fluxes.

Up to the mid-1970s, the predominant flux chemistry was rosin-based. Today, although rosin fluxes are still in use, great advances have been made in flux chemistries and a large variety of formulations with very different chemistries are being used.

The implementation by the European Parliament of Directive 2002/95/EC on the restriction of the use of certain hazardous substances (Restriction of Hazardous Substances [RoHS]) in electrical and electronic equipment, including lead in solder, has had significant impact upon the manufacturing process. Traditional tin-lead solder melts at 183°C, whereas the most common lead-free alternatives have a much higher melting temperature, including tin-copper (227°C), tin-silver

(221°C), and tin-silver-copper (217°C). This affects the substrate materials, the flux formulations, the cleaning materials and processes, among other things.

This chapter will review the assembly, soldering, and cleaning processes, briefly touch on choice of surface finishes for both printed boards and components, discuss the soldering flux in terms of its role in soldering, review the variety of flux chemistries available along with their advantages and disadvantages, and comment on the challenges for flux formulation and cleaning due to lead-free soldering temperatures.

45.2 ASSEMBLY PROCESS

The basic elements of an electronic assembly are the PWB, the components and the interconnecting metallization. The majority of PWBs are made of epoxy-glass substrate with copper or solder-coated copper metallization. In many cases, a solder mask covers most of the circuit traces, leaving exposed only those patterns where soldering will occur during assembly. Boards designed for through-hole components usually contain copper-plated through holes that may be solder-coated; those designed for surface-mount components will have metallized pads for interconnecting the surface-mount parts to form the assembly.

45.2.1 Assembly Process Issues

The assembly process for electronics includes wave soldering, reflow soldering, and vapor phase soldering as well as selective soldering. Components range from through-hole and surface-mount—BGA, μ-BGA, CSP, and stacked packages—to chip-on-board (COB). The high density and reduced size of today's electronics has led to system-in-a-

package (SIP), where the integrated circuit (IC) package contains several active devices, and system-on-a-chip (SOC), where all the functions of an electronic system are integrated on a single chip. These package types increase the complexity of the electronic assembly process, requiring adhesive attachment for bottom-side discretes, underfill for CSP, wirebonding and encapsulation for COB, and solder paste, paste flux, and liquid flux for various applications.

When manufacturing complex printed wiring assemblies (PWAs), the thermal process chosen must take into account the thermal mass of the assembly, the component density, the solder flux and solder paste characteristics, and the maximum temperature limitation of the components. Most of the components assembled to the board in the soldering process have a maximum temperature of 240°C for traditional Sn/Pb soldering. Some electronic components, such as electrolytic capacitors and plastic-encapsulated components, are not rated to experience the high temperatures required to process with lead-free solders. The resulting heat-induced degradation can result in early field failures. Also, the higher temperatures required for lead-free solders are not compatible with many optoelectronic components. The increased heat can cause a variety of conditions with these components, among them electrical variances, changes in silver-epoxy die attach properties, delamination between plastic and lead-frame parts, deformation of plastic encapsulants and plastic lenses, damage to lens coatings, and changes in the light transmission properties.

45.2.2 Assembly Temperature Profiles

IPC/JEDEC[2] has developed a recommended reflow profile for nonhermetic packaged semiconductor components. These

recommendations are based on the temperature taken at the top side of the packaged device, and also based on package volume, excluding external leads, or solder balls in the case of BGAs, and nonintegrated heat sinks. Table 45.1 lists the recommended range for Sn/Pb and Pb-free assemblies.

TABLE 45.1 Reflow Profiles Recommended for Sn/Pb and Pb-free Assemblies Based on Temperatures Taken on the Package Body

Profile Feature	Sn/Pb Assemblies	Pb-Free Assemblies
Average ramp-up rate	3°C/sec. max.	3°C/sec. max.
Preheat		
Temperature min.	100°C	150°C
Temperature max.	150°C	200°C
Time	60–120 sec.	60–180 sec.
Time maintained above melting Temperature	60–150 sec.	60–150 sec.
Time within 5°C of peak temperature (T_p)	10–30 sec.	20–40 sec.
Ramp-down rate	6°C/sec. max.	6°C/sec. max.
Time 25°C to T_p	6 min. max.	8 min. max.

The maximum recommended temperature for the package depends on the package thickness and volume. Table 45.2 lists the recommended reflow temperatures for Sn/Pb processing, whereas Table 45.3 lists the recommendations for Pb-free processing.

TABLE 45.2 Recommended Maximum Package Reflow Temperatures for Sn/Pb Process

Package Thickness	Volume <350 mm^3	Volume ≥ 350 mm^3
<2.5 mm	240 +0/−5°C	225 +0/−5°C
≥2.5 mm	225 +0/−5°C	225 +0/−5°C

TABLE 45.3 Recommended Maximum Package Reflow Temperatures for Pb-Free Process

Package Thickness	Volume <350 mm^3	Volume 350–2,000 mm^3	Volume >2,000 mm^3
<1.6 mm	260 +0°C	260 +0°C	260 +0°C
1.6–2.5 mm	260 +0°C	250 +0°C	245 +0°C
≥2.5 mm	250 +0°C	245 +0°C	245 +0°C

45.3 SURFACE FINISHES

Surface finish is defined as the outerlayer metallization on a component or substrate being soldered. Both the type and quality of the surface finish have a major impact on surface solderability and on process soldering ability. Here, *solderability* is defined as the ability of the surface to be wetted by a solder, and the forming of an intermetallic layer between the solder and the base metal. *Soldering ability* is defined as control of the soldering process parameters, such as a heating profile that produces that wetting action. The preference is always to have a surface that exhibits good solderability—that is, ease of wetting and formation of high-quality solder interconnections—for all soldering processes and materials to which it might be exposed. Soldering ability is best described as the quality of a solder process such that

the operating window is wide, that is, the process is not overly sensitive to minor shifts in process parameters such as time and temperature. Thus a process with good soldering ability would be easy to control and would produce high-quality interconnections given that the incoming materials have good solderability.

45.3.1 Substrate Finishes

The substrate surfaces of choice are usually one of the following: electroless nickel/immersion gold (ENIG), immersion silver (ImAg), and organic solderability preservative (OSP). Two other finishes, hot air solder leveling (HASL) and immersion tin, are also in use, but HASL has declined in volume and immersion tin has not reached significant volumes due to concerns over reliability.

- *ENIG* This finish is widely used because it provides a very flat surface for surface-mount component placement. It has good solderability and a long storage life but is somewhat expensive compared to other finishes. Careful control of the gold plating process during board fabrication is required to prevent a defect known as black-pad. Black-pad is caused by galvanic corrosion of the nickel layer, creating corrosion products that affect the ability of the surface to be wet with solder. If severe enough, black-pad will impact reliability of the final solder joint.
- *ImAg* Immersion silver provides a flat surface with good solderability and storage life. It is also less expensive than ENIG. However, the ImAg finish is prone to tarnish under certain atmospheric conditions; in the presence of sulfur, it forms sulfides that darken the surface and reduce solderability.
- *OSP* Organic solder preservatives are inexpensive and also provide a flat surface for surface-mount technology

(SMT) placement. Storage life for OSP is less than for the metallized finishes, and multiple thermal cycles cause it to degrade.

- *HASL* One of the oldest surface finishes, HASL is based on exposing the PWB to molten solder and then removing excess solder using hot-air knives. In the lead-free world, the processing temperature is higher than for tin-lead. HASL is inexpensive, has good solderability if the solder is sufficiently thick, but has the disadvantage of not being a flat surface.
- *ImSn* This finish is similar to immersion silver in most characteristics. However, because tin tends to form metallic whiskers that can cause electrical shorts, it is not widely used.

45.3.2 Component Surface Finishes

Component surface finishes, like those of substrate finishes, are intended to provide good solderability. In the past, the majority of component leads had a tin-lead solder finish. This finish was either plated on the base metal of the component or was applied by dipping the leads in liquid metal. Given the push for lead-free assembly, most of these finishes containing lead are being replaced by alternatives. The main contenders in replacement of lead containing finishes are based on noble metals (e.g., palladium or gold) or some form of tin plating. Palladium finishes have been in use for many years and are a known commodity. However, as noted previously, the tendency of tin to form metallic whiskers as a result of stresses in the plated layer is a matter of serious concern for the electronics industry.

45.4 SOLDERING FLUX

Soldering[3] is defined as the process of joining metallic surfaces with solder without melting the basis metal. For this joining to take place, the metal surfaces must be clean of contamination and oxidation. This cleaning action is performed by the flux,[2] a chemically active compound that, when heated, removes minor surface oxidation, minimizes oxidation of the basis metal, and promotes the formation of an intermetallic layer between solder and basis metal. The soldering flux has several functions to perform. It must:

- React with or remove oxide and other contamination on the surface to be soldered
- Dissolve the metal salts formed during the reaction with the metal oxides
- Protect the surface from reoxidation before soldering occurs
- Provide a thermal blanket to spread the heat evenly during soldering
- Reduce the interfacial surface tension between the solder and the substrate in order to enhance wetting

To perform these functions, soldering flux formulations contain the following types of ingredients: vehicle, solvent, activators, and other additives.

45.4.1 Vehicle

The vehicle is a solid or nonvolatile liquid that coats the surface to be soldered, dissolves the metal salts formed in the reaction of the activators with the surface metal oxides, and, ideally, provides a heat transfer medium between the solder and the components or PWB substrate. Rosin, resins, glycols, polyglycols, polyglycol surfactants, polyethers, and glycerine are among the major chemicals used. Rosin or resins are selected when more benign chemicals are required

since their residues are less apt to cause reliability failures. Glycols, polyglycols, polyglycol surfactants, polyethers, and glycerine are used in water-soluble flux formulations because they provide excellent wetting of the board surface and dissolve the more active materials used in these formulation.

45.4.2 Solvent

The solvent serves to dissolve the vehicle, activators, and other additives. It evaporates during the preheat and soldering process. The solvent chosen depends upon its ability to dissolve the flux constituents for a given formulation. Alcohols, glycols, glycol esters, glycol ethers, and water are common solvents used.

45.4.3 Activators

Activators are present in the flux formulation to enhance the removal of metal oxide from the surfaces to be soldered. They may be reactive at room temperature, but their activity is enhanced as the temperature is raised during the preheat step of the soldering process. Among the common activators found in flux formulations for traditional soldering fluxes are amine hydrochlorides; dicarboxylic acids, such as adipic or succinic; and organic acids such as citric, malic, or abietic. Higher molecular weight activators are needed for lead-free soldering. Activators containing halide and amine give excellent soldering yields but may cause reliability problems if not properly removed in a well-controlled cleaning step. The halides may be present in either ionic or non-ionic form depending on the level of activation desired. Ionic activators provide, in general, a higher level of activation for a given halide content.

45.4.4 Other Additives

Soldering fluxes often contain small amounts of other ingredients that serve a specialized function. For example, a surfactant may be added to enhance the wetting properties. This constituent can also assist in the foaming characteristics required for foam flux application. Other additives may be included to lower the interfacial surface tension between the molten solder and the PWB as it exits the solder wave, decreasing the chance for solder bridges to form. Solder paste formulations require the presence of additives to provide good viscosity or flow characteristics, low slump during the preheat step, and good tack characteristics for holding the component in place until reflow occurs. Finally, cored-wire flux used for hand-soldering contains a plasticizer to harden the flux ingredients that are present in the core of the wire.

45.4.5 Flux and Temperature Issues

The flux becomes active as it is heated. In traditional flux chemistry for Sn/Pb solder, the assembly is preheated to around 100 to 125°C to remove the solvent and begin to activate the chemicals used to remove the metal oxide. After this plateau, the temperature is increased above the melting point of the solder (183°C) to 240°C for sufficient time to reflow the solder paste, and then the assembly is cooled, solidifying the solder and creating a metallurgical bond between the board metallization and the components. For lead-free soldering, the preheat plateau temperature is higher—150 to 200°C—and the peak temperature is 245 to 260°C. This requires solvents that evaporate at a higher temperature and activators that become chemically active at a higher temperature. In addition, new activators are needed to address the new metallurgy on board surfaces and new

lead-free solders containing Ag, Cu, and much higher levels of Sn. The decrease in pitch for area-array packages has resulted in a need for finer solder powders. This is driving a change in paste flux chemistry since the higher surface area of these fine powders results in increased oxide formation and decreased paste stability.

45.5 FLUX FORM VERSUS SOLDERING PROCESS

Although one usually thinks of soldering flux as a liquid, in fact the soldering flux can exist in several different forms. *Liquid flux* is commonly used for wave-soldering or hand-soldering applications. *Paste flux*, a thick, viscous flux, is used to hold components to the board prior to reflow of the already present solder. Direct attachment of a solder-bumped chip or BGA packages to solder pads on a PWB is an example of paste flux's usefulness. Also known as *tacky soldering fluxes*, these materials are useful in repair of area-array devices. Solder paste contains *solder paste flux*, which is the solder paste without the solder particles. Solder paste is used in surface-mount attachment of components such as chip carriers, quad flat packs (QFPs), BGAs, μ-BGAs, CSPs, leaded packages, and discrete resistors and capacitors. *Flux-cored solder wire* is used for hand-soldering, and *flux-coated or flux-cored solder preforms* are used as the solder/flux source in some applications such as backplane connector pin reflow soldering.

Fluxing underfills can also be considered as a new type of flux material. Many fine-pitch, low-profile array packages suffer from poor reliability due to their low standoff from the substrate, small area of solder interconnection and CTE mismatch with the substrate. Often, a reinforcing material is dispensed around the solder joints after assembly to improve

attachment reliability. Fluxing underfills provide fluxing action for the solder process and cure into a hard supporting material during the soldering process, eliminating the need for a post-solder dispensing step.

45.6 ROSIN FLUX

Early flux formulations for electronics used rosin, which is a naturally occurring resin, obtained from the sap of a pine tree. Its exact composition varies depending on the part of the world from it originates as well as the time of the year. Rosin contains a mixture of resin acids, the two most common ones being abietic acid and pimeric acid (see Fig. 45.1). Rosin has been a favorite material for soldering because it liquefies during the soldering process, dissolves the metal salts, and then solidifies when cooled, entrapping and for the most part immobilizing the contaminants. In addition, rosin has some innate fluxing activity since its molecular structure contains a weak organic acid. Finally, rosin-based fluxes work well in hand-soldering and repair operations because rosin provides good heat transfer characteristics.

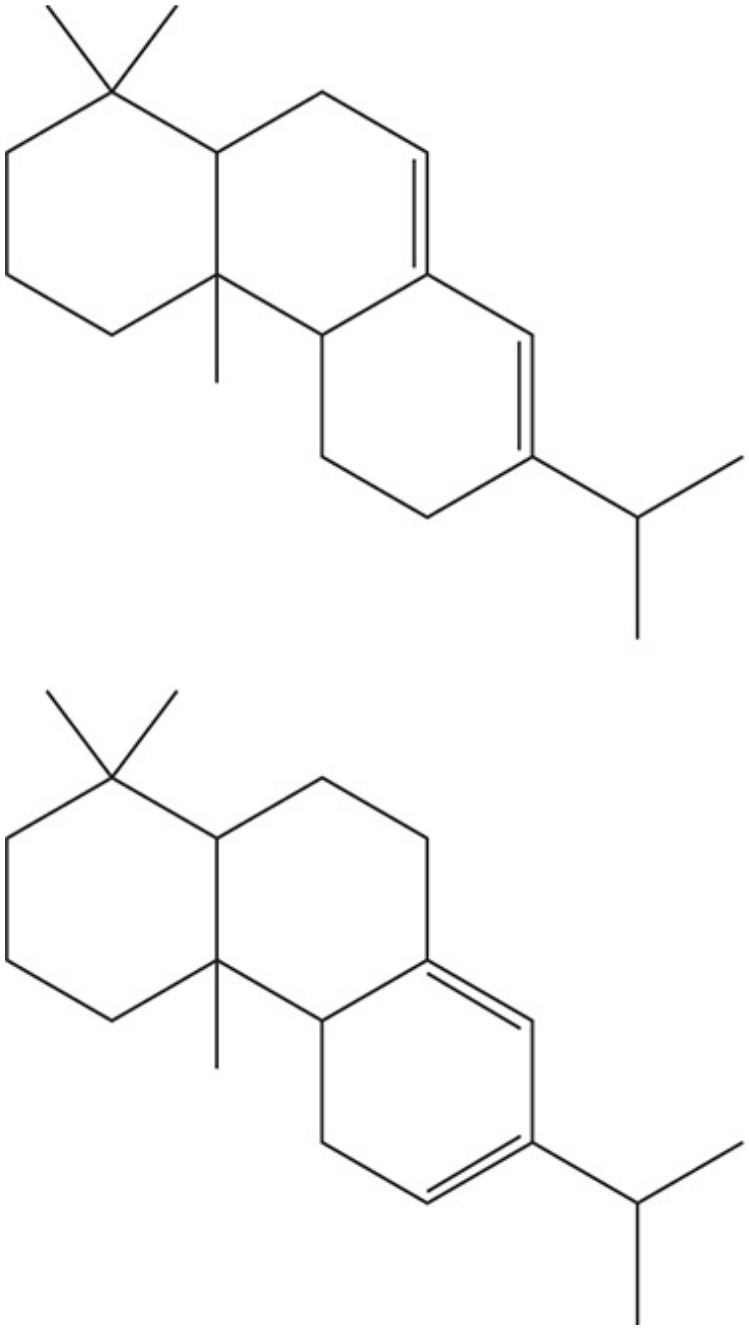

FIGURE 45.1 The two most common rosin isomers are abietic acid and pimaric acid.

The activity of a rosin-based flux will be determined by the activators and surfactants, which are part of the formulation. Some activators help to remove metal oxide but also leave residues that are essentially noncorrosive. Halide-containing

activators leave residues that could be corrosive if too much is left on the board.

Military specifications[4] in the past have required the use of rosin-based fluxes. These were defined as pure rosin (R), rosin mildly activated (RMA), rosin activated (RA), and rosin super-activated (RSA), based upon the level of halide activators they contained. Typically only R or RMA fluxes were approved for high-reliability military applications.

In the 1970s, telecommunication companies in the United States and Europe predominantly used rosin fluxes for their wave-soldering requirements. These companies had their own internal set of test methods for selecting noncorrosive rosin flux formulations. Using their selection criteria, they believed the fluxes to be sufficiently safe. For their applications, they cleaned only the bottom side of the assembly, where rosin residues needed to be removed to ensure good electrical contact during bed-of-nails testing.

In the early 1980s, the IPC developed a flux characterization criteria based on the flux and flux residue activity. Thus, fluxes were classified as:

L = low or no flux/flux residue activity
M = moderate flux/flux residue activity
H = high flux/flux residue activity

These designators were determined by a series of tests, including the copper mirror test, a qualitative silver chromate paper test for chlorides and bromides, a qualitative spot test for fluorides, a quantitative test for halides (chloride, bromide, and fluoride), a corrosion test for flux residue activity, and a surface insulation resistance test at accelerated temperature and humidity conditions.

The industry standard “Requirements for Soldering Fluxes” (J-STD-004A) includes a test for electrochemical migration and updates the earlier IPC-SF-818 solder flux specification to include some international elements from the

International Standards Organization (ISO-9454). In addition to defining the flux categories L, M, and H, it notes the absence or presence of halides by a 0 or 1 that is added to the descriptor. In parallel the international standards, industry standards list the basic chemical constituents as RO (rosin), RE (resin), OR (organic), or IN (inorganic) (see Table 45.4).[5] The test methods for this specification are contained in the Test Methods Document (IPC-TM-650).[6]

TABLE 45.4 Flux Constituents and Activity Levels

Flux Materials of Composition	Symbol	Flux Activity Level (% Halide)	Flux Type
Rosin	RO	Low (0%)	L0
		Low (<0.5%)	L1
		Moderate (0%)	M0
		Moderate (0.5–2.0%)	M1
		High (0%)	H0
		High (>2.0%)	H1
Resin	RE	Low (0%)	L0
		Low (<0.5%)	L1
		Moderate (0%)	M0
		Moderate (0.5–2.0%)	M1
		High (0%)	H0
		High (>2.0%)	H1
Organic	OR	Low (0%)	L0
		Low (<0.5%)	L1
		Moderate (0%)	M0
		Moderate (0.5–2.0%)	M1
		High (0%)	H0
		High (>2.0%)	H1
Inorganic	IN	Low (0%)	L0
		Low (<0.5%)	L1
		Moderate (0%)	M0
		Moderate (0.5–2.0%)	M1
		High (0%)	H0
		High (>2.0%)	H1

45.7 WATER-SOLUBLE FLUX

Water-soluble fluxes have also been called “organic acid fluxes.” This name is misleading since all fluxes used for electronic soldering contain organic ingredients and many contain organic acid activators. The term “organic acid flux” probably originated from the designation of water-soluble fluxes as “organic” and those activated with organic acid activators as “organic acid.” Other activators for these fluxes include halide-containing salts and amines. Although the correct name for this category of fluxes is *water-soluble*, it should also be noted that the flux solvent is normally not water, but alcohols or glycols.

As the name implies, water-soluble fluxes are soluble in water and their soldering residues are also expected to be water-soluble. These fluxes are much more active than rosin fluxes, have a wider process window, and give a higher soldering yield with reduced defects. This means that the final assembly will require less touchup or repair. On the down side, water-soluble fluxes contain corrosive residues that, if not properly removed, will cause corrosion in the field and long-term reliability problems.

As indicated earlier, water-soluble fluxes usually contain glycols, polyglycols, polyglycol surfactants, polyethylene oxide, glycerine, or other water-soluble organic compounds as the primary vehicle. These provide good solubility for the activators, which are usually the more corrosive amines and halide activators. With the onset of highly efficient cleaning equipment, this type of flux became popular for computer and telecommunication applications.

F. M. Zado[7] raised concern in the late 1970s that water-soluble fluxes affect the electrical characteristics of the epoxy-glass laminate by reducing the insulation resistance. This reduction was due to the dissolution of the polyglycols of the flux formulation into the epoxy substrate during the

soldering process. Later work by J. Brous[8] indicated that some polyglycols were much more deleterious than others. In general, polyglycol containing fluxes (and fusing fluids used by board manufacturers to fuse tin-lead plating) can cause an increase in moisture absorbance of the epoxy-glass substrate.

The user must consider several factors when determining whether to use water-soluble fluxes in a given application. One important factor is the operating environment. If the assembly will experience extremes of temperature while under power, it is possible that localized condensation will occur and dendrites will form, shorting out some of the circuit elements. Assemblies of this nature should be conformally coated. A second critical factor is the use of a board design and cleaning process, which ensures that corrosive residues are removed. A third consideration is the voltage gradient in the electrical design of the circuit. Within reduced lines and spacings, a failure mechanism called conductive anodic filament (CAF)[9] formation has been associated with high humidity and high voltage gradients. This will be described in detail in a later chapter.

45.8 LOW SOLIDS FLUX

Until the mid-1980s, liquid soldering fluxes were formulated in 25 to 35 percent (weight percent) solids or nonvolatile liquid. Then flux chemistries changed and new formulations that were lower in total solids content came on the scene. These fluxes are composed principally of weak organic acids, often with a small amount of resin or rosin. Early formulations had 5 to 8 percent solids, but today’s low solids fluxes are 1 to 2 percent solids composition. For lead-free soldering, weak organic acids with higher molecular weight are being used.

Nomenclature of these fluxes moved from “low solids flux” to “low residue flux” to “no-clean flux.” The thinking was that the amount of residue left by these fluxes after soldering was so minimal that it did not need to be removed. This is only true if the residues are noncorrosive.

One challenge of low solids fluxes is the processing window. Unlike water-soluble fluxes that give very low defect levels and have a wide processing window, the soldering process for low solids fluxes must be carefully designed. To begin with, the recommended preheat temperatures are different from those for rosin flux and the preferred solder wave temperature is lower than that for rosin. Additionally, the solderability of incoming boards and components must be ensured. Although water-soluble flux can cut through heavy metal oxide layers, the amount of fluxing ingredients in low solids fluxes is not sufficient to accomplish the task.

Lower cost manufacturing can be achieved with low residue fluxes if the cleaning step can be eliminated. This assumes that the incoming components and boards are clean, and that operators handling the boards are careful not to introduce contamination. This requires a flux with noncorrosive residues that will not impede or contaminate the electrical bed-of-nails test probes.

A new category of low solids fluxes was introduced in the early 1990s to meet the needs of localities where volatile organic compounds (VOCs) are regulated. These fluxes are marketed as VOC-free or low-VOC fluxes. The solvent in this case is 100 percent water or at least greater than 50 percent water. Use of these fluxes requires special care in the preheat step where the water (solvent) must evaporate before the assembly reaches the solder wave. Failure to do this will result in excessive solder ball formation.

Solder fluxes and pastes have gone through significant evolution since the early 1980s. As of 2006, in North America about 70 percent of the fluxes were not cleaned, 25 percent were water-soluble, and 5 percent were rosin-based for

military applications.[10] However, in the lead-free soldering world, more cleaning is required.

45.9 CLEANING ISSUES

Flux removal is motivated by several factors, and the importance of these factors varies with the end use of the product. In general, the purpose of cleaning is (1) to remove corrosive residues from the soldering process or handling operations (some fluxes have high levels of halide activators that would cause corrosion were they not removed); (2) to remove rosin, resin, or other insulating residues that would interfere with bed-of-nails electrical testing; (3) to remove rosin, resin, or other residues that attract dust, dirt, and other airborne contaminants; (4) to ensure that the board is free of residues and contamination prior to conformal coating.

In the early days of soldering, cleaning was either not done, because the flux was mostly rosin and noncorrosive (e.g., the telecom fluxes), or cleaning of rosin flux residue was done with solvents. Typically the solvent was a halogenated material, as such solvents were considered relatively nontoxic and were nonflammable. However, in the late 1970s, the Environment Protection Agency (EPA) listed some of these solvents, such as perchloroethylene and trichloroethylene, as suspected carcinogens and lowered the allowed level of these in the operator-breathing zone. This led to the application of CFC azeotropes with methyl alcohol, ethyl alcohol, and methylene chloride as replacements.

However, the CFCs were not without their own environmental problems. In September 1987 at the United Nations Environment Program Conference in Montreal, 24 countries signed the Montreal Protocol on Substances that Deplete the Ozone Layer. The protocol was the beginning of

an international agreement on the reduction of CFCs that were shown to have a deleterious effect on the stratospheric ozone layer that protects us from harmful ultraviolet radiation. The initial protocol targeted CFCs and halons (bromine-containing CFCs) and proposed a 50 percent reduction in production by 1998 based on 1986 levels. Revisions to the protocol led to a ban on the manufacture of CFCs and other ozone-depleting chemicals effective by the end of 1995.

45.9.1 Solvent Cleaning

With the general elimination of the halogenated solvents, manufacturers have changed their flux and cleaning choices. The new cleaning materials must be capable of dissolving the particular chemical residues from a given flux formulation. Several detailed cleaning references are available.[11,12,13,14,15,16]

Solvent cleaning options[17] have focused on semiaqueous cleaning, solvent defluxing using a blend of solvents, and vapor degreasing using a single or co-solvent mix. Semiaqueous cleaning usually involves a two-step process where the assembly is first cleaned in the organic solvent, then rinsed in a separate step. Terpenes have been widely used as the solvent with dibasic esters and non-ionic surfactants added to improve cleaning and rinsing. An alternative semiaqueous cleaning solvent is composed of high molecular alcohols. The solvent is usually sprayed under immersion onto the assemblies in its pure form. This step is followed by a rinse step that emulsifies the semiaqueous solvent and dissolves the ionic residues. Innovations[18] have shown that an aqueous emulsified solution of the solvent can also provide good cleaning.

Solvent cleaners may be inline or batch. Inline cleaning usually involves spray under immersion. The temperature of

the solvent wash tank is set below its flash point, and several rinse tanks follow the wash tank to ensure good cleaning before the final drying step. Solvents such as glycol-ether blends are used for this process. Batch degreasers may use n-propyl bromide in specialized applications.

Traditional batch cleaning was performed in a vapor degreaser that has a wash sump of boiling nonflammable azeotropic solvent and a rinse sump. A vapor blanket forms above the sump and is contained using cooling coils at the mouth of the machine. The assembly is first placed into the wash sump, and then is transferred to a rinse sump that contains clean solvent from the condensation at the cooling coils. As the assembly is removed, it is held for a period in the vapor blanket for a final rinse and drying of the remaining solvent.

Co-solvent cleaning involves the use of a rinsing agent that is volatile and a solvating agent that is not volatile. The assembly is placed into the wash tank of boiling solvent where the solvating agent enhances the cleaning process. The vapor blanket above the wash sump contains only the rinsing agent. The assembly is moved from the wash sump into the rinse sump, which contains only the condensed rinsing agent. Finally, the assembly is removed from the rinse sump and held in the vapor blanket for a final rinse and drying step.

45.9.2 Aqueous Cleaning

Aqueous defluxing is performed using a high pH saponifying solution that is diluted to a 10 to 25 percent aqueous solution. The saponifier may be organic or inorganic, with additives such as solvents and surfactants to improve wetting and cleaning. The organic cleaning agent usually contains an amine, such as monoethanol amine, whereas the inorganic cleaners use buffered metal salts such as

NaOH/sodium carbonate/sodium bicarbonate. The wash step is usually done in an inline spray machine, followed by a de-ionized (DI) water rinse with several spray sections to remove the more contaminated material, then by a final rinse and a final blow-dry step. The cleaning agents in the saponifier react with the rosin or resin from the flux to form a "soap" in the same manner that the detergent used to wash greasy dishes reacts with the grease and helps it dissolve, or at least be emulsified and removed in the rinse water. Once the rosin or resin is removed, the rinse water solubilizes the ionic residues that were on the surface of the board as well as those trapped within the solid rosin matrix.

Table 45.5 summarizes the possible cleaning agents for the various flux types.

TABLE 45.5 Soldering Flux/Paste Cleaning Options

Flux/Paste Type	Possible Cleaning Agents	Comments
1. Rosin/resin	a. Detergent cleaning	
	b. Semiaqueous cleaning	
	c. Solvent cleaning	
2. Low-residue flux	a. No-cleaning step	If flux is rated L0 or L1 in ANSI-J-Std-004
	b. Aqueous cleaning	If flux does not contain rosin or resin
	c. Detergent	If flux contains rosin or resin
	d. Solvent	
3. Water-soluble	a. Water	
	b. Detergent cleaning	

45.9.3 Flux and Cleaning Issues Related to Lead-Free Soldering

Solder flux residues are much more difficult to clean after lead-free soldering.[19,20,21] Fluxes formulated to remove oxidized metals (SnPb, Cu) for traditional tin-lead soldering must be modified to address the needs of different metallization for the solder, the board finish, and component terminations. Soldering flux formulations for lead-free soldering use higher molecular weight resins and activators for the more aggressive flux chemistry needed to achieve wetting. Also, the higher tin content of the alternative solders (SnAgCu, SnCu) requires more aggressive flux chemistries for good wetting.

The process window for lead-free soldering requires higher peak reflow temperatures and longer times above liquidus. Soldering in a nitrogen environment improves wetting and reduces oxidation of the flux residues and the solder. Due to the higher reflow temperature, greater polymerization of the flux constituents can occur—producing residues that are more difficult to remove.

The cleaning challenge represented by lead-free soldering must be addressed by modifying the cleaning process to increase the wash time, wash concentration, and wash temperature.

Cleaning for fine-pitch components soldered under lead-free conditions requires an increase in cleaning time, the use of increased solution agitation (e.g., ultrasonic), and the modification of spray nozzles and impingement angle. Flux residues are more difficult to remove when they set. Thus, it is important to minimize the time between reflow and cleaning. Aqueous cleaning chemistries should include wetting agents, solvating agents, and reactive agents. Water-soluble fluxes that can be cleaned with water after lead-based soldering conditions may require the addition of

some cleaning agent to remove the higher molecular weight organic acids and the tin salts created when the flux decomposes during lead-free reflow.

45.10 SUMMARY

This chapter has reviewed the processing issues and materials used for the soldering and cleaning processes. In the lead-free era, thermal profiles and component maximum temperatures require different reflow profiles. The various types of soldering fluxes, their constituents, and their role in the soldering process have been discussed and the formulation changes required for the higher temperature soldering examined. Cleaning materials and processes have been identified and the challenges with higher temperature soldering discussed.

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CHAPTER 46
SOLDERING FUNDAMENTALS

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

46.1 INTRODUCTION

The complexity of printed circuit assemblies continues to increase in every sector of the electronics industry. The number of solderable contacts of IC components is on the rise. In the portable electronics segment, smartphones dominate the consumer market. They have ever-increasing computer functionality with integrated optics for video and still photography, accelerometers for phone position sensing, audio systems including miniature speakers, GPS, storage for addresses, calendars, music and video players, Wi-Fi, Bluetooth, and more. They are rugged, shock-resistant and some are even waterproof, all packaged in a form that fits in the pocket.

Smartphones, smart TVs, gaming appliances, cloud storage and other smart devices, online banking, buying, stock transactions and myriad of other applications has spurred a new Internet boom. This has driven increased

reliance on and need for more powerful computer servers, routers and storage, which in turn has driven the need for more complex computer room equipment and a miniaturization of sorts as more computational power needs to fit into the same space for economic reasons. Today, blade servers are quite common and these powerful, modular, swappable units are small, energy efficient and run cooler all adding to the value proposition for computational service and cloud storage providers. The form factor for a blade is described as “1U,” meaning 1 unit that can fit into a 19-in rack, where 1U is 480 mm (19 in) wide and 44 mm (1.75 in) tall. Each blade may be composed of one to over hundred servers. In order to achieve this compactness, device input/output (I/O) has had to increase, electronic device package size has had to decrease and printed circuit board (PCB) layer-count has increased to aid in routing traces in the confines of the 1U form-factor.

Higher density boards and higher layer counts result in more thermally massive assemblies, which are difficult to solder during surface-mounting and doubly difficult to assemble by the wave solder process. Through-hole technology, although on the wane, is still prevalent. When both surface-mounting and wave soldering are used on the same assembly, it is referred to as mixed-mount technology. The proliferation of press-fit connections [force fitting compliant electrical contacts into a circuit board’s plated through-holes (PTH)] has alleviated some of the problems of mixed-mount assembly driven largely by the difficulties faced in wave soldering large and thick circuit boards. See Chap. 51 for an introduction to press-fit technology. Land grid arrays (LGAs) with separable pressure interconnect have become more prevalent especially for high-end motherboards for computing and telecommunications. LGA incorporation on a board has influence on layout and implications for soldering. This will be discussed in Chap. 52.

Soldering is a technology that has been used extensively for utilitarian and decorative purposes for thousands of years. The Romans and especially the Celts were masters of this art. In the last 100 years or so, soldering has been raised from art to science mainly driven by the need for joining electrical assemblies. By the late twentieth century, the tin-lead solder joint and properties of its constituent materials had been studied well enough that it could be modeled for purposes of predicting wetting, solder shape and reliability.

Circuit board soldering has traditionally been accomplished with eutectic or near eutectic tin-lead (Sn-Pb) alloy. The eutectic alloy is approximately 63 percent Sn and 37 percent Pb by weight (alloy Sn63) and was the mainstay of printed circuit board assembly until recently. A binary alloy (composed of two constituent metals), its melting, wetting, solidification and reliability are well understood and predictable. Being a eutectic alloy, it has a distinct melting point and for eutectic Sn-Pb that point is 183°C. This temperature is low enough that it is compatible with a significant set of materials such as circuit board laminates, integrated circuit (IC) package molding compounds and encapsulants, ceramics used for packaging, silicon IC devices, molded connector bodies, etc. Materials for these components were in part codeveloped to be compatible with Sn-Pb soldering processes. Now the electronics industry has made the move largely to lead-free (Pb-free) solders. This massive industry change was driven by the European Union's (EU's) environmental initiatives to limit electronics waste and restrict toxic materials used in electronics manufacturing.[1,2]

The main thrust of the EU directives was to limit or ban a short list of materials that the EU deemed harmful to the environment. Lead (Pb) is most prominent on the list of restricted materials, and limitations on its use have had the most dramatic impact on electronics manufacturing, since Sn-Pb solder was the preferred alloy for electronics assembly

worldwide. Now the industry has largely transitioned to Pb-free solder alloys. Most viable Pb-free alloys have a higher melting temperature than Sn-Pb and most Pb-free alloys are composed of three or more metals.

46.2 ELEMENTS OF A SOLDER JOINT

There are four important constituents of a solder joint: the two materials or surfaces to be joined, the solder itself and the process by which the materials are joined. Each has its own set of attributes and variables that contribute to the ease and quality of soldering. A delicate balance of material conditions and process parameters determine the solder joint appearance, resultant strength, and reliability of the finished assembly. The composition of the solder, the surface finish on lead, pad or PTH, environmental factors, chemical implications, and thermal conditions all impact the soldering process. Each will be discussed.

46.2.1 Common Metal-Joining Methods

Welding, brazing, and soldering are the three most widely used metal-joining techniques. Although this section does not provide a rigorous review of welding and brazing, a cursory comparison of these metal-joining processes is useful in setting the stage for a discussion of circuit board soldering. All three depend on metallurgical alloying; mixing and wetting of two or more molten metals.

Welding involves heating of two similar or dissimilar abutting metals to the point that they fuse into one another. Unlike brazing and soldering, there is considerable depth to the metallurgical changes in welding. Sometimes another

metal or filler metal is applied to lower the melting temperature of the weldment metals, to promote wetting or for desired mechanical properties of the finished bond. As in brazing and soldering, sometimes chemical treatment is required to help dissolve surface oxides and also a cover gas may be applied to retard oxidation during the high temperatures of the welding process. Typically welding is a very high temperature process; hot enough to melt the surfaces of the metals to be joined.

Brazing and soldering always involve the use of a filler metal (brazing compound or solder), which has a significantly lower melting point than the basis metals associated with the two bonding surfaces. The filler material must be able to alloy with the surfaces to be joined. As the filler is heated to liquidus, there is near-surface metallurgical dissolution and mixing (alloy formation) with the contacted bonding surfaces. Continued heating above the liquidus temperature of the filler metal results in its further spreading and alloying via molten metal surface tension effects. As the bonding surfaces are cooled, the filler metal returns to solidus and a bonded assembly results.

There are only subtle differences between soldering and brazing, the primary distinction being the temperature required for joint formation. Brazing is generally accomplished at a relatively high temperature (>450°C) as compared to soldering. (There is no consensus in the literature, but values between 400 and 500°C are commonly cited.) Brazing temperatures would be detrimental to most electronic components and PCBs. Since circuit board assembly is done almost exclusively by means of soldering at temperatures generally below 270°C, this chapter is devoted to that traditional joining method.

46.3 SOLDER OVERVIEW

Solder is the cement that joins lead to pad, imparts the mechanical robustness required for a reliable assembly, and also possesses the electrical conduction needed for circuitry. The metallic alloy choice, the solder, is chosen for a melting temperature compatible with other materials associated with the soldered assembly. It must be metallurgically compatible with the metals to be joined. Once molten, the solder must wet to the component lead and circuit board bond pad. Upon solidification, the resultant solder joint must provide sufficient electrical conductivity, bond strength and reliability for the intended application. It must resist corrosion, vibration, shock, thermal expansion and contraction cycles over a range of temperatures and environments commensurate with the assemblies use. All the factor are dependent on the materials used in and associated with the soldering process including the solder itself.

With the onset of RoHS and the wide adoption of Pb-free solders, tin (Sn)-silver (Ag)-copper (Cu) solder alloys, called “SAC,” have become the most prevalent alloy family. There is no clear consensus on which solder alloy is the best, but SAC305 is widely used. The “305” designation indicates that the composition is 3 percent Ag by weight, 0.5 percent Cu and the balance Sn. Although the industry has moved to Pb-free, a quick overview of the Sn-Pb system is provided for grounding in solder technology. It is a simple binary system (two-metal alloy) and much easier to understand and demonstrate than SAC solders (ternary systems … composed of a three-metal alloy). It is the best understood metallurgical system in terms of soldering, with very predictable bonding attributes.

Since the start of electronics, Sn-Pb eutectic alloy has been the dominant solder alloy choice. A eutectic alloy goes molten at one distinct melting point as opposed to a noneutectic alloy, such as SAC, which has a melting range but not a distinct melting point. Sn-Pb eutectic alloy possesses a relatively modest liquidus temperature (183°C)

and a molten working range typically about 205 to 230°C. This overage in temperature by about 20 to 50°C is the temperature range applied during the soldering process to ensure that all parts have achieved a temperature commensurate with good soldering and all solder joints are wetted sufficiently. It also may be necessary to reach such temperatures on thermally massive boards where the lightest parts may heat quickly while the most thermally massive parts may just barely achieve a temperature adequate for soldering. Everything in the electronics industry was tailored to working in that temperature regime. ICs and passive components, laminates, and process equipment associated with soldering have been qualified for use at those temperatures. Over the last several years, the electronics manufacturing industry has been adjusting materials and strategies to accommodate Pb-free soldering, since Pb-free alloys typically have liquidus onset of approximately 215 to 227°C depending on alloy choice. Adding a thermal overage as described for Sn63, then solder process temperatures for Pb-free alloys may be in the range of 260°C; a challenge to many of the conventional materials used in circuit board assembly.

46.4 SOLDERING BASICS

The case presented below is based upon eutectic Sn-Pb solder (Sn63) in contact with solderable and nonsolderable coatings on a basis metal.

Primary soldering steps include

- Intimate contact of the solder to materials being joined
- Slow application of heat to warm the parts to be soldered
- Oxide removal from the surfaces to be joined and from the solder itself

- Application of heat sufficient to melt the solder
- Solder wetting to joining surfaces and intermetallic formation
- Quenching of the solder liquidus

There are a few other materials that need to be covered for this discussion. The first is solder paste. This is a mixture of minute solder beads, flux, and other materials to give the paste specific rheological properties for dispensing, most notably stencil printing, and chemical agents for metal surface preparation. For surface-mount applications, it is typically stenciled onto PCB bonding pads. The paste is also formulated to hold its printed shape, even at elevated temperatures, otherwise, it would slump and cause solder bridging from bond pad to bond pad. Once printed, the electronic component is placed upon the solder paste deposit. The paste holds the component in place during the reflow process prior to the onset of solder liquidus. The second term is flux, which, as mentioned previously, is a key component of solder paste. Oxides, tarnishes and other contaminants inhibit soldering. Flux is a heat-activated chemical agent used to clean and strip oxides and tarnishes from otherwise solderable metal surfaces. Flux will be covered in subsequent sections of this chapter.

46.4.1 Intimate Contact of Solder to Surfaces to Be Joined

The most basic requirement is for the solder to contact the materials to be joined. The contact area of the solder is not wholly important as long as the solder is in point contact with the surface to be soldered when it reaches liquidus. Surface tension effects and metallurgical wetting will complete the spreading of solder between component lead and PCB pad.

46.4.2 Slow Heating of Boards and Parts to Be Soldered

This is important for three reasons: (1) Overly rapid heating can cause certain electronic devices to experience thermal shock and subsequent failure as in cracking or may cause degradation of device electrical characteristics. (2) Solder paste may spatter if heated too rapidly. (3) appropriate heating rate is crucial to good surface preparation through fluxing. A balance between time and temperature has to be determined so that the flux has enough time to accomplish its cleaning step and does not dry out prematurely or spatter. Conversely, an inappropriately long heating cycle may cause re-oxidation of flux-cleaned parts. If the process temperature is too high, the flux can denature and bake onto otherwise solderable surfaces and inhibit soldering.

46.4.3 Oxide Removal from Bonding Surfaces and from Solder

Most materials, when in equilibrium with Earth’s oxygen-rich environment, develop an oxide coating. Upon heating, solder surfaces as well as the bonding surfaces will more thoroughly oxidize in a normal air environment. If a silver-bearing surface is exposed to a sulfur-containing ambient (sulfur-tainted air, pollution), sulfidation occurs and that tarnish also inhibits soldering. Generally, the higher the storage temperature, the more oxidation is present unless oxide growth is self-limiting, as it is in some materials. The same holds true for soldering process temperature or process time. Higher temperature and/or the longer process time, results in thicker oxidation or tarnish on most metal surfaces and also may render the flux ineffective also.

An oxide or tarnish coating acts as a physical barrier preventing the molten solder from contacting metals to be joined. In the case of gold (Au), known to remain largely oxide-free, there is insufficient oxidation to degrade soldering. But unless oxidation is removed from the solder itself, soldering Au may not be possible or will be incomplete. Note that in most soldering processes, the ambient can be altered to mitigate the detrimental effects of oxygen or other airborne contaminants. This will be discussed later.

The most generally applied remedy for the effects of oxidation and tarnish as relates to the soldering process is the application of a chemical agent, flux. It is formulated to react with specific metallurgies for removal of tarnish and oxidation. It also acts as a barrier preventing fluxed metal surfaces from reoxidizing prior to and during the joining process. The word *flux* comes from the Latin *fluxus*, which means flow or flowing. Flux ensures that the solder, once molten, will flow over the surfaces to be bonded, unconstrained by oxide skins on the solder or the metals to be joined. Certain materials form oxides very rapidly, and some oxides are rather chemical-resistant. Nickel is one such element. Copper, like nickel, can also form resistant oxides and may necessitate the use of strong fluxing agents to achieve a bondable surface. Tin and silver oxides are easily attacked by even weak organic acids. Gold, which is known to remain oxide-free, can be applied as a thin, nonporous barrier over less noble, oxide-stripped metals such as nickel. During reflow, the gold dissolves quickly into the solder and the solder bonds to the underlying oxide-free nickel. Figure 46.1 shows the difference between a solder wettable surface and a flux-resistant oxide-coated surface.

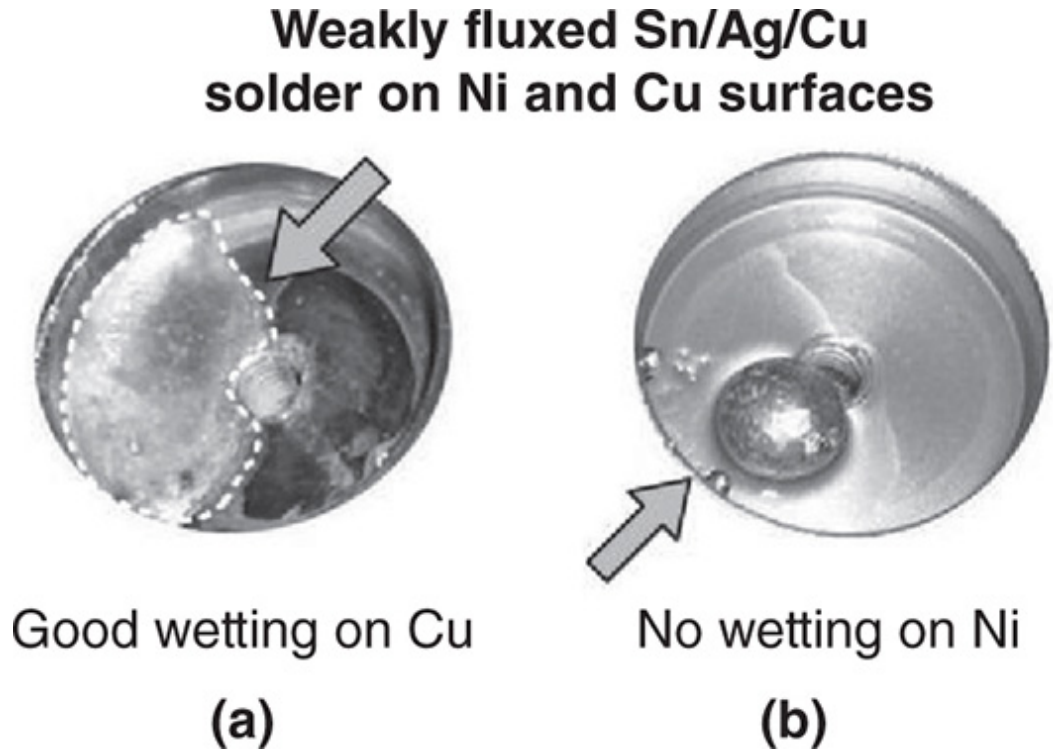

FIGURE 46.1 Comparison of soldering to copper (*a*) and nickel (*b*). In both cases, surfaces were treated with a weak organic solder flux and equal amounts of Sn-Ag-Cu solder were added prior to heating. Both were heated simultaneously to 235°C for 2 min. Note that in the case of the copper surface (*a*), the solder has wet and spread, characterized by a low wetting angle (the extent of wetting is indicated by the dashed outline). In the case of the nickel surface (*b*), the flux was ineffective in penetrating the surface oxide and the solder beaded up on the surface of the nickel; an indication of non-wetting. (*Courtesy of Hewlett-Packard*.)

Several types of fluxes are available for soldering, but only two broad categories are in widespread use. The first is aqueous-clean, also known as water-clean flux. This is generally composed of relatively strong organic acids and may be fortified with halogens to increase its chemical activity. Aqueous-clean formulations are meant to be thoroughly washed from the surface of the printed circuit assembly after soldering to prevent metal corrosion and ensuing electrical failure.

There are several electrical components that make aqueous-clean chemistry less attractive. These include dual inline package (DIP) switches (sealed switches, which are known to leak), high-density connectors, large area-array

packages, micro-BGAs, and any other components with low headroom between the underside of the package and the surface of the PCB. It is for this reason, plus the opportunity to eliminate an expensive and vagarious process step (aqueous-cleaning) and associated equipment, that the vast majority of electronics manufacturers have widely embraced soldering fluxes that require no cleaning.

The second broad category is termed “no-clean” flux. No-cleans are composed of resins or rosins with additives to make them chemically active to varying degrees. They are formulated so that the post-soldering residue is inert and can remain on the board obviating the need for cleaning.

46.4.4 Heating to Liquidus

Once heated to melting and oxide-free, solder begins to wet to oxide-free, solderable surfaces. It forms a metallurgical bond with contacted metals by dissolution of the surface, alloying with it. Of course, this process is dependent on having a largely oxide-free surface on the solder and the metal to be soldered. Once the wetting is initiated, alloying proceeds slowly, causing the solder to spread on solderable surfaces. The molten solder is drawn by surface tension to fill fine capillaries as between component lead and PCB bonding pad, and surface tension draws the solder up and around wettable surfaces forming *fillets*. Once solidified, the solder fillet acts as a mechanical gusset imparting strength to the resultant solder joint.

46.4.5 Solder Fillet Formation

The solder fillet is an overt manifestation of surface tension and wetting. Fillets are readily apparent in Fig. 46.2*a*, which

shows the fillet as a web of solder extending from the PCB bonding pad to the lead of this surface-mount component.

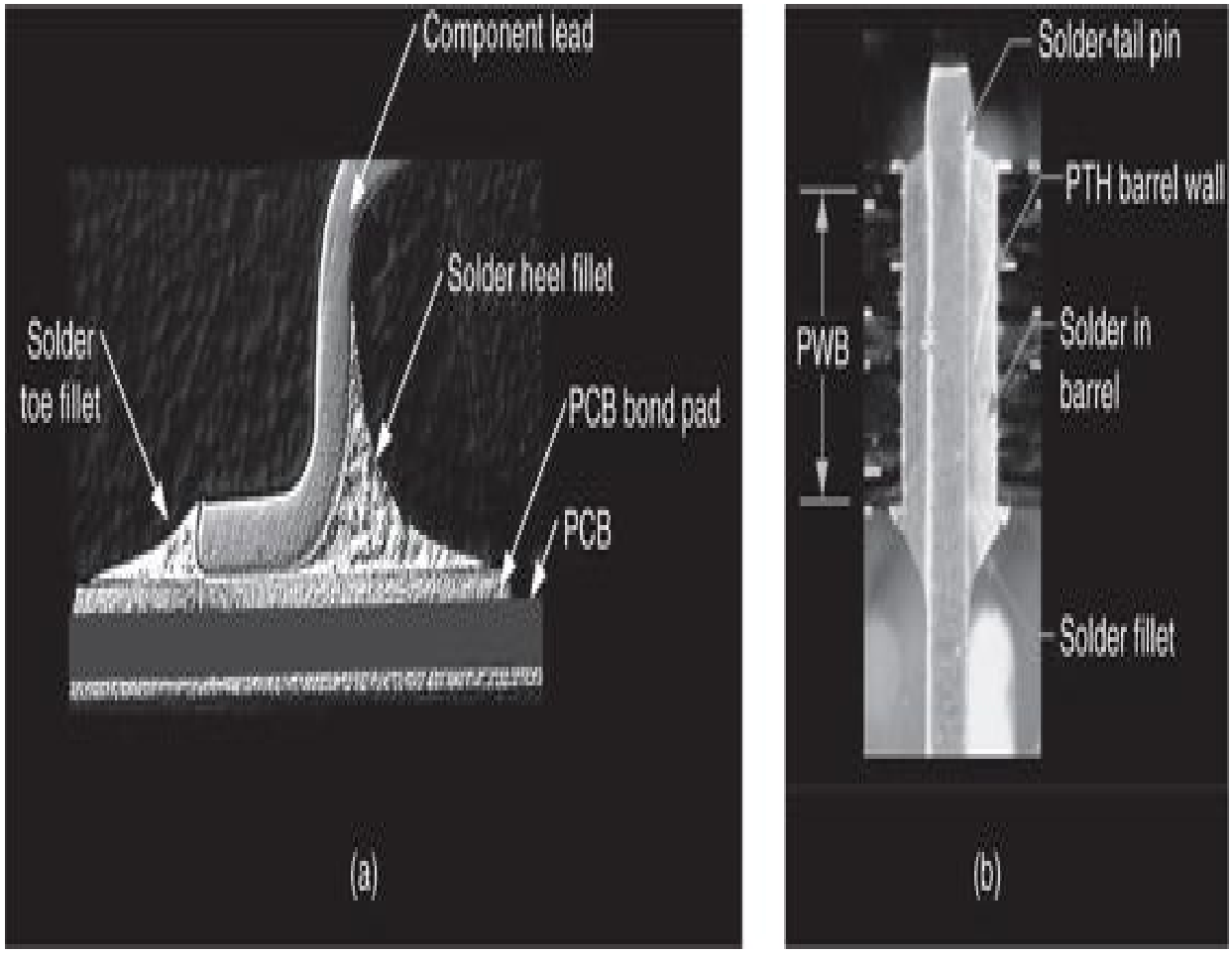

FIGURE 46.2 Solder fillet formation: (*a*) cross-section of an SMT solder joint, (*b*) a PTH solder joint. In the case of the SMT joint, solder has wet to pad and lead. Low wetting angles and good fillet formations are indicative of good solder wetting. The PTH solder joint shows good fillet formation on the secondary side of the PCB. At the top, the primary side, the fillets are not as well formed, probably due to lower temperature at the top-side of the board and onset of solidus before the wetting was complete or from a lack of solder. (*Courtesy of Hewlett-Packard*.)

Such gull-wing leads rely on good heel fillets for solder joint strength. Toe fillets may be present or absent depending whether there is exposed copper or other oxidized or unsolderable, exposed metal at the lead tip, where the lead-frame was excised from its tooling strip. Conventional no-clean fluxes as used for PCB assembly are

not strong enough to remove oxides from bare copper. Toe fillets are of little importance, adding no appreciable strength to the soldered assembly. The bulk of the strength comes from the heel fillet and the solder wetted to the capillary between the top of the bond pad and the bottom of the component lead. Similarly, side fillets may be present, but if the component lead width is on the order of the bond pad width, there may not be enough room to develop good side fillets. The wetting angle is also known as the *dihedral angle*. A low dihedral angle is an indicator of good wetting.

For an example of a PTH solder fillet, see Fig. 46.2*b*. The fillet is a reasonable indicator of the degree of solder wetting and, therefore, of process goodness. It is generally believed that the higher solder fillet, the better the solder joint, but high fillets can be indicative of three problems: (1) excessive heating, which can result in brittle solder joints; (2) excessive solder volume, and in the case of the gull-wing lead-form, and (3) loss of component lead flexibility which may affect solder joint reliability. If too much solder wicks up the lead, it may cause solder shorting, particularly near the package body, where the lead spacing may be finer than at the distil end of the lead. Therefore, fillet examination alone is not sufficient to accurately assess soldering process performance. But, for a fixed set of process parameters, fillet appearance may provide a good means of first-pass comparative assessment of solderability and soldering results.

46.4.6 Intermetallic Compound Formation

Intermetallic compound (IMC) formation is the key to soldering. IMC is the local alloying created at the boundary of the solder liquidus and the surfaces of the metal with which it is in contact. It is the essence of solder bond. There is

much misinformation about IMCs. One thing is certain: without intermetallic formation, there is no solder joint. This is stressed because some erroneously claim lack of IMC in such processes as laser soldering. In the case of that technology, the IMC can be exceptionally thin immediately after soldering due to the short time of liquidus, but it is and must be present for soldering to occur. High temperature, time, and intimate contact of the liquid solder enhance the rate and volume of intermetallic compound formation. The IMC is a crystalline intermediate alloy phase composed of some or all of the contacting metal constituents. This high-alloy concentration region generally has properties that are vastly different from those of either the solder or the contacted metals. Solder is thought of as a soft, forgiving material of low melting-point and good electrical conductivity. IMC, the essence of soldering, is the greatest irony of soldering technology. Although it is the basis for the actual bond, it is in fact, a brittle, high melting-point composition of generally poor electrical conductivity.

The IMC layer will grow over time even at room temperature. There are compositional mechanisms that slow its growth as in the case of Sn63 where Pb crystals line up and retard IMC advancement. Initial IMC thickness is largely predicated on the temperature and the time above liquidus. The thicker the IMC, the more brittle the solder joint; this is but one important reason that precise process control in soldering is required.

46.4.7 Cooling and Phase Change to Solidus

As the solder approaches solidus, the rate of IMC formation decreases. When it does reach solidus, the solder joint is formed. It is critical that the solder freezes prior to circuit board handling for two important reasons. First, accidental

movement of the PCB may cause the components to move in the molten solder. This could result in defects such as solder joint opens (dis-bonds) or solder shorts (unwanted bridging of solder from one bond pad or from one lead to the next). Second, a solder joint disturbance at the critical transition from liquid to solid may result in a bond of degraded reliability. This type of bond has an inherently grainy look and can even have microfractures within caused by motion-induced interruption of orderly crystal growth during solidification.

The cooling rate at the tail end of the process is as important as at the onset of heating. Extreme cooling rates may result in electrical device cracking or electrical performance degradation induced by differential contraction of materials.

More in depth discussions of soldering is included in subsequent chapters on soldering materials, fluxes, and process.

46.5 REFERENCES

1. Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE). The European Parliament and the Council of the European Union.
2. Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment, The European Parliament and the Council of the European Union.

CHAPTER 47

SOLDERING MATERIALS AND METALLURGY

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

47.1 INTRODUCTION

Design, materials, assembly, and usage are the parameters that dictate reliability of a printed circuit assembly (PCA). They all have profound impact on the individual solder joint, electronic device reliability or the reliability of the whole assembly. Design engineers must consider all of these factors when laying out a printed circuit board (PCB) and choosing components for same. Temperature extremes, thermal excursion ramps, mechanical shock and vibration, the number of power (on-off) cycles expected over its lifetime, exposure to airborne particulates, gaseous pollutants, humidity, and handling during shipment and use must be considered for the design. It also behooves the design engineer to consider the rigors of PCB assembly. Subtle changes in design can have dramatic impacts on the assembly process.

The process engineer needs to be cognizant of the influence of the process on every electronic component on a circuit board and the whole PCA. Each exposure to reflow or rework will influence the ultimate reliability of the product as will the choice of solder alloy, solder flux, or PCA handling during the process. It is important to use materials and equipment as intended. For example, overheating a flux or solder paste may dramatically alter the quality of a solder joint. Too hot a reflow process may cause brittle solder joints. A poor soldering profile may result in excessive entrapped voids in solder joints. Improperly stored ICs may suffer subtle damage during soldering. Components designed for wave soldering may not be appropriate for oven reflow soldering. Uncontrollable hand soldering methods may lift solder pads. Mechanical flexure or interference with storage racks on the factory floor may impact a PCA. These are but a few of the many process or materials shortcomings that influence the reliability of the final product.

The process engineer must possess excellent interdisciplinary skills to foresee and avoid process issues associated with mechanical forces, chemical influences and thermal consequences on a solder joint, electrical device, or PCA. The choice of process materials (solder, flux, adhesives, etc.) has bearing on the reliability of the finished product. If a PCA is assembled according to a strict, well-understood process with known and constant materials, it will have a reproducible reliability profile.

In some cases, the cost to repair a PCA or an entire product may exceed the value of the combined material and labor content of the first-pass assembled product. It is also well understood that the reliability of a repaired assembly is not as good as a properly soldered first-pass printed circuit assembly due to additional board handling and solder joint degradation as a result of resoldering. The repair solder flux chemistry and how it is applied and heated may also impact product reliability. These points reinforce the need to

understand PCA processes thoroughly and to solder properly the first time. The materials and requisite solder joint reliability properties for a desktop computer are markedly different from those for an automotive ignition system which are unlike those for a smart phone. As such, this chapter will strictly avoid offering up generalized rules for all soldering process applications. Instead what is presented are the fundamentals of metallurgies as relates to the assembly of the PCB.

47.2 SOLDERS

47.2.1 Alloy Systems

Nearly all solders are alloys. An alloy is formed by combining two or more metals in a molten state. When cooled, alloy properties are dependent on constituent metals and the ratio of the number of atoms of one constituent to the atoms of the other(s). Variations in these atomic ratios result in alloys of vastly different properties that are exploited to suit a particular application. Melting points or melting ranges can be adjusted, as can hardness, tensile strength, shock resistance, etc. In alloy formulation, adjustment of one constituent to achieve a suitable melting point will likely cause an impact to other material properties. Mechanical properties, for example, may degrade to the point that the alloy may not be suitable for its end-use application even though its melting point or melting range is ideal. Such is the case in the search for lead-free (Pb-free) alloy substitutes. Although the electronics industry made its dramatic move to Pb-free soldering several years ago predicated on the European Unions WEEE[1] and RoHS[2] directives, to date, no direct replacements approximate the properties of the well-understood standard of eutectic Sn-Pb (SN63 alloy) solder. In most cases, liquidus temperatures (the temperatures at

which a material goes from solid to liquid) of the Pb-free solder alloys are higher than that of eutectic Sn-Pb. As a result, the adoption of Pb-free alloys has imparted changes to process, process equipment, PCB laminates, electronic components and finished assembly reliability.

Families of alloys that are created from two or more metals in different ratios are called alloy systems. Tin-lead (Sn-Pb) is one such system, available in any number of compositions (50Sn-50Pb, 60Sn-40Pb, 10Sn-90Pb, etc.). Some solder alloys are composed of two elements. These are binary alloys such as Sn-Pb or tin-bismuth (Sn-Bi). Others are ternary systems such as tin-silver-copper (Sn-Ag-Cu), which is also commonly referred to as *SAC* [for the “S” in Sn (tin), the “A” from Ag (silver), and the “C” from Cu (copper)]. SAC305 is the alloy designation for 3.0 weight-percent Ag, 0.5 weight-percent Cu, and the balance Sn. Similarly SAC3807 is the designation for 3.8 weight-percent Ag, 0.7 weight-percent Cu, and the balance being Sn.

Quaternary alloys are composed of four elements (e.g., Sn-Ag-Bi-Cu) and pentanary alloys, five (e.g., Sn-Ag-Cu-In-Sb). Quaternary alloys are least understood, binary systems are best understood and easiest to formulate. Small differences in compositions (0.5 weight-percent) as seen in ternary, quaternary, and pentanary systems are difficult for solder vendors to control accurately during formulation. Also, in wave soldering, where the solder pot contents are in constant contact with metals from component leads and circuit board surface finishes, materials will be dissolved into the molten charge in the solder pot and will effect solder composition over the long term. Naturally, the minor constituents of a solder will be altered or depleted more quickly in such a situation.

47.2.2 Tin-Lead Solders

These alloys were the staple of PCB assembly until recently and still are used in some RoHS-exempted applications, with SN63 being the most prevalent. Knowledge of the simple Sn-Pb binary, the de facto standard of soldering, will set the stage for understanding and choosing Pb-free alloys.

47.2.2.1 The Sn-Pb Eutectic Alloy. Sn and Pb can be formulated into many alloys but its eutectic alloy is the most familiar to the electronics assembler. A eutectic alloy is characterized by having a distinct melting point rather than a melting range and its melting point below its constituent metals (Table 47.1).

TABLE 47.1 Sn-Pb Constituent Melting Points Compared to Its Eutectic Melting Point

Material	Melting Point, °C
Sn	232
Pb	327.4
Sn63wt% Sn:37wt% Pb*	183*

*Eutectic alloy composition.

The eutectic composition has the lowest melting point of any other members of its alloy family. At the eutectic temperature, the eutectic metals coexist in a liquefied alloyed state as opposed to a state where there are some solids of one metal and liquid of the other as often is the case in ternary alloys and above.

SN63 is a ductile metal exhibiting a melting point of 183°C, a temperature benign for most materials associated with or attached to a printed circuit board. Its fatigue resistance is sufficient for most commercial applications. Sn-Pb is easily fluxed by very weak organic acids and its shelf-life in terms

of solderability is long lasting and generally not an issue. There are many solder alloys to choose from, but few as compatible as eutectic tin-lead when it comes to production assembly soldering of PCBs. There are also several metallurgical properties that make this alloy attractive as a solder, which explains why it was so widely embraced and the paradigm by which all solders are gauged. That is not to say that other metal alloys cannot be substituted, but this composition has endured the test of time and countless investigations for alternatives.

When noneutectic Sn-Pb alloys melt, phases of Sn or Pb precipitate out of the liquid solution and give rise to a solid-liquid mixture with broad melting range rather than a discrete melting point. The further from the eutectic point, the greater the band of the melting range for the alloy. This region of broad melting temperature is known as the “pasty” or “plastic” range. Noneutectic compositions do not solidify as quickly as eutectic alloys. Because eutectic solders nucleate and crystallize very rapidly at the solidus point, fine grain growth and high mechanical strength in the solidified solder joint result. Upon solidification, noneutectic compositions result in internal stresses and coarse, dull solder joints with perturbed surfaces. These are all points in favor of using eutectic or near-eutectic solders for circuit board assembly.

47.2.2.2 High Pb-Content Solders. High Pb content Sn-Pb solders are known for producing compliant solder joints owing to elemental lead’s high ductility. Due to high melting temperatures, these alloys are generally used to solder nonorganic circuit board substrates like ceramic. An organic laminate such as glass-epoxy is likely to incur degradation through a reflow cycle at such temperature extremes as required by alloys as 5Sn-95Pb (melting range 301 to 314°C) and 10Sn-90Pb (melting range 268 to 302°C). For these solders, the assembly process temperature is generally

chosen to be about 20 to 40°C higher than the melting point or the upper bound of the melting range for reflow and even higher for wave soldering. High-temperature solders are difficult to work with and are relegated to niche applications such as ceramic hybrid circuits or as a contact material for ceramic ball grid array (CBGA) and ceramic column grid array (CCGA) packages and hand-soldering operations. Even in these applications, the solder ball or column is often soldered to the package using a lower melting-point formulation.

47.2.2.3 Tin-Lead Additives

47.2.2.3.1 Antiscavengers. Occasionally a small fraction of silver (Ag) is added (up to 2 weight-percent) to retard Ag scavenging. Scavenging occurs when there is the propensity of one metal to dissolve rapidly and thoroughly into another upon reaching liquidus. A good example would be silver traces on a thin-film ceramic device and the use of Sn-Pb solder to bond to it. During soldering, the Ag would readily dissolve into the Sn-Pb. If too much Ag is dissolved, then the bonding pad on the thin-film ceramic device may be rendered unsolderable due to the lack of a wettable surface finish. The addition of Ag to Sn-Pb solder slows the dissolution rate of Ag from the thin-film ceramic bond pad and retards scavenging.

47.2.2.3.2 Brighteners. Sometimes Ag is added to solder to improve wetting, making the solder joint smooth and shiny. When not used as a scavenger, the addition of Ag should be avoided as it is not usually needed for most electronic joining applications with Sn-Pb.

47.2.2.4 Sn-Pb Intermetallic Compound.

Intermetallic compound (IMC) is the localized alloy created at the interface between the solder and the surface to which it is wetted. Without IMC creation, there is no solder bond. IMCs are thin, brittle bonds composed of the constituents of both

the solder and the metal to which the solder is wetted. In the case of Sn-Pb solder wetted to Cu, the intermetallics present would be Cu_6Sn_5 and Cu_3Sn. Note the Pb is not part of the bond interface. Instead it has been alloyed with Sn (m.p. 232°C) to depress its melting point and for the metallurgical properties it imparts to the solder joint. Pb retards Sn-Cu intermetallic formation by piling up at the intermetallic boundary, frustrating further tin-copper intermixing. Sn-Cu intermetallic compound, while crucial for solder joint formation, imparts brittleness to the interface and the thicker the IMC, the more brittle the interfacial boundary. Solder joints with overly thick IMCs are more prone to failure during thermal cycling or mechanical shock. Thickened IMC layers come from overheating a solder joint either during initial assembly or during subsequent assembly processes.

Although Sn-Pb solder is known for its ability to wet well to a number of component lead platings and circuit board finishes, Pb actually inhibits wetting and keeps the solder localized to the targeted solder joint area. Excessive solder spreading can be detrimental in three ways. First, if solder wicks away from the intended solder joint area, the resultant joint will be solder starved, weaker than intended. Second, if the solder were too mobile, it would wick up connector leads and into the connector, decreasing inner contact flexibility, decreasing contact gap, and changing connector contact physics. This may result in a less reliable interconnect. Finally, if the solder wicks up too high on a gull-wing component lead, it would inhibit the flexibility of the component lead making it more susceptible to mechanical failure.

47.3 SOLDER ALLOYS AND CORROSION

Just as some metals are more corrosion resistant than others, the same is true of solder alloys. When a solder corrodes on a circuit board, it is more than an aesthetic issue. Contaminants on the surface of the PCB between adjacent, oppositely charged conductors can result in corrosion dendrites. These are tiny conductive crystalline filaments or filamentary networks that may extend from one conductor to the next. They may cause hard shorts that prevent an electrical system from operating or soft electrical shorting imparting an electrical leakage path that interferes with proper circuit functionality. Additionally, dendrites may short intermittently. In this case they carry enough current to heat and fuse. Once melted, it may return the circuit to normal proper operation. This can be a cyclical event with the dendrites growing, fusing, and regrowing, making diagnosis difficult. Finer-pitch surface-mount geometries and fine PCB conductor traces are particularly susceptible to this phenomenon if there are corrosives on the PCB surface. Sometimes, with repeated shorting and fusing, carbon tracks from arcing will occur resulting in permanent hard or soft short circuiting.

M. Abtew et al. published a chart of the electromagnetic force (EMF) of various metal couples present in some lead-free solder alloys.[3] As a rule, the lower the EMF, the more corrosion-resistant the alloy. Eutectic Sn-Pb, the basis of comparison, was by far the lowest value on the list at 0.010 V. The next nearest, Sn-51In, was 0.201 V or 20 times the voltage as that of Sn-Pb solder. Other values reported were Sn-57Bi at 0.323 V, Sn-9Zn at 0.624 volts, Sn-3.5Ag at 0.937 V, and Sn-80Au at 1.636 V. So tin-lead solder is significantly more resistant to corrosion and dendritic growth than the other seven alloys studied.

47.4 PB-FREE SOLDERS: ALTERNATIVES AND IMPLICATIONS

47.4.1 Elemental Alloy Candidates for Pb-Free Solder

Of the 90 naturally occurring elements, only 13 can be practically combined with each other to form a practical solder (Fig. 47.1).

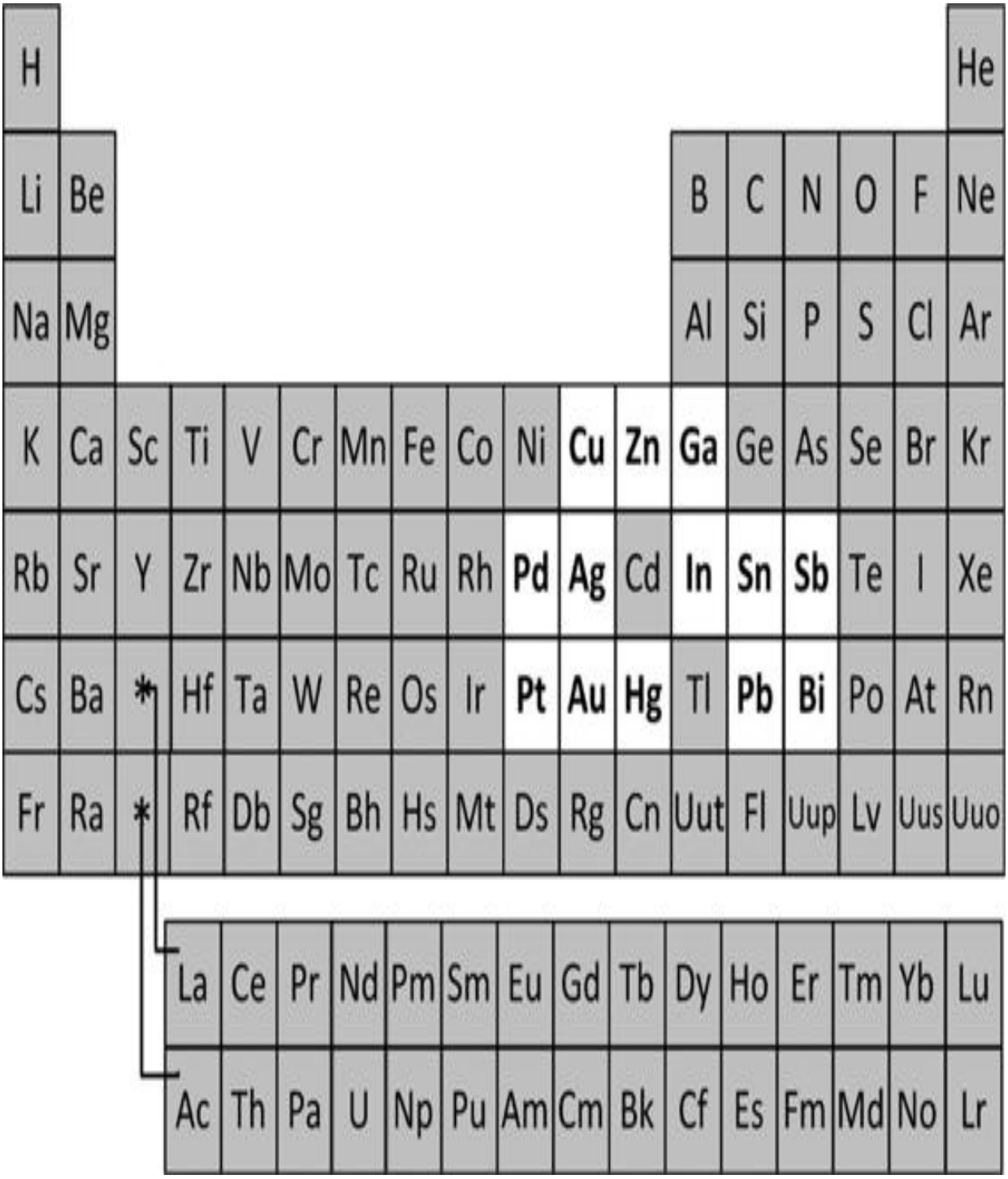

FIGURE 47.1 Highlighted elements can be combined to form solders useful for circuit board assembly. Grayed out elements are not useful for solder formulation for PCB assembly.

Of those elements that can combine to form solders, several have limitations that restrict their practical

implementation for solder use (Table 47.2).

TABLE 47.2 Elemental Candidates for Solders

Element	Symbol	Melting Point, °C	Comments
Antimony	Sb	630.5	Toxic. Currently in use as a minor constituent in some solders
Bismuth	Bi	217.5	In current use
Copper	Cu	1084.5	In current use
Gallium	Ga	29.75	Too expensive
Gold	Au	1063	Too expensive
Lead	Pb	327.5	Use restricted by EU RoHS Directive
Mercury	Hg	−38.83	Toxic. Use restricted by EU RoHS Directive
Palladium	Pd	1550	Too expensive
Platinum	Pt	1768.3	Too expensive
Silver	Ag	960.15	Expensive but in current use in some solders in small quantities
Tin	Sn	231.89	In current use
Zinc	Zn	419.6	In current use

Gallium (Ga), gold (Au), indium (In), platinum (Pt), and palladium (Pd) cannot be mined or refined in sufficient quantity to satisfy the needs of the electronics industry and are prohibitively expensive, blocking their consideration as a major constituent of a worldwide solder supply. The Bismuth

(Bi) supply, a by-product of lead (Pb) refining, would be marginally sufficient. Mercury (Hg) and antimony (Sb) are too toxic. Both Hg and Pb are already on the EU's RoHS list of restricted materials. Ga and Hg possess too low a melting point to be used on their own. This leaves five metals for practical solder alloy consideration: Bi, Cu, Ag, Sn, and Zn. Due to its value, silver, too, can only be used as a minor constituent of solder and is already in wide use that way today. Given the four remaining metals (Bi, Cu, Sn, and Zn), there are many possible metallurgical permutations available for solder alloying, but there are few that either possess low enough liquidus to be useful for circuit board assembly or have attractive physical properties as a solder. Although Pb-free solders have been in use for many years (jewelry making, plumbing, brazing, etc.), there is no one clear alloy choice for electronics assembly. Most have too high a melting point to be useful, and none come with the well-documented properties database as is the case for Sn-Pb solder.

47.4.2 Candidate Pb-Free Solders

Although many manufacturers completed the conversion to Pb-free soldering in time for the July 1, 2006, implementation of the RoHS directive in Europe, there was still no consensus across the industry for a single tin-lead solder replacement at the time. Pb-free alloy systems receiving the most attention include those listed in the Table 47.3.

TABLE 47.3 List of Lead-Free Solders and Their Temperature Ranges

Alloy Family	Most Common Compositions[a], Wt.%	Solidus Temperature[b], °C)	Liquidus Temperature[b], °C
Sn-Cu	Sn-0.7Cu	227	227[c]
Sn-Ag	Sn-3.5Ag	221	221[c]
	Sn-5.0Ag	221	240
Sn-Ag-Cu	Sn-3.0Ag-0.5Cu	217	221
	Sn-3.5Ag-0.9Cu	217[c]	217[c]
	Sn-3.5Ag-0.7Cu	217	220
	Sn-3.8Ag-0.7Cu	217	220
	Sn-3.9Ag-0.6Cu	217	223
	Sn-4.0Ag-0.5Cu	217	225
Sn-Ag-Bi	Sn-1.0Ag-57Bi	137	139
	Sn-3.4Ag-4.8Bi	200	216
	Sn-3.5Ag-5.0Bi	208	215
	Sn-3.5Ag-1.0Bi	219	220
	Sn-2.0Ag-7.5Bi	191	216
Sn-Ag-Bi-Cu	Sn-2.5Ag-1.0Bi-0.5Cu	214	221
	Sn-2.0Ag-3.0Bi-0.75Cu	207	218
Sn-Bi	Sn-58Bi	138[c]	138[c]
Sn-Zn-Bi	Sn-8.0Zn-3.0Bi	191	198
Sn-Zn	Sn-9.0Zn	199[c]	199[c]

Notes:

[a]There are too many noneutectic formulations composed of the same elements in varying ratios to list comprehensively here. Each variation in composition will have its own melting range. The ones listed in this table are examples only to show approximate temperature range and composition.

[b]Discrepancies in the literature exist as to the exact melting point or melting range of alloys listed, but the table will be useful for approximating phase-change characteristics of the alloys listed.

[c]Eutectic alloys have a distinct melting point; onset of solidus and liquidus is the same. Noneutectic alloy melting is characterized by a melting range, where the alloy is present as both solid phase and liquid phase(s), its pasty range. At the upper temperature of the melting range, only the liquid phase exists.

47.4.2.1 Characteristics of Pb-Free Solders. Pb-free solders generally exhibit poorer wetting and spreading characteristics than Sn-Pb alloys, but may offer an advantage in tensile strength and creep resistance. Each alloy will have its own properties in terms of the soldering process such as: propensity for solder void formation; oxide chemical resistance; solder paste shelf-life; fatigue characteristics; alloy interactions with board and component surface finishes; corrosion resistance; mechanical shock resistance and numerous other properties. Many of the lower melting point Pb-free solders have precious elements added to them, whereas some of the inexpensive alternatives wet poorly, are prone to oxidation during soldering, and tend to corrode. A few of the most favored alloy systems will be briefly discussed.

47.4.2.1.1 Bismuth Alloys. Bismuth (Bi), an element closely associated with Pb is, in fact, chiefly a by-product of Pb smelting. It is generally used for lower melting point solder alloys. Bi is in short supply and Bi solders cost about twice that of Sn-Pb alloys. Bi is compliant like Pb and shares several of its properties, such as high specific gravity and ductility.[4–6] Pure Bi melts at 271.3°C, about 50°C lower than that of Pb. Very easily oxidized, bismuth alloys are best soldered with the aid of highly activated fluxes or in a nitrogen environment.

Bi forms a binary eutectic with Sn in the proportions 58Bi:42Sn (m.p. 138°C). There are numerous bismuth alloys in use, many composed of two or more metals in addition to bismuth. The Sn-Bi eutectic, if contaminated with Pb, can be problematic as it is known to form a ternary alloy with a melting point of 96°C adversely affecting solder joint fatigue characteristics. In some applications, solder joints will fall apart if the service temperature is high and the low melting point Sn-Bi-Pb alloy is formed. This becomes all the more critical with smaller Sn-Bi solder joints. The Pb can come from solder predeposited on component leads,

noncollapsible Pb BGA balls, non-collapsible Pb CCGA columns or Sn-Pb hot-air solder leveled pads.

Bismuth expands upon freezing, whereas tin contracts. A phenomenon called fillet lifting has been reported[7,8] (Fig. 47.2). It is mostly associated with bismuth ternary alloys such as Sn-Cu-Bi and Sn-Ag-Bi used in plated through-hole (PTH) wave soldering, but has also been observed with the Sn-Bi binary. As the board cools, it contracts at a different rate than the solder, and the fillets may lift, especially if cooled slowly or contaminated with Pb. Rapid cooling (≥ ~3°C/s) has been advised but may not completely eliminate this phenomenon, but this cooling ramp may exceed manufacturer's specified thermal ramp rate for some components. Too high a cooling rate may result in component cracking or degraded component performance or reliability. Fillet lifting may also result in lifted or damaged PTH annular ring (bonding pad) if solder joint strength is high and bond strength of the ring to the board is also high.

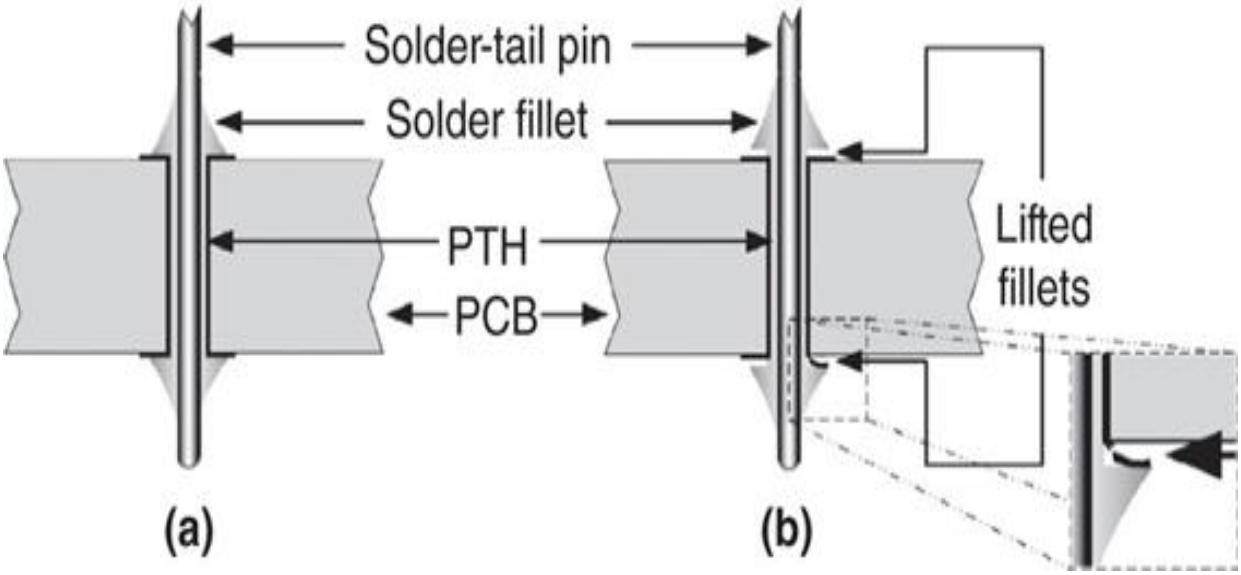

FIGURE 47.2 Bismuth alloy solder joints with fillet lifting: (*a*) normal wave soldered PTH joint, (*b*) expansion upon solidification in a bismuth-containing solder alloy may cause solder fillets to fracture and lift from the plated through-hole annular pads (see inset).

Some Bi alloys have too low a melting point for many applications. Despite its excellent tensile strength and thermal cycling endurance (better than Sn-Pb), Sn-Bi eutectic (m.p. 138°C) would not be practical for use in most automotive applications, where the service temperatures are exceptionally high. Bi also oxidizes rapidly, making Bi alloys difficult to maintain during wave soldering due to copious oxide (dross) production.

Bismuth soldering alloys are noted for their brittleness[9,10]; nonetheless, several bismuth solders are used commercially, the most popular alloys containing Bi in the 2 to 14 percent range. Aside from bismuth alloy's inappropriateness for high-temperature applications and potential for Pb contamination, hygiene is an issue. According to C. White and G. Evans,[11] safety is a concern when using alloys with high concentrations of bismuth as Cadmium (Cd), a poisonous metal, is a common bismuth contaminant. Care is recommended in handling this solder, and special venting requirements may also be mandated for its use. On the other hand, the RoHS legislation has reinforced prior EU restrictions on cadmium, limiting it as a constituent or contaminant to less than 100 ppm by weight.

Bismuth and indium alloys are suitable for *step soldering*, which refers to the use of two different solder alloys with two different melting temperatures used on the same circuit board. The higher temperature alloy (e.g., Sn-3%Ag-0.5%Cu, melting onset 217°C) is used to solder surface-mount components and an alloy of lower melting temperature (e.g., 58%Bi:42%Sn, m.p., 138°C) is used for wave-soldered components. The temperature experienced at wave solder will not cause the Sn-Ag-Cu to re-reflow, thus preserving the integrity of surface-mount technology (SMT) solder joints through wave soldering and avoiding re-reflow of same.

In the case of repair or replacement of top-side components, the use of low melting temperature solder will

have less adverse thermal effect on adjacent or bottom-side solder joints. In fact, use of low melting point solder reduces the possibility of pad delamination or through-hole barrel cracking; failure mechanisms associated with localized overheating, especially at repair. It should be noted that if there is a significant amount of the original solder on the bonding pad, it will alloy with the Bi-containing solder to create a new alloy of unknown properties.

47.4.2.1.2 Tin-Silver-Copper (Sn-Ag-Cu). As previously stated, the Sn-Ag-Cu (SAC) family is the most widely used Pb-free alloy for PCB assembly. Its tensile strength is superior to that of Sn-Pb, but its shear strength is worse. It is moderate in melting temperature; roughly 35°C higher than eutectic Sn-Pb solder. It is easily fluxed, but care must be taken to prevent premature flux activation or flux dry-out due to the elevated working temperature regime of SAC solders. Fluxing formulations for wave and reflow soldering have generally been formulated to accommodate the higher melting range of this alloy family by use of higher molecular weight resin fluxes and volatile organic compound (VOC)-free flux formulations. The eco-friendly VOC-free fluxes are devoid of alcohols or other low boiling organics which would enhance flux dry-out.

The SAC family has good compatibility with most Pb-free board surface finishes and Pb-free component platings. Its process window is narrower than that of Sn-Pb. It has been demonstrated that SAC can be used with parts containing Pb or vice versa, but the reliability of resulting solder joints is less than if soldering leaded to tin-lead or lead-free to lead-free. SAC solders sell at about two to three times the price of Sn-Pb solder alloys. A comparison of Sn-Pb solder to SAC solder is offered in Table 47.4.

TABLE 47.4 Comparison of Sn-Pb Solder with Pb-Free SAC Solder

	Solder Alloy	
	Tin/Lead Sn-37%Pb	Tin-Silver-Copper Sn-3.0 → 4.0% Ag-0.5 →0.7% Cu
Melting temp.	183°C	~215°C → ~223°C
SMT peak temp.	~215±10°C	~240±10°C
Wave solder temp.	245°C → 260°C	260°C → 270°C {with higher preheats and longer soldering dwells}
Solder reliability	Adequate	Still subject to investigation {Ag content related to mechanical shock resistance (increasing Ag decreases shock resistance)}
Process compatibility	Adequate	Adequate but still some development work underway

Figure 47.3 demonstrates the process temperature differences for SAC soldering as compared to Sn-Pb.

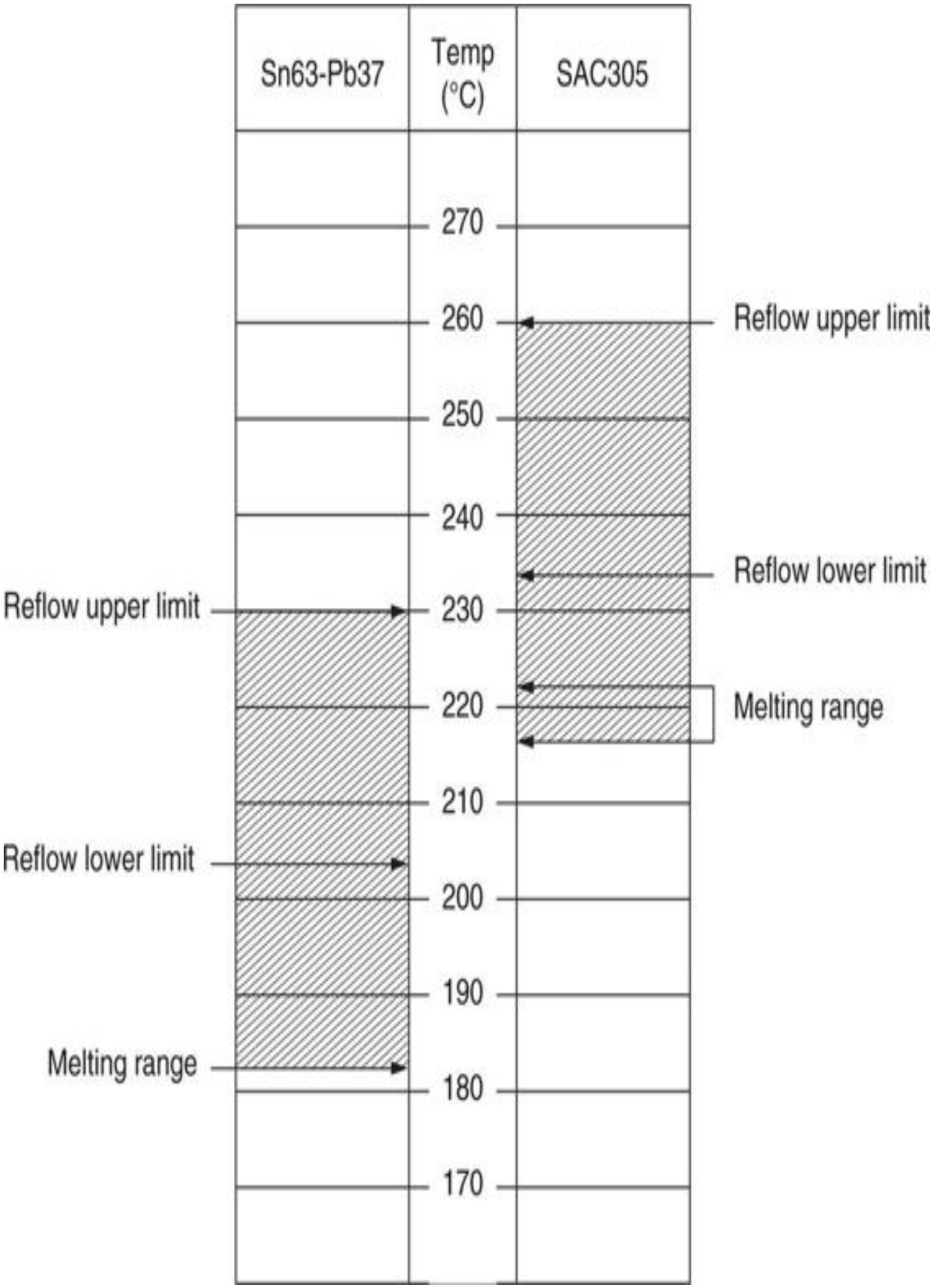
Sn63-Pb37
Temp (°C)
SAC305
270
260
250
240
230
220
210
200
190
180
170
Reflow upper limit
Reflow lower limit
Melting range
Reflow upper limit
Reflow lower limit
Melting range

FIGURE 47.3 Comparison of SAC solder to Sn-Pb solder in terms of upper and lower reflow process temperature ranges and onset of liquidus.

It should be noted that mechanical shock resistance of an assembly generally decreases with increasing silver content in the SAC formulation. SAC305 will be less shock resistant than SAC105 (1% Ag, 0.5%Cu).[12]

To improve the reliability of SAC solders, small amounts of impurity metals can be added. Zinc, cobalt, cerium, nickel and iron are but a few that have been investigated. Such formulations are called “SACX” solders. The intent of the additions is to impact the way the SAC solder constituents segregate or precipitate upon solder solidification, or to affect solder joint void content or grain size. There is no still no clear consensus as to which formulation is advantageous.[13]

47.4.2.1.3 Sn-0.7Cu Alloy. Eutectic Sn-Cu (m.p. 227°C) is being used as a wave solder charge material. It is compatible with most board surface finishes and component lead-frame finishes. Its relatively low cost (about 50 percent more than Sn-Pb solder) making it an attractive Pb-free alternative. It also has been demonstrated to be an effective alloy for Pb-free hot-air solder-leveled (HASL) surfaces on PCBs.

This alloy is in widespread use especially for wave soldering and to a lesser degree for oven reflow soldering of surface-mount PCBs. As mentioned previously, soldering is done at a temperature well above the onset of liquidus to add margin to the process, to ensure the whole board and components thereon are heated sufficiently for soldering and to provide conditions for good and efficient solder wetting. With a melting point of 227°C, this alloy must be boosted to about 265±10°C for wave soldering. Wave soldering is a dynamic process with the molten wave in constant motion and in contact with the bottom of the PCB during soldering. The action of the wave dissolves copper and other metals

from the PCB lands and component leads and because the soldering temperature is high and the copper content of this binary alloy is only 0.7 percent copper by weight therefore, only small changes in the copper content will upset the balance and change it from a eutectic composition with a distinct melting point, to a noneutectic, higher melting range alloy. The rise in melting point can be dramatic and if not identified and corrected will prevent proper soldering to occur. The eutectic composition of an alloy system has the lowest possible melting point for that system and noneutectic alloys have melting ranges rather than one distinct melting point. The high melting temperature of this alloy and the fact that it is 99.3 percent tin enhances rapid material dissolution from PCB surfaces and component lead platings. Care must be taken to top off the wave solder pot with an appropriate amount of Sn or Sn-Cu to maintain proper Sn-Cu alloy proportions. Sn-0.7Cu is also doped with small amounts of nickel, bismuth or other elements to affect its resulting grain structure and solder joint characteristics as for SACX.

47.4.2.1.4 Indium Alloys. This metal and its effect on the solder joint is very much the same as for bismuth. Indium (In) is very soft and ductile in its elemental form and melts at about 157°C. Indium-based soldering alloys are much more expensive—about 25 times that of Sn-Pb—due to indium's scarcity, thus it is not suited as a dominant alloy metal in solder. Price and supply make it unattractive even as a trace agent or a minor solder alloy constituent. B. Allenby et al.[14] concluded that the world's indium supply would be depleted in about 1 year if indium were consumed at the same rate as was Pb for Sn-Pb solders.

An In-Sn eutectic occurs at 58 weight-percent In with a eutectic temperature of 120°C. Copper is highly soluble in indium and it forms intermetallic compounds with copper from the circuit board's bonding pad or copper-based component leads. Indium has been demonstrated to be of

value in reducing the leaching of gold into solder as reported by Yost,[15] with a lower gold dissolution rate for indium-based solders as compared to tin solders. The use of indium allows soldering to gold films without thoroughly consuming the gold. The resulting solder joints are not brittle, as is the case of Sn-based solder joints exposed to too much gold.

Indium and some of its alloys can wet to glass, quartz, and other normally unsolderable inorganic substrates with the aid of an ultrasonic soldering tool. Ultrasonic soldering is discussed in the chapter on soldering techniques.

47.4.2.1.5 Zinc Solders. Zinc (Zn) alloys, once favored by some Japanese companies, oxidize rapidly. Solder paste shelf-life has been an issue even when these alloy pastes are refrigerated at very low temperatures. Dross formation in wave soldering has also been problematic. Zn alloys are prone to corrosion. The Cu-Sn-Zn alloy system can form ternary phases which may cause the solder spall.[16] None of the Zn alloys are in widespread use for PCB soldering.

47.5 BOARD SURFACE FINISHES

Most circuit boards consist of a stack-up of insulator material such as glass-reinforced epoxy and conductive layers (traces and planes) composed of copper. Copper oxidizes quickly and its oxides are chemically resistant necessitating the use of harsh fluxes to enable soldering. Copper also corrodes in the long term from left-over process residues, fingerprints (body salts), or airborne contaminants. It is for these reasons that copper traces on circuit boards are protected by solder mask and solder lands (bonding pads) are plating, or otherwise treated to enhance soldering. The following section covers the most common board finishes. The process engineer needs to bear in mind that in addition to

solderability, other surface finish-related issues that may affect manufacturing including the following:

- *Probe ability:* The ease with which conventional in-circuit test probes are able to make contact with a particular surface finish.
- *Cost:* Some surface finishes are significantly more expensive than others.
- *Shelf life:* Bears on the ability of a surface finish to resist oxidation, tarnish or other surface conversion or corrosion, and remain solderable.
- *Reliability:* Refers to the influence surface finish may have on resultant solder joint strength as it relates to long-term use, thermal cycling, resistance to mechanical shock or vibration, and other environmental factors.
- *Corrosion resistance:* Some surface finishes are more prone to corrosion than others. Immersion silver, tin and copper are three such finishes that are frequently associated with corrosion.
- *Tribology:* The frictional properties of a material become important for press-fit connections.
- *Other surface finish-related defects:* Immersion silver (Imm-Ag) surface finish has been known to exhibit linear arrays of microvoids at the intermetallic interface which detracts from solder joint strength. Electroless nickel/immersion gold (ENIG) sometimes results in brittle fracture if the plating chemistries are not maintained properly.

47.5.1 Hot-Air Solder-Leveled Surfaces

Hot-air solder-leveled (HASL) coated boards are manufactured by dipping, wave soldering or otherwise

coating a raw PCB with molten solder and using a stream of hot gas to blow off excess solder, thus leveling the solder which has wetted to PCB bonding pads. It was a common board finish for Sn-Pb.

There is the old industry adage that “nothing solders like solder,” which has made HASL a safe and preferred finish for many years. There are never solderability issues with this coating. If the coating is present then it is solderable. It is inexpensive, easy to apply, and has excellent shelf-life/aging properties. There have been fears about the flatness of the HASL finished pads and potential effect on surface-mount component placement and soldering. Pads need not be perfectly flat for component placement. Since 0.1 to 0.2 mm of solder paste are applied over the pads for reflow soldering, the notion of original PCB bond pad flatness is not a significant concern unless the HASL finish is grossly out of specification and escaped board shop final quality control. During reflow, the solder paste and HASL solder on the pad starts to reflow, it domes up as a liquid and will self-level. Once it wets to component lead, surface tension of solder to wetted pad and wetted lead will hold things to together until solidification. It is a well-proven surface finish for component lead pitches down to at least 0.5 mm. Reputable board shops no longer consider HASL difficult to apply and some board shops are finding new use for their expensive HASL application equipment by extending it to Pb-free solders. Sn-Cu has been demonstrated to be one such HASL coating material.

Since HASL constitutes a soldering reflow cycle there an intermetallic compound (IMC) layer present prior to PCB assembly and the thicker the IMC the less reliable the solder joint. But HASL was used for many years for Pb-bearing solders with complete success and the same should be true for Pb-free solders even though the soldering temperature is slightly higher. Since HASL usually has thin, probe-friendly oxides, it is a favored surface finish for in-circuit testing.

47.5.2 Organic Solder-Preservative Copper

Known as OSP-Cu,[17,18] organic solder-preservative copper is an organic coating applied to the copper lands on the PCB at the board shop to retard oxidation. The lands are first given a microetch to remove oxides and to increase surface area for OSP coating adhesion. The protective coating is an organometallic compound such as benzotriazole or imidazole, that chemically bonds with the freshly etched copper pads and plated through-holes of the PCB. It is formulated to retain copper solderability through multiple reflow cycles. OSP-Cu is widely used and best for “just-in-time” board assembly strategies since its effectiveness diminishes with time, temperature and humidity.

During the soldering process, the OSP coating degrades with each reflow cycle resulting in increasing levels of copper oxidation. Chemical-resistant copper oxide inhibits solder wetting, requiring ever stronger solder fluxes. This may be particularly evident with thick [≥2.36 mm (≥0.093 in)], thermally aggressive PCBs with mixed-mount technology since PCB heating regimes are necessarily high. Reflow results on the secondary side and primary side of such boards are generally satisfactory. But by the time such a board reaches the solder wave, the OSP coating may have lost enough of its effectiveness that remaining copper oxidizes and compromising PTH barrel fill. Today’s OSPs are formulated for the high temperature rigors of Pb-free soldering, and if PCBs are properly coated, stored in a cool dry environment as recommended by the PCB supplier and not abused during reflow and wave soldering, then the OSP coating should be effective for the two reflow soldering cycles and one wave soldering operation as is required for mixed-mount assembly.

When solder paste printing goes awry and the PCB needs to be cleaned of the misprinted or smeared solder paste, most organic solvents used for removing the paste may thin, or remove the OSP coating reducing its effectiveness in preventing copper oxidation. Care must be taken to ensure paste misprint solvent compatibility with the OSP coating.

Another deficiency of OSP-Cu is found at in-circuit test (ICT). As the board is passed through top- and bottom-side reflow cycles and wave soldering, the unsoldered and un-fluxed test points oxidize. The insulating oxide layer is difficult to pierce even with sharp, pin-type or blade-type ICT probes. Multiple fixture re-seatings may be necessary to attain probe penetration and electrical contact. This reduces the probe working life as probe sharpness is dependent on the number of contact activations. It is good practice to coat test points with solder; however, some no-clean flux residues are difficult for ICT probe contact. The best strategy goes against modern PCA practices: reverting to the use of water-clean paste and flux formulations and coating test points with solder. The postsoldering, aqueous cleaning cycle removes any flux residues, enhancing ICT probe contact on solder-coated test points on the finished PCA. But most large electronic manufacturers have worked diligently to remove aqueous cleaning from their factories—a move for improved process economics and significant environmental impact.

47.5.3 Electrolytic Nickel/Electrolytic Gold

This plating combination has been in use for many years and is considered a high-end surface finish but a highly reliable one in terms of solderability and product life. The amount of gold (Au) is small, but the plating process uses toxic and expensive materials that further increase the price of the plating. This plating system should not be confused with

electroless nickel/immersion gold (ENIG). That surface finish will be discussed separately and does not have the reliable history of electrolytic nickel/electrolytic gold.

The electroplated nickel (Ni) serves as a barrier between the copper and the gold. Ni on its own is a poor candidate for a solder pad coating as it oxidizes rapidly and its native oxide is very durable and stable; chemically tough to dissolve or react away. Un-oxidized Ni can alloy with tin, which means that it can be soldered. Were the gold deposited over the copper directly, the gold layer would begin to inter-diffuse with the copper even at room temperature forming a brittle intermetallic compound. The reaction rate is temperature-dependent. This intermetallic, like most intermetallic compounds, is difficult to solder, requiring a higher process temperature, a more active fluxing agent, or both. The Au-Cu system has poor solderability and the brittleness of this intermetallic results in diminished solder joint strength.

Ni/Au coatings are in widespread use. Ni coating thickness is generally on the order of ≥2.54 µm (≥100 µin). Au is a more difficult metal to plate. It tends to coalesce into islets, resulting in a porous coating. Any pores in the gold overcoat allow oxidation of the underlying Ni, rendering it locally unsolderable. To preclude this, the gold is liberally plated with a targeted minimum thickness greater than about 0.127 µm (5 µin) to ensure complete coverage of the Ni.

There are problems with the Ni/Au metallurgical system. First and foremost, it is well known that gold can cause solder joint embrittlement. When gold is alloyed with tin as in tin-lead solder, it forms alloys with both the Pb and Sn. The Au-Pb alloy has two predominant intermetallic compounds: Au_2Pb and $AuPb_2$. Of the two, the latter is of greatest concern. It begins to form at the Au-Pb eutectic (85 weight-percent Pb, m.p., 215°C), a temperature that encroaches into the normal reflow solder processing regime.

$AuPb_2$ is stable below 254°C and is characterized by brittle, plate-like structures. Regardless of the composition, size, and concentration of the intermetallic grains in the solder joint, they can either strengthen it (forming miniature reinforcing bars in a solder "cement") or embrittle it, detracting from the solder's inherent ductility.

Gold is nonoxidizing, like platinum and palladium, its noble metal neighbors in the periodic table. It readily alloys with most common solder alloy compositions, especially Sn-Pb and Sn-Ag-Cu. A. Korbelak and R. Duva[19] consider gold the most readily solderable material, but Sn-Au intermetallics are of even more serious concern than those of Au-Pb. The former is a characteristically brittle intermetallic that has been widely linked to solder joint failure. Too much gold in a tin-lead solder imparts a dull, grainy look to the resultant joint; the only possible visual clue, although there are other conditions that can lead to a similar appearance. It should be noted that most Pb-free solder joints have a grainy look even if inherently pure. There are marked differences in solder joint integrity when it is loaded with Au. The embrittlement causes a reduction in the joint strength and fatigue life. There is universal agreement that Au can be detrimental to the final assembly if its fractional weight-percent is not strictly controlled. There is wide disagreement on the exact amount of gold permissible. Reported values generally fall between 2 weight-percent and 10 weight-percent, with most experts agreeing that less than 2 weight-percent is a safe value.[20,21] Ebneter[22] determined that Au as a thin, protective coating 0.762 to 5.84 µm (30 to 230 µin) does not pose an embrittlement problem and that Au thickness required was a function of the plated grain size and porosity. Further, grain size is dependent on the type of plating bath (cyanide or acid) used. Hedrig[23] also concluded that >5 percent Au in Sn-40Pb solder was problematic. Foster[24] reported a small net increase in solder joint strength with a 2.5 percent Au

addition to the same alloy, but when the addition was as high as 10 percent, there was a marked degradation in solder joint strength. C. J. Thwaites[25] reported that 4 percent gold in a Sn-Pb solder joint is the threshold value above which there is a marked embrittlement and reduction in fatigue resistance.

There are three important Au-Sn intermetallics: AuSn, $AuSn_2$, and $AuSn_4$. Eutectic points are at about 85 weight-percent Sn (215°C) and 20 percent Sn (280°C). Gold can also form a ternary compound when joined with Sn-Pb solder, exhibiting a eutectic at about 175°C.[26] This can radically alter reflow characteristics and solder joint performance. Au, like Pb, is poorly soluble in Sn, which means that it dissolves in hot Sn, Pb, or Sn-Pb solder and precipitates out of solution during the liquid-to-solid phase. When it does, it forms brittle, plate-like crystals that are readily apparent, needle-like in cross-section.[27]

When an intermetallic forms a distinct interfacial layer or is in otherwise high localized concentration, it is a rigid structural element, prone to crack formation along its solder interface upon flexure. Therefore, in the case of Sn-Pb, even though the solder joint is composed of a ductile composition, its overall strength and endurance is dominated by the brittle intermetallic composition and its thickness and structure within the solder joint.

As component lead pitch decreases, so does the requisite solder volume. Au concentration becomes increasingly difficult to control because its plated thickness cannot be easily regulated to accommodate the reduced surface area and lower solder volumes that accompany finer-pitch component requirements. After all, Au deposit thickness is dependent on its deposition grain size and plated porosity.

Another pitfall of Cu-Au or Cu-Au-Sn systems is that of Kirkendall voiding. Voids in the solder joint or at copper-gold interfaces occur with time through solid-state diffusion.

Copper, which has a relatively high solubility and solid-state mobility in gold, diffuses into the gold. Transported by grain boundary diffusion at temperatures below 150°C and by bulk diffusion above that temperature, Au-Sn regions result along with atomic vacancies. When lattice vacancies are in profusion, microscopic voids can be observed, and this material depletion weakens the solder joint. Several references are available on this phenomenon.[28–31] Kirkendall voids should in no way be confused with voiding that results from entrapped gases or residues from solder paste in the surface-mount process or from fluxes or PCB laminate materials in wave soldering.

Although there is still much controversy on the subject of Au concentrations and effects on the solder joint, there is no doubt that this metal system is being widely exploited successfully in electronics manufacturing. It is, however, prudent to ensure that the Au levels are kept to a minimum via adequate vendor management and implementation of good process control methods for solder deposition. Note that because gold is a non-oxidizing material and therefore does not deplete the flux, more flux is available to work on the other components of the metallurgical system—namely, the underlying nickel (which must be kept from oxidizing), the solder, and the component lead. The Ni-Sn intermetallic is more brittle than that of Cu-Sn, and this surface finish is generally not recommended for applications where the product may experience high mechanical stresses such as shock or vibration.

It has been stated that in the Ni/Au system, the soldering actually occurs on the Ni surface and the Au serves as a protective coating. Another intermetallic of this system, $NiSn_3$, has been cited as a problem in long-term solderability degradation.[32] This IMC rapidly develops a platelet structure at low temperatures, with the greatest growth rate in the vicinity of 100 to 140°C. When intermetallic platelets grow

large enough, they may penetrate the surface of the overlying tin, oxidize, and become a material difficult to flux and solder. The presence of elemental Pb was determined to retard $NiSn_3$ IMC formation. Ni/Au surface finish is in use with Pb-free soldering, but there is currently a watch in the industry as sporadic brittle fracture has been observed on occasion. The exact nature of this fracture mechanism is yet to be understood and it is not certain that Ni/Au surface finish is at fault or just coincidental with some other failure mechanism.

47.5.4 Electroless Nickel/Immersion Gold

As the name implies, Electroless Nickel/Immersion Gold (ENIG) is not an electroplated surface finish. Still comprised of Ni over the PCB's copper, it has an overcoat of Au. ENIG is a lower-cost alternative than electrolytic Ni/Au and is in widespread use today. When the plating process is kept in control, it provides an excellent, solderable, and reliable surface finish. On the other hand, it is a finish that has caused many well-known reliability problems. Terms such as "black-pad," "black line nickel," and "mud cracks" describe some of the evidence of failed ENIG-related problems. These phenomena have been commonly observed on BGA packages plated with ENIG for package-to-ball attachment[33] and also at board level with solder joints built upon ENIG surface finish.

The main defect is brittle failure of the solder joint; a clean break beneath the intermetallic layer formed on the PCB bonding pad. Were the package completely pried loose from the board, a high surface area, dull finish bonding pad would be evident; the well-known "black-pad." Often the pad has an array of cracks visible on its surface reminiscent of mud

cracks. Once the failed component is removed, the black-pad afflicted bonding pads are unsolderable or unreliable for further use and the board must be scrapped. Although the exact cause of ENIG failure is not well understood, it seems to be linked to phosphorus concentration in the electroless nickel plating bath.

ENIG's appeal is its modest cost, flat topography consistent with all plated surface finishes**,** excellent solderability, excellent testability, and reasonable shelf-life if plated well. Unfortunately, the risk associated with this surface finish must be weighed alongside its benefits. In general, the assembler will find good results with ENIG. Unfortunately, there are no quick screening methods to weed out failure-prone ENIG plating lots.

47.5.5 Electroless Nickel/Electroless Palladium/Immersion Gold

A relatively new surface finish, it is immersion gold (Au) over electroless palladium (Pd) over electroless nickel (Ni) plated on the PCB's exposed copper (Cu) lands and traces. Pd serves as a diffusion barrier preventing Ni from intermingling with the Au in order to eliminate Au/Ni embrittlement. In many ways it is has qualities like ENIG but less chance of the "black pad" defect seen with ENIG. It is more costly than ENIG and highly dependent on the market price for palladium; a very expensive metal.[34] It has been shown that the interfacial strength of electroless nickel/electroless palladium/immersion gold (ENEPIG) is more robust than that of ENIG.[35]

It is also useful for press-fit as the Pd and Au offer some lubricity to the system which results in a slightly lower force needed during the press-fit process.

47.5.6 Immersion Silver (Imm-Ag)

This electroless silver-plated surface finish is in common use for Sn-Pb assembly and is also compatible with the most common Pb-free solders. Although it is has excellent solderability and good electrical test probe-ability, it has some negative attributes. Its solderable shelf-life is reasonable if stored properly (air-tight bags), but it readily combines with sulfur contaminants in the atmosphere and tarnishes (sulfidizes). Silver sulfide is somewhat resistant to weak organic fluxes as used for no-clean soldering. This makes it a poor choice for manufacturing locations where air pollution is prevalent and heat and humidity are not controlled within acceptable standards of practice.

A failure mechanism called “Planar micro-voids” or “champagne voids” associated with this surface finish has been reported.[36–38] These are small voids aligned atop the intermetallic layer of a solder joint bond line that impart diminished bond strength and resultant solder joint fracture (Fig. 47.4).

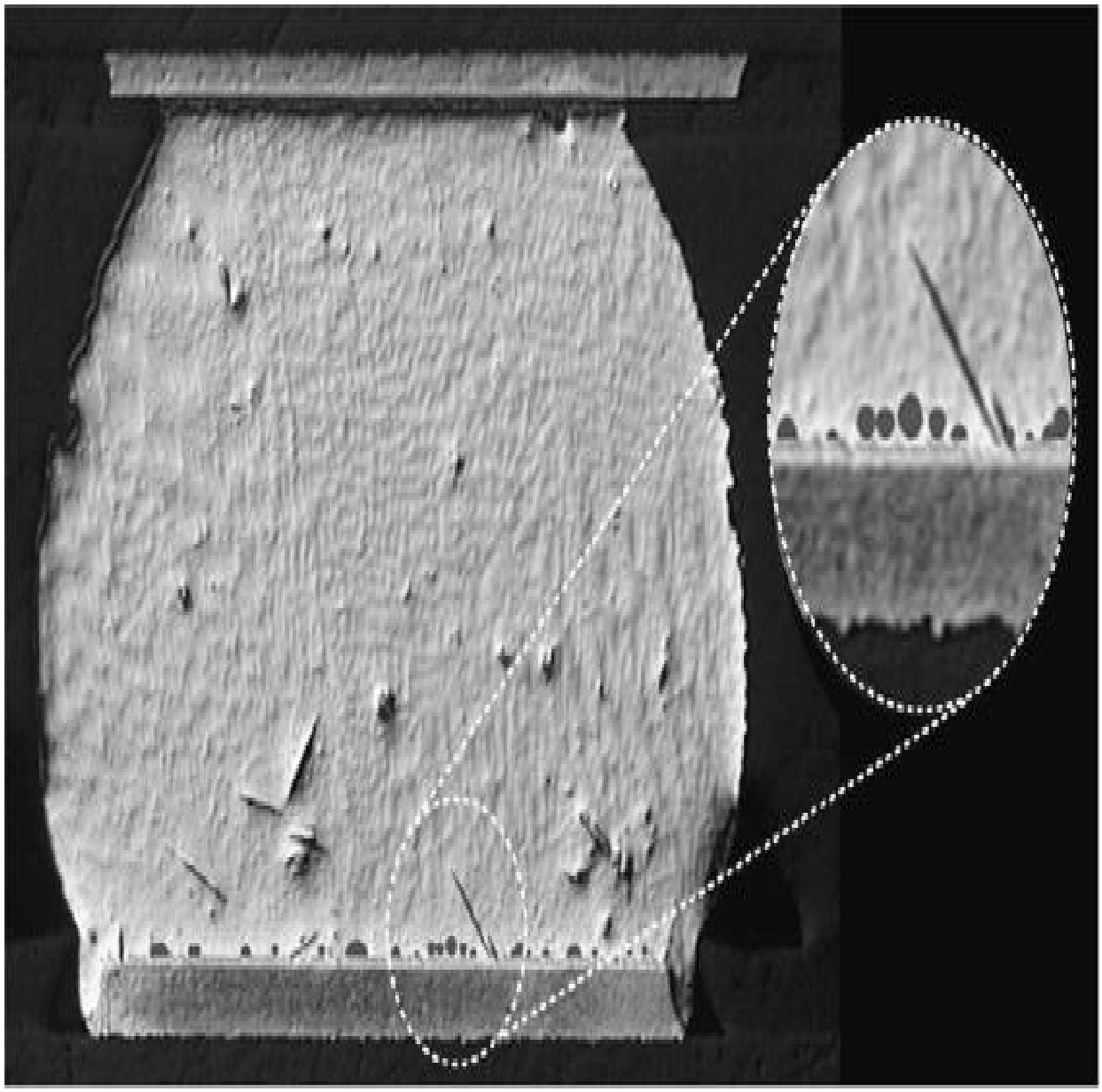

FIGURE 47.4 Cross-sectional micrograph of SAC BGA solder ball bonded to a silver surface finished PCB bond pad. Planar voids are clearly evident in the section and in the magnified inset. Voids in close adjacency above the intermetallic layer and the BGA ball can significantly detract from the solder joint strength. Note the Ag_3Sn platelets evident in the cross-section. These can occur from the immersion Ag or from Sn-Ag-Cu itself. They too can contribute to weakened solder joints. (*Courtesy of Hewlett-Packard*.)

This defect has been responsible for some noted product failures and recalls. The root cause of the microvoids is

generally believed to be the result of volatile organics incorporated during Ag plating at the board shop.

Silver ions are known for their mobility especially in the presence of an electrical field. Ionic residues on a board with silver-coated surface finish together with adsorbed moisture from the atmosphere can result in electrochemical migration and corrosion dendrites originating from any exposed, unalloyed silver plating (Fig. 47.5).

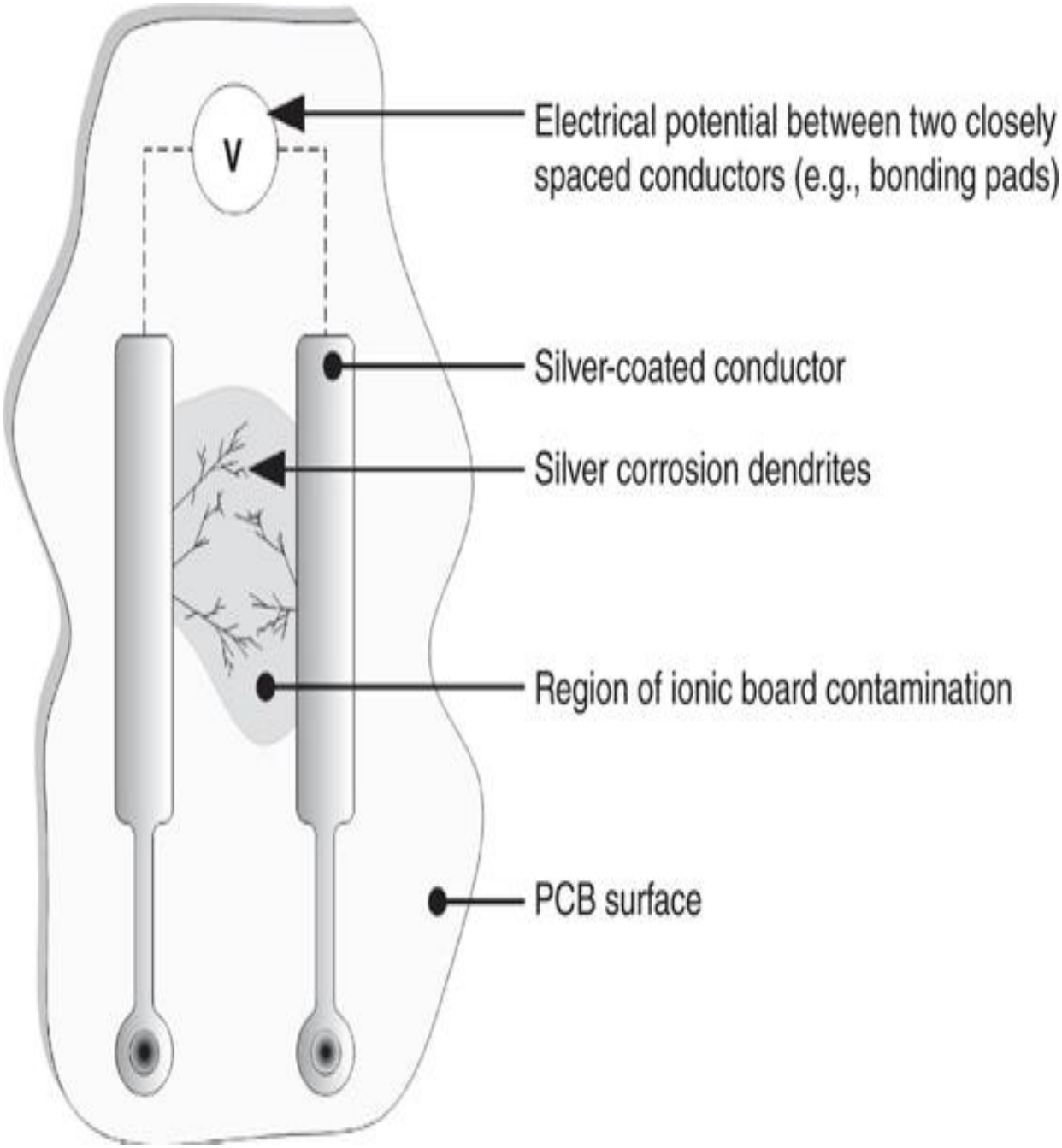

FIGURE 47.5 Ionic contamination on a board surface can adsorb moisture from the atmosphere. If an electrical charge is present, silver from bond pads may corrode and electrochemically migrate, resulting in a short circuit between bond pads.

Such dendrites not only occur on the board surface but can also develop under solder mask. If the dendrites are long enough, they cause electrical shorting to one another or to

adjacent traces. Since corrosion dendrites are exceptionally small in cross-section, they are poor electrical conductors and if enough current is passed, dendrites heat and fuse. Once melted back, the once-shorted circuit will become open again. If moisture and contaminant conditions are favorable, corrosion dendrites may re-form again once again resulting in an electrical short. This cyclical growth-and-fuse phenomenon can complicate locating and diagnosing the source of the shorting. Additionally, the shorting may cause surface carbonization around the dendrite; the carbon tracks acting as another source of electrical shorting.

Silver is an expensive metal. With its increased demand for solders (e.g., Sn-Ag-Cu), it is expected to rise in price, making it economically less attractive.

47.5.7 Tin (Sn)

Tin deposited directly over copper, whether by electrolytic or electroless methods, should be avoided except for low-end/low-cost, short-field-life products. Sn alloys with copper, even at room temperature, forming a brittle intermetallic compound, albeit slowly. It has limited solderable shelf-life at room temperature and the Sn-Cu intermetallic inhibits soldering and may result in incomplete solder wetting or solder joints of inferior strength. For tin to be used effectively, an appropriate nonporous barrier metal, such as Ni, should be deposited between oxide-free Cu and Sn. Immersion Sn can be plated only as a very thin layer since its deposition is by a self-limiting replacement reaction. When there is no more exposed Cu on the surface of the PCB during the surface-plating operation, Sn deposition ceases. Therefore, it is impossible to plate enough Sn by this method to extend the solderable shelf-life of the bond pad. When fresh, tin has good solderability, but tends to oxidize quickly.

There are two important phenomena that are associated with Sn platings: tin whiskers and tin pest.

47.4.7.1 Sn Whiskers. Not to be confused with corrosion dendrites, whiskers are crystallites (Fig. 47.6) that grow from pure tin surfaces into free space whereas corrosion dendrites grow on ionic contaminated, hydrated surfaces between two charged conductors. Corrosion dendrites are metals which plate out of areas of salt contamination whereas whiskers are born out of solid-state crystal mechanics. Although whiskers have been studied since the 1940s, their root cause is yet to be fully understood.

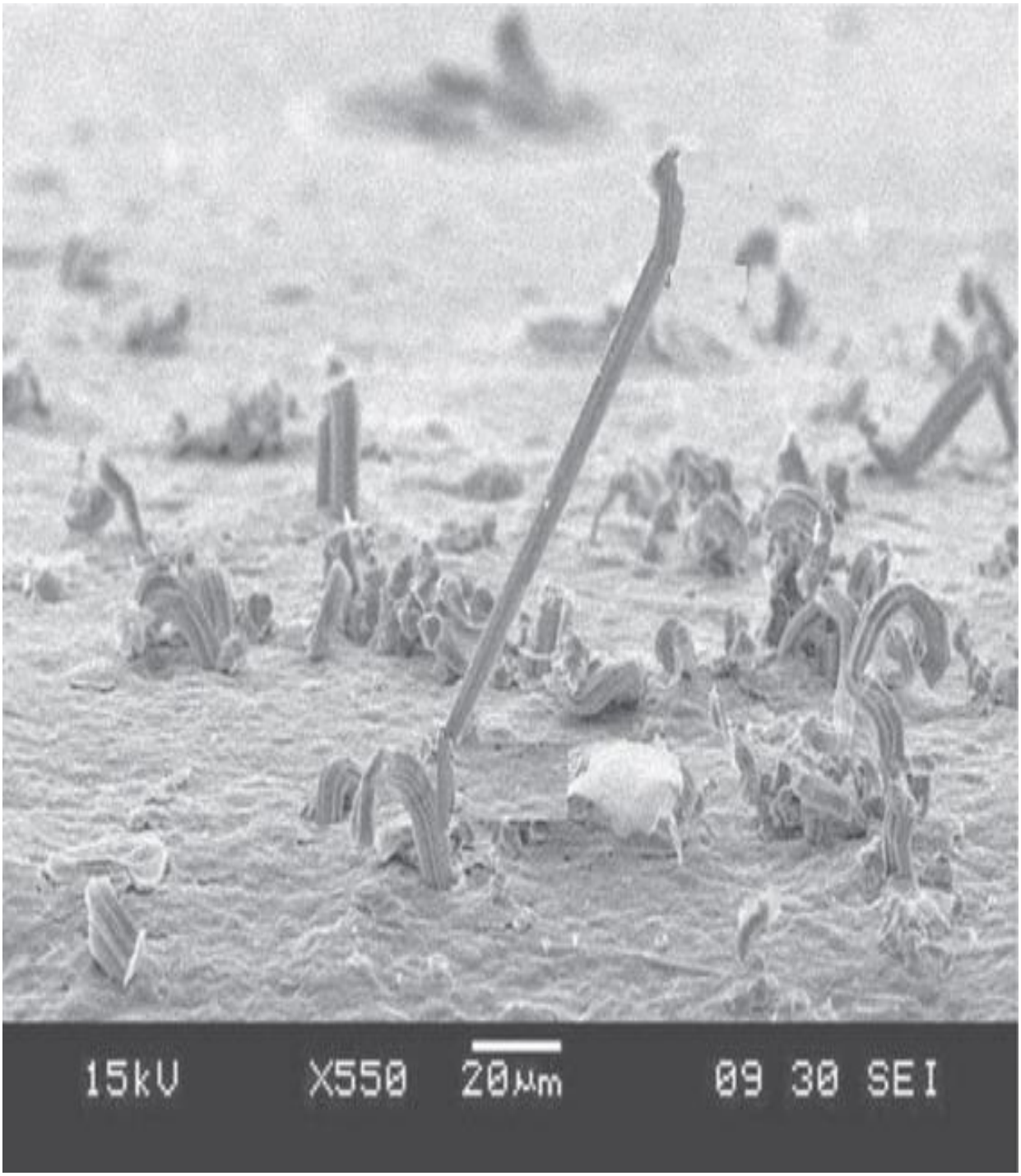

FIGURE 47.6 Scanning electron microscope (SEM) micrograph of Sn whiskers growing from a pure Sn surface. When whiskers break, they pose danger of shorting between fine-pitch conductors. Whiskers can also grow long enough to bridge to a nearby conductor. (*Courtesy of H. Hsu, Mitac Corporation, ShunDe, China*.)

The concern over whisker growth is twofold, both related to electrical short circuits. If a tin whisker is long enough, it may break due to mechanical shock, vibration or other perturbation. The broken whisker may bridge two closely spaced contacts or traces on a component or PCB. Whiskers need not break to cause a short circuit, as they can grow long enough to bridge two adjacent, closely spaced conductors. In 1998, the in-orbit Galaxy IV communications satellite failure was traced to tin whiskers.[39] Spare boards for that satellite stored on Earth clearly showed whisker growth in sufficient length and quantity to have caused the problem. It is ironic that the first known electrical-related whisker issue occurred in 1946 on Bell telephone equipment, which caused another telecommunications disruption.

Although tin whiskers have been studied since at least the 1940s, there is no definitive known mechanism for their formation, although theories abound. There are lattice dislocation theories and grain boundary diffusion theories. But the most prevalent theory for whisker generation relates their origin to compressive stresses within the tin lattice and perhaps weak spots in the overlying natural oxide on the tin surface. Where tin and copper are in contact with one another, copper is found to diffuse into tin faster than tin into copper. This causes a disruption of the tin lattice and resultant compressive strains. When tin grains are compressed against each other, and particularly when there are large compressive forces against a small, near-surface grain, the small grain may start to recrystallize or extrude in the least stressful direction, outward through a weak spot in the native oxide layer (Fig. 47.7). Growth continues until the lattice energy reaches equilibrium. Tin whiskers can grow to a diameter of approximately 1 μm and their length can reach tens of micrometers.

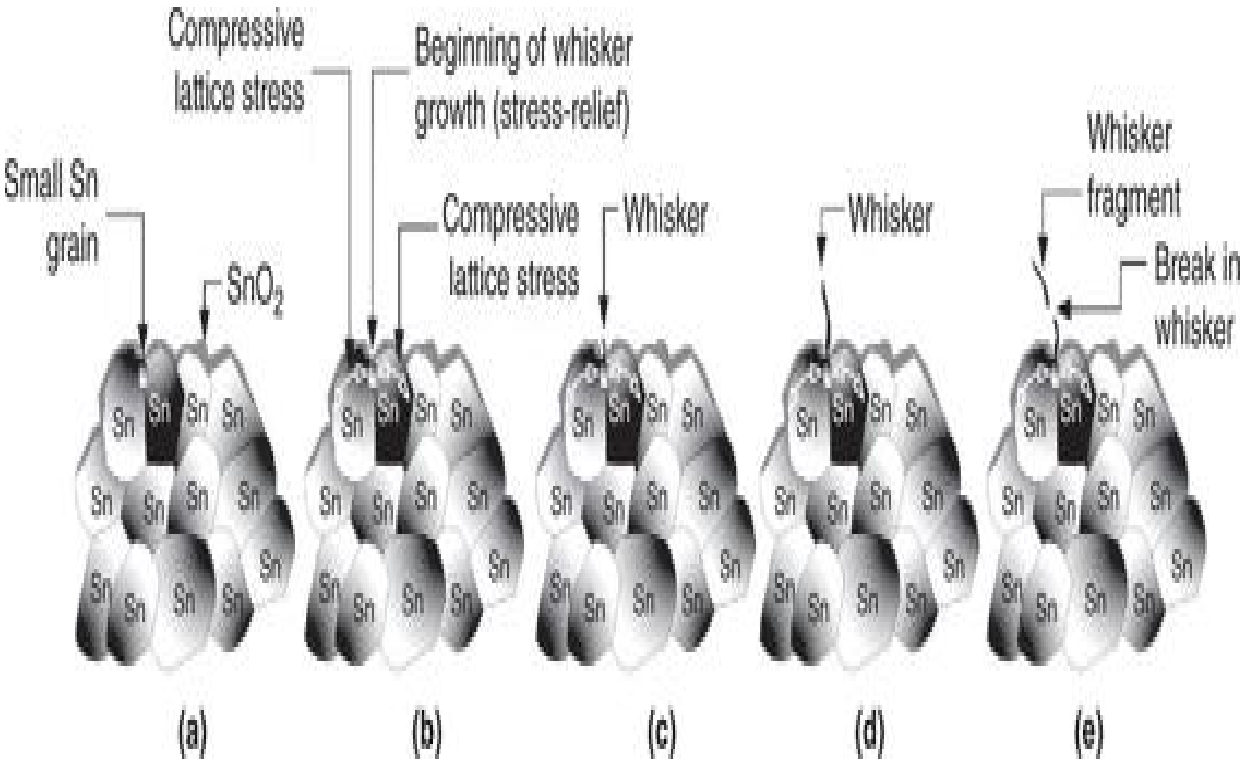

FIGURE 47.7 Compressive stress within the tin lattice may cause whisker formation. The picture sequence depicts a likely mechanism for tin whisker growth and risk to printed circuit assembly: (*a*) tin lattice with small, near-surface grain between two large grains; (*b*) compressive stresses cause recrystallization of grain and stress relief by extrusion; a thin spot in the oxide layer allows the rudimentary whisker to penetrate the surface, (*c*) continued whisker growth/stress-relief; (*d*) continued growth; if long enough it may pose a shorting hazard; (*e*) whisker breaks due to mechanical shock, vibration or handling. Whisker fragment poses a shorting risk to circuitry.

When Pb is even a minor constituent in Sn alloy the likelihood of whiskers diminishes. The resulting lead-doped tin lattice imparted some compliance, reducing Sn grain compressive forces to the structure and reduced the risk of tin whisker formation. The same has been noted for Bi or Sb. Now that Europe's RoHS legislation restricts Pb to a level of less than or equal to 1000 parts per million by weight in electrical and electronic assemblies, the addition of Pb is no longer considered an option for whisker prevention or reduction. The increased use of Sn-coated component terminals and Sn as a PCB surface finish has renewed the interest in Sn whiskers. Additionally there has been an

upsurge in the number of observed whiskers now that Pb has been removed from the assembly equation.

Matte Sn plating over a thick, nonporous nickel barrier layer over the copper reduces, but may not eliminate Sn whiskers. The relatively thick nickel deposit is generally under tension and the tin diffuses into the nickel faster than nickel into the tin. Since the nickel exerts no compressive influence on the tin lattice, tin whiskers are less likely to form. Besides metallic dopants, there are other ways to mitigate the growth of tin whiskers. Brighteners in tin-plating baths should be avoided. Annealing tin coatings is known to reduce whisker growth as recrystallization minimizes lattice stress. Ensuring that the reflow temperature during PCA soldering is above the melting point of tin (232°C) reduces whisker risk also.

47.5.7.2 Tin Pest (Tin Disease). In addition to risk from whiskers, tin also poses another, though rare, problem in some applications involving low temperatures. At about 13°C, tin undergoes a crystalline structure transformation. The ductile, tetragonal crystal of white (β) tin converts to the brittle, diamond-structured allotrope, gray (α) tin. Since gray tin has less density than white tin, there is an expansion of the tin lattice upon transformation and the tin starts to fall apart, turning to a gray dust.

Use of pure tin coatings should be avoided as a surface finish for low-temperature duty. The transformation is most profound at −40°C but will occur, albeit more slowly, at temperatures below the allotropic transition threshold. As in the case of tin whiskers, tin pest has been combated with the addition of a dopant metal such as bismuth, antimony, or lead. Lead addition, however, is no longer an option due to the RoHS directive and similar mandates.

It has been conjectured that on Napoleon’s army was victimized by tin pest.[40] Tin-soldered, brass uniform buttons may have fallen apart during the harsh winter of the Russian

campaign, hastening the defeat of an already beleaguered and hypothermic army. Tin pest has also been reported in the context of Pb-free soldering.[41]

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CHAPTER 48
SOLDER FLUXES

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

48.1 INTRODUCTION TO FLUXES

In a simplistic sense, the soldering process model is generally treated as solid and liquid metals interfacing with a gas (the soldering ambient). However, realities dictate a modified view. Nearly all metals oxidize when exposed to air and these oxides, whether on the solder itself or on the metals to be joined, always impede soldering. To keep the solder and surfaces to be joined bondable, metal oxides, tarnishes or other contaminants must be removed and bonding surfaces must be kept clean, tarnish-free and oxide-free until soldering is complete. To this end, a chemical fluxing agent has been used from ancient times to now and is essential to the process of joining. Fluxes are tailored to both the metals to be joined and soldering process temperature. Some metal oxides such as aluminum and nickel are notably thick and chemically unreactive, which make soldering difficult. Even copper oxides can be tough to

dissolve. Most fluxes used in printed circuit assembly are acid-based, formulated to be strong or weak depending on the metal systems to be joined, post-soldering treatments, and reliability needs.

Fluxes are typically composed of high molecular weight organic materials that are slow to dry, slow to evaporate, and slow to decompose as they approach soldering temperatures as well as acids. The acids are tailored to etch, dissolve, or disrupt oxides and tarnishes on solder and surfaces to be joined. Both the absence and presence of liquid flux have an effect on the extent of solder wetting. Some fluxes can transition from a runny liquid during preheat to a viscous liquid or gel and ultimately to a gummy solid as it dries out, polymerizes, and decomposes during the soldering cycle.

48.2 FLUX FUNCTIONS

Selection of the flux type depends on the soldering method, solder alloy, metal finishes on the board and on components, condition of the surfaces to be joined, requisite solder joint attributes, reliability requirements and the intended final use of the assembly. Some fluxes leave benign residues formulated to remain on the board. Flux residues may be difficult to clean, interfere with in-circuit test (ICT) probing or may hinder subsequent processes such as conformal coating or under-fill adhesive application. Postprocess flux deposits can cause corrosion, especially in the electric field between closely adjacent conductors on the surface of the PCB. Fluxes may impart gas bubbles, or voids, which may be “frozen” into the solidifying solder (Fig. 48.1).

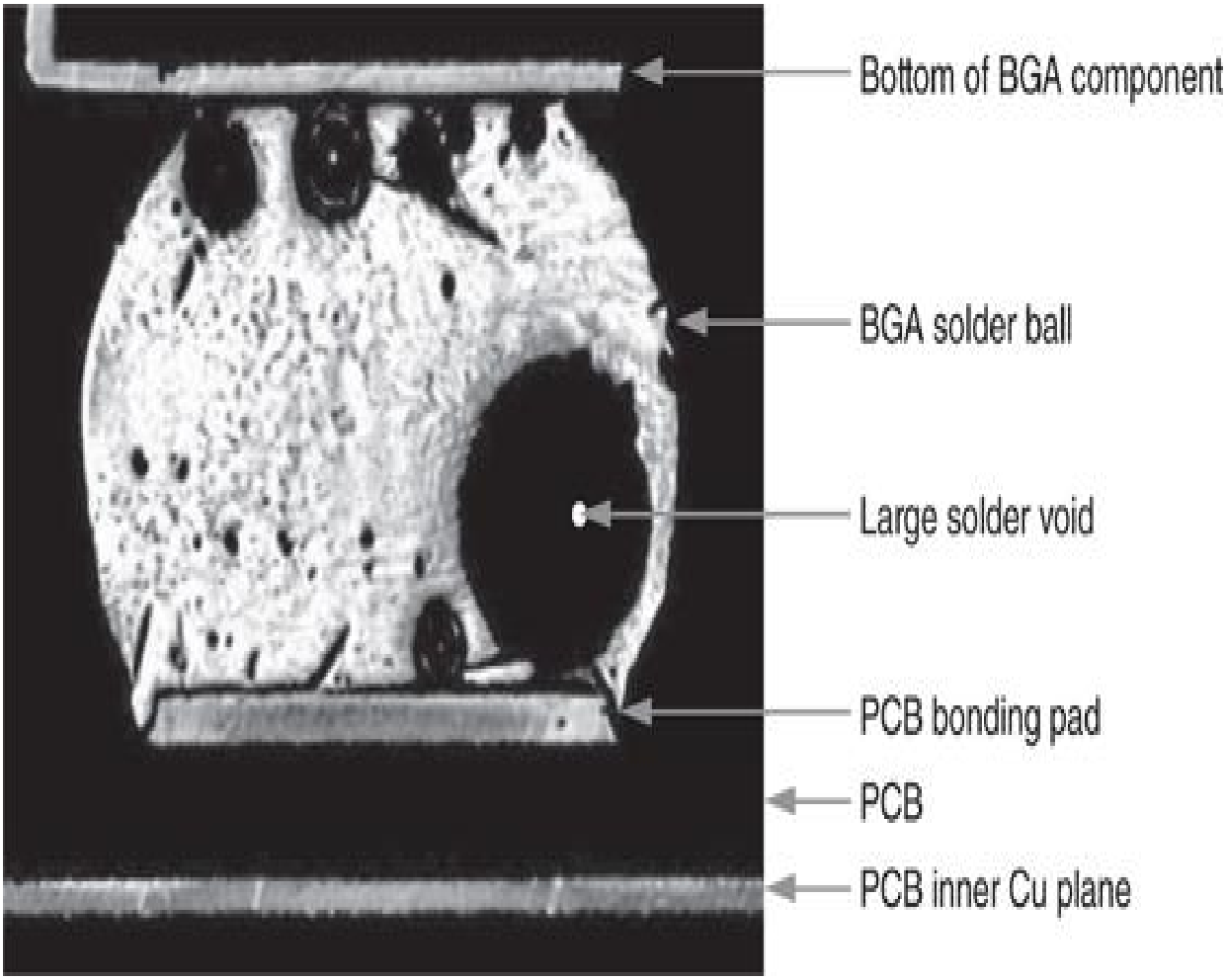

FIGURE 48.1 Metallographic cross-section of BGA component ball soldered to a PCB. Dark areas are solder voids; gas pockets frozen into the solder. Solder voids, if large enough or in abundance, may detract from solder joint reliability. (*Courtesy of Hewlett-Packard*.)

Resultant voids may detract from the mechanical strength if they are large enough, are in abundance, intersect bonding surfaces, or are in close proximity to one another.

48.2.1 Oxide Removal

The primary role for flux is oxide or tarnish removal from the metal surfaces to be joined. This includes oxides from the surface of the solder. In order for metals to alloy, the essence of soldering, each metal to be alloyed must be in contact

with one another. The metals must be free of any nonmetallic coatings including oxides, other coatings or contaminants. Flux is formulated primarily for dissolving oxides and tarnishes.

48.2.2 Reoxidation Inhibitor

Once the metal surfaces are denuded of oxide, they must remain that way until the soldering process is complete. Fluxed metal surfaces are chemically unstable, vulnerable to reoxidation if in an air environment, therefore the organic chemical constituents of fluxes are formulated to coat, protect and retard metals from reoxidizing until the soldering process is complete. If the solder flux is exhausted or overheated before or even after oxide stripping and prior to the onset of solder reflow, reoxidation would occur and solder joint formation would be impeded.

Solder fluxes are formulated for the high temperatures encountered during soldering. Were the flux to denature (polymerize or char), the byproducts would inhibit solder wetting. It is of utmost importance to follow the flux manufacturer’s guidelines for time and temperature during soldering for each flux or solder paste. Process optimization should be confined to the working limits (time-temperature) of the flux or solder paste.

48.2.3 Contamination Removal

Another role for flux is to disrupt and dissolve any organic contaminants on the surfaces of the metals to be joined. The organic solvent composition of the flux is appropriate for this. Fluxes are either alcohol-based or water-based, in either case they are composed of organic chemicals suited, not only to eliminate metal oxides, but to dissolve oils (e.g., body

oils) and other common contaminants that may be on the surfaces of metals to be joined.

48.2.4 Thermal Spreader

In some forms of laser soldering, the flow of hot flux may help to preheat leads and pads, readying them for solder joint formation. In the case of hot-bar soldering, a pool of liquid flux may help to even out thermal disparities over the length of the heated bar.

48.3 FLUX DELIVERY METHODS

Fluxes can be delivered in many different ways. For surface mounting, solder paste is used. The paste is a mixture of pure solder spheres, a fluxing agent and other materials to adjust rheology for efficient stencil deposition of the solder paste on printed circuit board (PCB) solder lands and also to endure the rigors of surface-mount oven reflow process. In wave soldering, a liquid flux is sprayed or otherwise applied to the secondary side of the board before preheat and soldering steps. In hand-soldering, the flux can be an integral part of the solder wire, which has flux-filled lumens within it (Fig. 48.2).

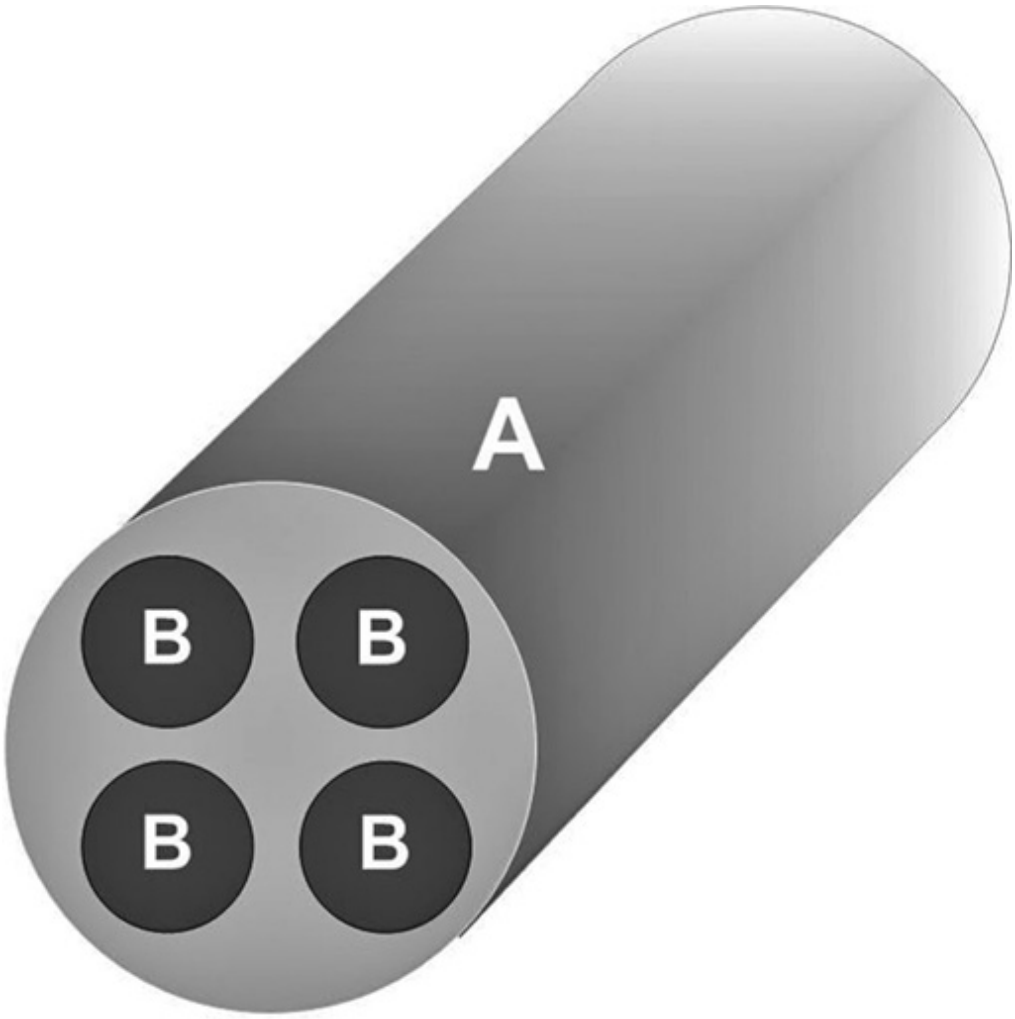

FIGURE 48.2 Schematic of a section of solder wire: (A) solder wire, (B) flux-filled lumens within the wire. The lumens extend the full length of the solder wire.

As the solder wire is heated and melts, the flux is released to do its job. For touch-up applications, a minute quantity of paste flux (a thickened gel) can be applied with a pick. Liquid flux for repair can be delivered through the use of a fine-tipped felt pen meant for flux application. Use of a dropper is discouraged as it generally dispenses too much flux and that can be a problem as discussed later in this chapter.

Not only can flux be dispensed as a liquid or paste, but it can even be delivered as a gas. Gaseous fluxing is rarely used but is gaining popularity especially in IC device manufacture because of its effectiveness and lack of residue.

This technology will be discussed briefly as it has been demonstrated to be applicable to PCB assembly.

48.4 FLUX ACTIVITY AND ATTRIBUTES

A flux's ability to prepare a surface for soldering is dependent on its chemical strength or *activity*. Just like reagents on the chemistry lab bench, there are various concentrations available. A flux may be naturally strong or it may have additives to enhance its reactive power. These additives are referred to as *activators*.[1] Activators accelerate the fluxing action either by direct chemical contribution or by catalysis. The activator can be an inorganic or organic material and combines with other ingredients in the flux, or decomposes with temperature to form an acid that is effective for oxide removal. Halogens, amino-halides, organic acids, and other materials are common activators. As the flux is heated, the activator begins its work. Flux heating for the soldering process has to be tempered for the particular type of flux formulation and solder system. Some activators may decompose if heated too quickly. Others may not be effective for a long enough time for the soldering process. Weaker fluxes (flux + activator) may require a longer preheat time and higher temperature in order to have sufficient chemical activity to remove oxidation and tarnish from parts to be joined as well as from the solder. Flux selection must be appropriate for the materials to be joined, the solder alloy melting temperature as well as for the type of soldering process. The solder chemistry chosen will greatly influence the process time-temperature profile required for the soldering process.

Like most chemical reagents, a flux's reactivity is in part a function of the exposure time and the temperature; many

exhibiting Arrhenius-like behavior, where time-dependent chemical performance increases sharply with temperature. Some fluxes are weakly active at room temperature, but most require a significant thermal assist to enable them to be useful. Ultimately the only valid test of flux performance is whether the system works for the types and conditions of printed circuit boards and components and process equipment for the soldering process. A more active flux may be needed for low melting point solder, especially if manufacturing demands high throughput for this process step. In this case, the flux will not have the benefit of longer exposure times and higher process temperatures to assist in its job of oxide or tarnish removal. Higher-temperature solder alloys require fluxes that can withstand the rigors of the required thermal process. The flux must not volatilize or decompose too rapidly nor polymerize or char at temperatures commensurate with bonding. Some metals are more prone to oxidation than others. Bismuth and zinc used in solder, and copper on circuit boards are notable examples that may require a more active flux. An inert environment is helpful in augmenting flux performance.

48.5 FLUX: IDEAL VERSUS REALITY

The ideal flux would be one that is potent, requires only a small quantity and leaves little or no residue. If it does leave a postprocess residue, the deposit would be thin, transparent, nonreflective, easily penetrated by in-circuit test probes, electrically insulating and chemically inert. If the residue is not inert, it should be easily and completely removable in an inexpensive solvent. However, this is far from reality of actual materials and process.

Flux must be applied in sufficient quantity for thorough oxide removal and to avoid both metal reoxidation and flux

exhaustion prior to solder wetting. Some post-soldering flux residues may have deleterious effects on the final circuit assembly since they may be chemically reactive and result in corrosion of exposed metals over the long term. The corrosive agents can be electrically conductive causing electrical leakage (soft shorts) between closely spaced, oppositely charged conductors on the circuit board surface. In reality, these residues are hygroscopic adsorbing moisture from the atmosphere further enhancing residue mobility and corrosiveness. Corrosion may be augmented either by natural electromagnetic force (EMF) couples between two different metals or driven by an imposed charge between two closely adjacent conductors. In either case, electrochemically driven metallic ions can plate out as metal dendrites on the once insulating, now contaminated surface of the board and produce intermittent or even persistent hard short circuiting (Fig. 48.3).

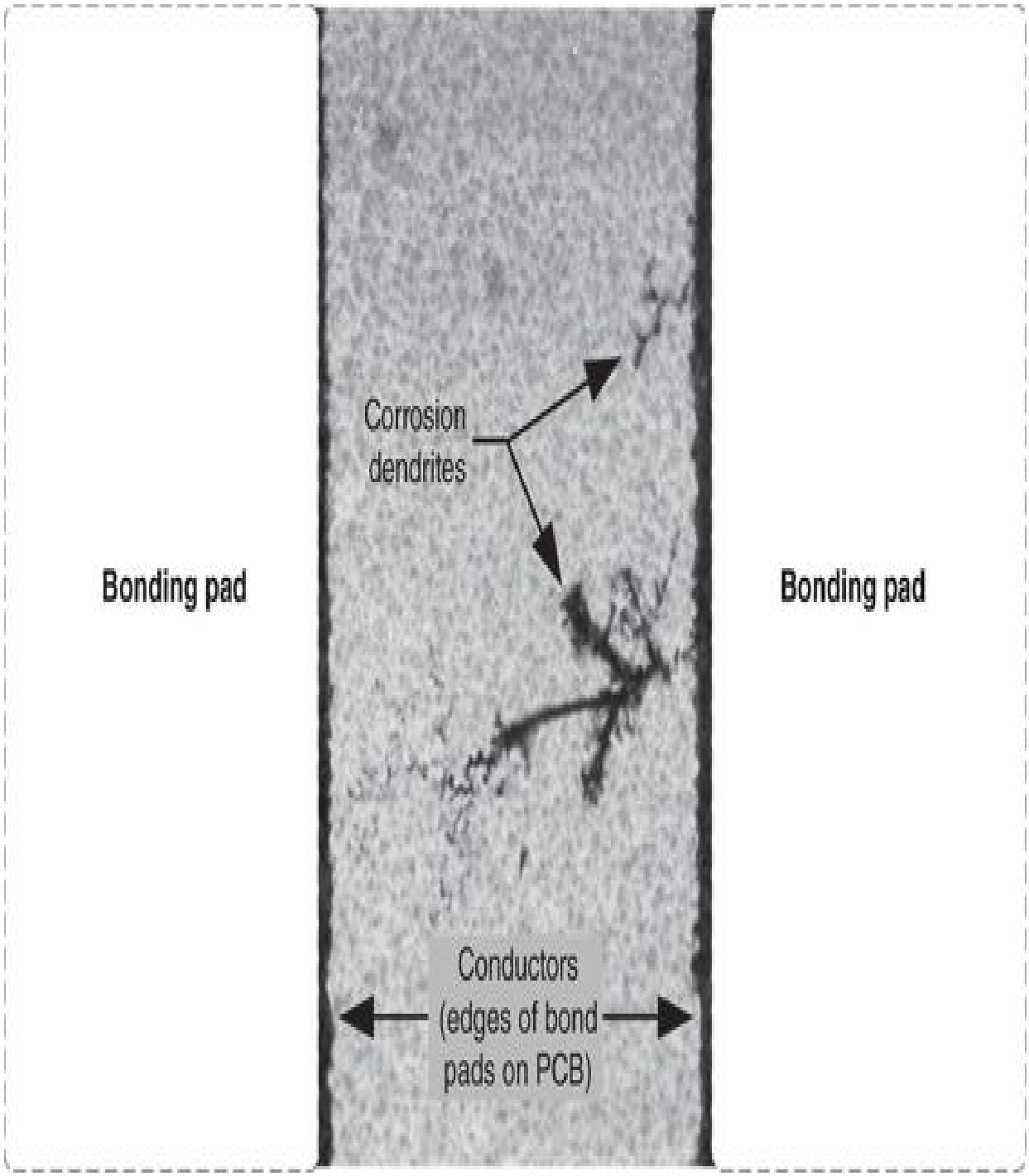

FIGURE 48.3 Corrosion dendrites caused by corrosive, hygroscopic flux residues. The dashed lines delineate the bonding pads. The corrosion dendrites are growing from the bonding pads across the PCB surface. (*Courtesy of Hewlett-Packard*.)

Flux must be heated to a temperature which allows the best reactive conditions while avoiding dry-out or

denaturation. For the sake of economy and cleaning, a thin application is necessary and should be confined to the bonding site(s) of interest.

48.6 FLUX TYPES

The 1989 adoption of the Montreal Protocol[2] imparted far-reaching changes to electronics manufacturing. In the circuit board assembly arena, it drove the elimination of chlorofluorocarbons (CFCs) and the reduction of volatile organic compounds (VOCs) for earth's ozone layer preservation. Many fluxes that used volatile organics such as alcohols were reformulated to use water as their solvent. Solvent-clean fluxes, which required nonaqueous cleaning chemicals [alcohols, CFCs and, hydrochlorofluorocarbons (HCFCs), etc.], were practically eliminated from the marketplace.

Today only two flux categories are in widespread use for PCB assembly: water-clean (aqueous-clean) and no-clean. The former leaves a residue that must be removed from the printed circuit assembly (PCA), otherwise, corrosion will occur. The latter, as the name implies, leaves a benign residue that is meant to remain on the circuit board. In fact, some no-clean residues perform as a conformal coating shielding the board from moisture and atmospheric contaminants. The choice between water-clean and no-clean has a profound effect on the process and may also affect subsequent process steps and long-term reliability. Both can be effective oxide strippers for soldering, but there are several considerations for choosing and using the proper flux.

48.6.1 Water-Clean (Aqueous-Clean) Fluxes

Also referred to as aqueous-clean flux or organic acid (OA) flux (a misleading term, because most fluxes are organic acid-based), this category contains the most aggressive fluxing agents used for large-scale commercial circuit board assembly. They are formulated with strong organic acids, inorganic acids, amines, amino salts, or often a weak organic acid fortified with reactive materials such as halogen salts (Br^-, F^-, I^-, Cl^-) that further acidify the flux. For this reason, as the name implies, this type of flux requires an aqueous wash step to remove any trace of reactive residue in order to avoid corrosion on the PCA.

Many of the water-soluble solder pastes are hygroscopic as are their residues. This property impacts solder paste or flux shelf life and the solder paste's physical attributes during printing. Of course any residue left on the PCA will affect the assembly's reliability. Most solder pastes are thixotropic; that is, they shear-thin as they are being squeegeed onto the board, becoming thinner with use. Generally, pastes are formulated to limit the degree of thixotropy. In addition to thixotropic thinning, water-clean solder pastes, when exposed to a humid atmosphere, pick up moisture, which further thins paste rheology. As a paste becomes runnier, solder paste stencil deposition becomes more difficult to control and tack (flux's stickiness as required for holding components in place), and slump characteristics (ability of paste to hold its printed shape) can be adversely affected. Ironically, some of these same organic acid solder pastes are prone to dry out in a low-humidity environment; a condition which also frustrates solder paste stencil deposition. Always check paste manufacturer recommendations for optimal temperature and humidity regimes for storage and use. Localized control of air temperature and humidity within the

printer enclosure or factory-floor air conditioning (temperature and humidity) control are necessary to preserve solder paste rheological characteristics for ease an reproducibility of printing.

48.6.1.1 Cleaning Process. PCB cleaning of unwanted flux residue consists of more than a dip in a tank of water. Generally commercially available conveyorized wash tunnels are used for effective removal of the reactive residue from the soldered PCA. Such equipment can be many meters long and may have numerous zones consisting of cold-water spray nozzles, hot-water spray nozzles, and hot-air drying. Some systems may incorporate sumps where the board is briefly submerged for a short time to enhance residue dissolution. High-purity (deionized) water is recommended to enhance washing and eliminate or minimize corrosion. Saponifiers are sometimes injected into the water stream to target organic residues and convert them to water-soluble entities. Following the saponification step, thorough rinsing with pure water is required to remove traces of the saponifying agent, which may be corrosive.

48.6.1.2 Component Compatibility. Not all components are compatible with the water-wash process. Circuit board mounted switches are notable in this regard. Even some switches sold as “environmentally sealed” or “water-wash compatible” have been found to leak during the high-pressure wash spray or submersion steps of aqueous cleaning. High pressure water jets may force water past the seals of the so-called “sealed” switches. This can result in failure of the switch to work properly (the water causes an electrical short within the switch) or, if there is enough ionic content in the wash water or in the switch itself, switch contact corrosion may occur in the long term.

Many circuit assemblies are very dense with parts. The higher the part density, the less effective aqueous cleaners

are. Like stones in a stream, the water swirls around them and eddy currents of relatively stagnant water form behind the stones. Components on a circuit board act in the same way, as they block the free flow of water and impede proper rinsing even in the most turbulent water spray systems. Many components have low clearance beneath them, inhibiting rinsing effectiveness. In the case of pin-grid arrays (PGAs), ball grid arrays (BGAs), ceramic column grid arrays (CCGAs), ceramic ball grid arrays (CBGAs), etc., the water's path is further frustrated by the presence of solder joints beneath the component. Increasing I/O count, increased package size, and decreasing space between the PCB and component underside make water washing all the more difficult. The same issues hold true for chip-scale packages (CSPs) where the headroom is little more than a capillary and good wash-water exchange is difficult to achieve. High-density, multi-row connectors are also difficult to rinse. To counteract this, aqueous wash machines have multiple spray nozzles directed at board surfaces in several directions and angles. All of the preceding are equally difficult to dry. Water beneath components or within components may interfere with in-circuit test or functional test results immediately following aqueous cleaning; the water causing shorts between adjacent circuit elements. Water from aqueous wash has been known to enter unsealed integrated circuit (IC) encapsulant fill/vent holes and cause electrical failure of the IC by shorting (Fig. 48.4).

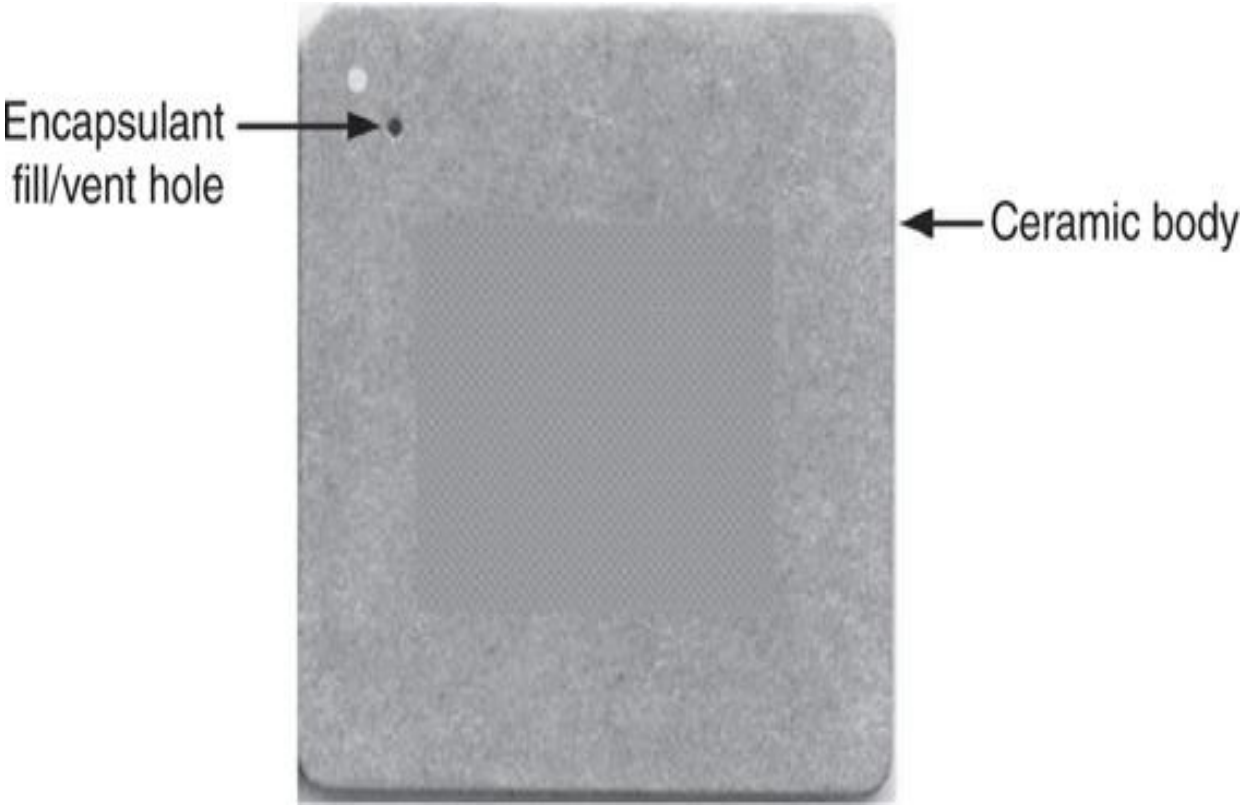

FIGURE 48.4 Top view of Ceramic PGA. If water enters an improperly sealed encapsulant fill/vent hole on an IC package, shorting or corrosion can occur within the IC package. (*Courtesy of Hewlett-Packard*.)

***48.6.1.3 Manufacturing Impact of Water-clean Process*.** There are several significant issues to consider when using water-clean fluxes and decisions are dependent on the specific parts and final product:

- *Expense:* Key financial costs include: capital equipment (washer, water treatment system); factory floor space; installation; utilities (water, compressed air, electricity); staff (operational, maintenance, training); maintenance (repair, routine). Aqueous washers are expensive and require a large footprint on the manufacturing floor. Depending on product throughput, multiple washers may be needed. Generally, high-purity, deionized water is used instead of tap water to enhance rinsing effectiveness and to minimize corrosion or shorts caused by tap water particulates or ionic species such as chlorine or fluorine as

found in treated public water supplies or even leachate from metal piping (e.g., copper, iron, lead, tin). Most aqueous systems are installed with closed-loop water systems where the water is purified onsite and reused. Regardless of reuse, some water has to be replaced due to evaporation (heating and atomization) and for rinsing of the ion exchange beds.

- *Additional process steps as compared to no-clean processing*. Washing represents several additional handling steps, and with each handling step comes risk to the board. Due to the force of the water jets in the cleaning machine, boards (especially smaller ones), are put in baskets or carriers to go through the water-wash process. This involves additional materials (baskets/carriers) and handling. There is ample opportunity to knock parts off the board during loading or unloading of these baskets. Occasionally tall parts (such as surface-mount capacitors) or miniature parts with fragile solder joints are blown off the board by the force of the water blast or solder joints can be cracked for the same reason impacting reliability. Boards that somehow escape the water-wash process or were not washed sufficiently will develop corrosion in short order.
- *Additional labor:* Besides the need for additional operators to load and unload the conveyorized wash machine, increased maintenance is required for the aqueous cleaning machine, deionized water system, and waste-water treatment.
- *Environmental impact:* The deionized water system requires frequent monitoring and filter replacement. Solder fines washed off the PCA must be filtered from the waste-water stream, and dissolved metals and other species harmful to the environment should be monitored and removed when the concentration reaches a critically high concentration before releasing spent water to the drain.

This process is not suited to geographies with water shortages, water restrictions, or poor-quality water, or where the cost of water is high.

- *Component compatibility:* As mentioned previously, some circuit board components may not be compatible with aqueous cleaning.

48.6.1.4 Benefits of Water Washing. There are significant benefits to using water-clean fluxes, but the decision involves trade-offs and must be made based on the specific needs of the parts and the product:

- *Unimpeded inspection:* PCAs that have gone through a proper aqueous cleaning process are easy to inspect because there is no flux residue on the surface to interfere with solder joint inspection by eye or automated optical inspection devices.
- *Best adhesion for conformal coating:* Some boards that are intended for harsh environments rely upon a coating of silicone, epoxy, or other material to enhance their resistance to moisture and airborne contaminants. Such treatment when applied thinly is called conformal coating (as opposed to encapsulation). Aqueous cleaned boards provide the best surfaces for adhesion of these coatings and for encapsulants (thick polymer coatings) also.
- *Recommended for use with under-fill compounds:* For added solder joint reliability, epoxies or other adhesives are sometimes dispensed under certain critical components to anchor them to the PCB surface. Aqueous cleaned PCBs will provide the best surfaces for adhesion of under-fill compounds.
- *Possible electrical implications for RF circuitry:* Flux residues can interfere with high-speed circuit conduction by changing top surface dielectric properties and increasing parasitic capacitance.[3] It is for this reason that

radio-frequency (RF) circuitry is often specified to be assembled using water-soluble fluxes.

48.6.2 No-Clean Flux

Boosted largely by cost, floor space, and environmental concerns, no-clean fluxes now dominate printed circuit assembly. This class of flux is generally composed of rosins (e.g., natural acidic plant residues such as pine pitch) and/or resins. Often, but not exclusively, the term *resin* is used to denote a manmade rosin analog.

Historically, pine sap (*colophony*, as it is referred to in older publications) is the most notable natural product used as a flux. Once extracted from the tree, the pine rosin is purified and neutralized to remove excess acidity imparted by the extraction process and dissolved in alcohol. Termed *water-white rosin*, the key fluxing agents are a mixture of abietic and pimaric acids. Water-white used to be the basis for many commercial flux offerings.

Rosin is a solid at room temperature, is water insoluble and can be dissolved or partially dissolved in alcohols. During the soldering process, the alcohol or other volatiles in the flux begin to evaporate and the rosin-based solids precipitate. The solids soften at low temperatures (50 to 70°C) and begin to flow, covering the surfaces to be fluxed. With higher temperatures comes higher reactivity and oxides and other tarnishes are stripped from metal surfaces, including from the solder, readying surfaces for solder wetting. The most widely used fluxes today are resins but act in the same fashion. Generally weak organic acid activators such as succinic, malonic, and adipic acids are added to increase the reactivity of the flux. These, too, volatilize or decompose during the reflow cycle and only a clear polymerized, noncorrosive residue is left on the board. If the process is conducted properly, the remaining deposit is relatively inert

and can remain on the PCB; hence the term *no-clean*. The best additives are ones that will not evaporate or decompose too early in the heating cycle but will completely volatilize or decompose at or near the peak temperature of the soldering process.

Halogenated activators should be avoided with No-clean chemistries. Some high-temperature organic acids may not completely volatilize or decompose, so reliability testing of the flux residues should be conducted to ensure that corrosion will not negatively impact product reliability. Besides adding activators, one can boost a flux's chemical reactivity by increasing the rosin or resin content, but the higher the rosin/resin content, the heavier the post-soldering flux residue. Pure rosinic residues, especially from high-rosin content formulations, are benign, hydrophobic, and electrically insulating, but they tend to be thick and sticky.

48.6.2.1 Benefits of No-Clean. No-clean advantages include lower manufacturing costs through fewer process steps, less board handling, less maintenance, and reduced floor space than is required for PCB assembly via water-soluble fluxing. There are also environmental benefits of no-clean, as there is almost no significant waste effluent other than from the solvent within the paste or flux that evaporates during the process and from solvents used to clean the stencil, squeegee blades, and any misprinted boards; the same stencil-related cleaning steps as needed for the water-clean process. This represents an extreme reduction in waste stream to the environment as compared to the use of water-soluble paste and flux equivalents. Most no-clean formulations are now VOC-free making this class of chemistries even more attractive from an environmental perspective. Such pastes and fluxes are generally compounded with a water-soluble solvent instead of an alcohol.

48.6.2.2 The Negatives of No-Clean. Before talking about the negatives of no-clean, it should be understood that the no-clean approach to circuit board assembly is widely embraced and is the mainstay of the industry. Any negatives of this technology are counterbalanced by major process, reliability, cost and environmental benefits. No-clean is impractical for only a small number of niche soldering applications.

48.6.2.2.1 Difficulty of Inspection. No-clean residues, especially from surface-mount technology (SMT) soldering, are generally hard, transparent polymerized deposits that interfere to some degree with solder-joint inspection. The flux deposit may crack upon cooling and sometimes operators will mistake the cracked flux residue deposit for solder joint cracking. The residue is also reflective, which can interfere with visual inspection or automatic optical inspection (AOI) methods.

48.6.2.2.2 Decrease in Barrel Fill at Wave Soldering. Since no-clean fluxes are weaker than water-soluble flux formulations, wave soldering is a somewhat less robust process. Poorer barrel fill is generally found with no-clean fluxes, although in most cases subtle changes to the wave solder machine configuration and wave solder time-temperature profile are sufficient to gain excellent or acceptable plated through-hole (PTH) barrel fill with No-clean flux at wave soldering.

48.6.2.2.3 In-Circuit Test (ICT) Probe Noncontact. Much of the no-clean flux residue associated with wave soldering of the secondary side of the board is washed off by the molten solder during the wave soldering operation. Generally, ICT is accomplished by bed-of-nails testing where sharp spring probes contact dedicated test pads located on the secondary side of the board. Although test points are masked during wave soldering through use of a selective wave soldering pallet (shield), sometimes the liquid flux,

when dispensed to the secondary side for the wave solder operation, wicks between the pallet and the PCB (Fig. 48.5).

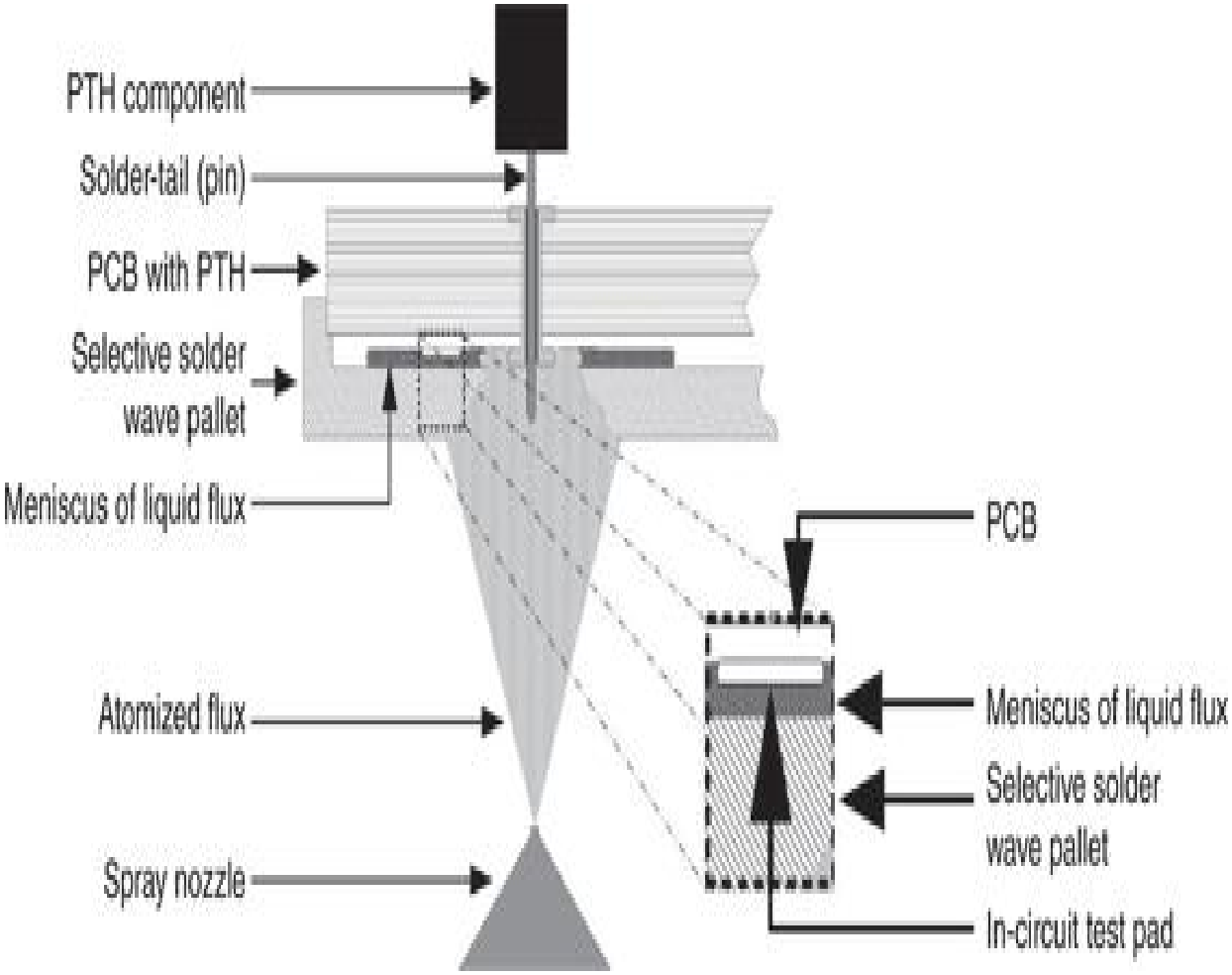

FIGURE 48.5 Spray flux wicked between the PCB and wave solder pallet forming a liquid meniscus covering an in-circuit test pad (see inset). Once run through the wave soldering process the flux will harden on the pad and interfere with ICT probe contact.

As the PCB is heated during the wave solder process, the flux hardens over the test pad and impedes post-soldering ICT probe contact (Fig. 48.6).

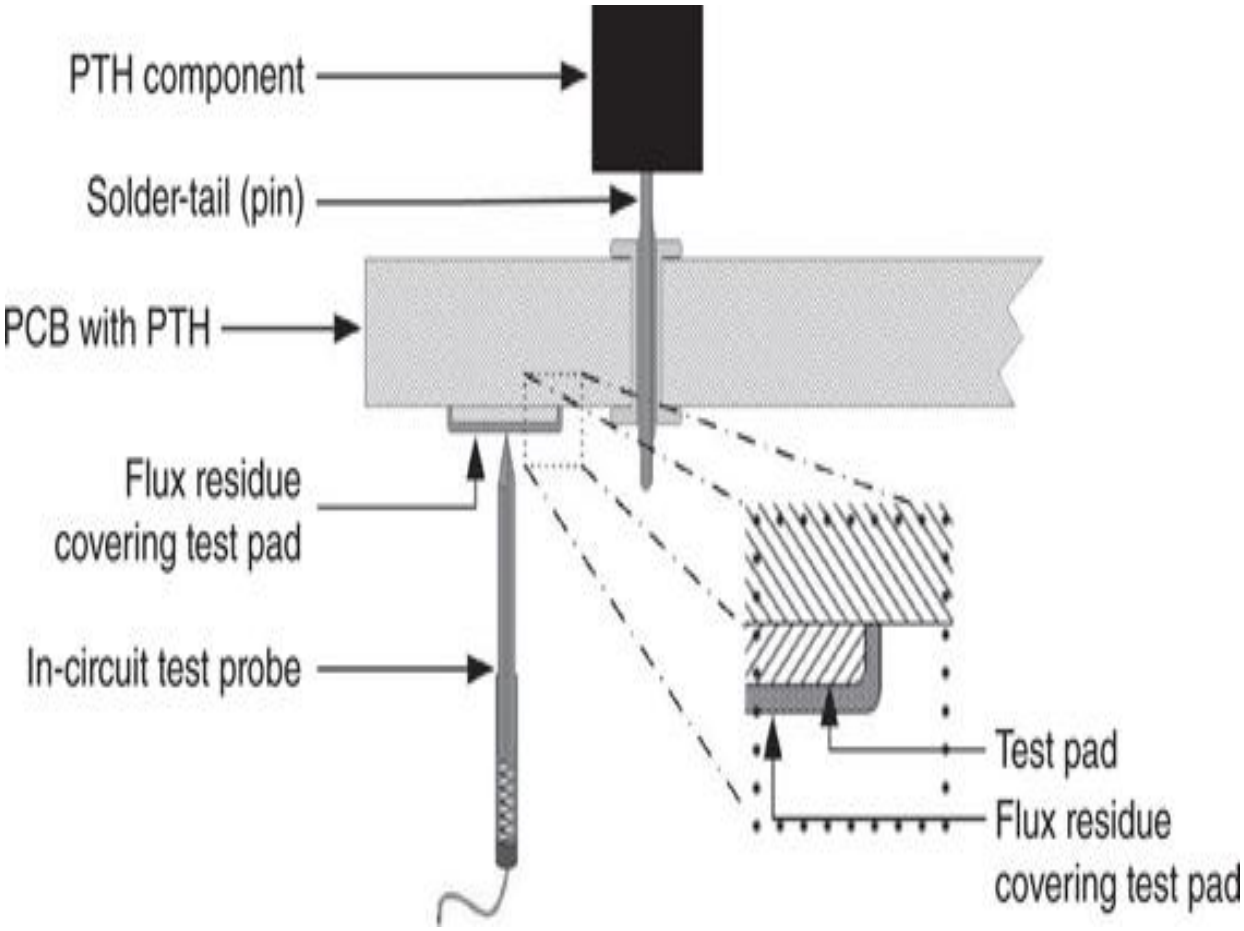

FIGURE 48.6 Hardened flux residue on test pad impeding ICT probe contact (see inset for detail). Even though the pad was shielded by the wave solder pallet, flux wicked in and hardened during wave soldering making probe contact difficult.

Without cleaning, these residues will persist. Adjustments to probe tip style and spring force may be necessary to overcome the noncontact issue. There are various types of test probes and different spring forces available. Generally, single-point probes rather than crown probes will have the best chance to penetrate hardened flux residue. With a single-point contact, point force is maximized rather than spread out over multiple points as would be the case with a crown-type probe. Using probes with high spring rates may cause the board to flex and damage solder joints or pierce through pads. Adjustment to the fluxing process, the wave

soldering process parameters or use of a different flux may help to eliminate this problem.

48.6.2.2.4 Not Recommended for Conformal Coating or Under-Fills. No-clean residue may inhibit adhesion of under-fills or conformal coatings. In fact, the flux residue may wick under a component and completely block an under-fill from entering the space between the board and the IC package to be under-filled. There are some new developments in this area and there are no-clean under-fill/flux combinations that may be effective.

48.6.2.2.5 Corrosion from Repair. Very often, even water-clean boards are repaired with no-clean formulations to avoid another aqueous cleaning step. Sometimes after a board is totally assembled, some hand-assembled mechanical components may not be suited for exposure to water. Although post-soldering no-clean residues are generally benign, care must be taken to minimize the flux dispensed during board repair. There is a chance that the pooled flux will not be fully heated (fully activated) and organic acids (activators) may not be driven off from the perimeter of the pooled flux (Fig. 48.7). If this happens, the flux will remain acidic and promote corrosion.

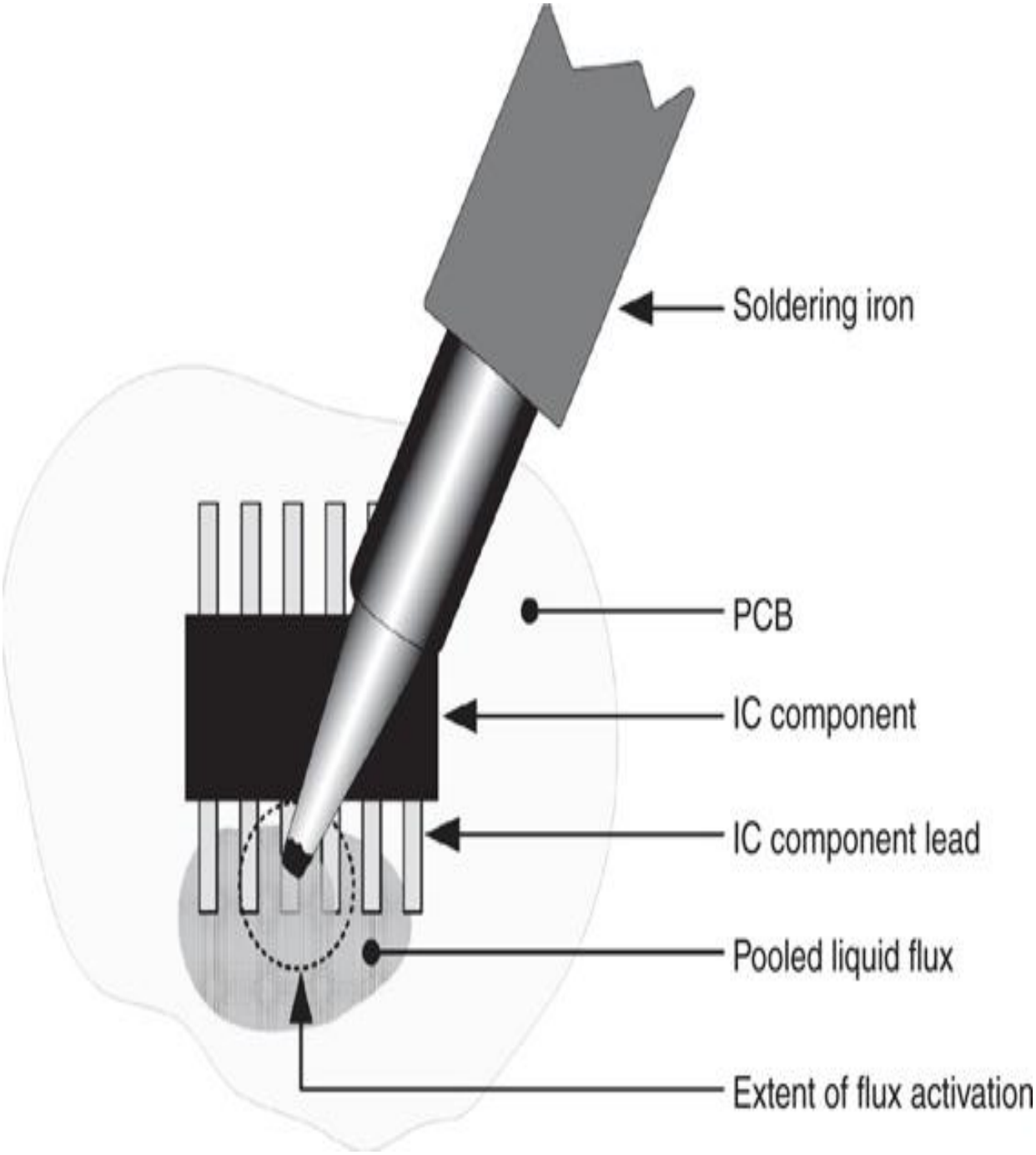

FIGURE 48.7 During repair a no-clean liquid or paste flux was dispensed and spread upon heating. Only the flux in close proximity to the soldering iron will reach sufficient temperature to be fully activated (within the dashed circle). If not fully activated, no-clean flux residue will be corrosive.

Follow these guidelines for use of no-clean solder flux:

- The use of flux-core wire guarantees that any flux for repair is fully activated.
- Use the smallest diameter flux-core solder wire for repair to minimize residue.
- If the use of flux-core wire is not practical, use the smallest amount of flux possible for each repair.
- Flux should be strictly confined to the area that is to be heated for repair.
- Dropper-dispensed liquid flux should be avoided. Liquid fluxes are prone to spreading and if not heated sufficiently any flux residue poses a corrosion hazard. Small amounts of liquid flux can be applied with an ultrafine, electrostatic discharge (ESD)-safe, felt-tip flux pen or artist brush.
- Use the smallest amount of paste flux as it too will spread upon heating and outer limits of pooled flux may not be fully heated (fully activated) and corrosion will occur. Minute amounts of paste flux can be applied with a fine pick or pin. Paste flux does not spread as much as a liquid flux. Once the heating begins, the paste will liquefy and spread but not to the extent of a liquid flux.
- Ensure that all the flux dispensed has reached a near-soldering temperature to drive off or denature any corrosives and render its residue less prone to corrosion.
- Use the same flux or flux from the same family for repair as was used for primary assembly of the PCB to avoid corrosion. Reputable solder flux manufacturers should be able to provide test data to show which fluxes are compatible with each other and which repair chemistries are compatible with which solder paste residues.
- Do not clean no-clean residues. Do the repair correctly the first time. Cleaning tends to spread flux residue. Often cleaning results in unsightly residues; much worse than was the original repair.

- Heating a repaired PCA in a box oven will activate any stray flux. Consult flux manufacturer for proper temperature-time range for activation. Ensure that all hand-assembled parts on the PCA will be compatible with the activation cycle.

48.6.3 Other Fluxing Caveats

Several general issues regarding fluxes must be considered before selecting one for a process and product.

48.6.3.1 Solder Paste Misprint Cleaning. When solder paste is printed in a manufacturing setting, occasionally the paste deposit is misprinted or smeared, requiring that it be thoroughly removed from the PCB before reprinting. Although this is not truly a fluxing issue, it does have ramifications to the process and reliability and is an important flux chemistry-related topic. The cleaning solvent may also diminish the effectiveness of OSP-copper coatings.

If the PCB has components mounted on one side while the other side is being printed, this too has implications for the misprint cleaning process. Here are some guidelines for accomplishing this:

48.6.3.1.1 Aqueous-Clean Solder Paste Misprint Cleaning

- A standard aqueous board cleaner or an aqueous stencil washer can be used for solder paste removal. DO NOT WIPE OR SMEAR THE PASTE. Allow the paste to wash off during the aqueous cleaning process.
- Ensure that all parts on the board are compatible with aqueous cleaning. Some surface-mount switches may not be compatible and may need to be removed from the board or masked to prevent damage from water leakage.

- If SMD placement has begun, remove any high-value components from the paste on the side that is misprinted or smudged.
- Do not wipe solder paste off the board, as this will force paste into vias, plated through-holes, and solder mask clearance areas. Once reflowed, any solid solder residues may interfere with PTH component insertion or press-fit operations (Fig. 48.8).

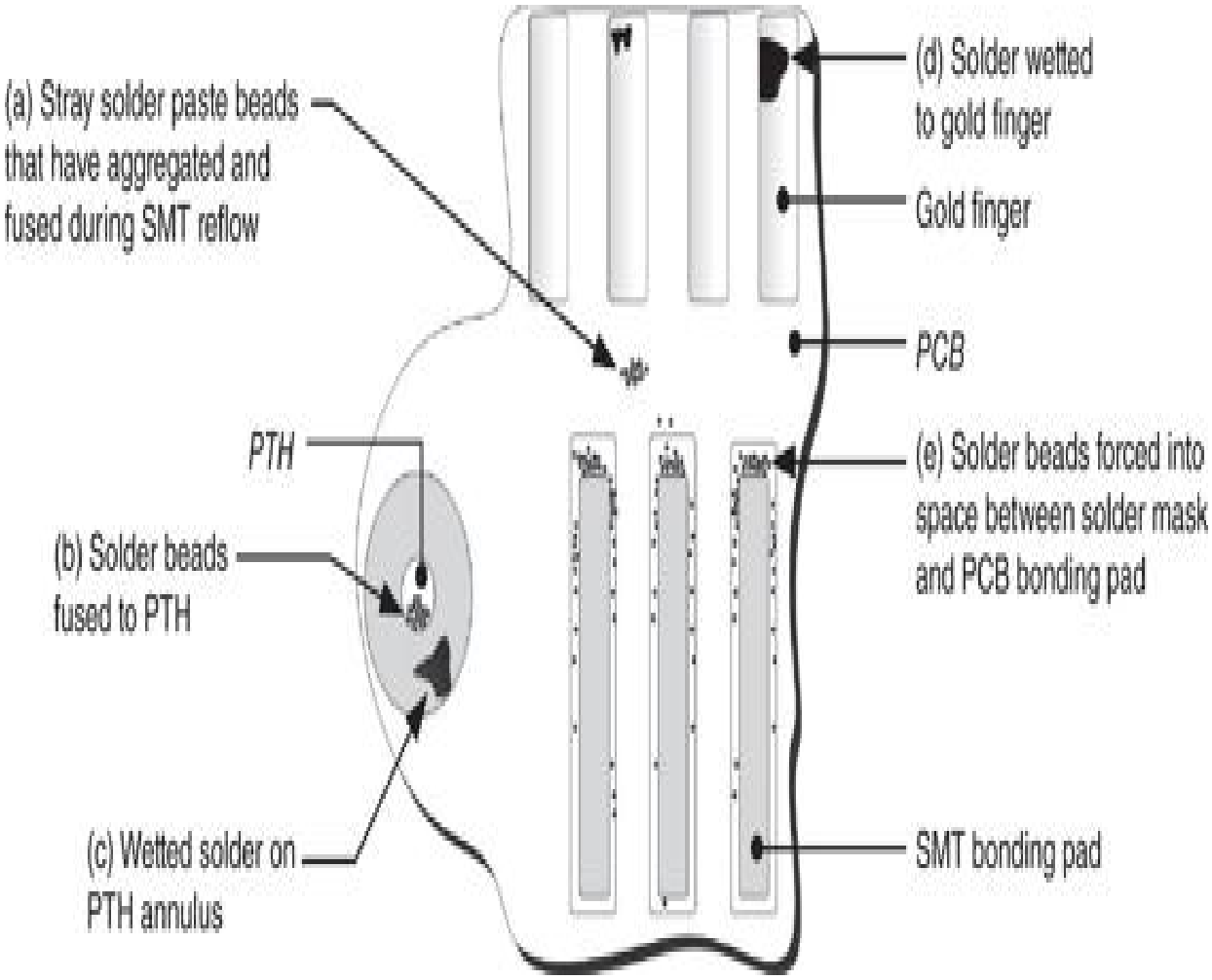

FIGURE 48.8 Common problems associated with wiping paste off of a solder paste misprinted PCB. Stray solder beads on the surface of the PCB (*a*) may weakly solder together and pose a shorting hazard. Solder beads fused to PTH (*b*) may prevent proper insertion of solder-tail. Stray solder on PTH annulus (*c*) may interfere with proper seating of PTH or press-fit component. Unwanted solder on gold fingers (*d*) may damage the mating edge connector. It may also result in an

unreliable contact in the long term. Solder beads swiped into the space between solder mask and bonding pad (*e*) may fuse and become a shorting hazard.

- If tape is used to mask gold fingers or other features, remove it before the commencing misprint cleaning to avoid entrapping solder beads or paste residue beneath the tape.
- Do not use a saponifier or solvents other than water unless the flux chemistry has been tested and qualified for compatibility and unless saponification or other solvent is in use with standard post-solder board cleaning.
- Do not use ultrasonic cleaners. Even random-frequency/random-amplitude ultrasonic cleaners may impact certain devices already mounted on the board (e.g., on the secondary side). Crystal oscillators are notoriously sensitive to ultrasonic cleaning. Other components have been known to degrade or fail as a result of ultrasonic agitation-induced damage to internal bonds or die attach.
- After cleaning, use a microscope with as high a magnification as is needed to see individual solder spheres from the paste. Ensure that stray solder spheres are not present, or, if they are, ensure compliance with the workmanship standard in use. Also confirm that paste beads are not agglomerated in plated through holes. Generally a ≥30× stereo-zoom microscope with good lighting is recommended for this inspection.
- If excess solder beads are still apparent, the board should be re-cleaned. Reposition the PCB in the cleaner rotating it 90° or 180° for the repeat cleaning cycle.

48.6.3.1.2 No-Clean Solder Paste Misprint Cleaning. Cleaning boards printed with no-clean paste requires a little more care, but most of the same rules apply as for removing paste from a PCB printed with water-clean solder paste. Generally misprinted boards are cleaned in the

same machine for cleaning stencils, using the same paste cleaning solvent as used for the stencil. In addition to the rules in the previous section, observe these for treating misprinted no-clean solder paste:

- If one side of the PCB has been soldered already do not use water to clean a no-clean soldered board unless the solder paste manufacturer recommends it especially. Mixing water with some no-clean flux residues may result in a sticky, white residue. Besides being unsightly, the hydrated deposit may impact electrical surface insulation resistance (SIR) and result in corrosion.
- Do not use saponified water with No-clean unless the process has been tested for materials compatibility and corrosion. SIR testing and electrochemical migration (ECM) testing should be performed to ensure that there are no destructive interactions.
- If using solder-preservative coated copper (OSP-copper), determine if the cleaning solvent has any adverse effect on the coating. Some solvents have been known to reduce the solder-preservative coating’s effectiveness.
- Direct immersion should be avoided. Immersion can cause cleaning solvents and diluted flux residues to enter previously mounted switches and other components. This, in turn, can result in an electrical short internal to the switch (from cleaning solvent conductivity), an open (from insulating flux residue), or corrosion (also from flux residue).

48.6.3.2 Mixed Repair Strategies. If a PCB has been soldered using a water-clean flux formulation, complete all solder repairs prior to a final cleaning using a solder flux chemistry compatible with the flux used for the original assembly. If the board requires repair after final cleaning it is common practice to complete the repair with a no-clean flux. This strategy precludes the need for another wash cycle. In

another situation, there may be parts that are added to the PCA after mass reflow such as electromagnetic interference (EMI) shields, enclosure pieces, heat-sinks and other mechanical or hand-assembled parts. These may not be compatible with an additional wash cycle as may be required for repair are accomplished with an aqueous-clean solder flux. This, too, necessitates the use of a no-clean repair strategy.

Once a board is repaired with a no-clean flux, it is imperative not to subject the board to an aqueous cleaning process for the reasons previously described (white residues, degraded reliability). Conversely, aqueous cleaning must be used if a water-wash flux chemistry is chosen for repair.

48.6.4 Test for Flux Compatibility

Certain no-clean fluxes are not compatible with each other. Their chemical interaction could result in corrosion on the PCA. To avoid corrosion issues, solder paste flux, wave solder flux, and repair flux should be tested separately and in combination for SIR and ECM for compatibility with each other and for compatibility with the board surface finish and solder mask.

48.6.5 Ensure Full Flux Activation of No-Clean Fluxes during Repair

As mentioned previously, it is important to heat no-clean flux sufficiently to activate it (make it chemically reactive) and to burn off the activators by the end of the soldering process. If an unactivated, insufficiently heated no-clean solder flux is left on a board, the weak organic acids in the flux residue often result in corrosion over the long term. Usually temperatures between 80°C and 150°C (depending on the

flux composition) are sufficient to activate a flux fully. To minimize the possibility of corrosion:

- Avoid pooling flux by banning the use of liquid fluxes or large quantities of paste flux for soldering iron-based repair.
- Dispense liquid flux sparingly by using an ultrafine artist paint brush, ESD-safe, fine-tipped felt fluxing pens or a bit of paste flux on a fine pick.
- Use finest diameter no-clean flux core solder wire to minimize flux deposition and for the best chance of reaching flux activation temperature. This is the only convenient strategy that guarantees full flux activation during repair. Flux-core solder wire is available in diameters less than 1 mm. Of course, flux-core solder wire cannot be used for area array device repair, but in that process flux is certainly fully activated by the soldering process.

48.6.6 Localized Solvent Cleaning of No-Clean Flux Residue

The need to remove no-clean flux residue from a PCB after repair is the sign of a failed repair strategy resulting in too much flux and reflective of poor workmanship. Often cleaning solvents are applied locally in an effort to move excessive flux deposits. Sometimes these solvents are formulated specifically for flux cleaning. Sometimes pure chemical solvents, such as alcohols, are used. Very often solvents and flux cleaners leave gummy residues on the board. They can also dissolve the no-clean flux residue and redistribute it, exacerbating the mess. There is danger that dissolved residues can find their way into board-mounted connectors via capillarity or dripping or onto board-edge gold fingers. This can result in electrically insulating flux residues

that interfere with proper electrical interconnect. In general, the use of flux removal solvents for localized cleaning should be avoided. Instead, either eliminate the need for repair or define repair methods that result in good workmanship and do not necessitate the use of a cleaning solvent.

When cleaning is mandated, as would be the case where flux or flux residue contaminates a board-edge gold finger, care should be taken in choosing a cleaning solvent. Some solvents have been known to result in corrosion. Others may interact with solder-mask or other materials on the PCB. Some have health and safety implications.

Some solvents are more effective than others depending on the quality of the flux residues. In general, methanol (methyl alcohol) is a better cleaner than isopropyl alcohol (IPA). It has lower water content and it dries much quicker and more thoroughly than the latter. Care must be taken with methanol as it is flammable and its fumes are toxic. This is often true of other commercially available flux cleaners.

Any cleaning solvent, if applied liberally, may remain trapped in connectors or under low-headroom devices such as chip-scale packages (CSPs) and micro BGAs, mounted on the PCA. Any flux cleaner, especially the slower drying ones such as IPA, may cause electrical shorting if not thoroughly dry before powering up an electrical circuit on a recently cleaned PCA.

Although sometimes flux cleaning is necessary or useful, it is best to avoid the need for cleaning by minimizing the flux dispensed and dispensing the flux only to the lead or leads to be repaired. Training, skill, patience, and practice are required for accurate flux dispensing and soldering. Best practice is to apply a dab of the flux cleaner to a lint-free wipe or lint-free swab and clean very locally taking care not to mar the PCB surface or damage any solder joints. Dry thoroughly after cleaning. Even a short drying cycle in a box oven at a low temperature (e.g., 45°C for 15 min) would be useful to ensure full evaporation of any entrapped solvent

before electrical power-up. But the very best practice is no cleaning whatsoever.

48.7 SOLDERING ATMOSPHERES

The natural heat of the soldering process, combined with the oxygen from the air, can inhibit soldering by creating oxides that compete with the action of a flux. To avoid this problem, inert or reactive gas atmospheres can be used during soldering.

48.7.1 Nitrogen Soldering

Nitrogen (N_2) as a cover gas for soldering has been in use for many years and is considered commonplace in today's electronic assembly.[4–14] Its role in reducing oxidation during the joining process ensures best solder wetting. Soldering in a nitrogen atmosphere has become increasingly important in recent years, driven by the rise of weaker no-clean fluxes and no-clean solder pastes and the upsurge in the use of area-array devices such as BGAs, CCGAs, CBGAs, CSPs, QFNs in reflow, and PGAs, along with complex, finer-pitch connectors in wave soldering.

Area-array devices have one thing in common: their solder joints are hidden by the package body and it is impossible to repair an isolated open solder joint beneath the package. Nitrogen provides added insurance that best solder wetting will result if soldering conditions and materials are process-appropriate.

The most recent increase in N_2-assisted soldering comes with the onset of large-scale lead-free soldering implementation around the world. Higher process temperatures, as necessitated by the most popular lead-free

solder alloys, translates to higher oxidation rates during soldering. Also, certain solder alloys (e.g., those containing Zn, Bi) are more prone to oxidation than conventional Sn-Pb or Sn-Ag-Cu solders.

48.7.1.1 Use of N_2 for Increased Fluxing Effectiveness.

The soldering environment is an important variable. Obviously the most common and least expensive soldering ambient is air, but many board assemblers choose to introduce nitrogen to their reflow ovens, wave soldering machines, or repair stations for the soldering advantage it offers. N_2 is particularly effective when working with no-clean solder pastes or fluxes and has gained increased importance with the conversion to Pb-free soldering. Most all of the Pb-free solders that are in widespread use for the electronics industry are slower to wet and require higher reflow temperatures than the old Sn/Pb standard. The higher the temperature of a metal in an oxidizing atmosphere, the more prone it is to oxidation. The introduction of nitrogen limits oxidation of the metals to be joined, the solder, and even the flux itself. Replacement of air with N_2 results in more effective removal of oxides and tarnishes and enhances solder wetting. At wave soldering, when N_2 is used there is a substantial reduction in dross production rates. Dross is composed of metal oxides from the solder that forms a dense, floating mat on top of the molten solder. It is known to cause wave solder defects (shorts and opens) and since it is oxidized solder, it represents a loss of solder mass therefore it has direct economic implications for the wave soldering or solder fountain processes. In order to cope with the dross, it has to be manually skimmed or ladled from the molten solder to keep the process in control; another time consuming and dangerous maintenance step.

48.7.1.2 Use of N_2 for Lighter, More Transparent No-Clean Residue. When circuit boards are soldered in air, some no-clean residues turn yellow or brown. This is more apparent after multiple reflow cycles as for mixed-mount assembly. Residue coloration is absent when soldering in a nitrogen environment. Clearer no-clean residues make for easier visual or machine inspection of solder joints on finished PCAs. It should be noted that the use of nitrogen even keeps the PCB laminate from darkening especially at the higher temperatures required for Pb-free soldering.

48.7.1.3 Nitrogen Negatives. There are some negative points that must be considered when working with N_2.

48.7.1.3.1 Cost. Nitrogen is an added expense for manufacturing, not only for the cost of the gas itself, but the infrastructure that is required for bulk N_2 delivery, storage and process use. In a factory environment it is impractical and dangerous to store large numbers of gaseous cylinders or portable liquid N_2 dewars onsite and manually change them out on a regular and frequent basis; for this reason, onsite, outdoor bulk gaseous storage is needed. This comes with facility capital costs including: cement pad for outside storage tank and vaporizers to convert stored liquid N_2 into usable room temperature gas. Pressure regulation is required for delivery into the factory as well as piping and further pressure regulation at point of use.

48.7.1.3.2 Tombstoning. It has been found that even modest flows of N_2 are beneficial. However, too much nitrogen during reflow leads to passive component tombstoning (Fig. 48.9).

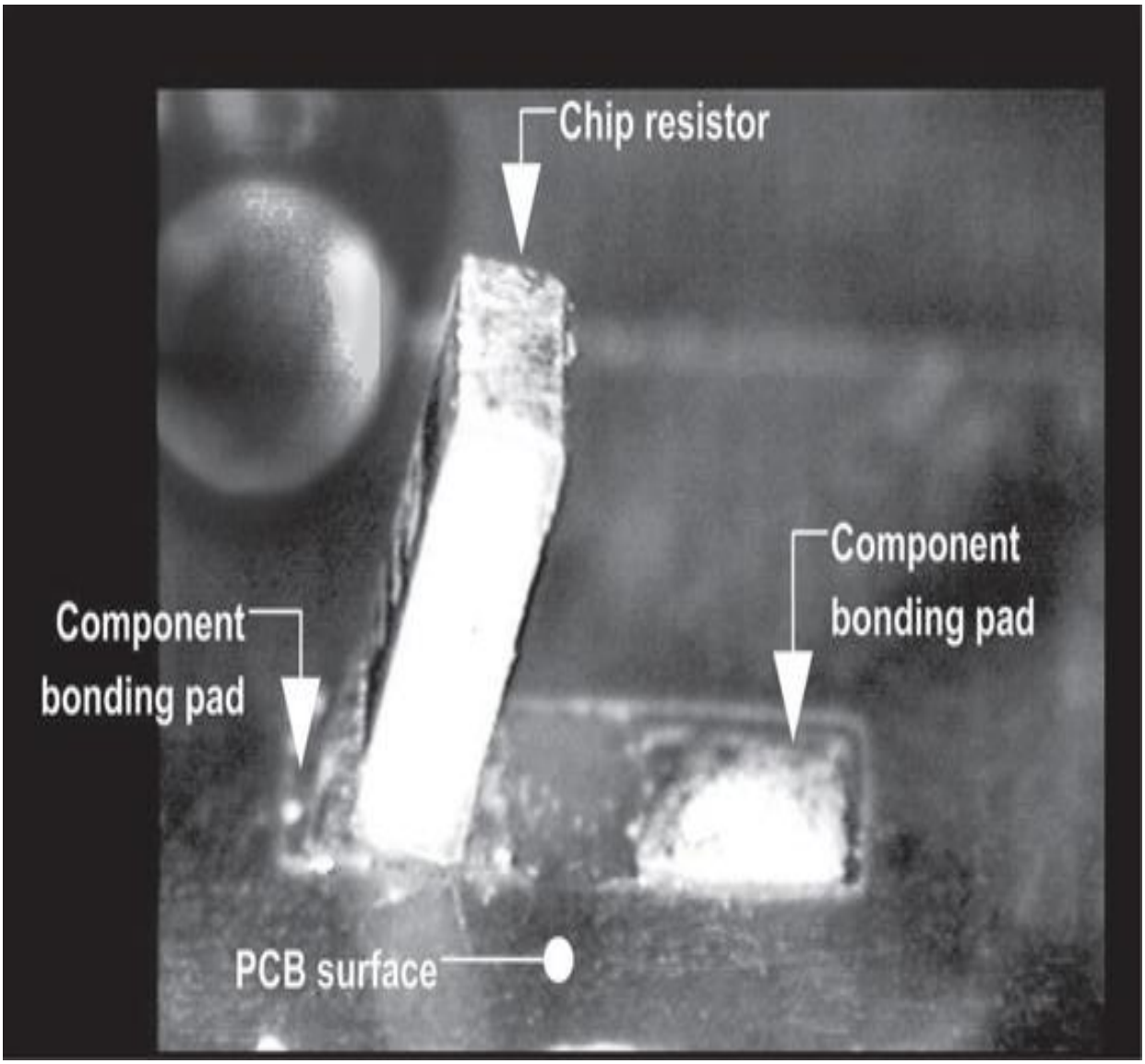

FIGURE 48.9 Passive component exhibiting tombstoning. Differential heating and surface tension effects have drawn the lightweight chip away from the surface of the PCB during reflow. On solidification, the component is frozen in the raised position and an open circuit results.

Often tombstoning is the direct result of a thermally imbalanced PCB design. One bonding pad is connected to a thick, slow to heat subsurface copper conduction plane or even multiple planes. The opposite bond pad is connected to a low thermal mass surface copper trace. During reflow, solder paste on the fine trace goes molten first. As the solder continues to wet around the one end of the passive device,

surface tension of the molten solder on that wetted end lifts the chip off the board before the solder paste on the opposite end goes fully molten and wets. An open solder joint results. This defect, sometimes referred to as the “Manhattan Effect,” “standing proud,” or “drawbridging,” is most often seen on the smallest passive devices.

The defect is exacerbated by an excessively low O_2 content (high N_2) of the reflow oven atmosphere. Low oxygen results in better fluxing which results in increased surface tension of available molten solder, since it is devoid of oxide platelets on its surface. Wetting to one end, the molten solder seeks its lowest energy state, a dome. As the solder continues to wet around one end of the passive component, it draws its one wetted end more fully into the dome lifting the other end clear of the PCB. Care should be taken in design for a thermally balance PCB design. Oxygen monitors can be used to sense the amount of nitrogen in an oven. Maintaining a reflow oven oxygen concentration level of about 1000 to 1500 ppm O_2 will benefit reflow and minimize tombstoning. Inerting to this level is also significantly more economical since nitrogen consumption is less than when running at lower O_2 concentrations. It is easier to maintain a constant O_2 level in this regime as opposed to ultralow O_2 concentrations since subtle drafts at reflow tunnel ends can result dramatic variations in O_2 concentration.

48.7.2 Fluxless Soldering

There have been many discussions and investigations into fluxless soldering, but often this term is incorrectly applied. Disruption of the integrity of oxides on the parts to be soldered and on the solder itself is a requirement for solder wetting. If a thermal or thermal-mechanical method is solely

employed (e.g., as by ultrasonic soldering), then it is truly a fluxless method. If a chemical agent is applied for oxide removal, whether it is in solid, liquid, or gaseous phase, it is still a flux-based process. Using cover gases alone does nothing to clean oxidized leads, bonding pads, or solder, but will limit further oxidation.

Work by G. Disbon and S. M. Bobbio[15] and K. Pickering, et al.[16] have demonstrated that a plasma can be used to strip oxides from circuit boards and components, and, if they are maintained in an inert environment, they can be soldered without the use of additional liquid fluxing agents. In these schemes, the plasma serves as the oxide-stripping flux. Such processes would not be appropriate for mass production of today's PCAs.

48.7.3 Gaseous Fluxing

It has already been discussed that flux can exist as a liquid, paste or solid (solidified rosin), but it can also be dispensed as a gas. There have been several investigations into the realm of fluxing with various gaseous species, including hydrogen, carbon monoxide, carboxylic acids, and others. Some have been demonstrated to be effective fluxing agents, but none of these methods have found their way to large-scale manufacturing. Instead, they are used in niche applications. Investigations continue in this area.

48.7.3.1 Hydrogen. There has been talk in the industry of hydrogen as a fluxing agent, but at soldering temperatures, hydrogen is predominantly an unreactive, diatomic, gas; in fact, even at 1730°C, it is only 0.33 percent dissociated at atmospheric pressure.[17] Therefore, it is relatively stable chemically, serving ostensibly as an expensive cover gas; an inerting blanket rather than a reactive fluxing agent. H_2 explosively combines with O_2 in

the presence of an energy source such as a spark, so it is typically mixed with N_2 or another inert gas when used for processing. This mixture, called *forming gas*, is susceptible to separation. Since hydrogen is lighter than air, it rises and may pocket in the upper recesses of the soldering machine or in the room. Its lower explosive limit in air is only 4.65 percent[18] so precautions have to be taken either to keep below this value or to preclude exposure to an ignition source (difficult to do in a reflow oven or today's PCA factory environment). Its upper explosive limit is 93.9 percent, above which hydrogen is once again considered safe, but this is impractical economically and a gas containment vessel would rule out a reasonable continuous process and affordable equipment and for use as a cover gas only.

48.7.3.2 Carbon Monoxide. Carbon monoxide is an interesting choice. Very dense, it readily displaces air from the soldering environment and is inexpensive. Since it is a heavier-than-air toxin with considerable public notoriety, it is unlikely that it will ever be considered an attractive assistive agent for reflow. Also, carbon monoxide does not dissociate sufficiently well at soldering temperatures to be useful for effective fluxing, but does make an excellent, weakly reducing cover gas much as hydrogen does.

48.7.3.3 Methyl Bromide. This material has been shown to be an effective fluxing agent but is toxic. In fact, it is now a banned pesticide in the United States.

48.7.3.4 Carboxylic Acids. The idea of a gaseous fluxing agent has much merit. It could be inexpensive, eliminate post-solder cleaning, and leave no residue to impede inspection or test. Without residues, the prospect of corrosion would be minimized.

Carboxylic acids in gaseous phase have been demonstrated to be useful in this regard, but it has yet to

undergo large-scale testing in a manufacturing environment. Of the carboxylic acids, formic and acetic have received some attention as fluxing agents. They are very simple materials, weak organic acids that decompose to water and carbon dioxide at temperatures above 160°C.[19] Acetic, in its dilute form, is vinegar. Carried as a vapor and introduced to the soldering environment, it is truly a gaseous flux. Both formic and acetic are widely used industrially and are inexpensive reagents. H. J. Hartmann[20,21] has shown that as formic decomposes, it is a good reducing agent for oxides of solder. The process produces metastable tin formate, which further decomposes, yielding elemental tin, water, and carbon dioxide. Acetic acid follows a similar reaction and decomposition cycle, forming metastable tin acetate and ultimately elemental tin. Especially attractive is the fact that there is no flux residue on the circuit board after the gaseous carboxylic acid reactive soldering process.

R. Iman et al.[22] have demonstrated formic and acetic acids to be especially effective for fluxing in the wave-soldering process in conjunction with a light application of adipic acid, a common food preservative and also a known fluxing agent. However, a water rinse was required to remove the adipic residue lessening its value as a fluxing agent.

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CHAPTER 49
SOLDERING TECHNIQUES

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

49.1 INTRODUCTION

Soldering has changed significantly over the millennia progressing from melting heated materials in an open fire to the fire-heated soldering iron to the blow-torch and to present electrical resistance-heated techniques. Although the materials and scientific knowledge have evolved drastically, the fundamentals of this joining process remain the same. The advent of the printed circuit board (PCB) drove the need for soldering and repairing finer geometries. Mass marketing of the finished printed circuit assemblies (PCAs) spurred the invention of a handful of soldering technologies to cope with demands of intricate assembly, timely manufacturing and machines for repair.

There are two categories of soldering methods: (1) mass soldering and (2) directed-energy bonding. Mass soldering techniques target the entire circuit board, soldering all components simultaneously. Directed-energy methodologies

are useful for localized soldering of a single component lead, whole component comprising two or more leads or for soldering a small section of a circuit board.

49.2 MASS SOLDERING METHODS

Mass flow or reflow methods are suited for high-volume manufacturing. The entire board is heated and the entire complement of components on the board are soldered simultaneously. The two most common of these methods are oven reflow soldering and wave soldering. A third technique, vapor-phase reflow soldering, has dwindled in popularity due to environmental concerns regarding the use of the chlorofluorocarbon-based solvents that were key to this process. Now, however, perfluorocarbons are substituted and the technique is still in use. Regardless, it is a slow technique as compared to oven reflow or wave soldering. Its benefits will be discussed in a subsequent section. The choice of soldering method is dictated by the types of components and boards being soldered, the required throughput rate, and requisite solder joint properties.

49.3 OVEN REFLOW SOLDERING

Oven reflow is used primarily for surface-mount component soldering. To prepare a board for this process, a mixture of minute solder spheres and paste flux (solder paste) is stenciled onto the circuit board. Stencil openings are cut to roughly match the size of the soldering lands on the PCB. Stencil thickness is tailored for the amount of solder paste needed and somewhat by the geometry of the solder lands. The paste flux, a constituent of the solder paste, prepares the metal surfaces for solder attachment while the solder

spheres provide the alloy for solder joint formation. Electronic components are precisely machine-placed onto the stenciled solder paste and the entire assembly is placed in an oven and heated through a controlled ramp and dwell cycle. The heating regime is dictated by the thermal mass of the assembly, thermal exposure rating of the electronic components to be soldered and the time and temperature requirements as specified by the solder paste manufacturer. After the solder reaches reflow temperature and slightly beyond, the PCB is cooled and the surface-mount process for that side of the board is complete.

The equipment used to accomplish the PCB heating and reflow is a conveyorized reflow oven and the board is moved past stationary heaters in an insulated tunnel. The oven is set to raise the circuit board and component temperatures gradually. Flux in the solder paste becomes active with increased temperature and strips oxides and other contaminants from metal surfaces on the components, on the solder lands (pads) on the board, and from the solder spheres that would inhibit solder joint formation. Finally, enough heat is imparted for the solder to flow (meaning to liquefy, also known as reflow). When implemented properly, the oven reflow process should result in a controlled and predictable heating and cooling cycle and reproducible solder joint formation.

Rapid heating of the solder paste is widely known to cause excessive gasification of solder paste volatiles resulting in bursting bubbles in the solder paste and in the molten solder. The spewed solder debris is one source of solder ball formation. Solder balls (isolated spheres of solder not necessarily connected to the solder mass of the joint) may induce electrical shorts, especially with finer-pitch components where solder ball diameters may be on the order of component lead or PCB pad spacing. Such solder fines also make for a messy assembly (Fig. 49.1).

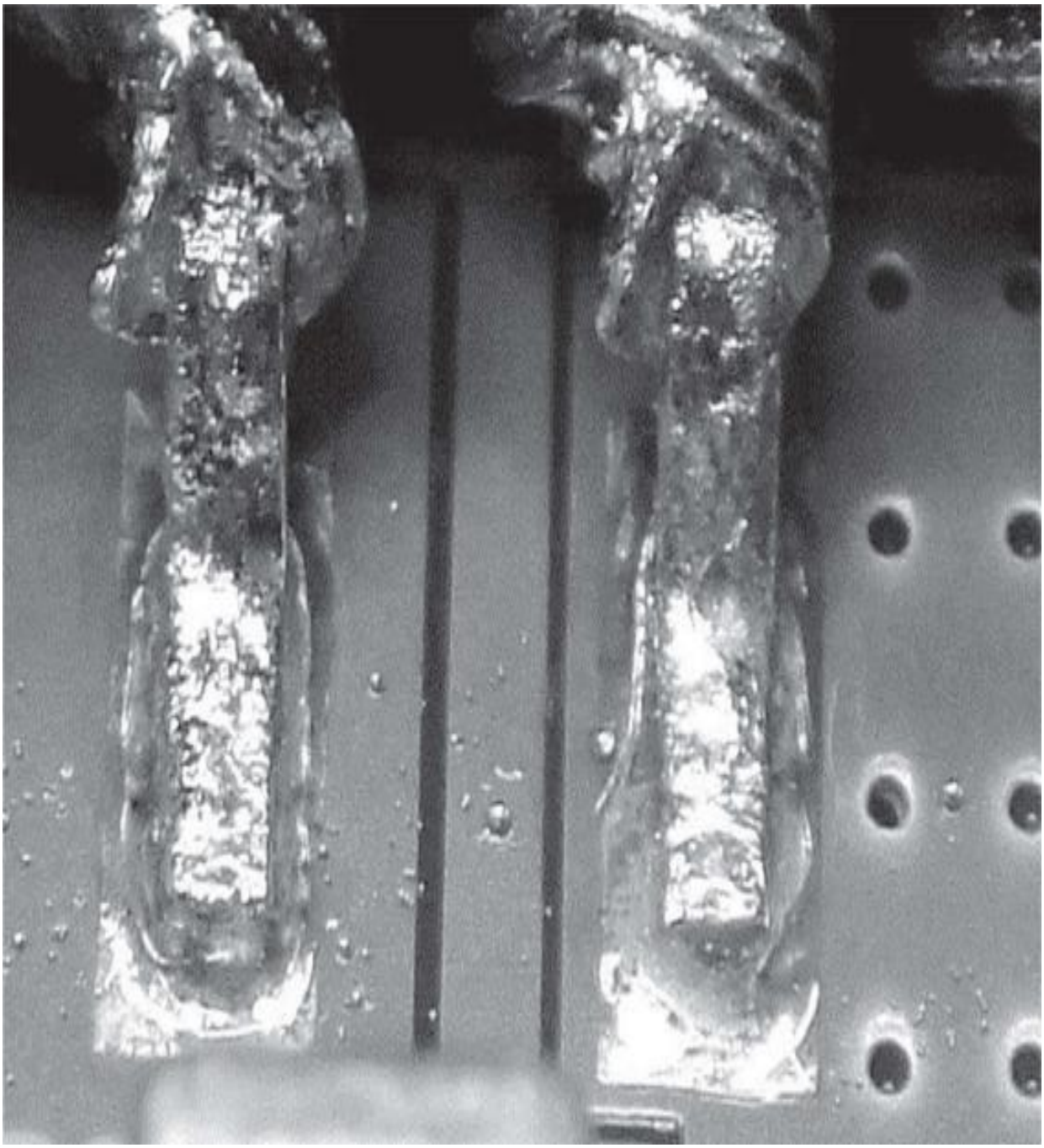


FIGURE 49.1 Solder balls on surface of PCB. Rapidly volatized solder paste constituents can result in explosive solder ball formation. (*Courtesy of K. Selig, AIM Solder*.)

The soldering time-temperature profile must be carefully adjusted to prevent excessive heating which can cause flux charring or “caramelizing,” reoxidation of fluxed soldering surfaces and solder joint degradation. Deterioration of the

circuit board (delamination, charring, etc.) or damage to thermally sensitive components may also result from overheating. Conversely, too low a temperature may result in solder opens or “graping”; a defect where the solder spheres have not fully melted and coalesced into a uniform solder mass. The spheres are either poorly soldered or sintered and look like clusters of grapes rather than a smooth, reflowed solder joint (Fig. 49.2).

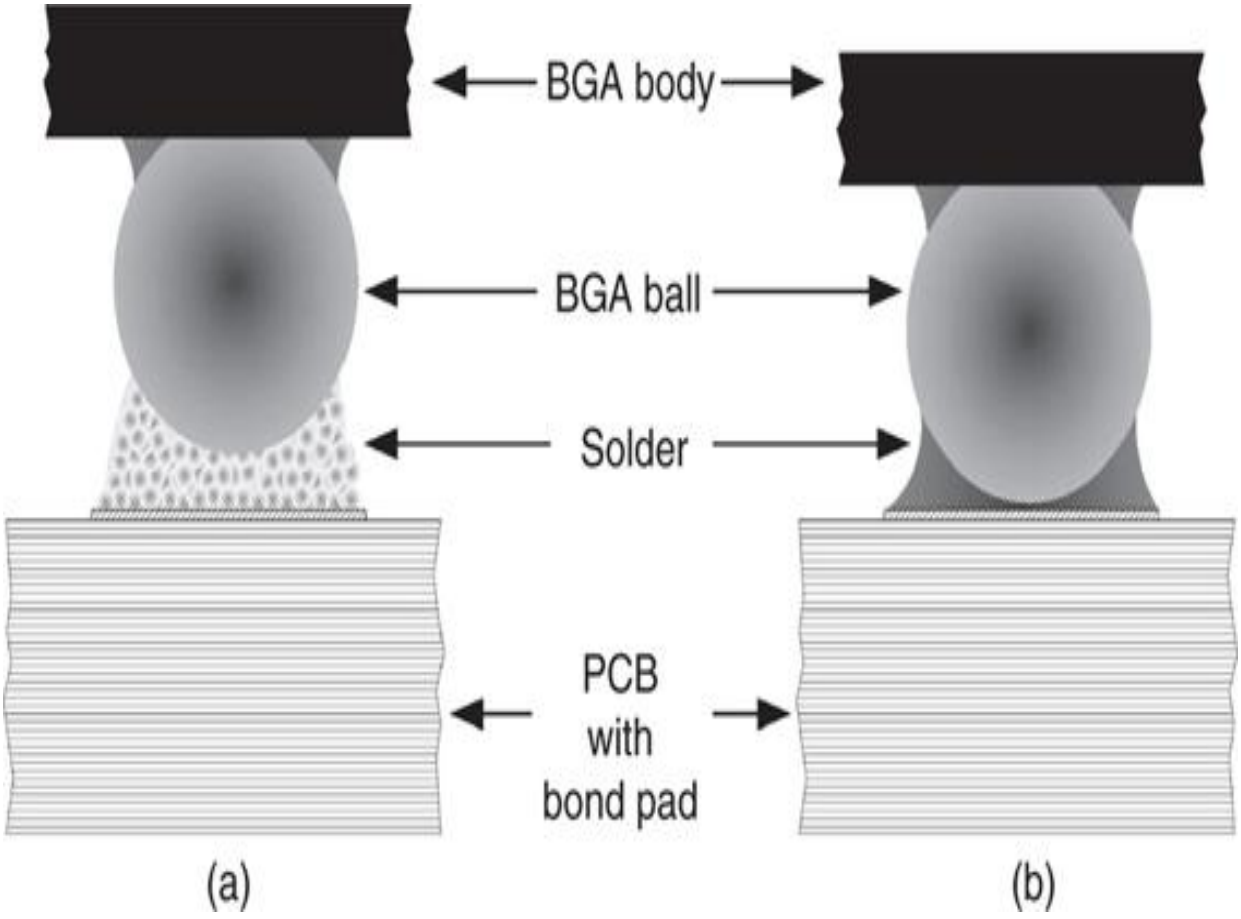


FIGURE 49.2 Illustration of the “graping” phenomenon. (a) shows “graping” where the solder balls of the solder paste have not coalesced in to a smooth and uniform solder mass. (b) is a normal solder joint properly reflowed. Smooth fillets bond the BGA ball to the PCB bond pad. “Graping” will result in a poor reliability solder joint.

Today’s reflow ovens are highly complex, precise and repeatable in performance. Accurate temperature and

precise control of the process temperature on all components is required for solder joint goodness.

49.3.1 Reflow Oven Subsystems

Even the simplest reflow ovens consist of several basic subsystems: insulated tunnel, board conveyor, heater assemblies, cooling, and venting (Fig. 49.3).

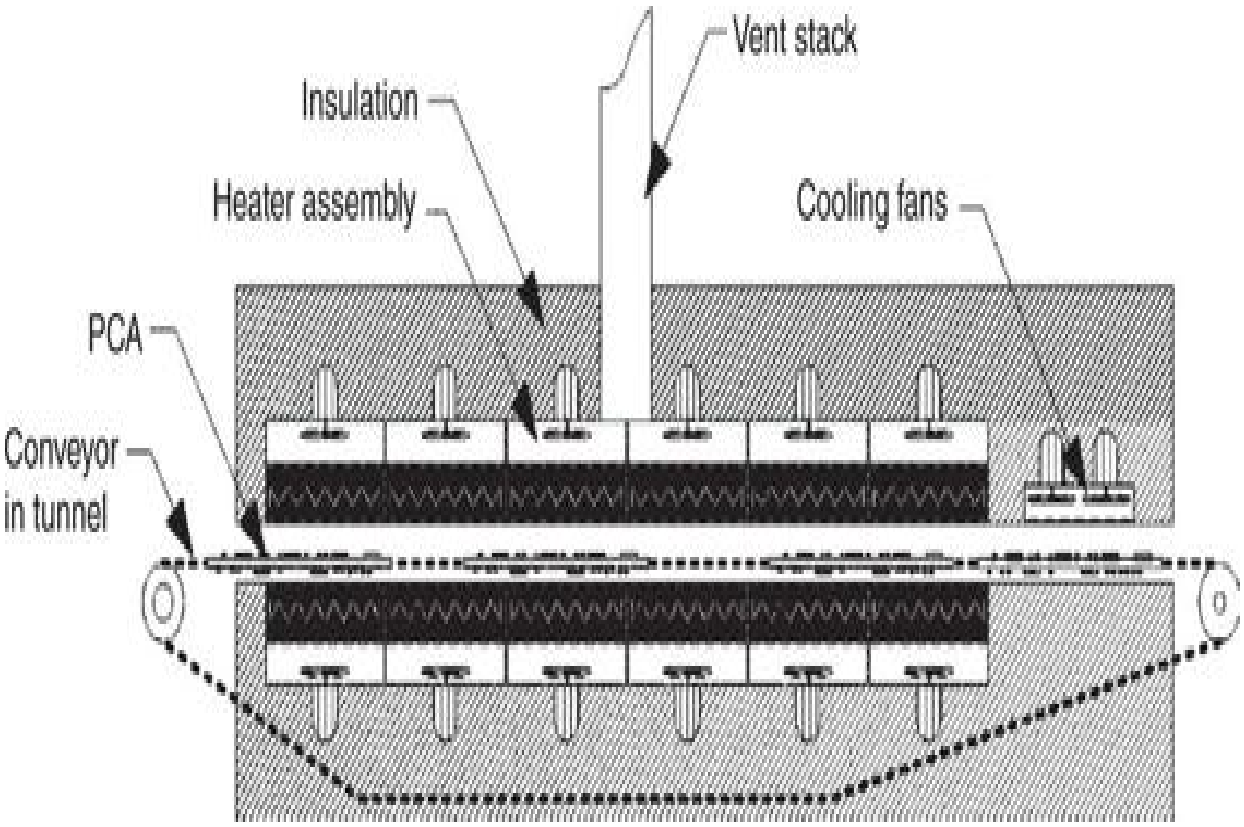


FIGURE 49.3 Cross-sectional view of reflow oven with top and bottom heater assemblies, cooling module, vent stack, insulated tunnel, and motorized conveyor.

Reflow ovens have reached a high level of sophistication, and there are many other items that enhance oven suitability for the manufacturing floor. Those items, beyond the basic reflow oven subsystems, are niceties, accessories, and gimmicks offered by oven manufacturers, not discussed

in this section; however, those subsystems previously listed are reviewed to impart an understanding of the basics of oven construction, operation and most advantageous configurations.

49.3.1.1 Tunnel. The tunnel is a thermally insulated passage through the length of the oven where the board is heated and cooled for a continuous reflow process. It serves to insulate the heaters and boards from the external (room) environment just as much as it is designed to preserve thermal conditions as prescribed by the process and demanded by the heaters.

Consideration of tunnel dimensions is critical for the reflow application. Short tunnel ovens may not permit an adequate profile for attaining requisite reflow temperature-versus-time profiles for larger, thermally massive PCB assemblies. Tunnel height dimensions must also be sufficient to accommodate the tallest components or component heat sinks. Tunnel width will limit the size of the board that can be introduced to it.

49.3.1.2 Conveyors. Boards are moved through the tunnel and past multiple heaters by a width-adjustable constant-speed conveyor permitting controlled and gradual pre-heating, reflow, and post-reflow cooling of the circuit board. There are two main conveyor systems used in reflow ovens: pin-chain and mesh belt. One is required and both are recommended for any reflow machine.

49.3.1.2.1 Pin-Chain Conveyor. The pin-chain conveyor, also known as an edge-hold conveyor, looks like a bicycle chain with a pin protruding inward from evenly spaced links, as shown in Fig. 49.4.

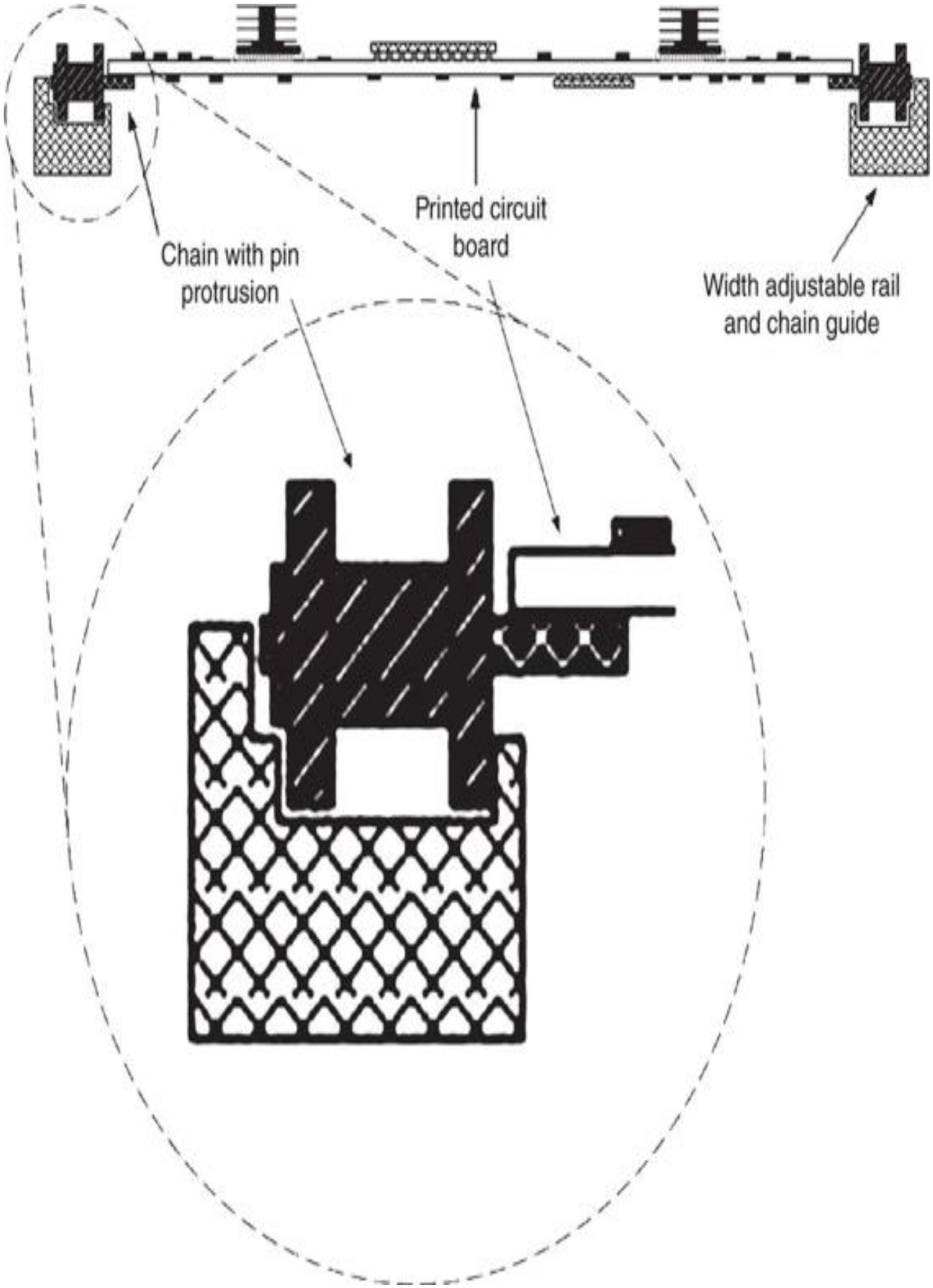

Printed circuit board
Chain with pin protrusion
Width adjustable rail and chain guide

FIGURE 49.4 Cross-sectional view of circuit board carried on oven pin-chain conveyor. Chain runs in guide slot to keep it positioned. PCB rests on pin-chain protrusion as illustrated.

There is one such chain on each side of the reflow oven. The circuit board rests on these pins on the inner aspect of the chains and is transported through the oven during the soldering process. The two chains are driven from a common motor, appropriately geared to ensure that the circuit board is conveyed through the oven evenly and to preclude angling and jamming of the board in the oven. Conveyor speed is adjustable and is one of the major variables of the reflow soldering recipe (time-versus-temperature) profile development.

Pin-chain conveyors are best for circuit boards with components on both sides since the circuit board is conveyed by its edges. This edge-hold method prevents misregistration of parts to be reflowed and also eliminates movement of or mechanical interference with previously reflowed components on the bottom-side of the board during transport through the oven. An edge keep-out area must be designed into the board such that there will be no pin-chain or component interference.

Thin, large circuit boards, may sag during reflow when held by the edges on a pin-chain conveyor. The sagging is due to thermal excursion above the glass transition temperature (T_g) of the PCB epoxy during the reflow process. T_g is the temperature at which a partially crystalline polymer will change from a hard structure to a rubbery, viscous state, as in the case of FR-4 and similar laminate materials used for PCB construction. The T_g of most circuit board laminates is generally below the peak reflow process temperatures of most solders. Sagging will be pronounced due to the fact that the board is unsupported at its middle as it surpassed its T_g during transport on the pin-chain conveyor. Copper ground and power planes within the board provide significant

support, but may not impart enough stiffness to counter this problem. Sagging alone or together with rail-to-rail non-parallelisms at process temperature can even lead to boards falling off the conveyor. Most of the major vendors in the reflow oven market have conquered the rail twist problem, but hot testing an oven with precisely toleranced test vehicles or even precisely milled aluminum plates should be performed prior to final acceptance of an oven. Board sagging can be mitigated, to some extent, by means of mechanical stiffeners affixed permanently or temporarily to the circuit board or by reflowing the board on a pallet. It should be noted that stiffeners and pallets affect the thermal mass of the board, making reflow more of a challenge. Care should be taken to ensure that the attachment of stiffeners or use of reflow pallets neither interfere mechanically nor thermally with components on the board.

Some ovens are sold with an accessory steel cable strung the oven length that is meant to serve as an antisag support or even a third pin-chain in the middle of the oven to contact the bottom of the PCB. A clearance (“keep-out” area) must be designed into the board or panel for the support cable or chain. The chain and its supporting rail may influence the reflow profile. The board will be cooler in the shadow of this additional thermal mass. In a properly designed oven, the pin-chain inflicts little thermal influence on the conveyor.

Some edge-hold systems have been known to impart a heat-sinking effect at board edges. To counteract this, some oven manufacturers have incorporated rail-heaters. It is best to avoid such systems because it adds further complexity to the oven and makes the job of process control all the more difficult. This should not be a problem with the conventional pin-chain conveyor because the pin-chain is only in point-contact with the circuit board. Thermal transfer through these contact points is very poor. Further, most of the newest reflow oven manufacturers have replaced carbon steel chains with stainless steel chains. Stainless steel has

better wear characteristics and is a poorer thermal conductor than other commonly available chain materials.

49.3.1.2.2 Mesh Belt Conveyor. Mesh belts used in reflow ovens are generally fabricated of stainless steel links. Some are wide open with large spaces, many centimeters from link to link. Others are more like chain-mail mesh (Fig. 49.5). Widely spaced links allow more air flow to the bottom-side of the board.

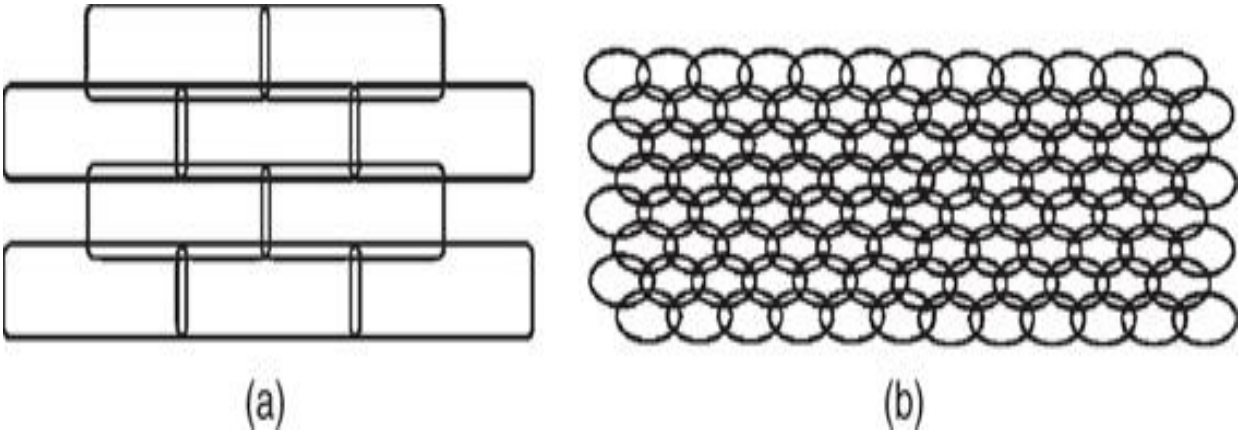


FIGURE 49.5 Mesh conveyor. A large space mesh belt (*a*) allows more air flow than the "chain-mail" mesh (*b*).

The mesh belt is close to the full width of the tunnel and traverses its entire length. Mesh belts offer exceptional versatility, as there is no need to adjust for various board widths and never a concern for board sagging or dropping, but they are best suited to single-sided circuit assemblies.

Preferred is a combination of conveyors with the pin-chain running above a mesh belt. In this case, redundancy can save boards, reduce maintenance time, and enhance personal safety. The mesh belt serves as either an optional means of conveyance for boards populated on a single side or as a safety net to catch a board that may fall off the pin-chain conveyor. Dropped boards are a rare occurrence if the pin-chain conveyor is set properly and the equipment, process, and materials are properly specified and controlled. If the mesh belt were not used with the pin-chain, any

dropped boards would smolder on the heater assemblies, resulting in the release of noxious fumes. Additionally, the heater or heaters affected could become encrusted with the decomposed board laminate, which may impact their thermal performance. If a thermocouple (sensing instrument for oven temperature control) is blocked by a fallen PCB, damaged or insulated by the laminate decomposition products, zone overheating may occur, causing oven damage, circuit board loss and manufacturing downtime.

If mesh conveyor is the only means of transport, any PCB with components on both sides of the board (double-sided assembly) would require a carrier (pallet) to prevent previously mounted components from contacting the mesh belt. The carrier adds thermal mass, so it is wise to minimize its thermal mass by removing unneeded material by perforating it to allow good air flow during the soldering process. Time-temperature profile development must include such a carrier.

49.3.1.3 Oven Heaters. Each heater's thermal output is sensed via a thermocouple, which is used to close the loop to the heater controller. In larger, production-worthy systems, heaters are located both above and below the plane of the circuit board and are at least as wide as the conveyor. Thermal uniformity across a 60 cm tunnel width can be better than ±2°C on top-of-the-line ovens. This is a function of tunnel insulation, heater performance, heater control, and convective mixing of the heated air or gas within the tunnel.

There are several heating schemes used in reflow ovens, the result of years of technological evolution. Focused infrared (IR) lamps have given way to secondary emission panel heaters and, finally, to forced hot-air convective ovens that are today's de facto industry standard.

49.3.1.3.1 Infrared Heater Types. Alternative IR heater types are shown in Fig. 49.6.

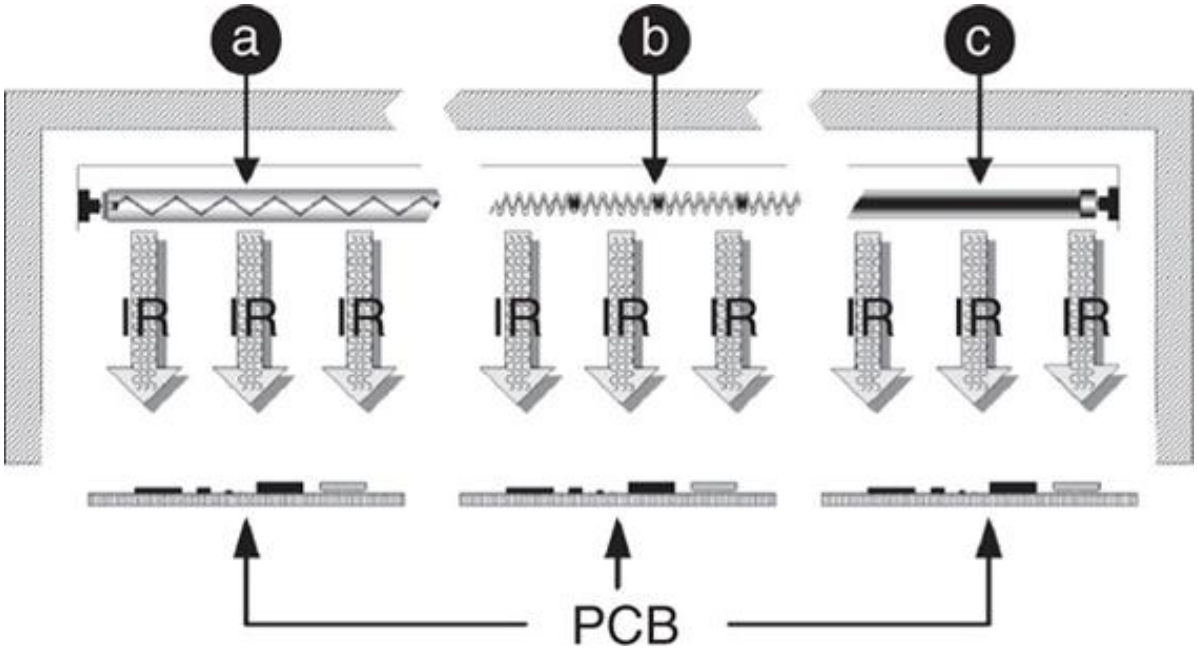


FIGURE 49.6 Three infrared heating schemes for reflow ovens: (*a*) IR lamp, (*b*) open resistance wire heater, and (*c*) resistance rod (calrod-type or cartridge heater). Note that each directly radiates the PCB.

Early SMT reflow ovens utilized focused and unfocused IR lamps, mounted in the reflow oven tunnel. These bathed the solder paste-coated circuit boards and associated components with a broad spectrum of photonic energy heavily weighted to the infrared (IR) end of the electromagnetic spectrum. The intensity of the IR and exposure time as regulated by the conveyor speed results in solder reflow. As the board travels beyond the last IR heaters at the exit end of the oven, the absorbed heat is lost to the environment and the solder solidifies. Alternatively, the molten solder may be actively cooled by fans to complete the solder joint.

Material such as plastic and ceramic component bodies, component lead and pad metallurgies, solder type, solder paste volume, PCB laminate and its lay-up, solder paste flux, and adhesives all absorb infrared radiation at different rates. Therefore, the direct radiative approach is known to cause overheating of some components and under-heating of

others. For this reason, direct IR heating is no longer the preferred method for reflow.

49.3.1.3.2 IR Panel Heaters. Better than direct IR heating is the secondary IR emitter panel (Fig. 49.7). Emitter panels are constructed of metal or ceramic platens heated either conductively via attached resistance heaters or by direct IR irradiation on the back side of the panel. They rely on longer IR wavelength radiation and natural air convection for heating the PCB, solder paste and associated electrical devices on the board.

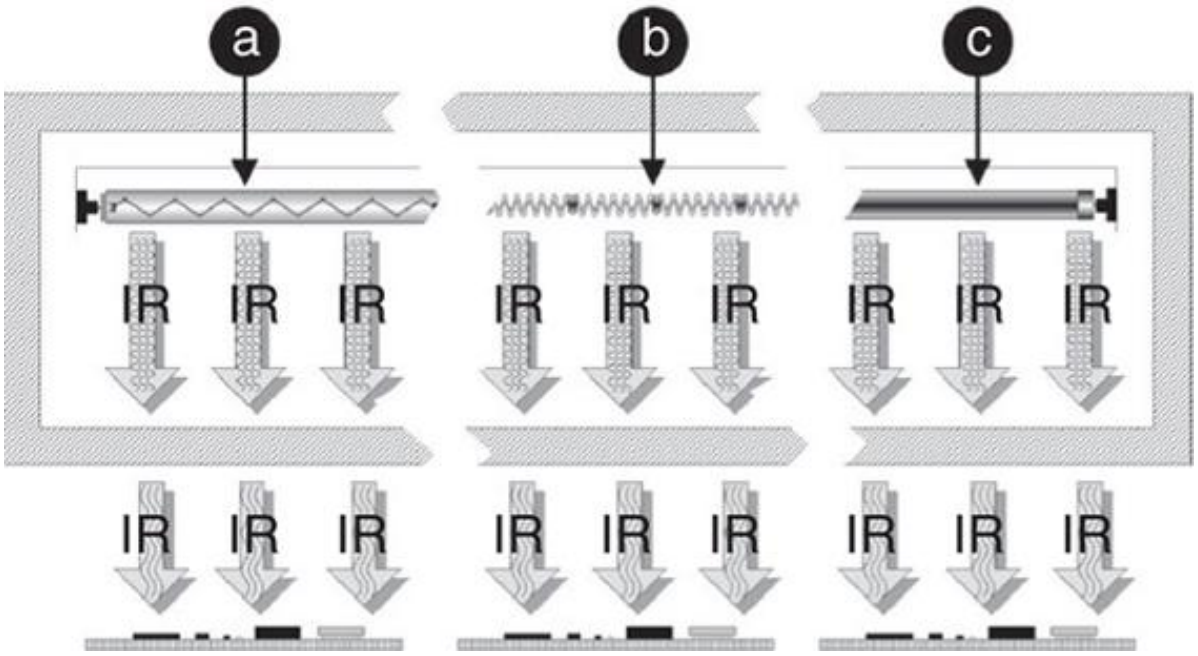


FIGURE 49.7 Secondary IR panels rely on radiant IR sources such as (*a*) lamps, (*b*) wire resistance heaters, or (*c*) heating rods/cartridge heaters. The primary IR impinges on a baffle and the absorbed short-wave radiation is converted to longer wavelength radiation which heats the circuit board. This imparts more even heating of the PCB and components during soldering.

During reflow, the circuit board is shielded from direct short-wavelength IR impingement. Instead, it is heated by blackbody emission of the heated platen, resulting in much longer IR wavelengths, slower heating rates, and more even heating—a significant improvement over the direct IR lamp oven reflow soldering method.

There are two variants of this method: convection IR oven and forced-air convection oven. The former relies on radiant or panel IR heating, but the air in the oven is stirred by fans to enhance uniformity of heating. However, techniques such as IR lamp, IR emitter, and combination convective units have been largely supplanted by forced-air convection ovens. In that technique the air is forced through the panel heaters at high velocity resulting in even oven temperatures and rapid heating response and control. Forced-air convection ovens are the mainstay of oven reflow and will be dealt with in a subsequent section.

49.3.1.4 Venting. Oven venting is required to remove harmful fumes from the oven tunnel. Too little venting and fumes will not be removed effectively. Too much exhaust will pull in too much room air through the tunnel entrance, tunnel exit, or both and may interfere with the oven's thermal performance. If nitrogen is being introduced to lower oxygen levels, too strong an exhaust draw will negate the effect of the nitrogen or make it difficult to control the oxygen level within the oven. A more detailed look at venting will be covered in a subsequent section.

49.3.1.5 Cooling. Just as important as heating the solder, the solder must be cooled to solid state before the board is handled. Otherwise, components sitting in liquid solder could move causing open- or short-circuits. Also, as a molten material such as solder solidifies and crystallizes, mechanical motion may perturb the solder's lattice structure. The resultant solder joints may be of poorer quality and lesser reliability. Some ovens rely upon passive cooling, whereas others have active cooling elements such as fans or chillers (fans blowing over actively cooled radiators).

49.3.2 Forced-Air Convection Reflow Oven

This is the preferred method for controlled, reliable reflow soldering. Dependent on heated air recirculated at high velocity in the oven tunnel, the only direct irradiation of the PCBs is by the longest IR wavelengths emitted by the hot surfaces within the tunnel and the bulk of the heating from the forced hot air.

49.3.2.1 Forced-Air Convection Reflow Module. Heating is accomplished primarily through heated air streams directed at the PCB's top and bottom surfaces. This method imparts greater thermal uniformity and controllability of the reflow process than any other reflow oven heating method. It precludes preferential absorption common to direct IR heating methods and resultant overheating of some parts and under-heating of others during the reflow process. Although the combination IR-convective method has helped in this regard, it is no substitute for the forced-air convection technology.

Top-of-the-line forced-air convection ovens have heating modules mounted above and below the board conveyor. Heating is accomplished by passing a high-velocity air stream drawn from the tunnel ambient over resistance heaters and through hot perforated platens. The stream of hot air is directed at board surfaces raising the temperature of the board, solder paste and placed components. The high-velocity air flows are baffled and regulated to impart a uniform temperature across the tunnel width. Each module is quickly heated and highly controllable. Several heating modules are set one after another along the length of the oven. It is typical to duplicate the top-side forced-convection module configuration on the bottom of the oven tunnel for even heating and controllability of the reflow time-temperature profile. Figure 49.8 depicts this arrangement.

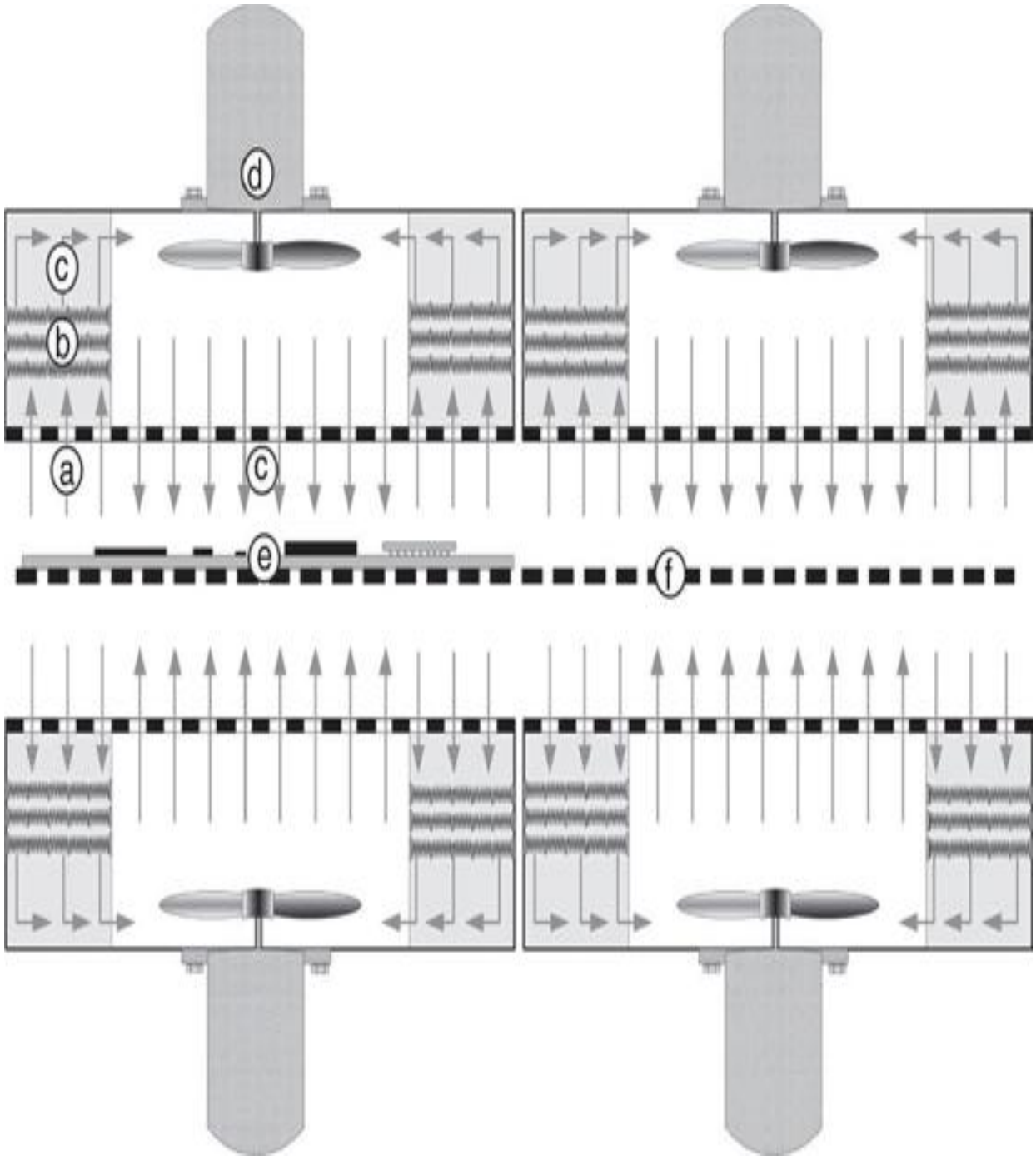


FIGURE 49.8 Forced-convection heating modules. Cooler air (*a*) is drawn across the resistance heater (*b*) by a fan (*d*). The heated air (*c*) is forced through a perforated plenum or multiple plenums tuned for even heat distribution to the PCB (*e*), which is riding on the conveyor (*f*). A second set of forced-convection heating modules is directed at the underside of the PCB. Several such modules are arrayed the length of the oven for precise thermal profile control.

49.3.2.2 Cooling. Some ovens rely upon passive cooling to bring the temperature of the PCB assembly below the solder liquidus point. In this case, the board traverses a region of the oven devoid of heaters. This is generally adequate for thin, low thermal mass boards. But multi-layer, densely packed PCBs necessitate active cooling to ensure that solder joints are solid prior to exiting the oven and before board handling. To this end, many ovens incorporate an area of active cooling after the last heating zone within the oven (Fig. 49.9).

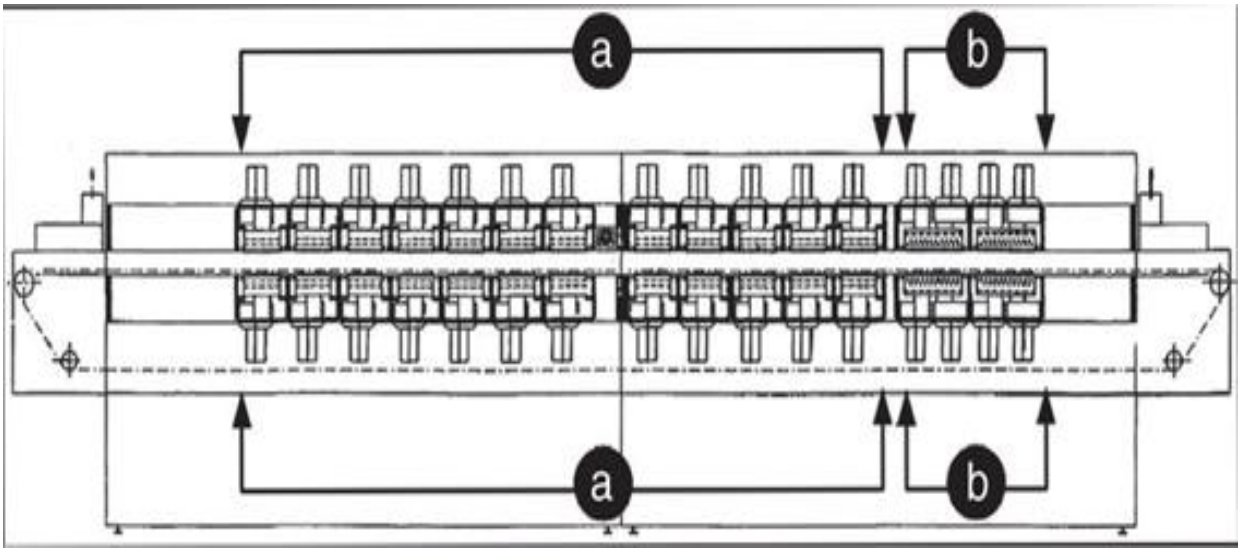


FIGURE 49.9 Forced-convection oven with 12 top and 12 bottom heating modules (*a*). Each module is independently heated and controlled. The last two top and bottom modules (*b*) are for active cooling of the soldered circuit board to ensure that solder has reached solidus before exiting the oven. In this machine, cooling zones are aided by fans blowing over water-cooled radiators. (*Courtesy of Heller Industries*.)

Active cooling comes in many forms. Some ovens use plastic “muffin” fans close to the oven exit. These must be kept on at all times to prevent overheating of the fan blades and the motor’s plastic fan support structures.

Forced-air cooling by fans is the most common. Fans can be deployed on top, on the bottom, or in combination for board cooling. Among the most exotic but the most efficient

is the water-to-gas heat exchanger found inside some ovens. This provides a stream of temperature-controlled cool air at the exit end of the oven for board cool-down and has distinct advantages for reflow systems using nitrogen atmosphere. It uses whatever process gas is in the oven, cooling it and redirecting it onto the circuit board mitigating the need for additional nitrogen for cooling. Also, it does not draw any additional air into the oven that might degrade the nitrogen atmosphere, and precludes the need for cooling fans outside of the oven adjacent to the tunnel exit. External fans create turbulence at the tunnel exit and may have a profound influence on the oxygen concentration in the oven's nitrogen-purged environment. Water-to-gas cooling is efficient, but it must be included in the reflow profile to ensure that thermal ramp rate is correct.

Some ovens use air rakes or air amplifiers to direct a flow of cooling compressed air or nitrogen at the board. In-oven cooling schemes often result in condensation of flux volatiles and flux decomposition products. As deposits build up on the coolest surfaces within the oven, they change the thermal transfer characteristics of the cooling system. This alters the thermal profile of the oven over a long period of time. Flux condensates may also drip onto circuit boards as they pass through the oven.

Nitrogen atmosphere ovens running no-clean solder pastes face the biggest challenge in trying to control these condensates. No-clean pastes give off abundant volatiles during reflow. Ambient air introduction or entrainment is kept necessarily low for precise control of the nitrogen ambient within the oven. Nitrogen volume is minimized to keep board processing costs reasonable. The result is low gas exchange within the oven's tunnel and little dilution of condensable vapors. Condensates build up rapidly on the cooler surfaces and are baked on over time and difficult to remove. Oven manufacturers have devised many elaborate schemes for flux condensate management. Gas stream filtration in and

around cooling zones, replaceable filters, cold traps, and cold fingers with self-cleaning burn-off cycles (kitchen oven-style) have been incorporated into some of the newest ovens. Several ovens have quick-change finned radiators that are swapped out, cleaned, and readied for the next change-out.

Many integrated circuit packages (ICs) and ceramic passive components have specifications for maximum thermal ramp rate. Exceeding this heating or cooling rate may damage die attach materials, crack packages, or otherwise alter electrical performance of the device. This is especially true of ceramic devices. Often the ramp is recommended in the range of 1 to 4°C/s. Additionally, some solders like Sn-Ag-Cu (SAC) require cooling rates in this range to allow for quick solidification and to discourage solder alloy segregation. Cooling too slowly encourages redistribution of alloy constituents and silver platelets, or needles can form that may detract from solder joint strength.

49.3.2.3 Venting. An often overlooked reflow oven subsystem is exhaust venting. This is most important from an industrial hygiene point of view, but it can also have a significant effect on the soldering process itself. During soldering, minute quantities of metal oxides accumulate in the oven atmosphere or coat oven tunnel surfaces. The dangers of prolonged exposure to micro-quantities of lead (Pb) or lead compounds are well documented. With the change to Pb-free materials, the risks are likely lower, but there should still be concern for inhalation of any metal or metallic compound particulates. As previously discussed, during reflow, solder paste volatilizes and releases flux reaction products. Since most solder pastes and fluxes are highly guarded proprietary formulations, the paste and flux vendors may neither accurately disclose the composition reagents nor report the decomposition products in the mandated Material Safety Data Sheet (MSDS). Additionally, if a PCB should fall off the pin-chain conveyor or a component

should fall through the mesh belt, it may land on a high-temperature surface—either the heater itself, or, in the case of forced-air convection reflow machines, the perforated baffles above the heater assembly. Either the PCB or plastic components mounted on it will overheat, decompose, and release unpleasant or even dangerous fumes. A properly designed and implemented exhaust system will mitigate these hazards.

A high-velocity exhaust may influence oven performance. Too much exhaust will cause a significant net flow of atmosphere through the oven. This may result in unwanted turbulence within the oven, upset intentional forced-convection patterns and make temperature regulation more difficult. If the exhaust is not constant and not damped for changes in outside wind speed or gusts, it may influence the soldering profile and induce process variability.

Some ovens are designed with one central exhaust flue; whereas others may be have an exhaust port near both the tunnel entrance and exit. A dedicated manometer or other vent sensor should be installed in each exhaust line to monitor setup and routine exhaust performance. Blast gates in the exhaust line permit flow adjustment. It is customary to mount vent sensors after the flow damping device. Follow oven manufacturer’s guidelines for exhaust requirements. Since the exhaust gases are laden with volatile materials, mostly from the solder paste, active exhaust systems should be checked routinely for performance. Impeller blades can foul because of the condensates from these cooling volatiles. Exhaust stack monitors should help pinpoint such problems. The smoke from a piece of smoldering cotton twine can be used to sense whether there is a net flow into or out of the oven. When venting is correct, there should be a lazy net flow into the oven at both the entrance and exit. Of course, the oven should be hot and fully operational for proper exhaust assessment. Similarly, it would be instructive to perform this test using hottest and coolest reflow profiles to

ensure that heater module settings do not affect the exhaust conditions for minimal net flow into the oven at entrance and exit. Once the exhaust properties are set, repeat the measurements with dummy boards in the oven and observe whether they have an influence on net flow. Fine-tune the exhaust flows and repeat testing as needed. Proper exhaust setting will help achieve consistency in oven reflow soldering and protect plant personnel from exposure to noxious chemical or particulates generated from the reflow soldering process.

49.3.3 Reflow Oven Requirements

49.3.3.1 Multiple Heating Zones. Reflow ovens are designed with multiple heating zones at the top and bottom along the tunnel length. Each heater or zone is independently settable and controlled to a different temperature for stable temperature control. Note that a zone here is the top and opposing bottom heater pair, as shown in Fig. 49.9. Multiple heater zones allow the required adjustment and shaping of the time-temperature soldering profile necessary for successful heating, activating of flux, reflow of solder paste, and cooling of the soldered assembly. The number of heating zones required depends on the thermal mass of the product being assembled and the necessary throughput; the more heating zones, the more controllable the reflow process.

49.3.3.2 Heater Independence. Zone separation—the influence of one thermal zone upon another—is also essential for controllable and repeatable reflow soldering. One heating zone set to 250°C should have minimal effect on an adjacent zone set to 200°C. There are no set rules for zone separation requirements; however, the greater the zone separation, the more controllable the process. Testing

this parameter prior to buying or deploying a reflow oven is necessary for proper process setup. To test, set one heater zone high and adjacent zones lower. Allow the oven to stabilize. Determine conditions that cause the higher temperature zone to influence the lower set-point zones. The lower set zones may rise in temperature above their set point; an indication that the hotter zone is causing an uncontrollable temperature influence on adjacent zone(s). In setting the oven for circuit board assembly, avoid the large differential zone-to-zone thermal conditions and stay within the range of safe zone separation as previously characterized. Overly aggressive oven venting may also influence zone separation, drawing too much room air into the oven's tunnel.

49.3.3.3 Temperature Distribution. Temperature distribution across the width of the tunnel determines the quality and uniformity of heating. Top-quality ovens have rail-to-rail thermal uniformity of about ±2°C, even for largest board widths. Such tight thermal distributions are necessary for controllable and consistent soldering.

49.3.3.4 Heater Responsiveness. Rapid response of the oven's heaters and accompanying thermal control circuitry are critical to oven performance. As a board or multiple boards pass through the oven, the oven's heat is absorbed by those cooler boards on their way to reflow. The oven has to respond to the net heat loss absorbed by the train of PCBs with their solder paste and components. The thermocouples built into the oven should sense the thermal impact on the tunnel's ambient and the net loss in temperature from the flow of product in the tunnel. Note: Boards should never be spaced too closely together, as doing so will fully segregate the top from the bottom heaters and alter oven performance. Testing should be accomplished to establish proper board-to-board spacing. The spacing is

dependent on line throughput requirements, thermal mass of the product design and effectiveness of forced-air convection and temperature control within the oven.

Board separation may be as small as a few inches, but the effects of board loading and spacing need to be determined empirically and checked to detect any impact on the process time-temperature profile. Assessment of new equipment ought to include load testing to ensure that the oven can handle anticipated process throughput and capacity. The oven's profile needs to be examined before, during, and after loading of the train of boards and compared to the performance with the same oven settings for a single board.

49.3.4 Elements of Reflow

The relationship of temperature with respect to time is of utmost importance in the oven soldering process. The settings for this relationship on the oven is referred to as the "reflow recipe" or "reflow profile." The profile will bring the PCB assembly to solder liquidus and back to solidus before exiting the oven. But it must be accomplished in a controlled manner and in accordance with the thermal requirements (maximum temperature and thermal ramp rate for heating as well as cooling) of solder paste, components on the PCB and the PCB laminate itself.

49.3.4.1 Profile Dependencies. The solder paste composition, circuit board lay-up (number of layers, thickness and quantity of copper traces and planes, PCB material), component types, component count, and the number of components per unit area on the PCB and PCB spacing within the oven will dictate or influence reflow profile characteristics. Oven performance such as heating characteristics (number of heater zones and responsiveness of each module) and repeatability of oven settings will

influence the reflow process and profile. Of course, of paramount importance is the attention to process detail of a well-maintained reflow oven by the process engineer.

49.3.4.2 Solder. The solder alloy chosen dictates the peak temperature and time required for reflow and wetting. It may also influence the post-reflow cooling rate chosen, as some solders, especially Pb-free compositions, have preferred cooling ramps.

49.3.4.3 Flux and Other Solder Paste Constituents. As discussed previously, solder paste is typically composed of three main ingredients: solder alloy, flux, and other materials added to help with rheological properties critical for solder paste printing on the PCB. The solder alloy dictates the peak temperature regime, whereas the flux and other paste components dictate the pre-reflow heating ramp rate. Heating too rapidly may prematurely dry out solder paste components. Overly rapid heating may cause the solder paste to spatter. Too little heat may not allow proper activation of the flux. There is no universal profile recipe for reflow for a given solder alloy. The solder paste manufacturer will provide guidance for the time-temperature profile for each solder paste formulation. The reflow characteristics should be consistent from batch to batch for a given paste formulation.

49.3.5 The Reflow Profile

There are four distinct steps in the reflow profile that must be accommodated by the reflow oven for successful soldering. Each step is tailored for the solder paste composition and accomplished in proper, controllable, and repeatable reflow equipment. A misstep at any of the four stages of reflow may result in product loss. Refer to Fig. 49.10 for this discussion on thermal profile.

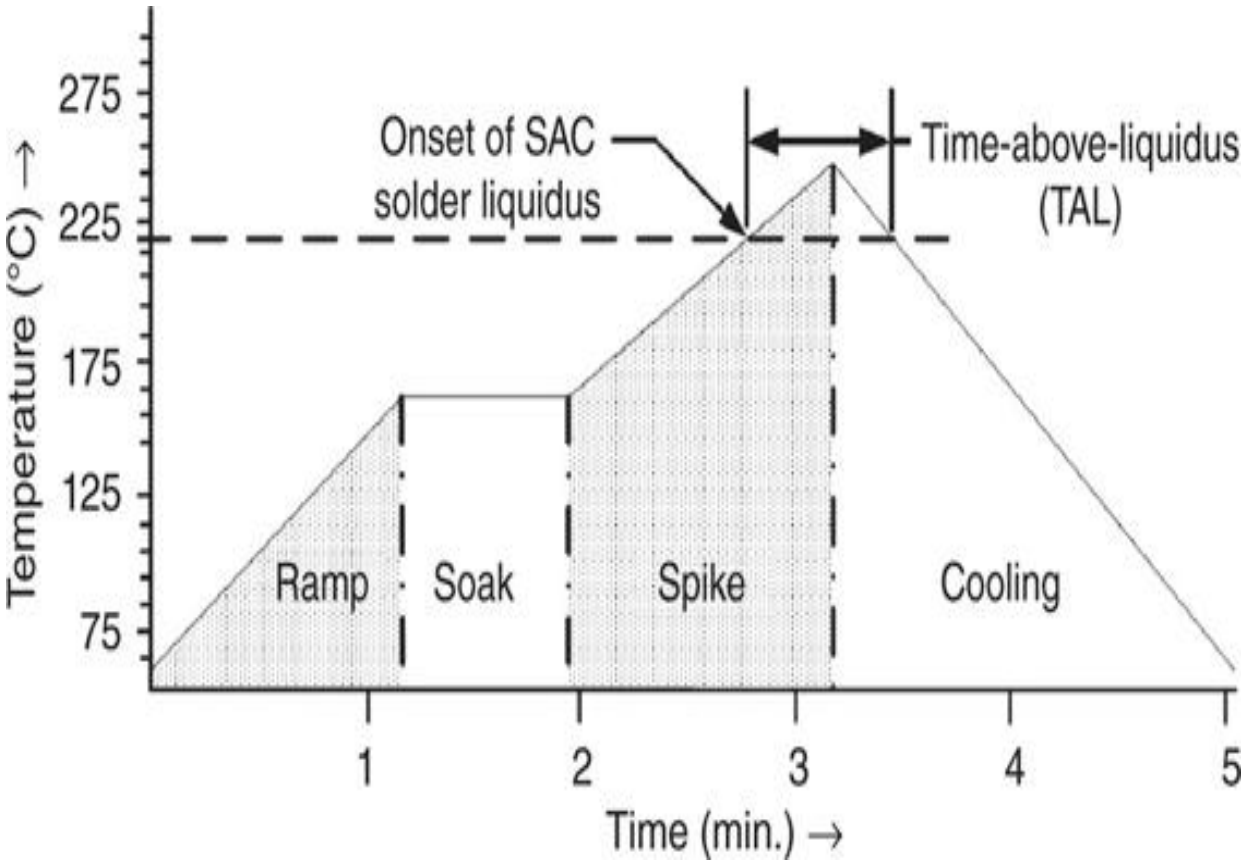


FIGURE 49.10 Schematic of a generic reflow profile for Sn-Ag-Cu (SAC) solder paste. Time-temperature values are not precise and are shown for illustrative purposes for a discussion of reflow soldering.

49.3.5.1 Initial Ramp. In this step of the reflow time-temperature profile, preheating of the boards, components, and solder paste is initialized. The solder paste begins to lose some of its volatile components and the flux becomes chemically active (activates). If the ramp gradient is too steep, volatiles will be given up too rapidly, boiling will result, and the solder paste will erupt spattering solder balls on to the PCB surface. This will result in decreased solder volume at eruption sites. The subsequent reduced solder volume may impair bond reliability. Unattached solder balls may bridge two closely spaced conductors and impart an electrical short circuit.

Overly rapid heating is known to cause component cracking. This is particularly true of ceramic components. To

be safe, restrict the ramp rate to between 2 to 4°C/s, but investigate component manufacturers' specifications as well as the solder paste vendor's recommendations for the maximum allowable heating ramp.

49.3.5.2 Thermal Soak. During this step, the solder, board, and components are further heated. The flux from the solder paste flows onto all metal surfaces in which it is in contact, continues to react away surface oxides, and also acts as a barrier to prevent reoxidation in the critical moments before the onset of solder liquidus and solder wetting (alloying). The soak is designed to provide the requisite time and thermal energy for the flux's prolonged chemical reaction with oxides and tarnishes on metal surfaces including on the solder itself.

49.3.5.3 Spike

49.3.5.3.1 Onset of Solder Liquidus. In this step, the solder undergoes a phase change from solid to liquid. The liquid metal solder wets onto fluxed metallic surfaces and flows along the component lead/PCB pad interface drawn by surface tension, capillary forces, and convective flows within the liquid metal. This is the essence of soldering and effective solder joint formation. Characterized by a rapid thermal rise, the spike's peak temperature is chosen to be well above the solder's melting point to ensure that all parts of the board, all components, and all solder paste deposits have surpassed solder liquidus onset.

49.3.5.3.2 Surface Tension Effects. While the solder is molten, surface tension effects draw component leads into best registration with circuit board pads if the component is light enough to float upon the molten solder. Passive devices (resistors, capacitors, inductors, etc.), most components with formed leads, and plastic or laminate ball-grid array packages (BGAs) self-align during this step. Solder surface tension is typically not strong enough to effect self-alignment

of heavy ceramic components such as ceramic ball grid arrays (CBGAs) and ceramic column grid array (CCGAs). Surface tension effects may also cause solder opens such as when small passive components “tombstone” (also known as “drawbridge”) because one end of the component reaches soldering temperature before the other.

49.3.5.3.3 Intermetallic Compound Formation. As previously discussed, intermetallic compound (IMC) formation occurs when the molten solder wets to metal surfaces of component leads and PCB pads. IMC thickness is dependent on the temperature and time especially when the solder is at or above liquidus. The longer the solder is heated, the thicker the intermetallic layer, and thick IMCs result in brittle bond lines and therefore degraded solder joint reliability. For this reason, overheating the circuit board during the spike should be avoided. Time-above-liquidus (TAL) should be roughly in accordance with the solder-paste manufacturer’s recommendation, which is typically 30 to 60 s, although there are no hard and fast rules for TAL. A longer TAL for some components may be evidenced on large thermal mass boards that are slow to heat and heat unevenly. In this case, some devices may overheat while others barely reach soldering temperature. Similarly, some component or board metallurgies may be slow wetting and a longer TAL may be necessary.

Some PCB finishes, such as hot air solder leveling (HASL) or reflowed tin on copper bond pads, possess a thin intermetallic layer between the applied surface finish and the PCB bond pads from the process at the PCB fabrication shop. During surface-mount technology (SMT) reflow, the additional reflow cycle will further its growth. Therefore, the TAL should be limited to minimize IMC but must be sufficient for good solder wetting.

49.3.5.3.4 Materials Degradation. During spike, board laminates, component bodies, etc., can degrade, so trials should be performed to ensure that all materials are

compatible with chosen reflow parameters. If plastic-bodied connectors are being applied during SMT reflow, make sure that the connector's normal contact force has not been jeopardized by distortion or softening of the connector body during the spike. Inspection of connector contact gaps before and after reflow and comparison to the connector manufacturer's specifications will provide clues as to whether the connector is truly compatible with the reflow process.

49.3.5.3.5 Cooling. The fourth and final stage of the reflow cycle is cooling. It is here that the board's temperature is lowered beyond that of solder liquidus prior to exiting the oven. Once again, recommendations for device heating- and cooling-ramp rates should be heeded. Most electronic packaging and board materials are reluctant to shed heat quickly. If the board is thick, the laminate, a relatively poor thermal conductor, will remain hot. It must be cooled to below solder liquidus prior to exiting the oven to preclude dislodging of any solder-wetted components or disturbing the solder joint solidification process. On the other hand, with the trends toward thinner circuit boards, slimmer components, and hot, fast-soldering profiles (to keep up with high-volume product demand), it is wise to ensure that the negative thermal ramp requirements are considered for this step also.

As mentioned previously, the solder paste manufacturer will provide recommended profile guidelines, but those are only a starting point. The process engineer must optimize the reflow oven profile with product profile boards and analysis based on actual product runs. Board profiling will be covered in a subsequent section.

Older textbooks and industrial references cite completeness of fillet formation and solder reflectivity as typical hallmarks of a good reflow process, but these are subjective measures that may not be true indicators of solder joint quality. As mentioned previously, overheated

joints will be brittle although they may appear to be well wetted. SAC and other Pb-free solder alloys have a naturally grainy-looking solid structure as compared to that of Sn-Pb, so a dull solder joint is not necessarily indicative of a poor solder joint. Tests such as tensile pull- peel, shock and vibration, thermal cycling, x-ray for solder void content, and metallographic cross-sectioning are much better means of assessing solder joint quality. There is yet another implication with the move to SAC solders. If not quenched quickly, this alloy is known to result in some constituent separation. Silver may precipitate out as platelets or needles. This can be minimized by using a fast cooling ramp. Check with component manufacturer's specifications so as not to jeopardize component integrity.

49.3.6 Successful Oven Reflow

Successful soldering is dependent on several factors including suitable, well-maintained and properly controlled reflow equipment; good-quality solderable parts; a thermally balanced board designed for the reflow process; a well-tested and reliable solder paste; a proven time-temperature profile; and good thermometry techniques.

49.3.6.1 Adequately Maintained and Controlled Reflow Equipment. The oven should have small thermal differentials across the width of the tunnel and should be capable of adequate heating and cooling ramps as well as appropriate zone separation characteristics. It should be stable for a given zone setting, not varying by more than a couple of degrees centigrade. Similarly, the conveyor speed should be stable, not varying by more than 1 to 2 cm/min.

49.3.6.2 Good-Quality Solderable Parts. The best reflow equipment, profiles, and solder paste will not make up

for inadequacies in part quality or restore solderability. Good solderable parts and boards are a must for successful reflow.

49.3.6.3 Coplanarity of Component Leads. Coplanarity of component leads, BGA balls, or CCGA columns is a must. All leads on a component should share a common seating plane within the specified tolerances associated with the component vendor's specification. The coplanarity requirement also depends on the stenciled solder paste height and paste deposit uniformity, as the solder paste accommodates some small differences in lead-to-lead coplanarity both as a paste and also as the solder assumes the characteristic dome shape upon melting.

49.3.6.4 Component Storage. Extended storage should be avoided and parts should be kept cool and dry prior to use. Sufficient quality control methods should be established to ensure that the solder and components leads are solderable. Plastic molded parts such as plastic quad flat packs (PQFPs) and plastic ball grid arrays (PBGAs) can absorb moisture from the atmosphere over time. When moisture-laden plastic packages are subjected to reflow soldering, the entrapped vapor may expand to the point where the package fractures, often damaging the silicon die and associated wires internal to the package. This phenomenon is commonly known as "popcorning" throughout the industry. Ensure that plastic packaged components are stored in unopened bags as supplied by the component vendor until time of use. Once the components are removed from the manufacturer's packaging, follow IPC/JEDEC guidelines[1] for useful shelf-life in the unbaked state and any bake-out requirements prior to soldering.

49.3.6.5 Board Design for Oven Reflow Soldering. Thermal balance of the board design is important for reliable and adequate reflow. Ensure that a

design for manufacturing (DFM) review of the board has been done and that thermally massive components are distributed over the board and not relegated to one portion of the PCB. Also, it is desirable to distribute smaller components rather than to create component fields to permit uniform thermal balance across the board. Components should be spaced adequately to prevent shadowing of smaller devices on the board by larger, neighboring components. This is particularly important in IR ovens without the forced-convection option. If the oven is characterized by poor uniformity across the tunnel width, the board should be oriented, if possible, to take advantage of the imbalance; that is, the board edge with greatest thermal mass should be aligned to the oven edge with the highest recorded process temperatures. Component placements should be designed far enough away from board edges to preclude mechanical interference with the pin-chain conveyor. Design in enough edge clearance tolerance to accommodate board movement on the pin-chain or variations in pin-chain length from machine to machine.

49.3.6.6 Paste and Profile. The profile provided by the solder paste manufacturer is only a recommended starting point that needs to be optimized for the reflow conditions and process time requirements. Solder paste with finer solder particles are more troublesome to flux owing to their greater total surface area and corresponding greater surface oxide volume per unit volume of solder. It is important to limit exposure to high temperatures and particularly time above liquidus, as it is in this regime that the intermetallic layer growth is most vigorous. The thicker the intermetallic layer, the more brittle and less reliable the solder joint will be.

49.3.7 Good Thermometry Techniques

Understanding the thermal impact of the oven on the board and the board on the oven is critical for a controlled and reproducible reflow process. Thermometry is the only practical method for validating these influences by means of oven profiling. Oven-and-board interactions are explored in this pre-soldering step and the oven is adjusted for proper time-temperature profile of the PCB with the parts to be soldered. Some of the most important process points determined through board and oven profiling are

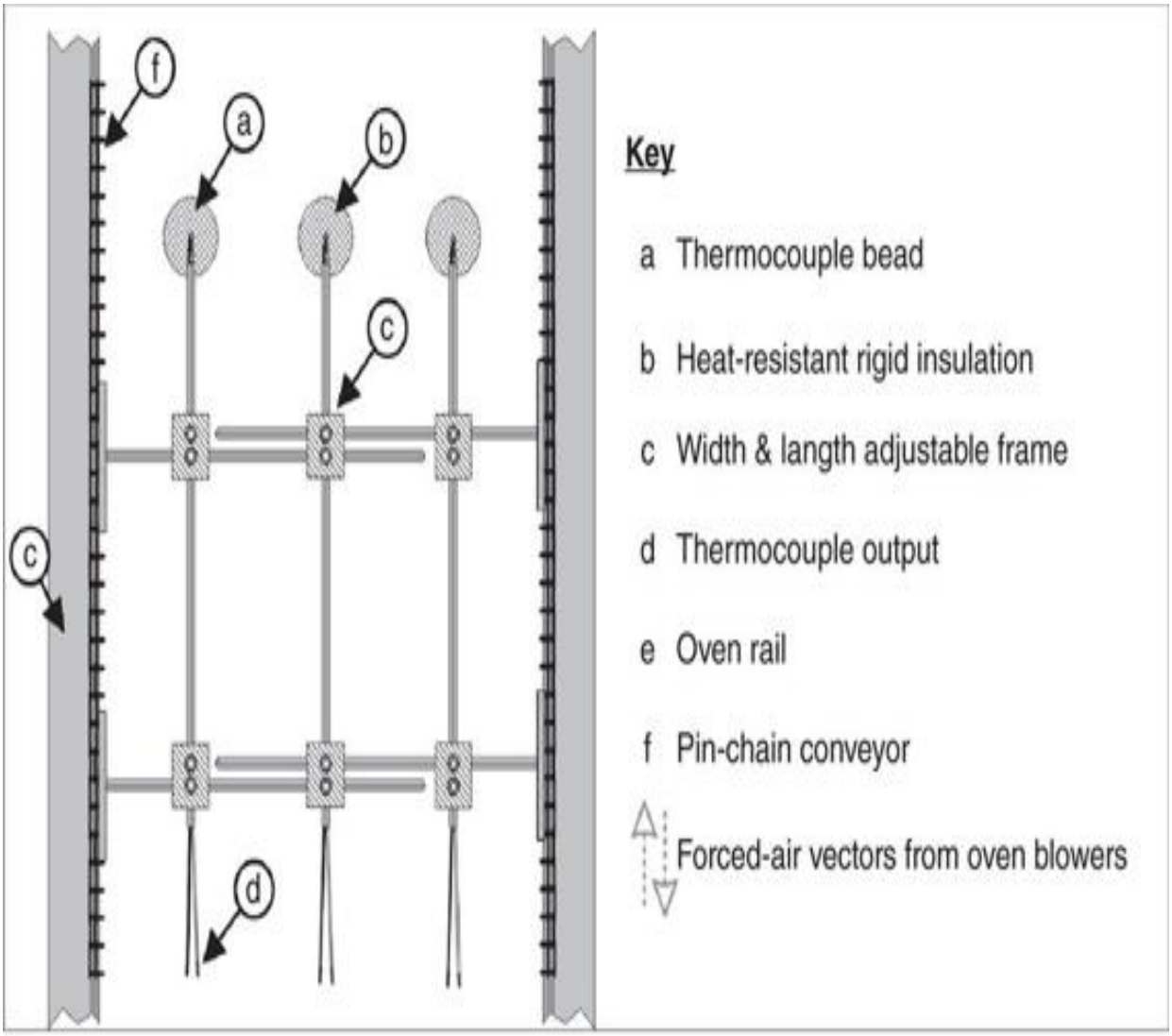
- Ensuring heating-cooling ramp rates are within the recommended bounds prescribed in surface-mount device (SMD) component and solder paste specifications
- Peak process temperature and duration
- Dependency on the heater types, quantities, cooling methods on board, and component materials
- Conveyor speed
- Heat distribution along the oven's width
- Heating characteristics of the PCB and the SMD components upon it
- Rate at which the oven reacts to the board's presence

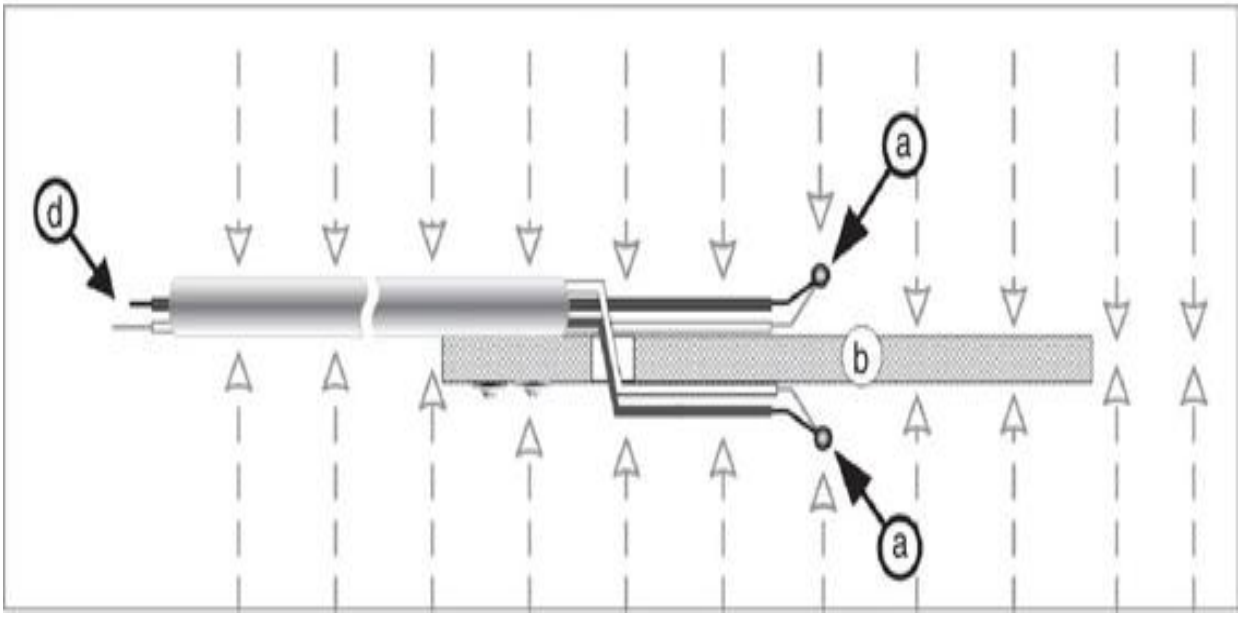
49.3.8 Product Profile Board

The only way to assess the impact of reflow variables as listed above is to accurately gauge the thermal environment in the oven in the presence and absence of the board or boards. Most process engineers trust their favorite profiling board to determine the health of their reflow oven or assess the performance of a new oven prior to purchase. The profiling board is simply a thermocouple-instrumented

product board or test vehicle that is run through the oven for the purpose of determining the oven’s effect on the board for given heater and conveyor speed set points. The thermocouples trace the temperature profile of the oven as seen by the component lead or package as the board is conveyed through the oven for reflow. However, reliance on a product board to determine oven performance may mask some inherent problems with the reflow oven. If the board is not thermally balanced in terms of component placements, component mass or board inner layers, it may not be able to detect a strong transverse (rail-to-rail) thermal differential. Also, when the same board is sent through the reflow process many times, the laminate starts to degrade. If layers separate or if thermocouples start to lift, false readings may result. It is for these reasons that a balanced oven diagnostic profiling device should be made and run to assess oven performance independent of a product board. The oven diagnostic board is not a direct replacement for the product profiling board. The product profile board is used to verify that the critical sectors of the board and device leads are heating per set profile. Thermocouples for this board should be deployed at the leading edge, trailing edge, center, and sides, with the thermocouple beads ideally embedded within the solder joints of disparate component types. Additional thermocouples can be placed on unusually massive components as well as on adjacent smaller components to determine whether a large component is thermally shadowing its diminutive neighbor. The number of thermocouples deployed depends on the package types, known oven characteristics, board thickness, board layout complexity, etc. The following sections describe good thermometry practices and the oven diagnostic board, as well as some of the thermocouple measuring innovations that are now routine for large-scale mass reflow manufacturing operations.

49.3.8.1 Oven Diagnostic Board. The oven diagnostic board can be a very simple or a rather complex device. Its job is to probe the normal operating conditions of the oven and determine variations in the oven and whether all the heaters and forced-convection fans are working properly. It is useful in assessing not only the oven's time-temperature profile parallel to the tunnel's long axis, but also perpendicular to it at the rail edges. The data recorded from this board are not necessarily translatable to the establishment of a product time-temperature profile, but are more suited to determining oven performance. The diagnostic board, whether a product board or a separate test board or other device, should be thermally symmetrical, made from a low thermal conductivity material, or best, a rigid thermal insulator. It should also be of low thermal mass. Attached to this are thermocouples mounted top-side and bottom in an evenly spaced array across the width of the material. They should be mounted close enough to the conveyor rails to gauge their influence on the thermal profile. Thermocouples should be identical in wire gauge, bead size, length and spacing from the insulating material. Furthermore, they should also be mounted slightly off the insulating material such that the heated oven environment can freely swirl around them. Measuring with such a device provides a true picture of the oven's thermal environment. Figure 49.11 shows a schematic of one such device developed for oven diagnostics.


f
a
b
c
c
d
Key
a Thermocouple bead
b Heat-resistant rigid insulation
c Width & langth adjustable frame
d Thermocouple output
e Oven rail
f Pin-chain conveyor
Forced-air vectors from oven blowers


d
a
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a

FIGURE 49.11 Schematic plan view and detailed side view of an adjustable oven characterization fixture (oven diagnostic tool) composed of pairs of thermocouples, shielded from one another by a rigid, heat-resistant insulator. The thermocouple positions are adjustable in width and length for investigating temperature distribution along the tunnel width.

49.3.8.2 PCB Thermometry. Knowledge of good thermometric practices and thermocouple use is critical to acquiring accurate and useful board time-temperature profiles and oven thermal performance information.

49.3.8.2.1 Good Thermocouple Practices. A thermocouple is composed of two atomically disparate metals or alloys in contact with one another. The wires are joined by twisting them tightly together or preferably by welding (Fig. 49.12*a*, *b*).

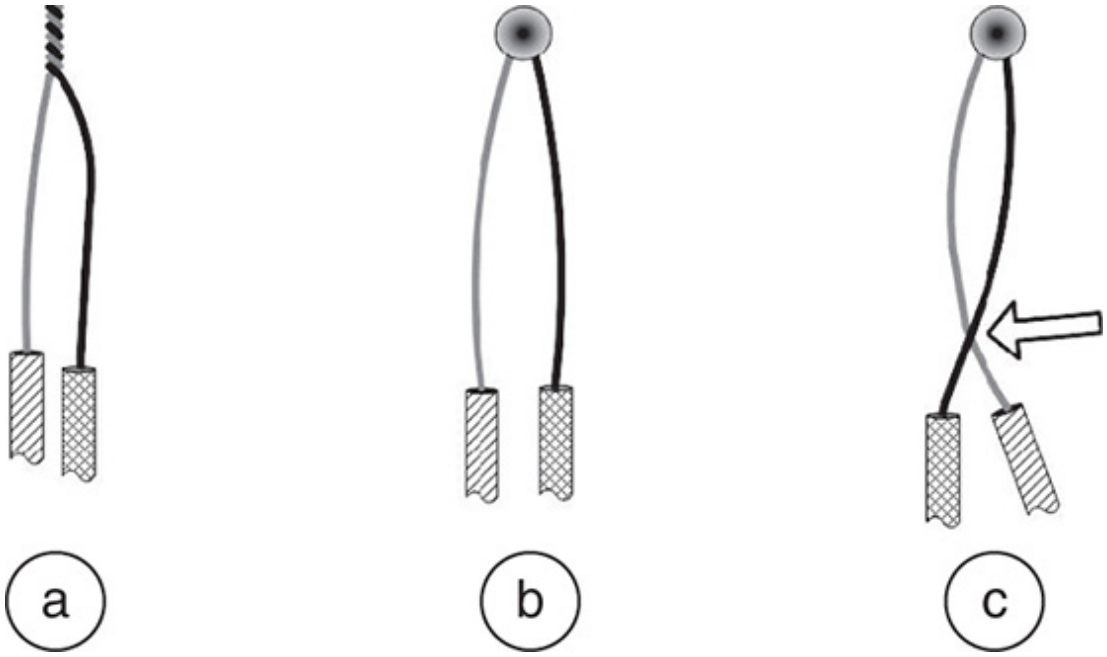

FIGURE 49.12 Thermocouples: (*a*) twisted couple; (*b*) welded couple; (*c*) welded couple with an inadvertent couple (see arrow).

Once joined together, the atomic difference between the two metals results in an electron flow and a measurable voltage which is temperature dependent. It can be calibrated and used for accurate temperature measurement.

Thermocouples are simple to make. The two different wires need only touch one another at a single, discreet point to form the couple. This simplicity in construction can also be problematic. If the two wires inadvertently contact (Fig. 49.12*c*), thermocouple output will be related to the temperature at that accidental juncture rather than at its termination. In the case of a thermocouple sandwiched between a component lead and PCB pad (Fig. 49.13) and an accidental junction formation nearby, the thermocouple will register the temperature of the oven air plus any thermal conduction along the thermocouple rather than the true temperature of the combination of component lead, solder and the PCB at that intended sensing location. Since the oven air temperature is generally much hotter than the PCB traveling through it, the resultant soldering time-temperature profile (based on the false thermocouple reading) may be cooler than desired and cold (under-reflowed) solder joints may result.

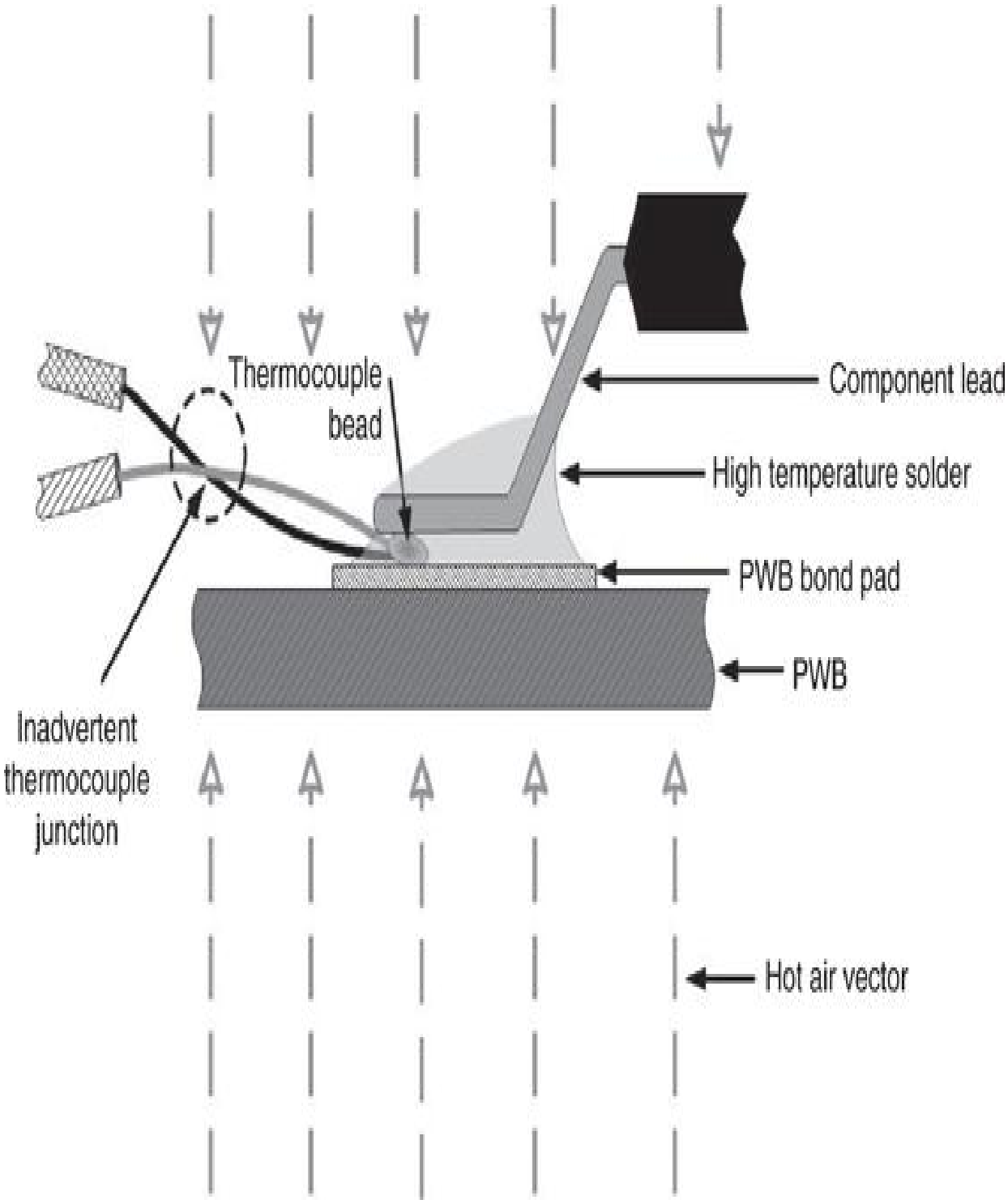

FIGURE 49.13 Arrows indicate impinging forced-convection flows from oven blowers. The inadvertent thermocouple junction (crossed wires) will record oven local air temperature rather than the intended measurement target—the solder joint area. The component lead is covered in high-temperature solder so it will not melt during reflow profiling.

49.3.8.2.2 Welded versus Twisted. A thermocouple wire pair should welded at its end to preclude noise-induced measuring errors from intermittent wire pair contact. Small, inexpensive bench-top welders are available for this purpose. Ideally, the two halves of the thermocouple pair should touch at only one point—that closest to the area desired for temperature measurement. The welded pair has a significant advantage in that the resulting weld bead can be made small and uniform in shape. As a rule of thumb, the weld bead diameter can be made as small as about 1.5 times the diameter of the individual wires that compose the couple. If constructed properly, the temperature will be sensed only at the weld bead. Regardless of whether the couple is made or bought, always check with a magnifier or microscope to ensure the integrity of the bead and that couple wires are only touching at the bead and not at any point below it. During manufacture of a thermocouple assembly, the usual practice is to twist the thermocouple wires together prior to welding. Upon welding, the twisted material will fuse and melt back to form the bead. After welding, it may be necessary to untwist the pair just behind the bead. While doing this, inspect the integrity of the bead to make sure it is a good metallurgical joint. Note that many thermocouple materials are brittle before welding and are even more so afterward.

49.3.8.2.3 The Most Common Couple. The most common thermocouple used for PCB profiling application is the “K” type, Ni-Cr/Ni-Al (chromel-alumel) couple, as it possesses a thermal measurement range best suited for soldering of circuit boards regardless of solder alloy type.

49.3.8.2.4 Measurement Instrumentation. There are two main devices in use for measuring the output of the thermocouple: the reflow tracker and digital (electronic) thermometer. The latter is a primitive device which uses a long thermocouple attached to a single point on the PCB and does not provide the wealth of information afforded by the

reflow tracker. Digital thermometers have an output that must be recorded by hand or connected to a time-based chart recorder.

Preferred is the electronic reflow profiler or tracker, an electronic package that can not only output the time-temperature plot of multiple thermocouples but can also make certain assessments of the data, such as heating ramp rate, preheat time, time above liquidus, cooling ramp rate, and other attributes. Tracker systems are computer-based and battery-powered and can generate detailed reports and graphs of a reflow cycle. They are made to travel through the oven with a profile board. As such they are designed with a thermal protective cover that protects their battery-powered electronics to survive the rigors of the high-temperature environment of the reflow oven. The reflow tracker eliminates the need for excessively long thermocouple wires as necessitated by the digital thermometer. Long thermocouples can result in resistive losses and thermal heat-sinking effects both of which detract from the accuracy of temperature measurement.

Tracker sampling rate can be selected to record the circuit board’s attached thermocouples at short time intervals (several times per second) for the entire trip through the oven’s tunnel. When the tracker emerges from tunnel, it is removed from its protective thermal barrier and docked to a computer. The data stored in the electronic tracker are uploaded to the computer, conditioned, displayed and or printed for analysis. The user defines the reporting format, including the type of data sought, thermocouple plots, and other relevant, run-related data. Some systems are capable of making predictive corrections to the profile based on tracker measurements and oven settings. This can further enhance the ease of adjusting a complex multizoned reflow oven to meet the requirements of a particular job. Whether a simple or complex model is selected, the reflow tracker is invaluable for setting up the oven and checking process

repeatability. Some reflow trackers even output temperature by a wireless transmitter so that measurement data can be observed in real time.

When an electronic tracker is used, its presence in the oven may have an impact on the resulting profile data by affecting the local aerodynamics within the oven. The trackers also have thermal mass, but all trackers are sold with an insulating cover to protect their electronics. It is best to check the influence of the tracker's presence as it traverses through the oven tunnel. To do this, ensure the oven has warmed to a steady-state operating condition, run the profile tracker with the tracker a fixed distance behind the profile board. Note that the tracker is usually placed to follow the board in reflow. Were the tracker to precede the thermocoupled profile board, it might cause the heaters to ramp up as the oven attempts to compensate for the thermal mass of the tracker or compensate from the disrupted or deflected air flow. Although that is what happens during a reflow cycle as a cooler board enters a heated zone of the oven, the oven would attempt to adjust for the board's thermal mass. The added thermal mass or disruption of the air flows from the profile tracker would not be a factor in the normal reflow process. Rather than assessing the reflow tracker effect on the profile, keep the tracker approximately one board length or slightly more away from the instrumented profile board, to eliminate tracker influence on the measured profile.

49.3.8.3 The Profile Board. The profile board is the keystone for any soldering process. It is a board loaded with its complement of appropriate components. Thermocouples are attached to critical locations to ensure that proper soldering temperatures are reached during the bonding cycle. Typically thermocouples are embedded under BGAs (innermost joint and outermost joint) and on fine-pitch device leads and even on some passive components to

ensure that that all parts are receiving enough heat without significantly overheating or under-heating other parts. Sometimes it is impossible to achieve the perfect balance, and in such cases the thermal advantage is given to the area array components (BGAs, CCGAs, etc.) to ensure good soldering beneath while slightly overheating the lighter components.

It is good practice to attach thermocouples to components on the leading edge of the board, the trailing edge of the board, the sides, and the middle. It may take more than one trip through the oven to collect all the data for all these locations and to get a good picture of the thermal effects of the profile on the various components on the PCB.

There is no substitute for a profile board. Some have tried weighing the board for an estimate of thermal mass. Generic profiles with overly hot peak temperatures have been applied and other supposed shortcuts have been attempted. None of these approaches have been proven to be reliable or successful over a range of board types. There is no replacement for preparation and proper thermal assessment with a profile board.

Typically for oven reflow soldering, one profile board is prepared for the secondary-side reflow profile (on which only secondary-side components are mounted), then another for primary-side reflow profile (in which both secondary- and primary-side components are mounted). Another board is prepared for wave soldering (all SMDs loaded plus PTH parts). These boards also double as rework profile boards.

It is wise to attach thermocouples to power and ground pins if that information is readily available. These connection points are the most thermally challenging points for a particular device. This is especially true on thick motherboards where there may be multiply interconnected, thick ground, or power planes embedded within the board. Thick copper planes are thermally massive, slow to heat and

slow to cool because they are somewhat insulated by the PCB's epoxy/glass lay-up.

Always allow the profile board and the reflow profile tracking instrument to cool to room temperature before attempting another profile check. Cooling with a fan greatly decreases the wait time.

49.3.8.3.1 Thermocouple Deployment. The size and position of the thermocouples is critical for accurate and reliable thermometry. There are many methods for securing the thermocouple bead to the PCB and some simple rules for proper thermocouple use:

- The thermocouple junction (the bead) must be in contact with the object to be measured.
- Each of the thermocouple legs must be kept at the same temperature.
- There should be only one junction (the bead) between the two legs of the thermocouple as mentioned previously.
- The measuring technique must not interfere with the outcome of the measurement.
- The thermocouple bead must be in intimate contact with the lead and pad combination of the solder joint to be measured. Therefore, the thermocouple bead should be inserted between the device lead and the circuit board bonding pad or as close to it as possible. Flattening the thermocouple bead also helps in positioning it between lead and pad. Flattening can be accomplished with smooth-jaw pliers, a smooth-jaw vise or a hammer.
- After flattening the bead, check to ensure that it is neither cracked nor broken.
- It is good practice to tailor the size of the thermocouple wire and, thus, the bead, for the scale of the solder joint to be measured.

49.3.8.3.2 Preparing the PCB for Thermocouple Placement. For BGAs and other area-array devices, it is necessary to drill a small diameter hole through the board and into the BGA ball or column. This procedure is done with a fine drill bit slightly larger (~0.25 mm) than the BGA ball. The drill bit should be kept short (slightly longer than the board plus ball thickness) to avoid breaking the bit and also to gauge the drill depth. Drilling on a drill press rather than with a hand drill will also serve to minimize breakage and improve positional precision.

It is helpful and easiest to drill the thermocouple hole locations for BGAs or other area array devices before populating the profile board with any components. Doing so allows the board to sit flat on the drill press table since there are no mounted components on either side of the board. After drilling, the board can be assembled (printed, SMD components placed and reflowed) using an overly hot thermal profile as this is only a mechanical assembly. It is critical that there are solder joints for each and every component on the board but solder joint quality is not important here.

Once assembled, the pre-drilled holes can be cleared of any solder by using a hand-held twist drill bit the same size as used for the original hole. The hole is deepened to extend into the BGA ball in preparation for thermocouple insertion. As long as the hole diameter is kept small, there is no need to add solder to retain the thermocouple within the BGA. If the hole is kept slightly larger than the thermocouple bead, the radiated air temperature within the hole and around the thermocouple bead should be the same as the ball temperature. Of course a very fine thermocouple is needed for this application (Fig. 49.14).

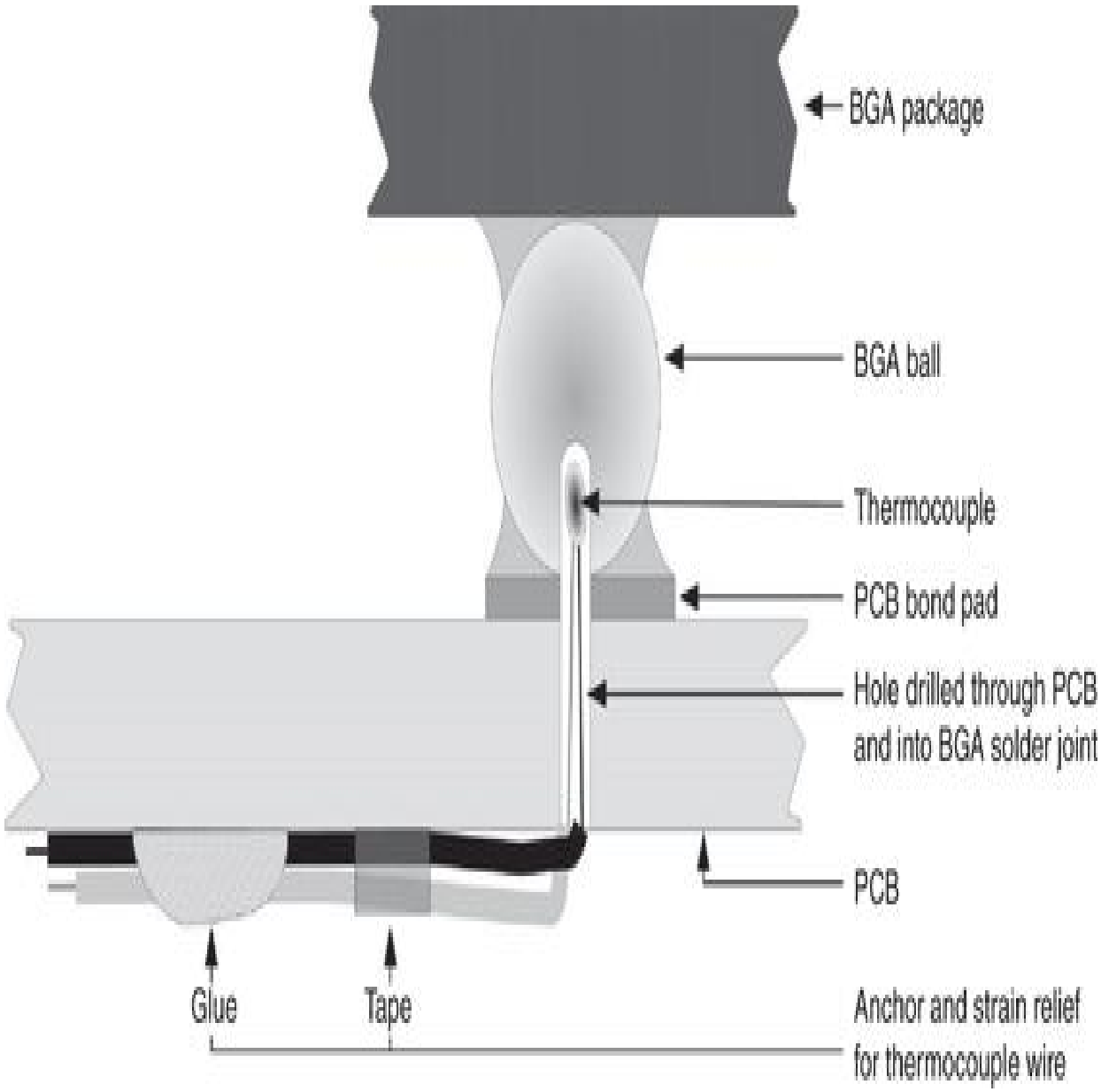

FIGURE 49.14 Thermocouple embedded into BGA ball. Thermocouple leads are anchored to the board with a small dot of high-temperature adhesive or high-temperature adhesive tape.

It is good practice to anchor thermocouple leads to the board to keep them in place and to prevent dislodging of the bead from its intended measurement target. The anchor also serves as a strain-relief for the thermocouple wire. A high-temperature adhesive or heat-resistant adhesive tape should be used. Tapes and glues are insulators, so care must be

taken to keep the anchoring glue or tape small in size and away from areas of thermal interest. Note that there is no need to seal the drilled hole into which thermocouples are inserted. These are miniature blind holes largely filled with thermocouple wires. Air transfer within this hole will be negligible. The air temperature in the hole will be fractionally close to the surrounding PCB and BGA materials. Use care so as not to cross thermocouple legs within the drilled hole as explained previously (Figs. 49.12*c* and 49.13).

49.3.8.3.3 Thermocouple Size. Many factors can confound the solder joint temperature measurement process, regardless of whether the thermocouple bead is properly deployed between lead and pad. Among these are the size of the bead and the thermal mass of the thermocouple assembly. In general, the use of finer-gauge thermocouples such as 30 to 36 American Wire Gauge (AWG) (Table 49.1) is recommended. Small size permits insertion between lead and pad even at very fine lead and pad pitches. It also facilitates inserting the bead into or near a solder ball of a BGA as discussed. Ideally the thermocouple bead will be completely embedded within the solder joint to be measured. If pitch is so fine that it is not practical to measure just one lead-pad combination, then it is reasonable to measure two sets of leads and pads.

TABLE 49.1 AWG versus Wire Diameter and Anticipated Thermocouple Bead Diameter

AWG	Wire Diameter, in	Wire Diameter, mm	Bead Diameter, in	Bead Diameter, mm
20	0.032	0.81	0.048	1.22
24	0.020	0.51	0.030	0.76
30	0.010	0.25	0.015	0.38
36	0.005	0.127	0.0075	0.19

Strive for the shortest possible length of thermocouple wire pair that is practical for the application. Long, large diameter wire may conduct heat away from the solder joint to be measured, altering its true heating nature and actual temperature.

49.3.8.3.4 Securing Thermocouple Beads

THERMALLY CONDUCTIVE ADHESIVE If an adhesive is to be used to hold a thermocouple bead to PCB pad or lead/pad combination, the adhesive's thermal conductivity must be taken into account. Most thermally conductive adhesives are not nearly as conductive as metal or solder. The best are filled with materials such as aluminum, boron nitride, or other thermally conductive materials. If the thermal conductivity is not high enough, a false thermocouple reading may result. Thermally conductive adhesives are meant to be applied thinly since conductivity depends on bond-line thickness. It is wise to baseline a filled adhesive against a soldered thermocouple to ensure that its insulating properties are not affecting measurement results. Also confirm that the adhesive will survive multiple reflow cycles and still maintain its thermal conductivity as reflow profile boards are used many times to establish the original soldering profile and to verify the profile from time to time.

Were the adhesive to release the thermocouple bead during the process, then measurement data would be useless. Many adhesives will not tolerate the high-temperature environment of soldering or the continuous thermal cycling encountered in trying to attain a proper soldering profile. This is especially true with the onset of lead-free soldering and the higher soldering temperatures associated with the move away from lead-bearing alloys.

ADHESIVE TAPE. Tape should be avoided for holding the thermocouple bead to the board. As tape heats, it stretches, expands, or even releases from the PCB allowing the thermocouple bead to float off its measurement target. If the thermocouple lifts, it will be gauging the environment rather than the lead/pad combination. Tape may also shield the thermocouple and the solder joint from the oven ambient, which is contrary to the task at hand. Some polyimide-based tapes can be used sparingly to anchor thermocouple wires (not beads) to the board to keep the wires in position and for strain-relief; but never for holding down the thermocouple beads.

HIGH-TEMPERATURE SOLDER. Best practice is to use a high-temperature solder to secure the thermocouple bead to its measurement site. The bead is not really soldered, as the K-type thermocouple wire is not easily wetted by most solders and fluxes useful for the surface-mount process. Instead, the solder bead is positioned under a component lead, and the lead/thermocouple/pad is covered over with the high-temperature solder alloy to anchor it in place (Fig. 49.15).

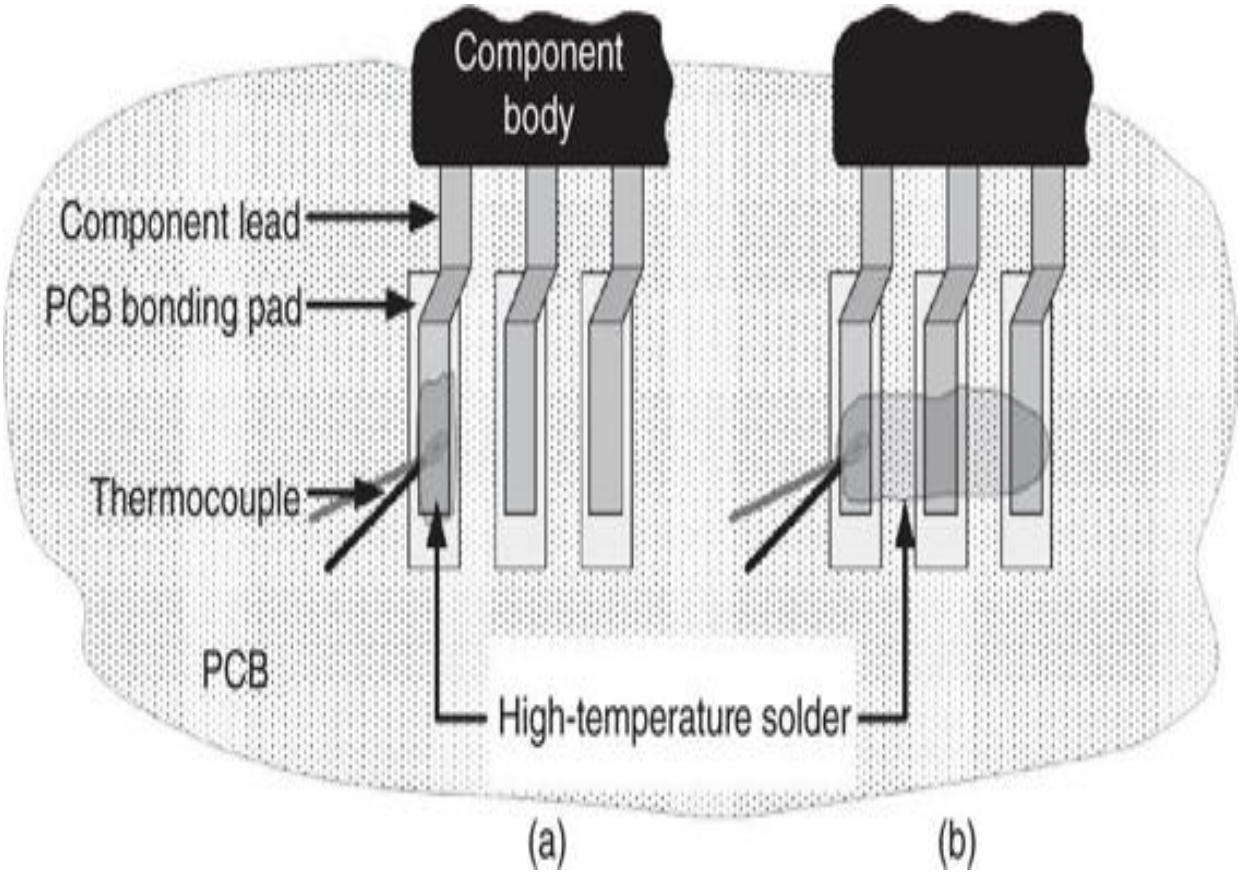

FIGURE 49.15 Check the quality of the thermocouple attachment: (*a*) a good thermocouple deployment. The bead is secured beneath a single lead and held in place with high-temperature solder. (*b*) The thermocouple is held in place by high-temperature solder but the solder has bridged to multiple leads and the bridged solder and extra leads has added significant additional thermal mass to the measurement. Temperature indicated will be that of the entire thermal mass of leads and solder rather than a single lead as in “a.”

The chosen high-temperature solder should have melting range or melting point well above the intended peak reflow temperature needed for PCA production. An alloy such as 10Sn/Pb (melting range near 300°C) is appropriate as most Pb-free solders melt in the vicinity of 220°C and the peak soldering temperature is generally less than 255°C. Before applying the high-temperature solder, it is advisable to use a fluxed copper wicking braid to remove any solder associated with normal manufacturing assembly of the board. The alloying of the high-temperature solder with the solder used for SMT may depress the melting range of the high-

temperature solder and increase the potential for reflow and release of the thermocouple bead during profiling.

For leaded components such as SOICs, QFPs and other externally leaded devices, a piece of polyimide tape can be used on the solder paste stencil to block the aperture associated with the thermocouple location. That will preclude the need to unsolder and remove solder from the component lead/pad for thermocouple insertion.

49.3.8.4 Profile Board Components. The profile board can be populated with dummy, electrically failed or reject components. It is not important that all leads be soldered, just a majority of them.

The board should last many profile cycles. Save the profile board after profiling is completed as it should be used to verify oven performance and profile prior to a manufacturing run.

49.3.8.5 Profile Board Spacing. In ovens with pin-chain conveyors, it is common practice to place the profile logging device (reflow tracker) on a dummy board that is trailed behind the profile board or on an expandable carrier made for holding the data tracker. The distance between the profile board and the dummy board or data tracker carrier should be at least one board length. Thermocouple wire length beyond the thermal profile board should be slightly longer than one board length (Fig. 49.16).

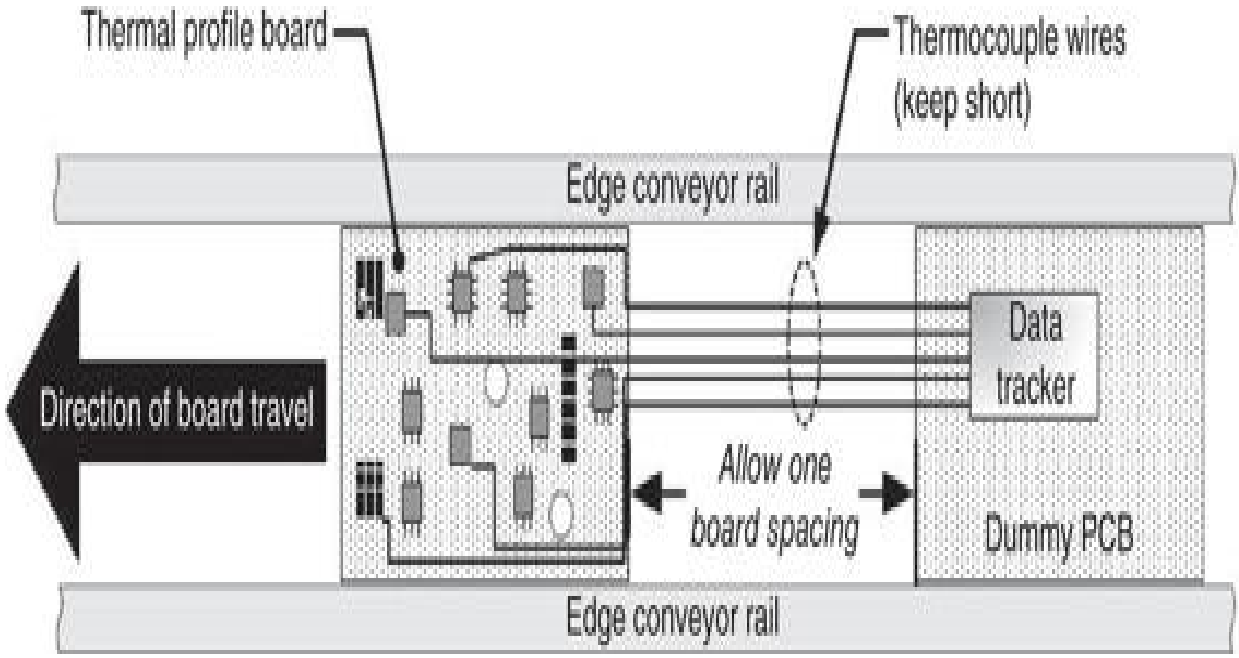

FIGURE 49.16 The thermal profile board should be kept a distance of about one board length from any dummy board or carrier for the data tracker. This enables the oven heaters and air-flow in the oven to function properly.

Were the two boards abutting, the heaters would try to compensate for a much larger thermal mass and tend to overheat; a situation different than during steady-state manufacturing. This rule also applies to thermal profiling at wave soldering.

49.3.9 Pin-in-Paste Soldering (Intrusive Reflow Process)

An adjunct to the surface-mount process, pin-in-paste (PiP) soldering, sometimes referred to as intrusive reflow, allows the soldering of some through-hole (solder-tail) parts into plated-through holes (PTHs) on the circuit board during SMT oven reflow. This process can eliminate or reduce the need for wave soldering—a step prone to defects.

To accomplish PiP soldering, solder paste is printed over PIP PTH locations during the SMT solder paste printing

process. Next, the through-hole components (axially leaded parts, pin-grid arrays, solder-tail connectors, etc.) are inserted into their respective PTHs before or after surface-mount component placement. Once the surface-mount components and the solder-tail parts are placed, the paste-bearing PCB is passed through the SMT reflow oven heated with an appropriate time-temperature profile. During the reflow process, the molten solder coalesces around the through-hole pins wetting between the pin and the PTH barrel. Surface tension and capillary action draw the solder paste down between the pin and the PTH barrel. As the solder alloy melts, it wets to the fluxed pin and barrel and upon cooling a solder joint results.

49.3.9.1 Solder Paste Deposition for Pin-in-Paste Soldering. To prepare a board for pin-in-paste soldering, generous amounts of solder paste are deposited over or adjacent to the circuit board's targeted PTH sites. This is done during solder-paste stenciling in preparation for SMD component placement and reflow (Fig. 49.17).

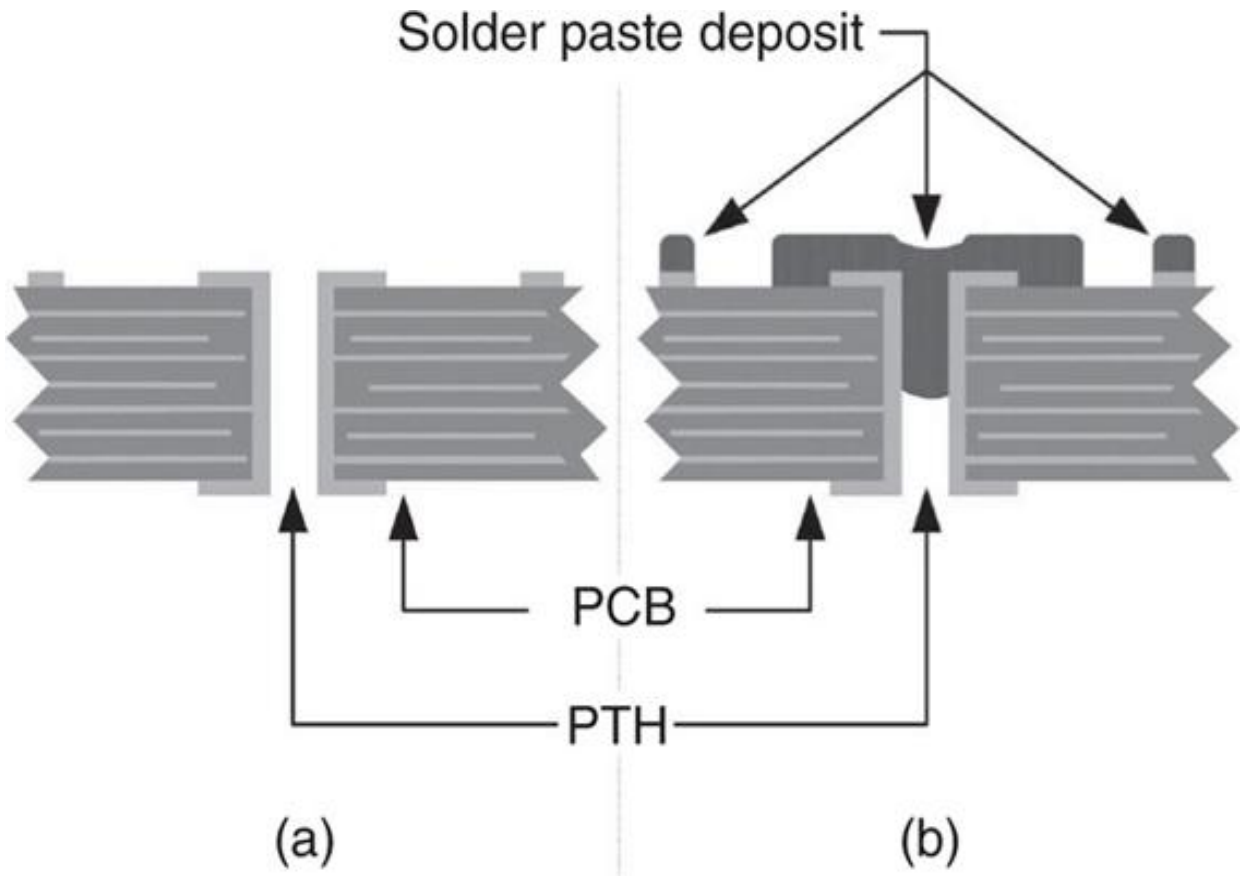

FIGURE 49.17 Solder paste stenciling in preparation for SMD and pin-in-paste component placement: (*a*) a PCB cross-section prior to solder paste deposition; (*b*) the same PCB after solder paste deposition. Note that SMD pads and plated through-hole (PTH) have received solder paste deposits. In the case of (*b*), paste has been forced into the PTH by the squeegee during solder paste printing (stenciling) process.

Of course, stencil apertures have to be created in the surface-mount stencil to accommodate paste deposition on PTH sites for pin-in-paste soldering.

49.3.9.2 Solder Volume. The inability to apply enough solder paste to meet standard through-hole solder joint acceptability criteria is one of the major shortcomings of pin-in-paste reflow. That is why this technique is usually relegated to thinner boards [≤1.6 mm (0.063 in) thick]. Requisite solder volume is dictated by: component pin pitch; available printing space between component leads; stencil thickness (generally limited by the smallest or finest pitch

surface-mount components on the PCB); PTH volume and associated component lead displacement volume.

Since necessary solder volume for pin-in-paste reflow is a function of the ratio of PTH volume to component lead displacement, it follows that reducing PTH barrel size is advantageous, especially in the case of thick PCBs. But if the annulus between lead and barrel is reduced by too much, there is a tendency for excessive void formation. Solder pastes formulated for surface-mount applications consist of solder spheres in a creamy matrix of organic chemicals composed of soldering flux and other materials to help with printing and component placement requirements for SMT processing. PTH voids during pin-in-paste soldering are generally caused by vaporization of solder paste organic components and entrapment of the gas in the molten solder or gaseous ejection of solder during the reflow process. Paradoxically, enlarging a plated-through hole in a thicker board may also benefit the pin-in-paste technique. The paste printing process drives solder paste into the PTH, effectively increasing the solder volume available for joint formation. A double-print cycle forces more paste into through-holes. If solder paste is in the PTH, some quantity of it will be displaced as the component's lead is inserted (Fig. 49.18*a*). Upon reflow, the solder generally wets back up the pin (Fig. 49.18*b*). Sometimes, though, the displaced solder will form a bead on the pin tip, as seen in Fig. 49.18*c*). Although electrically it is of no consequence and well adhered since it is soldered, it can interfere with critical clearances (such as aboard to chassis) or impede proper board seating at in-circuit test or in other fixtures.

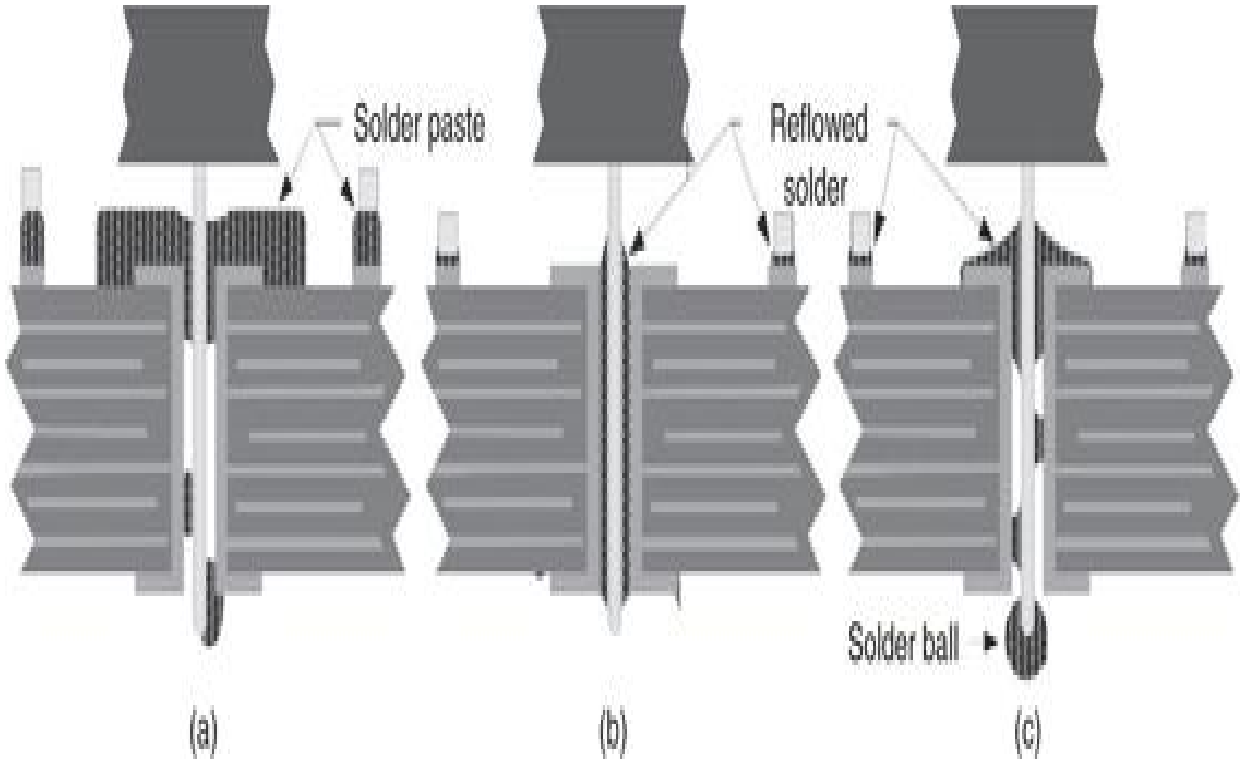

FIGURE 49.18 Board sections illustrating pin-in-paste process: (*a*) A PTH component pin inserted through solder paste squeegeed in and around a PTH. (*b*) At reflow, the solder has melted and wet to pin and component leads. If solder volume is correct, surface tension effects will draw the solder between pin and barrel and a good solder joint will form. (*c*) The solder paste displaced by the pin insertion has melted into a ball around the pin tip. So much solder was displaced that voids are apparent between the pin and the PTH barrel.

A solder paste stencil can be designed to occlude solder deposition on top of or in the board's PTH, as can be seen in Fig. 49.19.

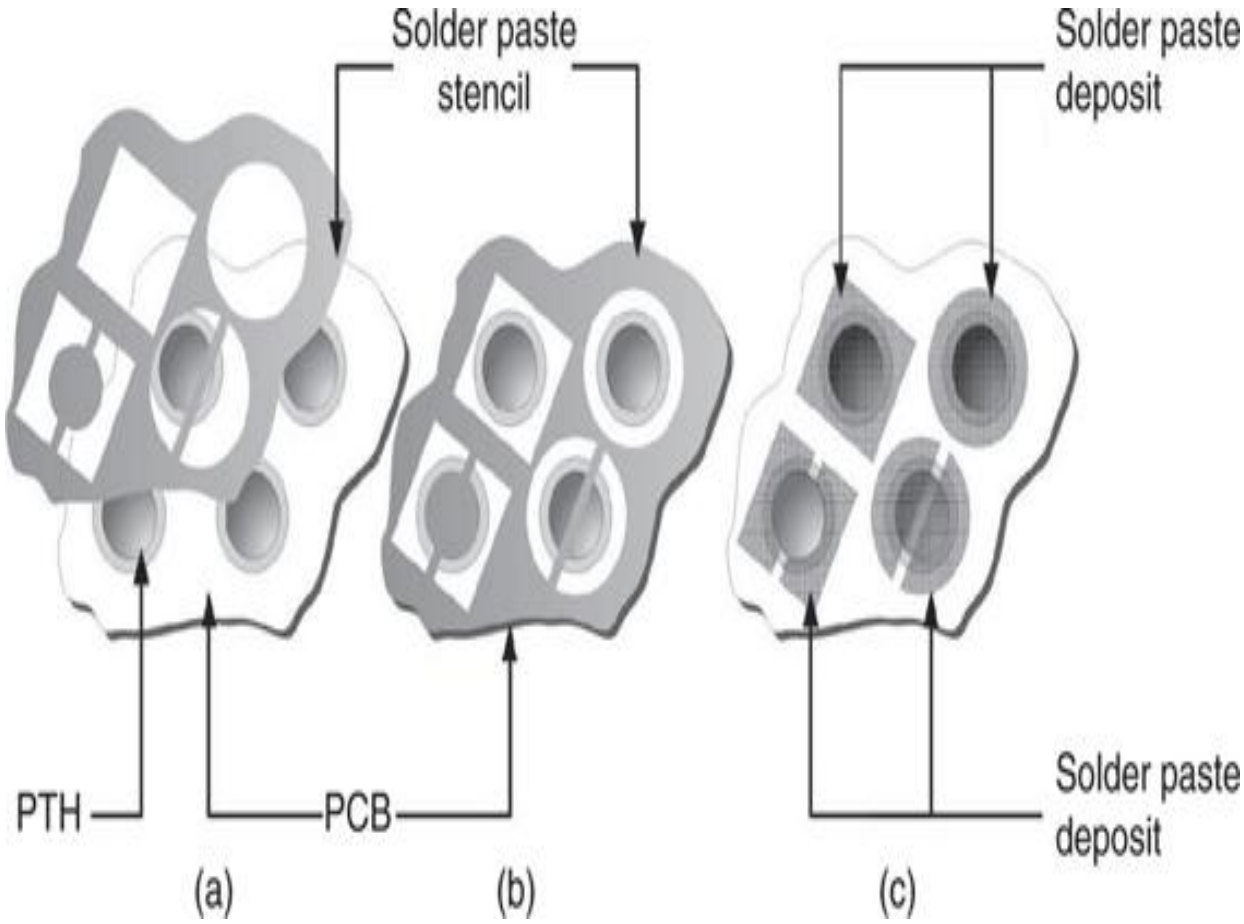

FIGURE 49.19 Solder paste deposition on PTH for pin-in-paste soldering: (*a*) stainless steel stencil being applied to a PCB in preparation for solder paste printing for a pin-in-paste component. The stencil has four typical pin-in-paste aperture types. Starting from the upper left are: square or diamond; circle, "half-moons," square aperture with a feature to prevent paste from printing in to the PTH. (*b*) shows the stencil aligned to the PCB and c) illustrates the resultant solder paste deposits. Note that in each case the solder paste has been over-printed onto the laminate of the PCB to increase the solder volume and hopefully result in fully wetted solder joints.

Stencil designs that preclude solder paste from entering the PTH also result in a significant reduction of solder paste on the top surface and in the PTH. These reductions may make the pin-in-paste technique impractical for some boards. If the solder volume is too low, the available solder distributes unevenly around the PTH pin and the PTH barrel, resulting in voids and inferior solder joints (Fig. 49.20).

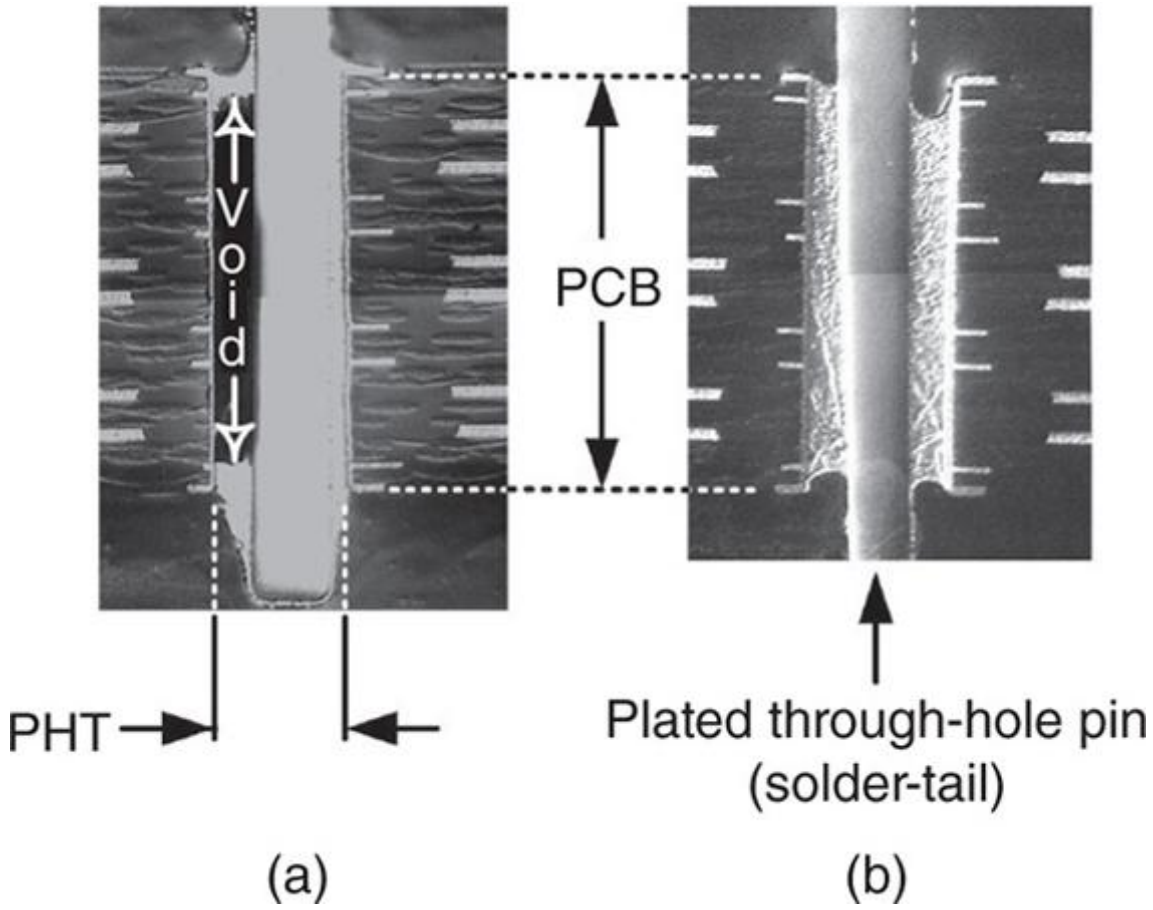

FIGURE 49.20 Solder joint defects can result from uneven solder distribution: (*a*) solder-starved pin-in-paste solder joint showing large void; (*b*) good pin-in-paste solder joint showing nearly 100 percent barrel fill, no voids and good wetting. (*Courtesy of Hewlett-Packard*.)

A normal-incident x-ray (x-rays perpendicular to PCB surfaces) will highlight circumferential voids in plated-through joints as evidenced in Fig. 49.21.

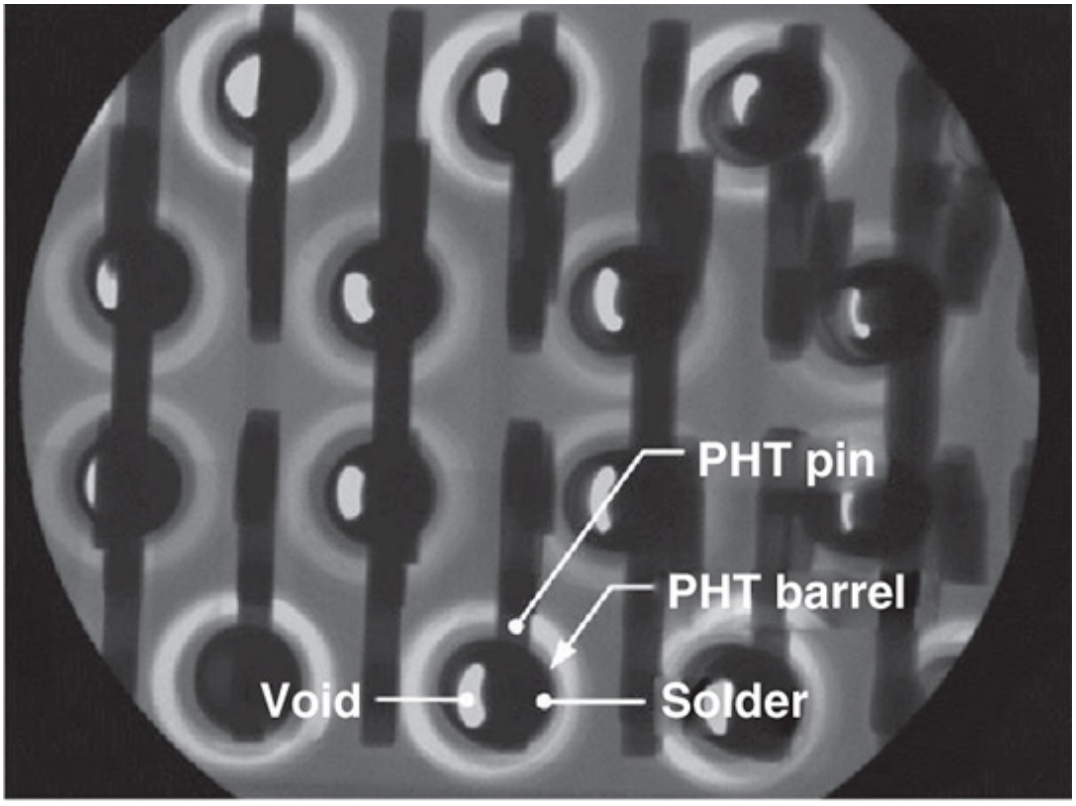

FIGURE 49.21 A normal incident x-ray photo of a connector soldered in SMT reflow with pin-in-paste technique. The light spots around the pins are solder voids (no solder) indicative of insufficient solder resulting from pin-in-paste soldering method. The dark area is solder wetted to PTH barrel and connector pin. (*Courtesy of Colab Engineering, LLC*.)

49.3.9.3 Pin-in-Paste on Thick Boards. Since the solder volume requirement increases proportionately with increasing board thickness, pin-in-paste soldering is best suited for thin PCBs (≤1.6 mm). The technique is limited by available solder and required solder volume for proper barrel fill. Adding additional solder by overprinting may result in nonwetted solder balls that separate from the solder paste mass during the reflow process and loose solder balls with an inherent short-circuiting hazard. There are three ways to augment solder volume for an effective pin-in-paste process:

49.3.9.3.1 Thicker Solder Paste Stencil. A thicker stencil will deposit more solder paste, but ultimately the solder paste stencil thickness must be tailored to suit the finest device lead-to-lead pitch on the board. Step stencils with

selectively thick areas can be used but care must be taken to ensure that there is sufficient transition in the step-up area to allow for proper squeegee action and solder paste deposition.

49.3.9.3.2 Addition of Solder with Foil Pre-Forms. Solder foil pre-forms (stamped solder foil) can be added to through-hole parts to augment intrusive reflow solder volume (Fig. 49.22). This approach is expensive and application of the pre-forms is tedious and time consuming.

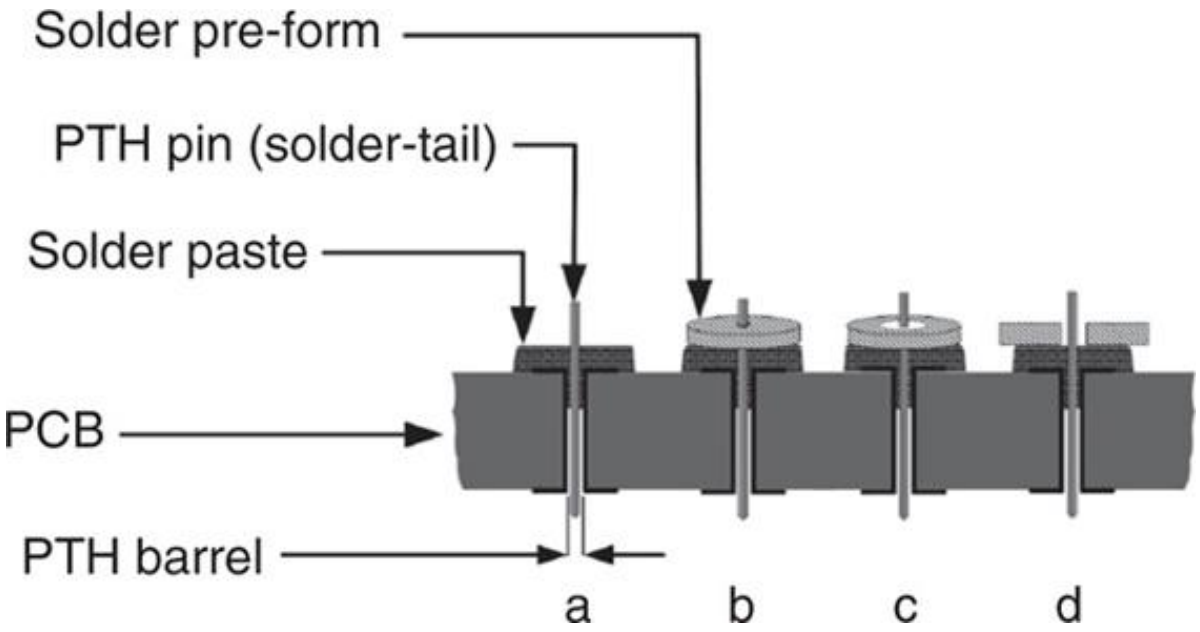

FIGURE 49.22 Various approaches to pin-in-paste (intrusive) soldering. Solder volumes in "b," "c," and "d" are augmented with solder foil pre-forms. (*a*) Stenciled solder paste only, (*b*) tight fitting solder washer applied to the solder-tail prior to placing the device into the PTH on the PCB. (*c*) Pre-form washer with a generous inner diameter hole such that the washer can be picked up with a special suction head at the SMT pick-and-place step and placed on paste deposit. (*d*) Orthogonal pieces of solder pre-form foil, also inserted at the pick-and place step. In each case, the flux for joint formation comes from the application of solder paste as required for the SMT process.

Large solder pre-forms can be deposited on the solder paste with the SMT placement machine. The flux from the solder paste will clean the pre-form during the reflow process to allow it to wet to the paste and solderable surfaces. Some

pre-forms come with a coating of flux, too. Ensure that the flux on the pre-form is compatible with the flux in the solder paste otherwise corrosion could result in the long term with ensuing circuit reliability issues.

49.3.9.3 Buried Intrusive Method. There is another method for formation of a somewhat nonstandard solder joint in thick PCBs. A foreshortened pin, on the order of that used for a board 1.6 mm in thickness, is used in the thick board. So, too, solder volume is treated as if for a board 1.6 mm thick. When the solder melts, it coalesces and wets to the pin and barrel as in any through-hole soldering process. Nearly all the solder is retained by surface tension forces around pin and barrel. If the solder volume is calculated properly and appropriately delivered, there is 100 percent pin wetting both longitudinally and circumferentially (Fig. 49.23). Accelerated thermal cycling followed by tensile testing has shown that resultant solder joint reliability is sufficient and equivalent to conventionally formed pin-in-paste or wave-soldered joints of twice the pin-wetted length.[2]

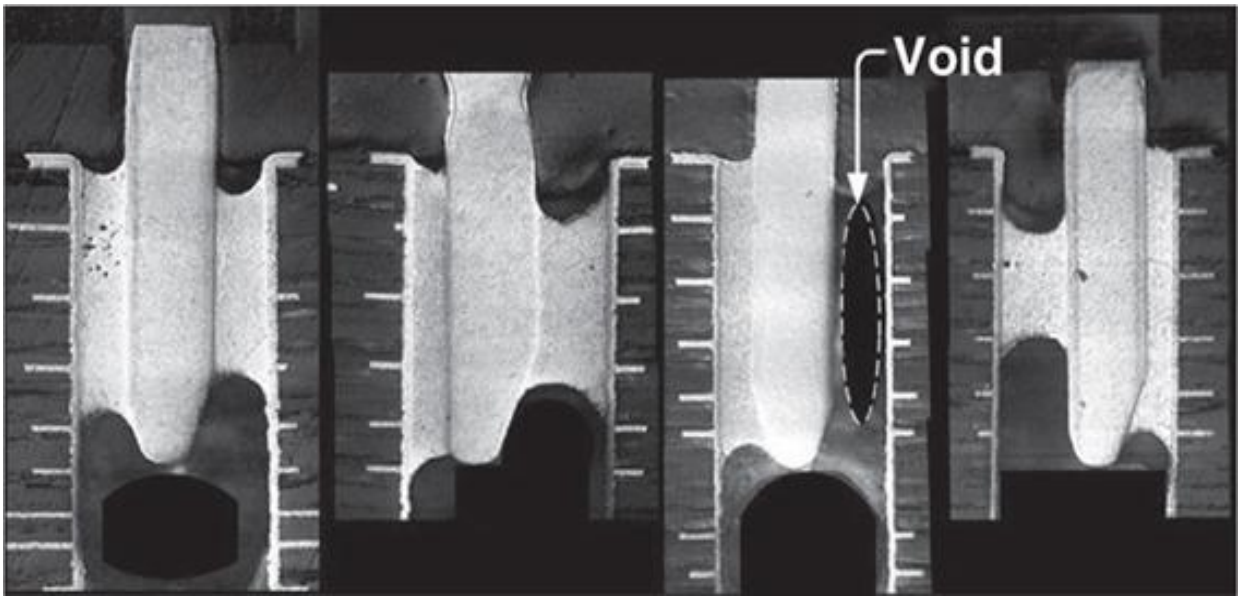

FIGURE 49.23 Cross-sectional micrograph showing pin-in-paste buried intrusive soldering. Note that in each case very little solder has drained down the PTH. Instead, it is held by capillarity between the solder-tail and the PTH barrel wall. All solder joints pictured are somewhat starved for solder. The left-most is the most robust solder joint and such joints are approximately equivalent to standard full-barrel wave soldered PTH joints in terms of resistance to thermal cycling and shock/vibration reliability.

49.3.9.4 Temperature Compatibility.

If pin-in-paste soldering is to be used, ensure that components are temperature-compatible with the oven reflow process. The high temperatures and long exposures associated with oven reflow soldering may cause unsuited, plastic molded component bodies to melt or warp. Connector contact normal force may be impugned if the molded body softens or distorts. Solder joints or wire bonds internal to some devices may become dis-bonded, and some devices, such as electrolytic capacitors, may leak or even explode as a result of an oven reflow cycle. Check component manufacturer specifications for thermal limits and compatibility with reflow oven soldering.

49.4 WAVE SOLDERING

Once the predominant method for mass assembly of circuit boards, wave soldering has taken a back seat to oven-based reflow soldering with surface-mount technology (SMT). The ease and speed of assembly with SMT led to its rapid dominance and the decline of wave soldering. Nonetheless, the need for through-hole componentry persists and mixed-mount (surface-mount plus through-hole) technology still may be the only alternative for some assemblies, and it is unlikely that wave soldering will disappear from PCB manufacturing in the short term. Since wave soldering, compared to reflow soldering, is fraught with defects, it

behooves the designer and assembler to minimize the number of PTH components on a board.

Wave soldering is an automated method for joining the pin of a component into a drilled through-hole on a PCB. The drilled holes are plated on the inside and a pad, also plated, is connected to the plated through-hole barrel (Fig. 49.24).

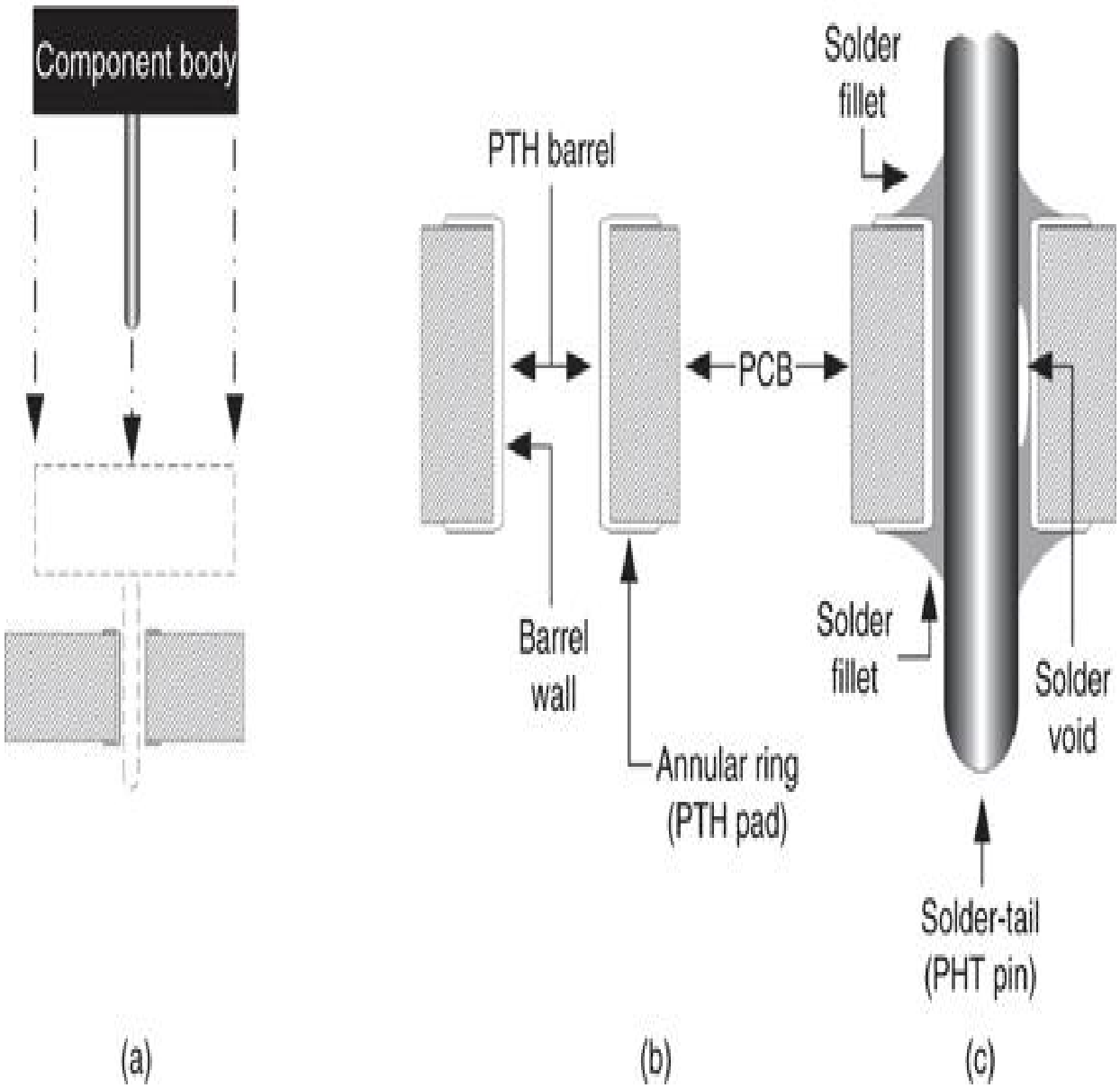

FIGURE 49.24 Schematic of a PCB section with a plated through-hole (PTH). (*a*) Solder-tail component is inserted into the PTH. (*b*) The PTH is composed of a plated barrel and annular rings on the top and bottom surfaces of the PCB. The annular rings are connected to the barrel. Surfaces of the rings and barrel are

solder-wettable. (*c*) During wave soldering, solder wets to the PTH and the pin and solder joints are formed. Gaseous inclusions in the solder are called voids.

The barrel may be connected to copper power planes or ground planes within the printed circuit board (PCB) or to surface traces for electrical connection to other components on the PCB. The PTH has three parts to it: a drilled, plated hole, a top-side plated annular ring and a bottom-side plated annular ring. During wave soldering, the PTH and component pin are first coated with a soldering flux to clean the parts of any oxides, tarnishes or contaminants. Next, the bottom of the PCB is exposed to a standing wave of molten solder. The solder wets to the solder-tail and also to the annular ring. As the board continues to heat, the solder wets to the PTH barrel and is drawn into the space between the solder-tail pin and the PTH barrel by capillary action. If conditions are right, the solder will wet to the pin and barrel and travel all the way up to the top-side annular ring. When the solder cools, it solidifies and solder fillets (wetting between the barrel, annular ring and the pin) will be present. Sometimes, entrapped air or volatiles from the fluxing agent will create bubbles in the molten solder. These are called solder voids. If a void is large enough it may detract from the mechanical integrity and reliability of a solder joint. Voids can be examined by mechanically cross-sectioning the finished printed circuit assembly (PCA). More practically, voids can be imaged non-destructively by transmission x-ray analysis.

49.4.1 Wave-Solder Process Basics

Wave soldering utilizes a reservoir of molten solder pumped and circulated to form a standing wave. The circuit board is prepared with devices for wave soldering in one of three ways:

1. Coarse-pitch surface-mount components, especially passive devices, are affixed to the bottom-side of the PCB using surface-mount adhesive. The adhesive is in contact with the body of the component, which is aligned with its respective pads on the circuit board in preparation for wave soldering. The adhesive is cured or partially cured prior to wave soldering.
2. Solder-tailed components, such as connectors, PGAs, or other through-hole devices, are inserted into PTHs from the top-side of the board.
3. Solder-tailed components such as axially leaded devices are inserted from the top-side of the circuit board and their leads are clinched on the bottom-side of the board to hold the components in place.

The circuit board is placed on a motorized, edge-hold conveyor where it is fluxed. Next, the loaded PCB is preheated, both to activate the flux and give the PCB a thermal boost in preparation for soldering. The board is next skimmed over the crest of the molten solder wave. Only the bottom of the circuit board is exposed to the molten solder (Fig. 49.25).

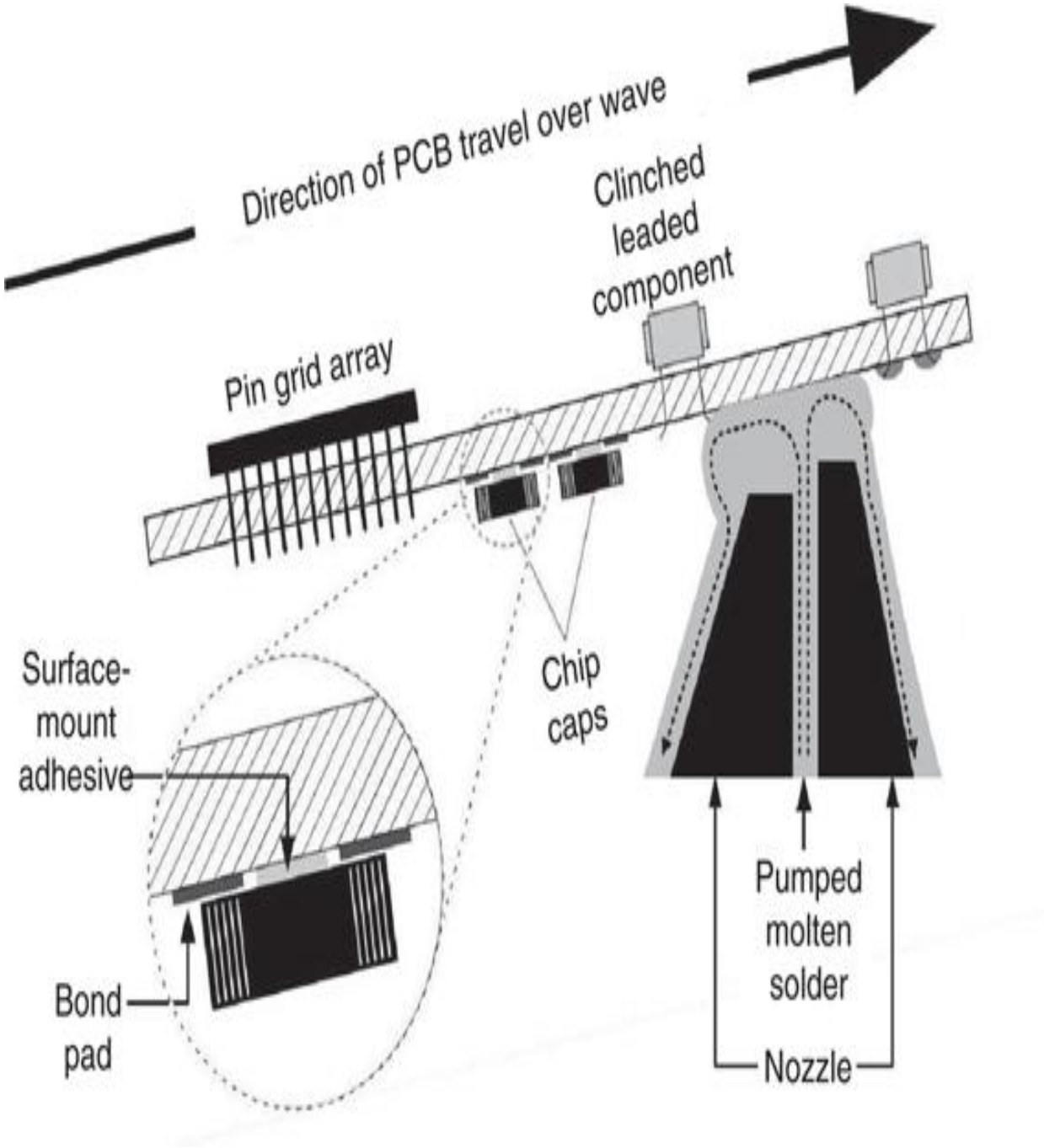

FIGURE 49.25 Schematic of a board going over a solder wave. The board is conveyed over the pumped standing wave of molten solder. The wave height is adjusted to contact the bottom of the board only. Some components are inserted, others inserted and clinched. Surface-mount adhesive can be used to hold small passive components to the bottom of the PCB for wave soldering.

When exposed to the wave, the adhesive-attached surface-mount devices pick up solder on their metal contacts

and the solder bridges from the contact to its corresponding bonding pad on the bottom-side of the PCB. In the case of solder-tail components, the molten solder is drawn by capillary action between the lead and the PTH barrel. If the barrel and lead (pin) are hot enough, well fluxed and properly sized, the solder fills up the barrel and wicks to form fillets from pin to barrel. As the board continues past the wave, it cools, solder solidifies, and joint formation is complete. One attribute of this process is the speed at which solder joints are formed. Much quicker than oven reflow soldering, the wave-solder process allows little time for preheating, fluxing and solder joint formation. This partially explains this process's variability.

49.4.2 Wave-Solder Machine Subsystems

There are six basic subsystems to a wave soldering machine, including: conveyor; fluxer; PCB preheater; solder circulation system (solder pot, heaters, pump, nozzles); ventilation. If alcohol-based fluxes are being used, it is wise to install a fire suppression system on the wave soldering machine, also.

49.4.2.1 Conveyor. As for the reflow oven, the wave solder machine is generally equipped with a mechanized, speed-controlled conveyor to transport the board at a constant velocity through the soldering process. In the case of wave soldering, the board is always held by a width adjustable edge-finger conveyor, which grabs the board by its edges and neither occludes solder exposure nor interferes with wave dynamics. The stainless-steel edge fingers need to be cleaned routinely to avoid flux build-up.

49.4.2.2 Fluxer. The fluxer is responsible for delivering a uniform application of soldering flux in a sufficient quantity

for solder joint formation. The short preheat and liquidus times characteristic of the wave-soldering process dictate the use of slightly stronger fluxing agents than are used in reflow soldering. Although this is the case, the vast majority of wave solder applications have migrated to the use of no-clean fluxes. For the flux to do its job, it must be heated to an ample temperature to permit best reactive conditions without drying or denaturing it. For the sake of economy and to minimize resulting flux residues, the thinnest flux application is deposited. The flux quantity has to be sufficient to remove oxides from the PTH barrels, solder, and component leads. On the other hand, since post-wave solder no-clean flux residues can confound in-circuit test probe contact, the thinnest application that still permits adequate fluxing is recommended.

Flux quantity may also be of concern in the wave-soldering process for yet another reason: fire hazard. Flux-laden boards are preheated going into the wave. If the flux application is too heavy, the flux may drip onto pre-heater elements. This may cause the flux to volatilize rapidly, combine with oxygen in the atmosphere, and provide the right conditions for flame initiation. Even if there is not direct exposure of the liquid flux to preheaters, if the quantity of volatile flammable components is sufficient and exposed to an ignition source (spark), then an explosive condition may develop. With the advent of more eco-friendly, water-based fluxes, fire hazard is less of a concern. Foam and wave fluxing have given way to spray fluxing as the predominant flux application method. All three techniques are discussed here.

49.4.2.2.1 Foam Fluxer. Foam fluxing is accomplished by pumping and aerating a stream of liquid flux through a porous metal nozzle, a fritted glass, or porous stone. The nozzle, also called a chimney, shapes the flow of the aerated flux. The board to be soldered is run over the foaming flux and then heated to activate the flux before reaching the

solder wave. As it moves past the solder wave, the solder wets to solderable metals and solidifies to complete the soldering process. Foam fluxing is particularly effective for soldering of PTH assemblies. Surface tension draws the foam into the PTH barrels, just as is the case with solder. The resulting flux deposit on the pin and barrel is thin and uniform.

49.4.2.2.2 Wave Fluxer. The wave fluxer works much as the solder wave itself. The PCB is moved over a standing wave of solder flux. The height of the flux wave and depth of the board penetration into the flux wave are adjusted to allow for proper flux application thickness. Capillary action, as in all the fluxing methods for through-hole components, draws the flux into the interstice between component lead and the PTH barrel. As with foam-fluxing, it is difficult to control the amount of flux delivered. For the most part, flux applied for wave soldering is largely removed by the turbulence of the solder wave; however, it is possible to bake on the flux if the pre-heater temperatures are set to too high. Resulting residues may inhibit fluxing or solder wetting to otherwise solderable surfaces.

49.4.2.2.3 Spray Fluxing. Because of its economy and accuracy, atomized spraying has grown to be the predominant flux deposition technology. Precise amounts of a low-solids flux can be applied generally to a board or can be selectively delivered to small areas of the board to be soldered. There are two principal methods of spray fluxing: air-spray and ultrasonic. Both are effective and well tested. Ultrasonic methods minimize flux volumes consumed in manufacturing.

If not set properly, spray fluxing may result in a flux-laden airborne mist that deposits wherever the air currents or process gases carry it. Flux contamination of card-edge gold fingers and contacts within connectors is most notable. This can disrupt proper electrical contact when a daughter-card is inserted into a connector. It is wise to cover any exposed

gold fingers with an acrylic adhesive polyimide tape[3] or other shielding to prevent contact fouling by flux droplets.

49.4.2.2.4 Fluxer Maintenance. As fluxes are exposed to the atmosphere, they are vulnerable to evaporation of volatile constituents. This is the case even with water-based fluxes. Evolution of volatiles is significantly enhanced in systems such as wave-fluxer or foam-fluxer. In these flux deposition systems, the flux is open to the atmosphere or the processing environment, has significant exposed flux surface area, and is constantly being recirculated. Therefore, the flux needs to be monitored and maintained. Although some automatic systems are available, most require routine measurement of the flux's specific gravity with a hydrometer and adjusted with a proper flux thinner to restore the specific gravity to compensate for these evaporative losses. In addition, the volume of the flux in the system must be monitored and adjusted to the proper level. The fluxer must be maintained to prevent impact on process yield. The flux manufacturer can provide information as to the proper specific target and also recommend an appropriate thinning formulation.

The flux reservoir should be emptied, cleaned thoroughly, and refilled with a fresh charge of flux periodically. Sometimes the flux develops a residue that changes the flux's surface tension characteristics, clogs nozzles, or dispensing pores in foaming systems. In addition, flux may become contaminated with debris conveyed by the PCB to be soldered, which may impact assembly quality. Since the PTH relies on a minute capillary to be filled first by flux and ultimately by solder from the solder-wave process, any small particulates entrained in the flux or the solder may impede PTH barrel fill. Also, while the flux reservoir is empty, it is a good idea to inspect it to ensure that the materials of construction are holding up to the rigors of system operation and prolonged contact with fluxing agents which may prove corrosive in the long term. An inspection of the materials of

construction for the entire system should be made prior to committing to the purchase of a wave-soldering machine. Unfamiliar or untested materials should be avoided unless there is sufficient literature, test results, or customer experience to ensure compatibility with fluxes that will be used in that system.

In the case of spray fluxing, since the flux is not exposed to the atmosphere until it is sprayed onto the PCB, specific gravity and “thinning” are not an issue as for foam fluxing or wave fluxing. However, care must be taken to ensure that the spray nozzle is kept clear of clogs and that it is spraying the correct volume for each PCB.

Gravimetric methods can be used to determine uniformity and reproducibility of spray. One such method utilizes identical witness pieces, such as microscope slides, attached the bottom side of a PCB or other rigid material with two-sided tape. Each slide is identified with a scribed designation, weighed ahead of time with micro-balance; its weight and position recorded (Fig. 49.26).

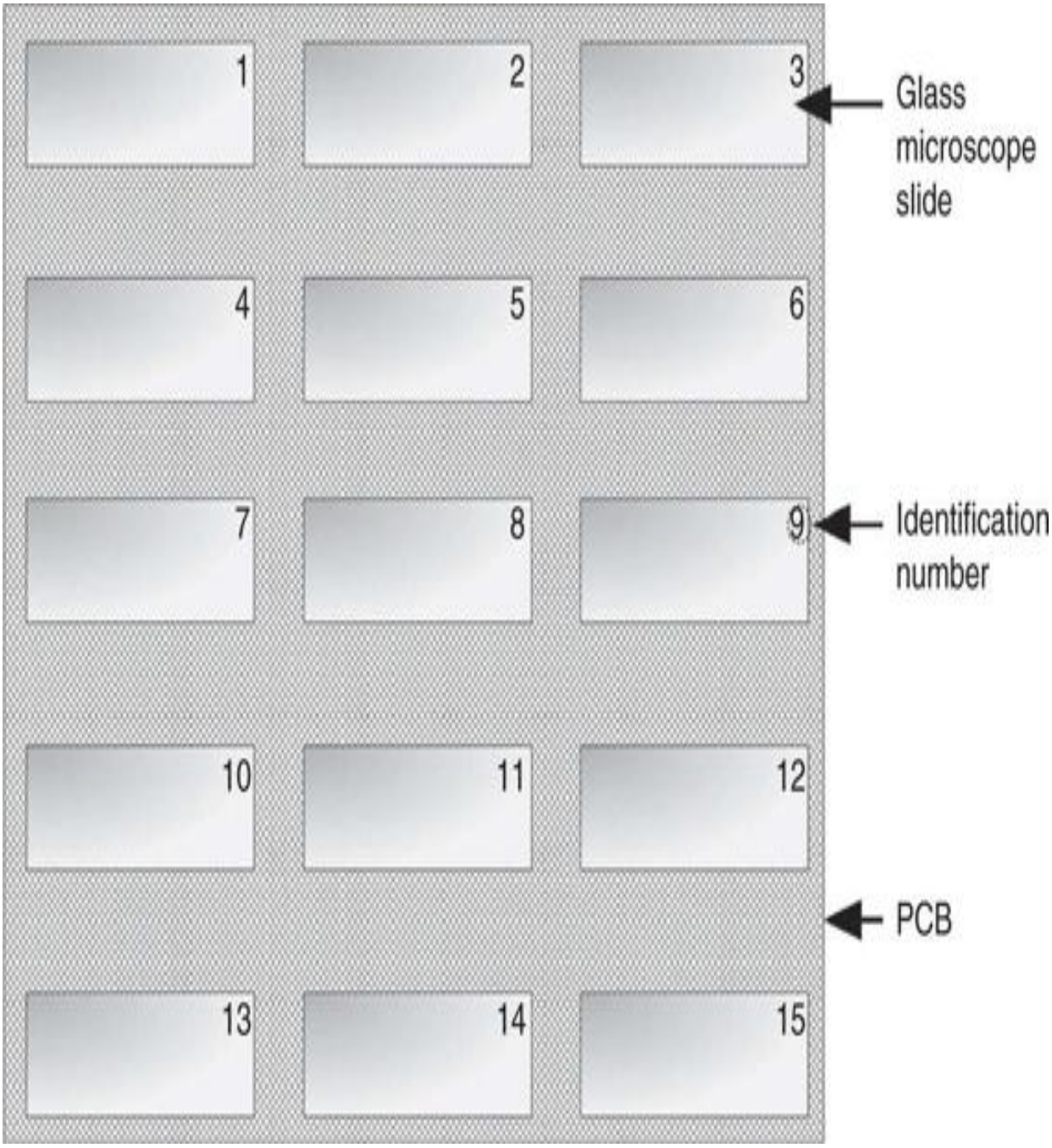

FIGURE 49.26 Microscope slides arrayed on the bottom-side of a circuit board for evaluation of flux deposition and uniformity.

Once set on the wave machine's moving conveyor, the spray fluxer is activated (generally, automatically by means of sensors), the flux is sprayed onto the bottom-side of the PCB and the attached glass slides. After spraying, the board must be removed before preheat and should not be exposed

to the solder wave. Next, it should be dried at low heat in a box oven to gently evaporate volatiles. Once dried and cooled to room temperature, each slide is weighed again and compared to its original, dry weight. Differences in uniformity from edge-to-edge and from front to back can be determined from this method. Compare the volume of flux dispensed to the flux manufacturer's recommended volume. Most manufacturers will provide guidance as to the dried-weight of their sprayed liquid flux.

49.4.2.3 PCB Preheating. Preheating the PCB and components serves three purposes in the wave soldering process:

1. Helps the board and components reach a temperature sufficient for the flux to activate. The activated flux cleans surfaces to be joined in preparation for wave soldering.
2. Lessens thermal differentials and decreases the likelihood of components cracking due to thermal shock when impacted by the intense and sudden heat of the molten solder wave.
3. Allows the board to ramp quickly to solder-melting and wetting temperatures when it comes in contact with the solder wave.

A component's resident time in the solder wave is 10 to 30 times shorter than for a comparable solder joint formed during reflow oven soldering, so everything in wave soldering has to happen very rapidly. On the other hand, heating time-temperature ramps must be observed in accordance with the component manufacturer's specifications. Components and PCB bonding pads must be fluxed sufficiently to allow adequate solder joint formation, yet there must be enough flux left on the circuit board after preheating to protect the newly fluxed surfaces from reoxidizing until the assembly reaches the solder wave.

Just as in the reflow soldering oven, there are multiple solder-wave preheater styles, but only two are in prevalent use: radiant preheaters (direct and indirect IR) and forced-air convection preheaters. Both are effective and both have their advantages. In fact, the best configuration is a combination of the two. Some wave-soldering machines can be equipped with both top and bottom preheaters. This can be advantageous for thermally massive boards.

49.4.2.4 The Wave. Numerous solder-wave configurations are available. Rather than provide a detailed discussion of each, this section offers a basic overview of the elements of the process in relation to the wave. As previously mentioned, the molten solder is pumped to form a standing wave. This is accomplished by a pump (and spinning impeller) on the bottom or side of the solder reservoir. Once the solder is molten, the impeller motor is activated and the solder wells up between baffles and nozzle that reside within the solder reservoir. A combination of impeller speed and baffles-and-nozzle configuration dictates overall standing-wave shape characteristics. The nozzles and baffles are generally adjustable, as are impeller speed, molten solder temperature, board introduction angle, and board conveyor velocity. These, along with flux type, flux deposition amount, preheater settings, define the process profile parameters or process variables that must be tamed to accomplish high-yield wave soldering. The quantity of process variables accounts for the difficulty in set-up, control and reproducibility of the wave soldering process.

Since the solder in the wave is a molten, turbulent, high conductivity liquid, thermal uniformity is generally not difficult to achieve as long as the wave contact area along the width of the PCB’s underside is adjusted to be uniform. Since the solder is in contact with the underside of the PCB and since the underside of the PCB is coated with flux, the molten solder has the opportunity to wet to PCB lands and

component leads. As the process progresses, solder wicks between the pin and barrel. After leaving the wave, the board cools rapidly, liquid solder solidifies, and solder joints result.

49.4.2.5 Wave-Soldering Accessories. Solder-wave manufacturers have devised a number of options that may be helpful to the process. Some of these have extended wave-soldering capability to allow finer-pitch soldering or permits wave soldering of thicker PCBs.

49.4.2.5.1 Gas Knife. The gas knife, more commonly called the air knife, directs a high-velocity stream of heated air or nitrogen at a glancing angle to the bottom-side of the board directly after the board emerges from the wave, while the solder is still molten. It can be effective in relieving solder bridges from tight interstitial component pin fields or closely spaced passive device fields. When the gas knife is used with air instead of nitrogen, increased rates of dross formation may result. Also, if the angle is wrong and the velocity is too high, the exit gases may disrupt the solder wave, resulting in solder opens or shorts. If it is set too cool, the knife will have little effect or may exacerbate solder bridging. Since the advent of the air knife, there has been less dependence on the use of tear-drop-shaped trailing pads used to minimize trailing edge solder bridges.

49.4.2.5.2 Sonic Assist. Although not in common use, this accessory imparts high-amplitude sonic pulses into the solder wave. This can help drive solder into PTHs and increase wetting, especially on thick PCBs. Care must be taken during setup, as very high amplitudes may pump so much solder into the PTH barrel that top-side solder flooding, bridging or solder splashing may occur. Its value is limited, since it does not affect board heating, which is the primary factor in barrel fill. This accessory is not in widespread use but could be considered for problematic wave soldering of thick boards.

49.4.3 Wave-Solder Diagnostics

As in all cases of mass soldering, the use of a product-specific, fully populated time-temperature profile board is necessary to ensure that critical areas of the board to be soldered are maintained at proper temperatures for each stage of the process. Top-side SMT component solder joints must be kept well below the melting point of the solder used to join them to the PCB. At the same time, PTH barrels and PTH components must surpass liquidus temperature to guarantee sufficient wetting and capillary rise of the molten solder. With the complexity of today's mixed-mount boards, this is more of a challenge than ever. A profile board should be constructed and instrumented just as for oven reflow soldering. Thermocouples should be attached to both sides of the board and monitored simultaneously during the wave-solder profile run. Connector bodies should be monitored to ensure that they are not overheated.

Generally, for most Pb-free surface-mount solder alloys, the PCB pre-heat temperature prior to wave should be about 50 to 70°C less than the liquidus temperature of the soldering alloy used for SMT. Of course, this thermal limit varies greatly with board size, thickness, component type, number of PCB layers, number of connections to inner planes, thickness of inner planes, component layout density and other factors. For SAC305 alloy with a melting range of approximately 217 to 221°C, it is best to keep the top-side temperature of the PCB in the 160 to 170°C prior to exposure to the wave. When the board reaches the wave, the board temperature will spike to at or near liquidus of the surface-mount solder alloy. The use of wave pallets (shields) to thermally mask the PCB will be discussed later in the context of selective wave soldering.

In addition to the profile board, there are numerous useful diagnostic tools commercially available for dynamically measuring the wave height and wave contact area, wave

depth and assessing resident time in the wave for a given conveyor speed.

49.4.4 Dross

Hot solder is prone to rapid oxidation at the air-liquid solder interface. Although the wave is in constant motion, the solder is actually flowing beneath a thin, stationary, plastic film of solder metal oxides. In Sn/Pb, Sn-Cu, or Sn-Ag-Cu systems, the skin is composed primarily of tin oxide but also contains oxidized traces of other alloy constituents or contaminants. The oxide skin on the surface of the wave and atop the solder in the reservoir is called dross. The dross has a beneficial aspect in that it helps to limit oxidation of the recirculating solder in the solder pot, but it also interferes with solder-wave dynamics and solder wetting.

When adjusted properly, the board meets the crest of the wave and disrupts the oxide skin. In doing so, the fluxed components and board are immersed in the flowing, oxide-free, molten solder. If all steps are carried out properly, the solder wets to the fluxed, oxide-free component leads, component pads, and PTH barrels. Upon exiting the wave solder machine, the assembly cools below the solder liquidus temperature and solder joints are formed. There are four factors that will determine the amount of dross produced:

1. System use (the number of hours of wave on-time)
2. Speed of the wave pump
3. Turbulence of the wave system
4. Temperature of the solder pot

Mostly, dross is the result of exposure of the molten solder to the atmosphere. It is worthwhile to work at minimizing any or all of these to lessen the effects of dross on the process.

49.4.4.1 Impact of Dross. Dross is of concern from three points of view:

- *Process impact:* Presence of excessive dross can result in shorts, opens or retard wetting.
- *Economics:* In high-volume manufacturing, the amount of solder lost to dross can mean hundreds of dollars of lost solder per week per machine. Of course, the actual cost depends on machine use, solder alloy, and quantity of boards soldered and the price of the original solder. However, the dross can be sold back to some solder manufacturers for recycling.
- *Sn (tin) drift:* Excessive dross on the surface of the solder can disrupt normal wave dynamics. In the case of Sn/Pb solder, Sn oxidizes more easily than Pb. The solder can become Sn-depleted over the long term. This is known as Sn drift. The same is true of Sn-based Pb-free solder alloys, but since some alloys are nearly all Sn (SAC305, 96.5 percent Sn by weight), this effect will be less dramatic. However, other Pb-free alloy perturbations such as dissolution of Cu become much more important. For example, in the case of the eutectic Sn-Cu alloy, the copper content is only 0.7 weight-percent. Small changes in the copper content by means of copper dissolution of copper pads on the board can have a dramatic effect on the melting temperature of the solder. The major cause of Sn drift is from depletion of Sn from contact with copper or species being soldered, but dross creation furthers the depletion of tin.

49.4.4.1.1 Dross-Related Process Defects. Dross can generally change the dynamics at the wave/bond-pad/component lead interface, discouraging adequate pull-back of the solder and encouraging defects. Molten solder droplets can become entrapped in the dross as a result of wave turbulence. Once the droplets are oxidized, they are

unable to rejoin solder in the reservoir. As the dross passes through a PTH pin field intended for soldering, the pins act as a strainer, raking the solder-laden dross, resulting in pin-to-pin short circuits (drossy shorts). This dross-thickened layer can also block the solder wave from effectively contacting PCB land and component lead, and opens (skips) may result.

49.4.4.1.2 Taming Dross. Various schemes have been devised to control dross, such as co-mixing the pumped solder with a mineral oil, which floats to the surface, blanketing the solder from the atmosphere. Liquid reducing agents can be added to the solder as well as fluxes. In the long term, none of these has proven popular. The most widespread method of dealing with dross is manually scooping dross from the surface of the solder reservoir with a ladle at routine intervals based on machine runtime. Machines that vacuum dross are also available and useful.

The use of an inert cover gas has been shown to be effective in reducing dross formation and ensuring best fluxing from no-clean or other weakly activated fluxes. Nitrogen is widely used in this regard. R. Iman et al.[4] have explored the use of formic acid in gaseous form as an additive to the nitrogen atmosphere for the soldering process. The fundamentals of this process were demonstrated by H. H. Hartmann,[5,6] who had shown formic acid to be an effective gaseous fluxing agent for soldering. Dross forms when the solder is exposed to the atmosphere, so limiting atmospheric contact limits dross production. As mentioned previously, nitrogen blanketing of the solder pot and the wave will help limit dross production. Another simple but effective method is to turn off the wave pump(s) when the solder wave is not in use as wave turbulence increases exposure to the atmosphere and increased dross production. Most wave soldering machines have sensors that can detect when a PCB is on its way to the wave. The sensor activates the wave in time for soldering and shuts it down when the board has passed.

49.4.5 Metal Contaminants

Metal contaminants can also affect wave soldering. These stem from three sources: (1) contaminants from the bar solder used to charge the solder pot, (2) slow dissolution of components of the wave solder machine (solder pot, nozzles, etc.) and (3) from the materials joined during the soldering process. As the hot, circulating wave washes over component leads and PCB through-hole lands and pads, materials are dissolved into the solder. Even if leads and pads are solder-plated or solder-dipped, there is the opportunity for adulteration of the solder in the reservoir, dependent on coating composition, thickness, underlying basis metals and impurities within surface finishes as well as resident time in the wave and wave temperature. Copper, gold, silver, additional tin or lead, and intermetallic compound precipitates are all common contaminants derived from the slight dissolution of component lead and pad or coatings during soldering. Refer to the previous chapter on flux for a discussion of these metals in the solder process.

Solder reservoir contamination can have significant process impact, eventually altering melting range of a solder, injecting particulates into solder joints, and altering wetting characteristics. This may lead to an increase in shorts or opens or even result in solder joint embrittlement. The composition of the wave reservoir can be assayed by a testing service to determine its impurity content by scooping a small amount of solder and checking its solidus and liquidus points (melting range) against a pure standard. This method is less accurate than chemical analysis for contamination assessment and is inadequate for detecting the presence of some impurities such as intermetallic precipitates that may not affect the solder alloy composition.

Excessively high temperatures in the solder reservoir and low speeds through the wave should be avoided to limit dissolution of component leads, PCB pads, and PTH barrel

materials. Note that the solder wave is maintained at fairly high temperatures, generally 245 to 270°C, depending on the solder alloy and thermal mass of the assembly being soldered, but board exposure is short (2 to 10 s). Compare this to oven reflow, where time above liquidus is typically 30 to 90 s. As in oven reflow, thermal shock in wave soldering can lead to component cracking or degradation problems, so the preheating rate should be tempered to match component vendor recommendations—sometimes to as little as 2°C/s.

Bar solder impurities such as aluminum, gold, cadmium, copper, and zinc can increase surface tension of the solder and make the process more prone to bridging. D. Bernier[7] reviews some of these contaminant effects and describes empirically derived impurity limits.

49.4.6 Hygiene

Airborne tin, metal oxide fumes, and other metal particulates are unhealthy to breathe. Risks associated with lead oxide intake are well documented, but inhalation of any particulate should be considered potentially hazardous. The health risks associated with working with Pb-free alloys are not as well-known as those of the Sn-Pb system, but likely less of a risk than the latter. With any alloy, precautions should be taken, especially during wave-solder system maintenance procedures, to preclude particulate inhalation. Donning a personal particulate mask and washable or disposable outer garments (contamination suit) is recommended. Proper hygienic venting of the work area, not only during maintenance procedures but for normal soldering operation, is necessary.

49.4.7 Wave Solder Machine Configuration

In most factories, defect levels at the wave step are higher than those for the oven mass reflow process. The defects can generally be correlated to process setup, inadequate process control, bad PCB design, or any combination of the three. Although wave soldering has been around for a long time, it is still not a very well controlled process, due mainly to varying machine configurations and number of process variables associated with this process.

Many wave designs are available from the various wave-solder machine manufacturers. There are wave machines that provide multiple smaller, turbulent wave(s), which are best for leadless components such as surface-mount passive devices (resistors, capacitors, etc.). Smoother-flowing waves are recommended for components with leads and through-holes as well as coarse-pitch surface-mount devices. Often a combination is used where the board first travels over a turbulent standing wave and then immediately over a smooth wave. This is a very effective method as the first (turbulent) wave not only ensures good soldering of passive devices in tight fields, this strategy initiates wetting of the PTH components which is completed in the second (smooth) wave. The extra boost of the first wave can is useful for boosting the temperature of the board for soldering of PTH pins but it also has to be controlled carefully so as not to induce re-reflow of top-side SMT components.

Wave dynamics are dictated by process values as well as the materials in contact with the wave. As the solder wets to the circuit board materials, solder wetting contact angle and solder viscosity impose wave peel-off characteristics (Fig. 49.27).

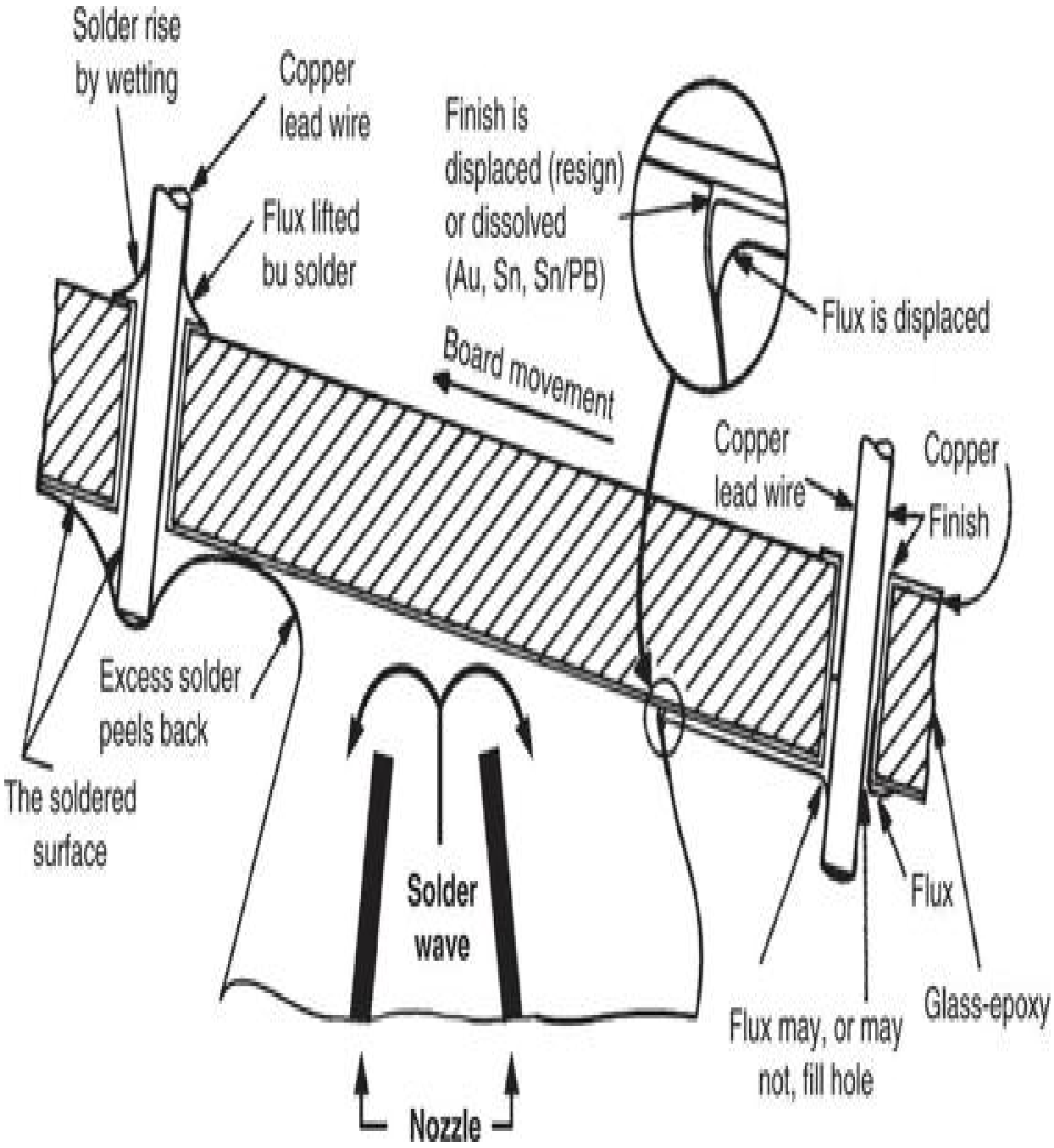

FIGURE 49.27 PCB passing over a solder wave. Flux, sprayed or foamed onto the bottom of the PCB and helped by the process heat, is wicked between the PTH barrel and the component pin. Note the tendency to pull a web of solder from the wave as the board passes over. The solder-wettable lead-pad combinations become one with the wave as the board passes through it. Good soldering relies on flux-aided wetting and the ability of the solder web to break cleanly from the wave when surface tension forces are exceeded as the board moves away from the wave and the solder meniscus stretched to its breaking point. (*Courtesy of Alpha Metals, Inc*.)

The hot-air knife, as previously described, is sometimes useful in removing unwanted solder bridges from between component leads while the solder is still molten. This is especially useful in connectors and PGAs with interstitially arrayed pin fields (Fig. 49.28).

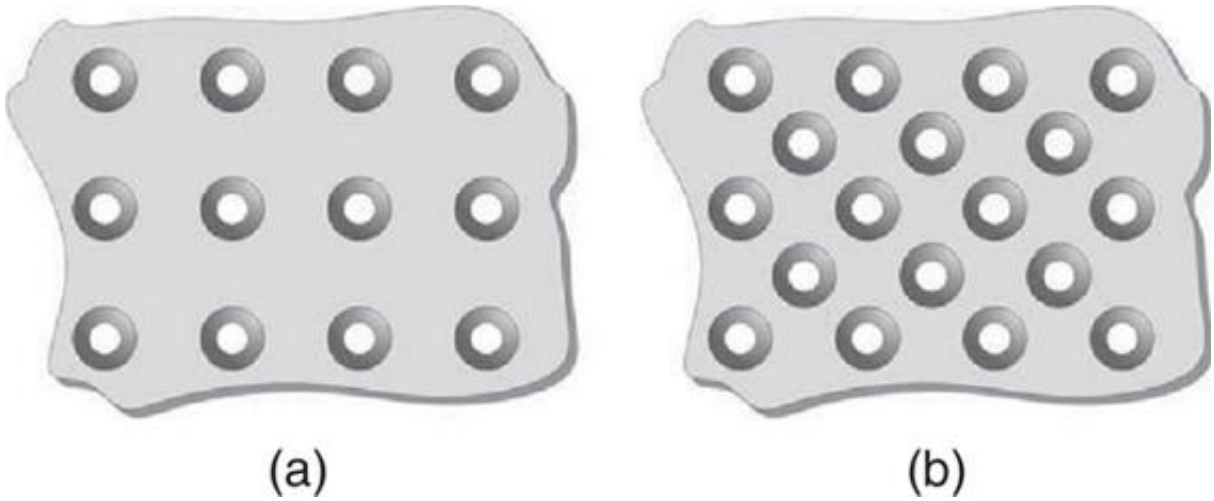

FIGURE 49.28 Pin field types. Circuit board segments with (*a*) orthogonally arrayed connector PTH pattern and (*b*) interstitially arrayed connector PTH pattern.

As the wave moves through the frustrated pin field of the interstitial array, some fluid flow stagnation may occur resulting in solder opens or insufficient PTH barrel fill. In addition, the interstitial pin field may not drain solder well enough in other areas, causing solder bridge formation (shorting multiple pins together with solder). Numerous wave solder machine designs and standing wave shapes are aimed at improving the soldering yields of these large packages, but there is no clear choice in wave style for all applications.

In designing circuit boards for the wave-soldering process, it is important to anticipate the flow of the wave over the bottom surface of the board. Placing tall components in front of short component fields should be avoided and component spacing should be maximized; otherwise, solder from the wave may be blocked from washing over the targeted joining

area. The taller component may shadow the flow of the wave, causing areas of flow eddying or stagnation in the vicinity of shorter components behind it. Also, if the SMT pad via extends all the way through the PCB, then its placement should be as far away from the leads as is practical to avoid the aforementioned problems of re-reflow.[8] Ideally the bottom-side via pad is shielded from the solder wave with a fixture (pallet) or by applying a mask such as tape or a peelable liquid masking agent that gels and dries at or near room temperature and leaves no appreciable residue when removed. Such peelable masks are made for wave soldering and rework applications. Other methods of shielding the PCB will be discussed in the next section.

49.4.8 Wave-Solder Pallets

The pallet, also known as the selective soldering pallet, or shield is a masking device meant to protect certain secondary (bottom-side) components, features or areas of the PCB during the wave soldering process. It is used to shield specific areas of the board from flux during flux application and from heat and solder during the wave solder process. Its top-side is designed with a recessed nest for the PCB and retention features to hold the PCB flat within the nest and tight against the shielding material. There are cutouts that expose those areas to be soldered to the flux and the standing solder wave (Figs. 49.29 and 49.30).

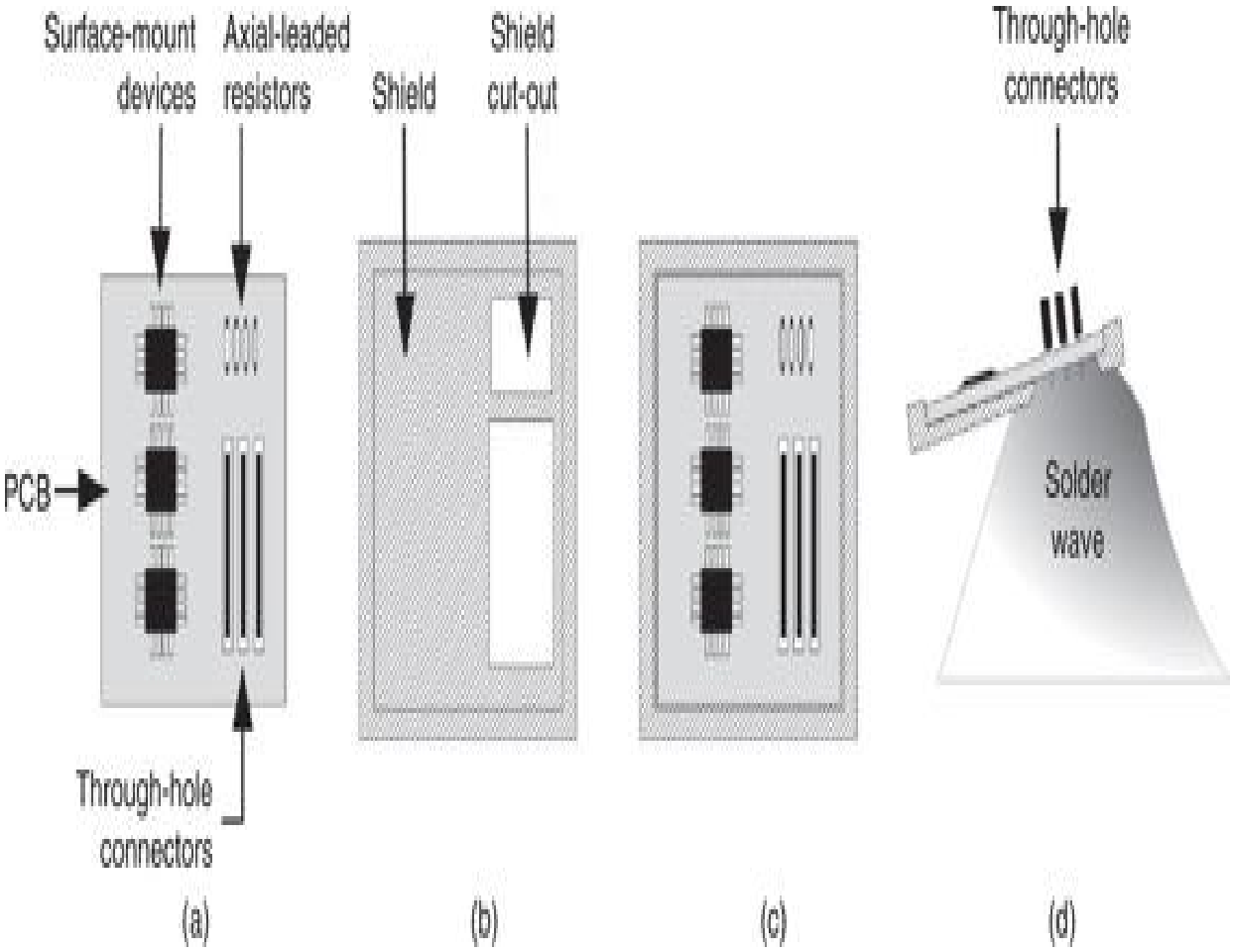

FIGURE 49.29 (*a*) PCB with SMDs and PTH part. (*b*) Shield (pallet) with cut-outs for PTH components. (*c*) PCB nested into shield. The shield protects SMDs from exposure to the solder wave. The cut-outs allow the wave to contact solder-tails. (*d*) The shielded PCB passing over the solder wave. The cut-out allows the PTH connector solder-tails to contact the wave for soldering.

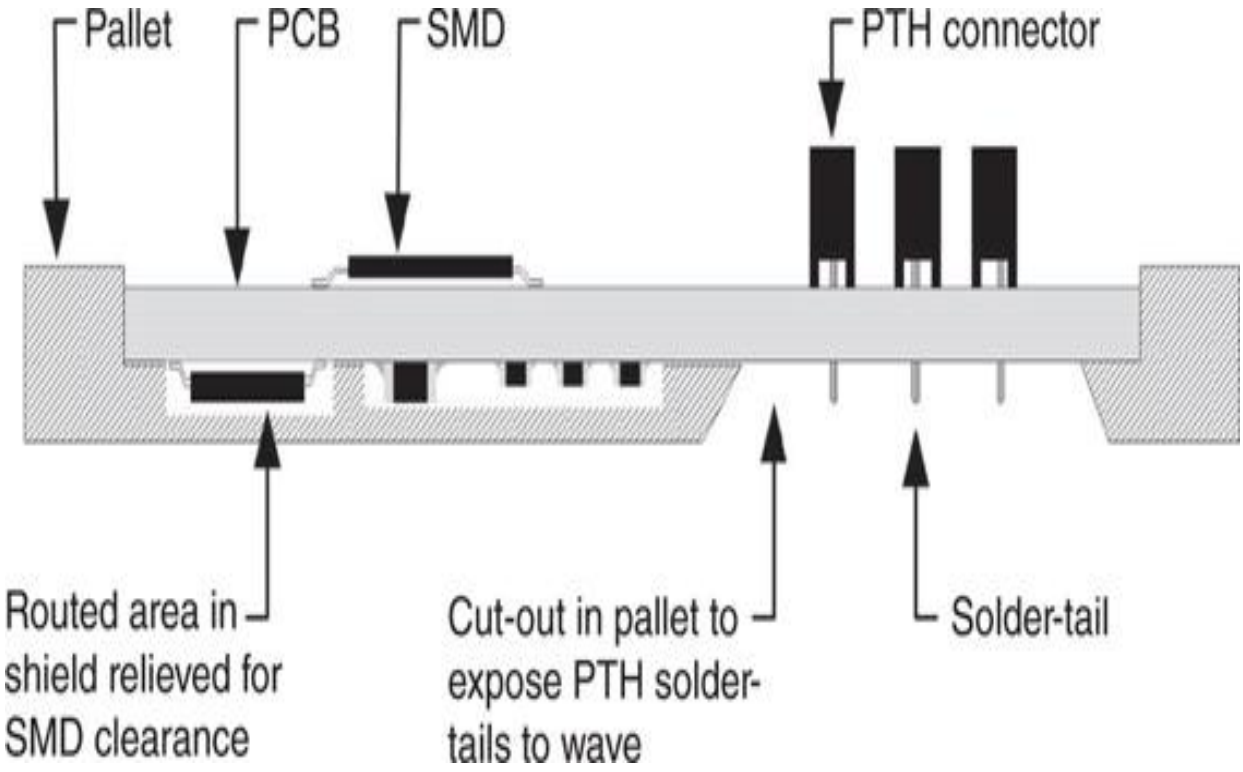

FIGURE 49.30 A wave-solder pallet for a mixed-mount PCB. Note the routed area to accommodate SMDs on the bottom-side of the PCB and the open area to allow exposure of solder-tails to the solder wave.

Wave solder pallets are generally is made of a non-wetting, electrostatic discharge (ESD) safe, thermally insulating material such as Delmat or other high-temperature epoxy-glass composites. Titanium has been shown to be useful for shielding also, although such pallets are very expensive.

Pallets are designed for repeated use but will degrade with time. Some fluxes will attack the epoxy of the glass-epoxy lay-up over time. Pallets may warp. If not cleaned routinely, they may build up hardened flux residues that will prevent proper seating of the PCB. They also may decompose with age and use. Pallets should be inspected after each use and before reuse.

49.4.8.1 Pallet Uses. A pallet may serve several purposes, including the following:

- Protection of bottom-side SMD components and their previously manufactured solder joints
- Shielding pad vias and via fields from solder[8]
- Masking edge-card gold fingers from solder (note: additional protection may be needed beyond the pallet, but the pallet is a first line of defense)
- Protecting press-fit connector sites by preventing solder from filling these holes
- PCB distortion prevention
- Protection of in-circuit test-points from flux and solder
- Shielding of plated mounting holes for attachment to the chassis
- Preventing flux deposition from where it is not needed

49.4.8.2 Wave-Solder Pallet Design. Although the wave solder pallet can prevent damage to a board, if not properly designed it can also interfere with soldering. Here are some design guidelines:

- *Thickness must be limited* such that the PCB will be in contact with the wave.
- *Must be thick enough* to provide the rigidity needed to hold the board flat during the process.
- *Must be flat enough* such that the PCB will seal against the pallet to prevent solder from flooding where it does not belong.
- *Pallet support must* include enough areas of support under the board so that a thin, large PCB will not sag as it traverses the wave.
- *Has to be durable* to survive the temperature regime, repeated use and direct exposure to flux (an acid) and molten solder.
- *Openings on the underside of the pallet should be chamfered* to promote solder wave contact in areas to be

soldered. The chamfers help prevent “gas lock,” enhancing the ability of air to be displaced by the molten solder ensuring smooth entry and exit at each pallet opening (Fig. 49.31).

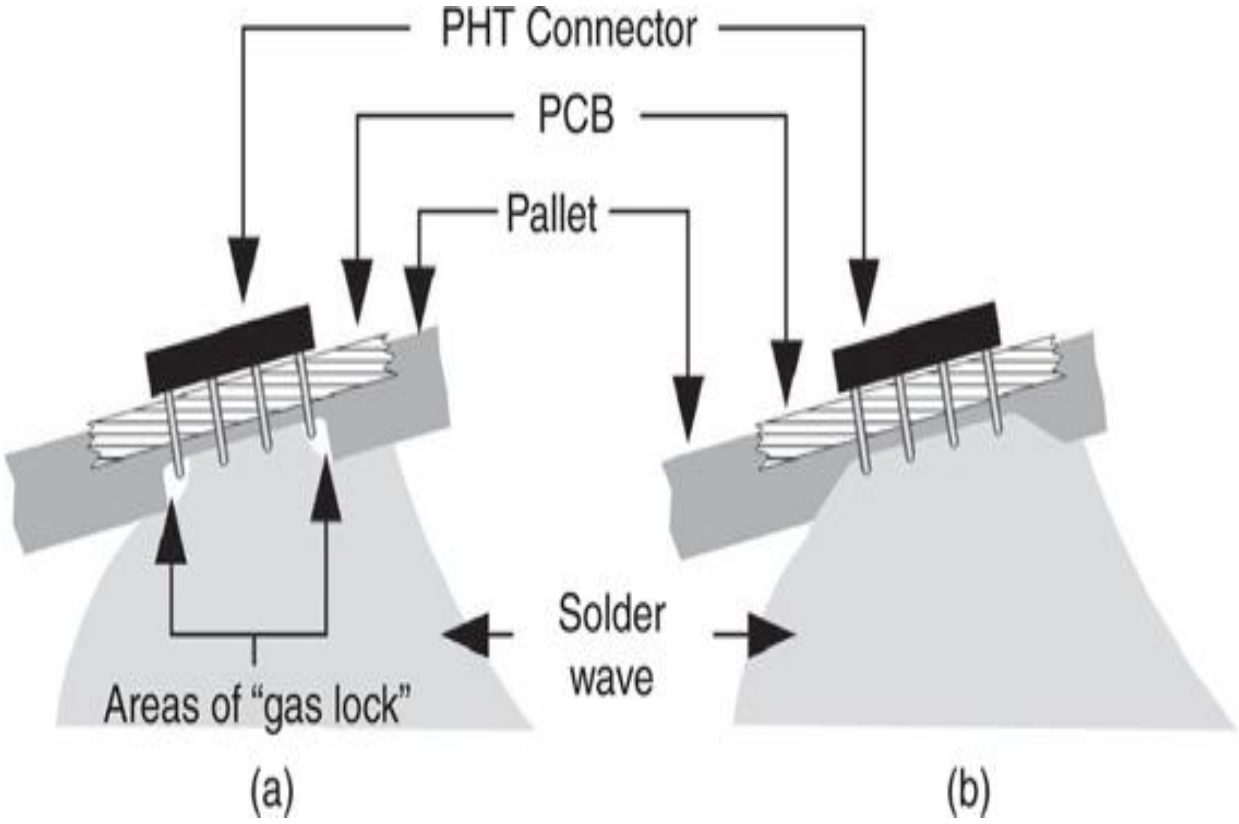

FIGURE 49.31 Openings on the bottom of wave solder pallets should be chamfered in order to promote flow of the molten solder from the wave. “a” depicts a pallet without a chamfered opening. “Gas lock” or “gas pockets” (entrapped air) may prevent the solder wave from touching some of the connector pins. No soldering or poor soldering will occur here. “b” has a pallet opening that is chamfered to promote complete solder coverage, minimizing “gas lock”, and enhancing solder flow to all pins.

- *Pallet openings should be as large as possible* for good PCA preheating and to permit-free access of the molten solder wave to the targeted areas for solder joint formation. The larger the pallet opening, the better the heating from preheaters and also from contact with the wave. If solder-tails are too close to a pallet opening, the molten solder of the wave may not make good contact

with pins to be soldered (Fig. 49.32). Further, the pallet will act as a thermal sink and may inhibit local heating. If solder-tails and plated through-holes are not heated sufficiently they will not solder properly.

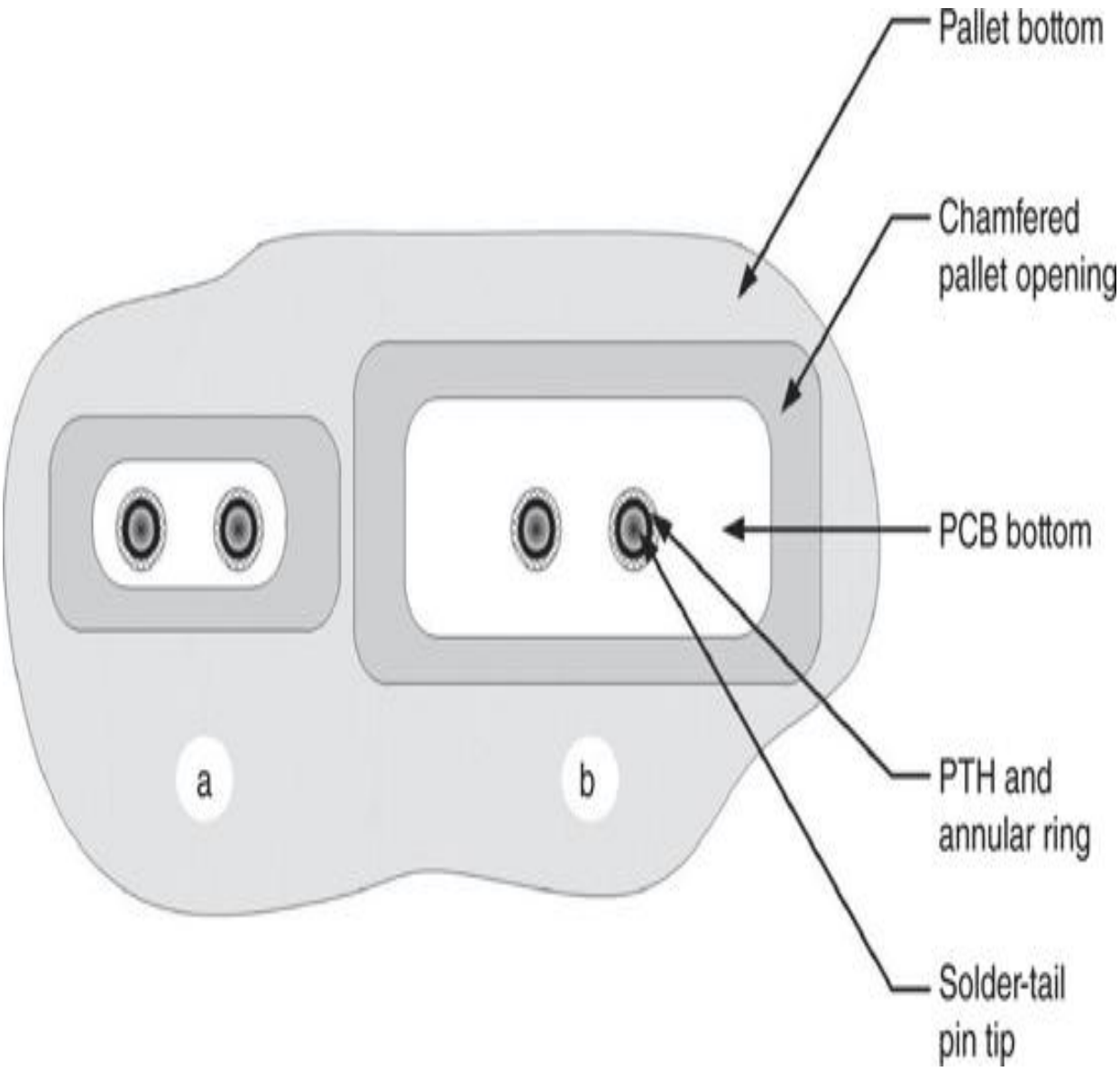

FIGURE 49.32 Small pallet opening vs. large pallet opening. Depicted is the bottom-side of a wave pallet showing two chamfered pallet openings. Within each opening is the bottom-side of a PCB and a set of plated through-holes with pins. Wave soldering success for “b” will be better than “a” since “b” has more surface area for better heating and significantly more accessibility to the solder wave.

- *Board-locks and over-clamps* should be incorporated into the pallet design (Fig. 49.33). The board-locks clamp the PCB into the pallet and seal it against the surface of the pallet. This prevents solder from intruding between the pallet and the PCB. Board-locks are rigid, spring-loaded, high-temperature fingers that can be rotated out of the way or removed to permit loading and removal of the PCB.

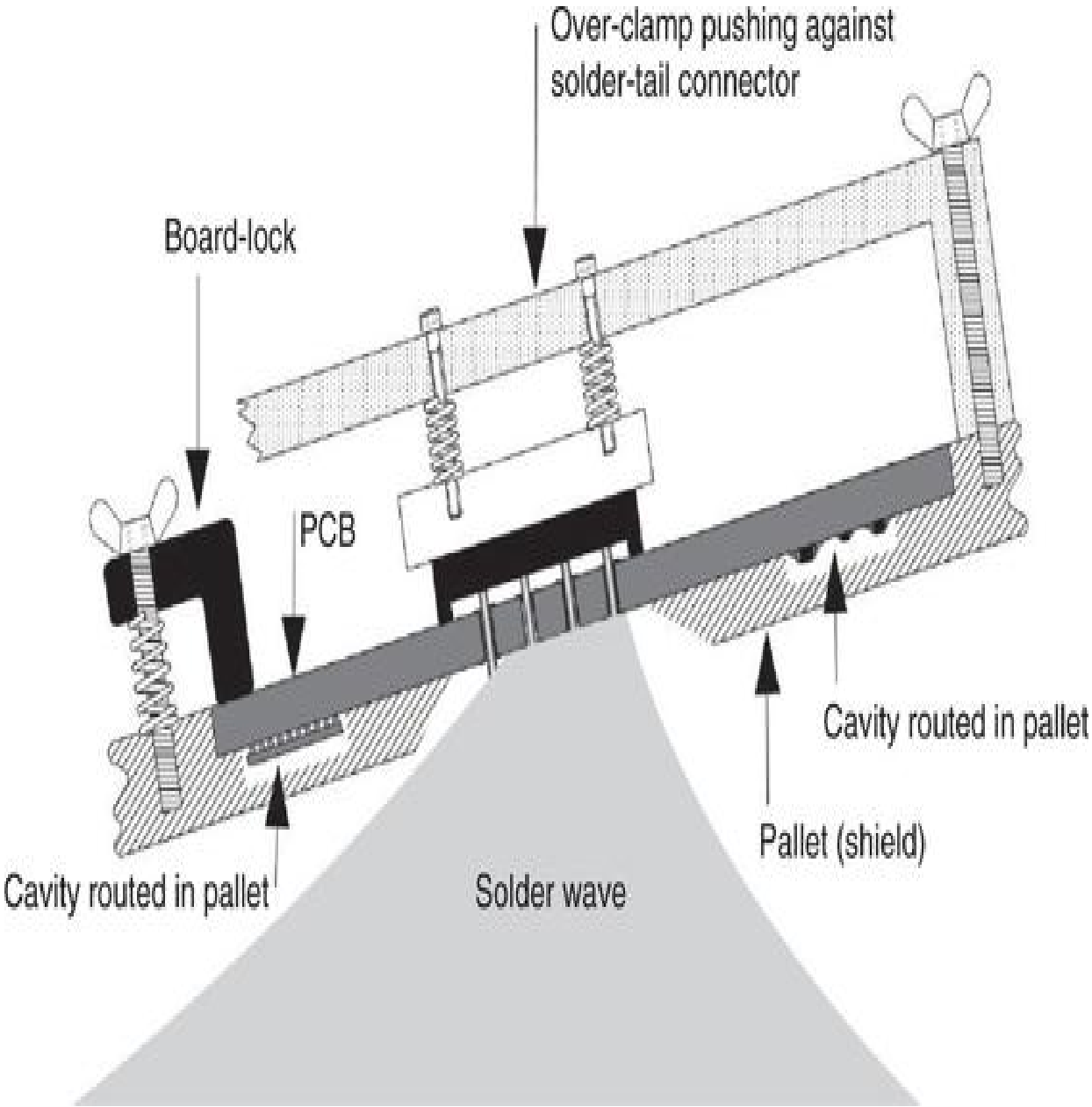

FIGURE 49.33 Advanced features of a wave solder pallet (shield). The pallet is cut out to expose solder-tails of the connector. The cut-out is chamfered to enhance the flow of solder over the connector pins. There are cavities on the bottom-side of the shield to allow clearance for previously soldered surface-mount components. One of several spring-loaded board locks is depicted, holding the PCB flat against the pallet. There is a partial view of an over-clamp, used to prevent the PTH connector from floating up when exposed to the molten solder wave.

- Over-clamps further help to seal the board to the pallet especially in the middle of large PCBs. They are generally incorporated for holding connectors and other nonclinched parts from buoying up when contacted by the molten solder wave. The design must take into consideration the thermal mass of the clamp and its influence on proper heating of the PCB during the wave process. Many PTH connectors have staking pins which hold the part by friction-fit onto the board. When this is the case, an over-clamp may not be necessary.

49.4.9 No-Clean Flux Residue and In-Circuit Test

During wave soldering, most of the flux from the process is either consumed or washed off the bottom-side of the board by the action of the molten solder wave. Any flux residue that seeps between the pallet and the board, will not be removed by the wave process. If this residue were to cover in-circuit test pads, it would inhibit in-circuit test probe contact. Care should always be taken to minimize flux deposition for wave soldering for this reason and to minimize flux usage and associated expense. Pallets should be inspected and cleaned frequently to ensure that flux residues are not being transferred to in-circuit test points from a poorly maintained pallet.

49.4.10 Designing PCBs for Wave Soldering

Complex PCAs with area array devices and fine-pitch SMT components (mixed-mount assemblies) on boards thicker than about 2.36 mm (0.093 in) may be difficult to wave-solder if care in layout is not observed. There are many important PCB design criteria that should be considered to enhance PCB wave soldering:

- *Clearance from the edge of the board to previously soldered SMT components* must be sufficient such that the wave solder machine's edge-hold conveyor does not interfere with these components.
- *PTH component spacing from the edge of the board* is dictated by wave flows and the surrounding structure. The wave dynamics at the outer edges of the wave may be different than inward body of the wave. Place difficult to solder components inward for best success at soldering. F. W. Kear's review[10] of the thermal aspects of through-hole solder joint formation offers a glimpse of the physical phenomenon of the wave-soldering process.

When possible, avoid placing PTH components directly against the edge of the board. There must be clearance from the PCB edge to the pallet to allow the board to nest within the pallet. A selvage edge (a removable and disposable board-edge extension that is part of the board itself) can be designed into the PCB or PCB panel (Fig. 49.34). After wave soldering, the selvage edge can be removed by rotary cutter or routing. Note that post-solder routing is not preferred, especially for no-clean soldered assemblies. The abrasive router dust may remain within connectors and scratch connector contact surfaces or mating connector contacts. The vibration, especially from poorly maintained routers or

from inadequate router fixtures, may also affect the reliability of certain components.

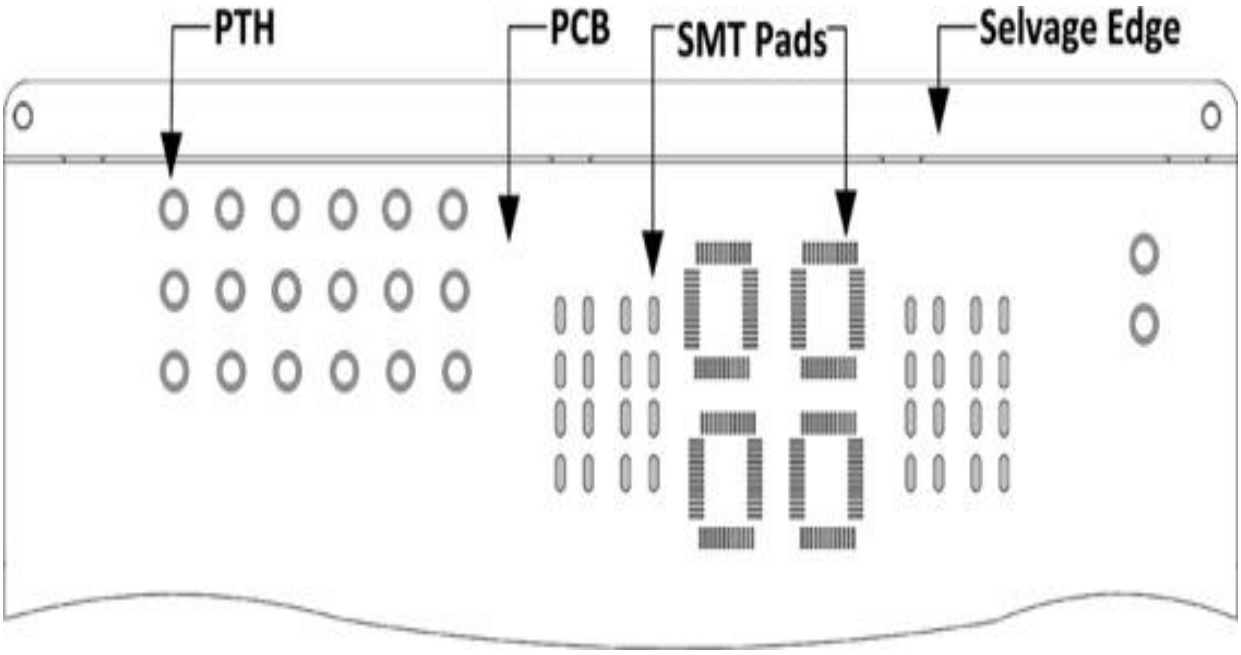

FIGURE 49.34 Board schematic showing a removable selvage edge; a disposable edge. In this case it was useful to enable wave soldering of the PTH connector near the finished edge of the board.

- *PCB width must be appropriate for the wave solder machine:* It must physically fit on the machine and components that will be wave soldered must be within reach of the solder wave.
- *Components should be oriented in directions favorable to good soldering:* Long connectors are generally oriented with their long axis parallel to the long axis of the solder wave (perpendicular to the direction of travel on the wave machine) to minimize solder bridging. The same applies to passive devices and device fields. The field should be oriented with the long axis perpendicular to the direction of travel through the wave solder machine. The device itself should be oriented with long axis perpendicular to direction of travel.

- *Minimize PCB thickness:* Since thicker boards are more difficult to wave solder. Boards thicker than about 2.54 mm (0.100 in) are notably difficult to wave solder IF there are surface-mount devices on the primary side of the board. Getting the board hot enough for good PTH barrel fill on such boards will often result in re-reflow of previously soldered surface-mount devices. Care in profiling and appropriate thermal shielding are a must for thick PCBs. It should be noted that very thick PCBs (even >6.35 mm (0.25 in) can be effectively wave soldered. Such boards rarely carry intricate SMDs and re-reflow of SMDs is of less concern so aggressive preheating and slow transit times through the wave are not a problematic.
- *Plated through-holes should be specifically tailored for the component pin* (also called solder-tail): Component manufacturers will generally provide such information, but there are industry standards and recommendations dealing with this topic such as IPC-2221.[11]
- The clearance between component pin and PTH barrel wall must be small enough to provide proper conditions for good capillary wicking of the solder from the wave as it wets to pin and barrel. If made too small, volatiles from the flux will easily expel the wicked solder from the PTH resulting in large voids that may detract from reliability. If made overly large, the hydrostatic pressure from the wave may cause solder to flood to the top-side of the PCB and cause solder shorts (bridges).
- *Avoid PTH components on both sides of the board:* Restrict the design such that wave soldering occurs only on the secondary side (bottom-side) of the board. PCBs with wave soldering on both sides are notably difficult to process. Bottom-side component height may interfere with machine clearances. Determine whether SMT or press-fit components can be used in the design to obviate the need for a second wave-soldering operation. The industry-

standard preference is to restrict all wave-soldered components to one side (components inserted through the primary side) of the PCB.

- *Incorporate heat-relief features into the PCB*, especially around power and ground pins of PTH components. Such pins are generally connected to multiple, thick copper conduction planes within the PCB. These planes are buried in the board and glass-epoxy circuit boards are somewhat thermally insulating, therefore they are difficult to heat sufficiently for proper soldering. The process heat applied during wave soldering (preheat and from the wave itself), instead, is conducted through the PTH barrels and into any attached power and ground planes. If the PTH barrel is not heated sufficiently, neither good fluxing nor proper solder wetting will occur.

Heat-relief structures are designed around the point where the PTH barrel is connected to a copper ground or power plane. These features resemble spoked pads; or more appropriately “anti-pads.” In the heat-relief design the PTH barrel is connected to the plane by spokes of copper rather than a broad, planar connection (Fig. 49.35). These spokes are designed to provide sufficient electrical conduction and at the same time are designed to limit thermal conduction away from the PTH barrel (the soldering target).

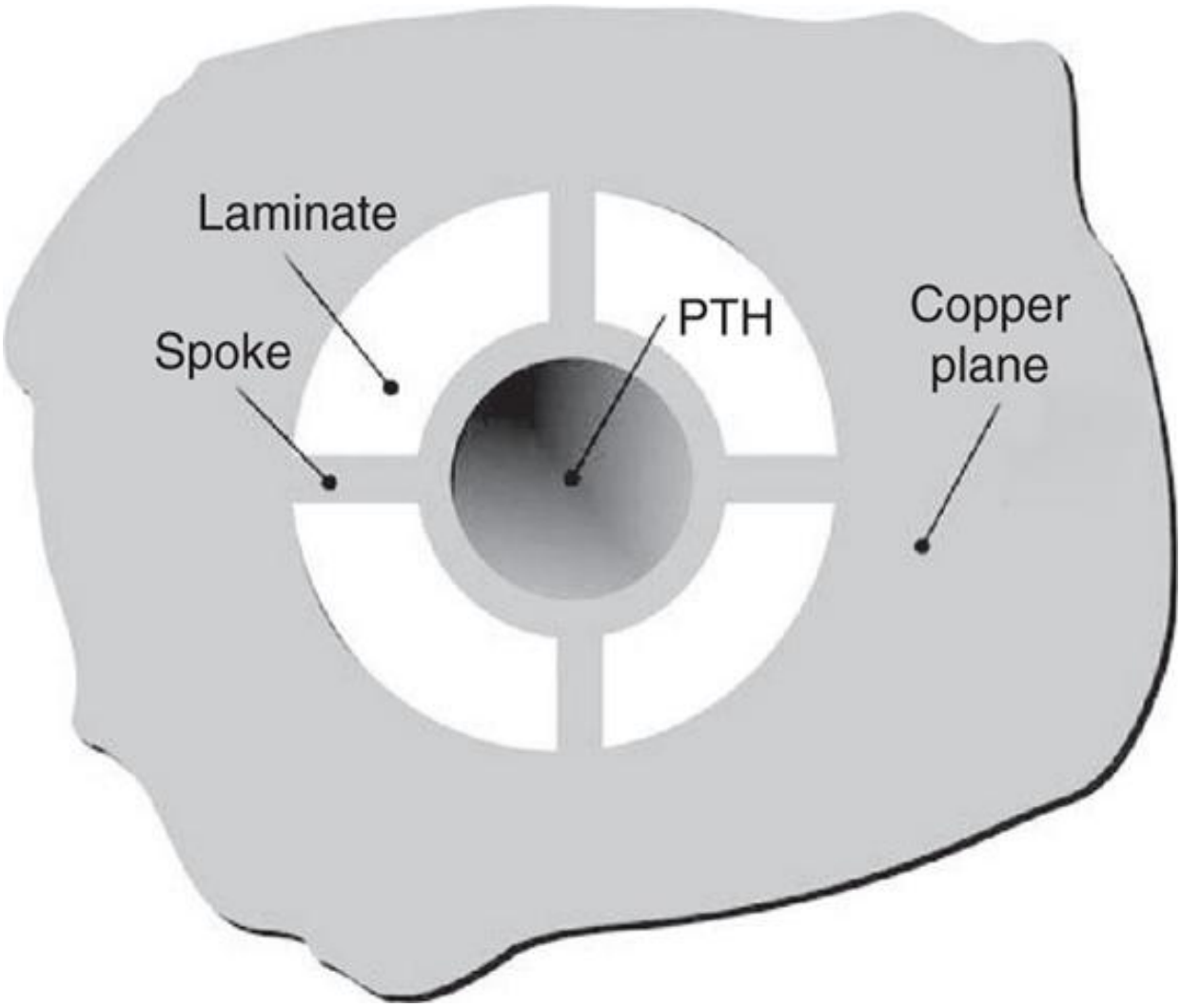

FIGURE 49.35 Schematic of a thermal relief features (antipads) within a PCB. The spokes connect the PTH barrel to the electrical conduction plane and limit thermal transfer from the PTH barrel to the conduction plane. The limited thermal path enhances heating of the PTH for soldering. Care must be taken in the design so that there is sufficient electrical conduction through the spoke for proper circuit operation and to avoid ohmic heating.

- *Limit the number of PTH barrel attachments to power and ground planes within the PCB* when feasible. Each attachment point will result in thermal dissipation into the copper plane even with antipad construction. This thermal loss will detract from the soldering process making the job of preheating and solder wetting all the more difficult.
- *Cluster PTH components and provide sufficient clearance between them:* Group wave-soldered components together

so there are fewer and larger openings in the pallet. It also may save time and materials at spray-fluxing. Avoid interspersing nonwave soldered surface-mount components within wave-soldered component fields. Conversely, avoid designs that place an isolated PTH component amid a field of SMD components. Such placements necessitate small wave pallet openings that inhibit: solder-wave fluid flow; preheating; wave contact.

- *Do not place wave soldered components near gold fingers:* Clearance from gold fingers is required so as not to contact the gold fingers with solder or foul them with flux. The gold finger should be away from pallet nest edges. Covering the gold fingers with an acrylic-based, high-temperature adhesive tape will help to keep solder and flux from contacting the gold fingers. The tape is not an effective mask if exposed directly to the solder wave.
- *Test pads positions should be designed as far from intended wave-solder pallet openings as possible* to avoid contacting them with solder or covering them with flux. No-clean flux residue is an effective electrical insulator and will inhibit good electrical contact by in-circuit test probes.
- *Restrict tall components to the primary side of the PCB:* Tall SMT components on the bottom-side of the board may interfere with wave soldering and prohibit adequate wave pallet design.
- *Keep the most complex SMT components as far from PTH components sites as is practical:* Devices such as fine-pitch SMDs, area-array devices, etc., may re-reflow if too close to wave soldered components. Re-reflow of these components may melt previously formed solder joints causing electrical opens, or the solder from the joints may be drain down pad vias compromising solder joint reliability.

49.5 WAVE SOLDER DEFECTS

There are many types of wave-soldering systems, each with its unique advantage as claimed by the manufacturer. The soldering engineer has to assess these improvements as they relate to the type of assembly being soldered. Wave soldering has had over 60 years to mature, but the degree of equipment intricacy and large number of process variables attest to the complexity of this process. If the machine and processes are not understood or not properly controlled, wave-soldering defects such as skip soldering (electrical opens) and bridges (electrical shorts) will occur. Another important defect is the influence of secondary-side wave soldering on primary-side surface-mounted components. If parameters are not controlled properly, it is possible to cause primary-side SMDs to reach reflow temperatures. This can induce solder opens, shorts, or solder-starved joints. This phenomenon is most commonly associated with thin, densely populated, double-sided PCBs with fine-pitch surface-mount devices such as quad flat packs and BGAs soldered to the primary side of the board. Thermal conduction from the wave through the board itself, through electrical vias and along electrical traces in and on the board, may provide enough heating to cause previously soldered parts to reflow again. Solder can be drained away through vias or wicked-up surface-mount component leads, resulting in opens or weakened soldered joints with an extreme hourglass-shaped attachment of solder from the bottom of the lead to the bonding pad.

A common defect associated with no-clean wave soldering is the seepage of flux between the pallet and the board. The resulting flux residue may inhibit in-circuit test probe contact. Care should be taken to ensure that the board fits well into the pallet nest, is rigidly indexed within the nest of the pallet, and is adequately retained against the pallet

surface. As a pallet ages, it may shrink, take on twist, or bow and even delaminate. All of these may interfere with proper board seating. Buildup of flux residues on the pallet may also prevent proper seating of the PCB into the pallet nest and allow board contamination by solder or flux.

If a PTH component body is seated tightly against the surface of the PCB, a gas pocket may form at the primary side of the hole. The pressure from gases evolved from the flux or just from entrapped air may work to either block or expel molten solder wicked into the PTH barrel. This results in either inadequate PTH fill or excessive solder void formation.

This can be remedied by applying a small spacer under the component to keep it from contacting the PCB as shown in Fig. 49.36. The spacer must be made of a heat-resistant material such as silicone or a dot of SMT glue on the PCB surface. If SMT glue is used, it should be cured prior to component placement, otherwise efforts to remove the component during rework, if required, will be confounded. Ensure that the glue does not foul solderable surfaces.

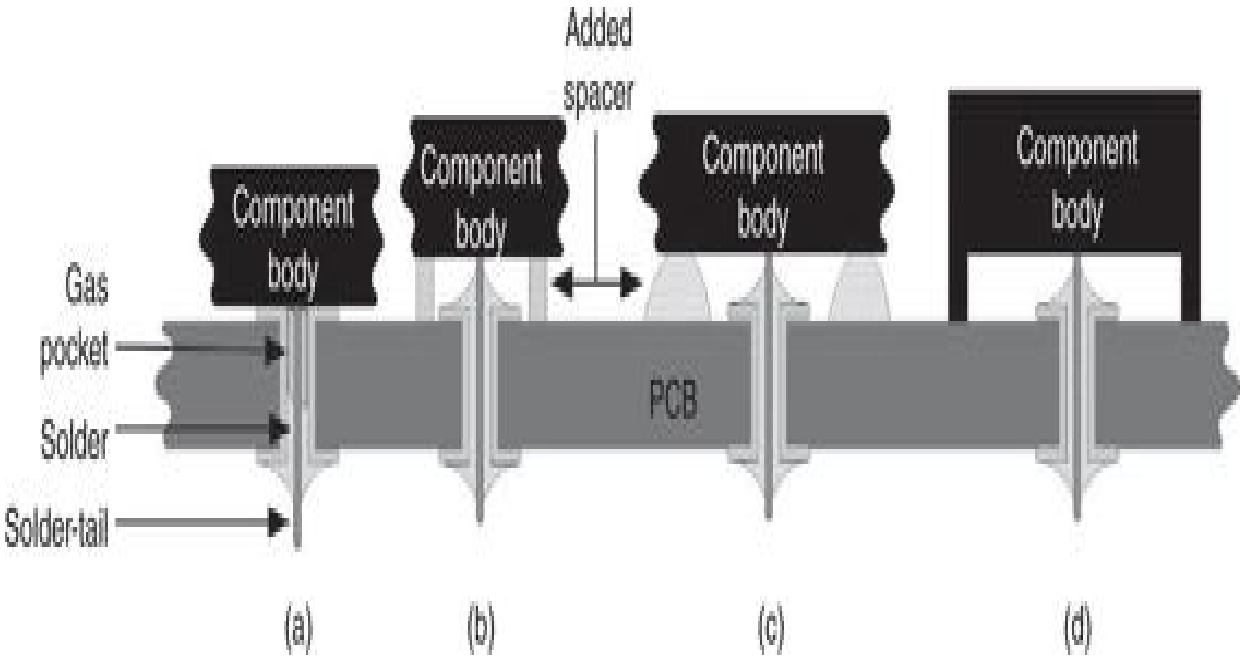

FIGURE 49.36 A component body tight atop a PTH can seal it causing “gas-lock” which retards or expels molten solder. (*a*) Component tight on PCB with large solder void; (*b*) silicone bumpers added to space the connector body off the PCB; (*c*) surface-mount glue can be used as a spacer also, however care must be taken not to contaminate solder surfaces; (*d*) many PTH connectors and parts have stand-offs molded in to prevent “gas-lock.”

When a stand-off is add as depicted, it is important that the sufficient solder-tail protrude to initiate solder wicking and to allow for good solder fillet formation. Both are needed for adequate PTH solder joint strength. Some connectors come with features molded into the insulator body to allow proper stand-off when the component is mounted properly.

Probably the most common defect in PTH soldering is the void; a lack of wetted solder within the PTH and on its accompanying solder-tail. Use the latest version of IPC-A-610[12] as a guide to assess the quality of PTH solder joints. There are several reasons why voids may be present in the PTH solder joint that fall into several broad categories (Table 49.2):

TABLE 49.2 Origin of Poor Wave Soldering as a Result of Solder Void Formation

Effect	Reason	Comment
Thermal	Board too hot	• Solder flux has burned off and either the PTH or the solder-tail has re-oxidized or the flux has reached such a high temperature that it has "caramelized" (denatured and created a lacquer) coated what should be solderable surfaces • Too much preheat • Too much dwell time in wave

	Board too cool	• Inappropriately low temperature caused solder to solidify before it can fully wet pin and barrel.
		  • From board design (PTH barrel connected to too many thick, conductive planes)
		  • From inappropriate wave solder pallet design (prevents proper PCB preheat or results in too little exposure of solder-tails to the molten solder wave).
		  • Insufficient preheat
		• Insufficient dwell time in wave
		• Temperature too low for proper flux activation. The flux has not stripped oxides from solderable surfaces and the oxides inhibit solder wetting

Material	Bad plating	• Poorly plated PTH or solder-tail will not allow solder to wet for joint formation
	Contaminated surfaces	• Contaminated PTH or solder-tail will not allow solder to wet for joint formation
Inadequate Flux Coverage	Inappropriately low volume of flux dispensed	• Too little flux dispensed prior to wave soldering • Improper distance of spray-flux nozzle to PCB
	No flux dispensed	• Improper fluxer set-up • Fluxer malfunctioned during the flux application process (clogged spray-fluxer nozzle)
Expulsion	Solder expelled from PTH by soldering flux	• Too much flux within the PTH may volatize and expel molten solder from the PTH during the solder-wetting process
	Expulsion from "gas-lock"	• Inadequate stand-off: if component sits too tightly atop PTH flux or entrapped air may expel flux and molten solder • If wave pallet design is poor, gas pockets may inhibit free flow of the wave over PTH solder-tails
	Porous PTH	• If the PTH barrel has pin-holes in its plating that are open to the laminate (glass/epoxy layer), the laminate may outgas during the soldering process and produce enough gas to displace solder in the barrel

Defects such as bridging and opens have been discussed previously.

49.6 VAPOR-PHASE REFLOW SOLDERING

Because of safety, environmental concerns and compliance with the Montreal Protocol for the reduction of ozone-depleting chemicals, this soldering technique had fallen out of favor. With the advent of Pb-free soldering, interest increased in vapor-phase soldering for SMT applications, but it is likely that it will continue to remain a niche application. Due to its continued diminished status, vapor-phase reflow is covered only briefly.

49.6.1 Basic Process

As for other reflow techniques, the board must be supplied with sufficient solder and flux for solder joint formation. Most commonly, solder paste is stenciled onto circuit board pads. Components are placed onto the solder paste in preparation for reflow. The board is conveyed into the reflow chamber, where it is exposed to the vapor phase of a boiling liquid. This liquid is inert with respect to the solder and board. It is a dense synthetic organic chemical of high molecular weight and high boiling point (slightly higher than that of solder liquidus but not high enough to damage the circuit board or components). Historically, chlorofluorocarbons were used, but now only hydrofluorocarbons (HFCs) are acceptable due to environmental concerns. Material cost for such chemicals are high, at several hundred dollars per pound.

When conditions are optimized, the hot vapors begin to condense on the cooler PCB, heating it. When sufficient

energy is transferred, the solder paste is activated and the solder melts wetting to the component leads and PCB pads. As the heat is lowered or the board is removed from the hot vapor, the molten solder solidifies, bonding component leads to circuit board pads.

49.6.2 Machine Subsystems

The vapor reflow soldering machine is composed of four main subsystems: conveyor, reservoir vessel, cooling coils, and heaters. The heated vessel has cooling coils surrounding it, placed well above the level of the liquid in the reservoir. These condense the vapors, returning the majority to the reservoir, as shown in Fig. 49.37.

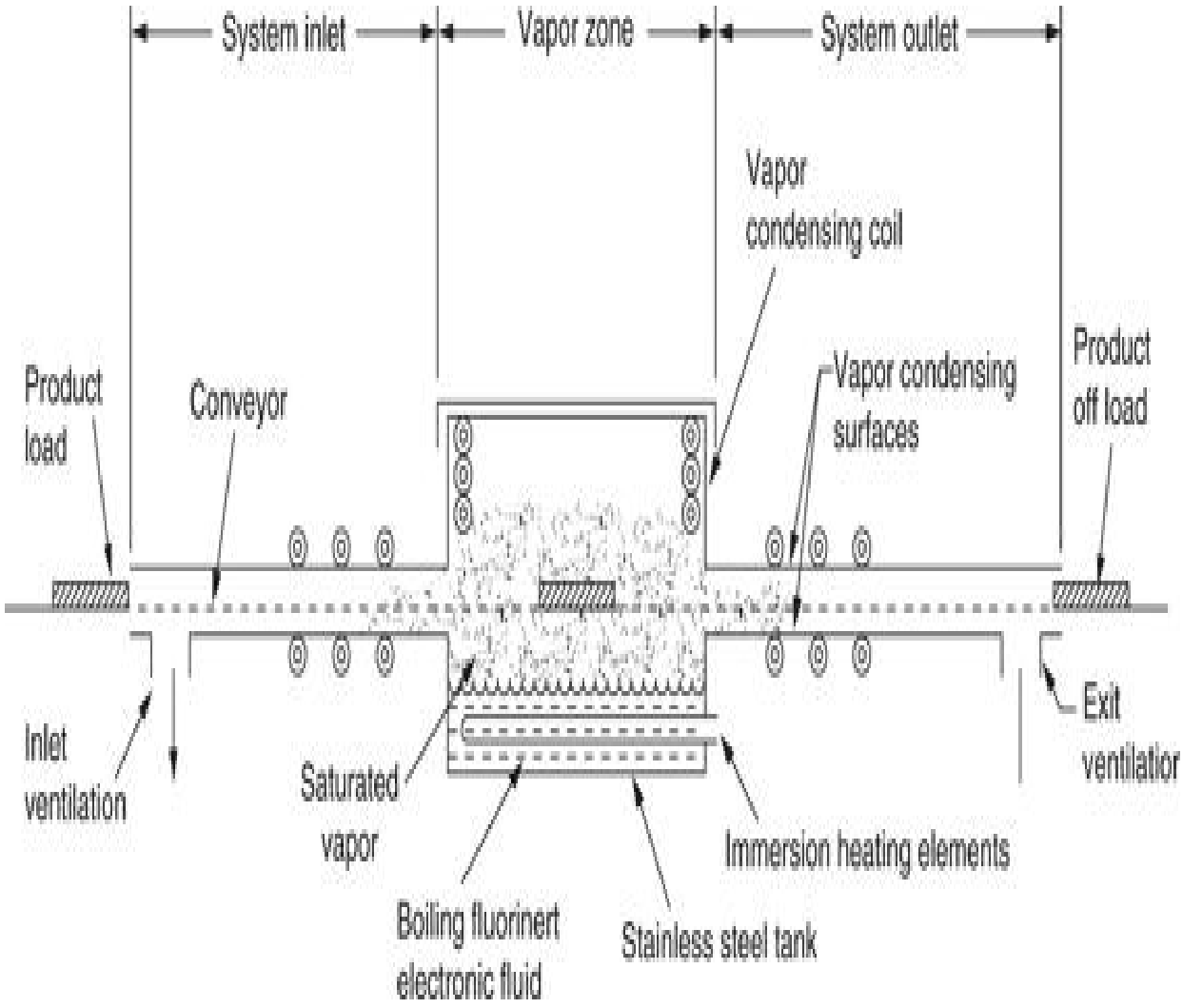

FIGURE 49.37 In-line single-vapor heating system schematic. (*Reprinted with permission from Electronic Packaging and Production, November 1982, p. 63, Fig. 1.*)

49.6.3 Advantages and Disadvantages of Vapor-Phase Reflow Soldering

The process is very precise in temperature and as long the as the boards to be assembled are not overly massive, they can be heated uniformly and rapidly by this method. Since the soldering occurs in an inert atmosphere, fluxes of lower

activation level can be used. In the absence of air, solder joint quality is generally excellent with low void content.

Although vapor-phase reflow has the appearance of being a fast process, solder paste reflow recommendations must still be followed. If the paste is heated too rapidly, paste volatiles may boil, resulting in explosive solder ball formation. As in other soldering methods, the maximum heating and cooling ramp rates must be commensurate with component manufacturer recommendations to prevent component damage. Components must be dried out prior to soldering to remove any moisture from within the devices. This is no different than for any other soldering method. A phenomenon known as “popcorning” may damage non-hermetically sealed packages. This occurs when moisture entrapped in the package is heated and expands. The pressure within may be high enough to rupture the plastic molded package body. When this occurs, the silicon die and associated wire bonds may be stressed and damaged as they are moved by deformation of the over-molded plastic package material.

Besides legislated environmental issues, there are health risks associated with vapor-phase reflow soldering. With the continued recycled use of HFCs, toxic materials such as hydrofluoric acid and perfluoroisobutylene are formed and concentrated. These must be neutralized and properly disposed.

When massive, densely populated boards are introduced to the vapor-phase reflow chamber, vapor collapse can occur—a condensation rate that outpaces that of vaporization. The result is that the internal atmosphere of the vapor-phase chamber thins dramatically to the point that it cannot sustain adequate reflow. Vapor-phase machines that rely on immersion heaters are prone to this phenomenon. More recent machines include massive heating element housings that surround the reservoir providing sufficient thermal inertia to preclude this problem.

Increased incidence of tombstoning, solder ball formation, and component displacement has been noted in this method of reflow. The condensing vapor transfers heat directly and rapidly to the best thermal conductors, component leads, and pads. Excessive solder wicking may occur, transporting solder from between the lead and pad up the lead, where it is not needed. This may result solder bridges proximal to the component body. Excess solder on the component lead decreases the lead's flexural compliance, making it less reliable. Furthermore, if the solder is wicked up the lead, the lead-pad interface may be solder-starved, resulting in an inferior solder joint. Additional information can be gleaned from older reference books and other authoritative publications, including previous editions of this book.[13,14]

49.7 LASER REFLOW SOLDERING

The laser has proven to be a versatile tool in many industries. For circuit board assembly, it can be used for marking, single-point soldering, or rework. Lasers can accommodate bonding of the finest or coarsest peripherally leaded surface-mount packages, and its performance and applicability are independent of device population density on the board, the thickness of the PCB, or the presence or absence of package heat sinks as long as there is a direct view of component leads. It can be used with most any PCB pad or component lead surface finish and any solder, including Pb-free alloys. When laser soldering is implemented properly, high soldering yields and exceptional bond characteristics are possible.[15] Its use is generally relegated to low-volume soldering applications. For successful laser soldering, it is necessary to use tooling to force or hold component leads in contact with circuit board pads.

Laser-based reflow is used for both primary soldering and as a rework tool. Some laser systems are packaged expressly for the purpose of rework and sold commercially. In such systems, PCBs are preheated to about 100°C within the system by means of a bottom-side resistance heater or by a hot-air stream. A diffuse laser beam is then scanned around the package by a rapidly moving galvanometer. The impinging energy heats surface-mount leads or an entire BGA to the point of solder reflow for package removal. This system has the advantage of such localized heating that only the package targeted for rework reaches reflow temperature. Everything around it stays close to the system preheat temperature with almost no thermal spill-over from the laser. This is a distinct advantage over conventional hot-air repair methods, where the hot gas stream used for package heating and reflow can inadvertently melt solder joints on adjacent components or components on the opposite side of the board.

Laser soldering requires no hot zones to profile or maintain, does not induce substrate warpage, and requires no heated bonding head that can degrade or vary with usage. Components can be spaced exceptionally close to one another—closer than currently permitted for other techniques, especially when one considers rework.

Delivery optics, placed in the path of the laser beam, direct it to the circuit board or, more specifically, the leads, pads, or lead-pad combinations. The beam can be easily steered by means of wavelength-appropriate mirrors and can be focused to the required spot size via a final objective lens to concentrate the beam density sufficient for the thermal rise to accomplish soldering. The delivery optics can be held fixed and the circuit board moved beneath or, conversely, the optics can be moved to direct the beam as needed. Either can be done with great precision sufficient for any PCB soldering task. Moving the beam and moving the board both have their own advantages. Moving the optics in any

direction is very simple and will not interfere with any PCB or surface-mount device fixturing requirements. Also, moving the circuit board may cause misalignment of component leads and circuit board pads. Fixed optics are more stable and require fewer adjustments, although, if engineered properly, moving optic beam delivery systems can be exceptionally stable and accurate. Fiber-optics are in vogue for laser beam delivery for Nd:YAG or laser diode systems, but it should be noted that, when dealing with high-energy-density laser beams as required for soldering, fibers are subject to damage if not precisely maintained. Fiber delivery has the advantage of allowing for easier steering of a beam in a complex machine that may preclude the use of orthogonal mirror beam steering.

The choice of laser for soldering is predicated on emission wavelength, required power, required beam diameter, machine reliability, and price. The optical properties of the target material are of primary importance in the laser selection process. In the case of surface-mount soldering, the absorption, reflection, and transmission characteristics of the PCB laminate as well as the reflectivity and absorptivity of the metallics (leads, pads, and solder) involved in the soldering process must be considered. The majority of circuit boards produced are composed of glass fiber-reinforced epoxy resin, although there are others. Each laminate has its own unique optical properties and characteristic laser damage threshold (LDT). LDT can be defined as the energy required to alter or damage the target material. In the case of an organic-based laminate PCB, it would be the necessary laser energy to char the board or cause the bonding pads to lift from the surface. Most any lead-pad surface finish on most any circuit board material can be soldered. For the purpose of this section’s discussion, the focus will be on industry-standard glass-epoxy laminate and most any tin-based solder.

49.7.1 Laser Choices

There are few practical choices for laser selection, since only a few possess the characteristic energy, production-tested reliability, and economics necessary for PCB assembly. The most common are the neodymium-drifted yttrium-aluminum-garnet (Nd:YAG) laser, an example of a solid-state laser, and the carbon dioxide (CO_2) laser, which has a gaseous lasing medium. While there are others, these two types of lasers are among the most common of the industrial tools. Each has been on manufacturing floors in various industries since the early 1980s. They are versatile in terms of applications and capable of the output required to weld, braze, solder, cut, and mark. Although other lasers could be used for soldering, the Nd:YAG and CO_2 types are the most commonly available. They have proven track records and are also the most commonly reported in terms of application to soldering.

There are excellent classic supplemental texts available for additional detail and instruction in laser technology. Those by S. Charschan,[16] Hecht,[17] and Ready[18] are particularly useful. Additional information on CO_2 lasers in the realm of soldering can be found in several references.[19–24]

49.7.2 Effects of Laser Wavelength

The long wavelength (10,600 nm) of the CO_2 laser is readily absorbed by organic materials (e.g., glass-epoxy laminate, polyimide, solder flux and plastics used for over-molded ICs). The shorter wavelength (1064 nm) of the Nd:YAG laser is more readily absorbed by metals such as tin plating and solder. There is yet another consequence of wavelength on the process: the shorter wavelength the smaller the achievable spot size.

The theoretical diffraction-limited spot size of a focused beam is directly proportional to the beam wavelength and lens diameter, as described in Eq. (49.1).

$$S = F\lambda/D \tag{49.1}$$

where S = diffraction limited spot size
F = focal length of the lens
λ = wavelength of the laser
D = lens diameter

Table 49.3 shows theoretical spot size for a 25 mm CO_2 or YAG laser beam focused by a wavelength-appropriate 25 mm diameter lens of 100 mm focal length:

TABLE 49.3 Theoretical Spot Size versus Laser Type*

Laser Type	Laser Emission Frequency, nm	Approximate Theoretical Spot Size	
		nm	μm
CO_2	10600	42,000	42
Nd:YAG	1064	4,200	4.2
Nd:YAG (frequency-doubled)	532	2,100	2.1

*For this example, the laser beam diameter is sized to fill the focusing lens diameter (D).

Imperfections in the lens or beam shape and other factors prevent practical achievement of these minimal spot sizes. Generally, the attainable focused beam diameter on the factory floor is about two to three times larger than the

ideally calculated spot size. Note that for an Nd:YAG laser, the spot size is at least 10 times smaller than that of the CO_2 laser, providing a fine, high-energy-density spot for soldering.

49.7.3 Laser-Soldering Fundamentals

There are relatively few variables associated with the laser in its application to soldering. This is one of the advantages for laser processing. Beam wavelength, irradiation time, and beam power are important to the process, as are the properties of the materials being joined. Reflectivity, thermal conductivity, and laser damage threshold must be understood before soldering is attempted. The wavelength will be fixed by the laser of choice, and the shorter the wavelength, the smaller the theoretical spot size, as discussed. Generally, the reflectivity of a metal is lower at shorter wavelengths, thus a metal is more easily heated by an Nd:YAG laser than with a CO_2 laser. The converse is true for many polymeric materials, which are more absorptive at longer wavelengths and therefore more prone to damage with increasing wavelength. Many polymeric materials are also absorptive at the UV end of the spectrum. A CO_2 laser beam is more likely to impart damage to a circuit board than the beam of an Nd:YAG laser, but either laser can inflict damage if the energy density is sufficient. In fact, either laser can easily cut through a component lead or drill through a circuit board if parameters are not adjusted properly.

The reflectivity of metals varies widely with composition and surface condition. Every metal can be heated with a laser as long as the energy density of the beam and dwell time are sufficient. This is also the case with laser-irradiated

component leads, board bonding pads, and solder during the laser bonding process. Measurement of the reflectivity of Sn-based solder shows that a eutectic alloy can be as high as 75 percent at 10,600 nm or as low as 25 percent at 1064 nm. Therefore, in the case of the CO_2 laser at 10,600 nm on a Sn or Sn/Pb-plated lead and solder-coated pad, much energy will have to be directed at the metals to start the absorption process, since so little laser energy is absorbed by the solder and converted to heat; the rest of the energy is lost to reflection. The reflected or multiply reflected beam may impinge on adjacent components and damage package bodies or even the circuit board itself, causing charring. Therefore, Nd:YAG is preferable for circuit board soldering.

49.7.3.1 Through-Lead and Through-Pad Bonding. Generally, the laser beam is directed at the component lead to accomplish soldering, but when the lead material is highly reflective, as would be the case with a gold-plated finish, as found in some flex-circuits, heating is slow and irradiation times impractically long. An alternative, "through-pad bonding," has been demonstrated whereby the beam is directed at an extended fluxed, tin-plated or solder-coated circuit board bonding pad (Fig. 49.38*b*). In through-pad bonding, the beam is directed at the more absorptive solder or on the circuit board land, increasing process efficiency and locally melting the solder in the vicinity of beam impingement. Since the molten solder is in intimate contact with the lead and pad, the heat from the bonding process is efficiently transferred. The process can result in rapid soldering along the entire length of the component lead and circuit board pad with rich solder fillets evident if the process is conducted properly. Compare this to the usual beam impingement on the component lead, or "through-lead bonding" (Fig. 49.38*a*).

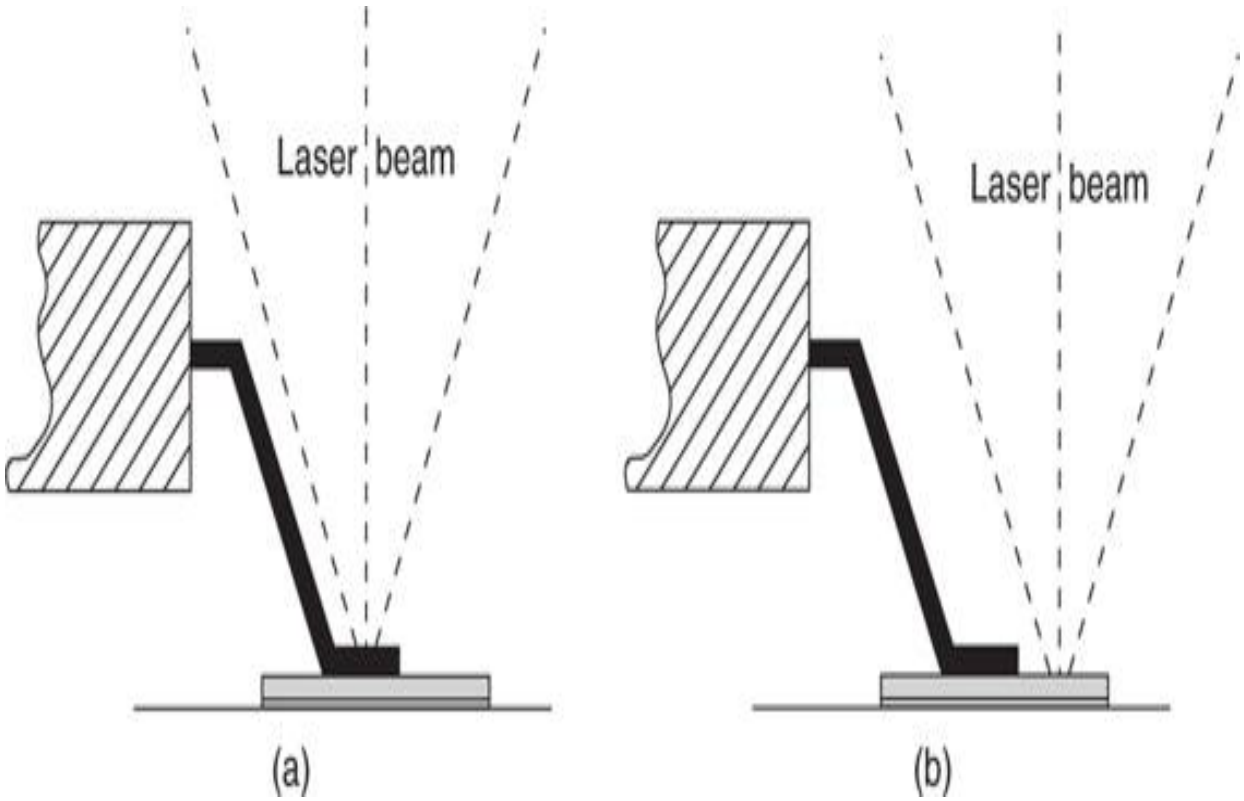

FIGURE 49.38 Through-lead versus through-pad laser soldering: (*a*) For through-lead laser soldering, the laser's beam is directed at the foot of the component. (*b*) For through-pad laser soldering, the beam is directed at a pad extension; this heats the solder directly.

49.7.3.2 Single-Point Laser Soldering. This method requires a laser beam that is smaller in diameter than the length or width of the component lead or bonding pad. The beam is stepped to each lead-pad combination and delivered with sufficient energy to result in solder reflow. The beam can be continuous-wave, pulsed, or multiply-pulsed to accomplish soldering as long as there is enough radiation delivered to cause the solder to undergo the phase change required for soldering and wetting. Due to the small beam diameter, as required by this technique for fine-pitch components, the energy density can be exceptionally high. In fact, it can be so high that if the lead is not in good contact with the bonding pad, then the laser's beam can melt or vaporize it. Overly intense irradiation can also cause a bonding pad to delaminate from the PCB.

In any laser soldering technique where very small spot size is required, the beam diameter must be precisely controlled. A small variation in beam diameter, either through change in laser parameters or in working distance (focus), can dramatically affect the delivered energy density. In the cases of a 10 W Nd:YAG laser beam focused to a spot of 0.1 mm (0.004 in) and a spot of 0.2 mm (0.008 in), this seemingly small change in spot-size will result in a large difference in power density [refer to Eq. (49.2)].

Equation (49.2), change in spot size and resultant difference in power density:

$$P = p/d \tag{49.2}$$

where P = power density
p = average power
d = focused beam diameter

For this example, the power density would vary from 1273 W/mm^2 for the 0.1 mm diameter beam to 318 W/mm^2 for the 0.2 mm beam diameter. This represents a fourfold reduction, emphasizing the criticality of strict maintenance and process control when working with a small spot size.

In most cases, a Gaussian distribution of the beam's energy distribution across the focused diameter is assumed. It is customary to measure the beam at the $1/e^2$ point (13.5 percent of the peak height), so, in fact, the beam is impinging on a slightly larger area. However, the most intense portion of the laser's beam is confined to the region bounded by the $1/e^2$ points in two dimensions, as shown in Fig. 49.39.

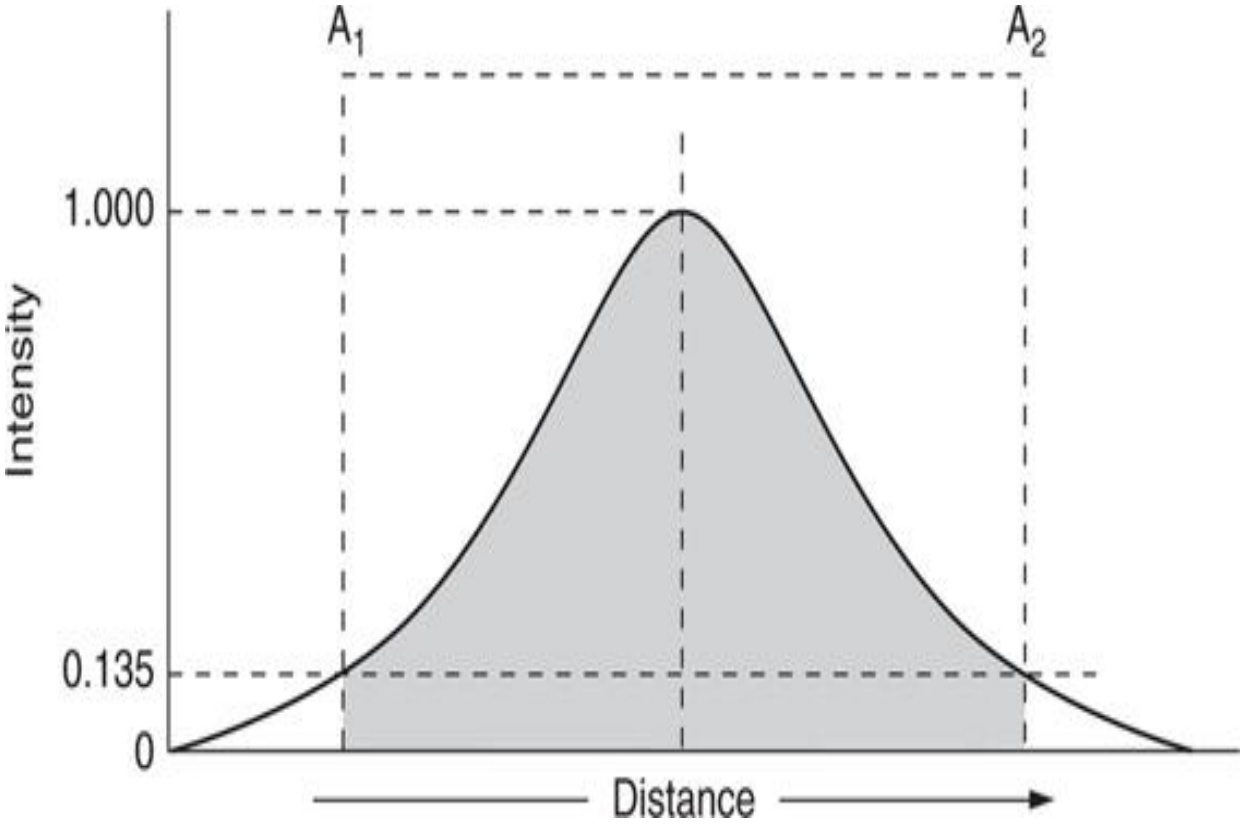

FIGURE 49.39 Gaussian energy distribution. Laser energy density is measured from points on the distribution curve where the beam's intensity is $1/e^2$ (13.5 percent) of peak intensity or between points A1 and A2 in this plot.

Single-point laser bonding has been used for soldering tape-automated- bonded (TAB) lead-frames to silicon die, TAB leads to PCB, or multi-chip modules[25] as well as for soldering gull-wing leaded components to circuit boards. This technique is not suited for bonding area-array devices such as BGAs or CBGAs to PCBs since there is no access to inner balls or columns.

49.7.3.3 CW Scanning. In sharp contrast to single-point laser soldering, this technique relies on a larger, defocused moving beam to accomplish the heating. The beam may be many times the size of the narrowest lead or pad dimensions. In this technique, the laser beam generally spills over onto the substrate material, irradiating the lead, pad, or lead-pad combinations as well as inter-pad PCB surfaces.

Because of the larger beam diameter, a long focal-length lens can be employed. This results in a wide process window in terms of final beam diameter and working distance of lens to the circuit board surface. The laser spot is moved at a rate such that the beam exposure to the board is below the laser damage threshold limit. It heats the lead-pad combination, the solder flux, and the board sufficiently to cause the solder to change state.

A variation of this technique utilizes orthogonally mounted galvanometers to move an Nd:YAG laser beam around the periphery of a surface-mount device sitting atop solder lands on a circuit board. The beam is repetitively scanned at high velocity around the surface-mount device until all leads are heated to the point of solder liquidus. As the beam is turned off, the solder solidifies and solder joints result. This same galvanometer-driven technique has gained commercial acceptance as a BGA rework tool. A slightly defocused laser beam is aimed at the body of the BGA. The beam is rapidly moved around the package body at an irradiance below the laser damage threshold of the packaging material. With each pass, the component heats up a little more, eventually melting the BGA solder joints. The package is removed with an automated vacuum pickup tool while the solder is still molten. A new BGA can be attached using this same technique. This method can be applied to any type of rework, although component leads and pads would be targeted rather than the body, as was the case for the BGA.

49.7.3.4 Multiple-Beam Laser Soldering. One of the attractions of working with a laser is the fact that its beam can be split for multiple use within one station or even shared between two or more stations. The split can be accomplished by the use of bifurcated fibers or beam splitting mirrors. The beam of a single laser cavity can be duplexed to solder two sides of a surface-mount component simultaneously. It is entirely possible to share a common

beam between two or more laser soldering stations either simultaneously or in a time-shared manner.

49.7.3.5 Tooling and the Need for Coplanarity and Intimate Contact. In all modes of laser bonding, the component leads must be in contact with solder lands on the PCB to accomplish joint formation. It is therefore necessary, in most cases, to use a specialized hold-down tool to ensure that leads contact pads. This detracts from the ideal of “noncontact” laser bonding. Several techniques have been developed and reported. One such method uses a transparent hold-down medium such as glass, quartz, or transparent high-temperature plastics. There are several problems with this approach, which can result in an inconsistent soldering process. First, these materials are rigid, making it impossible to hold a lead down to a low-lying pad abutted by normal height pads or, conversely, a high pad abutting lower pads (Fig. 49.40).

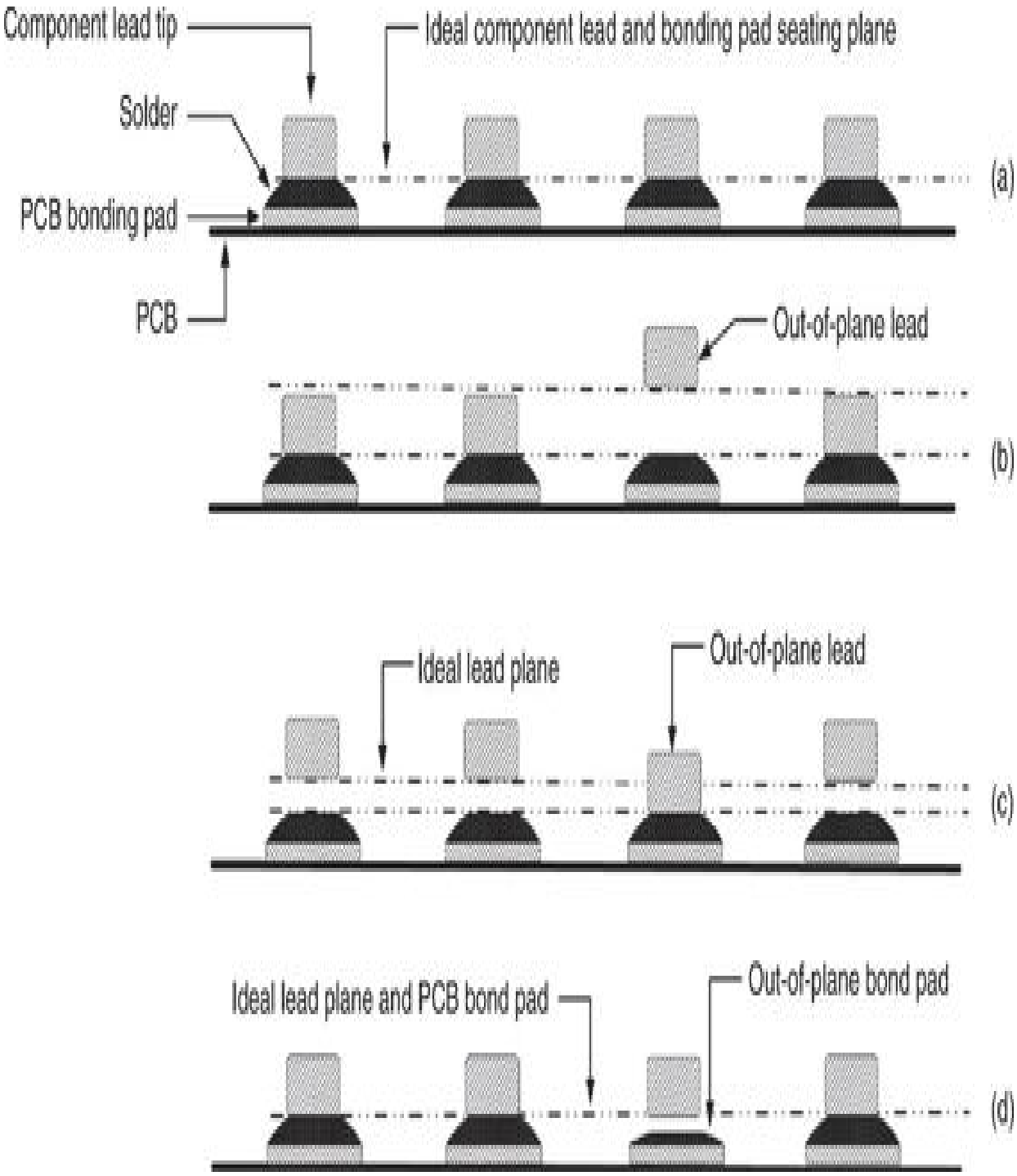

FIGURE 49.40 For laser soldering to be effective, it is necessary to have component leads in contact with PCB bonding pads as in “a.” If either component leads or PCB bonding pads are out of plane, then soldering will not occur (b, c, d). For this reason either a perfect part must be used or a fixture must be employed to hold leads in contact with bonding pads.

During the soldering cycle, the glass or other window material can accumulate spattered flux and flux by-products that may change the delivered laser beam intensity, adding variability to the process.

Comb or pin arrays have been applied that match the lead configuration of a package. This type of fixture is expensive and easily damaged; especially if the soldering flux “glues” the comb teeth to the bonded component lead.

The most common method for laser soldering of rigid-leaded surface-mount packages is the “body-push” method, in which a force is applied to the component body, springing the leads just slightly against PCB bonding pads. As the solder melts below the lead, the lead drops down to board level, where it is frozen in the cooling solder. It is necessary to control the amount of push such that too much stress is not frozen into the resultant solder joint. This is particularly important when laser bonding rigid leads of coarse-pitched component, where much force may be required to overcome lead coplanarity problems on stiff leads. When board pads and component leads are reasonably coplanar, then the “body push” method is adequate for high-yield, high-reliability soldering as long as any component lead non-coplanarity is not in a positive direction, as indicated in Fig. 49.40*b* as there is no mechanism to force the out-of-plane lead against its matching bonding pad.

A compliant hold-down method has been developed[26] (Fig. 49.41), which is inexpensive to fabricate and easy to implement. It is an aluminum fixture body with compliant silicone rubber feet that align with component leads. When pressure is applied to the fixture, component leads are forced against PCB pads. A slot in the aluminum fixture allows the beam unobstructed access to the lead-pad combination. It accommodates non-coplanar PCB pads and non-coplanar component leads. It has proven effective for TAB as well as for rigid-leaded surface-mount device laser soldering. This method obviates the problems associated

with transparent hold-down methods in terms of flux build-up on the window and does not have the fragility of comb hold-down methods.

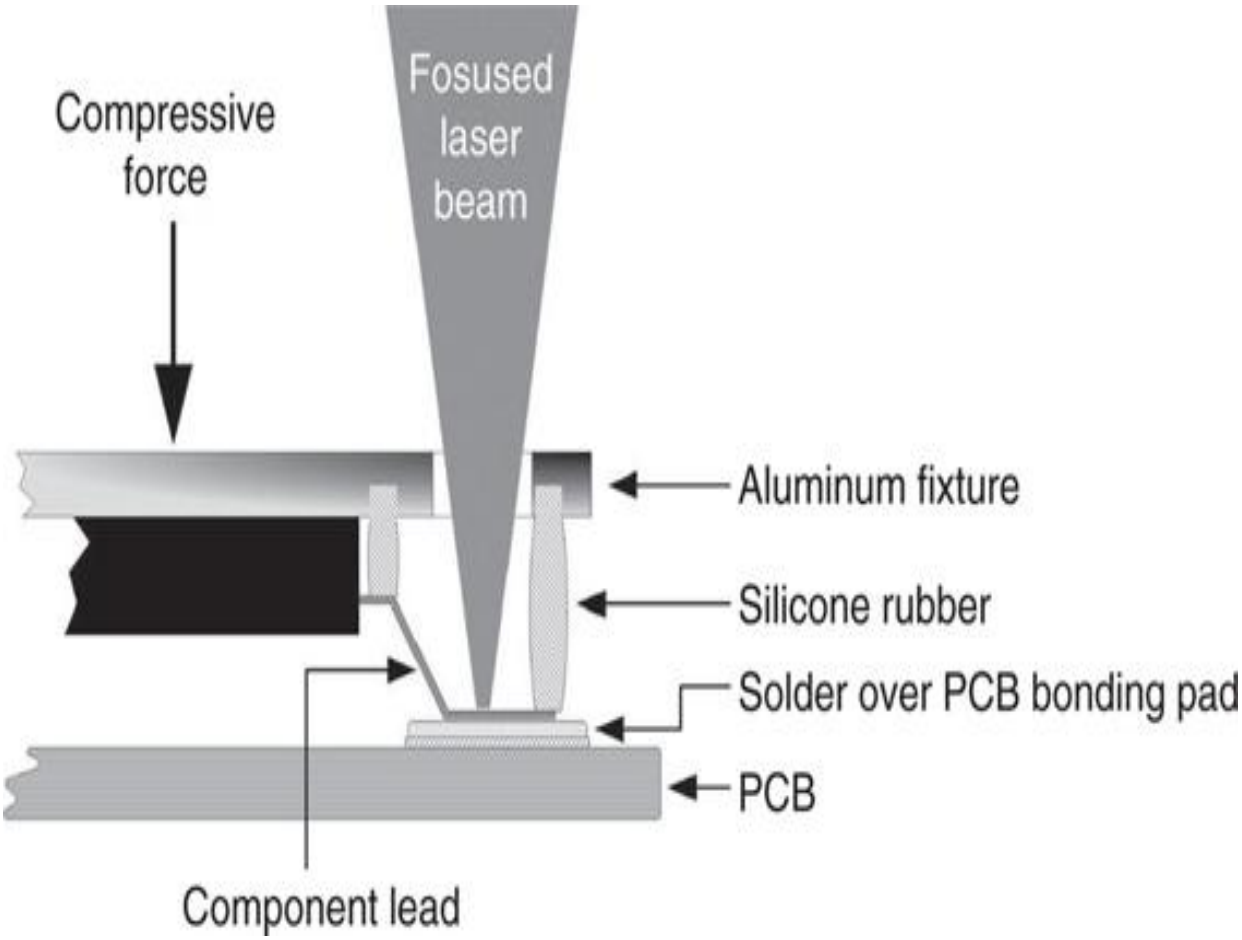

FIGURE 49.41 Window-less laser fixture with polymeric hold-down. The beam is focused through a slot in the aluminum fixture

49.7.3.6 Solder for Laser Soldering. Choice of solder alloy will have little to no influence on laser soldering. It should be noted that high-temperature solders are compatible with this bonding technique. There are systems where a single joint is soldered using an automated solder-wire dispense system. In that case the flux-cored solder wire is automatically pushed into contact with the component lead/PCB pad combination and then the laser is activated to

effect the soldering. The flux-cored solder wire provides the flux and the solder for the bonded connection.

It is also possible to preplate solder or otherwise predeposit solder onto circuit board pads. With this type of assembly, bonding pads are coated with a fluxing agent compatible with laser soldering. This will be discussed in a subsequent section. When the lead/pad combination is laser-heated to liquidus and cooled, the solder joint will be formed. The use of solder-foil pre-forms can also be used. Applying flux to the PCB prior to pre-form placement will keep the foil in place until the device to be soldered is placed on it.

Since laser soldering relies on a very high temperature for a very short duration, solder paste is not recommended for this process. A large fraction of solder paste is composed of liquids or gels that enhance its printability. When exposed to the rapid thermal rise and high process temperature of laser soldering, the solder paste is prone to spattering and solder ball formation. For that reason the use of predeposited solder and liquid solder flux is preferred.

49.7.3.7 Flux for Laser Soldering. Requirements are much the same as for other reflow methods. Flux must be active enough to remove oxides from the component lead, bonding pad, and the solder. But in the case of laser solder, the flux’s optical characteristics in terms of reflection, absorption, and transmission must not interfere with the laser beam or solder process. If too absorptive, the flux could char, overheat and damage the underlying circuit board. Also, if denatured by the intense laser beam, it may lose its chemical effectiveness as a fluxing agent. In laser soldering, particularly in the scanned methods, the flux adds a path of heat transfer to the board and preheats the next joint to be soldered. In the absence of a liquid flux, the PCB is more likely to be damaged if the laser impingement is not stringently controlled. During soldering, the laser beam’s output is quick and intense. The high energy of the process

results in exceptionally high process temperatures for very short durations. The high thermal excursion may aid in flux activation, making even the mildest of no-clean flux an aggressive oxide stripping agent.

49.7.3.8 Fluxless Laser Soldering. There have been many reports of fluxless laser soldering as used for inner-lead bonding to silicon die. Such bonding is done with a high-peak-energy, short-duration laser pulse. Under these conditions, when the mass of the lead and the bonding pad is small enough, the process is more akin to welding with the component lead melting and alloying with an underlying metal pad. To accomplish conventional reflow soldering by means of a laser, or any other technique, it is necessary to employ a solder flux to bond effectively. Plasma cleaning and inert storage may be one such method, but even the briefest exposure to air will start the re-oxidation process. Ultrasonic assisted laser soldering is another technology that can be effective, but is slow, requiring precise placement of an ultrasonically agitated head with the laser beam concentric to the ultrasonic tool or precisely adjacent to it. The ultrasonic agitation breaks up the oxides on component leads, bonding pads and the molten solder making conditions right for solder wetting.

The use of gaseous-phase carboxylic acid fluxing with laser bonding has been demonstrated.[27] This method precludes the need for conventional liquid fluxes and leaves no visible residues on the circuit board. No cleaning is required and the assembly reliability is not degraded from the use of a gaseous fluxing agent. Because liquid flux is not present, it is recommended that the laser’s beam impinge only on the lead-pad combination. Were the beam to hit the PCB, it would surely exceed the damage threshold limit and the board would char. Any charred material may be mildly conductive and an electrical short may result or become problematic in the long term.

49.7.3.9 Laser Solder Joint Characteristics. There are very few differences between solder joints prepared by laser as compared to those formed by other methods. Laser soldering results in intermetallic formation, but the layer is extremely thin if the laser soldering cycle heating is kept short; much thinner than found in solder joints manufactured by more conventional methods. Since the heating is highly localized, cooling is rapid resulting in exceptionally fine solder grain growth. The fine grain growth leads to greater joint strength initially. The strength advantage, although significant in initial magnitude, tapers off as the solder joint ages due to grain-coarsening of the solder and intermetallic layer thickening. Coarsening rate and intermetallic growth both depend on ambient temperature, device operating temperature and time.

49.7.3.10 Solder Sources and Defects Associated with Laser Reflow. Solder requirements are the same as for any other process. There are no alloy composition requirements specific to laser soldering, as this soldering method is compatible with leaded or lead-free solder alloys. Even high-temperature alloys can be soldered effectively. When single-point laser reflow is applied, the board quality and integrity are not compromised if parameters are appropriately chosen and adequately controlled.

Laser soldering is not prone to solder bridges and if component leads are held down to solder-coated PCB lands, then soldering defects are rare. Perhaps the most common characteristic defect unique to laser soldering is charring or burning of the circuit board, which occurs if too high an energy density is used and the laser damage threshold of the PCB is exceeded. Charring or burning of the PCB can also occur if the circuit board is grossly contaminated with grease or other organic contaminants. This is not to say that boards for laser soldering have extraordinary requirements for

cleanliness. Requirements should be considered the same for this technique as for any other reflow process.

A hidden defect associated with laser soldering is PCB bond pad delamination. If the PCB bond pad reaches too high a temperature during the laser soldering process, it may lose its adhesion to the laminate. This may result in reliability problems. It is best to check the process by doing lead pull testing to ensure that the laser process has not compromised bond pad adhesion strength.

49.7.3.11 Laser Safety Issues. Lasers are categorized by their safety hazard potential. For a full review consult ANSI Z136.1[28] in the United States and IEC 60825[29] internationally. Sufficed it to say, Class 1 is an intrinsically safe laser, posing no intraocular danger, while Class 4 lasers pose the greatest hazard. All lasers considered for soldering use are of the Class 4 variety. Because of this, they are generally embedded in appropriate interlocked cabinets with laser-safe viewing ports or a video camera incorporated for viewing the process to preclude direct ocular exposure to the laser's intense beam. When the Class 4 system is embedded in an appropriately interlocked cabinet, it is considered a Class 1 system and poses no hazard. Laser-safe eyewear need not be worn during normal operation except when interlocks are overridden for system maintenance. As mentioned previously, lasers, especially Nd:YAG, are known for their high uptime and lack of required expendables.

49.8 HOT-BAR SOLDERING

Specifically suited to surface-mount assembly of packages with lead-frames, hot-bar soldering has been in use for several years. The technique relies on a resistance-heated element to push component leads into contact with solder

and bonding pads, simultaneously reflowing the solder. Compression of the lead/pad combinations is continued as the heat is ramped down. Upon cooling, the solder solidifies and the heating element is withdrawn from the newly formed solder joints. The heated element, commonly referred to as the hot-bar, is also known as a “thermode.”

Hot-bar soldering is best suited for low-thermal-mass, single-sided surface-mount assemblies. Each component type requires its own hot-bar bonding head assembly. These can be expensive, with the price dependent on the complexity, materials of construction, precision required, and overall size of the bonding head.

49.8.1 Solder Application

The use of solder paste is discouraged because hot-bar heat-up is fast and bar temperature is typically well above solder melting temperature; conditions favorable for rapid volatilization of solder paste constituents and explosive solder ball formation. Also, the paste is likely to squeeze out from between the component lead and circuit board pad, which can cause the solder to bridge to adjacent conductors during fine-pitch component soldering. In fact, even with solid solder coatings on the circuit board, bridging can be problematic in hot-bar bonding for the same reason. This is usually a function of the volume of solder on the pad, the quantity of flux, its degree of activity, and lead/pad pitch. As the solder is melted and displaced by the hot-bar, it bulges laterally to the point that the solder masses of two or more adjacent pads may touch one another, forming a solder bridge. Once the bridge has formed, the forces associated with lead-to-pad wetting and capillarity will not be strong enough to overcome the surface tension conditions established during the solder bridge formation. If that is the

case, the bridging defect(s) will persist (Fig. 49.42). Bridges are easy to form and difficult to break.

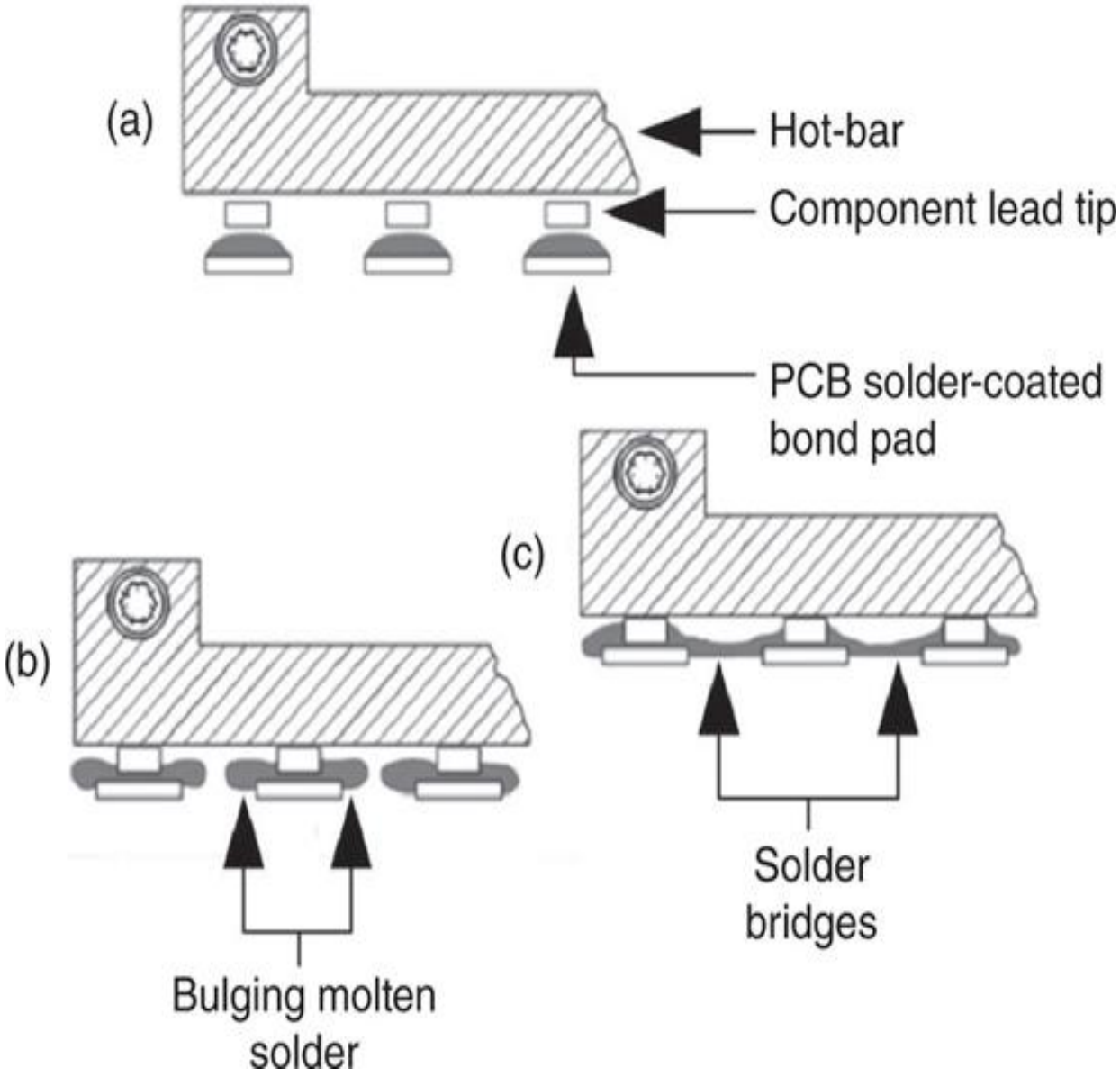

FIGURE 49.42 Hot-bar induced solder bridge formation. (*a*) Hot-bar aligned over lead tips and PCB bonding pads. (*b*) As the hot-bar is forced into contact with component leads and circuit board pads the molten solder may be forced out from under the compressed leads bulge laterally. (*c*) If adjoining molten solder bulges contact one another, solder bridges will form and persist upon solidification. Careful control of solder volume, controlled hot-bar pressure and temperature profile during hot-bar soldering is required to preclude this defect.

Solid solder coatings such as hot air-leveled pads, solder-plated boards, or stenciled and reflowed solder paste are preferred for this bonding method.

49.8.2 Fluxes and Fluxing for Hot-Bar Soldering

Soldering flux is applied prior to component placement and soldering. Tacky fluxes may be useful to hold components in place prior to hot-bar soldering. Flux choice should be tailored to the hot-bar process. The flux can be either liquid or paste. The flux chosen should be tested to resist charring and the development of polymerized decomposition products, or lacquers that may adhere to either the circuit board or the hot-bar or both. Residue build-up on the bar can adversely inhibit hot-bar performance by diminishing thermal transfer. The residue can also become thick and uneven enough to prevent the hot-bar from squarely contacting component leads. Baked-on aqueous-clean flux residues can make flux cleaning difficult. With no-clean flux, overheated residues may detract from the visual appearance of the printed circuit assembly.

49.8.3 The Hot-Bar Soldering Operation

Generally, the board is preheated on a hot stage beneath the hot-bar, off to the side or even in a box oven prior to soldering. Sometimes hot air is used for preheating. This step is generally done after flux application, so the thermal profile has to be adjusted to prevent complete flux dry-out. Once component leads are aligned with solder-coated PCB pads, the hot-bar is pressed against the lead-pad combinations and heated to reflow. Precise control of the

heating process is required to prevent flux spattering or solder bridging as discussed. A mechanical stop is employed to keep the bonding head from exerting too much force on the lead/pad combination. Excessive force can cause the component leads to slide off pre-reflowed (domed) solder-coated pads. It can also enhance solder bridge formation. Excessive force will displace solder from between leads and pads and resultant joints may be solder-starved.

One approach to preventing bridged or solder-starved joints is to retract the hot-bar by several hundredths of a millimeter once the solder liquidus begins to wet to component leads and PCB pads. Surface tension coupling of wetted solder between lead and pad reduces the propensity for solder bridge formation. Additionally it relieves compressive forces that would be incorporated into the final solder joint. Upon cooling, robust solder joints result. As in any other soldering process, it is important to maintain proper reflow time-temperature characteristics. In hot-bar soldering, it is of paramount importance that the blade seating plane is maintained normal to the surface plane of the PCB. On the other hand, it should be noted that the coplanarity of solder on the PCB pads does not have to be exact. The hot-bar will first reflow high solder spots. Once all the solder has melted, it will self-planarize and remain that way upon solidification.

49.8.4 Hot-Bar Construction and Effects

The hot-bar bonding head can be composed of one or several blades. They are designed to solder one side, two sides, or all four sides of a lead-frame simultaneously. Generally the hot-bar assembly is configured to accommodate the maximum span of a lead set, permitting simultaneous bonding of all leads on a package side. In the

case of some very long connectors or other large packages, the thermal uniformity of a single blade may not be adequate for the process. This is sometimes remedied by using a smaller hot-bar and stepping it along the length of the lead set until all leads are bonded. This may induce lead misalignment as the stepping progresses. Another approach uses multiple hot-bars side by side, each individually controlled, to achieve the span and required thermal uniformity. Bar configuration is designed for the lead-form to be bonded. It should sit flatly on the foot of the lead, neither contacting the radiused area of the lead-form nor significantly overhanging the lead toe, as shown in Fig. 49.43.

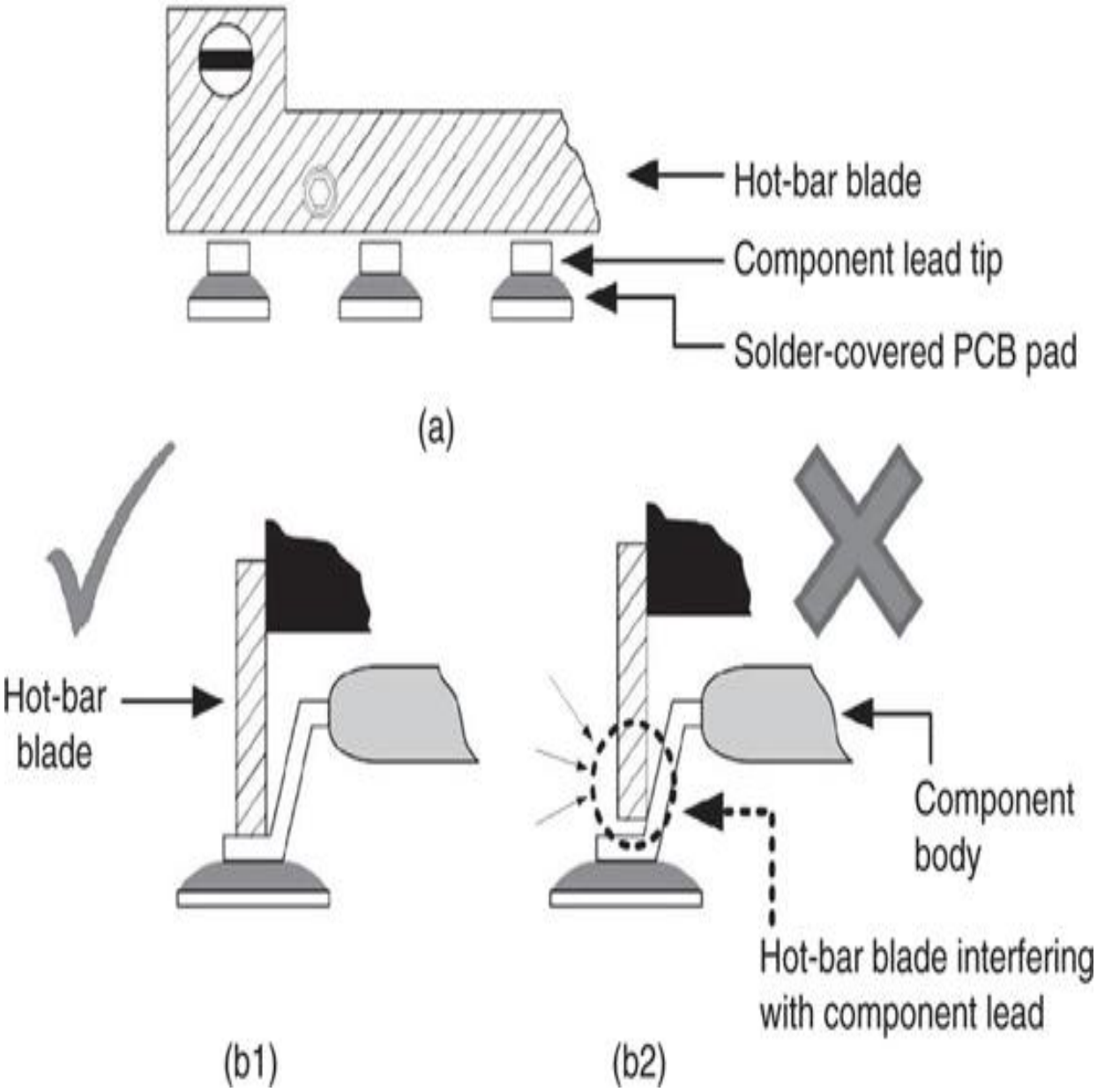

FIGURE 49.43 A hot-bar ready for bonding gull-wing component. (*a*) Transverse view; (*b1*) lateral view with the hot-bar appropriately contacting component lead toe, (*b2*) hot-bar incorrectly positioned interfering with the leg of the formed component lead (see arrow).

The bar itself can be manufactured to nearly any dimension, but there are limitations on its size; the longer the blade, the worse its longitudinal thermal uniformity. Variations in blade temperature may cause it to distort due to differential thermal expansion and contraction. Thermal

uniformity is critical for consistent lead-to-lead soldering and joint quality per component side. The allowable variation in bar temperature is limited by the component specification, the damage threshold of the board to be soldered, the solder, and product reliability requirements. As in any other soldering process, the variation in process temperature must be understood and controlled to ensure highest board assembly yields and best-quality solder joints. Most hot-bar systems are configured with a fine-gauge thermocouples welded to the bar, an integral part of a closed-loop, temperature-controlled hot-bar heater system. There may be more than one thermocouple per bar, especially on long bars.

Numerous bar designs and materials of construction are available; tungsten, titanium, and molybdenum are commonly chosen for their electrical resistance, durability, thermal conductivity, immunity to flux damage, and solder nonwetting characteristics. Some ceramics are also used for blade construction. The bar must be designed for uniform heating across its length and it must be able to shed heat rapidly to allow the solder to resolidify within a reasonable time. The blade has to expand and contract uniformly throughout the soldering cycle. Some blades have been seen to develop a “frowning” or “smiling” profile in their *z*-axis during heating due to differential thermal expansion or built-in stress in the metal, as shown in Fig. 49.44. For the same reasons, transverse warpage of the blade is also commonplace.

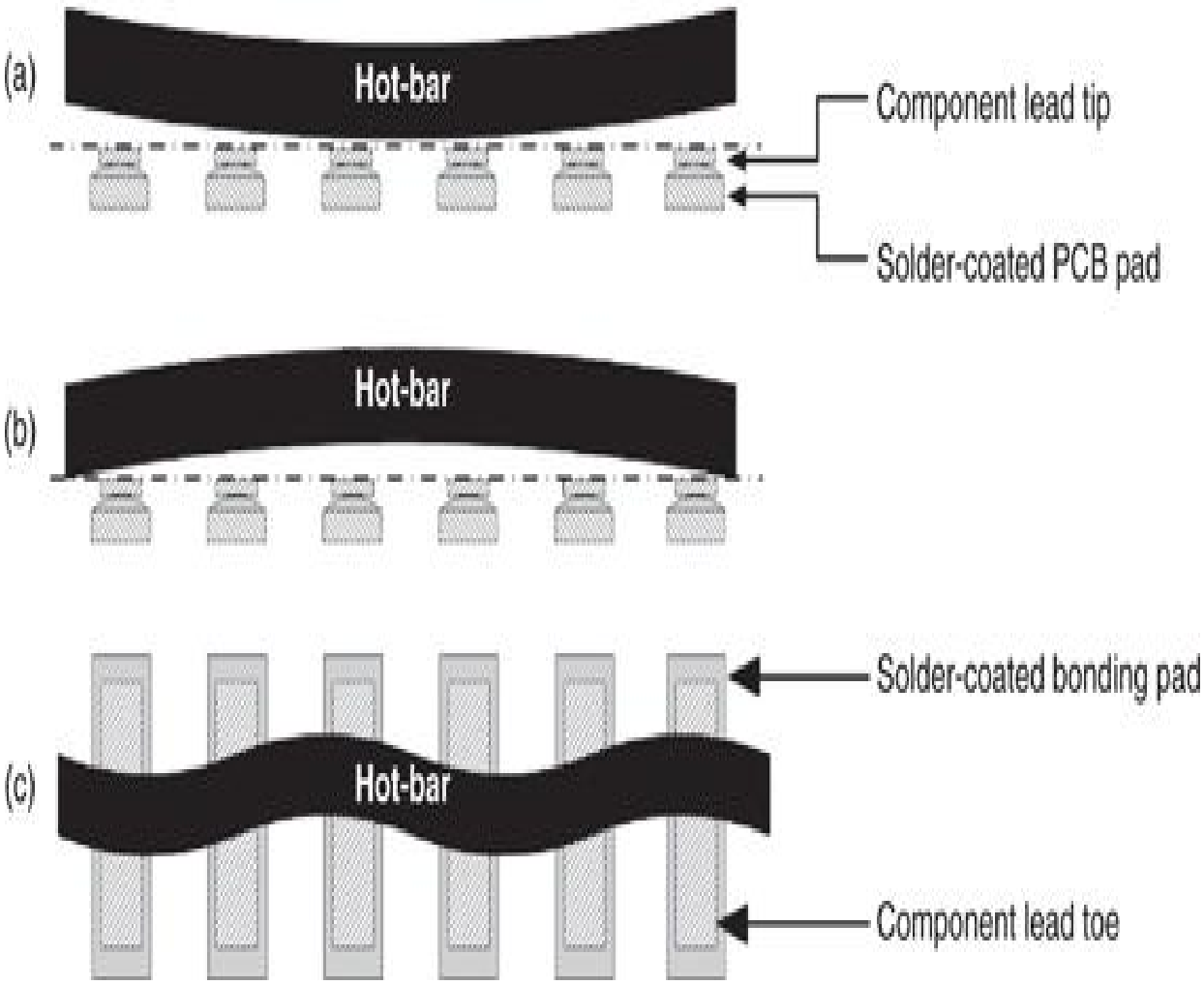

FIGURE 49.44 If not constructed properly, the hot-bar may distort: (*a*) "smiling" profile, transverse view; (*b*) "frowning" profile, transverse view; and (c) longitudinal warpage, plan view. The dashed line in (*a*) and (*b*) shows the desired hot-bar seating plane. All views have been exaggerated for illustrative purposes.

Such conditions detract from proper blade contact with lead and pad combinations and are indicative of poor hot-bar design or poor choice of materials. Blade warpage, if the curvature is sufficiently large, may result in solder opens. There have been many solutions proposed in the realm of structure, materials of construction, and electrical input to permit highest uniformity of blade heating and contact to the bonding pads. D. Waller et al. have patented a rigid molybdenum truss blade that has been found to be stable

dimensionally and thermally uniform over long spans (in excess of 76 mm).[30]

Usually the hot-bar blade is attached to a self-leveling, spring-loaded bonding head that allows each blade to self-planarize in relation to the underlying component leads and circuit board surface. Nonetheless, variations in board contour, such as a localized high or low spot, can render the concept of self-planarization useless and solder opens may still result. Rigid-member hot-bars are excellent for accommodating differences in lead coplanarity because the blade forces lead to pad. Driving a heavily sprung lead onto its corresponding bonding pad can, however, lock stress into the resultant solder joint because the solder is working to resist the spring force of the lead. This condition may result in premature joint failure.

49.8.5 Maintenance and Diagnostic Methods

As with any process equipment, it is important to maintain the hot-bar properly. Check it frequently for distortion. Ensure that it remains flat and perpendicular to the circuit board to be bonded. Scrub the hot-bar on a ceramic flat to remove any baked-on flux residue. This may need to be done every few bonding cycles, depending on the flux and the criticality of the assembly.

Several diagnostic tools can be applied to assess hot-bar conditions. The two most important characteristics that must be understood and monitored are thermal performance and blade planarity.

49.8.5.1 Thermal Monitoring. One of the most common methods of assessing hot-bar performance is to use a thermocouple-instrumented board, as is the case with any other soldering method. Preparing such a board for hot-bar

use has its own requirements. Fine-gauge thermocouples are attached to leads of the component or the bonding pad of the circuit board to be soldered. Positioning thermocouples at both ends of the lead set and also near its center helps quantify the longitudinal thermal uniformity of the hot-bar during soldering. It is also useful to deploy thermocouples on surrounding components to ensure that the hot-bar soldering process does not overheat closely adjacent, previously soldered joints.

When preparing the thermal profile board for hot-bar soldering, avoid placing the thermocouple bead(s) between component lead and bonding pad. The added height of the bead would prevent the bar from contacting adjacent component leads and results in point-contact heating that is not indicative of the bar's normal operation. Instead, place the thermocouple bead at the pad extension area in front of the lead tip or at the lead heel as indicated in Fig. 49.45.

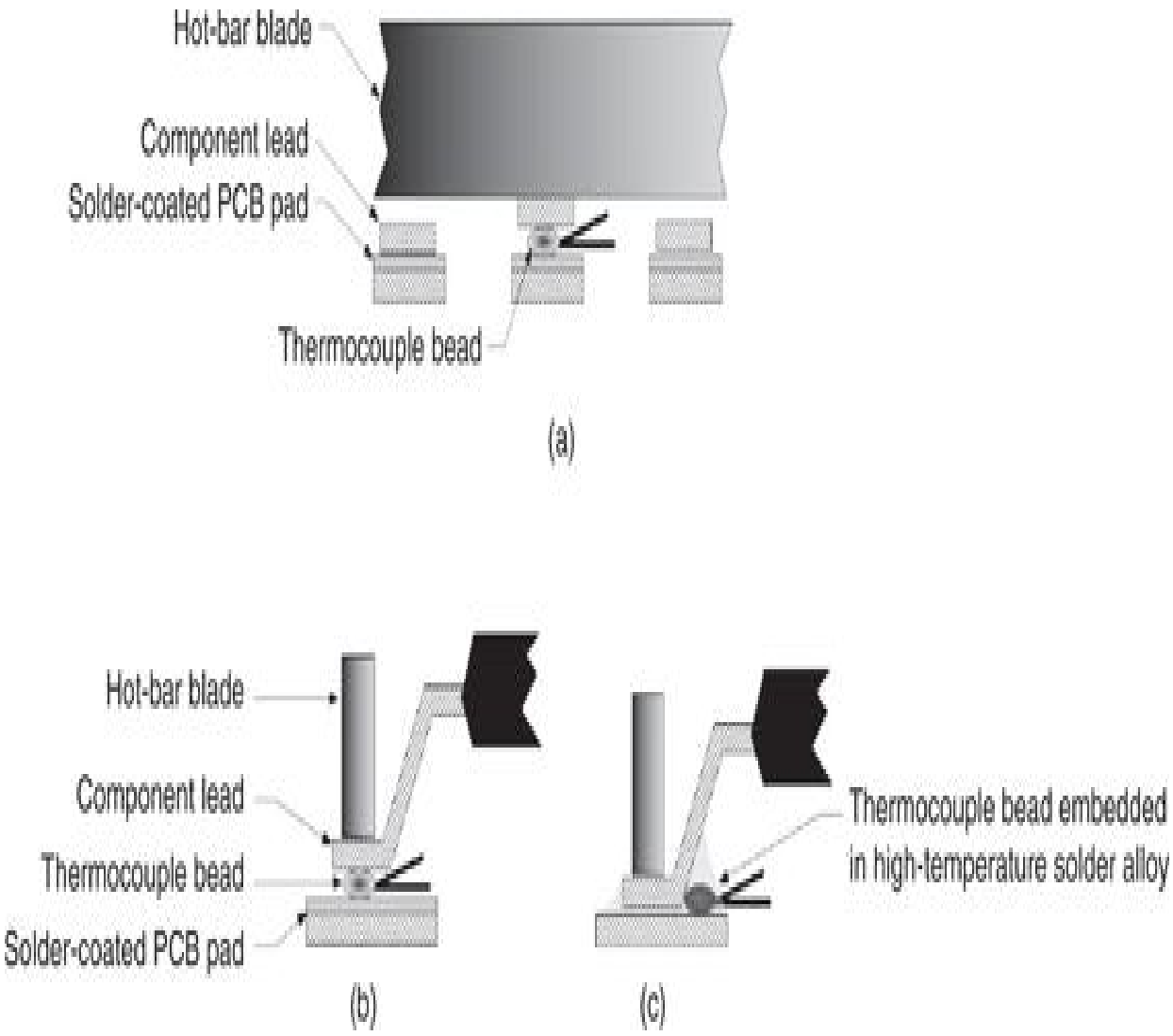

FIGURE 49.45 Hot-bar thermometry. A thermal profile board is needed for hot-bar soldering. (*a, b*) The thermocouple bead must not interfere with seating of lead to bonding pad or with the hot-bar blade to the lead/pad combination. (*c*) The thermocouple can be attached with a high-temperature solder alloy in front of or behind the component lead so that a common lead, pad, and bar seating plane is maintained.

If the high temperature solder alloy mixes with lower temperature solder alloy, its melting point or melting range will be depressed and the thermocouple may come loose and perturb the measurement.

49.8.5.2 Blade Planarity. As stressed throughout this section, the coplanarity of the hot-bar blade or multiblade

hot-bar assembly with respect to the bonding surface is of extreme importance to preclude solder opens during hot-bar soldering. There are numerous measurement methods that can help diagnose this; unfortunately, though, they are meant for evaluation of the blade(s) at room temperature, not at bonding temperature. As previously mentioned, a blade may distort temporarily or permanently during heating, but planarity measurements on hot blades are impractical. Therefore, the majority of techniques encountered are performed at room temperature.

Wilkins[31] suggests the use of a colorant, such as from a marking pen, applied to the cold bonding surface of a freshly cleaned hot-bar. Once the ink is dry, the blades are then scrubbed over a clean, flat ceramic plate. Low spots on the bar are indicated by the presence of colorant remaining on the bar after several circular swipes on the ceramic flat. Single-bar and two- or four-sided blade assembly planarity can also be evaluated using an array of ground, leveled, rigidly mounted pressure transducers. Bar pressure differential, an indicator of blade planarity, can be adjusted so as to be uniform from end to end and from blade to blade on two-up or four-up hot-bar assemblies. The use of pressure transducers has poor spatial resolution. Of course, some hot-bar assemblies are self-leveling, but even these should be checked for planarity and force per blade to ensure best uniformity during soldering.

49.8.6 Hot-Bar Process-Induced Defects

49.8.6.1 Solder Bridging. This is the most prevalent problem associated with hot-bar soldering. Recall that molten solder may squeeze out of adjacent solder joints and bridge, especially on fine-pitched components.

Bridges may also arise if the device being soldered moves off bonding pads, dragging molten solder with it.

As pressure is applied to component leads by the hot-bar prior to the onset of solder liquidus, leads are sometimes forced to slide down any domed solder deposits prior to reflow. This displacement causes misregistration of component leads to bonding pads. If the forces are great enough, it may also cause the whole package to move causing misalignment of the entire lead set and bridging on a massive scale.

49.8.6.2 Solder Opens. Result from lack of coplanarity between the hot-bar and the plane of the circuit board surface of component lead.

49.8.6.3 Brittle Solder Joints. Because of the thermal mass of the hot-bar as compared to the PCB being soldered, the hot-bar temperature is necessarily well above the solder liquidus temperature. If the time-temperature cycle is not carefully controlled, an overly thick intermetallic compound layer may form. This is especially true in this process, where the solder may be largely displaced from between lead and pad, and bond lines are excessively thin. Within the joint, the volume of intermetallic compound (hard and brittle) may be large compared to the remaining solder (soft and compliant). If this is the case, solder joints will be less reliable and more susceptible to brittle fracture. All of these obstacles have prevented the widespread acceptance of hot-bar bonding in manufacturing except in some niche applications where soldering by other methods may be difficult. Hot-bar bonding is most useful for low-volume, fine-pitch surface-mount soldering and rework.

49.8.6.4 PCB Pad Delamination. High localized temperature of hot-bar soldering may threaten the integrity of the bond between the PCB pad and the board laminate.

Destructive testing, such as pull/peel analysis and/or mechanical cross-sectioning should be employed to verify that the process is not impugning the PCB.

49.9 HOT-GAS SOLDERING

As the name implies, hot-gas soldering method relies upon a heated gas stream to effect reflow. This noncontact, directed-energy method is most suited to bonding surface-mount components. Although hot-gas soldering has been around for years and after numerous machine offerings, it is not a popular method for soldering despite its evolutionary improvements. Instead, it has made its mark in the area of component rework; removal of previously soldered devices from a circuit board and replacement of same with a good one.

There are three main disadvantages of this technique: (1) its thermal energy is not well localized, (2) it is a slow process, and (3) generally requires preheating of the PCB to be soldered. Most machines typically emit a hot-gas jet too large to be isolated to reflow only the device of interest. The impinging gas jet is deflected and its backwash may cause unwanted reflow of previously formed joints on closely spaced, adjacent components. This can be overcome by the use of baffles that are either applied to adjacent components or by a singular baffle that confines the gas jet to the component to be soldered.

The PCB to be soldered usually sits atop a preheating nozzle or preheating platen. This is necessary to heat the PCB sufficiently so components can be soldered with a hot-gas stream of modest temperature. If the air stream is too hot, it would scorch the PCB or degrade the reliability of the components to be soldered.

The use of hand-held hot-air soldering “irons” is not recommended as there is no consistency in process. Use of such systems often results in scorched circuit boards, damaged devices or poor solder joint quality.

49.9.1 Hot-Gas Soldering Nozzles

Available in a variety of forms, the simplest nozzles is the single orifice, which can be translated around the entire periphery of a component (Fig. 49.46*a*). Some machines offer a double translatable nozzle assembly that can solder two opposing sides of a component simultaneously (Fig. 49.46*b*).

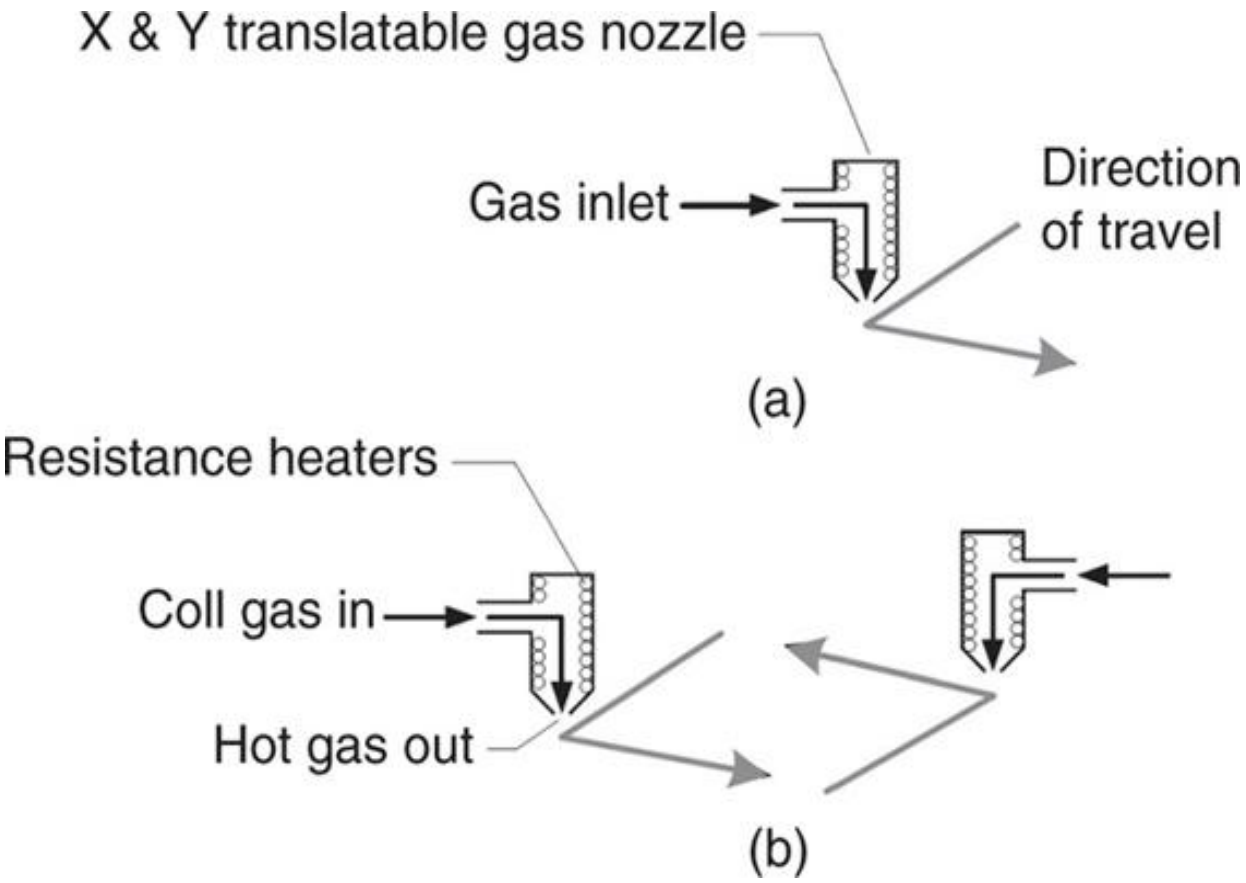

FIGURE 49.46 Hot-gas soldering nozzles. (*a*) Programmable moving nozzle translates hot gas in *x* and *y* axes; (b) double nozzles, each programmable, allow simultaneous soldering of all four sides of a component.

The shielded nozzle (Fig. 49.47) is commonplace, especially for rework. It directs the hot-gas to the components and vents it either laterally or out the top to minimize re-reflow of adjacent components. This will be discussed more fully in the section entitled Soldering Repair and Rework.

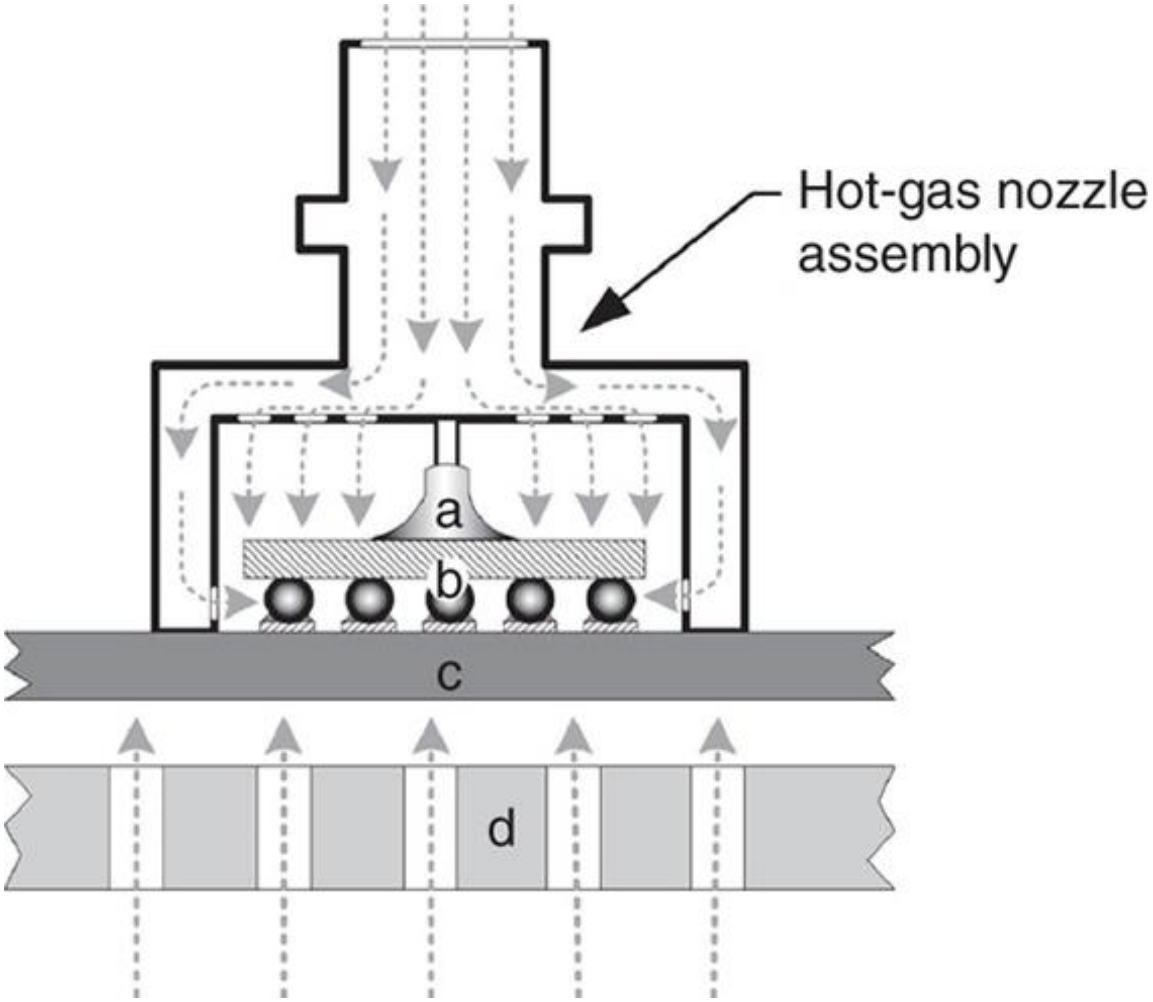

FIGURE 49.47 Cross-section of a hot-gas workstation composed of a shielded hot-gas nozzle and PCB preheater. (a) Integrated pick-up tool, (*b*) BGA, (*c*) PCB, (*d*) hot-gas preheat platen. Hot air flow indicated by dashed arrows

49.9.2 Solder for Hot-Gas Soldering

Solder can be applied to the board as a paste, solid pre-form foil, or solder-coated pad. In all cases, the component must be held down during the soldering process to ensure contact of component leads with bonding pads until the onset of liquidus. Proper gas pressure, temperature, nozzle translation speed (if in a moving system as illustrated in Fig. 49.48), and flux are required to effect solder joint formation. Otherwise, the same reflow considerations are required for this technique as for any other. Heating ramp rate, PCB and solder paste preheating, peak temperature, liquidus duration, etc., must be observed for successful joint formation and for reliable solder joints.

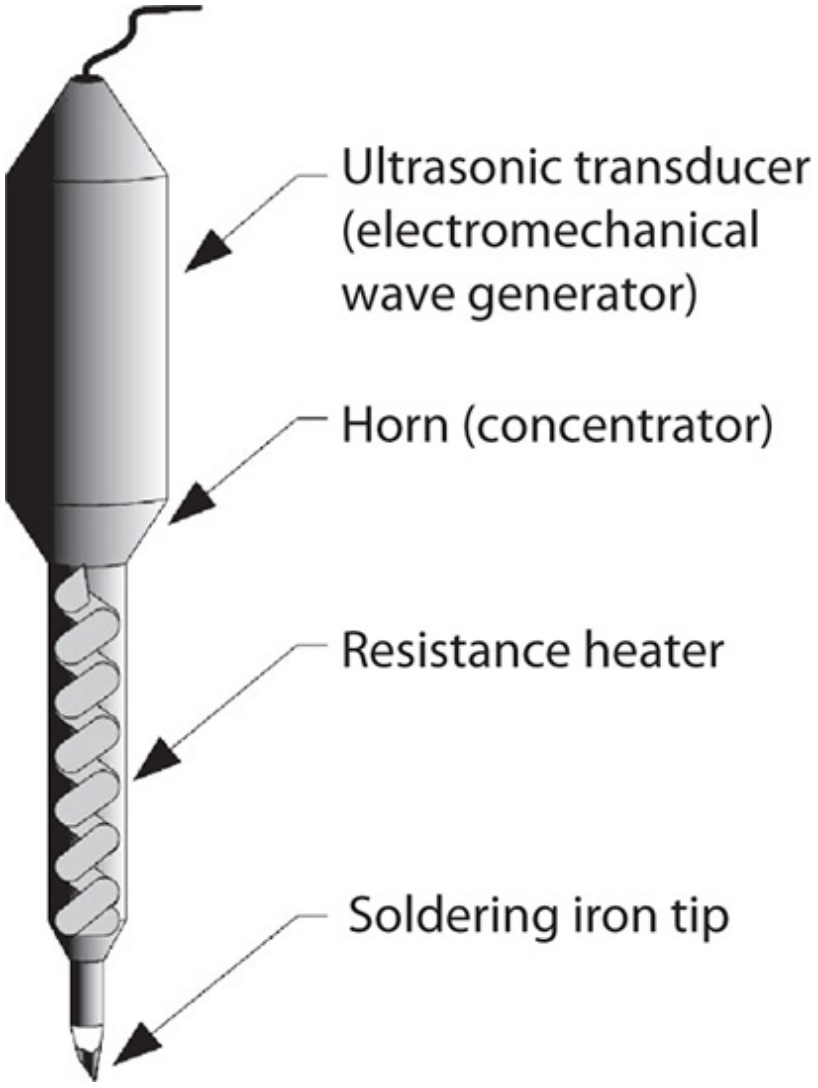

FIGURE 49.48 The ultrasonic soldering iron is composed of four main components: an ultrasonic transducer; a horn for concentrating and directing ultrasonic energy; a resistance heater; and the soldering tip, which emits both thermal and ultrasonic energy.

A thermocouple-instrumented profile board populated with components is needed to determine the proper soldering time-temperature recipe. Adding thermocouples to some solder joints on closely adjacent components is recommended to ensure that the soldering or component removal profile will not inadvertently re-reflow neighboring components.

49.9.3 Flux for Hot-Gas Soldering Nozzles

Solder fluxing agent for this technique is the same for any other soldering application. Solder paste, paste flux or liquid flux can all be used. Care must be taken to heed flux manufacturer's reflow profile recommendations.

If hot-air is being used for component removal/replacement, the flux should be the same used for the initial soldering so as to preclude flux interactions that may lead to corrosion and reliability degradation.

49.9.4 Gas for Hot-Gas Soldering

Two gases are commonly used in use in association with this soldering technique; air and nitrogen. By far, air is the more common of the two, but there are distinct advantages to the use of nitrogen (N_2).

N_2 provides an inert cover during the soldering process. In the absence of an oxidizing agent (air), fluxing agents are more effective and the molten solder is largely without oxide skins that restrict its ability to flow and wet. N_2-shielded

solder joint formation typically results in better wetting and more complete solder fillet formation. However, the cost of nitrogen has to be factored into the needs of the process. It can be used to effectively and more efficiently solder and normally results in better quality solder joints. This alone, may offset the cost of using N_2. It is also effective where soldering is most difficult as it promotes wetting, permits slightly lower process temperature, less flux application and sometimes results in a shorter process duration.

49.10 ULTRASONIC SOLDERING

This method relies on a heated, ultrasonically vibrated soldering tip that simultaneously melts and agitates the solder (Fig. 49.48). The ultrasonic energy is transferred from the soldering tip through the molten solder droplet beneath it and ultimately to the component lead and circuit board pad.

The high-energy agitation of the solder droplet helps to disrupt films of bond-inhibiting oxides and other contaminants from the solder, PCB pad and component lead at solder-metal interfaces. If soldering temperature is appropriate, any exposed solderable metal surfaces are rendered solder-wettable by this technique. Ultrasonic soldering precludes the need for chemical fluxing agents. Aluminum and other difficult-to-join metals can be joined by this method. The viability of this technique has been well proven on a commercial scale in the manufacture of air conditioner heat exchangers.[32,33]

Ultrasonic soldering has also been applied as a batch or continuous mass reflow process. In these instances, the molten solder is ultrasonically agitated while the assembly to be soldered is immersed in it. Similar arrangements have been made for ultrasonically vibrating the part while dipping

it in a molten bath or wave of solder. These mass processes are more common for nonelectronic assembly.

Care must be taken in ultrasonic soldering to tune the tip amplitude and/or frequency to the mass of the system being soldered. Excessive agitation may result in cavitation and splashing of the liquid solder resulting in solder voids and solder balls. The former may detract from joint reliability especially if voids are at a solder/metal interface. Solder balls may pose a risk for shorting fine-pitched leads or pads. Additionally, ultrasonic agitation increases the dissolution rate of any soluble metals into the solder for any given temperature as opposed to other soldering methods. If there is enough dissolution of soldered components, it may change solderability or solder alloy properties, such as melting point or melting range and perhaps negatively influence solder joint reliability.

This technique can be useful for the repair of opens or the installation of new or change-order components onto completed circuit assemblies because no flux is required. A previously cleaned board will stay clean through repair or upgrading operations. This technique is applicable to all peripherally leaded surface-mount components that are not susceptible to ultrasonic energy damage. It can also accommodate through-hole device soldering. Equipment availability is limited, with only a few manufacturers worldwide. Several past and recent publications provide a comprehensive review of this technology's applicability and attributes.[34–37] If this soldering method is employed, studies should be done to ensure that the application of ultrasonic energy combined with heat does not degrade PCB or electronic device performance or long-term reliability.

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CHAPTER 50

SOLDERING REPAIR AND REWORK

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

50.1 INTRODUCTION

As printed circuit assemblies (PCAs) become more densely populated, the probability of rework increases. So does the complexity of rework steps. Rework deserves consideration both in terms of board design as well as in conducting the repair. Deep preheating cycles, careful thermal profiling, and thermal masking of adjacent components become critical. PCAs are often mix-mount [surface-mount technology (SMT) and plated through-hole (PTH)] assemblies. Additionally, they may contain press-fit components or other subassemblies that may be sensitive to overheating. Aside from hand repair with a soldering iron, there are two techniques that are mainstays of repair: solder fountain and hot-gas. The former is a variant of wave soldering and is tailored to removal or post-soldering addition of PTH (solder-tail) components. Hot-

gas (also known as hot-air) soldering is used primarily for removal and replacement of SMT components.

Because repair of dense assemblies is difficult, this chapter covers some of the finer points of rework. The onset of Pb-free soldering has increased the difficulty of repair processes due to generally higher melting temperatures and slower wetting times that are characteristic of the most prevalent Pb-free solder alloys. Otherwise, repair involving Pb-containing solders and Pb-free solders is the same.

50.2 HOT-GAS REPAIR

This technique consists of directing a heated stream of air or other process gas such as nitrogen (N_2) at the component to melt solder for removal or replacement of a component. Modern hot-gas repair stations are sophisticated, with computer controlled heaters, programmable thermal cycles, predictive reflow profiling, vision systems to assist in component alignment to bonding pads on the printed circuit board (PCB) and preheating stations or stages. Hot-gas repair is most often used for SMT components but can be adapted for certain PTH component removal.

50.2.1 Hot-Gas Repair Equipment

50.2.1.1 Hot-Gas Nozzle. The heated gas is generally delivered through a component-specific nozzle. The gas stream is directed at the top of the component, under the component (between the PCB and component bottom), or a combination of the two, depending on the nozzle design (Fig. 50.1).

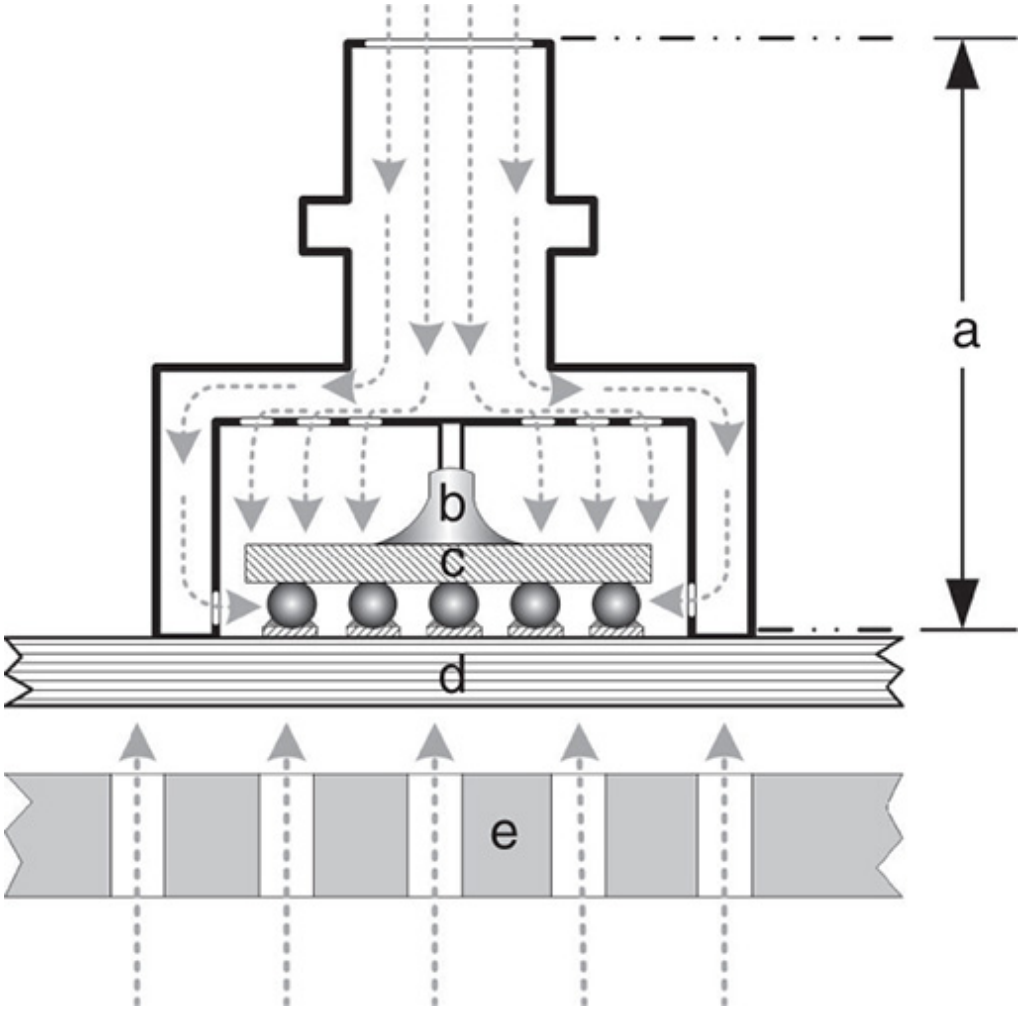


FIGURE 50.1 Schematic of hot-gas repair apparatus for removal and replacement of a surface-mount component. It is comprised of a baffled nozzle (*a*) which directs hot-gas at the component to be removed; in this case a BGA (*c*). Hot-air is also directed through a heated platen (*e*) on the underside of the PCB (*d*) directly beneath the component to be repaired in order to preheat the circuit board, lessening the thermal load and shortening the rework cycle. A heat-resistant suction cup (*b*) is used to remove the BGA once all solder joints have reached reflow temperature. It is also used to pick and place the new component to be soldered. Gas flows are shown as dashed arrows.

50.2.1.2 Preheater. Preheaters are used to help overcome the thermal inertia of the board. Since the nozzle exposes only a small amount of the board to a high-temperature gas stream, heating through this mechanism is limited due to the heat-sinking effect and large thermal mass of the PCA. The preheater uses hot gas or infrared lamps to heat a large area of the board. The preheating is set to a

temperature much lower than the reflow temperature of the solder, but high enough that reflow can take place on the targeted component in a reasonable period of time. Preheating helps to avoid overheating the component to be replaced or other components adjacent to the repair site. Most hot-gas repair machines have a built-in bottom-side preheater.

50.2.1.3 Vacuum Pickup Device. This is generally a silicone rubber suction cup or a metal tube nested within the nozzle and connected to a vacuum pump. Silicone is chosen for its heat resistance and compliance. The vacuum can be toggled on and off to pick up and release a component. The vacuum pickup device serves two purposes. First, it is used to remove a component from the circuit board once the component has been heated by the hot-gas to the point of solder reflow. Following preparation of the repair site, the suction cup is used to hold the replacement component rigidly so that it can be aligned to bonding pads and accurately placed.

50.2.1.4 Adjustable Stage or Adjustable Nozzle Assembly. This permits alignment of the nozzle to the component in need of repair. Such stages or gantries are generally adjustable in the *x, y, z*, and θ axis. It is important for component removal but even more critical for component replacement and alignment of component leads to PCB bonding pads.

50.2.1.5 Vision System. This is used to align component leads to PCB bonding pads. Usually a split-image video system permits a simultaneous view of both component leads and board bonding pads. The images are superimposed and the operator manually adjusts them for the best lead-to-pad alignment.

50.2.1.6 Computer Control. This is the heart of most hot-gas machines. It monitors and controls the various operations of the system, including preheat and thermal profile steps. The rework engineer programs the profile manually or uses a predictive routine to rough out a thermal profile and perfect it.

50.2.2 Hot-Gas Repair Process

50.2.2.1 Nozzle Selection. A hot-gas nozzle appropriate for the part is selected. Sometimes a nozzle can be useful for a family of parts but the nozzle must be size-appropriate so as not to interfere with other adjacent parts on the PCA. It must also be matched to deliver the right amount of hot gas for soldering the part. Most hot-gas station manufacturers have a standard set of nozzles available and can custom make nozzles appropriate for the task. Even some long connectors can be removed and replaced with hot-gas soldering with an appropriate custom nozzle.

50.2.2.2 Thermal Profiling. As with any reflow process, whether for first-pass build or for repair, it is necessary to construct a thermal profile board as previously described to assess the impact of heating and to ensure that the heating is adequate, in accordance with the thermal limits described by the solder paste manufacturer, the component specifications for thermal exposure, best solder wetting, and minimized intermetallic formation. In the case of repair, a dummy (profile) board is used with thermocouples attached to the component to be removed and critical adjacent components to ensure that reflow conditions are correct. For large ICs, multiple thermocouples are used to gauge the temperature in the center of the device and along the edges of the IC. Multiple thermocouples are also embedded in the profile board both to ensure that reflow conditions are met

and that adjacent components are not overheated through the rework process.

50.2.2.3 Component Removal Preheat. As discussed previously, preheating may be necessary to overcome the thermal mass of the assembly and to ready the board for the reflow step. This is accomplished with a heat source under the PCB such as hot-gas heater, heated platen or an infrared heater. Preheat temperature is set well below liquidus onset for the solder alloy in use. The goal should be to confine reflow to the device being removed or replaced and to discourage widespread reflow of component solder joints adjacent to the repair site.

50.2.2.4 Reflow and Removal. The same considerations apply for this as for any reflow step. The ramp, soak, peak temperature and time above liquidus are dictated by the solder alloy used and should roughly match the time-temperature profile parameters as for the initial assembly of the board. Once the component has reached complete reflow, the vacuum pickup tool is engaged and the component is lifted vertically. Care should be taken to minimize the time above liquidus to minimize intermetallic compound thickness, bond pad lifting or other PCB damage.

50.2.2.5 Site Dressing. During the component removal step, solder surface tension capriciously allows some of the solder from the joints to remain on package leads and some is left on the PCB bonding pads. In the case of some area-array packages [BGA, ceramic ball grid array (CBGA), mico-BGAs, etc.], the ball may remain with the package or with the land. This can make solder land dressing a labor-intensive operation. Care at this step is critical for success in reattaching a fresh component and for PCA reliability.

Following component removal and while the board is still hot, the solder lands on the PCB can be prepared for

component replacement by means of a hand soldering iron and a braided copper solder wick or a solder vacuum machine that simultaneously heats the pad by hot gas and vacuums up any excess solder. The goal is to roughly even out solder remaining on the pads making them smooth enough so as not to interfere with fresh component placement. If solder paste is to be added for component replacement, bond pad surface topography is even less critical because the solder paste will add significant vertical compliance and any remaining solder on the pad will melt into the solder mass of the solder imparted by the paste. The pads do have to be flat enough to allow the mini-stencil to sit flat on the board if solder paste is added in that manner. Too much pad dressing only encourages intermetallic build-up. If using the copper wicking braid, care must be taken not to allow the solder to freeze before the braid is pulled from the pad otherwise when the braid is lifted the pad from the board will be pulled up with it and the board will have to be scrapped.

50.2.2.6 Part Bake-Out. As with first pass soldering, it is important to observe rules governing component bake-out to remove any absorbed moisture and preclude part cracking (popcorning) during the reflow heating cycle. Guidance for part baking can be found in IPC/JEDEC J-STD-033.[1]

50.2.2.7 Solder Paste or Flux Deposition. For most SMT components, solder paste is added to either the board or the component to effect a reliable solder joint for component replacement. This is generally done by mini-stencil similar to what is used for SMT solder paste deposition for the PCB, but on a smaller scale; the stencil is only slightly larger than the component footprint. The paste is pushed through the stencil apertures with a razor blade or a miniature stainless-steel squeegee. Programmable syringe-dispenser machines are sometimes used, but solder paste is

known to separate when under pressure, that is, solder alloy separates from the solder flux. Choosing the largest needle bore, slowest dispense rates, and lowest pressures will help to mitigate paste separation. Also, use of direct drive auger pump rather than an air-pressure-driven dispenser will help to reduce paste separation. As a rule, the amount of solder paste used for repair should be roughly the same as for the initial build.

Instead of stenciling or depositing solder paste on the dressed pads, some choose to add flux to the pads following site dressing and use the solder from the BGA balls to effect solder joints. Another methodology is to print or dispense solder paste on the BGA balls then place the component onto the dressed site. Yet another variant is to dip the BGA balls into solder paste and then place the device on the dressed pads. For some applications these alternate techniques may be adequate but there are reliability concerns which will be discussed later in this chapter.

50.2.2.8 Soldering Preheat. After solder paste or flux deposition, the board is preheated to a temperature about 50 to 70°C below solder liquidus. Preheating of component and PCB is an important part of the reflow profile. Preheating should mimic the original SMT soldering cycle and align with solder paste or flux requirements as specified by the solder paste or solder flux manufacturer. Heating ramp rate should fall within the manufacturer's specification for the component to be soldered just as in SMT reflow.

50.2.2.9 Component Pickup. During the PCB preheat cycle, the component is picked up and readied for placement. After the component is placed on a pickup nest adjacent to the PCB, the nozzle with vacuum pickup is aligned and lowered over the component. Next the vacuum pick-up is activated. The component is raised up and brought over to the dressed site in preparation for placement.

50.2.2.10 Component-to-PCB Alignment. A split-vision optics system, part of the rework station, is used and the semi-transparent video image of the picked component is superimposed over the video image of the PCB bonding pads at the placement site in preparation for placement.

50.2.2.11 Placement. Once component leads are aligned to PCB bonding pads, the component is lowered on to the dressed, solder-pasted or flux-coated bonding pads and the thermal cycle continues.

50.2.2.12 Reflow. Heating to the component is increased by ramping up the temperature and volume of the hot-gas. Heating of the solder paste (or flux), the device to be soldered and the PCB should be in accordance with paste (flux), device and PCB manufacturer specifications. Just as in the original SMT oven reflow cycle, heating ramp-rates for the solder paste and for the IC being soldered must be observed.

50.2.2.13 Cooling. After reflow has been achieved through the preset profile, PCB and component heating is turned down or off in accordance with prescribed profile ramp-rate as is appropriate for the solder paste and the device being soldered. Once the solder joints have reached solidus, the PCB with its newly soldered replacement component can be removed from the hot-gas repair station ending the repair cycle.

50.2.2.14 Inspection. Due to the manual nature of hot-gas repair, it is even more important to inspect soldering results. For area array devices (BGAs, etc.), transmission x-ray inspection is suggested to ensure that all contacts are soldered and bridge-free. Visual inspection should be done looking for evidence of PCB charring, delamination, component cracking or unusual bulging (evidence of popcorning). Check adjacent components to ensure they are

still soldered, not cracked, scorched or otherwise damaged. Inspect bottom-side components for damage and solder joint integrity especially in the case of back-to-back BGAs when one is involved in removal and replacement. If in-circuit testing or functional testing is done on the first-build product, then it should be applied to the reworked product also.

50.2.3 Hot-Gas Rework Guidelines and Reliability

A repaired part will be less reliable than a part soldered in the initial surface-mount process. The key in all reflow steps is to limit the amount of time at or near solder liquidus in order to minimize intermetallic compound (IMC) formation. IMC thickness increases with each reflow cycle and its formation is temperature-dependent also. IMC is the weakest link in terms of solder joint structure. Due to its brittle nature, the thicker the IMC the more vulnerable the solder joint to shear, shock and vibration. Therefore, during component rework and replacement, minimizing thermal excursions to limit IMC thickness is all important. Strive to keep the reflow cycle similar to what was used during original SMT oven reflow soldering for that PCA.

When a component is removed and replaced, IMC from previous soldering operations or other thermal excursions remains on the pad. IMC cannot be removed from the pad since it a result of solder alloying with the pad and is an integral part of the pad. For illustrative purposes, consider the case of a surface-mount component with a copper lead-frame and copper bonding pad on the bottom-side of the PCA. During initial SMT assembly, the bottom-side of the board is built first. During that soldering process, an intermetallic layer forms where the solder is in contact with the joined metals (bond pad and component lead). During

top-side soldering of the same PCB, the components on the bottom side of the board undergo a second reflow and the IMC further grows. Assume that a part soldered during the bottom-side assembly fails and requires removal. The removal and replacement processes necessitate additional reflow cycles to the affected component site. Steps include (1) component removal, (2) site dressing, and (3) component replacement and re-soldering. In total, from the onset of the SMT build to the end of removal and replacement of the failed component, the PCB will have undergone five reflow cycles at the site of the replaced component. With each soldering cycle, the intermetallic layer builds and reliability generally degrades with increasing intermetallic layer thickness. Therefore, careful process control is needed to minimize time above solder liquidus. Figure 50.2 depicts soldering and repair steps and hypothetical impact to intermetallic layer thickness common to any soldering and repair cycle.

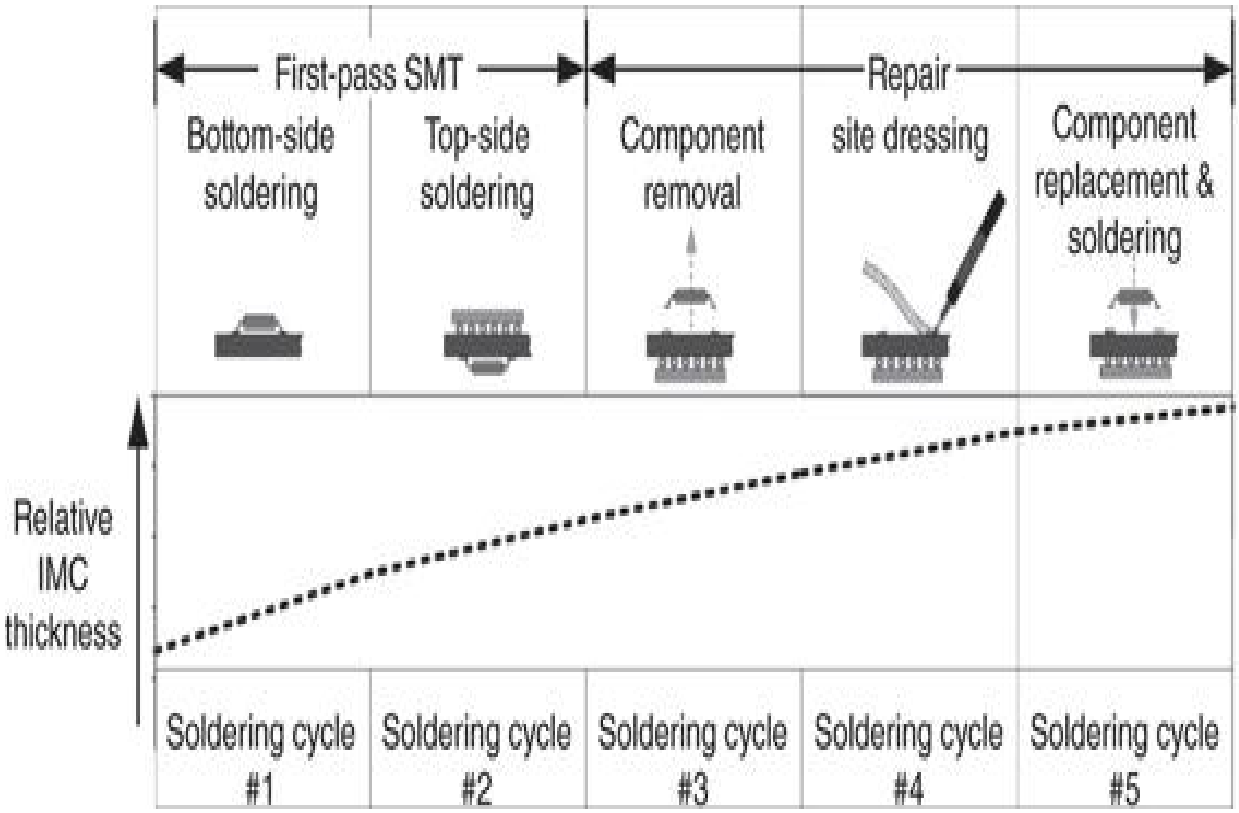


FIGURE 50.2 Intermetallic (IMC) thickness as a function of soldering cycles: the thermal history of bond pads. Soldering steps required for first-pass soldering of a bottom-side component on a PCB and successive reflow and pad treatment steps encountered during repair. Note that the intermetallic compound formation thickness is not truly linear with each step. IMC thickness is dependent on materials of the soldering system, time above solder alloy liquidus, peak temperature, etc. The illustration is meant to show that with each reflow cycle there is increased intermetallic layer thickness.

Generally the number of SMT solder rework cycles per component per board is kept to two or three. Beyond that, the board should be scrapped to avoid reliability problems.

The thermal profile used for component replacement should be predicated on the four things: (1) the solder paste manufacturer's recommendations for reflow; (2) component manufacturer's specification for peak temperature and heating and cooling ramp rates; (3) results of thermal profile established from trials with an instrumented product profile board; and (4) optimization of the reflow profile.

For no-clean boards, the same solder paste used for the initial assembly should be used for the repair. If solder paste is not added, then a paste flux (identical to that comprising the solder paste) should be used. This will obviate solder chemistry interactions reducing the likelihood of long-term corrosion. For aqueous-cleaned boards, no-clean solder chemistry is often used for repair to preclude the need for another wash cycle.

Sometimes in BGA repair, solder paste is not used. Instead, solder from the BGA ball provides solder for the bond. This technique requires the use of flux for the soldering. The flaw in this methodology is that resultant solder volume is lower as compared to the original joints where solder paste was utilized. Without the added solder (from the paste), BGA reliability is diminished. In fact, any repaired joint is less reliable than a first-pass solder joint due to thickening intermetallic layer formation that comes with each reflow cycle as previously discussed. Addition of solder paste compensates for small differences in BGA ball sizes. If the

component is light enough to float on the molten solder, as will most plastic BGAs, it will result in a taller solder joint which has more columnar compliance making it less prone to failure by mechanical perturbation. Eliminating solder paste is not an option for area-array devices with noncollapsible interconnects, such as ceramic column grid arrays (CCGAs) or ceramic BGAs (CBGAs) since their interconnects (balls or columns) are of a high-temperature solder alloy or metal and will not reflow under normal PCA soldering conditions. Therefore, solder has to be added for re-bonding of this type of component.

Often an attempt is made to salvage BGAs and other parts removed during the rework process. They are re-balled or solder paste is added to either the PCB or the part to re-solder it. Unless an IC device is qualified for the extra reflow cycles during rework (removal, re-balling, replacement on the PCB), then its reliability will be unknown. When IC manufacturers sell ICs, their technical specification for each device lists the intended number of reflow cycles. Beyond that number, device performance is either unknown or degraded in performance, reliability or both.

50.3 MANUAL SOLDER FOUNTAIN

PTH components are generally repaired by solder fountain, which is akin to a wave-soldering system with a vertically pumped jet or stream of solder. It is significantly smaller than a wave-soldering machine and can be configured with or without conveyor, fluxer, and preheaters. It can be so small that it is bench-top mounted. It permits an operator to manually remove parts and replace them. The classic solder fountain is a manually controlled system. Nozzles are chosen to shape the molten solder jet to match closely the size of the area to be soldered. Nonetheless, a shield or pallet

should be used to localize the soldering and to prevent contact of the molten solder to other previously soldered components on the board.

The board requiring repair is shielded, except in the area of component replacement, and positioned over the solder fountain. The shaped solder fountain is directed at the repair site. Once the component solder joints go molten, the component can be pulled out with gloved hand or pliers, some flux can be added, and a new component can be inserted to complete the rework within one thermal excursion. Flux used at repair should be the same as the one used for first-pass soldering of the device being reworked. If not the same flux, one from the same flux family should be chosen in order to prevent adverse interactions and corrosion in the long-term. Care must be taken to ensure that all solder joints have gone molten on the component being removed. If not, PTH barrels can be ripped out of the board or barrel annuli can be damaged resulting in a scrapped PCA.

To aid the solder fountain process, dense assemblies can be batch-heated in a box oven to make the repair process more efficient and limit exposure of the board to the turbulence of the molten solder wave. Limiting the soldered assembly’s time near or above solder liquidus is key for solder joint and product reliability. As mentioned previously, time above solder liquidus along with peak temperature will define the intermetallic thickness for a given metals system, and intermetallic thickness will in part define the solder joint reliability. The turbulence of the solder fountain, like its kin the wave solder machine, is known to cause the dissolution of metals, such as copper, into the molten solder. The manual nature of some solder fountains results in an out-of-control and irreproducible process entirely dependent on operator vagaries. Copper PTH barrels, barrel annuli (bonding pads atop the PTH) and PTH solder-tails can be thinned or completely dissolved, impairing electrical interconnect or degrading long-term solder joint or device

reliability. For this reason, precise process control, including strict exposure time limits and minimized solder pot temperature, must be imposed for such manual operations. This process is best suited for repair and should be avoided, if at all possible, for first-pass soldering of printed circuit assemblies. There are automated, commercially available systems that help to limit the potential damage of solder-fountain rework and provide a reproducible process.

50.4 AUTOMATED SOLDER FOUNTAIN (SINGLE-POINT SOLDERING)

This version of the solder fountain incorporates a programmable head and is used mostly for first-pass soldering, but can be an effective soldering repair tool. Once the PTH component is removed, the site is prepped, fluxed and a new component is inserted into the solder-cleared plated through-holes. A programmable nozzle emitting a precise jet of molten solder is directed at leads of the component to be soldered on the backside of the PCA. The nozzle allows point soldering of very fine PTH pitches en masse or even one lead at a time.

50.5 LASER

Laser is a recent innovation in rework and repair. In the commercial incarnation of this technique, a laser beam is quickly scanned repeatedly around component leads or, package surface to heat it. It is most effective for low thermal mass packages (small area-array devices such as BGAs and chip-scale packages (CSPs) but has been applied to thermally massive CBGAs, CCGAs, etc. Since the energy of

the laser beam is more tightly confined to the area it irradiates, the heating can be highly localized as compared to hot-gas repair methods. This can be advantageous when trying to remove or replace a component on a densely populated, double-sided PCA. Preheating of the PCA may be required to enhance reflow and package removal.

The same caveats must be kept in mind regarding IMC formation and pulling a component before it is fully reflowed. If irradiating component leads, care must be taken to assess the assembly for its laser damage threshold so as not to char components or carbonize the PCB surface during either removal or component re-soldering. Addition of flux to the component leads will help in the thermal transfer, aid in preheating the next lead to be unsoldered. It also minimizes the possibility of charring damage to the PCB surface.

50.6 CONSIDERATIONS FOR REPAIR

50.6.1 Mixing Aqueous with No-Clean Chemistries

Care must be taken when using fluxes for the rework and repair processes. If an aqueous-clean solder chemistry is used for building the PCA, then either no-clean or aqueous flux formulations can be used. If an aqueous chemistry is used for the repair, then the board must be subjected to another aqueous cleaning cycle. Be sure to check that all components at that stage are compatible with the aqueous cleaning process.

No-clean solder flux formulations can be used for rework and repair even if the PCA was manufactured with a water-clean chemistry and already cleaned, although the reverse is not recommended. Sometimes when a no-clean board is subjected to an aqueous cleaning process, the no-clean flux

residue takes on a white, gummy characteristic that is conducive to dendritic corrosion and ensuing soft or hard electrical shorting. Saponified aqueous cleaning can be used, but must be tested for effectiveness in removing the polymerized flux residue from the no-clean process and for compatibility with the selected no-clean flux to avoid generation of corrosive byproducts. This is particularly important under connectors, area-array devices, and other components with low headroom between the underside of the body and the PCB surface.

50.6.2 Pooled Flux

Another consideration when using no-clean solder chemistries is that of pooled, unactivated flux residue. No-clean solder flux is generally harmless after it has gone through the thermal cycle associated with solder reflow. It is activated and denatured by the heat of soldering. If the flux is applied generously and the flux pool does not see the high temperatures associated with solder joint formation, acids remaining in the unheated flux residue can cause reliability problems. These acids are normally denatured, evaporated, or sublimed through the high-temperature excursions of the soldering process. If the flux acids remain, corrosion can occur in the long term. There are commercial flux solvents that can be used to dilute and wash away excess flux; otherwise, the assembly can be baked briefly to about 120°C to denature the flux. Check with the flux manufacturer for specific recommendations regarding flux residue management and activation time and temperature. The problem can be avoided totally by eliminating the use of liquid flux and using small amounts of paste flux instead. In the case of flux-cored solder wire, use the smallest diameter practical to limit flux residue.

50.6.3 Component Bake-Out

Components that have been exposed to the factory atmosphere may be subject to water absorption. When they are heated during rework, where the heating cycle is more localized and perhaps more extreme than in the slow heating experienced during mass oven reflow soldering, moisture-induced popcorning may be a more serious problem. Follow IPC, JEDEC or component manufacturer recommendations for pre-soldering moisture bake-out regimes.

50.6.4 Gold Finger Protection

There is ample opportunity to ruin gold edge-connector fingers on a circuit board during the repair operation. Keep both solder and flux away from gold fingers during repair. Mechanical shields or acrylic-adhesive polyimide tape can be used to protect fingers from smeared solder paste, loose solder debris, or flux. If solder comes into contact with gold and heated to reflow, the gold will rapidly dissolve into the solder mass and the solder will spread on the finger. The solder cannot be removed from the gold finger without replating; a costly process that can also be a source of corrosion on the finished PCA. Solder is not a reliable connector contact material, especially with today’s high-density, low normal-force electrical connectors.

Keep solder away from gold fingers. Keep gold finger temperature as low as possible. Ensure that gold fingers are never handled, even with gloved hands. Avoid lint and fibers. If required after rework, clean gold fingers with a suitable solvent to dissolve any flux residue. Use a soft brush, lint-free cloth, or other nonabrasive material for this cleaning. Clean gold fingers on each side of the board separately. Avoid folding the lint-free cloth over both edges and wiping repeatedly; the cloth will wear against the glass-epoxy edge

and shred, leaving lint on the board. A better alternative is to use a soft, ESD-safe brush with solvent to clean the gold finger followed by a filtered, ionized air blow-off to dry and remove any remaining solvent, lint, fibers or bristles from the cleaning process. Avoid any materials that will scratch the gold surface finish on the fingers. The underlying nickel, if exposed to the atmosphere will oxidize and, is known to be problematic for separable contact reliability.

50.7 REFERENCE

1. IPC/JEDEC J-STD-033, “Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices.” JEDEC, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.

PART 9

NONSOLDER INTERCONNECTION

CHAPTER 51
PRESS-FIT INTERCONNECTION

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

51.1 INTRODUCTION

Electronic connectors are attached to printed circuit boards (PCBs) in four ways (see Fig. 51.1):

1. Oven reflow surface-mount technology (SMT) soldering
2. Wave soldering (for solder-tail components)
3. Pressure interconnect, a solderless method relying on mechanical forces to hold interconnect elements together to make contact
4. Press-fit, another mechanical, solderless technique (the subject of this chapter)

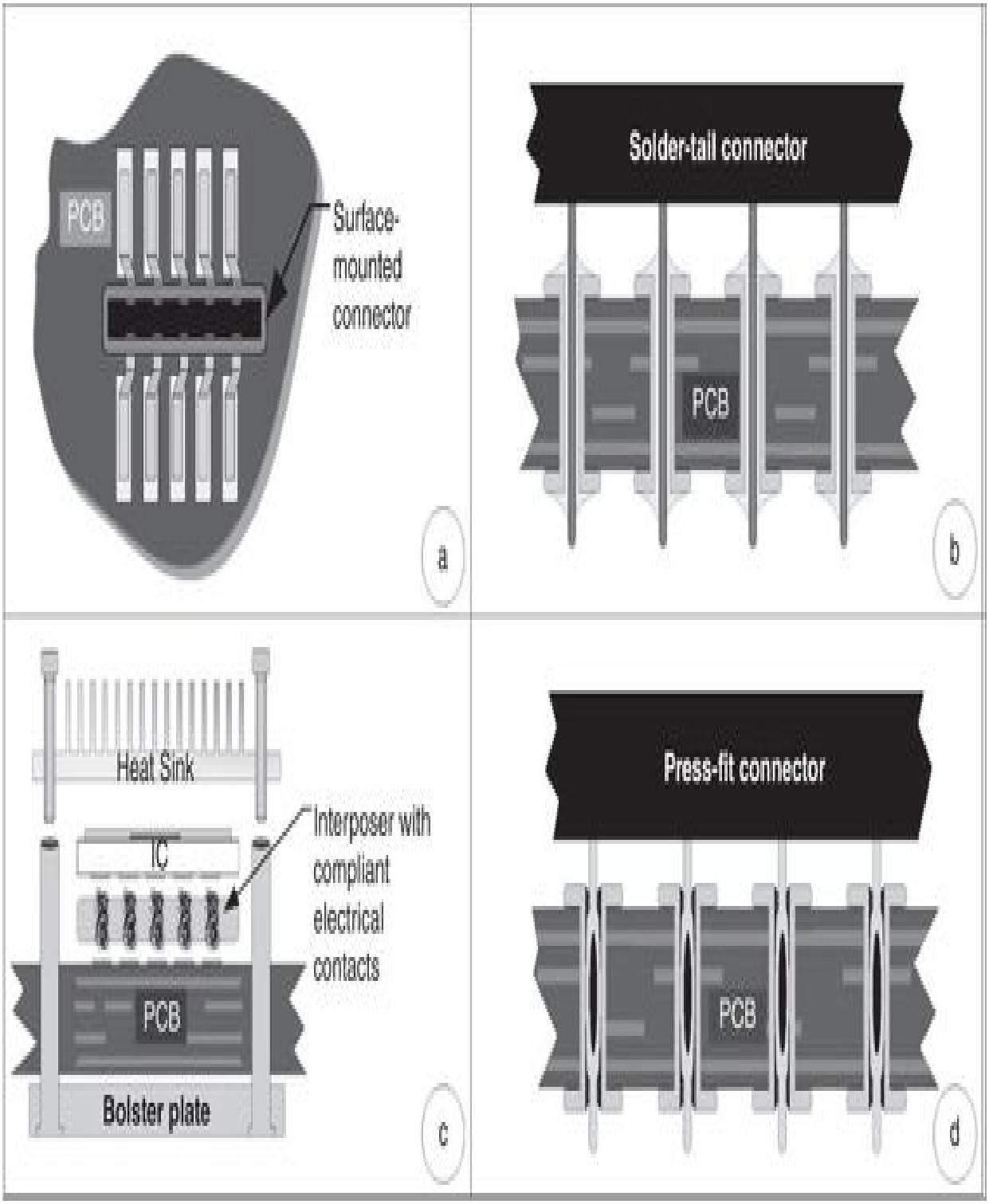


FIGURE 51.1 Four methods of connector attach to PCB: (*a*) SMT applied by oven reflow soldering; (*b*) plated through-hole (PTH) solder-tails that are wave-soldered; (*c*) pressure-interconnect, which relies on mechanical forces for electrical contact; and (*d*) press-fit, which relies on mechanical deformation of the connector lead and/or PTH barrel to make intimate electrical contact.

Press-fit, also referred to as *press-pin, compliant-pin*, and a number of other trade names, has been in use for many years and is a proven and reliable interconnect method. Once used exclusively for passive backplanes, more recently press-fit connectors have gained in popularity and are commonly incorporated on complex motherboards and daughter-cards. Just as circuit boards have become more complex (thicker, higher layer counts, densely routed circuit traces, and high component counts), so too, press-fit connectors are available with high pin density (pin pitch down to 1 mm) and pin counts in the thousands per connector and even strip-line shielding for enhanced high-speed signal performance. Press-fit connectors can be applied to either or both sides of a PCA and are repairable, although first-pass assembly yields are always near 100 percent. Press-fit is easier and more reliable than soldering and does not subject the printed circuit assembly (PCA) to additional thermal or chemical processes—an advantage for reliability, and especially advantageous for today's dense circuitry. Since it requires very little energy (no soldering), minimizes materials (no solder), and calls for no chemicals for its application, the press-fit process is environmentally favorable. The process is simple in theory and generally so in practice, relying on oversized connector leads forced into in plated through-holes (PTHs) in the PCB. The plated through-holes are sized specifically for the press-fit connector. As the connector pin is forced into the PTH barrels, there is slight deformation to the PTH barrel and the press-fit pin. The result is a mechanically stable, environment-impervious electrical contact.

51.2 THE RISE OF PRESS-FIT TECHNOLOGY

There is resurgence in the popularity of press-fit connectors driven by (1) increasing board complexity, (2) the component density of today's PCAs, (3) the appearance of hybrid backplanes populated with active components, and (4) new offerings of high-density, high-speed press-fit connectors. Press-fit connectors are typically used on very thick boards that would be difficult or impossible, to wave-solder. Elimination of wave soldering increases manufacturing yield and allows a denser component layout on the bottom side of the board.

Connector bodies may or may not be compatible with the thermal rigors of reflow or wave, so press-fit connectors are typically applied after all mass soldering (reflow and wave) of the PCA is completed. Further, press-pin connectors are not generally soldered into place since rework would be rendered impractical. Rework of press-fit connectors will be discussed later in this chapter.

51.3 COMPLIANT PIN CONFIGURATIONS

There are many different press-fit pin configurations, far too many to review. Instead, four styles will be described as an introduction to press-fit technology.

51.3.1 Square Pin

Composed of a pin of square or rectangular cross-section, it is sized to deform the board's plated through-hole slightly upon insertion. This is the proverbial "square peg in the round hole." The lead is tapered at its tip to facilitate initial PTH insertion (Fig. 51.2).

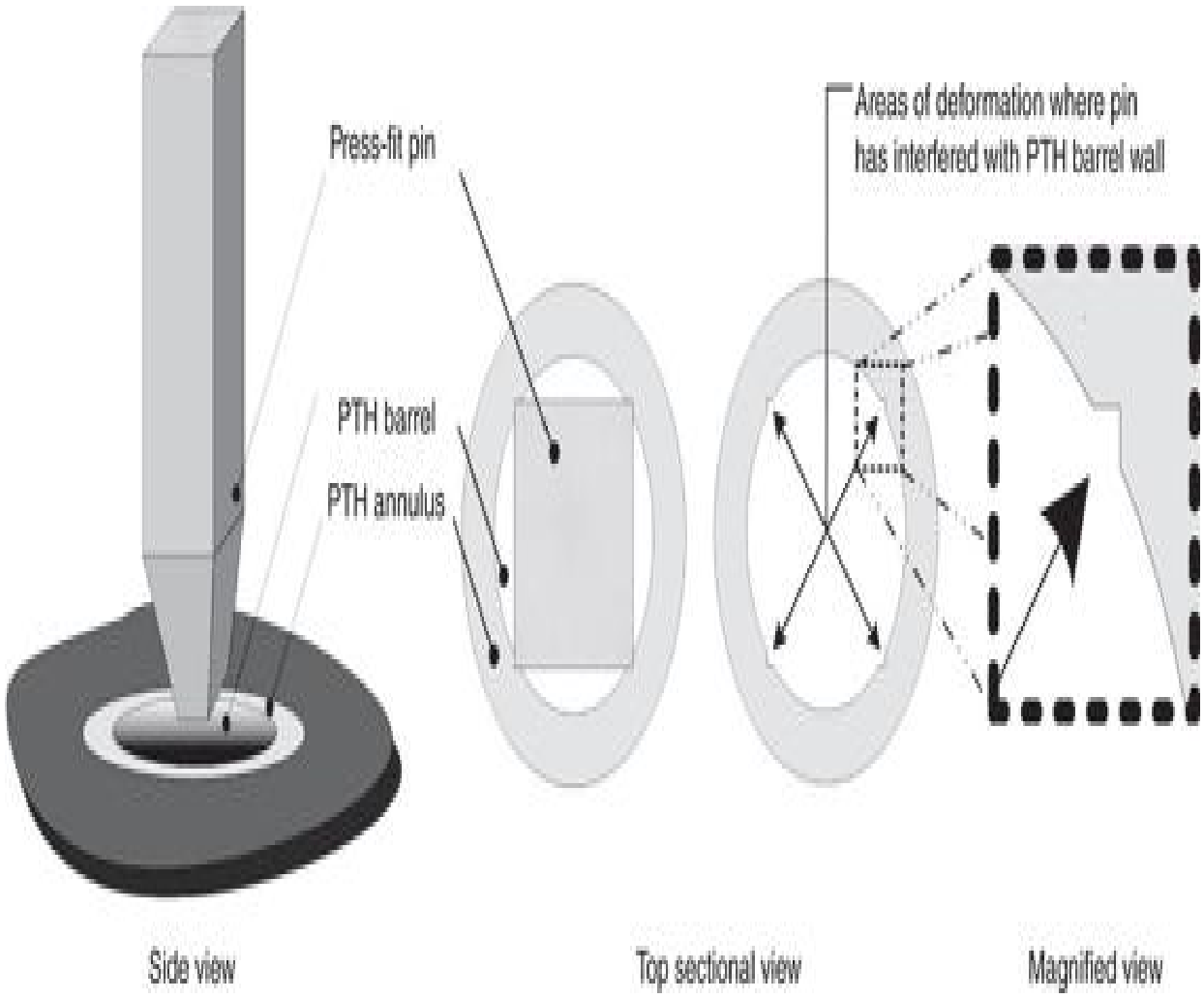


FIGURE 51.2 Tapered square or rectangular pin forced into a round hole. This is the most primitive of press-fit techniques and has been largely supplanted by “compliant-pin” technology.

51.3.2 H-Section

This is a variant of the square-pin. It consists of a sculpted rectangle; an “H” in cross-section. Its design imparts a slight amount of compliance as the tops and bottoms of the “H” section are meant to deform upon pressing into the PTH (Fig. 51.3).

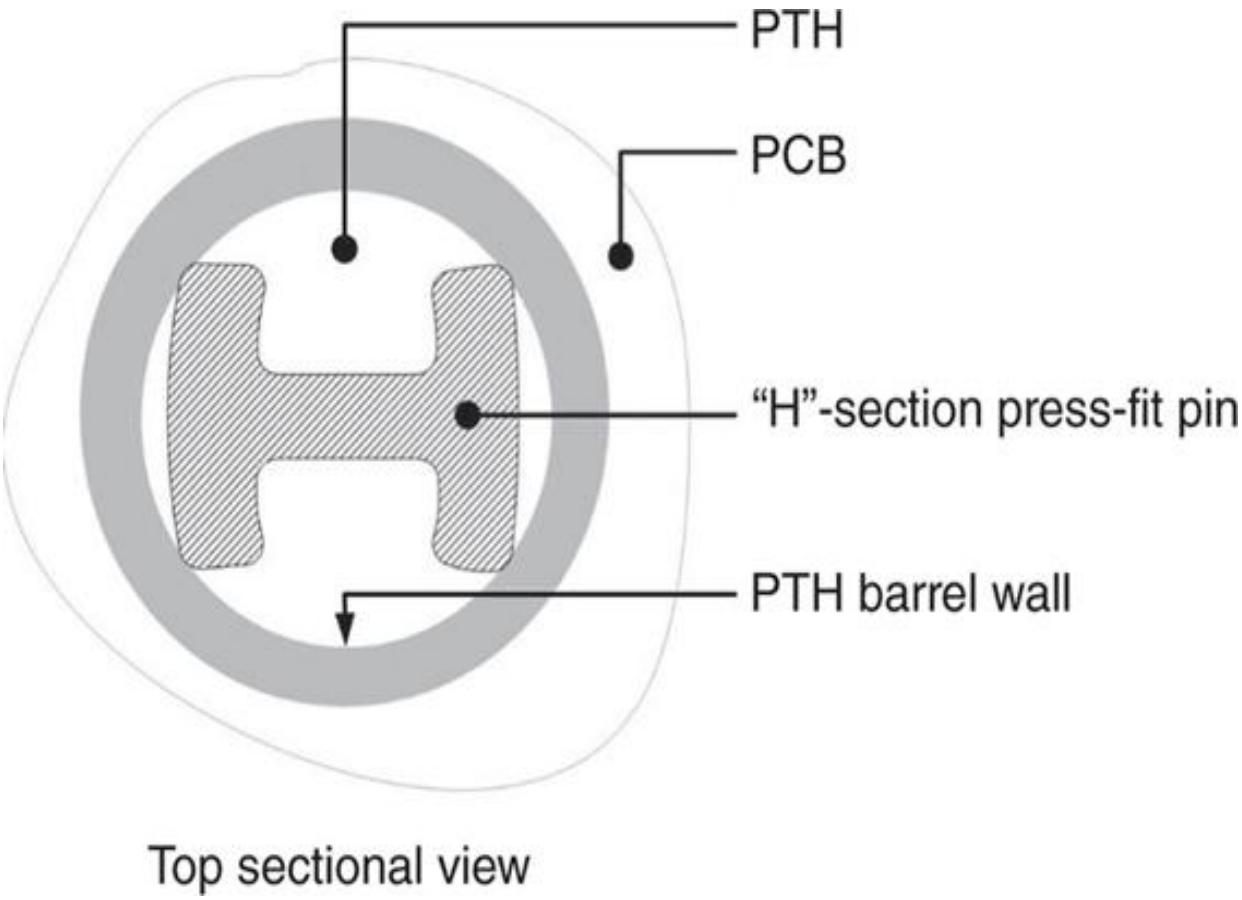


FIGURE 51.3 “H”-section press-fit pin. The sculpted cross-section of the pin allows it to deform slightly. This deformation, along with some deformation of the PTH barrel upon insertion, results in reliable mechanical and electrical contact.

51.3.3 “Action Pin”

It is composed of two separate blades, individually angled, one in front of the other. Upon pressing, the blades slide past each other in opposite directions and spring against the PTH wall to impart electrical contact and mechanical stability (Fig. 51.4).

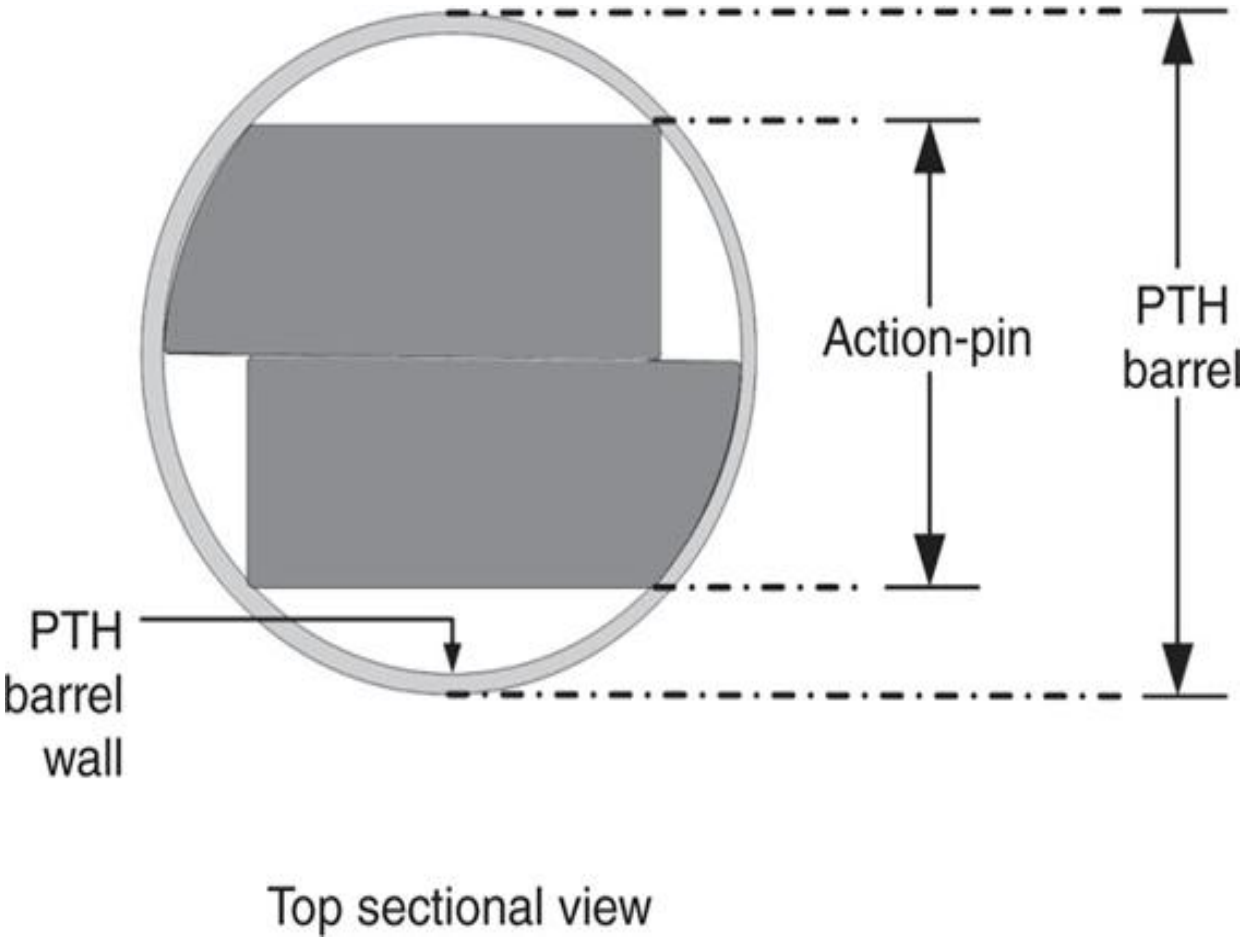


FIGURE 51.4 “Action-Pin”. Two independent blades, one in front of the other, slide past one another and are forced against PTH barrel wall for electrical contact and mechanical anchoring.

51.3.4 “Eye-of-the-Needle”

The fourth and most prevalent press-pin design is the collapsible pin known as “eye-of-the-needle” (EON) (Fig. 51.5). Upon insertion and pressing into the PTH, the compliant section of the pin folds upon itself axially in a controlled manner, as depicted in Fig. 51.6.

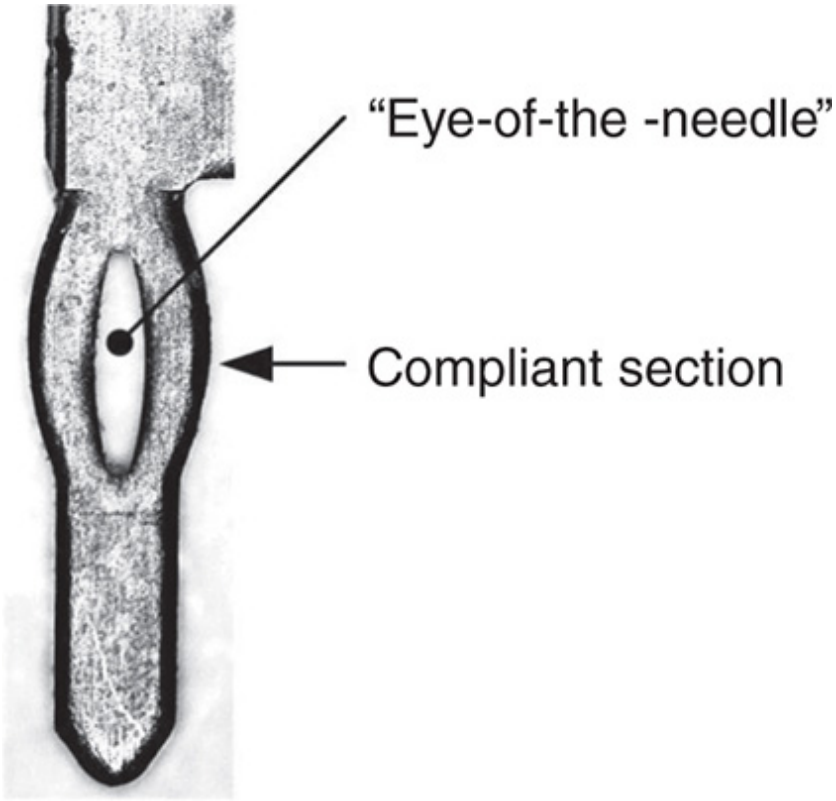


FIGURE 51.5 “Eye-of-the-needle” configuration press-fit pin, shown before compression. The compliant section is meant to deform into and against the PTH barrel upon pressing.

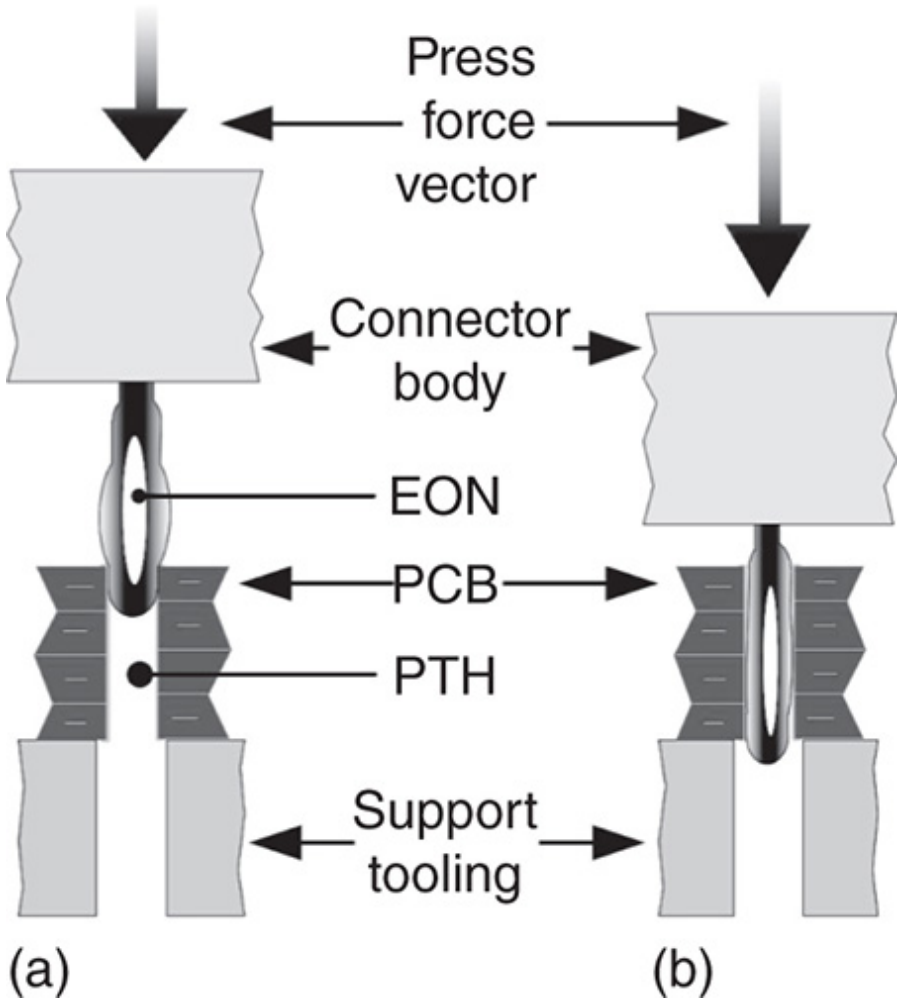


FIGURE 51.6 EON-type pin pressed into a PTH barrel. (*a*) Onset of the press cycle, (*b*) EON pin fully driven into the PTH barrel. Its compliant section collapsed inward upon itself. The resultant forces between the pin and the PTH barrel wall result in stable, intimate mechanical and electrical contact.

As a result of the pressing, the compliant pin deforms the plated through-hole barrel slightly due to mechanical interference of the press-fit pin against it. The resultant forces from the collapsed press-fit pin against the PTH barrel wall result in stable, long-term mechanical and electrical contact.

51.4 PRESS-FIT CONSIDERATIONS

51.4.1 Seating Force

The load necessary to apply a press-fit connector depends on a variety of factors, including pin design, pin material, pin size, pin surface finish (plating), PTH surface finish, PTH plating thickness, PTH finished hole size, and the number of pins per connector. The connector manufacturer should provide the required per-pin loading force for each connector and the force needed for proper insertion and connector seating.

51.4.2 Correct Design and Size

Press-fit connector leads are designed to work within a tight range of PTH barrel diameters. The compliant pin normal force exerted against the PCB plated through-hole barrel wall must be maximized to anchor the connector into the PCB reliably both for mechanical stability and electrical contact. The connector manufacturers will recommend proper PTH diameter, mechanical tolerances and PTH surface finish as tested for their product. The resultant press-fit coupling is analogous to the solder joint providing both electrical and mechanical functions.

If the pin and barrel are sized properly and materials are appropriately finished, the anticipated joint life will be better than that of soldered assemblies. Also if the pin and barrel are sized correctly, the pin-to-barrel normal force will be high enough to form a gas-tight seal for long-term electrical and environmental contact reliability. The pin must be strong enough longitudinally to prevent buckling during the pressing operation. Pin normal forces must be optimized so as not to damage the PTH barrel; high enough for good contact, but light enough that the pin insertion will not damage or eject the barrel or the PCB during the press-fit operation.

51.4.3 Reproducible Connector Press

Pressing force generally ranges from some tens of grams to kilograms per lead. The machine used for applying press-fit connectors must be range-appropriate and reproducible in operation. Manual presses or presses that impart significant variation in press speed and press force may lead to excessive process variation and less than satisfactory process results. Press attributes will be discussed subsequently.

51.5 PRESS-FIT PIN MATERIALS

51.5.1 Base Material

For purposes of affordability, mechanical integrity, electrical properties, and materials conservation, all electrical contacts, regardless of assembly methodology, are made from inexpensive base metals and plated with a minimum thickness of a more precious or more practical material. Many press-fit connectors were made of beryllium-copper alloy, but due to beryllium dust toxicity, a factor in press-fit lead manufacture, the switch to safer phosphor-bronze or other copper alloys has occurred throughout the industry.

51.5.2 Surface Finishes: Pin and Barrel

Press-fit connector compliant pins surfaces can be plated with a variety of metals with the two most common being gold and tin but other surface finishes are offered also. All circuit board surface finishes are suitable for press-fit

application, although some are more favorable than others. This will be discussed later in this chapter. “Organic solderability preservative” (OSP) copper, tin, gold, silver, tin-lead PCB surface finishes are all acceptable.

With soldering there is reliance on a fluxing agent to remove naturally occurring oxides from the surfaces to be joined prior to and during the solder alloying process. In a solder joint, the component lead and pad interface materials are wetted by and sealed in solder. Solder gives the interconnection mechanical rigidity and protects contact surfaces from degradation due to the environment (oxidation, corrosion, etc.). This is not the case with press-fit technology. Even though oxide may be present on the press-fit pin and PTH barrel (as would be the case of tin-plated pins and tin-plated PCB), the high frictional forces encountered during the press-fit process displaces oxides from both the compliant pin and the PTH barrel in the path of pressing, so generally there is little concern for oxidation on either part.

51.5.3 The Gas-Tight Seal

In the case of the press-fit connector pin, there is neither a physical wetting of materials nor metallic encapsulation to protect the interconnection as there is in soldering. Additionally, no chemical fluxing agents are used to remove native oxides from the PTH barrel or the compliant (press-fit) pin. Instead, the press-fit pin is anchored solely by the mechanical interference between connector lead and the PTH barrel of the PCB. Oxides on the surface of the press-fit pin and mating PTH barrel are broken loose by the high frictional forces associated with this type of assembly, so nobility of materials, oxide build-ups, and material shelf-life are less critical considerations than in soldering. If conditions are proper in terms of sizing and materials, the press-fit process results in a gas-tight contact between the connector

pin and the PTH barrel wall. Gas-tight is one of the most important concepts to understand in the press-fit connection.

The notion of a gas-tight seal as the product of a proper press-fit is crucial to connection reliability. If an electrical contact is to be reliable, the interface between the two mating surfaces must remain chemically and mechanically stable. The gas-tight, smeared, metal-to-metal contact attained during the press-fit operation mitigates oxidation of either contact (PTH barrel or press-fit pin) and prevents ingress of any atmospheric gaseous contaminants. Mechanisms such as fretting corrosion, a common failure mechanism for mechanically mated contacts, especially those subjected to vibration, is not a factor in a proper press-fit contact system. Press-fit interconnection is considered at least as reliable as a soldered connection and there is no solder joint to degrade or crack with time. Press-fit pins are designed and sized to result in long-term electrical and mechanical stability. Pin compression and resultant normal force are designed for a small range of PTH barrel diameters to achieve the long lasting press-fit gas-tight contact. The gas-tight seal prevents atmospheric gases (oxygen, gaseous contaminants such as sulfur, chlorine and water vapor) from contacting the freshly scraped surfaces that comprise the interconnection; a product of the press-fit process. If, for instance, a PTH barrel is sized too large for a given press-fit pin, the gas-tight seal may not form and the interconnection will not be reliable in the long term. If a PTH barrel is undersized, it may cause the press-fit pin to either crush beneath the connector or buckle in such a way that a gas-tight seal is not achieved. Care in reviewing specifications and inspection to ensure compliance to same is critical for the press-fit process.

51.6 SURFACE FINISHES AND EFFECTS

Surface finish of the PCB's plated through-holes has a significant effect on the force required to seat a press-fit connector and can have an effect on press-fit connection reliability.

51.6.1 Tribology

Every material has frictional (tribologic) properties. Some are naturally lubricating, such as lead (Pb) and its alloys and gold. Others are notably nonslippery, such as tin or copper. Copper is one of the least slippery of the surface finishes and in the context of press-fit, it typically requires more pressing force than Sn-Pb or gold surface finishes for a comparably sized hole. Tin's crystalline structure is also resistant to sliding. Regardless of surface finish chosen, the board shop should be alerted to the fact that holes are being placed in the board for press-fit connections, so more attention is paid to finished hole size (FHS), hole profile and surface finish conditions. For less slippery materials (Sn, Cu, etc.), the holes could be specified for the upper end of its FHS as expressed by the connector vendor to aid insertion and proper compliant section collapse.

If frictional forces are too great during press-fitting, then

- The PTH barrel can be pushed out of the board or otherwise damaged.
- Press-fit pins can buckle beneath the connector never making it into their respective through-holes.
- If they make it into their through-holes, pins may distort to the point that proper normal force is not adequate for a gas-tight seal.

- Contacts within the connector’s molded housing may be impacted imparting a change to the contact gap or even pushing the contacts out of alignment or out of the housing.

Trial boards and pressing parameters should always be assessed before full manufacturing commences. Only very small changes or imperfections can interfere with the typically high yields of press-fit connections. The process is dependent on having all material conditions right for pressing as well as having the proper process parameters too.

51.6.2 PTH Barrel Finish

Barrel finish can have a profound impact on the press-fit operation. If a PTH barrel is too thin or poorly sized for the compliant pin, the pin may pierce the barrel wall or break internal connections to it. OSP-copper finish—since it is a thin, watery, topical coating—adds no appreciable thickness to the PTH lands or barrel, so its control in high-aspect-ratio holes is not an issue in terms of press-fitting. Nonetheless, the copper thickness comprising the PTH barrel must be relatively uniform the entire length of the barrel. Electroless/immersion surface finishes are generally thin and self-limiting in thickness, and as with OSP-copper, such platings add no significant change in PTH hole diameter and no impact to the press-fit process other than the tribology issue already discussed.

At the other end of the spectrum are hot-air solder leveling (HASL) and electroplated finishes, which may add substantial material thickness to PTH barrel walls and annular rings. Too thick a HASL coating can result in PTH barrel diameter reduction. At the onset of the press cycle, compliant pin sections may be overcompressed, causing them to yield and

collapse beneath the connector rather than slide down their respective through-holes. Sometimes solder from the HASL surface finish can redistribute during SMT reflow cycles, causing a bulging meniscus within the PTH (Fig. 51.7*a*). This too may result in pin collapse or buckling. Compare this illustration to that in Fig. 51.7*b*, which shows a normally finished PTH with a relatively uniform barrel diameter, and an evenly coated primary-side annular ring.

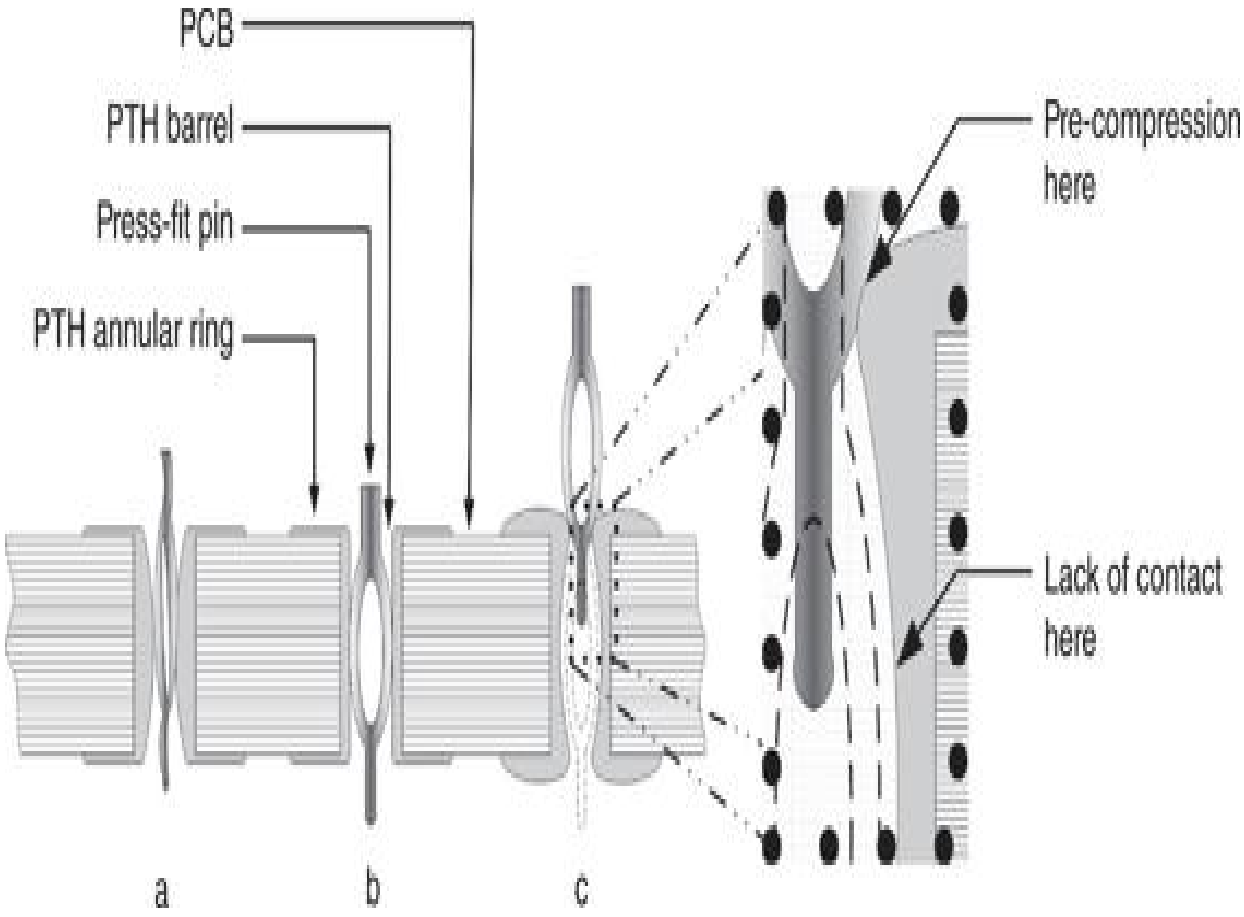


FIGURE 51.7 Barrel profile as a result of surface finish coating: (*a*) PTH barrel with excess surface finish from HASL, which formed a meniscus upon solder reflow within the PTH barrel. This resulted in crushed or distorted press-fit pin. (*b*) Normal PTH barrel with evenly coated walls and annular rings and a proper press-fit connection. (*c*) Excessive plating at top of barrel caused precompression of the EON pin. When the pin was fully inserted there was either insufficient normal force of the pin against the PTH barrel or no contact as shown in the magnified view (fully inserted pin shown in phantom). Both "*a*" and "*c*" pose reliability risks.

Figure 51.7*c* depicts the consequence of too much plating or solder deposit on the top-side annular ring. In this diagram, the compliant “eye-of-needle” is precompressed to the point of excessive plastic deformation of the pin. Once past the bottleneck at the top of the PTH it cannot make proper contact to the PTH barrel for reliable contact. Initially if electrical connection is detected, it may only be an asperity contact with either not enough conduction path for the application or it may be at risk for fretting corrosion in the long term due to lack of proper normal force of the pin to the barrel. With the advent of EU RoHS legislation limiting Pb use, HASL finishes for PCBs are less common, but press-fit may be needed for some exempted applications where Sn-Pb solder is still in use or when Pb-free HASL is chosen as a PCB surface finish. Excessive plating or deposits on PTH barrel walls and annular pads will register as excessive pressure during the press-fit process; another reason why precise equipment is needed for pressing as opposed to a manual machine such as an arbor press. Equipment will be discussed subsequently.

High-aspect-ratio holes (PCB thickness:PTH diameter) may have irregular plating where the thickness closest to the board’s outer layers is within acceptable thickness limits, whereas plating thickness in the middle of the PTH may be abnormally thin. These thin deposits are caused by plating bath stagnation and exhaustion—a zone of poor electrolyte circulation within the high-aspect-ratio PTH barrel. This condition may also lead to poor contact of the press-fit pin against the PTH barrel wall and contact reliability issues. The opposite can be detrimental also, where the PCB vendor strives to attain the proper plating thickness within the PTH barrel, but plates too much material at the barrel openings and on annular rings leading to the condition shown in Figures 51.7*c* and 51.8.

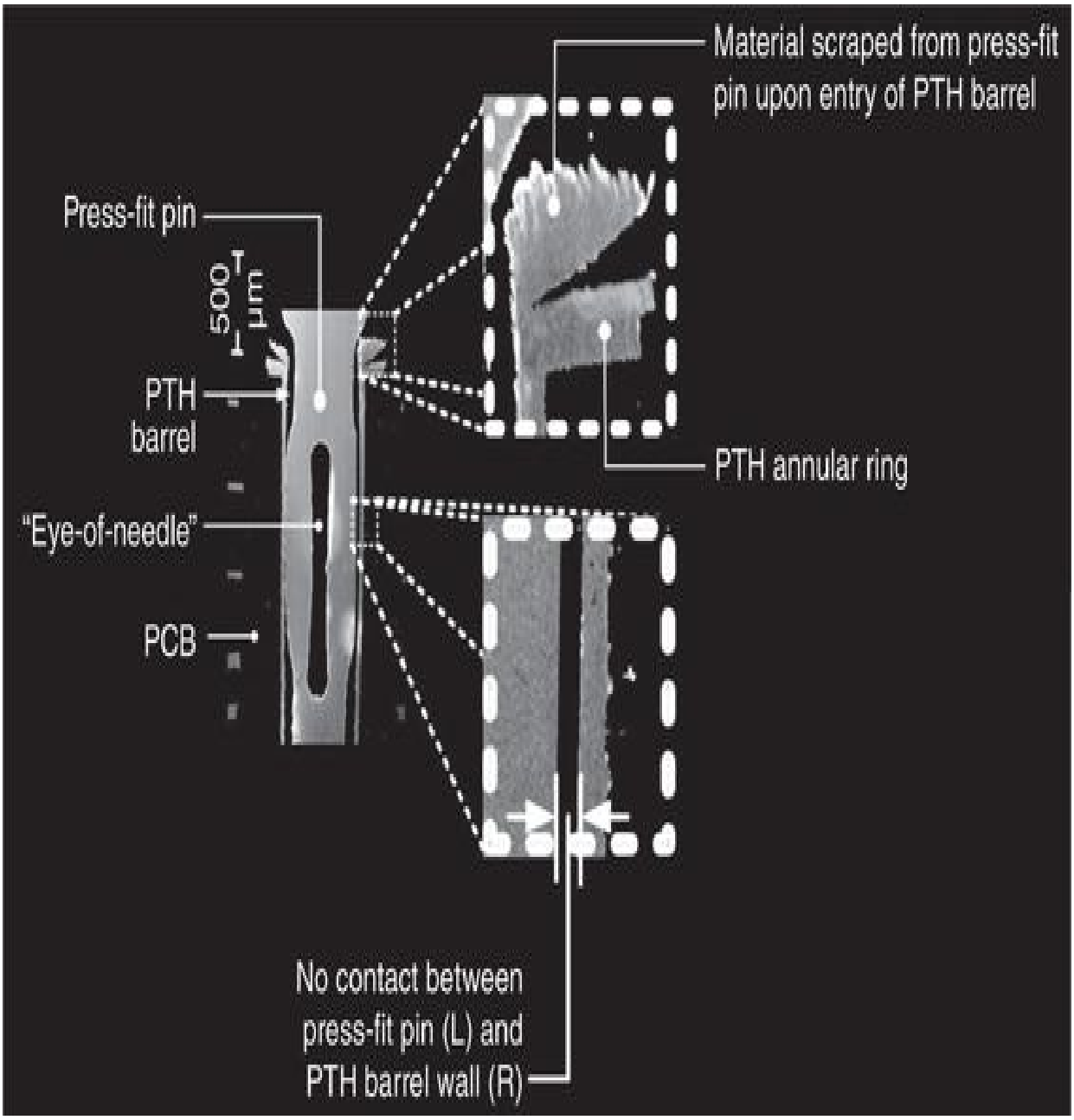


FIGURE 51.8 Excessive nickel plate on the PTH annular ring and at the PTH barrel entrance has caused an undersized finished hole at the top of the barrel. This has triggered three problems: (1) at the onset of the pressing process, the tight fit shaved the press-fit pin resulting in a metal mass that could become a shorting hazard were it to break free (top inset). (2) Forces were so great that it deformed the barrel and lifted the PTH annular ring slightly off the PCB surface (top inset). (3) It has overcompressed the EON section of the pin at the top of the barrel and there is a gap between the pin and the PTH barrel (bottom inset). (*Scanning electron microscope (SEM) micrographs courtesy of A. Alexander, Jabil Circuits, Penang, Malaysia*.)

51.6.3 Slivers

The Pb of Sn-Pb solder-coated barrels is known to reduce the force required for press-fit connector insertion and seating. Although Sn-Pb coating is one of the best surface finishes for pressing, if it is thick, then the press-fit connector pin may skive a thin sliver of solder and push it out the secondary side of the PCB (Fig. 51.9).

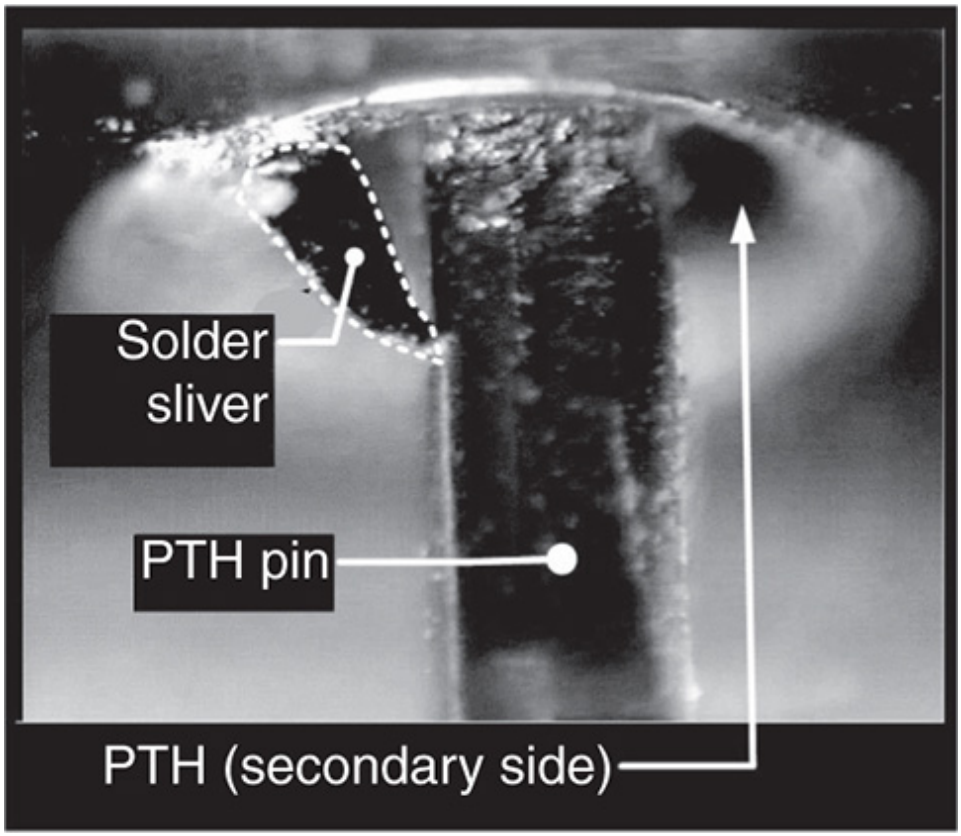


FIGURE 51.9 Micrograph showing a solder sliver on the bottom-side of a PCB. The sliver, if broken off may pose a shorting hazard to the PCA or to the system into which the PCA is installed.

Very often these slivers remain attached to the pin or the PCB, or they become jammed between the pin and barrel. The sliver may break free of its source and cause an electrical short locally or elsewhere in the system. Inspect for slivers after press-fitting especially with a new process, a new lot of PCBs, a new lot of connectors or when using the

same connector style from a different connector manufacturer.

51.7 EQUIPMENT

Several types of mechanical presses are used for applying press-fit connectors to PCBs. The lever-activated arbor press is the most primitive but may suffice for simple, low-lead-count, coarse-pitch connectors, although this is not recommended. One step up is the pneumatically driven press. Although it is easier to operate than the lever-activated arbor press, it does little for process control or assembly repeatability. Higher on the evolutionary scale is the pneumatic/hydraulic combination (the so-called “air-over-oil” press), which offers a somewhat more controllable process.

High-precision pressing cycles are mandated by the latest press-pin connectors with their delicate, molded body features, fragile electrical shielding, and fine pin pitch, so it is advisable to use a machine that is computer-controlled. Aside from force and speed precision for process reproducibility, the latest machines have data loggers that can store press cycle data; an invaluable tool for statistical process control and useful for press cycle root-cause defect analysis or machine troubleshooting. Computer-based machines store process recipes for ram force, speed of compression, ram position and component location if the machine has programmable axes for moving the PCA beneath the ram. The state-of-the-art connector press is electromechanically actuated, relying on a motor-driven lead screw with tachometer speed control, *z*-axis positional encoders, and load cell feedback for an accurate pressing cycle and excellent process repeatability (see Fig. 51.10).

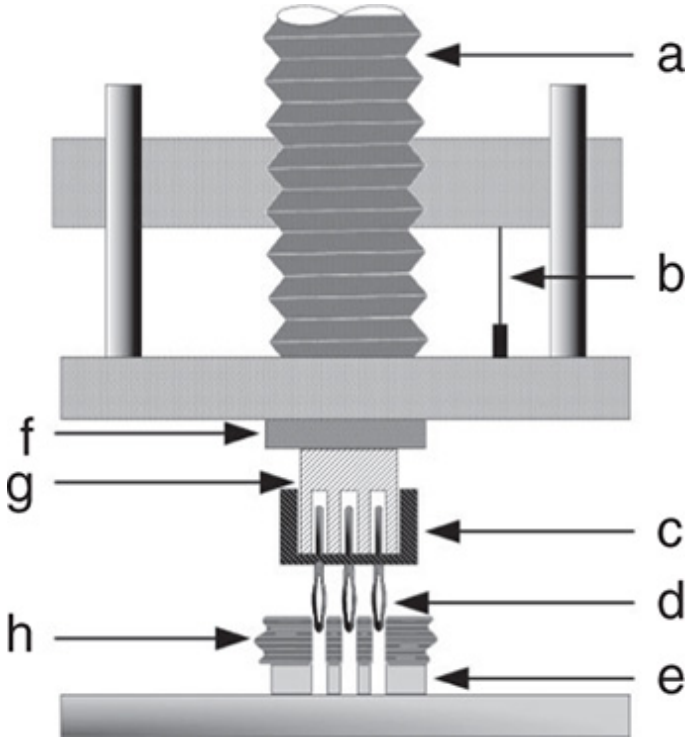


FIGURE 51.10 Schematic of electro- mechanical press used for press-fitting: (*a*) motor-driven ram screw, (*b*) z-axis encoder, (*c*) press-fit connector, (*d*) press-fit connector's compliant pins, (*e*) support tooling, (*f*) pressure transducer, (*g*) connector-specific pressing tool, and (*h*) PCB with plated through-holes.

Some commercially available machines are automated even to the point that they are able to shuttle boards into the press, pick and place connectors, select a connector-appropriate pressing tool and supporting tool anvil, rotate the tools to the proper orientation, and press multiple connectors sequentially on a single board or multiple nested boards. There are several ways to control the press-fit process. Methods and merits of each are discussed in the remainder of this chapter, but first a more detailed review of the mechanics of the press-fit process is in order.

51.8 ASSEMBLY PROCESS

Press tool and support plate are fabricated to match connector requirements and PCA layout. The PCB is placed on the press-fit tooling fixture support plate. The support plate is PCA-specific. It has tooling pins or a nesting feature to locate and immobilize the PCB during the process and has clearances to accommodate any soldered bottom-side components. The operator manually places the connector into the appropriate plated through-holes in the PCB. The ram and tool are aligned manually or automatically to the connector to be pressed. When press-fit connector leads are forced into PCB plated through-holes during a pressing cycle there is a characteristic fingerprint of force versus vertical distance traveled for each connector and PCB type. The various events and slopes that comprise the fingerprint are depicted in Fig. 51.11.

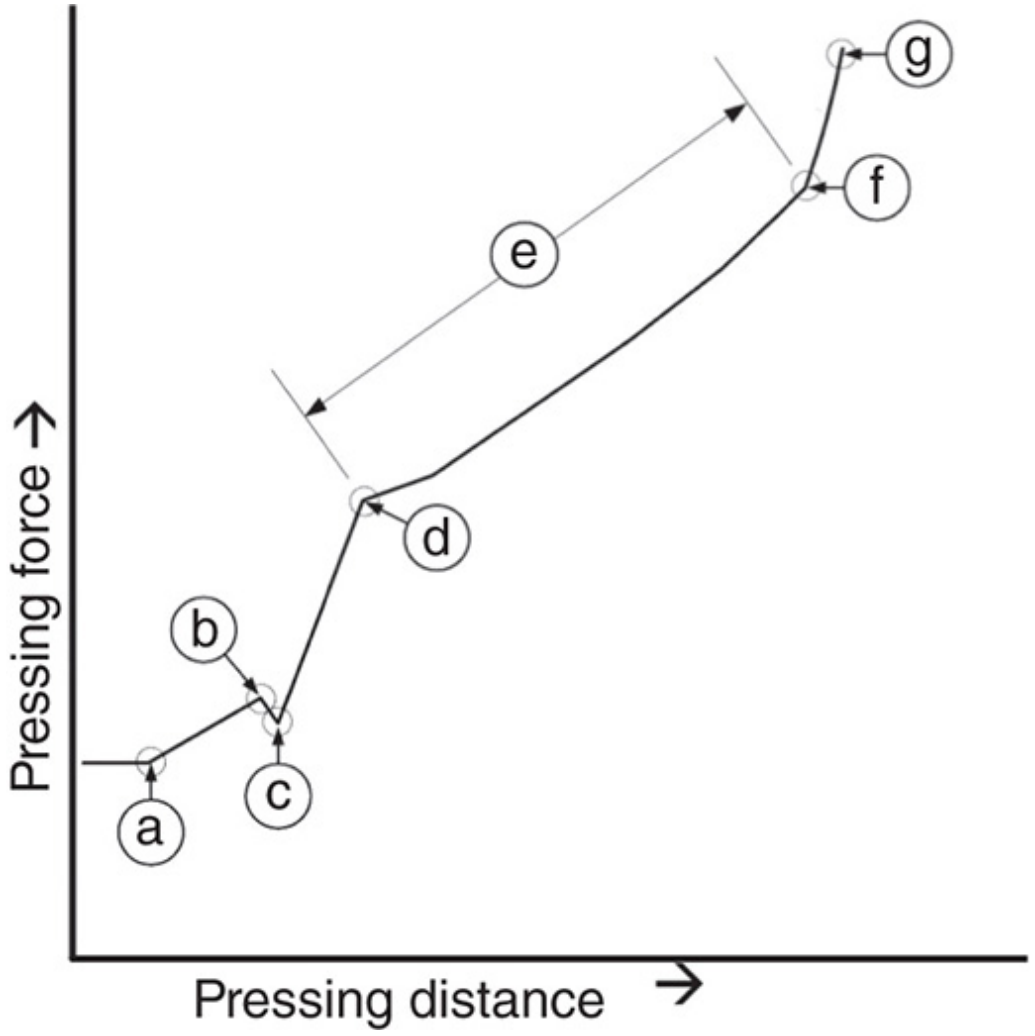


FIGURE 51.11 Force versus distance plot of a press-fit cycle. Inflection points and regions are as follows: (*a*) initial force applied to the press-fit connector and resistance is registered; (*b*) compliant section of pin starts to collapse; (*c*) further pin collapse allows pin to slide into the PTH barrel; (*d*) the pin continues to travel within the barrel resulting in increasing friction (region “e”); (*f*) connector fully seated; and (*g*) continued pressing makes little change in press distance signaling the end of the pressing cycle.

As pressing progresses, connector leads are forced into the plated through-holes and the compliant sections of its pins deform elastically, then plastically to some degree. Although there is plastic deformation, the pins and holes are sized so there is still elastic force present normal to the PTH barrel wall; enough to impart and maintain a gas-tight seal. Continued resistance is encountered due to the friction of the collapsed pins sliding along the PTH barrel walls. A final

inflection in the force/distance plot occurs when the connector housing is fully seated against the top surface of the PCB. Further force affects little or no change in vertical distance and the press cycle is ceased. Were the cycle to continue much after this final inflection, damage to the PCB or to the connector housing would result.

51.8.1 Press Routines

For best results, a method that allows real-time measurement and control of the pressing process is preferred and is available on today's commercial presses. There are four commonly used pressing routines, but only three take advantage of force-sensing, distance-sensing, or real-time feedback control of the modern connector press. Connector complexity and equipment availability dictate press-fit assembly methodology.

51.8.1.1 Uncontrolled Pressing. This was the most prevalent technique for a long time, but it rapidly lost ground to more sophisticated pressing methods, as described later in this section. It commonly relies on an arbor press and human muscle to force the press-fit connector into the PCB. There is neither force sensing nor speed control. It is the least reliable way to press connectors into PCBs and is not recommended for complex connectors or fragile boards. If too high a ram speed is used on a delicate connector, its pins may buckle. Also, this method may not provide enough force for some high-lead count connectors.

Although this type of pressing is discouraged, it may be adequate for low lead-count, coarse-pitch connectors in noncritical assemblies. As with any press routine, a suitable support fixture must be used beneath the board to keep the assembly from breaking or flexing. It should incorporate support to counter the forces of the ram, and relieved areas

to accept protrusion of press-pins below the bottom-side of the board and clearances for secondary-side components as shown in Fig. 51.12.

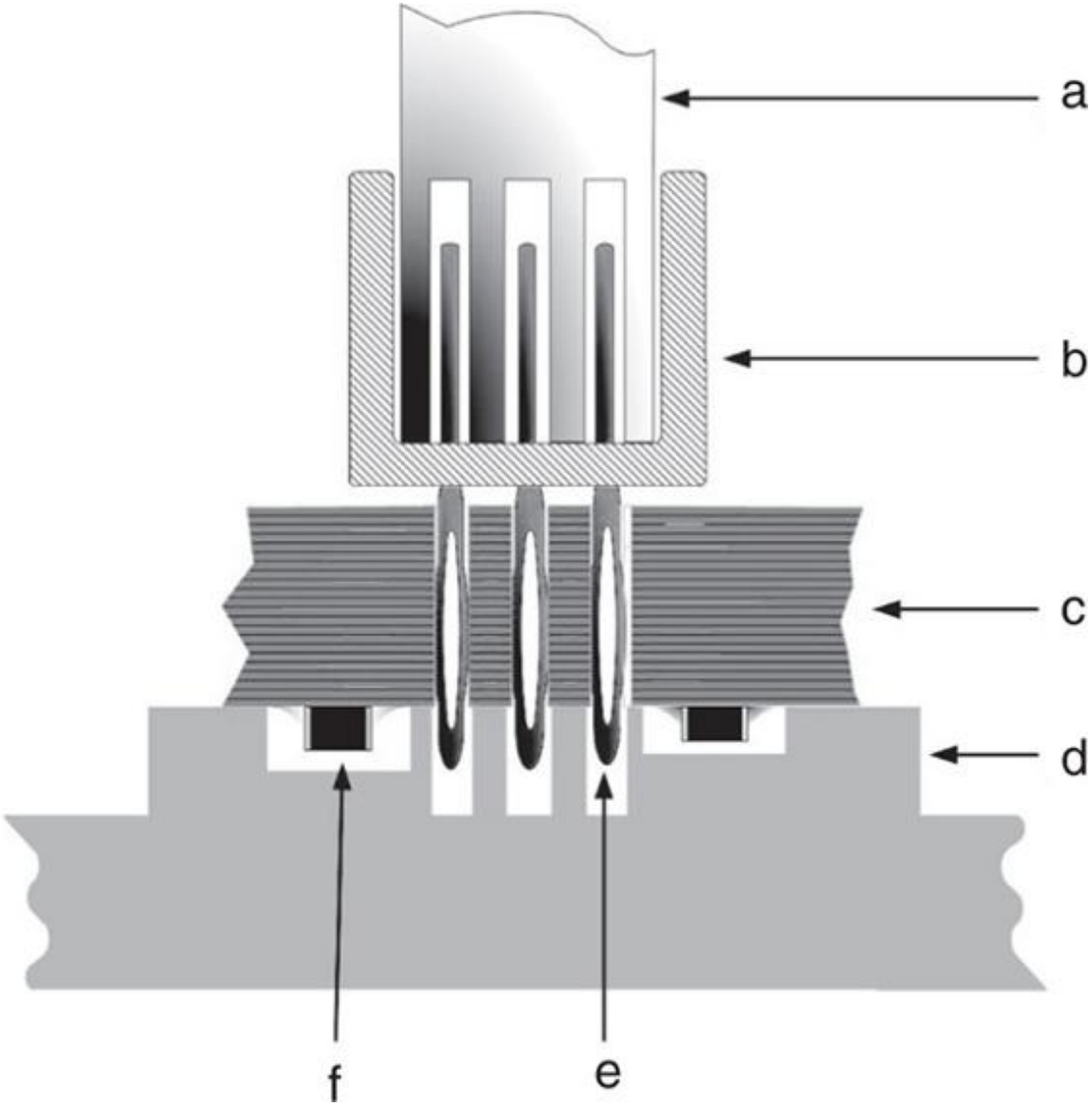


FIGURE 51.12 A rigid and properly designed support fixture is critical for a good press-fit process: (*a*) connector-specific pressing tool, (*b*) press-fit connector, (*c*) PCB, (*d*) support plate, (*e*) clearance in support plate to accommodate and clear press-fit pin tails, and (*f*) routed pocket in support plate to clear soldered bottom-side components.

51.8.1.2 Height-Limited Pressing. As previously described, connector presses have matured into

sophisticated machinery; improved greatly over the arbor press. Some are capable of precisely determining ram height above a datum such as the top surface of the PCB. If board-to-board thickness is consistent, then the connector can be forced into the board to a predetermined standoff height as required by the connector specification. Just as connector pin dimensions vary from connector to connector, so do plated through-holes in the PCB. Pressing to a predetermined height (i.e., *press to height*) ensures that the connector will be seated the same way each time, regardless of the pin or hole condition and the resultant force required to seat the connector (Fig. 51.13). Variations in PCB thickness, variability in the molded cross-section of the press-fit connector body, or molding flash can result in imprecision and negate some of the benefits of this approach.

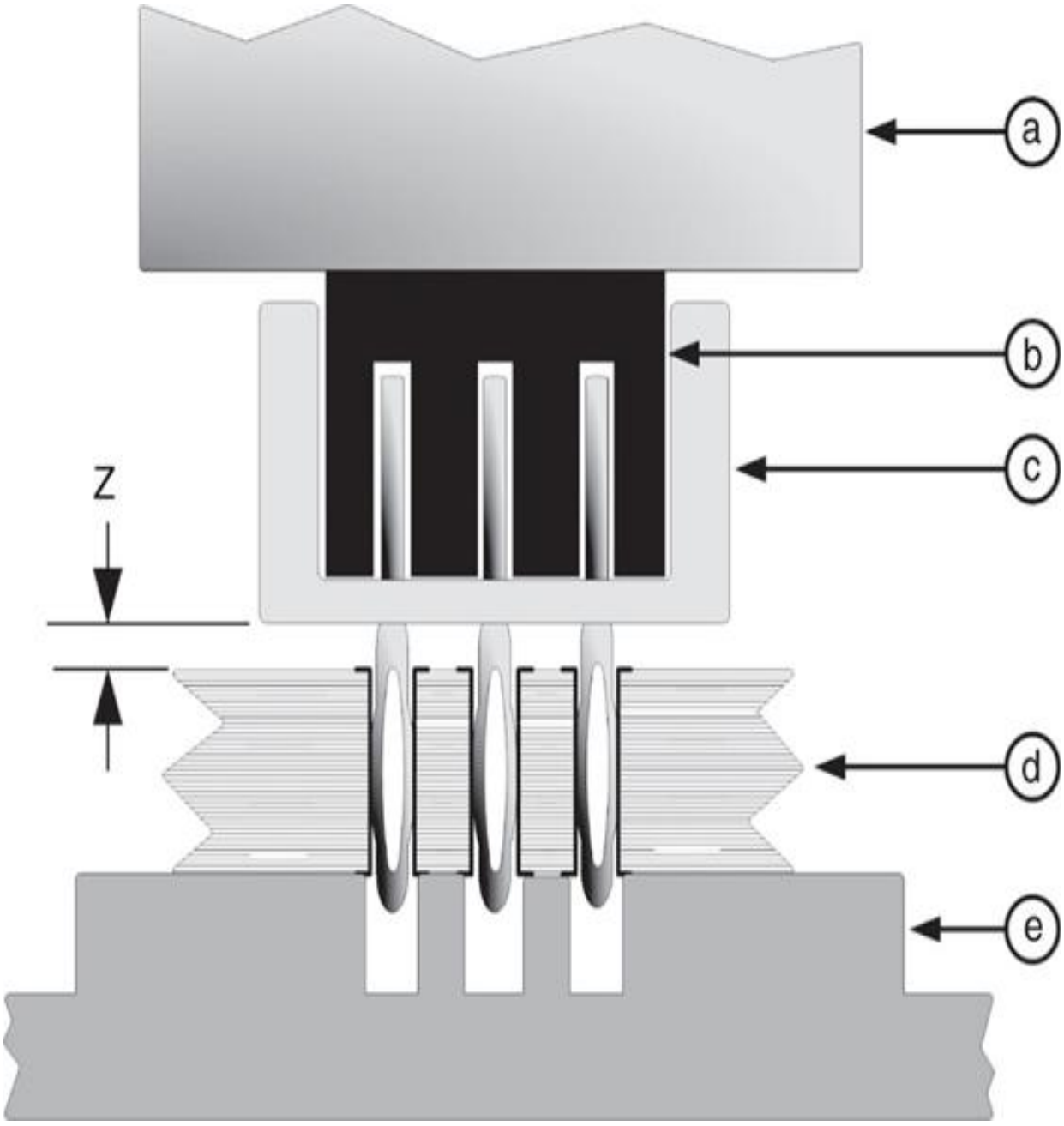


FIGURE 51.13 The “height-limited pressing” routine forces the connector to a predetermined standoff distance, “Z,” from the surface of the PCB. (*a*) Press machine ram, (*b*) connector-specific pressing tool, (*c*) press-fit connector, (*d*) PCB, (*e*) board-specific press-fit support plate (anvil).

51.8.1.3 Force-Limited Pressing. Force-limited pressing (or *press to force*) relies on the intelligence of an instrumented connector press to sense that a predetermined force limit has been reached, at which time the pressing

cycle is terminated. The force limit can be roughly set to coincide with the average force required per compliant pin (available from the press-fit connector manufacturer's specification) multiplied by the number of pins per connector. Application of upper and lower tolerances of specified force per pin coupled with knowledge from empirical trials will help refine the acceptable press force envelope for a given set of materials. This technique is highly sensitive to the material conditions of the compliant pins and the plated through-hole diameters.

51.8.1.4 Gradient-Limited Pressing. Also dependent on having an intelligent press machine, the slope or gradient of the final portion of the force-versus-distance plot (refer to Fig. 51.11 and the inflection labeled "f") can be used to trigger the end of the press cycle and retract the ram. This routine ensures that regardless of pin size, PTH condition, board or connector variations, the connector will not be over-pressed. This is most reliable when a very steep slope is chosen and refined empirically. Gradients in the range of ≥75 percent are generally favored. This routine is also known as *press to gradient*.

51.9 REWORK FOR PRESS-FIT CONNECTORS

The press-fit operation is inherently high yielding, but problems with the process or a bad press-fit connector or a crushed connector contact in the housing post-process may necessitate the removal and replacement of the failed connector. As a result of the press cycle, the compliant pins of a press-fit connector are plastically deformed. Therefore, once removed, the same connector cannot be reused. It must be scrapped. However, most press-fit connectors are

designed to be reworked—that is, removed or replaced. In some cases, individual leads or contacts can be replaced or banks of leads or contacts can be substituted. Most press-fit connectors require complete removal of the damaged connector for replacement with a new one. Many different press-fit connectors are on the market, and each has its own manufacturer-recommended repair strategy.

The through-hole in PCBs can generally accommodate two press-fit connector replacement cycles if sized properly in accordance with the press-fit connector manufacturer's specification. The two cycles are predicated on (1) the normal force exerted by the press-pin's compliant section on the PCB's plated through-hole barrel wall and (2) the quality and condition of the PCB's plated through-hole barrel surface after subsequent press-fit connector removals and replacements. Were the normal force of the compliant section on the PTH barrel of a press-pin excessive, it might cut through the barrel, damage surrounding inner layer interconnects or traces or push the PTH barrel out of the PCB. Instead, the press-fit connector normal force is optimized to permit gas-tight seal without excessive deformation or deep skiving of the barrel wall. Once a connector or connector pin is replaced, the new connector/pin must result in a gas-tight pin-to-barrel seal for reliable contact. Each time a new press-pin is inserted into a plated through-hole, there is opportunity for the barrel to deform; the more insertions into the barrel, the deeper the deformation. It is for that reason that the industry standard design goal for compliant-pin connectors is generally targeted at only two replacement cycles. Beyond two replacements, there is the possibility that the barrel will be thinned and damaged, impairing press-pin contact reliability or compromising PCB inner-layer trace-to-barrel interconnections.

Press-pin rework tools vary greatly. In some cases, they are designed to remove and replace a single pin. In other cases,

the tool may be designed to help dislodge an entire connector from a circuit board. In many cases, contacts are “bottom-loaded”; inserted into the bottom-side of the molded press-fit connector housing. For such connectors, the molded connector body (insulator) is pulled with pliers or a specialized tool, and then individual pins are pulled by pliers one by one in preparation for replacement. Sometimes multiple press-pin ground or power leads are stamped into discrete wafers, and then the wafers are inserted into the plastic molded connector body to form a single press-fit connector. In this case, individual wafers can sometimes be removed and replaced rather than having to replace single leads or the entire connector. Repair tools and repair strategies are generally available from the connector manufacturer.

A fixture can be constructed to facilitate removal of some types of connectors. A rigid board support is built to hold the PCB upside down with clearance machined into it to accommodate the failed part. A flat-rock tool (a piece of flat, hard metal stock) is positioned over the pins of the connector to be removed. The presses ram is slowly lowered onto the pin tails displacing them until they are flush with the bottom-side of the PCB. Although this does not remove the connector completely, very often it will push the compliant sections out of the PTH far enough out that it only takes a small force to remove the connector or the connector’s pins (Fig. 51.14).

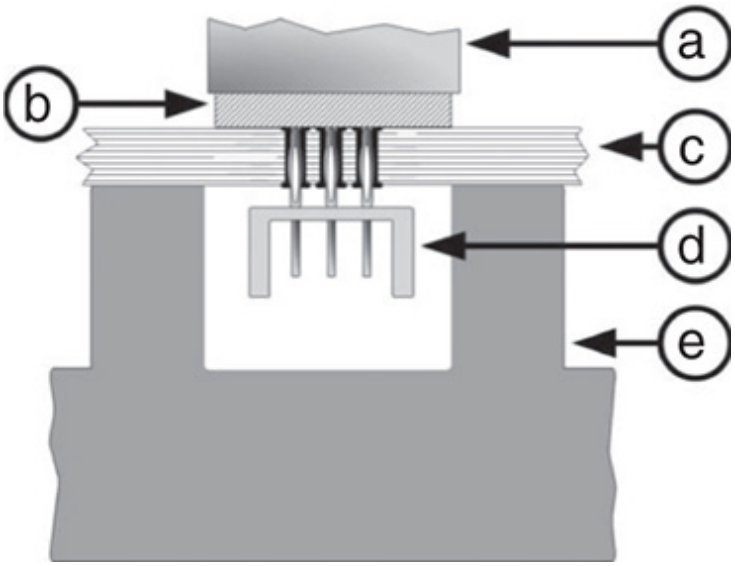


FIGURE 51.14 Pressing on connector pin tails will aid in removal of a failed press-fit connector. Pins can only be pressed flat to the PCB surface but this generally makes connector removal easier. Care must be exercised not to damage components or flex the PCB during component removal. (*a*) Press machine ram, (*b*) flat-rock tooling, (*c*) PCB, (*d*) failed press-fit connector, and (*e*) support tooling.

Removal of the connector or the pins is still relegated to a manual operation. Pliers or a special tool may be required for this.

Building a tool to fit inside the PTH barrel to completely remove pins is not recommended. There is danger of scraping the PTH barrel, pushing the barrel out of the PCB or damaging inner-layer interconnects to the PTH barrel wall if the tool is not sized properly, damaged or is even slightly out of alignment.

To avoid damage to the board, components, or solder joints during press-fit connector removal, the PCB must be supported so that it is not flexed. PCB flexure will break or crack solder joints and the damage will not be visually evident. It is a good practice to verify circuit integrity by electrical test before and after repair to ensure that it is not degraded as a consequence of the repair cycle. If a connector is replaced because of pin stubbing on the surface of the circuit board (Fig. 51.15), ensure that the surface and

underlying traces of the circuit board have not been damaged by an errant lead.

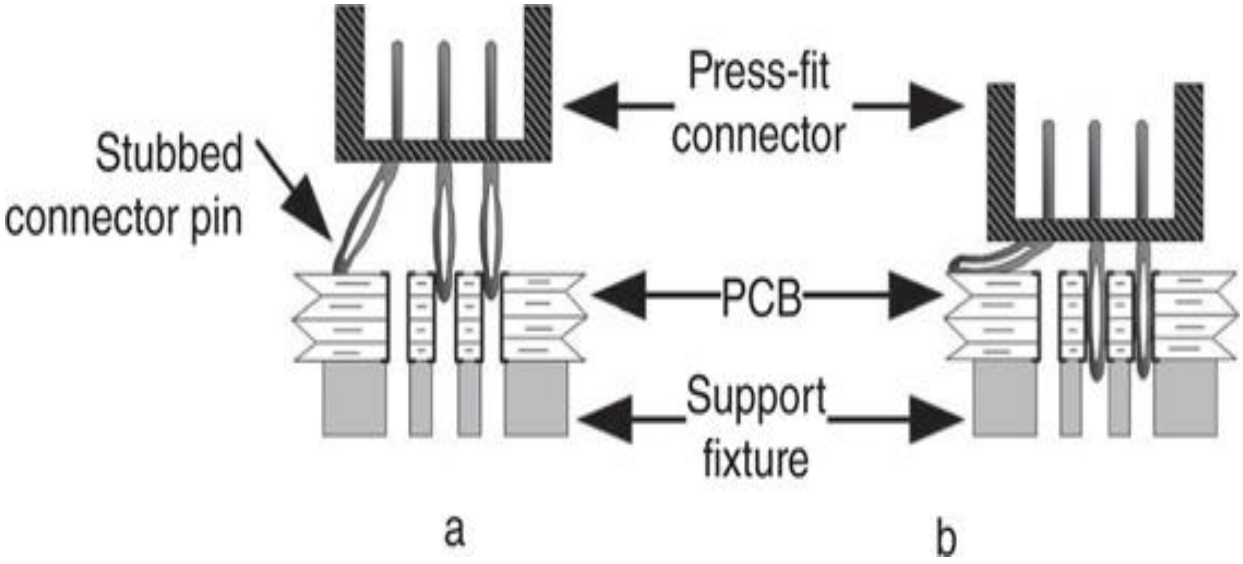


FIGURE 51.15 Stubbing: (*a*) misaligned pin impacting the surface of the PCB, and (*b*) stubbed pin folded under the connector as more seating force is applied by the press. Stubbing may damage surface or subsurface electrical circuitry.

Another defect occasionally seen at rework is surface damage caused by a leaning connector or by overpressing a connector into a board. Figure 51.16 depicts the leaning connector condition while the inset shows a micrograph of the damage to a subsurface trace.

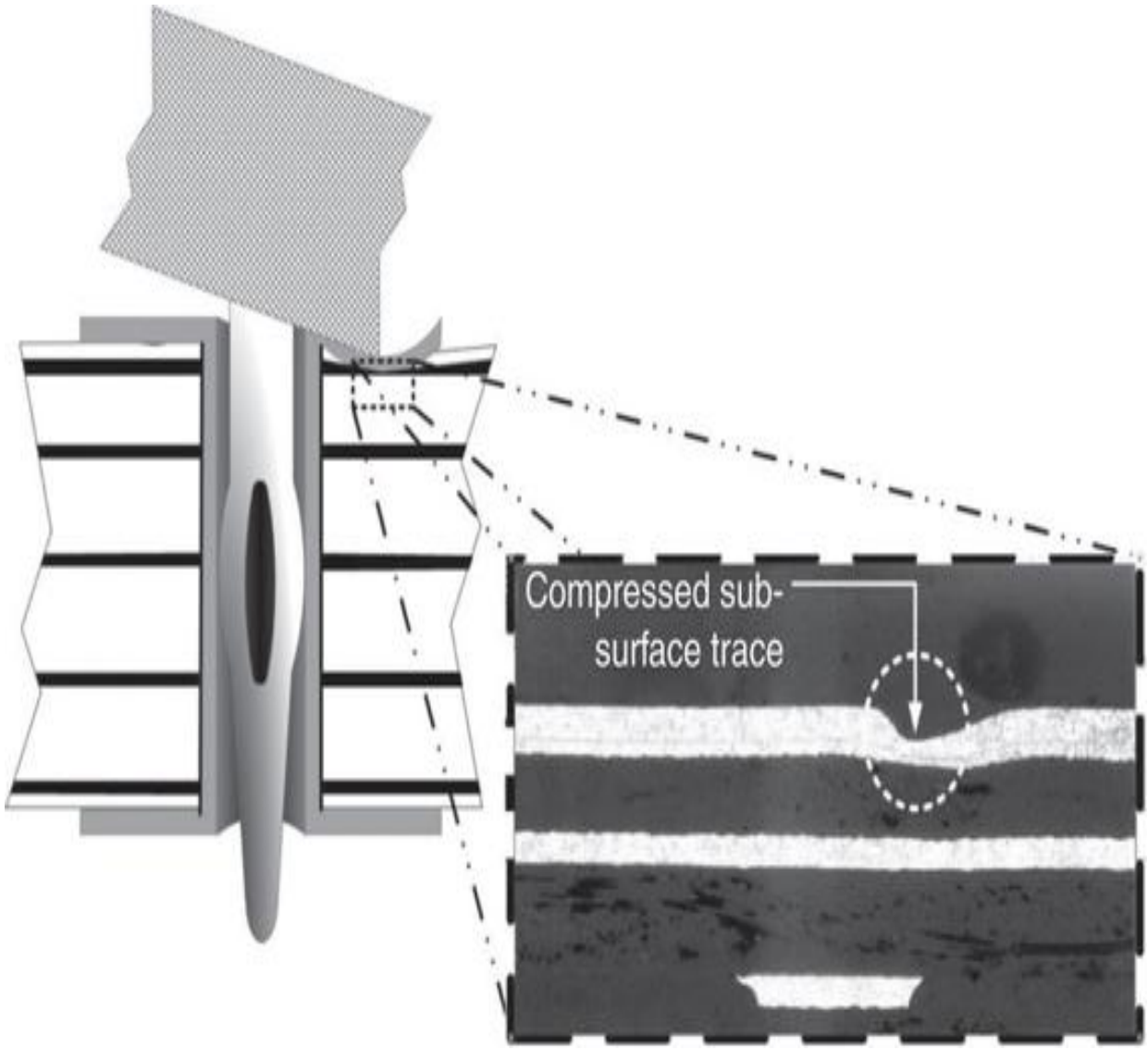


FIGURE 51.16 Canted connector during pressing caused sub-surface damage. The cross-sectional micrograph shows a copper trace below the PCB surface that was compressed to the point that it was no longer an appropriate conductor. In this case, circuit heating resulted due to the diminished cross-section of the trace and surrounding damage.

Compression of a conductor may sever it or thin it to the point that it can no longer conduct properly and excessive heating may ensue. While it is not practical to look for subsurface damage, there should be ample evidence of impact on the PCB surface.

51.10 PCB DESIGN AND BOARD PROCUREMENT TIPS

51.10.1 Clearance for Press-Fit Tools for Assembly

To avoid process problems and damage to adjacent components, there should be sufficient clearance in the board layout design to accommodate pressing tools and board supports.

51.10.2 Long Pins Preferred

When possible, use press-pin contacts slightly longer than the board thickness so that connector pins will protrude from the bottom-side of the board after the pressing cycle. Pin protrusion permits easy inspection of the finished assembly. A missing pin is evidence of pin stubbing, buckling or pin damage.

51.10.3 PTH Size and Surface Finish

Follow the press-fit connector manufacturer’s recommendation for PTH finished hole size, tolerances, and acceptable or tested surface finishes. Cross-section sample boards (mechanical scraps from board shop) to qualify the PCB vendor and determine typical PTH barrel profile. This is particularly important for PCBs with high-aspect-ratio (depth:diameter) holes. Ensure that wall thicknesses of plated through-holes are uniform through-out their depth and meet connector specifications. Make certain that the surface finish on the PTH annular ring does not interfere with

insertion of the compliant press-fit pin as may be the case with HASL or thick electroplate coatings.

51.10.4 Avoid Circuits Beneath Press-Fit Connector Stand-Offs

During press-fitting, molded connector housing stand-offs may crush any electrical traces or planes on or the near the surface of the PCB. Design in keep-out areas to avoid damaging circuit traces below.

51.10.5 Properly Space Connectors for Rework

Ensure that there is enough space between and around connectors to allow for rework. Devise the rework method before PCB lay-out so the designer can provide clearances in accordance with the rework strategy and requisite tooling.

51.11 PRESS-FIT PROCESS TIPS

51.11.1 Use a Proper Press

Use of an electromechanical press is recommended for best precision and process feedback. This will eliminate uncontrolled press cycles as from an arbor press. It will also improve the reproducibility of pressing as compared to using and “air-over-oil” type of pneumatic press.

51.11.2 Rely on Data Logging and Force Graphing

Today’s presses come with data logging options that enable statistical process control and diagnosis of press cycle failures. After pressing, examine the press-cycle force/distance graph to better understand the process. Set flags and warning on the press so that the operator is alerted when the process exceeds a process limit.

51.11.3 Check Connector Pins for Damage and Alignment

Prior to insertion into the board, visually inspect press-fit connector pins for straightness and integrity. An inexpensive go/no-go gauge (Fig. 51.17) can be machined to check that connector pins are in proper alignment. This is particularly advantageous for connectors that are complex, high lead-count, have delicate pins, of high value or are pressed into a high-value PCA. The gauge should be constructed so that it neither compresses the compliant section of the press-fit pin nor damages its surface coating. This is especially helpful for fine-pitch press-fit connectors (1 mm centers) and is better than relying solely on visual inspection for pin field integrity.

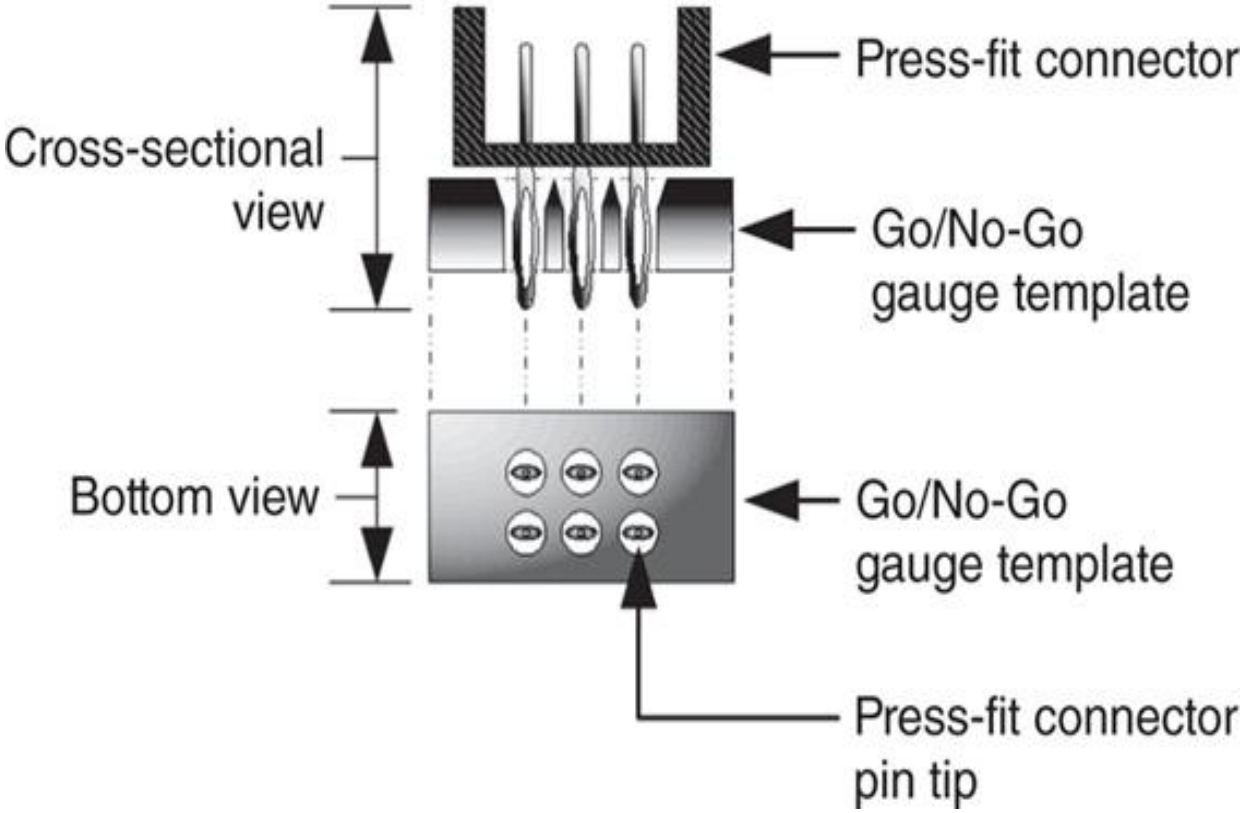


FIGURE 51.17 Gauge for checking connector pin positions prior to pressing. This is best used for high lead count, fine-pitch pin press-fit connectors. Clearance holes in the gauge should be just large enough to offer no mechanical interference when the connector is inserted. It should be made out of an ESD-safe material that will not cause any surface finish damage. If the connector slides in readily, it is an indication that pins are aligned and ready for the press-fit operation.

51.11.4 Keep the Press-Fit PTH Clear of Foreign Material

Protect press-fit PTH holes from extraneous solder, flux, surface-mount adhesive, spot mask, or other contaminants from surface-mount, wave-solder, or hand-solder processes. Use of a wave pallet or high-temperature masking tape (e.g., polyimide tape) to shield press-fit locations during other processing is advisable. If tape is used, inspect first articles to ensure that high-temperature masking tape residue does not foul press-fit holes. Polyimide tape with acrylic-based

adhesive is best for this application, as residues will be absent or minimal.

51.11.5 Use the Proper Press Tooling

Use hardened-steel pressing tools as sold or recommended by the connector manufacturer to avoid damage to the connector or the PCA. Aluminum tools wear out quickly and are easily damaged or deformed. Board supports can be made of aluminum.

51.11.6 Provide Proper Board Support

Adequately support the PCA during the pressing operation so that connectors can be fully homed and that the board is not overflexed. Excessive board flexure may cause solder-joint cracking, broken PCB circuit traces, and board delamination. This is especially important for the characteristically inflexible ball- or column-based solder joints of area-array devices such as BGAs and CCGAs.

The best support will be localized directly under the connector to be pressed. Ensure that the support includes clearance for backside pin protrusion; otherwise, pins will stub and bend on the supporting anvil. Support tooling design should carry appropriate relief features for bottom-side components and fixturing features such as tooling pins to accurately locate the PCA and hold it in position during the pressing process. Tooling pins should be kept as short as possible to facilitate removal of the PCA without inadvertent flexure. Tooling pins should have rounded (bullet) tops to enhance loading the PCA on the fixture and to avoid damage to the PCA due to sharp features as from a squarely cut pin.

51.11.7 Inspect Parts after Pressing

Set the press profile to match the connector manufacturer's instructions. After set up of the profile, press some sample parts to ensure that the pressing routine is not damaging the PCB surface, the connector or tooling. Do not overcompress.

Check the connector after pressing for even bottom-side pin protrusion, top-side connector body seating height, damage to the connector body or movement of contacts or electrical shields (if so equipped) within the connector.

51.11.8 Sliver Inspection

Check the bottom-side of the board for sliver formation (skived material from the pin or PTH barrel). If they are found, check PTH for finished hole size and uniformity of plating within it. Metallurgical cross-sectioning will be necessary for this inspection. Work with the board shop to ensure that drilled and plated holes are sized appropriately for the press-fit process and that excess material (HASL solder or plating) does not adversely alter the finished hole size or hole profile. Gauge the connector pins to ensure that they are within specifications also.

Loose slivers may cause electrical shorting on the board or other boards within the system enclosure. Brush any slivers with a soft, ESD-safe brush and use filtered, ionized air to blow-off the bottom-side of the PCA once silvers are removed.

51.11.9 Electrical Testing

In the case of high-friction surface finishes, such as OSP-copper or tin, forces applied during the press-fit process may be so great as to cause damage to the PTH barrel or adjacent

inner- or outer-layer circuit traces. Check the board visually and by electrical test (in-circuit and functionally) as part of a first article inspection.

51.11.10 Check Tooling Frequently

Check for excessive tool wear or damage. A damaged tool can ruin a connector or PCB and replicate the damage over many boards.

51.11.11 Soldering and Press-Fit Pins

Apply press-fit connectors after all SMT and wave-soldering operations. Do not try to solder press-pin connectors in place. Press-fit connector bodies may not be reflow-compatible. Soldering a press-fit connector will also make rework difficult or impossible.

51.12 FURTHER READING

Hilty, R. D., “Effect of Lead Elimination on Press-Fit Interconnects,” paper presented to the Institute of Electrical and Electronic Engineers (IEEE) HOLM Conference Lead Free Workshop, September 9, 2003.

Ocket, T., and Verhelst, E., “Lead-Free Manufacturing: Effects on Press-Fit Connections,” paper presented to the International Center for Electronic Commerce (ICEC) Proceedings, Zurich, September 2002.

Parenti, D., and Mitchell, J., “Validating Press-Fit Connector Installation,” *Circuits Assembly*, April 2003, pp. 26–29.

CHAPTER 52

PRESSURE-INTERCONNECT LAND GRID ARRAY SYSTEMS

Gary M. Freedman
Colab Engineering LLC, Stow, Massachusetts

52.1 INTRODUCTION

The solderless land grid array (LGA) device is a package that relies upon pressure contact to connect it mechanically and electrically to the printed circuit board (PCB). Interconnection is accomplished through a socket or interposer that is sandwiched between the LGA integrated circuit (IC) package and the PCB. The socket has compliant, conductive contacts that match LGA and PCB contact land patterns, all of which match each other in position and pitch. A system of insulators, stiffeners, and fasteners keeps the LGA in intimate mechanical and electrical contact with the PCB. Care in assembly and cleanliness are of utmost importance for successful interconnection and subsequent assembly reliability. The reader should be aware that there are leadless soldered packages also called land grid arrays, but this

chapter will deal with the pressure-interconnect variety of leadless package.

Most often, an LGA-type interconnect is used for mounting a central processor unit (CPU) chip or other active device to a PCB. It is also used for some connectors. An advantage of this type of interconnect is that it facilitates exchange of a chip or connector without the need to unsolder and re-solder it. This enables rapid rework or field upgrades without soldering and without degradation in reliability as may be the case for devices exposed to multiple soldering cycles. Although the technique has been in use for several years, it is still a niche technology but will likely increase in importance as input/output (I/O) counts continue to rise and package size limitations for soldering are encountered.

52.2 LGA AND THE ENVIRONMENT

Since the LGA connection to the PCB is solderless, it is environmentally friendly, requiring no unsoldering for rework. With no need for solder or other hazardous materials, such systems are generally compliant with the European Union’s (EU) Restriction of Hazardous Substances (RoHS) requirements and similar regulatory requirements around the world.

52.3 ELEMENTS OF THE LGA SYSTEM

There are five key essentials and several subelements that make the LGA system practical and reliable. A generic stack is pictured in Fig. 52.1. Key elements will be described in a generic sense in this chapter.

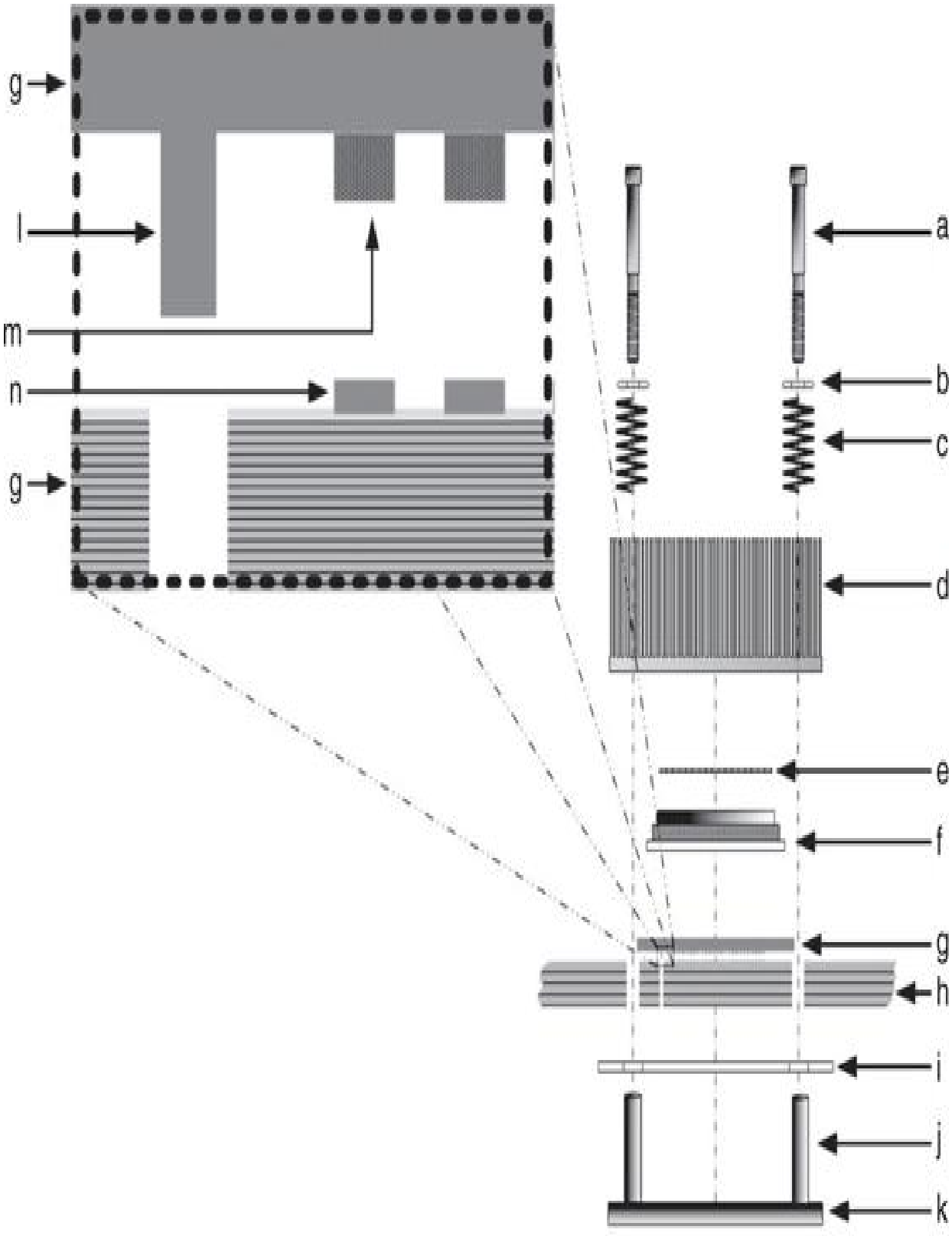


FIGURE 52.1 Exploded view of a typical pressure-interconnect system: (*a*) fastening screw, (*b*) washer, (*c*) compression spring, (*d*) pressure plate (in this

case a heat-sink), (*e*) thermal interface material, (*f*) IC package (LGA), (*g*) interposer (LGA socket), (*h*) PCB, (*i*) insulator, (*j*) bolster plate's threaded posts, (*k*) bolster plate, (*l*) socket alignment post, (*m*) compliant contact of interposer, and (*n*) plated PCB contact land.

52.3.1 PCB and LGA Issues

52.3.1.1 Contact Lands. The PCB is much like any other board and has surface lands to accommodate electrical interconnect of the LGA socket to it. The lands correspond in size and shape to socket requirements. Most often, the LGA lands on the PCB are electrolytic nickel covered by electrolytic gold. These pads are often plated with hardened gold for added contact durability and reliability. Other surface finishes can be used, but should be tested for reliable and long-lasting electrical contact.

52.3.1.2 Drilled Holes. LGA sockets have the requirement for two sets of drilled holes in the PCB. One set is used to accommodate fastening of the bolster plate through the PCB. The second set is used to orient and retain the socket on the PCB. The closely toleranced orientation holes correspond to molded locating posts on the LGA socket. These ensure alignment of the socket contacts to LGA lands on the PCB. The socket manufacturer will provide guidelines and drill pattern recommendations for the socket posts. Most often the LGA sockets come with two different sized posts. These polarize the socket so that it cannot be misapplied to the board.

52.3.1.3 PCB Layout Considerations. There are some layout considerations such as avoidance of components in the vicinity of the LGA socket, bolster plate, and pressure plate. Tall components under an overhanging heat-sink would also be problematic. PCB flatness should be considered so that best contact can be made to the board once the LGA interconnect system is fully assembled. Ensure

that test points will be accessible once the LGA stack is assembled.

52.3.2 Bolster Plate

The bolster plate is the rigid back-side element that serves to anchor the LGA system to the PCB. It is inserted through predrilled holes in the circuit board and provides the means for fastening the clamping mechanism that holds the LGA stack together. It is typically fashioned from a stiff metal such as stainless steel or thick aluminum (Fig. 52.2).

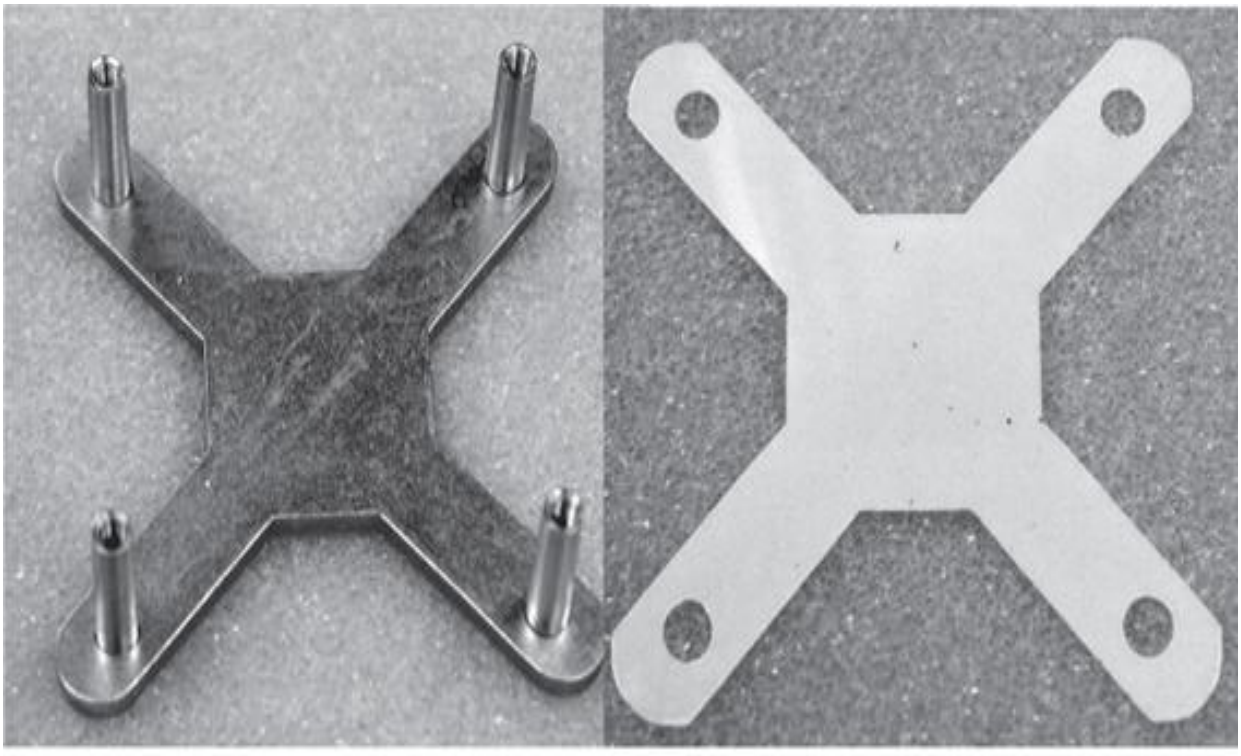


FIGURE 52.2 Stainless steel bolster plate with threaded posts (*a*) and insulator (*b*). (*Courtesy of Hewlett-Packard*.)

The bolster plate may be orthogonal or sculpted to accommodate components in the vicinity or to permit access

to test points for in-circuit testing (ICT) or diagnostics. It should be rigid and once fastened it must flatten out any local PCB bow or warpage in the vicinity of the LGA contact field. It has to impart mechanical stability to the assembled LGA stack to ensure consistent electrical contact over time and through various environmental conditions. Usually an ESD-safe insulator is applied over the surface of the bolster plate, positioned between it and the underside of the PCB. It prevents shorting of the metal bolster to any electrical features on the bottom-side of the PCB such as through-hole vias, test pads, etc.

Placement of electrical devices within the footprint of the bolster should be avoided. If components must be placed within its footprint, the bolster plate needs to be relieved to clear them, otherwise these components would be crushed during LGA assembly and they would also hinder the bolster plate from sitting flatly to the bottom of the PCB. If the bolster plate is relieved to accommodate bottom-side component clearances, it may require thickening so its rigidity is maintained in light of the removed material.

52.3.3 Active Component (LGA IC)

The LGA is an IC package usually made from a rigid substrate such as ceramic. It looks like a ceramic ball grid array (CBGA) without solder interconnects (balls) on its underside (Fig. 52.3). It typically has gold pads on its underside that serve as contact points for the LGA socket. In all other respects, it is like any other ceramic package. The contacts are usually electrolytic nickel over-plated with electrolytic gold. Often, a hardening agent such as cobalt is co-plated with the gold to enhance contact durability for improved long-term reliability.

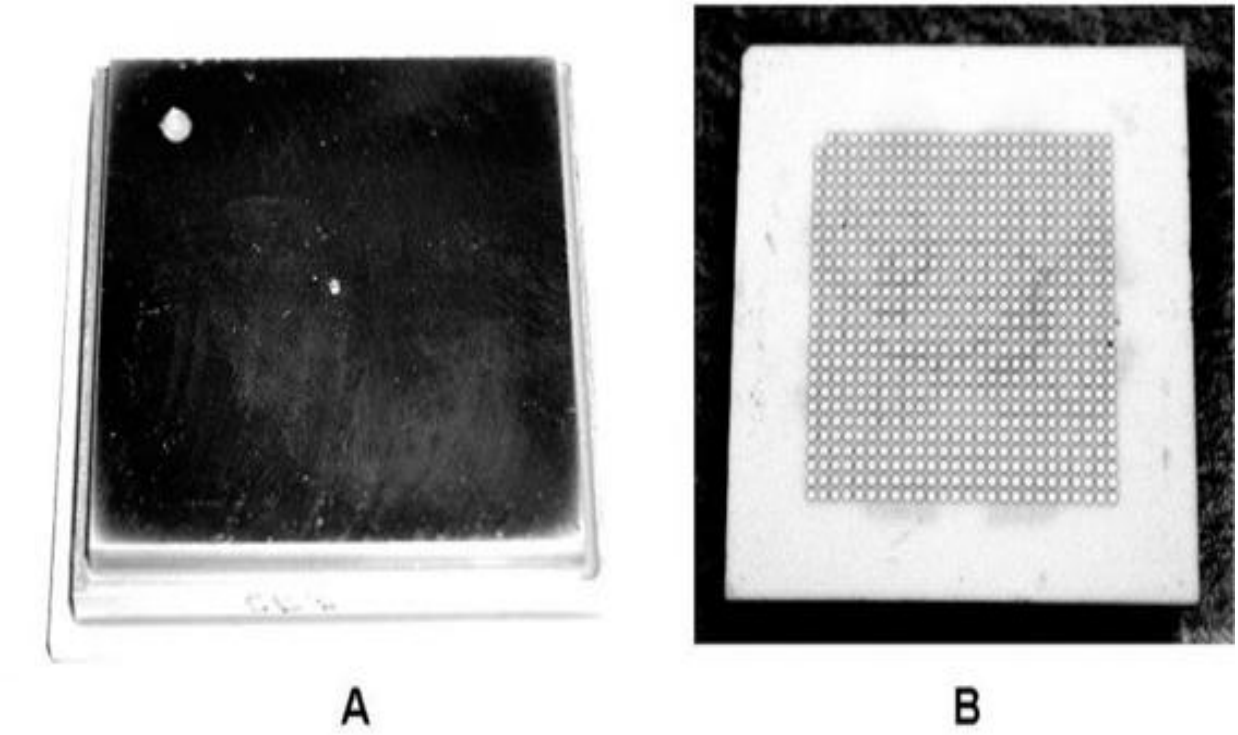


FIGURE 52.3 LGA IC package: (A) top-side of a ceramic LGA package, (B) bottom-side of same package with an array of gold contact. The package is similar to a CBGA without any solder balls. (*Courtesy of Hewlett-Packard*.)

52.3.4 Socket

Many types of LGA sockets (also referred to as *interposers*) are available. There are interposers with traditional dimpled leaf-spring contacts, “Fuzz-Button” contacts, and even metal-filled polymer connections. The contacts are held on a molded insulating substrate (Fig. 52.4). The contacts and socket frame are customized to fit the LGA package pattern and a corresponding footprint pattern on the PCB.

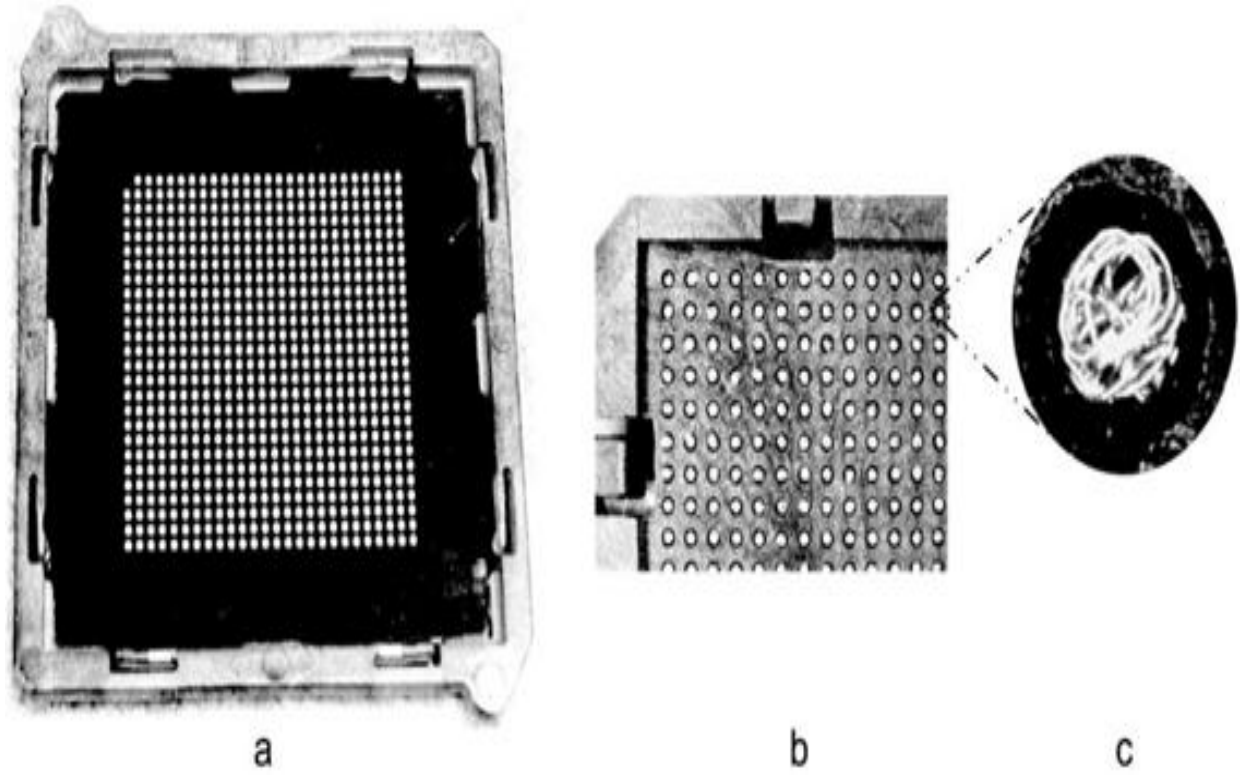


FIGURE 52.4 LGA socket: (*a*) a socket with metal-filled polymer contacts, (*b*) a socket with Fuzz-Button contacts, and (*c*) high-magnification view of a single wire-wound Fuzz-Button.

Each contact is interconnected through the molded substrate in some fashion so that one side connects to the IC and the other side to the PCB (Fig. 52.5).

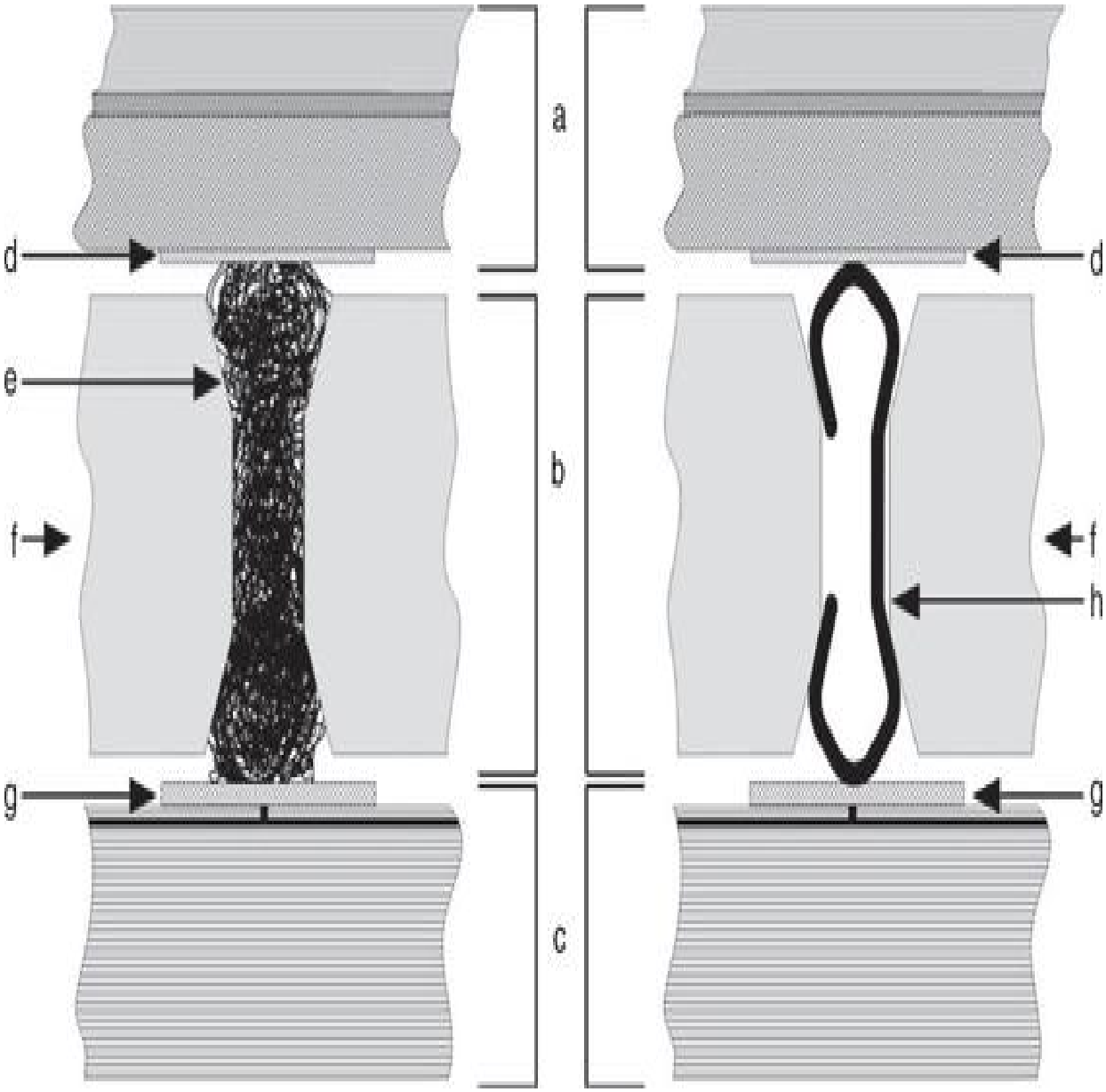


FIGURE 52.5 Interposer sockets electrically connecting an IC with a PCB: (*a*) land-grid array(LGA) IC, (*b*) LGA socket (interposer), (*c*) PCB, (*d*) contact on bottom of IC, (*e*) Fuzz-Button contact, (*f*) socket insulator, (*g*) contact pad on PCB, and (*h*) spring contact.

Additional subelements such as fasteners, washers and springs are required for assembly and to enhance shock and vibration resistance or for thermal management.

Although Fuzz-Button technology is among the most reliable of LGA interconnect schemes, some defects are common to this socket style. Pulled wires (Fig. 52.6) as well

as leaning and missing contacts can occur, although the interconnect reliability is quite high if the socket is in good condition prior to assembly and if the LGA stack is assembled correctly.

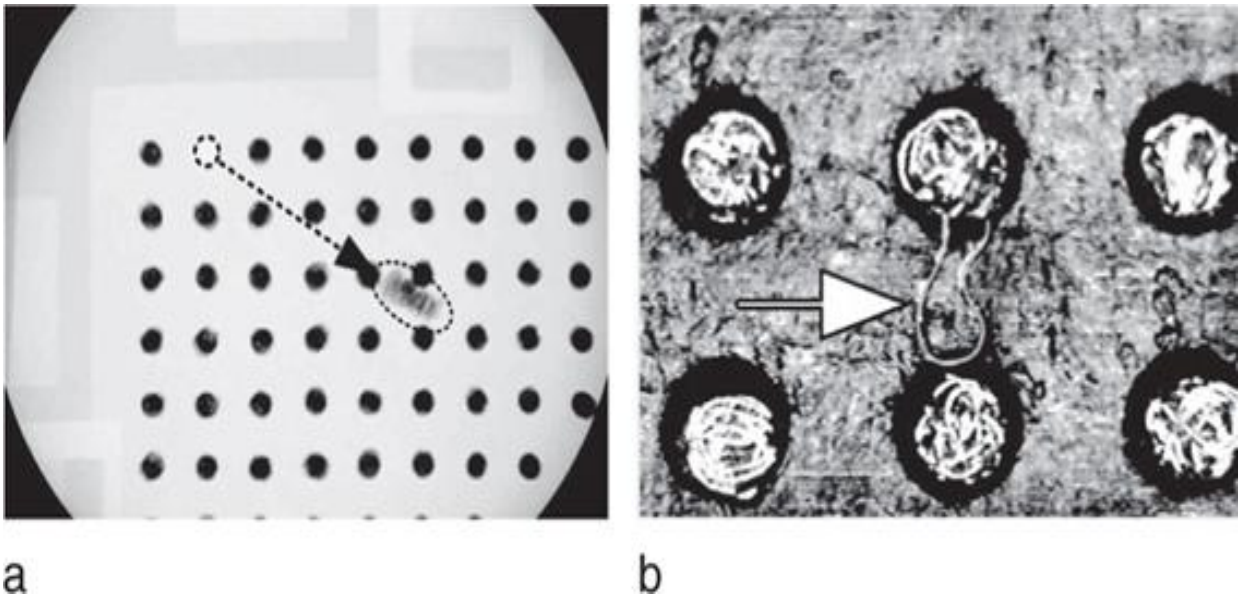


FIGURE 52.6 Defects associated with Fuzz-Button contacts. (*a*) X-ray image of an assembled LGA IC. The dashed circle denotes an empty contact position. The dislodged contact (within the dashed ellipse) lies between the IC and the socket. (*b*) Photograph of a Fuzz-Button contact with a pulled wire that is near shorting.

If too much pressure is applied to metal-filled polymer contacts, they can deform and flow over time, lessening contact pressure. As a result an open or intermittent contact failure may occur.

52.3.5 Pressure Plate

The pressure plate is fastened atop the LGA package and couples to the bolster plate under the PCB. It forces the LGA package in contact with the socket and the socket to the lands on the PCB for completion of the electrical circuit. Besides being responsible for interconnecting the socket to package and board, it imparts the necessary mechanical

rigidity to the LGA stack for shock and vibration resistance and dependable operation. Reliability of this stack is highly dependent on the materials chosen and mechanical design of same. Force on the stack has to be moderated to preclude damage to the IC package or the PCB. Guidance is needed from the LGA package manufacturer and from the LGA socket manufacturer as to how much force can be applied without damaging any elements of the pressure-interconnect stack.

52.3.6 Thermal Management

Frequently, thermal management solutions are built into the LGA stack. The heat-sink, if constructed properly, can serve as the pressure plate. A thermal interface material such as graphite foil or other thin thermal transfer material can be sandwiched between the heat-sink and the IC package to enhance heat dissipation from the IC package.

52.4 ASSEMBLY

In addition to good design, proper process strategy and precise assembly are crucial to LGA interconnect reliability. The following steps should help the engineer achieve good results, but as stated previously, if the design is flawed, interconnect reliability will be flawed as well.

52.4.1 Order of Assembly

LGA assembly should be done after all other soldering, press-fit and mechanical assembly steps are completed. LGA sockets are not rated for high-temperature excursions. The

stress of other manufacturing procedures may be enough to disrupt pressure-interconnection.

Gold pads on the PCB must remain as clean as possible—free of solder, flux deposits, chemicals, and contaminants. Once assembled, all chemicals must be kept away from the LGA socket. The heat of solder rework can also cause interposer damage or LGA device failure, so rework is best completed, where feasible, before LGA assembly or after removal of the LGA. If the LGA is removed for rework, use a shield to protect LGA pads on the PCB from solder, flux, or tool damage.

52.4.2 Prior to PCB Processing

A high-temperature masking tape can be used to cover LGA lands on the PCB. This will protect it from flux residue, spattered solder, stray solder beads, etc. The tape should be capable of sustaining multiple reflow cycles. A polyimide tape with acrylic adhesive[1] is recommended to minimize tape adhesive residue. Thoroughly test any tape before using it to confirm that it does not leave adhesive residue. Inspect PCB pads after tape removal to ensure no residue was left behind. Silicone-based adhesives have been found to leave deposits that can interfere with electrical interconnect. Since silicone is largely insoluble in most common solvents, attempts to clean any residue will be futile.

52.4.3 PCB and LGA Land Cleaning

Cleanliness is one of the most important attributes for successful pressure-interconnect assembly. Pads on the LGA IC and on the PCB should be cleaned and inspected prior to application of the socket. Even if a masking tape is used on the board during processing, there is the opportunity for

materials to condense under the tape. A wipe with isopropyl alcohol, methanol, or a Vertrel-based cleaner is useful for normal flux condensates and process residues. Do not flood the area with solvent. Instead, use a solvent-saturated lint-free wipe or non-shedding sponge. Even lint-free materials can snag on PCB pads, board edges, and drilled holes and leave fibers or debris. Tests should be made to find the most appropriate and abrasion-resistant wipe. Ensure that the cleaned lands are perfectly dry before assembly. A Vertrel-based cleaner is ideal for this due to its inherently low boiling point (generally below room temperature). Because it boils so quickly, it can cause some local moisture condensation which may leave a slight, localized, innocuous discoloration on land surfaces, but its quick drying nature ensures that there will be no liquids within the stack to short at in-circuit test (ICT) or power-up.

52.4.4 LGA Socket Cleaning

Although it is important for the socket to be clean, never wipe it as this could damage fragile contacts. Even the use of compressed air to remove dust may dislodge or damage a contact. It is best to work with the socket supplier to ensure that interposers arrive clean and ready for use.

52.4.5 Inspection

Inspect LGA pads on the PCB and on the LGA prior to assembly. Inspect both sides of the interposer to ensure that contacts are present and in good condition. Holding the interposer socket up to the light will quickly show whether there is a missing contact.

52.4.6 Socket Application

The socket seating plane must be kept parallel to the surface of the PCB. Applying it at an angle can cause damage to the delicate contacts of the socket and compromise contact reliability. The same can be said about sliding the socket on the board; it is likely to result in socket contact damage.

The socket must be oriented properly on the board so that the contact pattern of the socket matches the land pattern on the PCB. There are molded guide pins on the socket that help with this, with one peg larger than the other to match a similar drilled pattern in the PCB. The socket usually has a missing corner contact to match the LGA IC package and corresponding LGA land pattern on the printed circuit assembly (PCA). It is important not to drop the LGA IC package on the socket or slide it on the socket, as doing so could damage delicate socket contacts.

52.4.7 Fastening

So many mechanical designs are available that listing any particular method for LGA stacking is impractical. Some rely on spring clips whereas others use traditional screw fasteners, as shown previously. If held by four screws, as often is the case, then a “tire lug” torque pattern should be employed to ensure even tightening (Fig. 52.7).

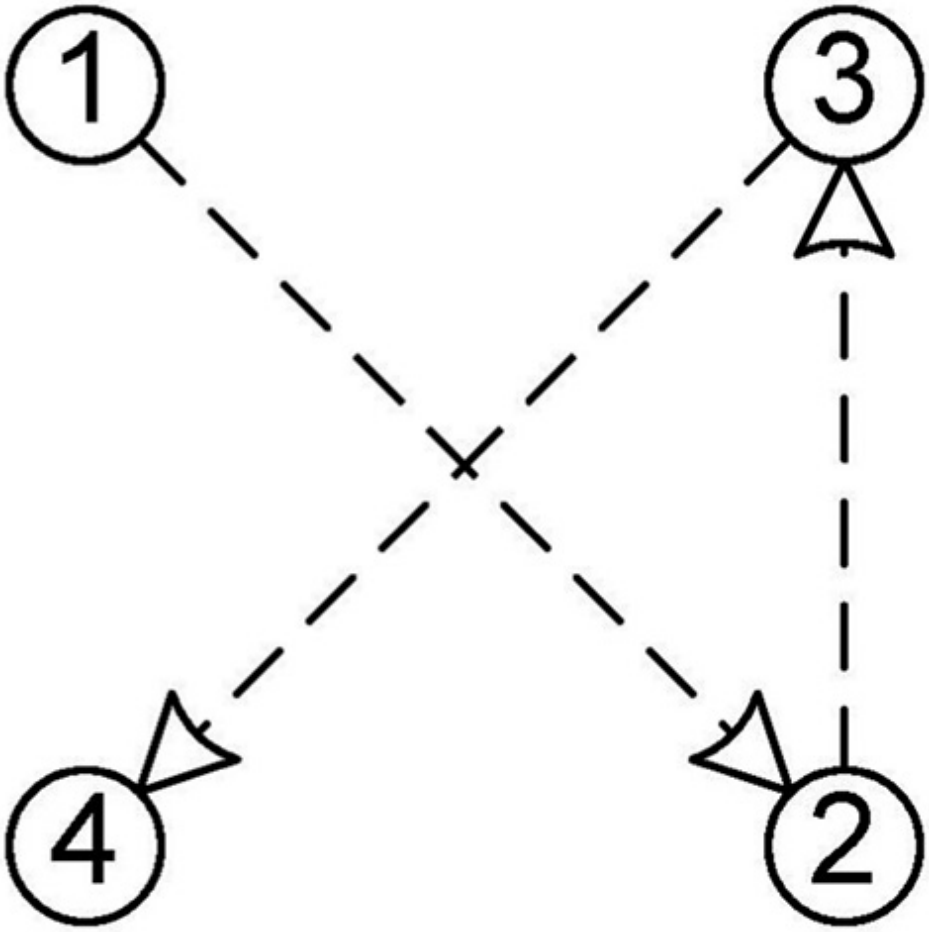


FIGURE 52.7 Manual torque pattern for even fastening of a four-screw LGA stack. Each fastener should receive the same number of turns or partial turns to ensure even seating of the LGA stack.

Slow and even tightening is important to avoid damage to the LGA IC device, the LGA socket or the PCB and to ensure proper compression for reliable electrical contact. The number of revolutions per fastener depends on the pitch of the screw and socket requirements. Ideally a four-headed torque driver should be used with each head rotating at the same speed and a calibrated slip-clutch on each driver to prevent overtightening of the stack.

A tooling plate with strategically located board supports should be created to hold the PCA during LGA stack assembly in order to both retain the board and minimize board flexure for the preservation of solder joints on the PCA.

52.4.8 LGA Socket Rework and Reuse

Ease of device replacement for upgrade or repair is one of the key benefits of using pressure-interconnect technology. Most pressure-interconnect sockets are designed for reuse. Check with socket manufacturer for the permissible number of reuses per their design. Some are specified for as many as twenty replacement cycles. Reliability and reuse depend on a number of factors, including mechanical robustness of the socket, thermal exposure history, shock and vibration experienced during operation, proper initial assembly and exposure to degrading contaminants from the initial process and during field use. Note that there are usually no reuse limits on other elements of the system (LGA IC package, printed circuit assembly, bolster plate, heat-sink, or pressure plate). After each disassembly all parts should be carefully inspected to ensure that contact platings are in good condition and that mechanical fasteners are not showing signs of excessive mechanical wear.

Sometimes, due to the malleability of gold (as used for LGA pads and PCB pads), interposer contacts may stick to this soft metal. Therefore when removing the LGA IC device from the socket or the socket from the PCB, ensure that the socket contacts have not pulled free or distorted. If there is a single contact sticking, this may be indicative of other bent, broken, or displaced socket contacts. Any of these symptoms may compromise interconnect integrity of the stack on reassembly. Sticking is prevalent with filled-polymer or Fuzz-Button contacts and there can be enough adhesion of plated spring contacts to LGA IC or PCB-plated lands to result in damage to these fragile elements.

52.5 PCA REWORK

If soldered joints on the PCA need to be reworked in the vicinity of the pressure-interconnect stack, use a thermal profile board, perform a mock solder repair, and measure the thermal effect on the socket. Ensure that the LGA IC and socket temperatures are maintained within their respective manufacturer’s thermal limit guidelines. Ensure that process chemicals (flux, cleaners, etc.) do not run under the LGA socket.

52.6 DESIGN GUIDELINES

52.6.1 Traces Beneath LGA Elements

It is advisable to keep active traces off the surface of the PCB where they could get crushed by the bolster plate or the socket. Since bolster plates are generally flat and large, the forces are spread out. The molded socket frame exerts a more concentrated force on the PCB surface due to its narrow outline and may compress any surface traces running beneath it.

52.6.2 Clearance for Tall Components

The pressure plate or heat-sink usually overhangs the LGA IC package. For this reason, tall components should be kept outside of the pressure plate/heat-sink footprint to prevent mechanical interference with the LGA stack.

52.6.3 Components under the Bolster Plate

As previously mentioned, placing components under the bolster plate should be avoided. If components are required in this area, then the bolster plate should be relieved to allow for appropriate clearances. This may require the use of an extra-thick bolster plate to preserve its stiffness after relief machining.

52.7 REFERENCE

1. Freedman, G. M., and Baldwin, E. A., “Method and Material for Maintaining Cleanliness of High Density Circuits during Assembly,” Proceedings of the SMTA Pan-Pacific Conference, February 2003.

PART 10

QUALITY

CHAPTER 53

ACCEPTABILITY AND QUALITY OF FABRICATED BOARDS

Robert (Bob) Neves
Microtek Laboratories, Changzhou, China

53.1 INTRODUCTION

53.1.1 Reasons for Appropriate Acceptance Criteria

Other than the financial tie between the user and supplier, nothing affects the relationship between these two more than product acceptability and quality. These issues define the relationship. As the printed circuit board (PCB) is the foundation for almost all electronic products, the user cannot tolerate defective boards. At the same time, cost is always a critical issue and imposing expensive and unnecessary acceptance criteria can be a major disadvantage. Failure to provide acceptable and quality product is the largest factor that affects the deterioration of the relationship between user and supplier. All of the components in an electronic

product rely on the PCB to get information and power from place to place. An interruption of this process because of a defective PCB results in a failed product. In other words, a poor quality product at a low price is worthless.

53.1.1.1 Customer Satisfaction. Brand name is one of the most valuable things that the original equipment manufacturer (OEM) possesses. A product's success or failure is quite dependent on the perceived quality that the brand name suggests. OEMs rely on getting products quickly from the design programs to market, and a slowdown due to quality issues can significantly impact a product's introduction and thereby affect their brand. The negative publicity from field failures can also have a significant effect on a brand. Agreed upon acceptance and quality criteria reduce the likelihood of nonconforming PCBs.

53.1.1.2 Reduction of Cost. If the PCB buyer clearly states the required acceptability and quality criteria to the manufacturer, the manufacturer can more clearly understand the buyer's costs. Cost reductions are a permanent fixture in the manufacturing environment. For companies to survive in this competitive market, they must address costs. Unacceptable, low-quality product that cannot be sold is a direct and significant cost.

53.1.1.3 Liability and Litigation. Showing that the PCB was purchased to mutually agreed upon "standards" goes a long way to reducing litigation and financial liability.

53.1.2 Printed Circuit Board Functions

A PCB is required to do three things for the buyer when it is received:

1. The PCB physical form should match the intended design. The dimensions and placement position of the interconnection points along with the quality of the coating on these interconnection points must be acceptable and of high quality to facilitate the attachment of components.
2. The PCB should provide proper interconnection between components. This allows the assembly to function properly as intended.
3. The PCB should provide insulation between interconnection points that should not be connected.

These three items should be “acceptable and of high quality” at the time of purchase and continue to remain “acceptable and of high quality” throughout the expected life of the product. There are a lot of details between the few preceding lines defining those three things. The rest of this chapter will define the details of “acceptability” and “quality” for the PCB in order to fill in the spaces created by the three previously listed requirements.

53.1.3 Industry versus Customer Standards

Properly implemented acceptability and quality criteria give both user and supplier a clear picture of what is expected. Without clear instructions on how the acceptability and quality of the PCB should be implemented at the supplier, the user is unlikely to get a product that meets his or her needs. A clear definition of what the user wants can help make the relationship between the two much more successful, especially as complexity of the PCB makes acceptability and quality criteria more critical and challenging. In general, PCB manufacturers have gotten larger and produce many more PCBs. This makes the user’s

individual PCBs a much smaller part of the big picture and their uniqueness may be lost. Therefore, it is essential to define what is required for acceptability and quality clearly and early in the relationship between the user and supplier.

53.1.4 Objectives of Acceptability and Quality Criteria

The PCB needs to be supplied at a quality level that is capable of withstanding the assembly process, as it will undergo several operations to mount and rework components and connectors. This assembly and rework process has gotten more complicated and damaging to the PCB, especially with the introduction of lead-free products. The acceptability criteria should attempt to anticipate the conditions of the soldering process to ensure the PCB will survive the assembly and rework process and still function as intended.

53.2 SPECIFIC QUALITY AND ACCEPTABILITY CRITERIA BY PCB TYPE

Many unique inspection properties for PCBs are dependent on their type of manufacture. There are two major classifications of printed circuits: rigid PCBs and flexible PCBs.

53.2.1 Rigid PCBs

Rigid PCBs make up the bulk of what is built around the world. Rigid PCBs are used in a variety of applications and products. The materials and testing procedures for each type

of PCB can be dramatically different. These manufacturing details are thoroughly covered elsewhere in this book and are only touched on here. The processing for multilayer PCBs is a multiple of that required for single- and double-sided PCBs, plus indexing and lamination processes are needed. The additional processes required for each additional layer introduce opportunity for anomalies to creep into the PCB.

53.2.1.1 Single-Sided PCBs. These contain no plated-through holes (PTH), eliminating the need to inspect the attributes associated with PTHs. These PCBs are much simpler to manufacture and PCB shops specializing in these types of PCBs have fewer processes to manage. Many single-sided PCBs are manufactured using a punching process to make part mounting holes and create the outline of the PCB. Single-sided PCBs are typically the least expensive type of PCBs and are usually used in simple and inexpensive applications.

53.2.1.2 Double-Sided PCBs. These differ from single-sided PCBs in that the circuitry is on both sides of the PCB and there are PTHs connecting the top to the bottom. Moving from single-sided to double-sided PCBs requires the manufacturer to keep consistency of the image from top to bottom, and also requires drilling and through-hole-plating processes. These additional processes also require increased inspection, as the attributes they represent can significantly affect acceptability and quality of the PCB.

53.2.1.3 Multilayer PCBs. These are much more complex than double-sided PCBs as they require that circuitry be embedded within the PCB. The PTHs must also make connection to internal layers as well as top and bottom layers. Multilayer PCBs also introduce the lamination process, which is where the manufacturer actually creates

the composite PCB from layers of circuitry in a lamination press under high pressure and heat.

53.2.1.4 Backplane PCBs. These multilayer PCBs have connector arrays installed that hold other PCBs. These arrays must be rigid enough to ensure that insertion of PCBs does not affect their performance and reliability. They usually have many layers and tend to be large and thick. Here, again, the manufacturing processes differ from those of traditional multilayer PCBs, and additional requirements for the connector area and PTH areas are necessary.

53.2.1.5 High-Frequency PCBs. These can be any of the preceding types of PCBs and have unique properties that allow high-speed electrical signals to travel within or on the PCB without significant degradation. The materials used and geometry of the circuit are critical to produce the correct impedance for these signals to maintain integrity. Additional testing is typically performed to verify the more precise nature of the requirements for these types of PCBs, such as controlled impedance.

53.2.2 Flexible PCBs

Flexible PCBs must be capable of bending and flexing, either for installation or continuously throughout the product's life, and come in single-sided, double-sided, multilayer, and high-speed versions just like the rigid PCBs previously described.

53.2.3 Rigid/Flexible PCBs

Rigid/flexible combination PCBs combine the benefits of the rigid PCB with integrated flexible parts. This type of PCB requires evaluation of both the rigid and flexible sections for acceptability.

53.3 METHODS FOR VERIFICATION OF ACCEPTABILITY

53.3.1 Production PCB

Most acceptability criteria are evaluated on the production PCB by visual or dimensional means. Visual inspection is typically done under low magnification by human operators. Although the human eye is very capable of catching inconsistencies in the circuit patterns and surface materials, it is not always consistent and can allow nonconforming attributes to slip through. Because of this, many companies have turned to using automated optical inspection (AOI) machines to check pattern integrity, consistency, and dimensions. AOI provides a much more consistent evaluation of circuit geometry than the human eye, but is a slower and more costly option. Many visual inspection attributes have dimensional attributes attached them. It is important to note that magnification for inspection of dimensional attributes should be sufficient to make an accurate measurement to determine acceptability.

53.3.2 Test Coupons and Patterns

For testing purposes, there are several reasons to utilize test coupons and patterns that are representative of the PCBs rather than the PCBs themselves. The downside of using coupons is that they take up space on the manufacturing panel and therefore increase the overall cost of the PCBs. Also, the test coupons are not actually part of the PCB and are typically placed at the edges of the production panel, whereas test patterns may be produced totally separately from the production panel. This can cause the coupons and patterns to reflect different attributes than the PCBs they are

attempting to represent. It is very important to take steps to ensure that the test coupons and patterns are actually manufactured in a manner that is representative of all the attributes of the PCBs associated with them. It is important to ensure that any holes in the coupon are drilled with the same tools and parameters as those on the corresponding PCB. Coupons and patterns are typically used in situations where using a PCB for testing would either not provide the information required or the PCB would have to be destroyed in order to get the information. Coupons and patterns can be used for microsectional analysis, electrical measurements, environmental simulation, and reliability evaluation. See Fig. 53.1 for an example of test coupons taken from IPC-2221. [Unless noted otherwise, figures in this chapter are courtesy of the Association Connecting Electronics Industries (IPC), and are taken from the publication IPC-600, “Acceptability of Printed Circuits.” These figures can be found in that document under the headings noted in this chapter for specific topics. Figures credited to the author of this chapter are taken from presentations made by him. Other figures are from the sources noted in the captions. For further details on design and placement of coupons, see IPC-2221.]

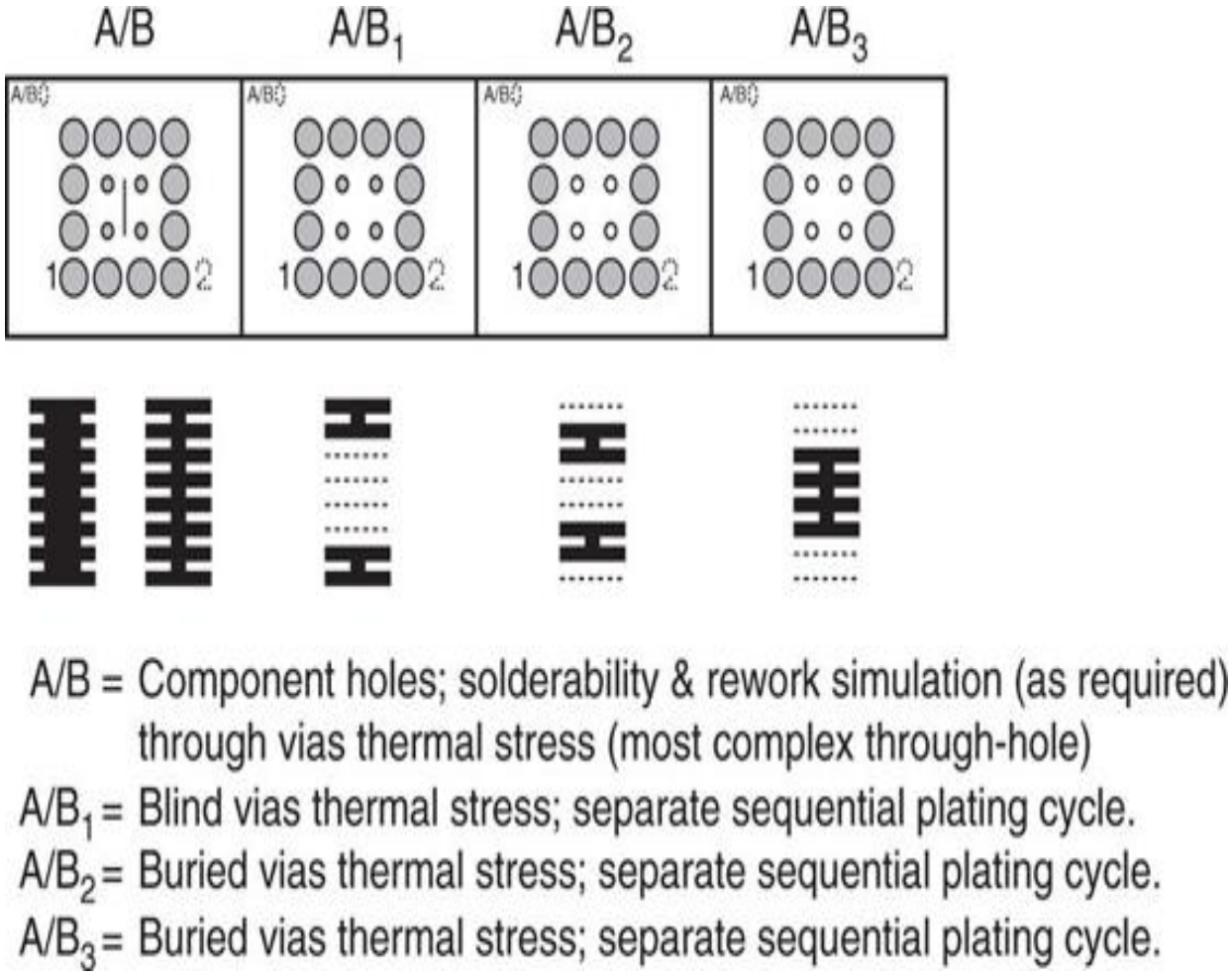


FIGURE 53.1 Quality conformance test coupons taken from IPC-2221. (*Courtesy of IPC*.)

53.3.3 Microsection

Microsectioning the holes from a PCB provides a cross-sectional view of the construction of the PCB. Microsectioning a PCB with a design that removes nonfunctional pads makes it virtually impossible to inspect all the interconnecting layers in the hole, so microsections are typically done on associated and optimized coupons containing PTHs that contain pads on all the layers. Microsectioning PCBs requires great skill, as the PCB contains both hard and soft materials and the area of interest is very small. Improper microsection technique can either create or

hide anomalies. For example, interconnection separation can be created or hidden by improper microsection preparation techniques.

53.4 INSPECTION LOT FORMATION

An inspection lot consists of all the PCBs fabricated from the same materials, using the same processing procedures and constructions that are produced under the same conditions. Differing PCBs can be combined to form an inspection lot, but then they must all be submitted together for inspection. It is the PCB manufacturer's responsibility to maintain traceability for all the PCBs in an inspection lot along with any corresponding test coupons that were separated from the production panels. The success of inspections greatly depends on how the inspection lot is formed. The goal of forming the inspection lot for a particular attribute is to allow, if applicable, a smaller sampling of the inspection lot to be representative of the entire lot. In forming inspection lots and sampling groups, the methodology for producing the attribute and the consistency of that methodology or process must be taken into consideration. Some PCB processes are done in batch form and others are done on a panel-by-panel basis. Understanding process techniques is critical in forming inspection lots and sampling groups that are representative of the product.

53.4.1 Sampling Inspection

For some attributes, 100 percent inspection is not necessary or prudent. In these cases, a sampling of the PCBs from the inspection lot is allowed to represent the entire inspection lot. Most performance specifications specify which attributes can use sampling inspection and to what extent sampling

may be performed. There are many sampling plans available; the most widely known, and historically used, is MIL-STD-105, which describes an acceptable quality level (AQL) for samples of an inspection lot. However, it allows a small amount of defective material to be considered “acceptable” and has typically been replaced by sample plans where defective parts that are found during inspection cause the lot to be termed “nonconforming.” This style of plan is defined as defective parts (C) equals zero (C = 0). If the inspection lot is considered “nonconforming” during a sampling procedure, the supplier may elect to screen 100 percent for the nonconformance, removing only the nonconforming PCBs from the inspection lot.

53.4.2 Inspection Tool Calibration

It is important that the all inspections be carried out with equipment that is calibrated and traceable to internationally recognized standards. Two of the documents that govern inspection equipment and facilities are ISO-17025 and IPC-QL-653.

53.5 INSPECTIONS CATEGORIES

53.5.1 Materials Inspection

This inspection usually consists of certifications from the material supplier, supported by data from the supplier’s own inspections. The materials used must be inspected by the PCB manufacturer to ensure compliance with customer requirements.

53.5.2 Qualification Inspection

The PCB supplier must provide proof to the user of its qualifications to build the product specified. The user must then review this proof in order to minimize the risk associated with buying from the PCB manufacturer. This process usually includes the PCB manufacturer supplying a self-declaration of capabilities such as those found in the IPC-1710, and then supplying some kind of physical sample or testing data to support the assertions made in the self-declaration. It is up to the PCB user to determine the level and detail of qualification required. This approach can leave things unverified or unaudited and recognizing the need from the PCB user community, the IPC has set up a PCB Supplier Validation Program that lists qualified manufacturers and products that have been tested and inspected to IPC standards like the IPC-6012 and IPC-A-600. Matching PCB user needs to the IPC Validation Services database is one way to significantly improve the chances of getting good information about the capabilities of a PCB supplier. More details regarding the program can be found on the Web at IPCValidation.org.

53.5.3 Quality Conformance Inspection

These product verification inspections use specified acceptability criteria and are performed prior to shipment of the PCBs to the customers. These inspections can be defined either by industry or customer standards, or a combination of both.

53.5.4 Reliability Testing

This testing consists of looking for imperfections in the PCB that may show up some time during the product’s field life.

They include accelerated life testing for both the interconnection and insulation attributes of the PCB. Please see Chaps. 59, 60, and 61 for a detailed discussion of reliability testing.

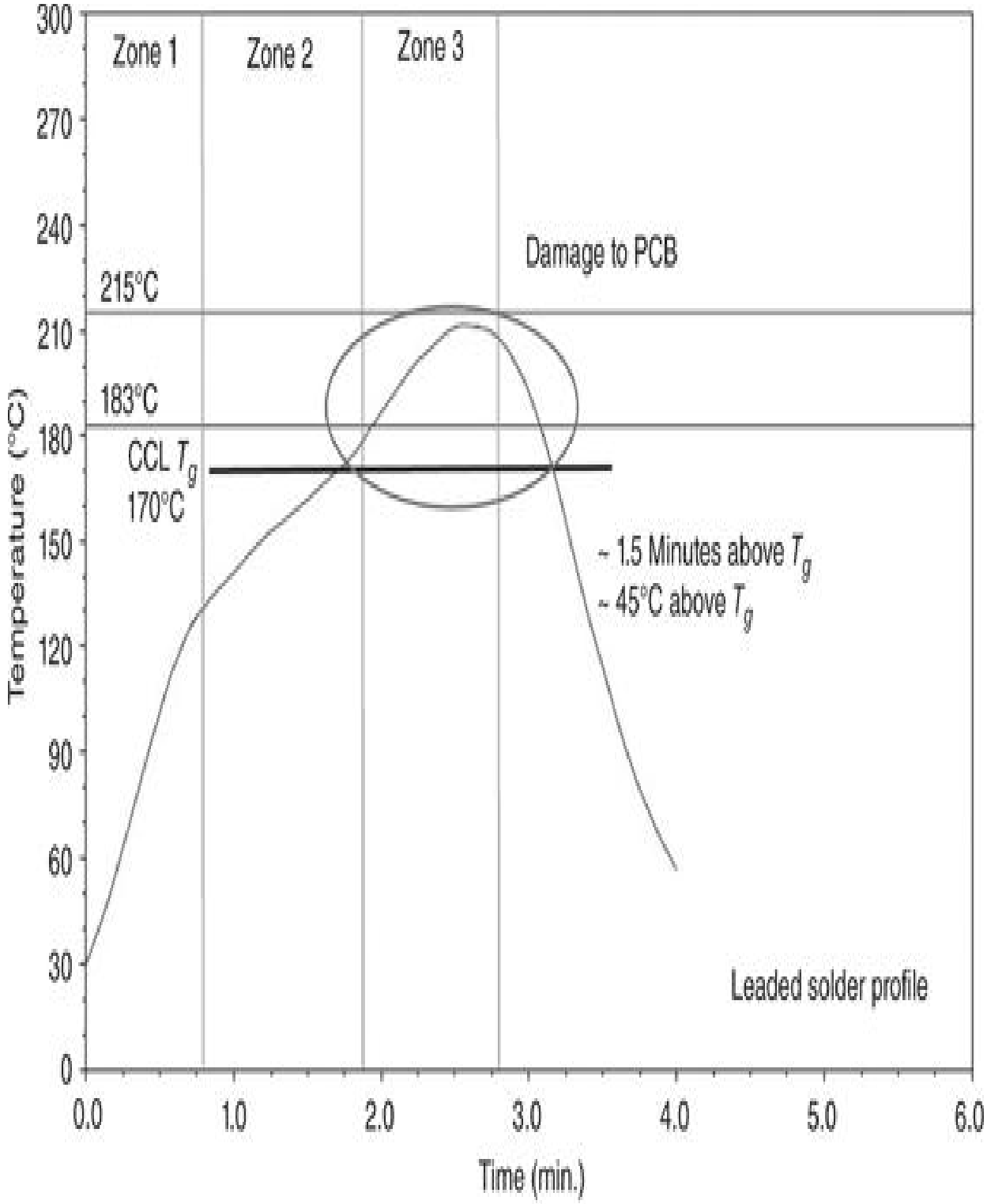
53.6 ACCEPTABILITY AND QUALITY AFTER SIMULATED SOLDER CYCLE(S)

The user expects the PCB to survive the assembly and rework process and still perform its job during the expected life of the product. Temperature excursions that approach or exceed the base material's glass transition temperature (T_g) can significantly affect some attributes of the PCB. For these attributes, it is important that the PCB be examined after solder cycling that simulates the type and quantity of soldering operations (rework included) that the PCB is expected to undergo during the assembly process. It is important to note that each rework process usually includes two soldering cycles: one to desolder the affected part, and one to reattach a new part.

53.6.1 The Effects of Lead-Free Assembly on PCB Acceptability and Quality

The lead-free assembly process can have a significant and detrimental effect on the PCB's reliability and quality, as it increases both the soldering temperature and the time the PCB is exposed to that temperature. This will accelerate degradation of the base material and can have significant impact on the PCB. Figure 53.2 shows damage related to time and temperature above T_g. It is essential to establish

that the PCB was capable of being assembled and was acceptable when it was delivered to the assembly organization, as poor assembly techniques can severely compromise the integrity of the PCB. It is almost impossible to look at a PCB after assembly and definitively state that the fault lies entirely with the PCB manufacturer or with the assembly organization.


Zone 1
Zone 2
Zone 3
Damage to PCB
215°C
183°C
CCL T_g
170°C
~ 1.5 Minutes above T_g
~ 45°C above T_g
Leaded solder profile
Temperature (°C)
Time (min.)
300
270
240
210
180
150
120
90
60
30
0
0.0
1.0
2.0
3.0
4.0
5.0
6.0

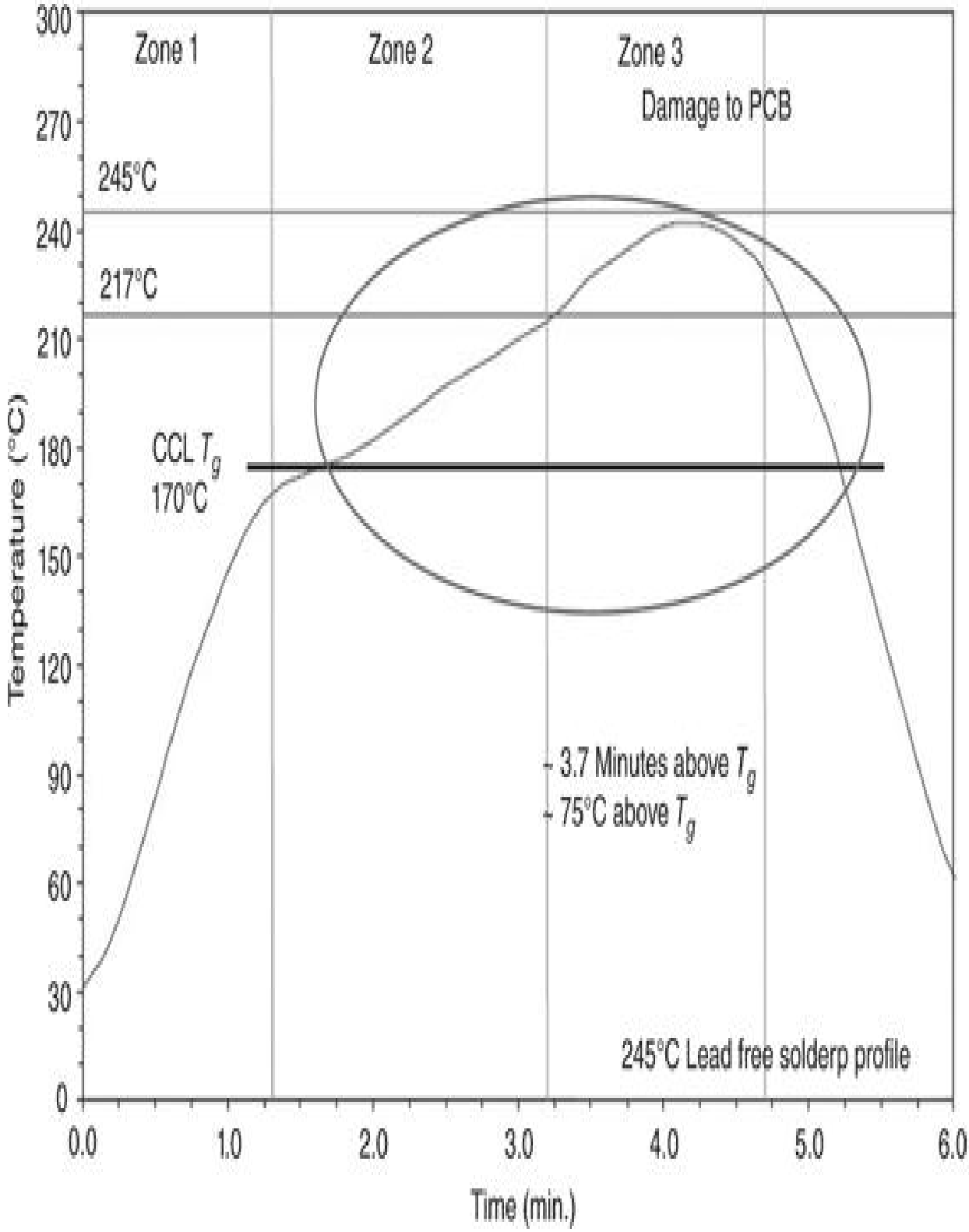

Zone 1
Zone 2
Zone 3
Damage to PCB
245°C
217°C
CCL T_g
170°C
~ 3.7 Minutes above T_g
~ 75°C above T_g
245°C Lead free solderp profile
Temperature (°C)
Time (min.)
300
270
240
210
180
150
120
90
60
30
0
0.0
1.0
2.0
3.0
4.0
5.0
6.0

FIGURE 53.2 Damage done to PCBs during typical leaded and lead-free solder cycles. (*Courtesy of Microtek Laboratories*.)

53.6.2 PCB Issues Created by Lead-Free Assembly

Copper reduction: Lead-free solder, when molten, rapidly dissolves copper into it. One must be very careful when using lead-free solder on copper surfaces without a protective barrier of some type (e.g., nickel); otherwise, the copper conductors and plated through holes may be reduced to a point where they are not adequate for the design.

Base material degradation: Base materials begin to degrade and decompose during soldering and can reduce the insulating properties and cohesion of the resin system in the base material causing electrical failure or delamination.

Conductive anodic filament: As the base material system degrades, the resistance to Conductive anodic filament (CAF) formation decreases.

Increased expansion causing premature PTH failures: Base materials expand when exposed to soldering temperature. This expansion becomes pronounced above the T_g of the resin system in the base material. The increased temperature of lead-free soldering can cause premature failure of the PTHs due to this increased expansion. See Fig. 53.3 for PTH expansion characteristics with temperature.

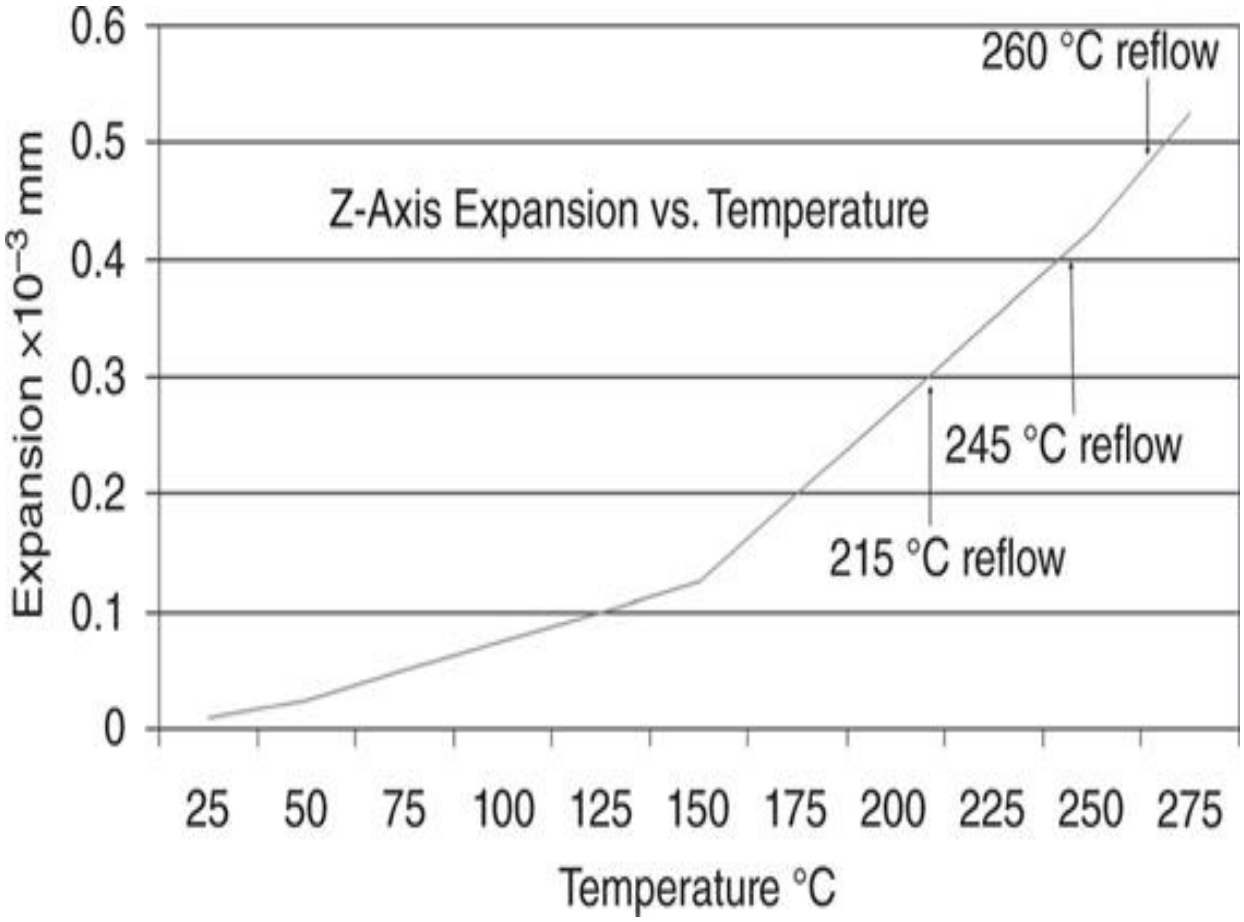


FIGURE 53.3 *Z*-axis expansion characteristics of 150°C T_g PCBs versus temperature. (*Courtesy of Microtek Laboratories*.)

Solderability: Lead-free solder does not wet as well to solderable surfaces as leaded solder does, so pad size, solder volume, and flux type and quantity must be taken into account.

53.7 NONCONFORMING PCBs AND MATERIAL REVIEW BOARD FUNCTION

Standards and customer documentation establish minimum quality and acceptability requirements for the inspections performed. If the PCB does not meet these requirements, it becomes nonconforming. This does not necessarily mean the

PCB is scrapped, although this often what happens to nonconforming PCBs. What it does mean is that with a generic standard, samples that do not meet the stated requirements must be “dispositioned” outside the standard. To determine whether a nonconforming PCB is or is not “scrap,” a material review board (MRB) must be established to evaluate the nonconformance(s). The MRB is usually made up of one or more representatives from the departments of quality, production, and design. The purpose of the materials review board is to disposition nonconforming products and effect positive corrective action within a short time to eliminate the cause of recurring discrepancies. The MRB’s responsibilities include

- Reviewing questionable PCBs or materials to determine conformance with acceptability, quality, and design requirements
- Reviewing nonconforming PCBs for effects on design functionality
- Authorizing repair or rework of nonconforming PCBs when appropriate
- Establishing responsibility and/or identifying causes for nonconformance
- Authorizing the scrap of excessive quantities of materials

When all else fails and the PCBs do not meet the intended end product use, they need to be scrapped.

53.8 THE COST OF THE ASSEMBLED PCB

The cost of the assembled PCB continues to increase because of density, complexity, and rising material and component costs. The value added to the PCB can be 10 to

20 times the cost of PCB. If it is found that a nonconforming PCB is the cause of failure, the total cost of the assembly process is likely to be passed on to the PCB manufacturer as their responsibility.

53.9 HOW TO DEVELOP ACCEPTABILITY AND QUALITY CRITERIA

53.9.1 Using Industry Standards

There are both advantages and disadvantages to using industry standards for acceptability and quality requirements.

53.9.1.1 Advantages

- International standards represent a consensus of what is possible and common for acceptance.
- They increase the likelihood of PCB users getting what they expected.
- The PCB manufacturer is unlikely to become as expert in complying with a “customer” specification as it would an industry standard.
- The repeated experience of inspecting to an industry standard means the quality personnel at the PCB manufacturer are more likely to spot nonconformance.
- Industry standards are a great place to start developing company-specific requirements for acceptability and quality.

53.9.1.2 Disadvantages

- International standards are developed by a cross section of the industry. The resultant standards often represent the “least common denominator” requirements in order to satisfy the broad range of participation.
- Although these standards may meet most of a PCB buyer’s needs, they often leave deficiencies that necessitate additional requirements being imposed upon the PCB supplier.
- By nature, international standardization efforts always lag the state-of-the-art in the industry.
- Standards can over- or underspecify requirements for an industry segment’s needs.

53.9.2 Industry Specifications

The following are lists of the most commonly used specifications for PCBs. IPC standards are the most widely used in the industry and therefore are referenced in this chapter as examples.

53.9.2.1 Defense Supply Center Columbus (DSCC)

MIL-PRF-55110, “Printed Wiring Board, Rigid, General Specification for”

MIL-PRF-31032, “Printed Circuit Board/Printed Wiring Board, General Specification for”

MIL-P-50884, “Printed Wiring Board, Flexible or Rigid-Flex, General Specification for”

53.9.2.2 International Electrotechnical Commission (IEC)

IEC-61188, “Design of Printed Boards and Printed Board Assemblies”

IEC-62326, “Printed Board Performance for Capability Approvals”

IEC-61189, “Test Methods for Printed Boards and Printed Board Materials and Printed Board Assemblies”

53.9.2.3 Institute for Interconnecting and Packaging Electronic Circuits (IPC)

ANSI/J-STD-003, “Solderability Tests for Printed Boards”

IPC-1710, “OEM Standard for Printed Board Manufacturer’s Qualification Profile (MQP)”

IPC-4552, “Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards”

IPC-4553, “Specification for Immersion Silver Plating for Printed Circuit Boards”

IPC-4554, “Specification for Immersion Tin Plating for Printed Circuit Boards”

IPC-A-600, “Acceptability of Printed Boards”

IPC-6011, “Generic Performance Specification for Printed Boards”

IPC-6012, “Qualification and Performance Specification for Rigid Printed Boards”

IPC-6013, “Qualification and Performance Specification for Flexible Printed Boards”

IPC-6016, “Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards”

IPC-6202, “IPC/JPCA Performance Guide Manual for Single- and Double-Sided Flexible Printed Wiring Boards”

IPC-TM-650, “Test Methods Manual”

53.9.2.4 Japan Printed Circuit Association (JPCA)

JPCA-PB01-2004, “Printed Wiring Boards”

JPCA-HD01-2004, “HDI Printed Wiring Boards”

JPCA-DG01-1997, “Design Guide for Multilayer Printed Wiring Boards”

JPCA-DG02-2006, “Performance Guide for Single- and Double-Sided Flexible Printed Wiring Boards”

53.9.2.5 Underwriters Laboratories (UL)

UL-94, “Flammability Testing”

UL-796, “Standard for Safety for Printed Wiring Boards”

UL-796F, “Flexible Materials Interconnect Constructions”

53.9.3 Using Customer Standards

Customer standards should reflect the unique nature and needs of the company’s products. Unfortunately, company history often can affect these criteria and overemphasize criteria for failures that were previously experienced. It is recommended that customer standards be used to augment, not replace, industry standards. Consider the following when creating a customer standard:

- Understanding where and how the product will be used can influence the use of extended or reduced criteria in specific requirement areas.
- Understanding the stresses to which the assembly process exposes the PCB is fundamental in defining the acceptability criteria. Process elements such as leaded or lead-free reflow or wave solder, double-sided reflow, hand-soldering, and rework all significantly impact the requirements of the PCB.

53.10 CLASS OF SERVICE

Functionality through operational life should be the ultimate criteria for acceptance. To account for the fact that a PCB will see different end-use environments and conditions, acceptance criteria are typically broken into three classes of service. Each company must establish the level of acceptance as it is dependent on the functional criteria to which the PCB will be subjected. The IPC has established recommended guidelines for acceptance, based on end use, categorized as Classes 1, 2, and 3. The following subsections describe the classes.

53.10.1 Class 1: General Electronic Products

Class 1 includes consumer products and some computer and computer peripherals suitable for applications where cosmetic imperfections are not important and the major requirement is the functioning of the completed PCB.

53.10.2 Class 2: Dedicated Service Electronic Products

This class consists of communication equipment, sophisticated business machines, and instruments for which high performance and extended life are required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.

53.10.3 Class 3: High-Reliability Electronic Products

Equipment and products for which continued performance or performance on demand is critical belong in Class 3. Equipment downtime cannot be tolerated, and the equipment must function when required (e.g., life support systems, flight control systems). PCBs in this class are suitable for applications in which high levels of assistance are required and service is essential.

53.11 INSPECTION CRITERIA

When inspecting PCBs, the requirements can be separated into externally observable attributes (those where acceptability can be determined from the outside of the PCB) and internally observable attributes (those that require microsectioning to determine acceptability). The actual requirements vary by specification, but the requirements stated in this chapter generally follow IPC document guidelines.

53.11.1 Externally Observable Attributes

Visual examination for applicable attributes is typically conducted at 3 diopters (~1.75× magnification). If it is not possible to determine whether the condition is acceptable at this magnification, progressively higher magnifications should be used to confirm acceptability. Dimensional requirements such as conductor spacing or width may require different magnifications and devices with measurement scales or reticules as part of the inspection

tool to allow accurate measurement(s) of the specified dimensions. The PCB users may also specify other magnifications and inspection tools. Note that the use of higher magnifications for visual-type attributes can produce false results due to illumination and attribute contour effects. Visual inspection criteria are difficult to define grammatically. An effective way to define visual inspection criteria is to use line illustrations and/or photographs. The IPC utilized this method in the publication IPC-A-600, “Acceptability of Printed Boards,” to “visually standardize” the many individual interpretations to specifications on printed boards.” Of the different types of inspections specified, surface visual inspection is the least expensive. Visual inspection is performed on 100 percent of the PCBs or on a sampling based on an established sampling plan. Inspection for visual imperfections, following a sampling plan, is done on the premise that the PCBs were 100 percent visually screened during the fabrication process. Externally observable imperfections can be divided into 10 groups:

1. Surface imperfections in the insulating material such as burrs, nicks, scratches, gouges, cut fibers, weave exposure, and voids
2. Subsurface imperfections such as foreign inclusions, measling/crazing, delamination, and base material voids
3. Conductive pattern imperfections such as loss of adhesion and reduction of conductor width or thickness due to nicks, pinholes, scratches, surface plating, or coating imperfections
4. Hole characteristics such as diameter, misregistration, foreign material inclusions, and plating or coating imperfections
5. Marking imperfections affecting such characteristics as location, size, readability, and accuracy

6. Solder resist surface coating, coverlayer, and coverfilm imperfections such as misregistration, blisters, bubbles, separations, adhesive squeeze out, delamination, adhesion, physical damage, and thickness
7. Flawed dimensional characteristics affecting such characteristics as PCB size and thickness, hole size, pattern accuracy and registration, conductor width and spacing, and annular ring (dimensional inspection is usually performed using a sampling plan)
8. An unclean PCB surface due to such materials as ionic and organic contaminates
9. Poor solderability of the PCB including wetting, dewetting and nonwetting
10. Electrical discontinuity, circuit shorts, and if required, impedance mismatch

53.11.1.1 Surface Imperfections in the Insulating Material. Surface imperfections include burrs, nicks, scratches, gouges, cut fibers, weave exposure, and voids. The imperfections, when minor, are normally considered to be cosmetic issues, and usually have little or no effect on functionality. However, they can be detrimental to function in the edge board contact area and if they reduce the insulating properties of the material below acceptability limits.

53.11.1.2 Subsurface Imperfections. Subsurface imperfections are those that are visible from the surface of the PCB but are below the surface of the PCB (see Fig. 53.4).

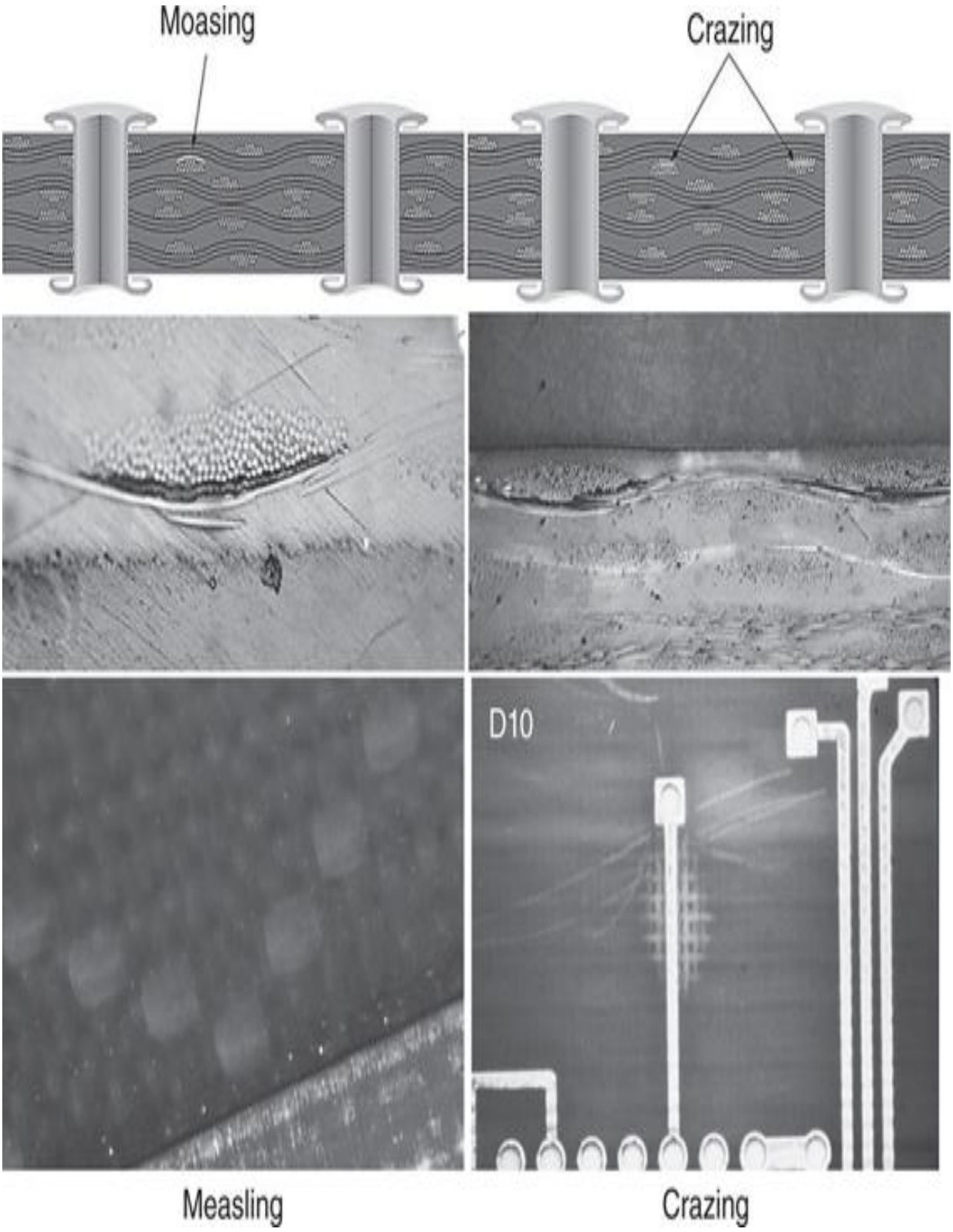


FIGURE 53.4 Base material defects: measling, crazing. (*Courtesy IPC*.)

53.11.1.2.1 Inclusion. An inclusion is a foreign particle, metallic or nonmetallic, in a conductive layer, plating, or base material. Inclusions in the conductive pattern, depending on degree and material, can affect plating adhesion or circuit resistance. Inclusions in the base material are put into the categories of translucent/nonmetallic and opaque/metallic. Translucent particles are acceptable. Opaque particles are acceptable as long as they do not reduce the minimum conductor spacing below the minimum requirement.

53.11.1.2.2 Measling/Crazing, Delamination, Blistering, and Weave Texture/Exposure. The IPC formed a special committee in 1971 to consider base material imperfections and to define them better with illustrations and photographs. The conditions are defined and discussed here:

- *Measling:* This internal condition occurs in the woven-fiber-reinforced laminated base material in which the bundles are separated at the weave intersection. Measling manifests itself in the form of discrete white spots or "crosses" below the surface of the base material. A report compiled by the IPC, "Measles in Printed Wiring Boards," was released in November 1973. The report stated that "measles may be objectionable cosmetically, but their effect on functional characteristics of finished products are [sic], at worst, minimal and in most cases insignificant." The IPC Acceptability Subcommittee readdressed the subjects of measles and crazing in 1994 and verified the 1973 findings. IPC standards allow measles in PCBs with the exception of "high-voltage" applications. As hole spacing has continued to decrease, new attention has focused on measles. There is a concern that measling could contribute to the formation of CAF on designs with close hole spacing, and the requirements for measles will likely adjust to accommodate these designs. In order to address this concern the IPC formed a blue ribbon committee which performed testing to determine if

measles contributed to CAF failure. In 2007 this committee presented a report based upon their testing that concluded that measles did not contribute to CAF growth.

- *Crazing:* An internal condition occurring in the woven fiber-based base material in which the glass fibers within the yarn are separated, crazing can occur at the weave intersections or along the length of the yarn. This condition manifests itself in the form of connected white spots or crosses below the surface of the base material, and is usually related to mechanical and/or thermally induced stress. Limited crazing is an acceptable condition as long as it does not reduce the space between conductive patterns below the minimum conductor spacing, the distance of crazing does not span more than 50 percent of the distance between adjacent conductive patterns, and no propagation results from thermal testing that replicates the manufacturing process. If crazing is present at the edge of the PCB, it should not reduce the minimum distance between PCB edge and conductive pattern.
- *Delamination:* This is a separation between plies within the base material, between a material and the conductive foil, or between any other planar separations within a PCB. Blistering and delamination are considered to be major imperfections. Whenever a separation of any part of the PCB occurs, a reduction in insulation properties and adhesion occurs. The separation area could house entrapped moisture, processing solutions, or contaminants, and could contribute to electrochemical migration or produce other detrimental effects in certain environments. The delamination or blister area may also propagate to the point of complete PCB separation, normally manifesting during assembly operations. Last but not least is the effect on solderability in PTHs. Entrapped moisture, when subjected to soldering temperatures, has been known to create steam that blows holes through the plated side

walls, exposing the resin and glass of the PTHs and creating large voids in the solder fillet.

- *Blistering:* A localized swelling and separation between any of the layers of a laminated base material or between a base material and a conductive foil or protective coating, blistering is a form of delamination.
- *Weave texture:* In this surface condition of base material, a weave pattern of glass cloth is apparent although the unbroken fibers of the woven cloth are completely covered with resin. Weave texture is an acceptable condition and should not be confused with weave exposure.
- *Weave exposure:* In this surface condition of base material, the unbroken fibers of woven glass cloth are not completely covered by resin. Weave exposure is considered a major imperfection. The exposed glass fiber bundles allow wicking of moisture and entrapment of processing chemical residues into the base material.

53.11.1.2.3 Haloing. A mechanically induced fracturing or delamination on or below the surface of the base material, haloing is usually exhibited by a light area around holes, other machined areas, or both. Haloing should not penetrate more than 50 percent of the distance to the nearest conductor and should not reduce electrical spacing below the given requirement.

53.11.1.3 Conductor Pattern Integrity. Several methods can be used to determine conductor pattern integrity. Comparison equipment, overlays, and AOI machines are routinely used compare the pattern to the digital image of the pattern. The most common conductor pattern inspection tool is the aided human eye using low (<3×) magnification. The loss of adhesion and imperfections that reduce the conductor volume or spacing make up this category of imperfections. Voids in conductors and lands can be detrimental to function, depending on the degree of

imperfection. Voids or pinholes reduce the effective conductor width, reduce current-carrying capacity, and can affect other design electrical characteristics, such as inductance and impedance. Voids in lands are also detrimental to solderability. Pinholes or voids in the conductor or land can undermine the finish coating. The presence of conductive elements in areas in which they were not intended can reduce spacing to a point where the insulation between conductors can be jeopardized. The degree that these imperfections affect the PCB depends on the intended design of the circuit. The imperfections in this group are defined as follows (see Fig. 53.5).

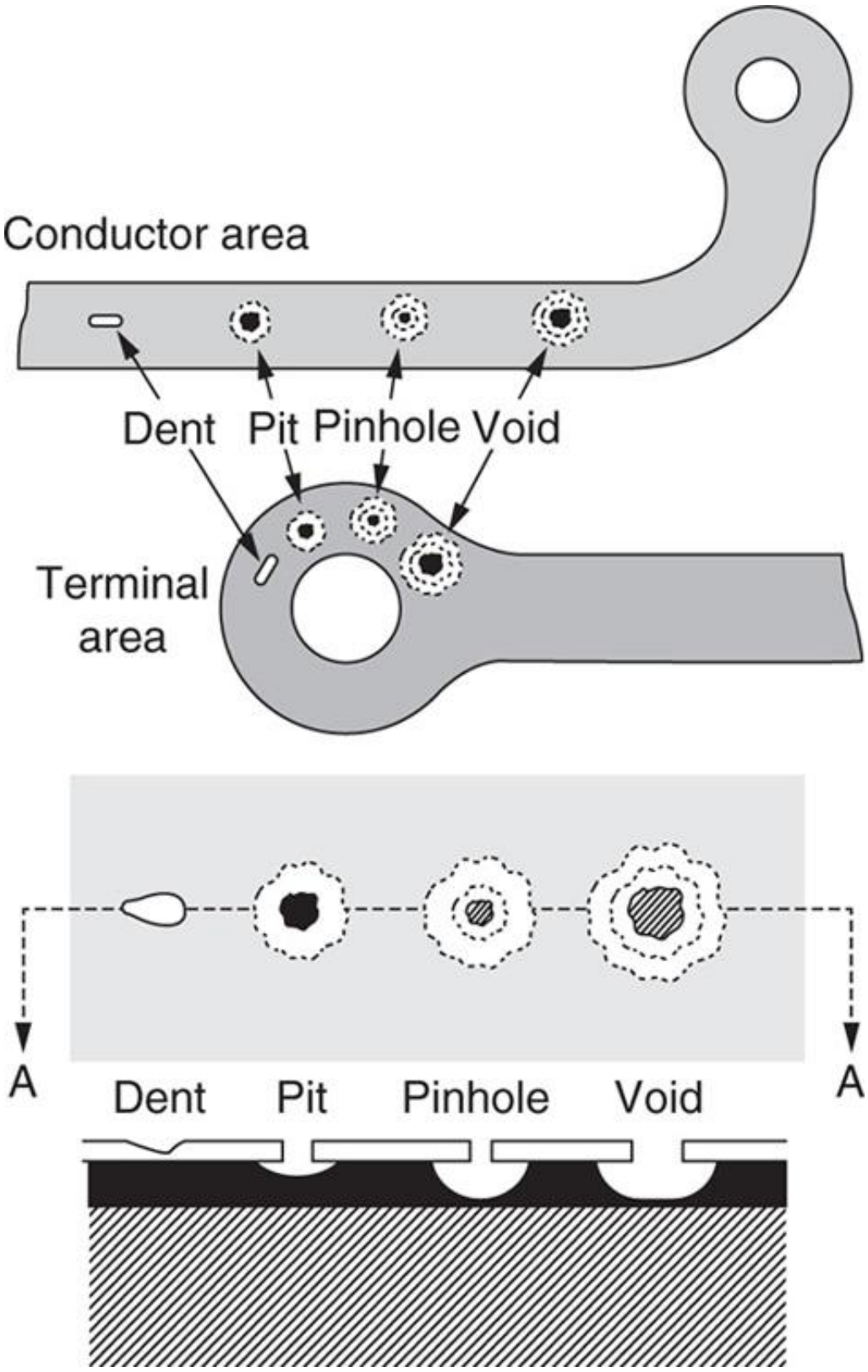


FIGURE 53.5 Dents, pits, pinholes and voids. (*Courtesy of Sandia Laboratories*.)

- *Dent:* This is a smooth depression in the conductive foil that does not significantly decrease foil thickness.
- *Pit or dish-down:* This is a depression in the conductive layer that does not penetrate entirely to the base material but does reduce the cross sectional area of the conductor. These imperfections are almost impossible to detect as they rarely give visual cues to the inspector.
- *Scratch:* This is a slight surface mark or cut that may or may not go all the way through to the base material.
- *Void or pinhole:* This is the absence of conductive material in a localized area going all the way to the base material.

53.11.1.3.1 Conductor Width. The conductor width is the observable width of a conductor at any point chosen at random on the PCB, normally viewed from vertically above unless otherwise specified. The conductor width affects the electrical characteristics of the conductor. A decrease in conductor width decreases current-carrying capacity and increases electrical resistance. Although the conductor width definition is very basic, there are two different interpretations as to where on the conductor the measurement is performed. The minimum conductor width (MCW) is measured at the minimum observed width of the conductor, and the overall conductor width (OCW) is measured at the observable width. Plating outgrowth of the top of the conductor during pattern plating can prevent the minimum width from being seen unless cross-sectioning is performed. The OCW is nondestructive and easily measured. The difference between the MCW and the OCW (see Fig. 53.6), which is measured from vertically above, can have an effect on the current-carrying capacity, inductance, and impedance of the circuit. IPC-6012, “Qualification and Performance Specification for Rigid Printed Boards,” addresses conductor width requirements and allows added width reductions for edge roughness, nicks, pinholes, and

scratches of 30 percent (Class 1) and 20 percent (Classes 2 and 3) from the minimum specified on the procurement documentation. The document states that this reduction also applies to the MCW reflected on the procurement documentation, and this allowance should be carefully considered against design needs.

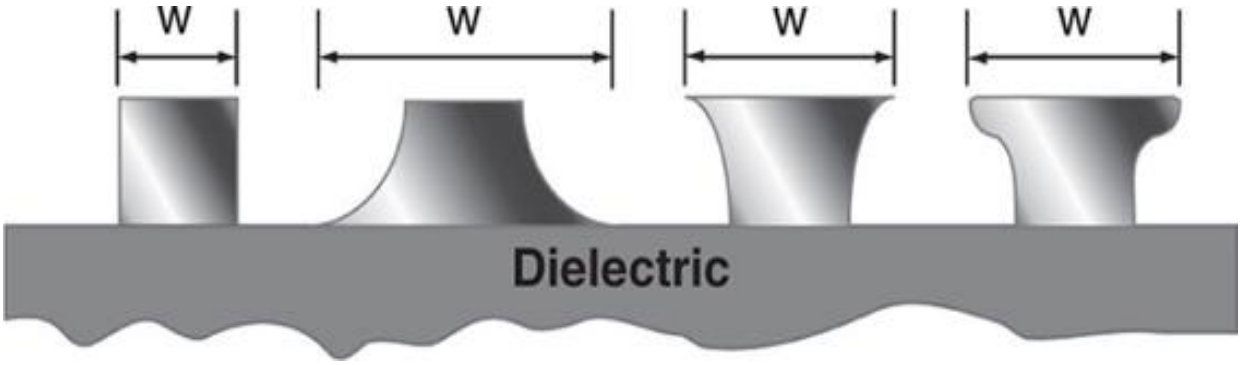


FIGURE 53.6 Overall conductor width measurement "W." (*Courtesy of IPC*.)

53.11.1.3.2 Conductor Spacing. Conductor spacing is the distance between adjacent edges (not centerlines) of isolated conductive patterns or features. The spacing between conductors and/or lands is designed to allow sufficient insulation between circuits. A reduction in the spacing can cause electrical leakage or affect the capacitance of the circuit. The cross-sectional width of conductors is usually nonuniform. Therefore, the spacing measurement is taken at the closest point between the isolated conductors and/or external *annular ring* (the portion of conductive material completely surrounding a hole). The primary purpose of the annular ring is that of a flange surrounding the hole; it provides an area for the attachment of electronic component leads or wires and acts as an anchor for the circuit. The PCB user must define the minimum annular ring dimension, which differs based on the function of the holes and whether they are plated.

53.11.1.3.3 External Annular Ring. The portion of conductive material completely surrounding a hole is called

the annular ring (see Fig. 53.7). The primary purpose of the annular ring is that of a flange surrounding the hole; it provides an area for the attachment of electronic component leads or wires and acts as an anchor for the circuit. The minimum annular ring dimension needs to be defined by the PCB user and will differ based upon the function of the holes and whether they are plated or not. Annular ring dimensions that are less than those specified can interfere with attachment of the component, and a pad breakout (zero annular ring) condition associated with the area where the circuit enters the pad can reduce the current-carrying capacity of the circuit. After verifying the dimensions of the PCB and then verifying that the minimum widths of the annular rings on all other lands are within the procurement documentation requirements, the pattern is found to be in registration with the drilled hole location. Front-to-back pattern registration can also be inspected in this manner.

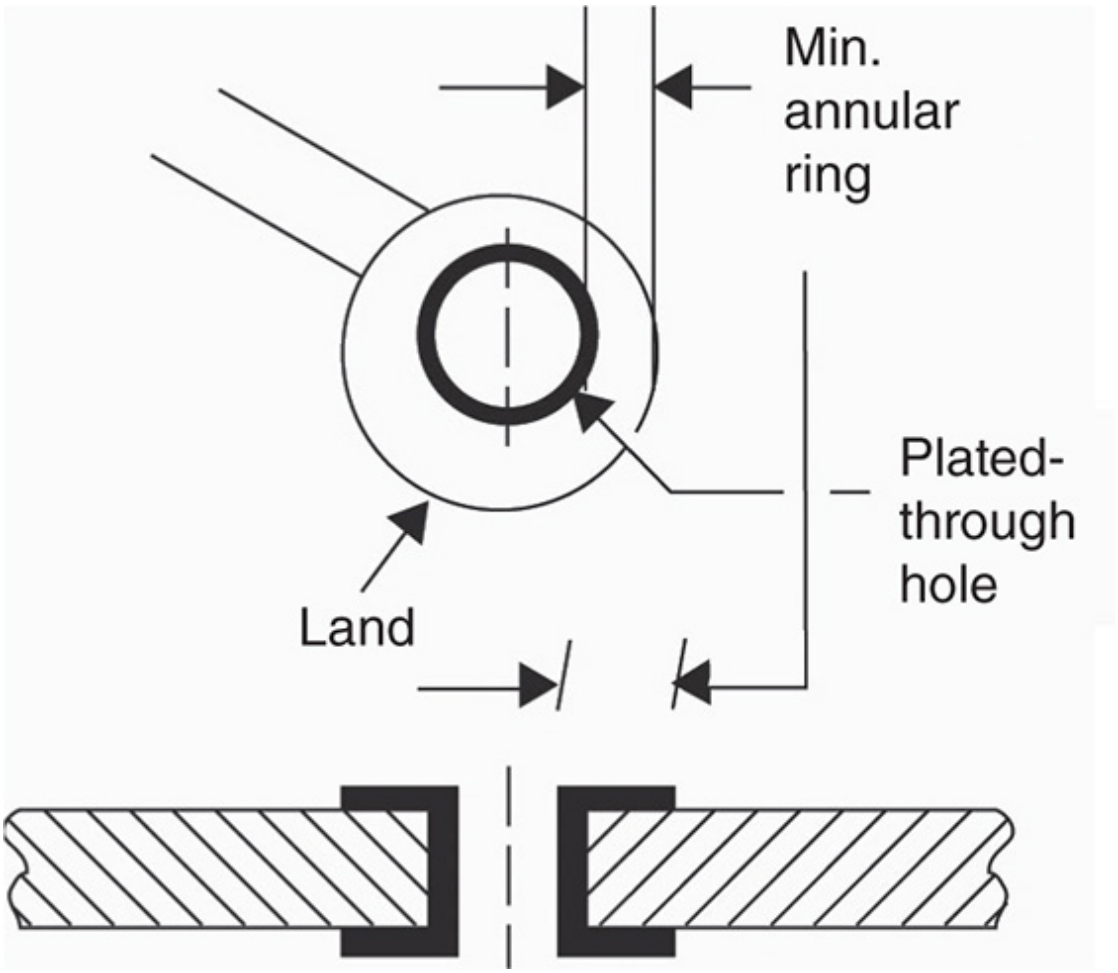


FIGURE 53.7 Minimum external annular ring (includes plating). (*Courtesy of IPC*.)

53.11.1.3.4 Plating Adhesion. A common method of inspecting for plating adhesion is the tape adhesion test, which is described in detail in the IPC test method IPC-TM-650,2.4.1. The basic test method is performed by adhering tape of known properties onto the plating, rapidly removing the tape, then inspecting the tape for removed plating on the tape adhesive.

53.11.1.3.5 Peel Strength. Peel strength is the force per unit width required to peel the conductor or foil from the base material. It is usually associated with the acceptance testing of copper-clad base material upon receipt, but it is sometimes used to test the adhesion of the conductors to the finished PCB. Peel strength tests of conductors are

usually performed after the specimens have been dip or reflow soldered. Peel strength tests of conductors are a good method of ensuring that the conductor-to-base material adhesion is sufficient to withstand assembly and rework operations.

53.11.1.4 Hole Characteristics. PTHs provide circuit interconnection from the surface of the PCB to internal layers and to circuitry on the opposite side. For this reason, much attention is correctly focused on the acceptability and quality of these holes. Nonconformance in the PTHs is a serious concern.

53.11.1.4.1 Roughness and Nodulation. Roughness is an irregularity in the side wall of a hole; nodulation is a small knot or an irregular lump found in or on the plating. Although roughness and nodulation are not desirable, they are allowable in small amounts. Roughness and nodulation create one or more of the following nonconforming conditions:

- Reduced hole diameter
- Impaired lead insertion
- Impaired solder flow through the hole
- Voids in solder fillet

53.11.1.4.2 Voids in the Plating and Finished Coating. A void is the absence of material where it is intended to be. Copper-plating voids are evaluated again during microsectional analysis, but this sampling is very small and this attribute should be thoroughly evaluated during visual inspection of the PCB. When visually evaluating voids in the PTH copper, no more than 5 percent of the holes on the PCB should exhibit evidence of voids. In holes that have voids (see Fig. 53.8), there should be no more than one void that is less than 5 percent of the hole length. Voids in the finish coating of the PCB (see Fig. 53.9) are allowed in larger

quantities than voids in the copper plating. There should again be surface finish voids in no more than 5 percent of the PCB holes, and these holes should have no more than three voids that are each less than 5 percent of the hole length.

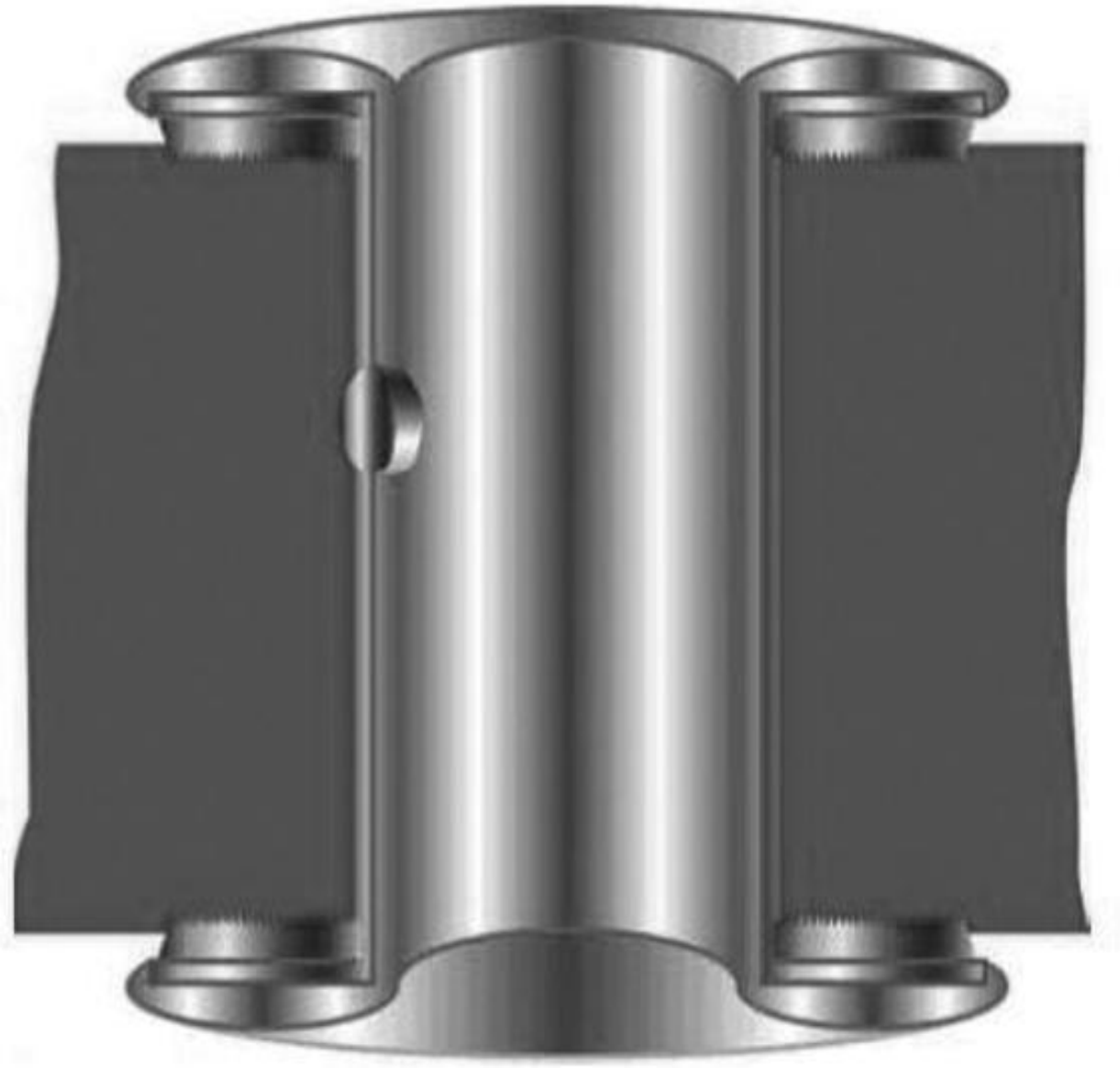


FIGURE 53.8 Plating void. (*Courtesy of IPC*.)

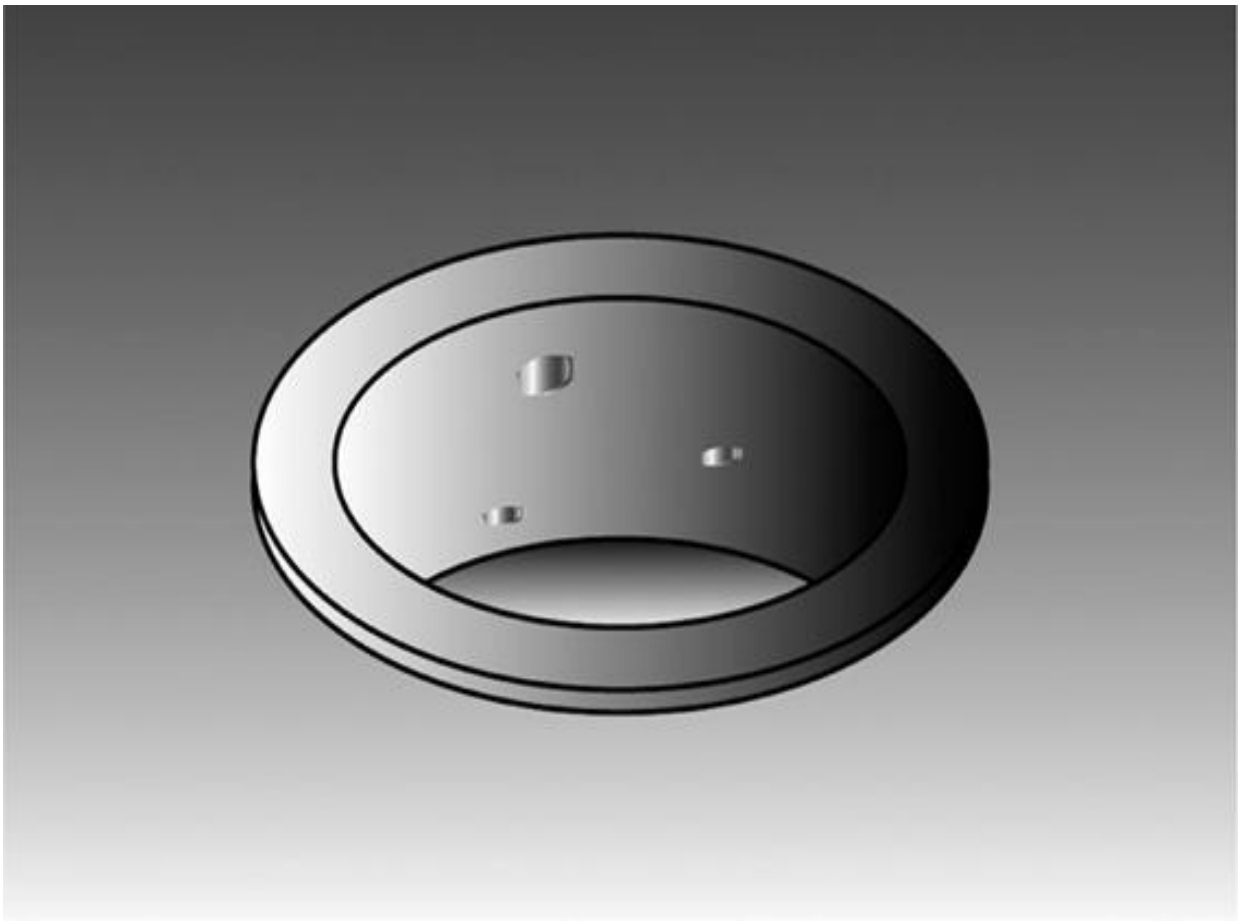


FIGURE 53.9 Voids in finished coating. (*Courtesy of IPC*.)

53.11.1.4.3 Hole Diameter. Hole size is the inner clearance diameter of the finished plated-through or unplated hole. A PTH is a hole in which electrical connection is made between internal or external conductive patterns, or both, by the deposition of metal on the wall of the hole. An unplated hole, termed an unsupported hole, is a hole containing no conductive material. Hole size measurement is performed to verify that the hole meets the intended design requirements. This size requirement is usually associated with the fit of component leads, mounting hardware, etc., plus adequate clearance for attachment metal. PTHs providing layer-to-layer interconnections, where no components are soldered into the hole, are called “via” holes. Via holes do not have a fit requirement, so only the

plating integrity is critical. Drill blank plugs and optical magnifiers are used to verify hole diameter. The latter method is utilized when soft coatings over the copper are used. The optical method prevents deformation or removal of the soft coatings within the hole. When drill blank plug gauges are used, the inspector should use a soft touch to prevent damage to the hole. The drill blank gauges should be cleaned prior to use to prevent solderability degradation. Plating nodules are sometimes present in the hole and restrict the penetration of the gauges. Forcing the gauges into the holes causes the nodules to be dislodged, resulting in voids in the PTH side wall.

53.11.1.4.4 Lifted Lands. During visual examination there should be no evidence of the lifting of lands from the base material surface. Lifted lands can trap contaminates during the assembly process and are considered undesirable for assembly.

***53.11.1.5 Marking (Legend/Silkscreen) Imperfections*.** The marking of part number, revision letter, part mounting information and orientation, etc., on a PCB is evaluated for location, size, readability, and accuracy. Marking imperfections are usually considered minor, but markings that are missing, incorrect, or partially obscured could have an effect on functionality. Marking that encroaches into the soldering area can also be a significant issue and should not reduce the solderable areas below what is stated in the procurement documentation.

***53.11.1.6 Solder Resist Coating Imperfections*.** A solder resist is a coating material used to mask off or to protect selected areas of a pattern from the attachment of solder. A solder resist can also be used as electrical insulation between isolated conductors or to define the soldering area for ball grid array (BGA) patterns. Attributes inspected are registration, blisters, bubbles, adhesion,

wrinkles, tenting, soda strawing, and delamination. Misregistration at land areas reduces or prevents adequate solder fillet formation or can expose adjacent conductors. The minimum land area to obtain adequate solder filleting should be reflected by the minimum acceptance criteria. Wrinkles, flaking, peeling, and delamination provide sites for moisture absorption and contaminants to settle on or into the PCB and can reduce the insulation between adjacent conductors, increasing the potential for electrochemical migration (ECM). When solder resist is used to define BGA patterns, the shape and position on or around the land is important to proper soldering of the BGA (see Fig. 53.10).

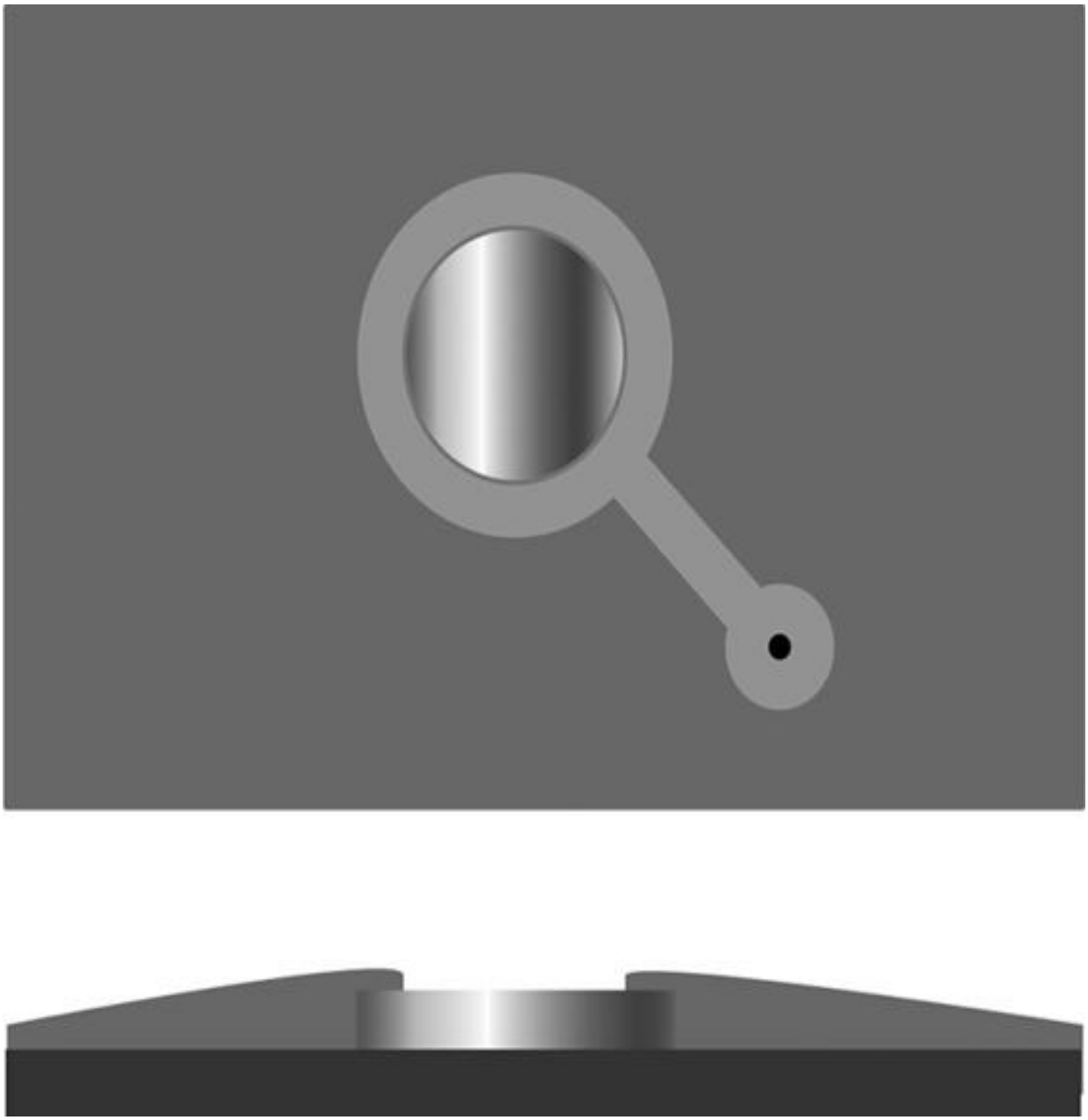


FIGURE 53.10 Soldermask defined BGA land. (*Courtesy of IPC*.)

53.11.1.6.1 Tenting of Vias. Tenting of via holes is the process of covering holes with solder resist without filling the holes, where soldering is not required or desired. This is done to prevent the potential for shorting during the assembly process and to allow for vacuum-based test fixtures to draw the assembly down onto test pins for functional test. The

requirement here is that all vias that are required to be tented are covered by resist.

53.11.1.6.2 Soda Strawing of Solder Resist. A soda straw is a long tubular void along the edges of conductive patterns where the solder resist is not bonded to the base material surface or edge of the conductor (see Fig. 53.11). If this void is allowed to reach the point where the solder resist meets the outside environment, fluxes, fluids, and other contaminates may end up trapped in the soda straw, leaving the potential for future ECM or corrosion.

FIGURE 53.11 Soda strawing between copper trace and soldermask. (*Courtesy of IPC*.)

***53.11.1.7 Coverlayer Characteristics*.** Flexible and rigid/flexible PCBs are covered with either a coating similar to solder resist or a coverfilm adhered to by acrylic adhesive. Covercoat acceptability requirements are the same as those for solder resist.

53.11.1.7.1 Coverfilm Separations. When a film is adhered to the flexible PCB surface, separations between the film and PCB surface can occur. There should be no more than three small separations that do not reduce the spacing between conductors by 25 percent or below the minimum stated in the procurement documentation. Separations along the edge of the PCB are not allowed, as they can trap contaminates.

53.11.1.7.2 Adhesive Presence on Attachment Surfaces. The presence of adhesive from the coverfilm should not reduce the solderable surfaces below the minimum reflected on the procurement documentation.

***53.11.1.8 Dimensional Characteristics*.** Contour dimensional inspection verifies that the outside border dimensions, cutouts, and key slots meet the procurement documentation requirements. Contour dimension requirements can be considered fit requirements. Both undersized and oversized PCBs can affect functionality, depending on the degree of requirement violation. Incorrect placement or size of key slots prevents the proper mounting of the PCB. Measuring methods vary from the use of a ruler or calipers to sophisticated coordinate measurement machines (CMMs). The sophistication of the method is naturally dependent on the required dimensions and tolerances.

53.11.1.8.1 External Dimensions. The external dimensions of a PCB are usually measured by calipers and micrometers. They can also be measured with a CMM or comparison gauges and templates. Tolerances for these dimensions should be reflected on the PCB procurement documentation. It is important to ensure that the measurement tools being used have sufficient accuracy to perform the intended measurements.

53.11.1.8.2 Registration, Layer to Layer, X-Ray Method. The x-ray method provides a nondestructive way to inspect layer-to-layer registration of internal layers of multilayer PCBs. It utilizes an x-ray machine and either Polaroid film or camera sensors to image the internal layers. The multilayer PCB is x-rayed in a horizontal position. The x-ray images are then examined for evidence of hole breakout of the internal lands. The lack of an internal annular ring denote severe misregistration of layers (see Fig. 53.12).

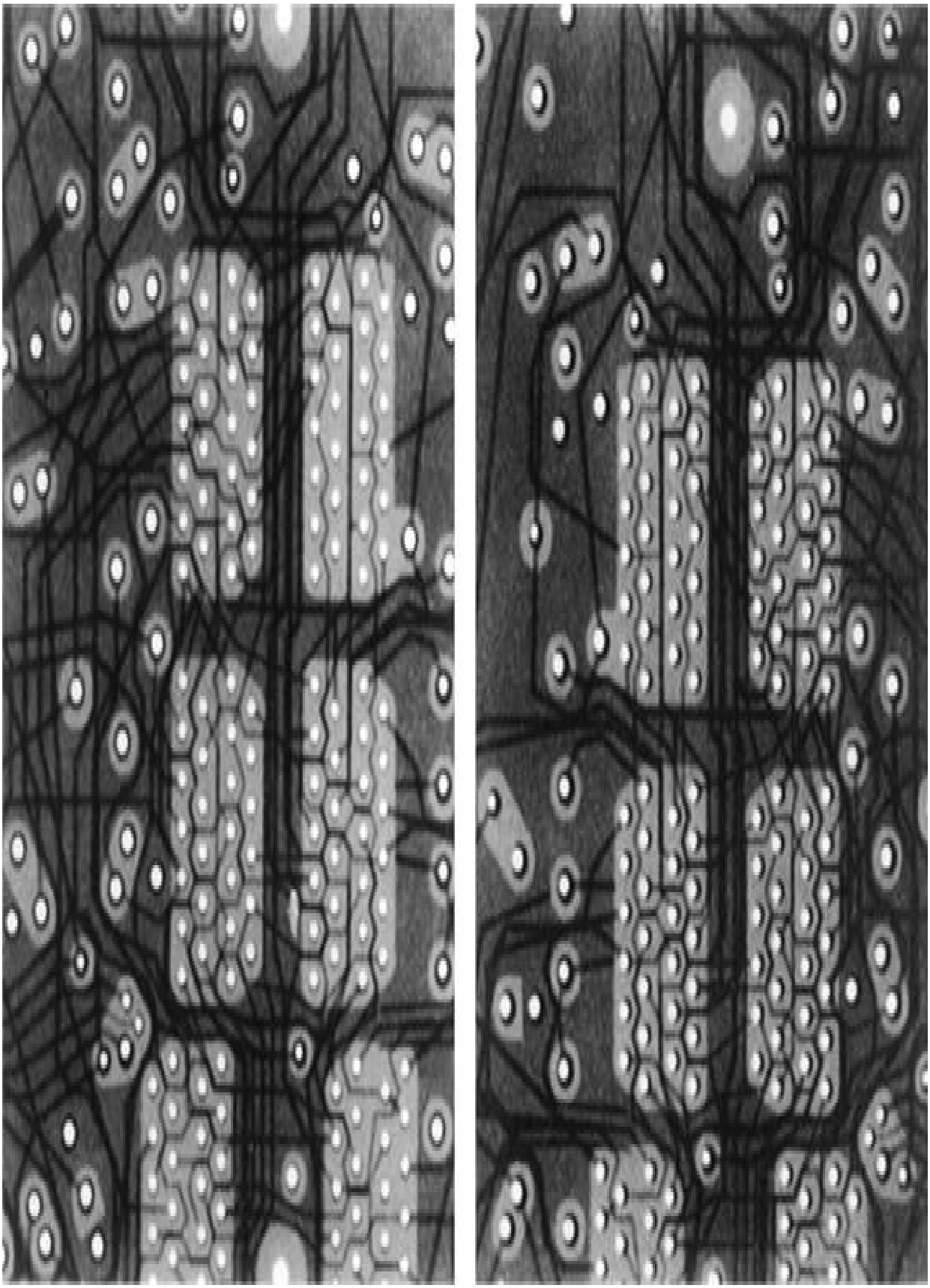


FIGURE 53.12 Layer-to-layer registration, x-ray method. (*Courtesy Sandia Laboratories*.)

53.11.1.8.3 Flatness (Bow and Twist). *Bow* is the deviation from flatness of a PCB characterized by a roughly cylindrical or spherical curvature such that, if the PCB is rectangular, its four corners are in the same plane (see Fig. 53.13). *Twist* is the deformation parallel to a diagonal of a rectangular sheet such that one of the corners is not in the plane containing the other three corners (see Fig. 53.14). Excessive bow and/or twist on a PCB are detrimental to the assembly process when the PCB must fit into card guides or packaging configurations in which flatness is critical. It can also interfere with the proper mounting of the assembly into the intended case. The method for bow and twist measurement can be found in IPC-TM-650 method 2.4.22. The maximum bow or twist allowed is 1.5 percent unless the PCB has surface-mounted devices (SMDs) attached where the requirement is reduced to a maximum allowable of .75 percent.

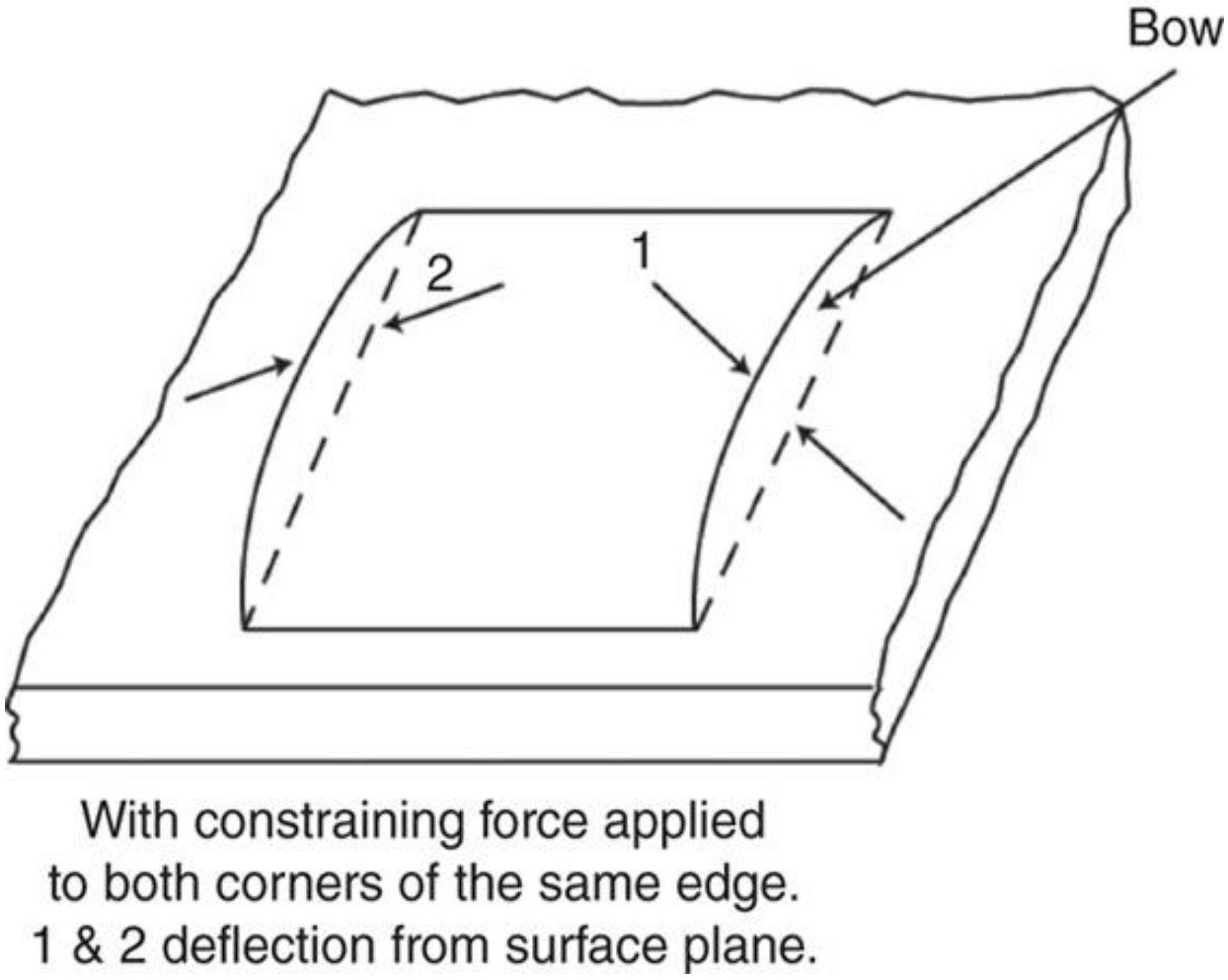


FIGURE 53.13 Bow measurement of PCB. (*Courtesy of IPC*.)

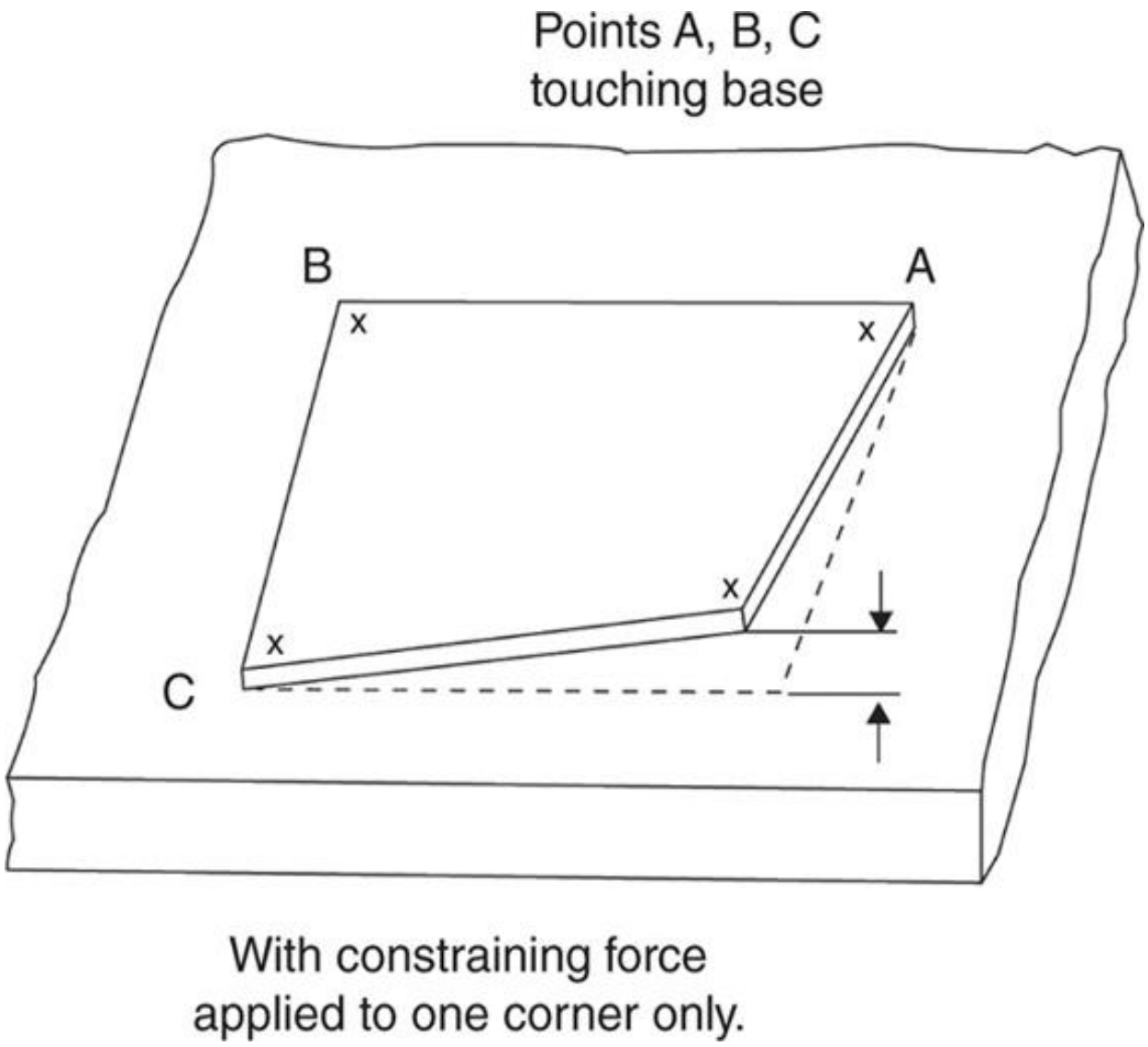


FIGURE 53.14 Twist measurement of PCB. (*Courtesy of IPC*.)

53.11.1.8.4 Cleanliness (Solvent Extract Methods). PCBs are fabricated using wet chemistry and mechanical techniques. Some of the chemical baths contain metallic salts and organic materials. These chemicals, if left on the surface, could affect the functionality of the PCBs by reducing electrical insulation resistance and promote corrosion or ECM on the conductor pattern. This condition is usually associated with low operating voltage (10 V or less) and requires three components: moisture, metallic contaminants, and voltage. The ionic cleanliness test

measures the conductivity of a deionized water and alcohol solution used to wash the PCB. Commercial equipment is available to perform ionic cleanliness testing. The organic cleanliness test uses an organic solvent wash (e.g., acetonitrile) to remove “loose” organics from the surface of the PCB. This wash solution is collected on a glass plate and the solvent is allowed to evaporate. Any organic contamination in the wash solution leaves a cloudy residue on the glass that can be subsequently analyzed for composition using ion chromatography. These two tests are mutually exclusive in that the organic test cannot detect ionic contamination and vice versa. Note that when a solder mask is required on PCBs, an additional cleanliness test is performed on the uncoated PCBs before coating.

53.11.1.9 Solderability Inspection. Solderability inspection measures the ability of the attachment points to be wetted by solder in the areas for the joining of components to the PCB. Three terms are used to describe acceptability of solderability:

- *Wetting:* The formation of a relatively uniform, smooth, unbroken, and adherent film of solder to a basis material, wetting is the preferred and acceptable condition.
- *Dewetting:* This condition results when molten solder has coated the attachment surface and recessed, leaving irregularly shaped mounds of solder separated by areas covered with a thin film of solder that fully covers the basis metal. Dewetting is not acceptable for attachment points but is allowed on ground or voltage planes for Class 1 and 2 products.
- *Nonwetting:* This nonconforming condition is the partial adherence of molten solder to a surface that it has contacted, leaving some of the basis metal exposed.

53.11.1.9.1 Solderability Testing and Coating Durability. Many methods for inspecting PCBs for solderability both quantitatively and qualitatively have been established. However, the most meaningful method is that used in the actual assembly soldering operation (hand, wave, drag, reflow soldering, etc.). ANSI/J-STD-003, “Solderability Tests for Printed Boards,” addresses the recommended test methods and subsequent storage conditions that have no adverse effect on the solderability of those portions of the PCB intended to be soldered. Test coupons or PCBs are subjected to accelerated aging for a length of time defined by a coating durability requirement reflected on the procurement documentation, followed by solderability testing. Solderability is acceptable when the surfaces to be soldered have fully wetted. See Fig. 53.15 for acceptable criteria for PTHs, and Fig. 53.16 for examples of nonwetting.

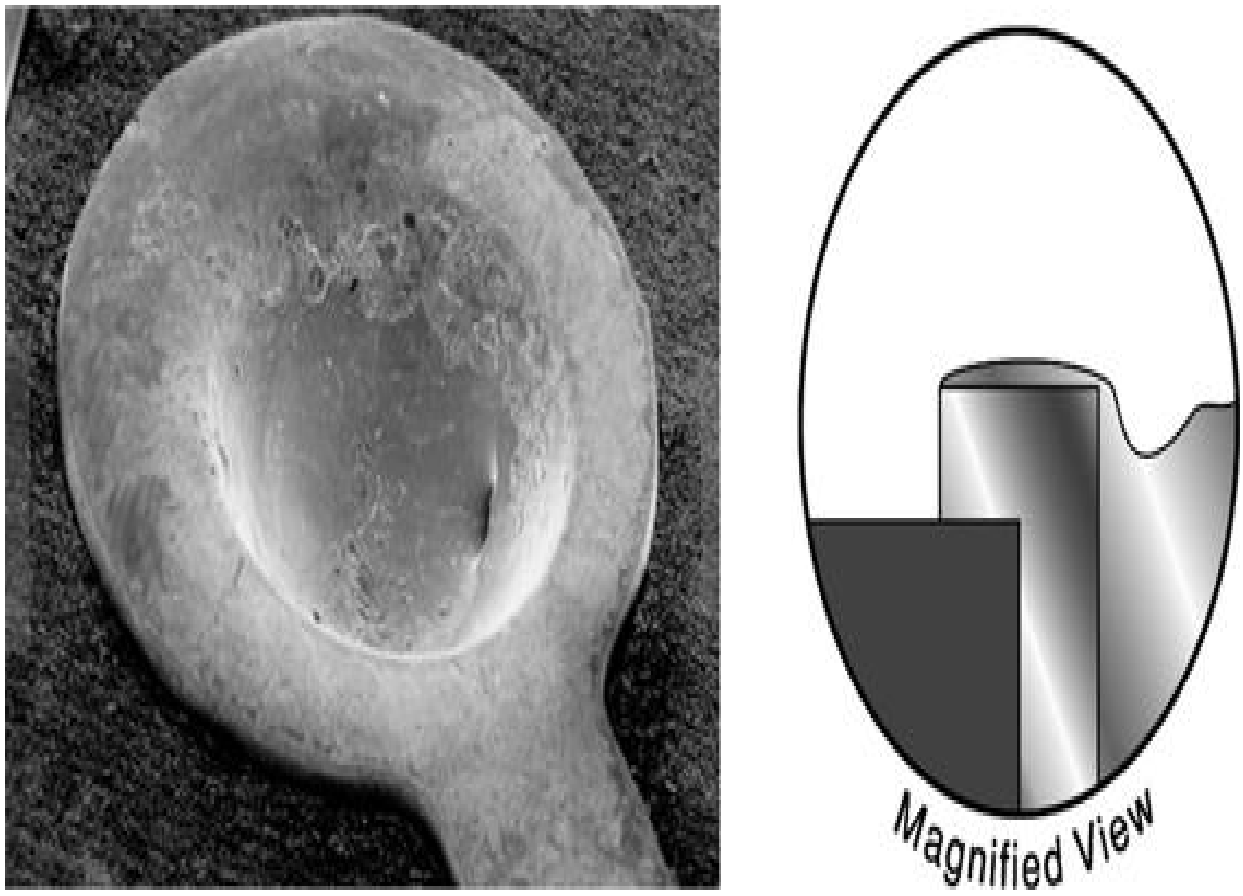


FIGURE 53.15 "Wetted" solder joint. (*Courtesy of IPC*.)

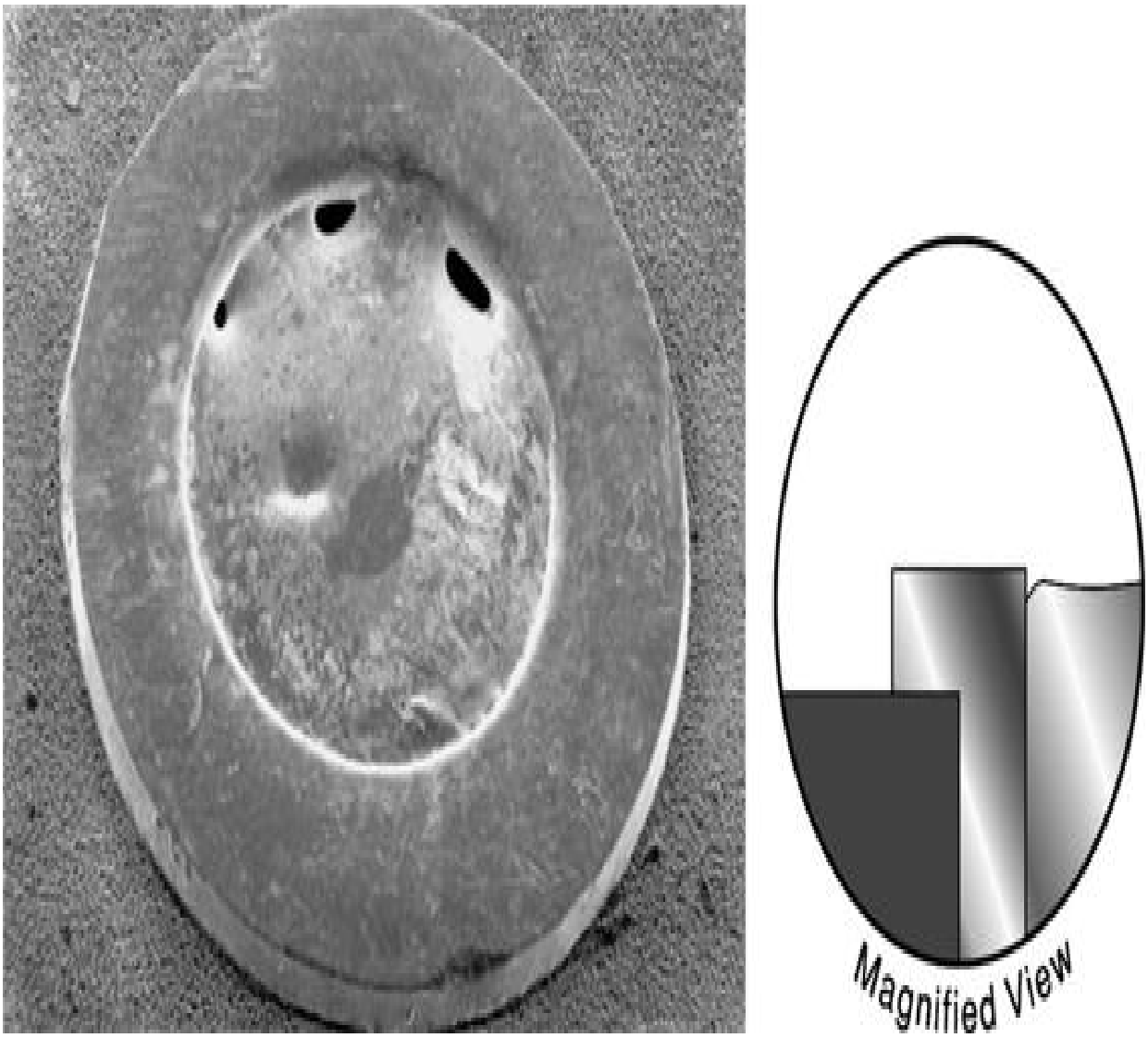


FIGURE 53.16 Non-“wetted” solder joint. (*Courtesy of IPC*.)

53.11.1.9.2 Coating Durability Requirements. The coating durability requirements are classified into three categories:

Category 1: Minimum coating durability is required. The PCB is intended to be soldered within 30 days from time of manufacture and likely to experience minimum thermal exposure.

Category 2: Average coating durability is required. This classification is intended for PCBs likely to experience

storage of up to 6 months from the time of manufacture and moderate thermal or solder exposure.

Category 3: Maximum coating durability is required. This classification is intended for PCBs that are likely to experience long storage (over 6 months from time of manufacture) and that may experience severe thermal or solder processing steps, etc. It should be recognized that there may be significant difficulty involved, a cost premium, or delivery delay associated with PCBs specified to meet this durability level.

53.11.1.9.3 Surface Finishes. Lead-free alloys are the most popular alloy used for surface finishes on PCBs due to RoHS requirements. There are many different compositions of lead-free alloys and they behave differently in practice. Other surface finishes are rapidly finding their way onto the PCBs. IPC-6012 lists more than 25 different surface finishes that are now in use for PCBs. Tin-lead solder alloys (e.g., 63/37) are also still appearing on PCBs where RoHS restrictions do not apply. It is important to understand that the composition and type of the surface finish influence solderability. The procurement documentation must state specifications for surface finish. Methods available for analyzing the alloy composition on the plated PCB include wet analysis, atomic absorption, and x-ray fluorescence (XRF). XRF is popular because of the ease of obtaining the alloy composition and thickness nondestructively.

53.11.1.10 Electrical Inspection. These inspections are performed to verify circuit integrity after processing and substantiate that the electrical continuity, signal integrity, and isolation characteristics of the PCB meet the design specifications. Electrical inspection methods are typically performed on the production PCBs, but evaluation of signal integrity is routinely performed on specially designed test coupons. Two popular nondestructive electrical tests are

insulation resistance and circuit continuity tests. These are usually performed on 100 percent of complex PCBs, especially multilayer ones. Automated electrical test equipment with either stationary or moving test probes allows the probes to make contact with the all parts of the circuit pattern in order to verify the continuity and isolation characteristics of the PCB.

53.11.1.10.1 Circuit Continuity. Continuity tests are performed on PCBs to verify that the printed circuit pattern is interconnected as designed. Testing can be performed with an inexpensive multimeter for simple PCBs or with more elaborate automated equipment such as a computer-enhanced bed-of-nails or flying probe tester. These types of automated testers can either be preprogrammed with the circuit interconnection information derived from the computer design files or can use a known good “golden” PCB as a test template to learn the interconnection information. The preferred method is to perform the continuity test on all PCBs submitted for acceptance. This method is especially recommended for multilayer circuitry, where the internal patterns and interconnections cannot be inspected visually after fabrication.

53.11.1.10.2 Insulation Resistance (Circuit Shorts). The purpose of this test is to measure the resistance offered by the insulation system of a PCB to an applied voltage. Low insulation resistances can prevent proper operation of circuits by permitting the flow of leakage current. This test can also reveal the presence of contaminants from processing residues. The test is performed by applying voltage to isolated nets and measuring the current flow between these nets. Test voltages of 40 to 500 V DC and minimum insulation resistances of 100 to 500 MΩ are popular. As with continuity testing, insulation resistance testing typically employs automated test equipment using stationary or moving probes.

53.11.1.10.3 Impedance. Impedance (see Fig. 53.17) is the amount of resistance a circuit offers alternating current (AC) signals. High frequency AC circuits require that the impedance of PCB circuits be matched to that of the components in order to transfer the most signal between the components on the assembly. Proper impedance matching also reduces radio wave emissions (EMF) from the assembly. Impedance is measured using Time Domain Reflectometry (TDR) and is typically measured using a specially designed test circuit on a coupon. Requirements for impedance as well as test circuit design must be supplied to the PCB manufacturer. Variations in impedance of up to 10 percent around the nominal value are expected and are not unusual do to standard process variations in circuit geometry and insulation make up. Tighter control of impedance is possible, but special attention must be made to processes and materials to achieve reductions in variation.

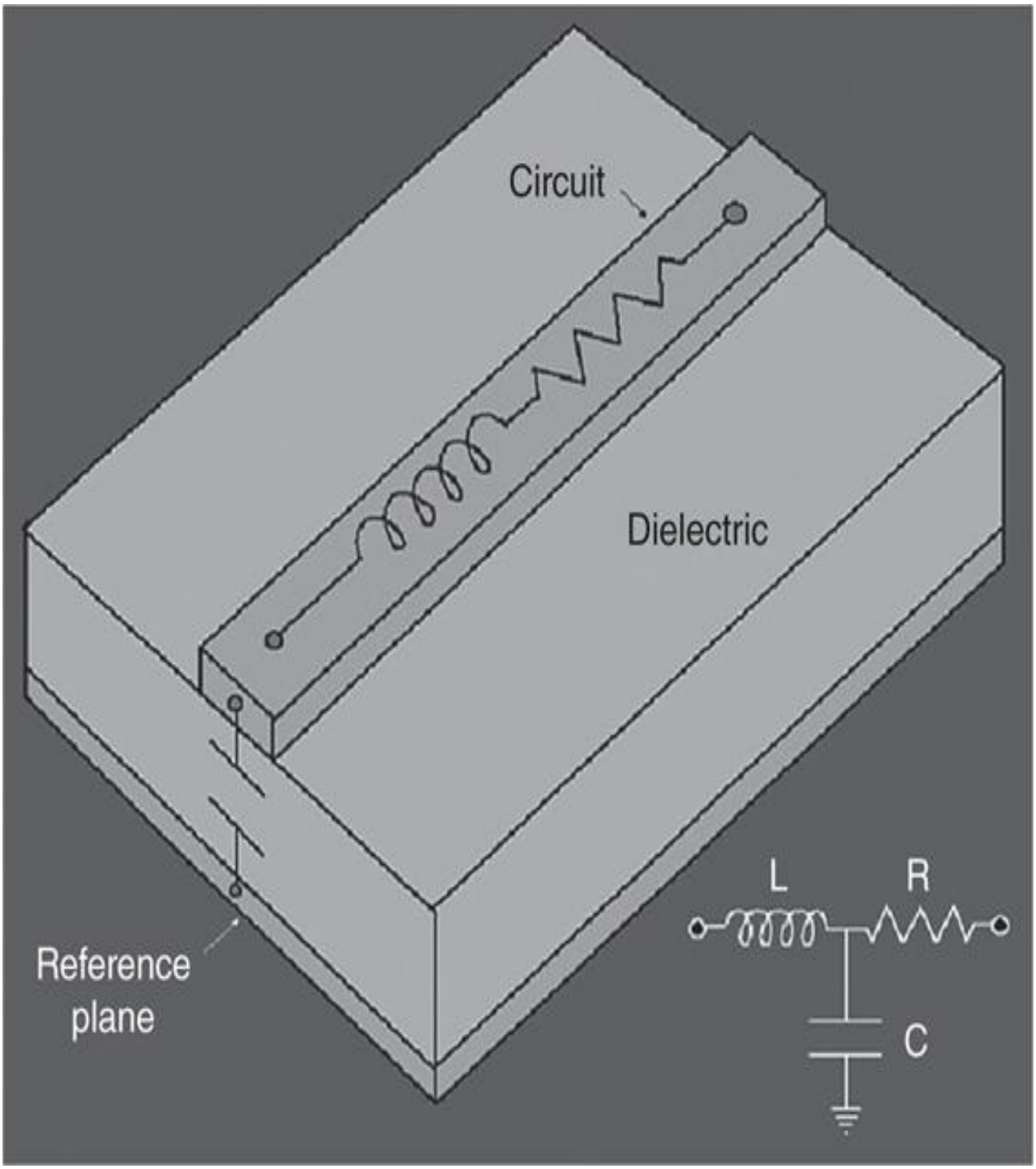


FIGURE 53.17 Impedance diagram of a PCB. (*Courtesy of Microtek Laboratories*.)

53.11.2 Internally Observable Imperfections

These are imperfections where evaluation from the outside of the PCB is not possible. They require the preparation of a microsection in order to view and evaluate conformance. Proper preparation of a PCB microsection requires a great deal of skill. The method of sample removal, the microsection materials used and the grinding/polishing techniques all significantly affect the ability to produce a microsection that will reveal and not hide imperfections. The basic methodology for the preparation of microsections can be found in IPC Test Methods 2.1.1 and 2.1.1.2, but numerous papers and articles have been written on the art of the microsectional preparation process. The use of test coupons to perform microsections is optimal due to the fact that internal layer connections do not always appear for every layer in holes on the PCB, whereas they always appear in a properly designed microsection test coupon. See Fig. 53.18 for a microsection of a multilayer PTH.

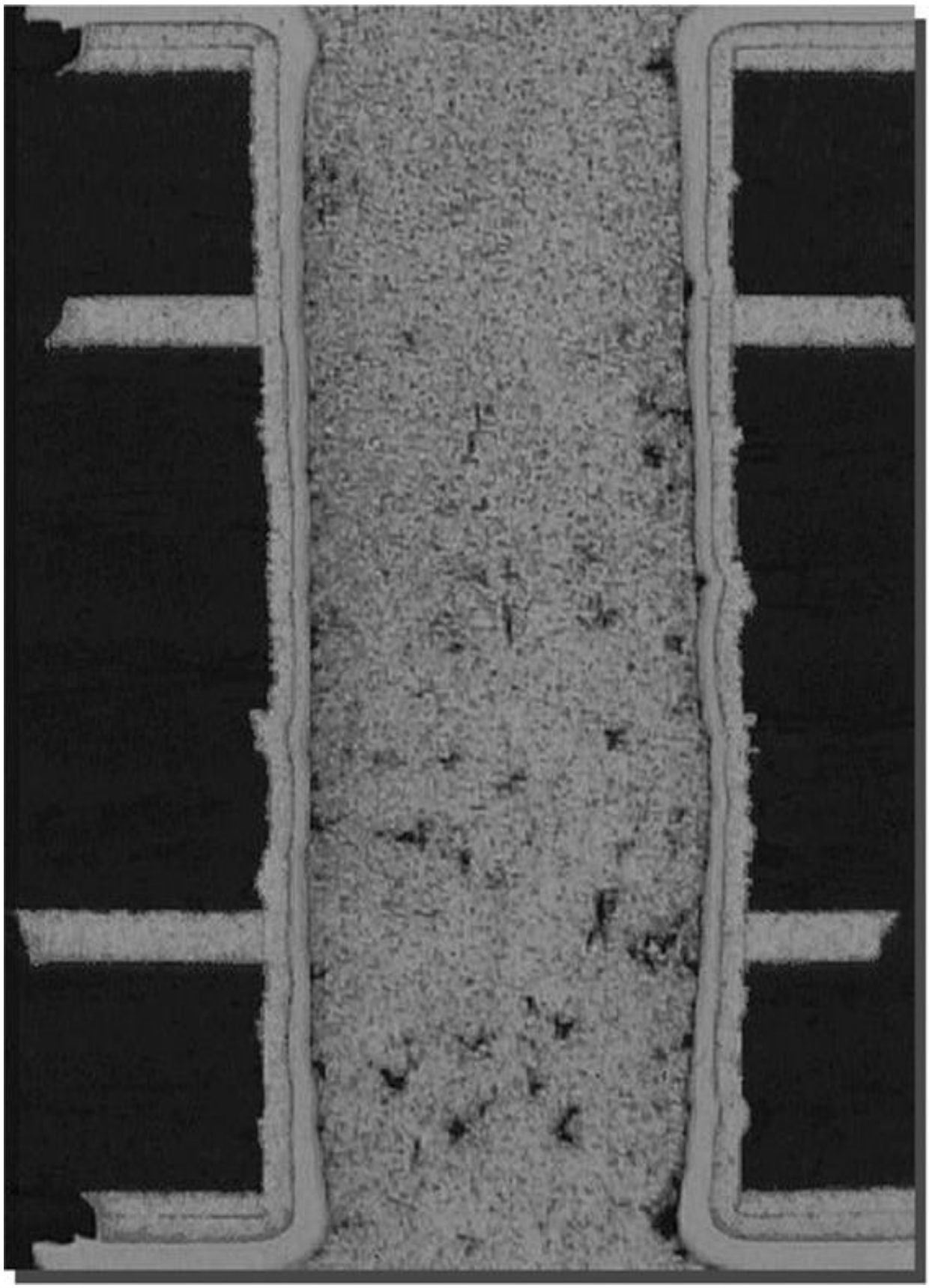


FIGURE 53.18 Vertical PTH microsection of a multilayer PCB. (*Courtesy of Microtek Laboratories*.)

53.11.2.1 Microsectioning. Samples for microsectioning are removed from the PCB or test coupon. The removed specimen should contain at least three of the smallest holes in a line that will allow microsectioning. Because shearing or punching of microsection samples from a PCB or coupon can result in creating failure mechanisms that are not truly present in the production PCB, the practice is not recommended. Routing or sawing microsection samples is the preferred method for sample removal. The samples should be mounted in a resin-based medium that does not produce too much heat during curing and does not shrink away from the surface of the holes being evaluated. Holes should be fully filled, as partially or nonfilled holes result in poor mount conditions, difficult sanding/polishing processes, and possibly erroneous thickness results. Examination under a microscope for internally observable attributes should be performed at 100× magnification. If it is not possible to determine whether the condition is acceptable, progressively higher magnifications should be used until accurate determination of acceptance is determined. Polishing vertical PTH cross sections to the center of the hole ±10 percent is critical. If the hole is polished less than or more than the center of the hole, the measured plating thickness will be artificially high. Horizontal plane, PTH cross sections are recommended as references for internal-layer interconnection quality and are prepared by grinding from the top down through the hole to the inspection area. See Fig. 53.19 for an example of a horizontal microsection.

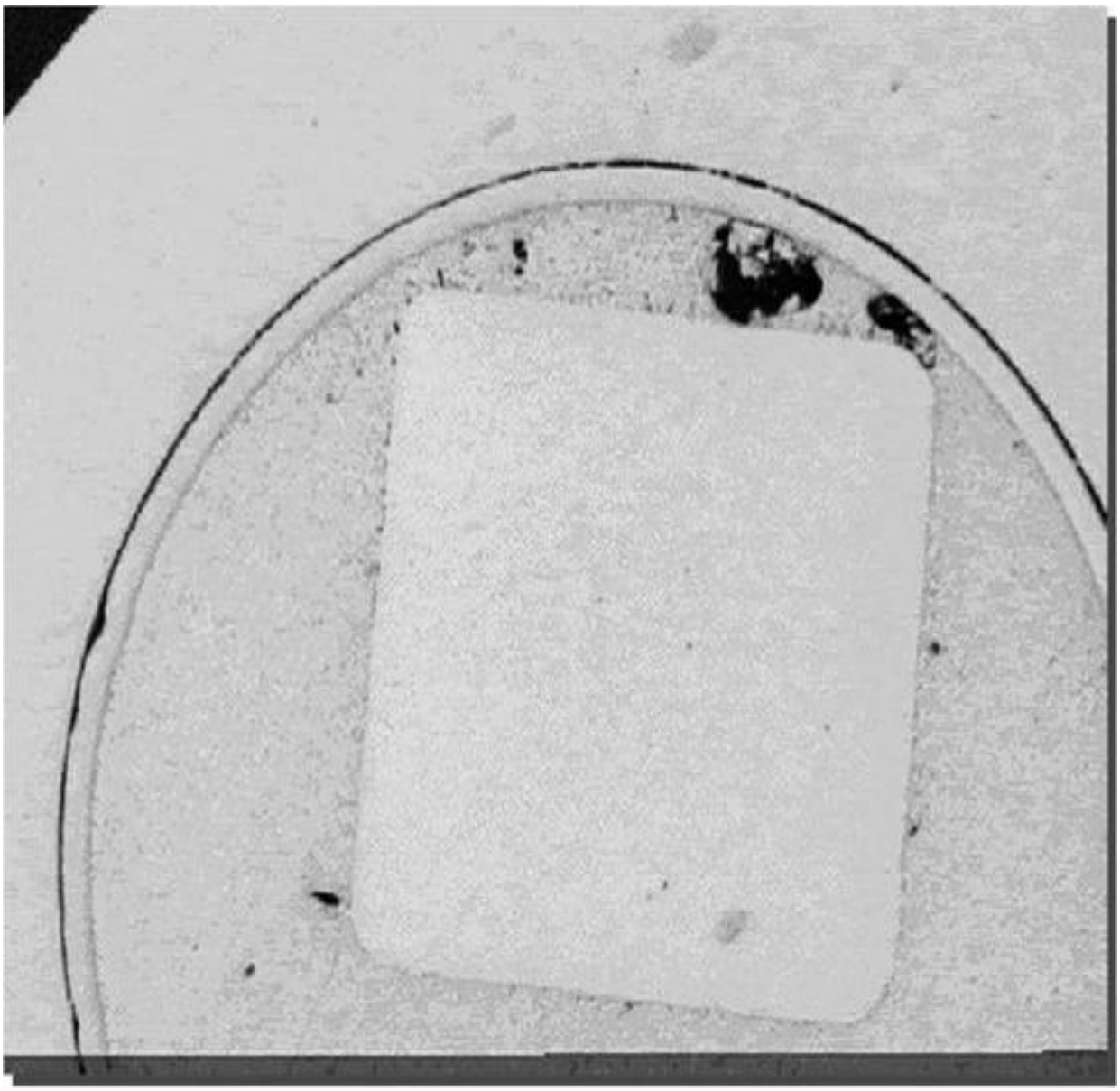


FIGURE 53.19 Example of interconnection separation in a horizontal microsection. (*Courtesy of Microtek Laboratories*.)

Although horizontal PTH cross sections are usually more accurate for plating thickness, interconnection separation, and annular ring measurements, they do not allow adequate inspection of other attributes such as voids, plating uniformity, adhesion, etchback, and nodules. Surface plating thickness measurements are taken from vertical cross sections of conductor areas. Microsection mounts are usually etched with an appropriate etchant to show grain boundaries

between the copper-clad foil and copper plating and to remove copper smearing introduced during the polishing process.

53.11.2.1.1 Thermal Stress Solder Float Test. The temperatures associated with component attachment and rework process expose PCBs to thermal and mechanical stress and may deform the PCB shape and cause premature degradation of the base material which in turn causes stress to the plating in the PTH. Thermal stress inspection is performed to predict the acceptability of the PCBs after the component attachment and rework process. PTH degradation, separation of platings or conductors, and base material delamination are induced or amplified by the thermal stress test. The PCB specimen is oven-conditioned to reduce moisture, placed in a dessicator on a ceramic plate to cool, fluxed, floated in a solder bath, and placed on an insulator to cool. Visual inspection for imperfections is followed by microsectioning of the PTHs and inspection under a microscope for integrity. Test coupons are typically used for thermal stress inspection.

53.11.2.2 Microsection Evaluation. The evaluation of internally observable attributes in the microsection consists of the following set of inspections:

- Subsurface attributes in the PCB material such as delamination, blistering, cracks, ground plane clearance, and layer-to-layer spacing
- Internal conductor attributes including over- and underetch, conductor cracks and voids, and foil thickness
- PTH attributes including size, annular ring, plating thickness, plating voids and nodules, plating cracks, resin smear, etchback, wicking, innerlayer (post) separation, and solder thickness

53.11.2.3 Subsurface Imperfections in the PCB Material

53.11.2.3.1 Base Material Voids after Thermal Stress. Heat from component attachment and rework process will transfer quickly through the copper holes and pads in a PCB to the base material in close proximity to the copper. This rapid heat movement can easily cause imperfections to occur in the base material and this area near the holes is exempted from evaluation for base material imperfections. This area is defined as the “thermal zone” and described in detail by IPC-A600. Outside this thermal zone, base material voids should not exceed 0.08 mm for rigid PCBs and 0.5 mm for flexible PCBs or flexible portions of rigid-flexible PCBs. Base material voids found in the same plane of flexible or rigid-flexible PCBs should not have a combined dimension greater than 0.5 mm (see Fig. 53.20).

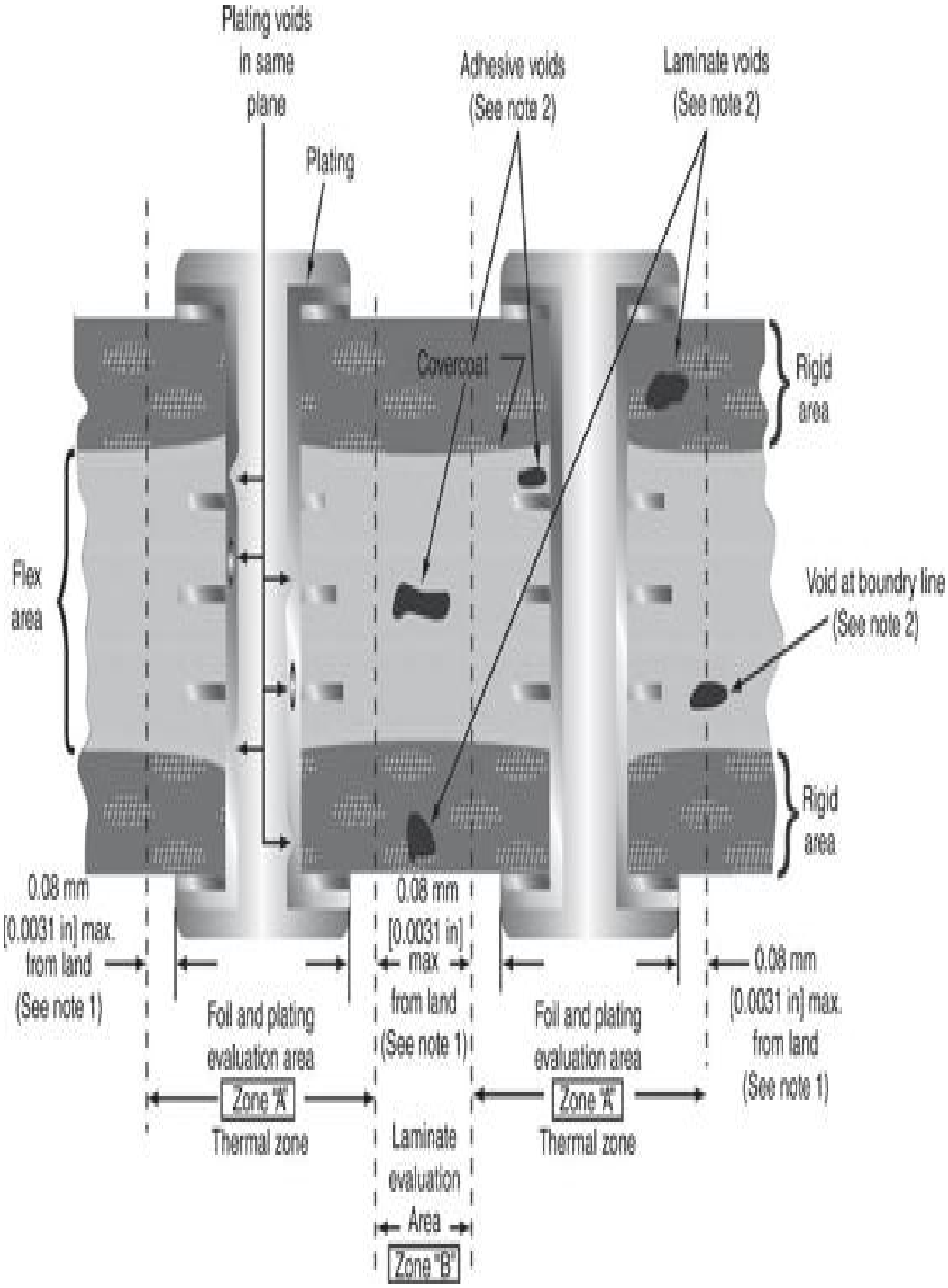

Plating voids
In same
plane
Adhesive voids
(See note 2)
Laminate voids
(See note 2)
Plating
Covercoat
Rigid
area
Flex
area
Void at boundry line
(See note 2)
Rigid
area
0.08 mm
[0.0031 in] max.
from land
(See note 1)
0.08 mm
[0.0031 in]
max
from land
(See note 1)
0.08 mm
[0.0031 in] max.
from land
(See note 1)
Foil and plating
evaluation area
Zone "A"
Thermal zone
Laminate
evaluation
Area
Zone "B"
Foil and plating
evaluation area
Zone "A"
Thermal zone

FIGURE 53.20 The thermal “A” zone in rigid/flex multilayer PCB. (*Courtesy of IPC*.)

53.11.2.3.2 Clearance of Holes to Power/Ground Planes. Electrical isolation between power/ground planes and nonconnected holes is necessary to ensure that shorting does not occur. This is especially true with holes that are nonplated and used for mounting of the PCB to a frame, as without proper clearance, the mounting hardware can cause shorting to the frame or between power and ground. The minimum distance of this clearance should reflect the minimum electrical spacing requirement on the procurement documentation (see Fig. 53.21).

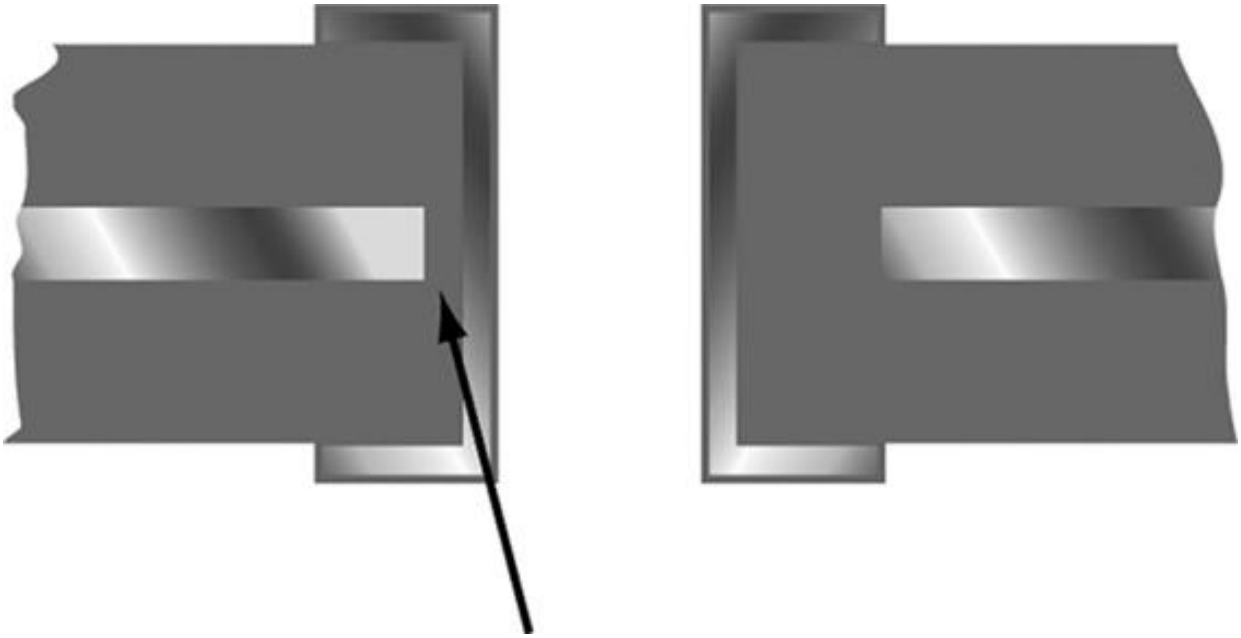


FIGURE 53.21 Clearance between PTH and power/ground plane. (*Courtesy of IPC*.)

53.11.2.3.3 Delamination and Blistering. Delamination or blistering observed in the microsection is a nonconforming condition and the inspection lot should be rescreened in accordance with the externally observable visual requirements for delamination and blistering set forth earlier in this chapter.

53.11.2.3.4 Resin Smear. Resin smear is transferred from the base material onto the surface or edge of the internal conductive pattern during the drilling process. Excessive heat generated during drilling softens the resin in holes and smears it over the exposed internal copper areas. This condition creates a resin insulator between the internal land and subsequent plating in the holes, and the result is open or poorly connected circuits. The imperfection is removed from the holes by chemical or plasma cleaning prior to metallization. Inspection for resin smear is per formed by viewing vertical and horizontal microsections of PTHs. And any evidence of it is nonconforming. (See Fig. 53.22 for an example of resin smear prior to etchback.)

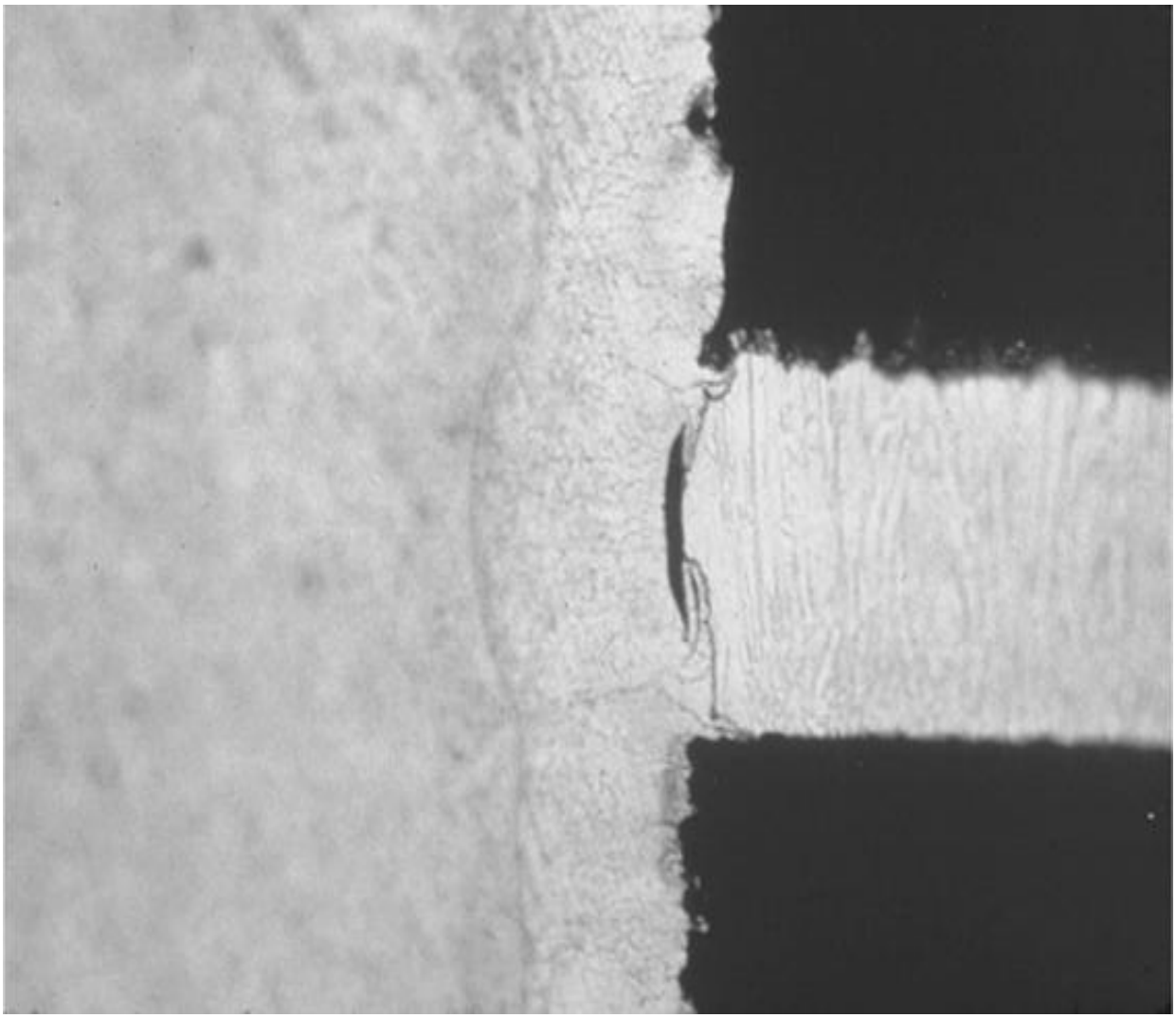


FIGURE 53.22 Resin smear in PTH, vertical microsection. (*Courtesy of IPC*.)

53.11.2.3.5 Etchback. Etchback is a process for the controlled, positive removal of nonmetallic materials from side walls of holes to a specified depth. It is used to remove resin smear and then to remove the reinforcement material laterally to expose additional internal conductor surfaces. The degree of etchback is critical to function. Too much etchback creates excessively rough hole side walls and causes weak PTH structures. Etchback requirements range between 0.0002 and 0.0031 in (0.005 and 0.08 mm). The degree of etchback is measured by evaluating vertical PTH cross sections of multilayer PCBs and is determined

“effective” if at least one of the top or bottom surfaces of the internal conductor is attached to the plated copper on both visible sides of every conductor layer. (See Fig. 53.23 for an example of acceptable etchback for all classes.)

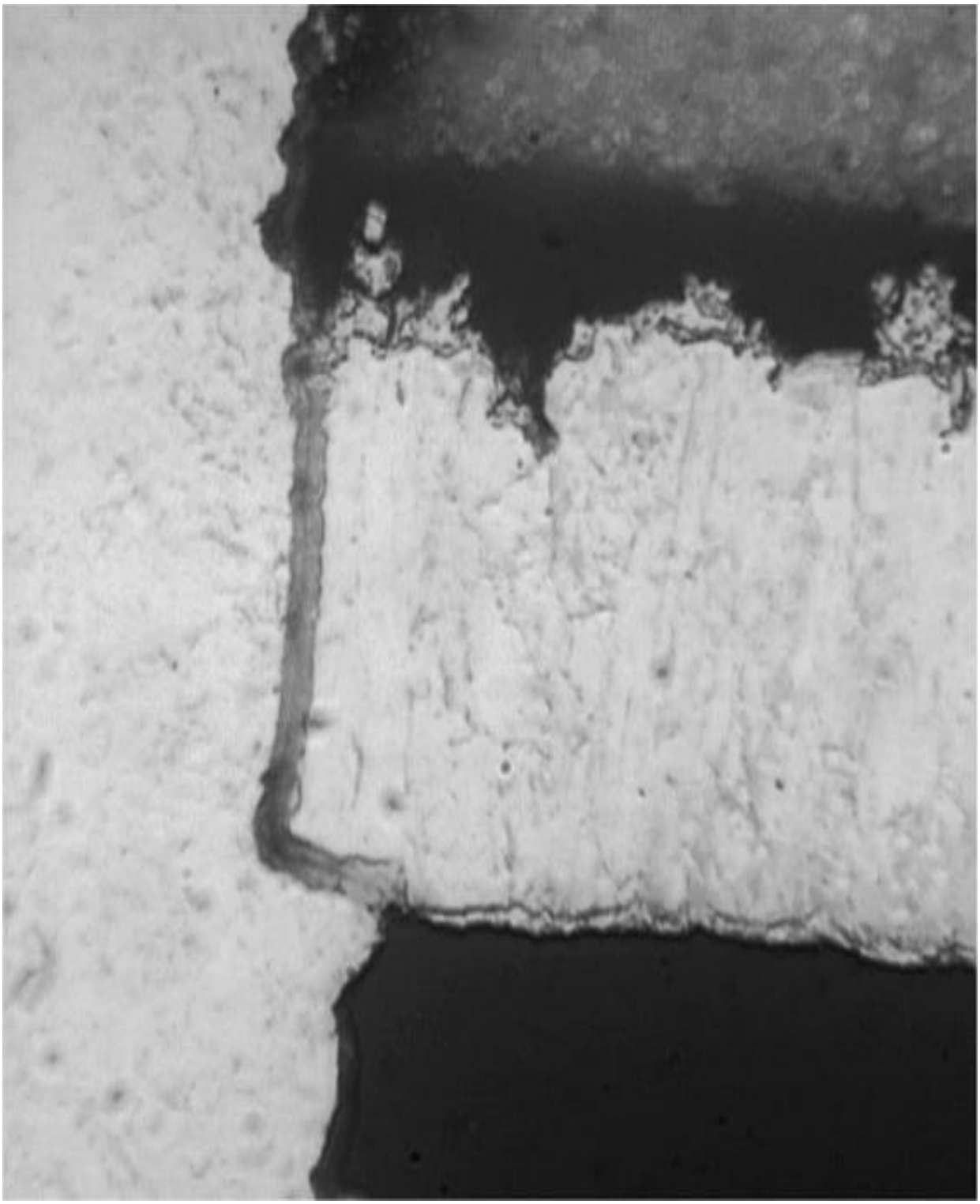


FIGURE 53.23 Effective etchback in PTH, vertical microsection. (*Courtesy of IPC*.)

53.11.2.3.6 Negative Etchback. This is a condition where the internal copper conductors rather than the insulating material in the hole have been laterally removed. This condition is not allowed when positive etchback is required. In all other cases, negative etchback should be minimal or nonexistent.

53.11.2.3.7 Layer-to-Layer Spacing. The minimum spacing between two consecutive layers in the PCB is determined by drawing an imaginary plane between the two most eccentric points of each of the two layers in the field of view and measuring the distance between these two planes. (See Fig. 53.24 for an example of minimum dielectric thickness between layers.)

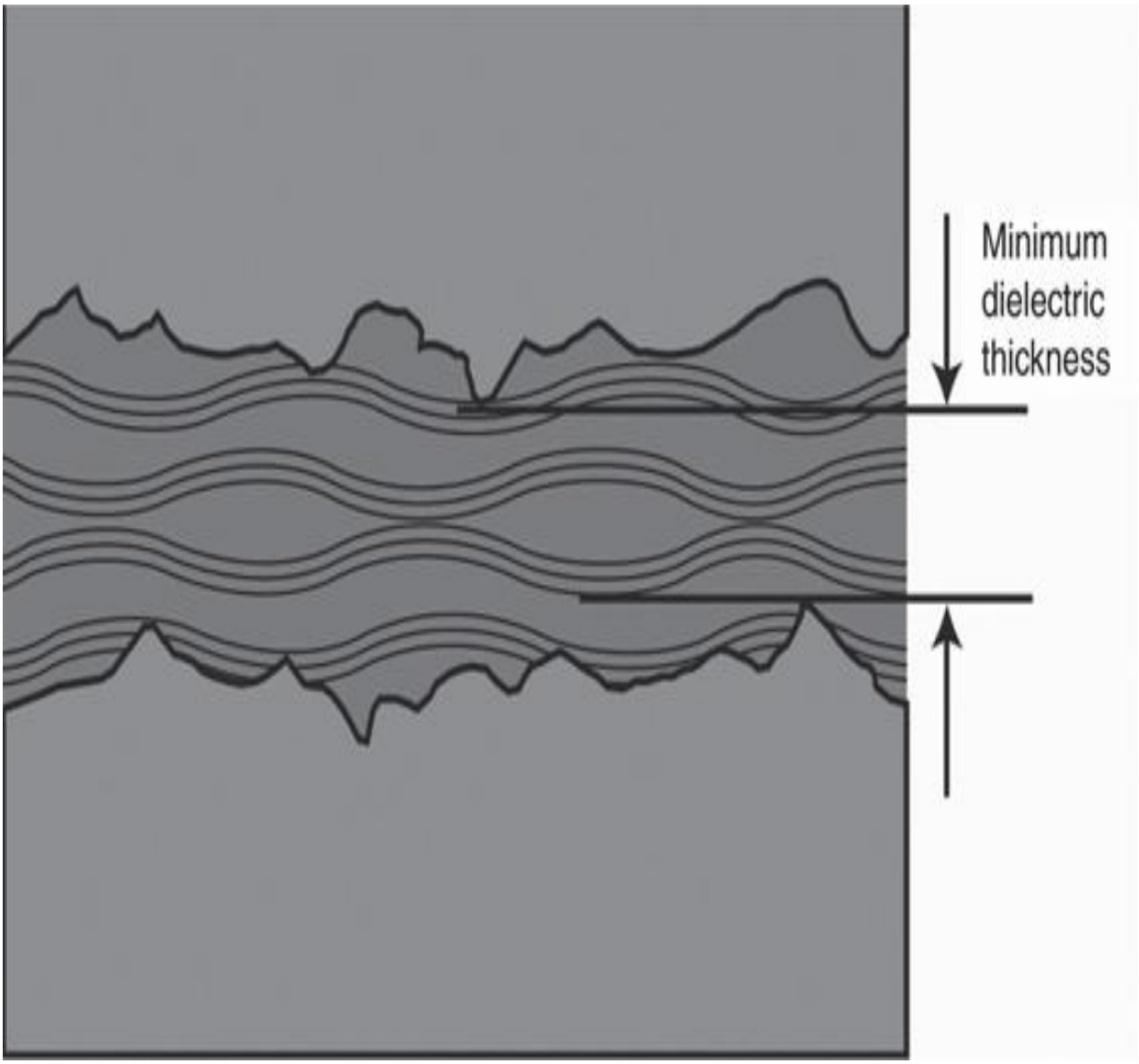


FIGURE 53.24 Layer-to-layer spacing, minimum dielectric thickness, vertical microsection. (*Courtesy of IPC*.)

53.11.2.4 Internal Conductor Imperfections in the Microsection. In theory, circuits should be rectangular. Circuits are usually designed with this rectangular shape in mind. In practice, circuits are trapezoidal. Depending on how the circuit is formed, this shape could be close to a rectangle or differ significantly from it. The further from a rectangle that the shape is, the less volume the circuit has to conduct current compared to a corresponding rectangular circuit. Terms like *outgrowth, undercut, overhang*, and *etch factor*

are used to define the attributes of these shapes (see Figs. 53.25 and 53.6).

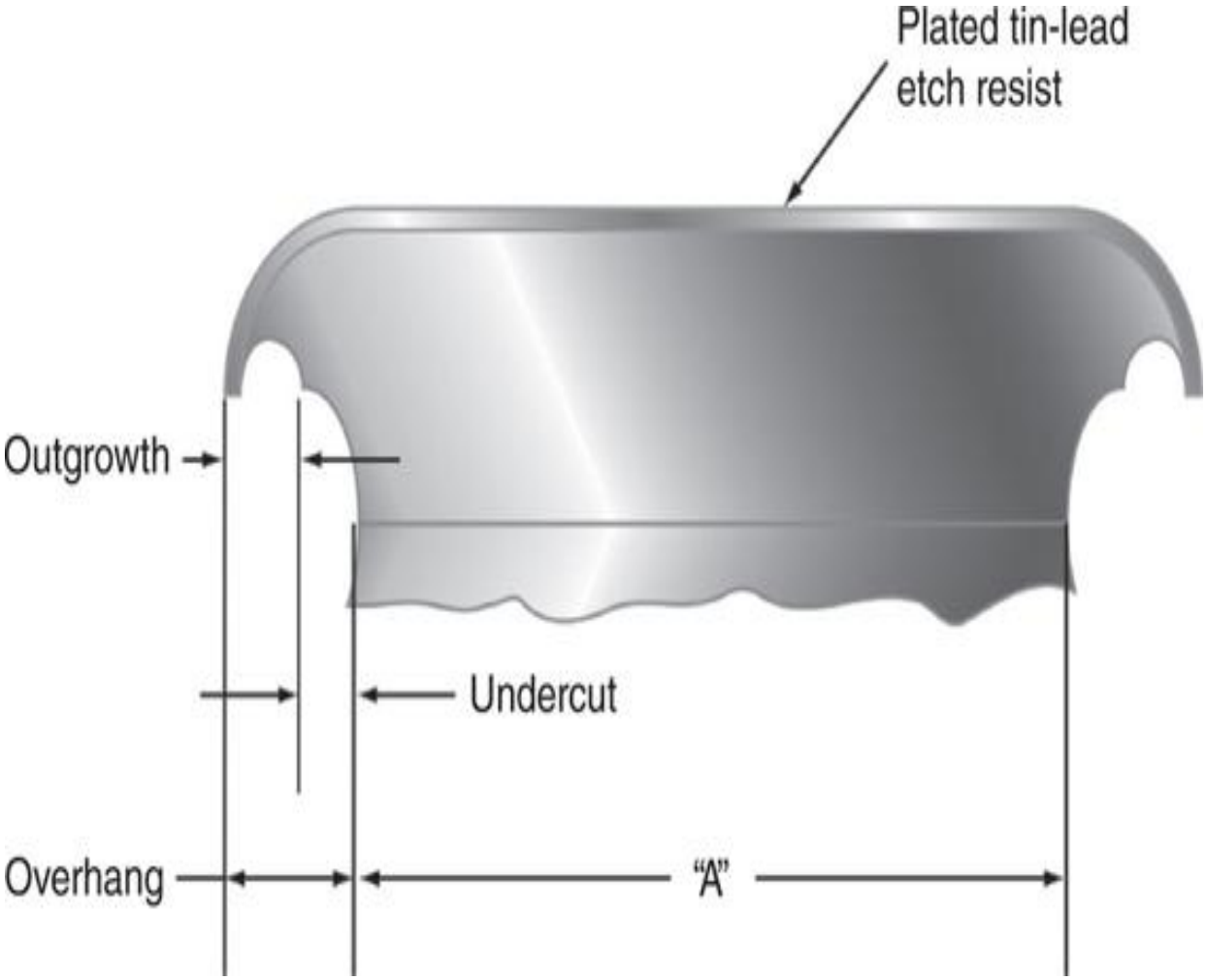


FIGURE 53.25 Circuit geometry. (*Courtesy of IPC*.)

53.11.2.4.1 Conductor Width. This attribute is measured at the widest point of the circuit in the microsection. The procurement documentation should state the minimum allowable width (see Fig. 53.6).

53.11.2.4.2 Conductor Thickness. Conductor thickness depends on the thickness of the base foil used and the additional plating added to the surface during any plating processes. Allowances for expected reduction of both foil and plating thicknesses due to manufacturing processes must be

considered. A detailed table of these minimum acceptable conductor thicknesses with allowances for manufacturing processing can be found in IPC-A-600.

53.11.2.5 PTH Imperfections. Nothing affects the function of the PCB more than imperfections in the PTH. These imperfections are usually not observable from the surface, and microsectional sampling of holes is limited to almost statistical insignificance. Despite this, evaluations of the microsection represent one of the most important evaluations that can be done on a PCB.

53.11.2.5.1 Annular Ring. Minimum internal annular ring is evaluated on the internal copper land that exhibits the shortest distance between its outer edge and where it ends in or at the plating in the hole. It should be noted that a microsection identifies layer shift in only one direction and that microsections in both *x* and *y* directions should be evaluated to better determine the actual shift that may be present. Horizontal sections from the top of the PCB down to the layer in question give a 360° view of the pad and can be used to exactly identify minimum annular ring and layer shift. The procurement documentation should specify the requirement for minimum annular ring (see Fig. 53.26), and in cases where the allowable annular ring is zero or “breakout,” the breakout cannot be allowed in the area where the circuit enters the pad (conductor-to-land junction area), as this will reduce the circuit’s current-carrying capacity.

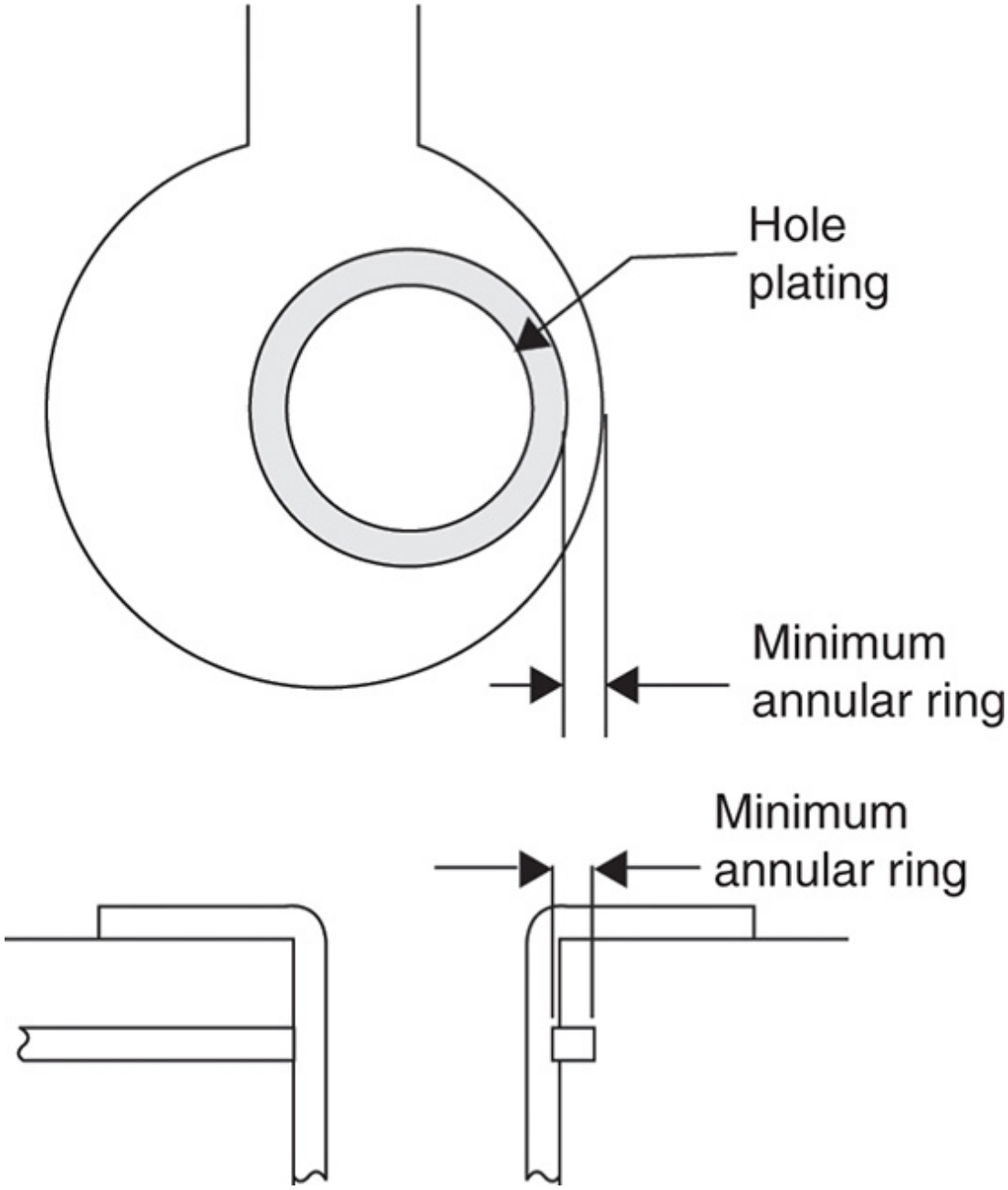


FIGURE 53.26 Internal annular ring measurement, horizontal and vertical microsection (does not include plating). (*Courtesy of IPC*.)

53.11.2.5.2 Lifted Lands. Lifted lands on the PCB surface prior to thermal stress are not allowed and if found, the entire inspection lot should be reevaluated to the externally observable visual requirements for lifted lands described earlier in this chapter. Lifted lands after thermal stress are allowed.

53.11.2.5.3 Cracks. Cracks in the foils and platings in the microsection are broken into the following six categories (see Fig. 53.27):

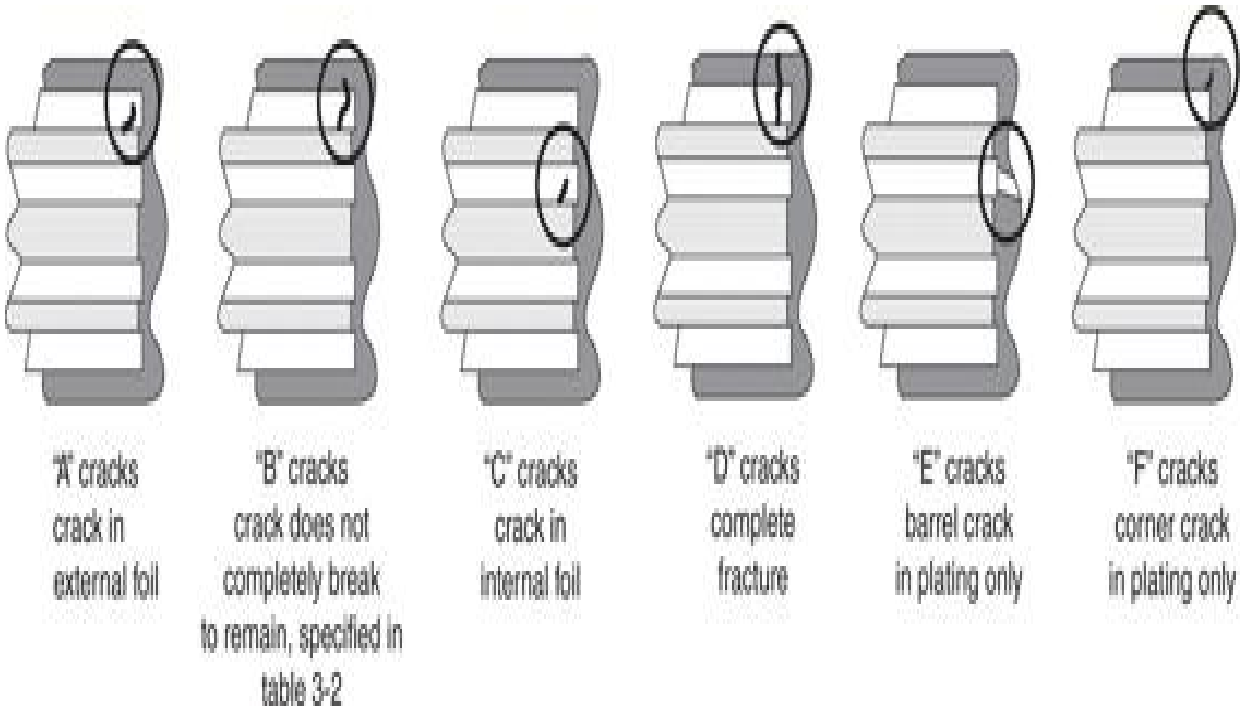


FIGURE 53.27 Types of cracks in the PTH, vertical microsection. (*Courtesy of IPC*.)

"A" type cracks occur in the external foil. They do not extend into the plating and are acceptable for all classes of PCBs.

"B" type cracks occur in the external foil. They go completely through the foil and extend into, but not completely through, the plating and are acceptable only for Class 1 PCBs.

"C" type cracks occur in the internal foil and are nonconforming for all classes of PCBs.

"D" type cracks completely penetrate the external foil and plating and are nonconforming for all classes of PCBs.

"E" type cracks occur in the barrel plating of the hole. They are nonconforming for all classes of PCBs.

"F" type cracks occur in the corner of the plating of the hole and are nonconforming for all classes of PCBs.

53.11.2.5.4 Plating Nodules. Plating nodules should not reduce the PTH diameter below the minimum requirement specified in the procurement documentation.

53.11.2.5.5 Plating Thickness. Plating thickness should be measured at three places in the plated hole and averaged. The absolute minimum plating thickness observed should also be recorded. The minimum plating thickness requirements for the three-area average along with the absolute minimum thickness observed are defined in IPC-6012 (see Fig. 53.28).

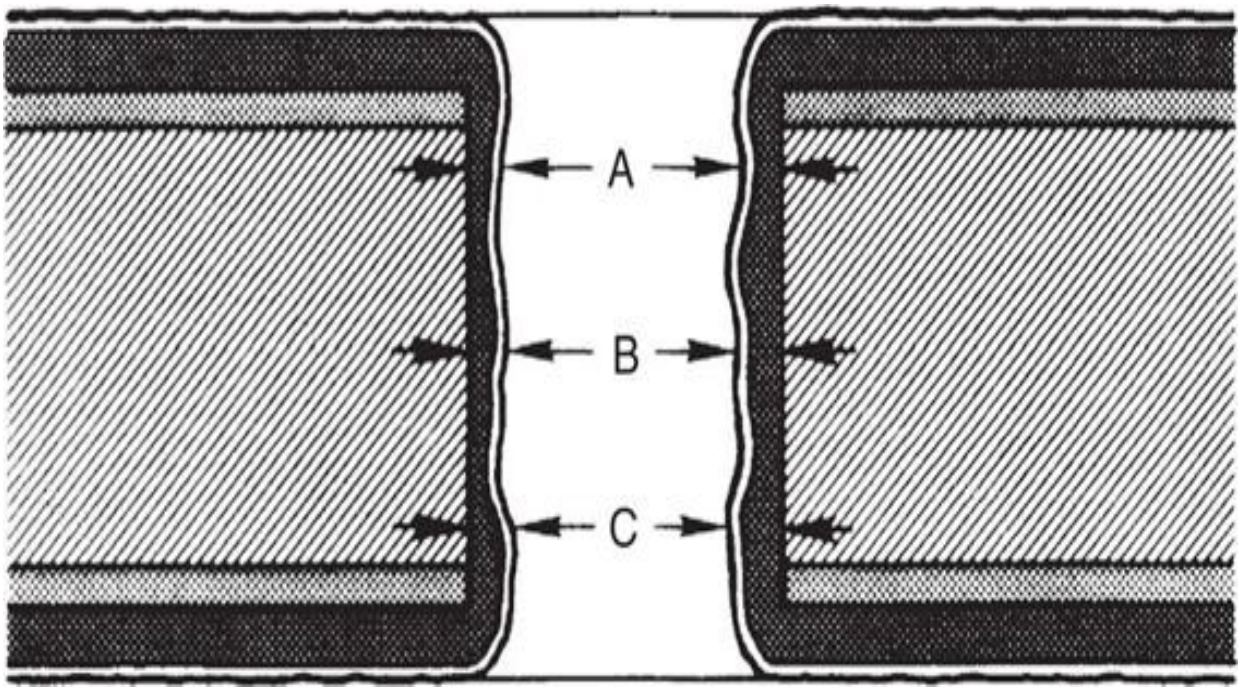


FIGURE 53.28 Measurement of plating thickness in PTH, vertical microsection. (*Courtesy Sandia Laboratories*.)

53.11.2.5.6 Plating Voids. When found in the microsection, plating voids should be limited to one per

microsection. No void should span more than 5 percent of the PCB thickness or be present at the interface of internal copper foil to the plating.

53.11.2.5.7 Solder Resist Thickness. When the procurement documentation specifies this thickness, it should be measured at the thinnest area observed between the copper and the surface of the solder resist. This is usually at the corner of the copper trace.

53.11.2.5.8 Wicking. During the drilling and hole cleaning process, glass fibers from the base material can be removed inward from the hole surface. During the copper-plating process, the copper will follow this glass removal topography, creating pockets of plating that extend laterally from the hole into the base material. This wicking can significantly reduce the electrical conductor spacing between holes or between holes and internal circuits. The maximum allowances for wicking can be found in IPC-A-600 (see Fig. 53.29).

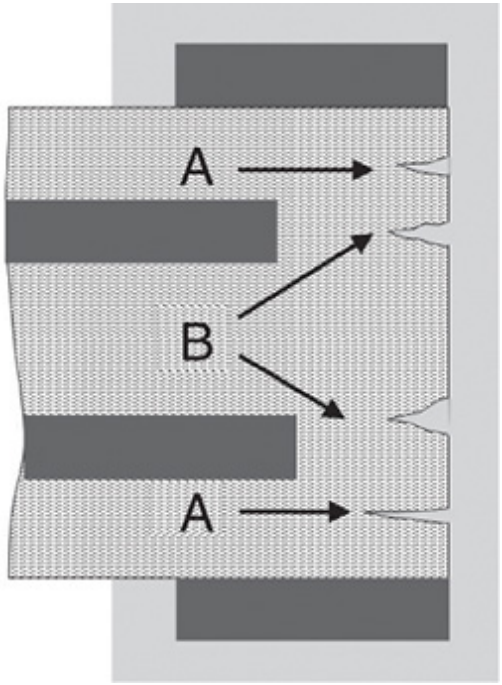


FIGURE 53.29 Wicking, vertical microsection. (*Courtesy of IPC*.)

53.11.2.5.9 Interconnection Separation. This is defined as the separation between the internal copper foil and the copper plating in the hole. It is also sometimes referred to as post separation. Any evidence of this imperfection in the microsection makes the associated PCBs nonconforming. This imperfection is a severe issue that will likely reduce the service life of the PCB (see Fig. 53.30).

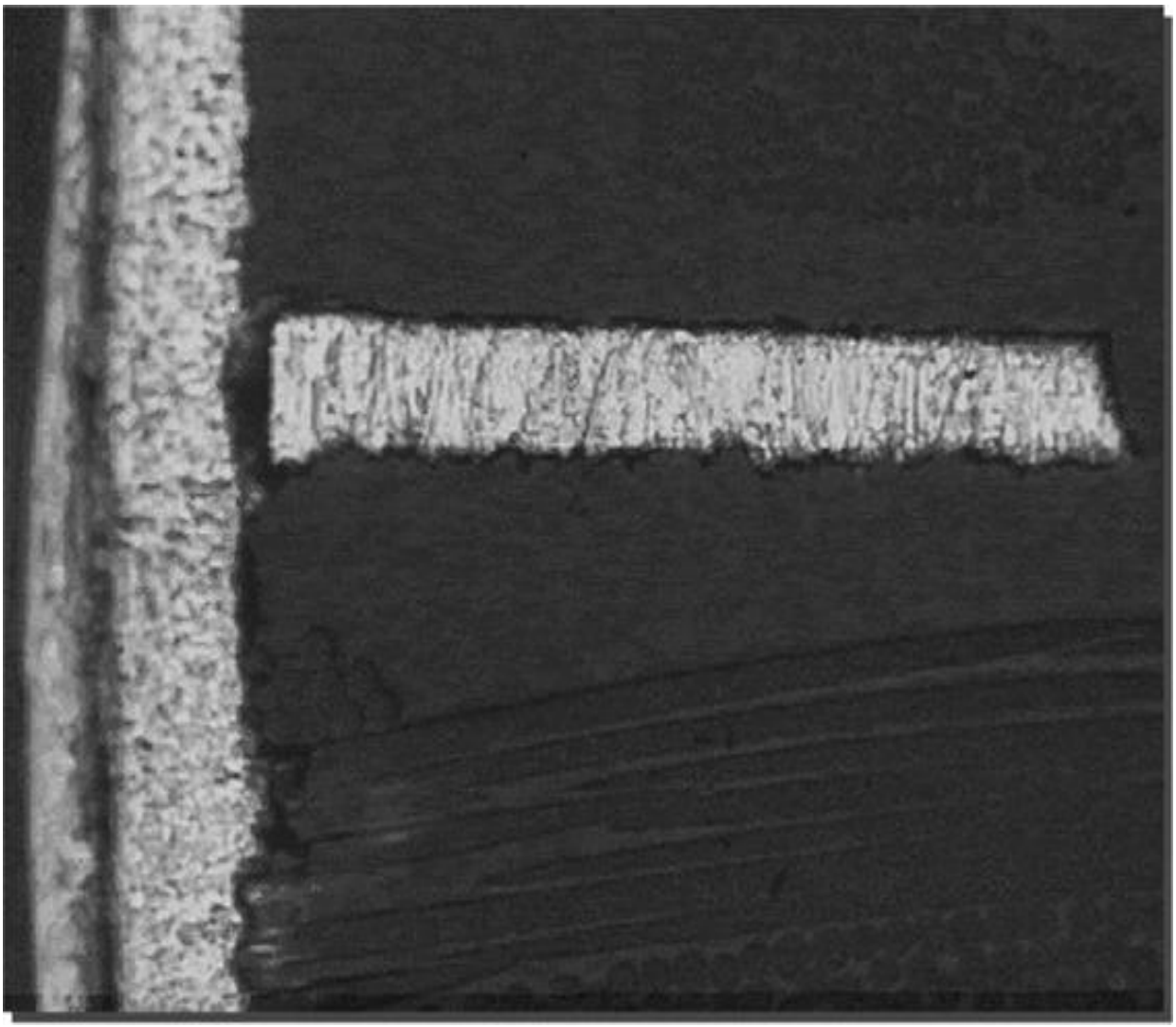


FIGURE 53.30 Interconnection separation, vertical microsection. (*Courtesy of Microtek Laboratories*.)

53.11.2.5.10 Material Fill of Blind and Buried Vias. When blind or buried vias are present in a PCB, it is important that

they be microsectioned and evaluated in addition to any through holes evaluated. Buried vias are typically filled with resin, and this resin should fill a minimum of 60 percent of each buried via.

53.11.2.5.11 Cap Plating over Filled Holes. For via holes that are designed to be filled and subsequently plated over, there should not be any plating voids exposing the via fill material. The copper wrap plating of the via structure which is located below the cap plating shall be continuous from the filled plated hole onto the annular ring and needs to extend at least 25 µm from the edge of the drilled via (see Fig. 53.31) and have a minimum thickness which is specified by IPC-A-600.

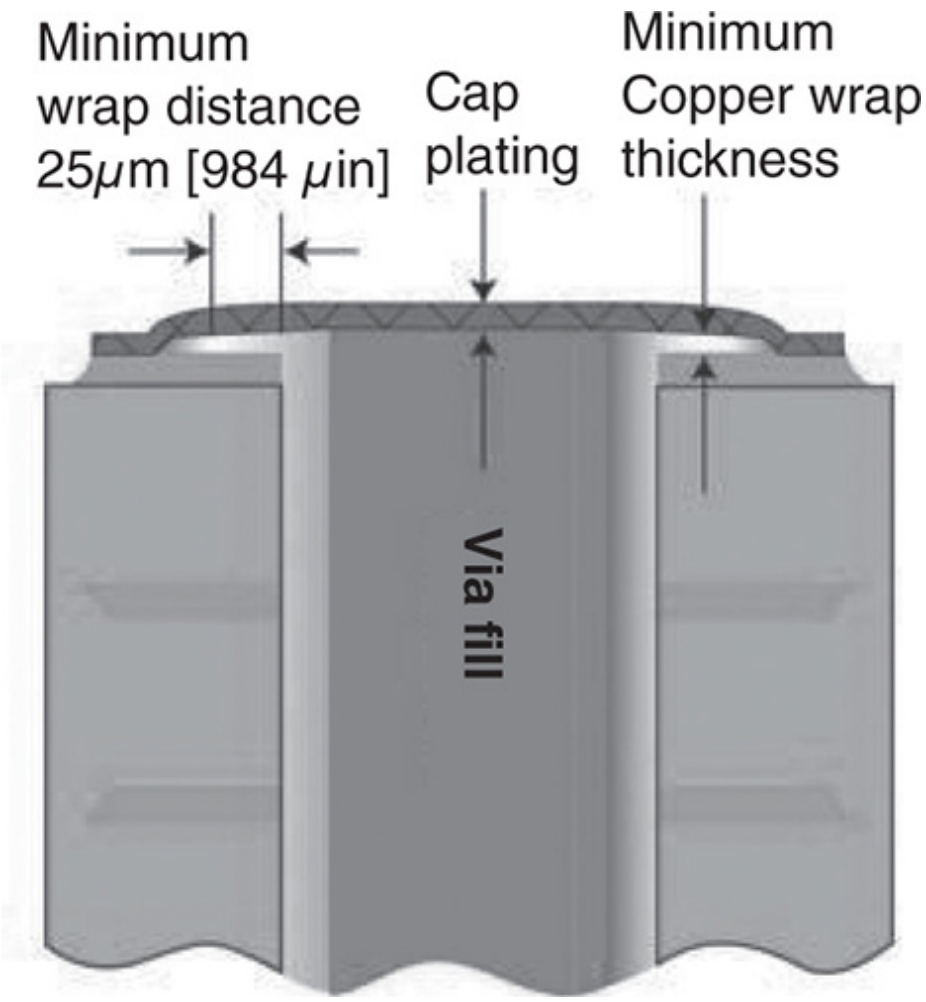


FIGURE 53.31 Surface copper wrap measurement (*applicable to all filled PTHs*).

53.12 RELIABILITY INSPECTION USING ACCELERATED ENVIRONMENTAL EXPOSURE

Reliability inspection consists of performing specific tests to ensure that the PCB will function under the influence of the climatic and/or mechanical forces to which it will be subjected during its expected lifetime. Environmental tests are performed on preproduction PCBs or specifically designed test coupons to verify design adequacy and manufacturing process control. Specific tests are sometimes specified as part of the PCB acceptance procedure to expose a prospective failure situation. Specific environmental testing, as part of the acceptance procedure, is prevalent in high-reliability products where long term life is desirable or necessary. Prior to performing reliability inspection, it is recommended that a simulation of the cycles required for component attachment and rework be performed as a preconditioning. Test results then relate to the actual condition of the PCB after the assembly process. Specific test methods for performing these tests can be found in IPC-TM-650.

53.12.1 Thermal Shock

The thermal shock test is particularly efficient in identifying (1) PCB designs with areas of high mechanical stress and (2) the resistance of the PCB to exposure of high- and low temperature extremes. This test is periodically required in IPC-6012 for product acceptance and is also used for PCB

supplier qualification inspection. A thermal shock is induced on a PCB by exposure to severe and rapid differences in temperature. The test is usually performed by transferring the PCB from one temperature extreme (e.g., 125°C) to the other (e.g., −65°C) rapidly, usually in less than 2 min. A resistance difference in excess of 10 percent between the stabilized hot side measurement at the 1st and 100th cycles is considered nonconforming, but requirements in the thousands of cycles are sometimes specified for high-reliability PCBs. The thermal shock test can produce cracking of plating in the holes and base material delamination (refer to IPC-TM-650, method 2.6.7.2, for the procedure). Note that continuous electrical monitoring during thermal shock cycling will detect intermittent electrical circuit anomalies that may not be detected with periodic measurement techniques. Intermittent circuit anomalies usually occur at the high-temperature extreme.

53.12.2 Surface Insulation Resistance

Surface insulation resistance (SIR) testing evaluates the electrical resistance between two surface electrical conductors separated by dielectric material. This test detects the bulk conductivity and electrical leakage through surface electrolytic contaminants when the samples are exposed to a high-humidity environment that allows the contaminates to become mobile on the surface. The test conditions are a relative humidity of 85 to 92 percent at a temperature range of 35 to 45°C without the use of an electrical forcing potential during the exposure. (See Fig. 53.32 for example of a SIR test pattern.)

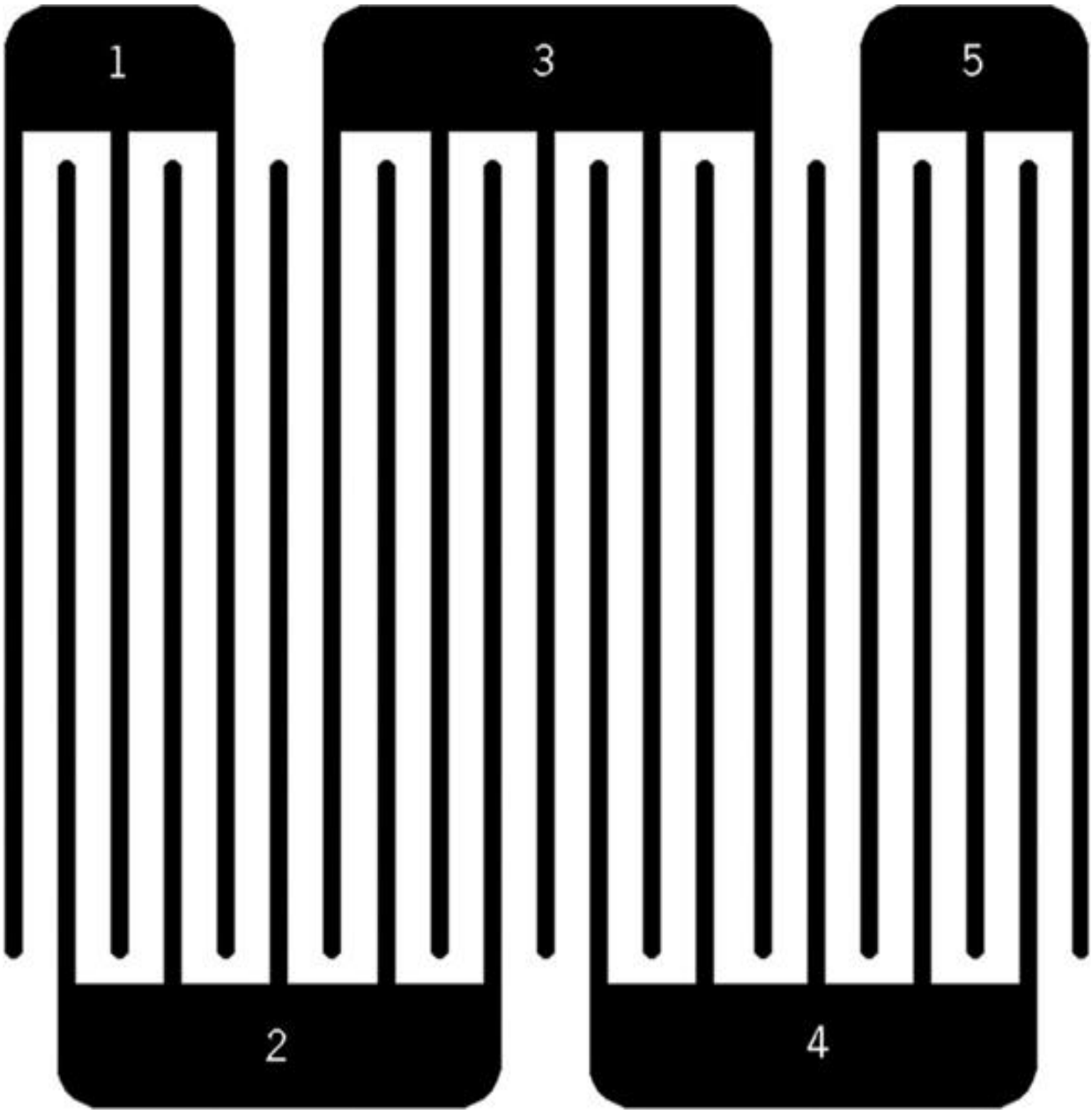


FIGURE 53.32 Basic SIR test pattern. (*Courtesy of Microtek Laboratories*.)

53.12.3 Moisture and Insulation Resistance

This is an accelerated method of testing the PCB for the deteriorative effects of condensing high humidity and heat conditions typical of tropical environments. The test

conditions are a relative humidity of 90 to 98 percent at a cycling temperature range going back and forth from 25 to 65°C with a forcing voltage potential of 10 to 100 VDC applied to the test circuit(s). After the required test cycles are completed, the PCB is subjected to insulation resistance testing. Test specimens should exhibit no blistering, measling, warp, or delamination after the MIR test.

53.12.4 Dielectric Withstanding Voltage

This test is used to verify that the component part can operate safely at its rated voltage and withstand momentary overpotentials due to switching, surges, and similar phenomena. It also serves to determine whether insulating materials and spacings on the PCB are adequate. The test is performed on either an actual PCB or a test coupon. Voltage is applied between mutually insulated conductors on the specimen or between insulated conductors and power/ground planes. The voltage is increased at a uniform rate until the specified value is reached. The voltage is held for 30 s at the specified value and then reduced at a uniform rate. Visual examination of the specimen is performed during the test for evidence of flashover or breakdown between contacts. The test can be either destructive or nondestructive, depending on the degree of overpotential used.

53.12.5 Electrochemical Migration and Conductive Anodic Filament Testing

Electrochemical migration (ECM) and conductive anodic filament (CAF) tests are intended to detect the growth of conductive metal filaments on or in a PCB under the influence of a direct current (DC) voltage bias. This filament growth may occur at either an external or internal surface or interface between dissimilar materials. Growth of the metal filaments is by electrolytic deposition from a solution containing metal ions that are dissolved from the anode in the test circuit and then transported by the electric field toward the cathode. ECM comes in two forms. First are surface dendrites, which form on the internal or external surfaces between the two oppositely charged electrodes. The second form of ECM is CAF, in which filaments form along the interface between the glass-fiber reinforcement and resin system between a hole and another hole or conductor along the path of the fiber. ECM and CAF testing is done at a relative humidity of 85 to 92 percent at a steady-state temperature range between 35 and 85°C using forcing potentials ranging from 10 to 100 V DC during the test depending on the end product application.

CHAPTER 54

ACCEPTABILITY OF PRINTED CIRCUIT BOARD ASSEMBLIES

Mel Parrish

STI Electronics, Inc., Madison, Alabama

54.1 UNDERSTANDING CUSTOMER REQUIREMENTS

When determining the acceptance criteria to use in building or manufacturing a printed circuit board assembly (PCBA), one first and foremost must look at the contract between the supplier and the purchaser of the product. Always determine the needs and/or wants of the customer through contractual communications or, less formally, by talking to the customer if a contract is not detailed enough or does not even exist.

In some situations, contracts are not the norm, such as for consumer electronics built for retail sale or captive production efforts where the customer and producer are one and the same. In these cases, the company must determine the level of quality desired based on company culture and goodwill, reputation for quality products, and the desired life

cycle of the product. Consequences for an unintended or unexpected failure may be a significant driver in this consideration. An electronic medical device used for life support has much greater consequence attached to continued successful operation than a disposable electronic device such as a toy that is intended to be discarded after a short term of use. Additionally, the intended operational environment may have an even greater impact on what should be expected for the acceptability of production. Consider that a product used for military operations such as space travel, arctic conditions, or tropical environments is subjected to much harsher conditions than an office product that sits on a desk in a temperature-controlled environment where the temperature will not vary more than 10°F during its expected life cycle. The range of these expectations is significant and is a paramount consideration for what can be defined as acceptable or nonconforming.

Most standards that define acceptability have roots traceable to the various Department of Defense (DoD) military standards established in the 1960s and 1970s. The advent of complex electronics systems required a standardized approach to acceptability based on lessons learned through testing and product failure analysis that was accomplished by laboratory or research activities. The resulting definitions for acceptance became very restrictive, and although the requirements were initially intended only for harsh environment exposure or products that have a significant consequence for failure, they were used successfully to increase performance of all soldered electronic assemblies. Most commercial production did not share the need for critical continued performance and the accompanying significant impact on production cost. Despite an effort to approach acceptance from a cost-prevention or value-added viewpoint, the military standards are no longer maintained and the DoD research sources for maintaining technology currency were eliminated. The demise of military

standards allowed the industry to develop consensus standards for soldering processes and also acceptability. Undoubtedly the most significant of these is IPC-A-610, which creates varying levels of acceptability for broad application ranging from medical and military products to disposable electronics. Not all products need to survive after an explosion or operate for 30 years without interruption.

Each company should decide whether to build its product to an industry standard such as IPC-A-610, “Acceptability of Electronic Assemblies,” or develop its own workmanship manual that would closely match IPC-A-610 levels for quality. The advantage of adopting a common standard is the universal understanding of expectations it supports between the customer and producer and thus circumvents the need for lengthy negotiations over individual interests. Where individual custom standards are used, the production processes must be adjusted for each customer or product as it is addressed for production. On the other hand, common standards can be transitioned from one project to the next without significant change. The use of a common standard can take into account the perspective of collective experiences of the consensus participants who are involved in the development. Creating an individual standard can also be a rather daunting and expensive task that can provide limited return without the broad application to bear the cost. In any case, the workmanship manual decision must support the company’s objectives to achieve customer expectations for quality with regard to its product.

Detailed specifications may be called out in a drawing or contract, or there may not be any documentation that identifies requirements. In the latter case, the recommendation is to revert to accepted industry standards or an internal quality requirement such as a workmanship manual.

54.1.1 Lead-Free Soldering

Any acceptance criteria decision should define lead-free materials and processes acceptability. Until the advent of the European Union's adoption of the Directive on Restriction of Hazardous Substances (RoHS), which went into effect in July 2006, all electronic design and also production control was based on the precedent that soldering processes would be accomplished with tin-lead (SnPb) soldering materials. Tin-lead solder has specific properties that were instrumental in the multitude of component attachment methods that evolved for production of electronics. Had the solder of choice over the years been other than tin-lead, many of these common configurations might have evolved differently. The current reality is that component designs intended for tin-lead attachments are being soldered with various lead-free alloys, driven by the requirement to remove lead from electronic products. Acceptability for these designs has not changed that much, as reflected in current IPC acceptability standards. The attachments still need to have solder that flows over the connection interface surfaces, forms a fillet, and wets to the constituents that form the attachment. What has changed significantly is the surface appearance of the resulting solder connection. Most lead-free solders exhibit surface roughness that would cause concern for those accustomed to the normal appearance of tin-lead. In fact, if solder finishes created by tin-lead had the same surface appearance, they would have rightly been considered contaminated or overheated. The current IPC-A-610 standard provides a side-by-side contrast of similar solder connections accomplished with both tin-lead and lead-free solder alloys for appearance perspectives.

Outside of the considerations of acceptability appearance, there are additional concerns for materials compatibility issues and adverse properties such as hot tear, tin whisker, tin pest, accelerated and increased process temperature

exposure, and others. These considerations should be developed elsewhere in this reference.

This section presents common possibilities for acceptance criteria.

54.1.2 Military, Space, and Commercial Specifications

Reference to these types of specifications is common in the applicable markets. No great amount of detail will be discussed; however, they are all worthy of some discussion since they can provide a great deal of insight into the rationale of “product acceptability” and its origin.

54.1.2.1 Military Specifications. Military specifications have been widely accepted for use in many markets outside of their intended military products. The one with the most relevance to workmanship or acceptability criteria at the assembly level was MIL-STD-2000, a unified standard created from several individual services and production standards. It was created to combine the various requirements into a single standard to make it easier for military contractors to implement a single performance requirement. Many lower-level supporting specifications for components, designs, materials, and printed circuit boards (PCBs) were part of the family of documents to support performance and acceptance requirements as a package. Each specification was designed to be compatible with the eventual success of the end product. In an effort to increase understanding by all of the parties involved, and to ease compliance issues, the services provided training and certification at various locations throughout the country, and even at some international locations. The typical training audience often included customer representatives as well as producers. The title of MIL-STD-2000 was “Standard Requirements for Soldered

Electrical and Electronic Assemblies.” However, all of the military soldering requirements standards, including MIL-STD-2000, have been rescinded for future production through DoD acquisition reform initiatives. Nevertheless, some products still use the requirements because they have been adopted internationally and because they provide relative benefit for the product’s specific industry segment.

MIL-STD-2000 was an extensive document that defined the nonconformance conditions that required disposition as rework, repair, or use as is. This of course required some action by the manufacturer to evaluate a given defect anomaly and make a decision regarding its impact on the form, fit, or function of the intended use. It also allowed some level of customer involvement concerning these decisions if the contract prescribed it. MIL-STD-2000 also limited the assembly materials for a manufacturer in terms of the solder alloys, flux activity levels, cleanliness, conformal coating, solder mask, and their acceptance conditions, either through a flow down to a supporting specification or internal requirements. Any deviation from standardized process and materials as specified in these documents required qualification and/or customer consent before use. However, the document allowed flexible contractual application dependent upon the product demands for performance. “General Requirements” for standard production were much less stringent than “Detail Requirements,” which were used for demanding performance or consequence products such as those intended for missile or space applications. Contracts were required to specify “Detail Requirements” before they were imposed; otherwise, only the “General Requirements” were required as a default. The intent of flexible requirements was to allow the use of a single standard for everything from complex weapon systems to office equipment. Unfortunately, they were not commonly applied that way, and the overly stringent requirements originally intended for critical systems were

attached to applications such as office or communication products that did not benefit from the more stringent and costly production effort.

Solder connection characteristics for both plated through-hole and surface-mount devices were defined by solder finish, fractures, voids, solder coverage and quantity, and wetting and filleting. The PCB requirements after assembly were detailed in terms of conductor finish and condition, conductor separation from the board, cleanliness of the assembly, weave exposure, delamination, measles, haloing, and bow and twist. In addition, part markings were expected to remain legible even after assembly processing.

If specifically imposed by individual contract, the services provided, through established training resources, traceable training and certification of the people making decisions. This training provided a cadre of qualified instructors who in turn could train people for their company or organization. Its interesting that prior to elimination of these schools, the majority of students attending the certification-training program were from commercial production companies with no contractual performance for DoD. In addition to establishing product acceptance criteria, the specification also detailed methods for process control and defect reduction to be used in assembly. One hundred percent inspection was required unless specific conditions were met, so that sample-based inspection might be used with confidence.

As a result of elimination of the various military standards, most DoD and termed high-reliability production is defined through contractual implementation of the commercial IPC equivalent standards, such as J-STD-001, and IPC-A-610.

54.1.2.2 Space Production Requirements. Standards associated with space applications have significantly different purposes than process control documents commonly used for large-volume production electronics. For

the purpose of space applications, there is seldom a large enough production volume to benefit from process development, and each individual product must be acceptable based on the environments experienced with space applications. These could be quite similar to the initial developments for DoD acceptance discussed earlier since they also involved space considerations. Current space application standards have evolved from NHB 5300 through to NASA-STD-8739.3, “Soldered Electrical Connections.” Additionally, the space user community has created a space addendum to the commercial standard J-STD-001 for the opportunity to employ consensus standards used by many of their contractors for various other programs. The addendum modifies requirements to a degree consistent with space interests and in effect makes the performance and acceptance requirements similar to that of the NASA-generated standard.

54.1.2.3 J-STD-001 and IPC-A-610 Industry Standards. These consensus industry association standards are widely recognized as the most common standards for requirements and workmanship for PCB assemblies, both nationally and internationally. They allow flexible definition of requirements based on three distinct classes of product, and the acceptability and performance requirements change based upon the contract provisions for the individual product as these classes are applied.

54.1.2.3.1 J-STD-001, “Requirements for Soldered Electrical and Electronic Assemblies.” Since “acquisition reform” and elimination of the very commonly adopted military standards, IPC standards have filled the resulting void and have also brought with them additional valuable practices and perspectives from commercial producers. J-STD-001, “Requirements for Soldered Electrical and Electronic Assemblies,” was first released in April 1992 as a modification of the previous IPC-S-815, which had limited

application, likely due to the competition from contractually imposed military and other industry-unique standards that were available to the users and managers at the time. IPC-S-815 had very similar criteria to that of the military baseline or “General Requirements” discussed earlier.

The resulting J-STD-001 defines three levels of electronic assemblies based on the intended end-item use. The three classifications were established to reflect differences in consequences of failure, harshness of the operating environment, and expected term of operation. The three classes are summarized as follows:

- *CLASS 1: General Electronic Products* This class includes products suitable for applications where the major requirement is function of the completed assembly.
- *CLASS 2: Dedicated Service Electronic Products* Class 2 includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.
- *CLASS 3: High-Performance Electronic Products* These include products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required. Examples include life support or other critical systems.

J-STD-001 addresses many of the same subjects as MIL-STD-2000, and in most cases for Class 1 and 2 production, the requirements are again similar to the “General Requirements” of the previous standards. The Class 3 requirements for the majority of the subject areas are similar to MIL-STD-2000, “Detail Requirements.” Since the deactivation of MIL-STD-2000 and the associated revisions, many contract performance requirements have been

transitioned to this document and family of IPC standards. As with the predecessor documents, it should be recognized that a successful soldering process requires consistent materials and the ability to select the materials for a given process that will perform well in combination with compatibility for the application. As with acceptability, users may have the flexibility to establish their own requirements for these materials, but it would be difficult to find suppliers willing to create materials qualifications for anything other than a standardized definition. The following discussion provides a brief overview of the “family of standardized criteria” for materials associated with acceptable production standards.

54.1.2.3.2 J-STD-002, “Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Wires.” This standard prescribes the recommended test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wire, stranded wire, lugs, and tabs.

Solderability evaluations are made to verify that the solderability of component leads and terminations meets the requirements established in J-STD-002 and that subsequent storage has had limited adverse effect on the ability to solder components to an interconnect. Determination of solderability can be made at the time of manufacture, at receipt of the components by the user, or just prior to assembly and soldering.

Similar to J-STD-001, J-STD-002 has its origin with military standards, which in this case was MIL-STD-202, Method 208. It defines standardized methods of evaluating the ability of a surface to accept solder and in addition defines the durability of the solderable surface with three categories of product and related conditioning to determine the product performance before soldering. Category 1 is the least demanding performance, where the product would be used soon after testing, and Category 3 is applied where the

product may be stored for extended periods of time before soldering. The intent is to identify solderability problems before the expense of production is added or the production schedule is delayed while waiting for solderable replacement parts.

For a more detailed discussion of solderability and the related issues, refer to Sec. 54.5.

54.1.2.3.3 J-STD-003, "Solderability Tests for Printed Boards." J-STD- 003, "Solderability Tests for Printed Boards," was released in April 1992 to complement the requirements of J-STD-001. This standard prescribes the recommended test methods, defect definitions, and illustrations for assessing the solderability of printed board surface conductors, attachment lands, and plated-through holes.

The solderability determination is made to verify that the PCB fabrication processes and subsequent storage have had no adverse effect on the solderability of those portions of the PCB intended to be soldered. This is determined by evaluation of the solderability specimen portion of a board, or representative coupon, that has been processed as part of the panel of boards and subsequently removed for testing per the method selected.

The objective of the solderability test methods described in J-STD-003 is to determine the ability of printed board surface conductors, attachment lands, and plated-through holes to wet easily with solder and to withstand the rigors of the PCB assembly processes.

For a more detailed discussion of solderability issues, refer to Sec. 54.5.

54.1.2.3.4 J-STD-004, "Requirements for Soldering Fluxes." J-STD-004 prescribes general requirements for the classification and testing of soldering fluxes for high-quality interconnections. This standard is a flux characterization, quality control, and procurement document for solder flux and flux-containing material.

This standard defines the classification of soldering materials through specifications of test methods and inspection criteria. These materials include liquid flux, paste flux, solderpaste flux, solder-preform flux, and flux-cored solder. It is not the intent of this standard to exclude any acceptable flux or soldering aid material; however, these materials must produce the desired electrical and metallurgical interconnection.

54.1.2.3.5 J-STD-005, "Requirements for Soldering Paste." This standard prescribes general requirements for the characterization and testing of the solderpastes used to make high-quality electronic interconnections.

54.1.2.3.6 J-STD-006, "Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications." This standard prescribes the nomenclature, requirements, and test methods for electronic grade solder alloys; for fluxed and non-fluxed bar, ribbon, and powder solders, for electronic soldering applications; and for "special" electronic grade solders.

54.1.2.3.7 Other Standards. There are many standards that comprise the necessary content for successful production practices that lead to acceptability. Each represents an element of the foundation that supports a complete and successful production effort. One example is moisture susceptibility and the procedures to ensure that the components are not damaged by popcorning during reflow. J-STD-020 and J-STD-033 provide classification and control for moisture-sensitive components. Others, such as IPC-CC-830, "Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies," deal with material acceptability of conformal coating. Each of the elements is important and should be considered as a package for overall acceptability.

Many of the material specifications reference test methods. Rather than include the actual test method with the publication of the specification, the IPC posts them on its

website, where they can be easily accessed and kept current without extensive revision of the various reference standards. This prevents possible conflict with outdated procedures. Criteria for the acceptance levels, however, are provided by reference standards such as J-STD-001, J-STD-004, and so on.

54.1.2.4 IPC-A-610, "Acceptability of Electronic Assemblies". Many companies use IPC-A-610, "Acceptability of Electronic Assemblies," as the standalone workmanship standard for their products. J-STD-001 establishes the requirements for soldering processes, whereas IPC-A-610 depicts the pictorial acceptability criteria for production, including soldering as identified in the J-STD-001 document. IPC-A-610 also addresses additional, broad criteria to define handling and mechanical workmanship requirements, among others. A large percentage of the acceptability criteria defined in this chapter is that which is illustrated in the IPC-A-610 standard.

The popularity of IPC-A-610 is apparent considering that it is available in many different languages and used throughout the world as the acceptance reference of choice for electronics.

The IPC-A-610 standard describes the acceptability criteria for quality electronic assemblies. It does not define process requirements, although the methods used must produce a completed solder joint conforming to the acceptability requirements as defined. Consistent with other IPC standards, the IPC-A-610 document details the acceptance criteria for each of three classes.

The three classes of product allow flexible application of the conditions for which the standard provides acceptance criteria. The customer should provide the inspector with the intended class for acceptability before the product is considered for acceptance. The three classes are 1, 2, and 3

and are the equivalents of the definitions provided by J-STD-001.

In addition, this standard discusses and visually illustrates degrees of compliance, such as “Target,” “Acceptable,” “Defect,” and “Process Indicator,” for each condition relative to the three classes of product. The importance of the condition varies with the expected performance of the class based on the preceding class criteria.

Acceptance definitions are summarized as:

- *Target* This condition is close to perfect or preferred; however, this desirable condition is not always achievable and may not be necessary to ensure reliability of the assembly in its service environment. Although this condition is not a requirement for performance based on the standard, it is provided to illustrate to users the desired condition that the creators of the criteria thought they should strive to achieve.
- *Acceptable* This condition, although not necessarily perfect, will maintain the integrity and reliability of the assembly in its service environment.
- *Defect* This condition may be insufficient to ensure the form, fit, or function of the assembly in its end-use environment. Defect conditions need to be dispositioned by the manufacturer based on design, service, and customer requirements. Disposition may be to rework, repair, scrap, or use as is. Repairing or using the assembly as is may require customer concurrence. A defect for Class 1 automatically implies a defect for Class 2 and 3. A defect for Class 2 implies a defect for Class 3.
- *Process indicator* A process indicator is a condition (not a defect) that identifies a characteristic that does not affect the form, fit, or function of a product. Such condition is a result of material, design, and/or operator- or machine-

related causes that create a condition that neither fully meets the acceptance criteria nor is a defect.

As established by the predecessor military standards, process indicators are not intended to be reworked or even dispositioned, and they can be included in product delivery without correction of the product. They are, however, not desirable and indicate the relative success of the process and materials; if the process or materials could lead to defect conditions, the process may need to be adjusted or corrected for future production. Process indicators should be monitored as part of the process control system. Should the number of process indicators indicate abnormal variation in the process or identify an undesirable trend, the process should be analyzed. This analysis may result in action to reduce the variation and improve yields before there is a defect trend that may require rework or scrap or, worst of all, result in customer dissatisfaction.

54.1.3 Workmanship Manuals

Many companies use a workmanship document of some sort to describe what the operations should achieve during production. IPC-A-610 is used frequently by manufacturing and also quality personnel to determine acceptable quality levels of their product. Some companies have also developed very good workmanship manuals for their own use, especially to cover unique or uncommon design requirements. If a need exists to develop a unique workmanship manual, then this manual should reflect the intended contract requirements. It is certainly desirable to use a manual already in existence since it can become extremely costly to develop your own, and because customer review is unnecessary since the customer should already be aware of the common requirements definition. If

minor changes are necessary to standard performance due to process, product or material limitations, they can often be addressed as a contractual waiver, addition, or exception to the standard definition.

54.2 HANDLING TO PROTECT THE PCBA

The handling of PCBs both before and after the soldering operation can be very important in terms of inducing possible damage to the board or contaminating the board such that subsequent operations are affected. There are three subjects that should be well thought out and controlled in an assembly operation for PCBAs: electrostatic discharge (ESD) protection, contamination prevention, and physical damage prevention.

54.2.1 ESD Protection

ESD is the rapid discharge of a voltage potential into an electronic assembly from a static energy source. The presence of a static discharge in the area of a sensitive device can damage the device even without actual contact. ESD-sensitive (ESDS) components found on the assembly and the amount of current generated by the discharge will determine whether immediate failure takes place. All types of ESD damage can be difficult to troubleshoot, but the most costly scenario is one in which the component is assembled and passes functional test only to fail later due to latent conditions resulting from ESD. This could cause the loss of a customer and even in some cases recall of the product.

Some electronic devices are more sensitive to electrostatic overstress (EOS) damage than others. The degree of such

sensitivity within a particular device is related directly to the manufacturing technology employed. The trend for electronic components is smaller size, wider band pass, and lower voltage. These are all contributors to the ESD protection problem and increased sensitivity of the component.

Where sensitive components are handled, protective measures must be taken to prevent component damage. Improper and careless handling accounts for a significant portion of ESD damage to components and assemblies. Before handling ESD-sensitive components, equipment should be carefully tested to ensure that it does not generate damage-causing spikes. The preferred workstation to be utilized in electronic assembly is shown in Fig. 54.1.

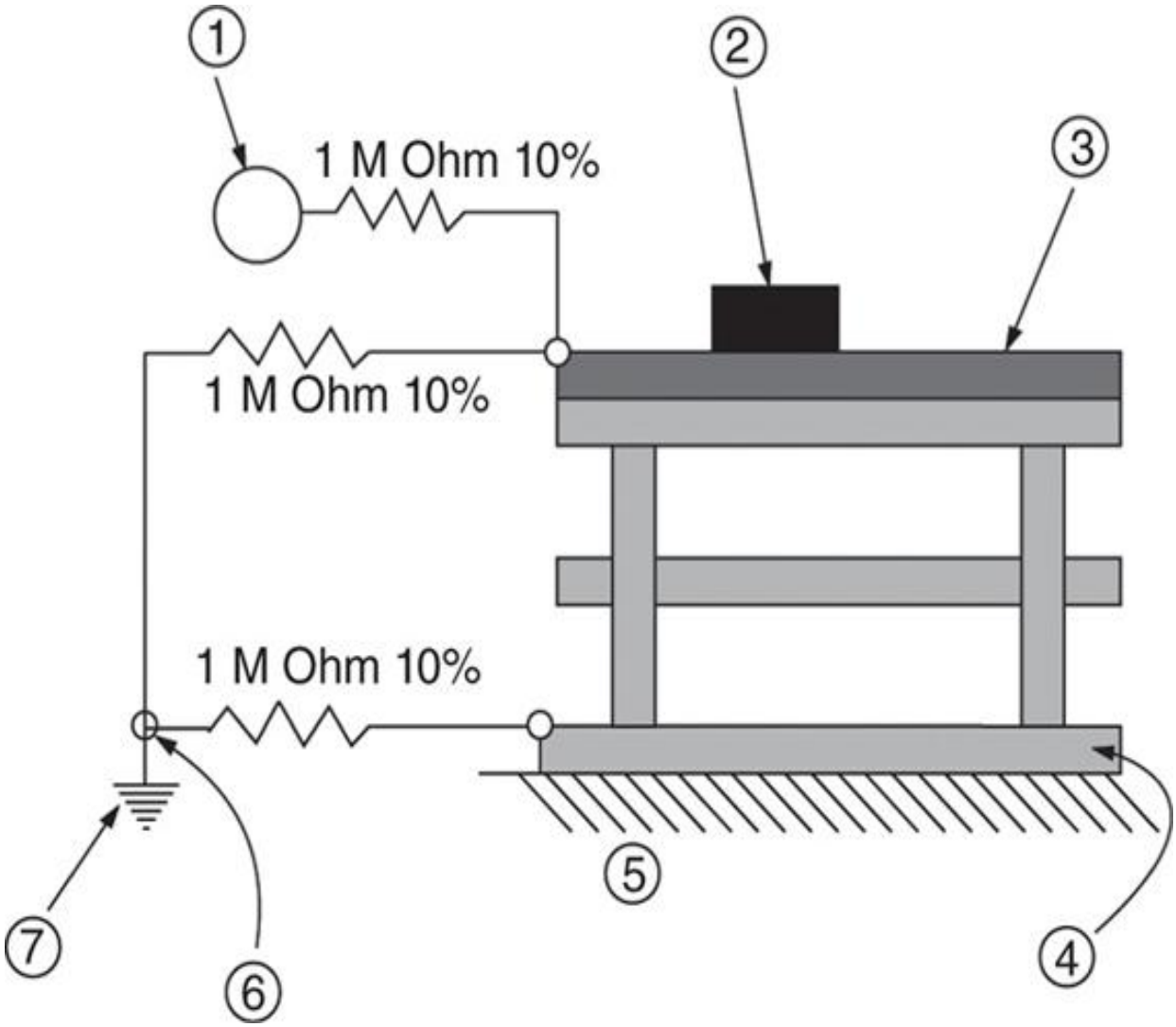


FIGURE 54.1 Target condition for EOS/ESD workstation (1) Personal wrist strap (2) EOS protective trays, shunts, etc. (3) EOS protective table top (4) EOS protective floor mat (5) Building floor (6) Common ground point (7) Ground. *(IPC)*

Static charges are created when nonconductive materials are separated. Destructive static charges are often induced on nearby conductors, such as human skin, and discharged as sparks passing between conductors. This can happen when a person having a static charge potential touches a PCBA. The electronic assembly can be damaged as the discharge passes through the conductive pattern to a static-sensitive component. Static discharges may be too low to be

felt by humans (less than 3,500 volts) and still damage ESD-sensitive components.

Sensitive components and assemblies must be enclosed in conductive, static-shielding bags, boxes, or wraps when not being worked on, unless otherwise protected. ESD-sensitive items must be removed from protective enclosures only at static dissipative or antistatic workstations.

For ESD safety, a path to ground must be provided for static charges that would otherwise discharge on a device or board assembly. Provisions are made for grounding the worker, preferably via a wrist strap or a heel strap, provided conductive flooring is used.

54.2.2 Contamination Prevention

The key to any contamination problem is to prevent it from happening. The cost of subsequent operations required to clean a product or rework a product is orders of magnitude more than any cost associated with preventing the contamination from occurring. These contaminants can cause soldering and solder mask or conformal coating problems. There are any number of possibilities for inducing contamination in an assembly environment, such as dirt, dust, machine oils, and process residues; however, in many cases, contamination is caused by the human body, specifically the salts and oils on the skin.

In a high percentage of assembly areas, good housekeeping will take care of contamination from the environment. It should be a common event on each shift to clean workstations, sweep floors, dust fixtures, empty trash, and so on. This not only prevents contamination, but it also helps to keep personnel morale at a higher level. After all, we all desire to work in a nice, clean environment. It will also serve as a positive point if visitors or possible customers visit the assembly area.

To prevent contamination from the human body, every individual must be aware of the possibility of contaminating the PCBA. Printed circuits should be touched only on the edges away from any edge connectors prior to the soldering operation (see Fig. 54.2). Where mechanical assembly procedures require a firm grip on the board, gloves or finger cots should be worn. If the PCBA is to be conformal coated after the soldering operation, the handling of the assembly should be prevented. In some cases, using finger cots, gloves, or fixtures can reduce the contamination. Many producers utilize cleanliness testing to ensure that contamination levels remain within an acceptable range before the coating process, and to ensure adhesion and eliminate localized contaminants that could impact circuit operation and long-term performance. J-STD-001 provides levels for cleanliness acceptability.

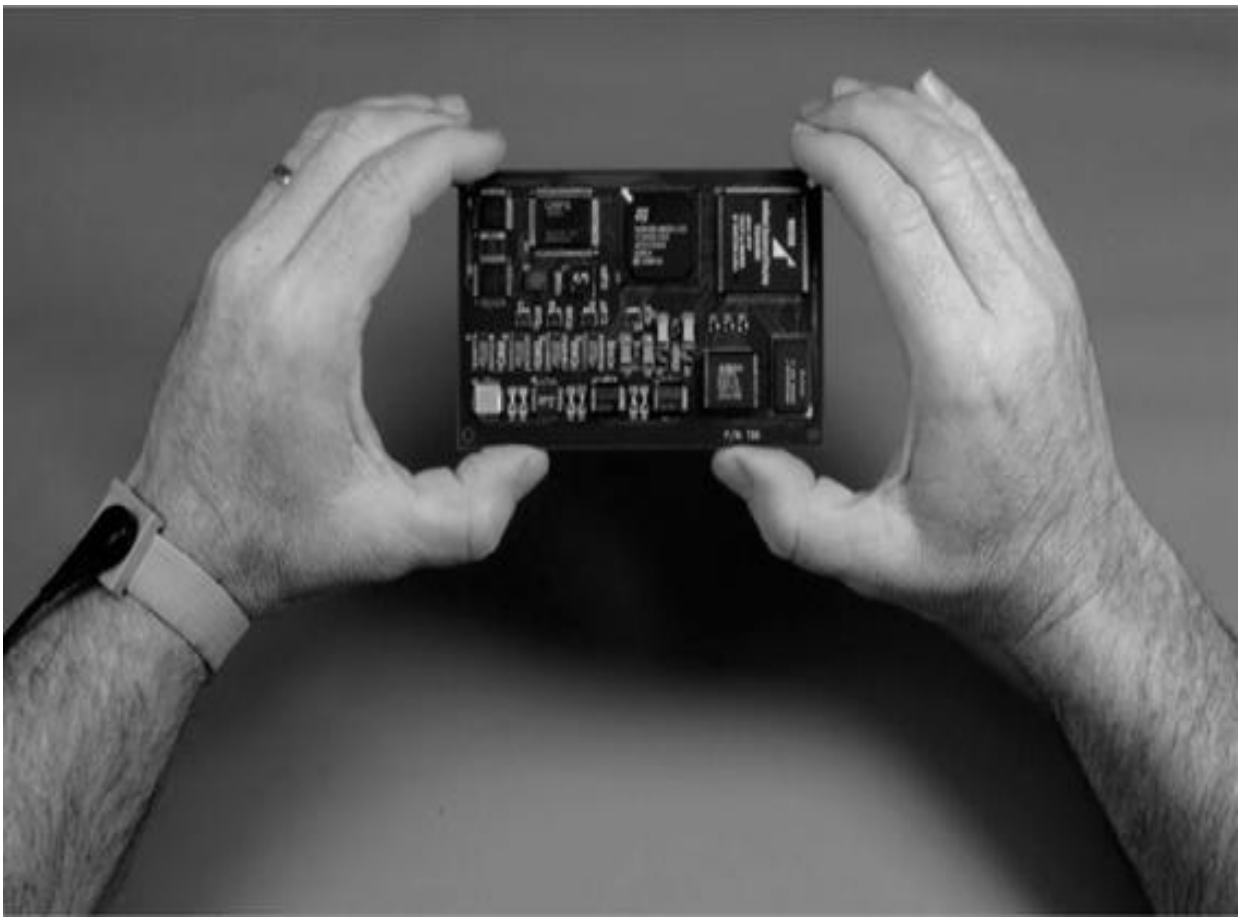


FIGURE 54.2 Appropriate method of handling board to avoid contamination and electrostatic discharger damage. Note position of fingers and the use of a grounding wrist strap.

54.2.3 Physical Damage Prevention

Improper handling can damage components and assemblies. Typical defects associated with handling are cracked, chipped, or broken components; bent or broken terminals; scratched board surfaces; damaged traces or lands; fractured solder joints; and missing surface-mount technology (SMT) components.

Physical damage caused by handling can ruin assemblies and cause a high scrap rate of components or assemblies. Scrap is costly and must be avoided to achieve an efficient and high-quality operation.

Well-maintained handling equipment is also very important in preventing physical damage. One good example is conveyor systems. PCBAs can be caught in conveyors and damaged beyond rework or repair capability and, unless the area of operation is staffed, the conveyor system can damage many assemblies in a very short period of time.

Care must be taken during assembly and acceptability processes to ensure product integrity at all times. The following guidelines provide general guidance:

- Keep workstations clean and neat. There must not be any eating, drinking, or use of tobacco products in the work area.
- Minimize the handling of electronic assemblies and components to prevent damage.
- When gloves are used, they need to be changed as frequently as necessary to prevent contamination from dirty gloves.
- Solderable surfaces are not to be handled with bare hands or fingers. Body oils and salts reduce solderability and promote corrosion and dendritic growth. They can also cause poor adhesion of subsequent coatings or encapsulant.
- Do not use hand creams or lotions containing silicone, because they can cause solderability and conformal coating adhesion problems.
- Never stack electronic assemblies, because physical damage may occur. Special racks need to be provided in assembly areas for temporary storage.
- Always assume the items are ESDS even if they are not marked.
- Personnel must be trained and follow appropriate ESD practices and procedures.
- Never transport ESDS devices unless proper packaging is applied.

54.3 PCBA HARDWARE ACCEPTABILITY CONSIDERATIONS

Most electronic assembly designs include a small percentage of mechanical assembly that requires hardware of various types. Some of the more common component types and the acceptability criteria associated with each are discussed in the following sections.

54.3.1 Component Types

54.3.1.1 Threaded Fasteners. Hardware stack-up for all threaded fasteners must be identified on engineering documentation. The stack-up can be critical, depending on the types of material used for both the hardware and the PCB. Any missing hardware must be found or replaced. Any damage to hardware that prevents it from accomplishing what it was designed to do is unacceptable. A good example of this is any screw or nut that has been stripped, cross-threaded, or damaged to the point that a screw or nut driver is no longer able to tighten or loosen the part (see Fig. 54.3).

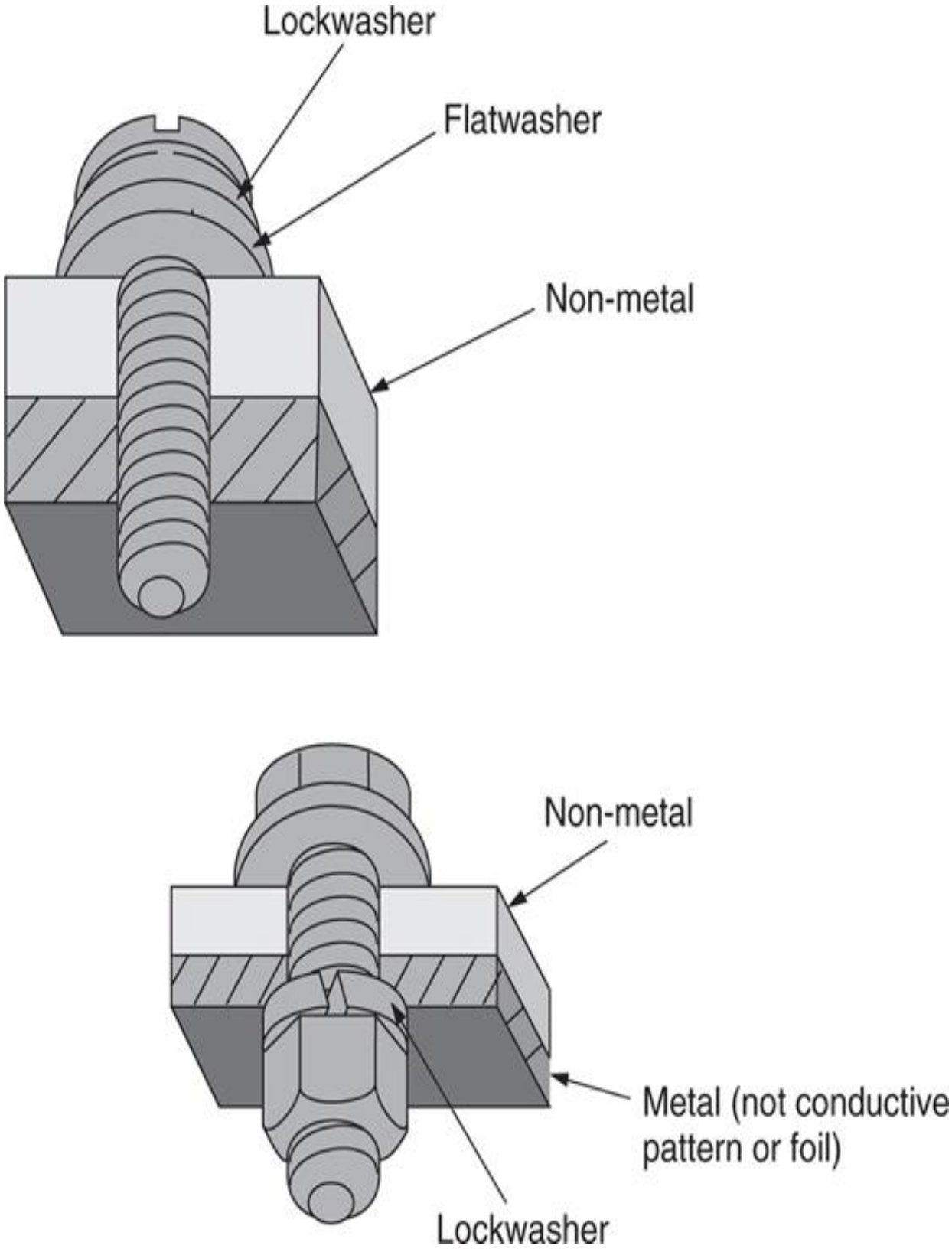


FIGURE 54.3 Hardware mounting for threaded fasteners (1) Lock washer (2) Flat washer (3) Nonconductive material (base laminate) (4) Metal (not conductive

pattern or foil). *(IPC)*

A minimum of 1½ threads should extend beyond the threaded hardware unless the hardware could interfere with other components. The maximum extension of threaded hardware is 3 mm plus 1½ threads for hardware up to 25 mm long and 6.3 mm plus 1½ threads for hardware greater than 25 mm long.

Threaded fasteners should be tight to the specified torque on engineering documentation. If torque is not specified on engineering documentation, a generic torque table should be available for use in the assembly environment. Such a table is sometimes included in a workmanship manual.

54.3.1.2 Mounting Clips. Uninsulated metallic components, clips, or holding devices must be insulated from underlying circuitry. Minimum electrical spacing between land and uninsulated component body must not be violated (see Fig. 54.4).

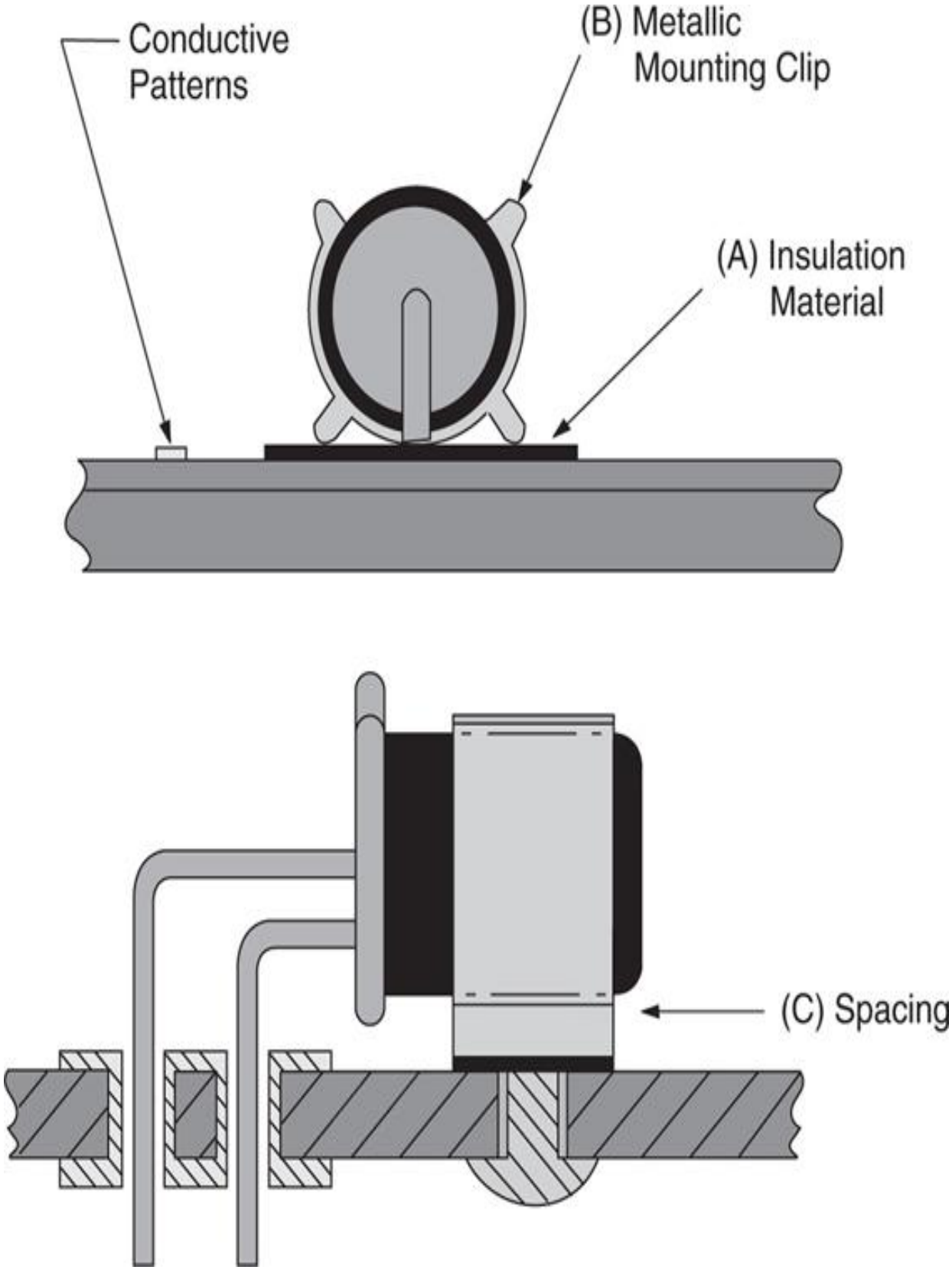
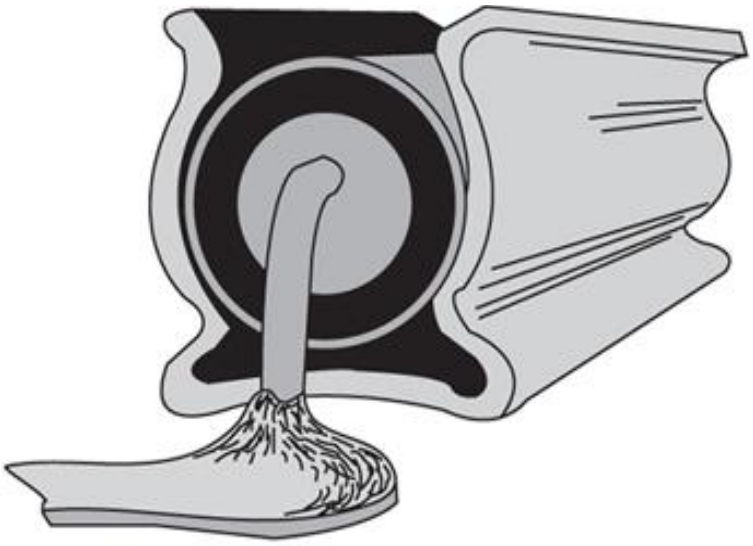
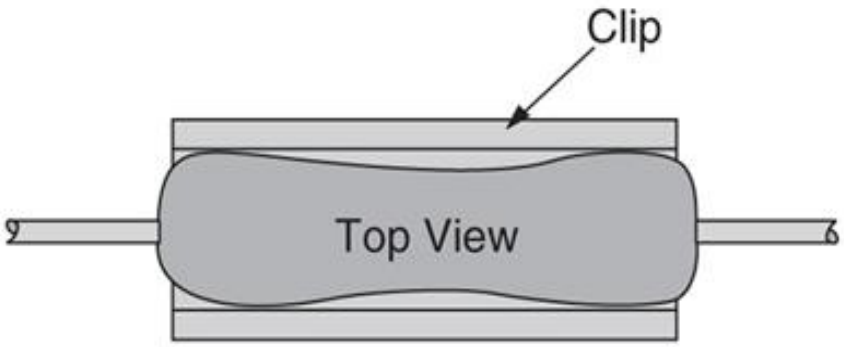

Conductive
Patterns
(B) Metallic
Mounting Clip
(A) Insulation
Material
(C) Spacing

FIGURE 54.4 Component mounting clip insulaton requirements (1) Conductive patterns (2) Metallic mounting clip (3) Insulation material (4) Clearance. *(IPC)*

The clip or holding device must make contact with the component sides on both ends of the component. The component must be mounted with its center of gravity within the confines of the clip or holding device. The end of the component may be flush or extend beyond the end of the clip or holding device if the center of gravity is within the confines of the clip or holding device (see Fig. 54.5).

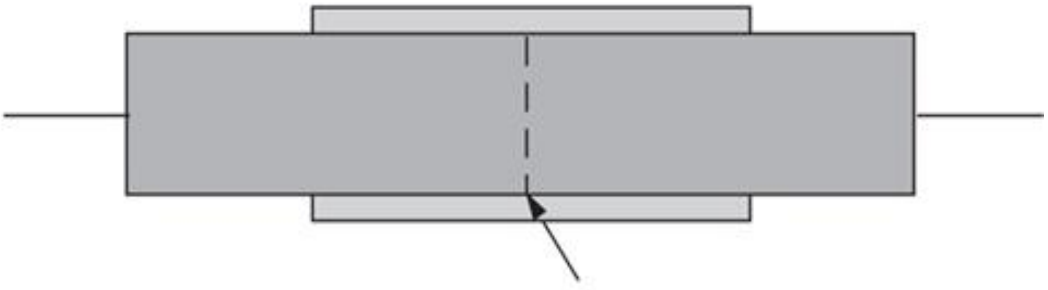


1.



Nonsymmetrical Body

2.



3.

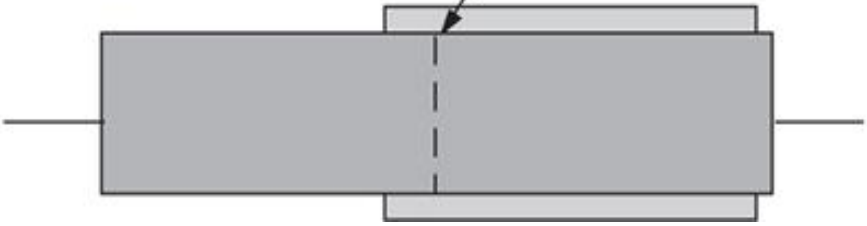


FIGURE 54.5 Component mounting requirements (1) Clip (2) Nonsymmetrical body (3) Top view (4) Center of gravity. *(IPC)*

54.3.1.3 Terminals. Terminals that are to be soldered to a land may be mounted such that they can be turned by hand, but should be stable in the z-axis. Terminals may be bent if the top edge does not extend beyond the base and no other mechanical damage such as fractures or breakage to the terminal or the solder joint have occurred (see Fig. 54.6). Common terminals utilized are turret, bifurcated, hooked, and pierced or perforated terminals. See Fig. 54.7 for an example of a damaged turret terminal and a cross section of an assembled board.

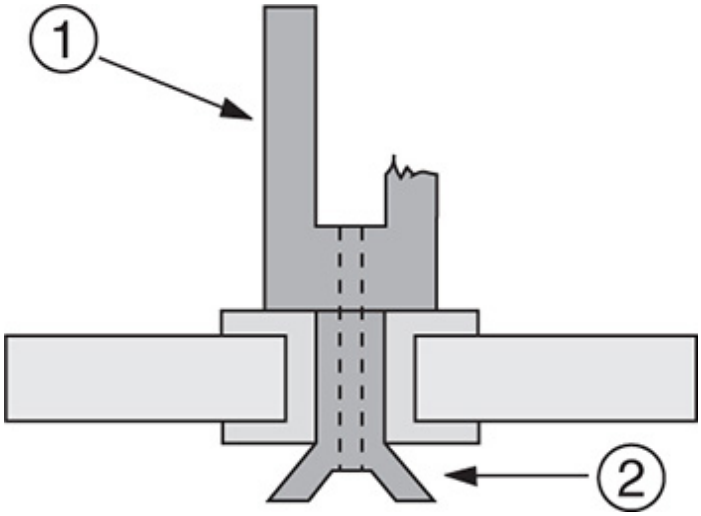


FIGURE 54.6 Bifurcated terminal (1) top edge and (2) base, swaged. Post is broken, but sufficient material is left to attach the specified wires/leads for class I. If both posts are broken, it is unacceptable. *(IPC)*

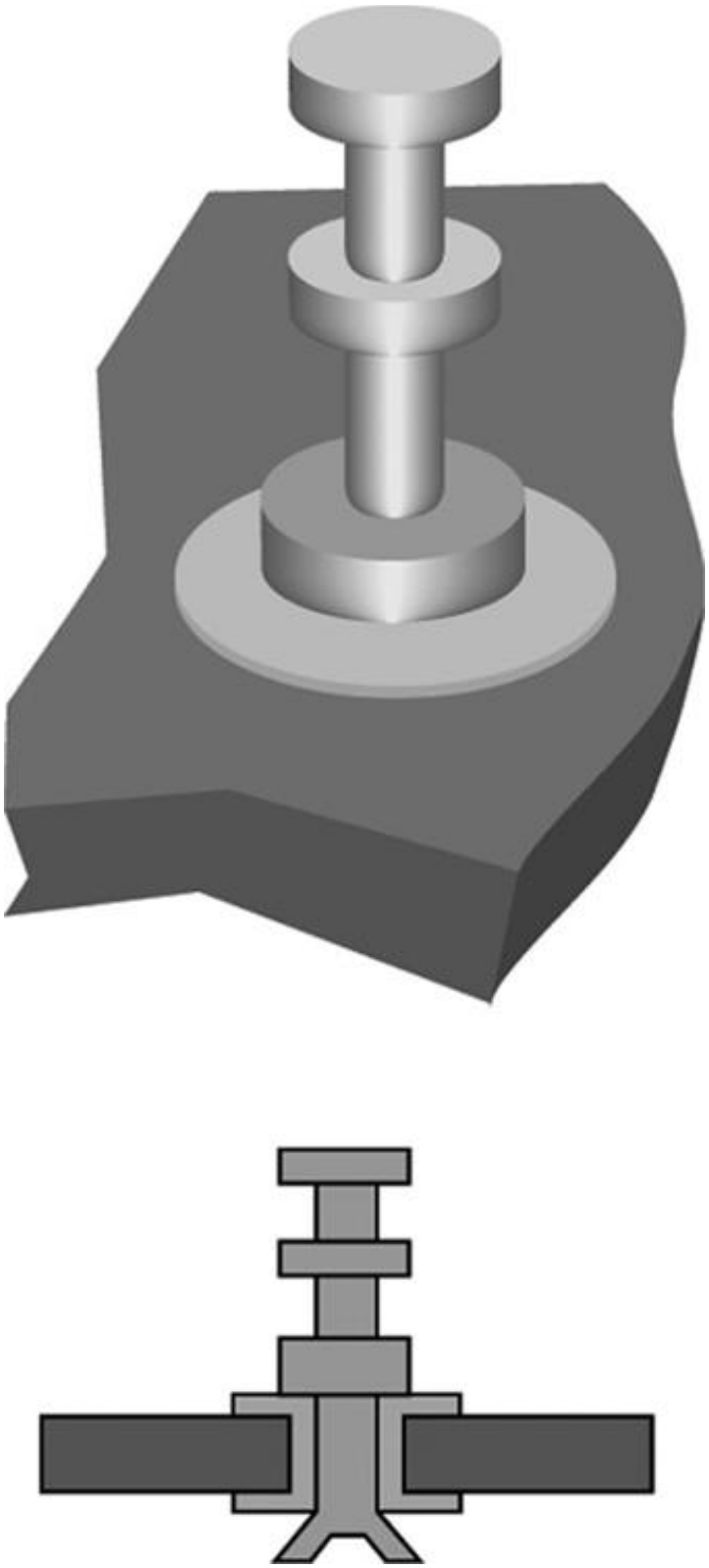


FIGURE 54.7 Acceptable installed turret terminal and cross section of assembled board. Terminal is intact and straight. *(IPC)*

54.3.1.4 Swaged Hardware, Flared Flange. The shank extending beyond the land surface is swaged to create an inverted cone, uniform in spread and concentric to the hole. The flange should not be split, cracked, or otherwise damaged to the extent that mechanical strength is compromised or allows contaminating materials to be entrapped in the rivet or funnel (see Fig. 54.8).

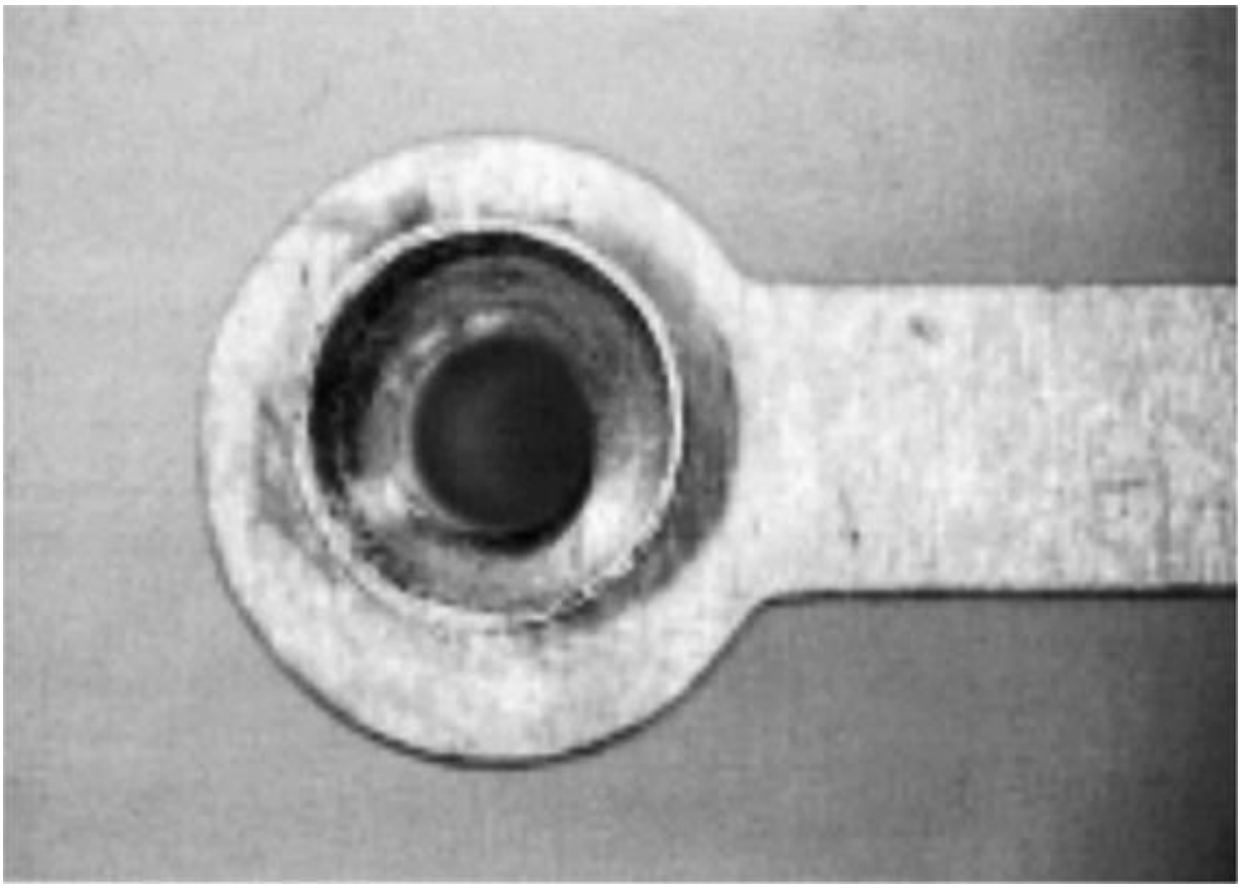


FIGURE 54.8 Flared flange. Acceptable for all Classes.

After swaging, the area should be free of circumferential splits or cracks. It may have a maximum of three radial splits or cracks, provided that the splits or cracks are separated by at least 90° and do not extend into the barrel of the rivet or funnel (see Fig. 54.9).

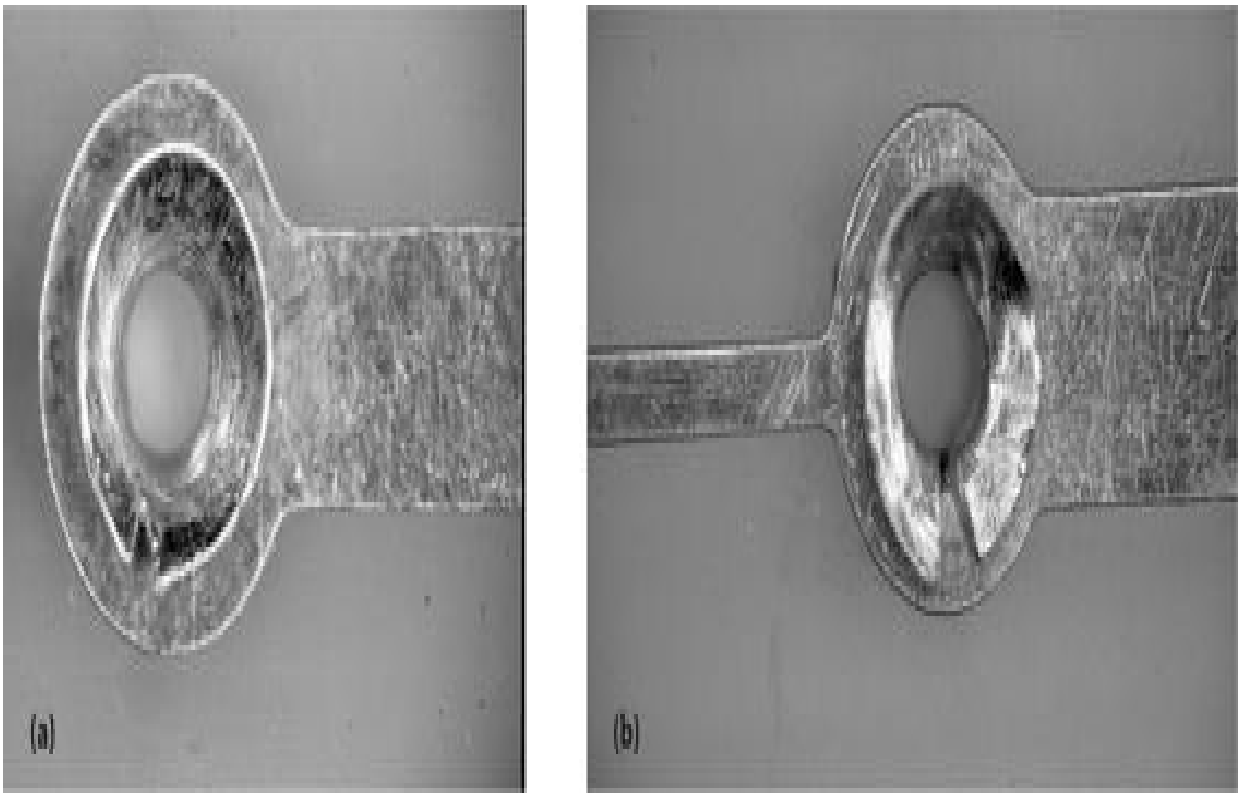


FIGURE 54.9 (a) Shows an example of acceptable flared swage-split while (b) shows an unacceptable split into barrel.

54.3.1.5 Connectors, Handles, Extractors, and Latches. Ejectors, handles, and connectors should not exhibit any cracks in the component material emanating from the roll pin or rivet that mounts the component to the PCBA.

Roll pins should not protrude more than 0.015 in. from the surface of the ejector, handle, or connector. The major consideration for roll pins should be to ensure that any protrusion does not mechanically interfere with any other assembly. Damage to the part, PCB, or securing hardware is unacceptable.

Connector damage can also affect the pins of the connector being pushed or bent out of specification. When connectors are mated, there is the chance that the female portion of the connector pin will be pushed backward and bent. This prevents adequate contact area between the male

and female pins of the connector, if they will mate at all. This circumstance is an unacceptable condition.

The male connector pins might also be bent. When the male pin is bent significantly, the mating of the female and male connectors can cause mechanical damage to the connector casing due to the male pin being forced into the wrong female connector slot. In most cases, the damage is deformation, cracking, or breaking of the connector casing material, all of which are unacceptable.

When connector pins are installed (such as compliant pin, press fit), the pins must be straight within 50 percent of the pin thickness from the perpendicular. For Class 1 and 2 equipment, the PCB land may be lifted less than or equal to 75 percent of the annular ring width. Any land that is lifted across more than 75 percent of the annular ring or has been fractured is unacceptable. For Class 3 equipment, no lifted or fractured lands are acceptable. For all classes, visibly twisted pins, damaged pins, or pins inserted such that there is a nonstandard pin height beyond a specified engineering tolerance is unacceptable.

54.3.1.6 Faceplates. Faceplates must be clean and free of scratches or damage on the front surface. This is important since this is the surface that is commonly viewed by the customer and presents the cosmetic appeal to the product being purchased. An exaggerated example of this is the purchase of an automobile. Few if any consumers would be willing to accept a new automobile with noticeable scratches in the painted surface.

A good rule of thumb for scratch criteria that some companies have adopted as a workmanship standard includes the following:

1. A scratch must be visible when viewed under the following conditions to be considered a defect:

a. From a distance of 18 in.

b. With no magnification utilized

c. With normal room lighting used in the assembly area

2. A scratch must be visible from more than one angle to be considered a defect.

3. Metal or plastic faceplate scratches that exceed 0.125 in. in length are considered defects.

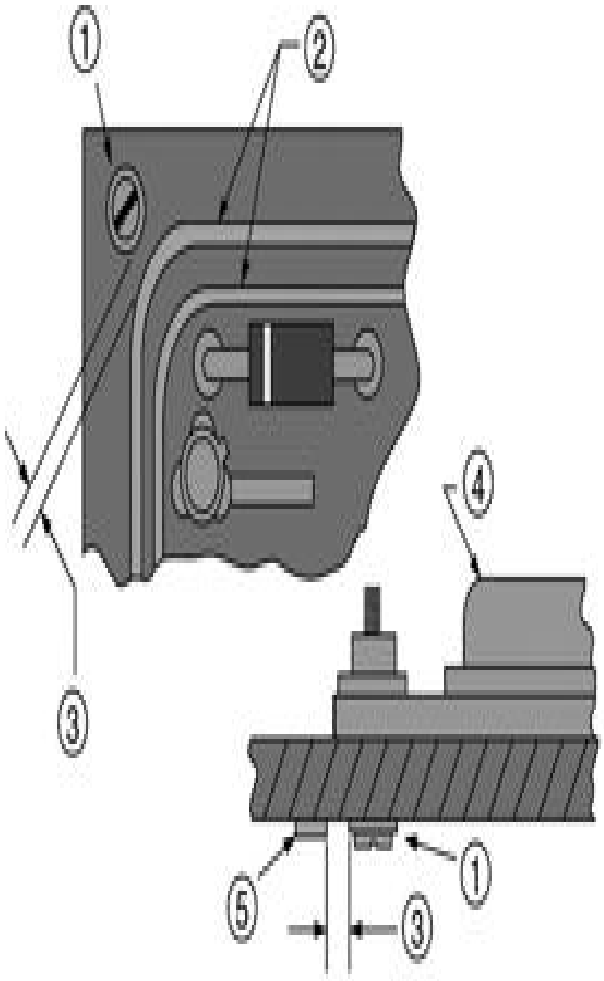
Surfaces exposed to frequent viewing should be free of blisters, runs, nicks, gouges, blemishes, or other abrasions that would detract from the general appearance of the finish. Faceplates must also be securely fastened to the PCB, that is, tightly enough to prevent physical movement.

54.3.1.7 Stiffeners. Stiffeners are commonly used on PCBA designs that are large in dimension to prevent warpage of the PCBA before, during, or after assembly operations. If a stiffener has kept a PCBA from warping outside acceptability criteria, it has done its job; however, the stiffener must meet the following criteria to be acceptable:

- Any marking or color coatings must be permanent. Loss of marking such that it is not legible, or fading or loss of color outside the color standard being used, is unacceptable.
- The stiffener must be properly seated and mechanically fastened. If the soldering operation is used to mechanically fasten the stiffener to the PCBA, then good wetting to the stiffener such that the stiffener is mechanically sound is required.
- It is unacceptable to have a loose stiffener on a PCBA. The stiffener must be securely fastened to the PCBA.

54.3.2 Electrical Clearance

Electrical clearance of hardware to components or electrical traces must be controlled by the design based on the expected voltage and environment’s exposure. As a default, design standards such as IPC-2221 create a spacing requirement unless it is specifically defined for the particular PCBA (see Fig. 54.10 for examples). Minimum electrical clearance can be referenced throughout the acceptability requirements such as with contaminants or board laminate defects related to the conductors. Any violation of minimum electrical clearance is cause for a defect disposition consideration for any class, since it will directly impact the electrical performance of the product. Any condition that compromises the clearance should be verified by assemblers or inspectors to ensure that a shorting condition does not occur.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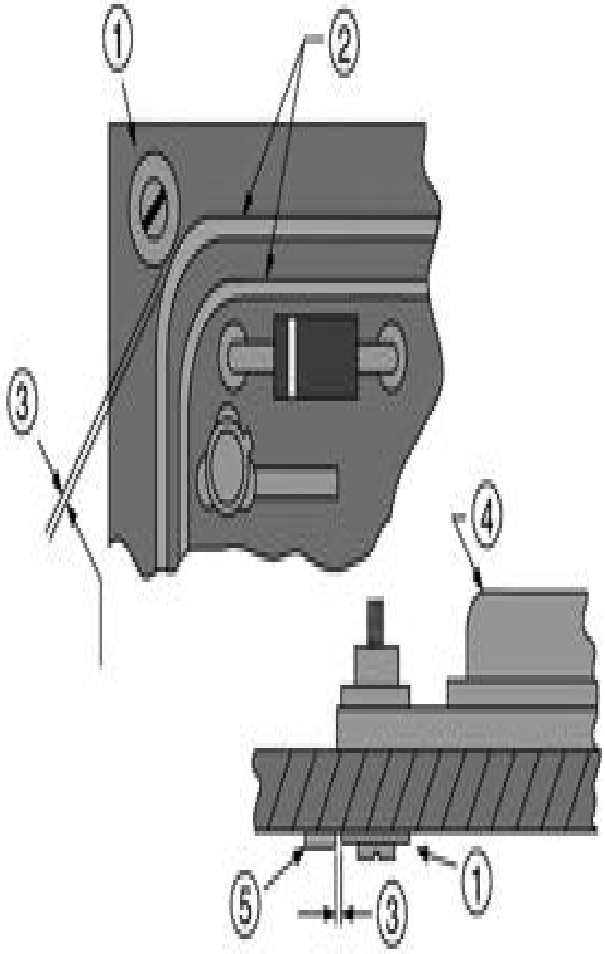
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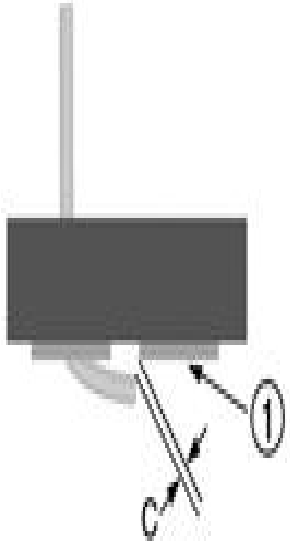
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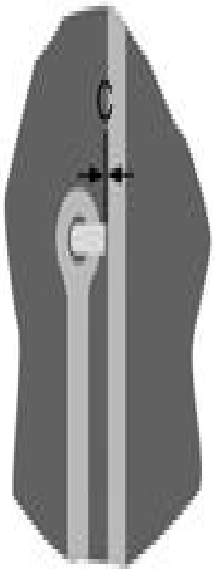

C

FIGURE 54.10 Examples of acceptable and unacceptable electrical clearance-hardware. (a) Acceptable where: (1) Metallic hardware; (2) Conductor pattern; (3) Specified minimum electrical clearance; (4) Mounted component; (5) Conductor; (b) Unacceptable where hardware reduces clearances to less than specified electrical clearance; (1) Metallic hardware; (2) Conductor pattern; (3) Spacing less than minimum electrical requirements; (4) Mounted component; (5) Conductor; (c) Unacceptable as lead is clinched toward a noncommon electrical conductor (1) and violates clearance; (C) requirement.

54.3.3 Physical Damage

Physical damage to hardware components in most cases refers to enough damage to a component to render it unusable in its application—for example, threads that are damaged to the point that mechanical fastening cannot be performed or a component that is fractured or broken such that it cannot perform the function for which it was intended.

Subjective judgments are common in this area since it is very much dependent on the application of the hardware in the given design, the environment in which the final product will be used, and life cycle expectations of the product.

54.4 COMPONENT INSTALLATION OR PLACEMENT REQUIREMENTS

Component installation or placement is the first step in the assembly of the PCBA. It may begin by preparation of the leads of a given package type in order to provide the correct lead protrusion, form the leads to fit the PCB plated-through holes or pads, or put a bend in the leads that will serve as a standoff from the component to the PCB.

54.4.1 Plated-Through Hole Lead Installation

Several requirements apply to all Plated-Through Hole (PTH) components. When using a polarized component, it must be oriented correctly. In all cases, if the orientation is incorrect, the board is unacceptable (see Fig. 54.11). When lead forming is required, the lead form must provide clearance and stress relief (see Fig. 54.12). Physical damage to the lead itself cannot exceed 10 percent of the diameter of the lead. Exposed basis metal as a result of lead deformation is a process indicator but does not render the board unacceptable.

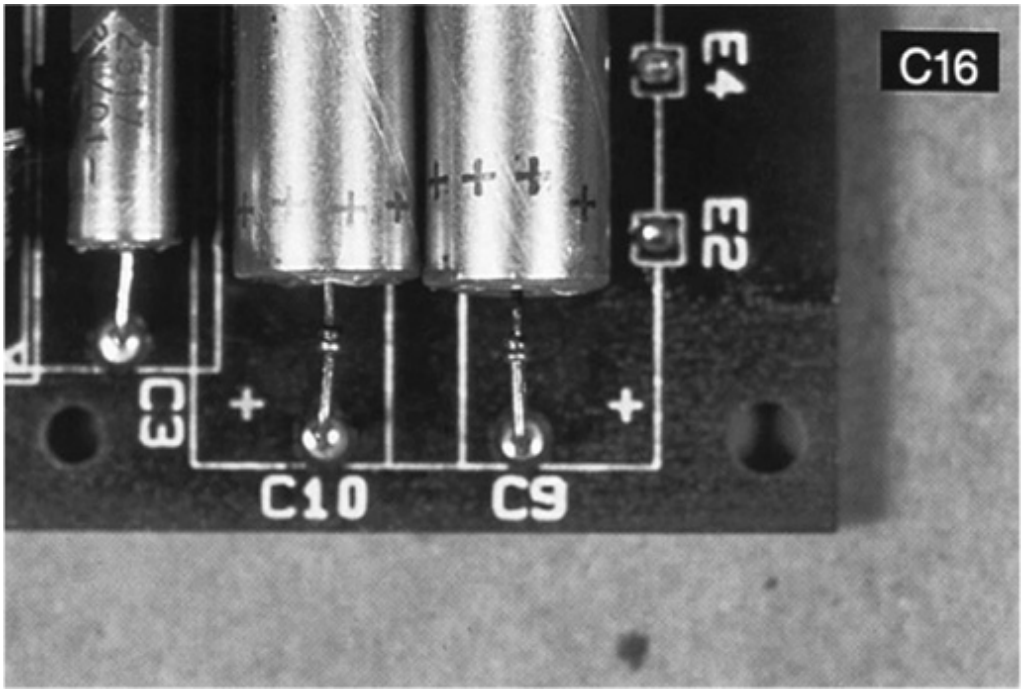


FIGURE 54.11 Component orientation–polarity. *(IPC)*

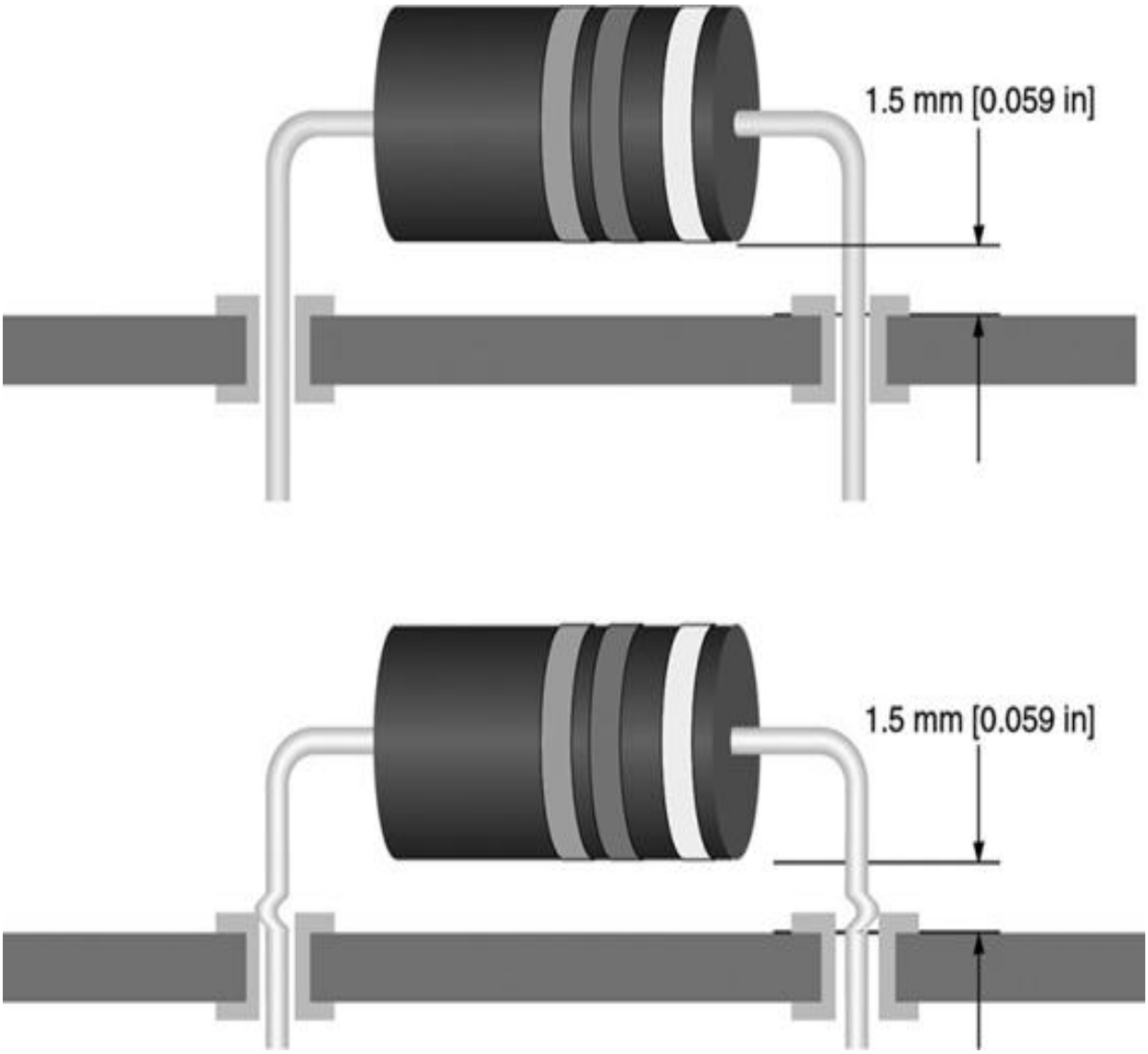


FIGURE 54.12 Examples of acceptable clearance and stress relief for PTH components. *(IPC)*

54.4.1.1 Axial Leaded Components. The target condition for axial components is that the entire body length of the component should be parallel and in contact with the board surface (see Fig. 54.13 for tolerances). If the component is required to be spaced above the board to avoid overheating the laminate, it must be mounted a minimum of 1.5 mm above the PCB surface. The maximum space between the component and the PCB surface should not violate the requirements for lead protrusion and cannot

be greater than 3.0 mm for Class 1 and 2 and 0.7 mm for Class 3 equipment (see Fig. 54.13).

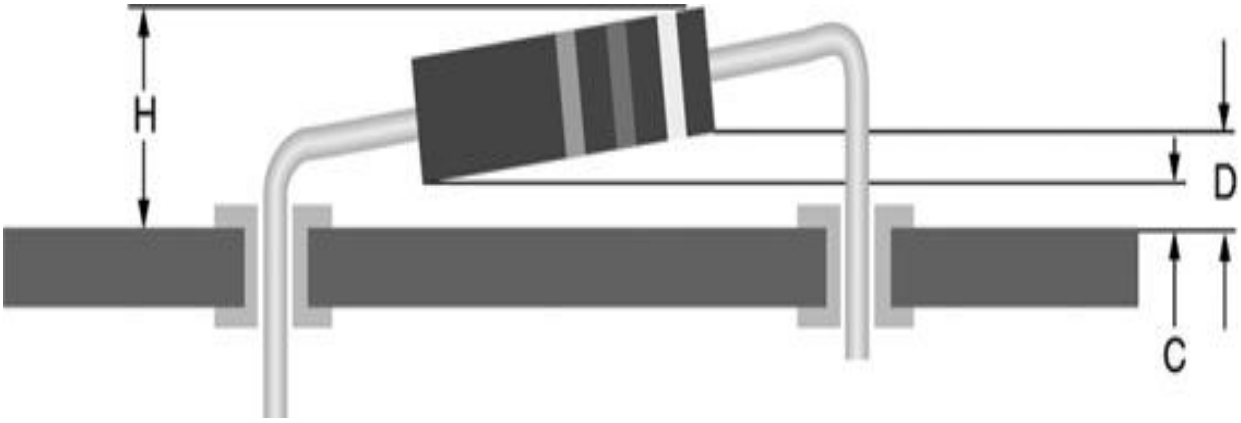


FIGURE 54.13 Amount of nonparallel allowed varies by class but is measured: (H) is component height, (C) is clearance between component body and board, and (D) is the farthest distance between the component body and the board.

Leads must extend from the component body at least one lead diameter (L) or thickness, but not less than 0.8 mm from the body or weld, before the start of the lead bend radius (see Fig. 54.14).

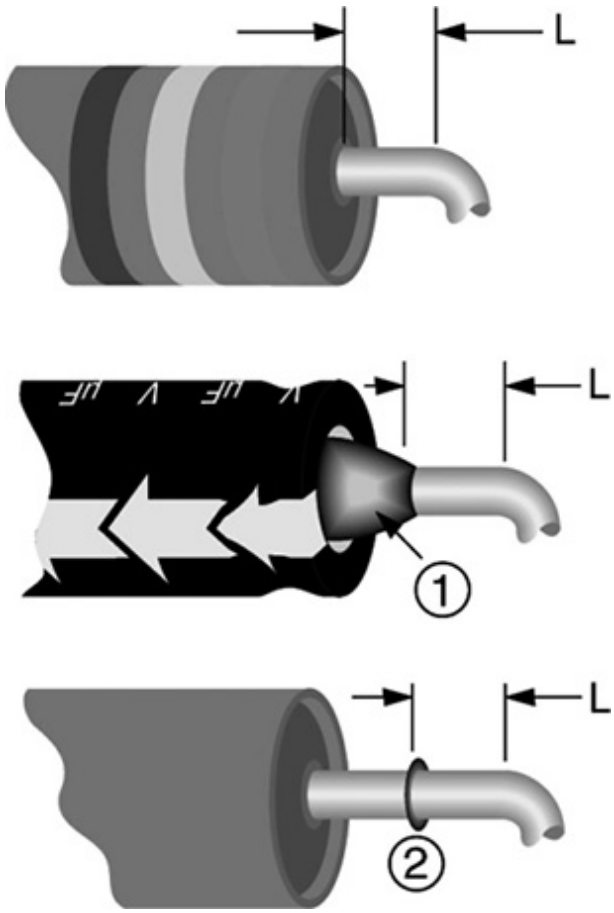


FIGURE 54.14 Lead extension from component body, where (1) is solder bead, (2) is weld. L is the distance from the effective component body to the bend. *(IPC)*

No physical damage, such as chips or cracks to axial components, should be allowed; however, it is acceptable to allow minor damage. It becomes unacceptable if the insulating cover is damaged to the extent that the metallic element is exposed or the component shape is deformed (see Fig. 54.15).

FIGURE 54.15 Example of physical damage to component after insertion. This is a “defect” condition and cause for rejection. (a) Axial lead component, (b) Chip component. *(IPC)*

54.4.1.2 Radial Leaded Components. The target condition for vertical radial components is that the body is perpendicular to the PCB and the component base is parallel to the PCB. It is an acceptable condition to have the component tilt from the perpendicular as long as it does not violate electrical clearance. The space between the component base and PCB should be between 0.3 and 2.0 mm (see Fig. 54.16) but it is considered a process indicator only if it exceeds that dimension. Some components, such as light-emitting diodes (LEDs) and switches, may need to be perpendicular due to mating requirements.

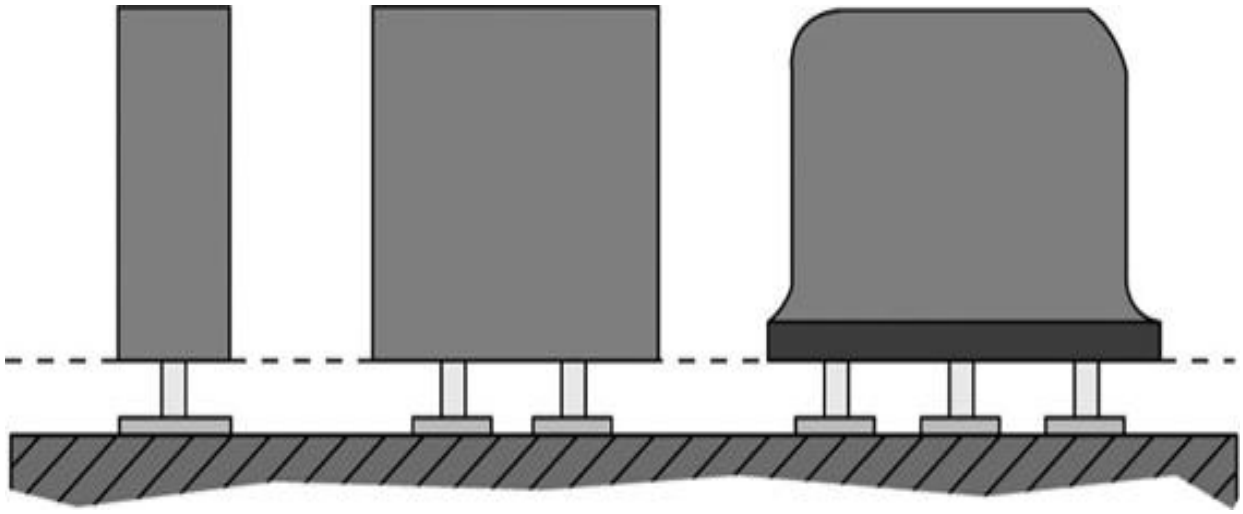


FIGURE 54.16 Radial leaded components spacing. Component is perpendicular and base is parallel to board. Acceptable clearance varies with Class. *(IPC)*

54.4.2 SMT Placement

Coplanarity is very important in the placement of SMT components with leads. Occasionally, lead preparation to form the leads of SMT components is necessary to achieve the proper coplanarity for manual or automatic placement of components on the PCB. Most times, however, the components are purchased packaged with leads prepared and ready to be automatically placed by pick-and-place equipment. Another critical parameter for all surface-mounted components is the accuracy of placement of the components onto the pads of the PCB.

54.4.2.1 Chip Components. Side overhang is acceptable up to one-half (one-quarter for Class 3) the width of the component end cap or PCB pad. End-cap overhang is not acceptable for all classes. The end-cap solder joint width is acceptable with a minimum solder joint length of one-half (three-quarters for Class 3) the component end cap or PCB land, whichever is less.

A side solder joint length is not required; however, a properly wetted fillet must be evident.

The maximum solder fillet height may overhang the land or extend onto the top of the end-cap metallization; however, the solder should not extend farther on the component body. The minimum solder fillet height must cover one-quarter the thickness, or height, of the component end cap for Class 3 but is required to be evident only for Classes 1 and 2. The component end cap must have overlap contact with the PCB pad. There is no minimum contact length specified see (see Fig. 54.17 and Table 54.1 for an example and list of specifications).

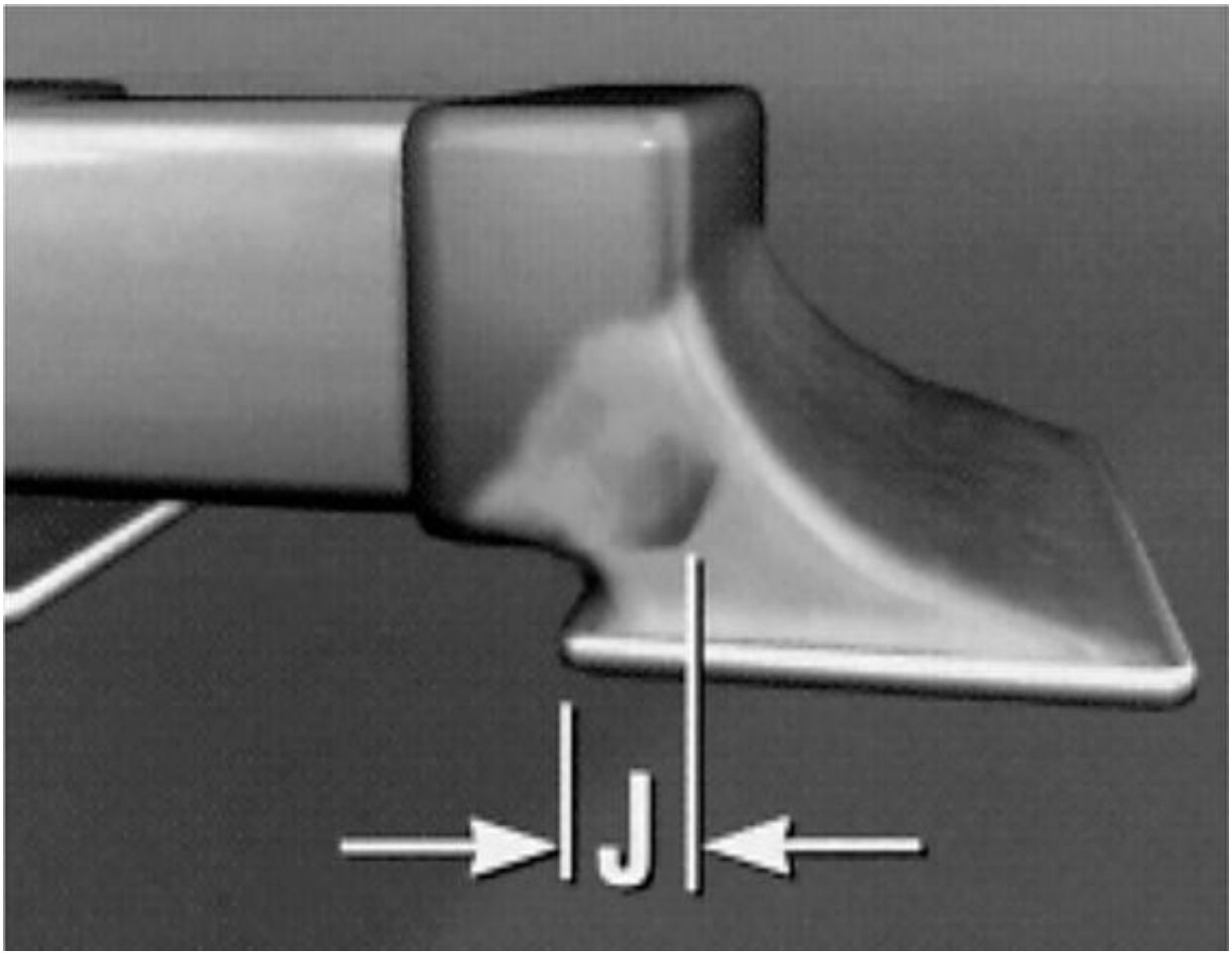


FIGURE 54.17 Example placement and solder fillet for surface mount chip component. Evidence of overlap of contact (J) between the component termination and the land is required. *(IPC)*

TABLE 54.1 Dimensional Criteria for Chip Components, Rectangular or Square End Components—One-, Three-, or Five-Side Terminations

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% (W) or 50% (P) whichever is less[a]		25% (W) or 25% (P), whichever is less[a]
End Overhang	B	Not permitted		
Minimum End Joint Width	C	50% (W) or 50% (P), whichever is less[b]		75% (W) or 75% (P), whichever is less[b]
Minimum Side Joint Length	D	Wetting is evident		
Maximum Fillet Height	E	The maximum fillet may overhang the land and/or extend onto the top of the end-cap metallization; however, the solder does not extend further onto the top of the component body		
Minimum Fillet Height	F	Wetting is evident on the vertical surface(s) of the component termination[c]		(G) + 25% (H) or (G) + 0.5 mm (0.02 in.), whichever is less[c]
Solder Thickness	G	Wetting is evident		
Termination Height	H	Unspecified dimension, determined by design		
Minimum End Overlap	J	Required		
Width of Land	P	Unspecified dimension, determined by design		
Termination Width	W	Unspecified dimension, determined by design		
Side mounting/billboarding[d,e]				
Width to Height Ratio		Does not exceed 2:1		
End Cap and Land Wetting		100% wetting land to end metallization contact areas		
Minimum End Overlap	J	100%		
Maximum Side Overhang	A	Not permitted		
End Overhang	B	Not permitted		
Maximum Component Size		No limits		1206
Termination Faces		Three or more faces		

Notes:

[a] Does not violate minimum electrical clearance.

[b] C is measured from the narrowest side of the solder fillet.

[c] Designs with via in pad may preclude meeting these criteria. Solder acceptance criteria should be defined by the user and the manufacturer.

[d] These criteria are for chip components that may flip (rotate) onto the narrow edge during assembly.

[e] These criteria may not be acceptable for certain high-frequency or high-vibration applications.

54.4.2.2 Metal Electrode Leadless Face or Cylindrical Termination. Side overhang is acceptable up to one-quarter the diameter of the end cap. This dimension is different from the other SMT components due to the cylindrical feature of the component. End-cap overhang is not acceptable for all classes. The end-cap solder joint width is acceptable with a minimum solder joint length of one-half the diameter of the component end cap for Classes 2 and 3 but is required to be discernable only for Class 1. A side solder joint length must be a minimum of one-half (three-quarters for Class 3), but again is required to discernable only for Class 1. The maximum solder fillet height may overhang the land or extend onto the top of the end-cap metallization; however, the solder should not extend farther on the component body. The minimum solder fillet height must cover one-quarter the thickness, or height, of the component end cap for Class 3, and for Classes 1 and 2 the minimum solder fillet must exhibit proper wetting. The component end cap must have 75 percent of the cap dimension overlapping the land for Class 3 and 50 percent for Class 2. There is no minimum contact length specified for Class 1 (see Fig. 54.18 and Table 54.2).

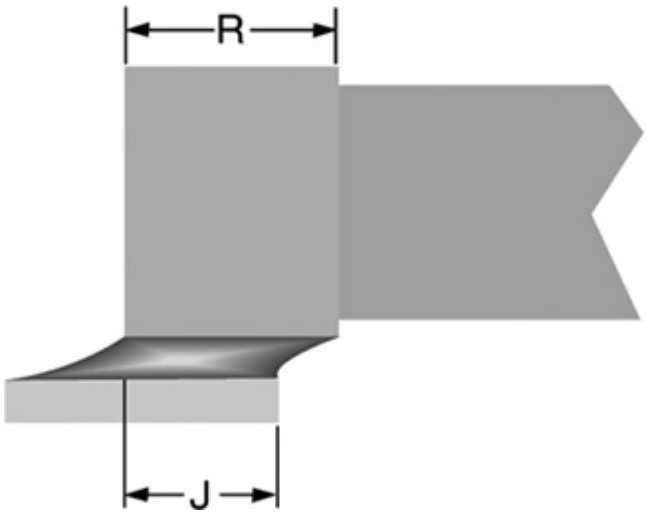


FIGURE 54.18 Cylindrical end cap (MELF) termination. “J” represents the overlap between component termination and land, “R” is length of component

termination. *(IPC*)

TABLE 54.2 Dimensional Criteria: Cylindrical End-Cap Metal Electrode Leadless Face (MELF) Termination

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	25% (W) or 25% (P), whichever is less[a]		
End Overhang	B	Not permitted		
Minimum End Joint Width[b]	C	Wetting is evident	50% (W) or 50% (P), whichever is less	
Minimum Side Joint Length	D	Wetting is evident[c]	50% (R) or 50% (S), whichever is less[d]	75% (R) or 75% (S), whichever is less[d]
Maximum Fillet Height	E	The maximum fillet may overhang the land or extend onto the top of the component termination; however, the solder does not extend further onto the component body		
Minimum Fillet Height (End and Side)	F	Wetting is evident on the vertical surface(s) of the component termination[d]		(G) + 25% (W) or (G) + 1.0 mm (0.0394 in.), whichever is less[d]
Solder Thickness	G	Wetting is evident		
Minimum End Overlap	J	Wetting is evident[c]	50% (R)[c]	75% (R)[c]
Land Width	P	Unspecified dimension, determined by design		
Termination/Plating Length	R	Unspecified dimension, determined by design		
Land Length	S	Unspecified dimension, determined by design		
Termination Diameter	W	Unspecified dimension, determined by design		

Notes:

[a]Does not violate minimum electrical clearance.

[b]C is measured from the narrowest side of the solder fillet.

[c]Does not apply to components with end-only terminations.

[d]Designs with via in pad may preclude meeting those criteria. Solder acceptance criteria should be defined by the user and the manufacturer.

54.4.2.3 Castellated Terminations. Side overhang is acceptable up to one-half (one-quarter for Class 3) of the castellation width. End overhang of the castellation is not acceptable for all classes. The castellation end solder joint width is acceptable with a minimum solder joint length of one-half (three-quarters for Class 3) of the castellation width (see Table 54.3). A minimum side solder joint length is required to extend beyond the edge of the component for all classes. The maximum solder fillet height is not a specified parameter for this type. The minimum solder fillet height must be 50 percent of the castellation height for Class 3 and 25 percent for Class 2. The only height requirement for Class 1 is that at least one fillet is visible.

TABLE 54.3 Dimensional Criteria: Castellated Terminations

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% (W)[a]		25% (W)[a]
End Overhang	B	Not permitted		
Minimum End Joint Width	C	50% (W)		75% (W)
Minimum Side Joint Length	D	wetting is evident	Depth of castellation	Depth of castellation
Maximum Fillet Height	E	G + H		
Minimum Fillet Height	F	wetting is evident	(G) + 25% (H)	(G) + 50% (H)
Solder Thickness	G	Wetting is evident.		
Castellation Height	H	Unspecified dimension, determined by design		
Land Length	S	Unspecified dimension, determined by design		
Castellation Width	W	Unspecified dimension, determined by design		

Note:
[a]Does not violate minimum electrical clearance.

54.4.2.4 Flat Ribbon, L, and Gull-Wing Leads. Side overhang is acceptable up to one-half (one quarter for Class 3) of the width of the component lead. Lead toe overhang is acceptable for all classes provided it does not violate minimum electrical clearance. The end-joint solder width is acceptable for Class 2 with a minimum solder-joint length of one-half (three-quarters for Class 3) of the component lead width. The lead-side solder-joint minimum length is one-time the lead width for Class 1. It must be three times the width when the lead length is greater than three times its width. If the lead length is less than three times its width, the side joint width must be equal to the length. For Classes 2 and 3,

the maximum solder fillet height on components such as small-outline integrated circuits (SOICs) or small-outline transistors (SOTs) may touch the package body or end seal, but not that of ceramic or metallic components. The minimum solder heel fillet height must cover one-half of the lead thickness for Class 2 and must be equal to the lead thickness for Class 3 (see Table 54.4).

TABLE 54.4 Dimensional Criteria: Flat Ribbon, L, and Gull-Wing Leads

Feature		Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang		A	50% (W) or 0.5 mm (0.02 in.), whichever is less[a]		25% (W) or 0.5 mm (0.02 in.), whichever is less[a]
Maximum Toe Overhang		B	Does not violate minimum electrical clearance		
Minimum End Joint Width		C	50% (W)		75% (W)
Minimum Side Joint Length[b]	When (L) Is ≥3 W	D	(1W) or 0.5 mm [0.02 in.], whichever is less	3 (W) or 75% L, whichever is longer	
	When (L) Is <3 W			100% (L)	
Maximum Heel Fillet Height		E	See Section 52.4.2.1		
Minimum Heel Fillet Height		F	Wetting is evident	(G) + 50% (T)[c]	(G) + (T)[c]
Solder Thickness		G	Wetting is evident		
Formed Foot Length		L	Unspecified dimension, determined by design		
Lead Thickness		T	Unspecified dimension, determined by design		
Lead Width		W	Unspecified dimension, determined by design		

Notes:

[a] Does not violate minimum electrical clearance.

[b] Fine-pitch leads require a minimum side fillet length of 0.5 mm (0.02 in.).

[c] In the case of a toe-down lead configuration, the minimum heel fillet height (F) extends at least to the midpoint of the outside lead bend.

54.4.2.5 J-Leaded Components. Side overhang is acceptable up to one-half (one-quarter for Class 3) of the width of the component lead. Lead toe overhang is not specified for any class.

The end lead solder-joint width is acceptable with a minimum solder-joint length of one-half (three-quarters for

Class 3) of the component lead width. A side solder-joint length must be a minimum of 1½ times the lead width for both Class 2 and 3, but Class 1 requires only a visible fillet. The maximum solder fillet height is not specified; however, the solder fillet may not touch the component package body. The minimum heel solder fillet height must cover one-half of the thickness of the component lead or the lead thickness for Class 3 (see Table 54.5).

TABLE 54.5 Dimensional Criteria: J–Leads

Feature	Dim.	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% (W)[a]		25% (W)[a]
Maximum Toe Overhang	B	Unspecified dimension, determined by design[a]		
Minimum End Joint Width	C	50% (W)		75% (W)
Minimum Side Joint Length	D	Wetting is evident	150% (W)	
Maximum Fillet Height	E	Solder does not touch package body		
Minimum Heel Fillet Height	F	(G) + 50% (T)		(G) + (T)
Solder Thickness	G	Wetting is evident		
Lead Thickness	T	Unspecified dimension, determined by design		
Lead Width	W	Unspecified dimension, determined by design		

Note:
[a] Does not violate minimum electrical clearance.

54.4.2.6 Ball Grid Array Components. Ball Grid Array (BGA) package components are a very popular design due to significant packaging density. This allows designers to get more function in a smaller space. The component package is virtually impossible to inspect visually as traditionally allowed with other components since the solder spheres are

located beneath the component. If cost justification exists, either due to volume or reliability provisions such as could be the case on Class 3 equipment, x-ray equipment can be used to verify the position quality and integrity of the solder joints. This could be costly in terms of the upfront capital investment of the x-ray equipment, but may pay for itself many times over in customer satisfaction or the prevention of defective product. Other options may use the x-ray as a process development tool where once the process is stabilized, the inspection is reduced to sampling or eliminated completely.

X-ray inspection can provide a visual depiction of the solder connection that must not contain solder bridges, incomplete reflow, attachment fractures, misalignment that violates minimum electrical clearance, or missing or damaged spheres. It's also considered defective for solder voids to displace more than 25 percent of a sphere (see Fig. 54.19).

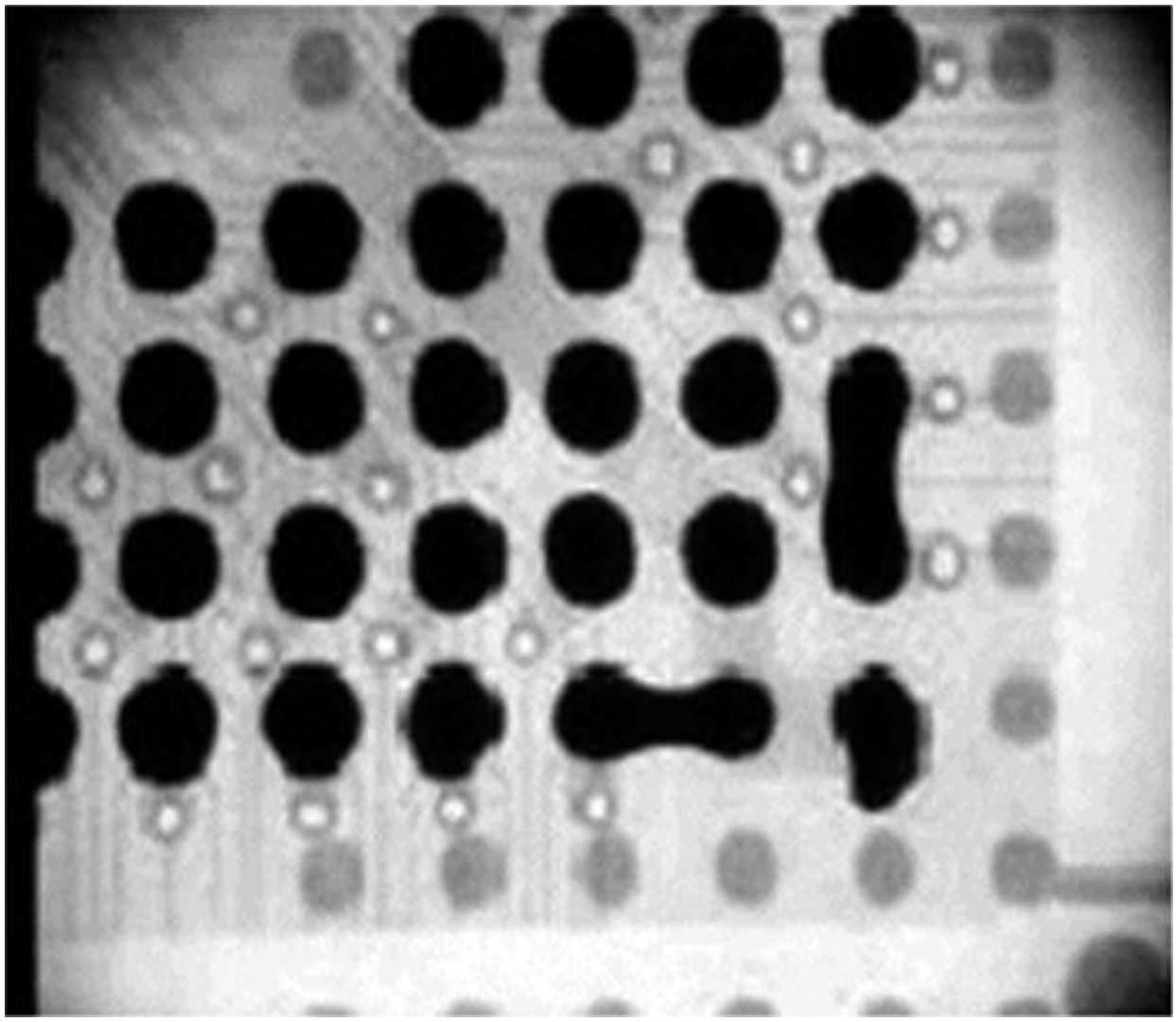


FIGURE 54.19 Ball grid array (BGA), bottom view showing solder ball connection. *(IPC)*

54.4.3 Use of Adhesives

Adhesives can often be used in SMT and PTH applications.

For SMT components, adhesive may be used to attach components to the bottom side of the PCB for mixed technologies (those containing both through-hole and SMT components). In some process flows, the SMT components are placed with adhesive between the solder pads; the PCB is processed through an adhesive curing cycle; then the

components are wave soldered or reflowed onto the PCB along with the PTH components. In some processes, the adhesive is a temporary (soluble) attachment to stabilize the components during soldering and is to be removed after the solder is attached. In some extreme cases, the adhesive is used for both through-hole and SMT components to support the physical attachment of the components for severe operational conditions such as physical shock or vibration. Where intended to support the component physically, the attachment is specifically defined by drawing or individual requirements. The SMT components are acceptable as long as the adhesive has not contaminated the solder joint. If adhesive has contaminated the component solderable surface, lead, end cap, or PCB pad such that an acceptable solder joint is not achieved, the PCBA is not acceptable (see Fig. 54.20).

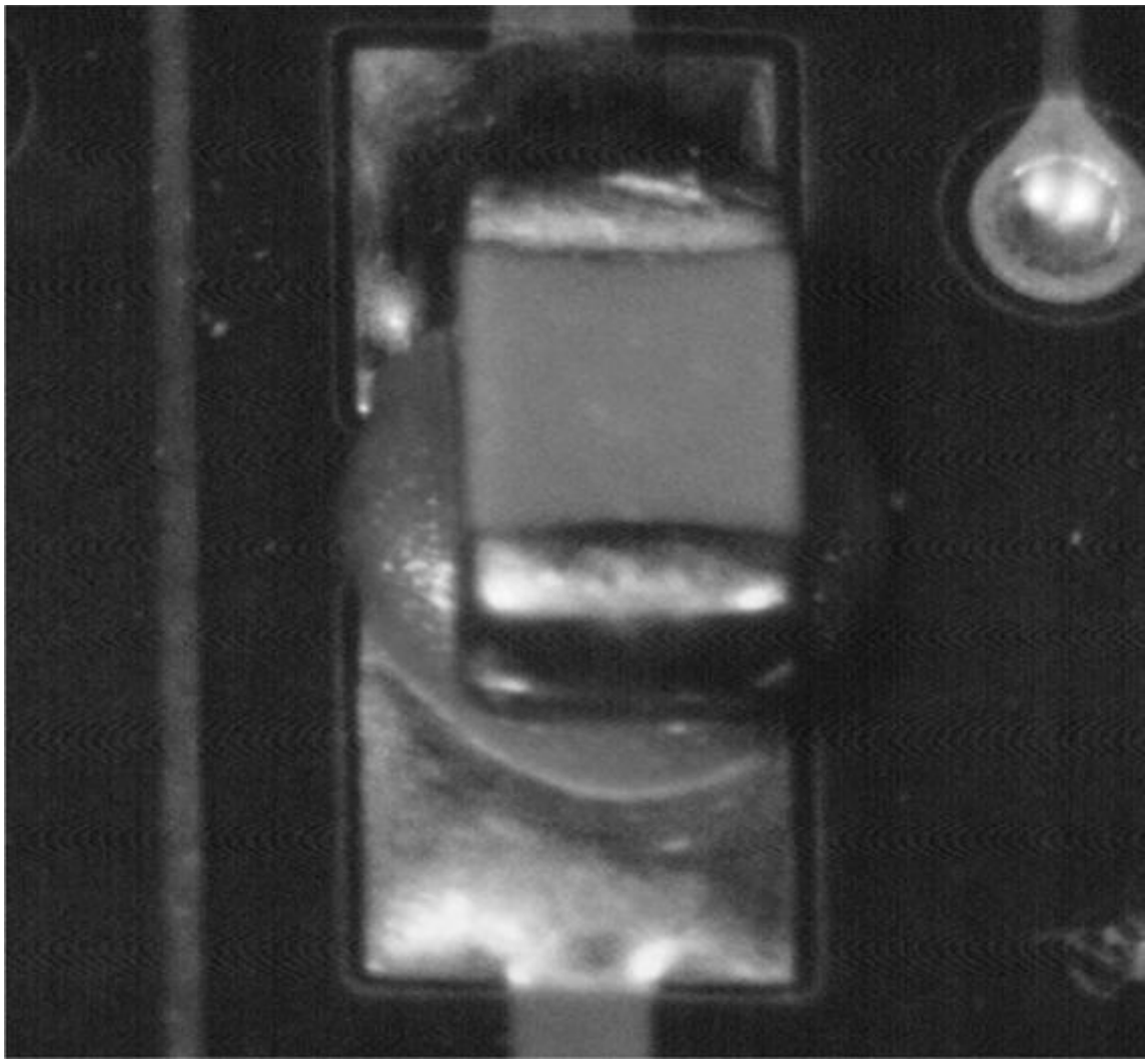


FIGURE 54.20 Adhesive visibly extended from under the component and visible in the terminal area. *(IPC)*

Normally in PTH component applications, adhesive is used to give large-profile and/or heavy components more mechanical stability. When adhesives are used in this manner, the following adhesive acceptance criteria apply:

- The adhesive must adhere to a flush-mounted axial component for 50 percent of the component length and 25 percent of its diameter on one side. The build-up of adhesive should not exceed 50 percent of the component diameter, and adhesion to the mounting surface must be evident (see Fig. 54.21).

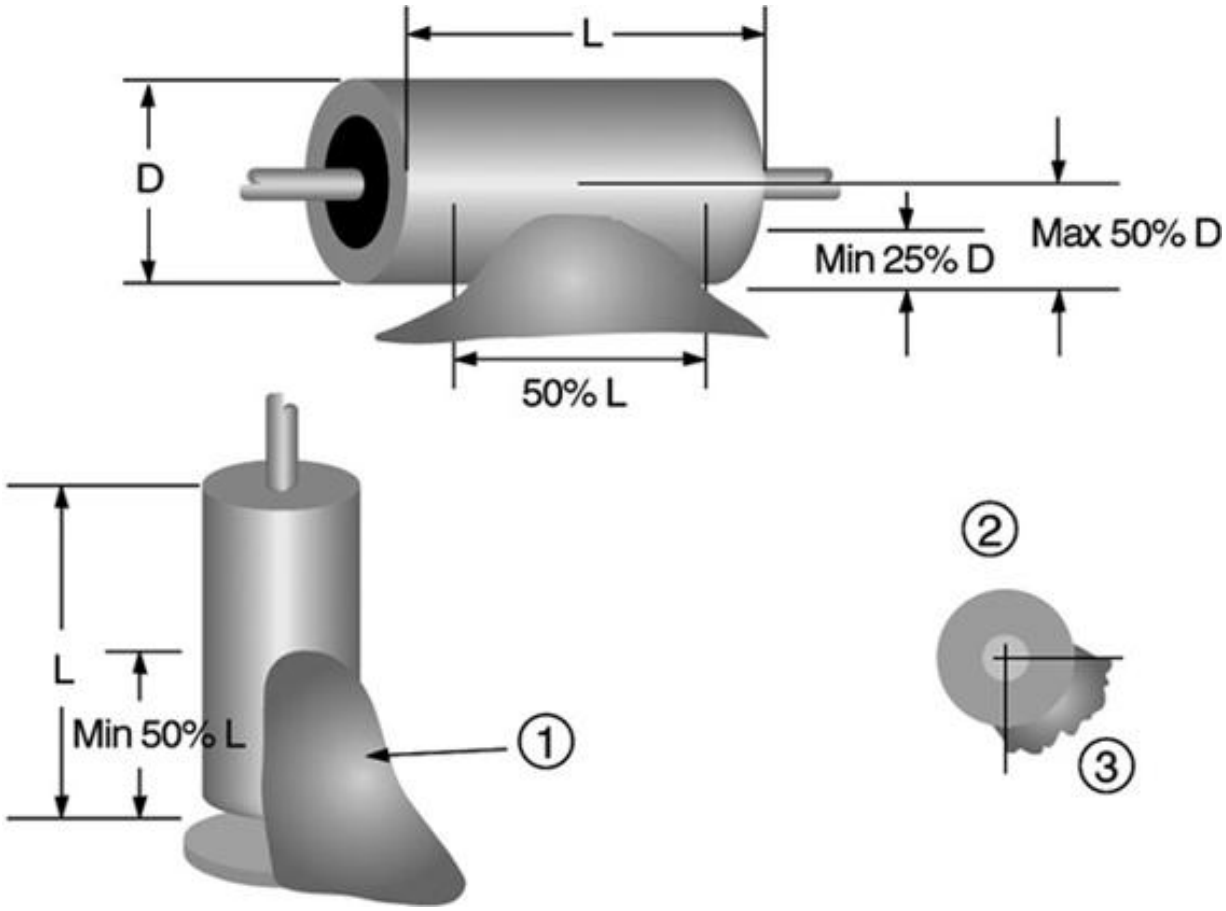


FIGURE 54.21 Adhesive on horizontal and vertically mounted components. (1) Adhesive, (2) Top view, (3) 25 percent circumference.

- The adhesive must adhere to a vertically mounted axial component for 50 percent of the component length and 25 percent of its circumference, and adhesion to the mounting surface must be evident (see Fig. 54.22).

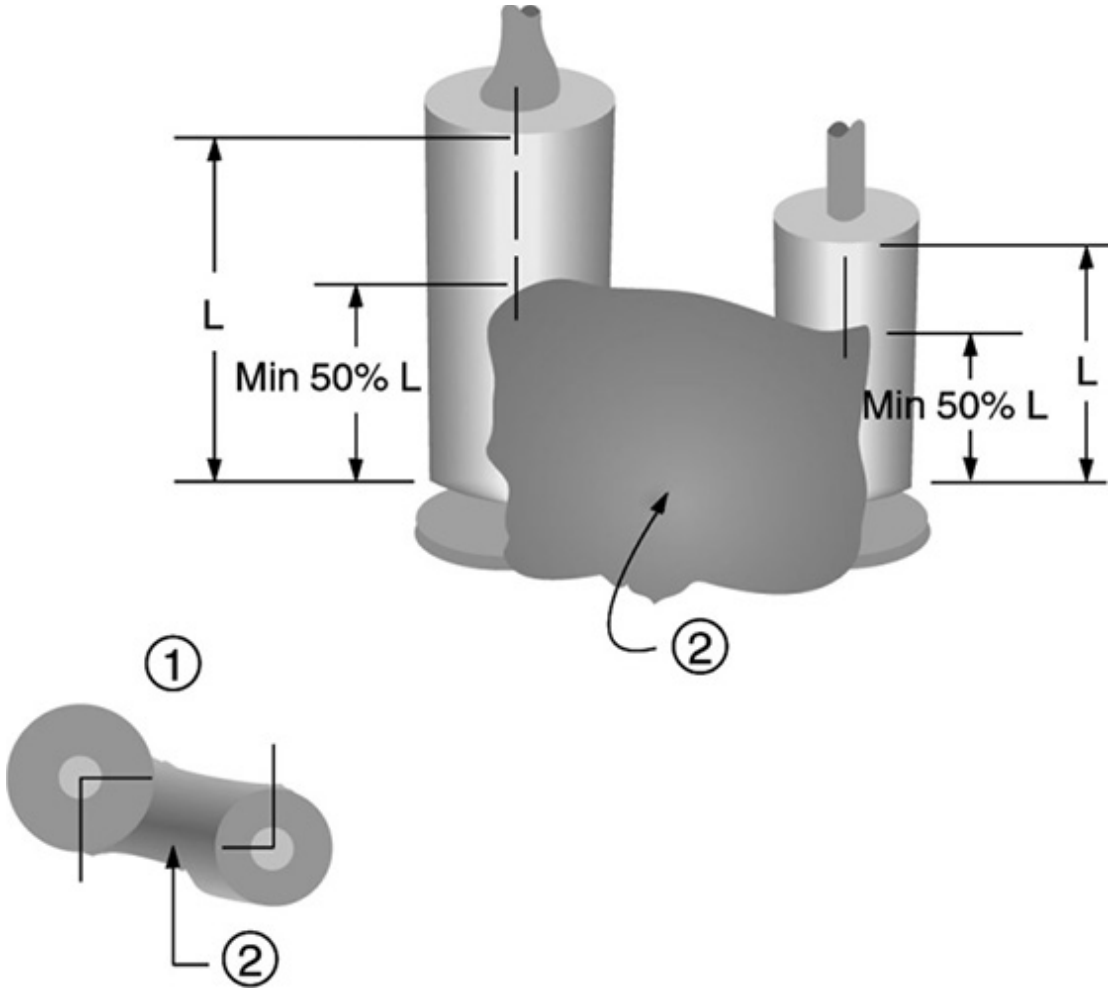


FIGURE 54.22 Adhesive on vertically mounted components. (1) Top view, (2) Adhesive. *(IPC)*

54.5 COMPONENT AND PCB SOLDERABILITY REQUIREMENTS

Component solderability, which includes the solderability of the PCB, is probably the most important single characteristic to consider when building PCBAs. To be successful in soldering PCBAs, good wetting must be achieved. It is an ongoing effort to ensure that all boards and electrical components purchased and received from suppliers maintain good solderability.

The key to success in this all-important task is to have an excellent working relationship with the suppliers and manufacturers of the components to ensure good, solderable components.

Until partnership relationships are achieved, there should be a sample of each lot or batch of components received that are subjected to solderability testing. This testing should be conducted in accordance with J-STD-002 and J-STD-003. These documents were written specifically to address solderability requirements for electronic assembly components and PCBs. The intent of the solderability testing is to qualify the surface to accept solder with less-than-optimum conditions. Additionally, artificial conditioning (aging) is used to simulate a normal aging period that the components might experience before use. Identification of weaker components can reduce the possibility of a solderability problem or production issues later on in the production cycle. Based on this lack of lead solderability, the components should be rejected and returned to the supplier, before they can be placed in the assembly process.

Packaging and handling of components are also important to maintain good solderability since many contaminants that could affect solderability can be transferred to solderable surfaces as a result of handling by equipment or personnel or the storage environment. Storage contamination may result from airborne contaminants, moisture, temperature, and also time. As tin-lead or lead-free component lead finishes age, they can oxidize, and this oxidation will affect solderability of the component. A rule of thumb used by many companies is to suspect the solderability of components two or more years old. In some cases, this age can be tracked easily for components marked with a date code. Other components too small to mark or that for some other reason are not marked with a date code cannot be traced as easily. Often companies keep records on the date of receipt and base the age of the component on this date.

Although these records may not be completely accurate, they still serve the purpose. If components are known to be over two years old, a new solderability sample may be pulled to determine whether the components are still usable before production. Often they are not usable due to oxidation, intermetalic growth, or some other contaminant that the component has been exposed to over time.

54.6 SOLDER-RELATED DEFECTS

All solder joints should exhibit wetting as shown by a concave meniscus between the component and PCB being soldered. The outline of the component being soldered should be easily determined. The most common solder defects produced by the soldering process are discussed in the following sections.

54.6.1 PTH Solder-Joint Minimum Acceptable Conditions

Table 54.6 shows the minimum acceptable PTH solder-joint criteria. Fig. 54.23 shows the basic elements of solder fill for all classes.

TABLE 54.6 PTHs with Component Leads: Minimum Acceptable Solder Conditions[a]

Criteria	Class 1	Class 2	Class 3
A. Vertical fill of solder[b,c] Note: Less than 100 percent older fill may not be acceptable in some applications: e.g., thermal shock. The user is responsible for identifying these situations to the manufacturer	Not Specified	75%	75%
B. Wetting on primary side (solder destination side) of lead and barrel Target for Classes 1,2, and 3 is 360° wetting present on land and barrel	Not Specified	180°	270°
C. Percentage of land area covered with wetted solder on primary side (solder destination side) The land area does not need to be wetted with solder on the primary side	0	0	0
D. Fillet and wetting on secondary side (solder source side) of lead and barrel	270°	270°	330°
E. Percentage of land area covered with wetted solder on secondary side (solder source side)	75%	75%	75%

Notes:

[a]Wetted solder refers to solder applied by the solder process.

[b]The 25 percent unfilled height includes both source and destination side depressions.

[c]Class 2 may have less than 75 percent vertical hole fill.

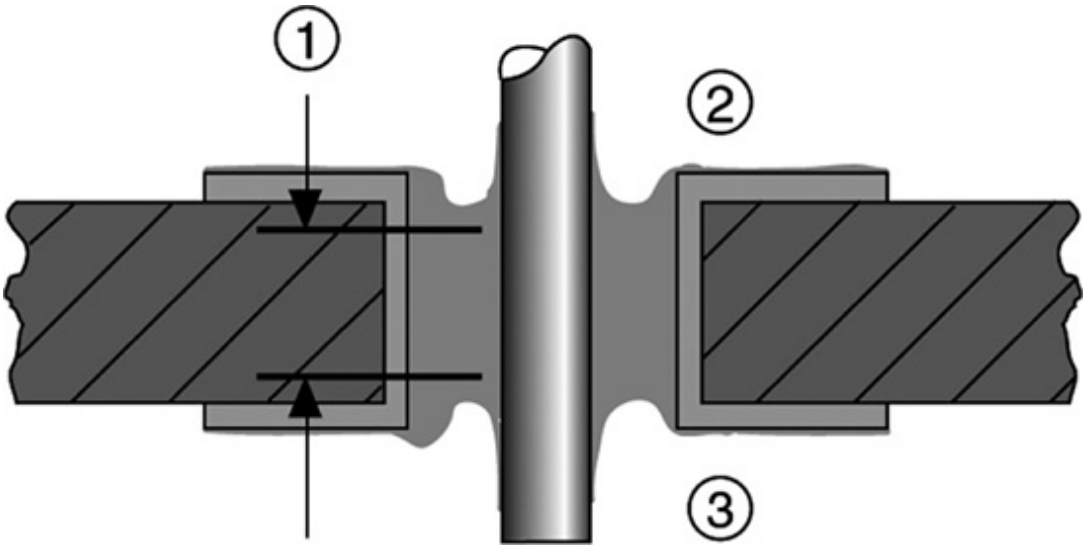


FIGURE 54.23 (1)–Vertical fill meets requirements of Table 54.6 (2)–Solder distination side (3)–Solder source side. *(IPC)*

54.6.2 Solder Balls or Solder Splash

Solder balls and splashes that violate minimum electrical design clearance, are not encapsulated in a permanent coating, or are not attached (soldered) to a metal surface are unacceptable (see Fig. 54.24).

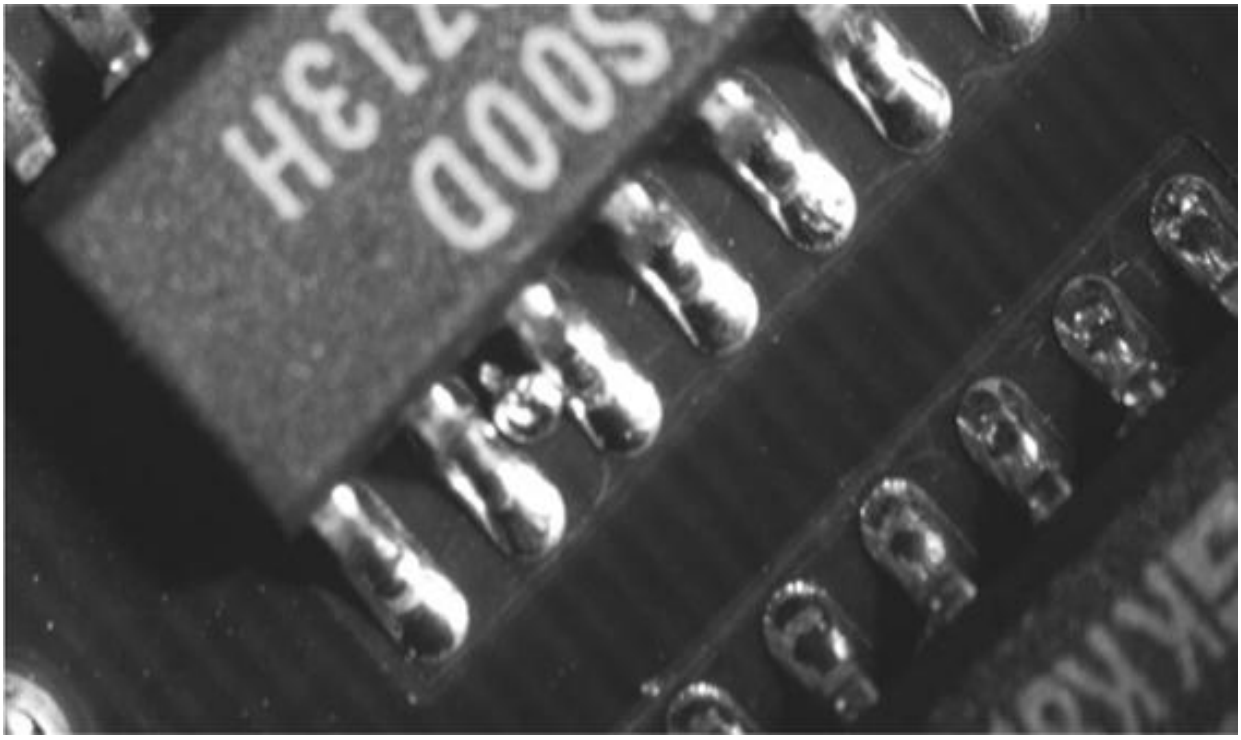


FIGURE 54.24 Solder ball causing a short circuit between pins in SOIC.

54.6.3 Dewetting and Nonwetting

Dewetting is a condition that results when molten solder coats a surface and then recedes to leave irregularly shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed (see Fig. 54.25). Nonwetting is the partial adherence of molten solder to a surface that it has contacted, while the basis metal remains exposed (see Fig. 54.26).

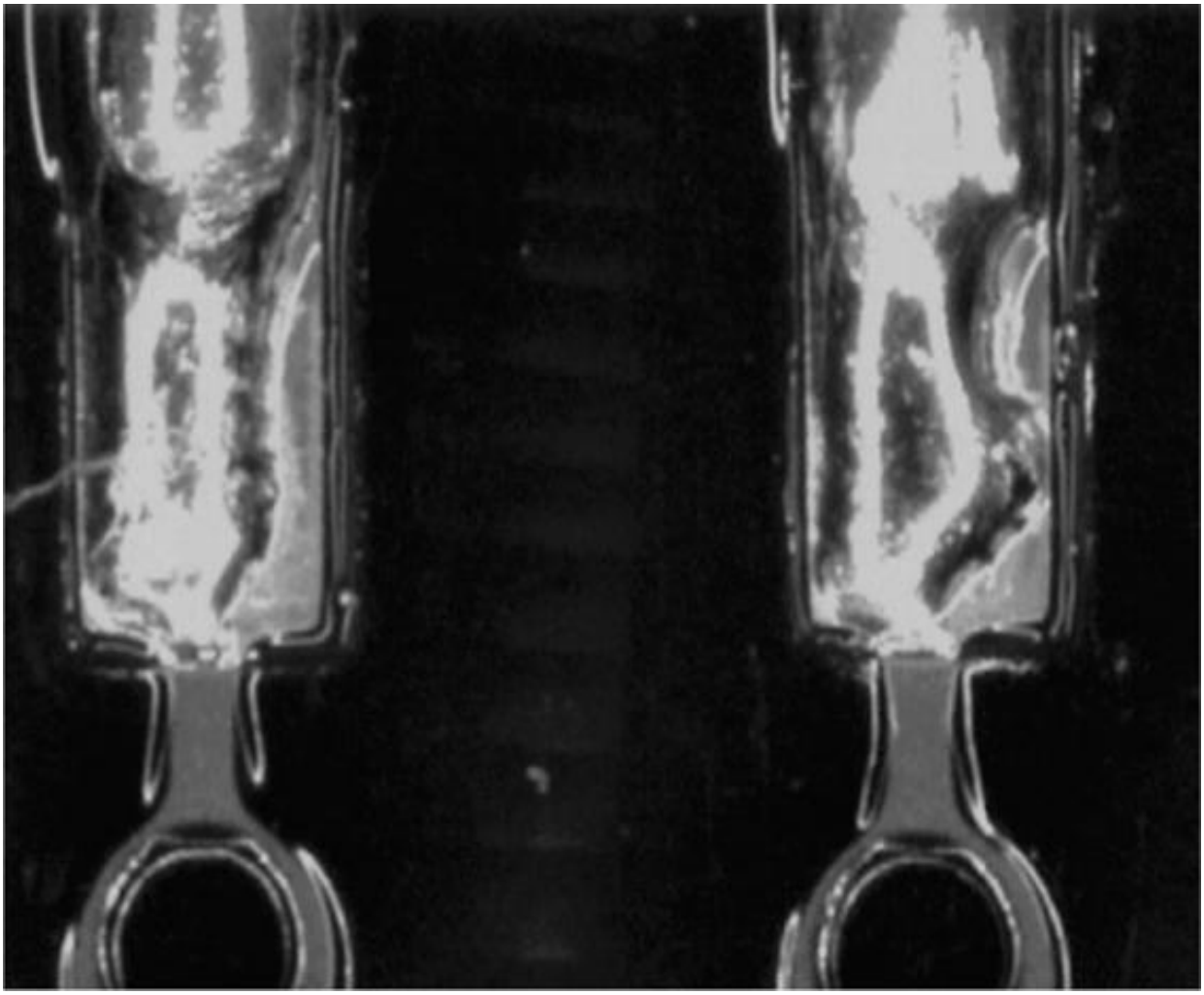


FIGURE 54.25 Example of dewetting. *(IPC)*

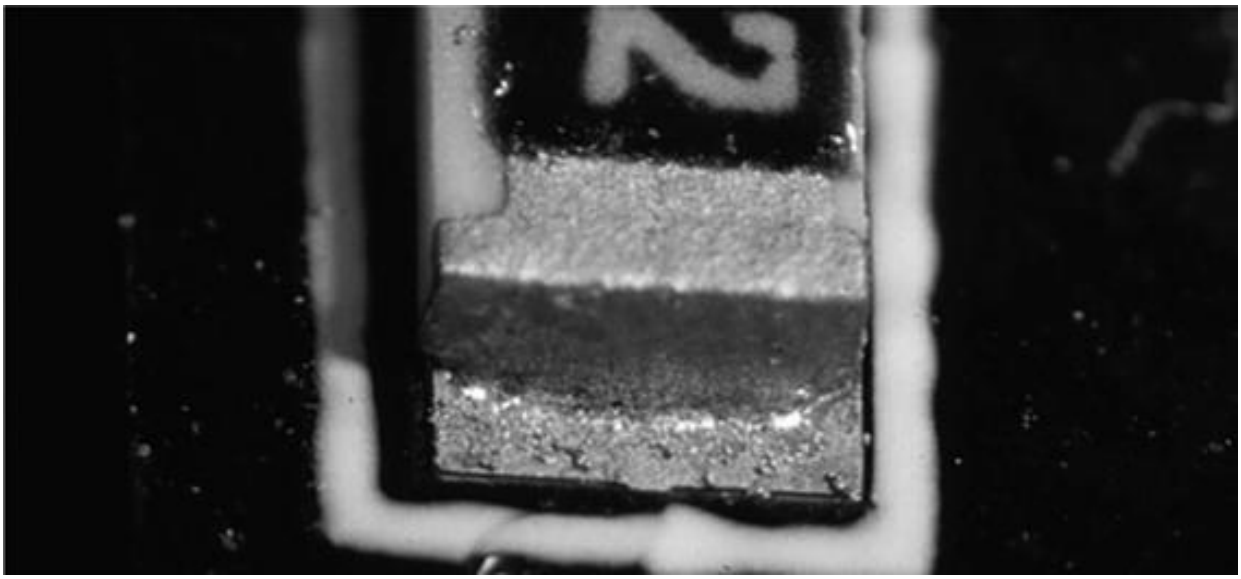


FIGURE 54.26 Example of non wetting. *(IPC)*

Dewetting and nonwetting of solder joints is generally caused by contaminants on either the component leads or on the PCB PTH or pads. A minimum of dewetting is allowed on solder joints assuming that the solder joint meets minimum requirements as defined in Table 54.6 and Sect. 54.4.2 by component package type, and good wetting is evident on the portion of the solder joint that does not display dewetting. Nonwetting is unacceptable since adequate wetting is not achieved and indicates a serious solderability problem on the component or the PCB.

54.6.4 Missing and Insufficient Solder

Missing solder is an obvious unacceptable condition since solder provides electrical continuity and some measure of mechanical attachment of the component to the PCB.

Insufficient solder becomes an unacceptable condition for SMT components when the minimum solder fillet requirements defined in Sec. 54.4.2 are not achieved. Insufficient solder becomes unacceptable for PTH components when the minimum requirements of section 54.6.1 and Table 54.6 are not achieved.

54.6.5 Solder Webbing and Bridging

Solder bridged between electrically noncommon conductors creates a shorting condition and is an unacceptable condition (see Fig. 54.27). Solder webbing is a continuous film of solder that is parallel to, but not necessarily adhering to, a surface that should be free of solder. Solder webbing is also an unacceptable condition (see Fig. 54.28).

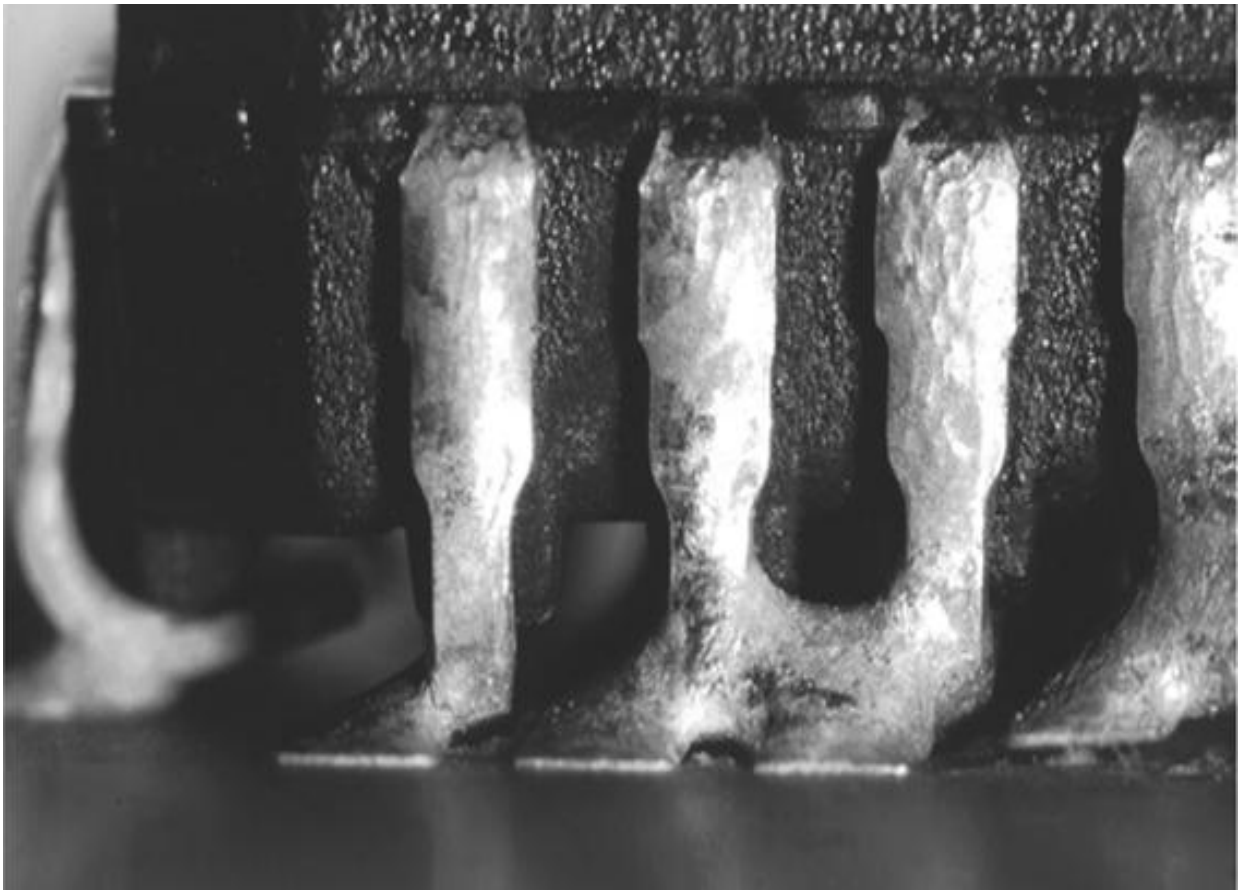


FIGURE 54.27 Solder connection across conductors that should not be joined. *(IPC)*

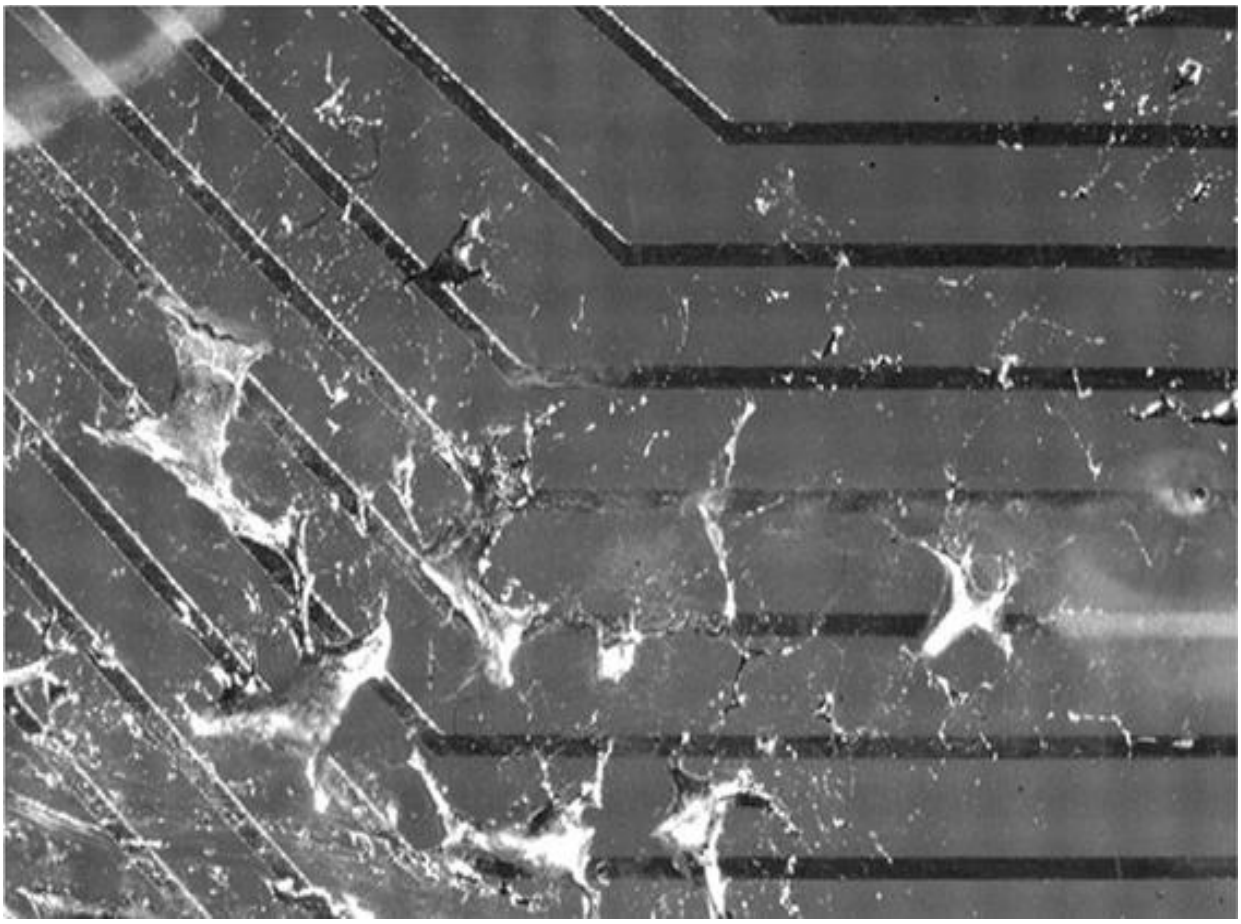


FIGURE 54.28 Examples of solder splashes and webbing. *(IPC)*

For components with leads, with the exception of criteria stated in sec. 54.4.2.4, solder cannot come into contact with the component body or end seal. Solder contacting the component body or end seal is generally unacceptable.

54.6.6 Lead Protrusion Problems

Measurement of lead protrusion is defined as the distance from the top of the PCB land to the outermost part of the component lead, which can include any solder projection from the lead.

Solder projections (icicles) are unacceptable if they violate lead protrusion maximum requirements or electrical clearance, or if they pose a safety hazard; otherwise, solder

projections are an acceptable condition on both SMT and PTH components (see Fig. 54.29).

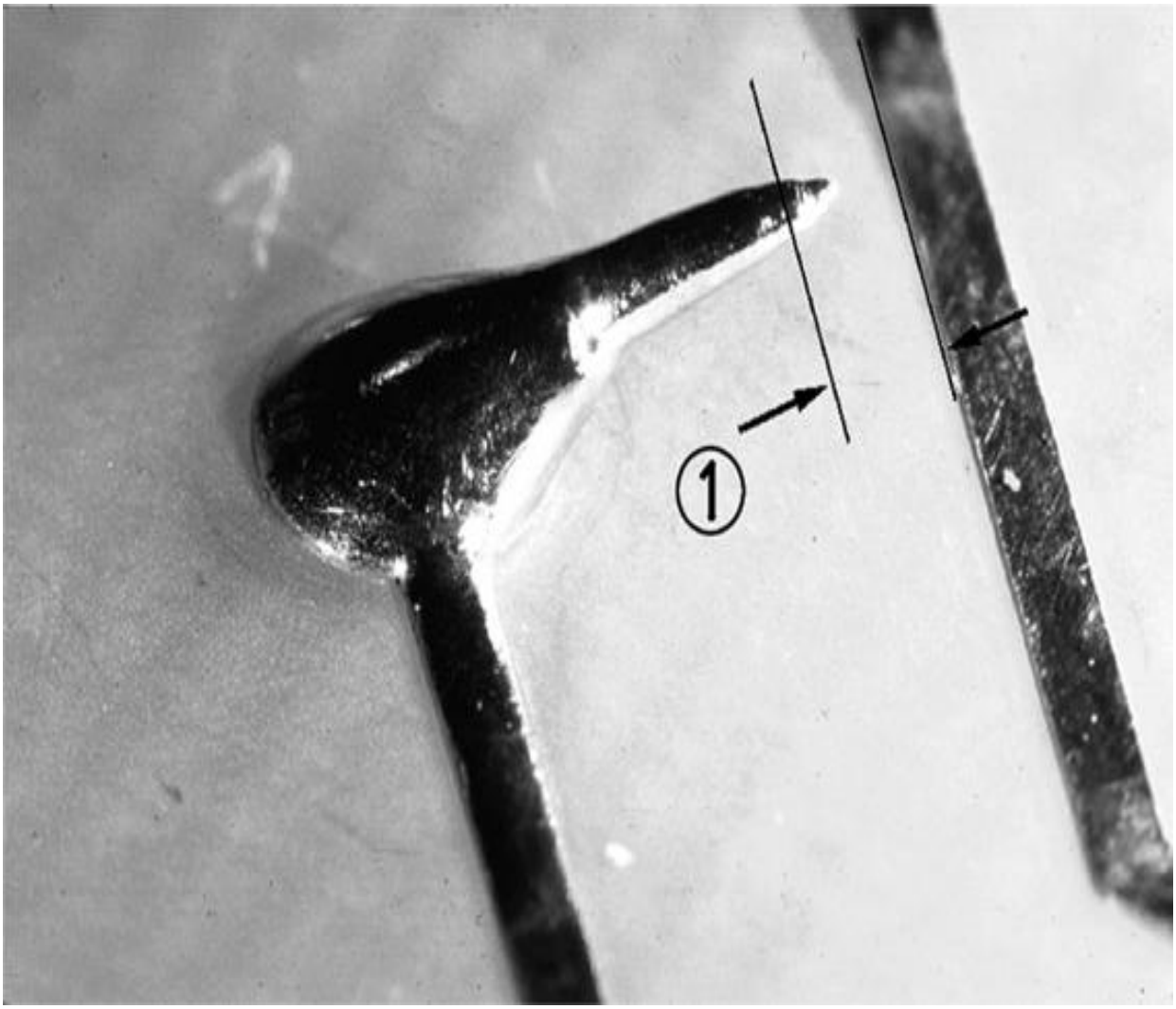


FIGURE 54.29 Projection violates minimum electrical clearance (1). *(IPC)*

For single-sided PCBAs, lead or wire protrusion must be visible in the solder for Classes 1 and 2, and must allow a clinch for Class 3. For double-sided and multilayer PCBAs in all classes, the minimum lead protrusion is for the lead end to be visible in the solder. The maximum lead protrusion for Class 1 is that there be no danger of shorts when the PCBA is used in its assembly application. For Class 2, the maximum

lead protrusion is 2.5 mm, and for Class 3 the maximum lead protrusion is 1.5 mm (see Fig. 54.30).

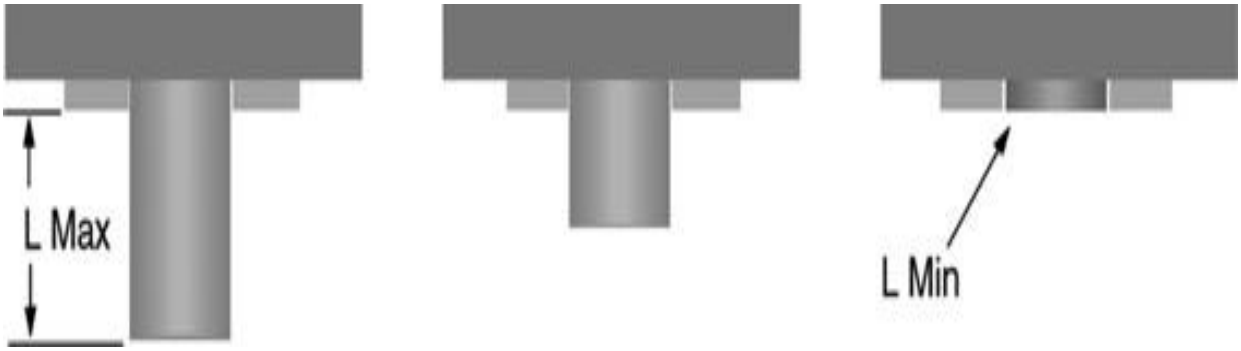


FIGURE 54.30 Lead protrusion violates minimum clearance requirements. Lead protusion exceeds maximum design height requirements. *(IPC)*

54.6.7 Voids, Pits, Blowholes, and Pinholes

Solder cavities (voids, pits, blowholes, pinholes) are acceptable for Class 1 and process indicators for Classes 2 and 3, provided the lead and land/pad are wetted and solder fillets meet requirements specified in Table 54.6.

54.6.8 Disturbed or Fractured Solder Joints

Solder joints may not be disturbed due to movement of the solder connection during solidification. However, a rough, granular, or uneven appearance, provided the wetting coverage criterion in Table 54.1 is met, is acceptable. Solder connections accomplished using many of the lead-free solder alloys and surface preparations will normally exhibit the rough or granular appearance more than eutectic tin-lead. Solder joints that are fractured or cracked are unacceptable for all classes of equipment.

Cutters cannot damage solder joints in which leads have been trimmed after soldering, due to physical shock transmitted through the lead. If lead cutting is required after soldering, the solder joint must be reflowed or visually inspected at 10 × magnification to ensure that the cutting operation did not damage the solder connection. No fractures or cracks are allowed between the lead and solder (see Fig. 54.31).

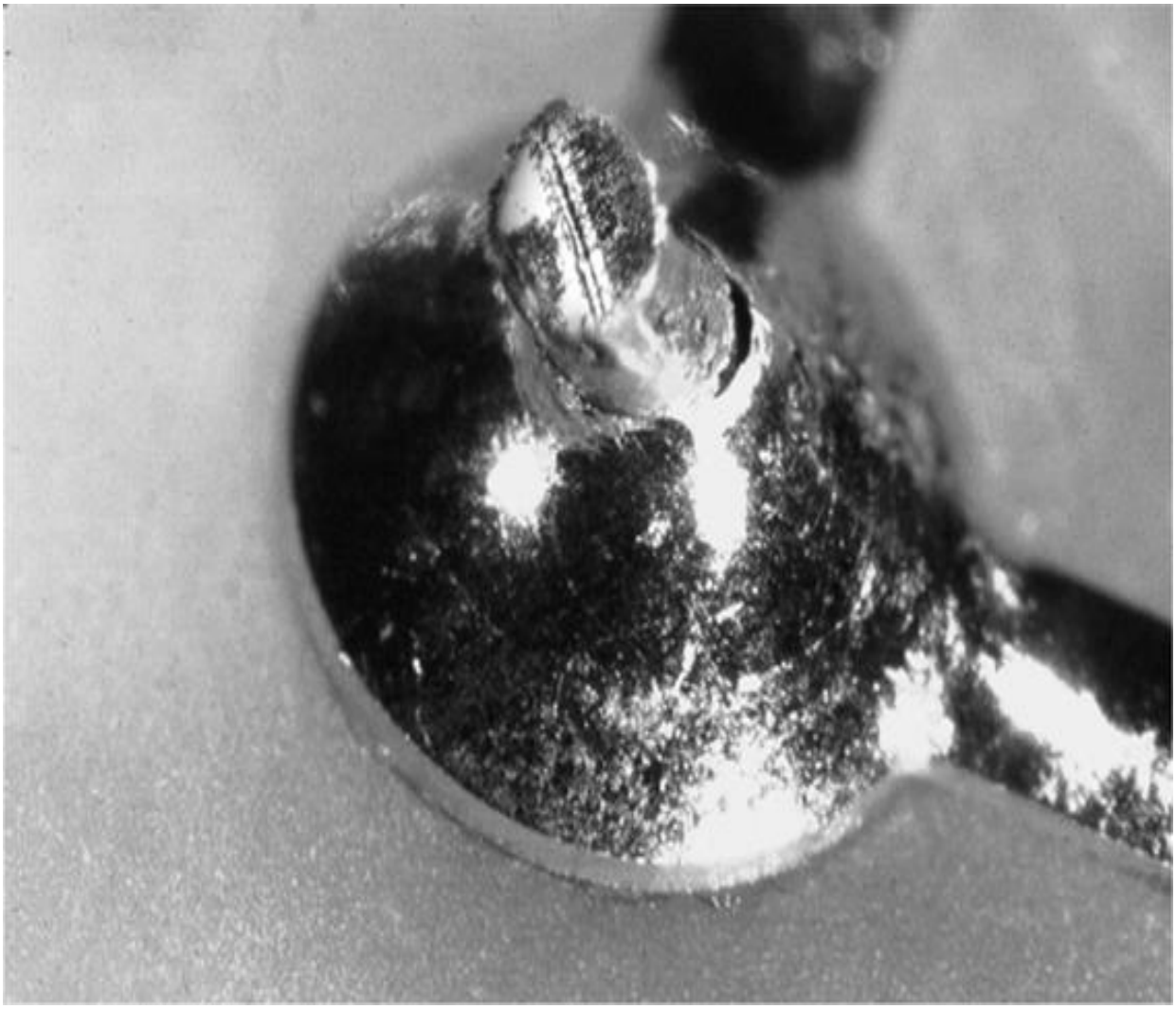


FIGURE 54.31 Example of disturbed solder joint on through-hole component joint. Note evidence of fracture between lead and solder fillet. *(IPC)*

54.6.9 Excess Solder

Excess solder conditions that produce a solder fillet that is slightly convex or bulbous and in which the lead is no longer visible are considered defects for unsupported hole lead termination. The solder should not flow onto the body of SMT components or touch the component body for through-hole components.

54.6.10 Solder Requirements for Vias

Plated-through via holes used only for interfacial connection do not need to be filled with solder. To prevent solder fill, manufacturers usually place temporary or permanent masks over the vias during the soldering process. PTHs or vias without leads when exposed to solder should meet the following acceptability requirements:

- The target condition is to have the holes completely filled with solder and the top of the lands showing good wetting.
- The minimum acceptable condition is to have the sides of the PTH wetted with solder.
- Solder that has not wet the sides of the PTH is considered a process indicator and product is not rejected (see Fig. 54.32).

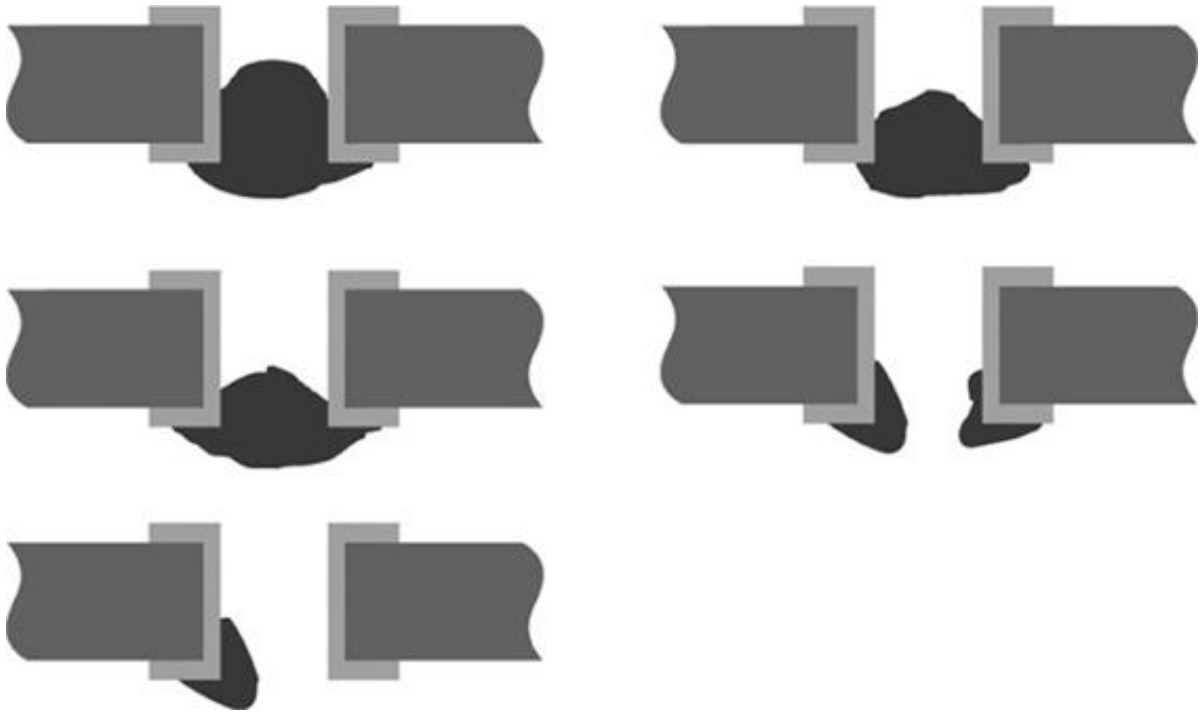


FIGURE 54.32 Via hole solder fill requirements. *(IPC)*

54.6.11 Soldering to Terminals

When soldering wires to terminals, the lead outline must be visible and good wetting between the wire and terminal must be evident to be acceptable. The wire insulation gap can be near zero if the insulation has not melted into the solder joint. Slight melting of the insulation is acceptable. If the insulation gap is too large and allows potential shorting of wire to an electrically noncommon conductor, the joint is unacceptable. If the wire insulation is severely burned and the melt by-product intrudes into the solder joint, the joint is unacceptable

For round post terminals, the contact of wrap must be 180° for Class 3 and 90° for Classes 1 and 2. Most of the other terminal types, such as pierced terminals, require 90° of wire wrap (see Fig. 54.33).

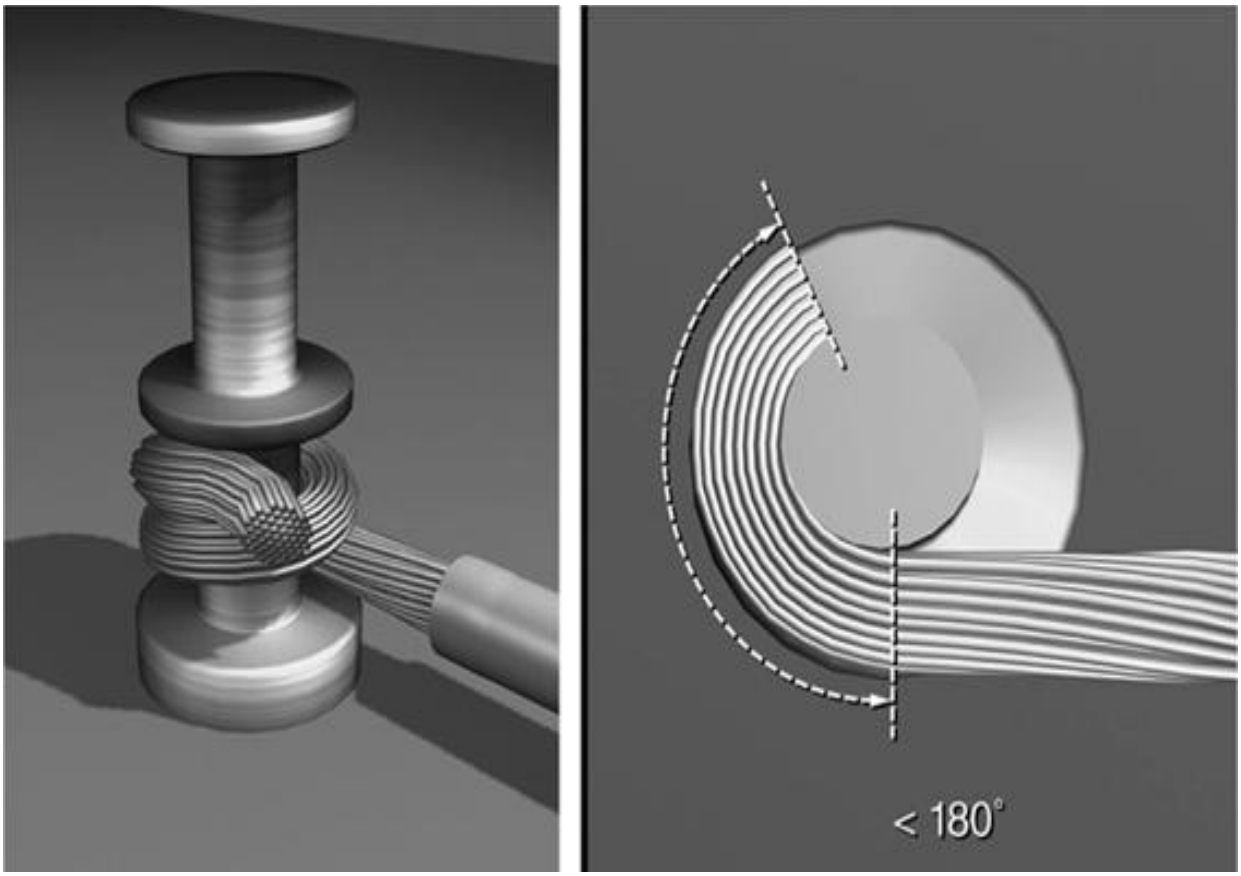


FIGURE 54.33 Minimum requirements for wrap of exposed wire on terminal for acceptable solder joint by class.

For solder cup terminations, the wire should be fully inserted to the bottom of the cup and solder fill must be greater than 75 percent of the milled edge.

54.7 PCBA LAMINATE CONDITION, CLEANLINESS, AND MARKING REQUIREMENTS

54.7.1 Laminate Conditions

Laminate defect conditions may be caused by the laminator, PCB fabricator, or assembly of the PCB. The major laminate

conditions seen are measling, crazing, blistering, delamination, weave exposure, and haloing.

54.7.1.1 Measling and Crazing. Measling is an internal condition occurring in laminated base material in which the glass fibers are separated from the resin at the weave intersections. This condition manifests itself in the form of white spots or crosses below the surface of the base material and is usually related to thermally induced stress.

Crazing is an internal condition occurring in laminated base material in which the glass fibers are separated from the resin at the weave intersections. This condition manifests itself in the form of connected white spots or crosses below the surface of the base material and is usually related to mechanically induced stress (see Fig. 54.34).

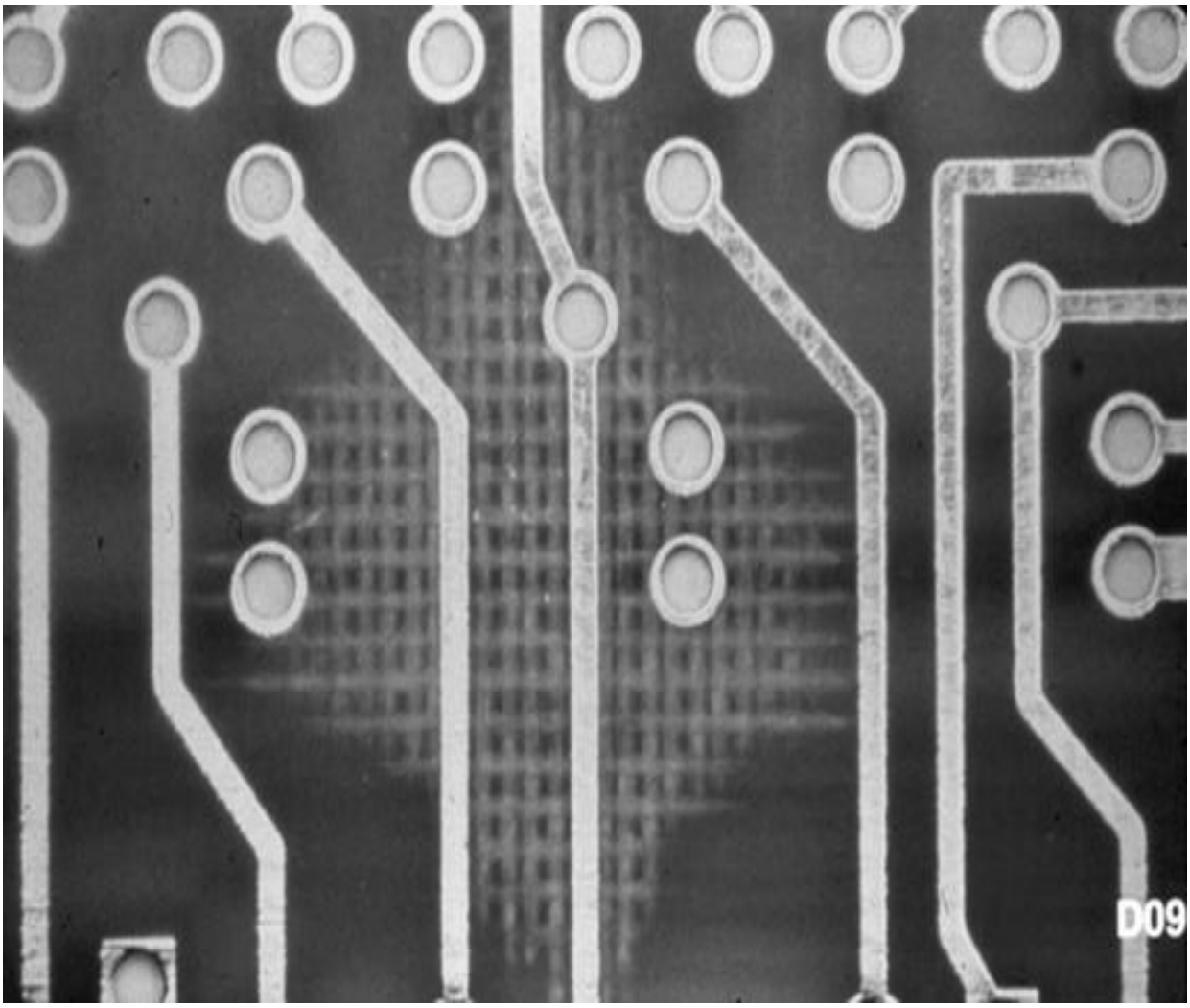


FIGURE 54.34 Crazing in base laminate. Crazing exceeds 50 percent of the physical space between internal conductors. *(IPC)*

Measling or crazing that occurs as a result of an inherent weakness in the laminate is a warning of a potentially more serious problem. If measling or crazing occurs in the assembly process, it usually will not propagate further. Measling is considered a defect for Classes 2 and 3 if the measle condition extends more than 50 percent of the span between internal conductors. The concern is in regard to the ability of the laminate to maintain dielectric integrity after exposure to high humidity and active chemistries and environments.

By the time that a PCB enters an assembly process, the operator who observes measling or crazing cannot determine the source of the problem. This fact places even more importance on getting high-quality PCBs from suppliers. This can be done through increased receiving inspection, source inspections, or a comprehensive qualification program and partnership with suppliers. In such a program, process control is exercised in the PCB fabrication, and parametric data from the supplier are sent to the buyer to review for compliance with requirements. This kind of information can also be used to justify a dock-to-stock program if desired.

54.7.1.2 Blistering and Delamination. Blistering is a localized swelling and separation between any of the layers of the base material or between the material and the metal cladding. Delamination is a separation between any of the layers of the base material or between the base material and the metal cladding. In contrast to measles that do not propagate, blisters and delamination conditions can increase in size with use.

Blistering and delamination cannot exceed 25 percent of the distance between PTHs or subsurface conductors (see Fig. 54.35).

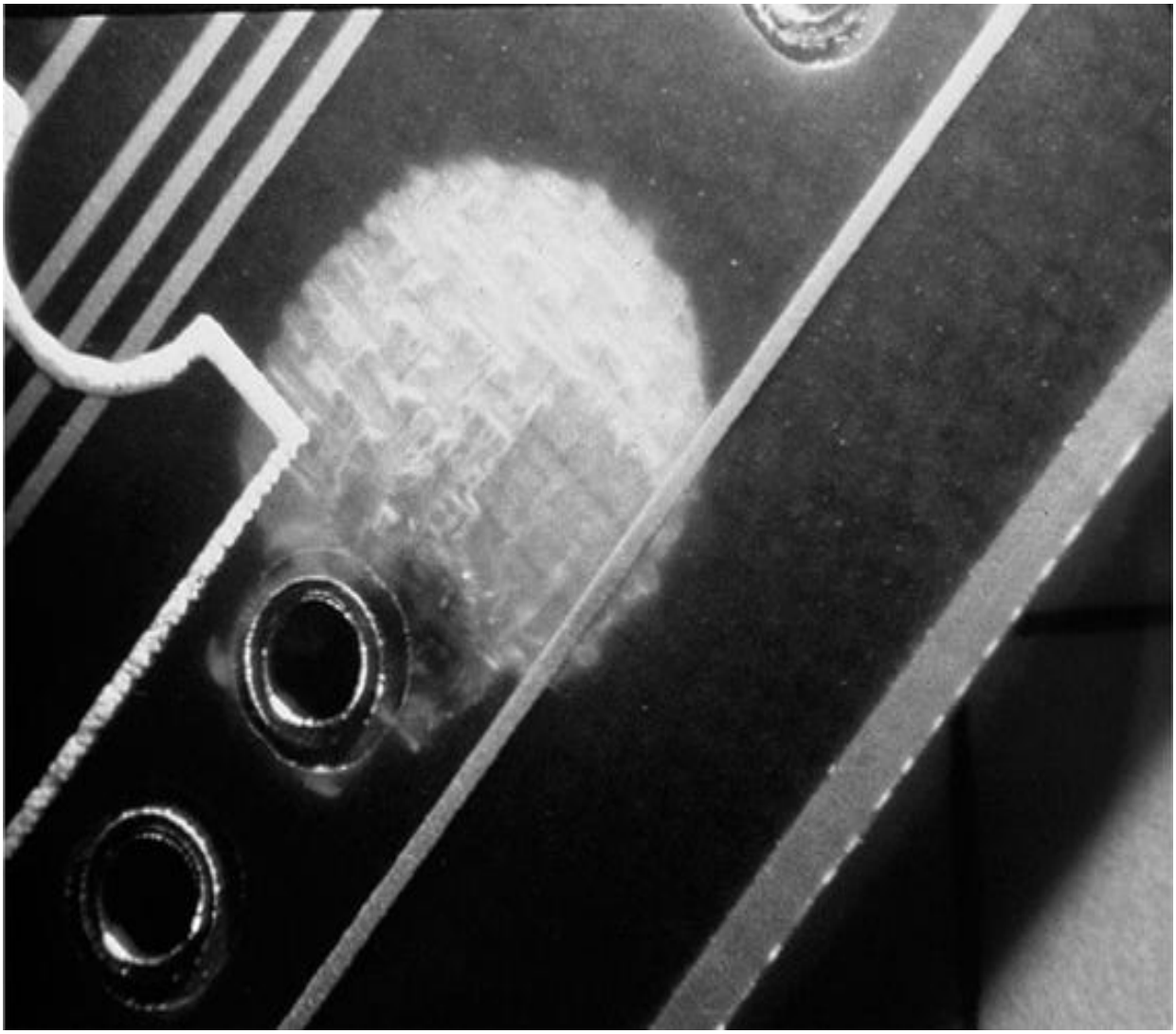


FIGURE 54.35 Example of blister in base material. *(IPC)*

54.7.1.3 Weave Exposure. Weave exposure is a surface condition of base material in which the unbroken fibers of woven glass cloth are not completely covered by resin. Weave exposure is acceptable if it does not reduce dielectric spacing below the minimum electrical clearance.

54.7.1.4 Haloing and Edge Delamination. Haloing occurs on or below the surface of the base material, appearing as a light area around holes or other machined areas. This condition is acceptable if the penetration of the haloing or edge delamination does not reduce edge spacing

more than 50 percent of that specified in the drawing or other documentation or 2.5 mm maximum.

54.7.2 PCBA Cleanliness

Board cleanliness is needed to ensure sufficient removal of contaminants that could affect functionality at present or in the future. Some contaminants can actually promote growth of undesirable substances on the PCBA that can cause shorting or corrosion that would affect the PCBA’s electrical functional integrity and dielectric properties over a period of time. These contaminants can be in the form of surface dendrites, internal conductive anodic filaments, and so on.

No visible residue from cleanable or any activated fluxes is allowed. Production operations may not be required to remove cleanable residues if qualification testing is performed that demonstrates no need for cleaning the assembly. No-clean or low-residue flux chemistries may be allowed during the soldering process. However, it is critical that the cleanliness of the elements such as the bare boards and components be specified, controlled, and closely monitored; otherwise, the contaminant build-up can far exceed allowable limits for the end item’s functional performance.

For processes utilizing potentially corrosive rosin based fluxes, simple test options to determine cleanliness such as resistance of solvent extract (ROSE) tests can be used. Other more significant tests may be required to determine the residue properties of organic residue fluxes, such as those commonly used during hot air solder leveling (HASL) of boards. The most common of these are ion chromatography tests that can characterize the residuals and their potential hazards to the product.

In the event of test failure, immediate process corrections for the cleaning process or elimination of the source of

residues must be accomplished before any additional product is assembled.

Particulate matter such as dirt, lint, dross, lead clippings, and such is not acceptable on PCBAs. Metallic areas or hardware on the PCBAs may not exhibit any crystalline white deposits, colored residues, or rusty appearance.

54.7.3 PCBA Marking Acceptability

Marking provides both product identification and traceability. It aids in assembly, in-process control, and field repairs. The methods and materials used in marking must serve the intended purposes and must be readable, durable, and compatible with the manufacturing processes as well as the end use of the product.

Fabrication and assembly engineering drawings should be the controlling documents for the locations and types of markings on PCBAs. Marking on components and fabricated parts should withstand all tests, cleaning, and assembly processes to which the item is subjected and must remain legible. Acceptability of marking is based on whether it is legible. If a marking is legible and cannot be confused with another letter or number, it is acceptable. Components and fabricated parts do not have to be installed so that reference designators are visible after installation. Missing, incomplete, or illegible characters in markings are unacceptable.

54.8 PCBA COATINGS

It should be noted that not all PCBA designs use conformal coating; however, when used, conformal coating must meet the following acceptability criteria. All PCBAs that utilize top- or bottom-layer etch (trace) runs have a solder mask over them if a solder wave or static solder bath process is used to

solder components onto the PCB. Without the solder mask, the solder would bridge between many solder wettable surfaces, causing short circuits.

54.8.1 Conformal Coating

Conformal coating is an insulating protective covering that conforms to the configuration of the objects coated when it is applied to a completed PCBA. The purpose of conformal coating is to provide a temporary barrier to environmental exposure of chemicals, humidity, and condensation. It is also a barrier from surface contact of contaminants caused by handling, and can provide physical support for components from shock and vibration. It is not, however, a hermetic seal and is eventually permeable. To be most effective, conformal coatings should be homogeneous and transparent. Most coatings will contain an ultraviolet (UV) tracer to make inspection easier through the use of a black light. The conformal coating should be properly cured and not exhibit tackiness. Defects associated with conformal coating are as follows:

- Applied where not required
- Not applied where required
- Bridging of conductors due to:
  - Mealing (adhesion)
  - Voids
  - Dewetting
  - Cracks
  - Ripples
  - Orange peel/fisheye
- Inclusions
- Discoloration

- Incompletely cured
- Wicking into connectors or mating surfaces

Conformal coating thickness requirements for five types of coatings are listed in Table 54.7. The thickness is commonly measured on a coupon that has been processed with the assembly.

TABLE 54.7 Coating Thickness

Type	Material	Thickness
AR	Acrylic Resin	0.03–0.13 mm (0.00118-0.00512 in.)
ER	Epoxy Resin	0.03–0.13 mm (0.00118-0.00512 in.)
UR	Urethane Resin	0.03–0.13 mm (0.00118-0.00512 in.)
SR	Silicone Resin	0.05–0.21 mm (0.00197-0.00827 in.)
XY	Paraxylyene Resin	0.01–0.05 mm (0.00039-0.00197 in.)

54.8.2 Solder Resist

Solder resist or solder mask is a heat-resistant film coating used to provide mechanical shielding during soldering operations. Solder resist material may be applied as a liquid or a dry film.

Solder resist would be ineffective and considered a defect when there are blisters, scratches, or voids that bridge noncommon circuits, or if the exposure has the potential to allow solder bridges. It could be considered a process indication if blisters or flaking expose bare copper.

54.9 SOLDERLESS WRAPPING OF WIRE TO POSTS (WIRE WRAP)

Many applications of wire wrap are still utilized in equipment design, and standards of acceptance should be consistent. Standards of acceptance in this area are shown in IPC-A-610 and in other standards.

54.9.1 Wrap Post

The wrap post cannot be bent or twisted before or after the wire is wrapped to the post. The wrap straightness may not exceed approximately one post diameter or thickness from its perpendicular position.

54.9.2 Wire Wrap Connection

Table 54.8 shows the number of wire wrap turns of insulated and uninsulated wire used on the wrapped connection. The connection is made using automatic or semiautomatic wire wrapping devices. For this requirement, countable turns are those turns of bare wire or insulated wire in intimate contact with the corners of the terminals starting at the first contact with a terminal corner and ending at the last contact with a terminal corner (see Fig. 54.36).

TABLE 54.8 Minimum Turns of Bare Wire

Wire Gauge	Turns
30	7
28	7
26	6
24	5
22	5
20	4
18	4

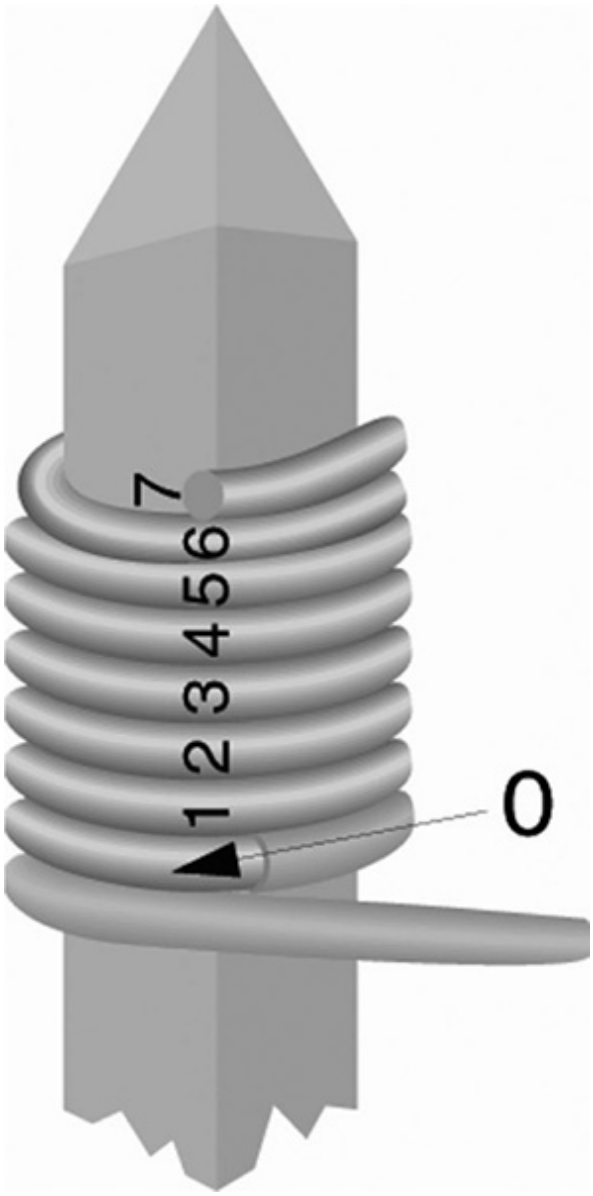


FIGURE 54.36 Solderless wrap acceptability. *(IPC)*

Maximum turns of bare and insulated wire are governed by the tooling configuration and space available on the terminal. The minimum countable turns must be as stated in Table 54.8. Electrical clearance between terminals as specified by engineering documentation must be maintained. Wire ends should in no case project to the extent that the required electrical clearance is compromised. The wire end should never project more than 0.12 in. (one wire diameter for Class 3) away from the terminal.

The wrapped conductors should be free of gaps (that is, each wrap should be in contact with the previous wrap), with turns not overlapping. The first and last one-half turns may have a space between turns, provided that the space does not exceed one diameter of the conductor wire. Excluding the first and last one-half-turns, the wrapped conductors may have a single space between them, if the opening does not exceed one-half the nominal diameter of uninsulated wire (see Fig. 54.37).

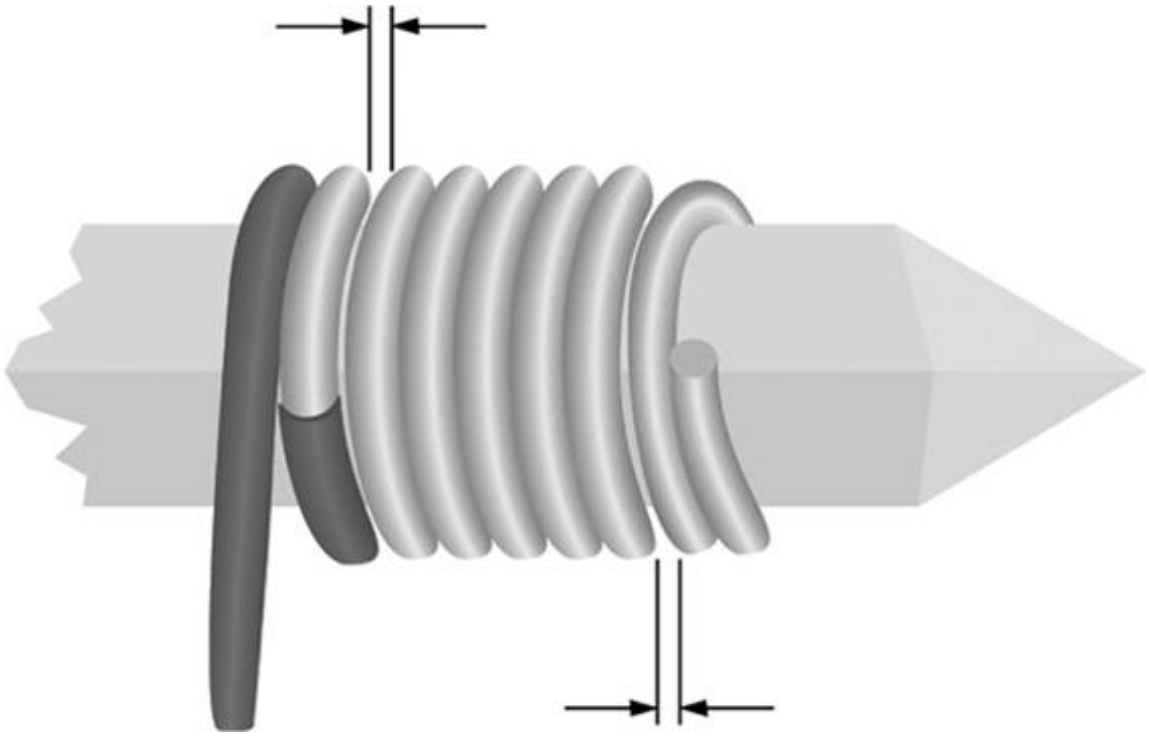


FIGURE 54.37 Solderless wrap with more than one space. Acceptability depends upon Class of product. *(IPC)*

54.9.3 Multiple Wire Wrap Spacing

Typically no more than three wires are wrapped to a single post. When more than one wrap is used on a single post, there should be visible clearance between consecutively wrapped wires. The final wire wrap turn on a post must not extend beyond the working length of the post (see Fig.

54.38). The first insulated turn of a higher-level wire wrap may overlap the last turn of uninsulated wire on a lower-level wrap by a maximum of 1 turn for Class 3.

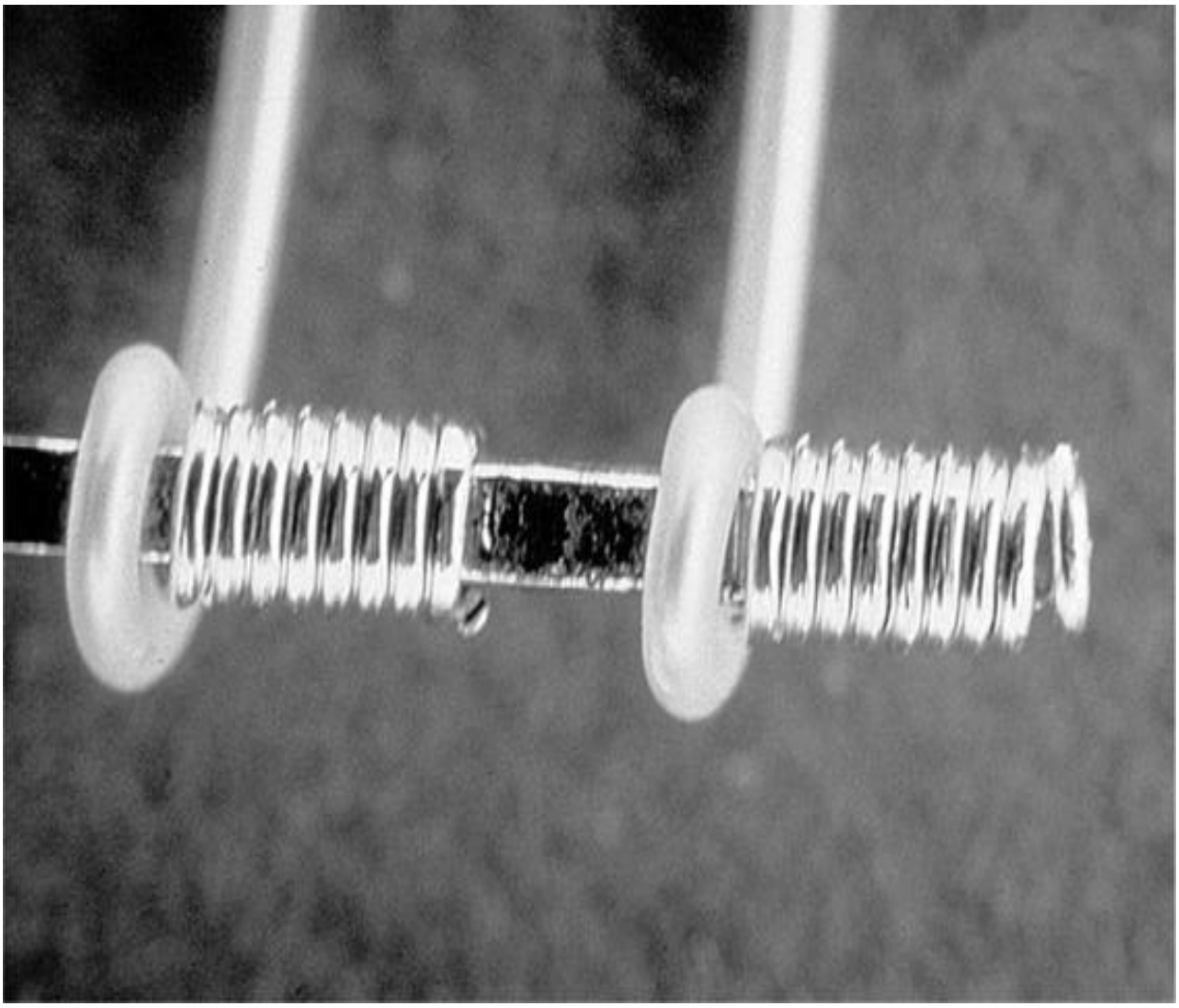


FIGURE 54.38 Multiple solderless wrap example. *(IPC)*

54.10 PCBA MODIFICATIONS

All modifications to PCBAs should be defined and detailed in approved engineering and/or methods documents. Jumper wires are considered components and are defined by

engineering documentation for routing, termination, staking, and wire type.

54.10.1 Cut Traces

Trace cuts should be at least 0.030 in. wide, with all loose material removed. They should also be sealed with an approved sealant to prevent absorption of moisture.

Care should be taken when removing etch from PCBs to prevent damaging the laminate material.

54.10.2 Lifted Pins

Lifted pins should be cut short enough to prevent the possibility of being shorted to the pad from which they were lifted should they be pushed back down. If the component hole from which the pad was lifted does not contain a jumper wire, it should be filled with solder.

54.10.3 Jumper Wires

Jumper wires may be used on all classes of equipment electronic assemblies and in thick-film hybrid technology. The wire may be terminated in PTHs, on terminal standoffs, on circuit lands, or on component leads. It should be noted for Class 3 equipment that a wire cannot be placed into the same PTH with a component lead.

Recommended jumper wire is solid, insulated, plated copper wire. It should be the smallest wire diameter that can reliably carry the required current, and the insulation should be capable of withstanding soldering temperatures.

Jumper wires should be routed in the shortest x-y route possible (see Fig. 54.39). Wire routing must be documented

for each part number. Assemblies having the same part number must be routed in the same pattern.

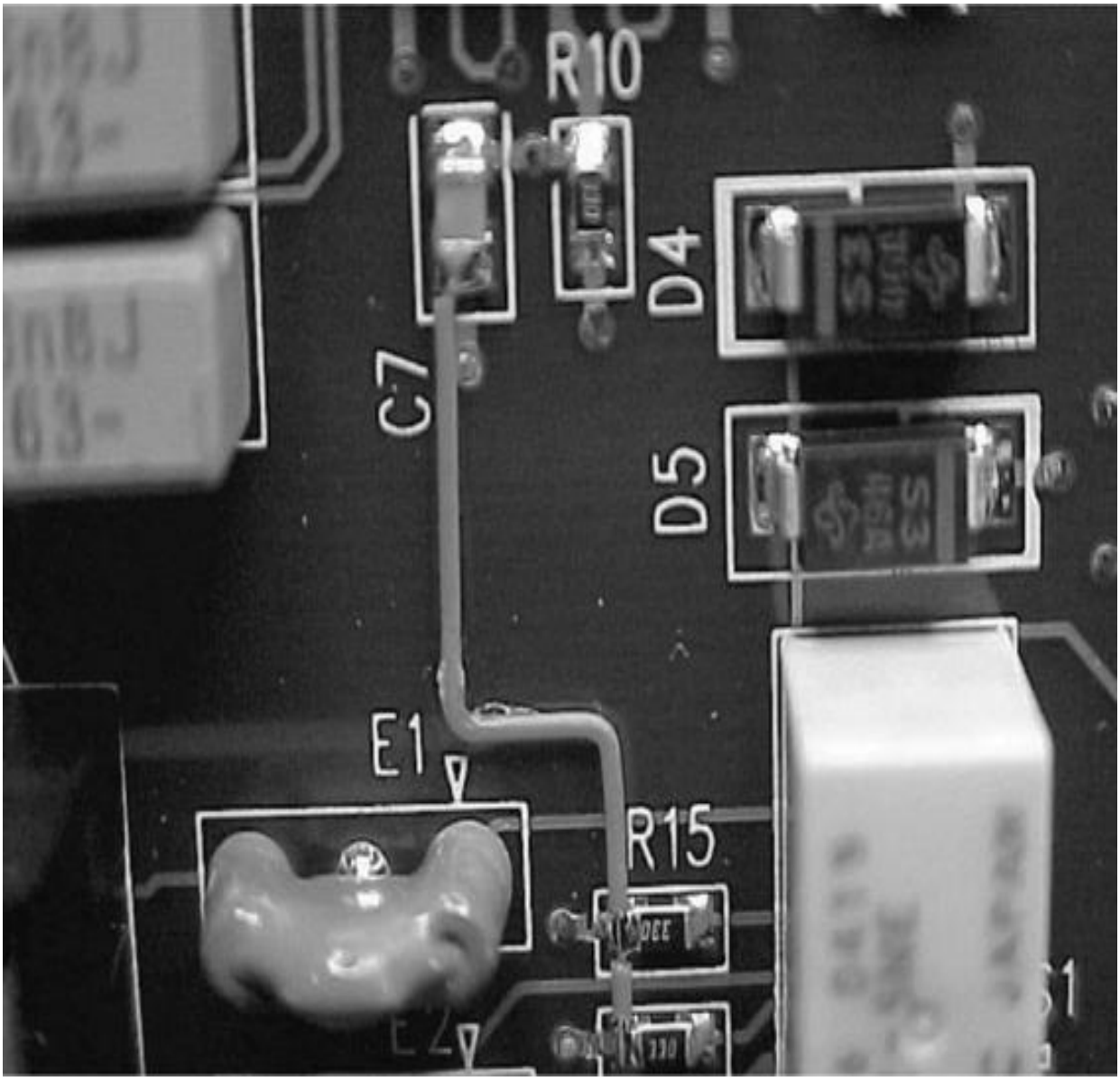


FIGURE 54.39 Example of X-Y routing of jumper wires. *(IPC)*

When jumper wires are used on the primary side (component side) of the PCBA, no wire is to pass over or under any components for Class 2 or 3. The wire may pass over lands, provided the wire can be moved away from the land for component replacement. To prevent damage to the

wire from excessive heat, care must be taken to avoid running wires near heatsinks or components that generate high temperatures.

When jumper wires are used on the secondary side of the PCBA, the jumper wire should not pass through component footprints unless the layout of the assembly prohibits routing in other areas. If this condition occurs, it should be considered a process indicator. There is an exception to this is rule for edge connectors on the PCBA. Jumper wires should not pass over test points or vias used as a test point.

Jumper wires should be staked to the base material with an approved adhesive or tape dots or strips intended for this purpose. If adhesives are used, they must be fully cured as part of the completed PCBA. The wire should be spot-bonded along its route and must not be applied to lands, pads, or components. The interval of staking must be defined in the applicable engineering documentation, but the wire must be staked at all changes in direction of the wire. No jumper wires may be staked to components that are socketed or any moving part. Jumper wires must be staked or taut enough to prevent the wire from rising above the height of adjacent components. No more than two jumper wires may be stacked on a given route.

When a jumper wire is attached to leads on the secondary side of the PCBA or to axial components on the primary side of the PCBA, it must form a full 180 to 360° loop around the component lead. When a jumper wire is soldered to other component package styles, the wire should be lap-soldered to the component lead.

Jumper wires may be installed into a PTH with another component lead for Class 1 and 2 equipment; however, this is unacceptable for Class 3 equipment. Jumper wires may also be installed into via holes (see Fig. 54.40).

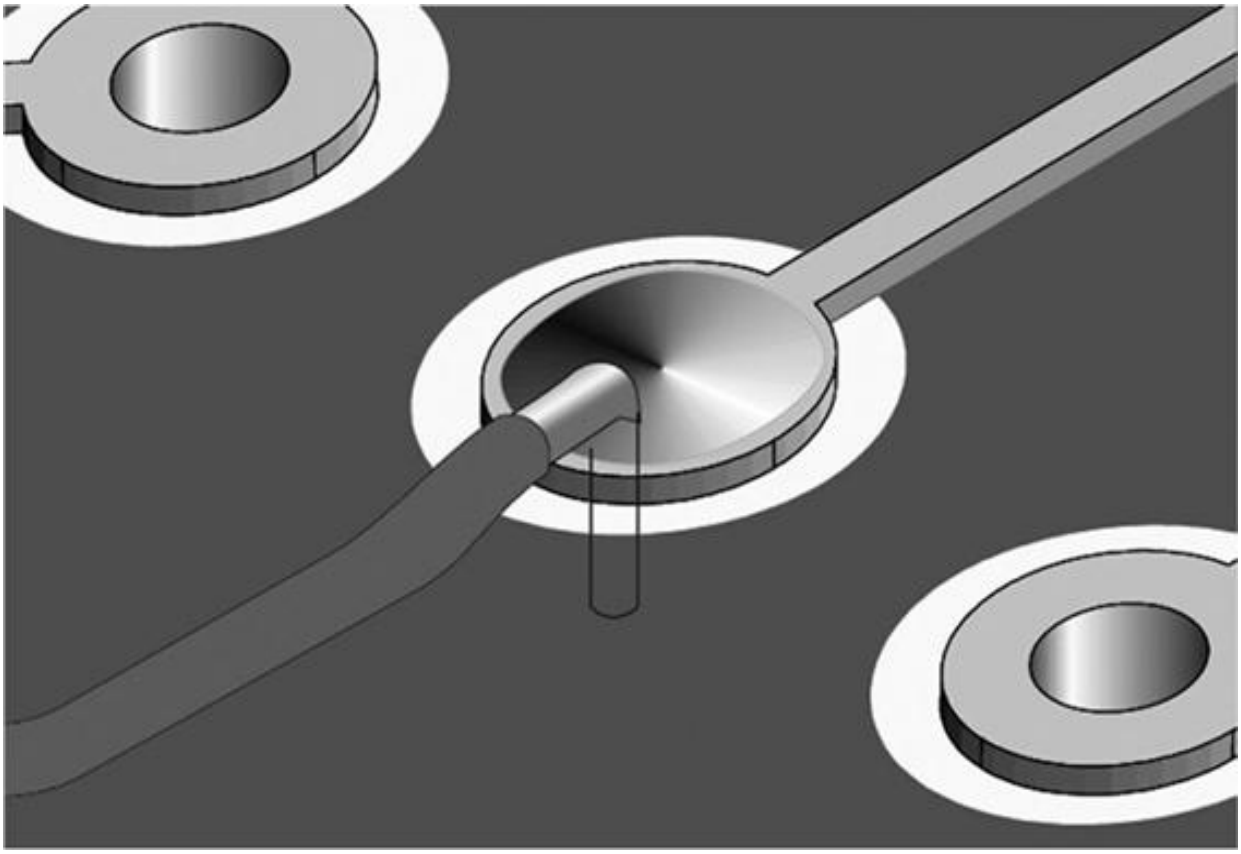


FIGURE 54.40a Example of jumper wire connected to plated through-holes (IPC).

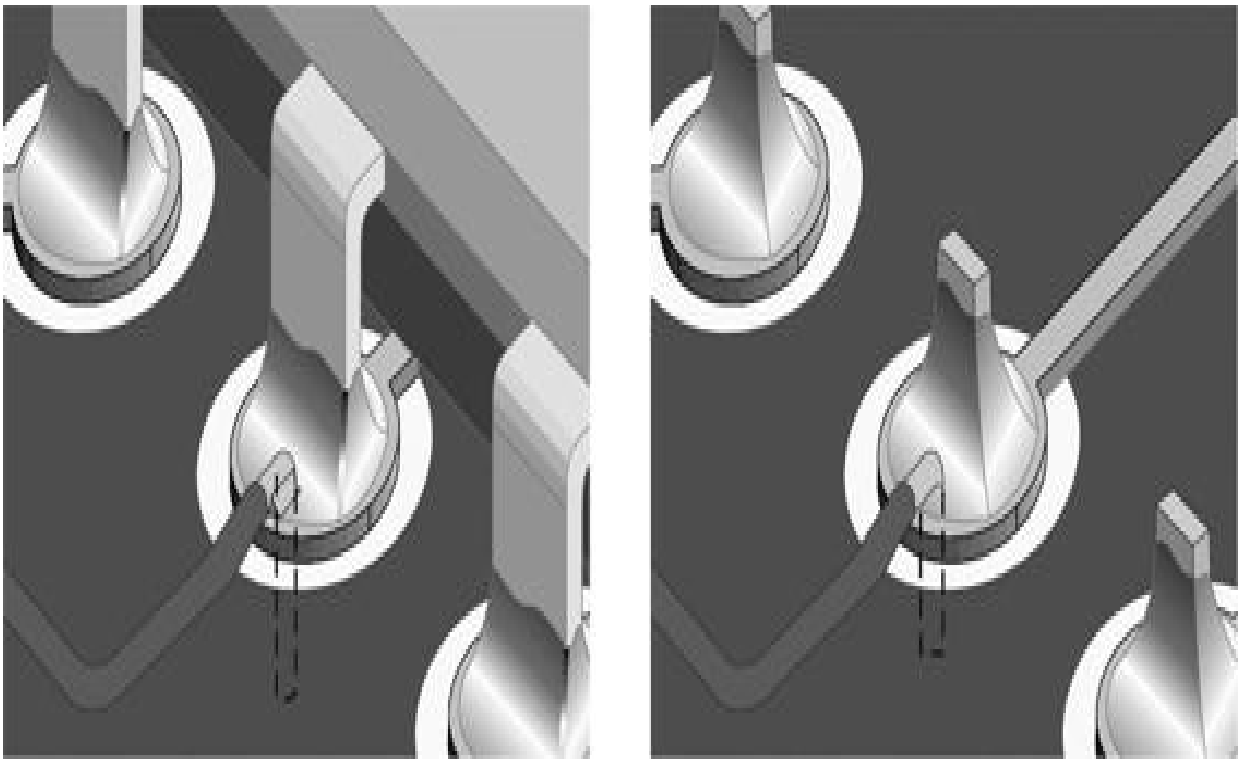


FIGURE 54.40b Example of wire connected to a via hole with a lead installed.

54.11 REFERENCES

1. ANSI/J-STD-001, “Requirements for Soldered Electrical and Electronic Assemblies.”
2. MIL-STD-2000, “Standard Requirements for Soldered Electrical and Electronic Assemblies.”
3. ANSI/J-STD-002, “Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires.”
4. ANSI/J-STD-003, “Solderability Tests for Printed Boards.”
5. IPC-A-610, “Acceptability of Electronic Assemblies.”

CHAPTER 55
ASSSEMBLY INSPECTION

Stacy Kalisz Johnson
Agilent Technologies, Gilbert, Arizona

Stig Oresjo
Agilent Technologies, Loveland, Colorado

55.1 INTRODUCTION

This chapter covers why manufacturers inspect printed circuit assemblies, how they have implemented and enhanced visual inspection, what automated inspection systems they are using, and how they have implemented these automated systems. The scope of this chapter includes only inspection of printed circuit assemblies during the assembly process, as typically shown in Fig. 55.1. Thus, it includes inspection of solder paste after the paste printing process step, components after the component placement process step, and solder joints after the solder reflow process step. Not included, however, is incoming inspection of components and the bare printed circuit board (PCB). The focus of this chapter is on production use of inspection, not

the collection of measurements during process development in a research and development (R&D) environment.

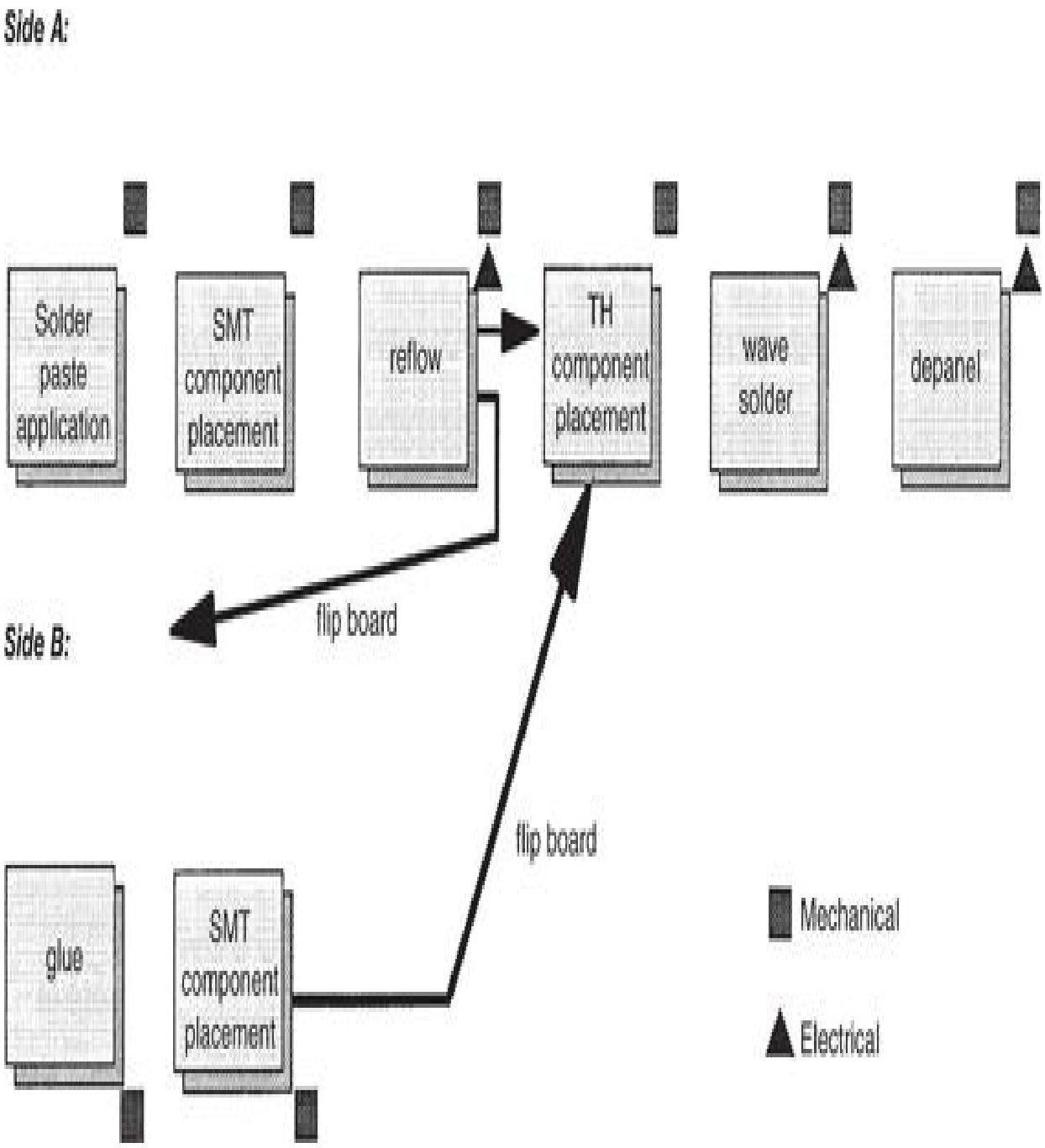


FIGURE 55.1 Generic manufacturing process for surface-mount technology printed circuit assemblies, including the possible locations within the process for inspection or testing of mechanical or structural attributes and electrical characteristics of an assembly.

55.1.1 Visual Inspection

Manufacturers of printed circuit assemblies have always visually inspected their boards at various points in the assembly process. There are a variety of reasons for visual inspection of assemblies, including eliminating obvious process defects quickly and meeting military specifications. With the advent and growth of surface-mount technology (SMT), visual inspection of printed circuit assemblies has also grown in importance and prevalence. SMT solder joints must carry a much bigger burden for mechanical or structural reliability than do plated-through-hole (PTH) solder joints. The pin-in-through-hole solder joint carries much of the mechanical burden, helping to keep the component attached to the printed circuit board. However, with SMT solder joints, it is often only the solder that keeps the component attached to the board. In some cases, only visual inspection could judge the mechanical reliability of an SMT solder joint.

As SMT geometries have continued to shrink and solder joints have become denser on printed circuit boards, visual inspection has become more difficult and thus its results have become less consistent and reliable. In addition, components such as pin grid arrays (PGAs) or ball grid arrays (BGAs) completely hide their solder joints from view, which makes visual inspection not possible at all for those joints. As Fig. 55.2 indicates, achieving a high assembly process yield is more important as the number of solder joints per assembly increases.

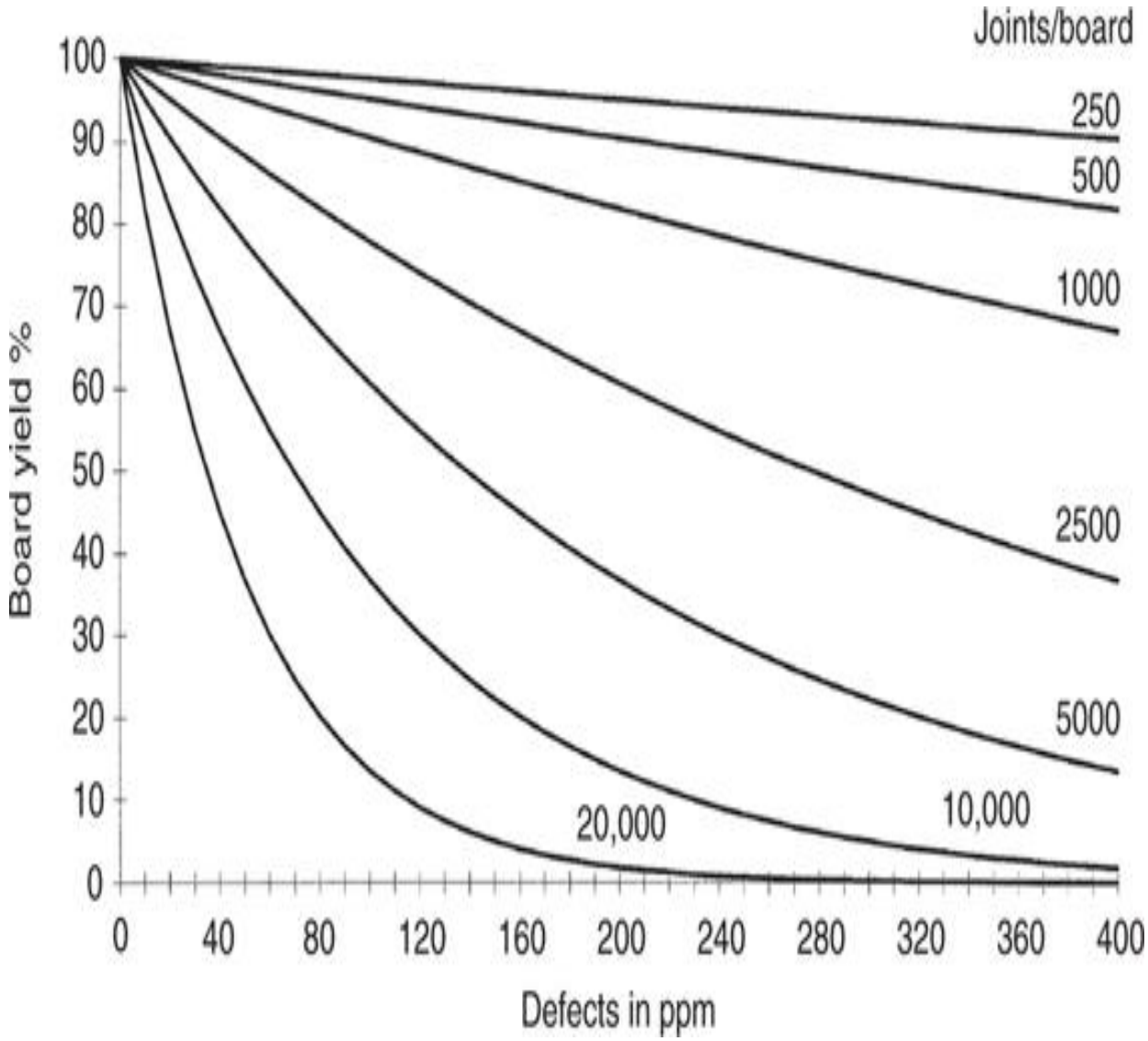


FIGURE 55.2 Printed circuit board yield decreases dramatically with increases in the number of solder joints per assembly if the defect rate per solder joint remains constant. For instance, at a 40 defects per million opportunities (DPMO) defect rate, the yield drops from 96 percent at 1,000 joints per assembly to 45 percent at 20,000 joints.

55.1.2 Automated Inspection

Inspection is an important source of process information without which high yields are difficult to obtain. Consequently, manufacturers have employed the following

range of techniques either simply to enhance visual inspection or automate inspection fully:

- Microscopes, mono- and stereoscopic, with magnification from 4× to 10×
- Real-time video images created using simple light, x-rays, thermal imaging, or acoustics
- Fully automated inspection systems using light, laser, or x-ray imaging

The automation of inspection has evolved into systems that resemble the automated test equipment used to make electrical measurements and find electrical defects (faults). These automated inspection systems acquire real-time images, process the images to find and measure features within the image, and make accept/reject decisions based on this image processing. Additionally, they provide data that can be used for long-term statistical process analysis. Thus these automated systems remove the human—and human judgment—from the inspection process altogether.

55.2 DEFINITION OF DEFECTS, FAULTS, PROCESS INDICATORS, AND POTENTIAL DEFECTS

Faults, defects, process indicators, and *potential defects* are terms that are important when discussing test and inspection, so this section will define and explain them:

- *A* fault *is a manifestation of a defect* An example is a digital device output pin that does not toggle correctly. For simplicity, think about a two-input OR-gate whose output is stuck high. This is a fault and is a manifestation of a defect. The causing defect can be any one of several,

including a defective component, an incorrectly placed component, an open input pin, or an open output pin. The fault class is a subset of the defect class. Electrical tests such as in-circuit test (ICT), boundary-scan, built-in-self-test (BIST), functional test (FT), and system test mainly detect faults.

- *A* defect *is, at the end of the manufacturing process, an unacceptable deviation from a norm* There may be defects that do not show up as faults. Examples are insufficient solder, a misaligned component, a missing bypass capacitor, and an open power pin. Inspection systems such as automated optical inspection (AOI) and automated x-ray inspection (AXI) detect many of the defects and also some of the same faults as electrical test. The definition includes the phrase “at the end of the manufacturing process,” which is important when compared with “potential defect.”

All defects, which also include the faults, need to be corrected before the product is shipped, if high quality standards are to be followed.

- *A* process indicator *is, at the end of the manufacturing process, an acceptable deviation from a norm* Good examples are insufficient solder or misaligned components. The insufficient solder may not be so lacking that it requires a repair action. However, if many of these conditions exist, a process improvement action may be required.
- *A* potential defect *is, in the manufacturing process, a deviation from a norm, that may or may not be a defect at the end of the manufacturing process* This category needs to be understood. An example is a pre-reflow misaligned chip component. This component may or may not self-align in the reflow oven. Another example is an insufficient

paste volume that may not end up as a defective solder joint at the end of the manufacturing process.

Test and inspection engineers at the end of the line are mainly interested in finding faults and defects. Process engineers responsible for improving the manufacturing process are mainly interested in potential defects, process indicators, and systematic defects. Systematic defects are typically defects that occur on a larger number of boards and are due to some systematic problem, such as a bent nozzle on a pick-and-place machine, soldering issues with one type of component, or a design for manufacturing (DFM) issue.

It is important to realize that electrical test at the end of the manufacturing line only finds faults. It is therefore important to complement the test strategy with steps that find all defects. Finding all defects is critical if shipping high-quality, reliable products is a priority. Identifying potential defects and process indicators can also help in adjusting the manufacturing process to result in lower defect levels, higher yields, and lower cost. Inspection is therefore a very important complement to electrical test.

55.3 REASONS FOR INSPECTION

Manufacturers inspect printed circuit assemblies during production for a variety of reasons. Most of these reasons fall into the following categories:

- Improvement of process defect coverage
- Improvement in ability to meet customer specifications
- Detection of process defects as quickly as possible after they occur
- Ability to decrease process defect rates through statistical process control (SPC)

55.3.1 Process Defect Coverage

The goal of higher defect coverage is to prevent any defective printed circuit assemblies from reaching assembly of the board and making it into the final product, whether final assembly is at the same site or at a separate customer site. Figure 55.3 shows a typical spectrum of SMT process defects. Some of these defects, such as misaligned solder joints and solder balls, can be discovered only by inspection, not by electrical, functional, in-circuit, or boundary-scan test. For instance, marginal solder joints are those that pass electrical tests just after assembly completion, but eventually fail because of inferior mechanical strength. Insufficient solder and components partially misaligned with printed circuit pads are the two most common causes of low mechanical strength.

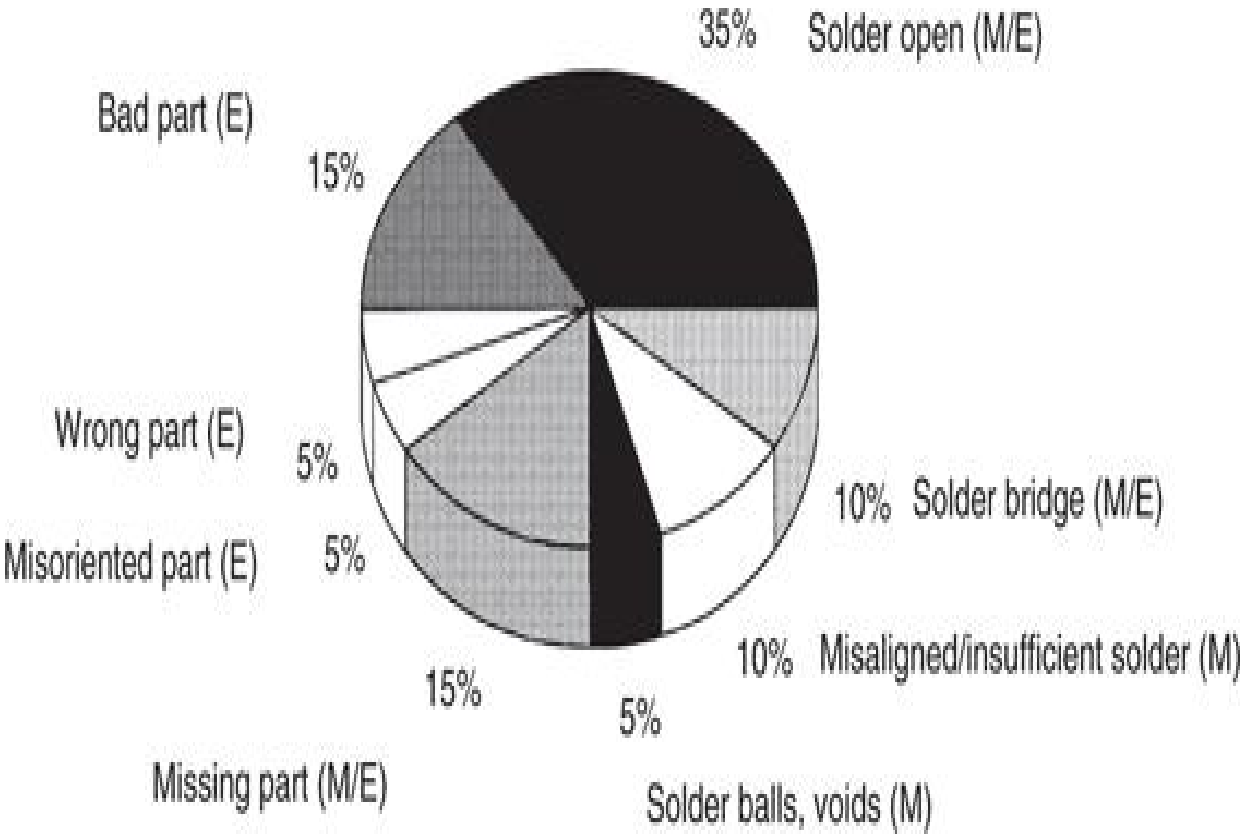


FIGURE 55.3 Typical process defect spectrum for surface-mount assemblies. Process defects marked "*E*" can be detected by electrical tests, those marked "*M*" can be detected by mechanical or structural inspection or testing, and those marked by "*E*" and "*M*" can be detected by either method.

Voids in solder joints, solder balls away from solder joints, and "cold" or dull solder are other examples of defects that can be found only by some kind of inspection.

55.3.2 Customer Specifications

Many printed circuit assembly workmanship specifications—including MIL-STD-2000A, IPC/EIA J-STD-001C, and, more recently, IPC-A-610D—require inspection of solder joints to ensure conformance to these specifications. For instance, MIL-STD-2000A prescribes, for all defense and aerospace government contractors, the attributes of solder joints to be inspected and describes the conditions that result in nonconformance. Most commercial customers of contract manufacturers also have very specific solder joint specifications that require some type of inspection of printed circuit assemblies. Although process control is theoretically preferred over 100 percent inspection, practically speaking, a majority of printed circuit production lines include some kind of inspection to ensure conformance to specifications. As the inspection speeds of the automated inspection systems have improved in recent years, this has become even more prevalent. It is likely that this trend will continue in light of the continued usage of finer pitch devices and the dawn of material challenges, such as lead-free implementation.

55.3.3 Quick Defect Detection and Correction

Quick detection of process shifts or defects can lower rework costs.

55.3.3.1 Preventing Defects. If a particular process step has drifted out of its control limits or specification limits, discovering this fact as soon as possible will prevent more defects from occurring. If the problem is found quickly enough and corrected immediately, perhaps no actual defects will occur.

55.3.3.2 Lowering Rework Costs. Defects found earlier in the process are often easier to repair. For instance, if a defect in solder paste deposition is found before a component has been placed in the paste, it is fairly inexpensive to wipe the solder paste off and start over. If this same defect is found after the solder is reflowed, the solder joint itself will have to be touched up, a more difficult and expensive rework step. The same is true for repairing component placement defects before the solder is reflowed, particularly for missing or misaligned components. Additionally, when organic solderability preservative (OSP) boards are being utilized for lead-free soldering, for example, they cannot be reworked as easily. Using process control and defect prevention can prevent a large number of non-reworkable boards in this case.

55.3.3.3 Making Defect Diagnosis Easier. Defects found earlier in the assembly process are often more easily diagnosed, shortening the overall repair time. An example is the inspection of solder joints. Inspection of solder joints detects defects specific to the solder joints and quickly determines each defect’s exact location and characteristic. Waiting until a later electrical test stage could make diagnosis more difficult because at that point there could be several causes of the defect, such as a defective component

and defects in other connections, in addition to the actual defective solder joint.

55.3.4 Statistical Process Control

SPC requires reliable data that can be analyzed either in real time or historically. Visual inspection collects defect data, such as the number of solder joint defects per assembly right after the solder reflow process (either reflow or wave soldering). Some manual and automated inspection techniques also take quantitative measurements of key assembly parameters, such as solder paste volume or solder joint fillet height. To the extent that these data are repeatable, manufacturers use defect data or measurements to characterize the amount of process variation from assembly to assembly or from solder joint to solder joint. When the amount of variation starts to drift outside its normal range or outside its control limits, manufacturers can assess the assembly process and monitor or choose to take action until the process is adjusted to eliminate this drift. Historical analysis of the defect or measurement data also helps discover the cause of process variation. Eliminating the sources of process variation reduces the process defect rate, thus creating savings in rework costs and increasing product reliability. As shown in Fig. 55.4, various charts to display available data from the automated inspection can be made available for corrective action and process control.

View History - Line21

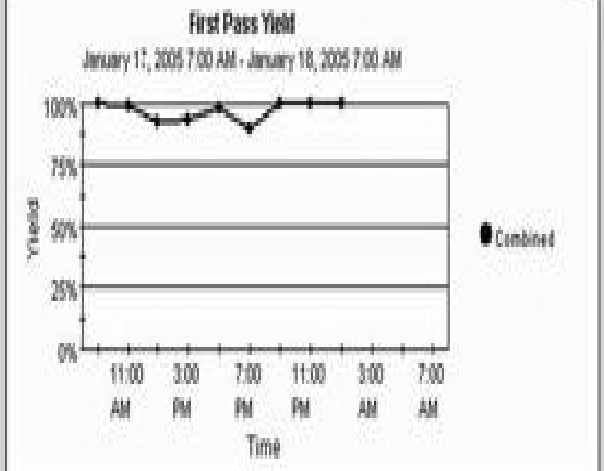
Test Stations: IE41500338

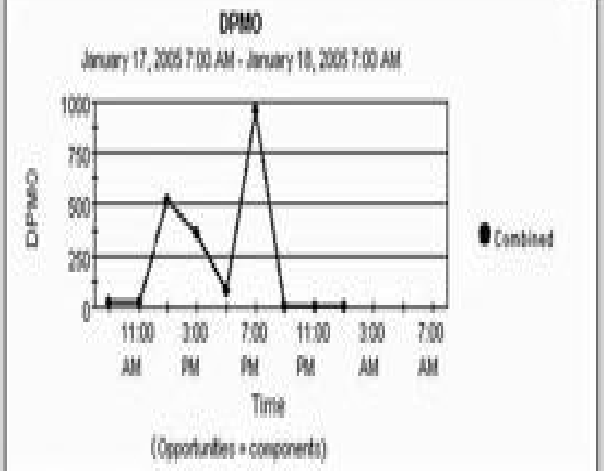
Board Types:

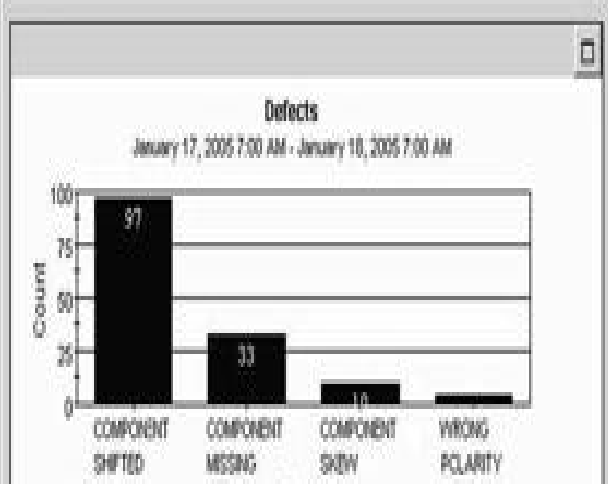
Time Frame: January 17, 2005 7:00 AM - January 18, 2005 7:00 AM

Edit Time Frame

Post-Repair Quality | False Call







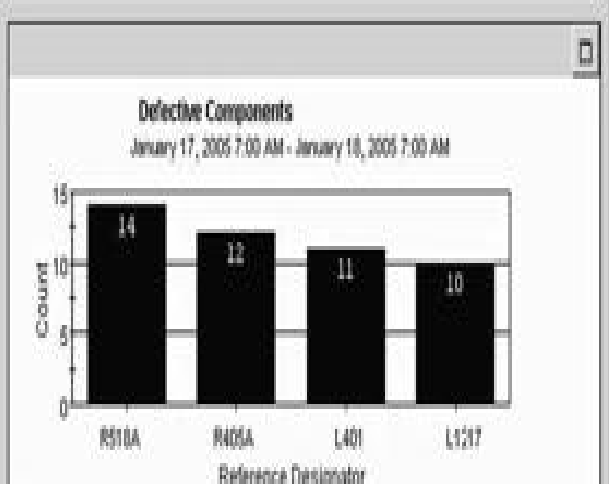


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FIGURE 55.4 Sample charts to display data from automated inspection.

55.4 LEAD-FREE IMPACT ON INSPECTION

Other chapters of this book have covered the lead-free process, but this section covers the lead-free process from an inspection point of view. In general, the lead-free process is a less forgiving one because the wetting forces for lead-free alloys are not as strong as for tin-lead, which means that defect levels are likely to increase and the need for inspection for process control and defect containment will increase. The figures illustrate wetting issues of the lead-free process. Figures 55.5 and 55.6 show x-ray close-ups of two gull-wing joints on the same type of quad flat pack (QFP) device.

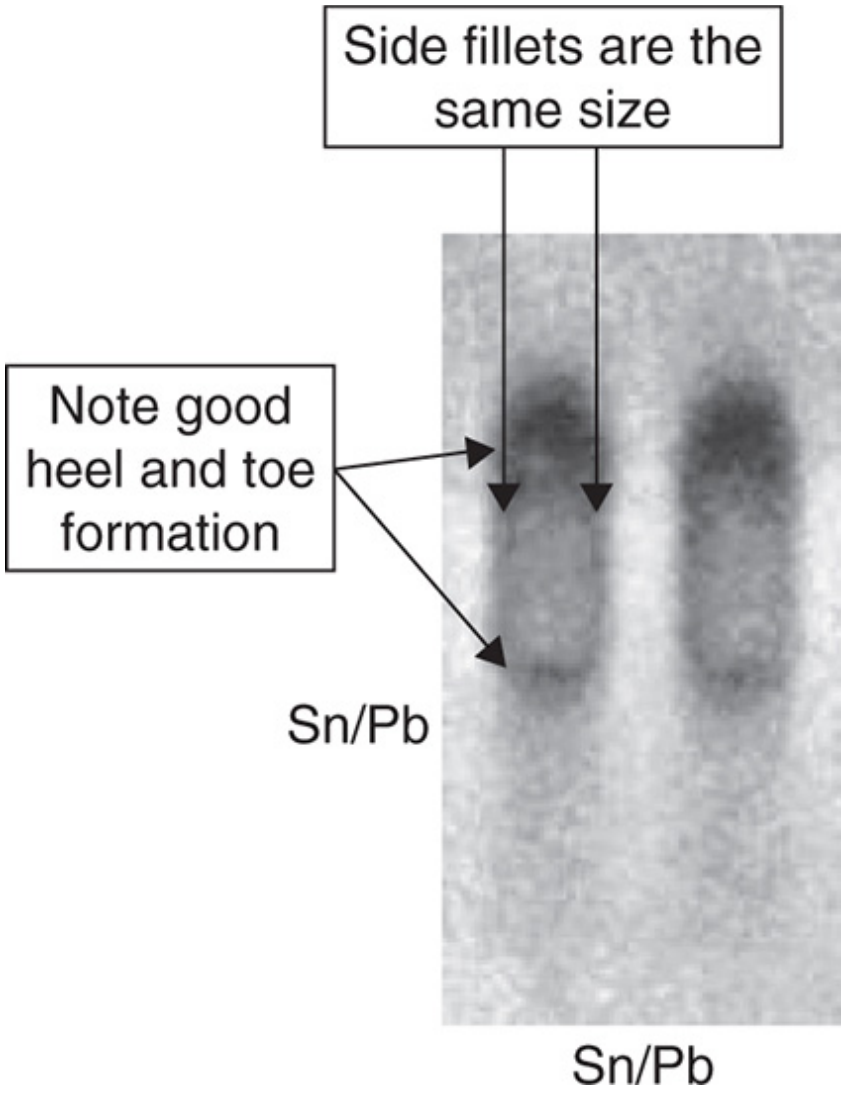


FIGURE 55.5 An x-ray image of a tin-lead example.

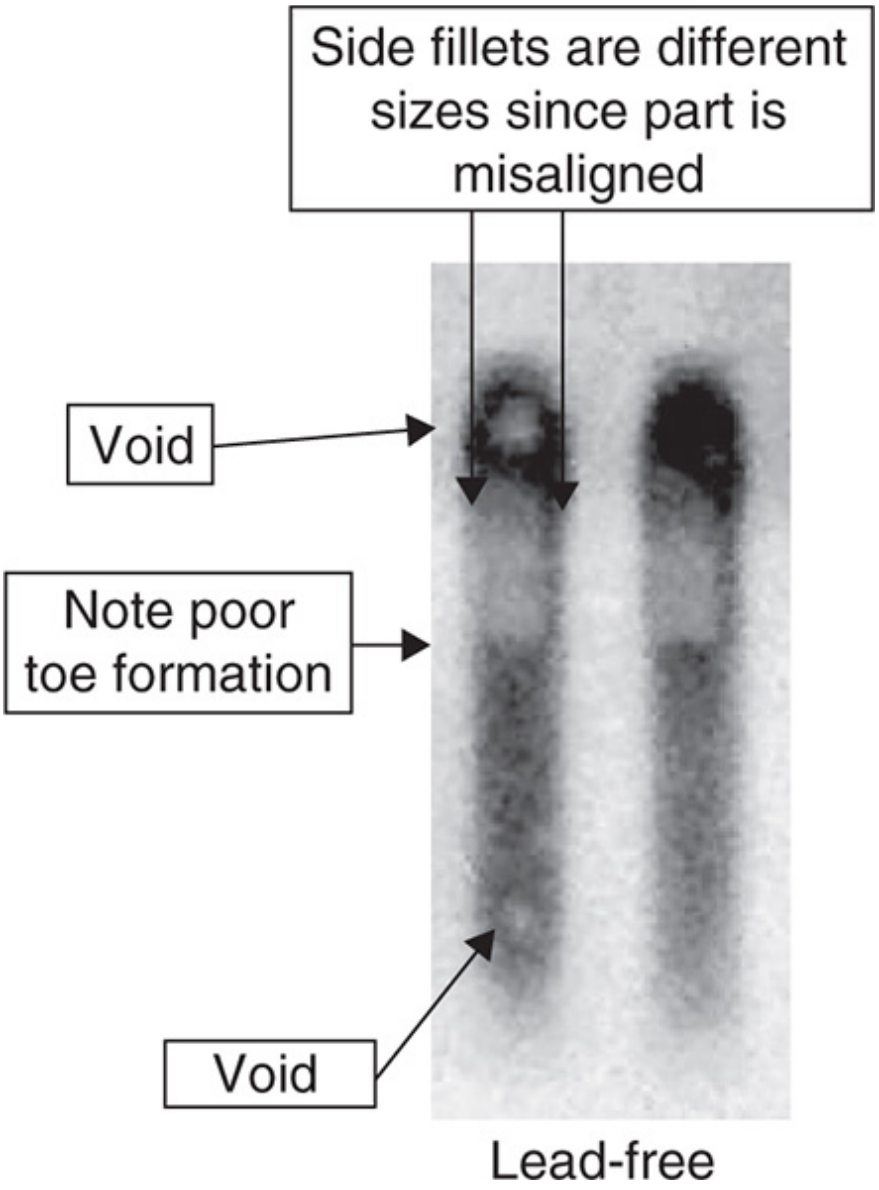


FIGURE 55.6 An x-ray image of a lead-free example.

A key issue for manufacturers is the lead-free alloy melting point of 217°C, higher than the 183°C for lead alloys. The higher melting point will have significant impact on manufacturing processes and potentially on component reliability.

During the transition to a lead-free process, it is important to understand all of the materials in use, as mixing lead-free and traditional tin-lead components will create many issues during the transition to a lead-free process. Ideally, all lead-

free components and materials will be utilized, but this is not always possible.

Figure 55.5 is an x-ray image of a tin-lead example. A good heel formation and toe formation can be seen. The side fillets are approximately the same, indicating that the component pins are centered on the pad. Note also that very little solder appears on the pad below the toe in the photo; all solder is around the component pins.

Figure 55.6 is an x-ray image of a lead-free example and reveals a couple of wetting issues. Solder is over the full pad. The pad sizes on both boards (Figs. 55.5 and 55.6) are approximately the same. Also, note that the side fillet to the right is stronger than to the left, indicating that the component is misaligned on the pad. The toe fillet is insignificant. The heel fillet has formed correctly; a void can be seen in one of them. A void is also visible on the same pin further down on the pad.

During the transition to a lead-free process, expect to see many of these types of defects. Defect levels are expected to increase. The following types of defects are typically noticeable during lead-free transitions: opens, bridges, misalignment, tombstones, and voids. Because of the higher reflow temperatures, component defects are also expected to increase. Large variations in defect levels should be expected. For some board types, small increases or no increase will be seen, whereas for others a significant (more than 10 times) increase in DPMO values will be seen. These defect levels will vary from one manufacturing site to another.

Inspection and especially automated inspection will be a significant help in addressing the tighter process window acceptable for a lead-free process. For process control, pre-reflow inspection will provide the biggest benefit. The obvious benefit is that solder paste inspection (SPI) and pre-reflow automated optical inspection (AOI) systems provide early defect and potential defect detection and prevention

specifically by identifying the defects that are expected to increase with the use of lead-free solder (opens, bridges, and so on, as previously mentioned in this chapter). An additional benefit—and perhaps the most valuable one—is the insight that the process engineer can gain by evaluating the results from SPI and AOI systems as lead-free materials are adopted. By integrating SPI and AOI systems in the manufacturing process as they move to lead-free materials, and then using the data for process optimization, the manufacturer can eliminate most of the process difficulties that a lead-free process creates. This implementation will in turn allow users to bring lead-free lines up to speed more quickly and efficiently, saving on labor, materials waste, and so on.

After reflow, the main objective is to identify defects so that repair action can take place. For this manual visual inspection, AOI post-reflow, or automated x-ray inspection, can be used. Even with good process control, defect levels are likely to increase, especially for higher-complexity boards. If defect levels are higher, then a good inspection strategy becomes more valuable.

55.5 MINIATURIZATION AND HIGHER COMPLEXITY

Printed circuit board real estate continues to be coveted. Boards are getting smaller and smaller as more and more capabilities are built on them. To keep up with this trend, complex packages and devices and miniature devices are cropping up. Many would argue that a 0402 chip component is small, but “small” becomes subjective when you consider 0201s and 01005s. The 01005 component’s sizes typically range from 0.10 mm (0.004 in.) × 0.304 mm (0.012 in.) to 0.20 mm (0.008 in.) × 0.40 mm (0.016 in.), depending on the supplier. Note that the 0201 typical is 0.60 mm (0.0236

in.) × 0.30 mm (0.0118 in.), thus it's quite a jump. With devices on this size order, the design considerations are large and the propensity for defects is higher. Inspection must catch the defects, but at these sizes, approaching the eye of a needle, it is not practical to conduct inspections visually, and thus such automated test and inspection become paramount. Automated test and inspection continues to spur the development of camera and algorithm technology to keep up with the throughput, coverage, and size requirements demanded by the industry. Miniaturization in itself is quite a driver for these technologies. Add this to the material changes that are going on with materials changes such as lead-free materials, and the need for automated test and inspection only increases. AOI systems including three-dimensional (3-D) and two-dimensional (2-D) solder paste and pre- and post-reflow component inspection are typically lead-free-ready, as are x-ray test systems, with a few minor programming updates.

The advancement of the miniaturization movement also drives technologies such as multichip modules (MCM), system-in-a-package (SIP), and so on. These devices or boards, depending on how one refers to them, have many interconnects among themselves in addition to the requirements that they pose when the entire MCM, SIP, etc., is adhered to a printed circuit board. The number of hidden joints increases, the types of hidden joints increase, and the complexity of the attachment to the SMT board in general increases. All of these are contributors to the ongoing need for increase defect containment and defect coverage that only automated inspection and testing bring.

55.6 VISUAL INSPECTION

Visual inspection is the visual comparison by a human of some attribute of the printed circuit assembly with specified standards that describe the acceptable range for that attribute. The inspector normally picks up the printed circuit assembly or places it under a microscope and carefully observes particular attributes, such as the condition or bend radius of component leads or the wetting of solder joints to a lead. Visual inspection always involves human judgment in comparing the attribute to its conditions of conformance to standards.

55.6.1 General Inspection Issues

As Fig. 55.1 indicates, visual inspection can occur after each of the several printed circuit assembly process steps. Visual inspection often has different purposes, depending on where in the assembly process it occurs. These purposes fall into the following major categories:

- Quick detection of an assembly process step that is not operating within its normal range
- Detection of process defects as specified by the customer or industry or internal standards

55.6.2 Solder Joint Inspection Issues

Visual inspection after the reflow and wave-soldering process steps can also be just a quick scan for obvious defects to detect a process condition outside of control limits. In this case, the operator visually inspects for solder bridges, large solder balls or solder splashes, lifted leads, and a number of other improper conditions. Often, however, visual inspection after the soldering process steps is aimed at finding solder joints that do not meet specifications.

Visual inspection of solder joints against specification can cover 100 percent of the visual solder joints on an assembly. Inspecting samples of solder joints in conjunction with a documented process control system is also done. Inspecting for this purpose can be a lengthy process, taking as long as a half-hour for assemblies with 4,000 solder joints being measured against military specifications. As a rule of thumb, this kind of visual inspection has a throughput of about 5 joints per sec. compared to automated inspection techniques, which have capabilities of over 100 joints per sec. Thus, inspection of solder joints against specifications normally requires visual inspectors dedicated to this function with no other responsibilities. Visual inspection may still provide a low-cost alternative to automated inspection in some low-cost regions, which is one major factor contributing to its continued usage.

The visual inspector must be very familiar with the specifications of the attributes for each solder joint type. Each solder joint can have as many as eight different criteria for defects such as insufficient solder, misalignment, etc. Each assembly typically has more than six different solder joint types such as BGAs and QFPs, corresponding to different component packages with individual requirements for each. As an example, Fig. 55.7 shows the specification attributes for one component type (rectangular passive chips). Table 55.1 gives the corresponding conformance criteria for each attribute for this component type. More importantly, the visual inspector must be highly trained to make an accurate judgment of conditions on the borderline between good and bad. For instance, accurately determining whether a fillet height is one-quarter of the way up a component side that is only 0.05 mm high to begin with takes a lot of practice. Visual inspectors typically do not use any tools to help make these judgments. Rulers or calipers are very difficult or impossible to use to measure solder joint dimensions or thicknesses. Using reticules in microscopes in

conjunction with coordinate-measuring machines is possible, but is usually much too time consuming to be done on a regular basis.

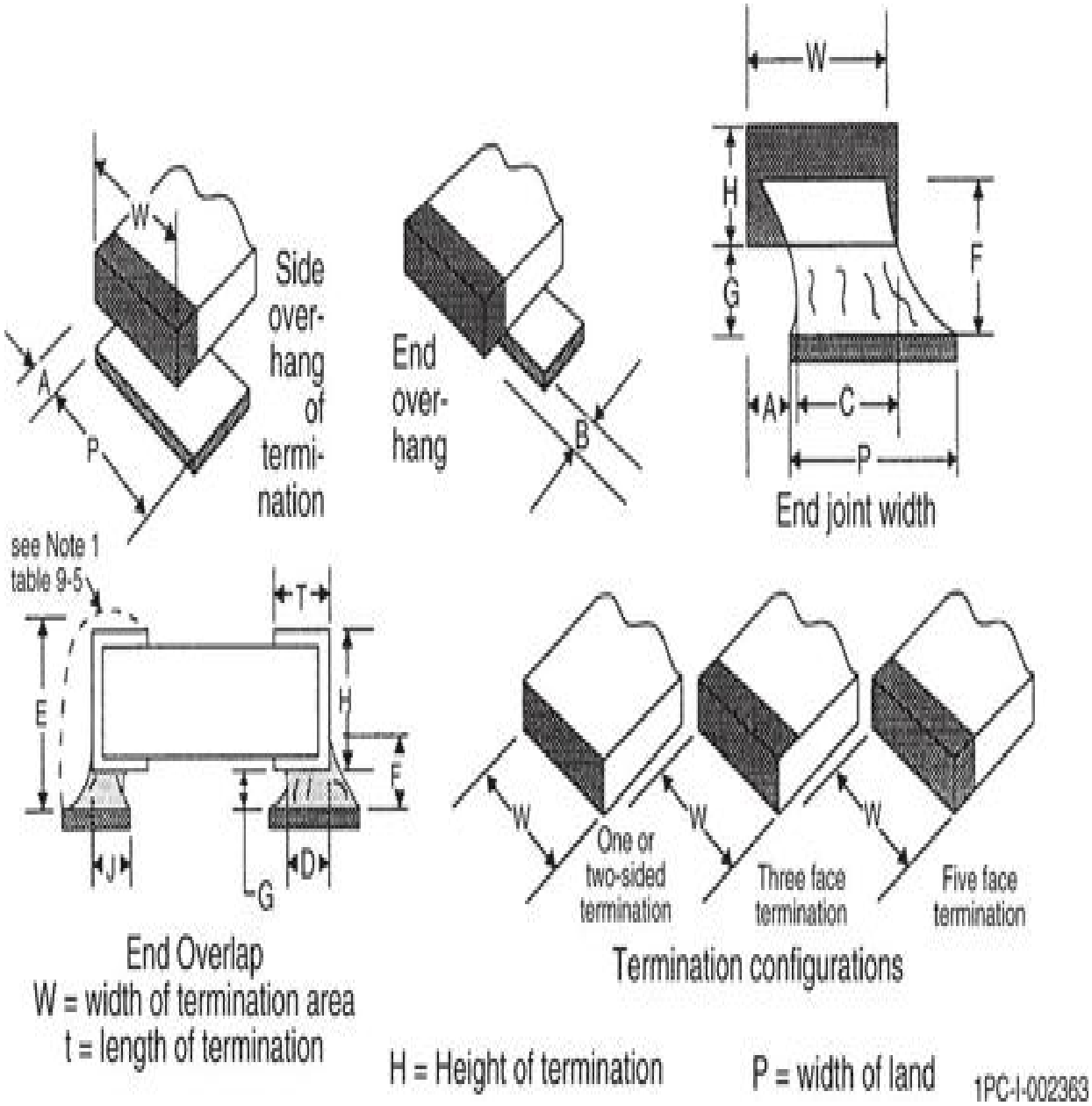


FIGURE 55.7 Inspection attributes for solder joints of surface-mounted rectangular passive chips.

TABLE 55.1 Dimensional Criteria: Rectangular or Square End Components (Dimensions in Millimeters)

Feature	Dim.	Class 1	Class 2	Class 3
Maximum side overhang	A	50% (W) or 50% (P), whichever is less; Note 1	50% (W) or 50% (P), whichever is less; Note 1	25% (W) or 25% (P), whichever is less; Note 1
Maximum end overhang	B	Not permitted	Not permitted	Not permitted
Minimum end joint width	C	50% (W) or 50% (P), whichever is less	50% (W) or 50% (P), whichever is less	75% (W) or 75% (P), whichever is less
Minimum side joint length	D	Note 3	Note 3	Note 3
Maximum fillet height	E	Note 4	Note 4	Note 4
Minimum fillet height	F	Note 3	Note 3	(G) + 25% (H) or (G) + 0.5 mm (0.02 in), whichever is less
Solder fillet thickness	G	Note 3	Note 3	Note 3
Height of termination	H	Note 2	Note 2	Note 2
Minimum end overlap	J	Required	Required	Required
Width of land	P	Note 2	Note 2	Note 2
Width of termination	W	Note 2	Note 2	Note 2

Note 1. Shall not violate minimum electrical clearance.

Note 2. Unspecified parameter or variable in size as determined by design.

Note 3. Properly wetted fillet shall be evident.

Note 4. The maximum fillet may overhang the land or extend onto the top of the end cap metallization; however, the solder shall not extend further onto the component body.

Visual inspection often occurs at the end of the assembly process or even after all of the electrical tests on the assembly have been completed. It is not possible, however, for invisible or hidden joints. The visual inspector looks for

scratches, partial delaminations, solder splashes or solder balls away from solder joints, and any other condition that does not affect assembly performance but does make the assembly look as though it might not be a high-quality product.

55.6.3 Standards for Visual Inspection

Many standards cover printed circuit board assemblies. Most major electronics manufacturers have their own internally developed workmanship standards. Several industry and military standards also exist. However, the joint industry standard IPC-A-610D, “Acceptability of Electronic Assemblies,” is the standard most often referenced for criteria defining reliable solder connections. This standard was developed by the Institute for Interconnecting and Packaging Electronic Circuits (IPC) (www.ipc.org).

The standard is a collection of visual quality acceptability requirements for electronic assemblies. It covers criteria for both pin through-hole and surface-mount technology solder connections. It also reflects requirements for three different classes of end products:

- *Class 1, general electronic products* These include consumer products and some computers and computer peripherals.
- *Class 2, dedicated service electronic products* This class includes communications equipment, critical business machines, and instruments where high performance is required and for which uninterrupted service is desirable.
- *Class 3, high-performance electronic products* These products include commercial and military equipment for which continued performance or performance on demand is imperative.

55.6.4 Capabilities of Visual Inspection

Visual inspection serves a number of important purposes well, but it also has several important limitations.

55.6.4.1 Advantages. Visual inspection can be an accurate and cost-effective method of defect detection for nonsubjective defects, such as larger missing components, larger misoriented or reversed components, or solder bridges. When low volume or lack of technical resources prevents the use of automation or more sophisticated tools, visual inspection is one alternative that finds many of the more subjective defects, such as solder joints with insufficient solder, lifted leads, or poor wetting. Finally, visual inspection can quickly detect when a process step has drifted significantly out of its control limits.

55.6.4.2 Disadvantages. Visual inspection also has many limitations, including the following:

- Low coverage of solder joint defect detection repeatability, particularly for fine-pitch parts, which results in high false accepts or defect escapes and high false reject rates
- Low coverage of component defect detection repeatability for smaller components such as 0402, 0201, or 01005 passive components
- Inability to see hidden solder joints in component types such as some connectors, PGAs, BGAs, chip-scale packages (CSPs), SIPs, or multichip modules (MCM)
- Inability to collect quantitative measurements in addition to defect data

55.6.4.3 Repeatability Limitations. Several studies have documented the low repeatability rate of visual

inspection of solder joints. One such study was conducted by AT&T at its Federal Systems Division.[1] This study showed that even the same inspector inspecting the same assembly twice had a defect call repeatability rate of only about 50 percent. Two different inspectors inspecting the same assembly had a defect call repeatability rate of only about 28 percent. This study did not include any very-fine-pitch SMT solder joints or 0603 passive components, which are more difficult to inspect visually.

To alleviate this severe limitation somewhat, manufacturers have implemented the use of microscopes with a magnification level of 10×. Often, stereoscopic microscopes are used to provide visual inspectors a better three-dimensional view. Not as frequently, manufacturers have implemented light sources and cameras to capture real-time magnified video images of the assembly being inspected. The lighting and high-resolution video images can make it easier for visual inspectors to see the acceptance criteria for which they are searching. These enhancements do improve the repeatability rate of visual inspection. But the requirement for subjective human calls and the tedium of carefully inspecting thousands of connections per hour still results in repeatability rates much lower than desired. Low repeatability means many missed defects that escape to final assembly or to customers, impacting reliability and wasting and possibly damaging rework of good connections.

55.6.4.4 Hidden Solder Joints. Several component types used in printed circuit assemblies do not provide visual access to solder joints. These components include packages with bump arrays where the solder joints are distributed in a matrix under the entire component body, such as ball grid arrays and chip-scale packages. For these components, all of the joints except those on the edges of the array are completely hidden from view. Other packages, such as J-leaded components, where the connections are under the

component body at the component edges, and 0.5 mm-pitch gull-wing components, where the solder joint heel is only 0.08 mm high and behind the component leads, also make visual inspection more difficult. Some manufacturers have attempted to solve this problem by using a penetrating imaging technique, such as x-ray, acoustics, or thermography, to acquire a live, magnified video image that the visual inspector can look at to make a defect call. However, the images resulting from these techniques are either less consistent or less well defined than a visual image, still requiring the inspector to make a difficult judgment call. Therefore, a low repeatability rate persists.

55.6.4.5 High-Complexity Boards. Many printed circuit boards today are entirely too complex to allow accurate visual inspection. Components as small as 0402, 0201, or even 01005 passive components are simply too small for accurate visual detection of missing parts and particularly misalignment defects. Add to this the fact that many printed circuit boards have hundreds of these component types per board, and the opportunity for the visual inspector to make a mistake becomes enormous. Further obstacles to accurate inspection are “families” of boards, where the basic layout of each board type is the same, but specific board types vary by purposely not mounting specific components. In these cases, a missing component can be completely acceptable even in places where the board layout may provide for a component to be mounted.

55.6.4.6 No Quantitative Measurements. Accurate quantitative measurements of dimensions ranging from 0.05 to 0.5 mm are not possible with visual inspection. Quantitative measurements provide much more information about a process step, allowing much tighter process control and providing insight into the causes of process variation, without which process improvement is a hit-or-miss

proposition. Some manufacturers have implemented semiautomatic measurement tools to allow operators to take quantitative measurements. Examples include optical-focusing microscopes and semiautomatic laser triangulation equipment. These tools do collect useful quantitative measurements, but are typically limited to sampling. Sampling is required because the tools are very slow. Measurement of solder paste height, volume, and registration with pads is possible because of easy visual access to solder paste depositions as well as their simple rectangular shape.

Automated inspection techniques using automated inspection equipment significantly overcome the repeatability and measurement limitations of visual inspection. It is for this reason that many manufacturers are implementing automated inspection.

55.7 AUTOMATED INSPECTION

The automation of inspection has evolved into systems that resemble the automated test equipment used to make electrical measurements and find electrical defects (faults).

Automated inspection systems generate images of the item to be inspected (normally solder paste, components, or solder joints), digitally analyze the image to locate and measure key features, and, based on these measurements, automatically decide whether a defect exists or not.

Just like visual inspection, automated inspection systems do not require physical contact with the printed circuit assembly to generate the desired images. Unlike visual inspection, however, automated inspection removes human subjectivity from defect detection, thereby increasing repeatability rates typically by an order of magnitude. Many of the automated inspection systems also provide accurate,

repeatable, quantitative measurements that directly correspond to process parameters, thus providing the means for process control and improvement.[2]

55.7.1 Measurements by Automated Inspection Systems

Figure 55.8 shows examples of measurements made by automated inspection systems.

55.7.1.1 Solder Paste Measurements. Typical solder paste measurements, shown in Fig. 55.8(a), are volume, area of pad covered, height, and misalignment with the pad. These quantitative measurements provide information about the paste viscosity, stencil registration, cleanliness, snap-off, and squeegee speed and pressure that can lead to improvement in the paste printing process.

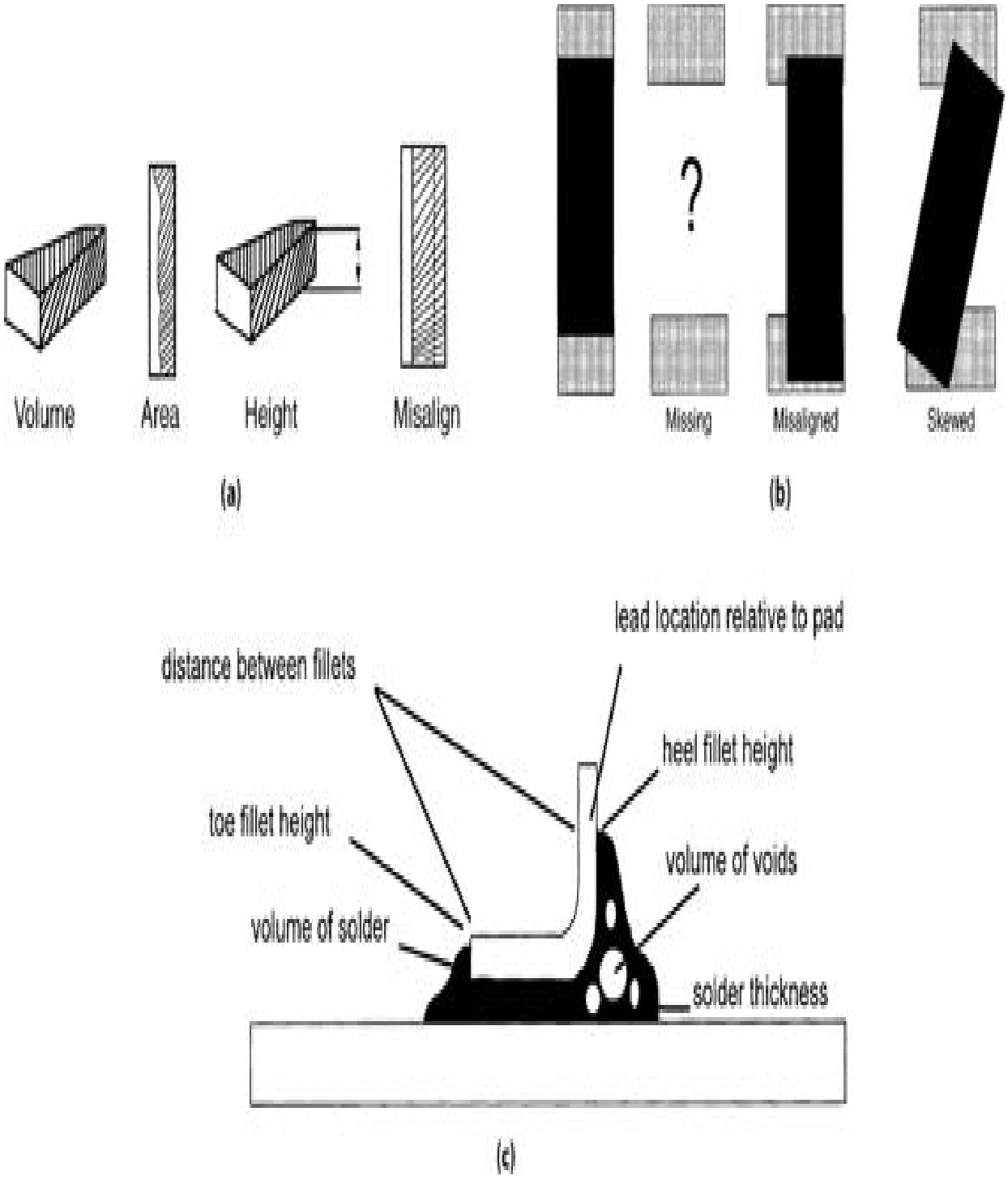


FIGURE 55.8 Measurements made by automated inspection systems: (a) Typical solder paste measurements made by automated inspection systems, including the volume of paste deposition, area of the pad covered by paste, height of the paste deposition, and offset of the paste from the pad; (b) typical component placement attributes inspected by automated inspection systems, including missing component, components misaligned along or across the pads, and skewed components; (c) typical solder joint measurements made by

automated inspection systems, including volume of solder, toe and heel fillet heights, distance between fillets, void volume, average solder thickness across the solder joint, and offset between the solder joint and pad.

55.7.1.2 Pre-Reflow Measurements. Typical pre-reflow component placement measurements, depicted in Fig. 55.8(b), include whether or not the component is missing, misaligned, or skewed. These measurements are usually attribute measurements, just separating good from bad. But quantitative dimensional measurement of the amount of misalignment, just after the placement process step, is also possible. Component placement measurements provide information about the rate of placement accuracy. Optical character recognition (OCR) and optical character verification (OCV) techniques allow for additional levels of verification, including correct part.

55.7.1.3 Post-Reflow Solder Joint Measurements. Solder joint measurements, such as fillet heights, average solder thickness across the pad, void volume, and pin-to-pad offsets, as shown in Fig. 55.8(c), provide information about the paste printing process, the component placement process, and the solder reflow process steps. Attribute measurements, such as solder bridges, opens, or insufficient solder, are most common. Quantitative measurements of solder joints are also possible and provide greater insight into process parameters. For instance, the variation of heel fillet heights and void volume across an assembly provides insight into the oven temperature profile and spatial distribution. The variation of average solder thickness provides insight into squeegee speed and pressure and stencil cleanliness. And the pin-to-pad offsets measure the component placement accuracy.

55.7.2 Types of Inspection Systems

Inspection systems normally are dedicated to one type of measurement capability: solder paste, pre-reflow, or post-reflow inspection. For example, systems for solder paste measurements do not normally also make component placement measurements. The cost of combining different measurement capabilities into one system would typically make that system prohibitively expensive. More importantly, to reduce manufacturing costs, manufacturers want to implement linear, sequential production lines where an assembly always flows in one direction and goes through each machine only once per assembly side. So automated inspection systems fall into three major categories:

- Those that make three-dimensional solder paste measurements
- Those that make quantitative pre-reflow two-dimensional solder paste and/or component placement measurements
- Those that make post-reflow solder joint measurements and attribute component measurements

For all three types, the automated inspection system compares the measurements taken against a specified conformance range to accept or reject automatically a solder paste brick, component placement, or solder joint as being within specification.

55.8 THREE-DIMENSIONAL AUTOMATED SOLDER PASTE INSPECTION

55.8.1 Operating Principles

Automated inspection systems designed for 3-D solder paste measurements use structured light sources and cameras or

digital light-emitting diode (LED) sensors to generate “three-dimensional images” of solder paste depositions. The structured light is normally some variation of a sheet of light or a laser line or spot. As Fig. 55.9 shows, the structured light sweeps across a solder paste brick, creating discontinuities and other features in the image that are calibrated to actual physical dimensions, such as height and area. In essence, the proportional nature of the deflection and height is turned into usable measurement results.

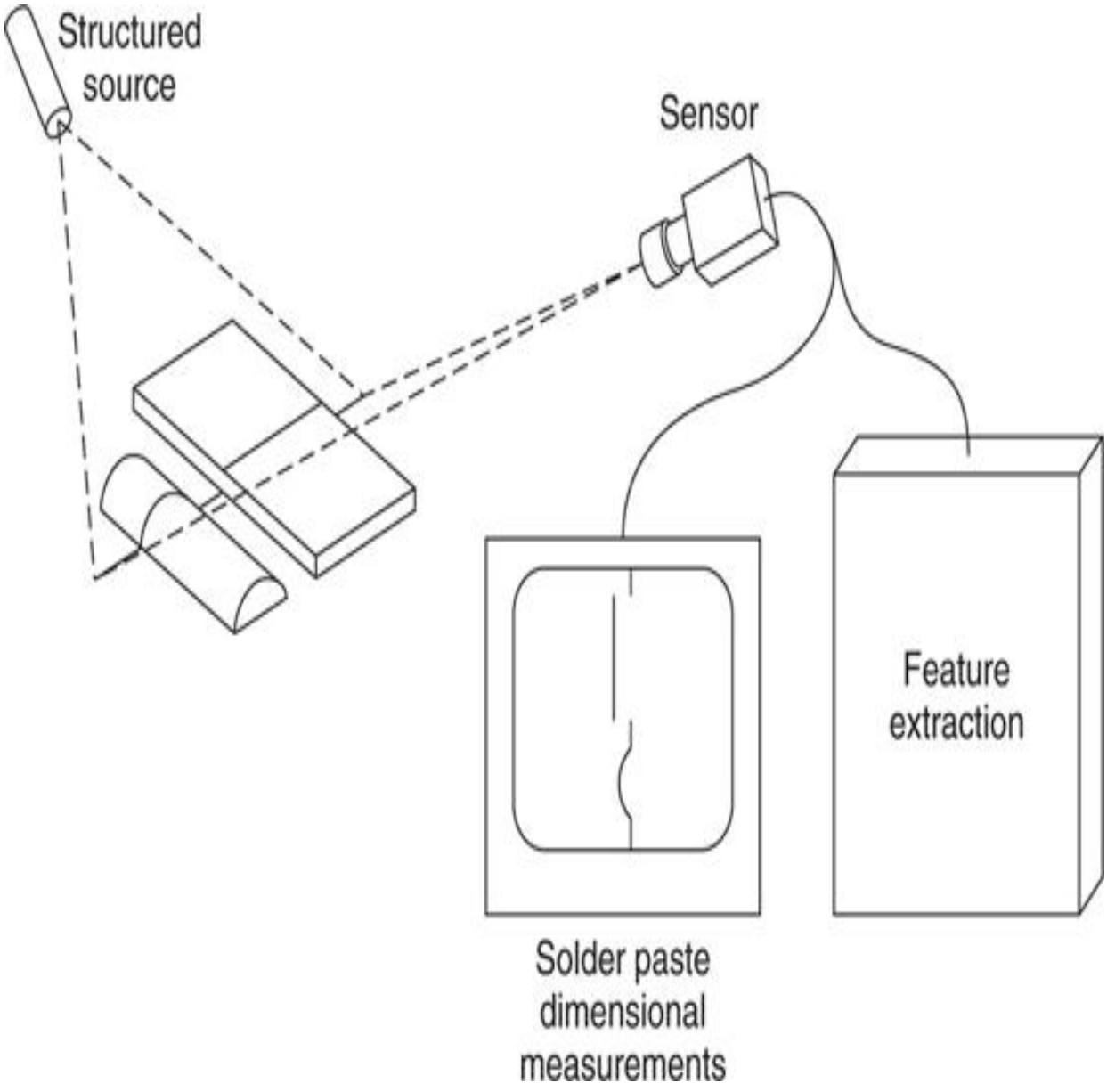


FIGURE 55.9 Schematic of automated inspection system for solder paste measurement. The camera or LED sensor obtains images with discontinuities in the laser line scan; the image-processing software finds these discontinuities, measures them, and calibrates them to real physical dimensions.

55.8.1.1 View Magnification. To achieve adequate accuracy, only a small portion of the assembly, called a *view*, is imaged at a single time. Magnification increases and digital quantization error decreases as the size of the view decreases. Views normally vary in size from 10 to 25 mm in diameter. So the automated inspection system may use more than 100 views to cover a typical assembly. The system moves the assembly or the image sensor on a positioning stage from view to view. The sum of move time plus image acquisition time normally makes up most of the total inspection time for a particular assembly.

55.8.1.2 System Throughput. The test speed for solder paste inspection systems varies anywhere from 2 to 22 cm^2/sec. The high end of this speed range can be fast enough to keep up with many automated printed circuit production lines. But for the slower systems, or even for the fastest systems on very-high-volume production lines, manufacturers inspect a specific subset of paste depositions on every assembly coming down the production line.

55.8.2 Applications

Automated solder paste inspection systems typically reside in the fastest speed ranges on the system throughput scale and therefore are utilized as process control tools in addition to defect detectors. Manufacturers typically use these systems to monitor the process by tracking the key quantitative solder paste measurements, normally height and volume, against control limits. The systems then alarm any condition where control limits are exceeded or definite

drifts are detected, allowing the manufacturer to assess the production line and monitor or choose to take action until appropriate adjustments have been made. (The alarm generated by the system is normally an obvious flashing message on a computer monitor.) Because the paste printing process step causes a large percentage of all production defects, tight production control of this process step using quantitative measurements can significantly lower the process defect rate. In fact, automated solder paste inspection systems have been linked through software to paste printing systems, allowing not only process control, but also closed-loop feedback for semiautomatic adjustment of paste printing parameters based on the paste measurements.

55.8.3 Advantages and Disadvantages

Automated 3-D inspection of solder paste depositions has the following major advantages:

- Real-time process control of paste printing to lower defect rates and rework costs
- Quantitative measurements, including volume, to help permanently eliminate the causes of paste defects
- Defect detection where rework is easiest, before component placement and solder reflow
- Process characterization during the lead-free conversion with minimal program tuning

Automated inspection of solder paste depositions has the following limitations:

- It is sometimes too slow to cover all paste depositions on an assembly.

- It does not measure or detect defects in component placement or solder reflow.

55.9 PRE-REFLOW AOI

55.9.1 Operating Principles

Automated inspection systems designed for 2-D component placement and solder paste quantitative measurements typically use optical techniques consisting of multi-angle light sources and charged-couple device (CCD) cameras to generate images. As Fig. 55.10 indicates, these systems extract specific features, such as edges of the components or solder paste deposits, in the images and then use these features to determine quantitative measurements of component and deposit misalignment or deposit area.

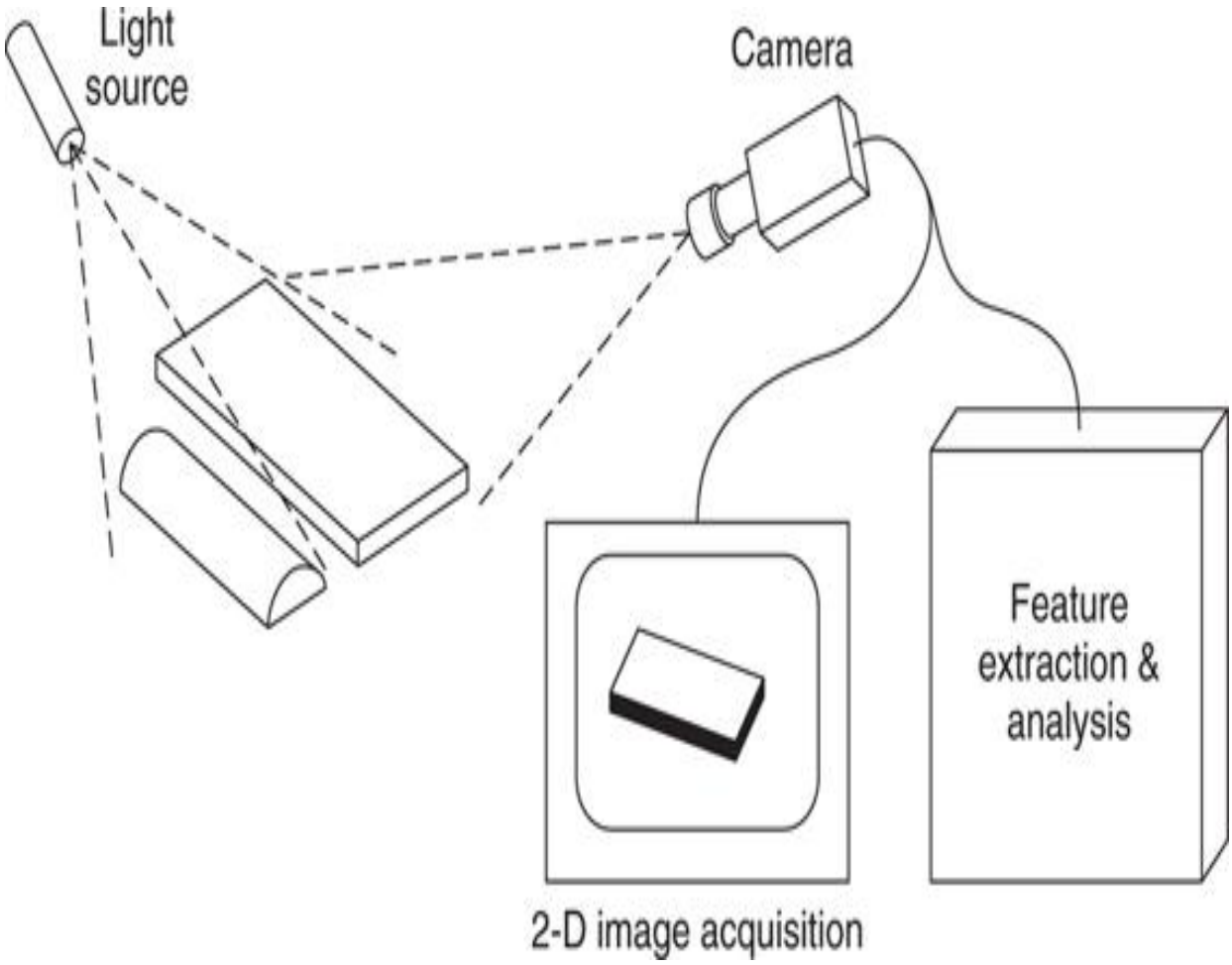


FIGURE 55.10 Schematic of automated inspection systems for component placement defect detection. The camera sensor obtains images of component positions relative to the printed circuit board. The image processing software extracts features from the image and compares them to present position limits to flag a placement as defective.

Automated optical inspection systems also image only a small portion, or *view*, of the assembly at a time. These systems normally can use somewhat bigger views than the 3-D solder paste systems because the features being extracted often do not require as much magnification as do measurements of solder paste depositions. However, inspection of components, such as 0402, 0201, and 01005 passive components, or very-fine-pitch deposits, can require the same level of magnification and therefore views as small as the 3-D solder paste inspection systems.

In general, pre-reflow AOI systems are typically two to three times faster than 3-D systems and range in inspection speed between 10 and 40 cm^2/sec. The prices of 2-D component and solder paste placement automated inspection systems are typically somewhat less than those of the 3-D solder paste systems with the fastest inspection speed capability.

55.9.2 Applications

The majority of pre-reflow AOI systems are placed directly following the pick-and-place process step in the production line. These systems therefore only measure the amount of misalignment of components and are generally fast enough to cover all components on a printed circuit board and keep up with the production line's cycle time. So manufacturers often use these systems to detect all misalignment defects as well as missing components. But the most important purpose of these systems is process control, just as it is for the 3-D solder paste inspection systems. The intent is to discover process drift early enough to prevent defects by tracking the key quantitative misalignment measurements against control limits. The systems then alarm any condition where control limits are exceeded or process drifts are detected, allowing the manufacturer to assess the production line and monitor or choose to take action until appropriate adjustments have been made. Some system suppliers in conjunction with pick-and-place equipment suppliers can develop closed-loop feedback software links allowing semiautomatic adjustment of the pick-and-place equipment.

Pre-reflow AOI systems also have the ability to inspect 2-D solder paste; however, this ability is utilized only to inspect a small percentage of the solder paste deposits combined with the component misalignment measurements. Component

misalignment measurements cover the passive components, whereas the solder paste measurements cover deposits for BGA, CSP, or fine-pitch QFP devices. Therefore, these systems are placed within production lines after the pick-and-place systems for passive devices but before the pick-and-place systems for the larger area-array and leaded devices. These systems serve the same purpose as those only meant for component placement measurement, both detecting defects and monitoring measurements within control limits to discover process drift as early as possible.

55.9.3 Advantages and Disadvantages

Pre-reflow AOI has the following major advantages:

- Real-time detection of systematic process defects where equipment is out of adjustment
- Detection of defects such as misalignment where rework is easier, before solder reflow
- Low-cost option for reasonable test coverage
- Process characterization during the lead-free conversion with minimal program tuning

Automated inspection of component placement has the following limitations:

- It does not measure or detect defects in solder reflow, and normally does not detect defects in solder printing.
- It does not measure 3-D for solder paste.

55.10 POST-REFLOW AUTOMATED INSPECTION

Solder joints have much more complex shapes than do solder paste depositions and components, so taking measurements of solder joints normally requires more complex imaging techniques than does measuring solder paste and components. Automated inspection systems for solder joints have used a variety of imaging technologies, including optical and x-ray imaging, thermography, cooling profiles of laser-heated solder joints, and ultrasonic imaging. But three technologies have dominated in these systems:

- Optical imaging using multiple light sources and cameras
- Transmission x-ray imaging
- Cross-sectional x-ray imaging

55.10.1 Post-Reflow AOI Systems

55.10.1.1 Operating Principles. Post-reflow AOI systems for solder joints are similar to, but more complex than, those for component placement. (Note that these systems also detect component defects such as missing, misaligned, or misoriented components, but their complex design is required for solder joint inspection.) Multicolor, multi-angled light sources are normally required to provide enough information in the images to allow sophisticated image-processing algorithms to detect the required features in the images accurately. If the light source is not multicolored or multi-angled, then many different cameras are usually used instead, each camera mounted at a different angle relative to the board being inspected.

The multiple light sources and cameras create and detect shadows from various angles to detect features of solder joints of all types oriented in different directions on the printed circuit assembly. These optical systems often use higher magnification, particularly for the smallest passive components and fine-pitch components, and therefore

capture a smaller portion of the assembly at any one time. The smaller views allow more image pixels per solder joint feature, allowing more accurate image processing and corresponding defect calls. The use of smaller views renders the throughput of these systems slower than that of component placement inspection systems. However, in general these systems are faster than 3-D solder paste measurement systems. Their throughput typically falls in the range of 10 to 40 cm^2/sec.

The systems' image-processing software uses sophisticated algorithms to extract specific features of solder joints, such as edges and areas of the solder joint in a specific range of angles relative to the board. Analysis of these extracted features then determines whether a defect exists or not. Defects detected include absence of solder, bridges, and grossly insufficient or excessive solder. These systems typically do not make quantitative measurements.

55.10.1.2 Application. These post-reflow AOI systems generate only attribute data. For instance, these systems detect the existence of a solder bridge between two joints or the absence or presence of a toe fillet on solder joints. But they do not measure the height of the heel fillet or the amount of solder in the solder joint. These systems typically do not measure how far a component is misaligned from its proper placement, but instead simply determine whether or not the component is misaligned more than a predetermined amount. These attribute data are not as useful for process control, and thus manufacturers use these systems strictly to detect defects. Normally these systems do, however, warn of a condition where the same defect has occurred several times consecutively or within a specific number of assemblies, indicating that some part of the process needs adjustment.

Post-reflow AOI systems cannot inspect hidden solder joints, such as those for ball grid arrays, pin grid arrays, and

in some cases J-leaded devices, and can have high false accept or reject rates for some component types, such as fine-pitch components at or below 0.5 mm pitch or small outline transistor (SOT) devices. If tall components are placed on the board very close to smaller components, post-reflow AOI systems can also have difficulty inspecting these smaller components.

55.10.1.3 Advantages and Disadvantages. Post-reflow AOI systems of solder joints have the following advantages:

- They eliminate visual inspection by automating solder joint defect detection, thereby also reducing unnecessary rework due to false reject calls.
- They reduce rework analysis time by pinpointing defects to the exact solder joint.
- They afford real-time process control of all three process steps—paste printing, component placement, and solder reflow—to lower defect rates and rework costs.
- They can be used during the lead-free conversion with minimal program tuning.
- They are a low-cost option for reasonable test coverage.
- Post-reflow AOI systems have the following limitations:
- Test throughput is not always fast enough to allow inspection of all solder joints within the manufacturing cycle time for the printed circuit assembly.
- A significant learning curve is required to become expert at developing solder joint tests with both low false accept and false reject rates.
- The ability to inspect hidden (or invisible) joints is not possible with post-reflow AOI.

55.10.2 Transmission X-Ray Systems

55.10.2.1 Operating Principles. Transmission x-ray systems radiate x-rays from a point source perpendicularly through the printed circuit assembly being inspected, as depicted in Fig. 55.11. An x-ray detector picks up a varying amount of x-rays depending on the thickness of metals that the x-rays are penetrating and converts the x-rays to light photons for a camera to create a grayscale image. The x-ray source is filtered so that metals of only a certain density range—lead, tin, gold, and silver—will absorb the x-rays. The copper leads and frames of components sitting on top of solder joints do not absorb the x-rays and are therefore practically invisible to the x-ray detector. Thus, x-ray systems can easily see the entire solder joint, no matter what component material may be on top of the joint blocking its optical or visual access. In other words, x-ray is the only automated inspection method equipped to inspect hidden joints such as those found in a BGA or CSP. The resulting x-ray image will be darker wherever the lead or tin solder or lead-free solder is thicker in the solder joint. The image processing capability of the system then searches for features, such as the heel and toe fillets, the sides of the solder joint, and even voids internal to the joint based on grayscale readings of the solder joint x-ray image. The system then uses predetermined decision rules to compare the grayscale readings to acceptance criteria to accept or reject a solder joint automatically. For example, the system might compare the relative grayscale reading for the heel fillet region, the center of the solder joint, and the toe fillet region. The acceptance criteria might state that the heel fillet reading should be twice that of the center and that the toe fillet reading should be 50 percent higher than that of the center. If the actual readings do not meet these criteria, then the solder joint is reported as being defective.

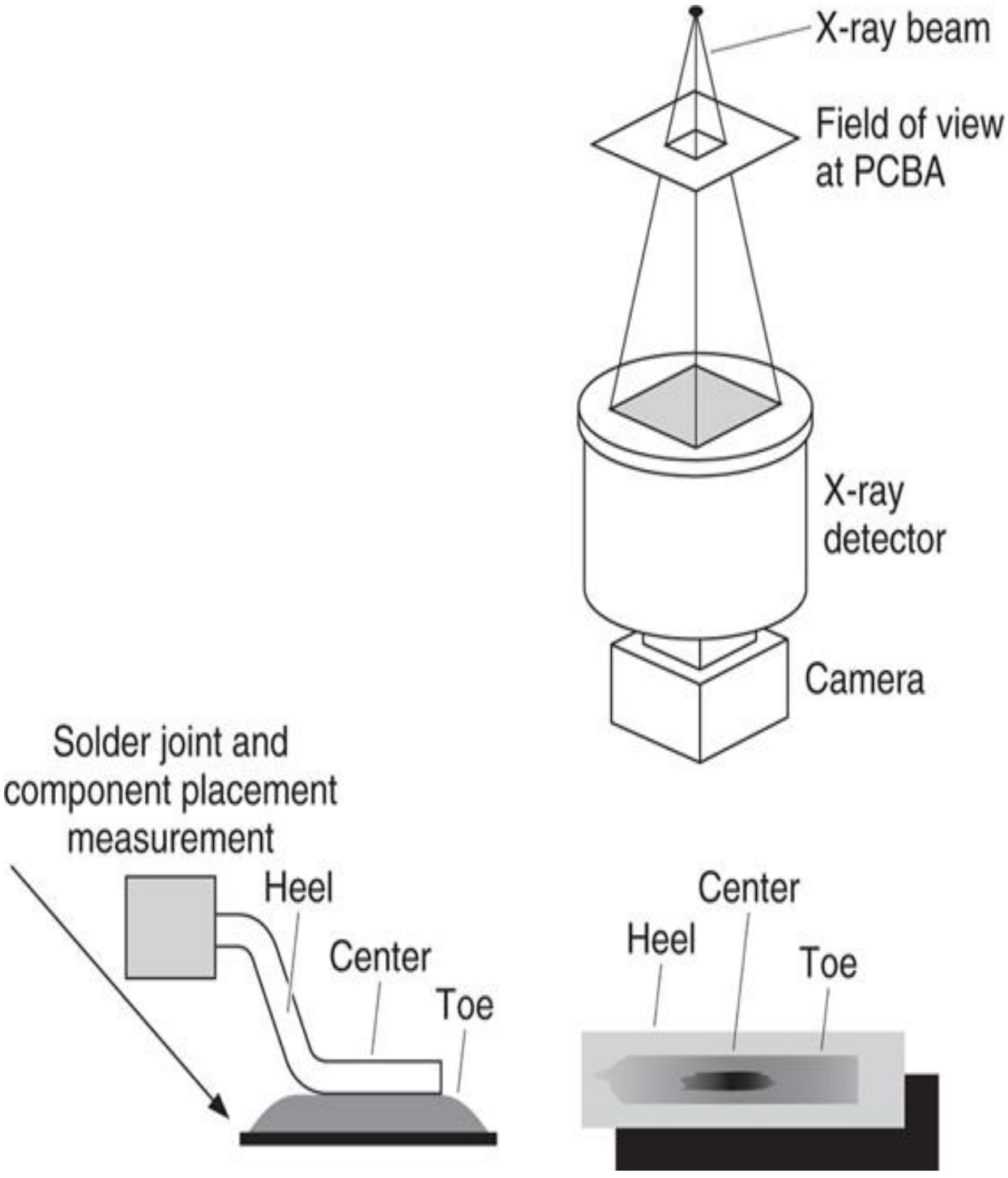


FIGURE 55.11 Schematic of transmission x-ray automated inspection system for solder joint defect detection. The x-ray detector converts a varying amount of x-rays to light, based on how much various parts of the solder joint absorb. The camera converts the light photons to an image, which is then processed to find solder joint features and flag defects accordingly.

The bottom of Fig. 55.11 shows an x-ray image of a gull-wing solder joint that shows the center of the joint as much darker than the heel fillet region. This solder joint is clearly defective, as the heel fillet region should always be darker and have a higher grayscale reading than the center of the joint, where the solder is thinnest for mechanically good solder joints. (The system's image processing capability is able to detect much more subtle changes in grayscales than can the human eye, allowing very accurate relative readings from one solder joint to the next.)

55.10.2.2 Application. Transmission x-ray technology works well for single-sided surface-mount assemblies. These automated inspection systems accurately detect solder joint defects such as opens, insufficient solder, excess solder, bridges, misalignment between pin and pad, and voids for most surface-mount solder joint types, including J-leads, gull-wings, passive chips, and small-outline transistors in hidden and nonhidden joints alike. These systems also detect missing components and reversed tantalum capacitors. Based on trends in grayscale reading, these systems also can accurately detect process drifts through real-time process control charting.

For double-sided assemblies, however, the transmission x-ray images of solder joints on the top side will overlap with the images of solder joints on the bottom side. The x-rays are absorbed by any solder in their path through the printed circuit assembly from the source to the detector. These overlapping images make accurate solder joint measurement impossible.

Transmission x-ray imaging also cannot easily distinguish between the top, bottom, and barrel of PTH solder joints or the bottom of BGA solder joints. So transmission x-ray systems cannot be used for accurate measurement of and defect detection in solder joints on double-sided assemblies or for PTH and BGA solder joints.

55.10.3 Cross-Sectional X-Ray Systems

55.10.3.1 Operating Principles. Cross-sectional x-ray systems radiate x-rays at an acute angle from vertical through the printed circuit assembly being inspected. As Fig. 55.12 indicates, images from all around the particular view being inspected are added together or integrated essentially to create an x-ray focal plane in space. This focal plane creates a cross-sectional image, approximately 0.2 to 0.4 mm thick, right at the focal plane, by blurring everything above and below the focal plane into the background, or *noise*, of the image. By moving the top side of an assembly into the focal plane, cross-sectional images of only the solder joints on the top side are created. By moving the bottom side of an assembly into the focal plane, cross-sectional images of only the solder joints on the bottom side are created. Separate images of top and bottom sides are always created, preventing any image overlap from the two sides.

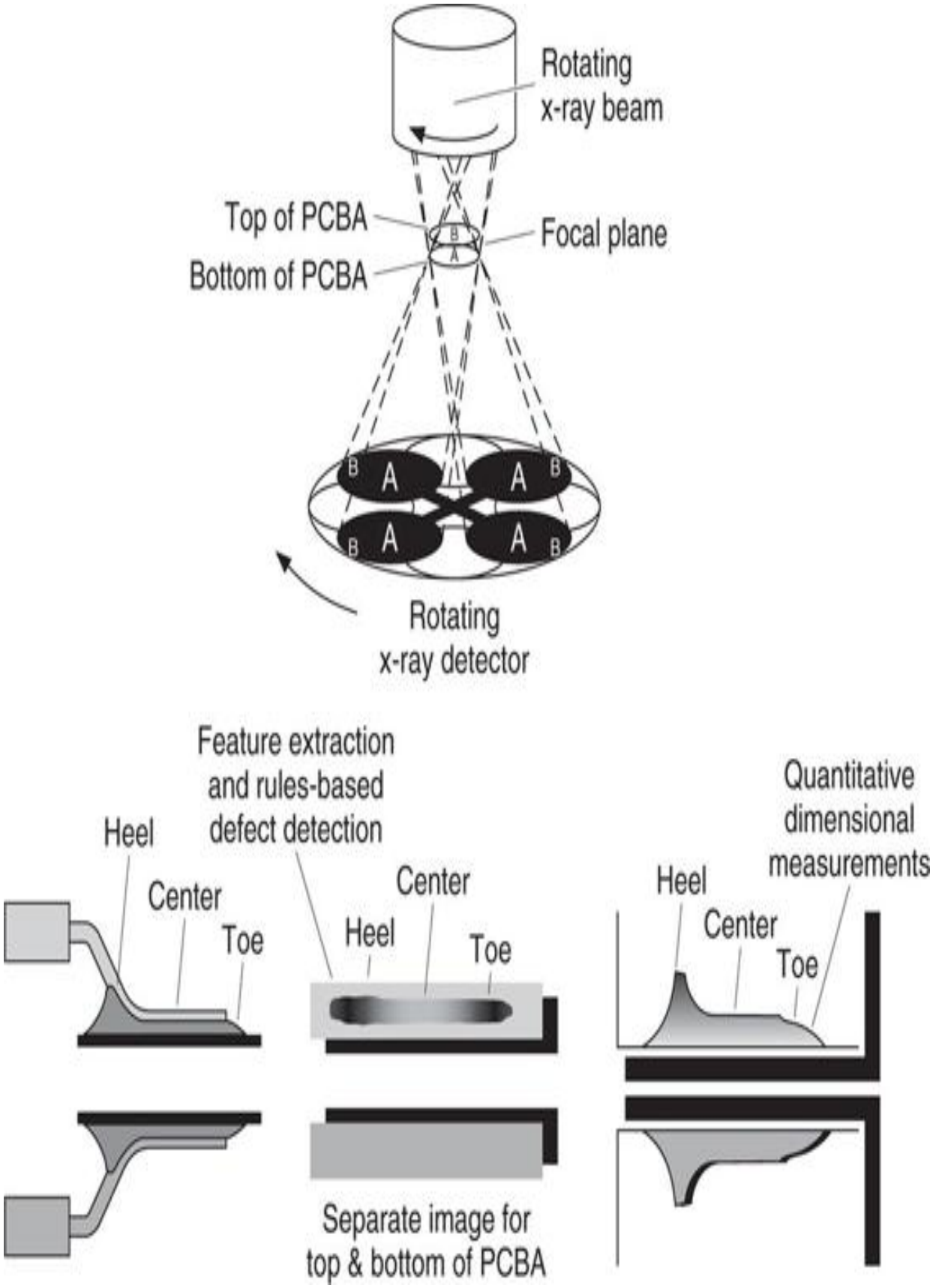
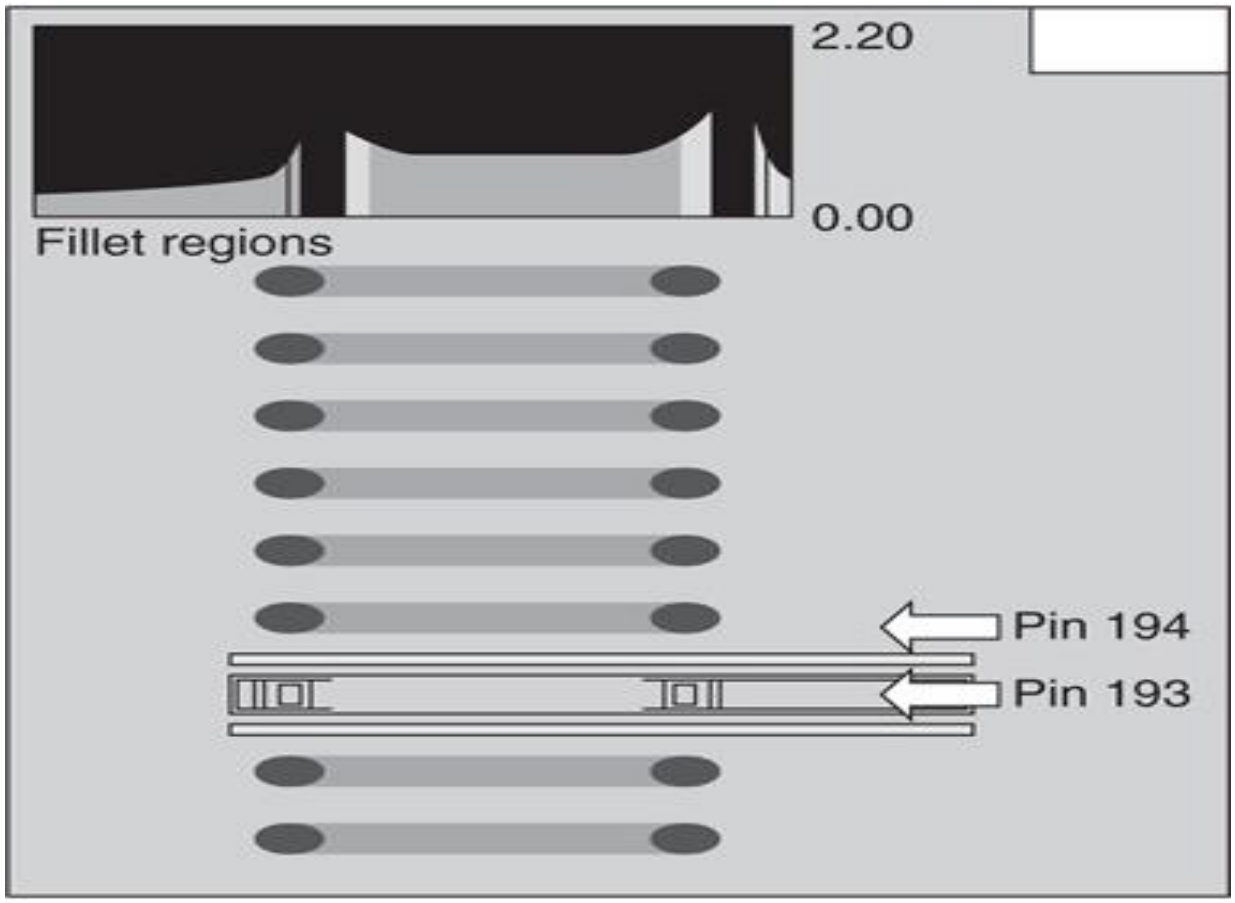

Rotating
x-ray beam
Top of PCBA
Bottom of PCBA
Focal plane
B
A
A
B
B
A
A
B
Rotating
x-ray detector
Feature extraction
and rules-based
defect detection
Heel
Center
Toe
Heel
Center
Toe
Quantitative
dimensional
measurements
Heel
Center
Toe
Separate image for
top & bottom of PCBA

FIGURE 55.12 Schematic of cross-sectional x-ray automated inspection system for solder joint measurement. Adding images around a circle from a rotating x-ray beam and detector creates a focal plane that captures just the solder joints of interest and nothing else below or above.

55.10.3.2 Application. Cross-sectional x-ray automated inspection systems work well for all types of printed circuit assemblies, including single-sided and double-sided, surface-mount, through-hole, and mixed-technology assemblies. These systems accurately detect the same solder joint and component defects as do transmission x-ray systems, but, in addition, the cross-sectional x-ray systems accurately detect insufficient solder conditions for BGA and pin-through-hole solder joints.

Some cross-sectional x-ray automated inspection systems go beyond just grayscale readings of specific solder joint features. By carefully calibrating grayscale readings to actual solder thickness, it is possible to generate real-world measurements, in physical units rather than grayscale numbers, of fillet heights, solder and void volume, and average solder thickness for the entire joint. Figure 55.13 shows an example of these calibrated measurements. This figure includes the actual cross-sectional x-ray image of tape automated bonded (TAB) solder joints.

Tape-automated bond (TAB)



Good board (pin 6)

Reference designator	Inspection point	Thickness (in 0.001")
U1 pin 193	Pad	0.59
	Heel	1.18
	Center	0.69
	Toe	1.34
U1 pin 194	Pad	0.58
	Heel	1.20
	Center	0.68
	Toe	1.30

FIGURE 55.13 Cross-sectional x-ray image of TAB solder joints. Image-processing software converts the grayscale readings of the image for pin 193 into the side profile of solder thickness shown above the image. The actual calibrated measurements of average solder thickness across the pad, heel fillet height, center thickness, and toe fillet height processed from the images of pins 193 and 194 are shown in the table below the x-ray image. These measurements indicate that both of these solder joints are good.

The profile shown at the top of the x-ray image is generated by the system in physical dimensional units by interpreting and calibrating the grayscale readings of pin 193 in the x-ray image.

The table below the x-ray image includes example measurements for both pin 193 and pin 194.

Analysis of these physical thickness measurements of solder joints provides the information required for process characterization and improvement. For instance, variations in average solder thickness or volume for the solder joints across a single assembly or from assembly to assembly provide insight into the quality level of the paste printing process as well as sources of defects.

The image-processing software then finds and measures solder joint features and flags defects accordingly.

55.10.4 Advantages and Disadvantages of X-Ray Inspection

X-ray solder joint inspection systems can reach average inspection speeds of around 50 to 150 joints per second. X-ray solder joint inspection systems also have higher prices, typically about 50 to 100 percent more than the price of the optical solder joint systems with the fastest inspection speed capability.

Automated x-ray inspection of solder joints has the following major advantages:

- Its defect detection capability is extremely high.
- It eliminates visual inspection by automating solder joint defect detection, thereby also reducing unnecessary rework due to false reject calls.
- It reduces rework analysis time by pinpointing defects to the exact solder joint.
- It affords real-time process control of all three process steps—paste printing, component placement, and solder reflow—to lower defect rates and rework costs.
- It provides quantitative measurements to help permanently eliminate the causes of defects from all three process steps.
- It reduces failures at final assembly and in the field due to defective hidden solder joints and marginal solder joints due to insufficient solder or misalignment or excessive voids.
- During lead-free conversion, it can be used with minimal program tuning.

Automated inspection of solder joints has the following limitations:

- Test throughput is not always fast enough to inspect all solder joints within the manufacturing cycle time for the printed circuit assembly.
- A significant learning curve is required to become expert at developing solder joint tests with both low false accept and false reject rates.

55.11 IMPLEMENTATION OF INSPECTION SYSTEMS

Successful implementation of automated inspection systems into printed circuit assembly production lines requires a significant investment in training, process analysis, and system integration.

The implementation can be a lengthy process that requires concerted effort by engineers or skilled technicians. Listed here are highlights of what several manufacturers have learned are key aspects of successfully implementing automated inspection systems:

- *Assess requirements carefully* Start by carefully assessing the requirements for automated inspection in the particular production environment into which the system will be integrated. Determine exactly what kinds of defects are most important for the inspection system to detect, which measurements will most help with process improvement, and what benefits will generate the quickest financial return on investment.[3] This assessment must consider the testing and measurement capability that already has been implemented as well as new requirements arising from future printed circuit assembly designs.
- *Evaluate a select set of systems thoroughly* Select a small number of automated inspection systems to evaluate thoroughly and compare them against the system requirements. The evaluation should include a benchmark using printed circuit assemblies from production to determine the system's capabilities to detect accurately the important defect types within the required false reject rate, repeatedly make the required measurements, and not exceed the required test time. Elements of cost of ownership should be well understood, including test development time, maintenance skills and cost, expected system downtime, supplier support infrastructure, and supplier maintenance services and prices.

- *Plan for factory system interfaces* Consider and plan carefully for interfaces to other factory systems. These systems include board-handling equipment, bar code–reading systems, computer-aided design (CAD) systems for automatic download of board layout and component package information, and quality data management systems for SPC and historical quality tracking.
- *Focus on SPC measurements* Start with a focus on SPC measurements instead of defect detection. Until the process variation is reduced, most manufacturers will encounter either a false reject rate or a false accept rate that is higher than desired. Allowing one rate or the other to be too high while focusing on reducing the process variation first avoids time-consuming, unproductive tweaking of acceptance thresholds. Reducing process variation requires correlating measurements to the process parameters causing the variation and defects, and then properly adjusting these process parameters.[4]
- *Define defects carefully* With an understanding of the selected system's capability, carefully define the defects that must be detected for product quality and reliability. Many of the visual inspection criteria used in the past are not appropriate for automated inspection systems because the system takes objective and different measurements.
- *Invest enough resources* Do not underestimate the initial resource investment required to obtain optimum benefit from an automated inspection system. The implementation plan should include dedicated technical support for the first six months of operation and test development. Developing a thorough understanding of the measurement results and correlating the data to process parameters are key to successful use of the system. Implementation should also address the fact that production personnel will have to be convinced of the

accuracy of the system's test results before full benefit can be obtained from the system.

55.12 DESIGN IMPLICATIONS OF INSPECTION SYSTEMS

Automated inspection systems in general do not require many changes or limitations in the design of printed circuit assemblies. Because these systems use noncontact measurement techniques, fixturing requirements present very few design limitations, for instance. However, the following requirements will facilitate automated inspection if they are considered during printed circuit design.

55.12.1 Automated Board Handling Requirements

- Parallel edges of the assembly or panel must have adequate clearance (typically at least 3 mm), to allow board-handling clamps or belts to grab the assembly.
- Three corners of the assembly or panel must include alignment fiducials (or solder joints in post-reflow configurations).
- Bar code identification of assembly number and serial number must be present at a predefined location on each printed circuit assembly.
- The board must be adequately rigid without a fixture to prevent excessive board vibration during movement.

Panels with prerouted breakaway boards or bare boards less than 30 mil thick present the biggest challenge: Component, heat sink, or daughter-board height above or

below the bare board must not exceed the height clearance of the targeted automated inspection system.

55.12.2 Test Development Ease of Use Requirements

- There should be as few suppliers as possible (ideally one) for each component type. Variation in lead and component package dimensions from supplier to supplier for the same component forces longer and more difficult development of inspection programs for each printed circuit assembly type.
- Pad shapes and sizes must be uniform, particularly for each component package type. Variation in pad size and shape within a component package type forces longer and more difficult development of inspection programs for each printed circuit assembly type.
- Solder joints for optical and structured light automated inspection systems must be clearly visible.
- For transmission x-ray automated inspection systems, no components should be opposite or under dense structures, such as transformers, large capacitors, or thick steel heat sinks.
- There should be no silk-screened outlines around components. Although such outlines may be useful for visual inspection, they just confuse automated optical inspection systems.

55.13 REFERENCES

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3. Baird, Dennis L., “Using 3D X-Ray Inspection for Process Improvements,” *Proceedings of Nepcon West Conference*, Hughes Aircraft Company, Cahners Publishing, 1993.

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CHAPTER 56
DESIGN FOR TESTING

Kenneth P. Parker
Agilent Technologies, Loveland, Colorado

56.1 INTRODUCTION

In the latter part of the 1970s, it became clear that forces of technology were causing an evolution in board complexity that was quickly outstripping testing technology. It is quite possible to design boards that essentially cannot be tested in an economical sense. This will doom projects and products to failure.

The author has personal experience here, having consulted in the mid-1970s with a Silicon Valley start-up company that had created one of the first dedicated word processors. This product was based on a customized processor that had been designed and sent into production with absolutely no thought about how it was to be produced in volume. There was no test strategy. When it was determined that volume production was impossible, the design team was brought onto the production floor in a last-ditch effort to produce shippable units. High-priced design engineers could only

produce one or two units a day, and they were no longer available for developing the next product. The company soon failed, a casualty of untestable design. The marketplace never got a chance to determine whether their product idea was a winner, because their design process was a loser!

In the 1970s and into the 1980s, it was very common for a design department to be physically and organizationally removed from the test department. The nature of product life cycles dictates that by the time a test department starts ramping up test program development for a board, the design team is off on the next project and finds it distracting to go back and help the test engineers with testing problems. Thus, in those years, the designers were unknowing contributors to difficult test problems. But what is different today, with the emphasis on outsourcing and contract manufacturing? Now, a design may be outsourced to one contractor, board layout to a second, test development to a third, and actual production to a fourth, all scattered about the globe.

Even if boards can be tested, the question bears asking, “Is there something a designer can do that will make testing easier, cheaper, more thorough, etc.?” The answer is that there is a great deal a designer can do (or fail to do) that will affect the testability of a board. The technology that addresses this problem is called design for testability (DFT).

By the middle of the 1980s, testing became a bottleneck in product development. The situation ultimately became severe enough that attention was paid to the effects that design has on testing. A landmark survey on DFT technology by Williams and Parker[1] brought DFT out of common lore and into the design lexicon of the electronics industry. That paper is still remarkably current[a] nearly 20 years later. In it were coined the terms *ad hoc testability* and *structured testability*. Before jumping into the DFT discussion, however, some definitions are crucial.

56.2 DEFINITIONS

These definitions are fully discussed in Chap. 55 and are repeated here in an abbreviated form for reference.

1. A *defect* is an unacceptable deviation from a norm.
2. A *fault* is a physical manifestation of a defect.
3. A *fault syndrome* is a collection of measured deviations from an expected good outcome.
4. A fault is *detected* when an operation with an expected outcome is conducted and this outcome is not observed.
5. A fault is *isolated* when an operation with an expected good outcome and one or more failing syndromes is conducted and the outcome matches a member of the set of failing syndromes.
6. A *test* is one or more experiments that are specifically constructed to detect (and possibly isolate) failures.
   - A *detection test* has an expected good outcome.
   - An *isolation test* has an enumeration of possible fault syndromes indexed to specific failures.

The technology of testing, as covered in Chap. 55, is highly influenced either positively or negatively by the design of boards being tested. If the preceding definitions are not clear, then the discussion of loaded board testing should be digested first.

56.3 AD HOC DESIGN FOR TESTABILITY

Ad hoc design for testability consists of a set of simple design rules of the form “Do this, don’t do that,” where “this” and “that” are often not motivated with reasons. For

example, when designing a board with ICs that have preset or clear pins, a rule might read as follows:

“Tie unused preset and clear pins off through a 100-Ω resistor to a power rail; do not tie them directly.”

The first-level reason for this is that a test engineer might want to access the preset/clear functions during testing, even though the designer did not use these functions. If these pins are tied through a resistor, a test engineer may still be able to manipulate them by applying a tester resource to them that can drive a signal in spite of the resistor. If these pins are tied directly to a power rail, the test engineer will never have that option. What might the difference be? Well, in a deeply sequential circuit, controlling the preset and clear functions might make the difference between a test that runs in milliseconds versus hours. Clearly, hours of testing (per board) are impractical, so the bottom line may be the difference between a thorough test and one that lacks significant fault coverage, affecting quality.

The real reason for the various ad hoc DFT rules is that, to effectively and economically test a circuit, one must be able to control and observe the circuit’s behavior. Most rules are related to controllability and/or observability of the circuit. The rule just cited is a controllability rule. Observability rules typically suggest ways one might be able to monitor signals that are deeply embedded in combinatorial circuitry, or that are activated only rarely by complex sequential events.

Ad hoc DFT is essentially the only way many products can have improved testability when those products are constructed with off-the-shelf merchant parts. Large, vertically integrated companies have the advantage of being able to customize testability into the heart of a design, including the very ICs themselves. Application-specific ICs (ASICs) allow more of this as well.

56.3.1 Physical Access

Testing is performed once the board to be tested is connected by some adaptor mechanism to the test system. This may be accomplished via the edge connector(s) of the board, where the tester is given the same access that the board gets in its end application. But far more common is “bed-of-nails” in-circuit test access, where the board to be tested is physically mounted on a platen and depressed into a field of precisely positioned spring-loaded probes (“nails”) that contact hundreds or perhaps thousands of internal board nodes. (See Sec. 55.4.2 in Chap. 55.) This can be a challenging mechanical proposition to implement, particularly when high-volume, reliable manufacturing is the goal.

Board designers must consider physical attributes of their boards early in the design process. They have a size target and then often find that there are density issues that may require fine-line geometries and two-sided component mounting to solve. The fact that in-circuit bed-of-nails access may be needed for testing should also be considered very early. See Ref. 2 for an excellent discussion of how test target pads need to be provided, and how artifacts of the board layout (particularly vias) may be used to satisfy some of these needs. However, due to the density revolution, full nodal access, which has been the holy grail of in-circuit testing, is often impractical. This leads to the question of what access is most important when full access is impossible. The answer to this question comes from the domain of circuit design.

56.3.2 Logical Access

Sometimes it is impractical to gain physical access to all nodes of a circuit. For example, Fig. 56.1(*a*) shows an IC

containing a large amount of complex logic, much of it deeply buried and effectively inaccessible from the I/O pins. Figure 56.1(*b*) shows the same IC with two additional gates added. The first is an exclusive OR gate that collects three buried signals, adds them together,[b] and brings the result to a spare I/O pin. This makes the states of those three signals much more observable. The second gate is an OR gate that allows us to insert a 1 from a spare input pin[c] into a deeply buried portion of the circuit. The assumption here is that the modified signal rarely reaches the 1 state in normal operation, so this extra controllability enhances our ability to manipulate the circuit for test purposes. Adding these extra gates can make it much easier to control and observe the performance of the IC. However, the downside is that we consumed a small amount of silicon area for the two gates, and, perhaps more importantly, we utilized two additional I/O pins. For many ICs, the extra cost of the pins could be a negative factor.

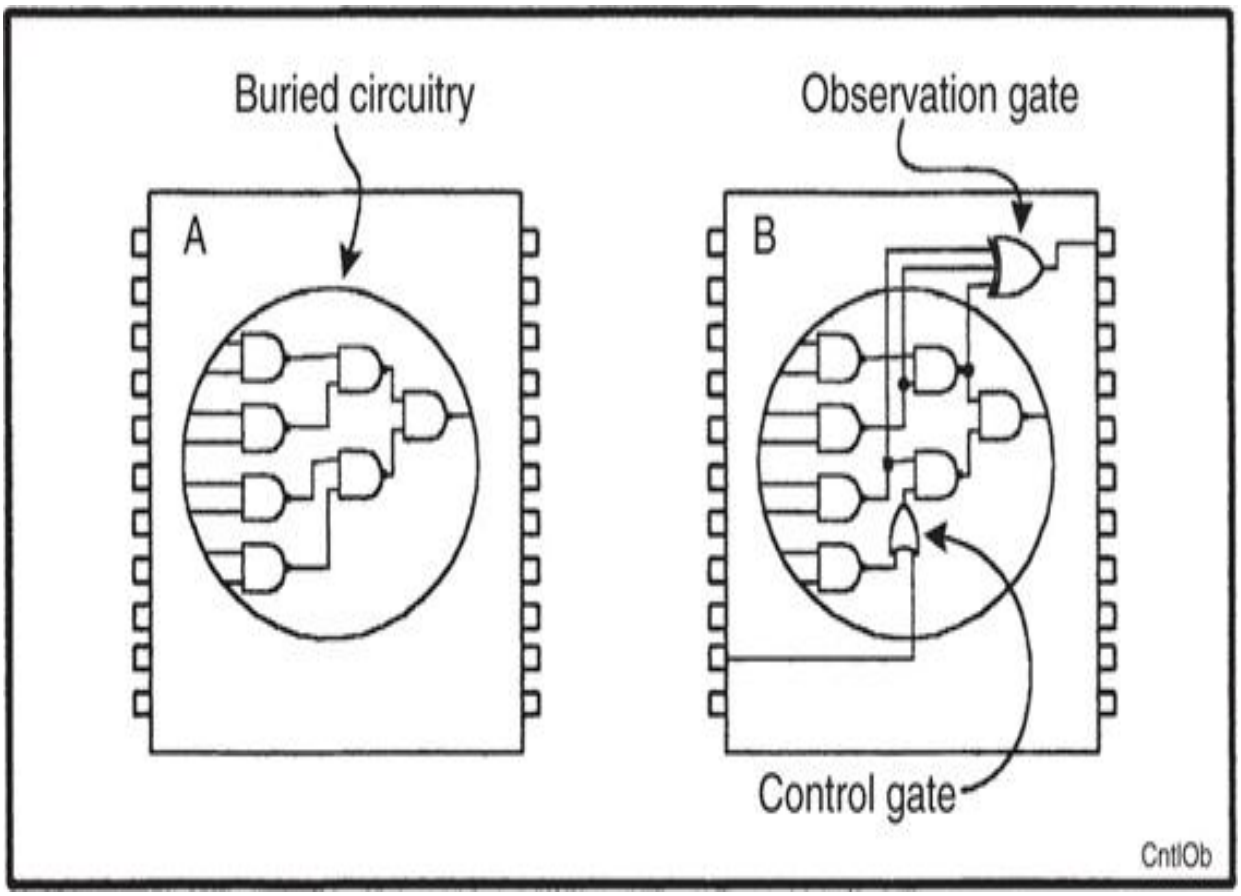

FIGURE 56.1 (*a*) An integrated circuit with deeply buried logic. (*b*) Same IC with controllability and observability logic added.

The choice of the optimal places to insert controllability and observability is not always clear, but rather is a trade-off of extra circuitry and pins vs. the difficulties that may be experienced in creating tests. There may be additional concerns as well with respect to circuit performance. For example, adding the controlling OR gate in Fig. 56.1 could add some signal propagation delay into the affected pathway, with detrimental results on system performance. When ad hoc circuit modifications are made for the sake of testability, it is likely that “seat-of-the-pants” decisions will be made rather than critical analysis. One person’s decisions might be remarkably different than another’s, with resulting great variability in testability improvements.

56.4 STRUCTURED DESIGN FOR TESTABILITY

Structured DFT was born inside companies that had vertical control over their designs, from custom ICs through systems. They also were well aware of their testing costs and realized that initial design decisions had a large impact on these downstream costs.

These companies studied the controllability and observability problems and instituted design rules into their design processes that, when followed, would guarantee that a circuit was testable. In the test department, where they also had complete control, they could utilize these added features with customized test development processes, gaining greatly enhanced levels of automation.

One of the earliest and most prominent structured DFT schemes was IBM's Level Sensitive Scan Design (LSSD), which was developed in the 1970s.[1] It is the precursor to what is called full internal scan technology now. In (greatly simplified) summary, LSSD design discipline requires every memory element (flip-flop or latch) to be constructed such that it obeys a testability protocol. This protocol allows two modes of operation: first, the normal operation of being a memory element in a design; and second, an operation for testing purposes, in which all memory elements can be connected into a serial shift register that can be loaded and unloaded by serial shifting. This makes every memory element a control point and an observation point within a circuit. No other memory elements are allowed in the design, e.g., no asynchronous feedback is allowed. This guarantees that circuitry between any control/observation point is combinatorial, not sequential (Fig. 56.2).

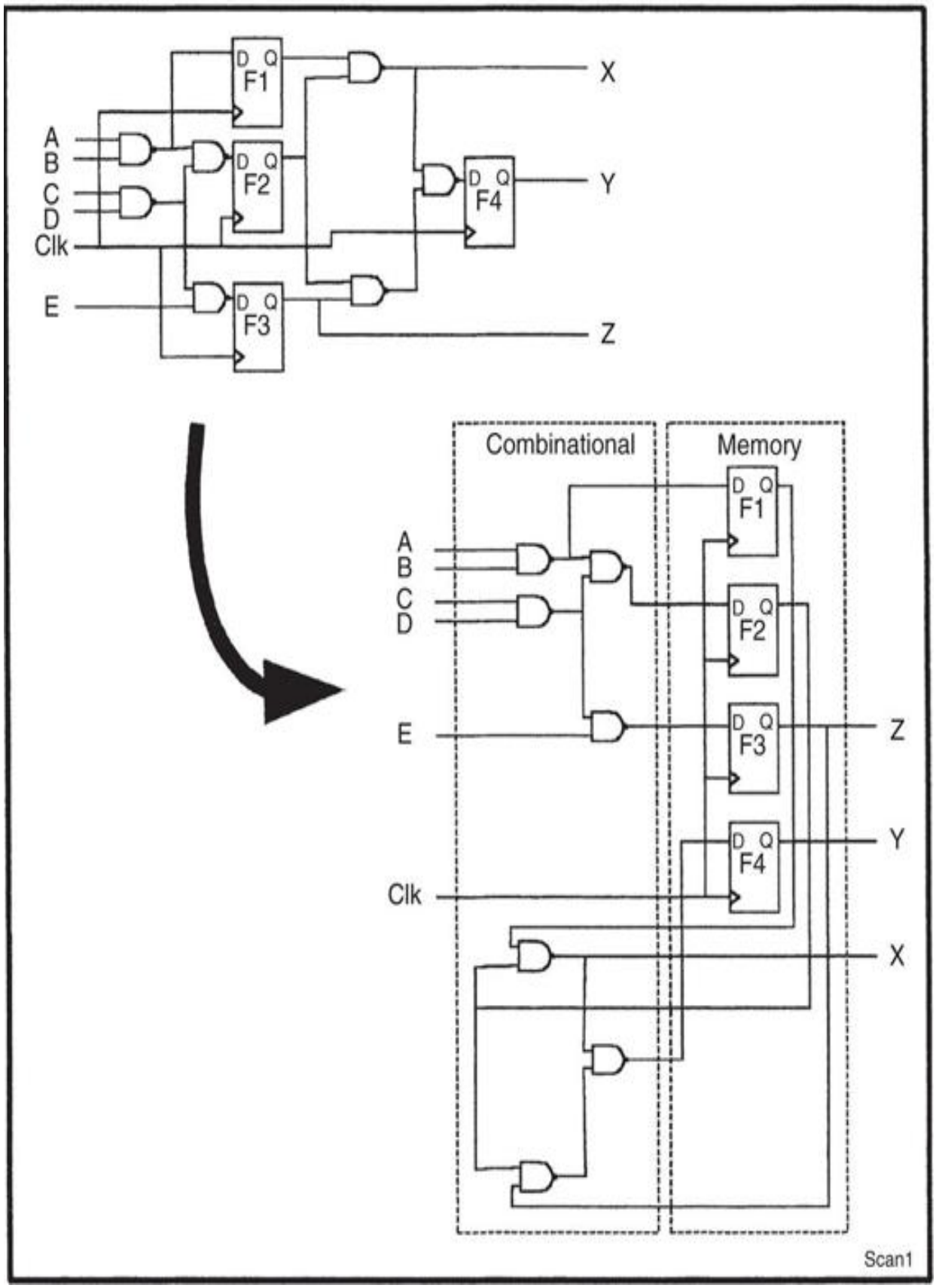
D Q
F1
F2
F3
F4
A
B
C
D
Clk
E
X
Y
Z
Combinational
Memory
Scan1

FIGURE 56.2 Circuitry made up of gates and flip-flops, redrawn to show that it can be represented as a bank of memory elements and a combinatorial circuit.

As might be imagined, these rules were looked upon by designers as restrictions of their creativity. Ed Eichelberger of IBM, a major proponent of LSSD, happens to stand about 5.5 feet tall. When asked in 1977 how designers received the LSSD rules, he quipped that, at the start, he was over 6 feet tall. Structured testability is not easy to implement. It requires commitment from the whole organization, starting with management.

The next piece of the puzzle was IBM's test generation software, which was able to automatically construct complete tests for combinatorial circuits (known as the D-algorithm and its derivatives). These tests could be shifted into the circuit and applied, and the results shifted out. This takes a lot of bookkeeping, but computers are good at that.

By using the LSSD discipline, IBM could verify that its designs would be completely testable, and those tests could be created by a computer program. Other companies such as Sperry Univac, Amdahl, Hitachi, etc., had similar proprietary structured approaches. Most smaller, nonintegrated companies were not able to participate in structured DFT—that is, until nonproprietary industry standards came into play.

56.5 STANDARDS-BASED TESTING

In the closing years of the 1980s, it became apparent that some sort of structured testability technology had to become accessible to the electronics industry at large. A small group of European companies led by Philips formed the Joint European Test Action Group (JETAG) and began work on a testability standard. The effort quickly attracted the notice of North American companies, giving rise to the JTAG standard.

As the proposal took shape, it was turned over to the IEEE, which ultimately produced IEEE Standard 1149.1-1990, Standard Test Access Port and Boundary-Scan Architecture,[3] in 1990.[d] Soon after 1149.1 came into being, a companion effort created IEEE Std 1149.4-1999, Standard for a Mixed-Signal Test Bus.[4] A complete coverage of these standards is beyond the scope of this chapter (see Ref. 5), so a brief summary is given here for an overview.

56.5.1 IEEE 1149.1, Boundary-Scan for Digital Circuits

The IEEE 1149.1 standard is a design discipline for digital ICs. It is a set of rules impressed primarily on the I/O structures of a device that allow two modes of operation, normal mode and test mode. In normal mode, the device performs its intended function. In test mode, the device obeys a protocol that has mandatory, optional, and customizable elements. The mandatory elements must exist, with the others being left as design options. The principle mandatory element of interest is a test mode dedicated to external test or EXTEST. When an 1149.1-compliant device is in EXTEST mode, its I/O pins are divorced from their normal operation and all internal functions of the device. Instead, the inputs become observation resources and the outputs become control resources[e] for test purposes. These resources are under control of the 1149.1 serial scan protocol. One can think of the I/O pins of the device being connected to shift register cells; states can be shifted in that will finally appear on all output pins (control) and the states of all input pins can be captured and shifted out (observe). This gives 1149.1-cognizant software a powerful tool for controlling and/or observing board-level node states. Figure 56.3 shows a simplified overview of the architecture.

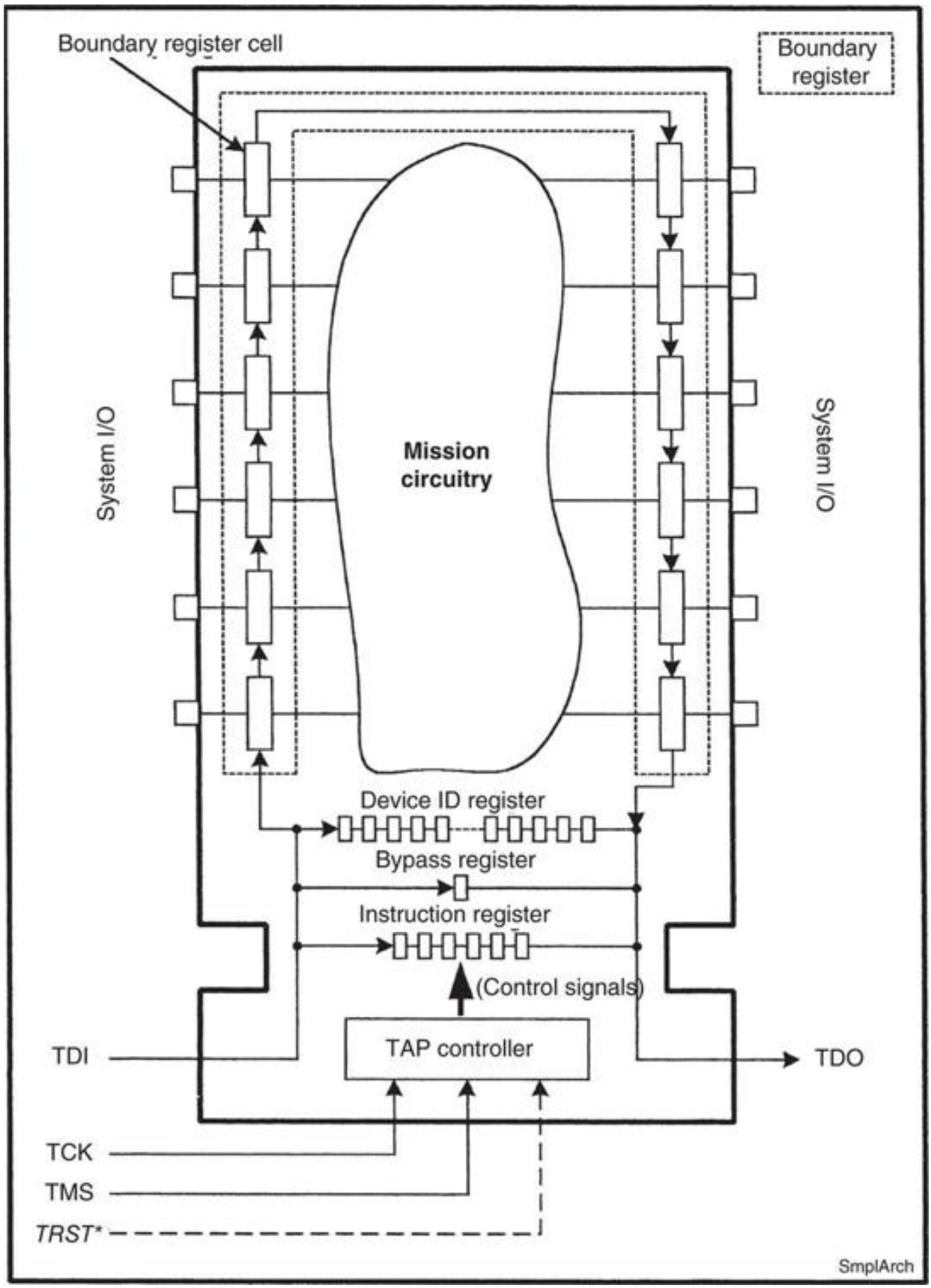
Boundary register cell
Boundary register
System I/O
Mission circuitry
System I/O
Device ID register
Bypass register
Instruction register
(Control signals)
TAP controller
TDI
TDO
TCK
TMS
TRST*
SmplArch

FIGURE 56.3 General architecture of an 1149.1-compliant integrated circuit.

Boundary register cells interposed between the IC pins and the internal logic surround the normal content of the IC called the mission logic. A small state machine called the test access port (TAP) is used to control the test functions. Four mandatory test pins (test clock [TCK], test mode select [TMS], test data in [TDI], and test data out [TDO])[f] give standardized access to the test functions. All 1149.1 devices have a 1-bit BYPASS register used to bypass the (much longer) boundary register if it is not needed in a given testing activity. Figure 56.3 also shows an optional IDCODE register that can be shifted out to uniquely identify the IC, its manufacturer, and its revision.

It is intended that collections of ICs (called chains, as shown in Fig. 56.4) with 1149.1 be connected TDO-to-TDI so that they may form a long, shiftable register structure. The primary use for the 1149.1 EXTEST capability is to conduct board-level tests for shorts and opens. This is an example of how resources included in an IC design may be used to help with the testing problem at other levels in the manufacturing process.

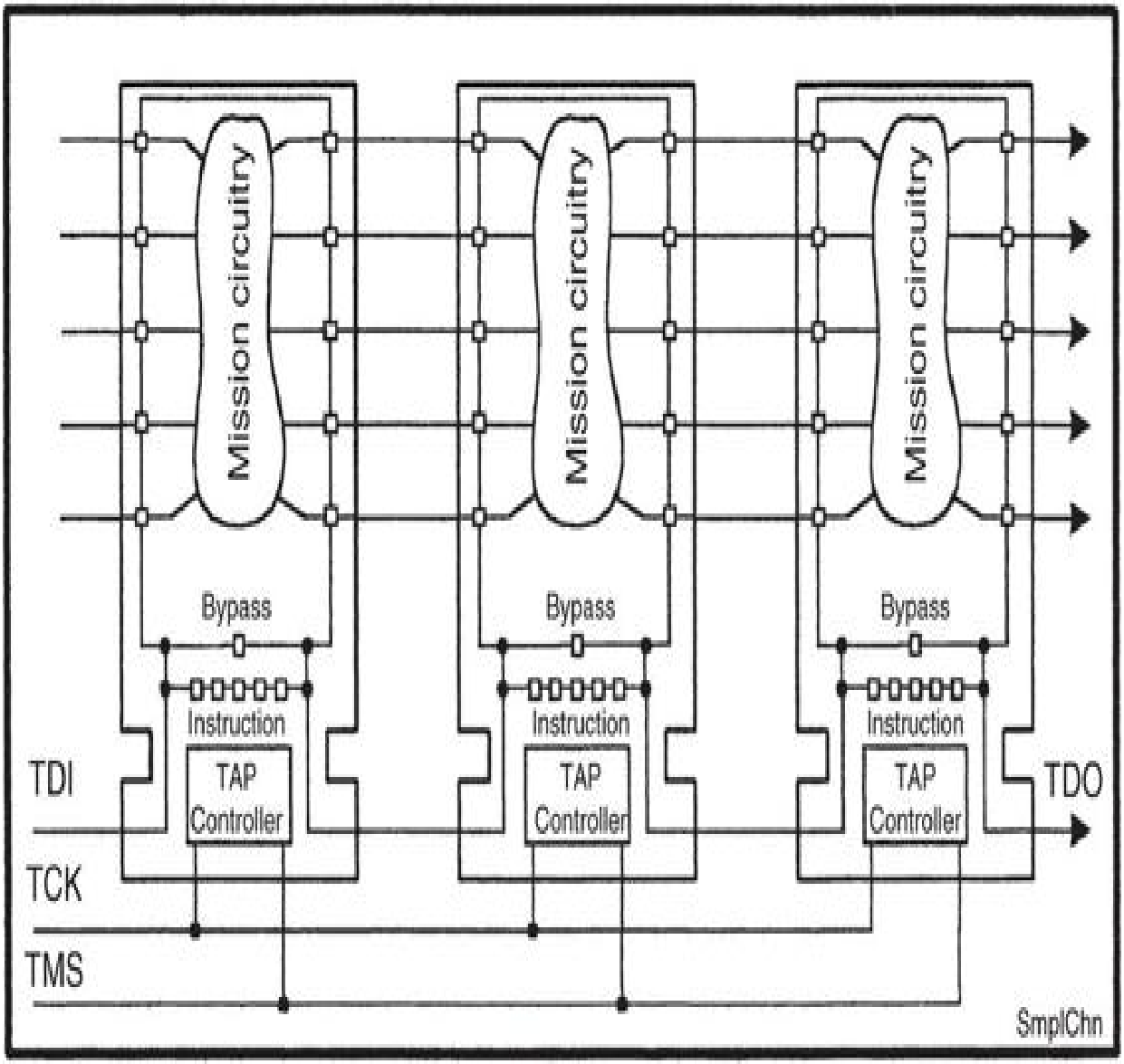

FIGURE 54.4 A collection (chain) of boundary scan devices can be used to test interconnections between ICs.

Briefly, interconnections between ICs are tested as follows. Consider the circuitry in Fig. 56.5. Some circuit nodes (also known as *nets* or *traces*) are accessible with a bed of nails and some are not. (To avoid clutter, the TCK and TMS signals are not shown.) Boundary scan can be used to test all the nodes; those with nails can be tested by coordinating nails with boundary scan resources and those without nails are tested solely with boundary scan.

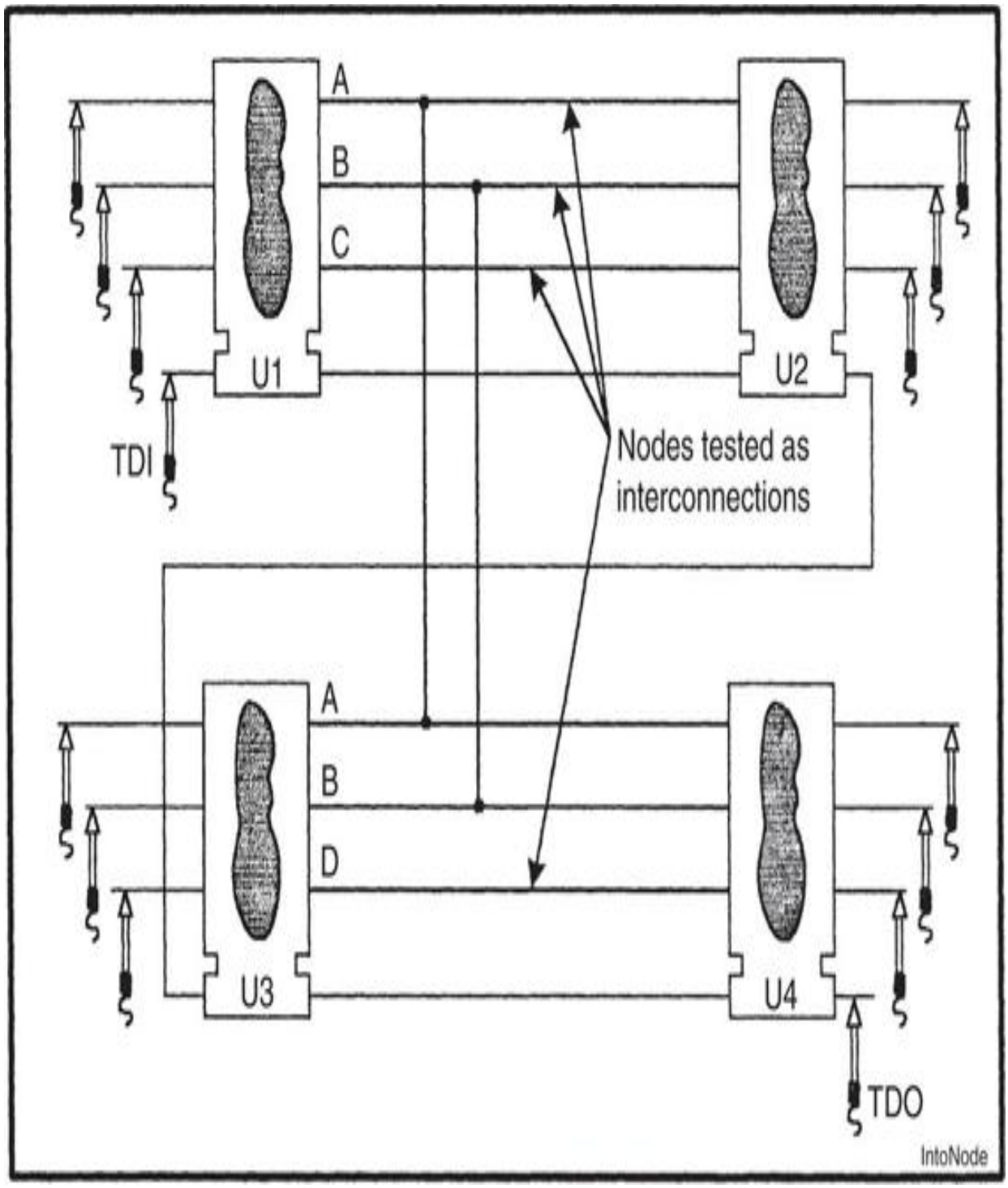

FIGURE 56.5 A set of boundary scan ICs with interconnections. Note that four nodes do not have bed-of-nail access.

As an example of this, boundary scan can be used to supply test patterns to nodes through a serialization process

that a human would find laborious, but that is simple for a computer. When a set of patterns has been delivered (to control) and monitored (to observe) by the appropriate boundary register cells, we have uniquely identified each node with a “signature.” A defect such as a short will cause two nodes to have deviant signatures, as shown in Fig. 56.6. Software can correlate observed deviations with the known boundary scan structure of each IC and the board netlist to yield a diagnostic message.

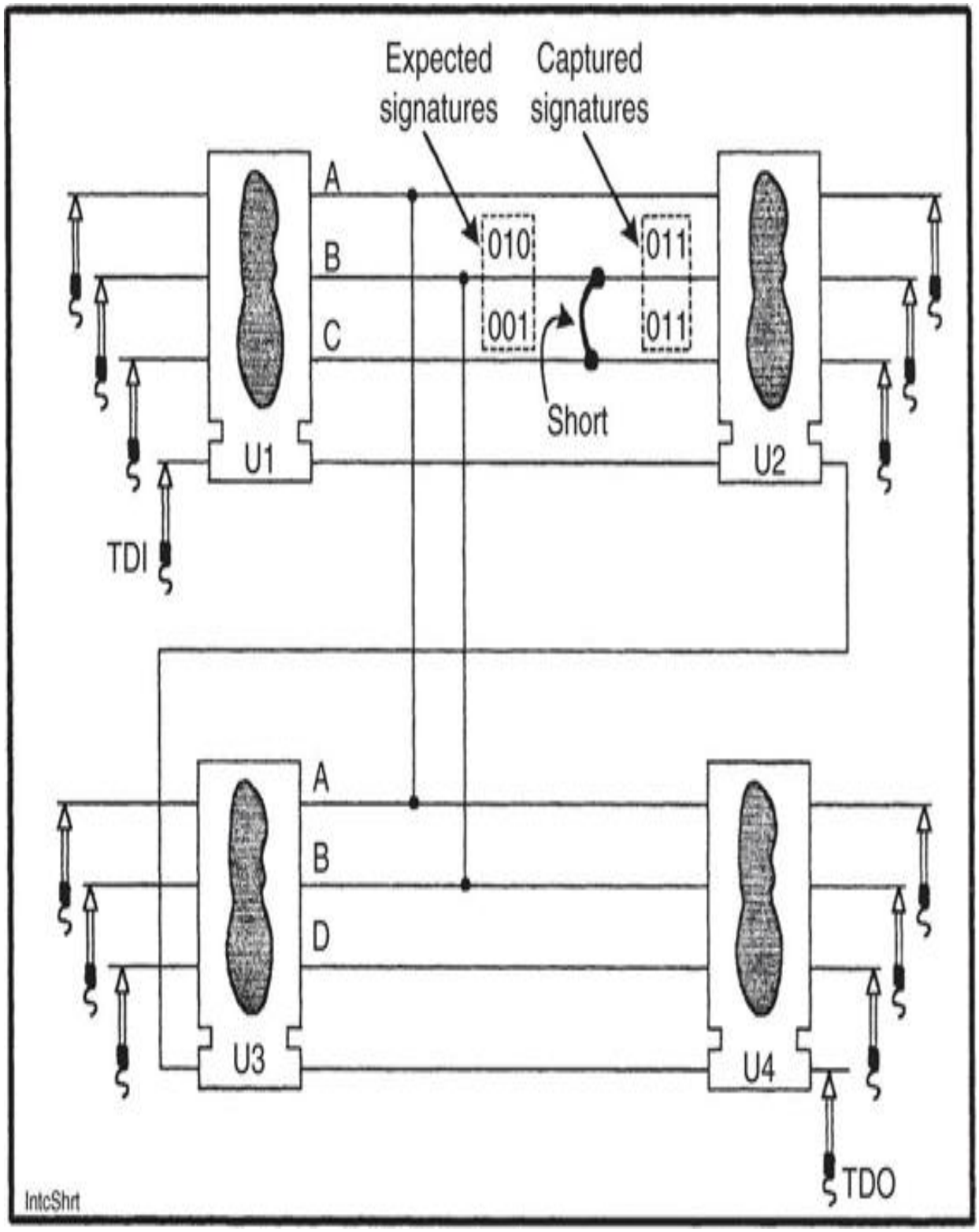

FIGURE 56.6 Interconnect testing drives unique patterns assigned to each node from drivers to receivers. In this case, a short is shown that creates a wire OR result.

The EXTEST capability can also be used during system testing to see if there are any system integration problems such as bad connections in backplanes and cabling. An IC designer may not see much attraction in EXTEST, but the 1149.1 standard offers other test modes that will allow a designer to access internal scan paths or built-in self-test functions. The 1149.1 standard's name has two parts, *Standard Test Access Port* being the first and crucially important one. It signifies that the standard anticipates being used as a standardized protocol for accessing any on-chip, board-level, or system-level testability scheme. In support of this, the standard is deliberately extensible, allowing clever designers to implement additional operational modes that can be used to solve unique testing problems.

The 1149.1 standard has proven itself to be quite useful and it has several contributions. First, it allows the creation of software that can automatically write tests for boards where in the past the same level of test effectiveness was nearly impossible to achieve, and then only with weeks or even months of skilled labor. It is not uncommon to see a boundary scan board test prepared in a single day that otherwise might have taken weeks. Second, 1149.1 ICs can "read" their input pins and scan out the result. This allows diagnostic software to pinpoint the location of open solder problems where in the past an IC might have been falsely indicted as faulty. Third, it allows tests to be performed on digital circuits without 100 percent accessibility to board nodes. With the trend toward miniaturization of components making it difficult to provide full nodal access, boundary scan is allowing the elimination of many access points. Of course, not all points may be eliminated, so one must understand which are still necessary. Finally, because many industry segments are affected by the test problem, a standard offers a way for everyone to benefit. One can find a large number of applications and tools available to solve testing problems that would not have been possible without a standard.

56.5.2 IEEE 1149.4, Boundary-Scan for Mixed-Signal Circuits

Boundary scan (1149.1) is a digital testability standard. However, there is also a trend in the superintegration of circuitry toward higher mixed-signal digital-analog content in our designs. The IEEE has developed a mixed-signal testability bus with a new standard 1149.4.[4–6] This standard is constructed as a superset of 1149.1 boundary scan, adding two additional analog test pins to the definition. The goal of the standard is to support opens and shorts testing of mixed-signal boards and to provide the capability of making analog value measurements of discrete analog components such as resistors, inductors, and capacitors without direct nodal accessibility, that is, a full bed of nails. (See Fig. 56.7.) It has been likened to in-circuit testing without a bed of nails, which is again not without caveats. (The elimination of test access points will still have to be done with thoughtful deliberation.)

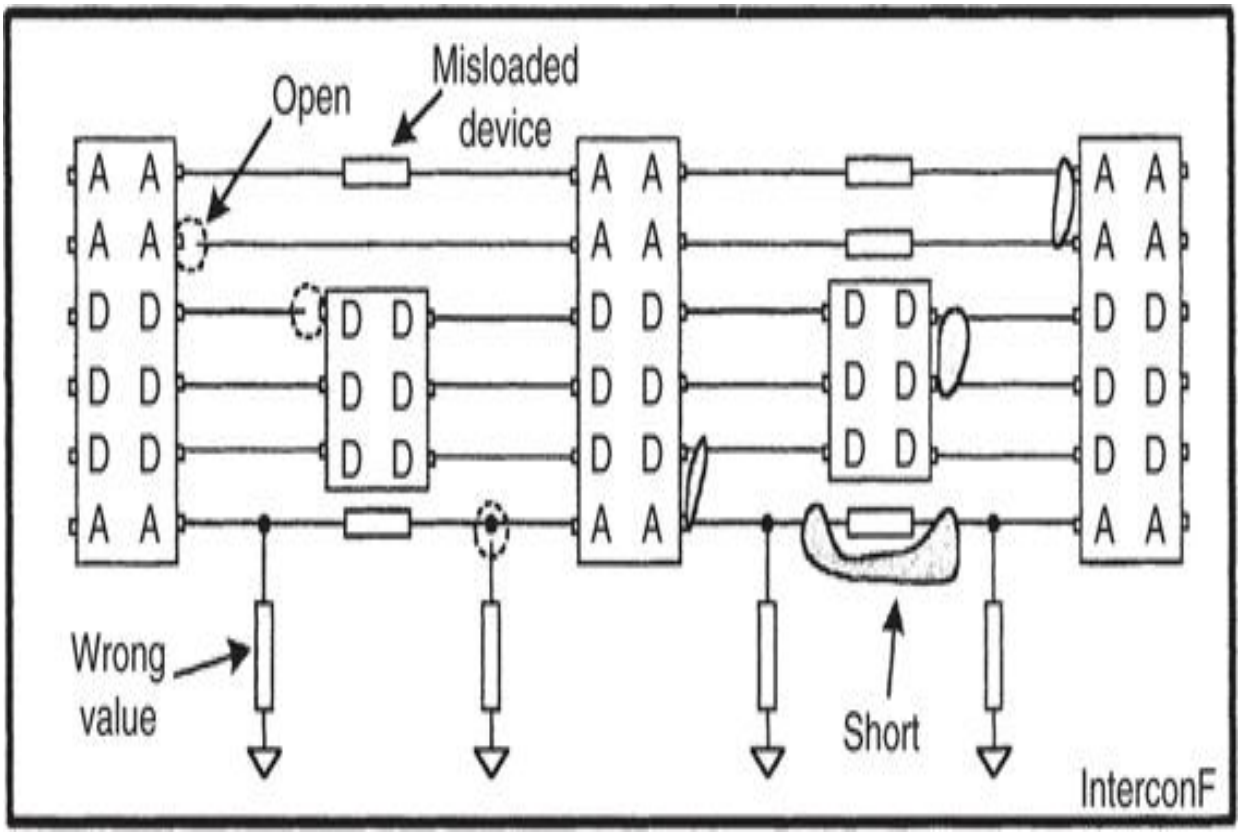

FIGURE 56.7 A mixed-signal circuit with some possible defects. IC pins marked A and D are analog and digital, respectively.

A mixed-signal device constructed with 1149.4 has the general architecture shown in Fig. 56.8. It is in many ways identical to an 1149.1 IC, but it has an additional analog test access port (ATAP) that is used to facilitate the control and observability of analog signals at device pins. The ATAP brings into the IC two additional analog signals that are used during testing.

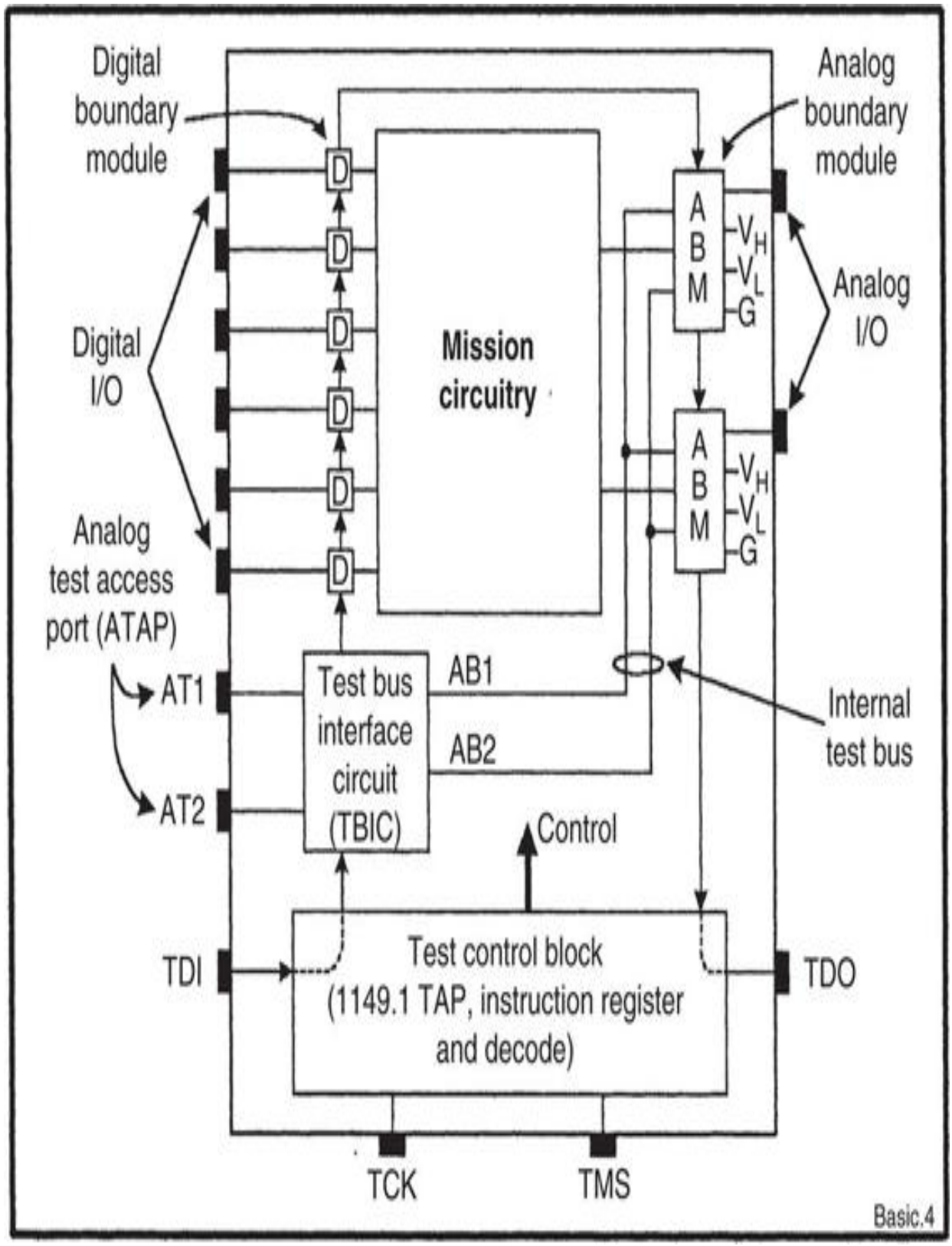

FIGURE 56.8 General architecture of an 1149.4-compliant IC.

With 1149.4, digital device pins are treated exactly as done with an 1149.1 boundary register. Analog pins have an augmented structure called an analog boundary module (ABM) as part of the boundary register. The ABM allows an analog pin to be tested for simple shorts and opens (this is called 1149.1 interconnect test emulation) as well as allowing the injection and/or observation of analog signals via the ATAP.

An ATE system can utilize the test resources in an 1149.4 IC as shown in Fig. 56.9. This requires the coordination of a digital test sequencer with analog test resources—in this case, a current source and voltmeter. Pathways from these resources and through the 1149.4 IC can be used to make measurements on discrete analog components on a board, even with no bed-of-nails access to the components.

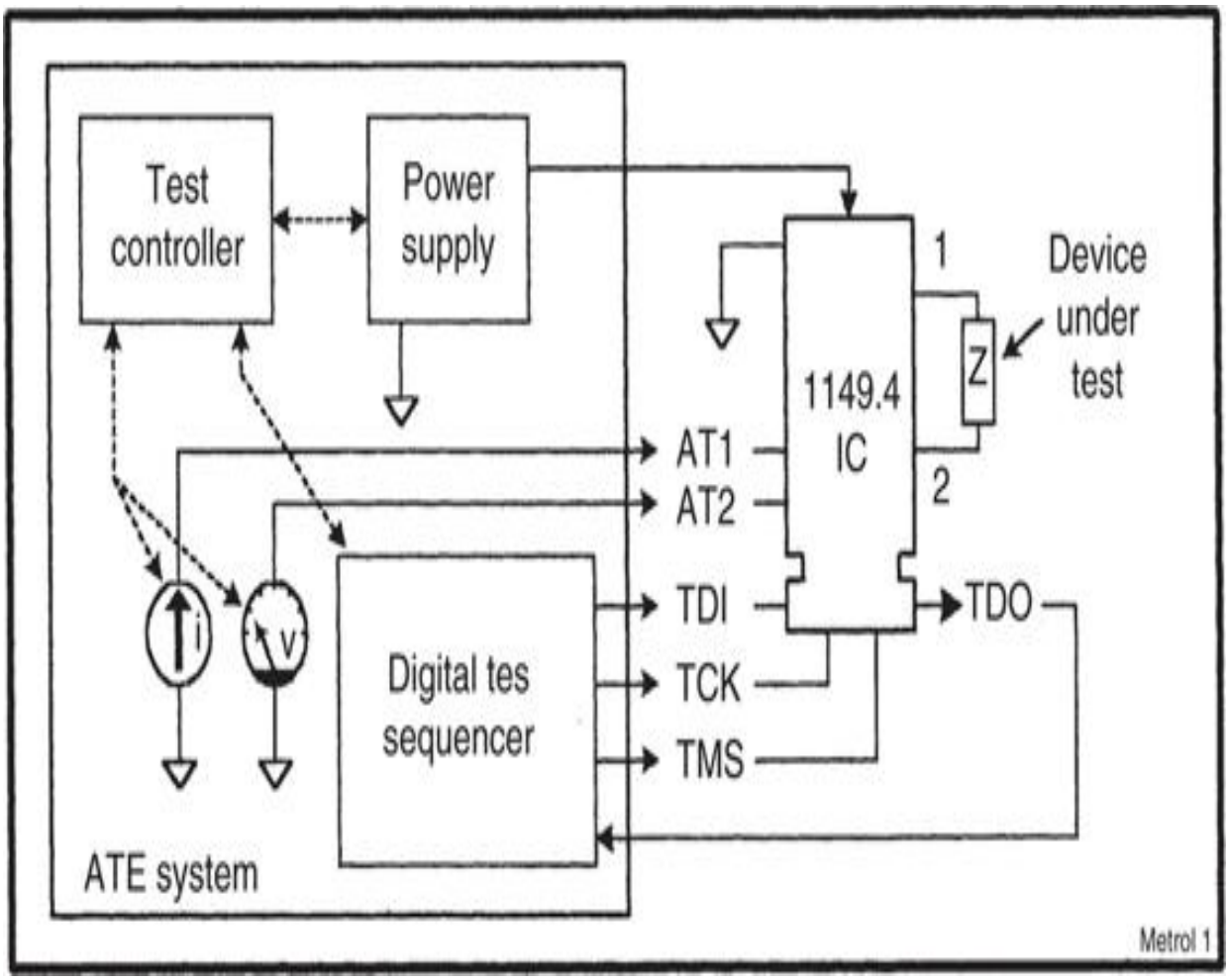

FIGURE 56.9 An ATE system can use 1149.4 resources to gain access to discrete analog components.

The pathways needed for a measurement are provided by silicon switches in the ABM. Because switches implemented this way have significant nonlinearity and nonnegligible impedances, these must be accounted for in the measurement processes. Figure 56.10 shows how an analog device can be tested with two measurements. First, the tester's current source is connected such that current can flow along AT1 into the IC. There it flows on the AB1 bus inside to the ABM connected to pin 1 of the IC. The current flows through Z and then into pin 2 of the IC. Pin 2's ABM directs the current to ground, completing the current path. In Fig. 56.10(*a*), the ATE system's voltmeter is connected via

the path AT2-AB2 to the ABM on pin 1, where it can observe the voltage at the top of Z. In Fig. 56.10(*b*), the voltmeter is switched to measure the voltage at pin 2, the bottom of Z. Subtracting the two voltage measurements gives the voltage drop across Z for a known current. Ohm's law gives us the value of Z, which we can check for the right value. This process works even with suboptimal silicon switches because we are using a current source to provide the known current and because the voltmeter pathway consumes a vanishingly small current and thus does not affect the accuracy of the measurement.

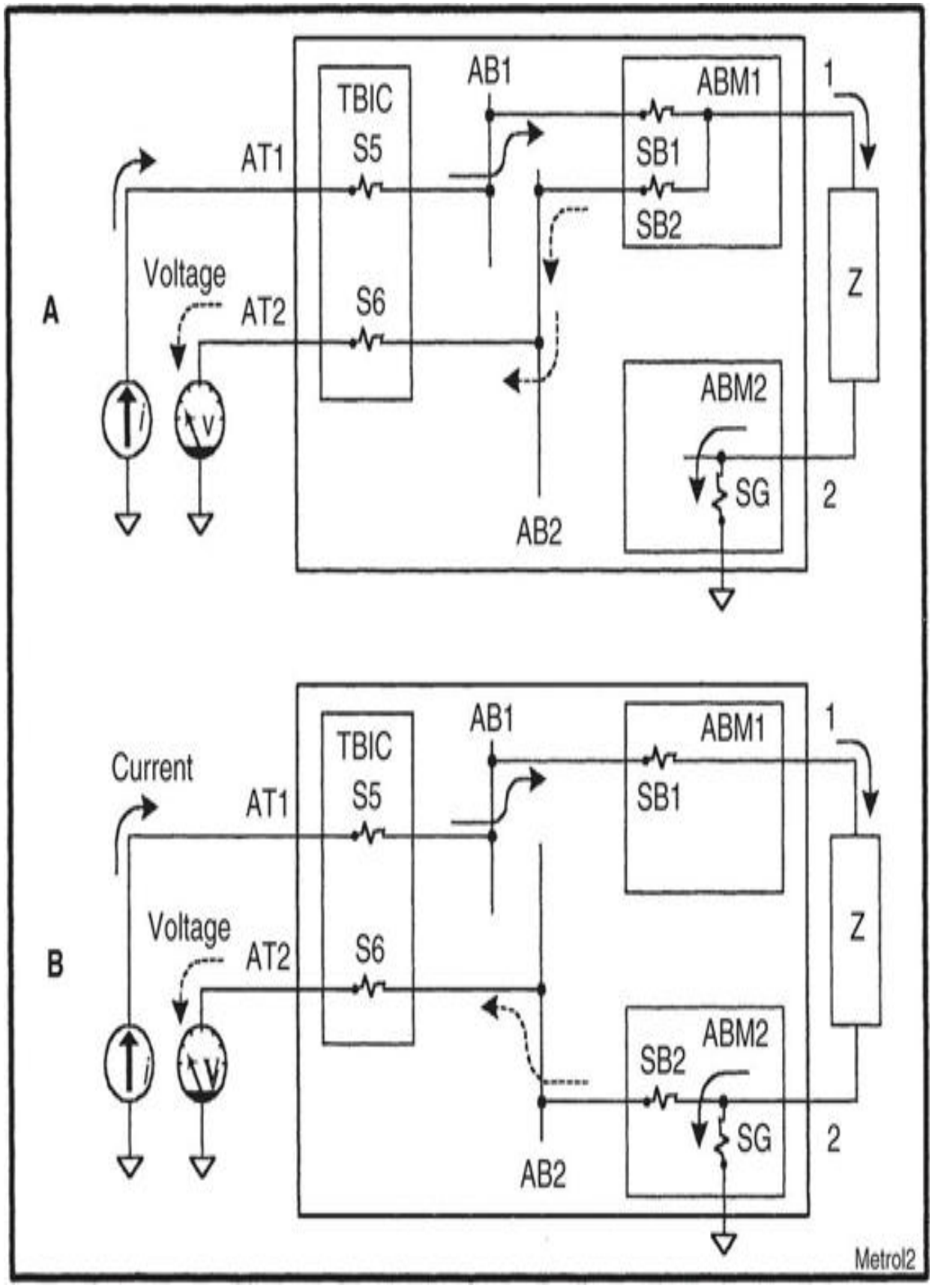
A
TBIC
S5
S6
AB1
AB2
ABM1
SB1
SB2
ABM2
SG
AT1
AT2
Voltage
Z
1
2
B
Current
Voltage
Metrol2

FIGURE 56.10 Two measurements (*a*) and (*b*) can be used to measure the voltage across Z for a known current.

In the future, with these and other standards, test engineers may be able to do complex tests on superdense circuitry with far less nodal access than they were afforded in the past. This will be an enabling technology because without it the electronics industry may find it uneconomical to produce superdense designs except in very high-end applications.

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[a] This survey does not cover the topic of standards-based testing (Sec. 56.5), because the testability standardization work promulgated by the IEEE began in the later 1980s.

[b] The addition is modulo-2 yielding a single bit. Any single-bit error delivered to the three inputs of the exclusive OR will cause the output to change from its expected state.

[c] This spare input pin should be held to a 0 value when the IC is performing its normal function. A pull-down resistor to ground could assure this, whereas during test, a tester signal could assert a 1 value when needed for testing.

[d] An IEEE standard has as a suffix the year of its creation or last update. A standard must be updated and/or reaffirmed every 5 years. Up to two supplements to a standard may be issued within the 5-year cycle. Users of a standard should keep up to date with it.

[e] Bidirectional signal pins can both observe and control the nodes to which they are connected.

[f] An optional fifth pin called Test Reset (TRST*) is an asynchronous active low reset for the 1149.1 circuitry. Because any TAP can be reset by five clock pulses to TCK while TMS is held high, TRST* is not actually needed for resetting an 1149.1 device. It is often included as a fail-safe measure with a board-level pull-down resistor providing a constant reset to the TAP. Many 1149.1-compliant ICs do not include the TRST* pin because the extra pin required may be too costly.

CHAPTER 57
LOADED BOARD TESTING

Kenneth P. Parker
Agilent Technologies, Loveland, Colorado

57.1 INTRODUCTION

Printed circuit boards, like everything else in the electronics industry, have been undergoing rapid technological evolution. This is only natural because everything, from the boards themselves, to the CAD systems that create them, to the components that populate them, to the assembly methodologies used to fabricate them, has been undergoing similar changes. These changes have common themes: greater functional density, better performance, improved reliability, and lower cost.

In the early 1990s, the move toward surface-mount technology (SMT) accelerated to the point that SMT designs became the rule. SMT supplanted, in large part, the familiar 100 mil centered through-hole package technology. The change came slowly, embraced by leading-edge applications that needed the density improvements that came with SMT. Many held back because they did not have a need for higher

densities and could not justify the risk of putting new processes in place to manufacture with SMT. The process of perfecting SMT brought to light a surprising fact—it was more efficient once the necessary automation was put in place and perfected. There are now applications that use SMT not because of the density improvements it affords, but rather because of the efficiency it provides. This is confirmed by the fact that many new devices can no longer be obtained in the old-style through-hole packages.

Along with SMT came increases in lead pitch density. First there was 50-mil pitch; soon came 25-mil pitch, then came 15-mil pitch, and so on. Other technologies such as tape automated bonding (TAB), chip-on-board (COB), multichip modules (MCM), and ball grid arrays (BGAs) are gaining acceptance. The industry has for some time been in the midst of a packaging revolution. This revolution has applied to boards as well. The average board, by virtue of high-density interconnect (HDI), now has more layers, finer lines and spaces, buried vias, devices mounted on both sides, and so forth. The net result is that loaded printed circuit boards are becoming incredibly densely packed with highly sophisticated components. We are in fact experiencing a density revolution. Figure 57.1 shows a range of common electronic devices superimposed on a penny to show scale.

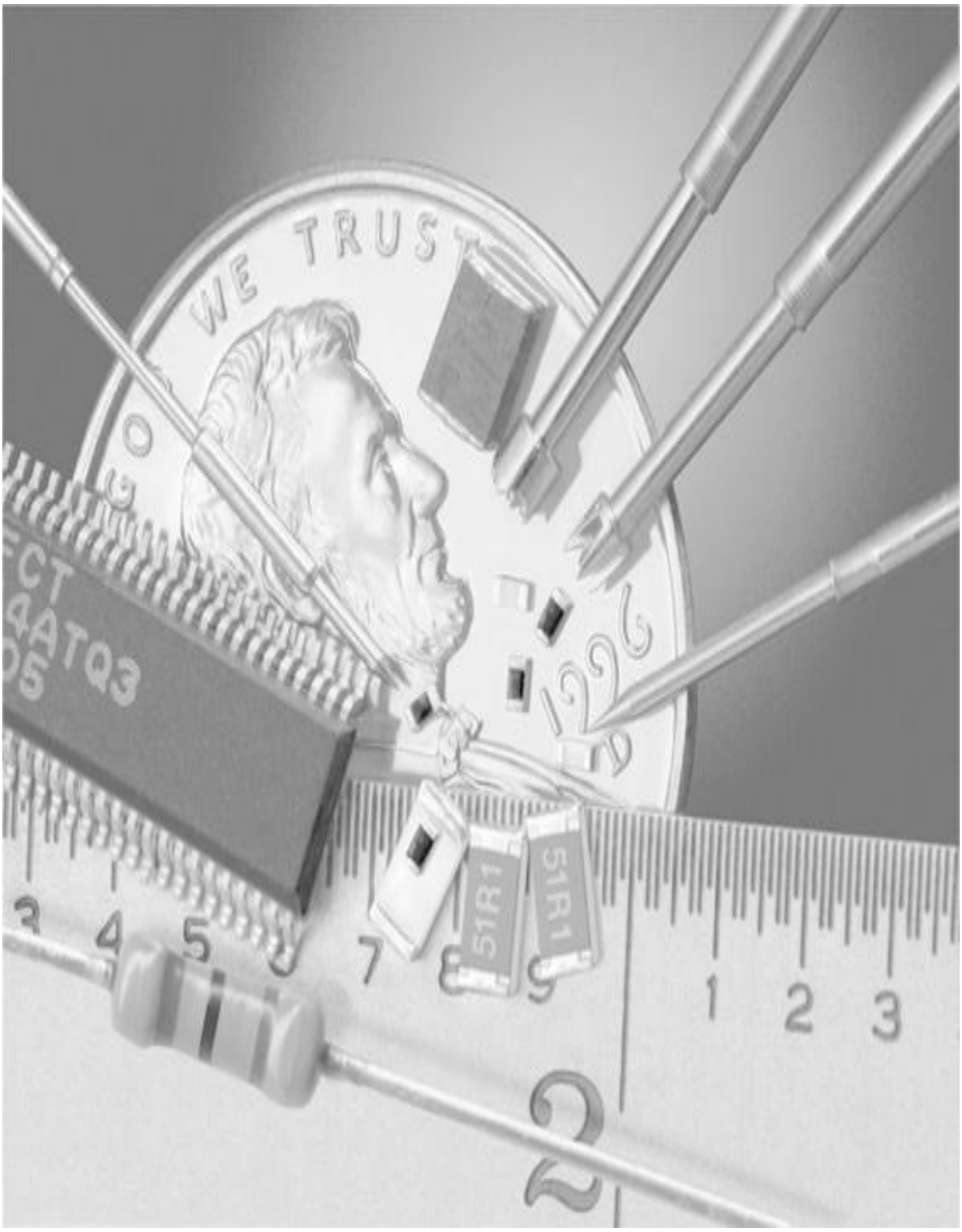


FIGURE 57.1 A US penny shows the size of some common PC board components, some older, some recent. The small black devices near Lincoln's bow tie are 04-02 (40 × 20 mils) surface-mount resistors. (Now 02-01 [20 × 10

mils] devices are being used.) Some 100-, 75-, and 50-mil test probes are shown for comparison. Note the lettering on the penny is done with 10-mil lines and the width of the circular part of the 9 is 35 mils, a common probe target size. *(Photograph courtesy of Agilent Technologies.)*

Testing has been impacted by all these changes. If perfect components were fed through perfect processes utilizing perfect machines run by perfect employees—testing would not be needed! Unfortunately, nearly perfect components are fed through processes that are subject to drift in many of the hundreds of variables that govern them, using machines that require careful calibration and preventive maintenance, operated by people who tire and err. For these reasons, testing is still an important part of loaded board manufacturing. However, as a result of the miniaturization brought on by the density revolution, our ability to gain the physical and electrical access needed for testing purposes is increasingly hampered. Because access to a circuit is crucial for testing, accessibility difficulties make testing steadily more difficult to accomplish. On top of this, the electronics industry is expected to provide continued improvements in cost, reliability, and quality. Testing plays a crucial role in these improvements, as will be seen.

57.2 THE PROCESS OF TEST

In the earliest years of the electronics industry—indeed, before anyone may have called it an industry—there was no concept of test. A product was put together and shipped, because inherent in the putting together was a basic appreciation for how the product was supposed to look and behave. This crafting quickly gave way to mass production[a] of somewhat more complicated items by workers who were not themselves experts in the craft. Of course, today, workers with little or no fathoming of what it is they are

producing turn out items of unbelievable complexity. If they had to know everything about the process, it would undoubtedly be too expensive to make the product.

It is also important to appreciate that boards are often themselves components of systems. Boards might have a respectable yield from a board test process of, say, 97 percent, which is to say, 3 of 100 still contain defects.[b] However, if 20 such boards are used in a system, the probability that the system will turn on is only 54 percent.[c] Because debugging a system is usually far costlier and more difficult than testing a board, there is much interest in higher post-test yields. This is why yields are being pushed into the 99 percent and higher levels.[d]

Test has gone through three stages of evolution during this time. It has been used as a sorting process, then as a repair driver, and finally as a process monitor.

57.2.1 Test as a Sorting Process

Test can be used to sort boards into two piles, good and bad. Essentially, such testing provides only one bit of information about a board. This one bit of information provides little clue as to what the problem is or how to repair it. If all we intend to do with a bad board is discard it, then one bit of information may be enough. In some applications, for example making $2 digital watches by the million, it may be economically impossible to attempt to repair bad units. However, as will be seen soon, discarding bad boards may also lead to discarding of valuable information about the health of our manufacturing process.

57.2.2 Test as a Repair Driver

It is very often economically justifiable to repair a bad board, if it can be done quickly and with little skilled analysis needed. This is where modern test systems begin to come into their own. More bits of information are needed per bad board; a diagnostic test is needed that accurately resolves failures into defect reports that can be acted upon to effect repairs. Because a freshly repaired board will need retesting to ensure it is now defect free, one also would like to find as many defects as feasible in each pass across a tester to avoid a glut of work in progress.

57.2.3 Test as a Process Monitor

When repairing boards, valuable information about the health of our board manufacturing process is at our fingertips. Indeed, the repair process may have the ultimate defect resolution because faults detected by a tester may still not be perfectly correlated with defects (see Sec. 57.3). If one views test as a process monitor, one can gain valuable insight into what is happening upstream in many of the subprocesses that come together to produce boards. For example, one may see solder opens as a chronic problem. Further examination may show that they are happening in one area of a board more than in any other. That may lead to the examination of the solder application process, which shows that a solder screen squeegee has an uneven amount of solder paste on it. The root cause of this uneven distribution of paste can then be sought and corrected.

It is quite important for the tester to do a good job of resolving faults into defects. Using an example of solder opens on digital devices, digital in-circuit test (detailed in Sec. 57.5.2) alone may indict devices as failing when it is really more of an open solder problem. The repair technician may notice this. However, it may well be overlooked because replacing the device “fixes” the problem. This pollutes the

information about our process, causing one to call the IC vendor with complaints when one should be examining the solder process. If tests are focused more closely on defects than on faults, then one may be able to better trust tester-derived process information. This requires test engineers to be students of their manufacturing process and available test technologies so that test techniques are kept in balance with the defects that are most important.

57.3 DEFINITIONS

Testing is a word often used in a vacuum. What are tests actually looking for? The answer to this question has a huge impact on how to go about testing effectively. It makes little sense to test meticulously for problems with low likelihood of occurring, just as it makes little sense to inadequately test for likely problems. However, many of the terms used in the testing industry are overloaded such that surprisingly little agreement on their definitions may be found. Worse, this confusion is often not realized, which complicates communications between process people, test people, and equipment vendors.

57.3.1 Defects, Faults, and Tests

57.3.1.1 Defects. A *defect* is an unacceptable deviation from a norm. As an example, a bond wire could be missing in an IC. This defect may in turn be due to a problem (the “root cause”) in a wire-bonding machine, such as it misfeeding wire. Other deviations may not be considered defects, but rather acceptable variations. For example, the plastic used to encapsulate a component may have significant variations in color that are still considered acceptable.

Defects require remedial action of some sort. Most often, defects lead to a repair operation that removes the defect and restores the product to acceptable status. In some cases, a defect may not be economically repairable and thus causes scrap. It is also possible that a defect will be overlooked and thus be delivered within a product to an end customer. In some cases, such as the manufacture of $2 wristwatches, some amount of defective product may be deemed acceptable. However, for many products, defects perceived by end customers can have grave economic consequences and are strenuously avoided.

57.3.1.2 Faults. A *fault* is a physical manifestation of a defect. (The word *fault* is often used synonymously with *failure*.) Thus a fault reveals the presence of a defect. A single defect may cause several faults (i.e., have several different manifestations), and a single fault could be the manifestation of several different defects.

A defect shows up as a fault. For example, the aforementioned missing bond wire on an input to a logic gate may cause it to see a permanent logic 1 rather than a time-varying signal. Several other defects can produce this same fault behavior. For example, missing solder between the input pin and the board, an electrostatically damaged input buffer within the IC, or a broken printed circuit trace between the upstream driver and the input will all exhibit the same faulty behavior. Similarly, one defect may cause several fault manifestations. For example, an open solder joint on an input pin (particularly a reset input) may cause an IC to show incorrect results, and these incorrect results vary in time.

An observed fault is not always a reliable pointer to a defect. For example, if an IC loaded onto a board has defective solder on one input pin causing an open circuit, this may appear to the IC to be a permanent, stuck-at-1 fault on that input. This faulty behavior may not be readily

apparent because the effect of the erroneous logic 1 must propagate through the internal workings of the IC before its effects (improper output behavior) are seen.[e] When this faulty output behavior is finally observed, it can be a highly challenging task to relate this observed behavior to the input stuck-at fault caused by the defective solder. This is illustrated in Fig. 57.2.

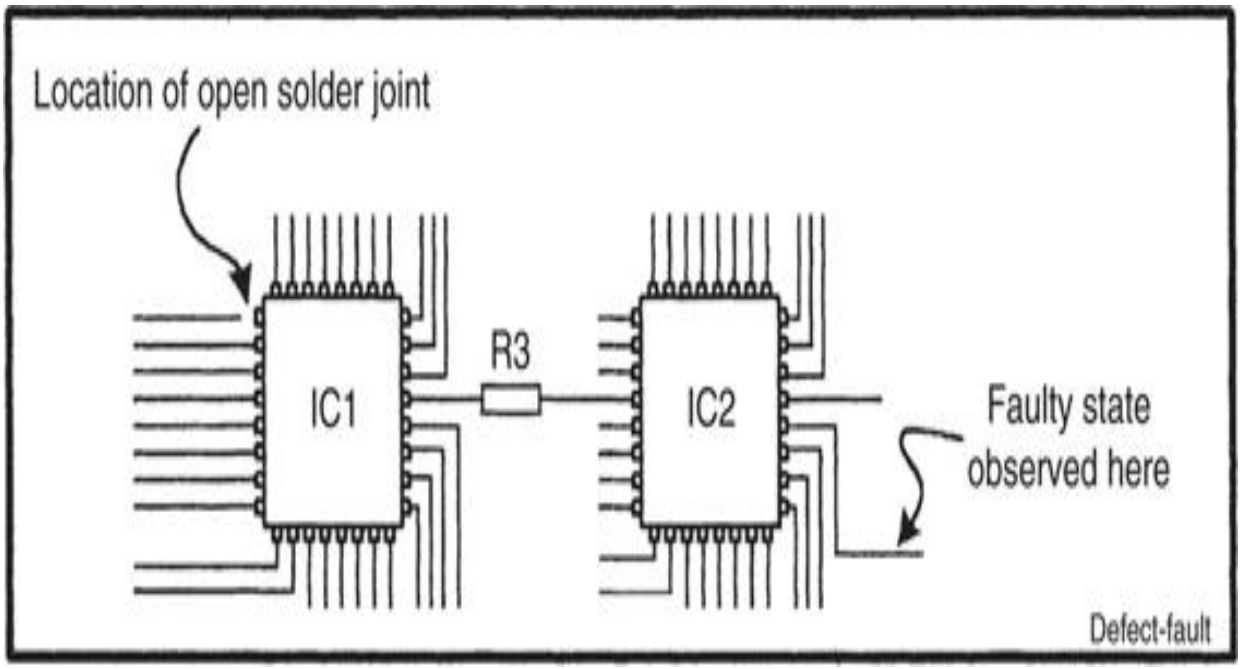


FIGURE 57.2 A defective solder joint on an input pin to IC1 causes a fault on an output of IC2. Note that IC1, R3, and IC2 are suspect, as well as six solder joints, two IC input buffers, two IC output buffers, and four IC bond wires.

57.3.1.3 Fault Syndromes. A *fault syndrome* is a collection of measured deviations from an expected good outcome. For example, a digital device may produce an incorrect response on several of its outputs when its inputs are stimulated in a certain sequence. The incorrect pins, their states at the point where they were incorrect, and the point in time where each failure was noted form a fault syndrome.

57.3.1.4 Fault Detection. A fault is *detected* when an operation with an expected outcome is conducted and this outcome is not observed. For example, when you turn on the power to a personal computer, you expect to see it boot up. If it doesn't, then you have detected a failure of some kind. There could be a plethora of reasons for this result, but you have little information to act upon. In other words, the underlying defect may not be easily resolvable.

57.3.1.5 Fault Isolation. A fault is *isolated* when an operation with an expected good outcome and one or more failing syndromes is conducted and the outcome belongs to the set of failing syndromes. For example, as your personal computer boots up, it may do a series of self-test operations. If any of these fail, a diagnostic message may appear on the screen that specifically identifies a failure. Again, the underlying defect may not be easily resolvable, but there is more information to act upon than you had when the fault was simply detected.

57.3.1.6 Tests. A *test* is one or more experiments that are specifically constructed to detect (and possibly isolate) failures. A *detection test* has an expected good outcome. An *isolation test* has an enumeration of possible fault syndromes indexed to specific failures. Thus, when a test fails, it provides us with information: a single bit of detection information, or a fault syndrome that may match an enumerated outcome, pointing to a fault.

A well-constructed detection test will detect a large number of potential failures. A well-constructed isolation test will accurately resolve a failure from a large list of potential failures. Note that an isolation test may encounter a failure that it was not constructed to isolate. If it fails (that is, if it detects the fault), it may not produce a syndrome that matches one from its list, or it may produce a match that is

erroneous. In either case, it has been reduced to a detection test.

Remember that an isolation test may point to a fault, but the fault may not be a good indicator of the actual defect that is present. For this reason, it is important to construct tests that target expected faults and that accurately resolve underlying defects. When defects are resolved correctly, it is then much easier to find and correct the causal problems.

There are, in general, three categories of faults being tested: performance faults, manufacturing defects, and specification failures.

57.3.2 Performance Faults

A *performance fault* is a fault in the performance of a system that occurs due to a mismatch of important parameters among the system's components. This mismatch is the defect. As a common example, the path delay seen by a digital signal as it passes through several components may exceed the intended design value, causing a malfunction. No single component in the path is defective, but the cumulative contributions of several components cause the performance fault. The repair for this defect is to replace one or more components in the path with new components specifically selected to give the proper delay.

There are several problems with testing for performance faults. First, the test developer must know about the circuit design in great detail. Second, it is difficult to set up a test that can resolve faults into specific defects (for example, the mismatch of parameters in several components). Third, it is difficult to avoid being confused by unanticipated defects that produce behaviors similar to the defects of interest.

Solving these problems implies great knowledge and understanding of a board design. Indeed, in some instances in a carefully designed board, the designer may have specific

knowledge of some critical parameter that has to be precisely managed and can alert those responsible for test. However, much of the testing for performance faults carried out in the past was not done with this knowledge, but rather because of a lack of this knowledge. In the past, tools that could help control the key parameters of a design were unavailable, or designers were using components that were incompletely specified, or perhaps they were too trusting of their “seat-of-the-pants” instincts. It was expected that performance testing would give adequate coverage of any problems that might occur. In effect, performance testing was used to validate a design after the fact.

The expectation that performance testing will somehow protect products from the effects of poor design is now obsolete. It amounts to wildly shooting in the dark against a well-hidden, stealthy enemy force of unknown size and distribution. Given the ever increasing complexities of boards, it is simply not reasonable to expect that test engineers could stumble at random across effective tests for all possible design problems, and certainly not within the lifetime of the design. With the increase in effectiveness of design tools, designers should no longer be relying on test for design validation. Testing for performance faults will still be important, but it must be used in its proper role—to verify that critical parameters identified in the design process are properly controlled.

57.3.3 Manufacturing Defects

A *manufacturing defect* is a defect resulting from a problem in the manufacturing process. Manufacturing defects tend to be fairly gross in nature. Table 57.1 gives a list of potential manufacturing defects.

TABLE 57.1 Examples of Manufacturing Defects Seen at the Board Level, Sources of the Problems and Causes

Defect	Source(s)	Cause(s)
Shorts between solder pins	Wave/reflow soldering	Too much solder, solder screen defect, pin misregistration, bent pins
Solder open	Solder application, wave/reflow soldering	Too little solder, solder screen defects, tombstoning, bent pins
Missing component	Placement, soldering	Shock, abrasion, too little glue
Wrong component	Placement setup, inventory, handling	Handling error, mismarked packages, operator error, wrong specifications
Misoriented component	Placement setup	Handling error, operator error
Dead component	Placement, soldering	Dead on arrival, handling damage, electrostatic damage

Manufacturing defects are the result of the havoc inherent in manufacturing processes. These defects result in faults that may be very easy to detect and to correlate with their root cause(s), but this is a function of the test approach. Some manufacturing defects can still be difficult to detect and resolve, as the example given of a solder open on a device input pin shows (Fig. 57.2).

57.3.4 Specification Failures

Specification failures are similar to performance faults. Performance specifications are checked against requirements for the full range of operating conditions expected, such as temperature, humidity, vibration, electronic noise, etc. Specification test is often a regulatory or contractual requirement. One may argue that these

specifications are largely unnecessary because, if a circuit design is robust, makes use quality components, is accurately assembled, and is thoroughly tested for manufacturing defects, one does not have to make it perform all of its functions to know that it works. This is the “proof by construction” argument, used by successful manufacturers of kitchen matches and bomb detonators. Full specification test may also be impossible in practical terms because there may be too many combinations of circuit functions versus operating ranges. If only a subset of combinations is to be checked, this begs the question of which subset.

If specification test is required nonetheless, such testing is usually carried out with custom-tailored test equipment that can simulate the range of operational environments of interest. Such testing may be quite time consuming, and the cost of the supporting test equipment may range from trivial to hyperexpensive. At one extreme, a manufacturer of I/O cards for personal computers may simply plug each one into a computer and see if it performs a simple loopback test. At the other extreme, a manufacturer of guidance computers for missiles may require a missile shot on a test range, full telemetry, and support from the Air Force and Navy. The bottom line is that you should seriously question the motivations for and expectations of testing for specification faults.

57.4 TESTING APPROACHES

We have seen a spectrum of faults, performance faults, manufacturing defects, and specification faults. Each has evolved a test technology.

57.4.1 Testing Boards for Performance Faults

Performance testers are often known as edge connector functional testers. They connect to the edge connectors of the board under test with mating connectors that are then adapted to the tester resources by a customized fixture called an adapter. In most cases, no other connections are made by the test fixturing to any internal nodes of the circuit. In essence, the board is tested in an environment that resembles its application environment to some degree.

Some performance testers have guided probe capability.[1,2] A guided probe is a manually positioned test probe with a measurement (and sometimes stimulus) capability and supporting software. It is used to temporarily gain access to internal nodes of a circuit, one at a time, where observations of internal circuit behavior during a test can be made and processed by software to provide enhanced fault resolution.

How does this software know what the nodes of a circuit are supposed to be doing during a test? One could enter all these data by hand if one knew the design of a circuit well, but this is impossible for any circuit that consists of more than a handful of gates. The most popular way to get these data is by logic simulation of the circuit.[f,2] Good circuit simulation is often used by designers to prove the circuit behaves the way they expect it to under various input conditions (input vectors) they are interested in. Fault simulation is used to study how a circuit behaves when that circuit is perturbed by a modeled fault. An example of a modeled fault is a stuck-at-0 on a gate output, meaning no matter what the gate's inputs are, the output is 0. The single stuck-at model is the most prevalent fault model in existence. It assumes that only one stuck-at (either 0 or 1) may exist in a circuit at any one time. A fault simulator can be used to predict, for a given modeled fault, how the circuit

will behave when stimulated with input (test) vectors. If the modeled fault causes one or more observation points (like circuit output pins) to deviate from normal behavior, we can declare the fault detected by that vector. In the common case of sequential circuits, it is more accurate to say all vectors detected the fault up to and including the one that caused the observable deviation.

Another technology used by some performance testers is the fault dictionary.[2] Fault dictionaries are prepared with fault simulators. A fault dictionary is a three-dimensional data structure of Boolean true/false bits (see Fig. 57.3). The first dimension is an enumeration of all test vectors. The second dimension is a list of modeled faults that are to be simulated. The third dimension is an enumeration of the circuit's output pins. A given bit in the fault dictionary is true if the corresponding output pin fails on the corresponding vector for a given fault.

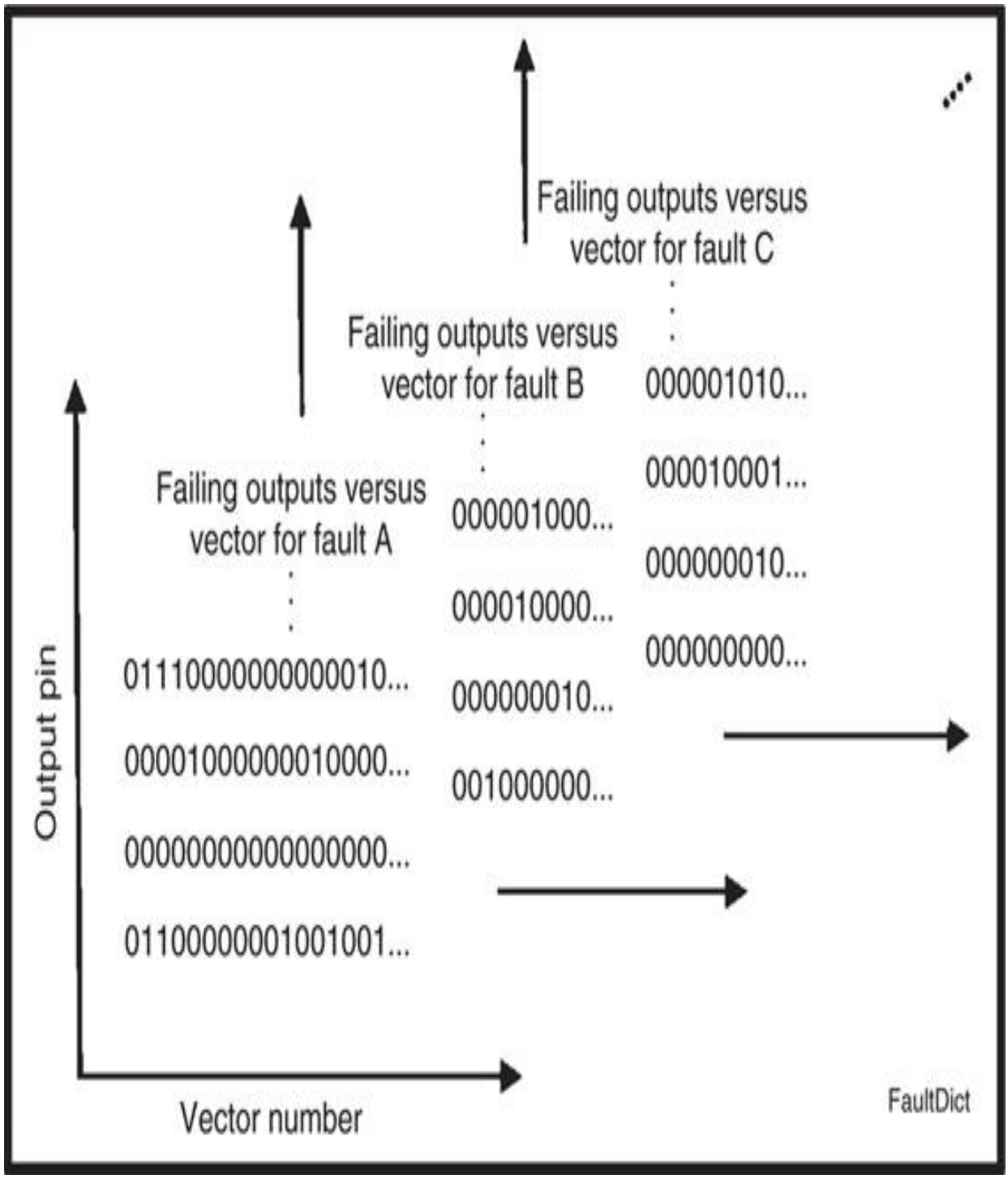


FIGURE 57.3 A fault dictionary. For each “page” corresponding to a modeled fault, bits set to 1 indicate that a given output pin fails for a given vector number. When testing is performed, the failing output(s) and failing vector number are noted and then each page is searched at those coordinates to look up a matching fault. (Note that more than one fault may produce a match.)

For a given vector and fault, the output pins that are expected to fail can be looked up in this dictionary. In a testing scenario, we take a failing test vector and list of failed output pins, and attempt to look up a fault (or faults) that match the failed pin behavior for that vector. Fault dictionaries work well when actual defects that cause a circuit to fail closely match the fault model. When defects occur that vary from the modeled faults, then a dictionary lookup may come up empty (no matching fault), or matches may be found but point to the wrong faults, or so many matches may be found that it is impractical to examine them all to see which (if any) are the actual problem. Dictionary generation is computationally intensive, dictionaries may consume huge amounts of storage space,[g] and dictionary lookups may not work. This technology was invented along with small-scale integrated bipolar technologies such as early TTL or ECL. The advent of large-scale integration and CMOS technology[h] has made fault dictionary technology nearly useless in board testing practice.

Performance testers are intended to emulate the environment the board would encounter in its native application. This means the tester itself needs to be carefully customized to supply this environment, or it must be a general-purpose tester with a great degree of flexibility. Flexibility brings cost, so commercial functional testers tend to be among the most expensive. Programming such machines is a complex task, due both to the flexibility of the tester and to the nature of the test requirements. It is difficult at best to get automated support for functional test programming. Typically, such programming takes extreme patience and a high level of skill—again, two more costs. To compound this, any last-minute design changes to the board may cause expensive and time-consuming test modifications or invalidate the tests altogether.

57.4.2 Testing Boards for Manufacturing Defects

Manufacturing defects can be detected by a functional test, but because functional testers are expensive and difficult to program, other techniques have arisen to test for them. These testers have one or more of the following advantages:

1. They are much easier to program, often requiring less than 10 percent of the time of functional test development.
2. Automatic test program generators that analyze the circuit design database do most of the work and relieve the skill required of the programmer.
3. Their programs are much less sensitive to design changes because they take a divide-and-conquer approach; the effects of design changes are localized, requiring that only a portion of the test be reprogrammed.
4. They offer much better defect resolution for many defects because localized portions of the circuit are being analyzed, reducing diagnostic complexity.

The principal technology is the in-circuit tester. This tester utilizes a high degree of nodal access—that is, connection to printed circuit traces—to perform its work. Nodal access is provided by a unique fixture called the bed of nails. (See Fig. 57.4.) This fixture is made up of a platen that supports the board under test. The platen is drilled with holes below each target point for nodal access. In the holes are spring-loaded “nails” that contact the target points on the board. (Special clamshell fixtures allow nail access to both sides of a board.) The platen with board forms the movable top layer of a vacuum chamber. When vacuum is actuated, the platen with board moves down, depressing the nail springs and causing nail contact with board nodes. (Sometimes mechanical

actuation is used in place of or to assist vacuum.) The nails are wired (typically with wire-wrap technology) to the stimulus/measurement resources of the tester. These resources contain mechanical relays that allow connection of various tester functions to a given nail.

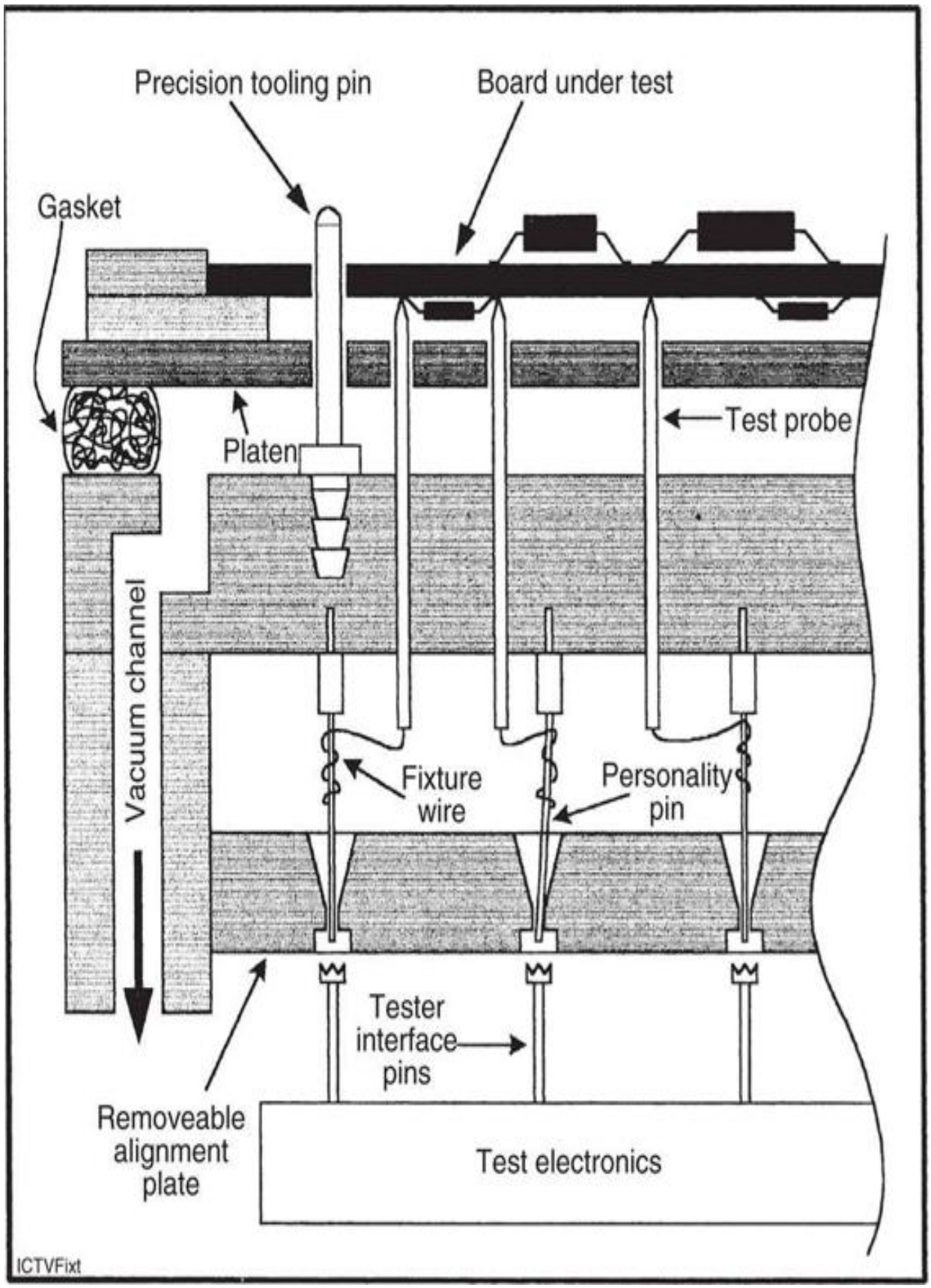

Precision tooling pin
Board under test
Gasket
Platen
Test probe
Vacuum channel
Fixture wire
Personality pin
Tester interface pins
Removeable alignment plate
Test electronics
ICTVFixt

FIGURE 57.4 Cutaway drawing of a board resting on top of an in-circuit vacuum-actuated fixture, the bed of nails. The interface pins (the mechanical interface to the ATE pin electronics) are placed very close to reduce path lengths.

Once a tester has access to the nodes of a board, it can perform in-circuit (also called in situ) tests. The idea is to test components as if they are standing alone, while they in fact are part of a board circuit. The actual electrical processes used in in-circuit testing are explained in Sec. 57.5.

57.4.3 Testing Boards for Specification Faults

There is not much to add here because often, testing for specification defects is very similar to testing for performance faults. However, if for (say) contractual reasons, you are required to show your boards working as specified, you may be required to construct “live” situations where they are performing in a realistic system setting. Again, the extreme case of a missile shot on a test range could be involved. The question must be, is there an easier way?

57.5 IN-CIRCUIT TEST TECHNIQUES

The problem of in-circuit testing can be subdivided into two main categories, analog in-circuit testing and digital in-circuit testing.

57.5.1 Analog In-Circuit Test

Analog in-circuit test addresses testing for shorts in the printed wire circuitry; analog components, passive devices such as resistors, inductors, and capacitors; and simple

semiconductor components such as diodes and transistors.[i] Analog in-circuit testing is conducted without applying power to a board; that is, it is an unpowered test methodology.

Shorts (unwanted connections between nodes) are tested for first because subsequent testing will profit from the assumption that shorts are not a factor, and subsequent testing may need to apply power to the board. Unpowered shorts testing may be accomplished by applying a small DC voltage [j] to a node while all others are connected to ground. If current flow is observed that is below a computed threshold, then the node cannot be shorted to any of the grounded nodes. If the current flow is above the programmed threshold, there may be an unexpected path to at least one of the grounded nodes. The destination node(s) can be determined by linearly searching the grounded nodes for the current flow (this is slow) or by using half-splitting techniques (which are fast[k]) to determine the other node(s) the current is flowing to. When the algorithm has finished stimulating all nodes sequentially, it can declare which nodes are shorted and use *x*-*y* position data to show where to look for the problems. Typically, shorts are repaired before continuing with other tests because they may confuse the resolution of defects and may cause physical damage when the power is later turned on.

Unpowered tests on analog components such as resistors, capacitors, inductors, etc., are performed next. Again, low stimulus voltages keep semiconductor junctions turned off. AC voltages are applied and phase-shifted currents are measured in order to deduce the values of reactive components (capacitors, inductors). For a simple measurement of a lone[l] impedance *R*, apply a voltage to one terminal of the component (through the bed of nails) and connect a current-measuring device (conceptually, an ammeter with zero impedance to ground) to the other component terminal. The current flow observed due to the

known stimulus voltage is related to R by Ohm's law ($R = V * I$). See Fig. 57.5(*b*).

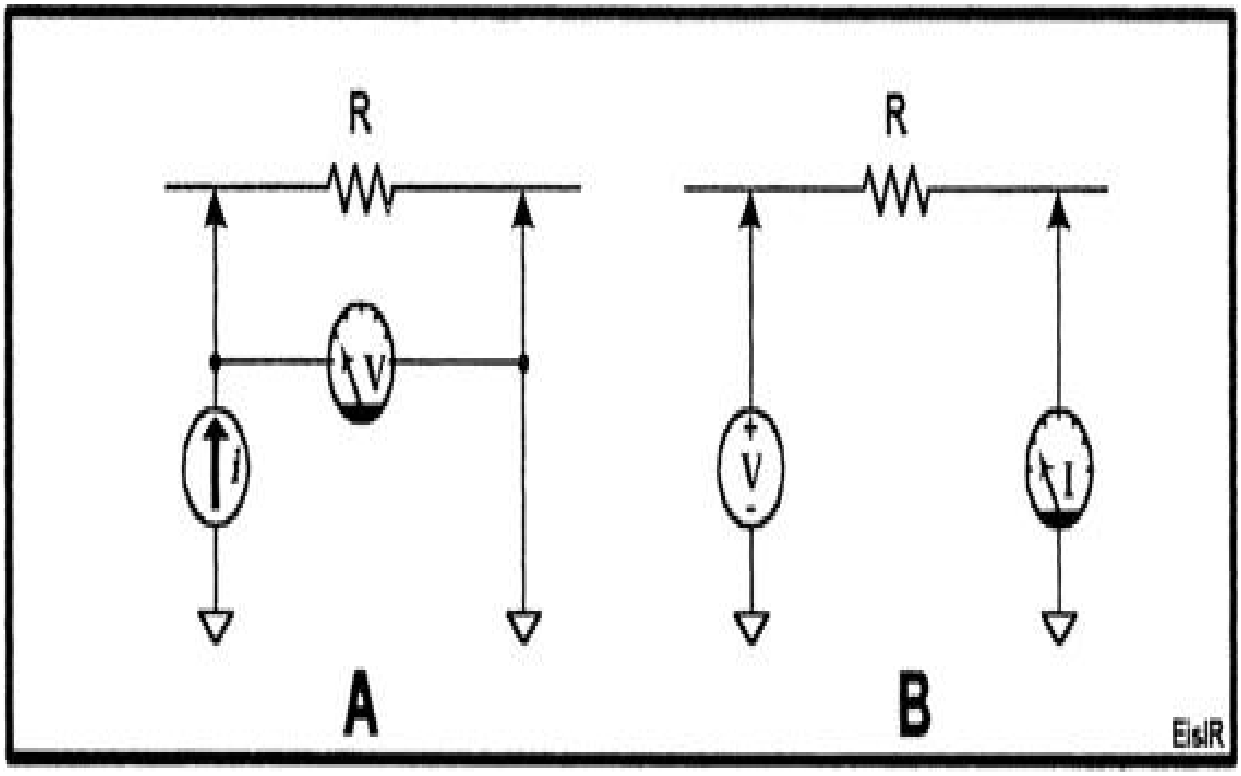


FIGURE 57.5 An analog component on a loaded board can be accessed by two in-circuit probes that connect its terminals with tester resources. There are two approaches: force a known current and measure a voltage (*a*) and force a known voltage and measure a current (*b*).

However, some discrete analog components may be connected to one another in ways that prevent simple measurement of the current flowing through the component due to parallel pathways that sidetrack some of the current. In Fig. 57.6, when applying a voltage to one terminal of R, a current also flows in a parallel path through R_a and R_b. The ammeter does not measure the true current through R because current from the parallel path also gets to the ammeter.

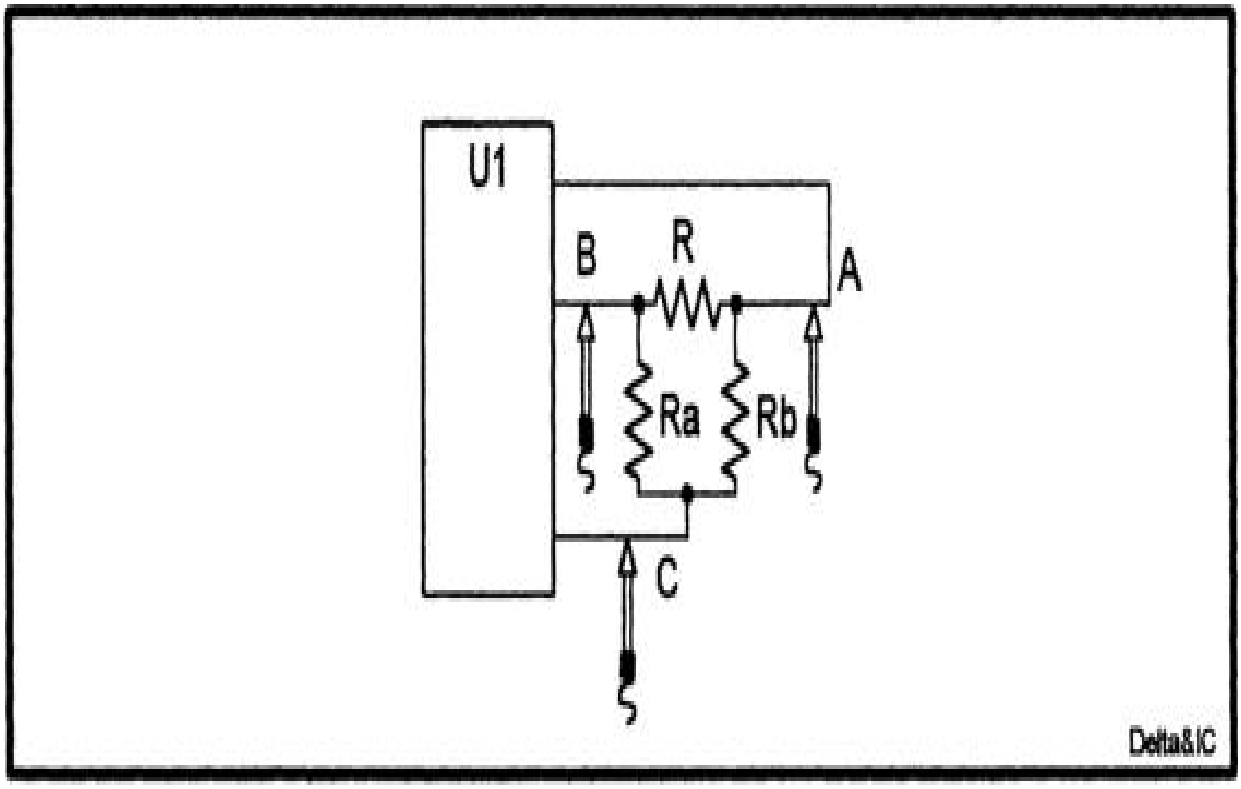


FIGURE 57.6 Three analog devices interconnected with an integrated circuit (U1).

The parallel path problem can be solved with a process called guarding. Guarding is accomplished by using a third nail to connect ground to the node marked *C* as shown in Fig. 57.7. When *C* is grounded, all the sidetracked current goes to ground because there is no voltage drop across R_b to attract current to or from the ammeter. All the current seen by the ammeter comes through *R*, so again Ohm's law gives the value of *R*. This is a classic three-wire measurement. It turns out that, for general component topologies, multiple guards (ground connections) may be required, but these are still considered three-wire measurements. In some cases where enhanced accuracies are needed or where there are extreme ratios of component values in a network, additional sense wires are used to eliminate errors that are due to small voltage drops in fixture nail, wire, relay, and trace

contributions. (See Fig. 57.8.) See Ref. 3 for a discussion of enhanced measurement accuracies.

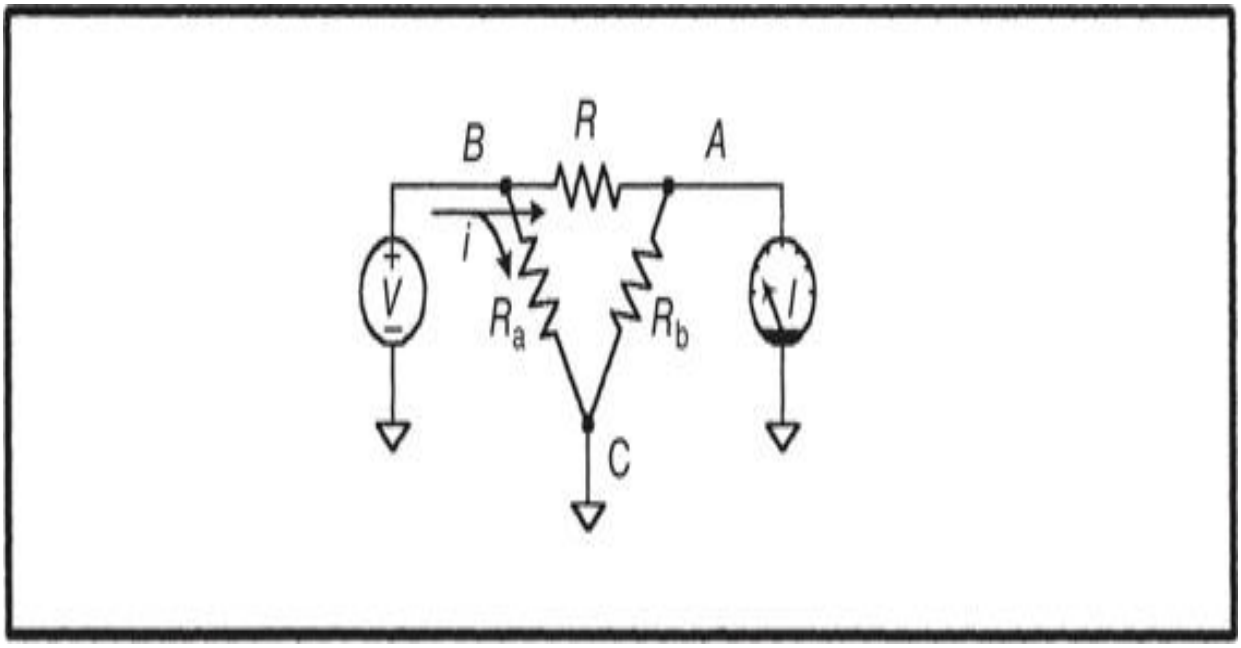


FIGURE 57.7 Equivalent circuit for Fig. 57.6 when making a guarded measurement.

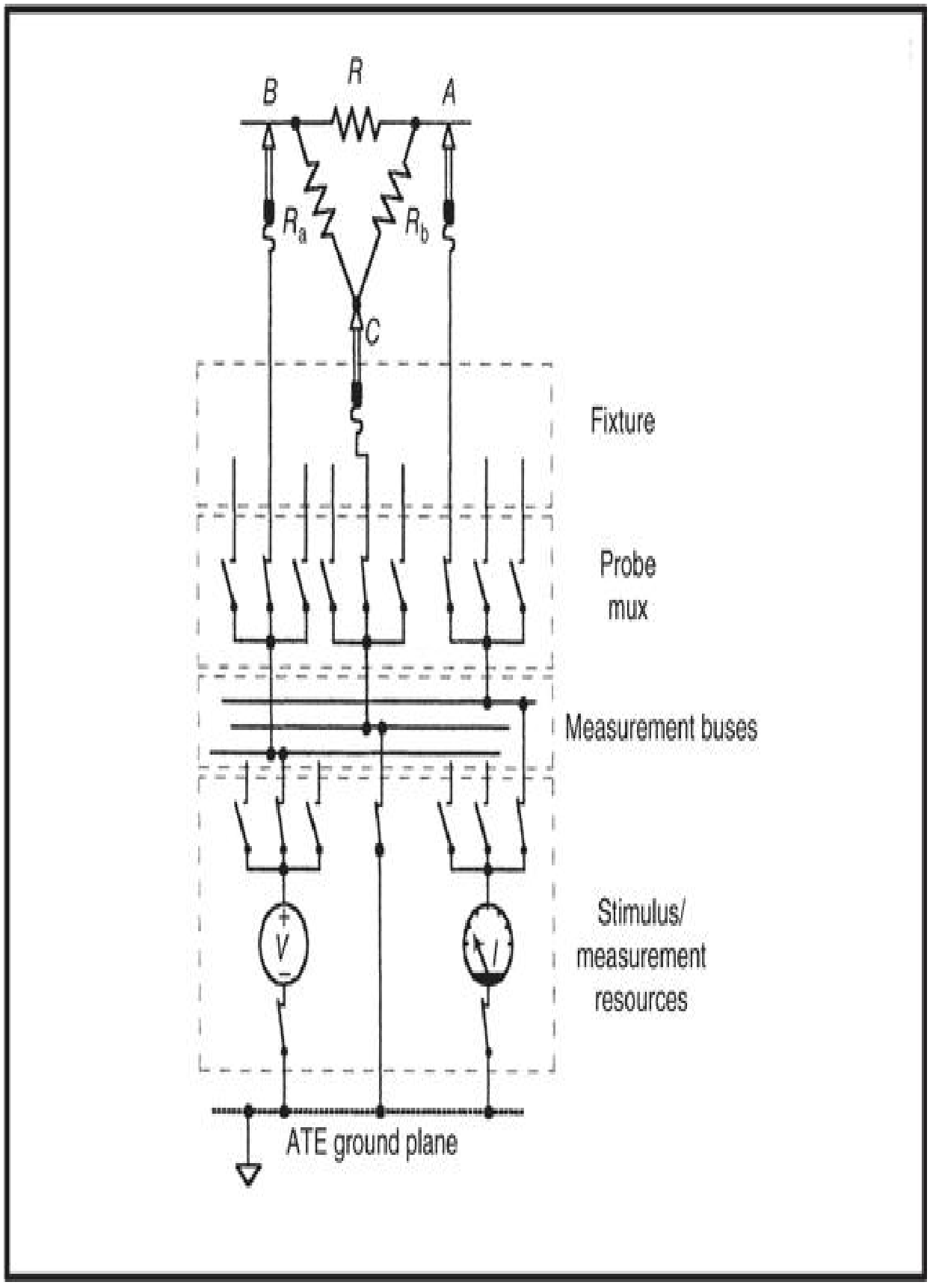

B
R
A
R_a
R_b
C
Fixture
Probe
mux
Measurement buses
Stimulus/
measurement
resources
V
I
ATE ground plane

FIGURE 57.8 Routing of tester resources to the circuit to be tested.

57.5.2 Digital In-Circuit Test

Digital in-circuit test focuses on the digital components residing on a board, and requires that power be applied to activate the digital logic contained within the ICs. Just as analog components can be tested without removing them from a board, digital components can be tested the same way. The key technology is backdriving. When applying digital stimuli to a digital device's inputs (via the bed of nails), a tester's driver must overcome the voltage levels that connected upstream devices are producing. This is done by equipping the digital in-circuit tester with powerful, low-impedance drivers that can backdrive upstream drivers with enough current to create the desired signal voltage in spite of their state. With tester receivers connected by nails to the device's outputs, the tester can monitor these outputs for expected responses to the stimuli. (See Fig. 57.9.)

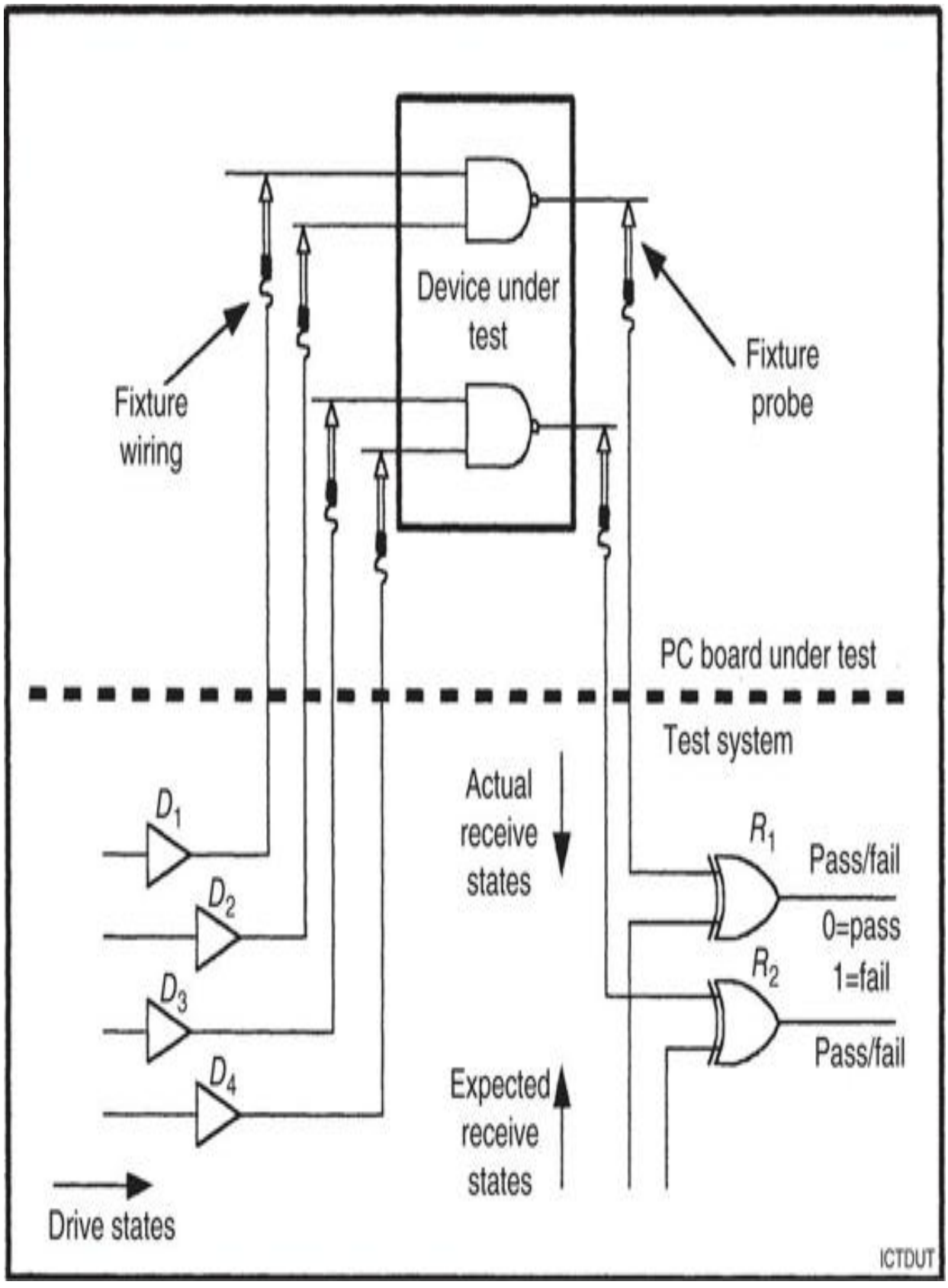

Device under test
Fixture wiring
Fixture probe
PC board under test
Test system
Actual receive states
Expected receive states
D_1
D_2
D_3
D_4
R_1
Pass/fail
0=pass
1=fail
R_2
Pass/fail
Drive states
ICTDUT

FIGURE 57.9 In-circuit digital test setup with full nodal access. The device under test is most often connected to other devices.

A problem with backdriving is that the tester drivers are abusing the upstream drivers in other devices[m] while testing the device of interest. Studies[4] have shown that this is a legitimate concern and that damage to upstream devices may occur. For example, overdriven silicon junctions or device bond wires may heat up enough to be damaged. Sometimes this damage may occur surprisingly fast (within milliseconds). This problem can be solved by careful application of tests with an eye toward their duration. If backdrive testing can be done quickly, and/or with appropriate cooling intervals, then damage can be successfully avoided.[5] This has allowed digital in-circuit testing to become the dominant testing technology.

A great advantage of digital in-circuit testing is that it is performed directly on the inputs and outputs of a targeted device. If the device should fail testing, this is seen directly, rather than having its identity masked by interactions with other devices. This is a major differentiation from functional testing. Faults typically can be resolved to two categories of defects: failed ICs or solder opens on I/O/power pins.

Another major differentiator is the ease—indeed, automation—of test programming that is possible with digital in-circuit testing. Tests for ICs can be prepared as if the ICs were standing alone,[n] stored in a library, and recalled from the library when needed. Modern digital in-circuit testers may have library tests for tens of thousands of devices. For custom, one-of-a-kind ICs for which a library test may not exist (e.g., ASICs), it is still substantially easier to create a test for just the one device than it is for a collection of ICs.

57.5.3 Manufacturing Defect Analyzer

A manufacturing defect analyzer (MDA) is essentially a very low-end analog in-circuit tester. One way it maintains low equipment cost is by not having power supplies to power up a board. Another cost savings comes by having only rudimentary programming and operating software. Some amount of test accuracy and yield must be traded for these savings.

57.5.4 General-Purpose In-Circuit Tester

The workhorse of the electronics industry is the general-purpose in-circuit tester that merges support for analog and digital in-circuit tests. An example of a widely used system is shown in Fig. 57.10. It contains power supplies for powering boards and often contains sophisticated analog in-circuit programming tools and extensive libraries of digital tests. The typical test and repair flow for this tester is shown in Fig. 57.11. Note the early exit to repair for boards that fail shorts testing. This avoids applying power to boards that contain shorts because these may present hazards to the board and human operator, plus they also confuse the diagnosis of faults later in testing.

Agilent
Agilent

FIGURE 57.10 Example of a commercial in-circuit test head and operator terminal, with a printed circuit board mounted in the testing position on top of the bed-of-nails fixture.

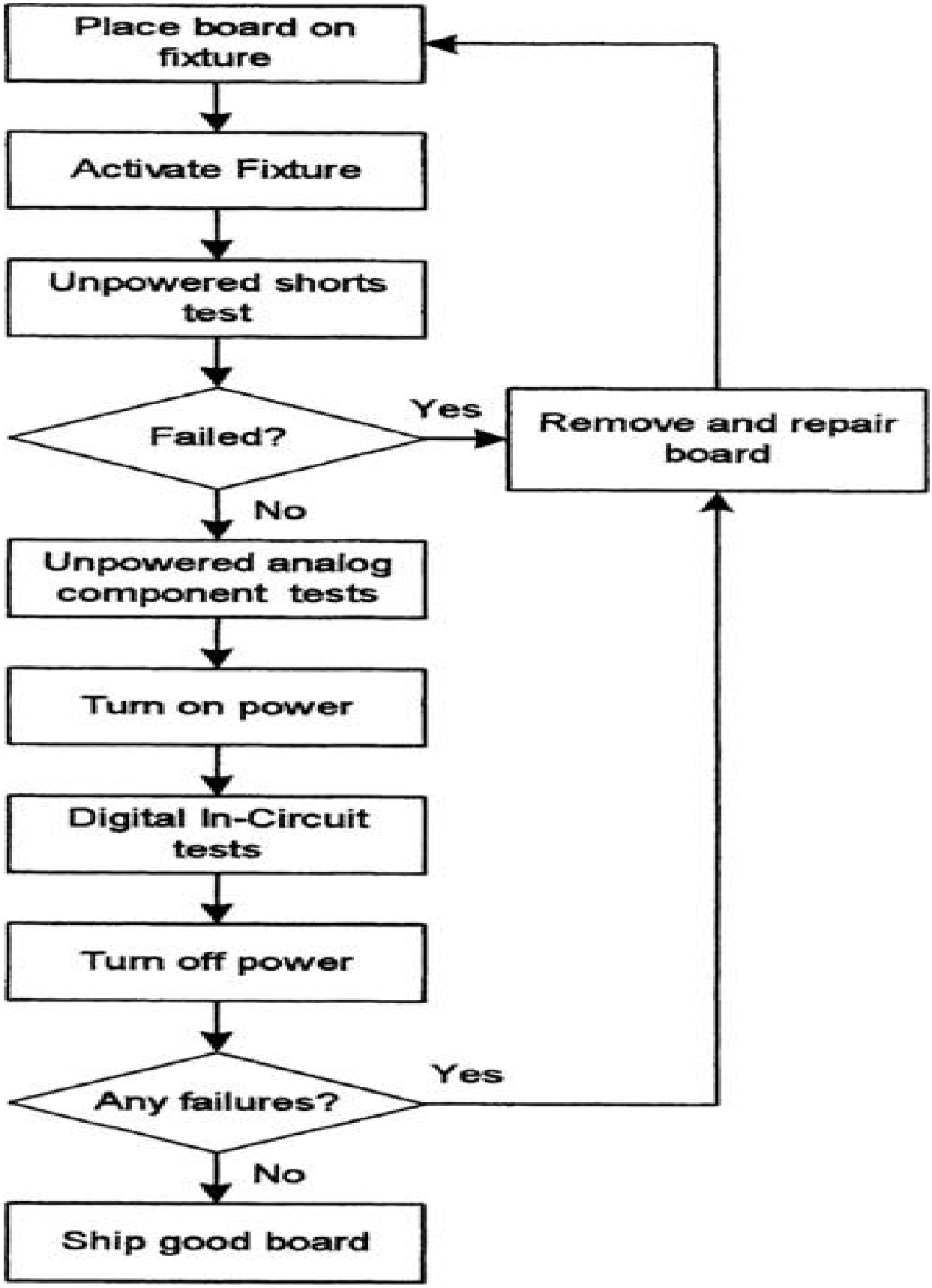

Place board on fixture
Activate Fixture
Unpowered shorts test
Failed?
Yes
Remove and repair board
No
Unpowered analog component tests
Turn on power
Digital In-Circuit tests
Turn off power
Any failures?
Yes
No
Ship good board

FIGURE 57.11 Typical test and repair flow for an in-circuit tester.

57.5.5 Combinational Tester

In situations where a manufacturing line has a variety of technologies in production, a need may exist for both functional and in-circuit testing. Thus, hybrid functional/in-circuit testers (commonly called combinational testers) exist. These machines give test engineers a full complement of tools to address testing problems. They also allow “one-stop” testing, where manufacturing defects and functional performance faults can be detected at one site in the production flow.

A combinational tester utilizes a bed of nails to perform in-circuit analog and digital tests. It may also utilize edge connector access to perform functional tests. In some cases these approaches are hybridized by constructing a two-stage bed-of-nails fixture that has two lengths of nails used in the bed, and a platen that has two stations of depression during operation. The first station is full depression, which brings all nails into contact with the circuit board for standard in-circuit access. The second station is partial depression, where only the longer nails still contact the board, perhaps at the board edge, for functional testing. The removal of the shorter nails removes the electrical loading they present to internal circuit nodes and allows the board to operate in a more natural environment.

57.6 ALTERNATIVES TO CONVENTIONAL ELECTRICAL TESTS

Alternative tests use radically different approaches to specifically address the resolution of defects. These may be

needed to address blind spots in traditional electrical test methodologies. Two specific examples of defects that are difficult to resolve by conventional tests are given here.

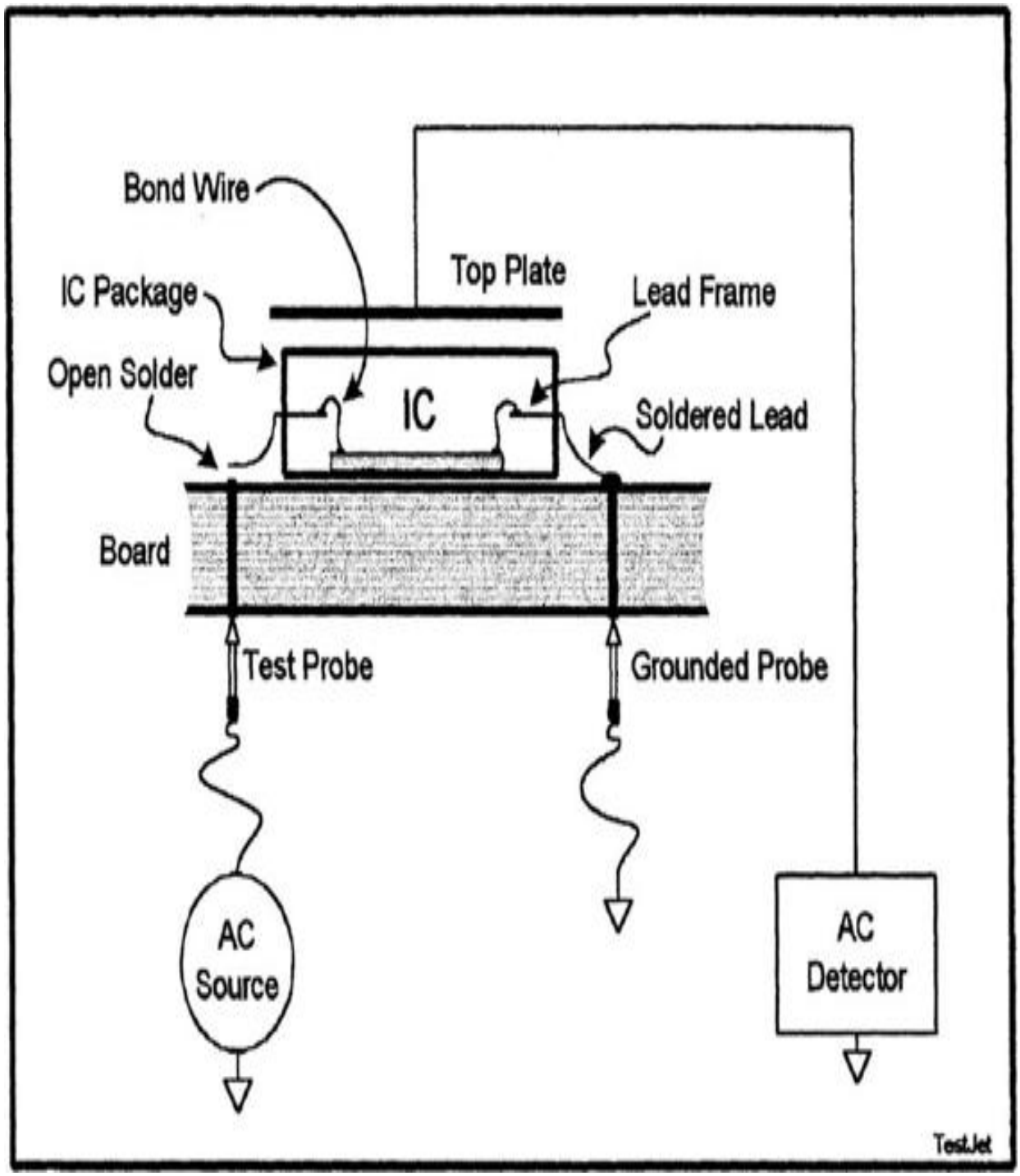


FIGURE 57.12 Capacitive leadframe testing used to find open solder joints.

First, consider a board with a large number of bypass capacitors. All of these capacitors are connected between power and ground so their parallel capacitances are summed. Using an analog in-circuit test, it is possible to test for this summed capacitance. However, if one capacitor is missing or tombstoned, the tester most likely will not notice because the resulting decrement in capacitance will likely fall well within the summed tolerances of the summed capacitances. The performance of the board at higher operating frequencies may be adversely affected, however, due to a loss of noise immunity. This could be detected (possibly) by a performance test. However, if this performance test failed, it could be very difficult to resolve which capacitor was missing. One non-traditional way to test for this problem is to use human visual inspection to look for missing capacitors. This may not find solder opens, however. Another approach would be to use an automated x-ray laminographic tester to check for the existence and solder integrity of each capacitor. Even the orientation of polarized capacitors can be verified. (See Chap. 55 for a discussion of x-ray inspection.)

Second, consider again the open solder problem on a digital device input. This defect may manifest itself as improper device behavior, but it would be wrong to replace the device (which would also fix the solder open) because the device is not at fault. Digital in-circuit testing has trouble resolving solder opens on input pins from bad devices.[o] Final resolution can be obtained either by visual inspection or by using a handheld probe to see if board signals reach IC legs, but this is becoming increasingly difficult as packaging dimensions continue to shrink (e.g., TAB) and newer attachment technologies (e.g., ball grid arrays) are used that prohibit visual inspection or probing altogether.

An alternative approach to the open solder problem uses a capacitive coupling technique to look for opens. The technique exploits the fact that many ICs have a leadframe

that forms the conductive path from the legs of the device to the die bond wire pads. Using the bed of nails, all but one node attached to the IC can be grounded (this is an unpowered technique) and a small AC signal can be applied to the node that remains. An insulated metal plate pressed against the top of the IC forms the top plate of a capacitor and the stimulated IC leg and lead frame conductor form the bottom plate.

Figure 57.13 shows an equivalent circuit for capacitive opens test for a properly soldered IC lead and for an open solder condition. The capacitance C1 may be on the order of 100 fF (100×10^{-15} F), which is small enough to require sophisticated detection electronics to measure in the face of environmental noise. Now, if the IC leg is soldered to the stimulated board node, the correct capacitance will be measured. If the solder joint is open, then a second small capacitance C2 now exists in series with the first. This reduces the measured capacitance by a factor of 2 to 10. Capacitive leadframe test allows testing of complex ICs for solder opens without knowing what the ICs actually do and without applying power. The technique requires no complicated programming, and gives accurate resolution of solder defects. The technique has been extended to allow testing of solder integrity for connectors and switches. A fixture for capacitive leadframe testing is shown Fig. 57.14.

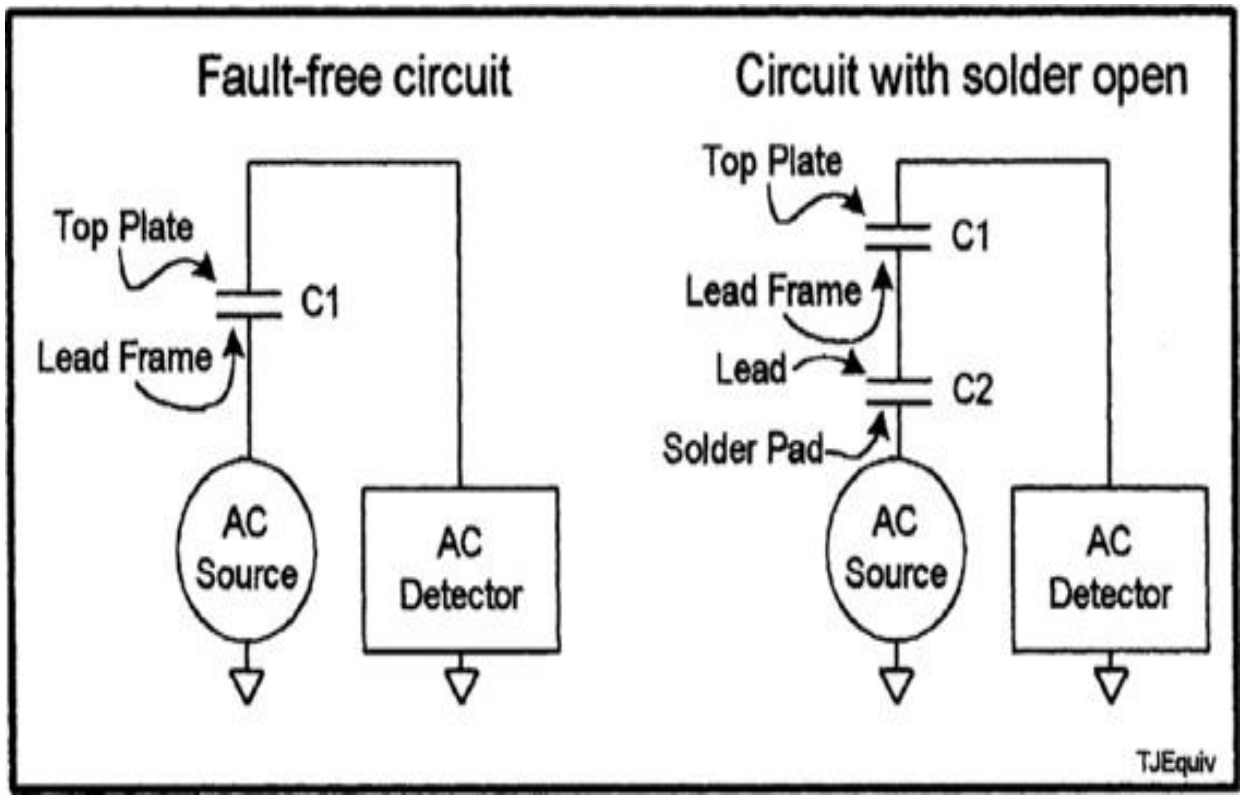


FIGURE 57.13 Equivalent circuits for fault-free and open solder conditions.

FIGURE 57.14 A test fixture with board on a bed of nails, with clamshell top fixture containing capacitive sensor plates. Notice eight closely spaced sensor plates (right) that test for opens in eight (white) connectors on the board.

57.7 TESTER COMPARISON

Table 57.2 summarizes the types of tester for comparative costs and capabilities. A majority of manufacturers value good diagnostic resolution and fault coverage, so it is not surprising that in-circuit and combinational testers are in widespread use. Next in prevalence are the MDA testers, which are typically used where coverage and diagnostic resolution may be sacrificed for ease and speed of programming, usually in low-cost, high-volume products. Functional and specification testers are becoming rare, and are often only justified by the existence of contractual or regulatory requirements.

TABLE 57.2 Costs and Capabilities of Various Testers

Tester Type	Typical Cost ($)	Programming Time	Diagnostic Resolution	Fault Cover	Comments
MDA	10^4–10^5	1–2 days	Fair	Poor	No digital coverage; requires known good board for programming.
In-Circuit	10^5–10^6	5–10 days	Best	Good	Fixturing is a major portion of preparation time.
Combo	10^5–10^6	10–30 days	Best	Best	Functional test programming is a major portion of preparation time.
Functional	10^5–10^6	1–4 months	Fair	Fair	Very high skill required for test preparation and interpreting results.
Specification	10^3–10^8	Weeks to years	Poor	?	Very high skill required for test preparation and interpreting results.

57.8 REFERENCES

1. W. A. Groves, “Rapid Digital Fault Isolation with FASTRACE,” *Hewlett Packard Journal*, vol. 30, no. 3, March 1979.
2. K. P. Parker, *Integrating Design and Test: Using CAE Tools for ATE Programming*, Computer Society Press of the IEEE, Washington, DC, 1987.
3. D. T. Crook, “Analog In-Circuit Component Measurements: Problems and Solutions,” *Hewlett Packard Journal*, vol. 30, no. 3, March 1979.
4. G. S. Bushanam et al., “Measuring Thermal Rises Due to Digital Device Overdriving,” *Proceedings of the International Test Conference*, Philadelphia, PA, October 1984, pp. 400–407.
5. V. R. Harwood, “Safeguarding Devices Against Stress Caused by In-Circuit Testing,” *Hewlett Packard Journal*, vol. 35, no. 10, October 1984.

[a] Perhaps the reader remembers the TV ads for Zenith televisions from about 25 years ago. They showed individual axial lead components being hand-wired onto lug strips and then soldered. The voice-over mentioned "*hand-crafted*" quality as if to imply that automated manufacturing (being used by Japanese manufacturers like Sony) was suspect.

[b] It is important to differentiate test yield from defect coverage of a test. The yield of the manufacturing process before test might be (say) 50 percent, and the yield after test may be 97 percent. This may be accomplished with a test that detects (covers) 90 percent of the important defects.

[c] From basic probability theory, $(0.97)^{20} = 0.54$ is the chance that 20 independently manufactured boards with a probability of 0.97 of being fault free will all be fault free.

[d] Measuring yields in percentages is telling. In the IC industry, yields are measured in parts per million. One ppm corresponds to 99.9999 percent, and 250 ppm, a good IC yield, equals 99.975 percent yield. Will the board industry ever get into these ranges? Will it make sense to try?

[e] See Sec. 57.6 for a discussion of how a new testing methodology may pinpoint a defect that conventional methodologies have difficulty isolating.

[f] Logic simulation implies the treatment of the digital nature of the circuit, typically omitting any interaction with any analog portions of the circuit. Analog simulators do exist, but are implemented in a very different technology from digital simulators. Mixed-signal simulation is not anywhere near as viable as digital simulation, which presents a problem for test engineers.

[g] For example, say a circuit has 100,000 gates. The number of stuck-at faults to be simulated may easily be 200,000. A set of test vectors for these may easily exceed 500,000. If the circuit has a fairly normal complement of 250 outputs, then a fault dictionary for this example would consume the product of faults times vectors times outputs (2.5×10^{13} bits, or about 3.125 terabytes, give or take a gigabyte). Fault simulation times lasting months, even on very fast computers, have been reported. Of course, larger circuits will need more!

[h] CMOS VLSI circuits have several defect modes that are inconvenient to model in popular fault simulators, and thus fault models are more likely not to match defects. Two of the offending defect modes are bridging faults (intermetal shorts) and metallization opens that may actually introduce capacitive memory into a circuit. These are difficult to represent with traditional fault-modeling techniques.

[i] Complex analog devices such as analog or mixed-signal ICs are not very amenable to analog in-circuit testing because they require power to be applied to the board. Simple diodes and single transistors can be tested by in-circuit stimulus that essentially examines the characteristics of their semiconductor junctions.

[j] The reason for using a small stimulus voltage (typically less than 0.2 V) is to prevent current flow through semiconductor junctions that may exist between nodes. This voltage will not turn on a junction. These junctions may exist in parasitic form within ICs and are not always documented.

[k] A half-splitting technique (also called a binary chop) is a fundamental algorithm of computer science. It works by successively considering half of a set of items (grounded nodes that are receiving current in this case) while removing the other half from consideration. It recursively divides sets repeatedly until only one item is left to consider. It has a complexity related to the logarithm (base 2) of the size of the original set of items. By comparison, a linear process has a complexity linearly related to the size of the original set.

[l] This component may not be alone in a physical sense, but because low stimulus voltages are used, other connected devices such as ICs may be electrically quiescent so that the component is electrically alone.

[m] This abuse can be mitigated by “conditioning” upstream drivers. One method is to disable the upstream drivers by devoting additional tester drivers to driving states on disabling inputs (when they exist) such as output enable pins. Of course, the problem may simply be moved upstream, because the disabling inputs may also be connected to upstream drivers that are now being overdriven in place of the original drivers. This conditioning process may be carried out to several levels, if desired.

[n] This assumes that the IC does not have any topological constraints on its I/O pins, such as having an input pin connected directly to ground or an output pin fed back to an input pin. In such cases, the prepared test may be incompatible with these constraints and may only be used after incompatible segments of the test are deleted, reducing fault coverage.

[o] Ignore for the moment the possibility of using boundary scan to solve this problem, which is discussed in Chap. 56.

CHAPTER 58

FAILURE MODES AND EFFECTS ANALYSIS

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

58.1 PROGNOSTICS AND HEALTH MANAGEMENT

Reliability has many dimensions. One current popular focus in the safety and availability of systems or products through the use of *prognostics and health management* (PHM). Prognostics is the process of predicting the future reliability of a product by assessing the extent of deviation or degradation of a product from its expected normal operating conditions. Health management is the process of decision making and implementation of actions to use, maintain, repair, or replace the product based on the state of health and expected future use of the product.

58.1.1 Key Elements of Prognostics

- Failure modes and effects analysis (FMEA) (see Fig. 58.1)

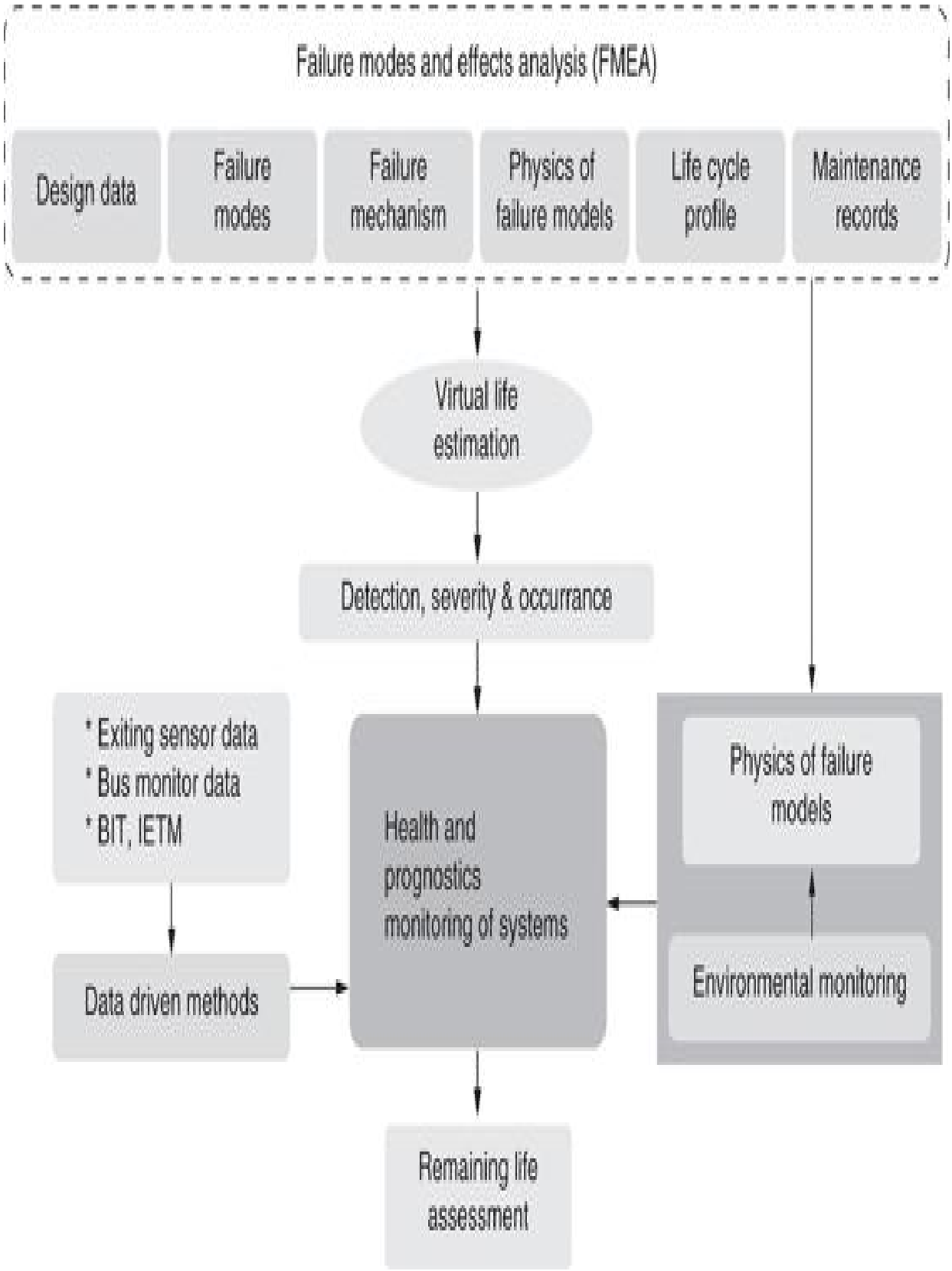

Failure modes and effects analysis (FMEA)
Design data
Failure modes
Failure mechanism
Physics of failure models
Life cycle profile
Maintenance records
Virtual life estimation
Detection, severity & occurrance
* Exiting sensor data
* Bus monitor data
* BIT, IETM
Data driven methods
Health and prognostics monitoring of systems
Physics of failure models
Environmental monitoring
Remaining life assessment

FIGURE 58.1 Overview of CALCE's approach on PHM implementation to improve the availability and safety of systems.[1]

- Physics of failure (PoF): (1) using expendable devices, such as fuses, (2) modeling of stress and damage utilizing knowledge of loading conditions and system properties (material, geometric, etc.)
- Data-driven approaches—monitoring and reasoning of parameters that are precursors to impending failure, such as shifts in performance parameters
- Synergistic techniques—combination of FMEA, PoF, and data driven methods

There exists a huge potential for product improvements using these methodologies, but it all starts with FMEA.

58.1.2 What Is FMEA?

58.1.2.1 Definition. FMEA is a systematic process to evaluate failure modes and causes associated with the design and manufacturing processes of a new product. [It is somewhat similar to the Potential Problem Analysis (PPA) phase of the Kepner-Tregoe program.] A list of (1) potential failure modes of each component or subassembly and causes associated with the designing and manufacturing of a product, (2) identify actions which could be eliminate or reduce the chance of a potential failure occurring, and (3) then document the process and give each mode a numeric rating for frequency of occurrence, criticality, and probability of detection. Finally, these three numbers are multiplied together to obtain the risk priority number (RPN), which is used to guide the design effort to the most critical problems first.

Two aspects of FMEA are particularly important: a team approach and timeliness. The team approach is vital because

the broader the expertise that is brought to bear on making and assigning values to the failure mode list, the more effective the FMEA will be.

Timeliness is important because FMEA is primarily a preventive tool, which can help steer design decisions between alternatives before failure modes are designed-in, rather than redesigning after the failure occurs. FMEA is equally applicable to hardware or software, to components or systems.

58.1.2.2 Comparison to FTA. Another similar process is fault tree analysis (FTA). While FMEA is a “bottom-up” approach, FTA is “top-down.” FTA starts with the assumption of a system failure mode, and then works down through the system block diagram to look for possible causes of that mode.

Thus, FTA requires fairly complete, detailed information about the system, and is most effective after the system is well-defined. (FTA could be performed, in a limited way, on alternative system concepts; this could be used to help decide the best of several alternatives.) A separate FTA must be performed for each system failure mode.

FTA and FMEA are complimentary. Whenever possible, both should be used. For practical reasons, FTA should be limited to the really serious system-level failure modes, such as those involving safety or permanent system damage. FMEA can be used at the component, subassembly, and module level, to help optimize those modules. There are excellent discussions and examples of FTA in the Further Reading section at the end of this chapter.

58.1.3 Benefits of FMEA

The RPN calculated by FMEA allows prioritization of the failure mode list, guiding design effort to the most critical

areas first. It also provides a documentary record of the failure prevention efforts of the design team, which is helpful to management in gauging the quality and extent of the effort, to production in solving problems which occur despite these efforts, and to future projects which can benefit from all the work and thinking which went into the failure mode and cause lists.

Eliminating potential failure modes has both short term and long term benefits. The short term benefit is most often recognized because it represents savings of the costs of repair, retest, and downtime, which are objectively accountable. The long term benefit is much more difficult to measure, since it relates to the customer's satisfaction or dissatisfaction with the product, and his perception of its quality.

58.1.3.1 FMEA Supports the Design Process

- Aiding in the objective evaluation of alternatives during design
- Increasing the probability that potential failure modes and their effects on system operation have been considered during design
- Providing additional information to aid in the planning of thorough and efficient test programs
- Developing a list of potential failure modes ranked according to their probable effect on the customer, thus establishing a priority system for design and test
- Providing an open, documented format for recommending and tracking risk-reducing actions
- Identifying known and potential failure modes which might otherwise be overlooked
- Exposing and documenting the ways a system can fail, and the effects of such failures
- Detecting primary but often minor failures which may cause serious secondary failures or consequent damage

- Detecting areas where “fail safe” or “fail soft” features are needed
- Providing a fresh viewpoint in understanding a system’s functions

58.1.3.2 FMEA Report Uses

- Formal record of the safety and reliability analysis and planning, to satisfy customers or regulatory agencies
- Evidence in litigation involving safety or reliability
- Design of diagnostic routines or built-in tests
- Basis for creating trouble-shooting procedures
- Means to consider and prevent manufacturing defects
- Problem follow-up and corrective action tracking
- Future reference to aid in analyzing field failures, evaluating design changes, or developing improved designs

58.2 THEORY

In simple terms, the FMEA process attempts to list every failure mode of each component of a system, and to predict its effect on system operation. Failure effects can be considered at more than one level, for example, effects at the subsystem or overall system levels.

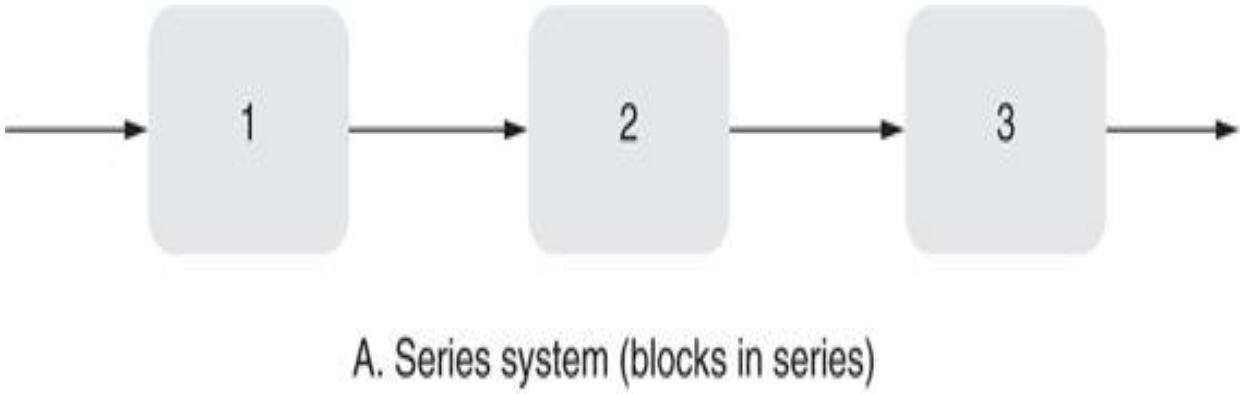
FMEA can be accomplished using either a component or functional approach. In the component approach, actual failure modes are listed (e.g., resistor open, bearing seizure). The functional approach is used when the details of the design are not yet fully defined. In this approach, function failures are considered (e.g., no feedback, memory lost). FMEA can also be performed using a combination of component and functional approaches. The failure mode is the symptom of the failure, as distinct from the cause of the

failure, which consists of the proved reasons for the existence of the symptoms. Reliability aspects of the components must be considered in this process. FMEA requires inputs from hardware, software, systems, customer service, and manufacturing in assessing component failures, effects at higher levels of the system, fault detection, and in evaluating failure compensating provisions in the design.

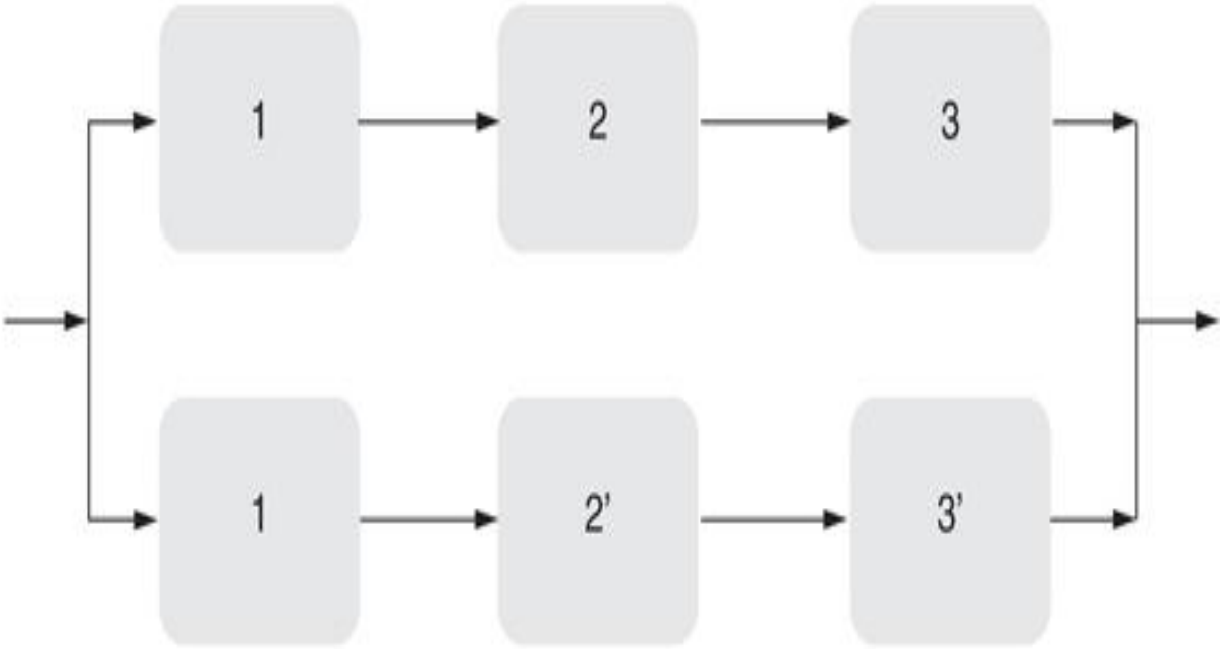
58.2.1 Procedure

FMEA should be performed by a team of people having broad knowledge of the system's design and application. All available information on the design should be obtained: external and internal reference specifications, schematics, computer-aided design (CAD) data, stress analysis, reliability prediction data, test results, etc.

A system functional block diagram and reliability block diagram (Fig. 58.2) should be prepared, as these are important for preparing the FMEA, and for understanding the completed analysis. All possible operating modes of the system and their functional relationships should be considered in the analysis. If the system has redundancy, it should also be considered by evaluating the effects of failure modes assuming the redundant system may or may not function.



A. Series system (blocks in series)



B. Redundant series system (series blocks in parallel)

FIGURE 58.2 Reliability block diagram examples.

FMEA can be performed from different points of view, such as failure detectability, safety, repair cost, availability, etc. The customer’s point of view should always be first, in order to improve customer satisfaction with the final product. The viewpoint being considered should be consistent throughout a particular analysis, in order to assign proper criticality

values. A hierarchical approach works well with systems, using a component approach at the lowest assembly level, and a functional approach to combine the effects of various subsystems. This also allows the FMEA to be performed even when some subsystems are not yet completely designed.

If CAD has been used on parts of the system, the FMEA can utilize that capability to simulate the effects of various failure modes. Such an analysis can greatly enhance the accuracy and objectivity of the FMEA process.

FMEA is an ongoing process which should be started as soon as initial design information is available. It should be updated and enhanced as the design evolves, so that the analysis can be used to improve the design. All possible design alternatives should be separately analyzed, so that the effect on system performance and reliability can be considered in deciding which option to implement. Test results should be used later to update the analysis.

58.2.1.1 Requirements to Perform FMEA. There are basically sixteen (16) steps to create a FMEA:

1. A team of people with a commitment to improve the ability of the design to meet the customer's needs
2. Schematics and block diagrams of each level of the system, from subassemblies to complete system
3. Component specifications, part lists, and design data
4. Functional specifications of modules, subassemblies, etc.
5. Design manuals
6. Manufacturing requirements and details of the processes to be used
7. FMEA forms and a list of any special considerations, such as safety or regulatory, applicable to this product

58.2.1.2 Steps in Performing FMEA (See Fig. 58.3)

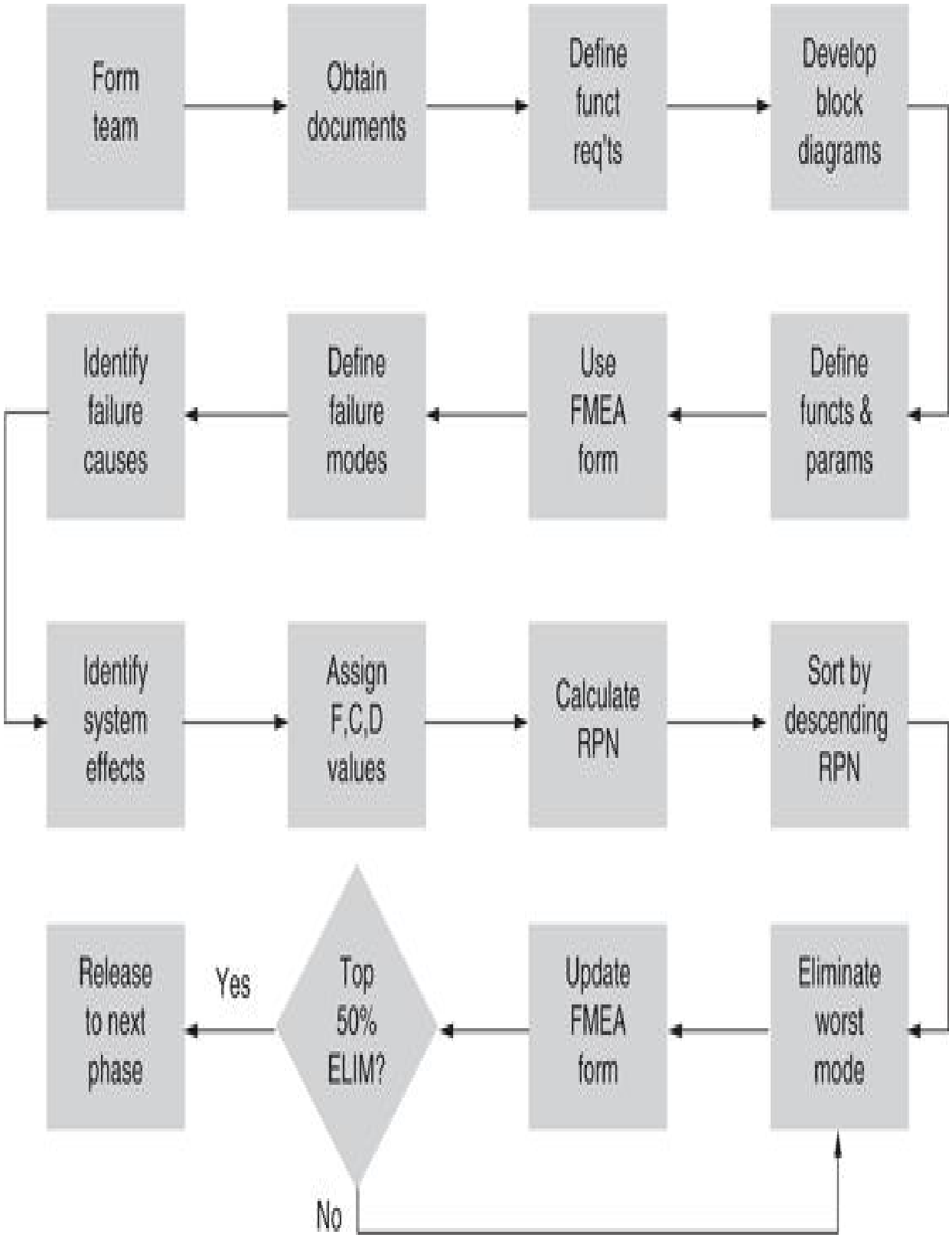


FIGURE 58.3 FMEA flow chart.

1. Discuss and define system functional requirements, including all modes of operation (list in order of decreasing importance).
2. Develop a functional block diagram and a reliability block diagram (Fig. 58.2) for each subassembly being analyzed.
3. Define parameters and functions of each functional block required for successful operation of the system.
4. Using the FMEA forms to document the further steps, identify potential failure modes for each of the functional blocks.
5. Analyze system or subassembly functions affected by factors such as those in the list of FMEA considerations.
6. Identify all possible causes for each failure mode of the functional block being analyzed. The causes must be detailed to the component level wherever possible.
7. Identify all possible ways the failure modes could affect the functions of the higher-level assemblies.
8. Assign the frequency, criticality, and detection values for each failure mode (see Tables 58.1, 58.2, and 58.3).

TABLE 58.1 Frequency Ranking

Criteria for Probability of Failure	Code
REMOTE probability of occurrence. Process capability shows at least X ± 4 SIGMA (99.99%) within spec.	1
LOW probability of occurrence, with process in statistical control. Capability shows at least X ± 3 SIGMA (99.87%) within spec.	2
MODERATE probability of occurrence for processes experiencing failures. Process in statistical control, with X ± 2.5 SIGMA (99.38%) within spec.	3
HIGH probability of occurrence, with frequent failures. Process is in statistical control, but capability shows X ± 2.5 SIGMA or less.	4
VERY HIGH probability of occurrence. Failure is almost certain to occur sooner or later.	5

TABLE 58.2 Criticality Ranking

Criteria	Code
MINOR nature of failure, no noticeable effect on performance, undetectable by customer.	1
LOW severity, causing only slight customer annoyance due to very minor subsystem performance degradation.	2
MODERATE failure causing some customer discomfort, dissatisfaction and annoyance due to subsystem or total performance degradation.	3
HIGH degree of customer dissatisfaction due to nature of the failure (inoperable subsystem or total system).	4
VERY HIGH severity ranking for failure mode involving potential safety problems and/or conformance to federal regulations. Nonregulated components with a 4 or 5 criticality code and frequency code >1 should be designated as control items.	5

TABLE 58.3 Detection Ranking

Criteria	Code
REMOTE likelihood that product would be shipped containing such an obvious defect, since it is detected by subsequent factory tests.	1
LOW likelihood for shipment with defect which is visually obvious or has 100% automatic checking.	2
MODERATE likelihood for shipment with defect since the defect is easily identifiable through automatic inspection or functional checking.	3
HIGH likelihood of shipping with subtle defect.	4
VERY HIGH likelihood that defect will not be detected prior to shipping (checks are impossible or defect is latent).	5

9. Obtain the risk priority number (RPN) by multiplying the three values assigned in step 8. This priority number will allow us to focus on the most important failure modes first.
10. Determine corrective actions for each failure mode, and update the design status as it progresses.
11. Summarize the failure modes and corrective actions in order of decreasing RPN.
12. Focus on eliminating at least the 50 percent of the failure modes with the highest RPN.

Two examples of a FMEA analysis are shown in Figs. 58.4 and 58.5.

Failure modes and effects analysis

Product: Wand Assembly: XMTR RF module

Engineer: Holden Date: 4/24/14

Assy ID	Functional block	Failure mode	Failure cause	Effect of failure on system	F	C	D	RPN	Corrective action or remark
1	Modulation	Wrong freq. wrong dev/level	Defective components	RCVR will not detect XMTR sig and error msg on the screen	1	4	1	**4**	RCVR AFC will try to readjust to the changed freq. and then display error message
		Output power level low	Defective Q1	Weak patient sig and possibly bit errors in that channel	2	3	3	**18**	Invalid data message on the screen
2	Oscillator tank circuit	No output frequency	Drift trim cap defect induc, cap, or Q1 shorted res	No RF sig from XMTR error mag on the screen	2	4	1	**8**	Error message to be defined. Trim caps should be sealed with epoxy
		Wrong freq. wrong dev level	Drifted trim cap						
3	RF tank circuit	Output pwr level low	Def transistor drifted trim cap or pot shorted CR3 shorted res	Weak patient sig and possibly bit errors in that channel	2	3	3	**18**	Invalid data message on the screen
		Output pwr level high	Drifted trimpot open CR3	High current drain from XMTR battery	2	3	5	**30**	Trim pots should be sealed with epoxy

F: Frequency 1=Remote 2=Low 3=Moderate 4=High 5=Very high

C: Criticality 1=Remote 2=Low 3=Moderate 4=High 5=Very high

D: Detection 1=Remote 2=Low 3=Moderate 4=High 5=Very high

RPN: Risk priority number = FxCxD

FIGURE 58.4 FMEA example 1.

Failure modes and effects analysis

Product: Wand Assembly: XMTR power supply

Engineer: Holden Date: 4/24/14

Assy ID	Functional block	Failure mode	Failure cause	Effect of failure on system	F	C	D	RPN	Corrective action or remark
1	Regulator circuit	Output vol high/ low	Defective regulator chip	XMTR RF freq may shift & DIG & ECG ckts may malfunction	2	3	2	**12**	For RF ckt +/–1% reqd & this voltage should be monitored
2	Analog switch	Ouput power low	Analog switch stuck closed	XMTR malfunct LB & DSB mag on the screen	2	3	1	**6**	
		No output voltage	Analog switch stuck open	No patient signal will be transmitted	2	4	1	**8**	Patient cannot be monitored
3	Ref voltage 2.5V ckt	Ref voltage high	Shorted R3 open R5 op amp stuck high	Effects unknown system will malfunction	2	2	1	**4**	
		Ref voltage low/ zero	Open R3 shorted R5 op amp stuck low	Effects unknown system will malfunction	2	2	1	**4**	
		Ref voltage unstable	Open C7 op amp unstable	Effects unknown system will malfunction	2	2	1	**4**	
4	LB and DB circuit	False alarm	Open R8 shorted R6 U5 stuck high	Battery drain unnec batt replace	2	3	1	**6**	Nuisance to maintenance personnel and user
		No alarm when req'd	Shorted R8 open R6 U5 stuck low	Could affect monitoring when battery is low	2	3	3	**18**	Special test should be conducted on the floor to detect this problem

F: Frequency 1=Remote 2=Low 3=Moderate 4=High 5=Very high

C: Criticality 1=Remote 2=Low 3=Moderate 4=High 5=Very high

D: Detection 1=Remote 2=Low 3=Moderate 4=High 5=Very high

RPN: Risk priority number = Fx Cx D

FIGURE 58.5 FMEA example 2.

58.2.2 FMEA Considerations—Alternatives

Hermeticity
Humidity
Exposure to radiation
Input/output sensitivity
Digital/analog separation
Work load
Technology
Part history
Old (well established) part
Stress ratio
Pins/configurations
Failure rate
Power dissipation
Cooling
Test points
Feedback stability
Protection methods
Error correction coding
Limited life
Overshoot
Trade-offs
Ergonomics
Service base
Documentation
Vendors/sources
Temperature
Shock and vibration
RPI/transient/ESD
Input/output timing
Duty cycle
Part circuit complexity
Packaging
New (unproven) part
Ratings
Tolerances
Material construction
Burn-in
Derating
Diagnostics
Identification/repeatability
Noise
Software functions
Fault tolerance
Wear characteristics
Interchangeability
Foolproof/fail-safe
Juxtaposition
Adjustments/redundancy
Regulatory agencies

58.3 WHAT IS PROCESS FMEA?

58.3.1 Definition

A process potential FMEA is an analytical technique utilized by manufacturing/process engineers as a means to assure that, to the extent possible, potential concerns have been considered and addressed. In its most rigorous form, a P-FMEA is a summary of the engineer's thoughts (including an analysis of items that could go wrong based on experience and past concerns) as a process is developed. This systematic approach parallels and formalizes the mental discipline that an engineer normally goes through in any manufacturing planning process.

The process potential FMEA identifies potential product related process failure modes, assesses the potential down-stream effects of the failures, identifies the potential manufacturing or assembly process causes and identifies failure modes ranking according to their effect on the "customer," thus establishing a priority system for corrective action considerations. The P-FMEA also documents the results of the manufacturing or assembly process.

A list of (1) potential concerns that might cause failure modes for each process or subassembly and causes associated with the designing and manufacturing of a product, (2) identify actions which could be eliminate or reduce the chance of a potential process failure occurring, (3) then document the process and give each mode a numeric rating for frequency of occurrence, criticality, and probability of detection. Finally, these three numbers are multiplied together to obtain the risk priority number (RPN), which is used to guide the design effort to the most critical problems first.

Two aspects of P-FMEA are particularly important: a team approach, and timeliness. The team approach is vital

because the broader the expertise that is brought to bear on making and assigning values to the failure mode list, the more effective the P-FMEA will be.

Timeliness is important because P-FMEA is primarily a preventive tool, which can help steer manufacturing development decisions between alternatives before failure modes are built-in, rather than reworking after the failure occurs. P-FMEA is equally applicable to hardware or software.

58.3.2 Steps in Performing P-FMEA

1. Discuss and define manufacturing and process functional requirements, including all modes of operation (list in order of decreasing importance).
2. Develop a functional block diagram and a reliability block diagram (Fig. 58.2) for each manufacturing/process being analyzed.
3. Define parameters and functions of each functional block required for successful operation of the process.
4. Using the FMEA forms to document the further steps, identify potential failure modes for each of the functional blocks.
5. Analyze process or subassembly functions affected by factors such as those in the list of FMEA considerations.
6. Identify all possible causes for each failure mode of the functional block being analyzed. The causes must be detailed to the component level wherever possible.
7. Identify all possible ways the failure modes could affect the functions of the higher-level manufacturing steps or processes or assemblies.
8. Assign the frequency, criticality, and detection values for each failure mode (see Tables 58.1, 58.2, and 58.3).
9. Obtain the RPN by multiplying the three values assigned in step 8. This priority number will allow us to focus on

the most important failure modes first.

10. Determine corrective actions for each failure mode, and update the manufacturing documentation as it progresses.
11. Summarize the failure modes and corrective actions in order of decreasing RPN.
12. Focus on eliminating at least the 50 percent of the failure modes with the highest RPN.

58.3.3 Summary

FMEA and P-FMEA are a continuing process which should be initiated at investigation/launch time of the design cycle and then be regularly updated as changes occur throughout the phases of product development. FMEA must be completed before the design is “frozen,” for its purpose is to affect the design and harden it against failures due to causes that can be anticipated. Potential manufacturing or assembly concerns known by the design engineer should be conveyed to the production engineers, using means such as the P-FMEA team meetings. Figure 58.6 provides a blank FMEA worksheet for your use.

Failure modes and effects analysis

Product:_____ Assembly:_____

Engineer:_____ Date:_____

Assy ID	Functional block	Failure mode	Failure cause	Effect of failure on system	F	C	D	RPN	Corrective action or remark

F: Frequency 1=Remote 2=Low 3=Moderate 4=High 5=Very high

C: Criticality 1=Remote 2=Low 3=Moderate 4=High 5=Very high

D: Detection 1=Remote 2=Low 3=Moderate 4=High 5=Very high

RPN: Risk Priority Number = FxCxD

FIGURE 58.6 Blank worksheet.

58.4 REFERENCE

1. *Procedures for Performing FM ECA, MIL-ST D-1629*, available from National Technical Information Service, Springfield, VA 22161.

58.5 FURTHER READING

Ireson and Coombs, *Handbook of Reliability Engineering and Management*, McGraw-Hill, 1988. ISBN 0-07-032039-X

O'Connor, P. D. T., *Practical Reliability Engineering*, 2nd Edition, John Wiley & Sons, 1985. ISBN 0-471-90551-8

Potential Failure Modes and Effects Analysis, Ford Motor Co., Sep. 1988. Available from FORD, Electronics Division, P.O. Box 6010, Dearborn, MI 48121-6010, Attn: Supplier Quality Manager.

58.5.1 Seminars

Applied Reliability Engineering and Product Assurance for Engineers and Managers, Univ. of Maryland, Center for Professional Development, University Blvd. at Adelphi Rd., College Park, MD 20742-1668, telephone (301) 985-7157.

Reliability in Product Design and Testing, American Supplier Institute, 6 Parkland Blvd. Suite 411, Dearborn, MI 48126, telephone (313) 336-8877.

Reliability Training Program (videotape seminar), Technicomp Inc., 1111 Chester Avenue, 300 Park Plaza, Cleveland, OH 44114, telephone (216) 687-1122.

58.5.2 Software Tools

PC FMECA (IBM PC Program), Management Sciences Inc., 6022 Constitution Ave. NE, Albuquerque, NM 87110, telephone (505) 255-8611.

Results (FTA Program), Management Sciences Inc., 6022 Constitution Ave. NE, Albuquerque, NM 87110, telephone (505) 255-8611.

TreeMaster (IBM PC Program), Management Sciences Inc., 6022 Constitution Ave. NE, Albuquerque, NM 87110, telephone (505) 255-8611.

PART 11

RELIABILITY

CHAPTER 59

CONDUCTIVE ANODIC FILAMENT FORMATION

Laura J. Turbini
International Reliability Consultant, Waltham, Massachusetts

Antonio Caputo
Isola Group, Chandler, Arizona

59.1 INTRODUCTION

Electrochemical migration (ECM) is the movement of ionic species in the presence of moisture under the influence of a DC bias. There are several factors which affect the rate of electrochemical migration. These include the nature of the substrate and metallization, the presence of contaminants, the voltage gradient, and the presence of sufficient moisture. This last element is critical, for without sufficient monolayers of water on the surface, ion mobility is impossible.

One type of ECM involves the corrosion of copper. A quantitative test for this has been developed and applied to

some weak organic acid fluxes. The effect of varying the accelerating temperature and humidity was evaluated.

A second example of ECM is the failure mode known as conductive anodic filament (CAF) formation which was first observed in the mid-1970s by two different research groups, Bell Laboratories and Raytheon. Since then, further studies have led to an understanding of the factors that affect CAF formation. Water soluble flux constituents can affect the rate of CAF formation because they are absorbed by the epoxy substrate. SEM/EDS has been used to demonstrate that copper and halide ions are present in the CAF filament around the epoxy/glass interface as well as within the epoxy matrix. CAF has been identified as a copper hydroxy chloride salt that causes catastrophic failure when it bridges because it has semiconductor properties. Brominated CAF—copper hydroxy bromide—can form when a high bromide concentration exists in the flux. The chemistry of CAF formation is explained in detail. A CAF test method for multilayer boards has been developed by Sun Microsystems, and then introduced as an IPC test method. This chapter will explore these topics in more detail.

59.2 ELECTROCHEMICAL MIGRATION

Electrochemical migration (see Fig. 59.1) is the movement of an ionic species under the influence of a DC voltage. Moisture is essential for electrochemical migration to occur. In the presence of moisture, metal ions form at the anode and migrate toward the cathode, where they plate out to form dendrites. When a dendrite bridges the gap between the electrodes, a short occurs that may burn out quickly due to the high current within the fragile dendrite.

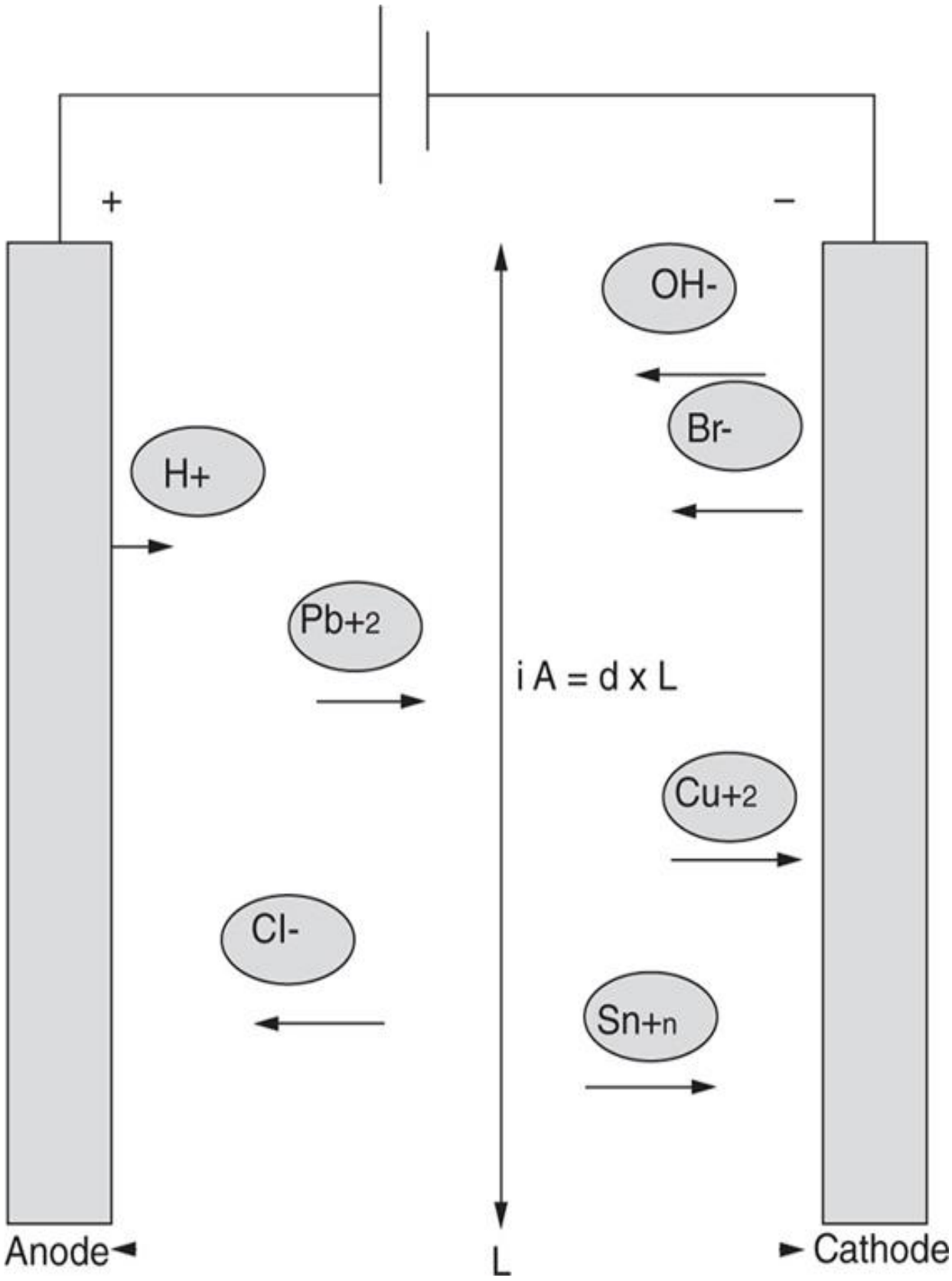

+
−
OH-
Br-
H+
Pb+2
i A = d x L
Cu+2
Cl-
Sn+n
Anode
L
Cathode

FIGURE 59.1 Electrochemical migration showing the movement of positive ions toward the cathode and negative ions toward the anode.

Electrochemical corrosion increases as circuit spacing decreases. This is due to the increase in the electric field, which is inversely proportional to the spacing between the conductors [see Eq. (59.1)].

$$E = \frac{V}{d} \tag{59.1}$$

where E = electric field
V = voltage
d = spacing between the conductors

Ohm's law [Eq. (59. 2)] describes the linear relationship between voltage, current, and resistance:

$$V = IR \tag{59.2}$$

where V = voltage drop
I = current in amps
R = resistance in ohms

Resistance is not an intrinsic property of a material. Rather, it depends on some geometric factors as well as the intrinsic resistivity of the substrate. For surface resistance, use Eq. (59.3):

$$R = \rho \frac{d}{A} \tag{59.3}$$

where ρ = resistivity of the material
d = the separation between the conductors traces
A = the cross-sectional area

Conductivity (σ) is the inverse of resistivity:

$$\sigma = \frac{1}{\rho} \tag{59.4}$$

Both resistivity and conductivity can be affected by processing chemicals. Electrochemical corrosion increases as circuit spacing decreases.

Ionic contaminants, which dissolve in the moisture on the surface, increase the conductance (lower the resistance) of the insulating layer between the anode and cathode. Their presence enhances electrochemical migration. How much the migration is enhanced depends on several factors: the solubility of the ion, the mobility of the ion, the effect of pH on solubility, the reactivity of the ion, temperature, and relative humidity.

The solubility of the ion and its mobility in water are important because conductivity depends on both of these factors [see Eq. (59.5)].

$$\sigma = \sum N_i q_i \mu_i \tag{59.5}$$

where N_i = the number of charge carriers of a particular type (e.g., Na^+ cations, or Cl^- anions)
q_i = the charge of the carrier
μ_i = the mobility of the charge carrier

The mobility of a given ion is dependent on temperature and its diffusion coefficient per Eq. (59.6):

$$\mu_{\text{ion}} = \frac{q}{kT} D_{\text{ion}} \tag{59.6}$$

where k = Boltzmann's constant
T = degrees kelvin
D_{ion} = diffusion constant for a particular ion

Tables of ionic conductance in aqueous solution as well as diffusion constants can be found in the *Handbook of Chemistry and Physics*.[1]

Most contaminants from processing do not exist in isolation from one another. Rather, there may be several ionic species present, some of which will interact with one another to create new ionic species.

Solubility of the contaminant salts also depends on the pH. Water ionizes under a bias voltage, creating an acidic medium at the anode and a basic medium at the cathode, as shown in the following reactions [Eq. (59.7)]:

$$\begin{aligned} &\text{Anode:} && \mathrm{H_2O = \tfrac{1}{2}O_2 + 2H^+ + 2e^-} \\ &\text{Cathode:} && \mathrm{2H_2O + 2e^- = 2OH + H_2} \\ & && \mathrm{O_2 + H_2O + 4e^- = 4(OH)} \end{aligned} \tag{59.7}$$

This creates a pH gradient from anode to cathode.

Temperature is another important factor to consider. An increase in temperature increases ion solubility, mobility, and reactivity.

In summary, several factors affect electrochemical migration. These include the nature of substrate and metallization, the presence of contaminants, the voltage gradient, and the presence of sufficient moisture. This last

element is critical, for without sufficient monolayers of water on the surface, ion mobility is impossible.

59.3 DEVELOPING A QUANTITATIVE COPPER CORROSION TEST

The IPC has a number of test methods to qualify substrates and soldering materials. Surface insulation resistance (SIR) is most commonly used to measure ECM susceptibility, but other common tests used over the years have been the copper mirror test (a qualitative measure of raw flux-induced corrosion), a flux corrosion test for assessment of flux residues on copper under harsh environments, qualitative and quantitative tests for individual halides, and for total ionics. At the present time a quantitative test for the corrosivity of flux residues on copper is needed—and this is important because copper is the base metal of almost all electronic circuits.

In 1989, Bono introduced the first quantitative test method.[2] The test coupon consisted of a consisted of a single-sided epoxy glass PWB with uncoated copper traces 9- to 10-μm-thick ~75 μm distance between points A and B (Fig. 59.2*a*). These traces constitute the anodes in an electrolytic cell with broad cathode tracks on either side of the thin copper traces. The separation between the anode and cathode was 2 mm. Each test piece contained five copper traces and a sixth electrolytic cell where the copper trace was replaced by a standard resistor approximately equal to the measured resistance of the printed traces. Figure 59.2*b* shows the anodic traces connected to a 12-V power supply (V_2) through a current-limiting resistor of 50 kΩ (R_2). The cathodic tracks were powered by a 250-V supply

(V_1) across a 5-kΩ resistor (R_1) used to monitor the SIR of the substrate.

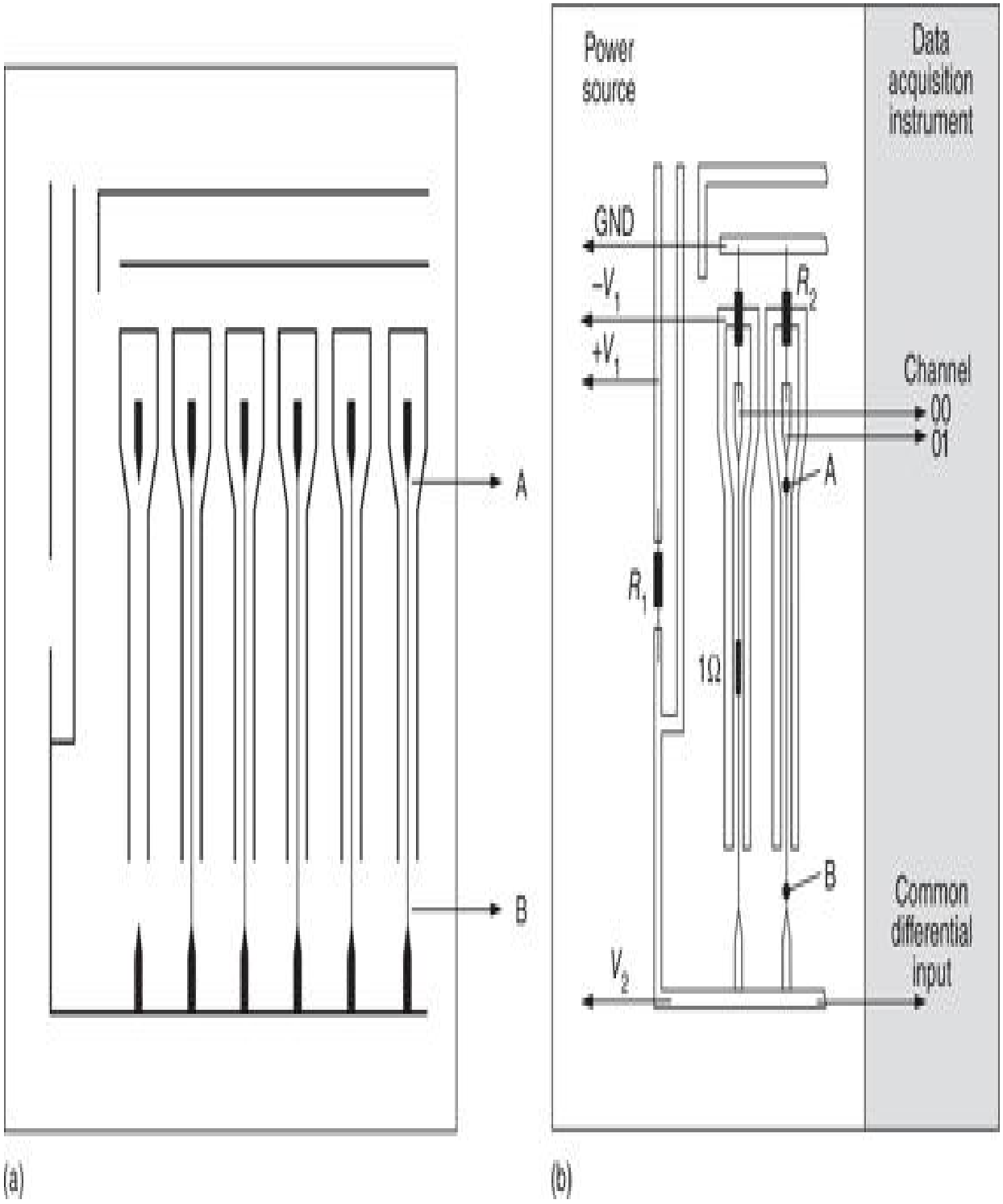


FIGURE 59.2 (*a*) Bono test coupon and (*b*) test configuration for corrosion test with V_1 = 250 V, V_2 = 12 V, R_1 = 5 kΩ and R_2 = 50 kΩ.[2]

The Bono test is designed to indicate the extent of corrosion by measuring the change in resistance of the copper trace over time while being exposed to controlled humidity and a bias voltage. The resistance R_{wire} of the copper trace is given by

$$R_{\text{wire}} = \rho \frac{L}{A} \tag{59.8}$$

where ρ is the resistivity of copper, L is the length of the trace and A is its cross-sectional area.

When corrosion occurs, the cross-sectional area of a trace decreases and R_{wire} increases. By measuring the resistance with respect to time, the extent of the corrosion can be assessed. A time dependent corrosion factor $CF(t)$ is defined as

$$CF(t) = \frac{R_{\text{wire}(t)} - R_{\text{wire}(0)}}{R_{\text{wire}(0)}} \times 100\% \tag{59.9}$$

where $R_{\text{wire}(0)}$ is the initial resistance of the trace and $R_{\text{wire}(t)}$ is its resistance at time t.

Liquid flux was initially used to evaluate the corrosion factor[2]; more recently, the method has been applied to flux-cored solder wire residues, although some parameters of the test coupon were changed.[3] For example, the spacing between anode and cathode in the first study was 2 mm, while it was reduced to 120 µm in the second. Also, the length of the anodic trace was changed from 80 to 145 mm. Other changes in the electrical parameters were even more significant; for example, the direct-current (DC) voltage V_1

applied to polarize the electrolytic cell was decreased from 250 to 20 V. Recently, this test was used to assess the corrosivity of solder paste residues.[4] However, no detailed parameters to define the test parameters were reported. To further develop this test method, it is necessary to precisely define all the parameters of the test method.

The Bono test was modified by Turbini et al.[5,6] to better characterize the effect of soldering flux residues on the metallic circuits of PWBs. Major changes shown in Fig. 59.3 were made to the test coupon. Each coupon consists of a single-sided epoxy glass printed circuit board with five electrolytic cells containing uncoated copper traces. See Figs. 59.2 and 59.3. The spacing between the anode and cathode was set to 0.5 mm to match the spacing on the IPC-B-24 test boards used for SIR testing of soldering fluxes. To enhance the sensitivity of the test, the length of a copper trace was increased by using U-shaped tracks, and its cross-sectional area was reduced through the use of a thinner, 8.6-μm copper film. Turbini et al.[6] also moved the resistors from the test board in the environmental chamber to an external terminal block to eliminate testing inaccuracies related to the high temperature and humidity inside the chamber. Another significant modification was the decrease of V_1 from 250 to 50 V to prevent formation of conductive anodic filaments (CAF), which had been the cause of failure in the original design of Bono, rather than reflecting the actual corrosion factor. Figure 59.4*a* and *b* show schematics of the electrical corrosion circuit of one electrolytic cell in Turbini's tests 1 and 2, respectively. In the case of the circuit for test 1 (Fig. 59.4*a*), breakdown of the insulation resistance of the substrate caused the current I_1 through the copper trace (R_{wire}) to become additive to the current I_2 from the power supply (V_2). Thus, a sensor was added to the circuit to determine whether such breakdown of insulation resistance was affecting the accuracy of the copper trace resistance

measurements shown in the circuit wiring (Fig. 59.4*b*). The direction of the current from the 10-V supply was changed so that any breakdown in the insulation resistance of the 50-V circuit would reduce the resistance value obtained and thereby signal a problem.

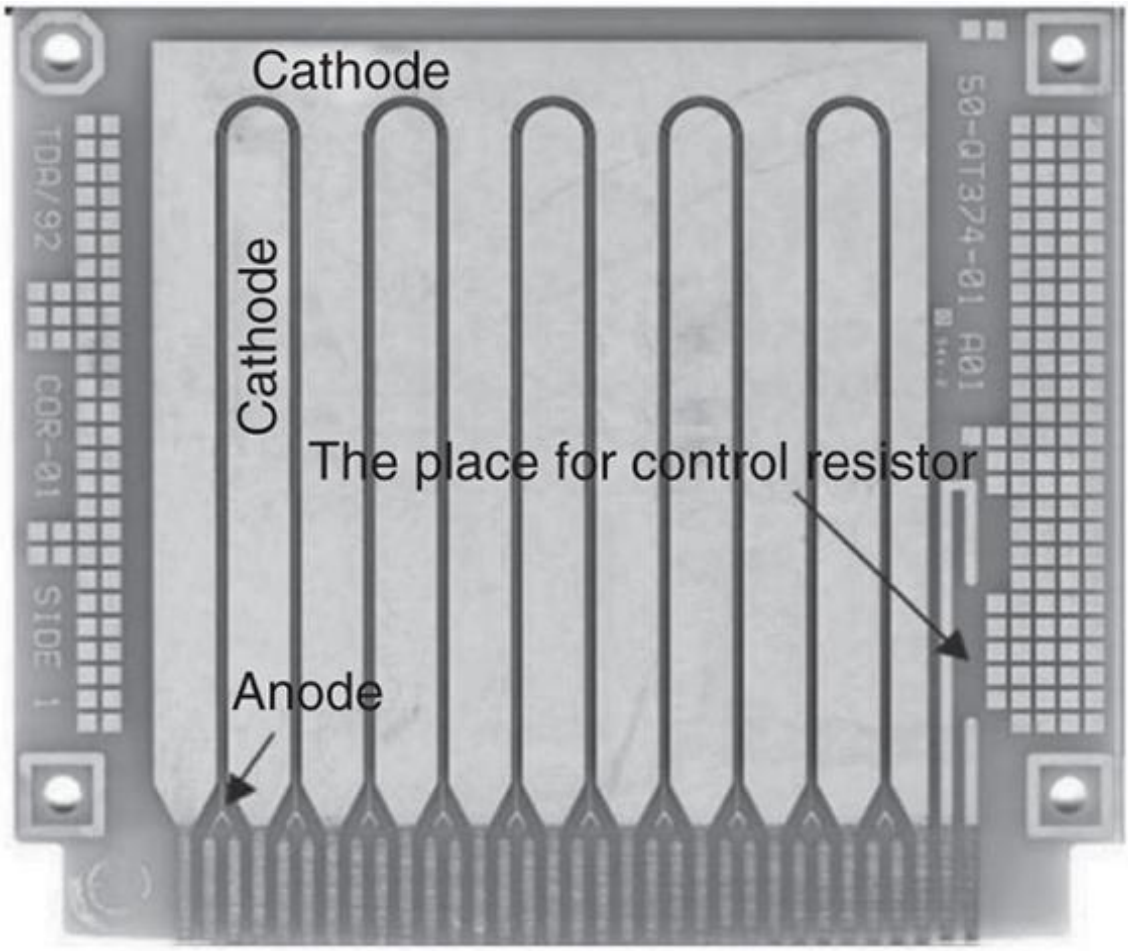


FIGURE 59.3 Schematic of test coupon used by Turbini et al.[6]

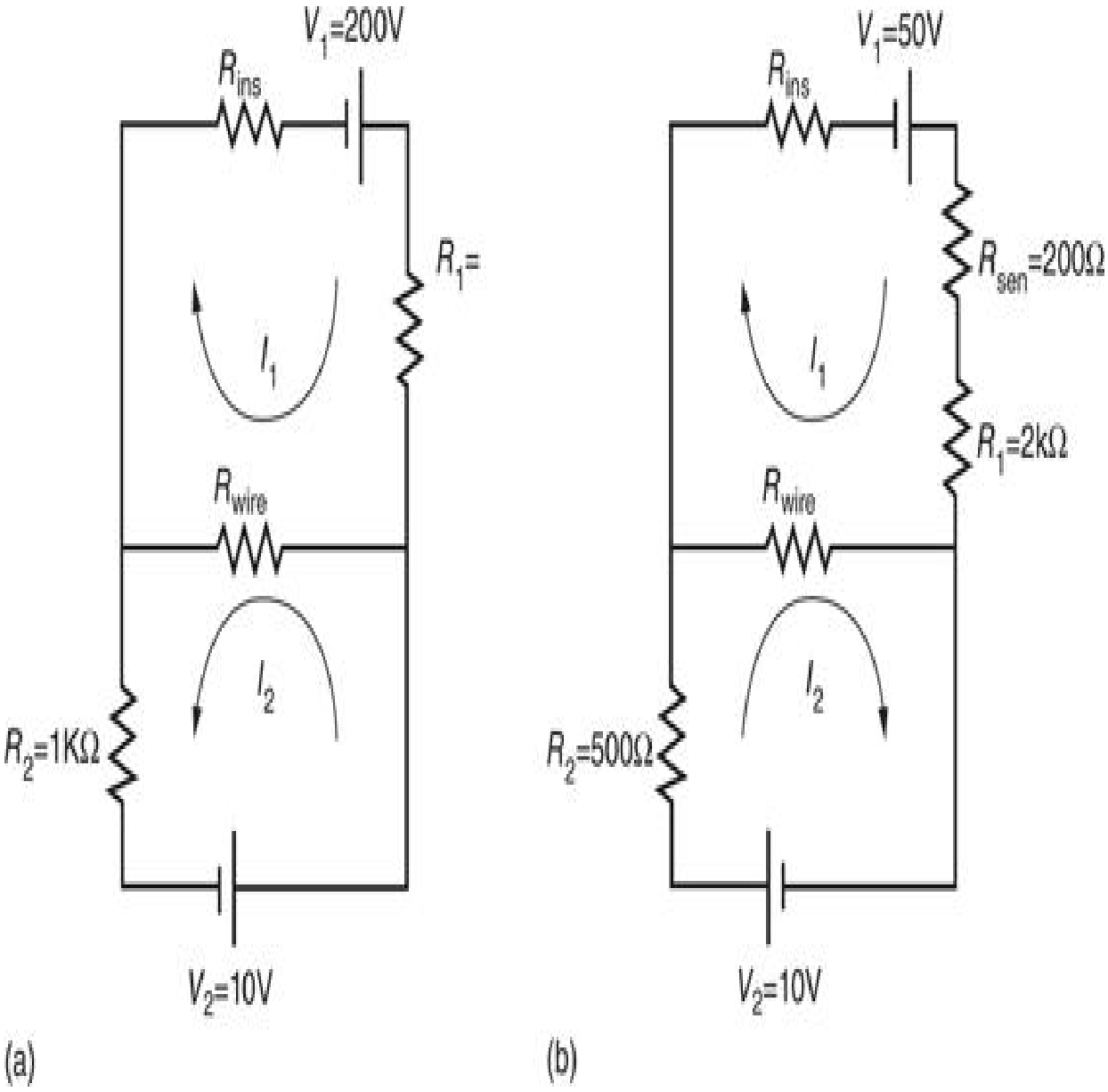
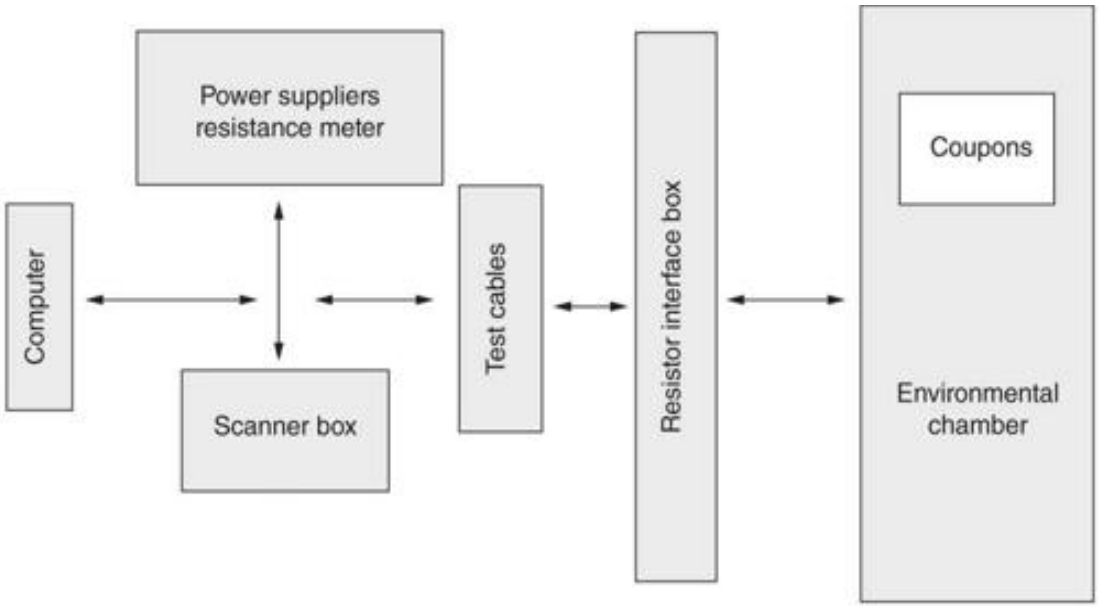


FIGURE 59.4 Electric circuit for an electrolytic cell in (*a*) Turbini test 1[5] and (*b*) Turbini test 2.[6]

Zhou et al.[7] developed a quantitative test method and used it to characterize the corrosion effects of five weak organic acid (WOA) fluxes (abietic acid, succinic acid, glutaric acid, adipic acid, and malic acid) on copper circuits. Experiments were performed under three temperature/humidity conditions (85°C/85 percent RH, 60°C/93 percent RH, and 40°C/93 percent RH) using two

WOA solution concentrations. The extent of corrosion under the various conditions was measured in terms of the %CF value.

Figure 59.5 presents a schematic of the electrical test system. An environmental chamber was used to provide different temperatures and humidities for accelerated aging. A Keithley 2420 source meter provided the precision voltages and currents to measure the resistance of the anodic copper wires. The test cables from the interface box were wired to the scanner box consisting of a Keithley 3706 switching system with a digital multimeter. The resistors (200 Ω and 2 kΩ) used for each test coupon were wired into the resistor interface box. The connectors in this box were standard serial connectors. The electrical wiring of each test coupon is shown in Fig. 59.6.


Power suppliers
resistance meter
Computer
Scanner box
Test cables
Resistor interface box
Coupons
Environmental
chamber

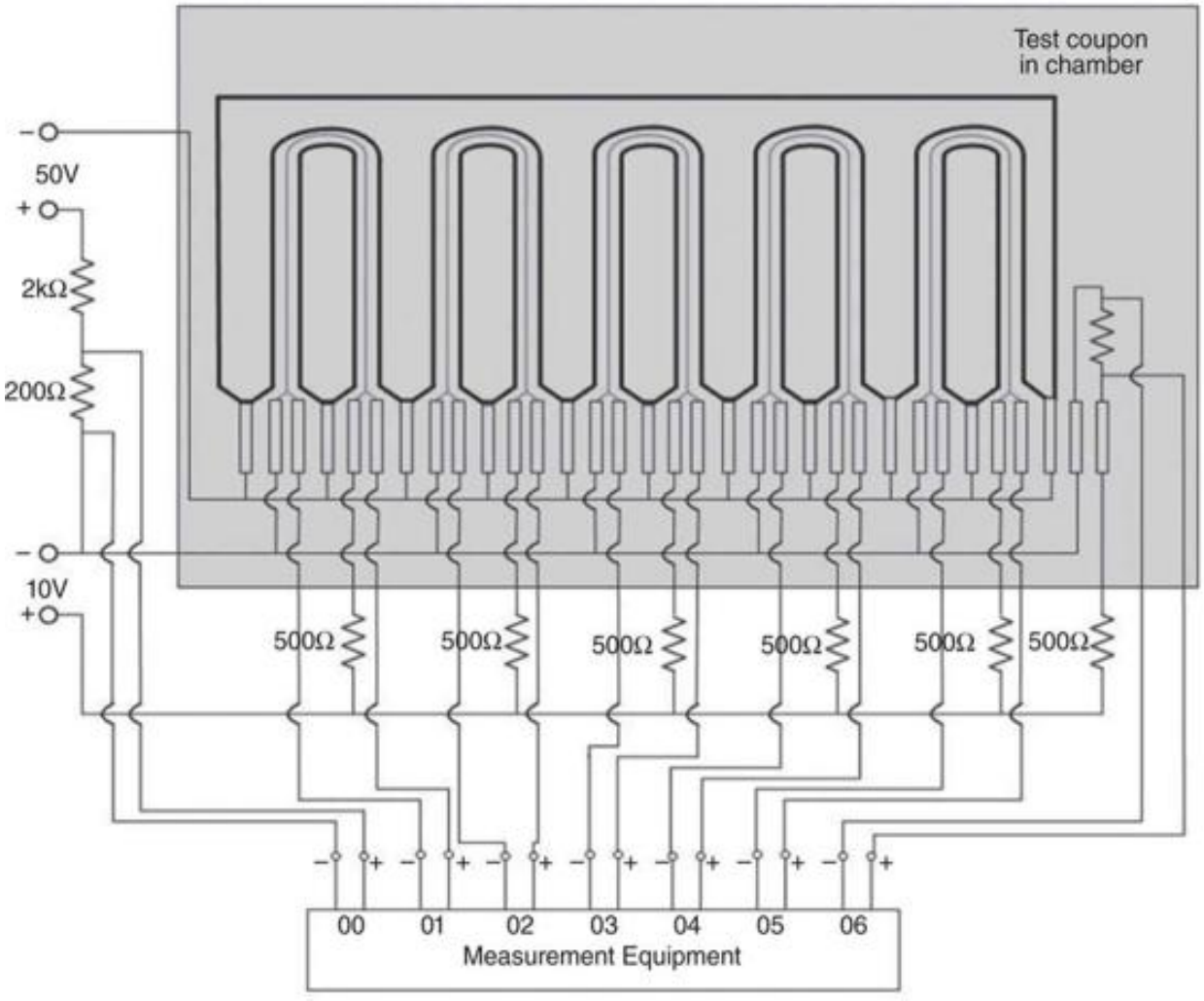
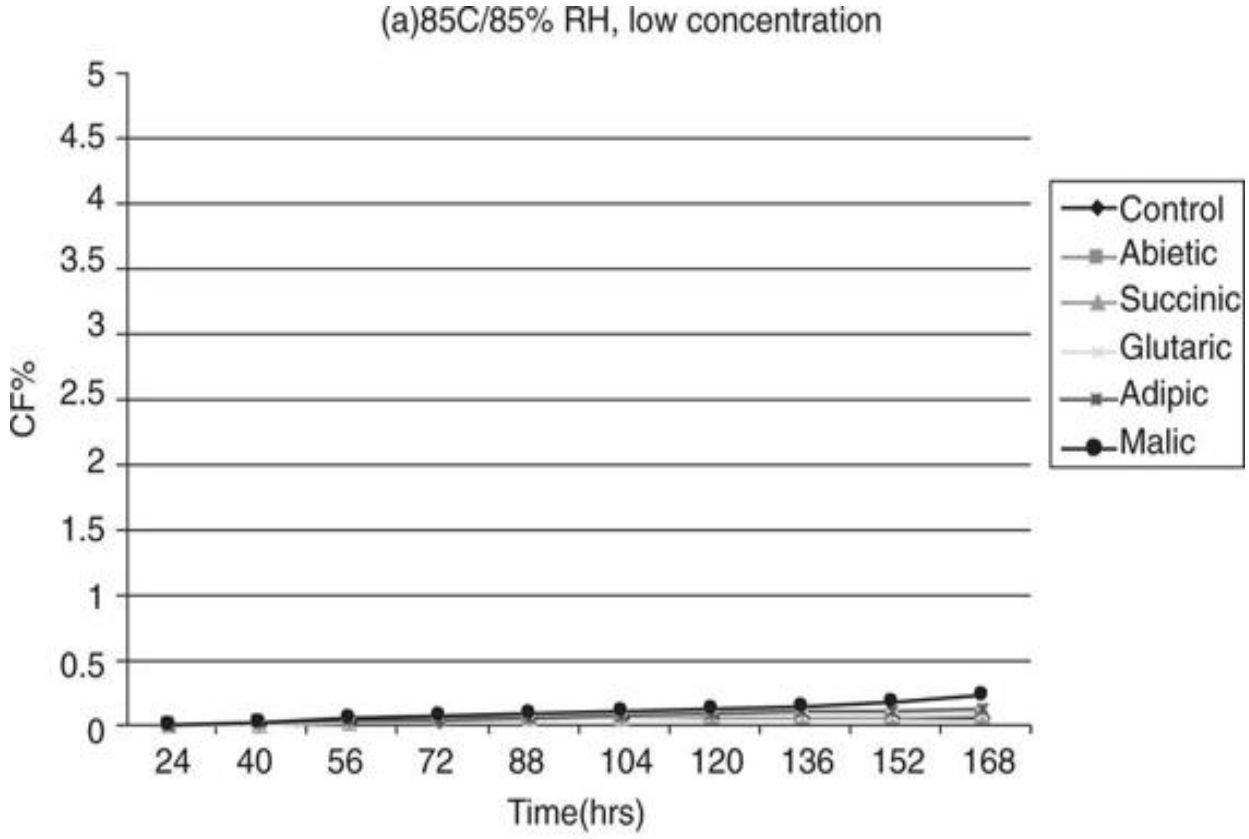

Test coupon
in chamber
50V
2kΩ
200Ω
10V
500Ω
500Ω
500Ω
500Ω
500Ω
500Ω
00
01
02
03
04
05
06
Measurement Equipment

FIGURE 59.5 Schematic of electrical test system.[7]


(a)85C/85% RH, low concentration
CF%
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
24
40
56
72
88
104
120
136
152
168
Time(hrs)
Control
Abietic
Succinic
Glutaric
Adipic
Malic

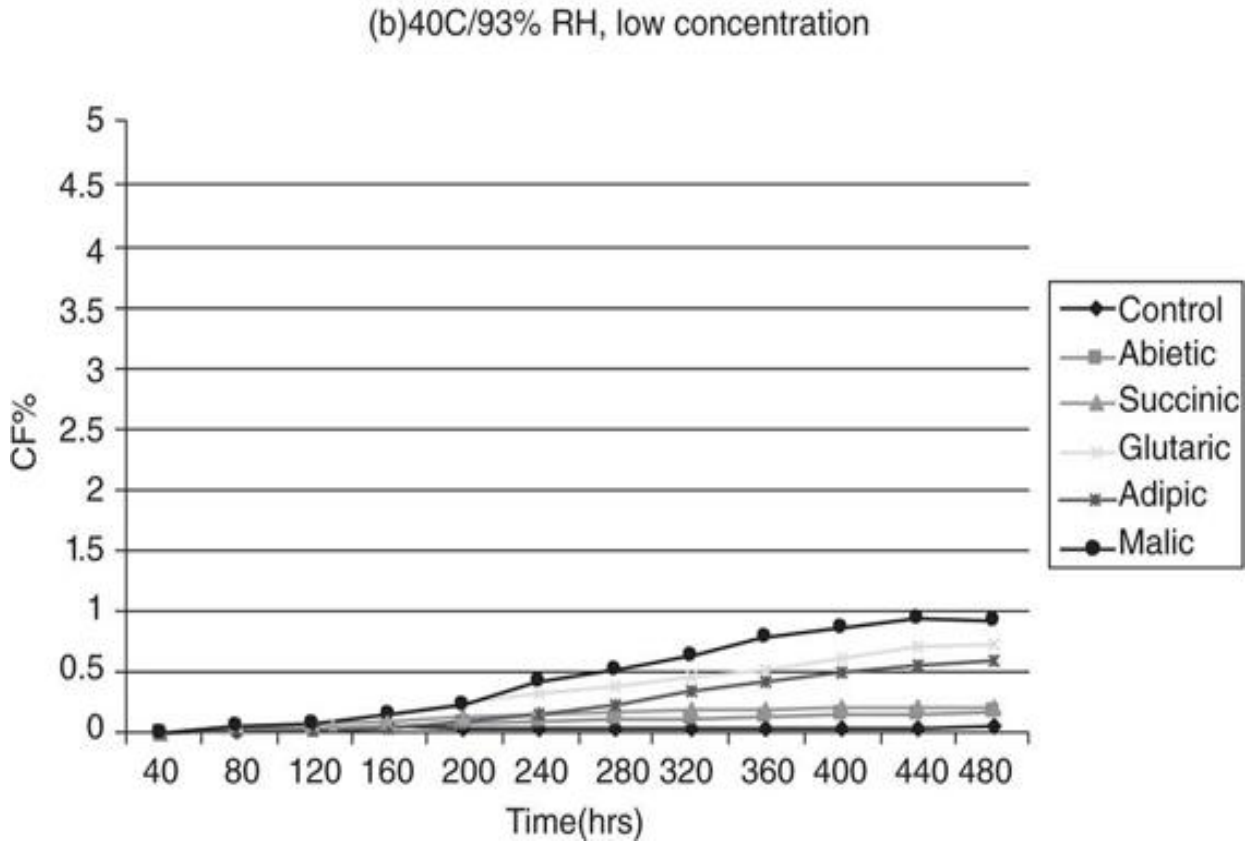

(b)40C/93% RH, low concentration
CF%
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
40
80
120
160
200
240
280
320
360
400
440
480
Time(hrs)
Control
Abietic
Succinic
Glutaric
Adipic
Malic

FIGURE 59.6 Schematic showing electrical wiring of each test coupon.[7]

Five sets of experiments were conducted with solutions containing each WOA at two different concentrations denoted as 1 and 2. In each case, concentration 2 was double concentration 1. The experimental conditions used for each of the five experiments are provided in Table 59.1. The test coupon used is shown in Fig. 59.3. It consisted of a single-sided epoxy glass PWB with five electrolytic cells. The thin uncoated copper traces act as anodes between two broad copper tracks acting as cathodes. The resistance of an anodic copper trace was measured to be approximately 5 Ω.

TABLE 59.1 Experimental Conditions in Tests for Each WOA

Test	Environment (°C, %RH)	Duration	Deposition (x 10^{-4} moles)
1	85°C/85%RH	7 days	4.5
2	40°C/93%RH	20 days	4.5
3	40°C/93%RH	20 days	9.0
4	60°C/93%RH	20 days	4.5
5	60°C/93%RH	20 days	9.0

The test coupons were fluxed and reflowed, allowed to cool and then a standard resistor was soldered to each board for reference. The board was inserted into a card edge connector and placed in an environmental chamber at the desired temperature and humidity conditions. Measurements of the resistance of the anodic traces were taken once equilibrium was reached, after 24 h for the 85°C/85 percent

RH tests and 40 h for the 60°C/93 percent RH and 40°C/93 percent RH tests. When the test had been completed, the coupons were removed from the chamber and examined with an optical microscope.

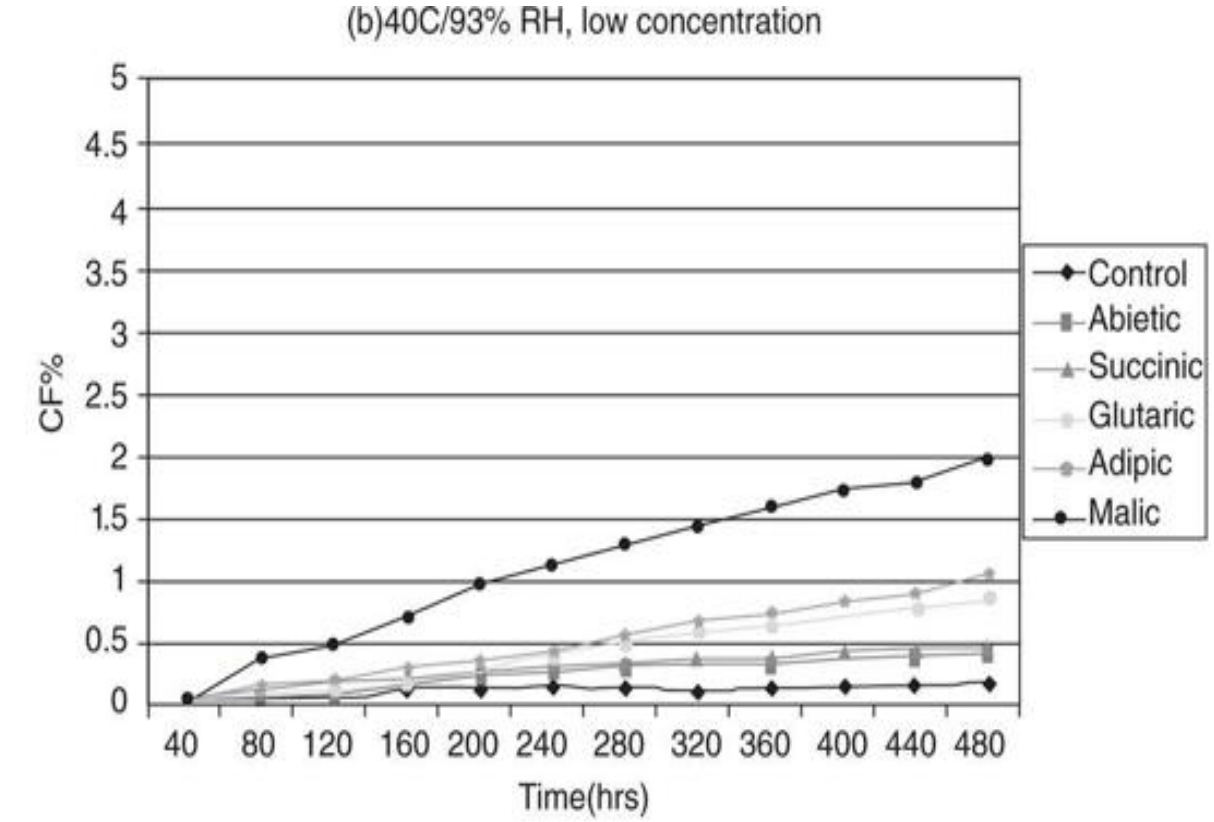
A summary of the final %CF values of each acid under the five test conditions is presented in Table 59.2. This table and subsequent plots present the average and standard deviation of the final CF values measured on the ten copper traces on two test coupons exposed to each acid. Figure 59.7*a* shows the evolution of %CF over the course of test 1 at the experimental conditions of 85°C/85 percent RH with the lower flux concentration. As shown in Table 59.2, all of the CF values remained below 0.2 percent, indicating no significant corrosion of the PWB copper traces. This result is expected because almost all the WOA depositions would have evaporated or decomposed at 85°C, as noted by Christian[8] and Tellefsen.[9] All the test boards were clean with no visible residues, except for a color change of the copper metal where the WOA had been applied. The results of test 2, conducted under conditions of 40°C/93 percent RH at low WOA concentration for 20 days, are shown in Fig. 59.7*b*. Clear evidence of corrosion which varied among the fluxes tested was observed in this case. Small amounts of unevenly distributed blue and green residues appeared on the anodic tracks on boards exposed to malic acid.

TABLE 59.2 Summary of Final CF Values for Each Acid in Tests 1 to 5

WOA	Test 1 85°C 85% RH 1x[a] (%)	Test 2 40°C 93% RH 1x (%)	Test 3 40°C 93% RH 2x[a] (%)	Test 4 60°C 93% RH 1x (%)	Test 5 60°C 93% RH 2x (%)
Abietic	0.1 ± 0.0	0.2 ± 0.0	1.5 ± 0.1	0.4 ± 0.2	1.6 ± 0.2
Succinic	0.1 ± 0.0	0.2 ± 0.1	2.0 ± 0.2	0.5 ± 0.2	2.1 ± 0.3
Glutaric	0.1 ± 0.0	0.7 ± 0.1	3.6 ± 0.2	0.8 ± 0.2	4.3 ± 0.4
Adipic	0.1 ± 0.0	0.6 ± 0.1	3.4 ± 0.3	1.1 ± 0.4	3.7 ± 0.4
Malic	0.2 ± 0.0	0.9 ± 0.1	6.9 ± 0.4	2.0 ± 0.4	8.7 ± 2.3[b]

[a]1x represents concentration 1, and 2x represents concentration 2

[b]This average value was taken from CF values of nine traces as one trace was broken.


(b)40C/93% RH, low concentration
CF%
Time(hrs)
Control
Abietic
Succinic
Glutaric
Adipic
Malic

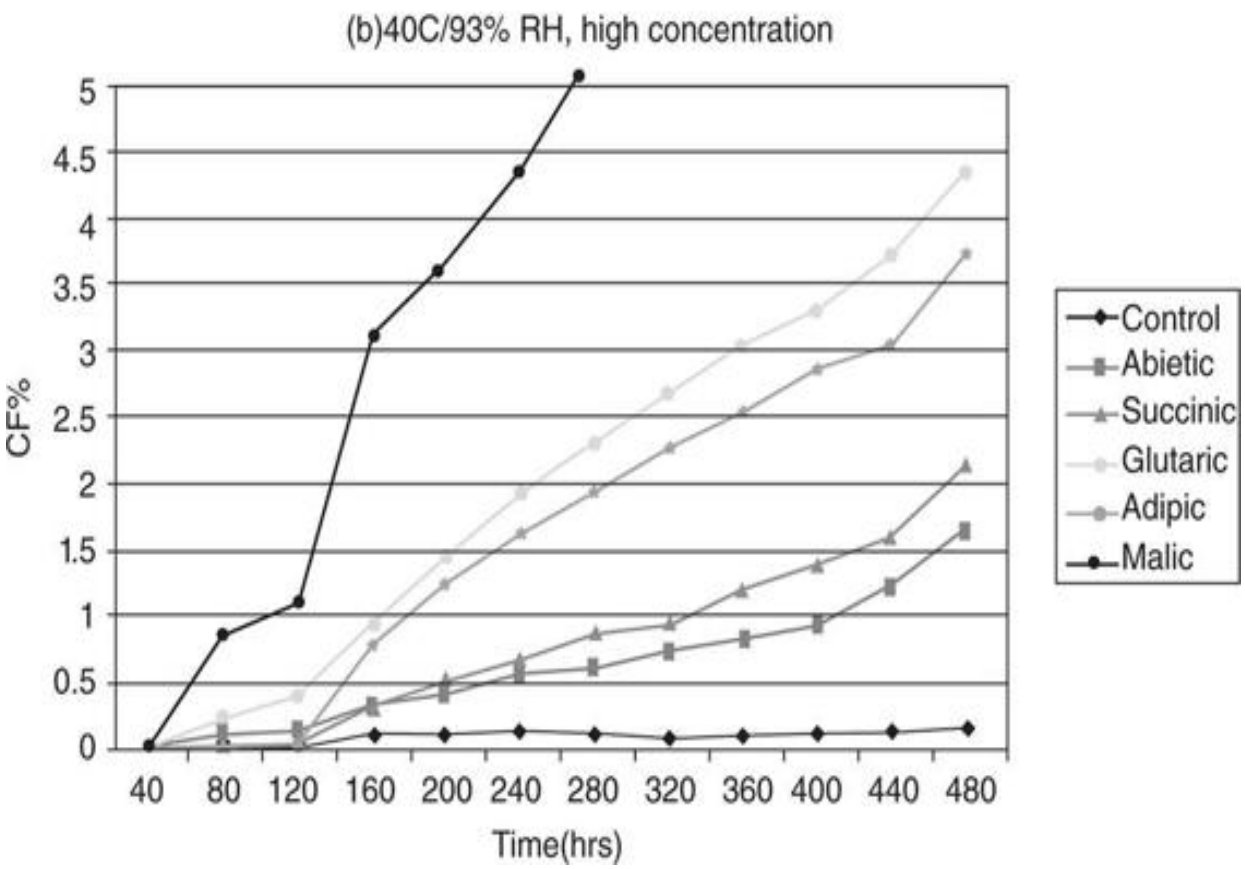

(b)40C/93% RH, high concentration
CF%
Time(hrs)
Control
Abietic
Succinic
Glutaric
Adipic
Malic

FIGURE 59.7 Evolution of %CF values during the course of (*a*) test 1, (*b*) test 2, (*c*) test 4, and (*d*) test 5.[7]

The WOA solution concentration during test 3 was double that used during tests 1 and 2, with the other accelerating conditions (40°C/93 percent RH) maintained the same. It was easy to observe dark-green residues on the copper traces of the malic acid flux at the end of the experiment, as well as long copper dendrites. It was observed that the %CF values obtained in test 3 compared with those measured in test 2 reveal the very strong effect of WOA concentration on copper corrosion. Test 4 was conducted under the condition of 60°C/93 percent RH at low WOA concentration for 20 days. Except for temperature, all other conditions were identical to those in test 2. As shown in Table 59.2 and Fig. 59.7*c*, the corrosion factors for each acid were greater than those obtained in test 2 but less than those measured in test 3; no dendrites were identified on any coupon at the end of test 4. Test 5 was conducted at high WOA concentration, intermediate temperature (60°C), and high RH (93 percent) for 20 days (Fig. 59.7*d*). The coupon exposed to malic acid showed excess green residues over most of its surface. The %CF values among the fluxes tested were easily distinguishable from one another under these test conditions and were also higher than those measured during any other test. The corrosivity of the WOAs was found to increase in the following order: abietic acid < succinic acid < adipic acid ~ glutaric acid < malic acid, which agrees with that of SIR measurements reported in the literature.[10]

The CF values at 60°C were greater than the values at 40°C, which were greater than the values at 85°C. This suggests that a temperature of 40°C is not high enough to enhance the rate of corrosion. At 60°C, corrosion likely occurs faster than the evaporation and/or thermal decomposition of the WOA. Thus, the results clearly show that this is the best temperature for distinguishing the

corrosion effects of the different WOAs. Consequently, T/H conditions of 60°C/93 percent RH are the recommended stress conditions for corrosion testing. Although the original tests at 60°C were conducted for 20 days, it is clear from the data that a testing duration of 10 days should be sufficient to easily distinguish between the %CF values obtained for the various WOAs.

59.4 UNDERSTANDING CAF FORMATION

In the mid-1970s, Bell Labs' researchers were concerned about potential failures of printed wiring boards intended for high-voltage switching applications. They reported[11,12] on accelerated life testing of flexible PWBs coated with ultraviolet (UV)-cured resin, and identified two new failure modes: conductive bridges between conductors on the surface, and conductive shorts through the substrate.

AT&T Bell Labs' test vehicle (see Fig. 59.8) was a flexible epoxy glass PWB, 0.005 to 0.007 in thick with comb patterns of 0.008 in lines and 0.009 in spaces. Some combs were biased on the surface and some were biased through the substrate. Processed boards, coated with conformal coating, were tested from 35 to 95°C, 25 to 95 percent relative humidity (RH), and direct current (DC) voltages up to 400 V. For accelerated testing at 85°C, 80 percent RH, and 78 V bias, failures occurred within 2 to 5 days.

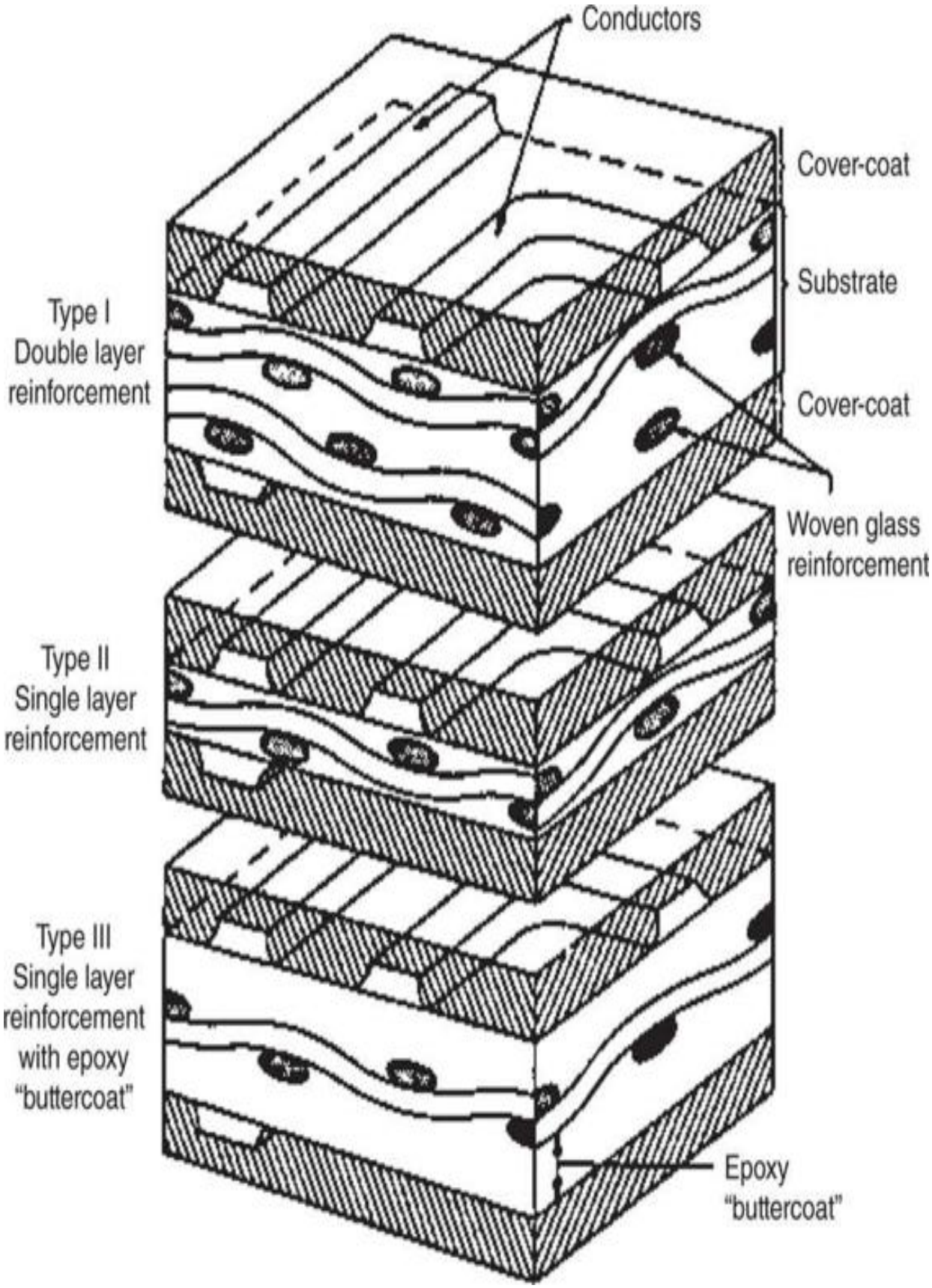

Conductors
Cover-coat
Substrate
Cover-coat
Woven glass reinforcement
Type I
Double layer
reinforcement
Type II
Single layer
reinforcement
Type III
Single layer
reinforcement
with epoxy
"buttercoat"
Epoxy
"buttercoat"

FIGURE 59.8 AT&T test vehicle compared (*a*) double layer glass reinforcement, (*b*) single layer glass reinforcement, and (*c*) single layer glass reinforcement with extra "buttercoat."[11] (© 1976 IEEE.)

Bell Labs identified two major failure modes that they described as causing "catastrophic loss of insulation resistance due to the formation of conductive bridges between conductors." The first failure mode—*through-substrate shorts*—only occurred above 75°C and 85 percent RH and thus was not considered to be a problem at use conditions (see Fig. 59.9).[11]

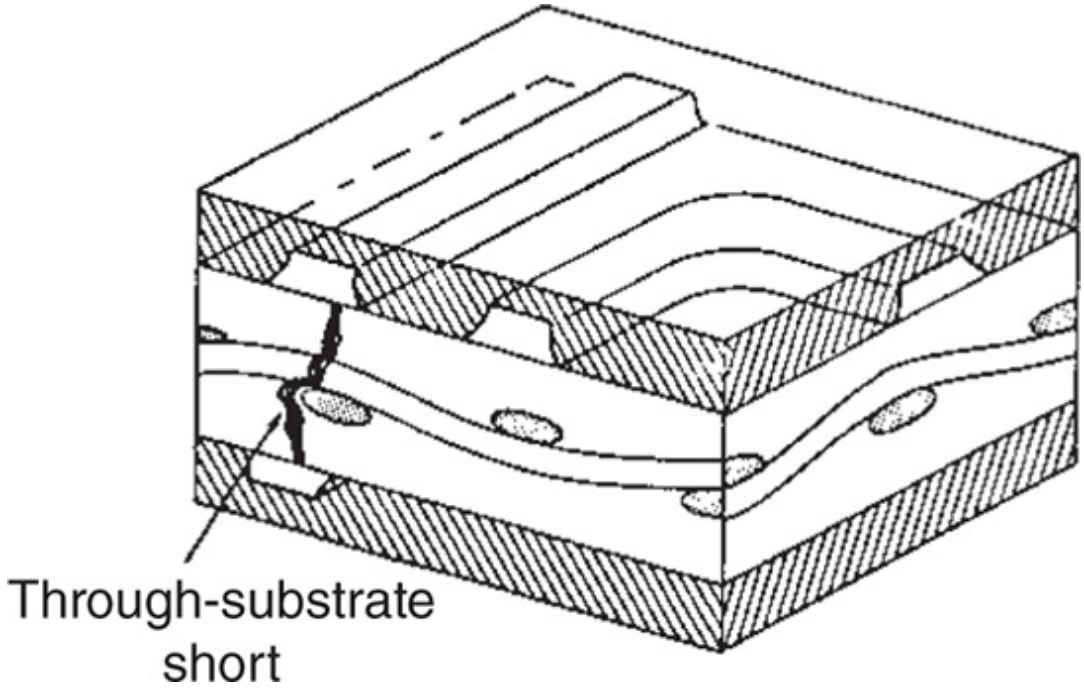


FIGURE 59.9 Through-substrate short.[11] (© 1976 IEEE.)

The second mode involved shorts between conductors on the same side of the board in which conductive material accumulates between the glass bundles and the epoxy (see Fig. 59.10). R. H. Delaney and J. N. Lahti[12] noted that the thicker the buttercoat, the less this failure was observed. They also detected a failure, which they termed *anodic eruption failure mode*, in which corrosion products emerged

from the anode to the covercoat surface, charring the surface, and then growing back through the covercoat to the cathode, where it shorted (see Fig. 59.11).

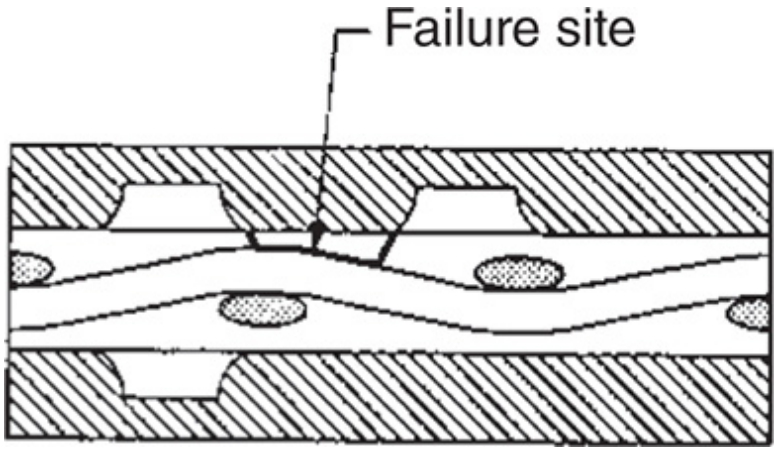
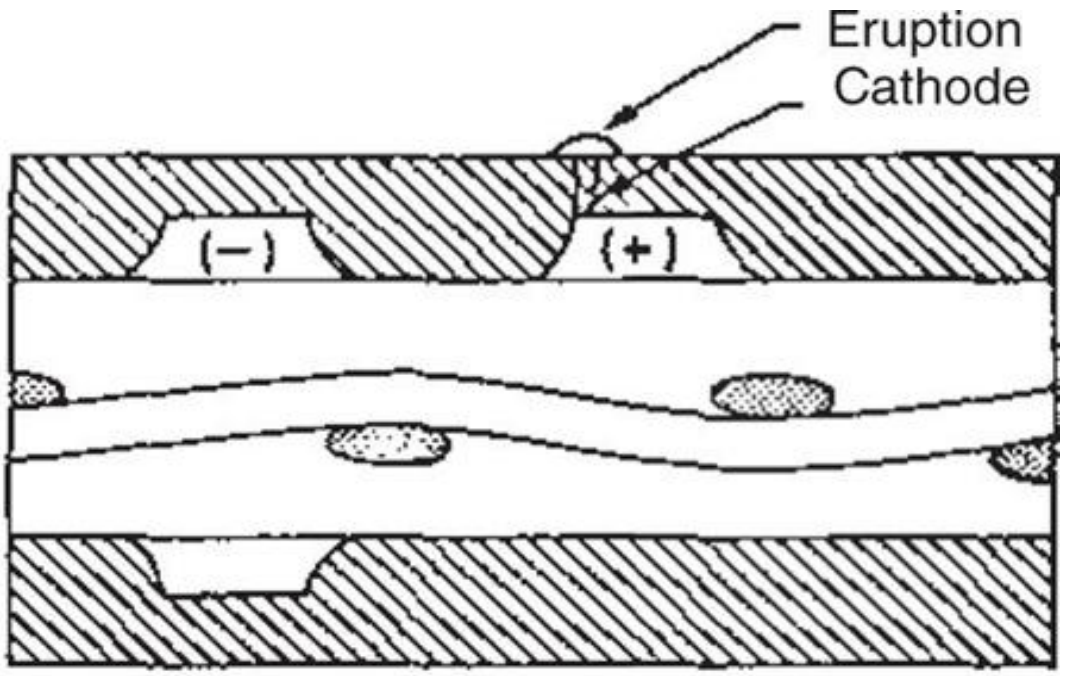
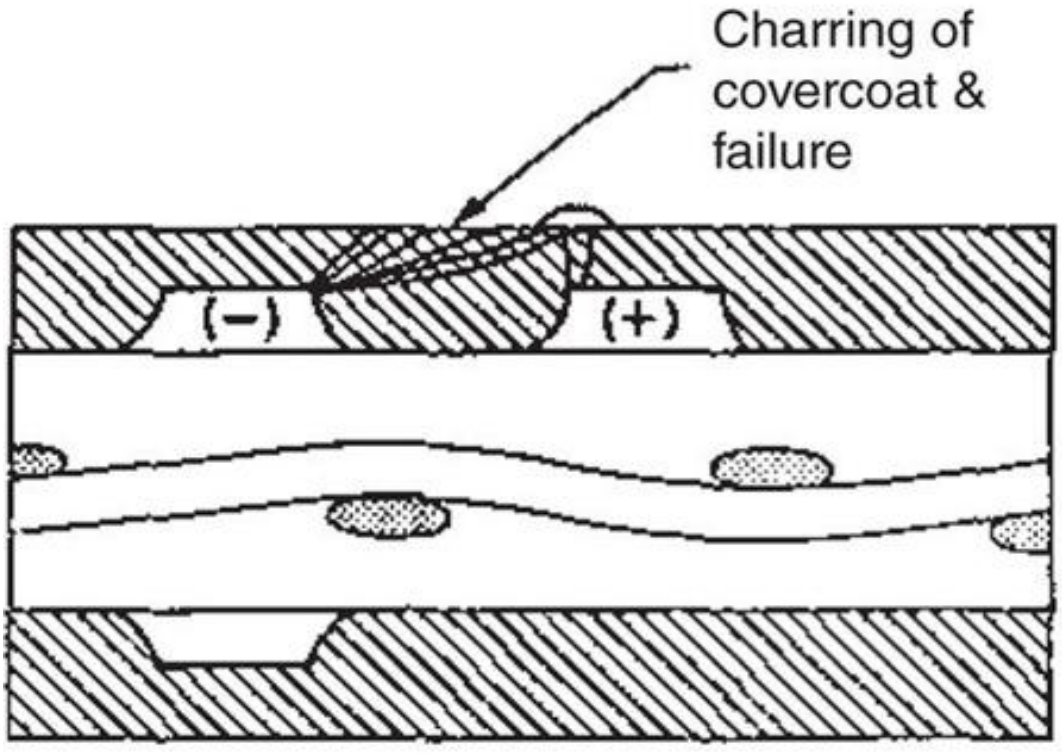


FIGURE 59.10 Subsurface substrate failure.[11] (© 1976 IEEE.)



Early stage



Late stage

FIGURE 59.11 Anodic eruption failure mode.[11] (© 1976 IEEE.)

In 1976, Der Marderosian at Raytheon, while studying measling, crazing, and delamination, examined the reliability of multilayer PWBs by applying a DC voltage between ground planes and conductor traces (see Fig. 59.12).[13] Test coupons were biased at 100 V and aged at 65°C and 95 percent RH for 10 days. Based on the results, Der Marderosian reported a failure that he termed the “punch thru” phenomenon. This is similar to the “thru substrate shorts” reported by Delaney.[12] To study this failure further, Der Marderosian obtained test coupons from three different vendors biasing some at 100 V DC, others at 100 V AC, and a third group was unbiased. Since “punch thru” was observed only when DC bias was applied, Der Marderosian concluded that this failure was due to electrochemically initiated metal migration. He reported that the number of incidents of “punch thru” decreased as aging voltage was decreased. The addition of a urethane conformal coating appeared to accelerate, not suppress, the problem.

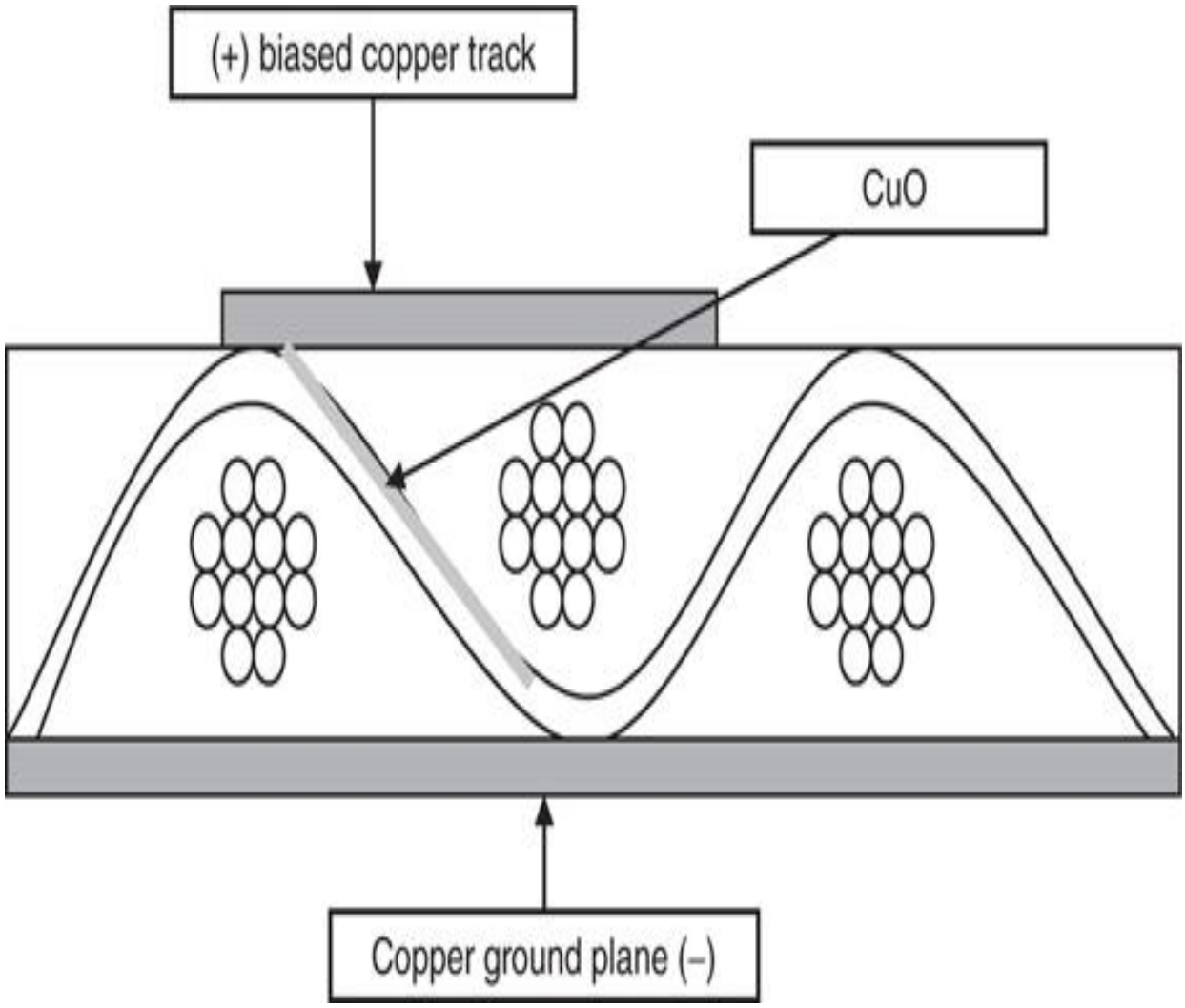


FIGURE 59.12 Raytheon test coupon with “punch thru” from anode trace to copper ground plane.[13]

“Punch thru” is an electrical failure that eventually manifests itself in a rupture of the insulation between two layers of copper metallization. In the early stages, Der Marderosian observed conductive copper-containing deposits that he assumed were CuO along the glass fibers. Eventually these deposits shorted to the cathode, carbonizing the epoxy causing it to be more conductive. Epoxy blowout then ruptured the glass fibers. In the later stages, Der Marderosian observed melting of the copper traces.

Equation (59.10) represents Der Marderosian's concept of the production of CuO and $Cu(OH)_2$ at the anode. At the cathode, reduction takes place yielding copper and hydrogen gas. He noted that copper hydroxide decomposes to copper oxide above 60°C.

$$3Cu + 3H_2O = CuO + Cu(OH)_2 + 2H_2 + Cu \qquad (59.10)$$

Lando et al.[14] first used the term conductive anodic filament (CAF) to describe this failure in 1979. They defined the mechanism of CAF formation as a two-step process: degradation of the epoxy/glass interface, followed by the electrochemical reaction [see Eq. (59.10)].

$$\begin{aligned} &\textit{Anode:} && Cu = Cu^{n+} + ne^- \\ & && H_2O = \tfrac{1}{2}O_2 + 2H + 2e^- \\ &\textit{Cathode:} && 2H_2O + 2e^- = H_2 + 2OH^- \\ & && H_2O + \tfrac{1}{2}O_2 + 2e^- = 2OH^- \\ & && Cu^{n+} + ne^- = Cu \end{aligned} \qquad (59.11)$$

In 1980, T. L. Welsher et al.[15] reported that CAF was potentially a serious reliability problem for closely spaced conductors and proposed a mean time to failure (MTTF) based on Eq. (59.11):

$$MTTF = a(H)^b \exp(E_a/RT) + d(L^2/V) \qquad (59.12)$$

where H = humidity
E_a = activation energy
R = gas constant
T = temperature in Kelvin
L = conductor spacing
V = voltage
a, b, Ea, d = material dependent

Welsher et al.[15] noted that additional work was needed to determine the exact dependence of CAF on conductor spacing and humidity. They also reported that glass-reinforced triazine is CAF-resistant.

In 1980, they expanded their view of the MTTF and reported it as shown in Eq. (59.13):

$$\mathrm{MTTF} = \alpha\left(1+\beta\frac{L^n}{V}\right)\cdot H^{\gamma}\exp\frac{E_a}{kT} \tag{59.13}$$

where α, β = material-dependent constants
γ = humidity-dependent constant
n = related to the orientation of the conductors
L = spacing
V = voltage
H = humidity
E_a = activation energy
k = Boltzmann's constant
T = temperature in kelvins

Ready and Turbini[13] studied the effect of voltage and spacing on CAF failures for a hole-to-hole test pattern (see Fig. 59.13). Using two different spacings (0.50 and 0.75 mm) and two different bias voltages (150 and 200 V), they were able to show the relation is L^4/V^2 [see Eq. (59.14)]:

$$\text{MTTF} = C \exp(E_a/kT) + d(L^4/V^2) \tag{59.14}$$

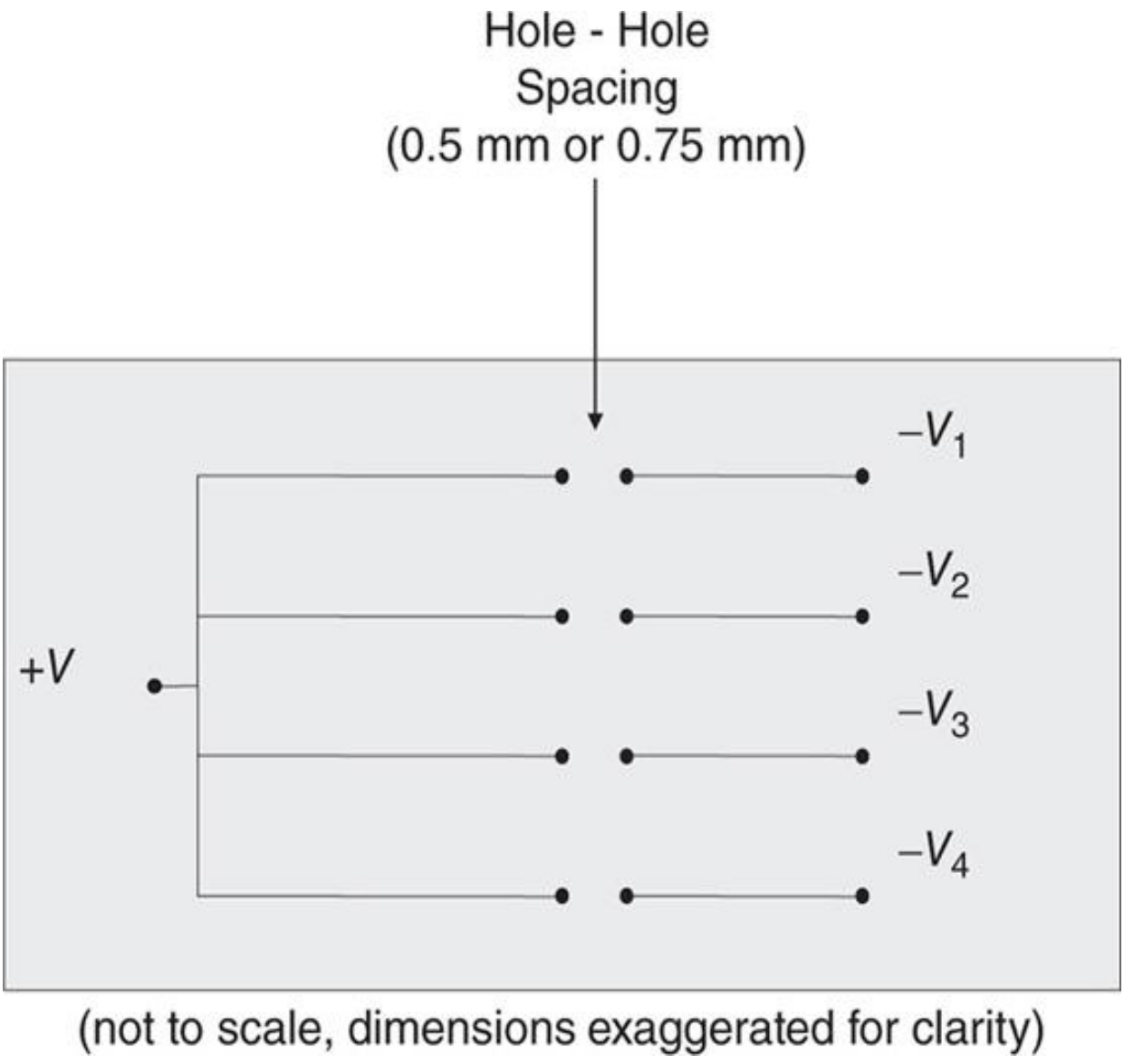


FIGURE 59.13 Hole-to-hole test vehicle used by Ready et al.[16]

59.4.1 CAF Formation

In the case of CAF formation, copper ions are created electrochemically at the anode. Residual chloride ions from the reaction of epichlorohydrin with Bisphenol A (forming a precursor to the epoxy) exist at low levels in the FR-4 substrate. These react with the copper ions and later water to produce the CAF[16]—$Cu_2(OH)_3Cl^-$, which grows from the anode since it is insoluble in acid. The favored path for this is at the epoxy glass interface.

Ready and Turbini[16] identified the chemical nature of CAF as atacamite: $Cu_2(OH)_3Cl$. An examination of the Pourbaix[17] diagram (see Fig. 59.14) for the copper-chlorine-water system reveals that copper hydroxy chloride is insoluble below pH4 and thus this salt will grow from the anode, which is acidic. They also explained that the high conductivity of this salt, which causes catastrophic failure when it bridges to the cathode, suggests that it conducts through electrons and holes, that is, it has semiconductor properties. CAF filaments are typically no larger than 50 μm in diameter and 0.2 mm in length.

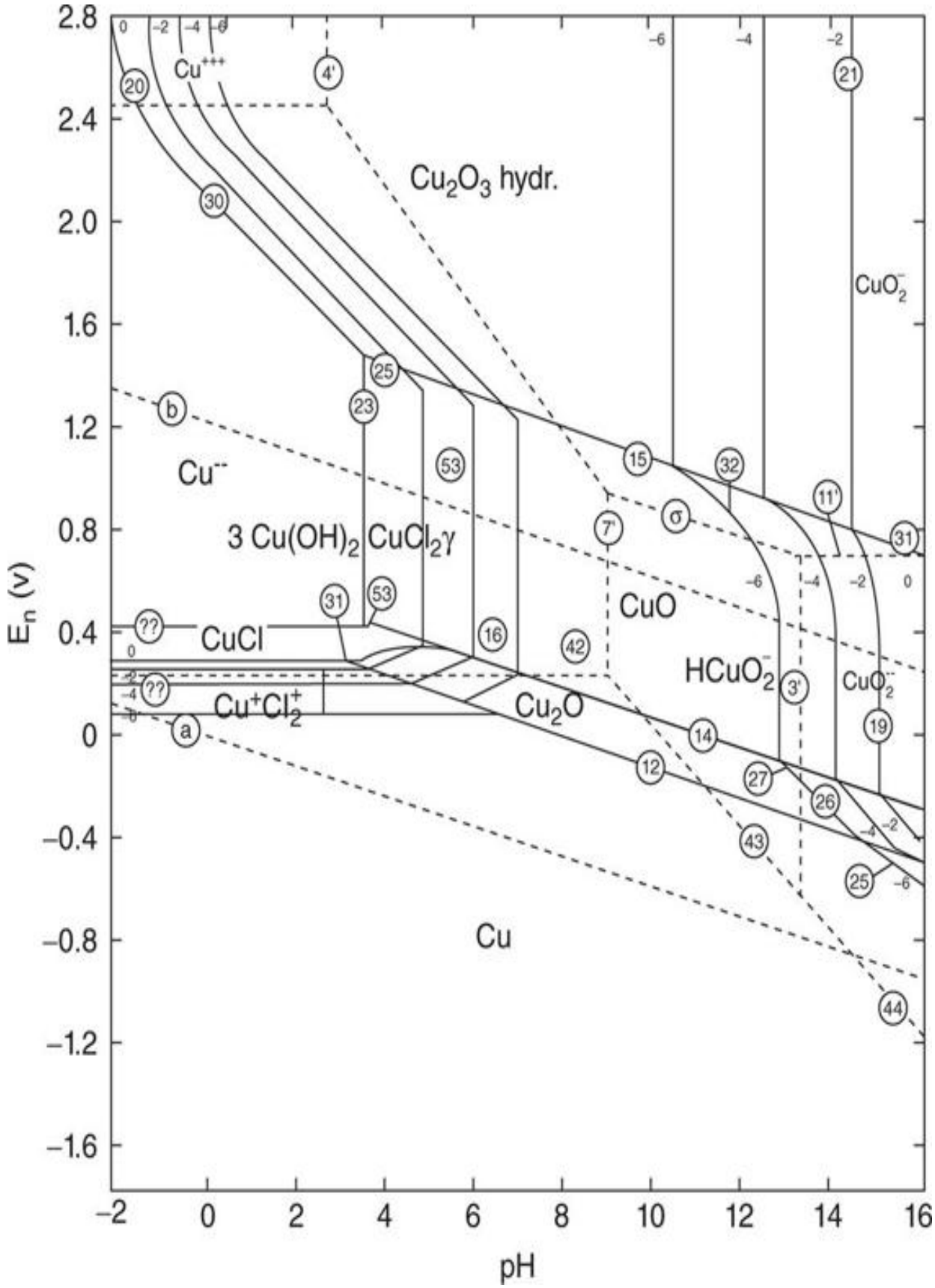

E_n (v)
pH
Cu^{+++}
Cu_2O_3 hydr.
Cu^{++}
$3\,Cu(OH)_2\,CuCl_2\gamma$
CuCl
$Cu^+Cl_2^+$
Cu_2O
CuO
$HCuO_2^-$
CuO_2^{--}
CuO_2^-
Cu

FIGURE 59.14 Pourbaix diagram of the copper-chlorine-water system.[17]

59.5 FACTORS THAT AFFECT CAF FORMATION

A number of factors affect CAF formation. These include substrate material, conductor configuration, processing, voltage and spacing, soldering flux, and humidity in the storage and use environment.

59.5.1 Substrate Material

Lando et al.[14] compared FR-4 with several substrates: G-10 (a non-fire-retardant epoxy/woven glass material), polyimide/woven glass (PI), triazine/woven glass, epoxy/woven kevlar, and finally polyester/woven and chopped glass. Similarly, B. Rudra et al.[18] performed an extensive experimental comparison among the substrates: bismaleimide triazine (BT), cyanate esters (CE), and FR-4. In addition, Ready[19] compared the CAF susceptibilities of FR-4 with CEM-3 (a substrate similar to G-10 except with chopped glass) and MC-2 (a blended polyester and epoxy matrix with woven glass face sheets and a chopped glass core). Of all materials tested by these investigators, the BT material proved to be most resistant to CAF formation (due to its low moisture absorption characteristics). Conversely, the MC-2 substrate proved to have the least resistance to CAF formation. The susceptibility of the materials follows the trend below:

MC-2 > Epoxy/Kevlar > FR-4 ~ PI > G-10 > CEM-3 > CE > BT

To ensure immunity to CAF, the laminate of preference is BT. In recent years, laminate suppliers have developed other CAF-resistant substrate materials. However, there is a cost penalty to consider.

59.5.1.1 Conductor Configuration. Lando et al.[14] evaluated several different conductor configurations:

Hole-to-line (H-L)
Hole-to-hole (H-H)

This evaluation showed that susceptibility to CAF is H-H > H-L > L-L. Lahti et al.[20] demonstrated that the smaller the spacing between conductors and the greater the proximity of the glass fibers to the copper conductors, the faster the growth of CAF. They noted that for a multilayer board, failure initiated in the most deeply buried layers.

59.5.2 Processing

The epoxy glass bond can be weakened by the drilling or depaneling processes in PWB manufacture. It will also be weakened during the soldering process due to the difference in coefficient of thermal expansion (CTE) of the epoxy and glass. Data from Turbini et al.[21] demonstrated that the increased soldering temperature associated with lead-free alloys significantly increases the incidence of CAF.

Another processing factor is the diffusion of polyglycols from water-soluble flux into the PWB substrate that occurs during soldering. Since the diffusion rate is temperature-dependent, the length of time that the board is above the glass transition temperature will affect the amount of polyglycol absorbed into the epoxy, and that will in turn affect its electrical properties. J. A. Jachim et al.[22] reported on water-soluble flux-treated test coupons that were

prepared using two different thermal profiles. Those which experienced the higher thermal profile exhibited a surface insulation resistance (SIR) level that was an order of magnitude lower than those processed under less aggressive thermal conditions.

59.5.2.1 Voltage and Spacing. Two other critical factors used in determining CAF susceptibility are voltage and spacing. The CAF growth is fueled by the electric field (*V/d*), and failure occurs more quickly with smaller spacing between conductors.

59.5.3 Effect of Soldering Flux

It has been shown that polyglycols[22] (which are found in water-soluble fluxes) diffuse into the epoxy during soldering. This absorption has been shown to reduce electrical performance by increasing moisture uptake by the substrate.[23] Jachim et al.[24] were the first to link the use of polyglycols in soldering fluxes and fusing fluids to increased susceptibility to CAF formation.

Ready et al.[25] showed that the use of certain water-soluble fluxes or fusing [hot air solder level (HASL)] fluids could increase CAF formation. In examining a catastrophic field failure (see Fig. 59.15), they demonstrated the presence of a copper-bromide containing salt between an inner layer power plane and ground pin, separated by 0.005 in. Using a test coupon manufactured in the same lot as the failed product, they extracted the flux residues from an inner layer of the multilayer board and used ion chromatography to match the residues from the board's inner layer with the constituents of the flux.

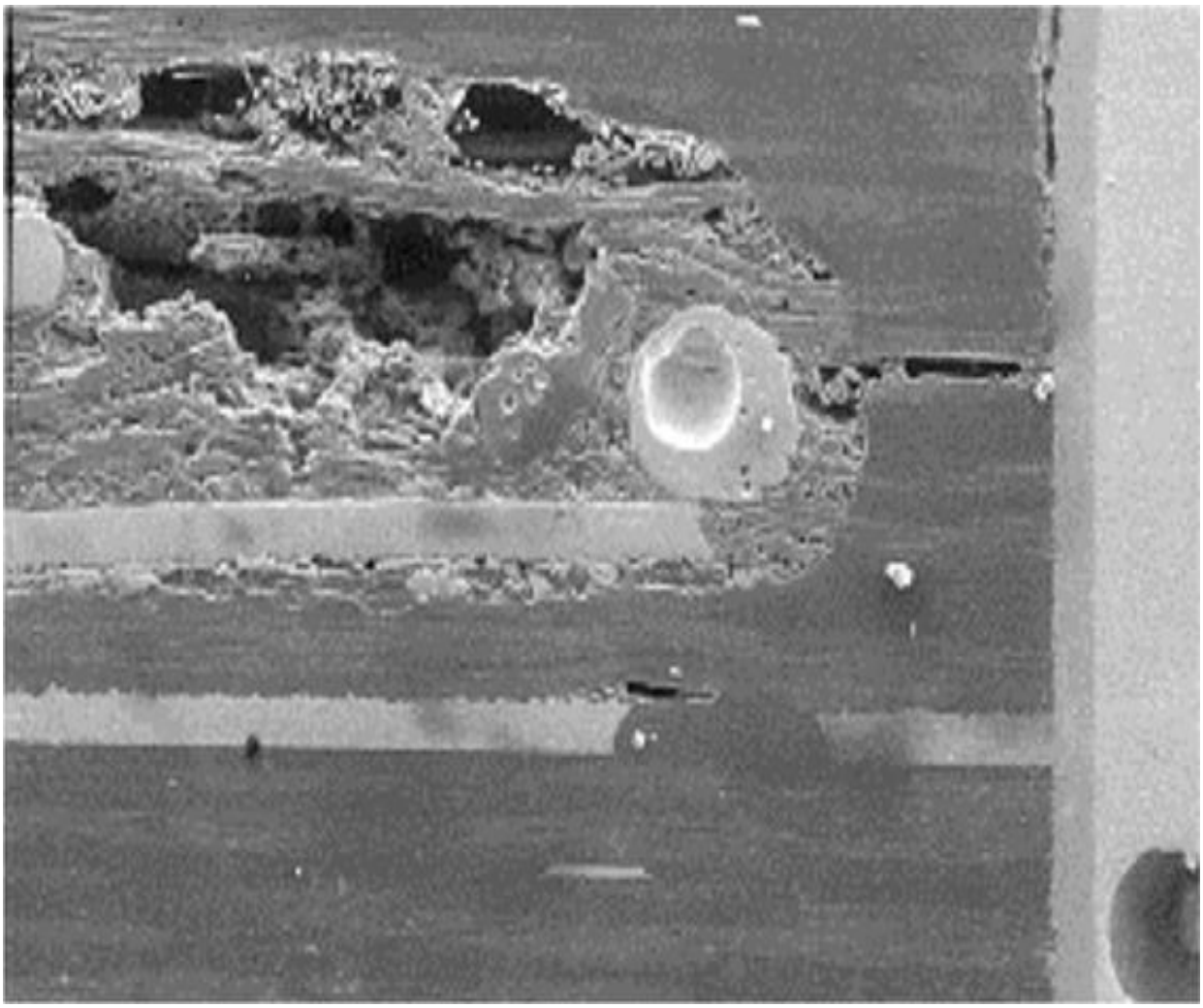


FIGURE 59.15 Catastrophic field failure of military hardware. The conductive filament grew from the +20 V ground plane to the −20 V ground pin. Flux residues enhanced this failure rate.[25]

59.5.4 Humidity in the PWB Storage and Use Environment

J. A. Augis et al.[26] determined that there is a humidity threshold below which CAF formation will not occur. They found that this relative humidity threshold depends on operating voltage and temperature. It is important to remember that this relative humidity need not be present in the operating environment. Moisture absorption can occur

during any part of the assembly's lifetime. This is particularly critical during transportation or storage, when the assembly may experience harsh environmental conditions.

59.5.4.1 Determining the Chemistry of CAF Formation. It was noted that the morphology of CAF appeared different when certain fluxes are used.[16] In Fig. 59.16*a*, when no flux is used, CAF forms only as a crystalline filament at the epoxy glass interface; in Fig. 59.16*b*, the flux contained polyethylene propylene glycol (1800) and there appears to be a copper-containing compound in stratified layers within the matrix in addition to the filament at the epoxy-glass interface; and in Fig. 59.16*c*, the flux contained a linear aliphatic polyether and one sees a copper-containing compound appearing in a striated morphology as well as the crystalline filament at the interface. The analysis of the copper containing compound in the epoxy matrix leads to a complete description of the chemistry of CAF formation in the works of Caputo, et al.[27–29]

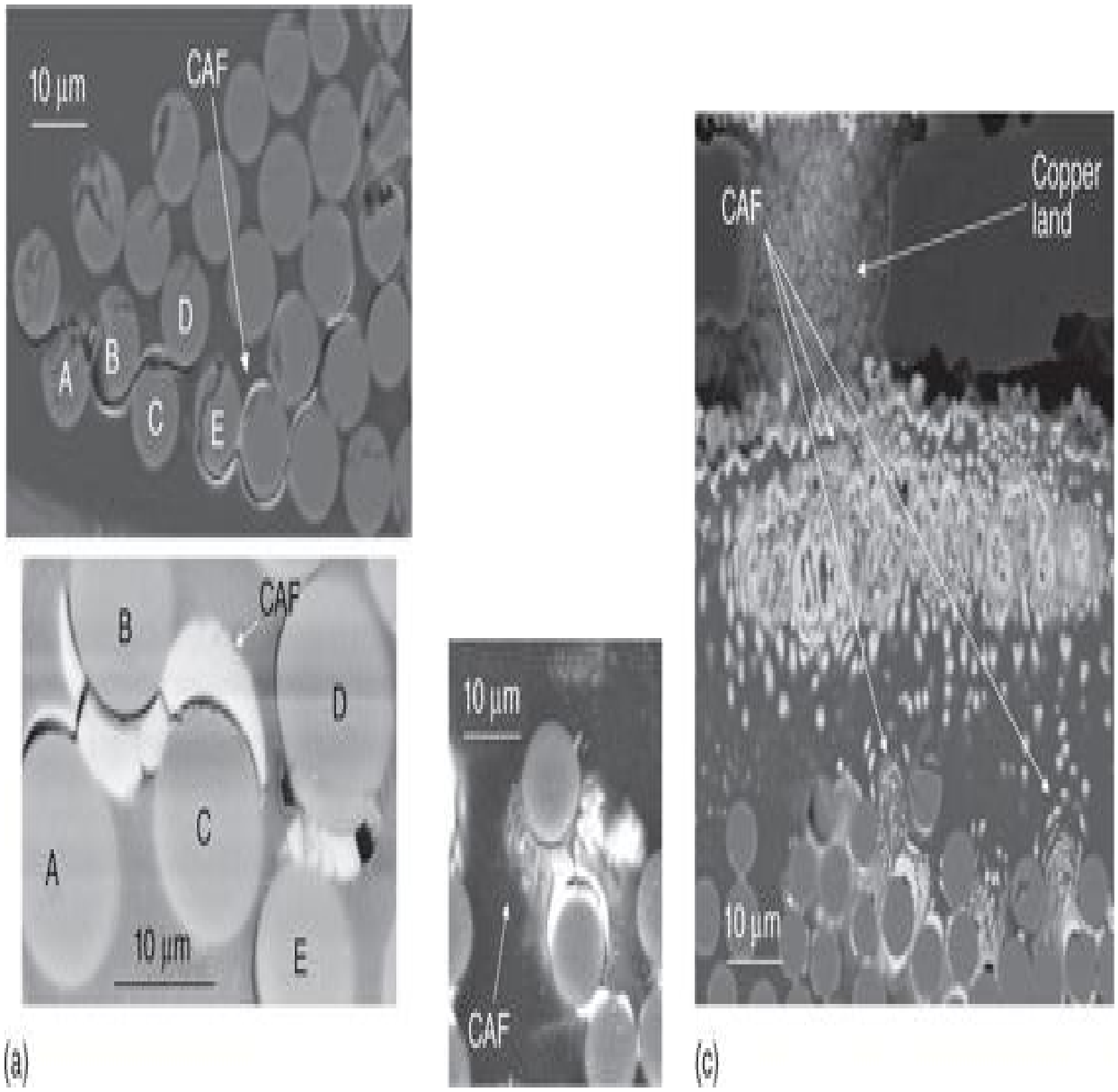


FIGURE 59.16 Morphology of CAF differs when different flux constituents are used: (*a*) CAF only at the glass epoxy interface, (*b*) copper-containing compound in stratified layer plus CAF.[16]

59.5.5 Chloride CAF

While CAF is normally found in the inner layers of multilayer boards, earlier work used single or double sided PWB in studying it since CAF can be visible as a shadow growing from the anode (Fig. 59.17).

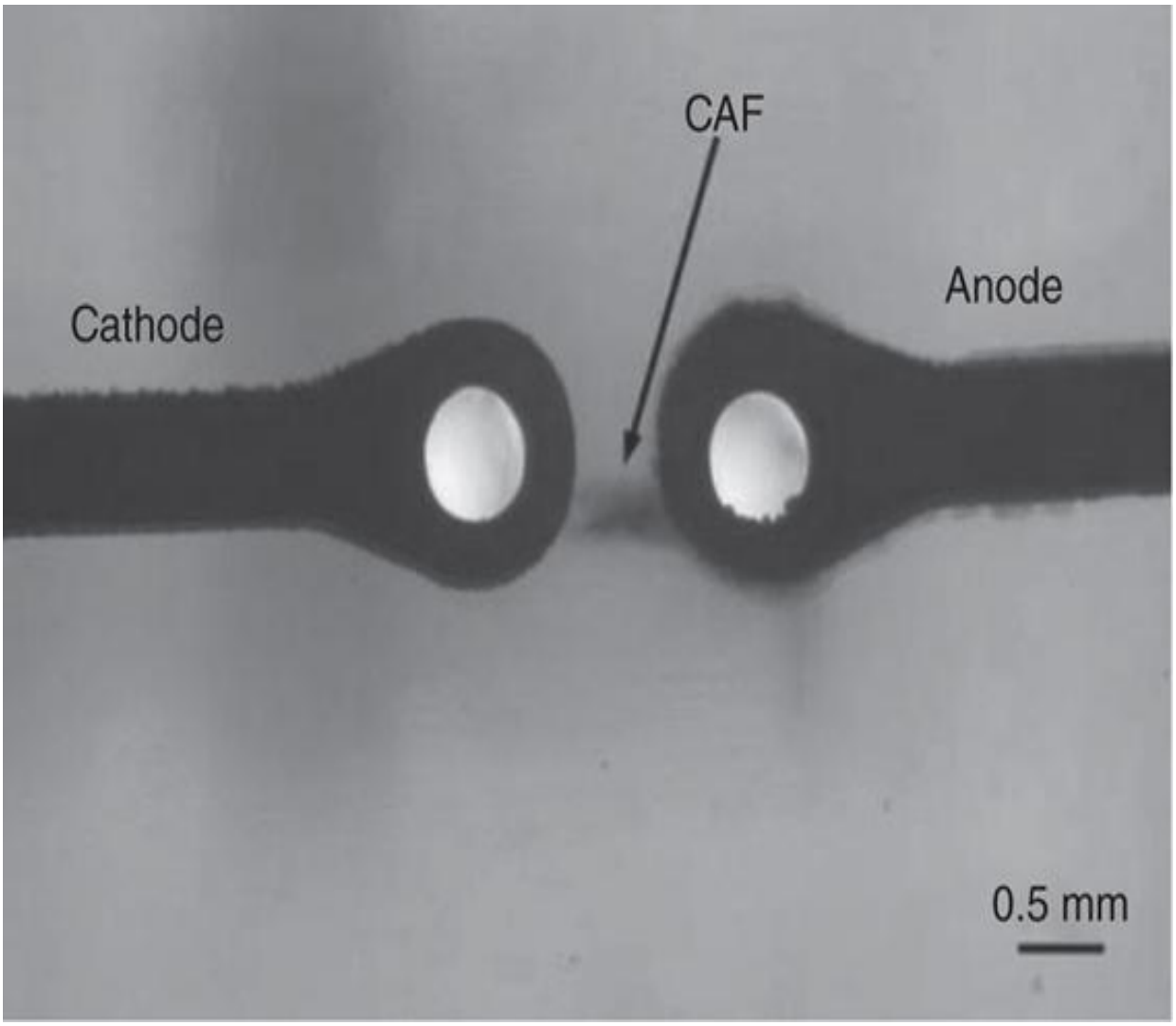


FIGURE 59.17 Typical backlighting image of CAF.[27]

In the case of CAF formation, copper ions are created electrochemically at the anode. Residual chloride ions from the reaction of epichlorohydrin with bisphenol A (forming a precursor to the epoxy) exist at low levels in the FR-4 substrate. These react with the copper ions and water to produce the CAF—$Cu_2(OH)_3Cl$—which grows from the anode since it is insoluble in acid. The favored path for this growth is at the epoxy glass interface. An SEM/EDS image of a cross-section of a board processed with polyethylene propylene glycol (PEPG) flux reveals that the compound within the polymer matrix contains copper and chlorine (Fig. 59.18).

XPS was used to identify the compound as Cu^{+1} and Cl^{-1} by matching the binding energies for the copper and the chloride. Based on CuCl being the copper compound in the polymer matrix, the following mechanism for CAF formation is proposed to occur at the anode (Eq. 59.15):

Attack of copper with chloride

$$Cu + Cl^- \leftrightarrow CuCl + 1e^-$$

Generation of oxygen and hydrogen ions

$$2H_2O \rightarrow O_2 + 4H^+ + 4e^- \qquad (59.15)$$

CAF formation

$$12\ CuCl + 3O_2 + 6H_2O \rightarrow 4Cu_2(OH)_3Cl + 4Cu^{2+} + 8Cl^-$$

The Pourbaix diagram for the copper, chlorine, water system (Fig. 59.14) shows that $Cu_2(OH)_3Cl$ (CAF) is insoluble below pH4 and thus begins to grow from the anode.

59.5.6 Bromide CAF

Ready et al.[16,25] also demonstrated that the halide content affects the chemical nature of the CAF. When coupons are processed with either no flux or flux containing 2 wt.% chloride or 2 wt.% bromide, CAF contains both copper and chlorine. When flux containing 15 wt.% bromide was used, Ready et al.[25] found that bromide-containing CAF could be created. To verify this and to analyze the cause of the bromine-containing CAF, Caputo[29] processed test boards (Fig. 59.13) with the high bromide flux which caused the catastrophic field failure described above (see Table 59.3) The boards were reflowed between 240 and 245°C either 1 or 2 times and cleaned. After accelerated aging of the boards

at 85°C/85 percent RH using +200 V bias and +100 V test for 28 days, coupons were cross-sections. SEM/EDS analysis was used to show that the CAF contained Cu and Br (Fig. 59.19) and that the residues in the polymer matrix also contained Cu and Br (Fig. 59.20). TEM analysis of the CAF sample produced x-ray diffraction patterns matching $Cu_2(OH)_3Br$. The Pourbaix diagram[30] (Fig. 59.21) of the copper, bromide, water system shows that $Cu_2(OH)_3Br$ is insoluble below pH 7.

TABLE 59.3 Extraction of Chloride and Bromide from Fluxed and Control Coupons

	$Cl^{-1}(\mu g/cm^2)^a$	$Br^-(\mu g/cm^2)^a$
Control	0.51	0.07
One reflow with HASL fluid	0.35	7.9
Two reflows with HASL fluid	0.23	4.2

[a]Ion chromatography analysis for as-received HASL flux: Cl^- (3.69×10^4 µg/l) and Br^- (1.959×10^7 µg/l).

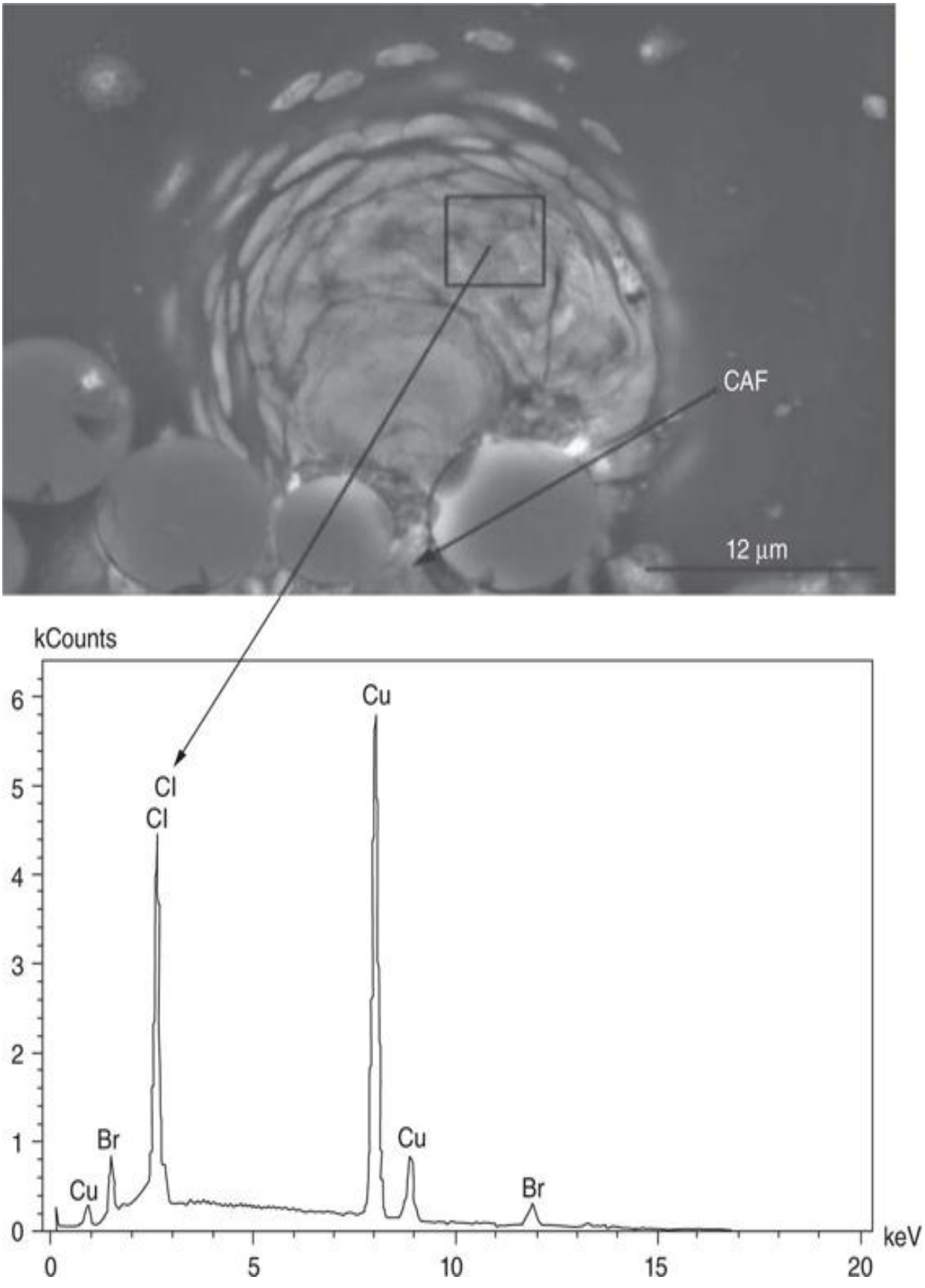

CAF
12 µm
kCounts
6
5
4
3
2
1
0
Cu
Cl
Cl
Br
Cu
Cu
Br
0
5
10
15
20
keV

FIGURE 59.18 SEM and EDS spectra of the copper-chloride-containing compound found in the matrix for coupons processed with PEPG. The Br peaks come from the brominated epoxy substrate.[28]

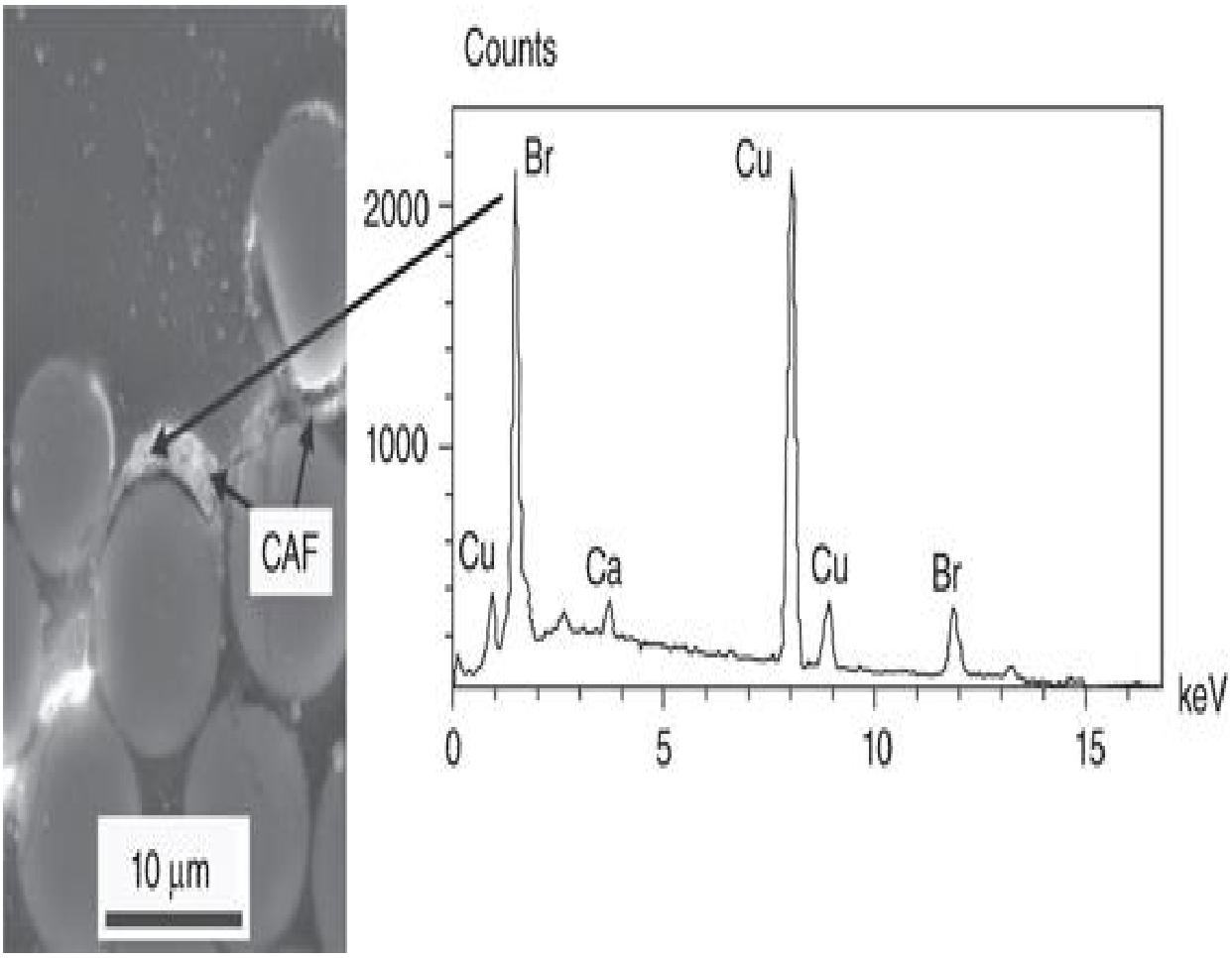


FIGURE 59.19 Image showing bromide CAF and spot EDS analysis for a HASL-processed coupon.[29]

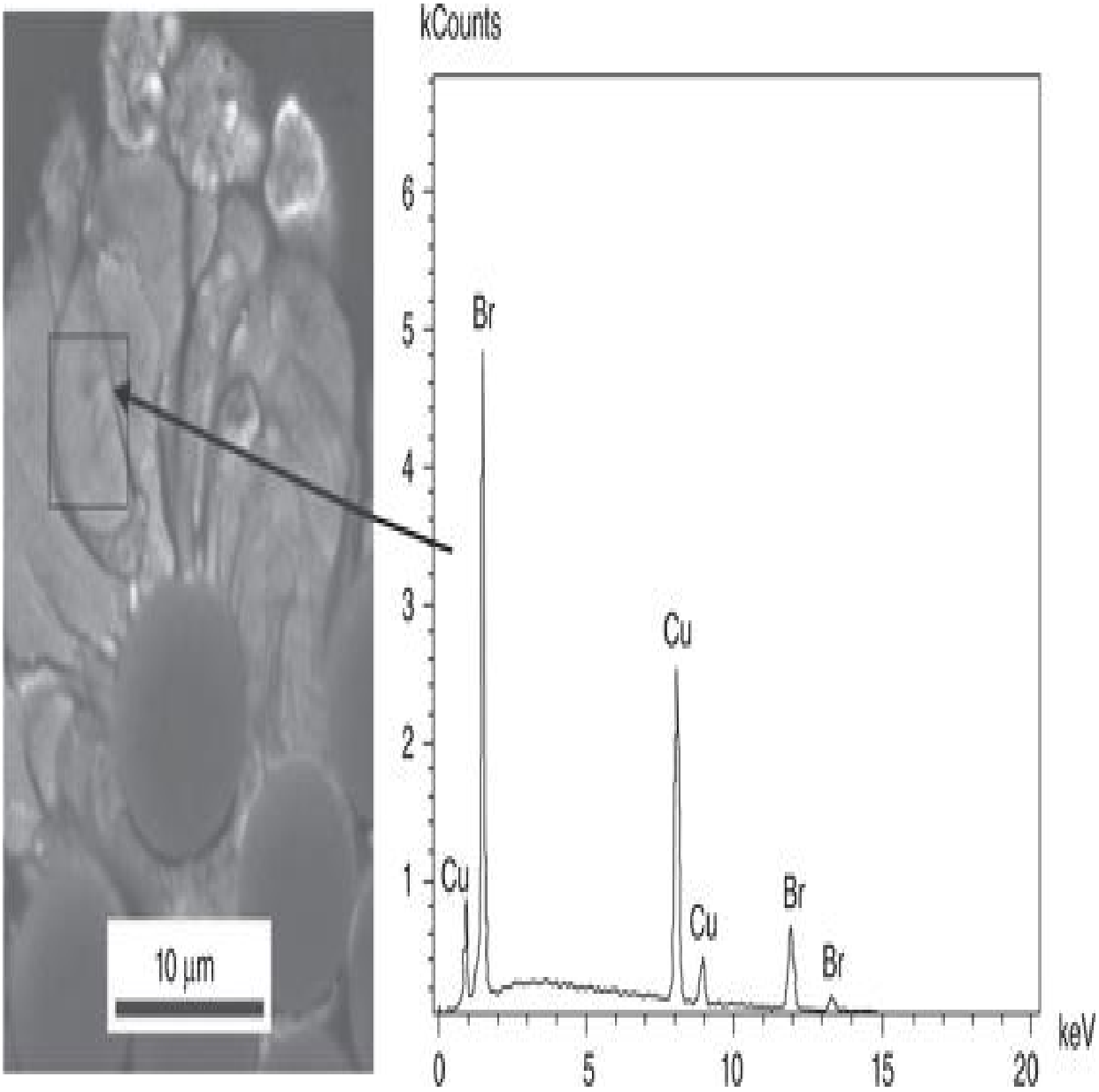


FIGURE 59.20 SEM/EDS analysis illustrating copper and bromine in the polymer matrix for a coupon processed with HASL flux.[29]

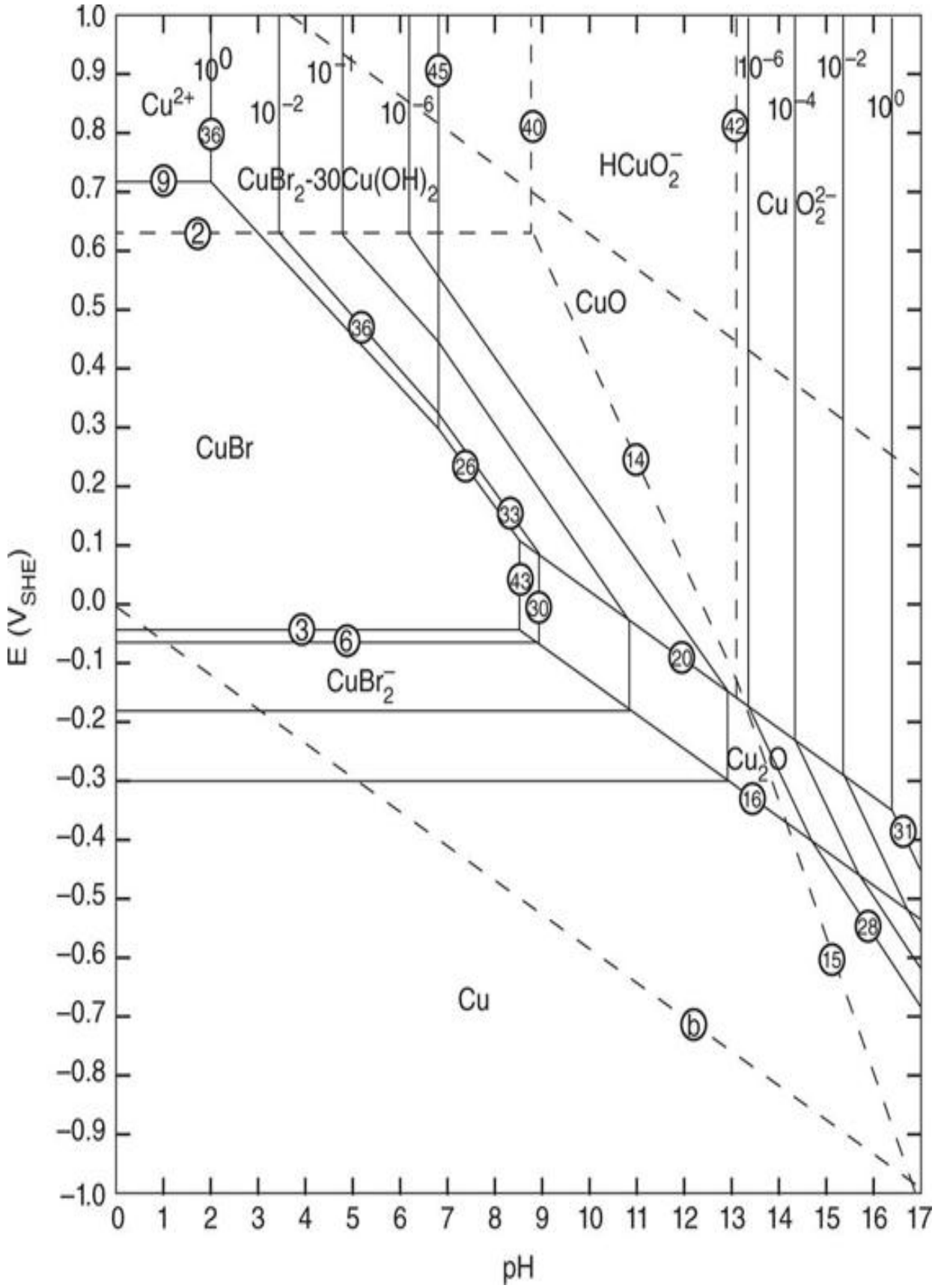

E (V_{SHE})
pH
Cu^{2+}
10^{0}
10^{-2}
10^{-4}
10^{-6}
$CuBr_2$-30$Cu(OH)_2$
$HCuO_2^-$
CuO_2^{2-}
CuO
CuBr
$CuBr_2^-$
Cu_2O
Cu
36
9
2
45
40
42
14
26
33
43
30
3
6
20
16
31
28
15
b

FIGURE 59.21 Pourbaix diagram for the copper-bromide-water system.[30] (© *NACE International 2004*.)

XPS was used to identify the copper bromide compound found in the polymer matrix as $Cu+^{1}$ and Br^{-1} by matching the binding energies for the copper and the bromide. Previous work shows that electrodissolution of copper in bromine behaves similarly to the chloride system[31,32] and thus the bromide CAF forms according to the following equation [Eq. (59.16)]:

$$4CuBr + O_2 + 4H_2O = 2Cu_2(OH)_3Br + 2Br^{-1} + 2H^{+1} \quad (59.16)$$

Extraction of ionic residues from the coupons was performed by placing the coupons in Kapak polyester bags and covering them with a measured volume of 50/50 v/v solution of isopropyl alcohol (IPA) and deionized (DI) water solution. The chloride and bromide ion levels are listed in Table 59.3, where the unprocessed control board is compared with others exposed to one or two reflows with the HASL flux. The data indicate that bromide ions are absorbed by the brominated epoxy coupon whereas the chloride ions from the HASL flux were not.

Meeker and LuValle[33] had suggested that there are two competing reaction products in CAF formation: a corrosive copper chloride compound and some innocuous trapped chlorine compounds. Caputo found no evidence of any "innocuous trapped chlorine compounds." Thus the physical evidence shows that Eq. (59.15), a nonreversible reaction catalyzed by H^+ ions, is the more appropriate explanation for CAF failure in PWBs.

59.6 TEST METHOD FOR CAF-RESISTANT MATERIALS

In the late 1990s, laminate suppliers began to develop new materials that they marketed as CAF-resistant. To evaluate these materials, K. Sauter[34–36] developed a CAF test vehicle, which consisted of a multilayer board with daisy-chained hole-to-hole spacing of 0.27, 0.38, 0.50, and 0.65 mm. The holes were either in line with the glass fiber direction or staggered. Accelerated aging was done at 65°C and 85 percent RH for 500 h. Sauter's results[36] show variations based on laminate material, manufacturer, and diagonal versus inline holes, with the former being more CAF-resistant. He also defined a "readily conductive region" around the plated-through holes, which must be considered in establishing design rules. This test vehicle and procedure has been developed as an IPC Test Method (IPC-TM-2.6.25A), "Conductive Anodic Filament (CAF) Resistance: X-Y Axis."[37]

59.7 MANUFACTURING TOLERANCE CONSIDERATIONS

Test board designs for performing statistical studies of CAF-resistant materials must take into account the limitations of the PWB manufacturing process.[38] As the hole-to-hole spacing becomes closer, the limits of the drilling process must be considered. Drill wander can be caused by splay when the drill enters the board at an angle. These two factors are exacerbated with smaller drill size. Sauter studied field data for production boards and recommended a minimum spacing of 0.65 mm hole-wall to hole-wall for telecommunication applications cycled 365 times per year. Using a high *Tg* dicyandiamide FR-4 laminate material and a specific PWB supplier he could achieve 20 years minimum expected product service life.

CAF-resistant substrates are frequently more expensive than traditional FR-4, and therefore they are reserved for

products that require high reliability, optimizing both cost and performance. Designs are multilayer rather than double-sided rigid boards. An important difference between a multilayer board and a double-sided rigid board is the glass-to-resin ratio. In drilling the holes, more damage will occur at the epoxy glass interface for boards with higher glass content.[39] Typical double-sided PWBs use eight sheets of 7628-glass cloth with a thickness of 0.175 mm to create a 1.5 mm thick board. The portion of resin in this board would be 30 to 40 percent. For a multilayer board, the glass cloth thickness may range from 0.035 to 0.10 mm per layer. In this case, the amount of resin in it ranges from 55 to 65 percent in the case of the 0.035 mm glass cloth thickness and from 45 to 50 percent in the case of the 0.10 mm glass cloth thickness. In the drilling process, the board with a higher resin content creates less hole damage than one with a lower resin content.

Microvias that are created by laser drilling can be located at a reduced pitch for CAF studies because one does not expect drill damage from a laser-ablated hole and it will not be subjected to the drill wander of a mechanically drilled hole.

The catastrophic failure presented earlier in this chapter (see Fig. 59.15) was caused by a power plane (anode), which created a CAF that shorted to the hole (cathode). In designing a test board, the power plane must always be the anode in order to reduce the current density for corrosion. A large cathode in contact with a small anode creates a high-current density at the anode and increases the corrosion rate.

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CHAPTER 60

Reliability of Printed Circuit Boards

Reza Ghaffarian

Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California

60.1 INTRODUCTION

This chapter describes the reliability of printed circuit boards (PCBs) in response to environmental stresses—that is, their reliability in service—and the influence of design, materials, and manufacturing decisions on this behavior. A variety of stresses may be present in the service environment of the PCB assemblies. Thermal stresses come from fluctuations in the ambient temperature in the service environment of the assembly or from power dissipation of high-power devices mounted on the PCB. There are also thermal stresses associated with assembly and rework. Mechanical stresses may be due to bending and flexing of the assembly during later assembly steps or in service, mechanical shock during transportation or use, or mechanical vibration, for example, from cooling fans. Chemical sources of environmental

stresses include atmospheric moisture, corrosive gases (e.g., smog or industrial process gases), and residual chemically active contaminants from the assembly processes (e.g., from flux).

These environmental stresses may act singly or in concert with one another and the electrical potential differences that exist when the assembly is functioning to cause electrical failures in the PCB and printed circuit assembly (PCA). This chapter will focus on the reliability of the PCB only. Reliability of the other elements of PCA including interconnections and components is beyond the scope of this chapter.

This chapter will focus on the delayed effects of PCB manufacturing defects and the wear-out mechanisms of properly manufactured product. Reliability of PCB with plated through holes (PTHs), plated through via (PTVs), and with microvias is discussed. PTV and microvia technology are required for implementation of high density and high I/O area array packaging assemblies. The remainder of this chapter is organized into three major technical sections:

60.2 PCB Trends and Reliability
60.3 PCB Fabrication and Failure Mechanisms
60.4 PTH Thermal Cycle Reliability and Projections Methods

60.2 PCB AND MICROELECTRONICS TRENDS AND RELIABILITY

This section first briefly presents the three elements that play key roles in defining reliability for a microelectronics system, that is, PCB, packaging, and global/local interconnections. The characteristics of these three elements are (1) PCB (e.g., polymer, Cu, plated through hole, and microvia), (2) packaging (e.g., die, substrate, solder joint, and underfill), and (3) solder joints (e.g., via balls or

columns). The section then focuses on the PCB manufacturing and via technologies and reliability under various environmental conditions. It specifically discusses reliability of PCBs with plated through holes (PTHs). The section also discusses in detail, the key failure mechanisms for PTH and analytical models developed for projection of accelerated environmental testing of PCBs with PTHs to field environmental requirement.

60.2.1 PCB/Microelectronic Packaging Trends

Figure 60.1 categorizes single-chip microelectronic packaging technologies into three key technologies: (1) plastic ball grid arrays (PBGAs), (2) ceramic column grid arrays (CGAs), and (3) and smaller foot print wafer level packages.[1–8]

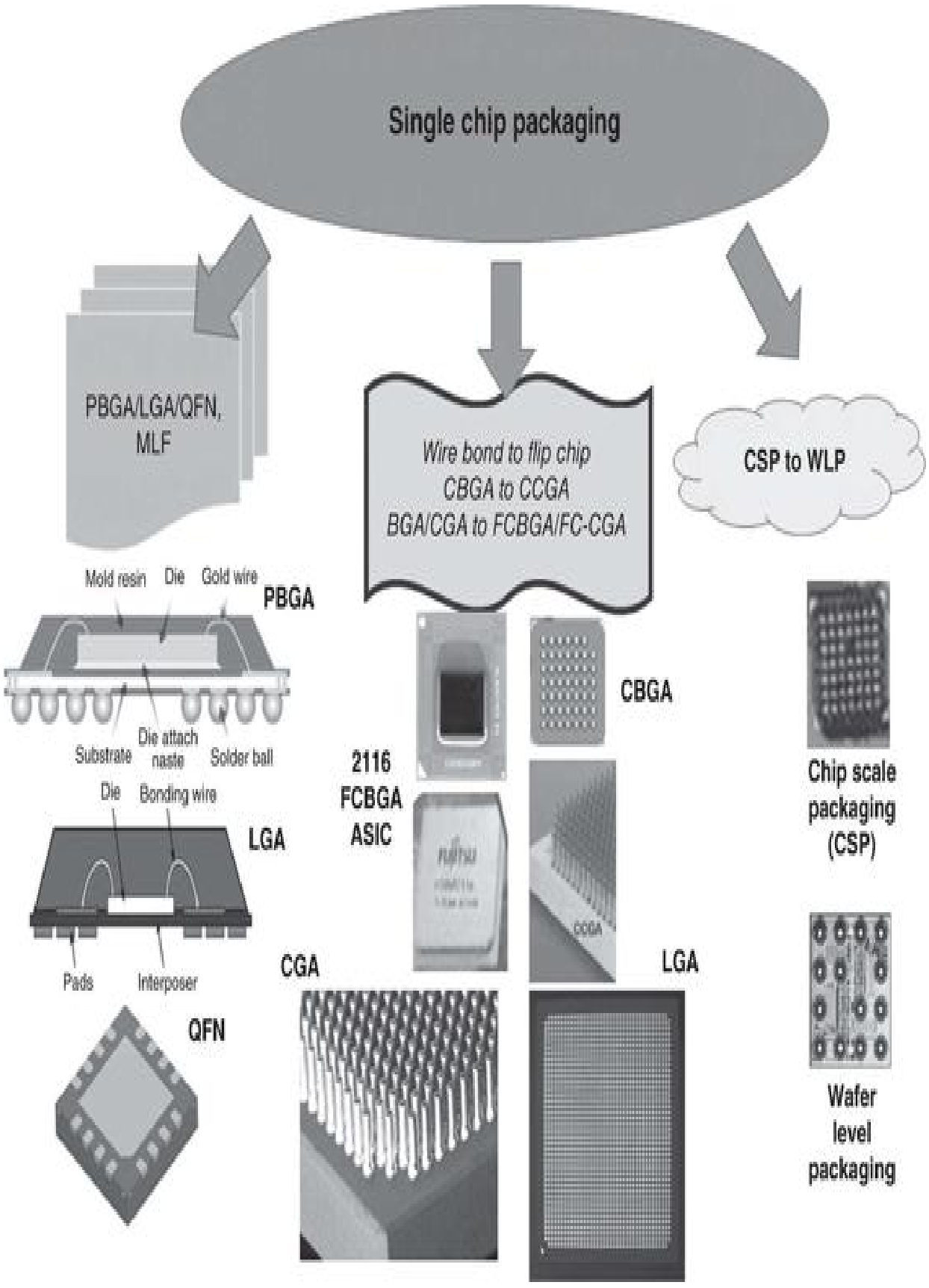

Single chip packaging
PBGA/LGA/QFN,
MLF
Wire bond to flip chip
CBGA to CCGA
BGA/CGA to FCBGA/FC-CGA
CSP to WLP
Mold resin
Die
Gold wire
PBGA
Substrate
Die attach
paste
Solder ball
CBGA
2116
FCBGA
ASIC
Chip scale
packaging
(CSP)
Die
Bonding wire
LGA
Pads
Interposer
QFN
CGA
LGA
Wafer
level
packaging

FIGURE 60.1 Single-chip packaging technologies is divided into three categories to better address various technologies.

PBGAs, chip scale packages (CSPs), and wafer-level packages (WLPs) are now widely used for many commercial electronic applications, including portable and telecommunication products. Ball grid arrays (BGAs) with 0.8- to 1.27-mm (32- to 50-mil) pitches are implemented for high reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid-1990s to the CSP, also known as fine-pitch BGA (FPGA), having a much finer pitch from 0.4 mm down to 0.3 mm (16 to 12 mil). Wafer-level packaging, protecting die at the wafer stage, is another option with CSPs.

To accommodate higher I/O single-chip die, the flip-chip BGA (FCBGA) is developed. FCBGA is similar to PBGA, except that internally a flip-chip die rather than a wire-bonded die is used. Because of these developments, it has become even more difficult to distinguish different area array packages by size and pitch; only now, its internal die attachment configuration also need to be considered. The ultimate size reduction can be achieved by protecting single die at the wafer level; hence, introduction of wafer level packages. WLPs also addresses the key issues of using single bare die; it improves ease of handling and functional testing.

Conventional PCBs with PTH vias with 150 μm (6 mil) or larger diameters are still the vias of choice used for conventional and area array packages with larger pitches. PTHs serve to electrically connect different conductor layers in multilayer PCBs. The denser packages with tighter pitches or higher I/O with fully populated arrays of balls/columns require use of high density interconnect (HDI) technology with microvias to meet miniaturization and performance requirements. Use of PCBs with microvia technology, also

known as sequential build-up (SBU), is a must when area array die are directly attached on a board to accommodate their finer (0.254-mm (10-mil) pitch and smaller).

Figure 60.2 compares PTH and microvia technologies used for conventional and fine pitch area array board assembly, respectively. The PTHs can be buried (providing interconnection between innerlayers), semi-buried (providing interconnection from one of the two outer layers to one of the internal layers), or through vias (providing interconnection between the outer two layers). Microvias are generally blind surface vias with sizes of 150 µm (6 mil) or smaller.

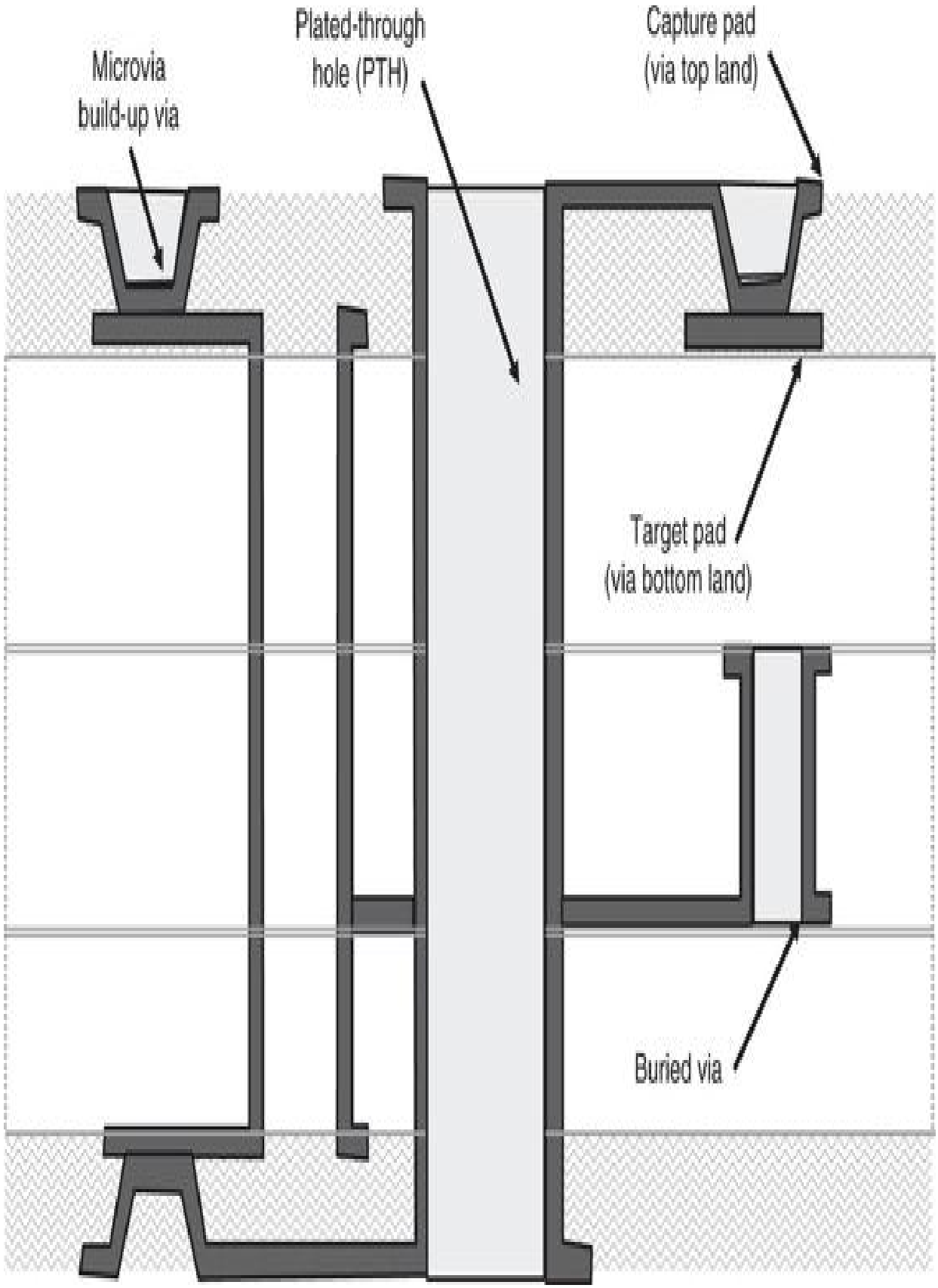

Microvia
build-up via
Plated-through
hole (PTH)
Capture pad
(via top land)
Target pad
(via bottom land)
Buried via

FIGURE 60.2 Comparison of plated-through hole via and microvia technologies.

Figure 60.3 shows an x-ray of a PCB having both PTH vias, PTH via in pad (PTHViP) and microvias with either as plated or filled.[9,10] Note that dark columns represent filled vias since x-rays are absorbed by filling materials, and therefore, these are darker compared to unfilled versions. Microsections of microvias and filled via in pads are also shown in the figure.

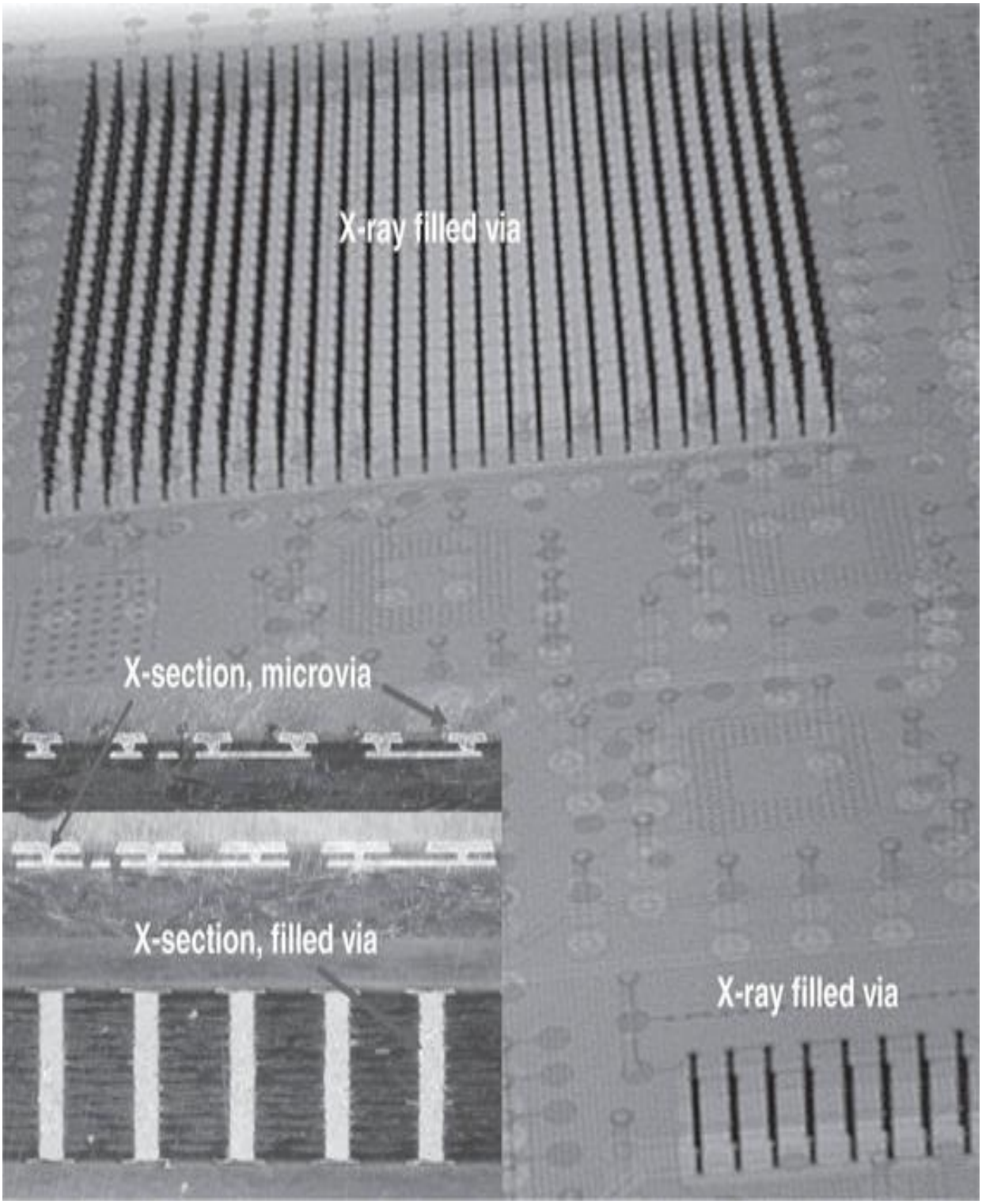


FIGURE 60.3 Microsection of microvia and filled via with x-ray of PCB with filled (dark) and unfilled microvias.[9]

IPC is an excellent resource for reviewing printed circuit board specifications and guidelines including IPC-TR-609,[11] Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in PCBs, and high density interconnect (HDI), guideline documents, design rules, materials, and test specifications. A few key standards on PCB technologies are given below.[12]

- Figure 60.4 shows the hierarchy of IPC performance and qualifications including IPC-6012 for rigid PCBs and IPC-6016, which contains the general specification for high density substrates not already covered by other documents.

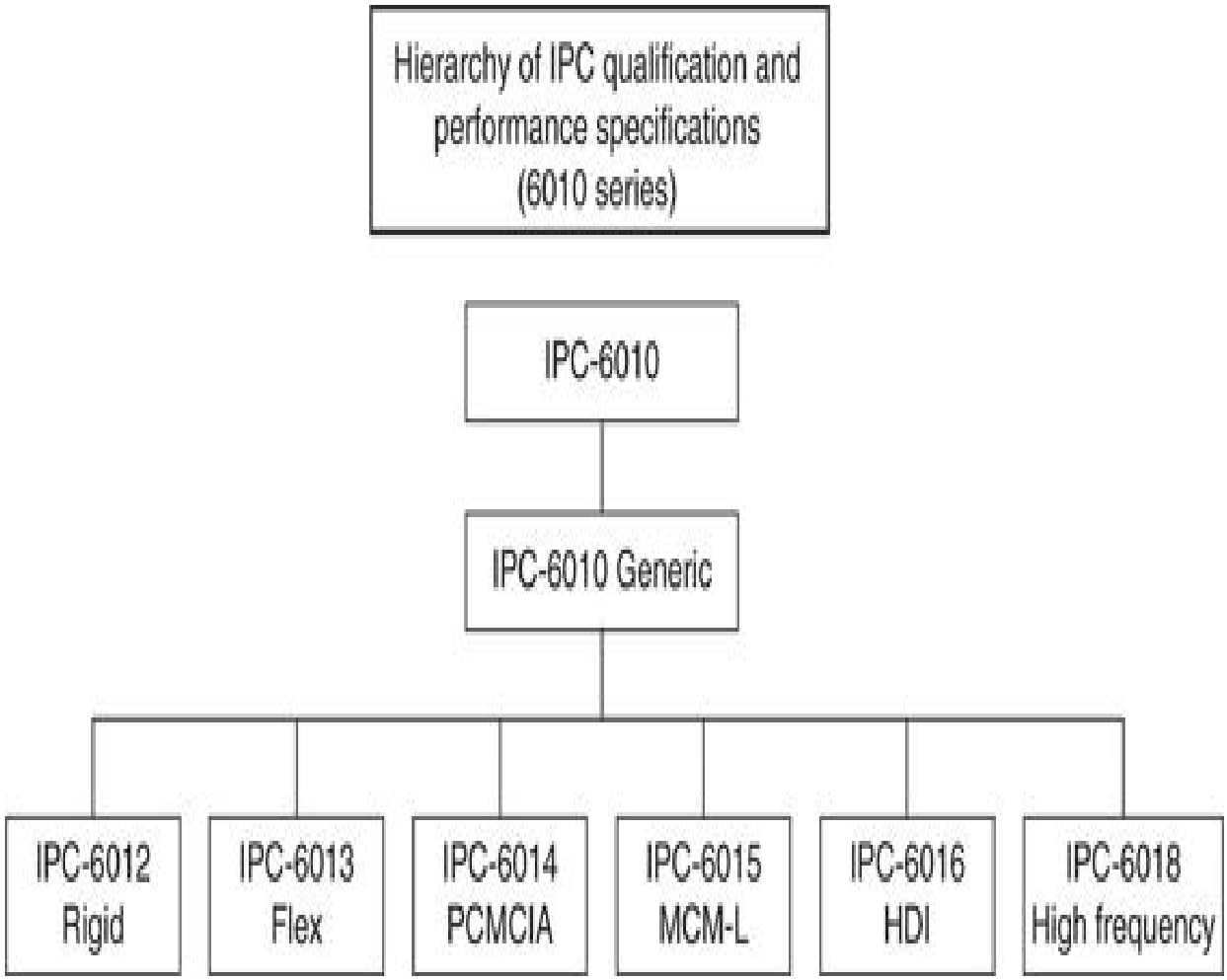


FIGURE 60.4 Hierarchy of IPC qualifications specifications for PCBs.[12]

- IPC-2315, the purpose of which is to provide guidelines for HDI technology, including educating users in microvia formation, selection of wiring density, selection of design rules, interconnecting structures, and materials characterization.
- IPC-4104, the purpose of which is to identify materials used for HDI structures. A series of specifications are defined for specific available materials, each outlines engineering and performance data that could be used for ordering.
- IPC-TM-650-2.6.26, in which the 2.6.26 test provides guidelines on changes in resistance measurements of a PTH/PTV when subjected to thermal cycling. IST coupons (designed by Interconnect Solution Inc.) are used to provide application of DC current through the interconnections. The number of cycles to failures provides a qualitative assessment of the performance of all interconnections. Test 2.6.8 provides the PTH/PTV interconnection resistance to thermal cycling effects of extreme heat due to heat exposed during the assembly, rework, and repair process.

60.2.2 Reliability of Microelectronic System

Reliability under thermal stress for package, PCB, and assembly depends on the reliability of constituent elements, for example, the PCB and its global/local interfaces (attachments). As schematically shown in Fig. 60.5, three elements play key roles in defining reliability for a system, global, local, and interconnections. The characteristics of these three elements—package (e.g., die, substrate, solder joint, and underfill), PCB [e.g., polymer, copper (Cu), plated

through hole, microvia], solder joints (e.g., via balls, columns)—together with the use conditions, the design life, and the acceptance failure probability for the electronic assembly determine the subsystem reliability.

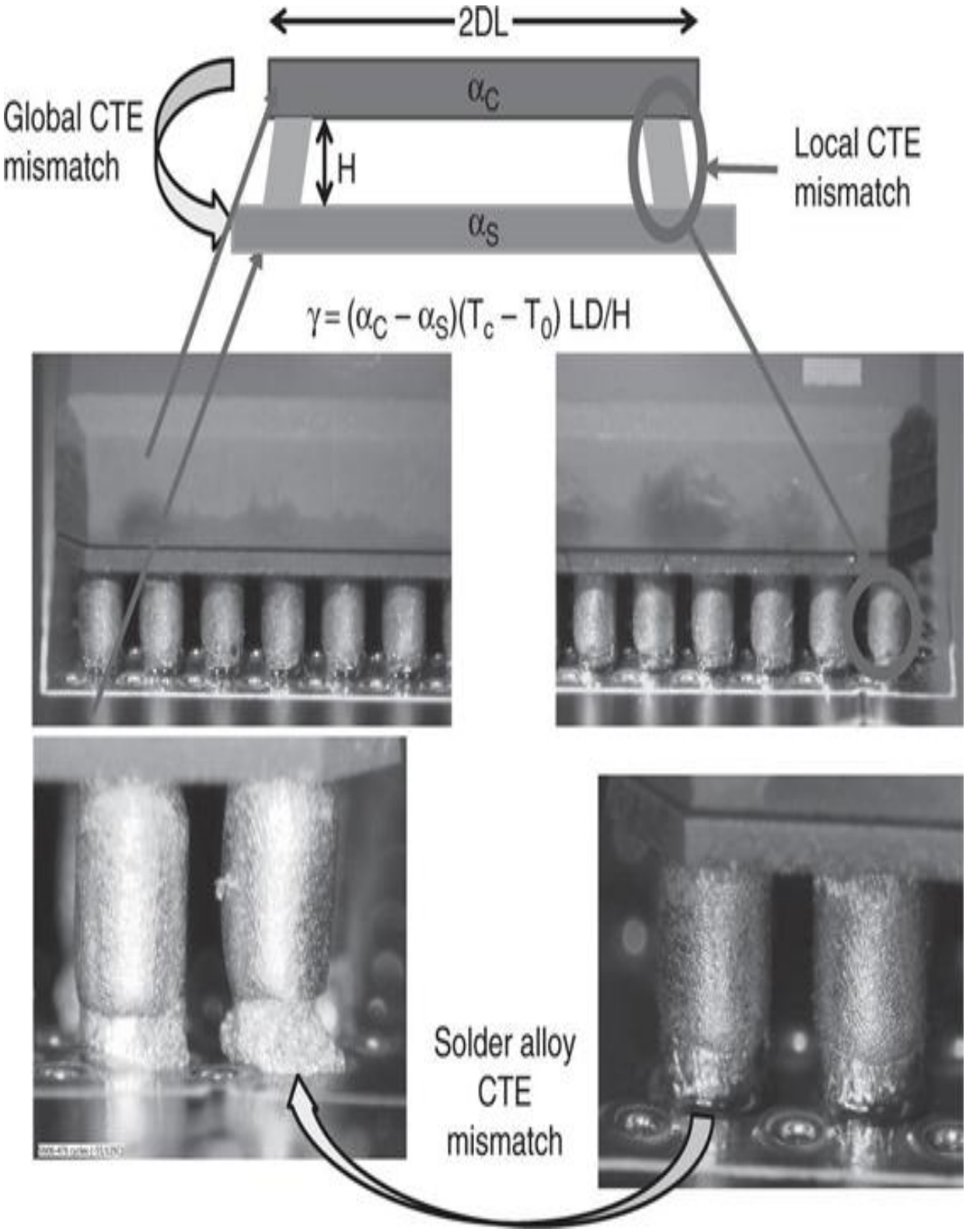


FIGURE 60.5 Three key elements defines reliability under thermal stress are due to global, local, and solder alloy coefficient of thermal (CTE) mismatches.

In other words, reliability is the ability of a system (here microelectronics) to function as expected under the expected operating conditions for an expected time period without exceeding the expected failure levels. However, reliability is susceptible to early failure by infant mortality due to workmanship defect, lack of sound manufacturing, and use of a design without reliability consideration. Design for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on, are prerequisite to ensure the reliability of the product. Only a design for reliability (DfR) can assure that a manufactured product with an acceptable quality will also be reliable in the product application. The elements of the system reliability are schematically shown in Fig. 60.6, and they are comprised of device/package/PCB and interconnections and also include consideration of design for reliability prior to assembly and subsequent manufacturing and quality assurance implementation.

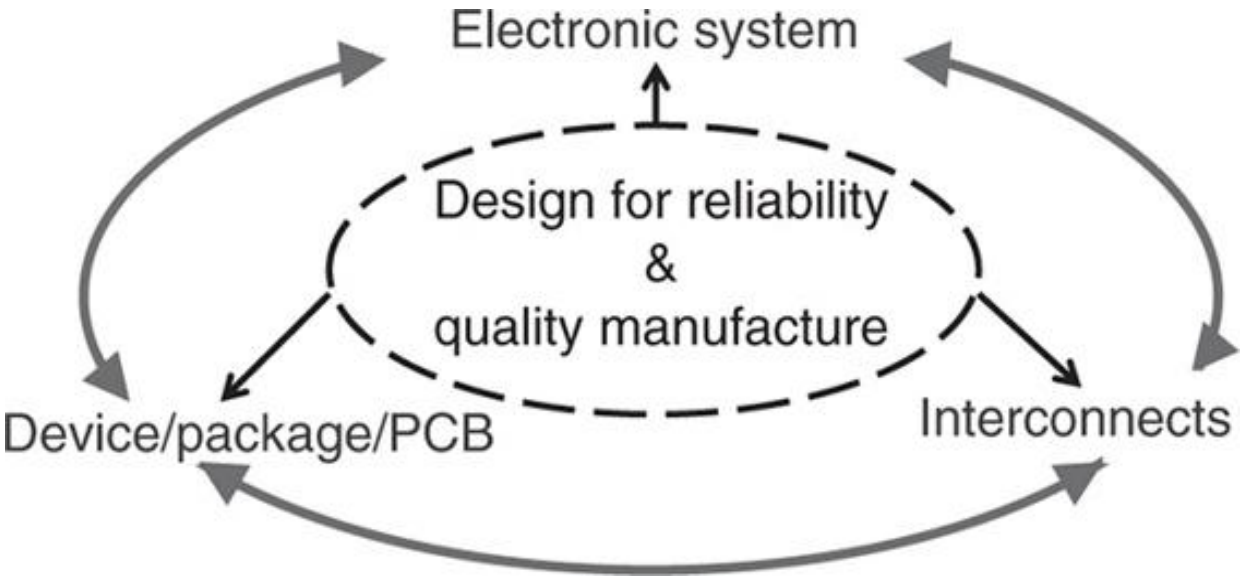


FIGURE 60.6 System reliability achieved through design for reliability (DfR), sound manufacturing, and quality to packaging/ device/PCB and interconnections.

In general, both statistical and probabilistic modeling approaches are considered in reliability methodology. Statistical approaches are employed after testing, whereas probabilistic predictive modeling is employed at the product design (DfR).

60.2.3 Reliability and Failure (Bathtub Curve)

Mathematically, the reliability of an object at time t can be stated as[13]

$$R(t) = 1 - F(t)$$

where $R(t)$ is the reliability at time t (i.e., the proportion of parts still functioning), and $F(t)$ is the fraction of the parts or systems that have failed at time t. Time may be measured in calendar units or some other measure of service time such as on/off cycles or thermal or mechanical vibration cycles. The unit of time that makes sense depends on the failure mechanism. When several failure modes are present, it is often helpful to think in terms of several time scales.

A plot of the failure rate of a product as a function of time typically takes the shape of a “bathtub” curve (see Fig. 60.7). This curve illustrates the three phases that occur during the lifespan of a product from a reliability perspective. In the first, infant mortality phase, there is an initially high but rapidly declining failure rate caused by infant mortality. Infant mortality is typically caused by manufacturing defects that went undetected during inspection and testing and lead to rapid failure in service. Burn-in can be used to remove these units before shipment. The second phase, the normal operating life of the product, is characterized by a period of stable, relatively low failure rates.

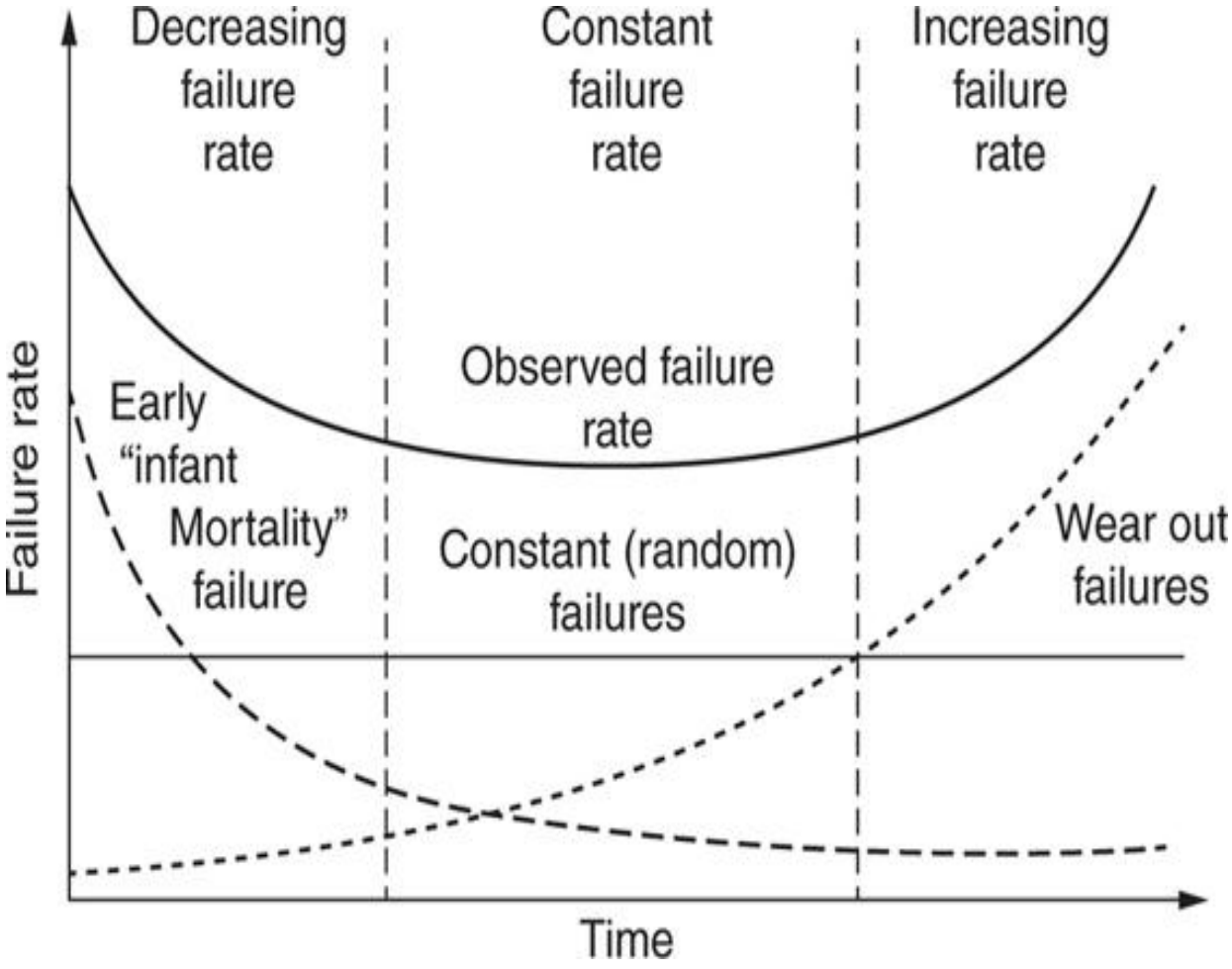


FIGURE 60.7 Classic bathtub reliability curve showing the three stages during the life of a product from a reliability perspective: infant mortality, steady-state, and wear-out.

During the operating life, failures occur apparently randomly, and the failure rate r is roughly constant with time. An exponential life distribution is often assumed to describe the behavior in this region. In that case,

$$r = (N_t / N_o)\left(\frac{1}{\Delta t}\right)$$

and

$$R(t) = e^{-rt} = e^{-1/MTBF}$$

where N_t = number of failures in time interval Δt

N_o = number of samples at the beginning of the interval

$MTBF$ = mean time between failures

During the third phase, the wear-out period, the failure rate increases gradually due to wear-out phenomena until 100 percent of the units have failed. For some systems, the second steady-state region may not exist; for PCB PTHs/microvias and solder joints, the wear-out region may extend over most of the life of the assembly. The key focus of this chapter is to understand and define specific wear-out phenomena, which manifest themselves in properly manufactured PCBs after a period of service, and to predict when they will significantly affect the failure rate.

Most wear-out phenomena can be characterized by cumulative failure distributions governed by either the Weibull or the log-normal distribution. Weibull distributions have been successfully used to describe solder-joint and plated-through-hole fatigue distributions, while log-normal distributions are generally associated with electrochemical failure mechanisms. While these distributions may be quite narrow in some cases, their use should serve as a reminder that even with nominally identical samples, failures will be statistically distributed over time.

A practical use of fitting a distribution to reliability data is to extrapolate to smaller failure rates or other environmental conditions. To simplify the equations, the expressions in the text refer to the mean life of the relevant portion of the assembly. If the constants that define the failure distribution are known, the time to reach a smaller proportion of failures may be readily calculated. For example, for failure modes that are described by a Weibull distribution, the time t to reach x percent failures is given by

$$t(x\%) = t\ (50\%)\left[\frac{Ln(1-.01x)}{Ln(0.5)}\right]^{1/\beta}$$

where β is the Weibull shape parameter, usually between 2 and 4 for solder-joint failures.

Recently, a complex three-step concept (TSC) reliability model was proposed for microelectronics.[14] The classical statistical Bayes' formula was suggested to be used first as a diagnostics tool. Its objective is to identify, on the probabilistic basis, the faulty (malfunctioning) device(s) from the signals ("symptoms of faults"). Then, physics-of-failure-based Boltzmann–Arrhenius-Zhurkov's (BAZ) model could be used to estimate the remaining useful life (RUL). If the RUL is not long-enough, further, corrective restoration of the faulty device becomes necessary. The restored device is then put back into operation (testing), provided its continuing failure-free probability of operation is found to be satisfactory. If the operational failure nonetheless occurs, the third, technical diagnostics step should be undertaken to update reliability. Statistical beta-distribution, in which the probability of failure is treated as a random variable, is suggested to be used at this step.

60.2.4 Reliability Testing Methods

Almost every reliability test program must solve the problem of determining whether an object is reliable in a time that is much shorter than the expected use period. Obviously, one cannot spend 3 to 5 years testing a personal computer that will be marketed for an even shorter time span or 20 years testing a military system. Depending on the failure mechanism, there are two approaches that may be combined: (1) accelerate the frequency of the occurrence that causes failure and test the ability of the object to

survive the expected number of events, or (2) increase the severity so that fewer occurrences are needed. Drop tests that simulate shock during transportation are an example of the first approach. Since the time between drops does not affect the amount of damage caused, a lifetime of drops can be conducted in rapid succession. However, the effect of temperature and humidity on corrosion over the lifetime of the product can be tested only by increasing the temperature, the humidity, the concentration of contaminants, or some combination of these factors. The difficulty is ensuring that the test reproduces and/or correlates to the failure mechanism in service.

To use this data for making true reliability predictions—that is, the probability of failures at a given time under given conditions—testing must be continued until enough parts fail that a life distribution can be estimated. Unfortunately, this process can be time consuming, so qualification tests are often substituted. Qualification test protocols specify a maximum number of failures that may be observed in a specified period in a sample of specified size. If few or no failures occur, a qualification test provides almost no information about the failure distribution; for example, the probability of failure during the next time interval is unknown. This limitation of qualification testing is minimized when the life distribution for properly manufactured samples is already known or can be estimated based on experience with similar designs.

Many reliability or qualification testing approaches do not follow either of these schemes. Instead, they test the ability of the product to survive a sequence of tests under extremely severe conditions for a short time or small number of exposures. Again, this type of testing may be adequate when it is supported by long experience with both the product type and its use environment; however, it is risky because it is not based on ensuring that probable failure modes will not occur in the life of the product. When new

technologies or geometries are introduced, the old tests may not always be conservative. By the same token, irrelevant failure modes that would not occur in service may be introduced by the harsh test conditions.

60.2.5 Design for Accelerated Reliability Testing

Accelerated reliability test design is summarized into seven key steps.

1. *Identify the service environment and the acceptable failure rate over a specified service life*.
2. *Identify actual environment of the PCA (modified service environment)*. The service environment should be translated into the ambient environment actually experienced by the PCA. For example, the temperature experienced by the PCA is influenced by both power dissipation and cooling. The mechanical environment is influenced by shock-absorbing material, resonances, and so on.
3. *Identify probable failure modes* (e.g., solder-joint fatigue, conductive anodic filament growth). Accelerated reliability tests are based on the premise that the frequency and/or severity of the environmental exposure can be increased to accelerate the incidence of the failure that occurs in service in a known way, that is, that the data can be used to predict the life distribution for the in-service PCA environment. This assumption makes sense only if the same failure modes occur in the test as in real life. It cannot be overemphasized that the accelerated tests must be designed around the real failure modes. Probable failure modes may be identified from past service experience, the literature, or preliminary testing or analysis.

4. *For each failure mode, construct an acceleration model*. An acceleration model that allows test data to be interpreted in terms of the expected service environment is crucial to life distribution estimation. It is also extremely helpful in designing good tests, so ideally the acceleration model should be developed before the accelerated reliability tests are carried out. As an example, for solder-joint reliability modeling, Coffin-Manson relationship relating cycles-to-failure to strain in solder joints to rigid components can be used. The relationship predicts that increasing strain will decrease the number of cycles to failure in a specific way. Within a certain temperature range, increasing the temperature cycling range is a way of increasing the strain.

In general, the acceleration model should be based on the rate-controlling step in the failure process. In some cases, the rate will be determined by an Arrhenius type equation; for example, if diffusion is the rate-controlling process:

$$D = D_o \exp(-E_a/KT)\; X \propto \sqrt{Dt}$$

$$t_2 = (D_1/D_2)t_1 = t_1 \exp[-E_a/K(1/T_1 - 1/T_2)]$$

where D = diffusion rate

D_o = diffusion constant

E_a = activation energy for the process

K = Boltzmann constant

and T_1 and T_2 and t_1 and t_2 are two temperatures and corresponding equivalent diffusion times.

Note that even when temperature is an important factor, *an Arrhenius relationship may not exist;* in the preceding thermal cycling example, the failure rate is roughly

proportional to $(\Delta T)^2$. Some acceleration models will be explored in the following sections.

The limits of applicability of an acceleration model are as important as the model itself. Increasing or decreasing the temperature too much may promote new failure modes that would not occur in service or invalidate the quantitative acceleration relationship. For example, if the temperature is elevated above the glass transition temperature, T_g, of the board, the *z*-axis CTE increases sharply, and the modulus decreases. This may actually lessen the strains imposed on solder joints, but it may also promote PTH failures.

Finite element modeling/analysis (FEM/FEA) can be invaluable in developing and/or applying acceleration models for thermal and mechanical tests. Two-dimensional nonlinear modeling capability will usually be required in order to get meaningful results. Models can be constructed to estimate the stresses and strains in the material (e.g., the Cu in a PTH barrel or the solder in a surface-mount or through-hole joint) under operating conditions as well as under test conditions. These estimates will be far more accurate than the simple models provided in this overview because they can account for the interactions between materials in a complex structure and both elastic and plastic deformation.

5. *Design tests based on the acceleration models and accepted sampling procedures*. Using the acceleration model and the service environment and life, select test conditions and test times that simulate the life of the product in a much shorter period of time. The sample size must be large enough that it is possible to determine whether the reliability goal (acceptable number of failures over the service life) has been met.[15] Ideally, the life distribution in the accelerated test should be determined, even when the test period must be extended to do so.

6. *Analyze failures to confirm failure mode predictions*. Since an accelerated test is based on the assumption that a particular failure mode in the accelerated test is the same one that occurs in service, it is important to confirm by failure analysis that this assumption is valid. If the failure mode in the accelerated test is different from the one expected, several possibilities should be considered. (1) The accelerated test is introducing a new failure mode different from the one that will occur in service. Usually this means that the acceleration of one parameter (e.g., frequency, temperature, humidity) was too severe. (2) The initial determination of the dominant failure mode was incorrect. In this case, to understand the significance of the test results, a new acceleration model must be developed for this failure mode. The new failure mode may be promoted more or less effectively by the test conditions than the mode originally assumed. (3) There may be several failure modes. In this case, the two failure distributions should be considered separately, so that life predictions will be meaningful. The difficulty in determining which of the above scenarios holds is that for genuinely new technologies or service environments, the failure mode in service may not be known. In these situations, it is desirable to conduct a parallel test with less aggressive acceleration for comparison.
7. *Determine life distribution from accelerated life distribution*. The accelerated life distribution should be determined by fitting the data with the appropriate statistical distribution, such as the Weibull or log-normal distribution. The life distribution in service can be determined by transforming the time axis of the life distribution using the acceleration model. This predicted life distribution in service can then be used to estimate the number of failures in the specified service life.

The following discussion of testing for some specific failures will provide examples of this methodology.

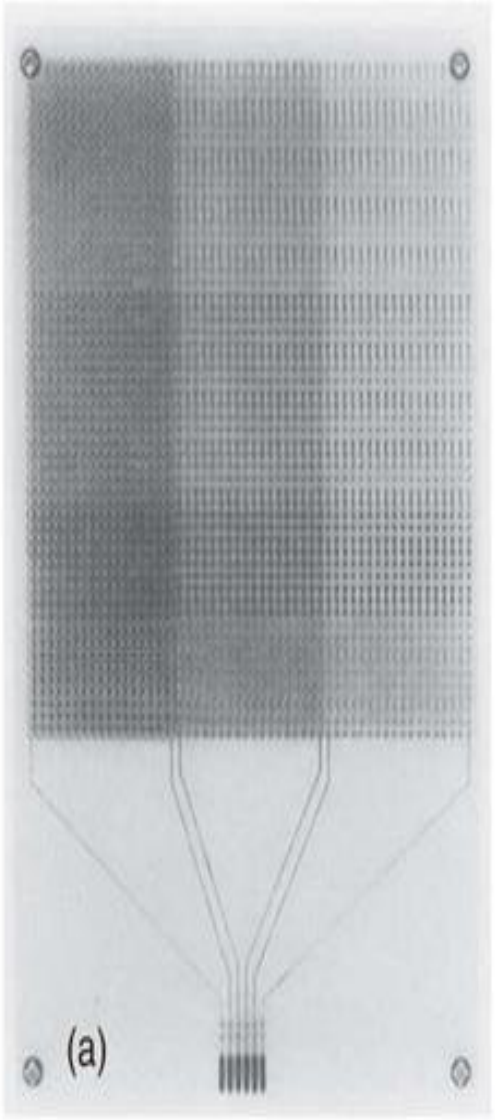
60.2.6 Printed Circuit Board Reliability Tests

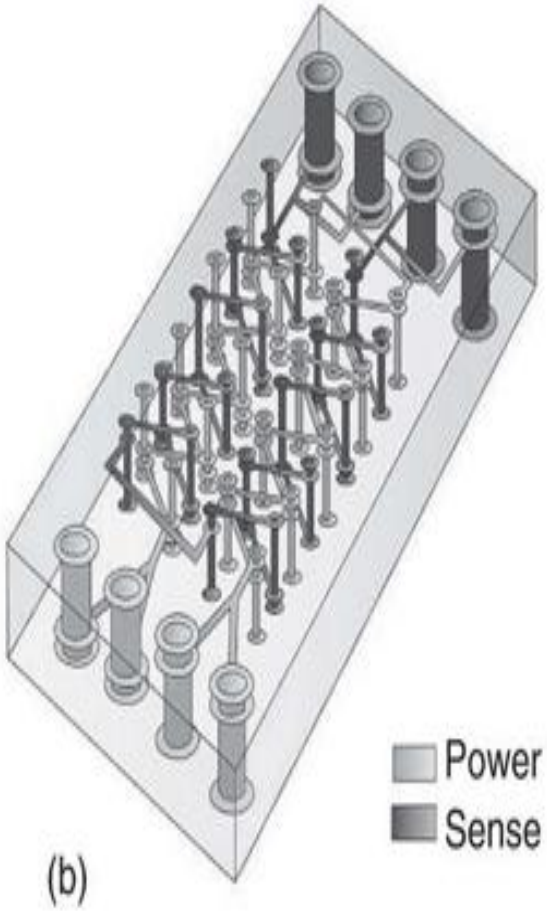
60.2.6.1 Thermal. PTH failures are the predominant source of PCB failures in service, and predicting them is the primary goal of PCB testing at elevated temperatures. PTH reliability testing should simulate the thermal excursions of a PTH throughout its life. Generally, the most severe thermal cycles are experienced during assembly and rework. One of the older acceptable thermal stress test is MIL-P-55110 (also found in IPC-TM-650). Following baking at 120 to 150°C, the specimens are immersed in an RMA flux and floated in a eutectic (or near-eutectic) Sn-Pb solder bath at 288°C for 10 s. For lead-free, the bath temperature is at 260°C or higher. Following the test, the samples are cross-sectioned, and the PTHs are examined for cracks. This is a severe test that ensures that the sample will survive a single wave-soldering or solder pot rework cycle.

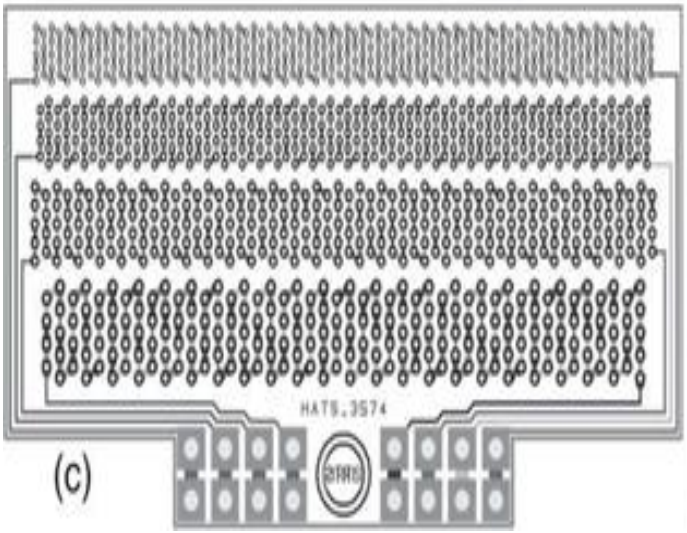
Most thermal cycling tests for PCBs cycle the PCB repeatedly over a wide temperature range; many are actually thermal shock tests using liquid-liquid cycling. The results of five accelerated tests with different temperature extremes, ramp rates, and dwell times have been compared by the IPC, which also provides a simplified analytical model to estimate PTH life.[11] The results of all tests suggest the same approaches for maximizing PTH reliability, but they do not all correlate well quantitatively.

Figure 60.8 shows a number of suitable test coupons for PCB PTH/microvia evaluation. These include (1) a test coupon that contains 3000 PTHs and varying annular ring sizes,[13] (2) an IST (interconnect stress testing) coupon with

hundreds of PTH and microvias with direct current induced thermal cycling,[16] (3) an HATS (highly accelerated thermal shock) coupon with 4 daisy-chain nets and up to 36 coupons per chamber and air-to-air cycling,[17] and (4) PCQR^2 (process capability, quality, and relative reliability) test panel for standard comparison of printed circuit board manufacturing processes.[18]


(a)


Power
Sense
(b)


HATS.3574
(c)

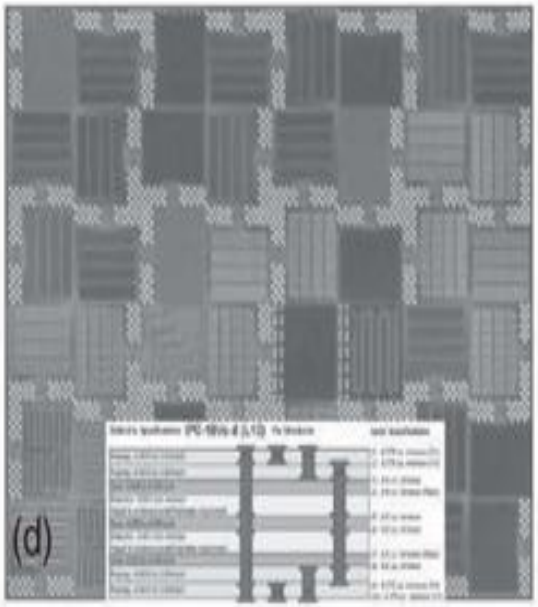

(d)

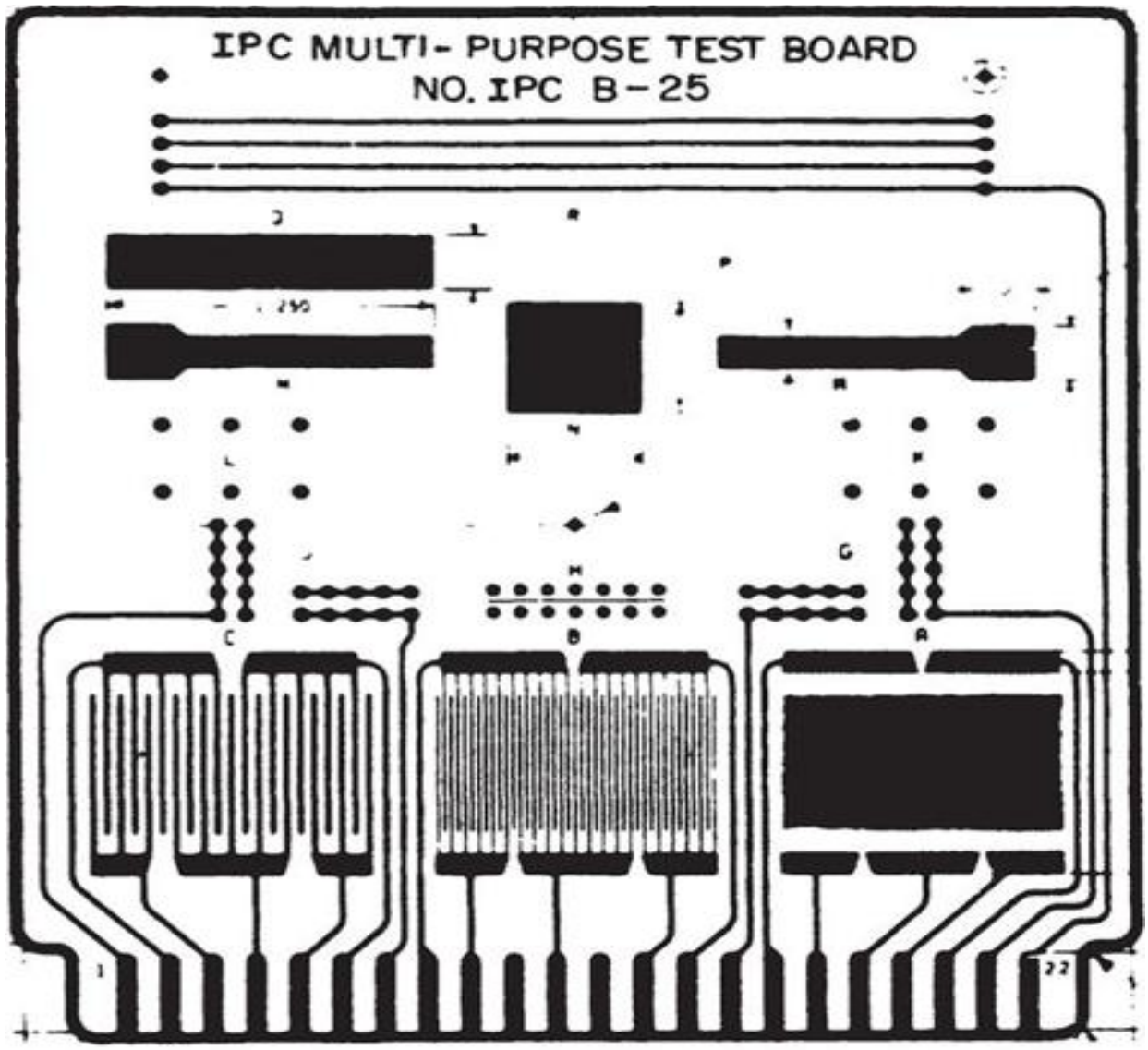
FIGURE 60.8 Representations of PTH reliability test coupons: (*a*) coupon contains three sets of 1000 PTHs interconnected in series, (*b*) interconnect stress testing (IST) coupons, (*c*) highly accelerated thermal shock (HATS) coupon, and (d) process capability, quality, and relative reliability ($PCQR^2$) coupon.

60.2.6.2 Mechanical. PCBs are rarely subjected to mechanical tests that could cause electrical failures; however, adhesion of both Cu and solder mask to the laminate is critical and is often tested. Loss of solder mask adhesion can provide a place for corrodents and moisture to accumulate, which can be the cause of electrical failures when the board is exposed to temperature and humidity.

Adhesion is commonly tested using the peel test described in IPC-TM-650, Method 2.4.28. The simplest version of this test is conducted by scribing the adherent and dividing it into small squares. If the Cu or solder mask pulls off with a piece of tape with strong adhesive, the adhesion is inadequate. More quantitative tests that measure the actual peel strength are performed primarily by laminate and solder mask suppliers.

60.2.6.3 Temperature, Humidity, Bias. These tests are designed to promote corrosion on the PCB surface and conductive anodic filament growth, either of which can cause insulation resistance failures. Surface insulation tests utilize two interleaved Cu combs with an imposed dc bias across the combs. These combs may be designed into existing boards or a coupon such as the IPC-B-25 test board (shown in Fig. 60.9) may be used. The measured resistance (ohms) from the comb pattern can be converted to surface resistivity (ohms per square) by multiplying the measured resistance by the square count of the pattern. The square count is determined geometrically by measuring the total length of the parallel traces between the anode and cathode and dividing by the separation distance. Special precautions are needed to make accurate measurements of insulation resistance.[19] Measurements of resistance above 10^{12} are

very difficult and require careful shielding. Measurements of resistance below 10^{12} can be conducted in most laboratory environments if certain precautions are taken.


IPC MULTI- PURPOSE TEST BOARD
NO. IPC B-25

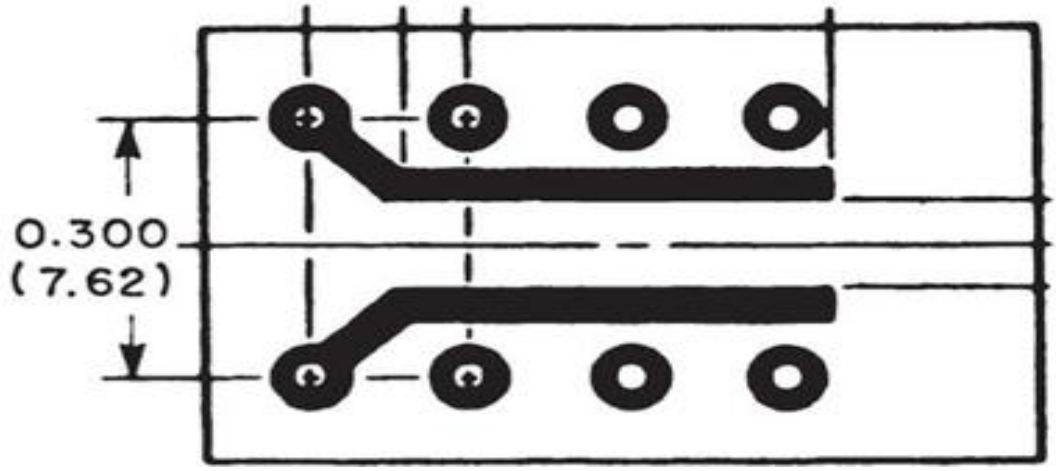

0.300
(7.62)

FIGURE 60.9 Test coupons used to check moisture, insulation, and metal migration resistance: (*a*) the IPC-B-25 test board, used to qualify the process; and (*b*) the Y coupon, designed to be incorporated into production boards for statistical process control. (*From IPC-SM-840*.)

The actual tests are usually conducted at elevated temperature and humidity with an applied dc bias. A test for moisture and insulation resistance of bare printed circuit boards is included in IPC-SM-840A. The severity of the test depends on the intended use environment; for typical commercial products (Class 2), the test is conducted at 50°C, 90 percent RH, and 100 V_{dc} bias for 7 days. The minimum insulation resistance requirement is 10^8 Ω. The military test procedure for moisture and insulation resistance is specified in PCB military specification, MIL-P-55110.[20] The moisture resistance test should be conducted in accordance with military specification, MIL-STD-202, Method 106, with applied polarization voltage (100 V_{dc}) and Method 402, Test condition A. IPC-SM-840A also includes a test for electromigration resistance. The test is conducted at 85°C/90 percent RH at a 10 V_{dc} bias with a limiting current of 1 mA for 7 days. A significant change in current constitutes a failure. The samples are also microscopically inspected for evidence of electrolytic metal migration. A common test for dendritic growth due to flux residues is 85°C/85 percent RH/1000 h at a -20 V_{dc} bias. These tests are empirically based; however, several investigators have attempted to develop acceleration factors for these and similar tests.[21,22]

60.2.7 Accelerated Thermal Cycle/Shock Tests

Figure 60.10 shows a representation of thermal cycle and shock tests currently being used for PCB reliability evaluation. Thermal cycle qualification of PTHs has evolved

within the last decade to accommodate effectiveness and cost.[23,24] Thermal shock oven temperature cycling testing has a well-established history as an indicator of the long-term field life of PCB products. However, verified correlation with actual long-term field life has been difficult to achieve due to the long time required for testing and the associated expense. In the 1990s, interconnect stress testing (IST) was developed, and more recently highly accelerated thermal shock (HATS). Testing has been developed as a more practical indicator based upon the through-hole via and internal interconnect reliability of printed wiring boards

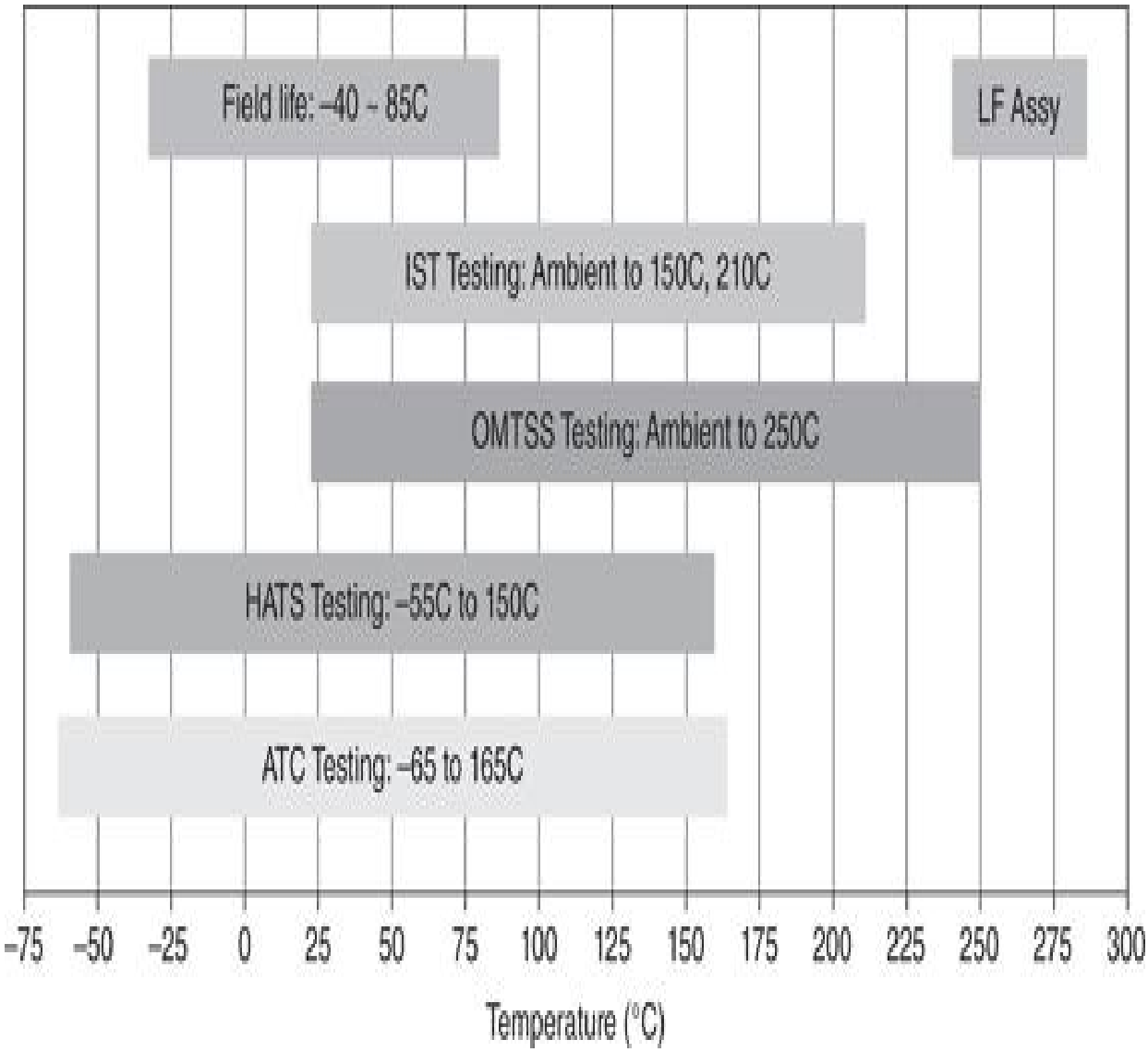


FIGURE 60.10 Representation of accelerated thermal cycling and shock currently practice for PTH/microvia PCB reliability characterization.[23,24]

60.2.7.1 Thermal Shock Oven Testing. This test method measures cycles to failures (CTFs) on actual functional production boards or appropriately designed test boards/coupons. The ovens are capable of air-air cycling over a potentially large temperature range (−40 to +145°C). Transition rates between 25 and 35°C/min are used for this testing, with a 20-s dwell at both high and low temperatures.

60.2.7.2 IST Testing. This test method measures CTFs on specially designed IST coupons that are thermally cycled using current flow through internally heated circuits that heat the coupon and the adjacent plated-through holes. Failure is defined as a 10 percent increase in the resistance of the plated-through hole. Reference: IPC-TM-650, 2.6.26.

60.2.7.3 HATS Testing. This test method measures CTFs on specially designed HATS coupons typically having 4 daisy chain nets each. There can be up to 36 coupons per chamber load that go through air-to-air cycling over a potentially large temperature range (−55 to +160°C). Transition rates for this testing are usually at least 25°C/min up to 50°C/min, depending upon the high and low temperature and the HATS equipment capability.

60.2.7.4 Thermal Shock Testing. The thermal shock test method (TSM, IPC-TM-650, Method 2.6.8) that uses conventional stress/microsectioning is long and more difficult to characterize and detect failure. The IST is now an accepted test method by the IPC and found to better detect ILS failure than conventional TSM. The IST (IPC-TM-650, Method 2.6.26) is a DC-current-induced thermal cycling test that can also be used to determine PTH barrel cracking based on industry round-robin testing. It was shown that (1) qualitative correlation exists between ILS and TSM for

“gross” innerlayer separation, (2) IST is more consistent and sensitive for “fine-line” innerlayer separation, and (3) IST testing shows that smaller diameter vias are less likely than larger-diameter vias to exhibit innerlayer separation on the same panel.

For example, recent studies have shown that microvias require testing above the resin T_g. It has been recently established that the IST testing of microvias should be thermal cycled to 190°C. Testing at 190°C allows enough thermal expansion to cause a compromised microvia to fail in less than 500 cycles and at the same time does not produce any artifacts in the failure mode. Testing at 150°C will produce mean time to failure well in excess of 1000 cycles. Testing at temperatures higher than 190°C produces faster time to results but, upon microscopic analysis, the failure mode may not reflect the same failure mechanisms that are experienced in assembly or the end-use environment.

The IPC process capability, quality, and relative reliability (PCQR^2) has been demonstrated by testing a reasonably good correlation of the HATS test results with the more established thermal shock oven temperature cycling testing over the same 185°C temperature range (−40 to +145°C). The test failure criterion was a 10 percent increase in resistance. The temperature ranges for these cycling/shock tests are listed in Table 60.1.

TABLE 60.1 Comparison of Thermal Profile for Various Thermal Cycle/Shock Conditions Uused to Qualify PCBs and Microvias

Test Type → Thermal Cycle ↓	Oven Standard	IST Standard	IST Microvia	HATS
Lower temp (°C)	−50	22	22	−40
Upper temp (°C)	125	128	190	145
Delta T (°C)	175	172	168	185
Dwell time (min)	10	3	3	0.25
Cycle time (min)	60	5	5	9.6
Cycle/day	24	288	288	150

60.3 PCB FABRICATION AND FAILURE MECHANISMS

Printed circuit boards can be divided into the following types:

- Rigid boards that are widely used as single-sided or double-sided boards, or multilayer boards
- Flexible and rigid-flex boards
- Others including metal-core boards and injection molded boards

PCBs evolved from single-sided (all interconnections on one side) to double-sided and multilayer boards to meet the demand of higher performance systems requiring higher packaging density and faster propagation speeds. Currently, PTHs provide connections between the PCB's top and bottom side allowing wires to cross over each other without the need for jumpers. Multilayer PCBs provide the routing requirements to meet the increased pin count of IC

packages. Only multilayers have power and ground planes that are a must for high-performance systems. The planes are needed to meet controlled impedance for the high-speed traces, the need for bypass capacitors, and the need for low inductance values for the power and ground distribution networks. In multilayer boards, the PTHs can be buried (providing interconnection between innerlayers), semi-buried (providing interconnection from one of the two outer layers to one of the internal layers), or through vias (providing interconnection between the two outer layers).

When choosing among PCB substrate materials their mechanical, electrical, chemical, and thermal properties must be considered. At present, the copper-clad laminates and the prepregs are made with a variety of different matrix resin systems and reinforcement materials, such as woven glass fibers. The most commonly used resin systems for commercial applications are fire resistant (FR-4) difunctional and polyfunctional epoxies. The glass transition temperatures, T_g, range from 125 to 170°C, which may not be sufficiently high for some applications. Polyimide resins with higher T_g (>200°C), long-term thermal resistance, lower coefficient of expansion (CTE), and long plated-through via (PTV) life and high reliability are used for high-performance multilayer PCBs with a large number of layers.

Most multilayer boards are made of glass-reinforced with one of these or other resin systems not discussed here. Rolls of glass cloth are coated with liquid resin (A-stage). Then the resin is partially cured to a semistable state (B-stage or prepreg). The internal circuits are made on single- or double-sided copper-clad laminates. Two approaches are used to pattern Cu conductors, either by removing or etching Cu (subtractive process) or adding (additive process) Cu as required. Conductive paste is now also an option to form layer pairs and to attach substrates together in multilayers. The innerlayers are stacked up with B-stage polymer. The

rolls are cut into large sheets, and several sheets are stacked to form the desired final thickness sheets separating the layers. Rigid pins are used to establish layer-to-layer orientation. The B-stage prepreg melts during lamination and reflows. When it is cured, it glues the entire package into a rigid assembly. An alternative approach to pin-parallel composite building is a sequential buildup of the layers, which allows buried vias.

60.3.1 PCB and Via Types

Typical hole-diameters for PTV to microvia ranges from 300 to 50 µm (12 to 2 mil). These vias are divided into three general categories:

1. PTV. The plated-through-hole vias are formed through the entire thickness of the PCB. If it is used for component mounting it is identified as a PTH (plated-through hole) to distinguish the case when is as used solely as an interconnect (PTV).
2. Blind via. Blind vias are located on the outer layers at the top or at the bottom of the PCB and formed such as to make contact with the innerlayers.
3. Buried Via. Buried vias are holes formed within the innerlayers of a PCB without access to the top or bottom surfaces. These via holes are formed before lamination and plated and filled depending on the PCB build-up technology.

High density interconnects (HDIs) constitute the newest layering connection approach for multilayer PCBs and substrates in electronic packaging that accommodate dense and fine pitch package and die requirements. The high density requirement is achieved by using much smaller via (microvia) structures. Microvias are vias of less than or equal

to 150 µm (6 mil) in diameter used as blind and buried vias to form interconnections through one dielectric layer within a PCB. Microvias are cost effective and more reliable when are used in outer layers in a blind via construction where the outer layers of a multilayer PCB are connected to the next adjacent signal layer.

Microvias offer several distinct advantages[25,26] over their mechanically produced counterparts) from both the aspect of physical features and electrical performance, including the following:

- Microvias within the pads (via-in-pad) allow significant reduction in fan out and routing and therefore increased packaging density for assembly with a reduced layer count, greater layout efficiency, and improved cost effectiveness for a given PCB.
- PCBs with microvias enable the designer to incorporate the newest high density packages and die into their system. The microvia is especially valuable or may even be required when using parts such as full array packages, CSPs, and flip chip direct attach (FCDA) designs. PCBs with conventional through-hole fabrication technology have physical size limitations that cannot support parts with fine-line geometry.
- PCBs with microvias show better electrical performance and signal integrity due to their physical structure. As the physical size of microvias become smaller and shorter, both the inductance and capacitance decrease, resulting in a reduction in switching noise.
- RFI/EMI/ESD (radio frequency interference/electromagnetic interference/electrostatic discharge) can be improved by effective grounding. Increased routability area combined with the microvias-in-pad implementation enable a designer to utilize more

ground plane around the component, thus reducing the ground return loop.

- Proven microvia technology yields higher reliability because of the significantly lower area aspect ratio (1:1) due to its fabrication in one dielectric layer when compared to a larger drilled through-hole via having a much high aspect ratio (>10:1).

60.3.2 PCB Failure Mechanisms

PCB failure mechanisms can be categorized into three key types:

- Thermally induced failures. The most common failures are due to PTH/PTV and HDI microvia failure. For this reason, these types of failures will be discussed in detail below.
- Mechanically induced failures can occur during mechanical loading into test fixtures or insertion into box/brackets, or when the assembly experiences mechanical shock or vibration in use. In general, a PCB is stronger than the packages and interconnections; therefore, this failure mechanism is less important for PCBs and will not be discussed further.
- Electrochemical failures generally cause reduction in surface insulation resistance (SIR) and if excessive SIR degradation occurs, unacceptable cross talk between circuit elements may occur, causing the circuit to cease functioning properly. Exposure to humidity, especially when ionic contaminants are present, is a common cause of insulation resistance failures that is accelerated by elevated temperatures and electrical bias. The impedance often decreases slowly over a long period of time. If the SIR value falls below the designed level, there will be cross talk between circuit elements that should be isolated, and the circuit may not function properly. Insulation resistance

deterioration is particularly harmful for analog measurement circuits. The medical products that use sensors attached to a patient also pose special concerns, because deterioration of insulation resistance has the potential to cause electrical shock. Electrochemical failures are usually accelerated by temperature, humidity, and applied bias. Even though this type of failures are critical, it is beyond the scope of this chapter.

- Conductive contaminant bridging of circuits by conductive salts may occur if plating, etching, or flux residues remain on the board. These ionic residues are good conductors of electricity in a moist environment. They tend to migrate across both metallic and insulating surfaces to form shorts. Corrosive byproducts, such as chlorides and sulfides formed in industrial environments, are chemically similar and can also cause shorting. An example of this type of failure is shown in Fig. 60.11.[27]

FIGURE 60.11 Migration of corrosion products across the surface of FR-4 bridging two conductors.[13, 27]

- Dendritic growth occurs by the electrolytic transfer of metal from one conductor to another; consequently, it is

also termed *electrolytic metal migration*. It is also referred to as *electromigration*, although it should not be confused with the process that occurs in aluminum conductors in integrated circuits, which has a different mechanism. It is significantly accelerated by the presence of hydrolyzable ionic contaminants (e.g., halides and acids from flux residues or extracted from polymers). Delaminations or voids that promote the accumulation of moisture or contaminants can promote dendritic growth. The dendrite resembles a tree, since it consists of a stalk with branches. When the growth touches the other conductor there is an abrupt rise in current, which sometimes destroys the dendrite but may also cause an electrical circuit to temporarily malfunction or damage a device. An example of this type of failure is shown in Fig. 60.12.

FIGURE 60.12 Transmitted light micrograph through a PCB that failed in the field. Dendritic growth has formed at the interface of a UV-cured screened solder mask and the FR-4 surface.[13]

- Galvanic corrosion occurs between dissimilar metals because they have differing affinities for electrons (i.e., they are more or less electronegative). Galvanic series have been compiled for many common metals and alloys. Metals near the top of the series (noble metals) do not

corrode; those near the bottom corrode easily. When these metals are near each other, the more noble metal becomes the cathode, the less noble the anode. Moisture is required to couple the two metals electrically. Applied bias is generally not required, but may accelerate the reaction if the polarity is correct. When the anode is very small compared to the cathode, its corrosion can be very rapid. Conversely, if the anode is much larger than the cathode, corrosion is unlikely to be serious, particularly if the difference in electronegativity is small.

- Conductive anodic filament growth. Conductive anodic filament growth (CAF) causes electrical shorts when a metal that dissolves anodically is redeposited at the interface between the glass (or other) fibers and the resin matrix of a printed circuit board. Conductive anodic filament growth is promoted by delamination at the glass-polymer interface, which may in turn be promoted by various environmental stresses including high temperatures (greater than about 260°C (500°F) for FR-4) and thermal cycling. Shorts seem to occur most rapidly when a single fiber bundle connects two pads. Once delamination has occurred, the metal migration that causes shorts to occur is promoted by increasing temperature, relative humidity, and applied voltage
- Whiskers. Whiskers are faceted filament-like structures that grow spontaneously on the surface of a plated metal and can cause shorts between closely spaced conductors. Whiskering can be differentiated from other causes of shorts such as dendritic growth, because neither an electrical field nor moisture is required for whiskers to form. Whiskering is a particular problem with pure tin. The whiskers grow in response to internal stresses in the plating or external loads. Sn whiskers are commonly 50 µm (2 mil) long and 1 to 2 µm (0.04 to 0.08 mil) in diameter.

60.3.3 PTH/PTV Failures under Thermal Stresses

Figure 60.13 shows schematically several common key failures and failure locations of the PTH that are frequently observed due to thermal cycling exposure of a PCB. Barrel cracking occurs due to high CTE mismatch between the organic resin matrix and the Cu in the Z direction since the embedded reinforcement material (for example, glass or aramid fibers) has minimum effect on lowering the CTE in this direction. The effective CTE in the X and Y directions in general is much lower due to the lower CTE of the reinforcement material. In addition, the resin CTE increases sharply above its glass transition temperature, causing further CTE mismatch strain induction on the Cu and the potential of PTH/PTV failure.

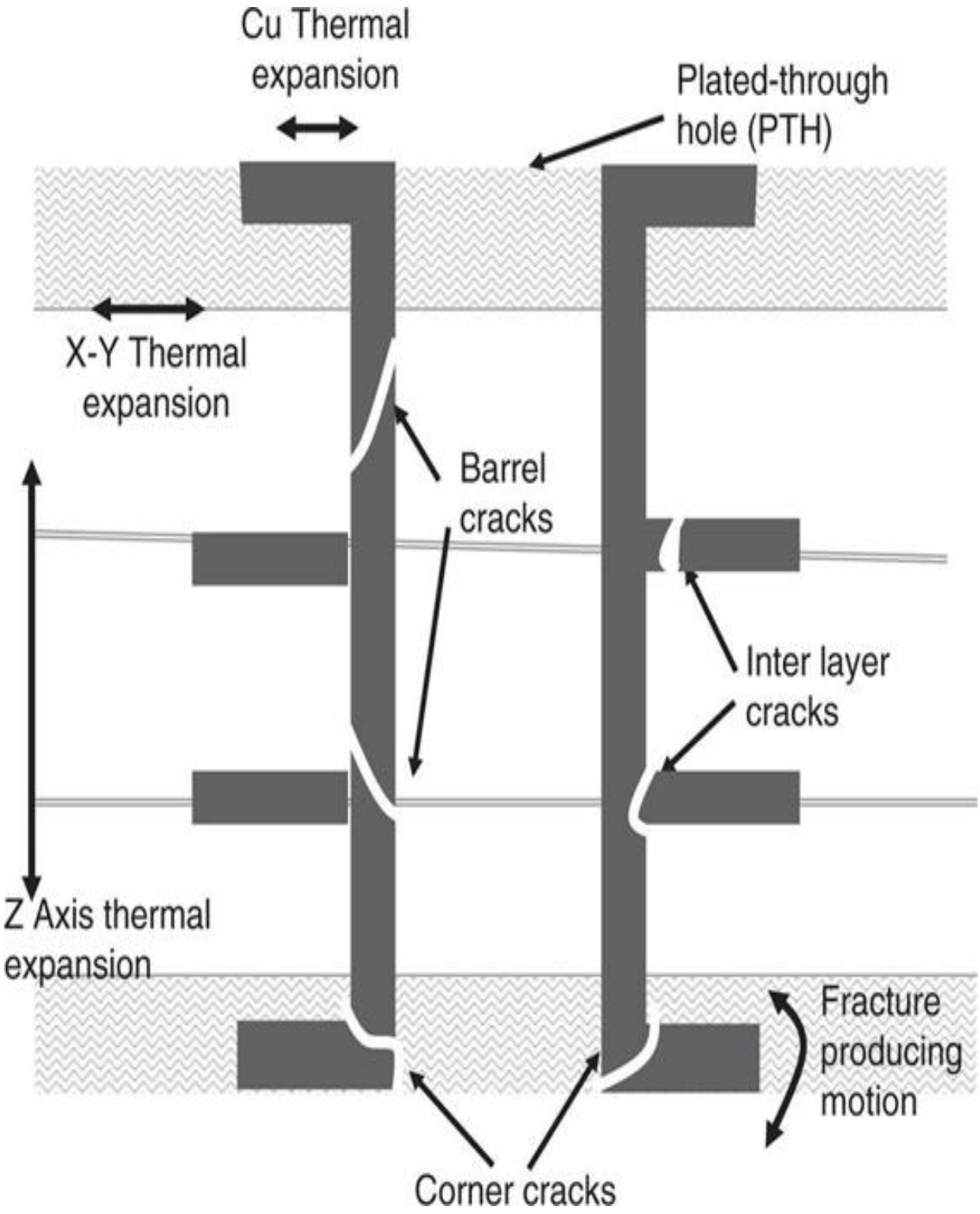


FIGURE 60.13 Common failure mechanisms for plated-through-hole vias.

Innerlayer separation (ILS) can be in the form of innerlayer Cu foil failure, separation of the foil and Cu flash, or

separation of the Cu flash and electrolytic Cu. Whereas barrel cracking and land rotation is caused by the *z*-axis CTE mismatch, ILS occurs in the *x* and *y* directions due to resin expansion into the free space of the PTH. If the Cu wall is thick enough to deform only elastically, then ILS typically does not result. However, if the barrel wall is thin and unsupported, the barrel will plastically deform inwards causing a large tensile stress at the PTH inner attachment points. A Cu foil with good quality can delay failure due to these stresses.

60.3.4 PTH Reliability and the Effects of PCB Fabrication Parameters

60.3.4.1 Laminate and Lamination. Delamination in PCBs may occur between the laminate materials or between the laminate material and the Cu foil. One cause of delamination is defective laminate material. Defects such as incomplete bonding at the resin/fiber interface can result in delamination due to formation of voids at these interfaces. Other common causes of delamination are excessive lamination pressure and/or temperature, contamination at interfaces, heavily oxidized Cu foil surfaces, and lack of oxide treatment to enhance adhesion between Cu innerlayers and prepreg. Debonding increases the risk of conductive anodic filament growth because it provides a place for moisture to accumulate. It can also result in increased stresses on the plated-through holes (PTHs) during thermal cycling.

Laminate voids and resin recessions are separations of the laminate material from the copper conductor that may occur during multilayer PCB lamination. Most acceptability specifications prohibit voids larger than 76 µm (3 mil); however, smaller voids are not generally considered to be detrimental to reliability. Some of the causes of laminate voids are entrapped air during lamination, improper flow of

resin, and improper epoxy cure, perhaps due to improper lamination pressure and/or temperature, inappropriate heating rate, or too little prepreg.

60.3.4.2 Cu Foil. The major cause of innerlayer foil cracks seems to be poor ductility of the Cu. Poor foil ductility can have a more significant effect on PTH reliability than such well-known culprits as insufficient plating thickness and excessive etchback. A minimum of 8 percent elongation is required for 1-oz foil to eliminate this problem. Foils plated in a Hull cell can be easily evaluated for room-temperature ductility using a 180° bend test.[28] Poor copper ductility can be correlated to the microstructure observed in metallographic cross sections.[29]

60.3.4.3 Drilling and Desmear. Poor drilling and desmear (etchback) can cause PTH failures by providing stress that contributes to conductive anodic filament growth. The following paragraphs describe the effects of poor desmear and some drilling defects that can cause poor plating, such as resin smear, rough walls, loose fibers, and burrs. Resin smear can cause weak connections between plated-through holes and innerlayer copper that fails under environmental stress. There is always some resin smear, which is removed by the desmear (etchback) process. If the desmear process is not effective, or if the resin smear is excessive, poor interconnection to the innerlayers can result. Possible causes of excessive smear are a dull drill or the wrong feed rate or drill speed, all of which can cause increased drill heating, resulting in more smear.

Similar errors in drilling setup can cause rough hole-walls, loose fibers, or burrs. These defects are not serious in and of themselves, but can lead to rough plating or copper nodules, which introduce stress concentrations. Rough walls are typically associated with an incorrect feed rate or drill speed, or insufficiently cured material. Loose fibers may be caused

by incorrect drilling parameters or improper cleaning. Burrs are usually associated with too fast a drill feed or a dull drill.

Poor drill registration can also decrease reliability of innerlayer via connections or the soldered connection to through-hole components. Poor registration can cause breakout on innerlayers; that is, the drill hole may fall outside the pad on the innerlayer it is intended to connect to. Breakout increases the probability of PTH barrel failures. Breakout on outer-layers means that the solder fillet for a through-hole component will be partially missing, resulting in decreased reliability for some critical components.

Whether caused by excessive resin smear or not, poor etchback can result in a weak connection between the plating in the hole and the innerlayer copper. Etchback (see Fig. 60.14) removes laminate resin and woven glass in the hole so that the internal copper projects slightly into the hole, permitting the plating to make contact with the innerlayer foil on three sides. This strength is important to prevent cracking at the interface under thermal shock conditions. A review of innerlayer cracking in or around the electroless copper at the junction between the innerlayer foil and the electroplated Cu in the hole suggests that *negative* etchback, in which the electroplated Cu projects into the laminate may also give good results. Zero etchback, when innerlayer foil is flush with the hole wall, is the most dangerous case because the bond line between the foil and the plated copper is located at the point of maximum stress.[30] However, flush etch back is considered the least dangerous and most reliable configuration by others.[31] Causes of insufficient etchback include improper lamination and curing, hardened epoxy smear, a depleted smear removal bath, or a host of process control issues, including improper bath temperature, agitation, or time exposure.

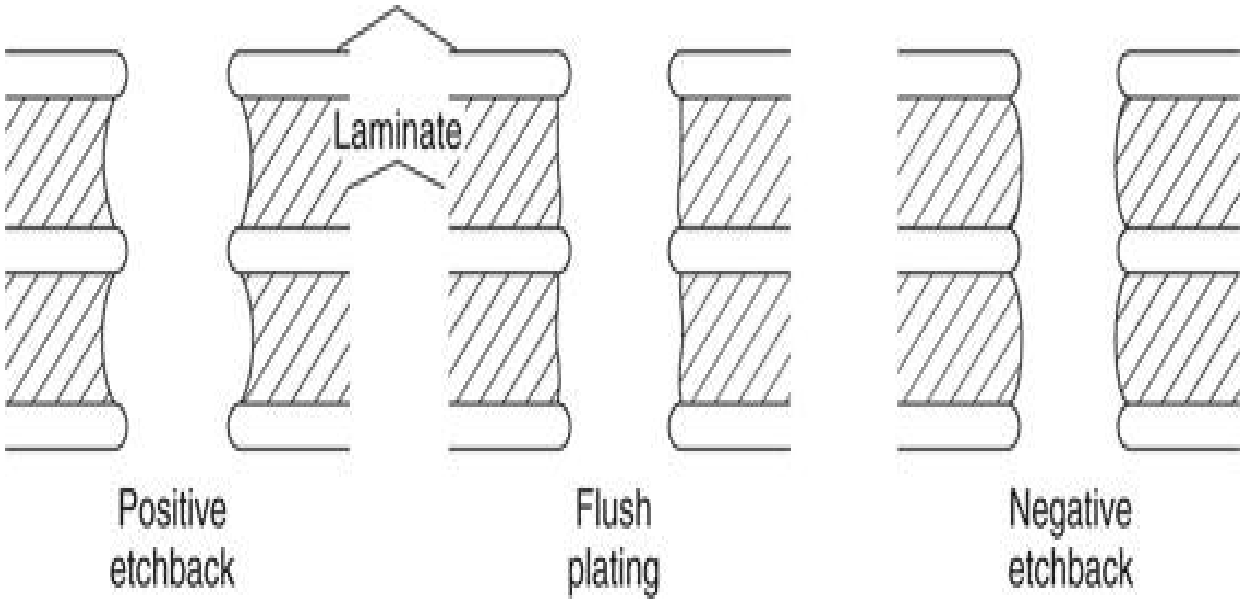


FIGURE 60.14 Schematic illustrations of positive, flush, and negative etchback. (*After M. W. Gray*.[30])

60.3.4.4 Plating. Defects from the plating process can be responsible for a variety of PTH reliability problems; in addition, as previously described, problems in earlier process steps such as drilling and desmear often show up as plating defects. Uniform coverage of the hole with electroless Cu is critical to the strength of the through hole and the adhesion of the metallization to the laminate. Oxidation of the innerlayer copper prior to electroless Cu plating is one source of poor plating adhesion. Poor control of bath composition can have the same effect.

The adhesion of the electroplated Cu to the electroless Cu and the ductility of the electroplated Cu also strongly affect PTH reliability. If the adhesion between the layers is poor, this interface may be the weak point, where failure initiates when the PTH is subjected to thermal stresses. Causes can include tarnished electroless copper that is insufficiently micro-etched, burning the electroless copper with too much current in electrolytic plating, and film contamination in the electrolytic copper.[30] Susceptibility to innerlayer cracks may be identified by looking for cracks in microsections after a

solder float test. The fatigue life of the Cu is directly related to its ductility. Plating process parameters and plating additives can strongly affect the plating ductility.

Insufficient plating thickness in the barrel also directly reduces PTH reliability because the stress and, consequently, the strain in the Cu are increased. Overall insufficient plating thickness can be caused by a depleted bath or insufficient plating time, among other things. Insufficient plating thickness in individual holes can also occur as a result of nonuniformities in plating current caused by nonuniform Cu feature density. It is particularly difficult to obtain adequate plating thickness in the center of high-aspect-ratio PTHs; good process control is important for aspect ratios greater than 3:1. Good coverage is difficult to obtain for aspect ratios greater than 5:1 by electroplating.

What constitutes “sufficient” plating thickness in PTHs is a subject of some controversy. Specifications range from 12 to 25 µm (0.5 to 1 mil) Cu thickness in the barrel. There are at least two reasons why there is no one right specification. First, different applications provide different levels of thermal stress and demand different levels of reliability. Second, design factors such as the aspect ratio of the plated holes determine the susceptibility of the PTHs to thermal fatigue. The IPC recommends an average minimum copper-plating thickness of 12 µm (0.5 mil) for consumer products (Class 1) and 25 µm (1.0 mil) for general industrial and high-reliability applications (Classes 2 and 3).

Poor coverage at the PTH knee can significantly accelerate PTH failures because it means the plating is thin at a point of high stress. It can be caused by excessive concentration of the organic leveling agents added to an electroplating bath.

60.3.4.5 Solder Mask Application. If it is properly applied, solder mask plays an important role in reducing the possibility of insulation resistance failures on PCBs. The solder mask protects the substrate from moisture and

contaminants, which would otherwise promote shorting under electrical bias. The ability of the solder mask to perform this function depends on good conformity and adhesion of the solder mask to a clean, dry substrate. If solder mask conformity or adhesion is poor, moisture and other contaminants may accumulate at crevices or delaminations between the solder mask and the substrate. Substrate cleanliness is particularly critical because, in addition to causing poor solder mask adhesion, it can also provide the ionic species needed for rapid electromigration. When the laminate material absorbs moisture readily (e.g., polyimide, aramids), baking before reflow may be required to prevent solder mask delamination (as well as reinforcement/resin delamination).

Other causes of poor adhesion or conformity include moisture on the board when the solder mask is applied, improper solder mask lamination or coating parameters, and improper solder mask cure parameters. Incomplete solder mask cure can create local soft pockets, which are common sites for delamination or contaminant entrapment. Solder mask over solder should also be avoided because delamination caused by reflow of the solder may allow contaminants to be entrapped.

60.3.4.6 Rework. Rework, whether repair of open or shorted solder joints or replacement of defective components, has a significant negative effect on component and PCB reliability. Rework of large through-hole components, such as pin grid arrays (PGAs) and large connectors, poses special problems. If it is improperly done it can result in PTH failures. Because the damage during these large thermal cycles is cumulative, the number of rework operations at a given site should be monitored and limited to a safe number. The number of cycles that will cause a fatigue crack to initiate in the copper in the barrel and propagate to failure depends on the aspect ratio of the PTH,

the type and thickness of plating in the hole, the substrate material, etc.

Due to the large number of joints that must be melted at once and the large thermal mass of the components, rework of large PTH components is often done with a solder pot. The thermal shock caused when the molten solder hits the board can cause PTH cracking due to *z*-axis expansion. A preheat step (to about 100°C for FR-4) helps to reduce the damage. The time the board is in contact with the solder fountain should also be minimized since dissolution of the copper plating inside the PTH occurs during this time. Thinning the plating in the PTH tends to increase the strain in the Cu during thermal cycling, further accelerating failure. If the total time for part removal and replacement is kept under 25 s, little dissolution is measured.[32] Weakening of the PTH by copper dissolution during PGA rework can be essentially eliminated by using NiAu plating. Although the thin Au coating that protects the Ni dissolves almost instantly during soldering, Ni dissolves quite slowly and effectively prevents thinning of the PTH metallization.

Rework temperatures also weaken the adhesive bond between the Cu conductors on the PCB and the laminate material; use of force to remove components when the solder is not completely molten can cause the pad to lift off the board. The latter can be a particular problem when using a soldering iron.[33,34]

60.3.5 PTH Reliability and the Effects of PCB Properties

60.3.5.1 Substrate. Difunctional FR-4 is the key material for high-reliability PCBs because its moderate *z*-axis expansion and moisture uptake characteristics are available at relatively low cost. Alternative substrate materials (see

Table 60.2) are generally selected for more favorable properties in one or more of the following three areas: thermal performance, including maximum operating temperature and glass transition temperature; thermal expansion coefficient; and electrical properties, such as dielectric constant. Thermal performance characteristics and thermal expansion coefficient can have a significant effect on PCB and solder joint reliability. Other characteristics of these materials, such as moisture absorption, can also affect reliability.

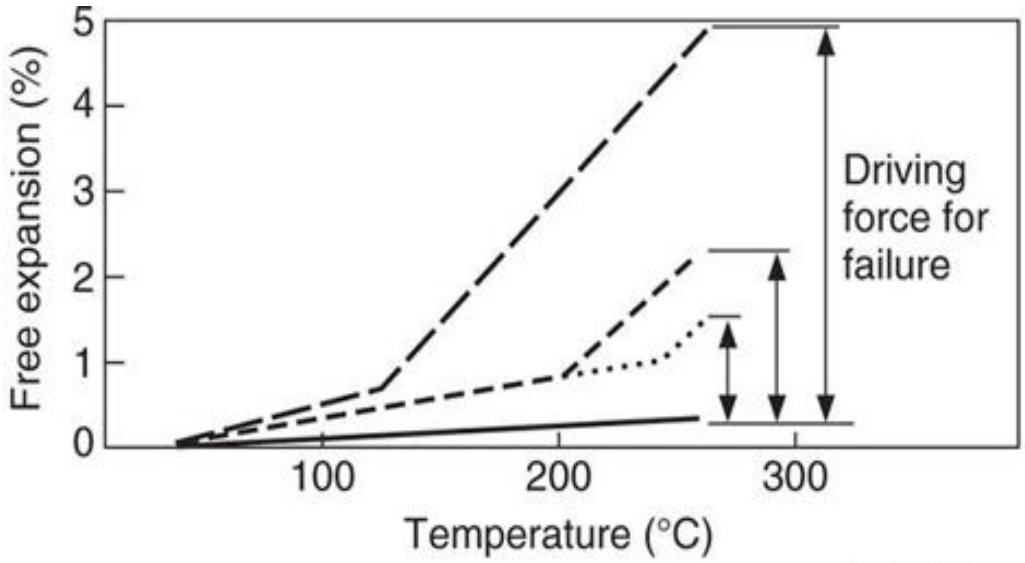
TABLE 60.2 Physical Properties of Some Printed Circuit Board Laminate Materials (IPC Dd-279)

Material	CTE, Y ppm/°C	CTE, Z ppm/°C	T_g, °C
Epoxy glass (FR-4, G-10)	14–18	180	125–135
Modified epoxy glass (polyfunctional FR-4)	14–16	170	140–150
Epoxy aramid	6–8	66	125
Polyimide quartz	6–12	35	188–250

PTH reliability can be improved by selecting a laminate with a lower *z*-axis CTE or a higher T_g. The damage caused to the PTH during a thermal cycle depends on the total *z*-axis expansion during the temperature change since the CTE is much lower below T_g than above.

The PTH strain can be reduced by increasing the T_g so that more or all of the cycle is below T_g (see Fig. 60.15*a*). Figure 60.15*b* shows that the increase in life can be quite significant. The strain imposed on the PTH can also be

reduced by decreasing the CTE at temperatures below T_g, but the effect on total z-axis expansion is much smaller.



Material	T_g, °C	z-axis CTE, ppm/°C
Copper	—	17
FR-4	125	73/300
FR-4/CE blend	200	50/230
CE	240	50/230

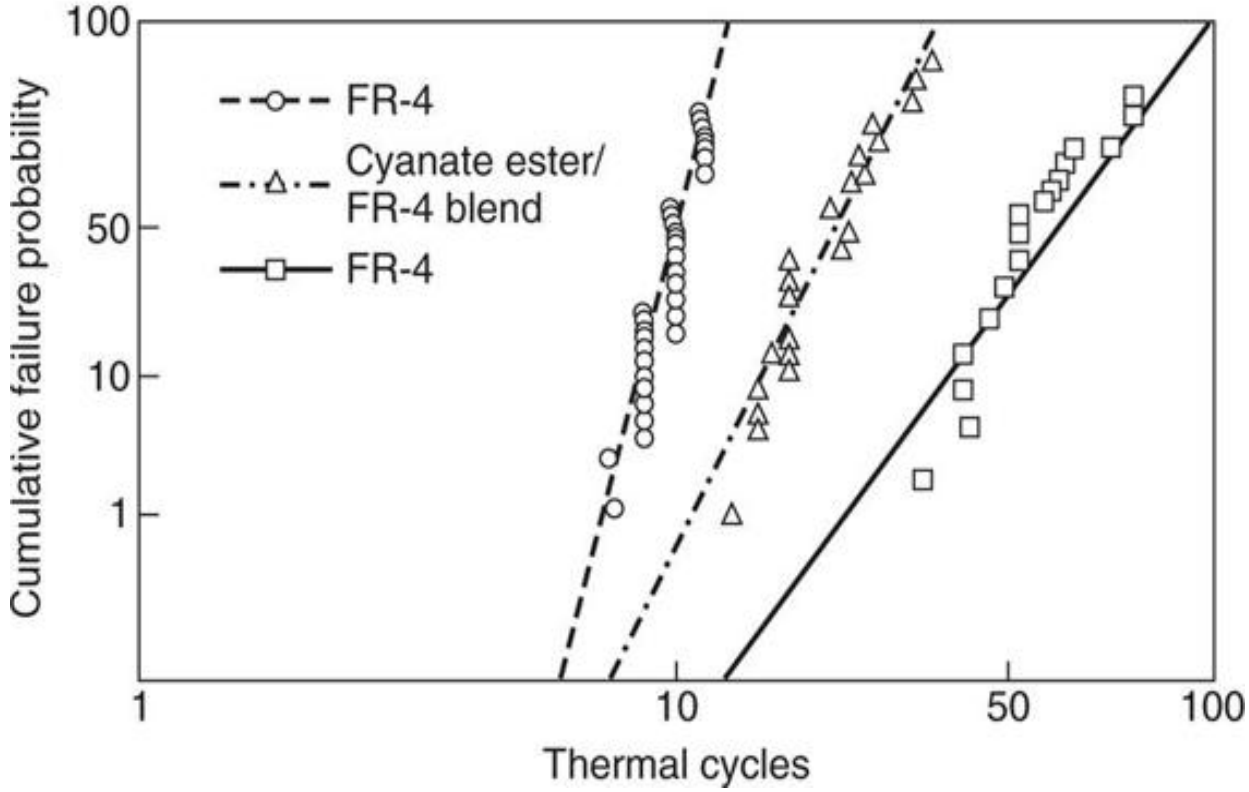


FIGURE 60.15 (*a*) Effect of differences in CTE below T_g and T_g on the free *z*-axis expansion of FR-4 (epoxy glass), cyanate ester (cyanate ester glass) and a cyanate ester/epoxy blend. T_g and CTE for each material below/above T_g are indicated. Cyanate ester is abbreviated CE in the figure. Cu is shown for comparison. (*b*) Weibull plot of PTH failures for these substrates during thermal shock cycling between 25 and 260°C. PTHs are 0.029-in diameter on 0.100-in grid on 0.125-in-thick laminate.[35]

Low-thermal-expansion metal cores or planes can also lower the overall substrate CTE because they constrain the expansion of the polymer material they are laminated to. Copper-invar-copper (CIC) is the most widely used material for constraining metal cores (also termed polymer-on-metal or POM construction), followed by copper-molybdenum-copper (CMC). The PCB and core are bonded with a rigid adhesive, usually in a balanced construction to minimize warping. Other special processing is also required. The CTE of the assembly can be estimated using a simple model for composite structures most often written as

$$\text{CTE(overall)} = \Sigma E\alpha t \,/\, \Sigma Et$$

where E, α, and t are the elastic modulus, coefficient of thermal expansion (CTE), and thickness, respectively, of the various layers. A more sophisticated model can be found in reference.[36] An example of the low overall CTE for a CIC core is shown in Fig. 60.16.

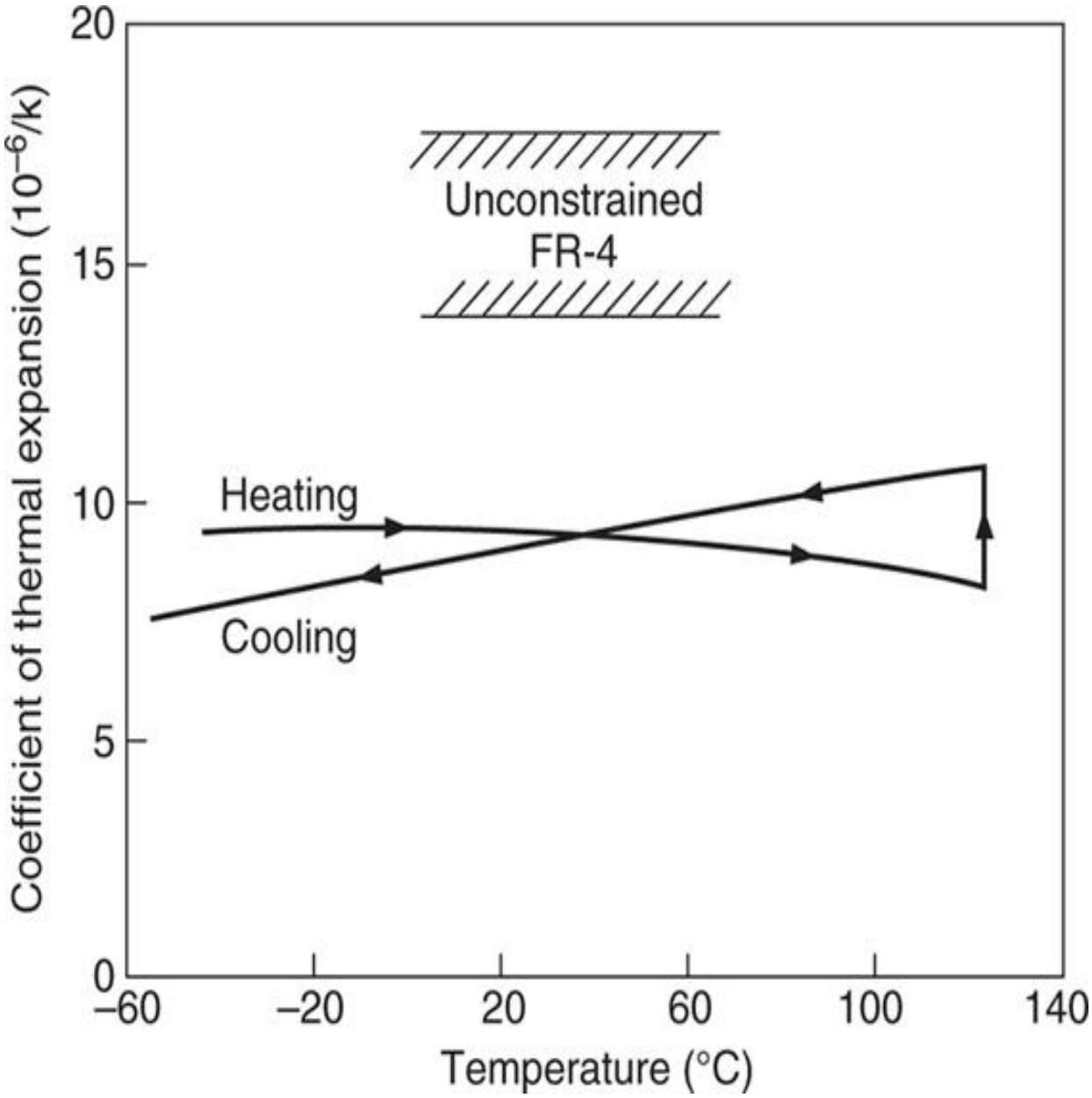


FIGURE 60.16 Example of the low overall CTE that can be achieved for a metal core construction. Two 1.4-mm-thick (0.055-in) multilayer FR-4 boards were bonded to a 2.2-mm-thick (0.085-in) copper-Invar-copper core.[13,30]

A variety of specialty resins with increased T_g is available, albeit at higher prices. Modified FR-4 materials with higher functionality offer the best combination of improved T_g at a reasonable price. Further improvements in T_g and other characteristics can be obtained with bismaleimide triazine

(BT), GETEK, cyanate ester, and polyimide, but at greater price penalties.

A lower *x*-*y* plane thermal expansion coefficient laminate can be obtained by replacing the continuous-filament E-glass used in most FR-4 PCBs with an alternative material. The CTE decreases as the fraction of silica dioxide (SiO_2) decreases and the level of quartz (as well as the cost) increases in the progression E-glass, S-glass, D-glass, and finally quartz, which has a CTE about one-tenth of E-glass. Aramid (Kevlar) actually has a negative CTE, but it is available in only a few glass styles. Some of the disadvantages of aramid fibers are higher *z*-axis expansion and higher moisture absorption relative to glass fibers that can result in decreased susceptibility to PTH failures and corrosion-related insulation resistance failures, respectively.

Because of its high T_g and low CTE below T_g, polyimide imposes much lower strains on the PTH for a given thermal cycle than other dielectrics. Resin material can affect fiber/resin delamination, one of the prerequisites for conductive anodic filament growth. Measling occurs at about 260°C for FR-4, but may occur at lower temperatures for boards with more hygroscopic resins.

60.3.5.2 Solder Mask. The three major types of solder mask—liquid screen-printed, dry film, and liquid photoimageable (LPI)—come with different benefits and concerns from a reliability perspective. The solder mask material should be selected for its compatibility with the heat and solvent characteristics of the assembly process, its capability to provide good conformity over surface features on the PCB, and its ability to tent vias if required. Since many of these characteristics are product-specific, only a few general guidelines can be provided here. Where tenting of vias is required to keep solder, moisture, or flux from wicking up under components, dry film solder mask should be used. However, excessively thick solder mask, particularly dry film

over closely spaced traces, can result in crevices. If the solder mask cannot flow enough to adhere closely to the board, the resulting crevices can entrap contaminants such as flux that can accelerate corrosion later. LPI solder mask provides excellent coverage, resolution, and alignment to other features, but it generally cannot be used to tent vias. IPC-SM-840 defines the performance and qualification requirements for solder mask.

60.3.5.3 Metal Finish. The metal finish on the SMT and TH pads can have an impact on PTH reliability and on the reliability of the solder joints made to these pads. Common metal finishes for solder-mask-over-bare-copper (SMOBC) boards include hot-air solder leveling (HASL or HAL), organic-coated copper (OCC), and electroless NiAu. Galvanically plated CuNiAu and CuNiSn made by another processing route are also available. These finishes provide a solderable finish for later printed circuit assembly. Of the common metal finishes, HASL is the only one that can directly reduce reliability of the board. In a typical HASL process, the board receives a severe thermal shock when it is dunked into a bath of molten eutectic Sn-Pb solder. The PTHs can survive only a certain number of solder shocks without failure; this process uses up one of these thermal cycles before the board leaves the fabricator.

CuNiAu boards fabricated either with the NiAu as the Cu etch resist or by the SMOBC process followed by electrolessly plating Ni and Au can confer improved PTH reliability. There are two mechanisms for the observed improvement: the enhanced rivet effect provided by the Ni and the elimination of Cu dissolution during solder shocks such as wave soldering or PGA rework. For high-aspect-ratio holes, electroless Ni confers an additional benefit because the plating thickness in the barrel is more consistent than for conventional electroplating.

In the simple picture of PTH failure shown in Fig. 60.17, the comparatively low CTE metal-plated PTH acts as a rivet that resists the *z*-axis expansion of the PCB. Because Ni has a higher elastic modulus than Cu, it strains less under the stress imposed by the expanding PCB. Consequently, adding Ni plating lowers the strain imposed on the Cu and lessens the amount of fatigue damage. In this model, the Ni protects the Cu, increasing PTH life.

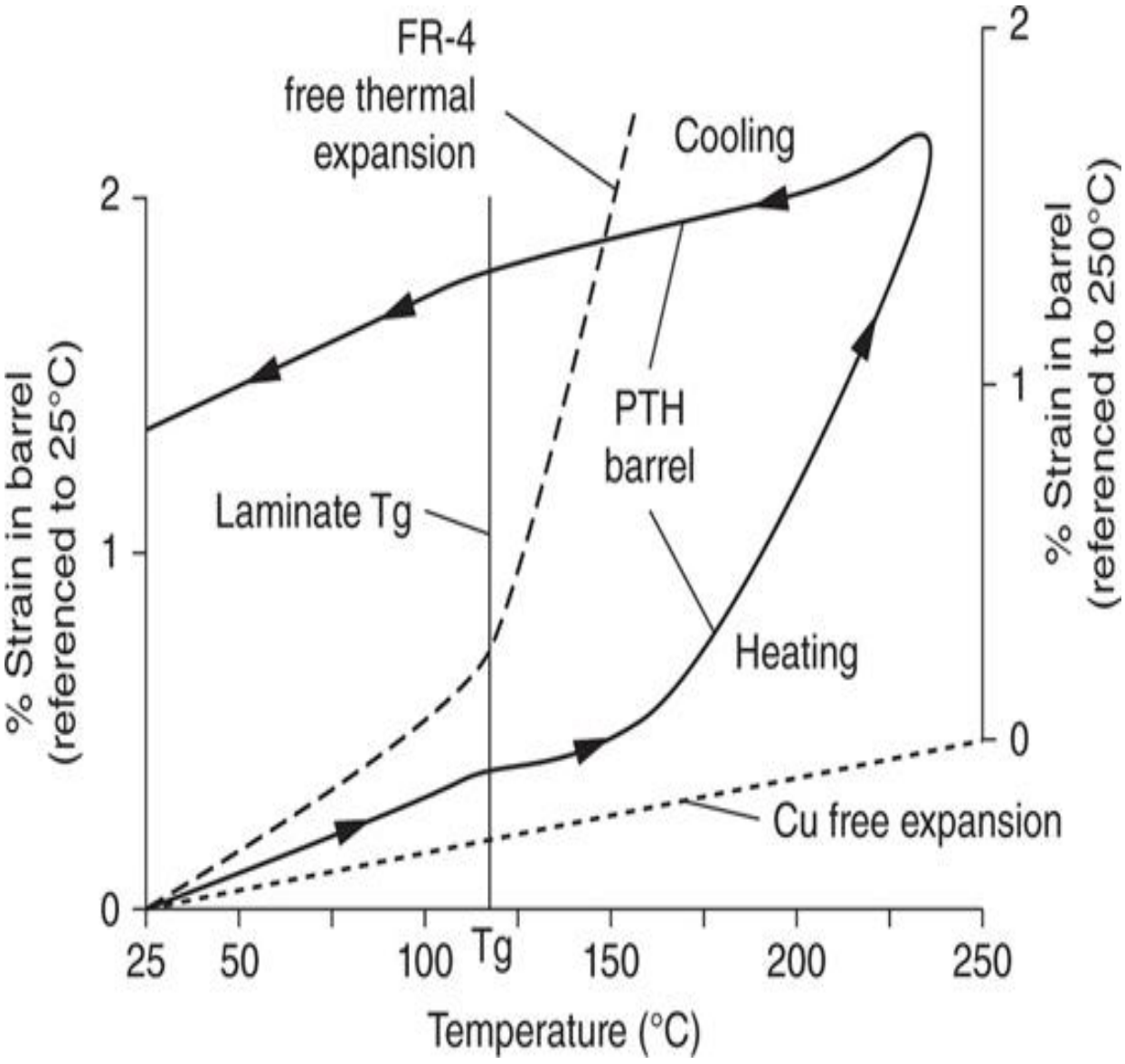


FIGURE 60.17 Strain versus temperature for FR-4 (epoxy glass), copper, and a PTH barrel in an FR-4 board during a single thermal cycle from 25 to 250 to 25°C.

While the thermal expansion of the individual materials is fully reversible, much of the strain in the Cu PTH barrel is plastic, so most of the strain is not reversed during cooling. Note that the rate of thermal expansion of the FR-4 increases sharply at T_g.[39]

The ability of the Cu to withstand the forces imposed on it by thermal expansion of the PCB is also dependent on the thickness of the Cu in the PTH. Unfortunately, in the SMOBC process all subsequent steps after pattern or panel plating reduce the Cu thickness from the plated amount. Nickel plating is resistant to the etches and developers used in later processing steps, so it protects the underlying copper from thinning due to dissolution. The HASL process and rework of large through-hole connectors or pin grid arrays (PGAs) can have particularly negative effects. Cu dissolves rapidly into molten eutectic Sn-Pb solder. During the HASL process or component removal and replacement with a solder fountain, large amounts of Cu can dissolve from the knee of the PTH. Nickel barrier plating minimizes this effect because Ni dissolves far more slowly in eutectic Sn-Pb solder than Cu does.

Use of Au plating can embrittle the eutectic Sn-Pb solder most commonly used in electronic assembly. Gold plating of various thicknesses is used for a variety of reasons, including as a solderability preservative over nickel plating, for connector contacts, and to provide wire-bondable pads. Reliability problems can arise because Au has a high solubility in eutectic Sn-Pb solders at reflow temperatures and dissolves extremely rapidly. In most cases, the Au finish on a PCB or component termination will be completely dissolved into the solder. In a wave-soldering process, the Au is washed into the bath, requiring monitoring and bath changes to maintain the Au concentration at a low level that does not affect the process. However, in a reflow process, this Au remains in the finished solder joint. To avoid embrittlement of the solder by the $AuSn_4$ and $AuSn_2$

intermetallics that can form, the Au concentration should be kept below a critical level that most authors set at 3 to 5 percent by weight.[37,38]

60.4 PTH THERMAL CYCLE RELIABILITY AND PROJECTIONS METHODS

Plated-through holes (PTHs) and microvias are the most vulnerable features on PCBs to damage from thermal cycling and the most frequent cause of PCB failures in service. PTHs include holes for through-hole (TH) components and vias that make electrical connections between layers. Most organic resin-matrix substrate materials are highly anisotropic, with a much higher CTE above the glass transition temperature T_g in the through-thickness (z) direction than in the plane of the woven matrix cloth (the x-y plane of the board). Since above T_g the CTE climbs sharply, aggressive thermal cycles can result in large strains in the z direction and, consequently, on the PTHs. The PTH acts like a rivet, which resists this expansion, but the Cu barrel is stressed and may crack, causing electrical failure. Figure 60.17 illustrates the increasing strains on the barrel associated with low- to high-temperature excursions, especially excessive strains above the T_g excursion.

Failure may occur in a single cycle or may take place by initiation and growth of a fatigue crack over the course of a number of cycles. PTHs are subject to repeated thermal shocks from room temperature to solder reflow temperatures (220 to 250°C during board fabrication (e.g., hot-air solder leveling) and assembly (reflow, wave soldering, and rework). For high-aspect-ratio PTHs, these thermal cycles are severe and potentially could cause failures after 10 or even fewer of

these cycles. PTH fails in a number of ways depending on the stress condition and the weakest points. A representation of these failure mechanisms is shown in Fig. 60.18. In the following sections, models that have been developed to address each specific failure mechanism are addressed.

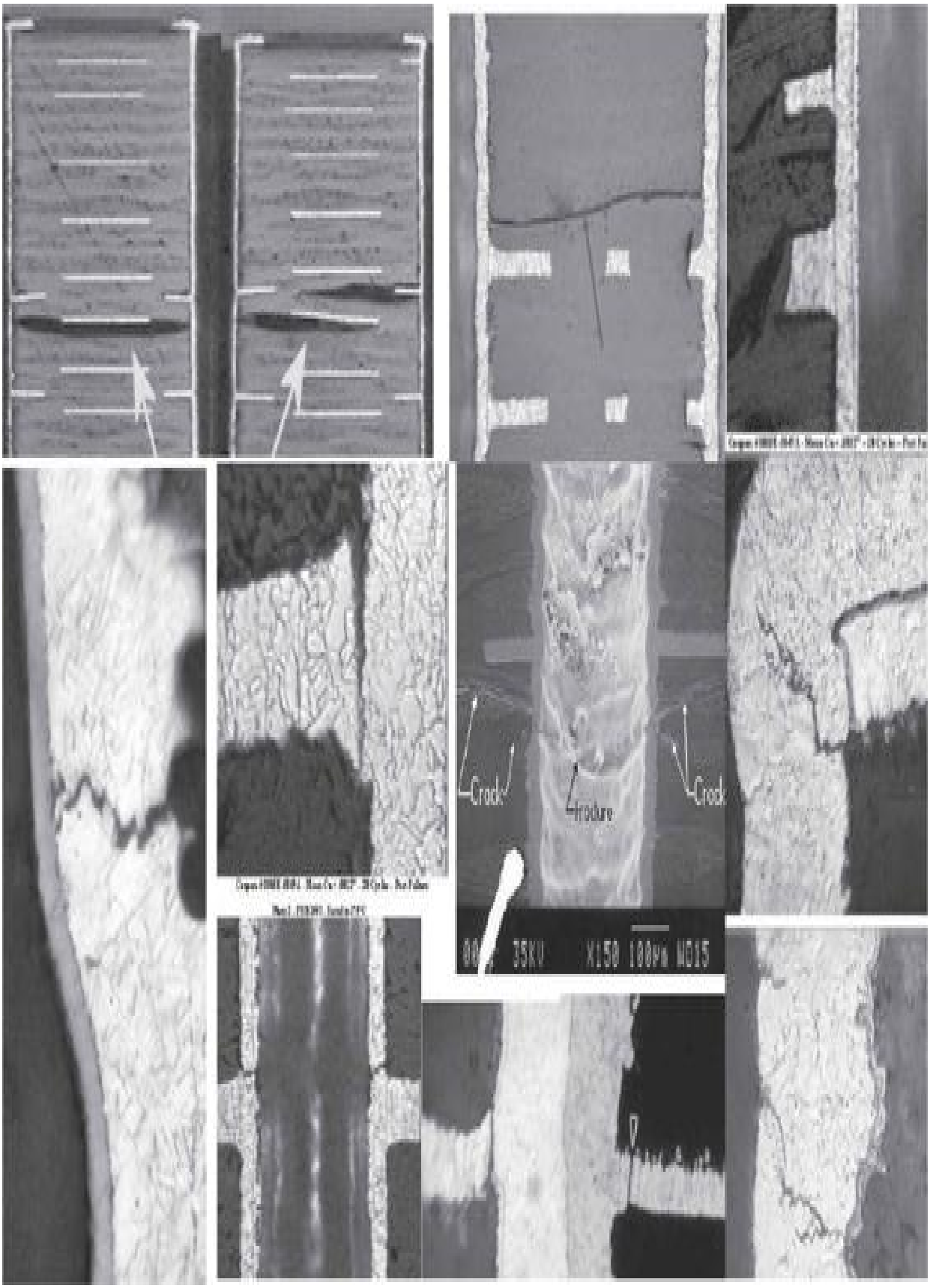

Crack
Fracture
Crack
X150 100μm WD15

FIGURE 60.18 Representation of Cu PTH failure mechanisms.

60.4.1 Coffin-Manson Relationship

On a physical level, the number of thermal cycles to failure is affected by the strain imposed on the Cu PTH in each cycle and the fatigue resistance of the copper.[40] These factors are, in turn, controlled by a number of environmental, material, and manufacturing parameters. Low-cycle metal fatigue, in which most of the strain is plastic strain, can be treated approximately with the Coffin-Manson relation:

$$N_f \propto \frac{1}{2}(\varepsilon_f/\Delta\varepsilon)^m$$

where N_f = number of cycles to failure
$\Delta\varepsilon$ = strain
ε_f = strain ductility factor, which correlates closely with tensile ductility
m = constant near 2

This relation significantly underestimates life for high cycle fatigue, which can occur after repeated thermal cycling in service. The strain $\Delta\varepsilon$ can be estimated by finite element modeling or analytically. If no other data are available, ε_f for electroplated Cu can be approximated as 0.3. The number of cycles to failure can be increased by increasing $\varepsilon_f/\Delta\varepsilon$, primarily by decreasing $\Delta\varepsilon$.

There are, however, issues with the use of the simplified Coffin-Manson relationship since real PTH behavior is confounded by a number factors[11] including (1) physical limitations such as

- Anisotropy of thermal expansion (x and y versus z)

- Lack of homogeneity between glass and resin layers (different CTEs)
- Microstructural features that have the same scale as the PTH structure itself (grain size = Cu thickness)
- Large variations in mechanical properties (i.e., ductility) from lot to lot and board to board (even in well-controlled conditions)
- Defect structures (i.e., glass fibers and Cu grain boundaries) interacting at geometric strain concentrations (barrel/pad junction)
- Cu dissolution in solder pot (or Pb-free HASL) repair processes
- The catastrophic nature of the failure

And (2) simplifying assumptions that do not meet reality including

- Steady-state temperature distribution
- Uniform metal thickness
- Room temperature properties of copper
- No strain rate effects on copper properties
- Perfect registration of hole to pattern

A semi-empirical relationship developed as part of IPC round-robin testing to better define key parameters affecting reliability of PTH under thermal cycling.[11] This and other models are discussed in the following sections.

60.4.2 Semi-empirical Relationship

A semi-empirical analytical relationship was proposed for low-cycle fatigue mechanisms under thermal cycling. Figure 60.19 shows this relationship and detailed parameters required to calculate the mean cycles to failure.

$$\overline{N}_f^{-0.6} D_f^{0.75} + 0.9 \frac{S_u}{E} \left[\frac{\exp(D_f)}{0.36} \right]^{0.1785 \log \frac{10^5}{N_f}} = \Delta\varepsilon_{max}(\text{eff})$$

Plastic Strain Low-Cycle Fatigue

Elastic Strain High-Cycle Fatigue

Effective Cyclic Strain Range

$\overline{N}_f$ = mean cycles to failure

D_f = fatigue ductility from IPC-TM-2.4.2.1

S_u = ultimate tensile strength

E = modulus of elasticity

$$\Delta\varepsilon_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T}{1+\gamma}, \quad \text{if } \sigma_{avg} \le S_y$$

where $\sigma_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T E_{Cu}}{1+\gamma}$ and $\gamma = \frac{E_{Cu} A_{Cu}}{E_E A_E}$

α_E, α_{Cu} = CTEs of epoxy, copper

S_y = yield strength of ED copper

E_{Cu}, E_E = modulus of elasticity of copper, epoxy

A_{Cu}, A_E = load-bearing area of copper, epoxy

$$A_{Cu} = \frac{\pi}{4}\left[d^2 - (d-2t)^2\right], \text{ load-bearing area of copper}$$

$$A_E = \frac{\pi}{4}\left[d_E^2 - d^2\right], \text{ load-bearing area of resin}$$

d = drilled hole diameter

t = thickness of barrel wall

d_E = diameter of area of influence of PWB (undefined)

h = thickness of PWB

$$\Delta\varepsilon_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T E'_{Cu} - \gamma' S_y (1 - E'_{Cu}/E_{Cu})}{(1+\gamma')E'_{Cu}}, \quad \text{if } \sigma_{avg} > S_y$$

where $\sigma_{avg} = \frac{(\alpha_E - \alpha_{Cu})\Delta T E'_{Cu} + S_y(1 - E'_{Cu}/E_{Cu})}{1+\gamma'}$

and $\gamma' = \frac{E'_{Cu} A_{Cu}}{E_E A_E}$

E'_{Cu} = modulus of plasticity of ED copper

FIGURE 60.19 Semi-empirical model for projection of cycles-to-failure for Cu PTH in PCB.[11]

Figure 60.20 shows the plot of this relationship showing the effective strain in percent versus the average number of thermal cycles. Assumptions made for the PTH properties are also shown. Figure 60.21 shows a similar plot, which also includes the range of cycle-to-failure and experimental test data from another source.[41]

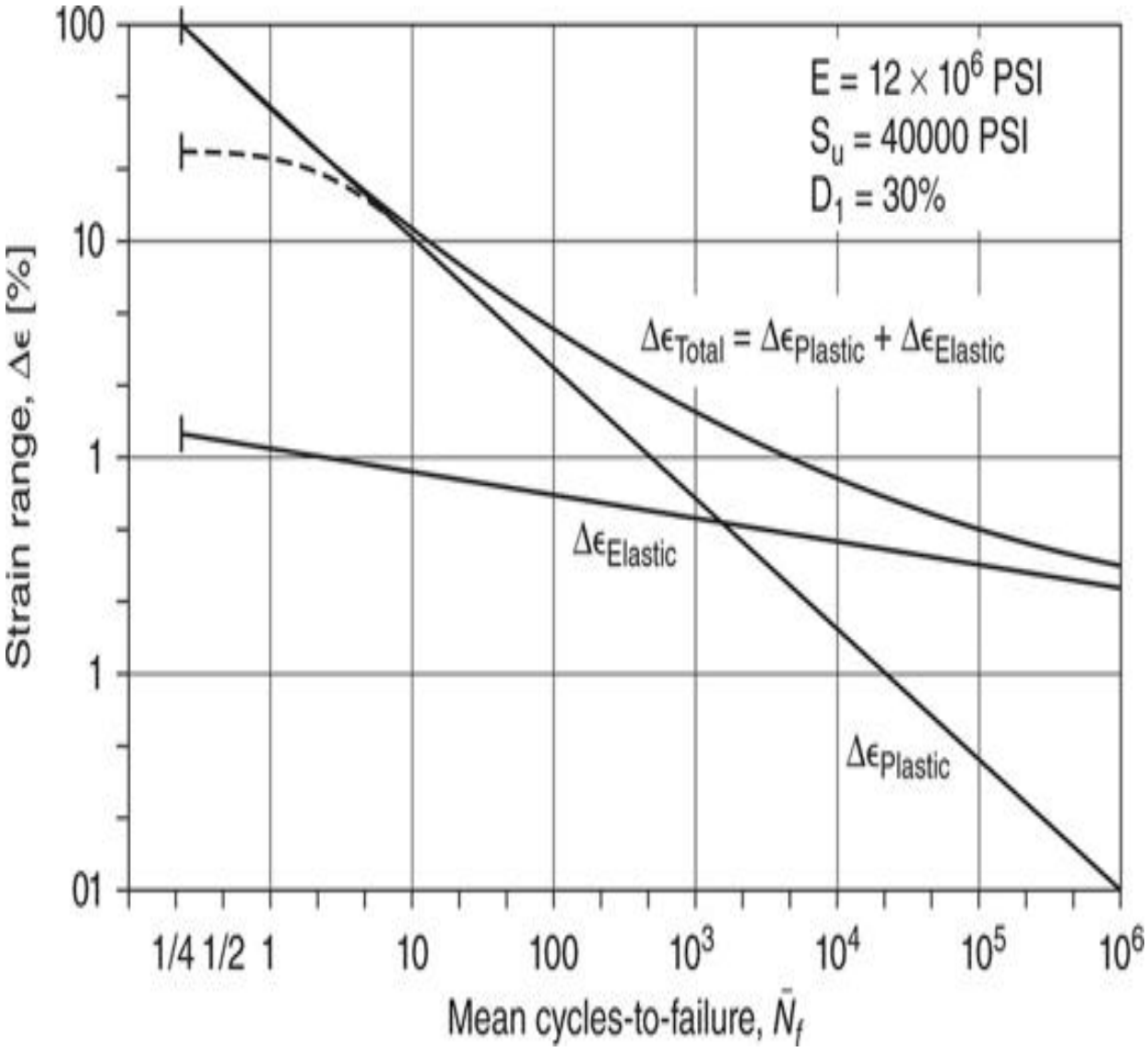


FIGURE 60.20 Semi-empirical relations (Coffin-Manson) strains versus fatigue life plot for electrodeposited copper.[11]

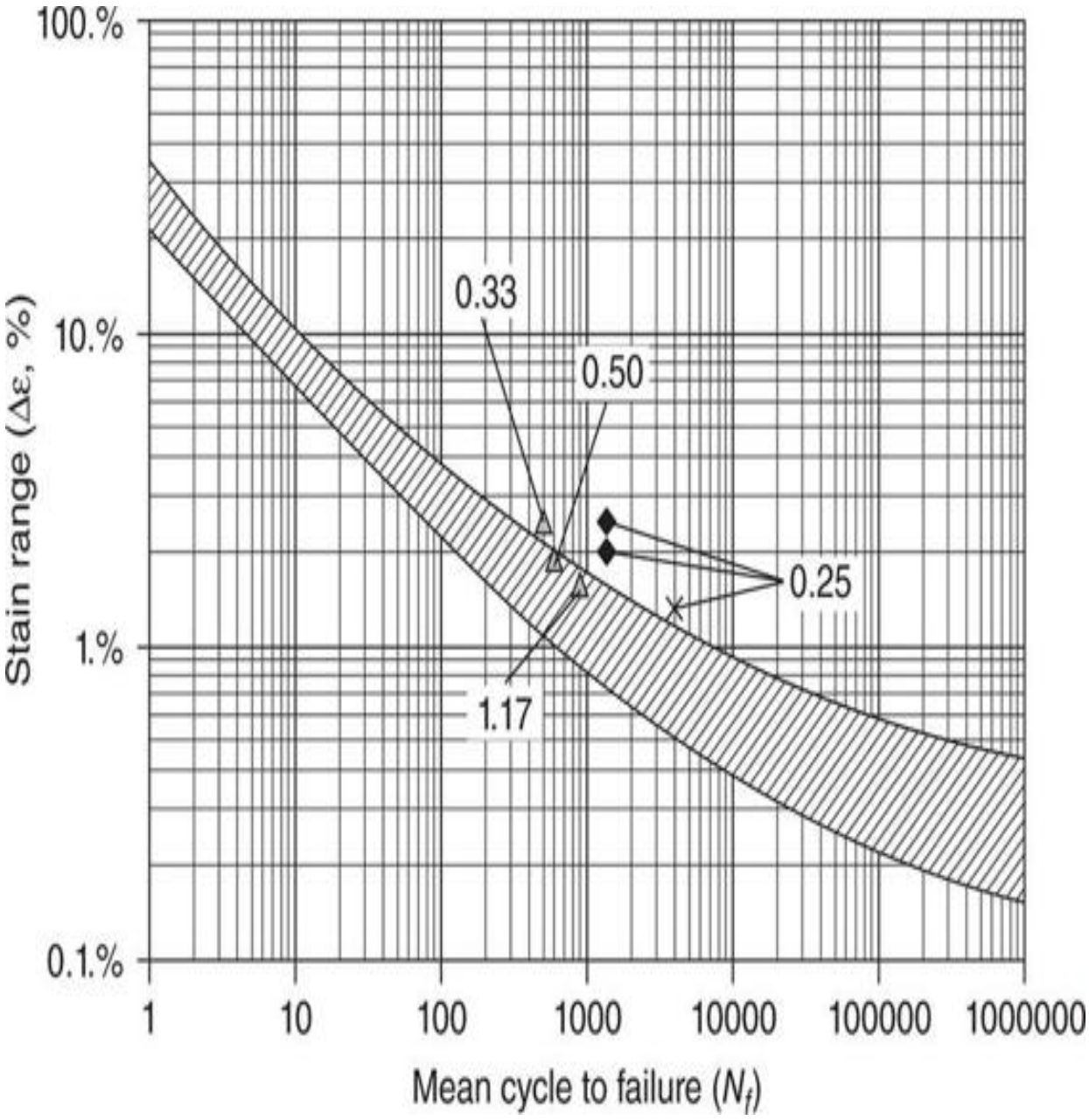


FIGURE 60.21 Shaded area is the life prediction from several copper fatigue models, triangles, diamonds, and one "X" are the experimental test data with strain ranges calculated by 3D the FE model.[41]

Life calculation for PTHs subjected to thermal cycling is a three-step process. The first step is to calculate the stress being experience by the Cu barrel of the PTH. Two simple formulas are assumed for calculation: (1) a linearly perfectly elastic behavior for below-yield strength, and (2) a linear

stress-strain relationship above the yield strength (see Fig. 60.22). It is further assumed that there are infinitely stiff outer lands and no inner lands. The PTH stresses are transferred to strains since strains are important to determining cyclic fatigue life to cyclic fatigue damage. The average cycles-to-failure, then, is calculated by iteratively solving the semi-empirical relationship.

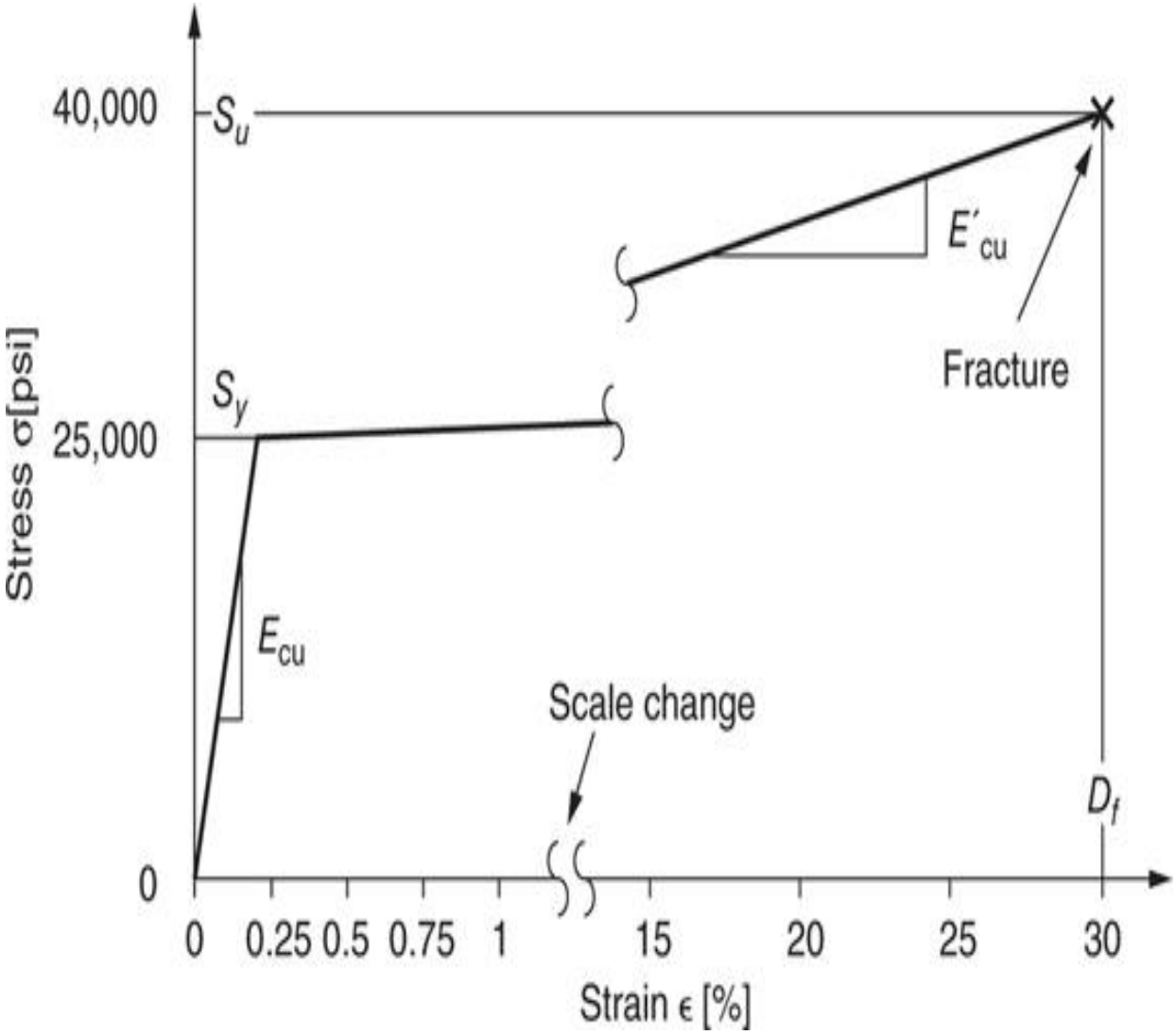


FIGURE 60.22 Linearized stress-strain diagram for electrodeposited copper (S_u = 40,000 psi, S_y = 25,000 psi, $E_{cu} = 12 \times 10^6$ psi, D_f = 30%).[11]

Round-robin test data indicated distribution cycles-to-failure due to severe strain concentration and PTH Cu nonuniformity properties. In addition, the assumption was made that properties are independent of temperature and time over the entire thermal cycle temperature range. In addition, the strains need to be adjusted by two other factors: a strain distribution factor, K_d and a PTH quality factor K_Q.

$$\Delta\varepsilon_{\text{eff}} = K_d\, \Delta\varepsilon\, (10/K_Q)$$

Table 60.3 lists cycles-to-failure test data from round robin[11] with predicted mean fatigue lives for various use environment using semi-empirical model for PTH. It includes CTF projections for marginal quality ($K_Q = 5$) and superior quality ($K_Q = 10$) of plated conditions.

TABLE 60.3 Predicted Mean Fatigue Lives for Marginal Quality ($K_Q = 5$) and Superior Quality ($K_Q = 10$) Plated-Through Hole Subjected to Ddifferent Tests/Cycles Environment[11]

	Plated-Through Hole Design Parameters			
	Plating Thickness = 0.75 PTH Diameter = 10 PWB Thickness = 90		1.25 mils 20 mils 30 mils	
Cyclic Stress Test: Environment [°C]	$K_Q = 5$	10	$K_Q = 5$	10
IEC OIL-T-SHOCK & FLUID SAND-T-SHOCK: +25/+260°C, ΔT = 235°C	74	307	144	667
MIL-T-CYCLE: −65/+125°C, ΔT = 190°C	114	506	284	1,530
APD OIL-T-SHOCK: −35/+125°C, ΔT = 160°C	161	763	533	3,510
COM-T-CYCLE: 0/+100°C, ΔT = 100°C	463	2900	2,850	47,300
USE ENVIRONMENTS:				
−40/+80°C, ΔT = 120°C	302	1,660	1,690	19,600
−40/+40°C, ΔT = 80°C	811	6,340	5,980	184,000
+20/+80°C, ΔT = 60°C	1,830	22,200	19,100	1,660,000
+20/+40°C, ΔT = 20°C	230,000	91,000,000	66,300,000	55,000,000,000

* $S_u = 40{,}000$ psi, $D_f = 30\%$, $E_{cu} = 12 \times 10^6$ psi, $K_f = 2.5$

In summary, the designer and the PCB manufacturer have the following controls over the reliability of PTHs.

- Out-of-plane CTE of the printed board

- Plating thickness
- Aspect ratio (hole diameter over board thickness)
- Plating material properties (strength and ductility) and plating quality

One limitation of the semi-empirical model[42] is its dependence upon the quality of the PTH (i.e., the presence of defects such as voids, cracks, folds, etc.) whereas the strain distribution factor tends to be set to a value of 1.6. The quality factor, K_Q, can range from 0 to 10 with the following delineations

- Extraordinary (K_Q = 10)
- Superior (K_Q = 8.7)
- Good (K_Q = 6.7)
- Marginal (K_Q = 4.8)
- Poor (K_Q = 3.5)

For validation of a software that was developed for analytical PTH reliability prediction,[42] a quality factor was used to capture the sensitivity of the PTH to the quality of Cu plating. Quality factors were identified by two approaches: (1) by assuming a conservative quality factor, either good (K_Q = 6.7) or marginal (K_Q = 4.8) and (2) by calculating the quality factor from the IST or HATS test results.

The two-parameter Weibull probability distribution was used to describe the failure behavior of the PTHs. The Weibull distribution is generally accepted as a good distribution for reflecting low cycle fatigue behavior of ductile metals. Two key parameters in distribution are the characteristic life and the shape factor (slope). The slope typically describes the quality and the higher the slope the closer the time to failures are.

As stated, the PTH reliability prediction depends on a quality factor that may not be known in the design state. The quality factors were derived from published test data (see Table 60.4) to provide guidance on values that should be selected during design evaluation.[42]

TABLE 60.4 Quality Factors Calculated from Published Test Ddata[42]

Reference	[1][2]	[1][3]	[2]	[3]	[4]
Year Published	1988	1988	1997	2000	2002
Hole Diameter (mm)	0.25	0.33	0.35	0.30	0.34
Plating Thickness (mm)	20	32	25	30	25
Board Thickness (mm)	2.28	2.28	1.5	1.5	2.36
Out-of-Plane CTE (ppm)	70	83	63	50	N/A
Mean Time to First Failure (thermal cycles)					
-35 to 125C	300	N/A	N/A	N/A	N/A
-40 to 125C	N/A	N/A	N/A	N/A	750
-55 to 125C	N/A	N/A	925	2190	N/A
-65 to 125C	N/A	371	N/A	N/A	N/A
Calculated Quality Fador	6	8	7.5	7.2	9

Barker and Dasgupta[43] performed modeling studies to determine critical stresses in PTH and to determine qualitatively the effect of several geometric parameters. The parameters investigated included PTH spacing, inner-planes, nonfunctional internal pads, aspect ratio, plating thickness, solder filling with and without voids, and transient thermal

stresses due to the wave soldering process. The model was an idealization ignoring manufacturing flaws, such as plating thickness, variations, presence of stress concentrations, and interfacial delamination. The findings are summarized in the following:

- Decreasing PTH spacing improves mechanical reliability.
- Decreasing aspect ratio (thickness/radius) either by decreasing PCB thickness or by increasing PTH diameter is beneficial, with PCB thickness having a more pronounce effect.
- For FR-4 PCB materials, the effect of solid inner-planes, nonfunctional internal pads, and functional signal layers resulted in local stress relief in the vicinity of inner-planes/pads/layers. However, local stress increased for Kevlar-polyimide PCB materials.
- Solder filling with and without some voids did not significantly affect the critical PTH barrel stresses; which were also found to be independent of the PCB material.
- The PTH exposed to a wave soldering showed two opposing effects on the life of the PTH. The transient thermal stress consumed 33 percent of life whereas improved 25 percent of life due to compressive stresses upon cooling.

In another approach, the authors presented a simplified PTH analytical model to project the effect of various parameters, including influence of CTE and PTH, on cycles to failure (see Fig. 60.23).[44] In addition, the author performed experimental tests using IST coupon and subjection to thermal cycling in the range of RT to 150°C to determine the effect of PCB materials properties, surface finish, and drill diameter (see Table 60.5). As expected, material A with a lower T_g and a higher CTE showed the lowest CTF (~370 cycles) whereas material C with the lowest CTE and a lower

T_g showed the highest CTF (~2900 cycles). On the effect of PTH surface finish, the material with the highest Young's modulus and the lowest CTE (ENIG) yielded the highest CTF even though the thickness of ENIG was slightly lower than HASL. The test result on the effect of PTH surface finish is shown in Fig. 60.24.

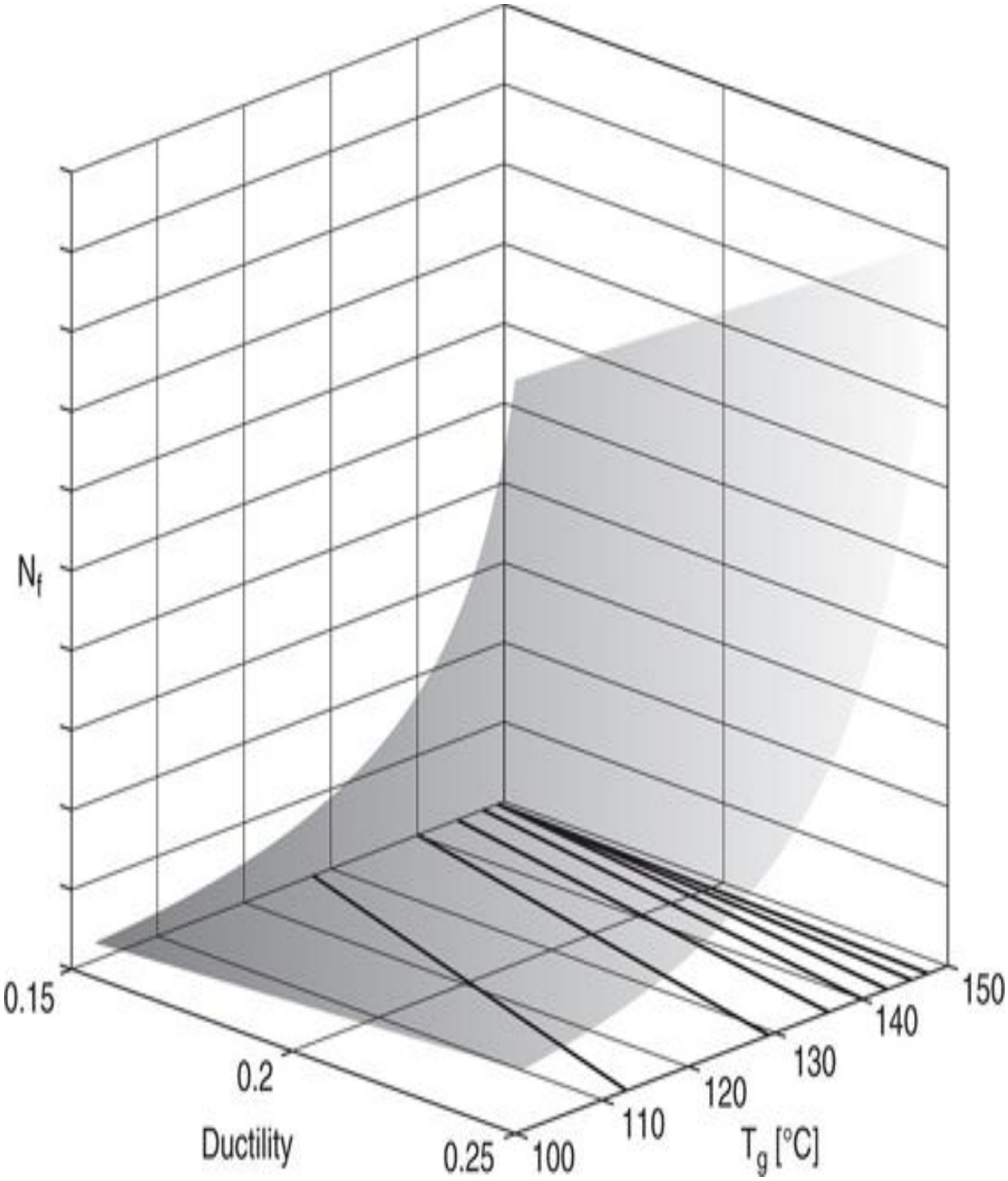


FIGURE 60.23 Projected Cu PTH cycles-to-failures versus Cu ductility and PCB glass transition (T_g) in the *z* direction.[44]

TABLE 60.5 Cycles-to-Failure from IST Coupon (RT/150ªC) and the Effects of (1) Z-CTE (α_{epoxy}), (2) Surface Finish, and (3) Effect of Ddrill Size[44]

Properties	T_g °C	α_{epoxy} $T < T_g$, ppm/K	α_{epoxy} $T > T_g$ ppm/K	CTF IST RT/150°C
Material A	138	61	278	370
Material B	144	60	255	1300
Material C	170	42	200	>2932

Finish Type	Thickness	Young's Modulus, KN/cm^2	CTE, ppm/K	CTF IST RT/150°C
ENIG	5.5 µm	20000	13	1500
HASL	7.6 µm	3500	25	1100
Sn	2.3 µm	5300	27	950

Approach	Size	CTF IST RT/150°C
Drill	$d < 350$ µm	400
Drill	$350 < d < 650$ µm	800
Drill	$650 < d < 1000$ µm	870

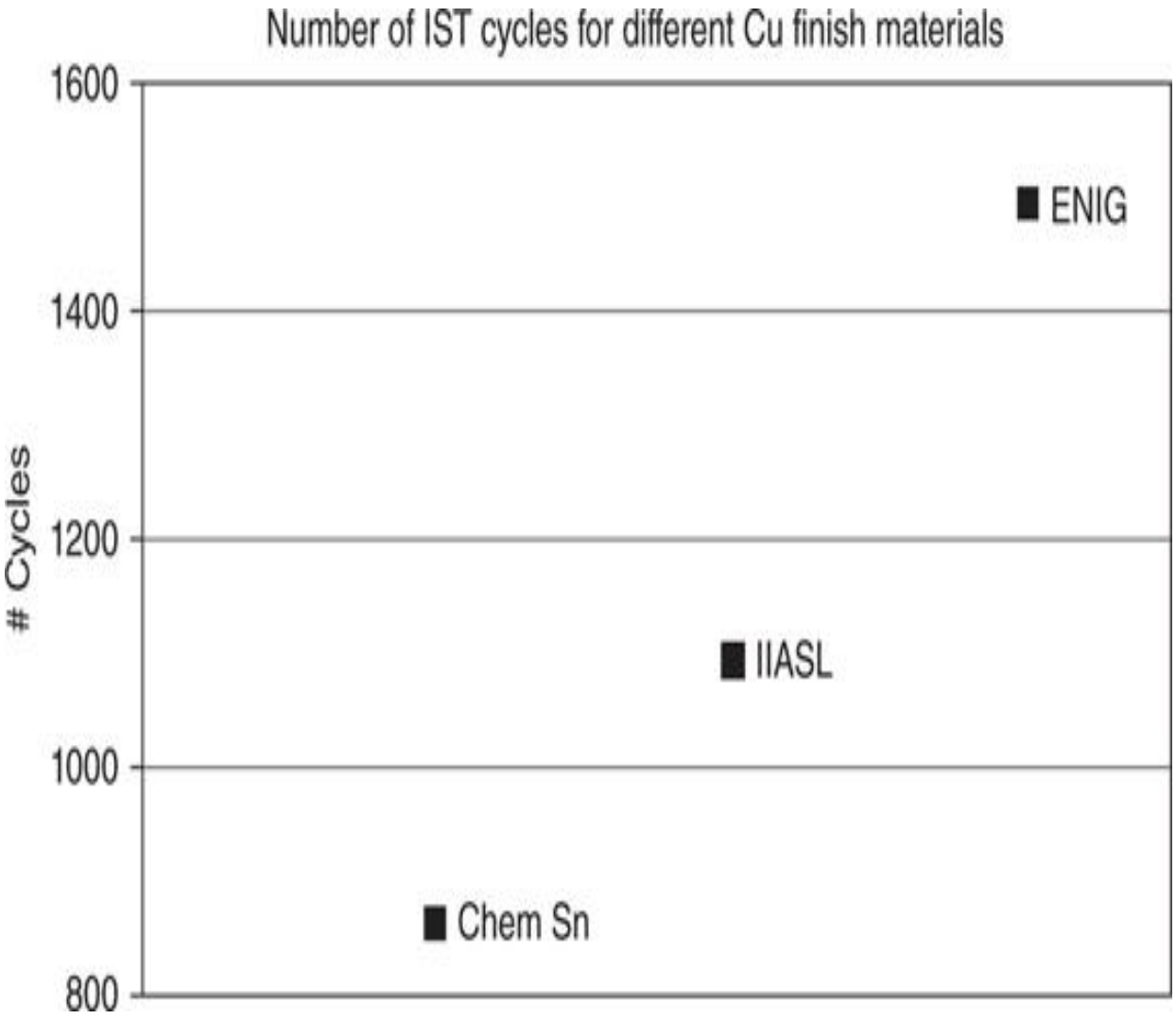


FIGURE 60.24 Effect of surface finish on cycles-to-failure.[44]

Goyal et al. performed both experimental and FEA analyses to determine the effect of various design and manufacturing parameters on reliability of high density PTH PCBs with and without solder fill.[45] The PTHs were subjected to 1000 thermal cycles in the range of −55 to 125°C (condition B) and −65 to 150°C (condition C). No failure of PTHs with solder fill via to 1000 cycles; however, the no-fill PTHs showed failures at various cycles that increased with increase in thermal cycling. The cumulative failures under condition B at 100, 200, 500, and 1000 cycles were 1, 3, 24, and 59 percent, respectively. The cumulative rates of failures

were higher under condition C and at 200, 500, and 1000 cycles were 10, 82, and 100 percent, respectively. Failures were due to PTH barrel necking and cracking with classical cup and cone features indicating ductile fracture of the plating. The fracture was found to occur near the center of the PCB thickness. The entire circumference showed cracking that initiated from the inside edge of the plating and propagated into the PCB material. The cracking of the PTH plating was also initiated from the regions of defects such as voids in the plating and/or at the plating to the PCB interface. The FEA analytical modeling showed the following key findings:

- The CTE mismatch (mainly along *z* direction) between Cu and organic laminate was the cause of excessive stress in the PTH barrel. The higher the CTE in the laminate structure, the larger the thermal fatigue damage at the barrel. Also, it was found that an increase in PCB thickness by 20 percent resulted in increases of 8 to 30 percent to the Cu layer stress.
- The increase in Cu plating thickness from 12 to 38 µm (0.5 to 1.5 mil) reduced its thermal stress by 25 to 70 percent while an increase in Ni plating thickness from 2.5 to 15 µm (0.1 to 0.6 mil) resulted in lowering the Cu plating layer stress by 30 to 70 percent. It was found that increasing the Ni plating thickness had a larger effect than increasing the Cu plating thickness in lowering Cu plating thermal stress. Also the results suggested use of a Cu layer with higher ductility and lower yield strength to minimize the PTH barrel fatigue damage generated in T/C stress.
- The use of solder-filled vias should reduce the thermal fatigue stress of the PTH barrel plate by 20 to 70 percent, depending on the plating material properties and the PCB layup. Different filling materials have varying impact on via thermal fatigue performance. However, the one with a

CTE value close to that of Cu would provide the most improvement in the reliability of the PTH.

In a more recent publication,[46] FEA simulation results calculated for total strains (elastic plastic strains) were compared to those presented by the IPC's semi-empirical model. A better correlation was found when failure was based on 20 percent changes in the daisy-chain resistance of vias. The FEA numerical results for the PCB/PTH specimen for the thermal cycle range of −30/150°C shown in Fig. 60.25*a* shows that the maximum von Mises stress occurs at the middle part of PTH during thermal cycle, it was 229.0 MPa at 150°C and 232.7 MPa at −30°C. The maximum residual strain at the center was 9613 μm (378 mil). The relevant simulation results are shown in Fig. 60.25*b*.

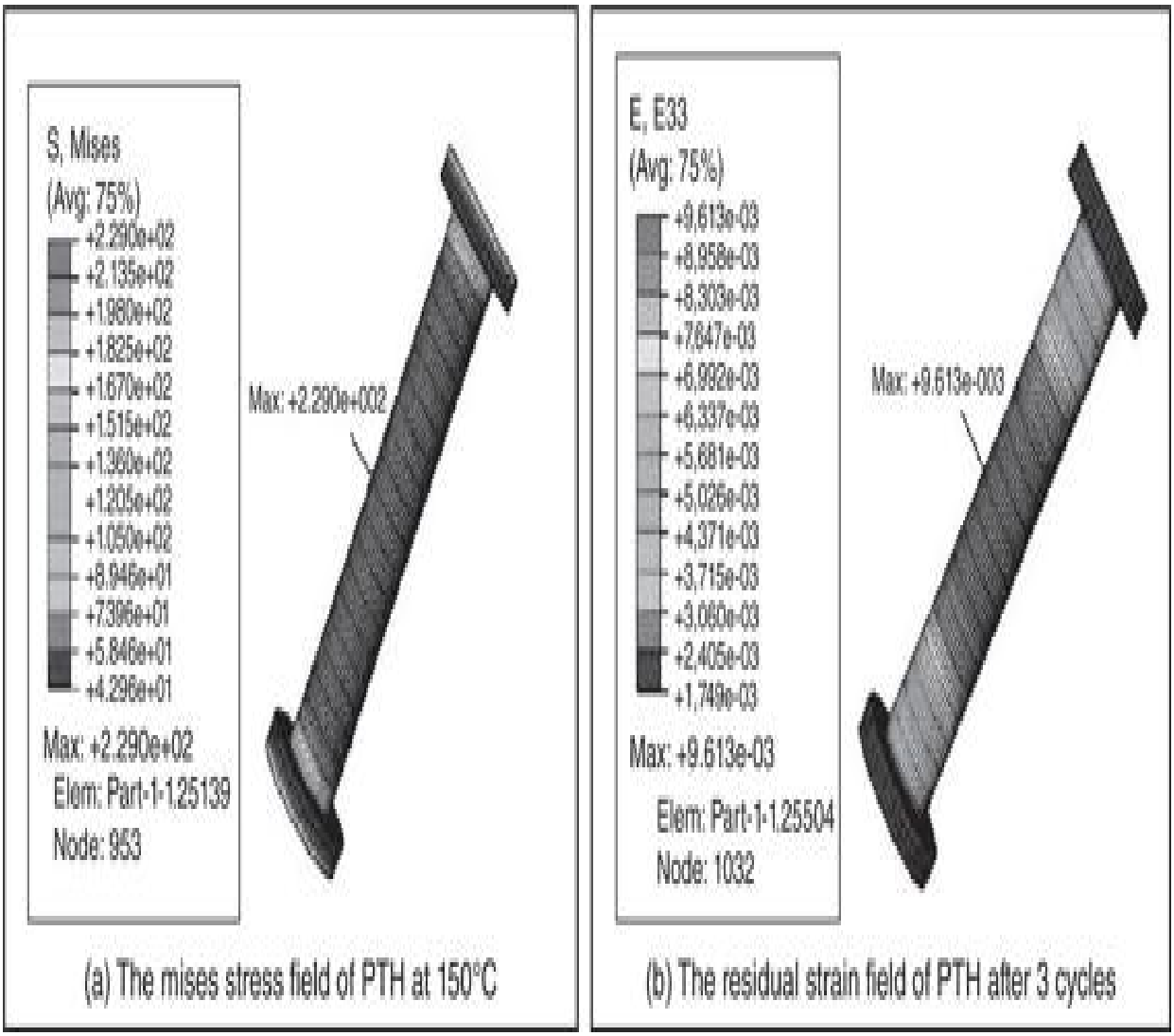


FIGURE 60.25 Finite element simulation of PTH for thermal cycle range of −30/150°C: (*a*) the maximum Von Mises stress is in the PTH center with 229.0 MPa at 150°C and (*b*) the maximum residual strain, 9613 μe.[46]

FEA with experimental thermal cycle (−65/125°C) tests were carried out to determine the key factors affecting the PTH thermal cycle reliability of rigid-flex printed circuit (RFPC), a laminate with mix of rigid and flexible substrates.[47] Both FEA and failures of RFPC test coupons revealed that the maximum barrel strain was not located at the center of PTH, but depended on the properties of bonding material, plating thickness, drill hole size, and board thickness. The use of

acrylic adhesive with a lower T_g resulted in a larger strain than the epoxy polyimide adhesives (see Fig. 60.26).

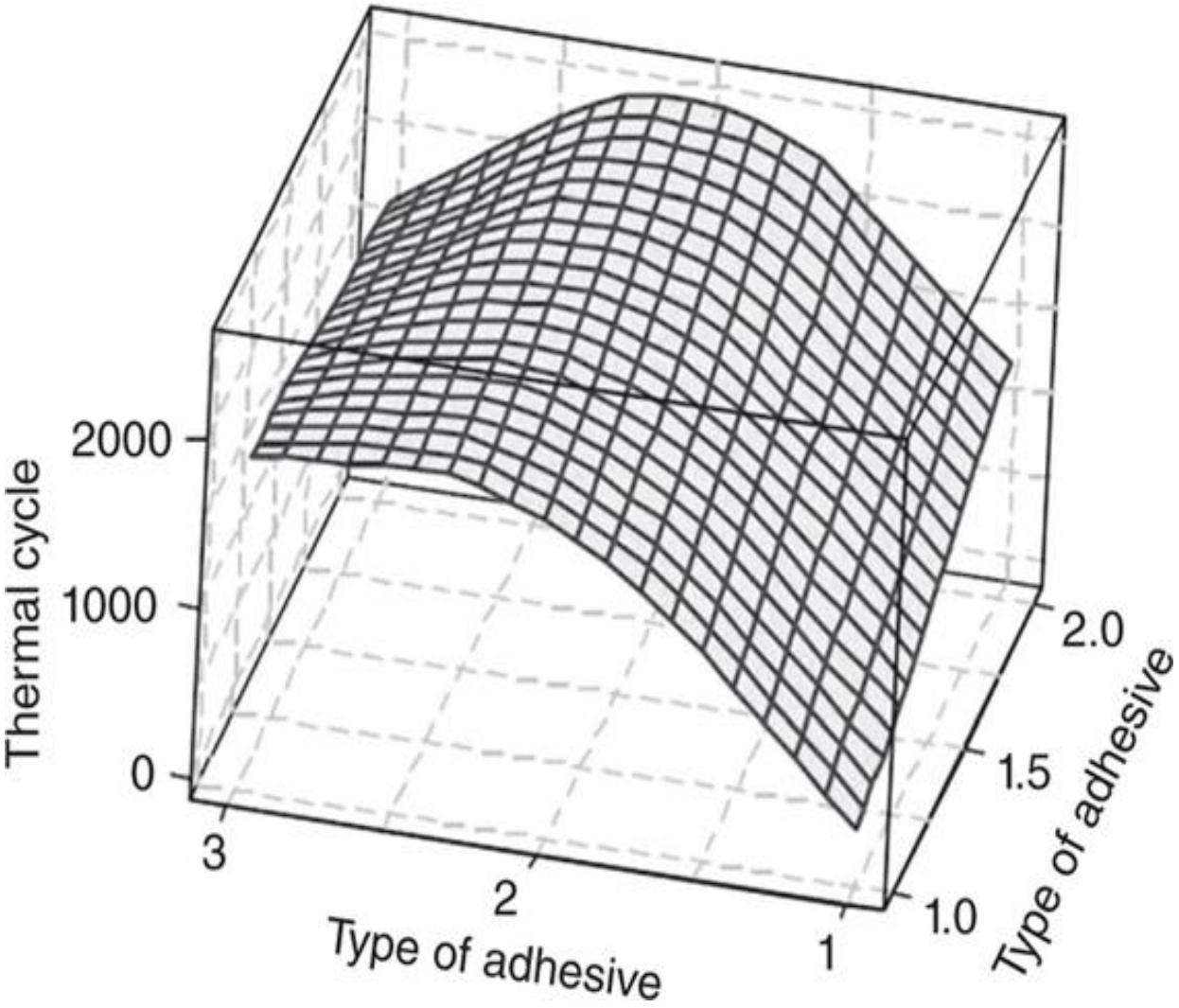


FIGURE 60.26 D surface plot of thermal cycle versus type of adhesive and plating thickness.

60.4.3 Inverse Power Law Relationship

Freda and Barker used the inverse power law (IPL) relationship for projection of PTH reliability under thermal cycling.[48] It was stated that IPL is widely used for nonferrous

metals such as Cu. Models such as those of Arrhenius or Eyring are not appropriate for the PTH since they deal with failure modes that are thermally induced. The authors applied the IPL relationship to project life or correspondent stress versus temperature cycles-to-failure.

The equation for the IPL relationship, after a logarithmic transformation, follows a conventional linear line. The relationship and log/log scale are

$$L(V) = 1/KV^{n}$$

$$\mathrm{Log}_{10}\, L(V) = -n \log_{10} V - \log_{10} K$$

where L = a quantifiable life measure; for this paper both mean life and T_1% percent life are used

V = the stress level

K = one of the model parameters to be determined, $K > 0$

n = another model parameter to be determined

To generate the IPL relationship, Freda and Barker[48] used the IST test coupons[16] to determine the effect of maximum temperature (RT is always starting temperature) on the PTH failure and changes in failure mechanisms. Four temperatures above T_g were chosen: 215, 235, 255, and 275°C. The rationale for the two extreme temperature were that the 215°C is about the lowest temperature that is still above the T_g, the CTE transition zone associated with a significant changes in laminate material properties. The rational for the 275°C exposure was to determine if there were changes in via failure modes at temperatures above the expected maximum Sn/Ag/Cu lead-free soldering temperature zone. Indeed, the IST coupons tested at 275°C did result in POST interconnect failures, two out of 12 coupons. POST interconnect defined as holes drilled at 0.85 mm (33.5 mil) diameter; a 3.3:1 aspect ratio, with daisy

chain connecting holes between 2nd and 3rd layers and between 25th and 24th layers. With the exception of these two coupons, the remaining 46 coupons from test above T_g were all PTH failures.

Figure 60.27 presents the raw data for the 48 IST test coupon failures characterized by Freda and Barker showing variations, especially below and above the T_g. An inflection point (or discontinuity) was assumed at the laminate T_g transition zone with data below T_g and data above T_g following a different trend line. However, selection of an inflection point can have a significant effect on the cycle-to-failure estimates at a 95°C field life temperature. The plot also includes the precondition data; it seems that the 10× precondition samples have a life close to 6× or if slightly longer. The authors were unable to provide an explanation for the life reversal with preconditioning; they stated that “a combination of a relatively small sample size and random chance may be a contributor.”

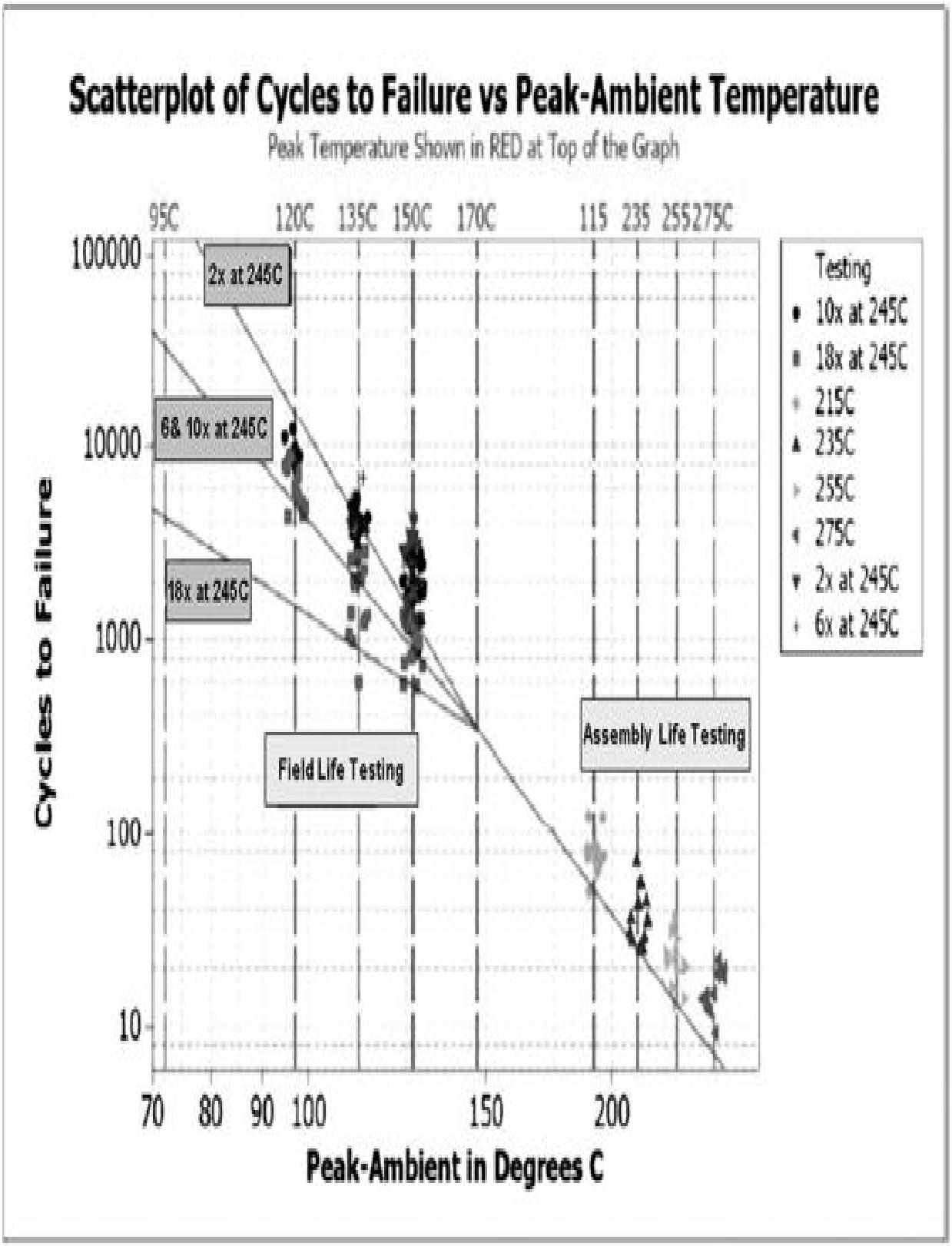


FIGURE 60.27 Log-log plot of all cycle to failure data versus temperature.[48]

Freda and Barker[48] also used Minor's rule to determine the average cycles-to-failure at temperature below T_g using CTFs for testing at 245°C and those at 120, 135, and 150°C with the same preconditioning. This allowed determination of the acceleration factor at each temperature relative to test data at 245°C. Monte Carlo simulation was used to determine failure variations from the average values. TMA and DMA testing methods were inventively used to address the large change in laminate material properties below and above T_g by generating the plot of temperature versus stress. TMA showed CTE increases from 28.9 ppm/°C below T_g to 128.7 ppm/°C above T_g; a 4.45 times increase. DMA showed a decrease in storage modulus) from 18,000 MPa below T_g to 2500 MPa above T_g, a 7.2 times decrease. Figure 60.28 shows log-log plot of scatter cycles-to-failure versus stress derived from the DMA stress/temperature relationship. These plots are now similar to classic S-N plots. The highest cycles-to-failure estimates of any of the analysis methods were listed, and it was shown that even with excessive preconditioning of 18× (> 2.5× is allowed on actual product with eutectic solder) at 245°C, the worst case estimate of cycles to failure is 3500 cycles, equivalent to >9 years in the field at one thermal cycle/day.

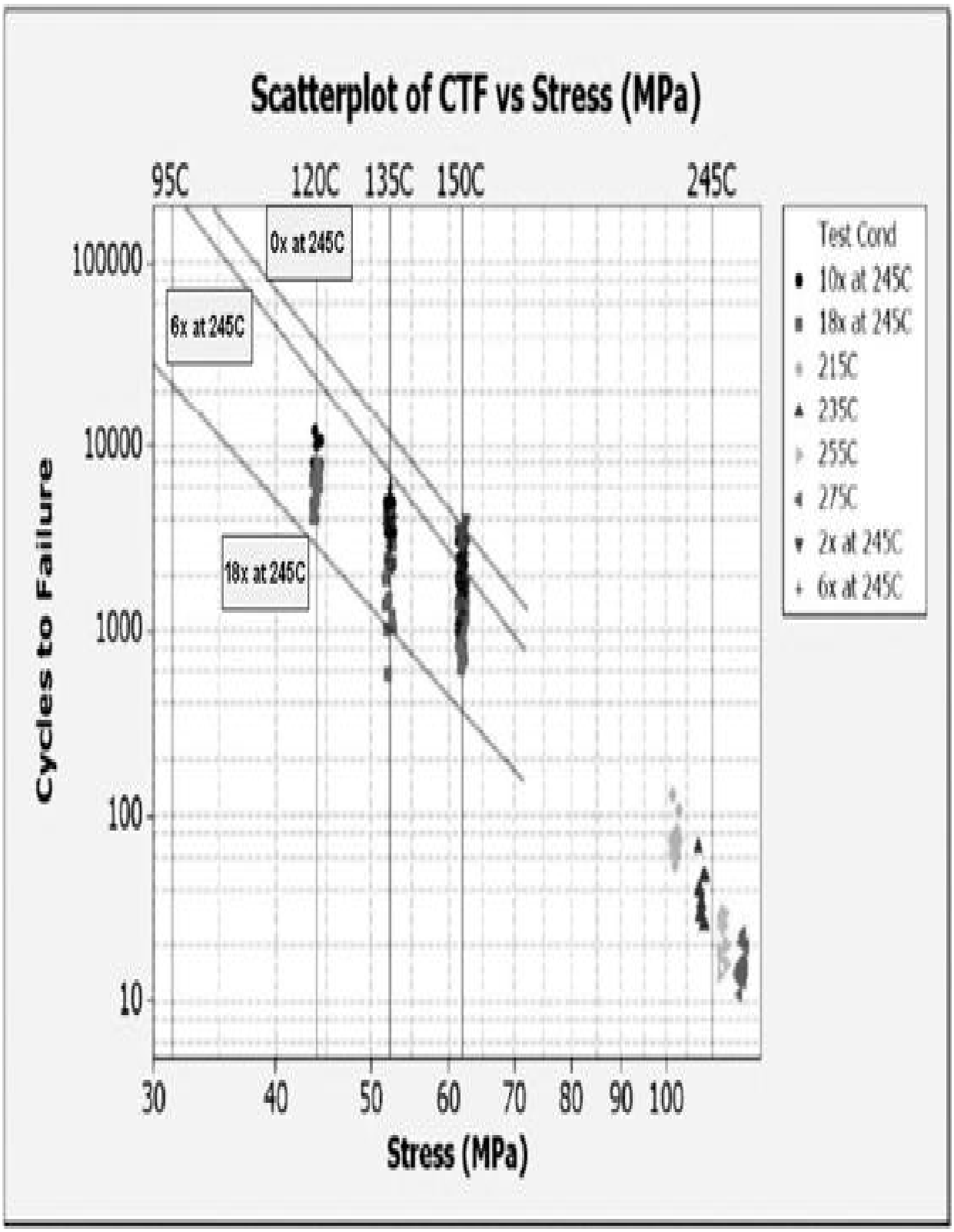


FIGURE 60.28 Cycle to failure versus stress scatter plot of all the raw data. The three parallel lines of cycles to failure versus stress were based upon Miner's

rule.[48]

A number of key findings:

- Material properties alone was inadequate to ensure high quality and reliably finished PCBs. Testing and evaluation of multilayer product was required. Internal damage was not detectable by surface visual inspection.
- The through-hole via pitch had a major impact on material survivability in Pb-free assembly with the tighter 0.8-mm (32-mil) pitch considerably more susceptible to damage compared to the 1-mm pitch.
- In the majority of cases, the 6× thermal shock at the 288°C test condition was more severe than the 6× reflow cycles at 260°C. Considering the complexity of the product (20 layers, 2.92-mm (0.115-in) thick, 11.5:1 aspect ratio) it is accepted that the requirement for six solder float thermal excursions is a very challenging. Hole wall separation was caused much more often after 6× reflow at 260°C than after 6× thermal shock at 288°C. This is believed to be a function of the longer time at temperature associated with the reflow oven compared to the very short duration of the thermal stress test.
- Hole wall separation was noted more often in the CAF sections compared to the 1-mm and 0.8-mm (40-mil and 32-mil) pitch IST and air-to-air (AtA) test vehicles.
- In both AtA and IST thermal cycling, while plating partially affected reliability, the *z*-axis CTE was the key contributor. Materials with lower CTE-Z below T_g (α1) provided the highest plated-through-hole reliability. Lower resin content constructions, which also have lower *z*-axis coefficients of thermal expansion, lasted considerably longer in thermal cycling without failure compared to the same materials used in the higher resin content constructions.

- When the material T_g, specifically as measured by DMA storage modulus, was below the testing temperature of both IST and ATC, then IST and ATC correlated very closely, and IST could be used to as an alternative to AtA thermal cycling for field life predictions.
- Supplier advertised data on *z*-axis CTE below T_g (α1) did not correlate with measured data on actual multilayer constructions, and hence, cannot be considered valid.

Park et al. also used an IPL relationship to determine relationship between cycles-to-failure and ΔT.[49] PCB test coupons with PTHs were subjected to two thermal cycle conditions in the range of -35/125°C and -55/125°C. The authors confirmed that the failure mode of PTH is copper barrel crack. From the Weibull plots of CTFs, the B10 (bearing at 10 percent, cycle-to-failure at 10 percent) values were estimated to be 606 cycles for Δ*T* of 180°C and 1065 cycles for delta of 160°C. Based on the IPL projection, it was shown that the acceleration factor was 49 and 28 relative to the field with a Δ*T* of 80°C (−40 to 40°C).

60.4.4 Corner Cracking Failure and Reliability

A majority of failures reported by industry indicate PTH failures at the center of barrel, but finite element analysis shows that the largest stresses occur not only at the center, but also at the shoulder of PTH as well as at the surface pad (see Fig. 60.29). Fehrer and Haddick reported corner cracking in FR-4 PCB when subjected to an extreme temperature cycling, immersion in hot oil at 240°C followed by cooling to room temperature by forced air.[35] The exposure was stated to be representative of solder and repair processes (tin-lead), particularly for high-pin-count through-hole devices. Both FR-

4 PCBs and cyanate ester PCBs were used. The average number of cycles-to-failure was 10 for FR-4 PCBs and 50 for cyanate ester PCBs. The primary failure mechanism was corner cracking in FR-4 PCBs and a combination of corner cracking and barrel cracking in the cyanate ester materials.

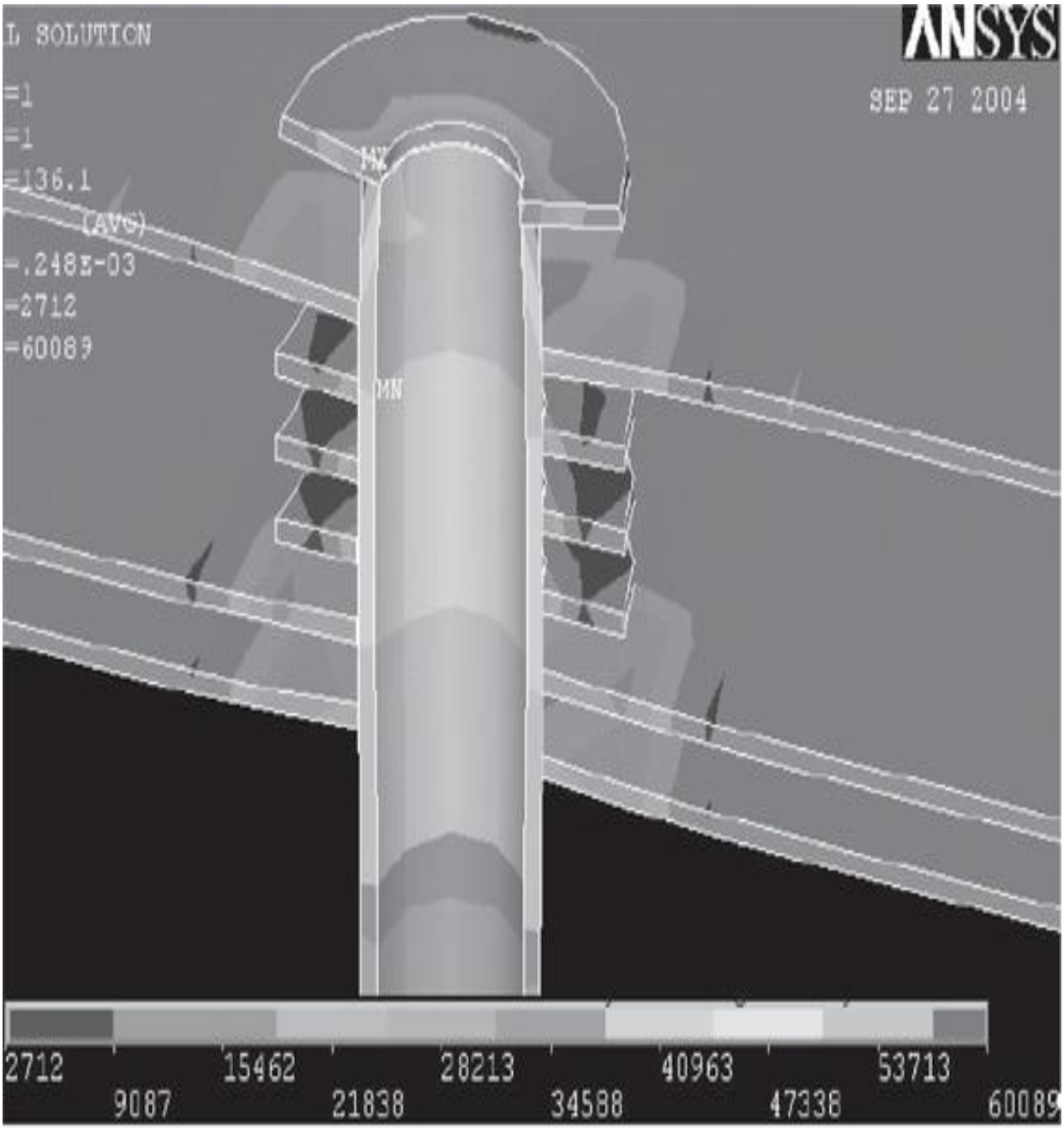


FIGURE 60.29 Finite element modeling of Cu PTH showing location of high stresses at the corner of surface pad and at the center of the PTH barrel.

The modeling, using modified pad tilt geometry in combination with the Coffin-Manson relationship, also projected low-cycle fatigue failures. For the pad tilt case, strain was assumed to be the same as the maximum strain acting at the support end of a cantilever beam, and this is shown in the following:

$$\varepsilon_f = Mc/EI = PL\ c/EI = 3EI\ \text{del}\ Lc/L^3\ EI = 3\ \text{del}\ L\ c/L^2$$

where ε_f = strain ductility
S = stress
E = Young's modulus
I = moment of inertia
C = distance from neutral axis
b = pad thickness
M = moment
L = pad annular ring
P = load
del = deflection

Now: c = pad thickness/2 = b/2, and del = free expansion of laminate = t CTE T = td, where t is half of the board thickness and d = thermal expansion of the laminate, substituting for c and del in equation, the strain in the pad-to-barrel joint:

$$\varepsilon_f = 3\ drb/(2L^2)$$

Misalignment of drilled-hole location to etched pattern should be taken into account. Therefore, in the graph of strain versus pad annular ring (Fig. 60.30), the dimensions will be representative of "minimum remaining annular ring." For reference, calculated barrel strain versus pad annular ring for an FR-4 PCB is also plotted in the figure.

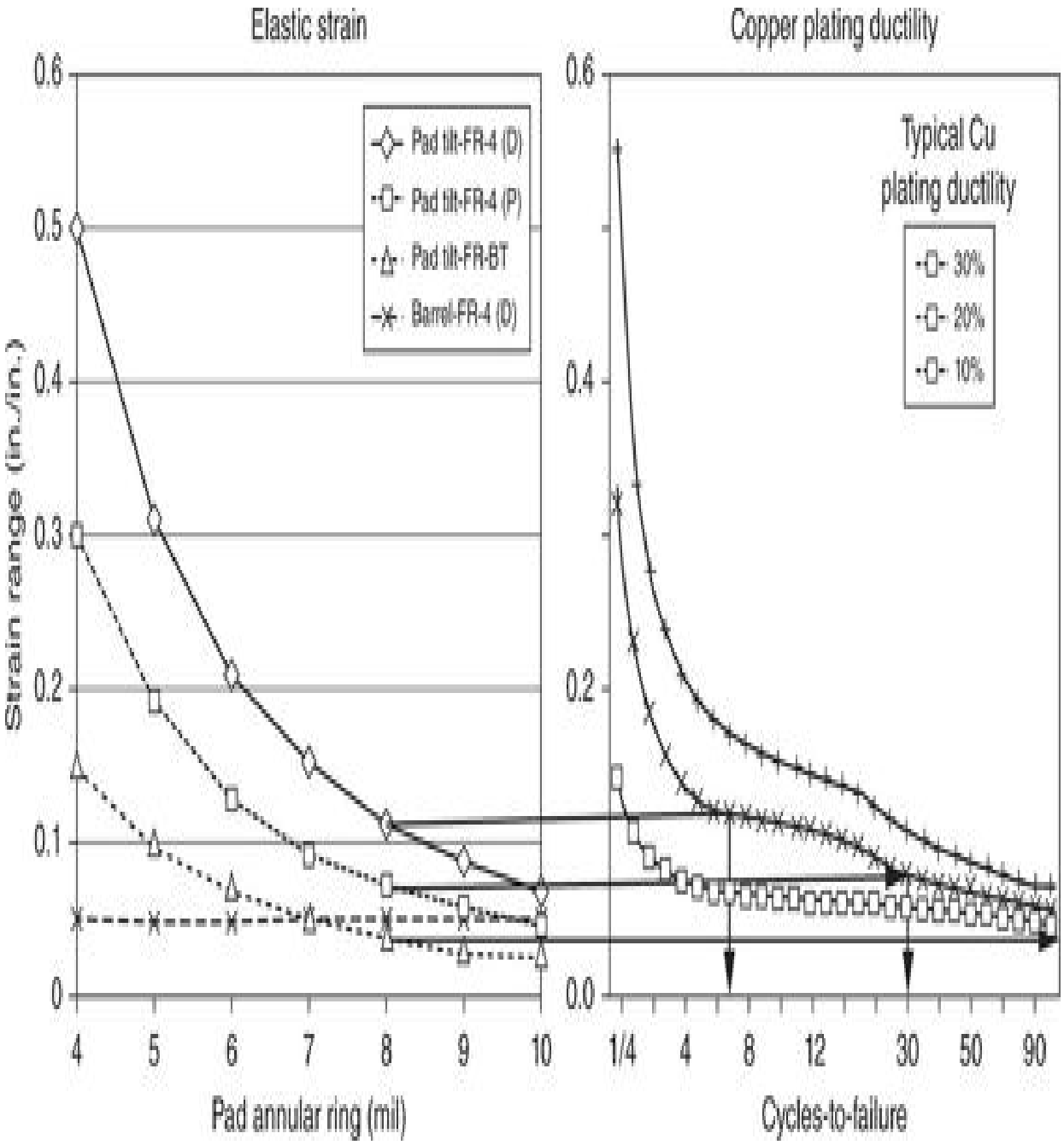


FIGURE 60.30 (*a*) Pad tilt strain versus pad annular ring and (*b*) cycles-to-failure.[35]

Tanaka et al.[50] was reported corner cracking for the case when PTH were filled with solder and then subjected to thermal and shock cycling, even though the PTH-filled solder showed longer life (see Fig. 60.31). The authors showed experimentally that the condition of solder fill affects crack

initiation in solder such that induces cracking through corner PTH and its failure after 500 cycles. Microsectional samples shown in Fig. 60.32 clearly show that cracks are first initiated in solder followed by the corner cracking of the PTH. Crack initiation in solder was prevented by forming a solder dome over the PTH copper ring. This condition did not show both formation of solder cracking as well as Cu PTH cracking. So, the Tanaka et al. concluded that there is a strong relationship between solder cracking and PTH solder-fill condition.[50]

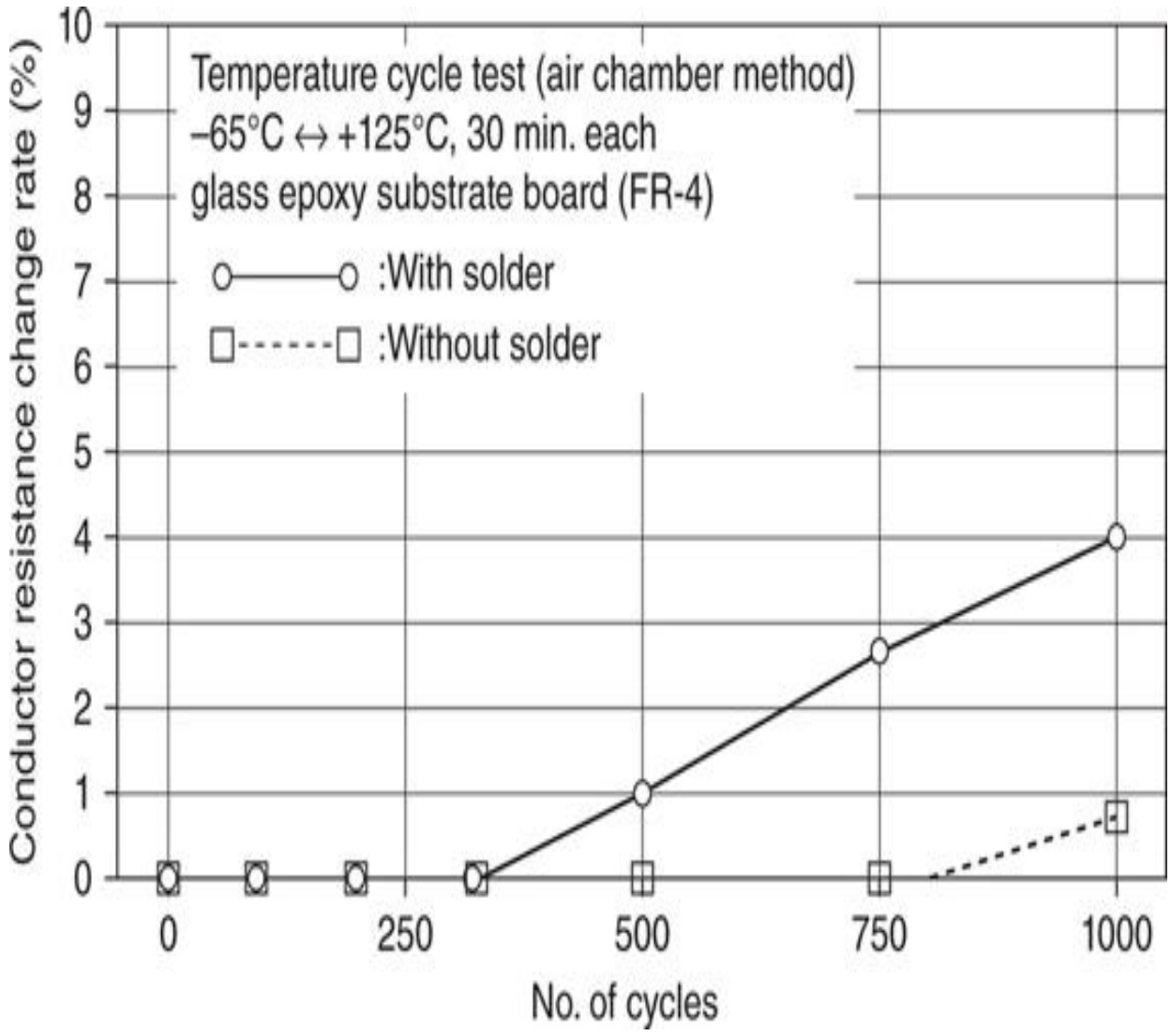


FIGURE 60.31 Cycles-to-failure for PTH with no-fill and solder fill.[50]

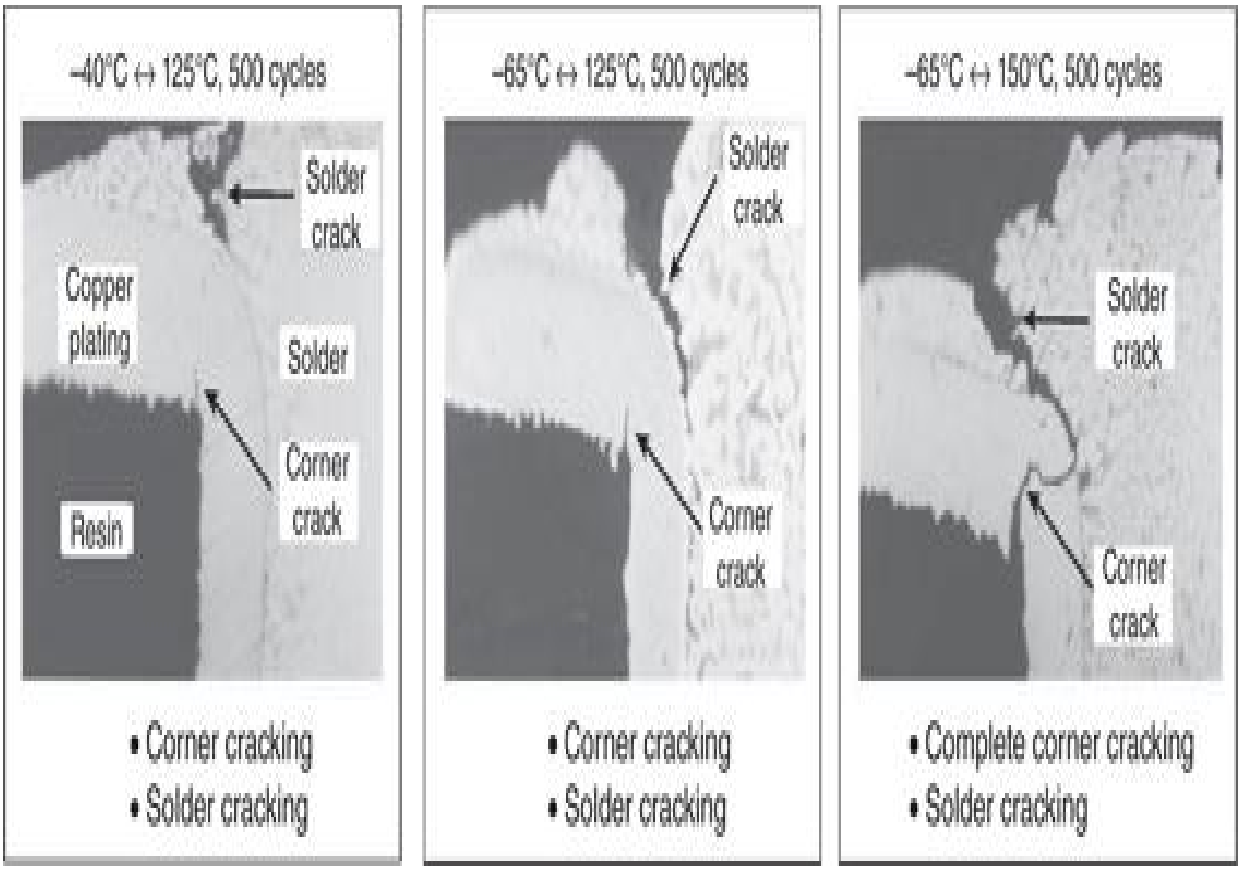


FIGURE 60.32 Corner crack initiation and failure for three thermal cycles at 500 cycles. Cracking is seen to be associated with solder fill cracking.[50]

60.4.5 PCB Properties and PTH Fill and Reliability

Wua et al. tested reliability of small PTH diameter and their failure phenomena using 0.25- to 1.5-mm (10- to 60-mil) diameters on the multilayer PCBs with 96 mil thicknesses.[51] The test boards were subjected to thermal cycle testing for 6000 cycles: from 0 to 100°C with 10°C per minute ramp rate (IPC 9701).[12] No failure was found for any PTH with a diameter larger than 18 mil or an aspect ratio less than 5.3 in this study. The first failures for 0.25-, 0.3-, 0.4-mm (10-, 12-, and 16-mil) PTH diameters were 2518, 1830, and 3985, respectively. The Weibull scale and characteristics values

were 4.92 and 3932 cycles for 10-mil diameter, 5.70 and 4439 for 0.4-mm (12-mil) diameter, and 11.89 and 5037 cycles for 0.4-mm (16-mil) diameters. The failures were dominated by wearout mode. The cross-section results show PTH failures were due to fracture at the barrel of the through hole (see Fig. 60.33) with a no-electrical-open caused by intermittent contact at the PTH shoulder.

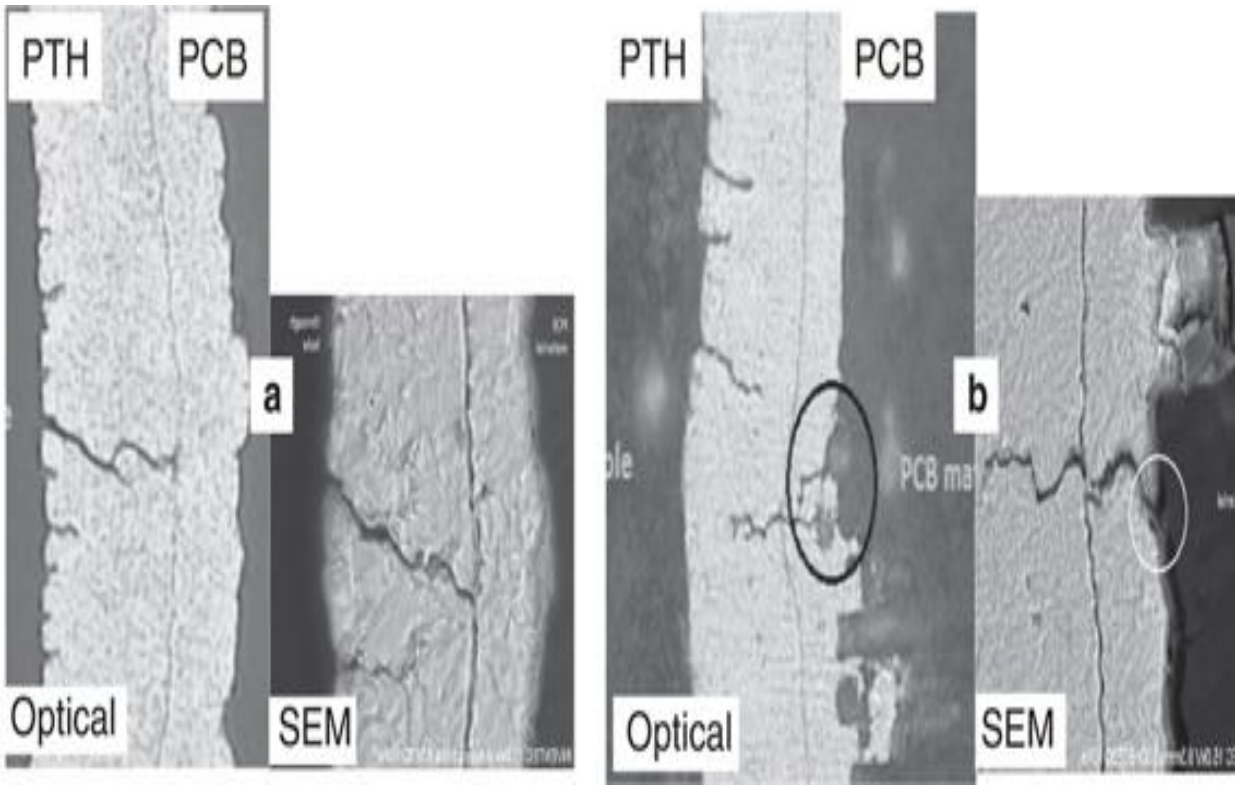


FIGURE 60.33 Optical and SEM photomicrographs showing the failure phenomena resulted from two physical mechanisms. (*a*) The crack originates from the inside edge of the plated copper and then propagates to PCB material. (*b*) Crack starts from weakness of plated copper or defect at the plated copper-PCB material interface.[51]

Based on Wua et al.,[51] the smaller the hole size, the less robust the hole reliability. The large heavily plated holes tend to have interconnection problems while small holes fail for barrel cracks. Another author, Reid, states that test data show that the hole size as small as 114 μm (4.5 mil) are robust with one key drawback.[31] The problem with such

small holes in a grid size of 0.5 mm (20 mil) is their tendency for crazing damage (generating a network of fine cracks). Crazing tends to be a path for conductive anodic filament (CAF) growth. So, the applications for the small hole and grid sizes are limited to the control environment with no humidity exposure.

Figure 60.34 shows PTH mean life cycles-to-failure for four different resin systems using 4 to 12 coupons tested from room temperature (23°C) to *T* (high) temperatures.[52] The curves reveal significant characteristics of the base resins, in particular, other than polyimide, which has a T_g above that of the temperature range tested, the approximate T_g of the materials is evident as the point of distinct change in slope of its curve. FEA revealed (see Fig. 60.35) that the difference in fatigue life of the plated through hole does not change significantly when the diameter of the plated through hole changes from 203 to 305 µm (8 to 12 mil), at least on a 0.48-mm-thick (190-mil) board.

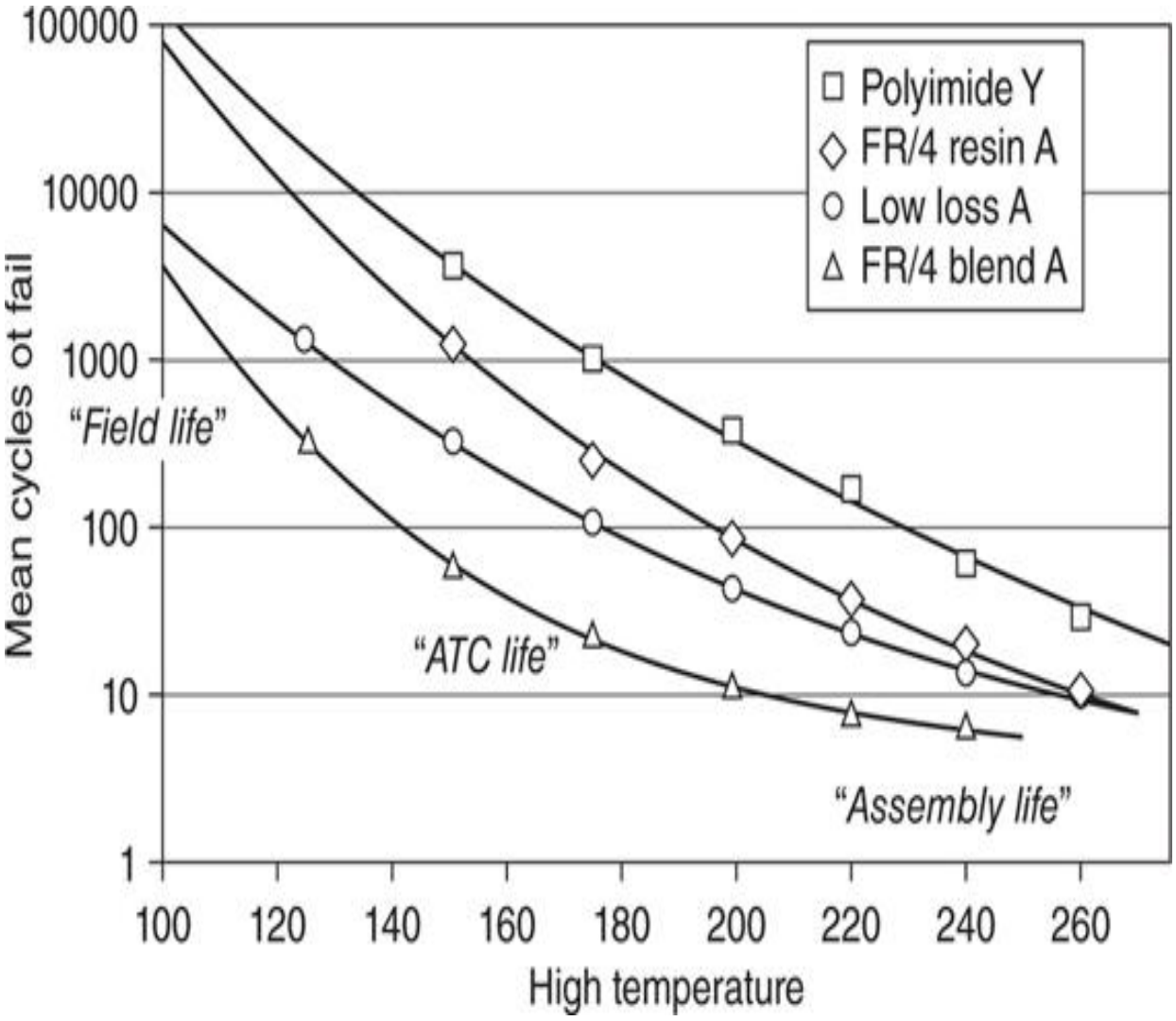


FIGURE 60.34 "PTH life curves" for 4 resin systems with CITC 23°C to *T* (high). Coupons 3.0 mm (0.120 in) thick, 0.25 mm (0.010 in) vias.[52]

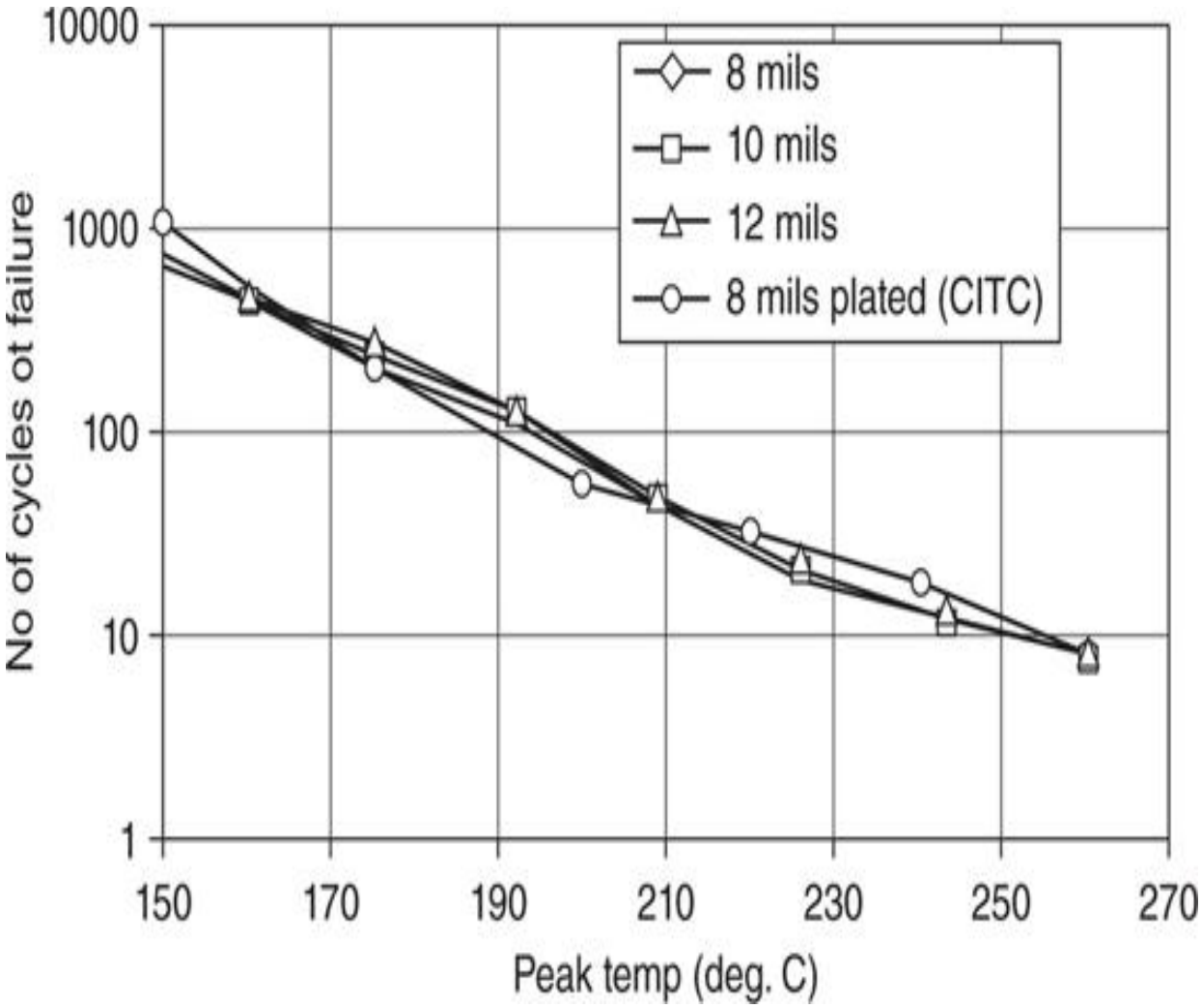


FIGURE 60.35 FEA fatigue life predictions vs. cycles-to-failure (CITC) life data.[52]

Recent data generated based on the HATS testing (−55/145°C)[24] for via sizes from 203 to 355 μm (8 to 14 mil) showed only slight differences with no clear trend (see Fig. 60.36). There was a significant increase in the stresses and strains in the PTH structure with an increase in the CTE of the hole-fill material. Figure 60.37 shows a plot of the vertical sidewall stress versus CTE.[53] Similar trends were shown for the von Mises stress and strain within the PTH. The location of the maximum displacement shifts from within the via to the center of the composite as the CTE of the hole fill is increased. In general, a low CTE hole-fill material is preferred

for a lower stress level in the PTH. The effect of hole-fill modulus was also studied. A similar trend was observed in that the stresses in the system increased with an increase in hole-fill modulus. A lower hole-fill modulus resulted in lower stresses in the PTH system.

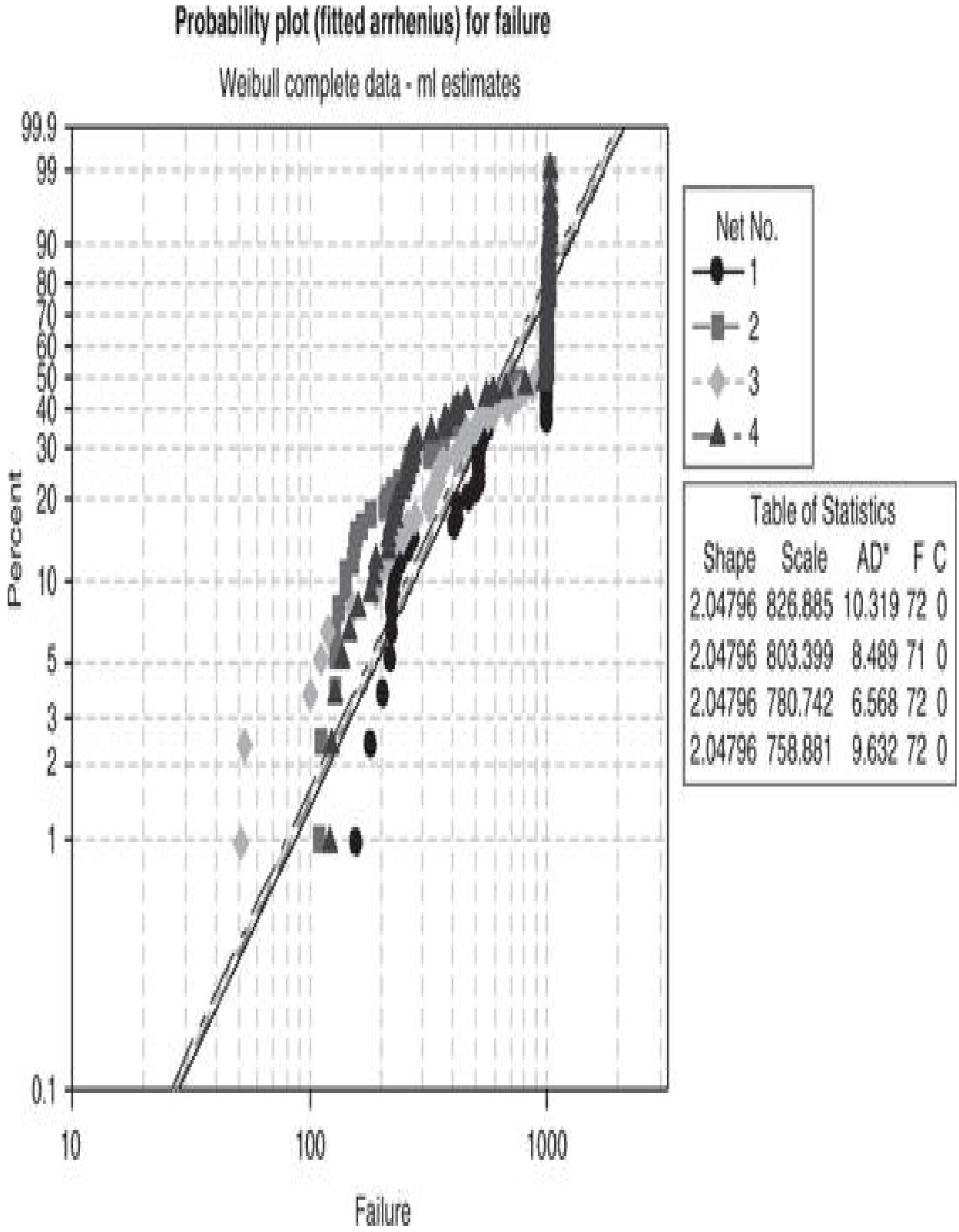


FIGURE 60.36 HATS cycles to failure of PCB with various PTH sizes [1 = 355 µm (14 mil), 2 = 305 µm (12 mil), 3 = 254 µm (10 mil), 4 = 203 µm (8 mil)].[24]

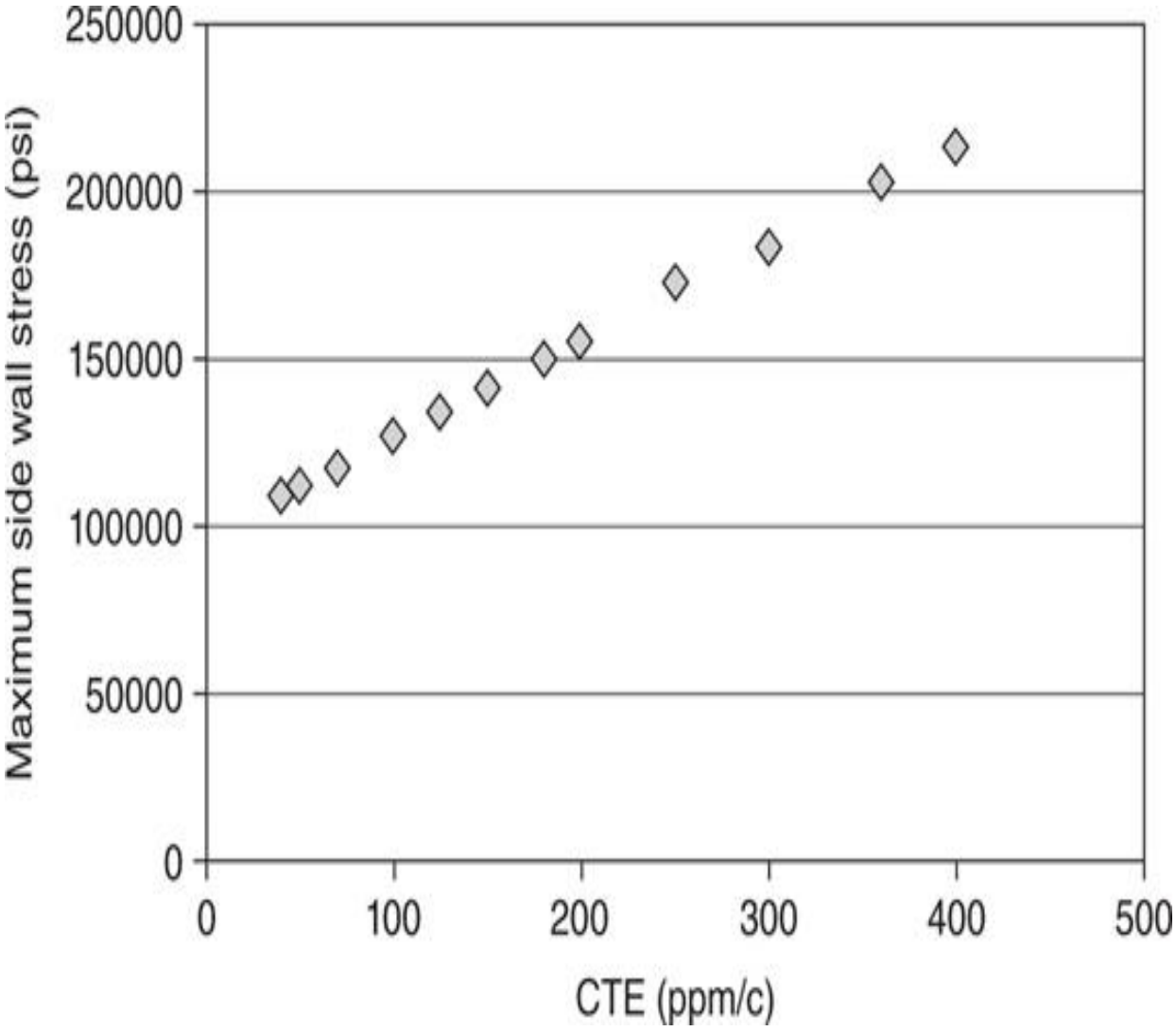


FIGURE 60.37 Vertical sidewall stress versus hole-fill CTE.[53]

However, under all hole-fill CTE and modulus conditions (keeping the rest of the material properties of the PTH build up constant), the stress in the via sidewalls did not fall below the yield stress of copper. This indicates that the necking of the copper barrels cannot be prevented by modifying the hole-fill material alone. The results of the study show that lowering the modulus of copper and the out-of-plane CTE of the FR-4 material can significantly reduce the stresses in the PTH and the via walls. Hence, modification of the PTH geometry such as the copper plating thickness and via size

may become necessary to prevent the failure of the PTHs during the assembly processes.

In another investigation on the effect of via-in-pad (ViP),[54] it was experimentally shown that thermal cycle reliability for a Pb-free SAC alloy depends on the particular device package type. For a BGA, reliability decreased with the use of ViP (see Fig. 60.38). For the BGA192, where the presence of ViP has a significant impact on the thermal cycle performance, the average void percent in diameter and area on the corner and adjacent solder balls is roughly four times greater for the ViP construction than the non-ViP construction. Authors believed that the voiding associated with the conformal microvia to be the cause of the reduced solder joint life, however, the failure analysis results, were not conclusive. The impact and size of the void associated with a microvia in a pad is a function of the component type, solder ball size, microvia drill size, and laminate thickness. However, the void location is more important than its size having a greater potential impact on solder-joint failure when voids are located in the fatigue crack path. Based upon this, it has been hypothesized that microvias in pad construction should result in poorer fatigue life performance for Pb-free than SnPb solder joints since the former exhibited a somewhat higher incidence of failure due to cracking in the board side of the solder ball where microvia related voids can influence fatigue-crack propagation.

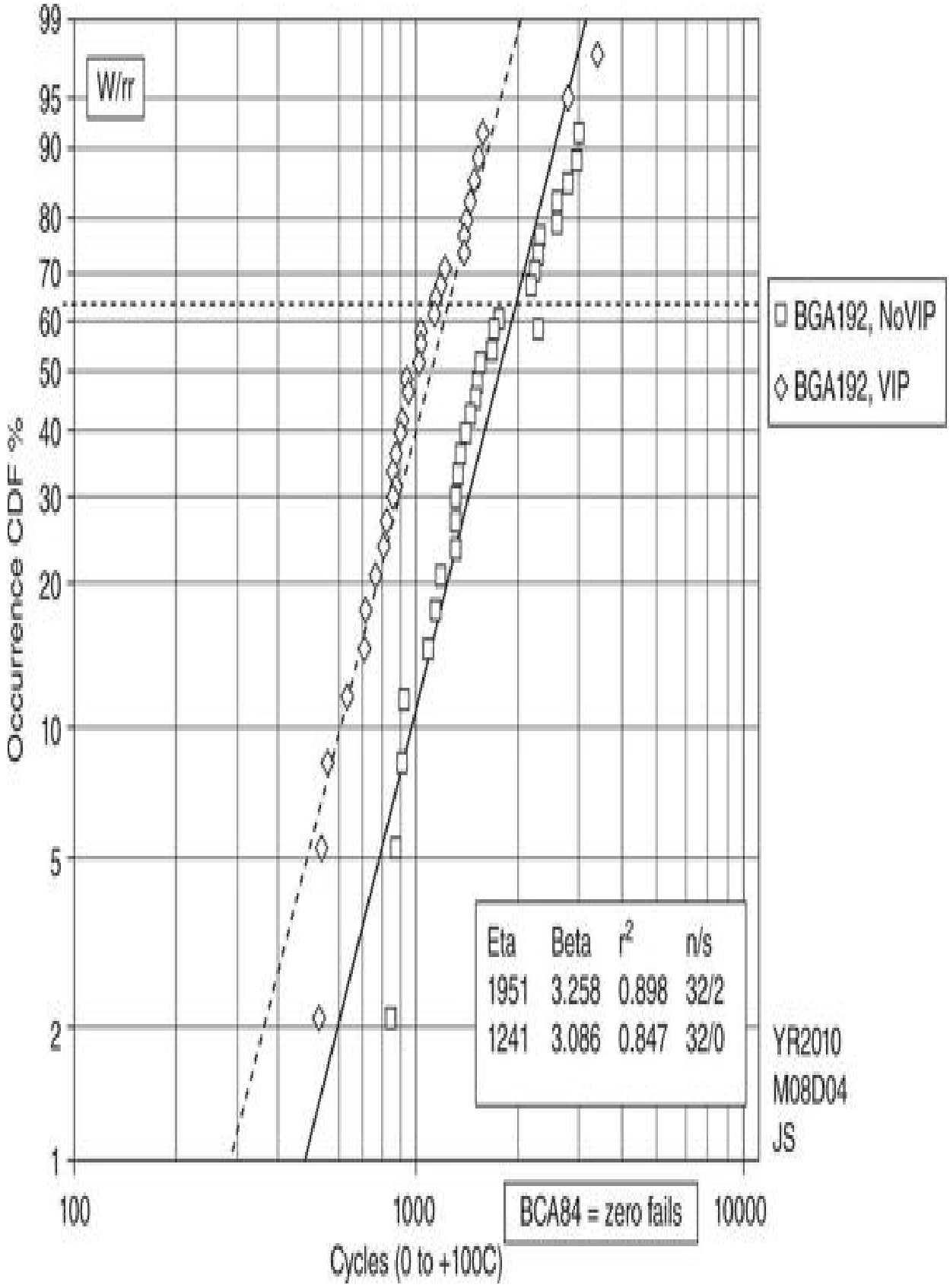

W/rr
99
95
90
80
70
60
50
40
30
20
10
5
2
1
Occurrence CDF %
100
1000
10000
Cycles (0 to +100C)
BCA84 = zero fails
BGA192, NoVIP
BGA192, VIP
Eta Beta r² n/s
1951 3.258 0.898 32/2
1241 3.086 0.847 32/0
YR2010
M08D04
JS

FIGURE 60.38 Weibull plots of the BGA192 failure data with ViP and No ViP.

Through hole via pitches of 0.8 mm (32 mil) are more susceptible to internal material damage during Pb-free reflow or other thermal stresses than 1 mm (40 mil) or greater via pitch. Because of the closer pitch of the vias at 0.8 mm (32 mil), the stresses built up during Pb-free assembly resulting from the CTE differences between the copper plated through holes and the laminates, plus any vapor pressure generated during reflow, are less able to be distributed across the material between the vias. In the worst case this results in severe internal delamination of the materials.

60.4.6 Reliability of PCB under Pb-Free Assembly

Regarding the high temperature Pb-free reflow process, the primarily threat to the reliability of printed circuit boards (PCBs) comes from one source, the temperatures required during the soldering processes for the assembly of the components onto the PCB.[55] The PCB reaches temperatures higher than most components in the assembly. These temperatures can be between 230 and 245°C for soldering with SnPb-solders, and 265°C and 280°C when soldering with Pb-free solders. The FR-4 materials currently standard for PCBs are inadequate in their capability to survive the higher soldering temperatures required for most LF-solders. The effect of two and three reflow soldering preconditioning at 250°C, representative of lead-free solder reflow, is shown in Fig. 60.39.[24] Subsequent to preconditioning, the PCB test vehicles were subjected to highly accelerated thermal stress (HATs) testing in the range of −55/145°C (air to air). Even though the Weibull plots are not linear indication of a stress free region, it clearly shows significant reduction due to one additional soldering reflow. The 63 percent cycles-to-failure

decreased from 422 cycles to 292, about 30 percent reduction.

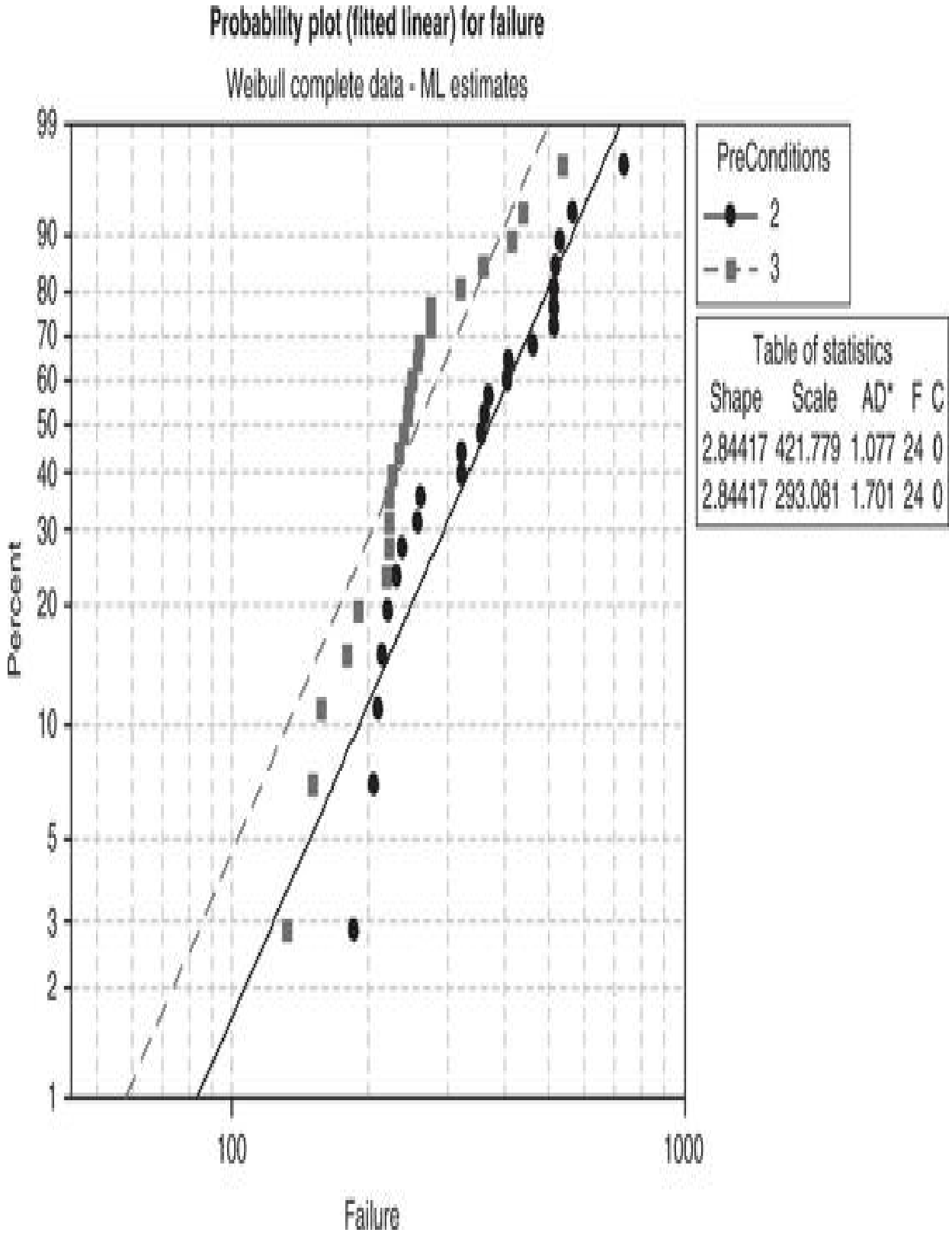


FIGURE 60.39 Effect of two- and three-cycle preconditioning at 250°C on subsequent number of cycles to failure (−55/145°C, air to air). It reduced the

average CTF from 422 to 294 cycles.[24]

The standard FR-4 materials for PCBs may be inadequate in their capability to survive the higher soldering temperatures required for most Pb-free solders. While today's FR-4s are significantly improved over the materials which were available previously, the improvement has occurred primarily with the glass transition temperature, T_g. Increases in T_g as well as possibly decreases in coefficients of thermal expansion (CTE) and increases in decomposition temperature, T_d, are also necessary. The improvements in T_g and CTE are required to ensure the integrity of the PCB interconnect structures (i.e., PTV copper barrels and barrel/innerlayer interconnects), whereas the improvements in T_g and T_d are necessary for the thermal stability of the PCB resin to mitigate barrel fractures as well as innerlayer separations (ILS). Smaller diameter PTVs tend toward barrel fractures, while larger diameter through-holes tend toward ILS. Resin degradation and decomposition occur at temperatures too high for that particular resin system. Werner Engelmaier proposed that three resin properties are needed to be improved to assure the survival and reliability of PCBs during the high soldering temperatures for Pb-free solders.[55]

- Glass transition temperature, T_g
- Decomposition temperature, T_d
- Coefficient of thermal expansion, CTE

The soldering temperature impact index (STII) was proposed to capture these three properties. The relationship is given as

$$\text{STII} = (T_g + T_d)/2 - [\%\ \text{thermal expansion 50 to 260°}] \times 10$$

The effect of STII for a large number of FR-4 PCB test vehicles was investigated under HATs (−55/145°C) thermal cycling.[24] The results are shown in Fig. 60.40. The STII varied from 181 to 247.

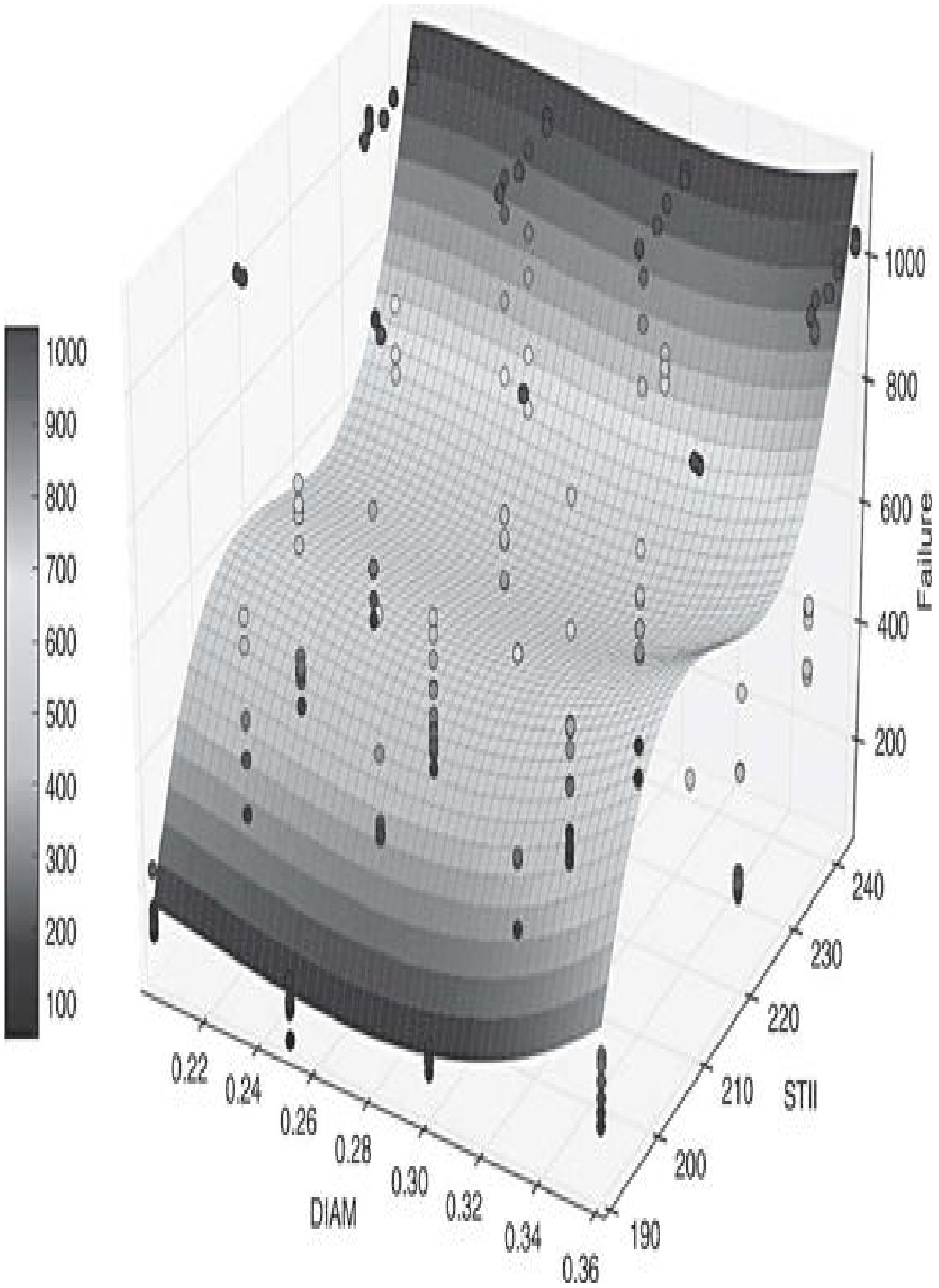

1000
900
800
700
600
500
400
300
200
100
0.22
0.24
0.26
0.28
0.30
0.32
0.34
0.36
DIAM
190
200
210
220
230
240
STII
1000
800
600
400
200
Failure

FIGURE 60.40 The effect of PTH diameter and STII on the number of cycles to failure (−55/145°C, air to air). As the STII increases, the CTF increases.[24]

The higher soldering of Pb-free temperatures, together with the very high Sn-contents of solders, leads to a significant increase in the rates of copper dissolved during soldering processes. Reductions in copper thickness by as much as 12 μm (0.5 mil) have been reported. Therefore, the minimum copper plating thickness needs to be increased to accommodate decreased plating during high temperature Pb-free soldering. In addition, the copper plating absorbs moisture that generates damage during PCB soldering processes due to high internal vapor pressure. The higher the moisture content and the higher the temperature, the higher the vapor pressure and resulting greater damage. Thus, for Pb-free soldering, the amount of moisture absorption should be reduced by a more rigorous moisture bake-out prior to soldering to assure the survival and reliability of PCBs.

In addition, when a PCB is exposed to elevated temperatures for long periods, the adhesion between the Cu and the laminate decreases, and the flexural strength of the laminate gradually degrades. Discoloration is usually an early symptom of such degradation. Cu adhesion is measured using a peel test. Adhesion at elevated temperatures or after elevated temperature exposure gives some insight into the ability of the material to withstand rework and other high-temperature processes. Flexural strength stability is compared by measuring the times at 200°C before the flexural strength decreases to 50 percent of its original value. The quality of the bond between the resin and reinforcement is compared by measuring the time it takes for copper-clad laminate to blister during a solder float test at 290°C.

An industry consortium investigated the PTH reliability of 20 different Pb-free capable PCB materials test vehicles with

27 different layer constructions built by three manufacturers all having Pb-free capable materials (Smetana et al.)[56] The materials were tested using both air-to-air (AtA) thermal cycling and interconnect stress testing (IST) methodologies. Both as built and after 6× Pb-free (260°C) reflow were evaluated.

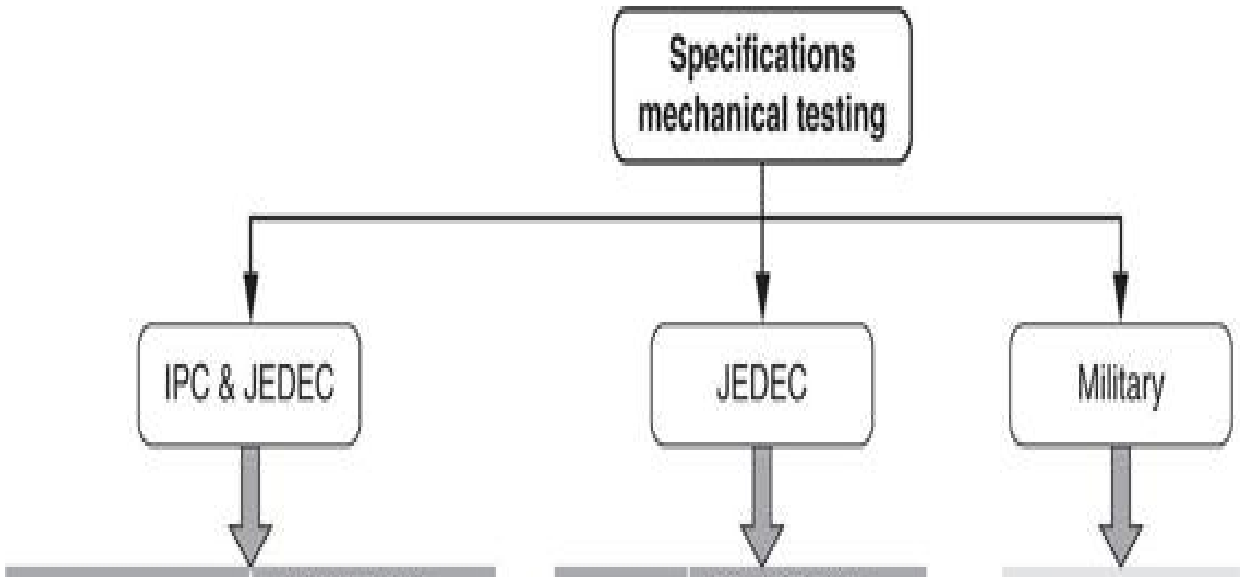
After 6× reflow, both AtA cycling from −40 to +135°C with 10 min dwell and ramp times and IST testing from ambient (23°C) to 150°C with 3-min heating ramps, 2-min cooling ramps, and no dwell at either temperature extreme. Testing was initially continued to a maximum of 3000 cycles, and then extended to 6000 cycles on certain materials that proved to be very robust. The Smetana et al. reference significant other evaluations, including the conductive anodic filament (CAF) tests, moisture sensitivity testing, stress versus temperature relationships, electrically quantifying the consistency of product construction, dielectric thickness, and material damage through assembly and characterization of the electrical characteristics of each laminate.

When evaluating Pb-free survivability, in the majority of cases, the 6× thermal stress at 288°C test condition was more severe than the 6× reflow cycles at 260°C. The 288°C thermal stress methodology is both easy to implement at the PCB fabricator and a valuable tool for looking at the first article, or as a production check on an actual design. It is recommended to use both the combination of reflow cycling and solder float testing when material and product qualification is important.

As a general observation, the laminate integrity of the Pb-free materials after 6× reflow cycles at 260°C was significantly better than earlier evaluation, showing that the materials industry is learning and maturing relative to materials ability to survive multiple cycles through Pb-free assembly.

60.4.7 Specifications for Field Life Requirements

Before field life projection, desired lifetime and product performance metrics need to be identified and documented. The desired lifetime might be defined as the warranty period or by the expectations of the customer. A meaningful reliability prediction must take into account the environment in which the product is used. There are several common approaches to identifying the environment. One approach is to identify the environment involves the use of industry/military specifications. Recent specifications on mechanical testing are summarized in Fig. 60.41. These have been generated in recent years by commercial industry, particularly by the Association Connecting Electronics Industries (IPC) and the Joint Electron Device Engineering Council (JEDEC) in response to increasing demands on area array packages and their miniaturized versions and stack technologies. It also includes the key military specification (Mil-STD-810F) (that was updated in 2008). The key specifications for evaluation under mechanical testing are as follows:



IPC/JEDEC-9702	Monotonic bend characterization of board-lavel interconnects
IPC/JEDEC-9703	Mechanical shock test guidelines for solder joint reliability
IPC/JEDEC-9704	Printed wiring board strain gage test guidelines
IPC/JEDEC-9707	Spherical bend test method for characterization of board level interconnects
IPC-9708	Test methods for characterization of printed board assembly pad cratering

JESD22-B111	Board level drop test method of components for hand held electronic products
JESD22-B110A	Subassembly mechanical shock

Mil-STD-810F Vibration/shock methods 514/516

FIGURE 60.41 Key Commercial and military specifications for mechanical testing, including those that define bending, drop, vibration, and shock for behavior of microelectronics.[2]

1. Joint IPC/JEDEC 9702 covers basic mechanical bend testing characterization and strains to failures using four points, a bend test method commonly used by industry. Specific strain gage attachment requirements are delineated in IPC-JEDEC-9704.
2. Joint IPC/JEDEC 9707 covers a new test method that is more applicable for area array packages. It uses spherical loading at points rather than loading through cylindrical rod as was used in four-point bend testing defined in IPC 9702. This standard supplements existing standards for mechanical shock during shipping, handling, or field operation, as well as filling the gap for IPC/JEDEC 9702 to better characterize maximum strain levels. The two specifications provide a common method of establishing the fracture resistance of board-level package interconnects to flexural/point loading during PCB assembly and test operations. No pass/fail qualification requirements are provided, since each package/assembly is considered unique.
3. IPC 9703 covers generic guidelines for mechanical drop and shock testing. These are only guidelines because of requirements differences between industries. The document scope includes: (a) methods for defining mechanical shock use conditions, (b) methods to define system-level and system-board-level component testing that correlates to the use conditions, and (c) guidance on the use of experimental metrologies for mechanical shock tests.
4. IPC 9708 was generated in response to newly observed board failures (pad cratering) resulting from the move to implement Pb-free solder alloys. Pb-free solders are generally stiffer than tin-lead solders; they can transfer

more of the applied global strain to the assembly. The Pb-free approach requires higher reflow temperatures that induce higher residual stress/strains in the assembly. Pb-free is typically assembled with phenolic-cured PCB materials that are more brittle than conventional dicyandiamide-cured (dicy-cured) FR-4 materials. These strains could eventually relax over time, but if mechanical strain is applied shortly after reflow, pad cratering could occur at lower mechanical strain levels.

5. JEDEC JESD-B111 was developed for portable electronics in response to the need to define resistance to repeated drops, which is required for mobile applications. The shock pulse requirement for a PCB assembly is defined based on JESD22-B110, condition B, Table 60.6 (or JESD22-B104-B, Table 1) with 1500 Gs, 0.5 ms duration, and half-sine pulse. This specification is widely used by industry, and data are valuable for high-reliability applications. JESD-B210A defines resistance to mechanical shock.

TABLE 60.6 Thermal Testing Protocols for Nnine End Product Uuse Environments[59]

Use Category	Min. T, °C	Max. T, °C	Δ T°C	Dwell hrs.	Cycles per Year	Yrs of Service	Acceptable Failure Probability
1. Consumer	0	+60	35	12	365	1-3	~1%
2. Computers	+15	+60	20	2	1460	5	~0.1%
3. Telecom	-40	+85	35	12	365	7-20	~0.01%
4. Commercial Aircraft	-55	+95	20	12	365	20	~0.001&
5. Industrial/Automotive-	-55	+95	20	12	185	10	~0.1%
Passenger Compartment			&40	12	100		
			&60	12	60		
			&80	12	20		
6. Military Ground &	-55	+95	40 & 60	12	100	10	~0.1%
Ship					265		
7. Space (leo/geo orbits)	-55	+95	3 to 100	1	8760	5-30	~0.001%
				12	365		
8. Military Avionics	-55	+95	40	2	365	10	~0.01%
			60	2	365		
			80	2	365		
			&20	1	365		
9. Automotive-Under	-55	+125	60	1	1000	5	~0.1%
hood			&100	1	300		
			&140	2	40		

6. Mil-STD-810F covers many aspects of environmental testing (including mechanical vibration and shock), and it is well established for conventional microelectronics for high-reliability applications.

Other specifications are MIL-HDBK-310, SAE J1211, Telcordia GR3108, and IEC 60721-3. IPC-SM-785, and IPC 9701.

For example, for accelerated thermal cycle reliability testing of solder attachment, IPC-SM785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, has been in use for more than a decade. Only recently industry has agreed to release an industry-wide specification, IPC-9701, in response to BGA and CSP technology implementation.[57] The IPC-SM785 guideline, although very valuable and still valid, did not answer the key question of what the data means in terms of product application and data comparison. As has been well established by industry, many variables could be manipulated to either favor or disfavor test results. Considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This is especially likely for a novice user/supplier.

The IPC 9701 specification addresses how thermal expansion mismatch between the package and the PCB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, numerous materials and process parameters were specified.

The newest revision, IPC-9701A (released in 2006) includes guidelines for Pb-free solder alloys.[58] The appendix added to the specification requirement establishes guidelines for modifications required for lead-free solder joints. Its Appendix A provides examples of test data and modeling approaches that are considered to better define the effects of various thermal cycle parameters on accelerated test

results and projection for product reliability. Lack of extensive field reliability data for Pb-free electronic products in 2006 made reliability comparison with tin-lead based on accelerated laboratory test data even more difficult.

For the SAC (SnAgCu) Pb-free solder alloys, dwell (soak) time might be required to be increased in order to accommodate their slower creep rates. A requirement for increased dwell is specified as another condition when experimental comparison between tin-lead and Pb-free solder alloys are deemed to be necessary. The thermal cycle (TC) test ranges, test profile, and the number of test cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 to 100°C (TC1) and the severe military cycle condition of −55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

The advantages of using a specification for projecting field reliability include the low cost of the standards, their comprehensive nature, and agreement throughout the industry. If information is missing from a given industry, a user may simply choose standards from other industries. The disadvantages include the age of the standards (some are relevant to an older technology) and the lack of validation against current usage. The standards both overestimate and underestimate reliability by an unknown margin.

Table 60.6 provides for end use thermal testing.[59] Not all electronic systems experience the same environmental/operational requirements over their lifetime because of their different operating conditions. The traditional test methods are still in use, even with the advent of new materials and new processes. It is advisable to always question the methods that were used to establish field reliability predictions. No doubt, thermal stress, thermal shock, and thermal cycling will still be around for many

years; however, the limits of the testing range and time of testing may come under question. So, thermal modeling is still needed to project field reliability for PTHs and assemblies.

60.4.8 Field-Life Projection for PTH Reliability

Another approach to identifying the field environment is based on actual measurements of similar products in similar environments. This gives the ability to determine both average and realistic worst-case scenarios. All failure-inducing loads can be identified, and all environments, manufacturing, transportation, storage, and field, can be included. Such field information with appropriate modeling approaches, the field life can be more realistically projected.

So, the goal in modeling PTH reliability is to be able to estimate the available lifetime of a product after it has been subjected to all the manufacturing processes and burn-in testing.[60] The available PTH filed life are estimated by using the Pad/Barrel concentration model, semi-empirical relationship and fatigue Minor's rule. The damage accumulation rule (minor rule) is as follows:

$$A n_i/Ni = n_1/N_1 + n_2/N_2 + n_i/N_i = C$$

n_1, n_2, … n_i is the number of thermal cycles applied to the test or field coupon at a specific temperature or stress level

N_1, N_2, … N_i is the known number of cycles to failure, that is, the life at a specific temperature or stress level

C is a constant determined by experimentation and is usually found in the range of $0.7 \leq C \leq 2.2$

If $C = 1$, then Miner's rule becomes a simple equation of what proportion of life is used at each temperature

Table 60.7 shows calculation of cycle to failure for various manufacturing and effective strains, here specified as total strain range (TSR). The assumptions were for a typical PTH with the following parameters:

TABLE 60.7 Typical Small Hole Predicted Reliability[60]

			Nf (Cycles-to-failure)				
			TSR (in./in)		15% (Ductility)		
Thermal Cycle	Max Temp (°F/°C)	Failure Site	Min	Max	Min	Mean	Max
Generic	450/232	Barrel	0.044	0.106	5	17	29
		Knee	0.042	0.050	23	27	32
		Interconnect	0.029	0.030	64	66	69
Power On/Off	200/93	Barrel		0.003	19400		
		Knee		0.004	8780		
		Interconnect		0.002	30000		

- Drilled hole diameter = 0.0135 in
- Minimum plating thickness = 0.0010 in
- Maximum plating thickness = 0.0015 in
- Laminate material = FR-4 (difunctional)

Using both the barrel and the knee as the weakest members, the mean life fraction consumed during assembly (assuming 7 generic thermal cycles for manufacturing) as, Barrel:

$$n/N = 7/27 = 0.41 \text{ and Knee: } n/N = 7/17 = 0.26$$

Thus, 41 percent of the PTH barrel and 26 percent of the knee life will be consumed at the completion of the seven

assembly process steps. The remaining 59 and 74 percent of the PTH life, respectively, will be consumed by some fraction of the 19,400 operational cycles for the barrel and 8780 operational cycles for the knee (see Table 60.7), i.e.:

$$\text{Barrel: } n/N = n_b/19{,}400 = 0.59 \text{ or } n_b = 11{,}446 \text{ cycles}$$

$$\text{Knee: } n/N = n_k/8780 = 0.74 \text{ or } n_k = 6497 \text{ cycles}$$

For this case, the knee will wear out first after approximately 6500 field cycles. Based on the above, each additional assembly cycle is equivalent in the amount of damage induced to 1175 field cycles at the barrel and 318 field cycles at the knee.

60.4.9 PTH Reliability Improvement Approaches

Numerous publications and industry joint efforts covered the key PCB fabrication and properties and Cu PTH parameters that affect thermal cycle reliability. The strain accumulation on Cu PTH depends on strain level induced at each thermal cycle excursion. To increase the useful life cycle, the following approaches can be implemented:

- The PTH reliability can be increase by increasing the ratio of $\varepsilon_f/\Delta\varepsilon$ since the number of cycles-to-failure (N_f) is proportional to ½ $(\varepsilon_f/\Delta\varepsilon)^m$. This ratio can be increased by increasing the Cu ductility (increases ε_f) and yield strength (decreases $\Delta\varepsilon$). Cu strength and ductility are often inversely related, so these two factors must be balanced against one another.
- The number of cycles to failure can be dramatically decreased by defects in the hole wall or Cu plating in the

hole or PTH knee that act as stress concentrations (increasing the local stresses and strains) and/or facilitate crack initiation.

- Decreasing or eliminating thermal shocks by preheating the PCB before hot-air leveling, wave soldering, rework with a solder pot, etc.
- Decreasing the range of the thermal cycle (see Fig. 60.42). Decreasing the range of the thermal cycle is the single most effective measure for increasing the life of the PTH, especially if the thermal cycle exceeds the T_g of PCB.

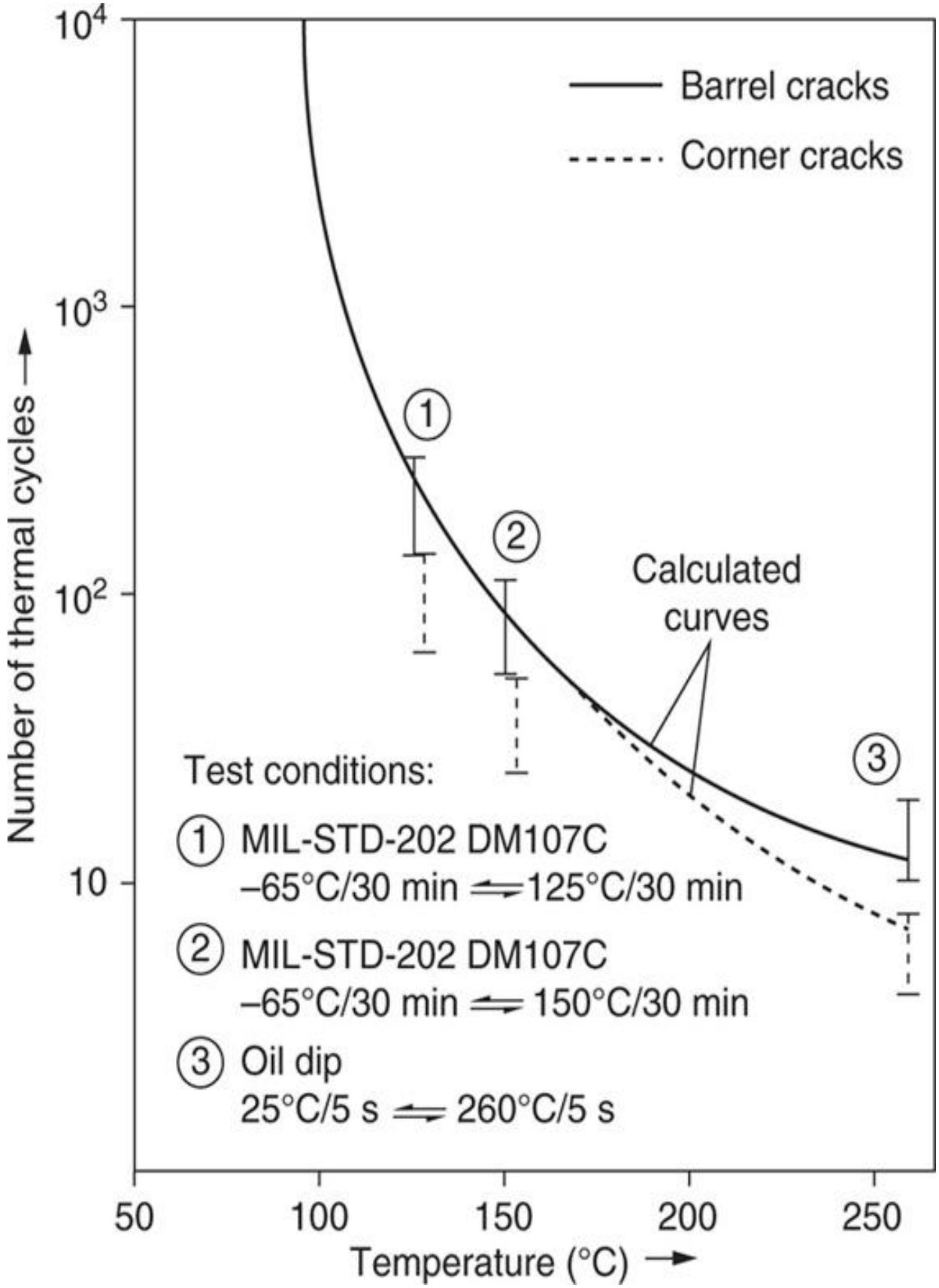

Barrel cracks
Corner cracks
Calculated curves
Number of thermal cycles →
10^4
10^3
10^2
10
50
100
150
200
250
Temperature (°C) →
Test conditions:
① MIL-STD-202 DM107C
–65°C/30 min ⇌ 125°C/30 min
② MIL-STD-202 DM107C
–65°C/30 min ⇌ 150°C/30 min
③ Oil dip
25°C/5 s ⇌ 260°C/5 s

FIGURE 60.42 Peak temperature versus number of cycles to failure by PTH barrel (solid bars) or corner (dashed bars) cracking in three different tests. Calculated lines are shown for comparison. Results are for acid-sulfate copper and FR-4. Other parameters are total strain energy required to cause fracture, 50 J/cm^3; hole radius, 0.45 mm; distance from hole center to free end, 0.8 mm; plating thickness, 0.02 mm; distance from hole center to pad edge, 0.8 mm; board thickness, 2 mm.[57]

- Decreasing the free thermal expansion of the laminate over the thermal cycle. The free thermal expansion can be reduced primarily by choosing a laminate material with a higher T_g, but also by choosing a laminate material (e.g., with Aramid fibers) with a low CTE below T_g (see Fig. 60.43).

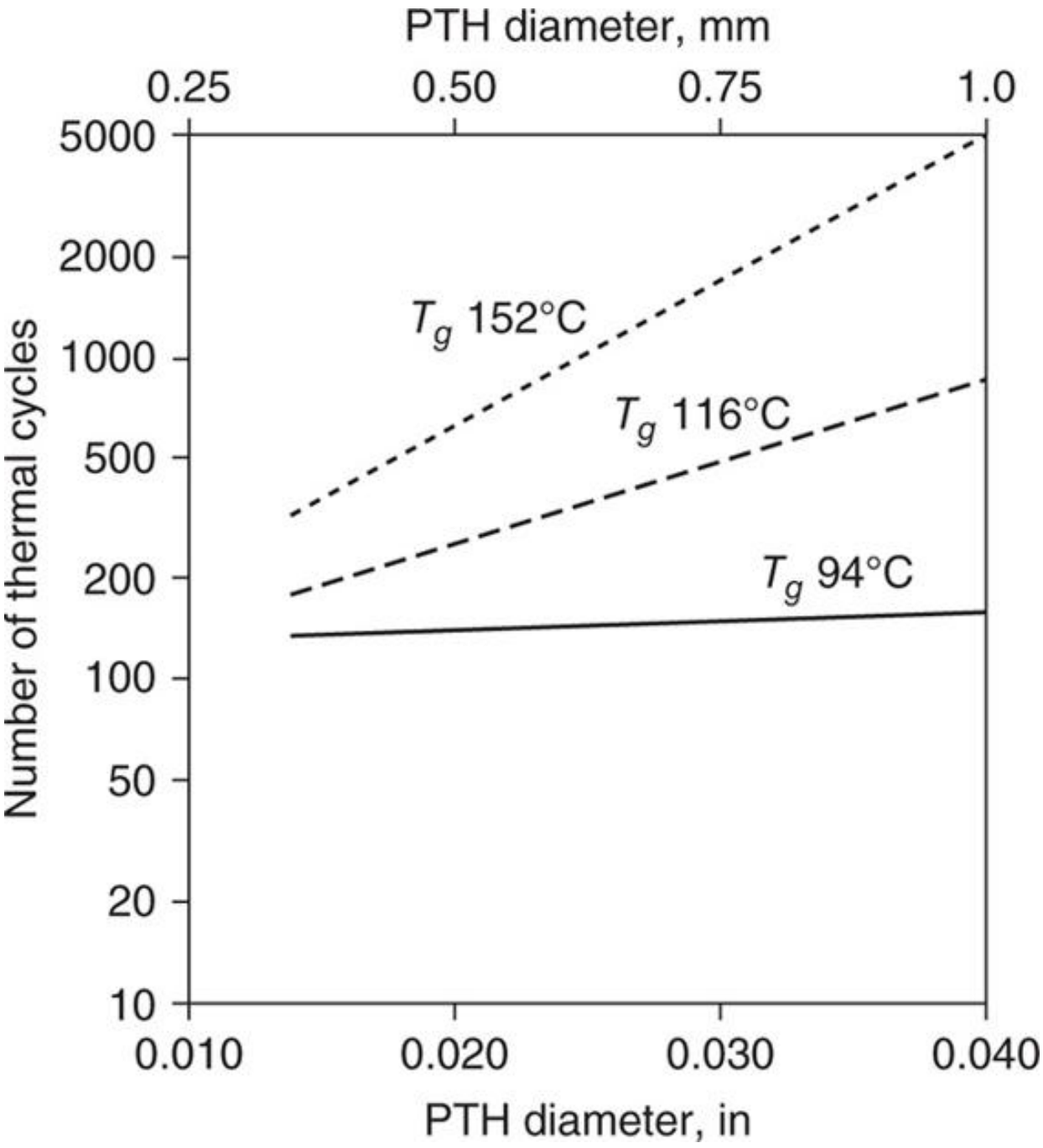


FIGURE 60.43 Effects of substrate T_g and PTH diameter on mean number of cycles to failure. The thermal cycle was 2 h with extremes at −62 and −125°C. Multilayer printed circuit board thickness 2.5 mm (0.10 in); Cu in unfilled PTH is 30 μm (1.2 mil) thick.[60]

- Decreasing the PTH aspect ratio (usually quoted as board thickness divided by finished hole size) by decreasing the board thickness or increasing the hole diameter (see Fig.

60.44). Aspect ratios tend to be higher in boards with eight or more layers because of their thickness and via density; aspect ratios greater than 3:1 require good-quality plating and aspect ratios higher than 5:1 are not recommended, in part because of the difficulty of achieving adequate plating thickness in the center of the barrel.

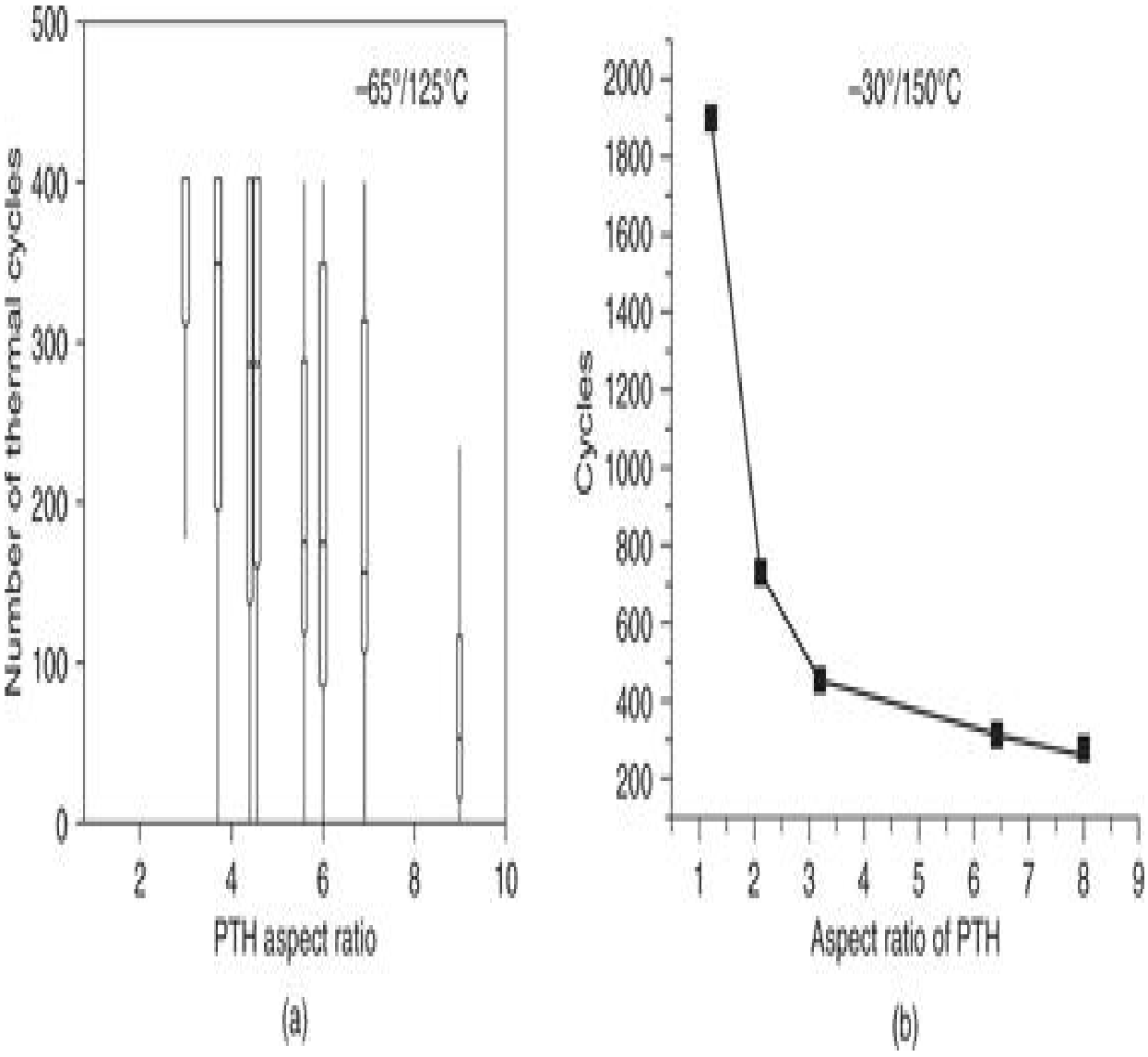


FIGURE 60.44 Cycles to failure versus PTH aspect ratio (*a*) for −65 to 125°C thermal shock cycles. Various hole diameters, board thicknesses, and board constructions[11] and (*b*) for −30 to 150°C thermal cycles modeled for two-layer PCB at a thickness 1.6 mm and plated copper thickness of 32 μm.[46]

- Increasing the Cu plating thickness (see Fig. 60.45). Increasing the plating thickness also increases the distance a fatigue crack must propagate to cause an electrical failure.

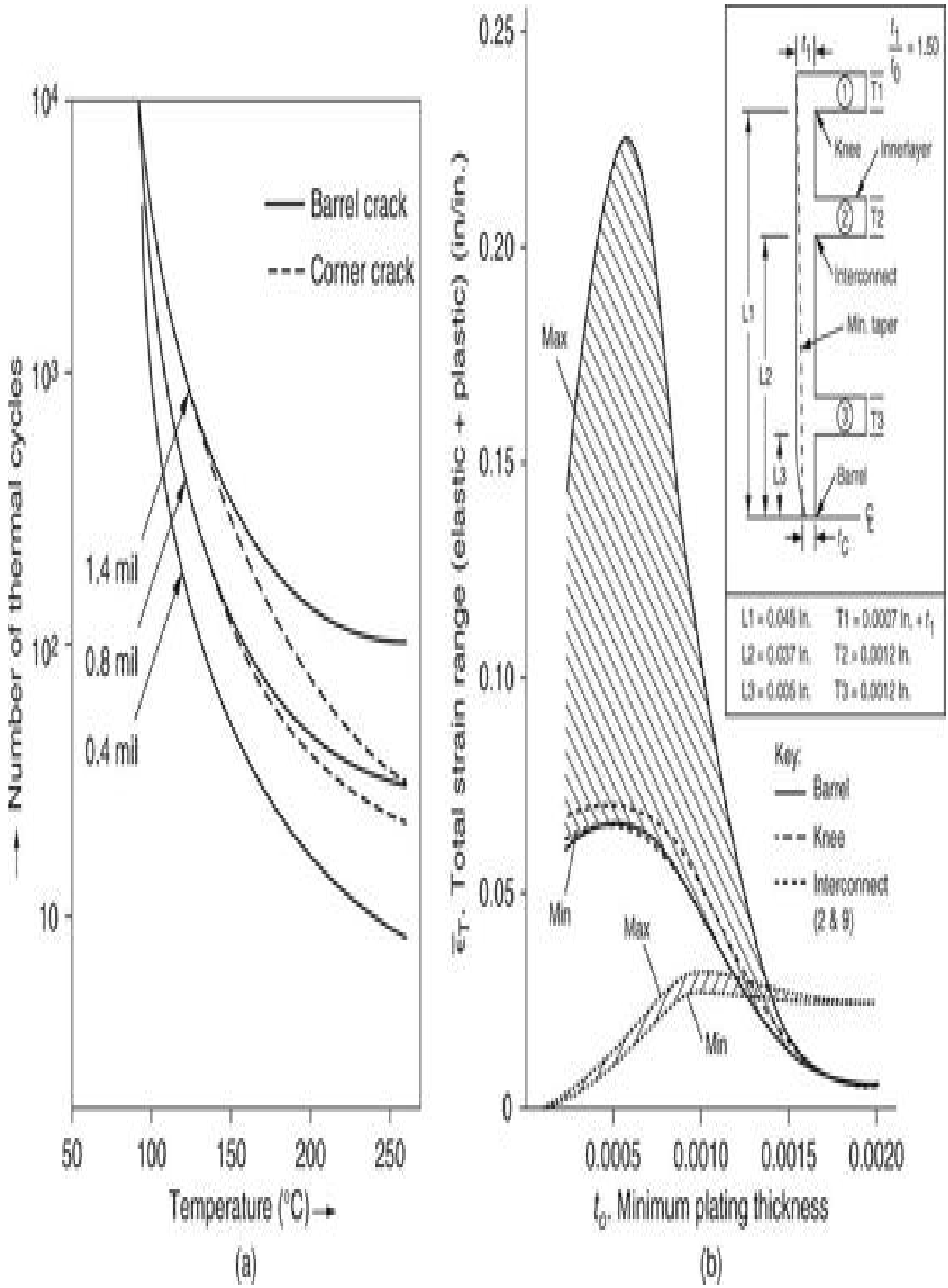

Barrel crack
Corner crack
1.4 mil
0.8 mil
0.4 mil
Number of thermal cycles
Temperature (°C)
(a)
Max
Min
Max
Min
Key:
Barrel
Knee
Interconnect (2 & 9)
ε_T. Total strain range (elastic + plastic) (in/in.)
t_0. Minimum plating thickness
(b)
Knee
Innerlayer
Interconnect
Min. taper
Barrel
L1 = 0.046 In.
L2 = 0.037 In.
L3 = 0.026 In.
T1 = 0.0007 In. + t_1
T2 = 0.0012 In.
T3 = 0.0012 In.

FIGURE 60.45 Effect of PTH plating thickness (*a*) on number of thermal cycles to failure for thermal cycles with the indicated peak temperatures for acid-sulfate copper and FR-4 boards[61] and (*b*) on the total strain energy induced at various plating locations.[60]

- Using Ni plating over the Cu. Nickel as one of the layers of a surface finish is either good, or, detrimental in PCB reliability. Normally well applied nickel extends the life of circuit boards by a factor of three or more.[31] Usually, the nickel interconnect structure survives 1000 cycles. The nickel stops the crack and performs well in thermal cycle testing. The crack forms after many thermal excursions but stops when it hits the nickel. However, coupons with nicks, bubbles, or breaks in the nickel finish will fail early. They tend to fail in a third the time of the same coupons without nickel. It appears that a defect in the nickel will force a crack that will crack from the nickel layer into the hole. This is called nickel acceleration. It is a rare condition but is common enough that it should be taken seriously.
- Decrease the number of PCB layers and increase PTH density (see Fig. 60.46). In the multilayer PCB, the quantity of stack up and copper foil layers may vary dramatically, from one to dozens. Based on a fixed PCB thickness of 1.6 mm (63 mil), a PTH diameter of 0.25 mm (10 mil), and a plated copper thickness of 32 μm (1.26 mil), the fatigue life of PTH in PCB with two, four, six, and eight layers of copper foil were modeled.[46] The predicted results are shown in Fig. 60.46. It can be seen that the fatigue life of PTH decreases with the increase of PCB layer quantity. The effect of PTH density on fatigue life also indicates that the board with more populated PTH (higher density), the higher the number of cycles-to-failure.

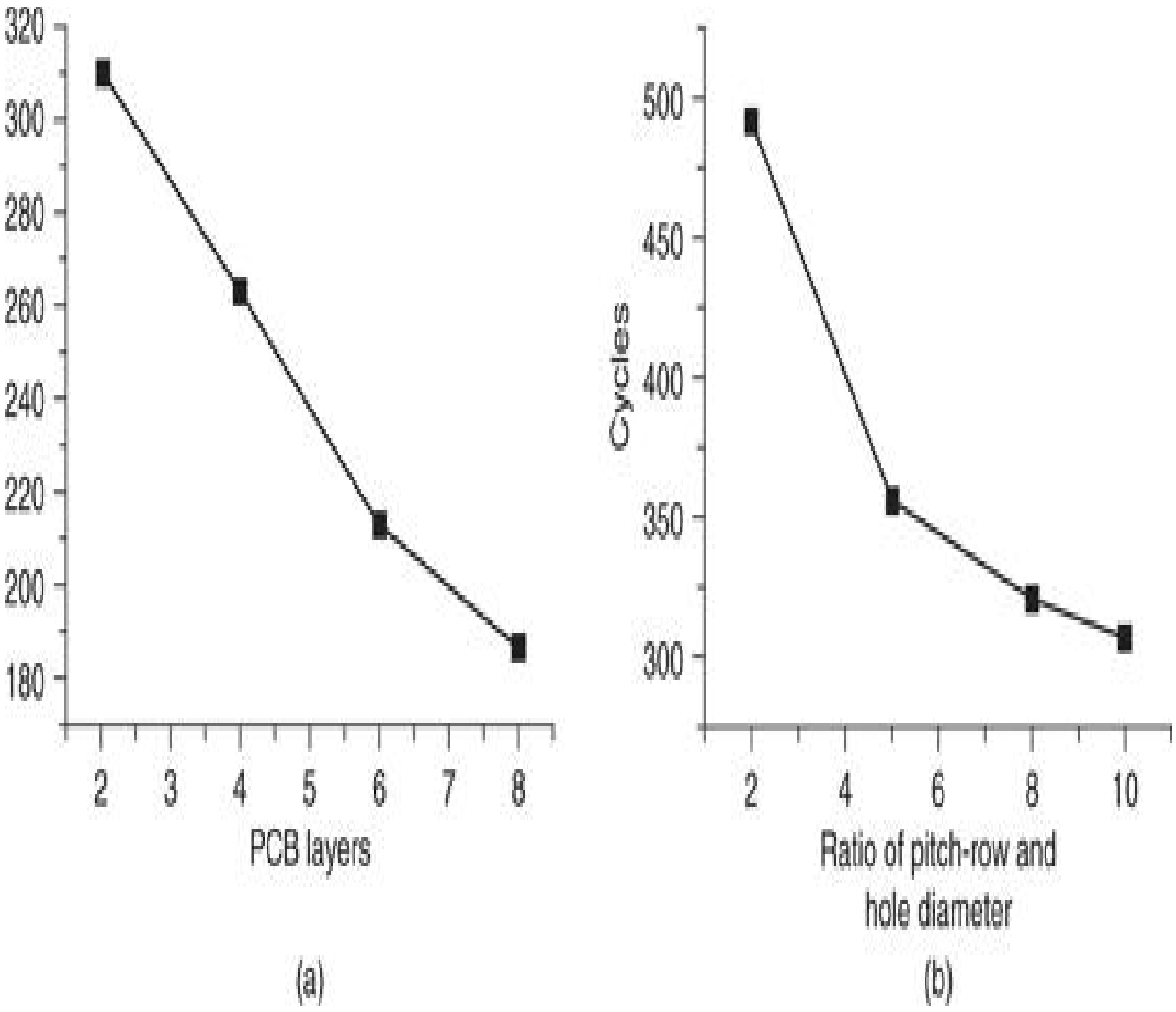


FIGURE 60.46 Prediction showing the effect of PCB geometry on PTH cycles-to-failure: (*left*) number of layers and (*right*) number of PTH (density).[46]

- The effect of types of internal copper interconnections on PCB reliability are yet to be fully characterized, but must be taken into account. Basically there are three types of internal interconnection formats, flush interconnections, etch back interconnections, and “three point” contact interconnections (see Fig. 60.47).

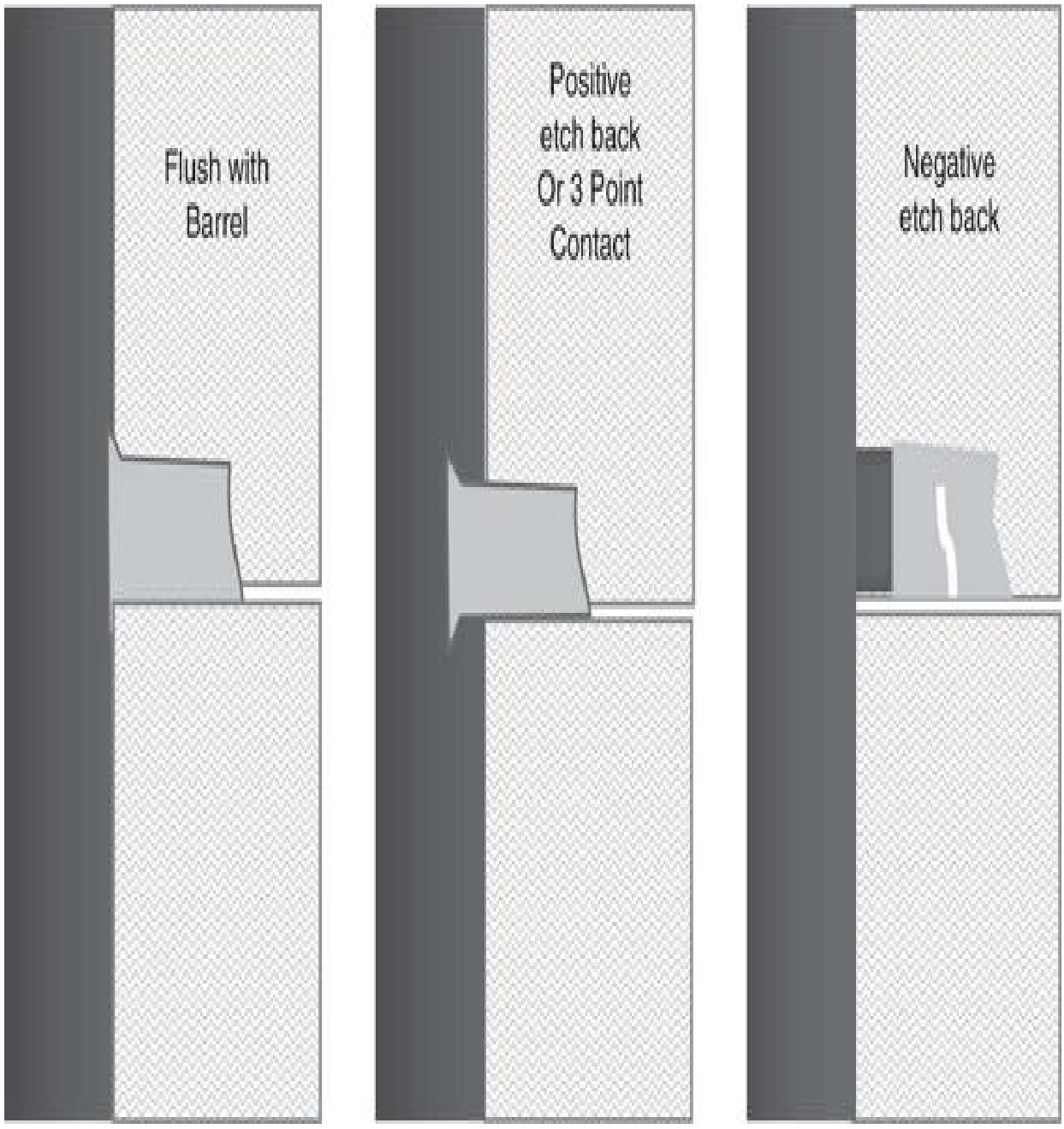


FIGURE 60.47 Three types of internal interconnections with decreasing reliability from flush to negative etch back.

Reid states,[31] although negative etchback is about as robust as flush it appears that the three-point contact has a tendency to cause foil cracks.[31] Furthermore, Reid states that “it is counter intuitive but three point contact is the least reliable” of the copper layer interconnections.[31] This is

due to potential foil cracks of the copper at the internal layer. Thus, the reliability ranking would be; flush, negative etch back, and the least reliable would be the three-point contact.

Also, numerous task groups from the IPC have performed round-robin tests to address PTH reliability including the following.

- PTH barrel cracking has been studied and the results reported in IPC-TR-609: “Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards.”[17]
- Cu foil characteristics have been reported in IPC-TR-484: “Results of IPC Copper Foil Ductility Round Robin Study.”
- For “gross” failure, thermal stress with microsectioning is performed per IPC-TM-650, “Thermal Stress of Plated-Through-Hole.”
- For “finer” failure, monitoring of a larger number of PTH samples, and objective results with numerical value, the IST test can be use which is documented in IPC-TM-650, Method 2.6.26.

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60.7 FURTHER READING

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CHAPTER 61

RELIABILITY OF MICROVIA PRINTED CIRCUIT BOARDS

Reza Ghaffarian

Jet Propulsion Laboratory, California Institute of Technology, Pasadena, California

61.1 MICROVIA FABRICATION

Vias are formed by many methods, plated through holes (PTHs) are normally made by mechanical drilling followed by plating, whereas microvias are often made by other processes, including chemical means and ablation even though for larger microvias, advanced drilling techniques may be used.[1-6] Because of chemical and ablation limitations, the microvia layers generally do not have glass reinforcement that provides the rigidity needed for handling and end use structural requirement. With advancement in ablation techniques and materials, new procedures are being developed to address this limitation. The key methods of fabricating vias are as the following:

- Advanced mechanical drilling

- Laser drilling with UV-YAG, CO_2 or UV excimer
- Photo definition processing with unsupported photosensitive dielectric
- Plasma etching using a microwave-induced gas plasma

Fabrication of nondrilled microvias may have additional conductive materials replacing either the copper foil or copper metallization.

Mechanical drilling has traditionally been the most widely practiced method of hole creation. However, for creating microvias its use is limited. It cannot be used to generate microvias, and even if it could, its isotropic drilling feature is undesirable. The vertical walls of mechanically drilled holes are straight up and down, making them less desirable for the subsequent plating operations. Other fabrication methods generate anisotropic walls with a larger opening at the top, allowing for a better subsequent wall metallization. The process steps for three major methods of fabricating nonmechanically drilled microvias are shown schematically in Fig. 61.1.

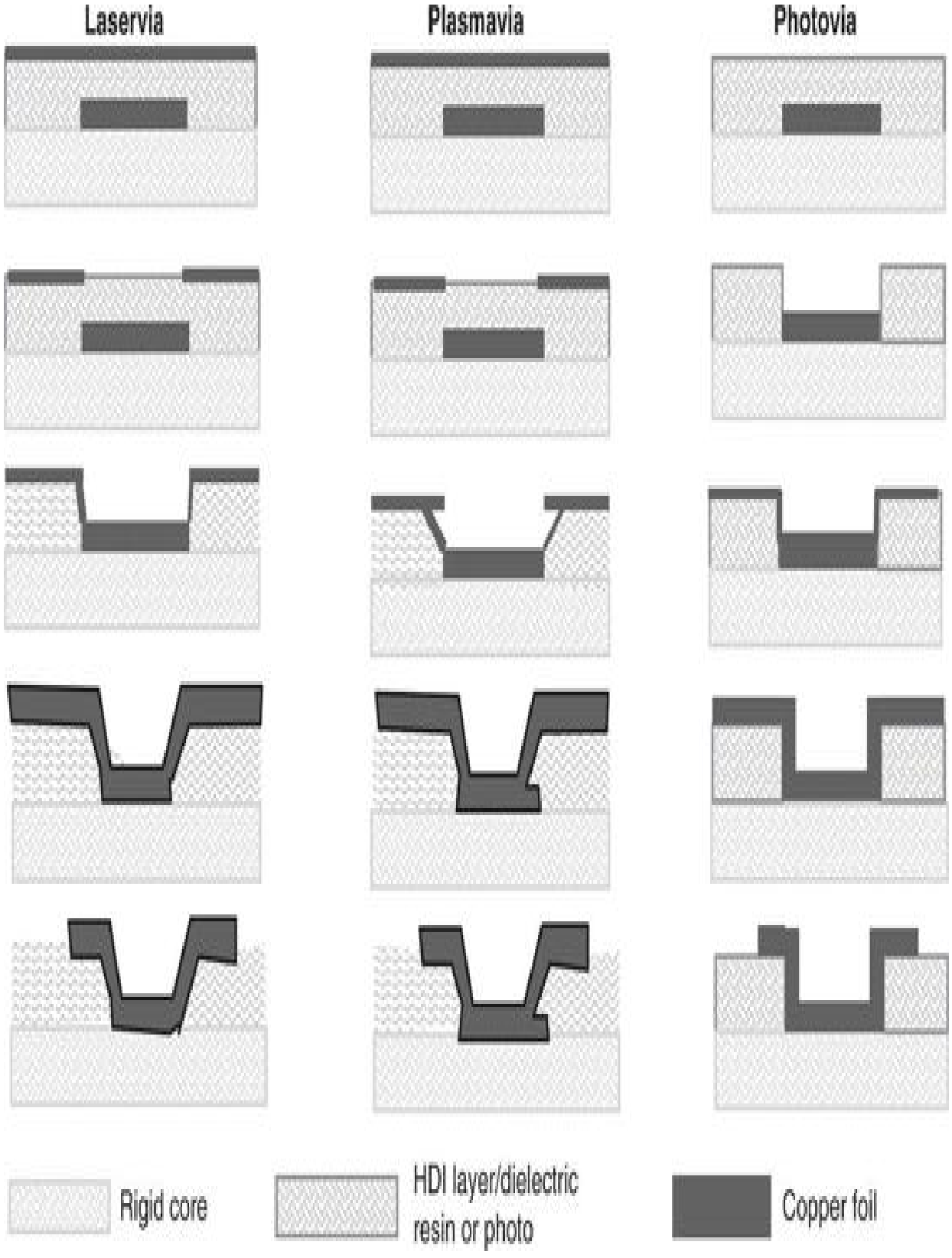

Laservia
Plasmavia
Photovia
Rigid core
HDI layer/dielectric resin or photo
Copper foil

FIGURE 61.1 Schematic drawing showing key process steps in the fabrication of three nondrilled microvias.[1]

61.1.1 Processes Involved for Fabricating Nonmechanically Drilled Holes

- *Laser ablation:* The laser-ablated formation of vias currently requires the use of nonglass reinforced laminate, such as aramid or resin-coated copper (RCC), for the dielectric. Three different drilling options for forming microvias in use are (1) transverse excitation in atmospheric pressure, (2) excimer laser, and (3) Nd:YAG (neodymium:yttrium-aluminum-garnet). The industry is making major strides to improve the throughput with lasers to make the cost more competitive with mass generation techniques such as photo and plasma vias.
- *Photovia technology:* The photovia approach is based on a photoimaged dielectric, usually a resin, and pattern plating to form the via and circuitry connections. The different photovia approaches can be broken down into three categories determined by the metallization process: (1) panel plate, (2) pattern plate, and (3) full-build pattern plate.
- *Plasma etching:* Plasma-etched vias rely on the use of copper clad nonglass reinforced laminate, such as polyimide or epoxy resin–coated copper (RCC) for the dielectric. The copper foil is used as a conformal mask to define the via openings in the process.

Paste via technology is another category that is widely used to produce via interconnections for commercial applications. Two common technologies in this category are ALIVH™ (Any-Layer Interstitial Via Hole), which is a

trademark[1,2] and B^{2}it^{TM} (Buried Bump Interconnection Technology, another trademark).

Table 61.1 and show the compatibility of via formation by the three techniques: laser, photo, and plasma, on four basic surface dielectric structures.[1,3] Laser vias can be produced in all four structures, whereas use of the other two techniques are limited. This is one reason why laser vias are more widely used. Table 61.2 shows a number of HDI design rules presented in IPC-2315 [1].

TABLE 61.1 Compatibility of Via Formation by Various Techniques

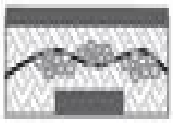
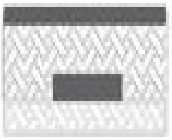
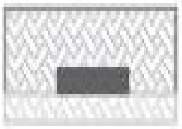
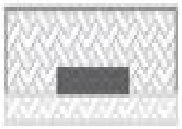
	Standard Configuration	RCC	Thermally Curable Resin	Photoimageable Resin
				
Photo via	No	No	No	Yes
Laser via, CO_2	Yes?	Yes?	Yes	Yes
Laser via, YAG	Yes	Yes	Yes	Yes
Plasma via	No	Yes?	No	No

TABLE 61.2 Example of HDI Design Rules Illustrated in IPC-2315[1]

Feature	High Yield/Low Cost, µm (mil)	Common, µm (mil)	Top-Level Fabricator, µm (mil)	Exotic Fabricator, µm (mil)
Microvia hole diameter at target land, no plating	125–200 (5–8)	100–200 (4–8)	75–250 (3–10)	35 (1.5) min
Microvia diameter at capture land	350 (14)	300 (12)	250 (10)	150 (6)
Trace spacing on rigid outer layer	125 (5)	100 (4)	87 (3.5)	5 (2)
Minimum HDI dielectric thickness	75 (3)	62.5 (2.5)	50 (2)	25 (10)
Minimum aspect ratio	< 1.0	1.0	1.0	1.3 min
Minimum plated thickness	25 (1)	25 (1)	30 (1.2)	(1.20)

61.1.2 Microvia Failure Mechanisms

Figure 61.2 shows schematically a microvia with several common key failures and locations. The most common failure modes are a separation between the microvia base and the target pad, followed by a barrel crack and a corner crack. Occasionally, a pull-out failure occurs due to a circumferential crack around the via base.[4] The buildup interconnects are stacked microvias or stacked microvias on buried vias, where they are also copper capped as part of the electronic circuit. Stack microvias show additional failure modes and a greater tendency for corner cracks, particularly with the copper filled version. The extra failure modes require a mature process that is in balance in order to produce robust buildup structures.

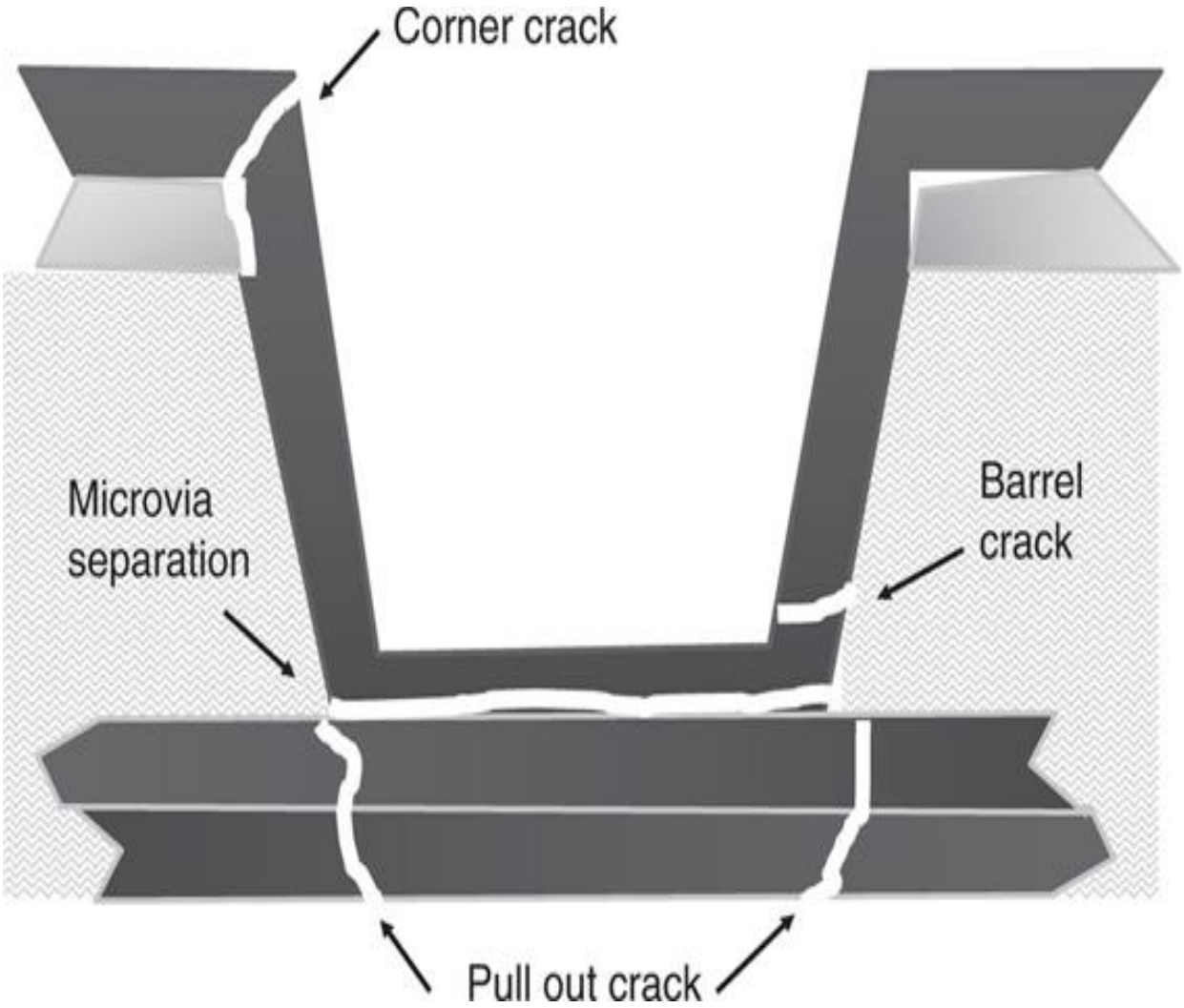


FIGURE 61.2 Common failure mechanisms for plated-through hole vias.

61.1.3 Microvia Reliability under Thermal Cycling

Microvia reliability covers two key areas: (1) the reliability of the printed circuit board (PCB) with microvias as formed and its resistance to normal assembly processes and subsequent user applications, and (2) after assembly, the effects of via-in-pad microvias on solder voids and the effect of the via structure on use conditions, including exposures to thermal and mechanical exposures. In late 1990, ITRI (the former

R&D division of the IPC) established limitations in size fabrication and relative reliability of various microvias. Further, more recent investigations on this subject are first discussed followed by the results of an internal thermal cycle testing.[5,6] Reliability modeling approaches and projections are also presented.

61.1.4 Microvia Voiding

One of the main assembly issues for the via-in-pad (ViP) microvias is the formation of voids in solder joints. Blind ViP is the most efficient routing to accommodate high-density interconnects, especially for area array packages with pitches lower than 0.8 mm (32 mils). Voids could result when gases trapped in microvias do not escape during reflow. A number of authors[7,8] investigated the effects of package pitch size, board design (including microvia sizes and surface finish), and assembly process parameters on the formation of voids. Their findings for tin-lead solder are summarized as follows:

- With the exception of 1.27 mm (50 mil) BGAs, as the pitch decreased so did the occurrence of voids.
- The smaller the microvia size, the smaller the void size. The centered and off-design microvias had the most voids, whereas the copper-filled and inverted microvias showed virtually no voids.
- Electroless nickel immersion gold (ENIG) surface finish PCBs tend to generate more voids compared to IAg (immersion silver) and organic solder preservative (OSP) finish; ENIG with 25 percent higher voids than IAg. In addition, with ENIG, voids were present at the component site after the first reflow and moved to the PCB site after the second reflow.

- A reflow profile with extended soak above 150°C, a lower peak reflow temperature, and a shorter reflow time were all effective to some extent in reducing voids. Conversely, solder paste type, solder particle size, and double-pass paste printing had a minimum effect on voiding. The addition of silver to tin-lead eutectic solder paste decreased void size.
- The 4-mil ViP accounted only for 6 percent of the total voids, whereas the 150- and 200-µm (6- and 8-mil) ViPs had equally high void percentages with 40 and 46 percent, respectively. Microvias with one layer of depth accounted only for 12 percent of the total voids, whereas those with three layers of depth (layer 1 to layer 3) accounted for 56 percent of the total voids.
- The thinner the PCB, the more voids produced.

For SnAgCu (SAC) solders, the voiding rate arising from microvias was studied by simulation.[9] It was shown that the lowest voiding was for Sn95.5Ag3.8Cu0.7 and Sn95.5Ag3.5Cu1.5. The voiding rate increased with decreasing Ag content from Ag3.5, mainly due to increasing surface tension. Voiding arising from microvias was governed by via filling and exclusion of fluxes. The voiding rate decreased with decreasing surface tension and increasing wetting force, which in turn was dictated by the solder wetting or spreading. Both low surface tension and greater solder wetting prevented the flux from being entrapped within the microvias. A fast wetting speed might also facilitate reducing voiding. However, this factor is considered not as important as the final solder coverage area.

61.1.5 Microvia and PTV Failures

Microvias as part of the PCB design are exposed to thermal stresses during manufacturing and applications. These

exposures may be either prolonged at an elevated temperature or isolated with repeated temperature cycles. These exposures could lead to PCB and microvia failures. The most important sources of thermal stresses are

- Thermal shocks and thermal cycles during PCB manufacturing. The thermal shock occurs when an assembly is exposed to rapid changes of temperature causing transient temperature gradients, warpage, and stresses within the part and/or assembly. The rate of temperature change for thermal shock is usually greater than 20°C/min (see, e.g., IPC-9701A).[10] Processes that can induce this rate of temperature change are solder mask cure and HASL (hot-air solder leveling).
- Thermal shocks and cycles occurring during assembling the PCB. Examples are glue cure, solder reflow, wave soldering, and rework using soldering irons, hot air, or molten solder in a pot.
- Thermal cycles in service. Depending on the application, these can be severe or mild, but include temperature changes from inside to outside the electronic box and component local temperature rises due to functioning internal electronics.

Two key issues are important in reliability of microvias. These are (1) the continuity of plated microvias providing interlayer connections and (2) the insulation among different nets. Similar to the PTH, but to a lesser extent, microvia failures occur due to thermal strains induced due to CTE mismatch between the plated microvia and the resin.

Manufacturing issues and board-level reliability were studied for a 0.4-mm (16-mil) pitch FPBGA, where microvias exist both in the package substrate and the PCB.[11] Results were compared after thermal cycling, drop testing, and mechanical bending. ViP package substrates showed better resistance to thermal cycling by 20 percent relative to non-

ViP (NViP) package substrates. Failures were both microvia and solder-joint cracking (see Fig. 61.3). ViP/NViP combination showed excellent drop performance with the first failure after 148 drops whereas ViP-ViP combination showed poor performance with failure after seven drops. In contrast, the best bend cycling results were for the ViP-ViP followed by the NViP-ViP combinations.

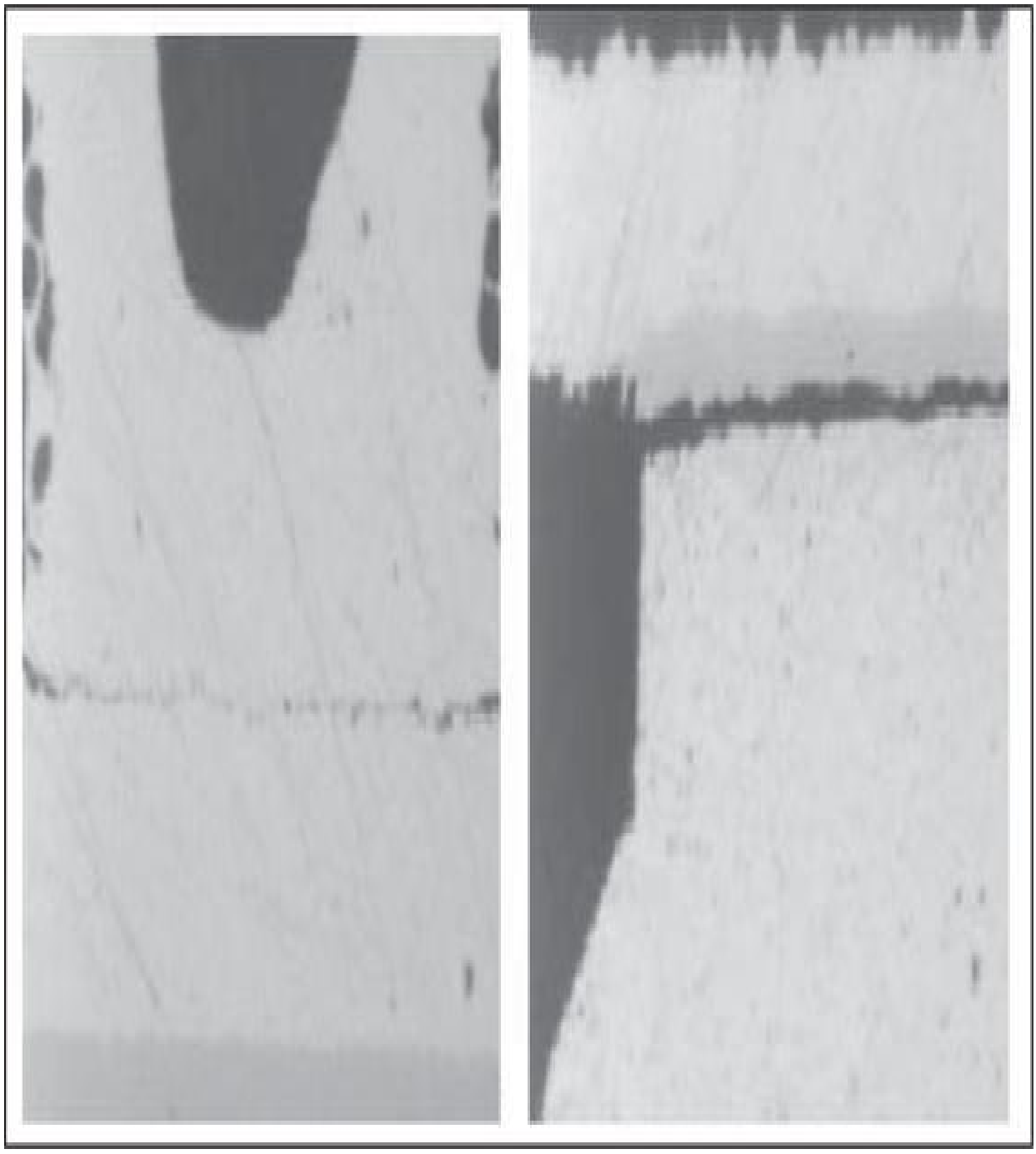


FIGURE 61.3 Package-via crack and solder-joint crack during drop test.[11]

The effect of ViP on the mechanical cycle bending behavior was investigated for 196 I/O Globtop PBGA packages with 1-mm (40-mil) pitch that were assembled onto PCBs with ViP structure.[12] Test results in conjunction with finite element

analysis indicated that the ViP structure by itself does not pose a reliability risk. However, increased applied loads could induce dielectric cracking that in turn could lead to trace and via failures.

The proximity of microvias to PTHs and its effect on the reliability of microvias was evaluated[13] under exposure to liquid-liquid thermal shock (LLTS) in the range of −55/125°C with 10 s in transition. Results indicated (see Table 61.3) that the maximum failures were from the vias at a distance of 1 mm (40 mils) [1.5 mm (60 mils) center-to-center distance from 0.5 mm (20 mils) PTH] from the PTHs. In addition, few failures were found in the vias at the distance of 125 µm (5 mils) from the PTH. The first failure was after 1100 LLTS cycles.

TABLE 61.3 Thermal Cycle Resistances of Microvias for Various Via Formation Technologies[1]

Via Hole Formation Technology	Dielectric Material	Failure Mechanism
YAG laser	Glass reinforced	No failure to 2000 LLTS (−55/125°C, 10 s transition)
YAG laser	Nonreinforced	Crack at the via pad interface
YAG + CO_2 laser	Glass reinforced	Improper cleaning of the glass fibers crack through the via
Photodefined	Nonreinforced	Crack at the via pad interface

Andrews, Parry, and Reid found that double-sided, PCB SMT assemblies for high-end use showed intermittent opens during electrical testing.[14] Using an IR technique, they were able to narrow failures to microvias. Cross-sectioning revealed a target pad to copper plating separation at the bottom of microvia. Further investigation showed that a

small percentage of microvias exhibited barrel cracks, and sometimes, knee corner cracks.

Having marginal microvia coupons, an IST study was conducted to determine the most effective testing parameters. After five cycles of preconditioning of coupons at 230°C, the coupons were tested to maximum temperatures of 150, 170, 190, 210, and 220°C. The mean cycles to failures were 1000, 789, 464, 76, and 44 cycles, respectively. For the 190°C maximum temperature dwell, the mean cycles to failure was less than 500 cycles; therefore, this temperature was selected for subsequent thermal cycling for a Pb-free board process assembly. Failures for 210°C and above included those of knee crack, material delamination/break down, and barrel cracks that are considered to be testing artifacts; and therefore, these temperatures are unacceptable for qualification to represent realistic environment.

Phenolic-based FR-4 coupons with microvias passed 1000 IST thermal cycles at 190°C after five times at 230°C. The effect of the lead-free reflow profile at 260°C conditioning on microvia degradation was severe. The coupons that were able to achieve 788 cycles at 150°C were reduced to a mean of 443 after 6 times at 230°C cycle and only four cycles after lead-free preconditioning, six times at 260°C.

Bora evaluated ALVIH-G board technology used for cell phones having a double stack of microvias on the outer layers.[15] The microvias were laser drilled, and the interconnection was conductive copper paste. The typical design rule was 100/100 microns line/space and 200/400 via/land. Reliability of a double-sided surface-mount assembly through two reflow operations and one rework using an eight-layer thin board [0.8-mm (32-mil) thick] epoxy glass with low moisture absorption instead of aramid that has a higher moisture absorption. Assemblies with BGA passed 500 thermal shocks in the range of −25 to 125°C and a 1000-h humidity test at 85°C/85 percent. Cross-sectioning

revealed graininess of solder after thermal shock with no separation of the microvia connection to the capture pad. In addition, no layer-to-layer separation was observed when the phone level drop test was performed at 1.5 m on a hard vinyl surface.

The effects of voids on reliability of filled microvias were investigated.[16] It was shown that void shape and void size are the two important parameters affecting the degradation of microvias. Voids with a larger size, but rounded corners, were less susceptible to cracking than voids with a smaller size, but sharp corners (see Fig. 61.4). The failure mechanism was identified as low cycle fatigue, where plastic deformation occurred at locations with a stress concentration. Two (out of 65) of the nonvoided samples degraded sooner than 22 (out of 29) of the voided ones. This indicates that voiding could be beneficial to microvias in some cases by relieving stresses.

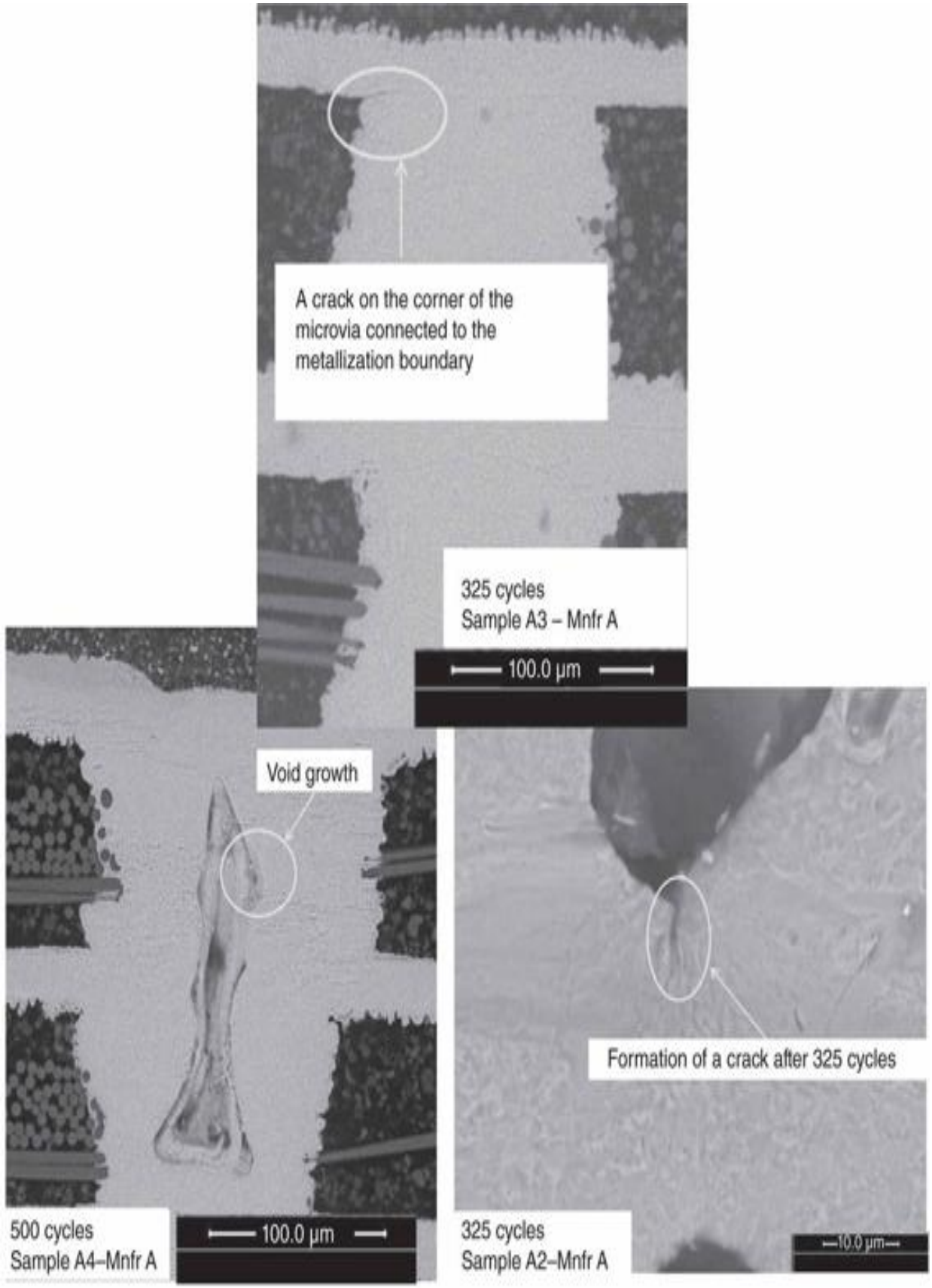

A crack on the corner of the microvia connected to the metallization boundary
325 cycles
Sample A3 – Mnfr A
100.0 µm
Void growth
500 cycles
Sample A4–Mnfr A
100.0 µm
Formation of a crack after 325 cycles
325 cycles
Sample A2–Mnfr A
100.0 µm

FIGURE 61.4 Formation of cracks on the nonvoided samples after 325 cycles (−55/125°C), top and formation of void growth and void crack (bottom).

In another investigation on the effect of via-in-pad (ViP), it was demonstrated that thermal cycle reliability for Pb-free SAC alloy depends on the particular device package type.[17] For BGA, reliability decreased with the use of ViP (see Fig. 61.5). Specifically, for the BGA192, it was found that the average void percent, including undercorner solder balls, was roughly four times greater for the VIP construction than the non-VIP construction.

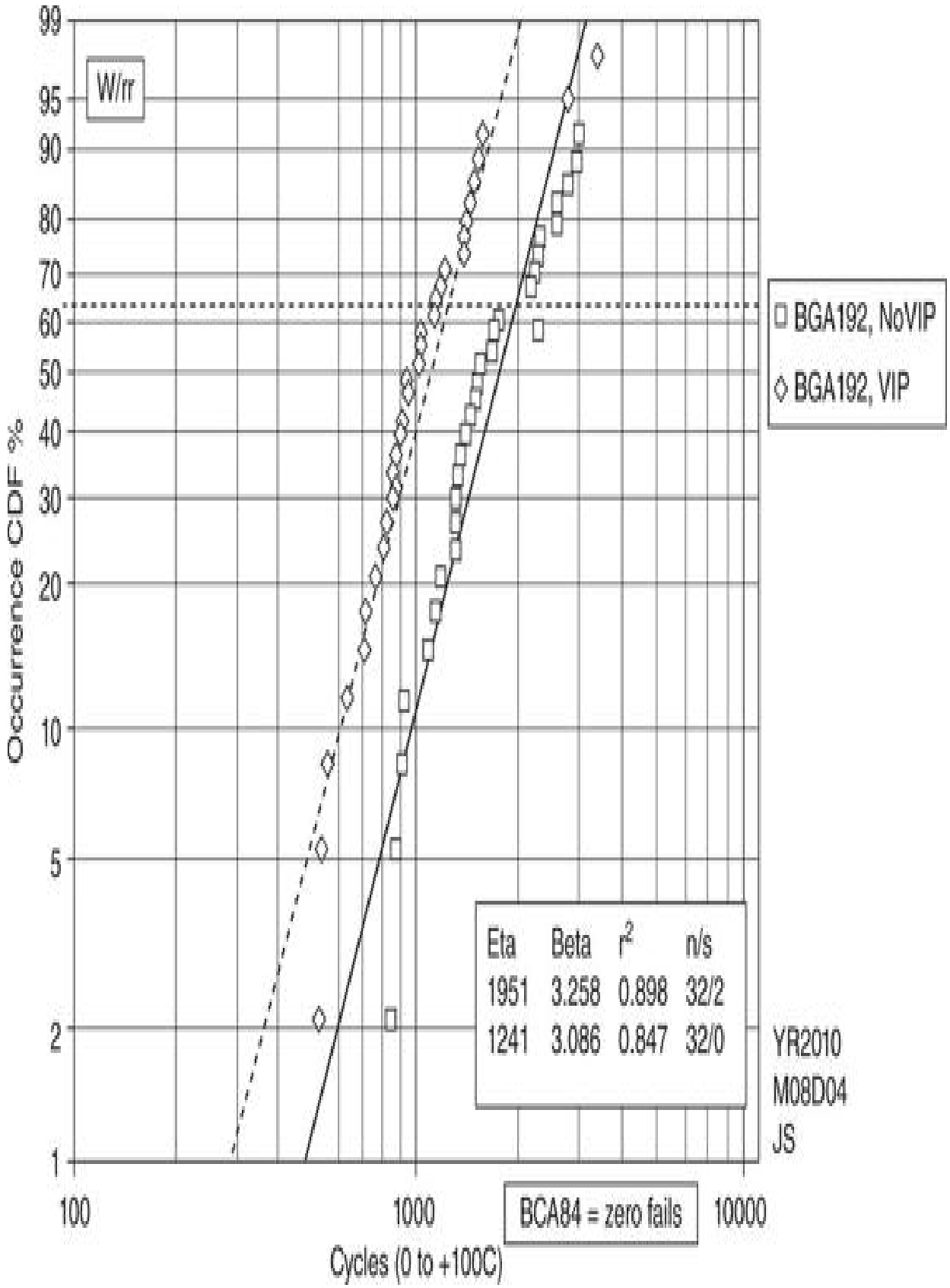

W/rr
Occurrence CDF %
99
95
90
80
70
60
50
40
30
20
10
5
2
1
100
1000
10000
Cycles (0 to +100C)
BCA84 = zero fails
BGA192, NoVIP
BGA192, VIP
Eta Beta r² n/s
1951 3.258 0.898 32/2
1241 3.086 0.847 32/0
YR2010
M08D04
JS

FIGURE 61.5 Weibull plots of the BGA192 failure data with ViP and no ViP.[17]

The authors believed that voiding associated with the conformal microvias to be the cause of the reduced solder-joint life even though the failure analysis results were not conclusive. The impact and size of the void is a function of the component type, solder ball size, microvia drill size, and laminate thickness. The voids in the fatigue crack path have a greater potential impact on solder-joint reliability than their sizes. Therefore, a greater number of voids in microvias for Pb-free than for SnPb indicates a lower life performance for Pb-free solder-joint assemblies.

In a comprehensive study,[18] both x-ray and visual inspection were utilized to characterize behavior of fine to standard microvias and nonfilled and filled vias. Figure 61.6 shows optical photomicrographs of acceptable (top) and unacceptable (bottom) microvias chosen from the two PCB lots. A number of microvias were designed with a daisy-chain configuration to monitor their integrity during environmental testing. Figure 61.7 shows representative daisy-chaining in three photomicrographs taken by optical microscopy and x-ray. Apparent in the figure are two of the daisy-chain microvias (filled) with 3- and 4-mil diameters showing darker images by x-ray, whereas the 2-mil microvias are unfilled (top row daisy chain).

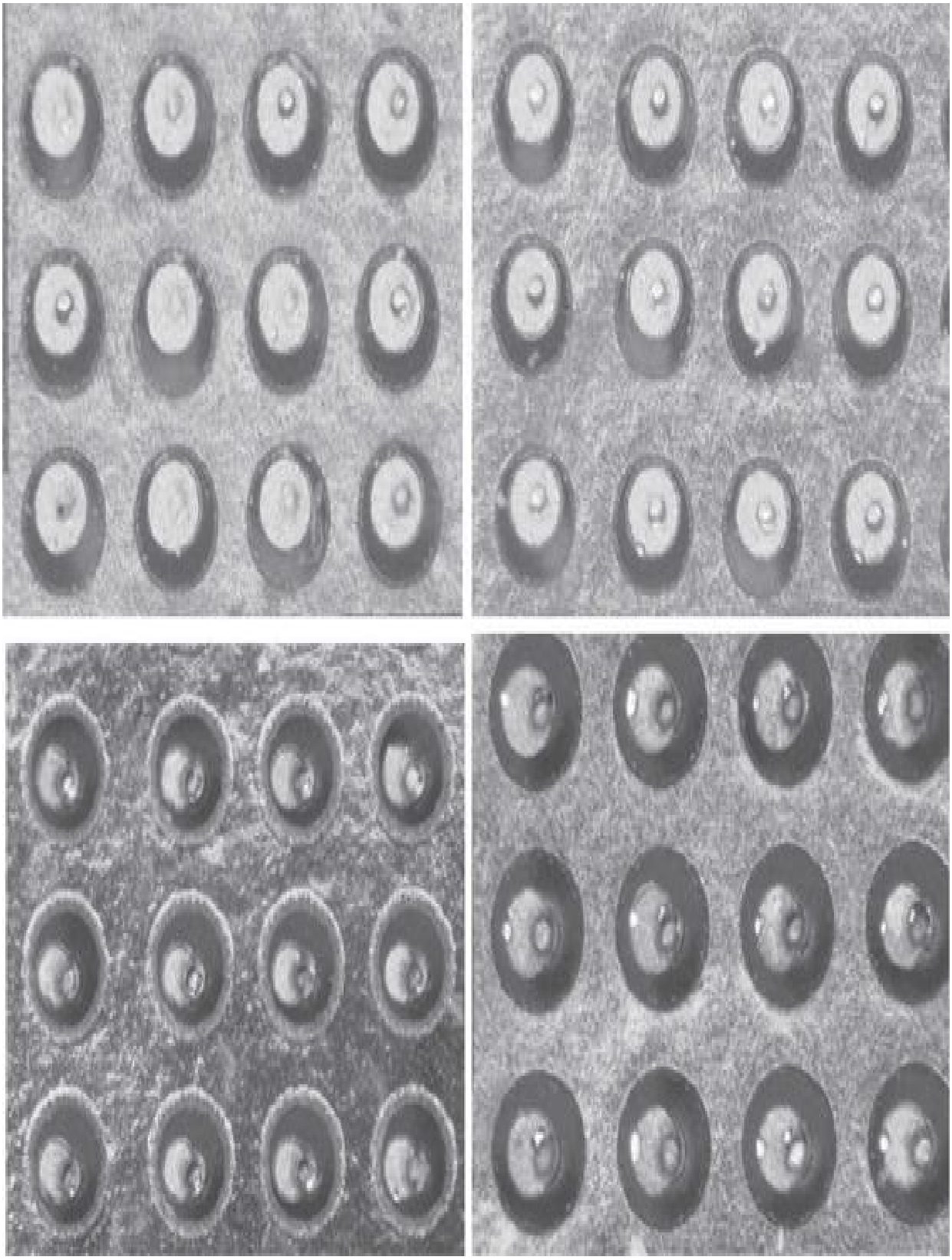


FIGURE 61.6 Optical photomicrographs of acceptable (top) and unacceptable microvias.[5]

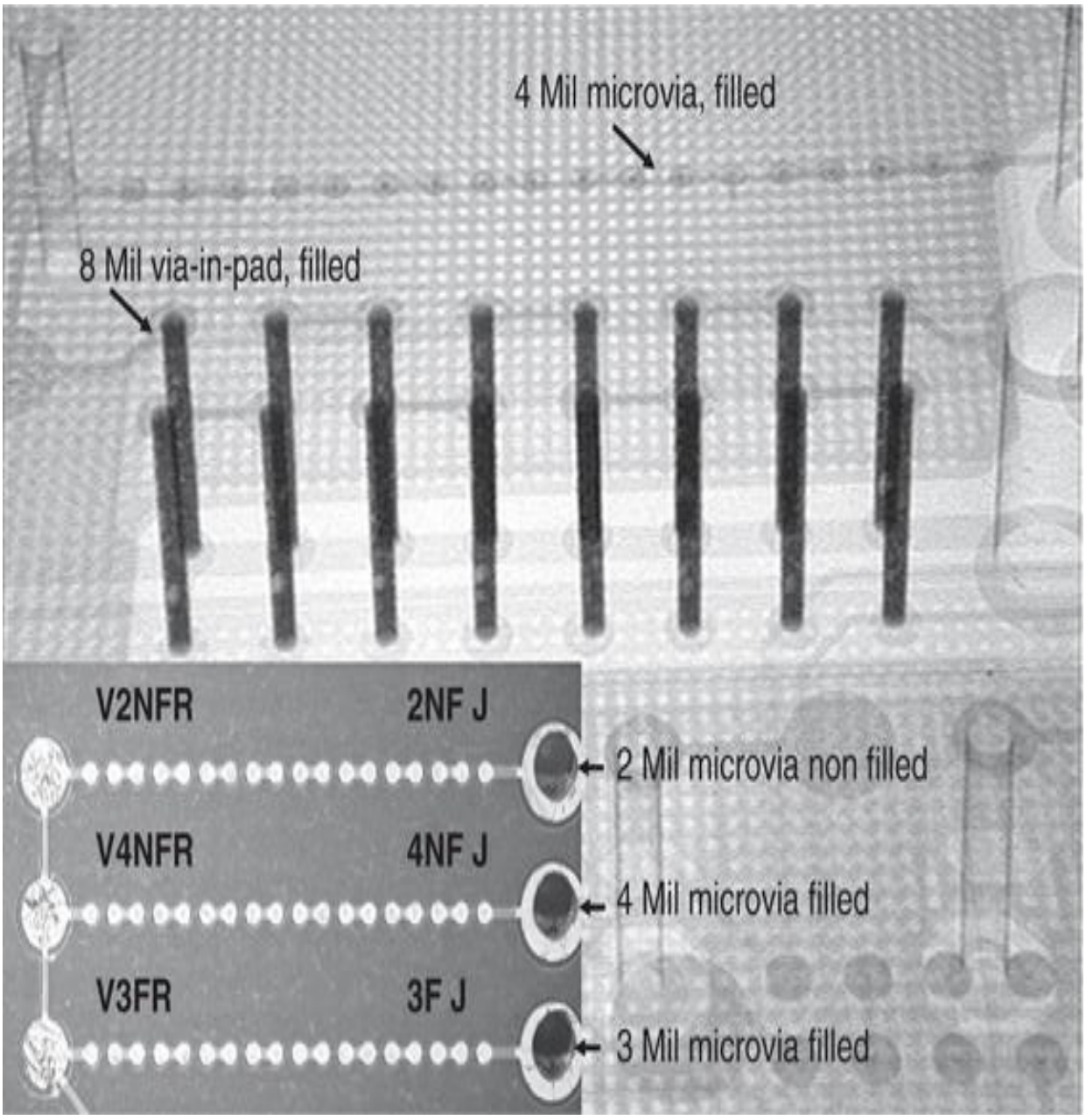


FIGURE 61.7 X-ray and optical photographs of daisy-chain microvias, filled (dark) and unfilled vias.[5]

Even though optical inspection and photomicrographs can provide some insight as to the quality of microvias, because of their fine sizes, other more power techniques (such as

SEM) are required to be performed to better characterize failure mechanisms and failure. A representative SEM photomicrograph showing failure is included in Fig. 61.8.

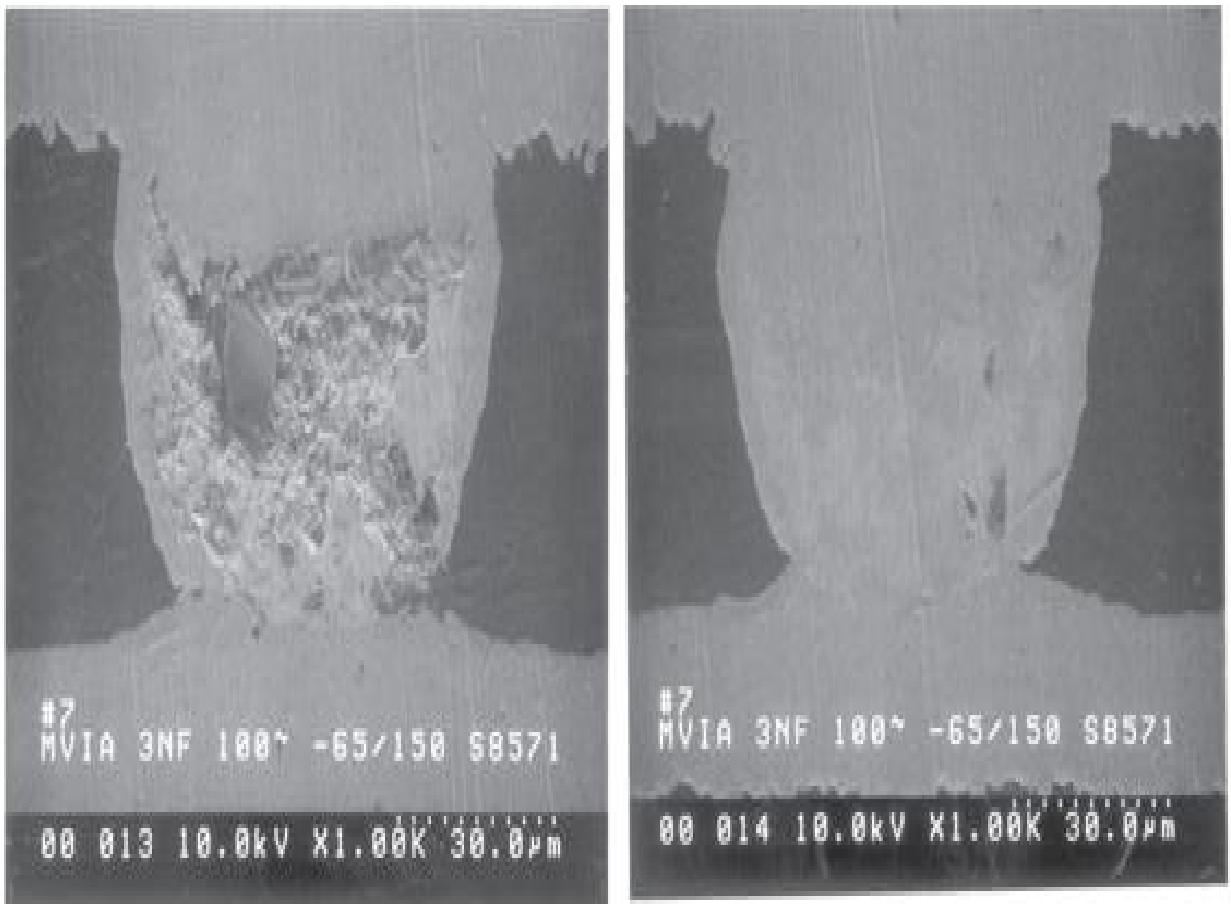
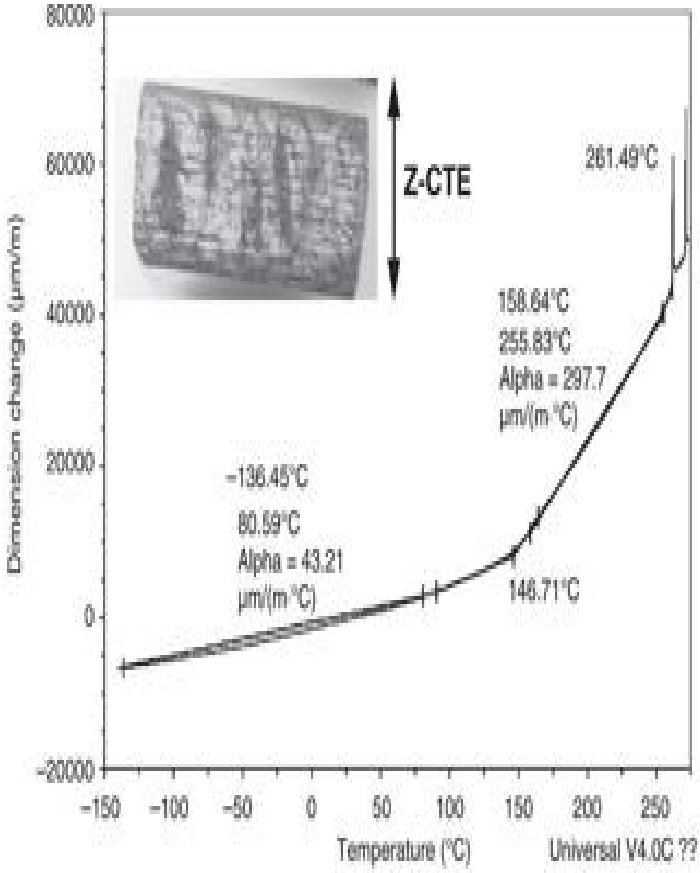
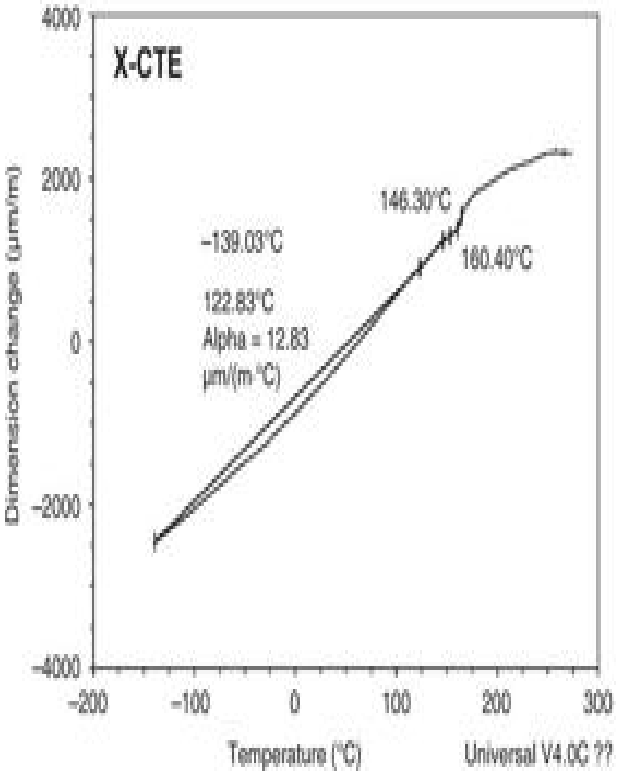


FIGURE 61.8 SEM photomicrogrphs showing cross-sections of a 3-mil, nonfill microvia after 100 thermal cycles (−65/150°C). Note, both microvias are filled even though a nonfill condition set.[5]

Figure 61.9 shows thermal expansion (CTE) for the *z, x*, and *y* directions, respectively. The CTE for the *z* direction is 43.21 ppm, which is about three times that of the *y* and *x* directions having values of 14.62 and 12.83 ppm, respectively. Above the T_g, the CTE in the *z* direction significantly increases and become 297.7 ppm. The T_g of the PCB is about 145°C (146.71°C). The T_g experiences significant changes detected about 260°C. After exposure to

this temperature, the sample was cooled to RT, and it was noticed that the PCB had delaminated. It was presumed that at lower temperatures—even with repetitive exposure—delamination would not occur.


Z-CTE
261.49°C
158.64°C
255.83°C
Alpha = 297.7
µm/(m °C)
-136.45°C
80.59°C
Alpha = 43.21
µm/(m °C)
146.71°C
Dimension change (µm/m)
Temperature (°C)
Universal V4.0C ??


X-CTE
146.30°C
-139.03°C
160.40°C
122.83°C
Alpha = 12.83
µm/(m °C)
Dimension change (µm/m)
Temperature (°C)
Universal V4.0C ??

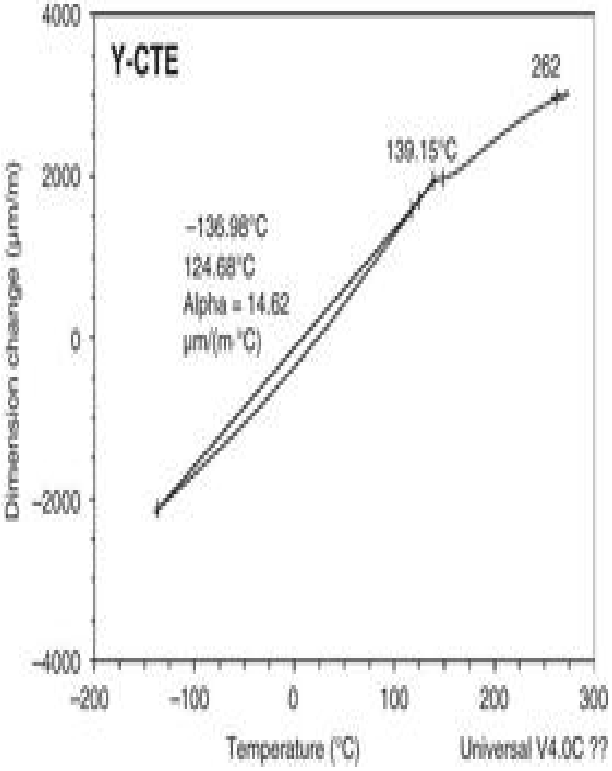

Y-CTE
262
139.15°C
-136.98°C
124.68°C
Alpha = 14.62
µm/(m °C)
Dimension change (µm/m)
Temperature (°C)
Universal V4.0C ??

FIGURE 61.9 X, Y, and Z CTEs by TMA for a thermal-cycled PCB.[5]

61.1.6 Microvia and Stack Reliability Modeling

Microvias and stack microvias are currently used for package substrates and PCB package assemblies. Readers should refer to other publications[19,20] for high-density interconnect (HDI) and through silicon via (TSV) 3D packaging technologies. For microvias used in PCBs, they are usually the most robust interconnections when considered on their own.[4] There are three types of microvias: (1) surface-mount microvias, (2) stacked microvias, and (3) buried vias (see Fig. 61.10). The most robust microvia is a surface microvia without a fill material followed by a buried microvia filled at "b-stage." The least robust are microvias with a third fill material and copper-filled microvias. It appears that copper-filled microvias are just too new and have a tendency to have corner cracks. It should be noted that stand-alone microvias with caps or without caps have no advantage, or detrimental effect, if the process is robust.

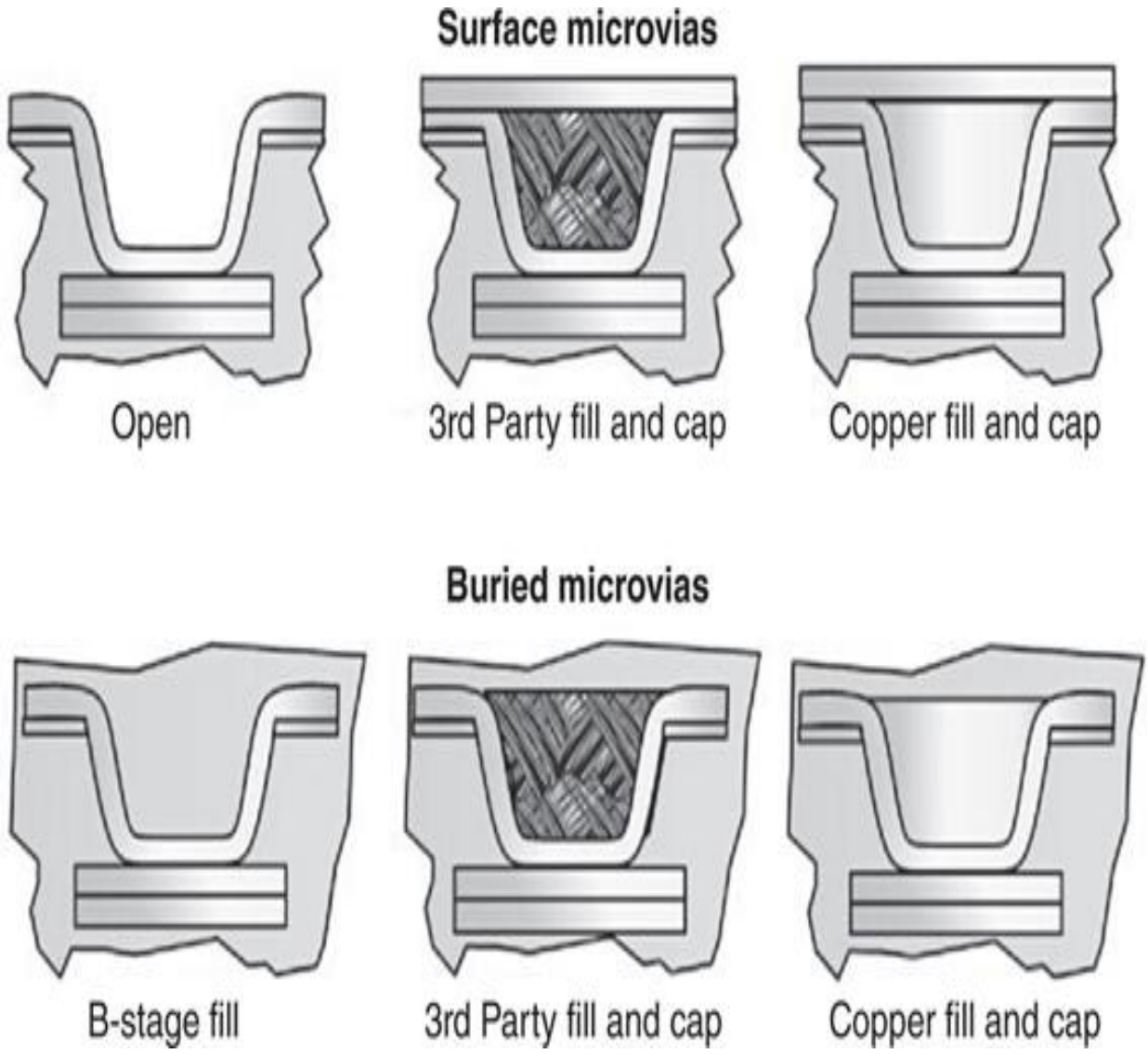


FIGURE 61.10 Three types of via fills—external and internal microvias.[4]

Improvement and control of copper plating processes was found out be a key factor for improving yield and reliability of microvias.[21] A finite element model was developed to perform a systematic analysis of the various geometric parameters of the microvias. Figure 61.11 shows the variation of TSR as a function of the diameter of the microvia. As the microvia size decreases, the TSR increases. Therefore, this leads to a lower fatigue life for the smaller microvias. It should be noted that the above study was carried out for a given dielectric thickness of 70 μm (2.75

mils). It was shown also that increasing the wall thickness of the microvia reduces the value of TSR. For 20 μm (0.78 mils) thickness, the microvia has hardly any plastic strains; therefore, they will fail due to high cyclic fatigue.

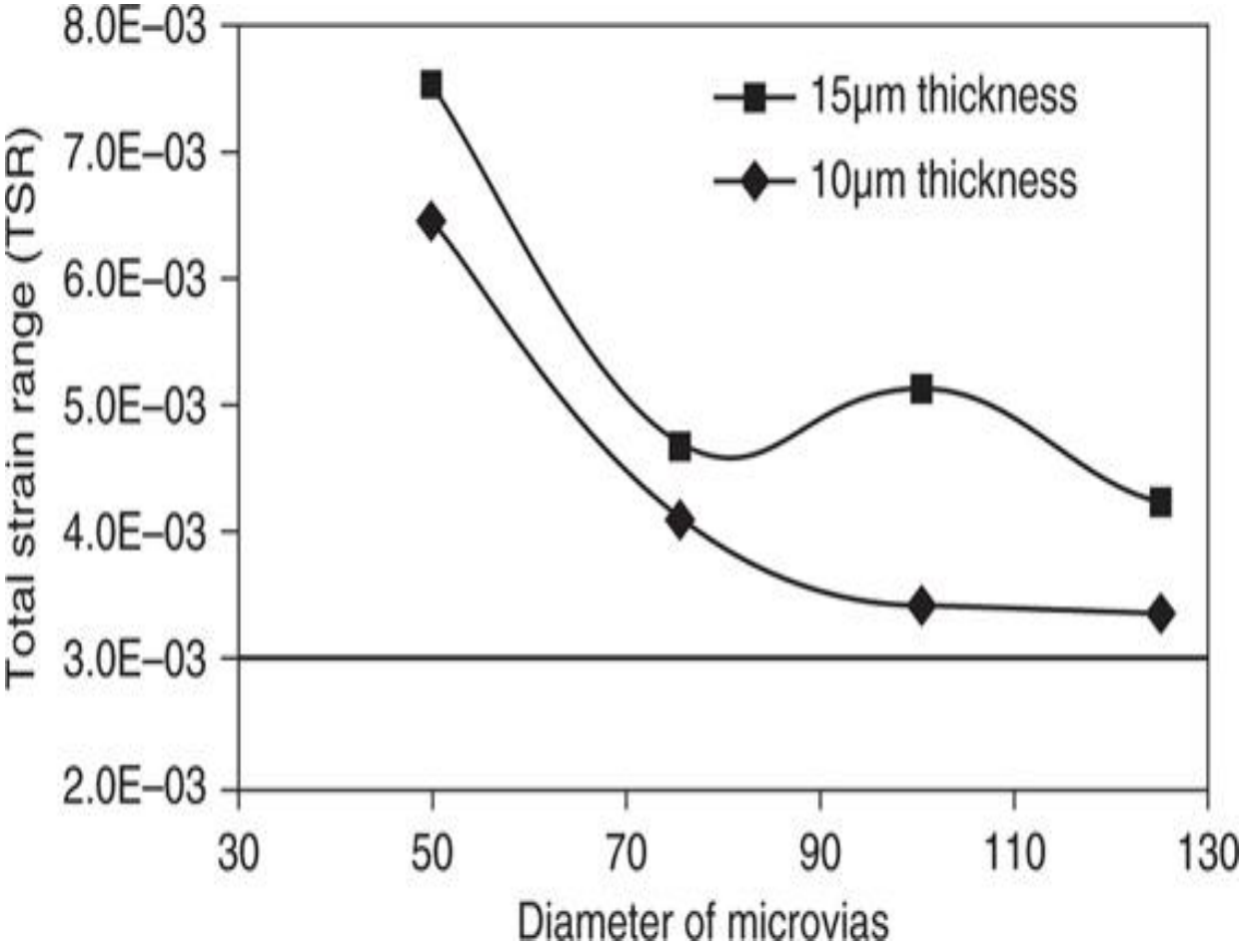


FIGURE 61.11 The variation of TSR as a function of diameter of the microvia.[22]

Analytical modeling was carried out to determine the effects of microvia buildup PCB on the wafer level chip scale packaging assembly (WLCSP). The diameters of the microvias were varied from 0.1 mm (4 mils) to 0.15 mm (6 mils) (see Fig. 61.12). Solder-joint reliability was modeled using time–temperature-dependent nonlinear analyses for Pb-free (96.5Sn–3.5Ag) and tin-lead solders (62Sn–2Ag–

36Pb). Modeling analyses showed the following effects of microvias in a WLCSP assembled onto a PCB.

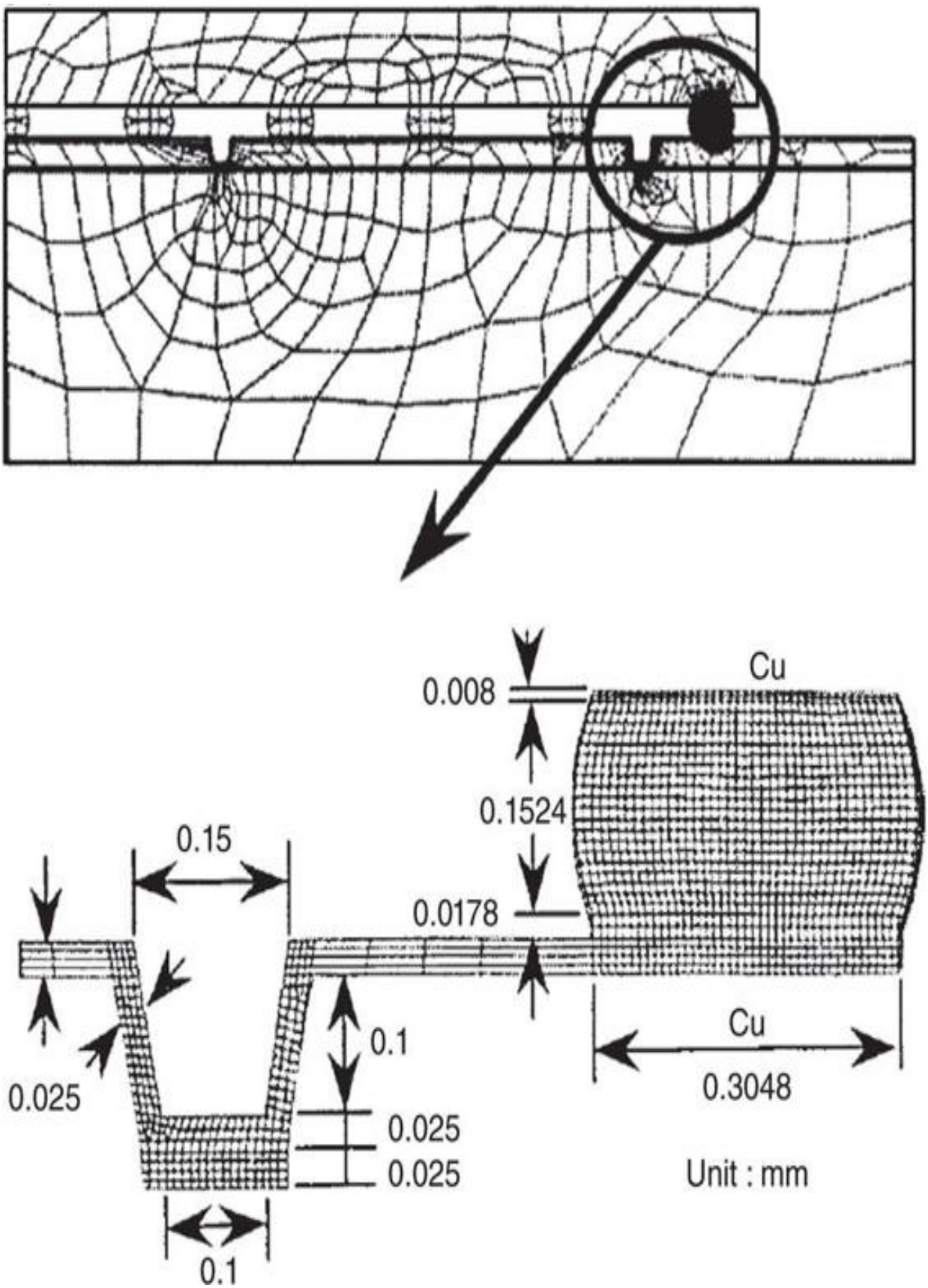

0.008
Cu
0.1524
0.15
0.0178
0.025
0.1
Cu
0.3048
0.025
0.025
Unit : mm
0.1

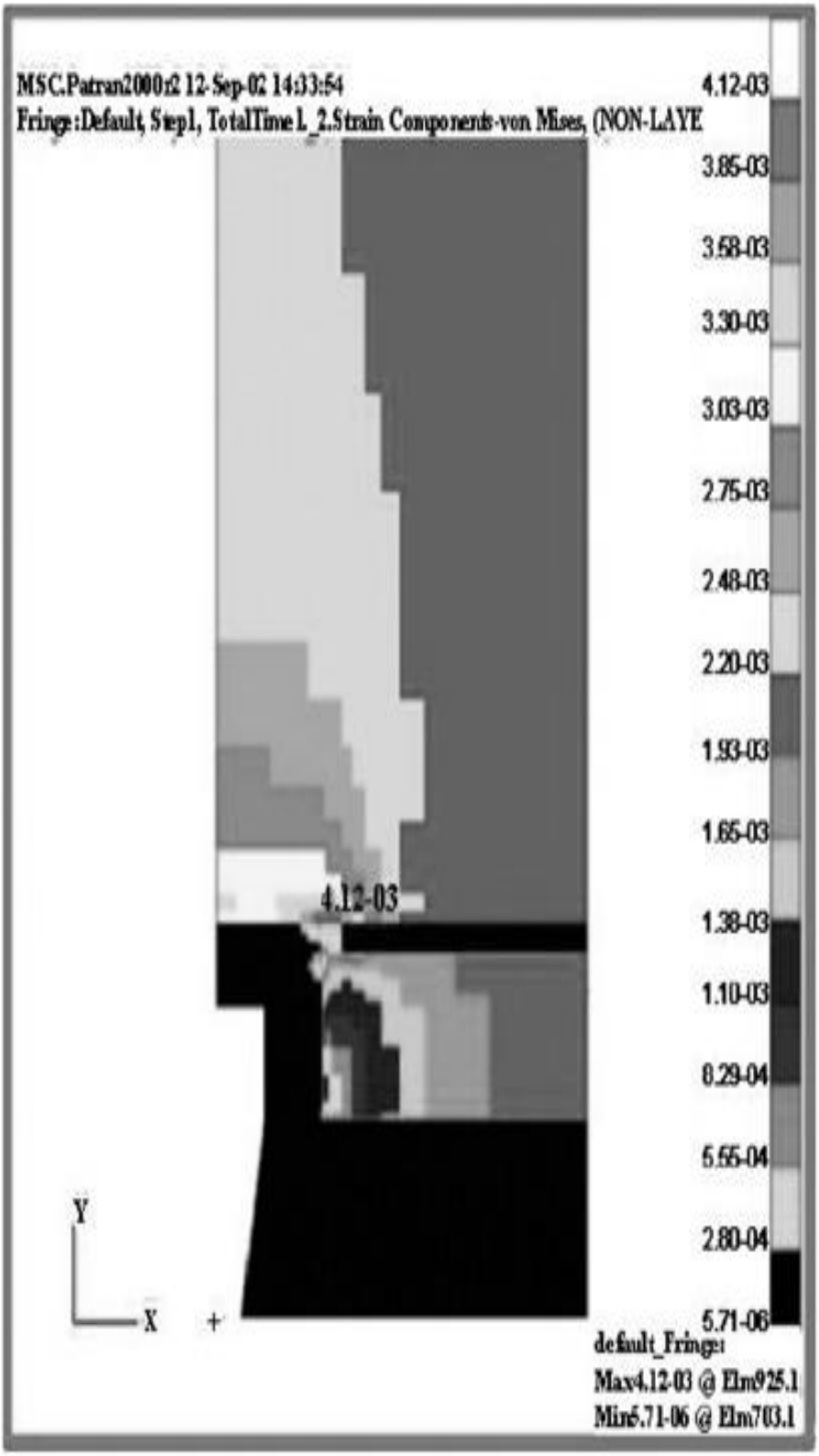
FIGURE 61.12 Detailed geometry of two-dimensional (2D) finite element mesh for WLCSP assembly.[21]

- A microvia reduces the global deflection of the assemblies and increases the local displacement of the solder joints.
- A microvia increases the shear stress range, shear creep strain range, and creep strain energy density range in the solder joints. These parameters were slightly larger for 96.5Sn–3.5Ag than 62Sn–2Ag–36Pb.
- A microvia reduces the thermal fatigue life of the solder joints.
- The maximum stress in the microvia under thermal loading was less than the ultimate strength of the electroplated copper. Also, the maximum strain in the microvia was rather small.

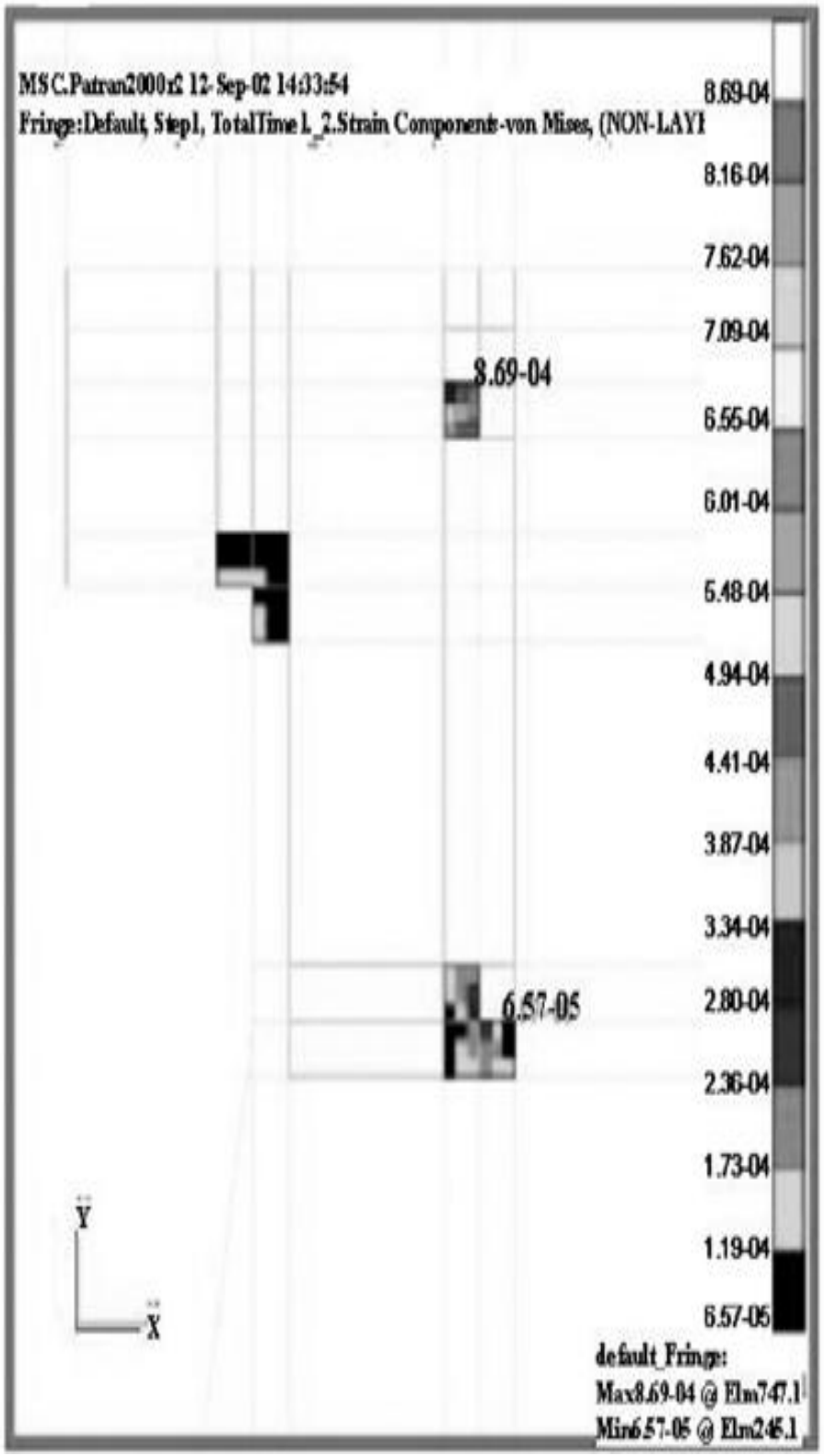
Wong et al. performed an experimental study to design, fabricate, and test various configurations of microvias over the military thermal environmental range.[23] The parameters were solder mask on printed wiring board, microvia pitch, and microvia size, with each having either two or four levels of variation. The test vehicles were subjected to temperature cycling from −55 to 125°C with continuous monitoring of microvia integrity using a daisy chain configuration. The destructive physical analysis (DPA) results showed that (1) the smaller the microvia sizes, the higher the occurrence of manufacturing defects; (2) the microvias, having electrical continuities before the test, can survive 1000 temperature cycles; and (3) there is no influence or inclusive observation of the microvia pitch variation on the microvia fatigue damage. In addition, a thermomechanical analysis with nonlinear finite element computer code applied in a 100-μm-diameter (40-mil) microvia was performed to illustrate this microvia integrity when subjected to thermal cycling.

The model consists of 1333 elements and 1413 nodes. In the FEA, the effective strain of the copper barrier was calculated using an isothermal model, which started at 25°C

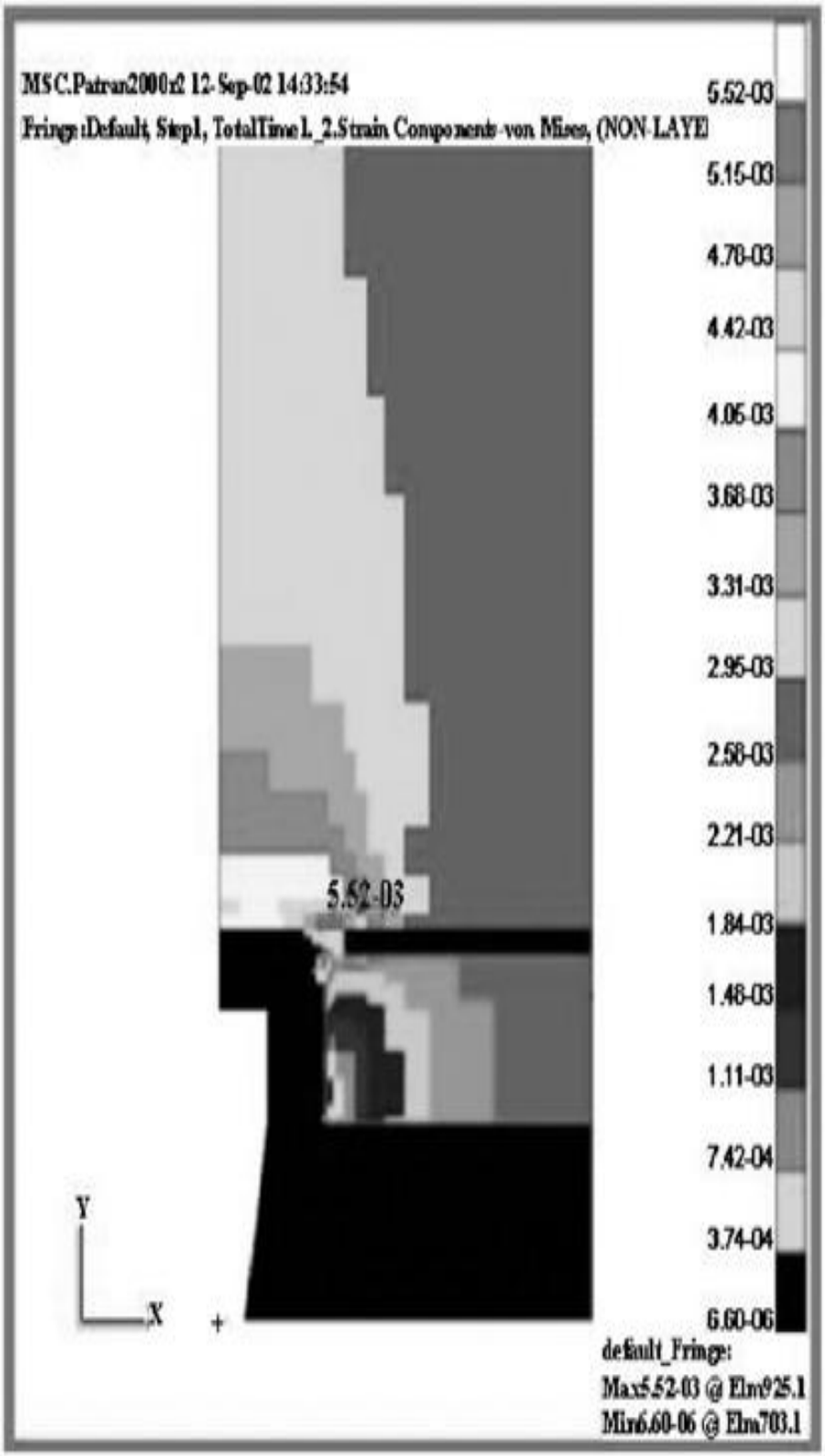
(strain-free temperature) and cycled from –55 to 125°C. The contour plots of the effective strains at −55 and 125°C are shown in Fig. 61.13. The fatigue life prediction model was based on the semiempirical model, IPC-TR-579, which relates the amount of copper strain range developed to the number of cycles needed to induce copper failure. The microvia thermal fatigue life was predicted to be 2607 cycles. The author stated that this, “agrees with the test observation that the microvia survived 1000 cycles without failure.”[23]



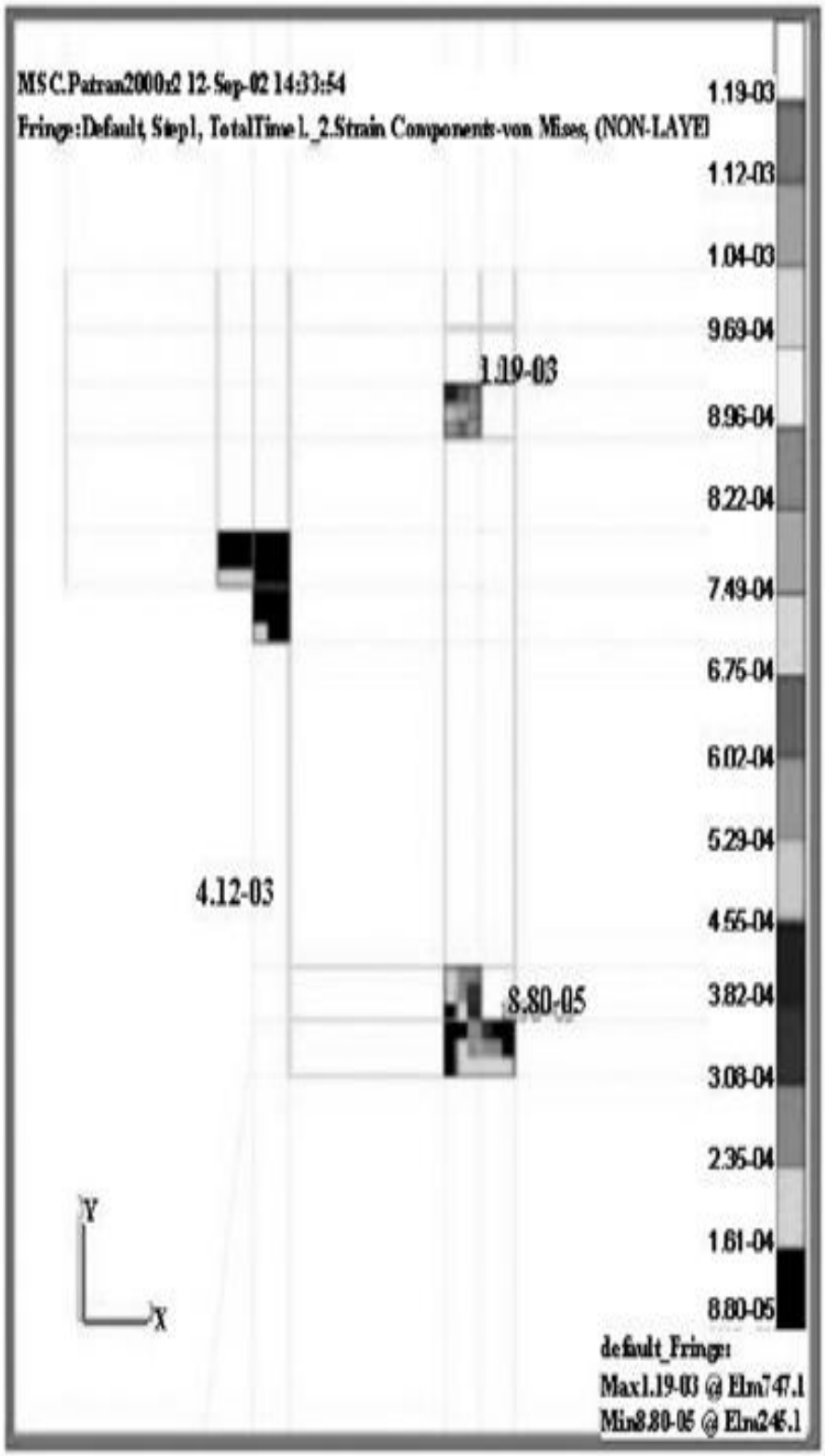
Effective Strain
Entire Model
at –55°C



Effective Strain
Critical Areas on
Copper
at –55°C



Effective Strain
Entire Model
at 125°C

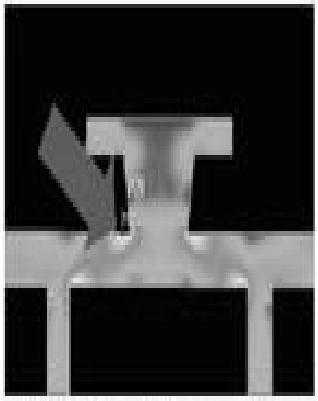
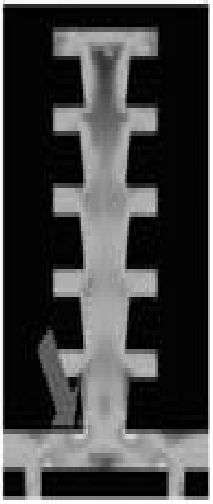


Effective Strain
Critical Areas on
Copper
at 125°C

FIGURE 61.13 Modeled effective strains at −55 and 125°C.[23]

Modeling analysis was carried out to determine the reliability effects of single and stack microvias under thermal cycle conditions of −40 to 150°C.[24] Stack microvias were assumed to be either vertically stacked on resin filled PTH (RFP) or were offset to the side of RFP. Analysis showed that as the number of stack microvias increased, the stress on the bottom microvia's corner increased (see Table 61.4). Figure 61.14 shows plots of stress versus strain for increasing microvias. The offset stack microvia showed a lower stress, it decreased from 37 kgf/mm^2 [~53 ksi (1000 lb/in^2)] to 30 kgf/mm^2 (~43 ksi).

TABLE 61.4 von Mises Stresses and Strains for the Single Microvia to Stack of Five Vias[24]

Number of Cu Stack	1	4	3	2	5
von Mises stress (kgf/mm^2)	29.737	33.327	35.631	36.930	37.192
von Mises strain (%)	0.3345	0.3749	0.4008	0.4155	0.4184
Location type A	 VIA bottom left connection between VIA and RFP type A	Same as ←	Same as ←	Same as ←	 Same as ←

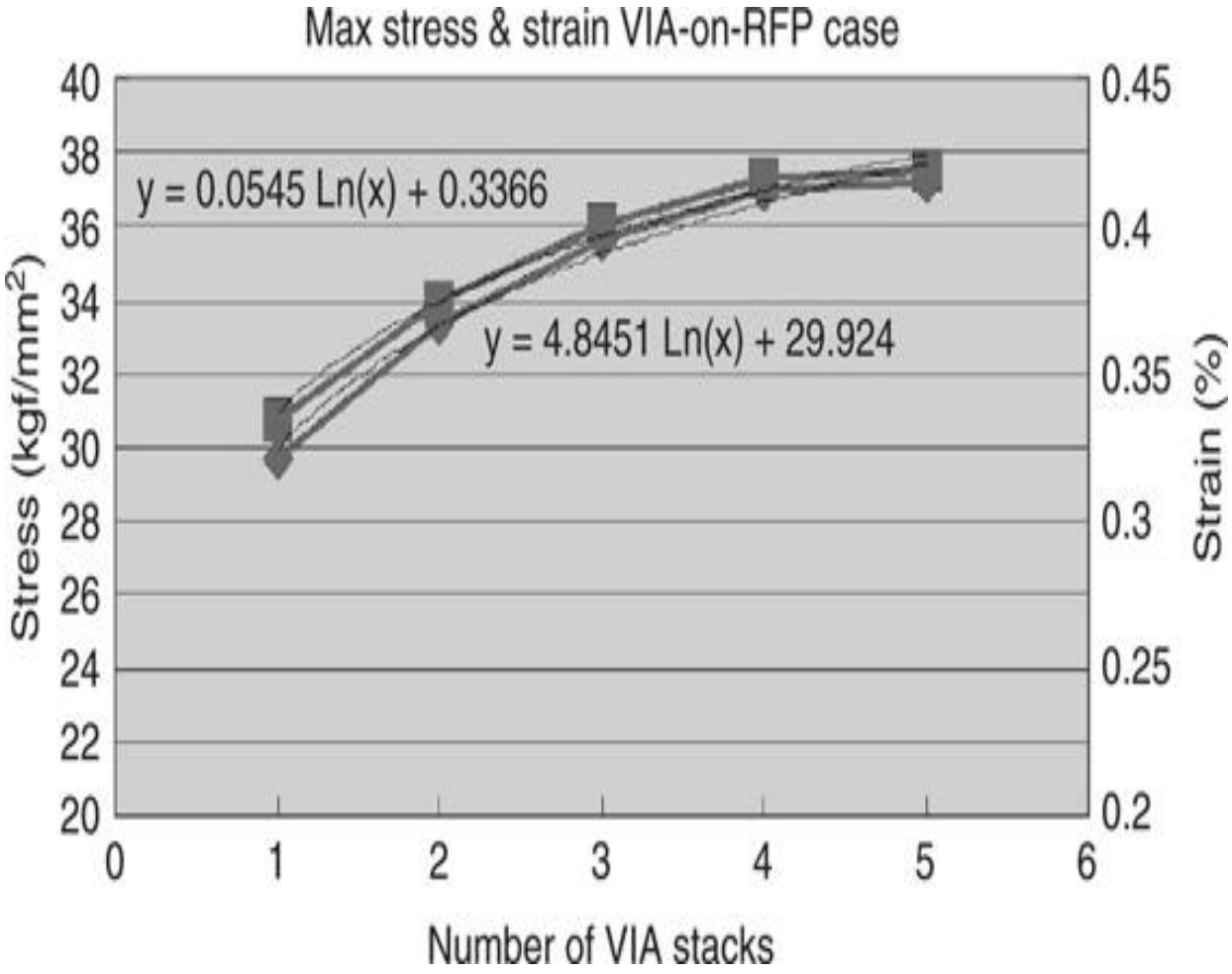


FIGURE 61.14 Maximum stresses and strains versus number of stack vias.[24]

Stack microvias show complex behavior under thermal stresses. For the stacks of three or more microvias, the microvia pad rotation was reversed on the stacks of three or more microvias.[4] The pad rotation was downward for the individual or staggered microvias (see Fig. 61.15); however, the pad rotation became upward for the stacked microvias. The stacked microvias, especially copper-filled ones, show greater tendency for corner cracks. It was shown experimentally that the stacked microvias were two orders of magnitude less robust than the staggered microvias.

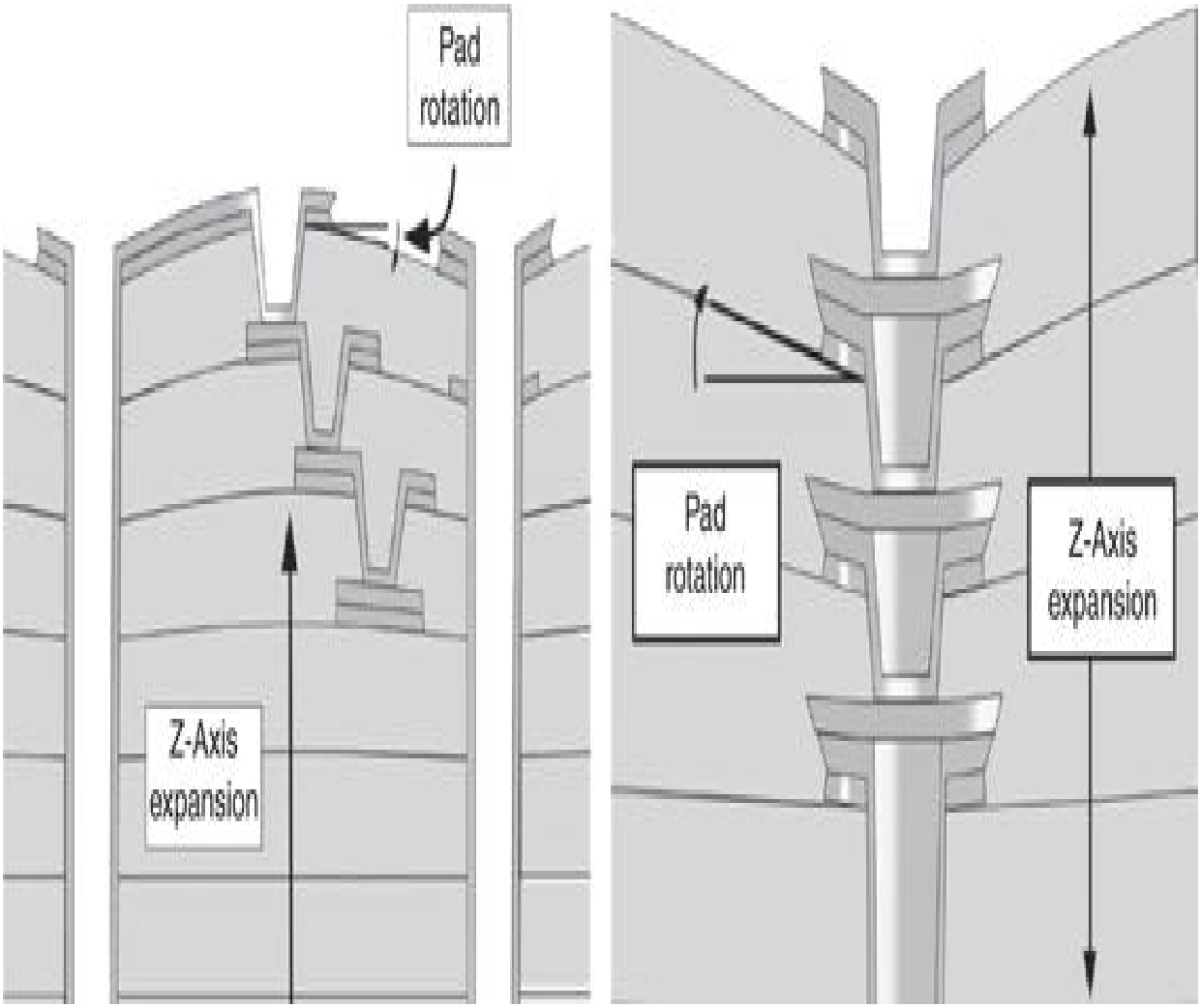


FIGURE 61.15 Pad rotation in stacked versus staggered microvias.[4]

61.1.7 Key Findings on Microvia

Key findings on microvia and plated via are summarized below. These include

- Microvia reliability involves two aspects: (1) failures due to routine PCB microvia formation and subsequent assembly processes and (2) failures due to void formation in the solder with subsequent failure during field thermal and mechanical exposures.

- Regarding microvia reliability, in the late 1990s ITRI (once part of IPC but now dissolved) with industry-wide participation performed a microvia fabrication feasibility and reliability investigation. This was an important activity with a wide-industry participation.
- Regarding microvia reliability and modeling, only limited work is available in the literature. Presentations included characterization of the effects of various PCBs and manufacturing parameters on ViP void formation at board sites, the combination of ViP/NViP in package substrates and ViP/NViP on PCBs, and the effect of distance of microvias to PTHs.
- Regarding voids in microvias, void shape and void size are the two important parameters affecting reliability. Voids with a larger size but rounded corners were less susceptible to cracking than voids with a smaller size but sharp corners.
- Limited test data indicate that reliability of conformal microvia-in-pad construction is not only device dependent, but it also depends on the solder-joint alloy used. Assemblies showed poorer fatigue life performance for Pb-free solder joints than for SnPb solder joints.
- In early 2000, a consortium successfully built test vehicles having ViP microvias from 50 to 100 μm (2 to 4 mils). Some microvias were filled, and others were nonfilled. These, as well as 200-μm (8-mil) THViPs, were first characterized visually and by x-ray before environmental testing.
- Visual inspection by optical microscopy was more effective in determining the condition of the microvias than x-ray radiography. X-ray radiography clearly identified filled vias, but it was of limited value for detecting other conditions.
- Microvia thermal cycling characterization revealed failure for 50-μm (2-mil) microvias after 100 cycles in the range of

−65/150°C. No failures were observed for larger vias.

- TMA characterization of cycled PCBs revealed that the T_g of the test boards was about 150°C with delamination starting at 260°C. TMA was also used to thermal cycle specimens between −100 and 245°C. The latter temperature is representative of a lower reflow temperature for a Pb-free assembly. After three cycles, no delamination was observed. The samples that were exposed to 260°C; however, did exhibit delamination.
- Microvia fatigue life was predicted to be 2607 cycles using the Cu PTH semiempirical relationship (IPC-TR-579). This agreed with the test observation that microvias showed no failure until 1000 cycles (−55 to 125°C).
- Single and stacked microvias showed a greater tendency for corner cracks, particularly with copper-filled stacked microvias. Staggered microvias were two orders of magnitude more robust than the stacked versions.

61.2 SUMMARY

Reliability of electronic systems is a complex subject. This chapter has touched on only one aspect of the problem: understanding the primary failure mechanisms of printed circuit boards. This approach provides the basis for analyzing the impact of design, materials choices, and manufacturing processes on printed circuit reliability, specifically plated-through-hole and microvia interconnections in tin-lead and Pb-free soldering environment. It also provides the foundation for developing accelerated testing schemes to determine reliability of PTH and microvia. It is hoped that the fundamental approach will enable the reader to apply this methodology to new problems not yet addressed in mainstream literature.

61.3 LIST OF ACRONYMS

ALIVH	Any-layer interstitial via hole
AtA	Air to air
ATC	Acceleration thermal cycle
B_{10}	Bearing at 10 percent, cycles-to-failure at 10 percent
B^2it	Buried bump interconnection technology
BGA	Ball grid array
BT	Bismaleimide triazing
CAF	Conductive anodic filament
CBGA	Ceramic ball grid array
CCGA	Ceramic column grid array
CGA	Column grid array
CIC	Copper invar copper
CMC	Copper molybdenum copper
CSP	Chip scale (size) package
CTE	Coefficient of thermal expansion
CTF	Cycles to failure
Cu	Copper
DfA	Design for assembly
DfM	Design for manufacturability
DfR	Design for reliability
DfT	Design for test
DMA	Dynamic mechanical analysis
DPA	Destructive failure analysis

EMI	Electromagnetic interference
ENIG	Electroless nickel immersion gold
ESD	Electro static discharge
FCDCA	Flip-chip direct chip attach
FCBGA	Flip chip ball grid array
FEA	Finite element analysis
FEM	Finite element analysis
FPBGA	Fine pitch BGA, a.k.a. chip scale package (CSP)
HASL	Hot-air solder leveling
HATS	Highly accelerated thermal shock
HDI	High-density interconnect
I/O	Input/output
IAg	Immersion silver
ILS	Innerlayer separation
IPC	Association connecting electronics industries
IR	Infrared
IST	Interconnect stress test
LASER	Light amplification by stimulated emission of radiation
LGA	Land grid array
LLTS	Liquid-liquid thermal shock
LPI	Liquid photoimageable
MLF	Micro lead frame
MTBF	Mean time between failures
Nd:YAG	Neodymium-doped:yttrium-aluminum-garnet

Nd:YLF	Neodymium-doped:yttrium-lithium-fluorine
Ni	Nickel
NViP	Non-via-in-pad
OSP	Organic solder preservative
PBGA	Plastic ball grid array
PCA	Printed circuit assembly
PCB	Printed circuit board
$PCQR^2$	Process capability, quality, and relative reliability
PGA	Pin grid array
PTH	Plated-through hole
PTHV	Plated-through hole via
PTHViP	Plated-through hole via-in-pad
PTV	Plated through via
PWA	Printed wiring assembly
PWB	Printed wiring board
QFN	Quad flat no-lead
RCC	Resin-coated copper
RFI	Radio frequency interference
RFPC	Rigid flex printed circuit
RH	Relative humidity
RMA	Rosin mildly active
RT	Room temperature
SBU	Sequential buildup
SEM	Scanning electron microscopy
SIR	Surface insulation resistance
SMT	Surface-mount technology

STII	Soldering temperature impact index
TCE	Also CTE, thermal coefficient of expansion
Td	Decomposition temperature
T_g	Glass transition temperature
TH	Through hole
THViP	See PTHViP
TMA	Thermal mechanical analysis
TSM	Thermal shock method
TSR	Total strain range
UV	Ultraviolet
ViP	Via-in-pad
WLP	Wafer level package

61.4 ACKNOWLEDGMENTS

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also goes to Judith Glazer at Hewlett-Packard Company for her authorship of this chapter in the previous edition of *Printed Circuits Handbook*.

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CHAPTER 62

COMPONENT-TO-PWB RELIABILITY: THE IMPACT OF DESIGN VARIABLES AND LEAD FREE

Mudasir Ahmad
Cisco Systems, San Jose, California

Mark Brillhart
Palo Alto, California

62.1 INTRODUCTION

The mandated conversion to lead-free assemblies has led to the convergence of several critical issues in the microelectronics industry. The conversion has further compounded several other factors that have been pushing the envelope in Component to Printed Wiring Board (PWB) reliability, including

- Radical increases in package-to-board input/output (I/O)

- Rapid reduction in interconnect pitch
- Overall rise in surface-mount component density
- Higher speeds and correspondingly higher heat dissipation

All of these factors pose tremendous challenges with respect to reliability, and they cause complex design trade-offs that must be considered while maintaining product reliability at required levels. Time to market and aggressive product life cycle pressures also require PWB designers to consider the impact that alternate designs and material sets may have on reliability, in a rapid fashion.

The PWB designer is faced with myriad packaged device types, field use environments, connectors, PWB materials, cost considerations, and real estate restrictions, which all must be optimized without degrading system reliability. Designers need tools to assess experimental reliability data, transform laboratory results into actual field loading conditions, and rapidly assess the reliability of different PWB layouts, material sets, and package types. Engineers must also have the capability for addressing complex loading conditions such as mini- and power-cycles and the knowledge of how they impact interconnect performance.

This chapter focuses on the design variables that impact the reliability of PWB-to-package interconnect (second- and third-level interconnect) of grid array devices and the impact of lead-free conversion on these design variables.

Some of the critical variables discussed in depth include

- Double-sided construction
- PWB stiffness effect
- Multiple packages in a small area
- Package and PWB warpage; assembly and reliability challenges
- Solder joint geometry; assembly and reliability challenges

- Package and PWB pad size
- Heatsink design and attachment
- Package and PWB surface finish; Black Pad, Brittle Failure, and Kirkendall voiding
- PWB electrical test architecture
- Carrier chassis design
- Package design parameters such as overall size, silicon technology, ball array, ball size/pitch, heat spreader/stiffener, material selection, die/package aspect ratio, substrate material, low-k dielectrics, and so on

The chapter is broken up into the following sections. Section 62.2, “Packaging Challenges,” outlines several of the performance challenges faced by next generation packages, and the key technical drivers behind these challenges.

Section 62.3, “Variables That Impact Reliability,” contains a discussion of the common design variables that could impact the reliability of a product; ranging from PWB design rules to package design parameters. The failure modes relating to the choice of different package design parameters are outlined, along with recommendations on ways to mitigate different manufacturing and test-related failure mechanisms.

62.2 PACKAGING CHALLENGES

The reliability of many types of leadframe components (see Figs. 62.1 and 62.2) has been assessed in great detail.[1] Figure 62.3 shows the typical definitions of interconnect levels in assemblies. While leadframe devices are by no means infinitely reliable at the first- and second-level interconnects, they have historically posed a lesser risk than grid-array packaged components, such as ceramic ball grid arrays (CBGAs), plastic ball grid arrays (PBGAs), ceramic

solder column carriers (CSCCs), flip-chip ball grid arrays (FCBGAs), and chip scale packages (CSPs). This is because the compliant leadframe in leadframe packages can absorb the differential strain induced in the solder joints, due to the mismatch in thermal expansivity between the silicon chip and the PWB. Ball grid array packages, on the other hand, rely entirely on the discrete solder balls absorbing the differential strain. Depending on the package construction, the solder joints at critical high strain locations could fail early, resulting in lower long-term reliability of the assembly. Figure 62.4 shows various grid array packaged devices.

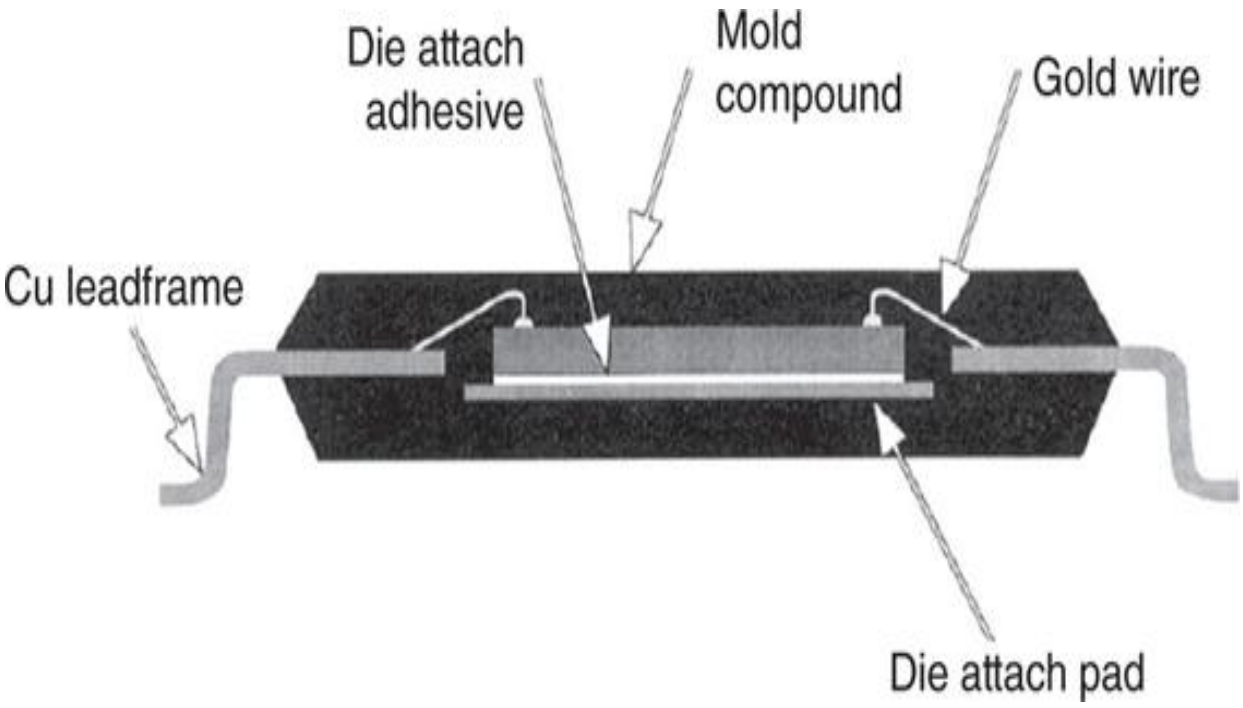


FIGURE 62.1 Diagram of a quad flat pack. Note the copper (Cu) leads that are attached by gold wire bonds to the die. This is the primary (or first-level interconnect) between the die and the package. The second-level interconnect will be created when the Cu leadframe is soldered to a motherboard via some type of surface-mount attach process. (*Courtesy of Amkor Technology, Inc*.)

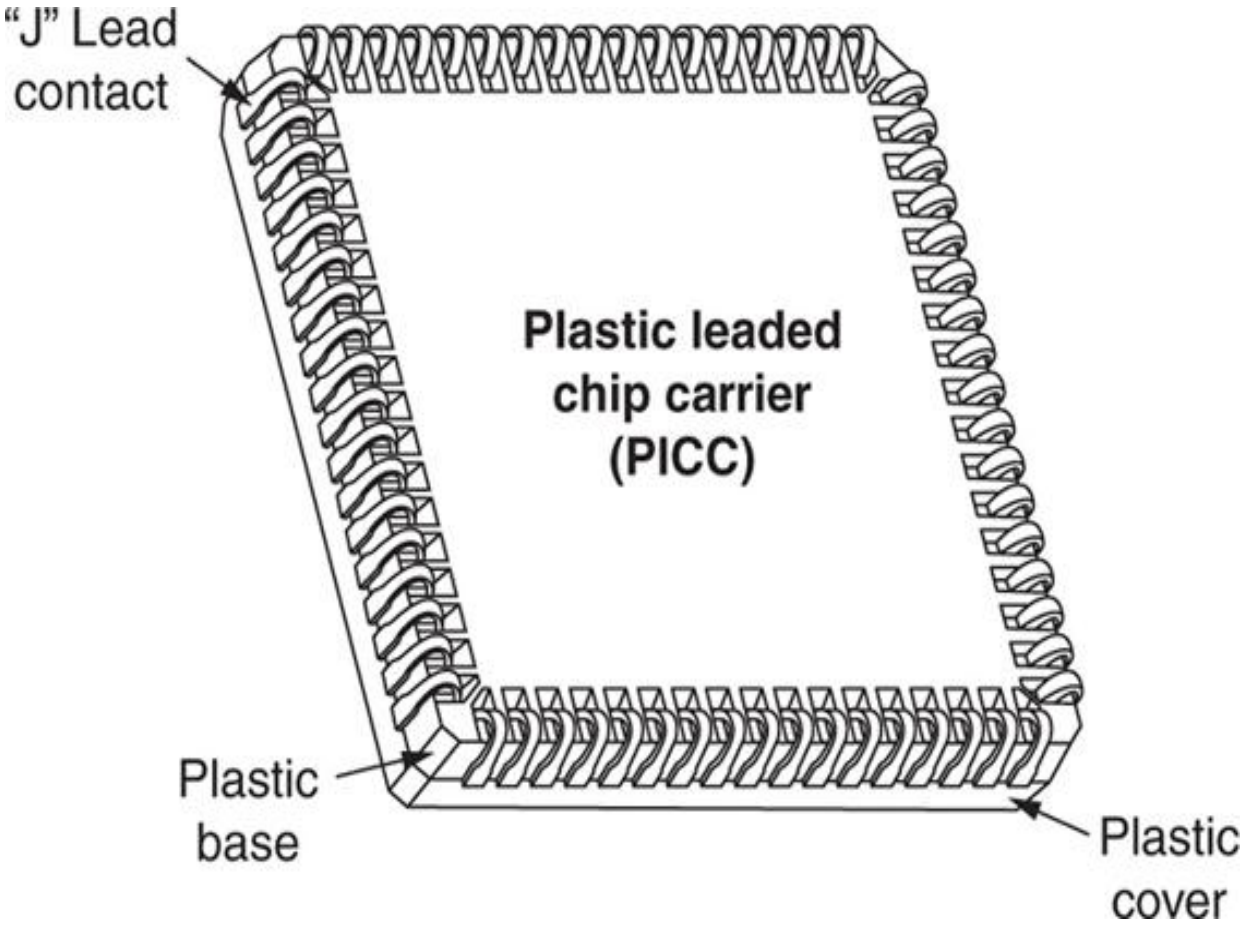


FIGURE 62.2 J-leaded device oriented bottom side up. (*Reprinted with permission from J. Lau, Ball Grid Array Technology, McGraw-Hill, New York, 1995, p. 20.*)

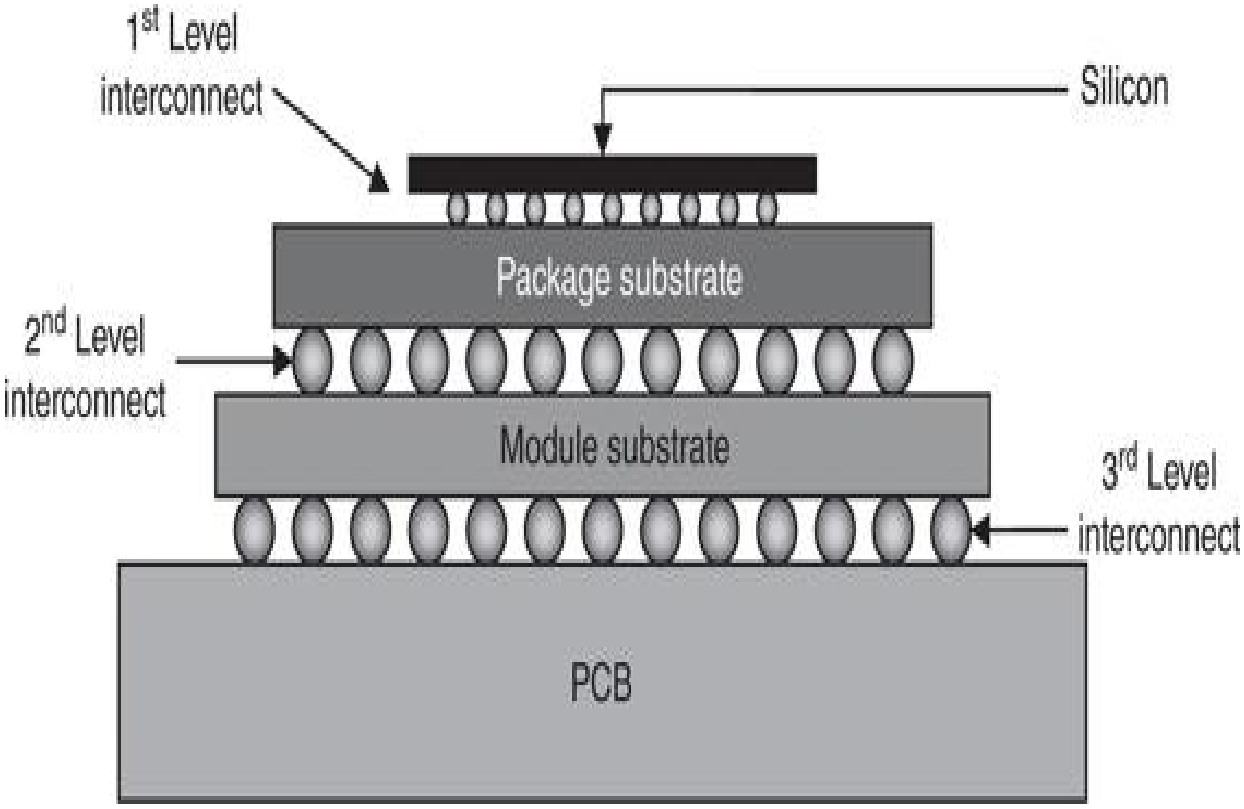


FIGURE 62.3 First-, second-, and third-level interconnects defined, employing a flip-chip assembly as an example. The first-level interconnect is the primary connection between the silicon die and the package substrate. In this example it is created by the solder bumps between the die and the package. The second-level interconnect in this example is the “next” level of connection between the package substrate and the module substrate. The third-level interconnect in this example is created when the solder balls on the bottom side of the module substrate are attached via SMT to the PWB.

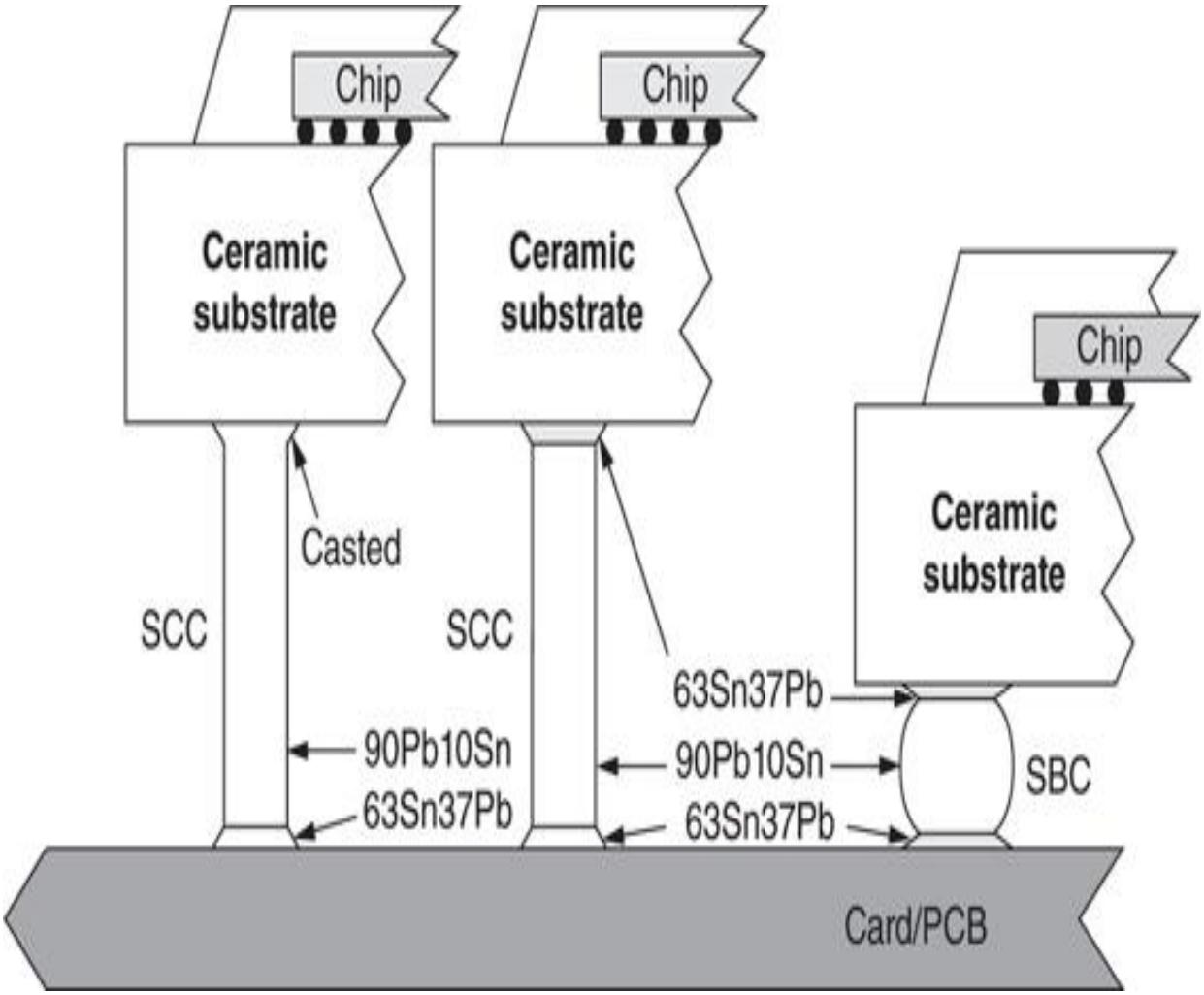


FIGURE 62.4 Cross-section of a ceramic solder column carrier and ceramic ball grid array (CBGA). Solder column carriers (SCC) and a solder ball carrier (SBC) are shown. The SBC is often referred to as a CBGA package due to the fact that it is a ceramic package substrate that employs solder balls to create a second-level interconnect between the package substrate and the PWB. The solder column carrier employs a column of high-lead solder (which is either casted onto the ceramic package substrate or attached by a layer of eutectic 63Sn/37Pb solder paste) to create a second-level interconnect between the ceramic package substrate and the PWB. A lead-free version of the SCC, made of copper columns is also being developed.[2] Typical ceramic ball grid array packages cannot achieve required reliability when body sizes exceed 32 mm per side. Ceramic packages having larger body sizes either employ SCC-type technology or connectors to create a second-level interconnect. (*Reprinted with permission from J. Lau, Ball Grid Array Technology, McGraw-Hill, New York, 1995, p. 27*.)

To meet increasing I/O density requirements, many of these types of packages are either increasing in body size,

decreasing in pitch, or both, to a point where the standard reliability envelope is being pushed to extreme levels. Additionally, most grid array packaged devices are high in cost (in many instances the grid array packaged devices are the most costly component on a printed circuit assembly) and thus cannot be deployed in a redundant design. Lack of redundancy creates critical path single points of failure (SPOFs). Failure of one of these devices can lead to catastrophic system-level failures. The proliferation of high-I/O, small-pitch grid array packaged devices throughout the electronics industry impacts almost all PWB engineers because any design has a high probability of containing one or more of these types of components.

Moreover, at higher speeds, there is an ever increasing need for reduction in signal delay between processors and the memories they communicate with. These processors could be microprocessors, network processors, programmable logic devices (PLDs), and application-specific integrated circuits (ASICs). This has given rise to the prominence of System-in-Package (SiP) modules, which significantly reduce the delay between on-PWB memory and ASICs (Fig. 62.5). SiP modules can have more than eight memories communicating with a single ASIC. The ASIC package is typically a flip chip, whereas the memories could be CSPs, stacked packages or PBGAs.

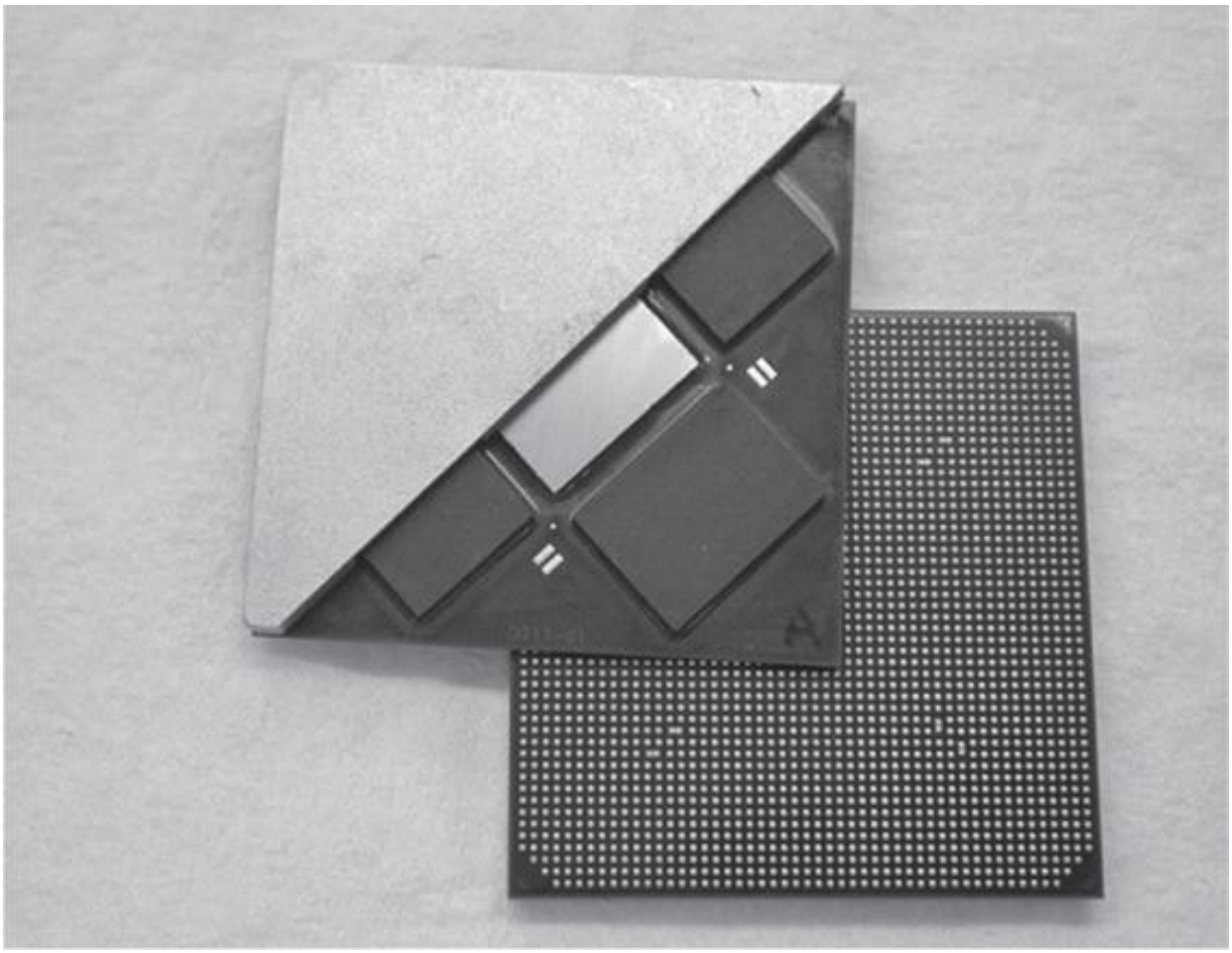


FIGURE 62.5 System-in-Package (SiP) module. SiP modules help reduce signal delay between a processor and the memory devices it communicates with. This SiP has one processor in the middle, surrounded by four discrete memory packages, all on one module. The module is soldered to the PWB via the solder balls on the back side of the module substrate.

Stacked die and stacked package memories have also become more prevalent in applications where space is a constraint (Fig. 62.6). Stacking helps compact more memory within the same foot print and in applications where height is not a critical constraint, they help conserve valuable PWB real estate while at the same time providing greater integration and performance. But stacking technology raises its own unique set of reliability challenges. These challenges include heat dissipation from the multiple dies, reworkability and the reliability of the interconnects between the individual stacked dies or stacked packages.

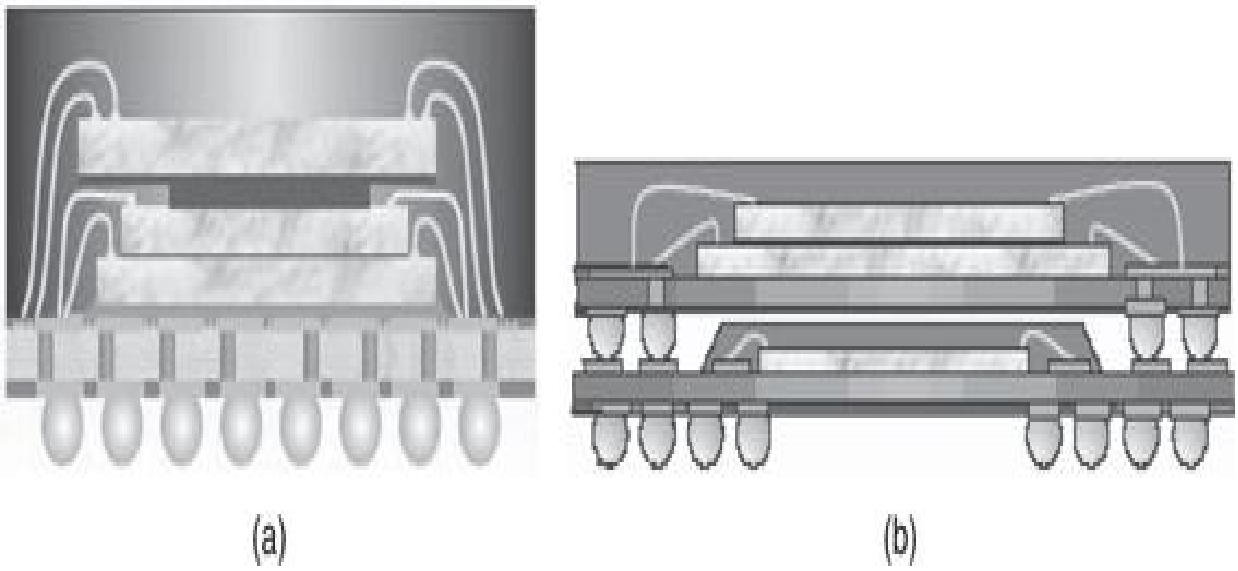


FIGURE 62.6 (*a*) Stacked-die package. Several dies are stacked within a single package and wirebonded to a single substrate. (*b*) Stacked package. Several wirebonded packages are stacked on top of each other with solder balls. (*Courtesy of Amkor Technology, Inc*.)

62.3 VARIABLES THAT IMPACT RELIABILITY

Electronic packages are composed of complex materials that are assembled via intricate processes and then subjected to a wide range of service environments. It is crucial to note that both the die-packaging processes and surface-mount technologies can impart stresses and create residual stresses in the final packaged assembly that impacts its interconnect reliability. Assessing the reliability of package devices requires that all variables that can hinder or enhance reliability be considered.

62.3.1 Actual Product Environment

The actual product environment is what drives the reliability of the assembly. Printed circuit assemblies are deployed in a

wide range of environments. Packages can be subjected to extreme temperatures and humidity. Automotive applications, for example, can see temperature ranges from −55°C to well over 95°C[3] along with up to 100 percent humidity. The rate at which temperature and humidity changes occur can be quite severe under the hood, causing components to transition from extreme cold to heat in a matter of minutes. This creates a very difficult environment to model, as the rate of occurrence of thermal and humidity cycles must be thoroughly understood. Severe shock and vibration can also be imparted to assemblies in this type of service environment, which adds to the complexity of reliability assessment. Great care must be taken when assessing these types of aggressive environments and their impact on packaging reliability. A thorough experimental analysis that employs thermocouples (to assess temperature conditions) and accelerometers (to assess shock and vibration loading conditions) should be employed to determine the actual end-use environmental conditions. These stressful environments are the primary driver for automotive applications employing extreme protection measures such as full encapsulation/potting for electronic devices placed under the hood.

Computer room environments represent the other extreme, with temperatures and humidity controlled to very tight tolerances. While servers, switches, hubs, routers, and other devices are housed in a controlled environment, their extremely large packages, coupled with power and mini cycles (discussed in the next chapter), create a set of loading conditions that are different from those found in automotive applications, but that are equally challenging. Worst-case loading conditions for a variety of end-use environments can be found in Table 62.1. Note the broad variation in temperature extremes, frequency of thermal cycles, and expected service life.

TABLE 62.1 Examples of Worst-Case Environments for Different Use Categories[3]

Use Category	T_{min}, °C	T_{max}, °C	t_D, h	Cycles per Year	Typical Years of Service	Approximated Acceptable Failure Risk, %
Consumer	0	+60	35	12	1–3	1
Computers	+15	+60	2	1460	5	0.1
Telecom	−40	+85	12	365	7–20	0.01
Commercial aircraft	−55	+95	12	365	20	0.001
Industrial and automotive passenger compartment	−55	+95	12	20–185	10	0.1
Military ground and ship	−55	+95	12	100–265	10	0.1
Space	−55	+95	1–12	365–8760	5–30	0.001
Military avionics	−55	+95	1–2	365	10	0.01
Automotive under hood	−55	+125	1–2	40–1000	5	0.1

T_{min}, minimum temperature; T_{max}, maximum temperature; t_D, dwell time at the operating temperature.

Prior to initiating any reliability assessment, it is crucial to understand the thermal, humidity, and mechanical loading conditions that a packaged device will be exposed to throughout its expected life time. Temperature maximums and minimums as well as the frequencies and rates at which the component cycles between extremes must be thoroughly understood. Complex thermal cycles (such as an outdoor product experiencing daily temperature changes coupled with a more local effect such as under-the-hood heating and cooling due to engine usage) must also be considered.

Humidity and vibration loading conditions must also be evaluated as part of an overall package qualification process.

End-use conditions can be estimated by attaching thermocouples, humidity, and shock/vibration sensors in the final product because it is used in field operating conditions. This data needs to be analyzed over time and different expected field conditions to get useful estimates of the end-use environment as illustrated in Table 62.1.

Once this data is generated, it can be used in typical acceleration factor models relating accelerated stress tests to field data. For example, if it is determined that it takes *x* hours or cycles for an assembled package to fail in a laboratory test, the acceleration factor model can be used to extrapolate expected life of the device in typical field operating conditions. Details on acceleration factor models and sample calculations are provided in the next chapter.

Although environmental impact has a large effect on interconnect reliability, there are some basic design variables that can have a positive or negative impact on solder joint reliability. These critical design variables and their impact on reliability are discussed in the following sections.

62.3.2 Double-Sided (Mirrored BGA)

The high-density revolution has forced PWB designers to place increasingly complex surface-mount devices in smaller and smaller spaces. This PWB density increase (where density refers to the number of components per unit area of PWB) may force designers to consider mirror BGA placement (see Figs. 62.7 and 62.8) or to place multiple devices on one side of a PWB.

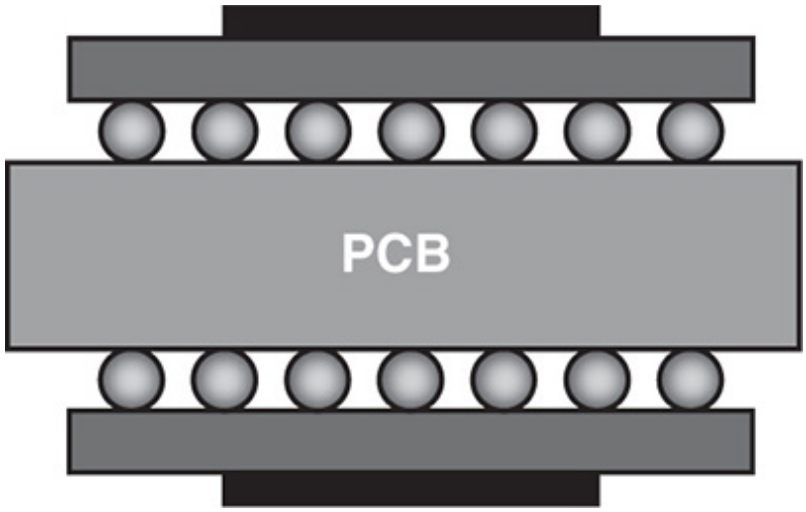


FIGURE 62.7 Double-sided BGA in mirror configuration. Note that the PCA is an exact mirror about the center line of the PWB. In some instances the top- and bottom-side packages share common vias.

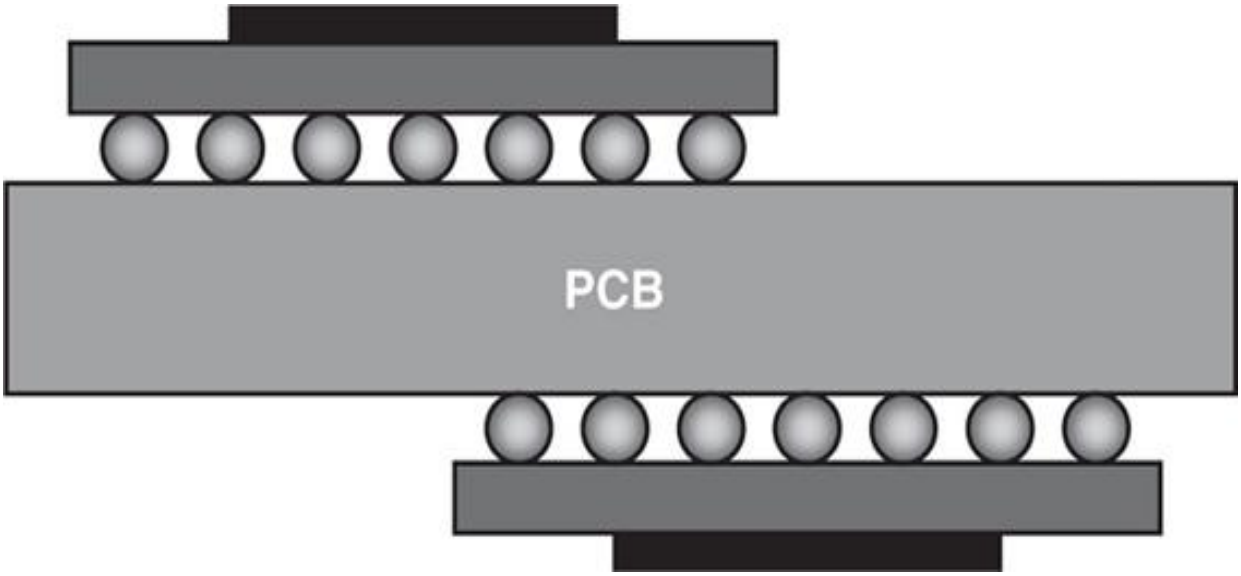


FIGURE 62.8 Double-sided BGA in quasi-mirror configuration. Note that although the packages are not right over each other, there is some overlap when looking from the top down or from the bottom up.

The beginning of the density revolution occurred when designers began implementing double-sided technologies to allow for the placement of surface-mount components on both sides of a PWB. The continued push toward device density has resulted in placement of BGA components in

mirror and quasi-mirror configurations, shown in Figs. 62.7 and 62.8.

While the double-sided configuration certainly reduces signal delay, the primary disadvantage is a significant reduction in the thermomechanical reliability of the solder joint interconnects between the packages and PWB. Placing BGA packages in mirror or quasi-mirror configurations tends to rigidize the PWB assembly such that it does not bend as much during temperature cycling. The increased stiffness of the PWB due to double-sided mounting means the solder joints have to absorb more differential strain between the packages and PWB, resulting in as much as a 50 percent reduction in solder joint fatigue life (Figs. 62.9 and 62.10).[4] In terms of solder joint strain, the effect is the same as having a thicker or stiffer PWB. The primary failure mode is cracking in the solder joints near the package/joint interface.

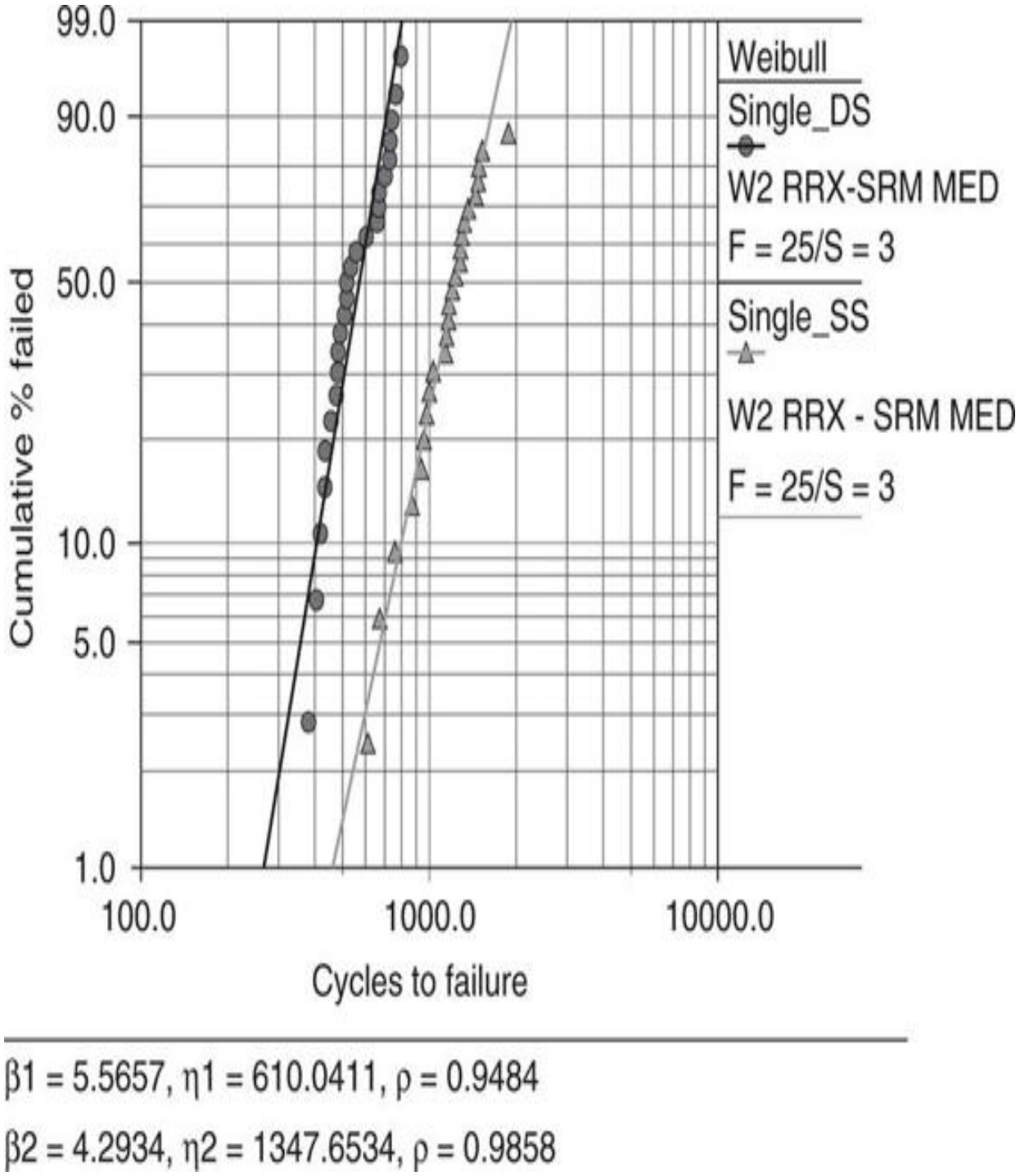


FIGURE 62.9 Weibull plot of single and double-sided mounting of single lead-free extremely thin chip scale package (PS-etCSP®). (*Reprinted with permission from Amkor Technology, Inc./© [2004] IEEE ECTC*.[4])

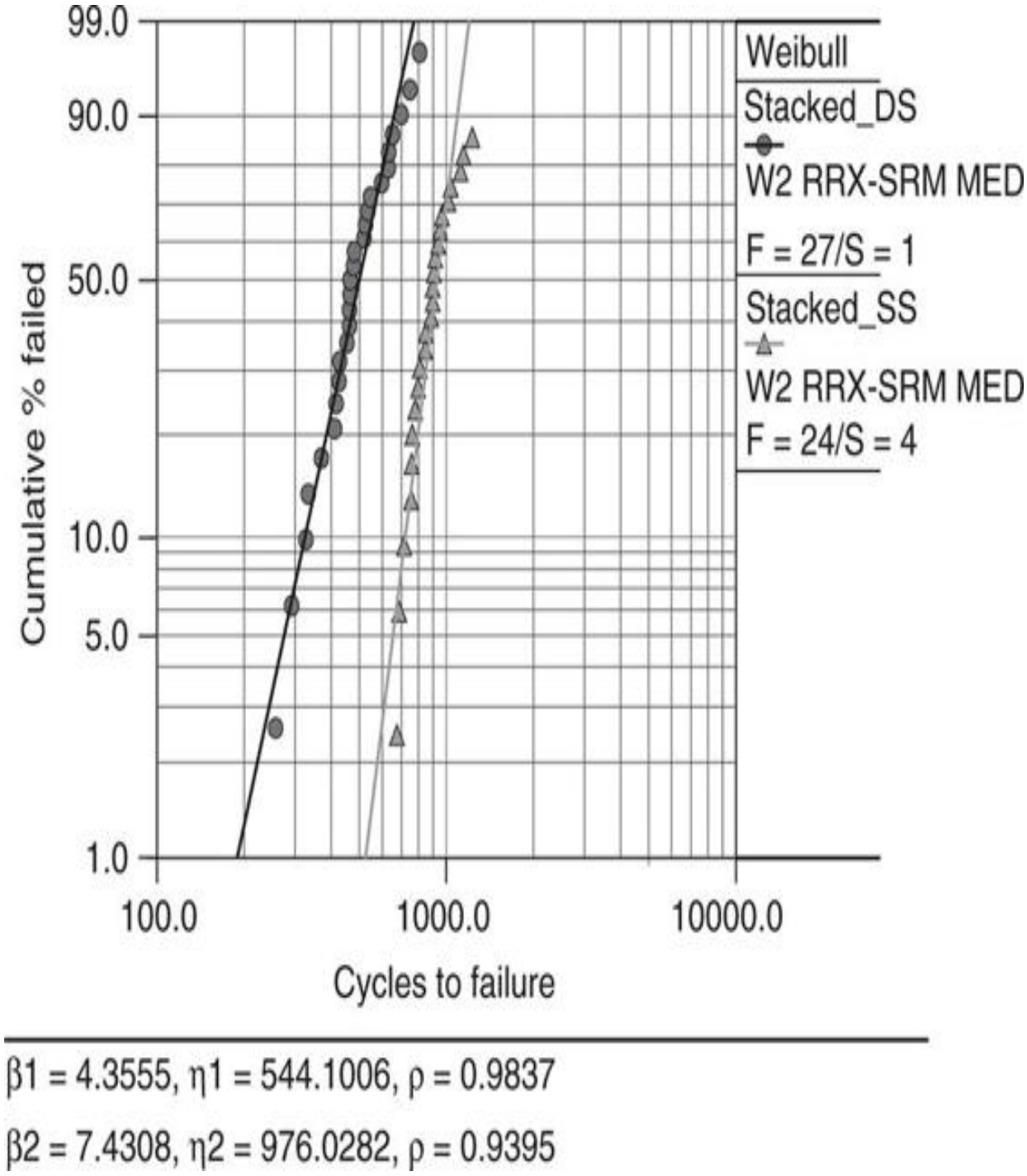


FIGURE 62.10 Weibull plot of single and double-sided mounting of stacked lead-free extremely thin chip scale package (PS-etCSP®). (*Reprinted with permission from Amkor Technology, Inc./© [2004] IEEE ECT.*[4])

Due to the dramatic decrease in assembly reliability when attempting mirrored configurations, these types of

configurations should be avoided whenever possible. When it is impossible to avoid a mirror configuration, a quasi-mirror configuration without common through-hole vias is recommended (see Fig. 62.8). Common through-hole vias in this configuration tend to rigidize the assembly and contribute to further reduction in solder fatigue life. A standard rule of 50 percent reduction in fatigue life when employing a mirror configuration may be taken as a first-pass approximation. Thermal cycle testing should be performed to ensure that the reliability degradation will still keep service life at an acceptable level when either a mirror or quasi-mirror configuration is considered.

62.3.2.1 Effect of Lead-Free Conversion. The reduction in lead-free package reliability when employing a mirrored double-sided configuration has been experimentally assessed.[4] Figures 62.9 and 62.10 show failure rates for single and stacked packages in single-sided and double-sided mirror positions.[4] Note the almost 50 percent reduction in fatigue performance when a single device is placed in a mirror configuration. The reduction is slightly less for the stacked packages, but the baseline reliability of the stacked package is 10 percent lower than that of the single package. The same trends have been shown with tin-lead eutectic assemblies, so it appears that the conversion to lead free would not mitigate this reduction in solder joint fatigue life due to double-sided mounting.

For details on Weibull distributions and failure life analysis, please refer to Sec. 59.2.2 in Chap. 59.

62.3.3 Board Stiffness Effect

As with the double-sided case described earlier, solder joint reliability generally decreases with PWB thickness. The thicker the PWB, the higher its stiffness, and the higher the

differential strain that the solder joints have to absorb. However, the percent reduction in solder joint fatigue life due to board thickness varies for different package constructions (e.g., CCGA, CSP, FCBGA, and PBGA).[5] The reduction is more pronounced in ceramic packages as compared to organic packages because of the higher mismatch in the coefficient of thermal expansion (CTE) between the package and PWB. Both thickness and number of layers of copper contribute to the stiffness of a PWB. As a result, the PWB thickness and layer count used to perform qualification testing should be representative of the end-use conditions in which the package would be used.

62.3.3.1 Effect of Lead-Free Conversion. The negative effect of PWB stiffness on solder joint reliability also applies to lead-free assemblies, as evidenced in Fig. 62.11. However, the amount of degradation could be different depending on the package type. Best practice recommendation is to use two different board thicknesses to perform temperature cycling qualification. This helps generate data for a specific package type over a range of board thicknesses. This recommendation is in line with the guidelines in the industry standard IPC 9701.[6]

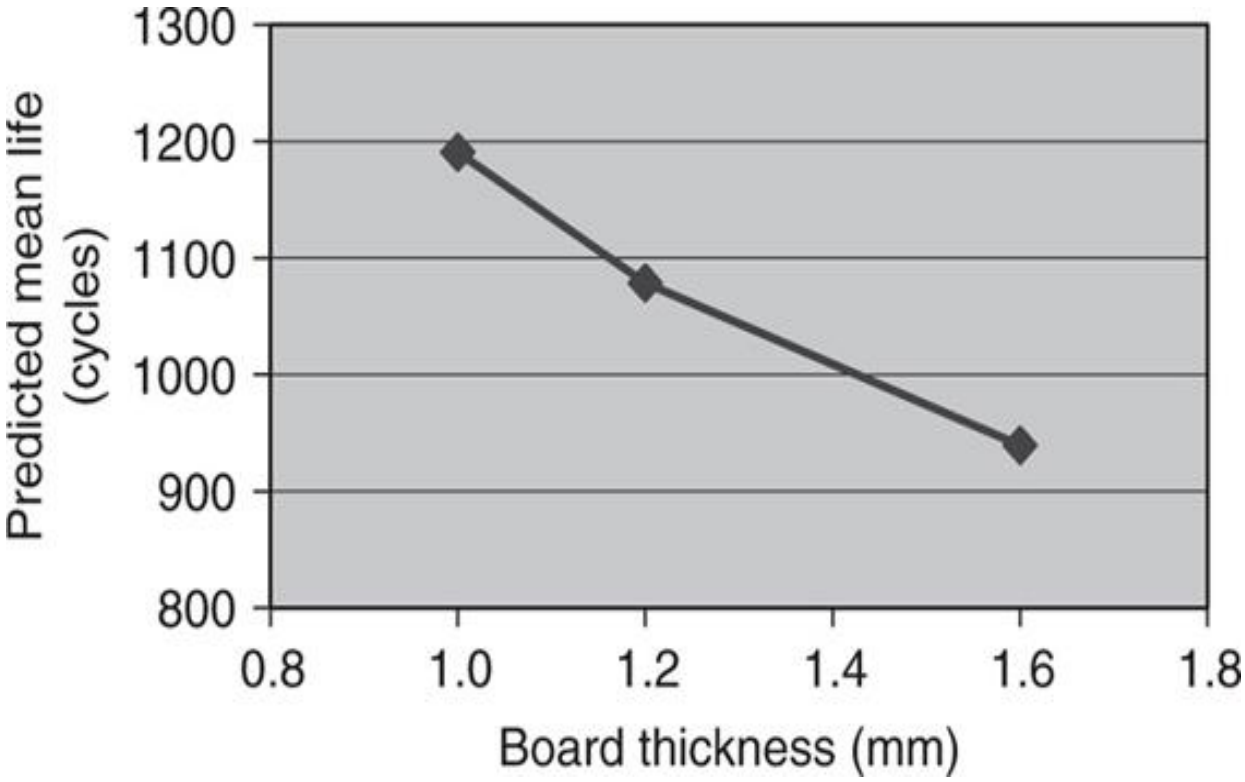


FIGURE 62.11 Effect of board thickness on solder joint reliability of stacked lead-free extremely thin CSP (PS-etCSP). (*Reprinted with permission from Amkor Technology, Inc./© [2004] IEEE ECT.*[4])

62.3.4 High Density due to Multiple Packages in a Small Area

A second source of reliability degradation due to density increase can be observed when a designer attempts to place many BGA packages in a small area on a thin PWB (see Fig. 62.12). The effective CTE of the packaged die or module tends to be much lower than that of the actual PWB. During reflow, the PWB and packages are in a stress-free state. Upon cooling, however, the packaged die contracts at a reduced rate (due to the lower effective CTE) than the underside of the PWB, causing a convex-type curvature to be imparted to the PWB. Moreover, if the thermal mass of the packages on the top side is higher than that on the bottom

side, this can lead to a skew in the temperature distribution across the assembly, which in turn exacerbates the warpage of the assembly. Thus, care should be taken to distribute the packages as uniformly as possible across the PWB on both sides, and also to balance the copper in the PWB itself.

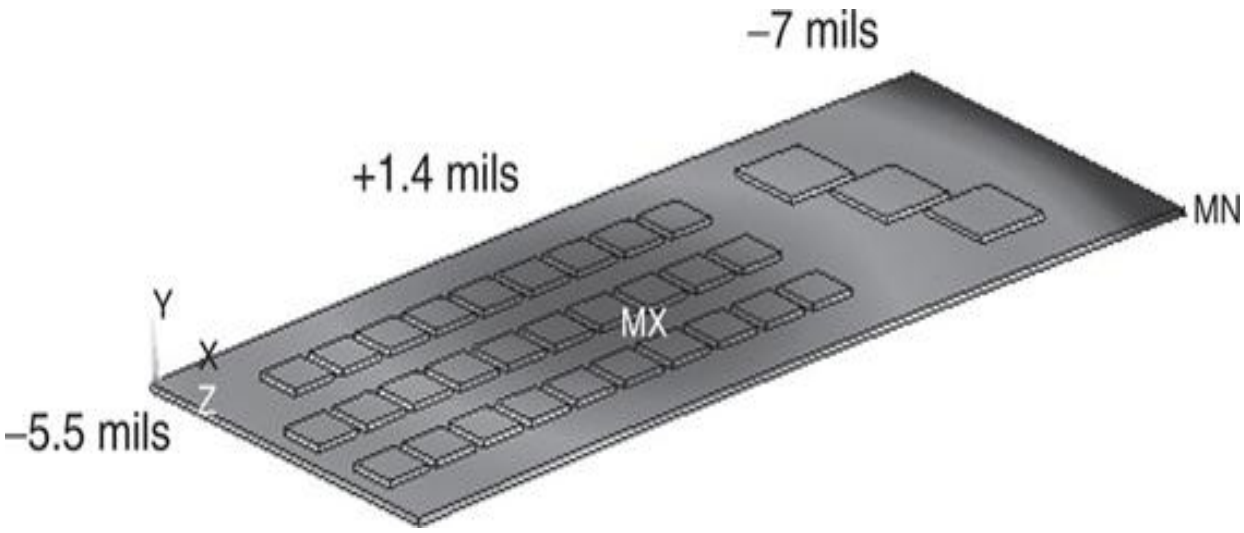


FIGURE 62.12 High-density placement of BGAs on top side of a PWB. This diagram illustrates the convex-type curvature of a PWB assembly where multiple BGA devices are all placed on one side of a board.

62.3.4.1 Effect of Lead-Free Conversion. Typical lead-free reflow temperatures (235 to 260°C) are higher than tin-lead reflow temperatures (220°C). As a result, the residual stresses built into the assembly after reflow could be higher in lead-free assemblies. These higher residual stresses are also a function of the cooling rate. Thus, it is important to not only control the heating side of the reflow profile, but the cooling side as well. The use of multiple zones for cooling is preferable, as it ensures better control. Moreover, forced convection ovens would be preferable over IR ovens for better control. Due to significant variations in the thermal mass of typical boards, it is difficult to provide universally applicable recommendations on reflow profiles.

62.3.5 Warpage Issues

The impact of warpage on a PWB assembly is multifaceted. First, warpage must typically be overcome when a PWB is placed in a card cage. Card cage placement of warped boards results in a rapid change in the loading of the solder joints that may lead to micro-crack formation or, in severe instances, solder joint fracture. Severe PWB warpage may create a card that physically cannot be placed in a card cage, resulting in a non-manufacturable product. Warped boards should be clamped in a controlled fashion to reduce the stress imparted to solder joints upon installation in a card cage.

62.3.5.1 Effect of Lead-Free Conversion. With the conversion to lead free, it is imperative to ensure that the base material used in the PWB is compatible with the higher reflow temperatures. While more industry wide research is needed, the use of materials such as Dicyandiamide (DICY) cured FR-4 appears to be limited to applications with less than 240°C peak reflow temperature, whereas Phenolic cured PWBs are preferred for applications higher than 240°C. This is because of the better resistance to delamination observed for the phenolics after multiple reflows.[7,8] The thermal mass of the components and the amount of copper in large panel boards could make it difficult to maintain temperatures below 240°C. Detailed temperature measurements and reflow profiling should be performed on large boards to ensure that the temperature rise across the PWB is compatible with the PWB material.

62.3.6 Die and Package Stress Issues

A second issue associated with board warpage is die and package stress. The package experiences an amount of stress as it constrains the PWB from contracting during cooling after reflow. If this stress is severe enough, the silicon may crack. Also, severe stress may create multiple types of package delamination and/or cracking. The extreme danger here is that a device could pass full first-level qualification (first-level qualification typically consists of thermal cycling, humidity and temperature exposure, extreme-temperature storage, and shock and vibration experiments performed on packaged devices not attached to a PWB) yet suffer from delamination/die cracking due to stresses imparted by a warped PWB. This is one of the primary reasons that many packaged IC suppliers and consumers require that second-level qualification test vehicles include daisy chains at the first-level interconnect. Inclusion of first-level joints or wire bonds allows for the impact of second-level attach on first-level reliability to be assessed simultaneously with second-level solder joint reliability during a second-level qualification.[9]

62.3.6.1 Effect of Lead-Free Conversion. Lead-free conversion exacerbates these potential silicon-level failures. Since the assembly is subjected to a higher temperature range than with tin-lead assemblies, there is a higher propensity for early failures due to residual stresses during cool down. In addition, there are potential concerns over the effect on low dielectric constant (k) materials in the silicon during second-level temperature cycling. This is discussed in more detail in Sec. 62.3.13.9. The effect of mold compound and underfill material selection on first-level interconnects is also discussed in more detail in Secs. 62.3.13.5 and 62.3.13.6, respectively.

62.3.7 Back-Side Component Issues

A third challenge related to warped PWBs concerns the back-side components in double-sided designs. During cool down after reflow, the top of the PWB is restrained from contraction due to the smaller effective CTE of the packaged device. This results in the bottom side of the PWB over contracting during cool down. The state of stress on the bottom solder joints due to warpage may be severe enough to fail solder joints or crack the die in bottom-side components. Additionally, the back-side components may be subject to residual stresses imparted after the second reflow (when the top-side components are attached via SMT) that may impact the long-term reliability of the devices on both sides and their second-level interconnects. As a result, it is important to characterize the thermomechanical reliability of the components that are mounted on the back side by performing temperature cycling qualification.

62.3.8 Solder Joint Geometry Issues

Another consequence of severe warpage is the shape of the post-assembly solder joints. Joints can become excessively deformed, such that the cross-section is too small to withstand fatigue. Joints can also become compressed or elongated, causing shorts or opens in some cases.

Moreover, with significant increases in body sizes of packages, there is a higher propensity for opens or bridges during reflow. For example, a 20-mm body-size package (1 mm pitch) would be easier to assemble on a relatively thin PWB, but with a 50-mm organic package, warpage is much more difficult to control, and it is a challenge to assemble it on a thick (≥125 mil, 20 + layer) PWB.

Tolerances are also difficult to control on large-panel, thick PWBs. Typical tolerances on high end PWBs are ±4 mils over the package site. Ensuring tolerances less than this is cost prohibitive. Current JEDEC guidelines[10] require ±8 mil

coplanarity across the package. However, there are no specifications on the maximum acceptable warpage of the package at or above the reflow temperature. The typical relationship between maximum diameter and warpage is shown in Figs. 62.13 and 62.13.

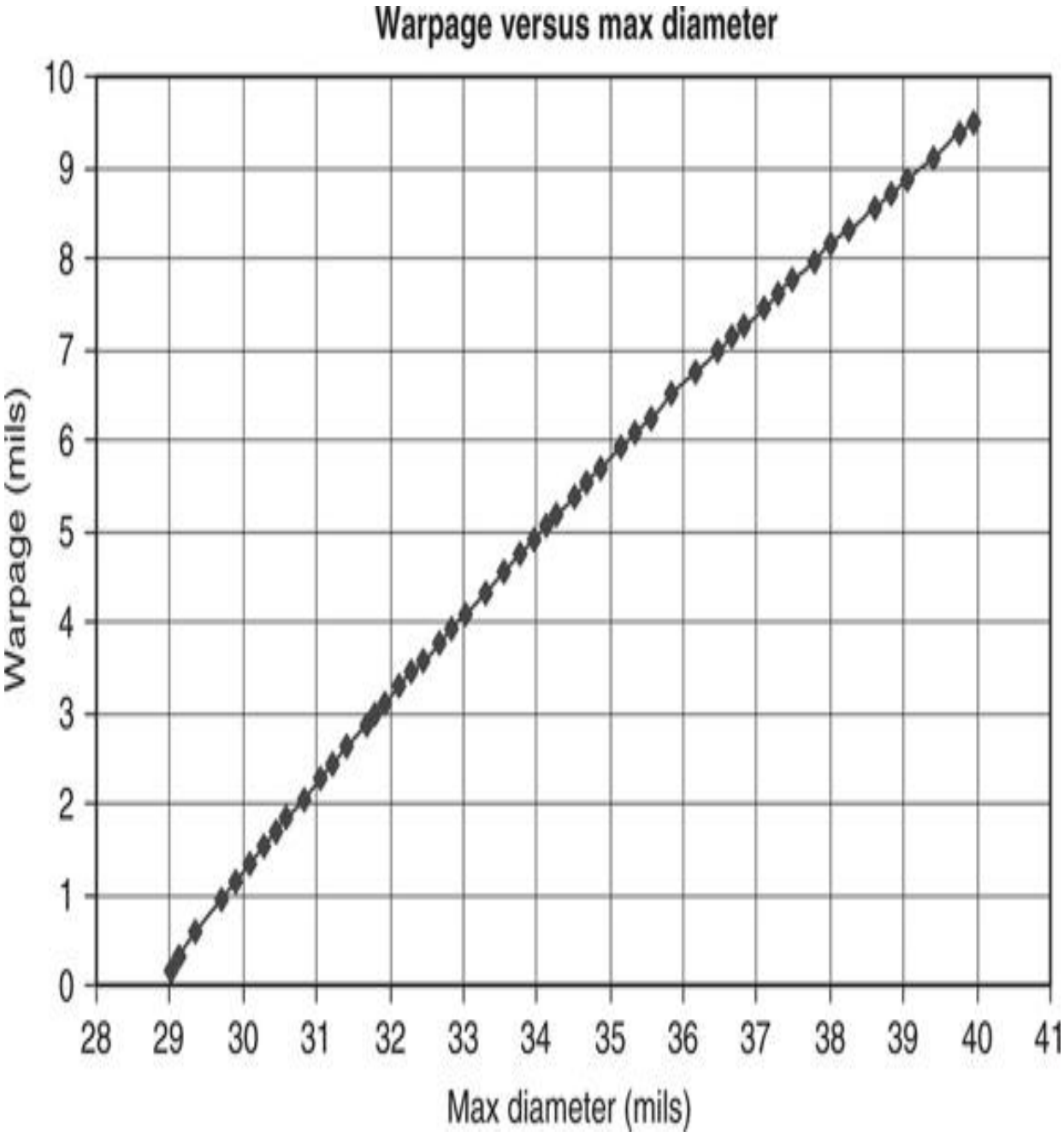


FIGURE 62.13 Warpage versus max diameter for solder joint bridging. (© *ASME, 2005*.)[11]

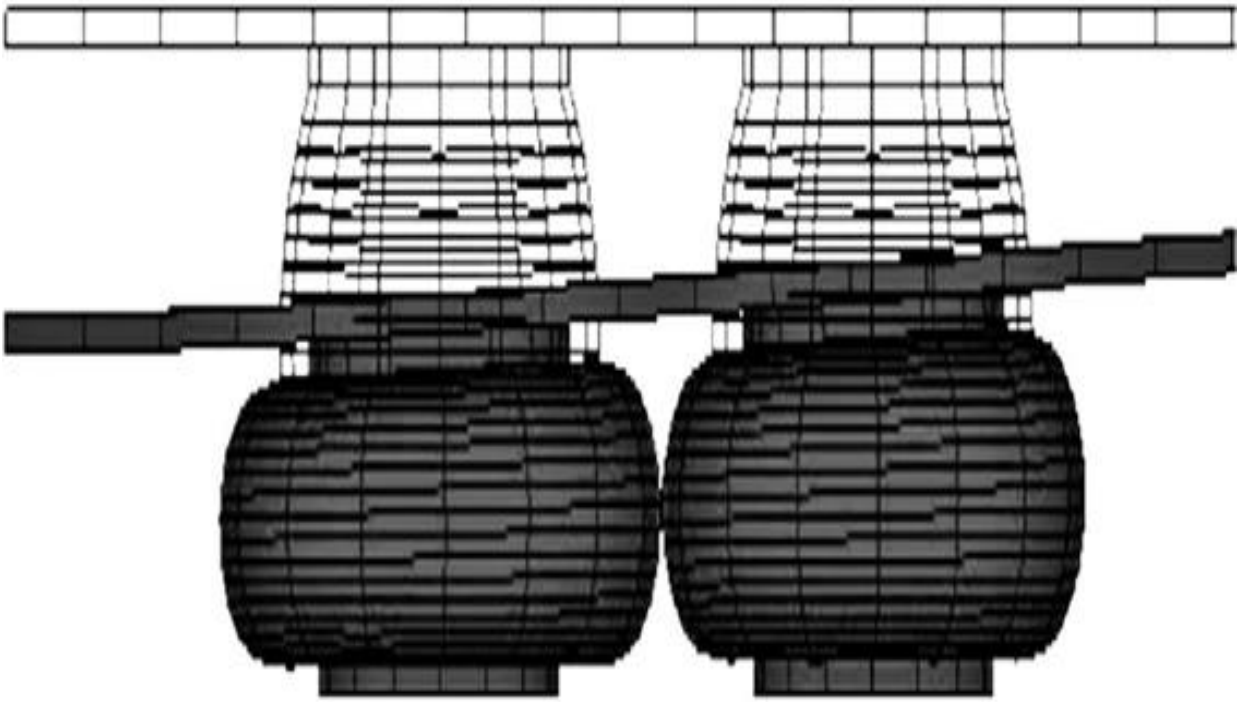


FIGURE 62.14 Bridging of solder joints—wireframe (unwarped), contour (warped). (© *ASME, 2005*.)

The joint parameters used in the analysis are

Paste volume (m^3)	4.909576e-011
Solder ball volume (m^3)	1.130972e-010
Upper pad diameter (mm)	0.60
Lower pad diameter (mm)	0.55
Viscosity of solder (Pa-sec)	2e-3
Surface tension (Nm^{-1}) (Tin-lead)	0.386

For a 1-mm pitch joint array, if the maximum diameter exceeds 40 mils (1.016 mm), bridging will occur. Based on the analysis results, if the effective warpage exceeds ~9 mils (0.23 mm) over a 7-mm distance along the package, the joints will bridge (Figs. 62.13 and 62.14). Due to

misregistration, bridging could occur at lower warpage levels. But, for the sake of clarity, the base of the solder joints has been assumed to have no warpage. Thus the predicted value (9 mils) is the *effective* warpage of the assembly. In practice, if the board has a concave warpage of 5 mils and the package has a convex warpage of 4 mils over 7 mm (above solder melting temperature), it could result in bridging.[11]

Given these values, there are a few critical points to note:

a. Simply maintaining the JEDEC recommended 8 mils coplanarity could be insufficient in some applications (e.g., large body size packages on thick PWBs).

b. It is important to characterize the *effective* warpage between the package and PWB in addition to the warpage of the free standing package alone.

c. This warpage characterization should be performed over the entire reflow temperature range, as opposed to at room temperature. Of critical value is the warpage at or above the melting temperature. The data should be recorded in accordance with the JEDEC high temperature package warpage measurement specification.[12]

d. Where possible, the characterization should be performed on PWBs that are representative of actual PWBs used in volume production.

One useful way to mitigate solder bridging is to depopulate the corner-most balls of the package. In large body-size organic packages, a significant amount of warpage occurs at package corners, so depopulating the 6 corner-most balls at each corner could help absorb about 2 mils of effective warpage (Fig. 62.15). This helps minimize the likelihood of solder bridging/opens. Many package suppliers already depopulate the four corner balls to improve long-term reliability of the solder joints.

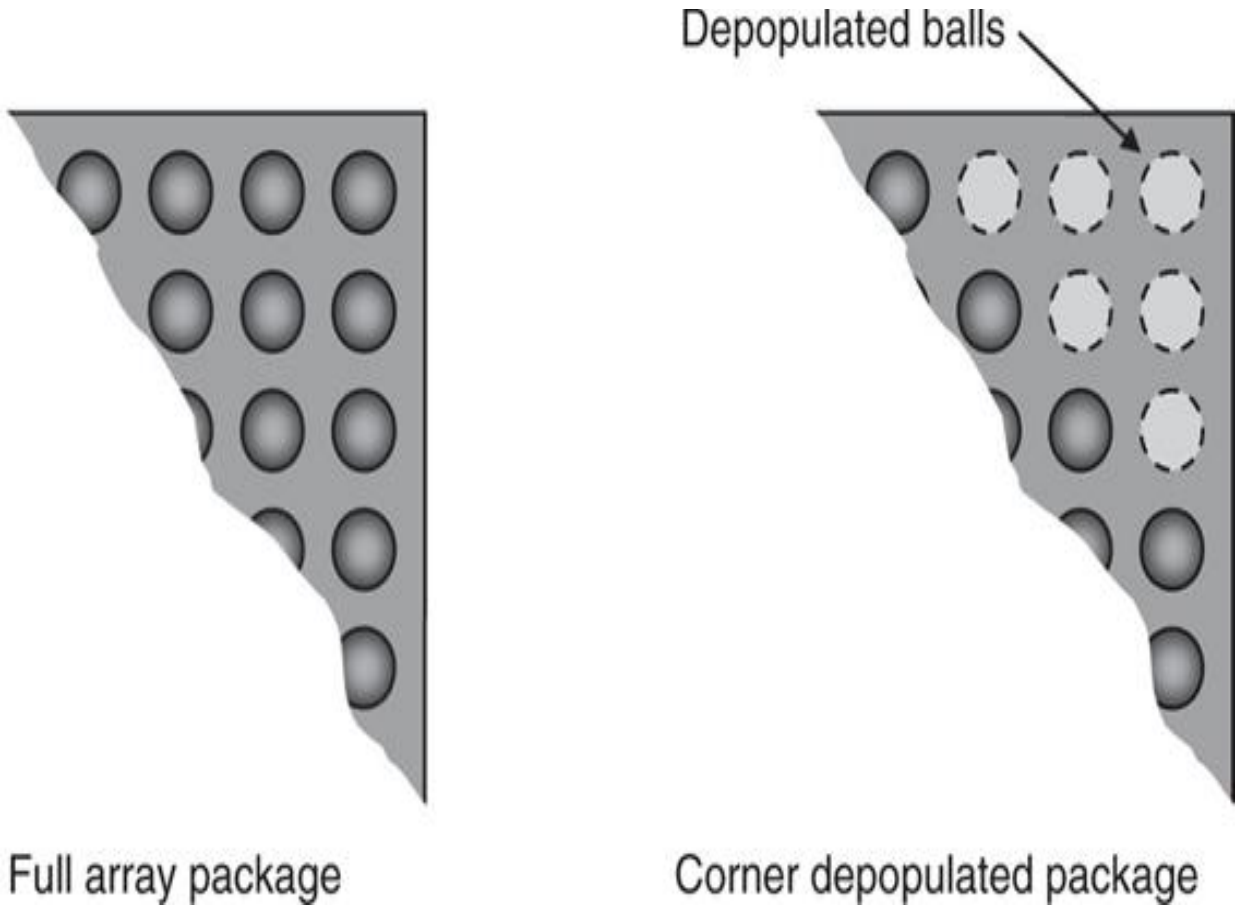


FIGURE 62.15 Depopulated corners to improve warpage-related assembly yield.

62.3.8.1 Effect of Lead-Free Conversion. It is important to note that the data presented in Figs. 62.13 and 62.14 is based on the surface tension of tin-lead solder. The surface tension[13] and contact angle of lead-free solders is higher than for tin-lead solders, but analytically, for the solder joint parameters analyzed, the warpage versus ball diameter curve is not significantly different from the data presented in Figs. 62.13 and 62.14. This is because the wetting area is presumed to be fixed in the analysis. For other solder geometries (gullwing, J-lead, QFN, and so on), the behavior of lead-free solders can be different.

62.3.9 PWB Pad Design

The size and shape of the pad used on the PWB has a significant impact on the reliability of BGA solder joints. In general, the reliability is optimal when the pad size/opening on the package side is the same size as that on the PWB side. Deviation from the same pad size could result in a reduction of up to 25 percent in solder joint fatigue life.[14] The side with the smaller pad size tends to fail earlier because the stress concentration is higher near the smaller pad. Generally, non-solder mask defined (NSMD) pads are used on the PWB for packages with solder pitches in the range 1.27 to 0.8 mm. As opposed to solder mask defined (SMD) pads, NSMD pads do not have a localized stress concentration around the solder joint, which tends to degrade the thermomechanical fatigue life of solder joints (Fig. 62.16).

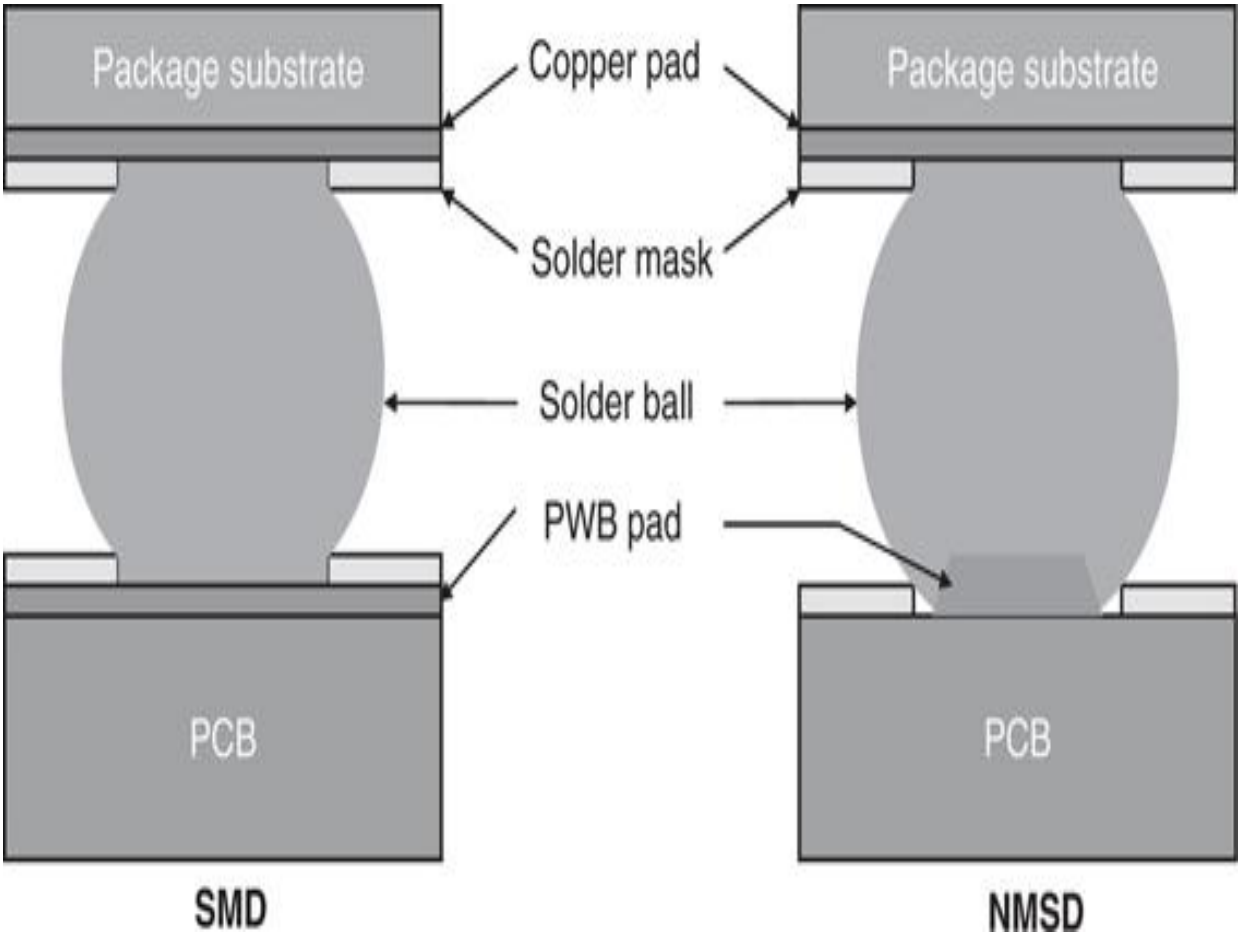


FIGURE 62.16 Solder-mask defined (SMD) and non-solder mask defined (NSMD) pad construction. For optimum reliability, the pad size on the PWB should be kept within 80 to 100 percent of the wetted pad area on the package side. This allows the stresses to be vectored equally between both ends of the solder joint, and if the PWB pad is slightly smaller, it allows a slightly higher stand-off height, which also tends to enhance solder joint reliability.

For packages with solder joint pitches less than 0.8 mm, a mix of NSMD and SMD pads is sometimes inevitable. At small pitches, it is difficult to route the traces from the pads in the typical “dog bone” fashion. Thus, to allow routability, the common, power and ground pads are “bussed” together to form one large pad. The connected pads are SMD, whereas the individual signal pads are kept NSMD.

In general, it appears that while SMD pads tend to improve the resistance of solder joints to mechanical shock loading conditions, they also tend to degrade the thermomechanical fatigue life of the joints. Therefore, when the choice of pad construction is made, the impact on both thermomechanical fatigue and shock conditions should be characterized. (Details of typical shock testing conditions are outlined in Chap. 59.)

It is important to note that the pad size specified in the fabrication drawings is not always the pad size that actually comes on all the fabricated PWBs. Actual measurements of pads specified at 12 mils NSMD could range anywhere from 9 to 15 mils. This is particularly critical for small pitch packages, because the solder volume is smaller and such variations in pad sizes could significantly alter the shape and reliability of the solder joints. A tolerance analysis such as worst case (WC) or root sum squares (RSS) should be conducted and a pad size specified such that it would not significantly exceed the pad size specified on the package side. Refer to the IPC-7351 specification for details of such tolerance analysis.[15]

Finally, it is clear that one common theme in the foregoing recommendations is that the PWB pad size should be pegged

to the package side solder wetted area. Across the industry, the challenge with this recommendation is that the package pad size/opening is not always provided by package suppliers in relevant datasheets and mechanical drawings. To address this issue, JEDEC revised the JEDEC Publication 95[10] in 2004 to include nomenclature showing the pad size and construction on the package mechanical drawings. Adoption of this JEDEC nomenclature by package suppliers would go a long way in ensuring that the PWB design used by end users does not deleteriously impact the reliability of the package.

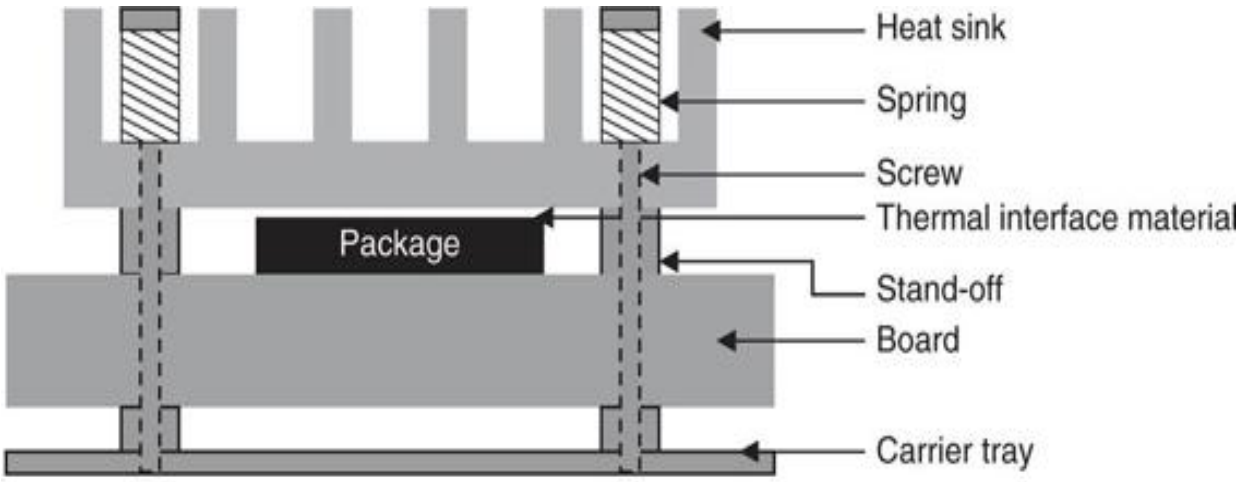
62.3.9.1 Effect of Lead-free Conversion. The impact of un-optimized pad size selection is detrimental to both tin-lead and lead-free assemblies. Fine pitch components (<0.8 mm pitch), regardless of solder metallurgy are much more prone to pad size-related failures.

62.3.10 Heatsink Design Issues

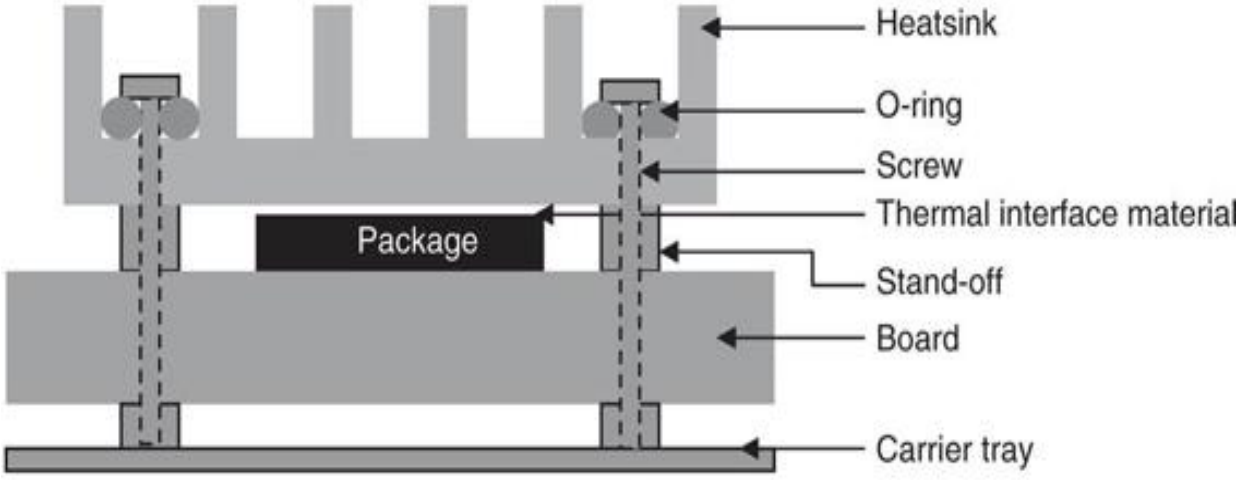
As PWB designs get more complex and more densely populated, the power dissipation from single cards can be on the order of 1000 W. A lot of heat needs to be transferred from individual cards, and from the chassis as a whole. Consequently, heatsinks are becoming larger and heavier. Heatsinks as large as 10 sq. in, weighing more than 1 lb are not unheard of. If not designed correctly, large heatsinks could transfer a significant amount of compressive load to the packages they are meant to cool. This compressive load could result in cracks in the package/ silicon, or cause the solder joints to deform and bridge.[16] On the other hand, smaller heatsinks that are anchored to the package substrate could impart additional bending moments on the substrate that could negatively impact the reliability of the package.[17]

For bolt-down heatsinks, a significant amount of the compressive load comes not from the heatsink weight but from the bolt down mechanism itself. Tolerance variations in package height, warpage, heatsink stand-offs, and so on only make the applied load worse. The attachment mechanism should be such that it can accommodate these variations in tolerance without transferring excessive load to the package.

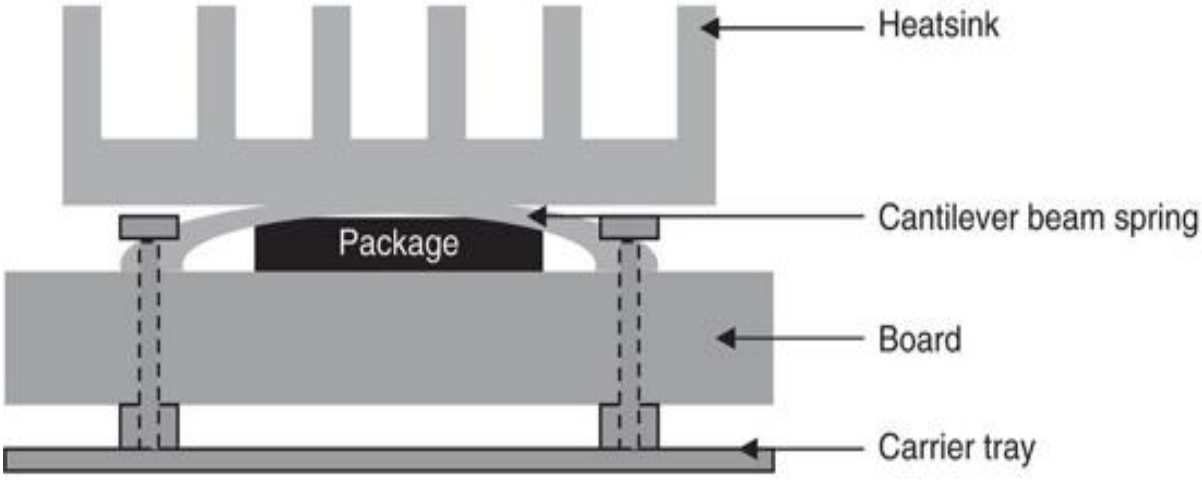
Some of the attachment methods that could help accommodate tolerance variations and minimize the amount of loading imparted on to the package are shown in Fig. 62.17. The trade-offs of using each method are summarized in Table 62.2.



Spring-loaded solution.



O-Ring solution.



Integrated cantilever spring solution.

FIGURE 62.17 Heatsink attachment methods.

TABLE 62.2 Comparison of Different Heatsink Attachment Methods

Attachment Method	Advantage	Disadvantage
Spring-loaded solution	Useful for absorbing significant tolerance variations by varying spring constants.	Relatively expensive. Bulky
O-ring solution	Less expensive. Less bulky.	Marginal control in tolerance stack-up induced pressure.
Integrated cantilever spring solution	More versatile. Could be range of expected loads.	Requires custom heatsink design. Could be more cumbersome to install.

Pressure-indicating film can be used to verify the amount of load applied on the package. The film contains tiny microcapsules of colored dye. These microcapsules rupture depending on the amount of pressure applied on the film, producing a pressure footprint. The results are not extremely precise, but can be used to estimate the amount of load applied, as a first pass approximation.

To verify the impact of heatsink loading on package solder joint reliability, temperature cycling can be performed on packages with heatsinks and compared with control samples. However, there are two caveats:

1. The heatsinks tend to cool the packages during temperature cycling, thus producing improved reliability data. The improvement may simply be because the solder joints are cycled over a lower temperature range. Thus it is important to either thermally shield the heatsink fins or calibrate the thermal cycling chamber such that the solder joints run at the same temperature range as control samples; in spite of the heatsinks.

2. Packages thermal cycled under compressive load could undergo two failure mechanisms: cyclic loading (fatigue induced opens) and static compressive loading (bridges due to solder collapse). Temperature cycling can accelerate the cyclic loading portion, but not the static loading portion. Thus, simply performing temperature cycling and comparing with control samples may not suffice. The static-loading component should also be accelerated, for instance, by dwelling at a high static temperature.

62.3.11 Surface Finish Issues

In recent years, the role of package surface finish in the robustness of BGA packages has gained more prominence. Several different surface finishes are used across the industry, and there are trade-offs with the use of each one. The surface finish used could impact intermetallics formed in the solder joints, which in turn can impact the thermomechanical and mechanical reliability of the package.

In recent years, a number of surface finishes have become more prevalent. The surface finishes with which the effect on package reliability is relatively well known, are outlined in this section.

62.3.11.1 Electroless Nickel Immersion Gold. This has been the surface finish of choice for most high-end, flip-chip BGA packages. It enables the routability of fine pitch traces in high pin count packages. Historically, Electroless Nickel Immersion Gold (ENIG) produces excellent board-level solder joint reliability.

However, there are two primary concerns with ENiG:

1. *Brittle fracture* This failure mode is seen in high strain/strain rate conditions, such as shipping, testing, and handling. A typical signature of this failure mode is a clean

separation in the intermetallic between the pad and the solder joint. This failure typically has a low defect rate in production, but the ensuing line stops, customer returns, and root-cause analyses are quite expensive. Moreover, the unpredictability of the failure and the susceptibility to mechanical handling/testing/shipping conditions makes it quite undesirable.

There are a few failure mechanism theories proposed to explain brittle fracture,[18] but no conclusive failure mechanism has been agreed upon in the industry. The predominant theory is based on the formation of Kirkendall voids during reflow, in the phosphorus-rich Ni layer and Sn-Ni intermetallic interface. Kirkendall voids are voids that form at the interface of two dissimilar materials. They form because the two materials diffuse into each other at different rates. Other factors such as the concentration of P in the Ni-P+ layer and the density of mudflat cracks in the Ni-P+ layer have also been shown to have an influence on the propensity of brittle fracture. The intermetallics formed in the joint during the assembly process are shown in Fig. 62.18.

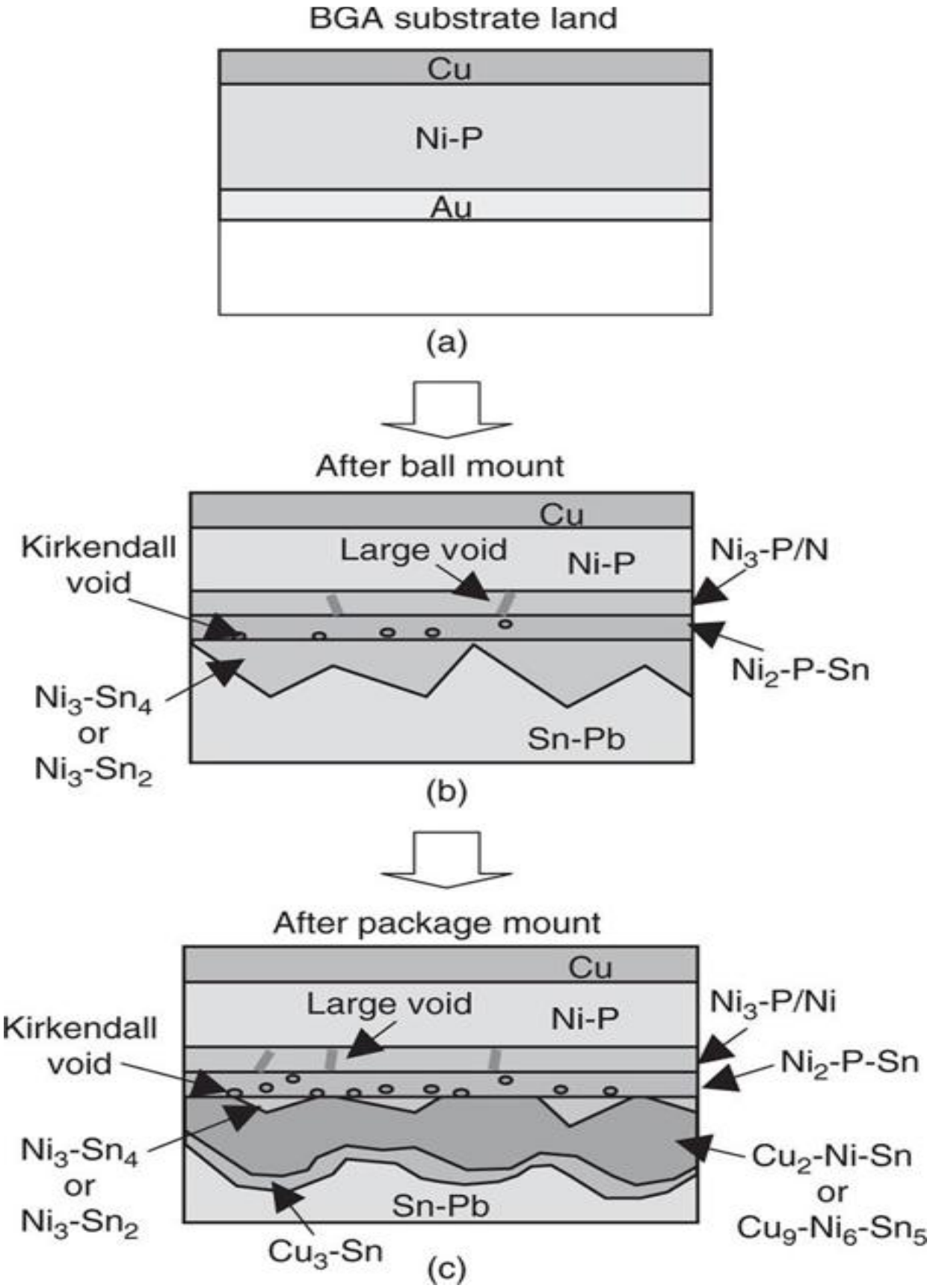

BGA substrate land
Cu
Ni-P
Au
(a)
After ball mount
Cu
Kirkendall void
Large void
Ni-P
Ni3-P/N
Ni2-P-Sn
Ni3-Sn4 or Ni3-Sn2
Sn-Pb
(b)
After package mount
Cu
Large void
Ni-P
Ni3-P/Ni
Kirkendall void
Ni2-P-Sn
Ni3-Sn4 or Ni3-Sn2
Cu2-Ni-Sn or Cu9-Ni6-Sn5
Sn-Pb
Cu3-Sn
(c)

FIGURE 62.18 Solder joint intermetallic formation. (a) The constituent material stack up in a BGA substrate land pad. (b) After the ball is attached, a number of intermetallics are formed between the copper pad and the SnPb solder joint. Kirkendall voids are known to form at the phosphorus-rich Ni layer and Sn-Ni intermetallic interface. (c) After board-level reflow, the interface region thickens and several more intermetallics are formed.[19] (*Reprinted with permission from Renesas Technology Corp./© [2003] IEEE ECTC*.)

The presence of pervasive Kirkendall voids could reduce the strength of the solder joint. A mechanically applied strain could result in the sort of brittle solder joint failure shown in Figs. 62.19 and 62.20.

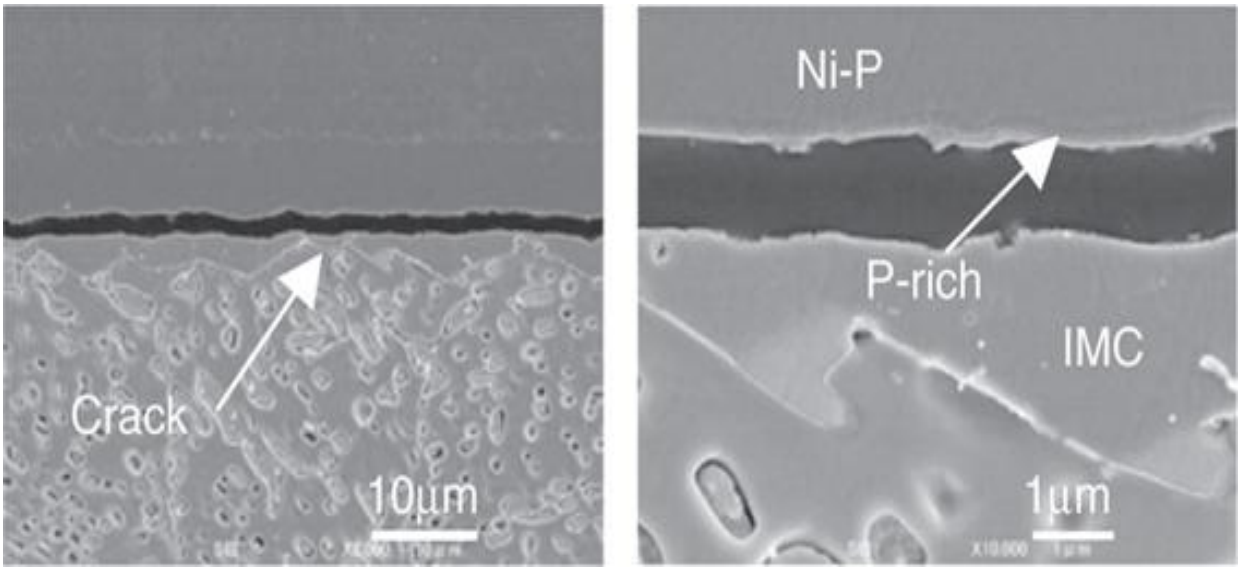
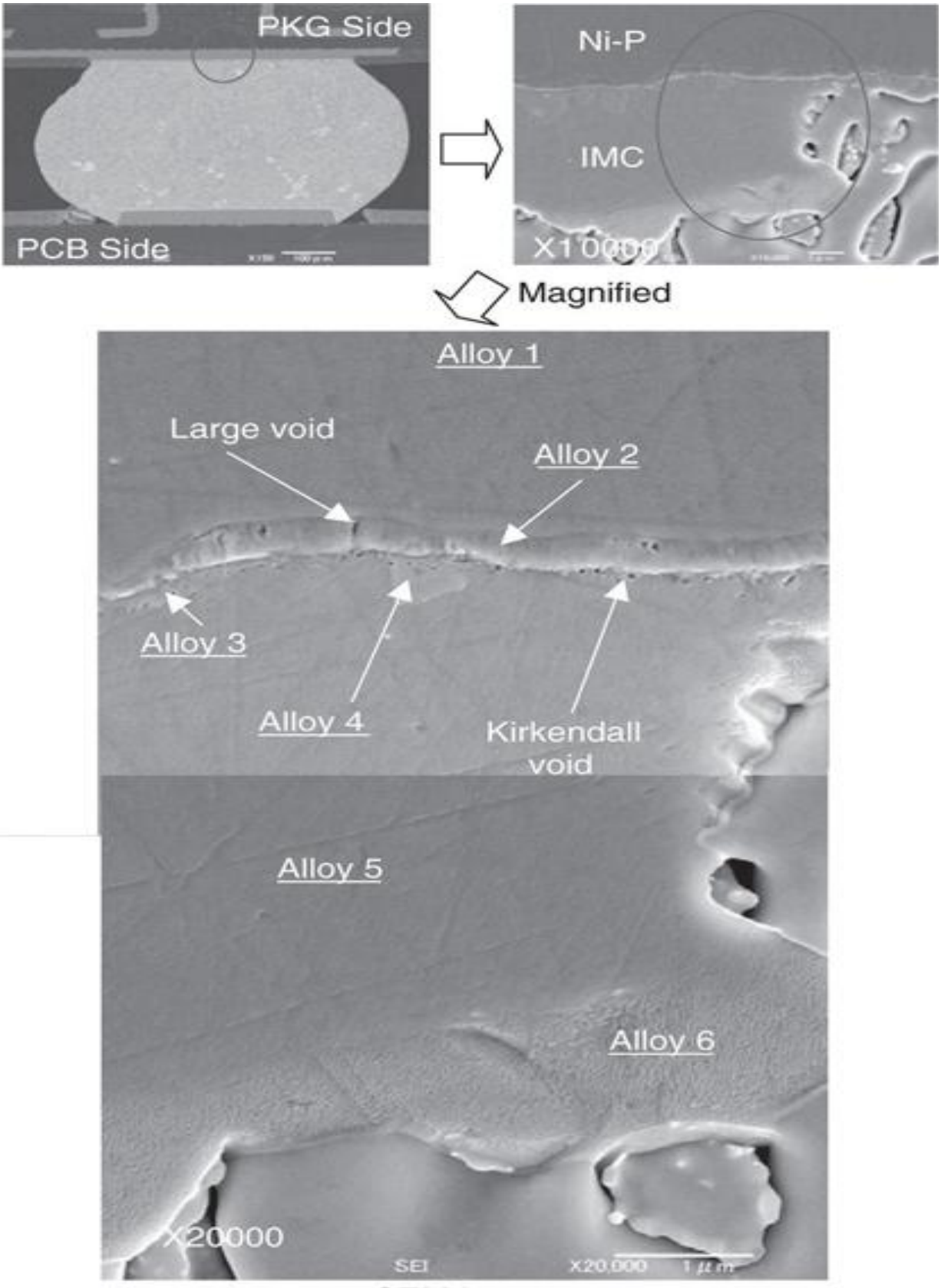


FIGURE 62.19 Brittle solder joint failure.[19] A clear separation between the P-rich phase and IMC on the package side is shown. (*Reprinted with permission from Renesas Technology Corp./© [2003] IEEE ECTC*.)


PKG Side
PCB Side
Ni-P
IMC
X10000
Magnified
Alloy 1
Large void
Alloy 2
Alloy 3
Alloy 4
Kirkendall void
Alloy 5
Alloy 6
X20000
SEI
X20,000 1 μm

SEM image

FIGURE 62.20 Intermetallics formed in solder joint with brittle fracture.[19] (*Reprinted with permission from Renesas Technology Corp./© [2003] IEEE ECTC*.)

- *Ni-Cu-Sn intermetallic* Another phenomenon reported to cause a similar failure is based on the formation of a Ni-Cu-Sn ternary intermetallic in the solder joint.[20] The Ni-Sn intermetallic forms on the component side during ball attach. When the part is mounted on the board, copper migrates from the board pad side, across the BGA ball, to form a Ni-Cu-Sn intermetallic on the component side. The thickness of this ternary intermetallic, typically 3 to 5 mm thick, could grow with additional reflows.[20] Clearly, an important factor contributing to this phenomenon is the surface finish on the PWB side. If the surface finish has a barrier like Ni to prevent copper from migrating across the BGA ball, this ternary intermetallic is less likely to form on the component side.
- *Strain/strain rate* It has also been observed that the strain to failure of solder joints is a strong function of the strain rate. The higher the strain rate, the lower the strain-to-failure. One theory to explain this strain rate dependency is that the stiffness of bulk solder itself is strain rate dependent: at low strain rates, solder tends to deform and absorb some of the applied strain. Thus, less strain is actually transferred to the Kirkendall void-rich region. At high strain rate levels (typically above 5000 uε/s), bulk solder behaves more like a linear elastic material and transfers more of the applied strain to the voids, causing brittle solder joint fracture. A graph illustrating the relationship between strain and strain rate for solder joint failure is given in Chap. 59.

  It is important to note that brittle solder fracture does not always occur exclusively. Frequently, it can be accompanied with pad lift, substrate cracking, or other intermetallic-related failure.

2. *“Black pad” corrosion phenomenon*[21] This is a discoloration phenomenon caused by excessive oxidation of the Ni. This leads to increased contact resistance, which causes intermittent opens during electrical testing. It is believed that the “black pad” phenomenon is caused by impurities in the plating bath during the ENIG plating process. The impurities create pores in the gold plating, thus exposing the Ni to moisture and other contaminants. Consequently, the Ni oxidizes and manifests in varying extremes as a discoloration in the pad. Tighter process controls during the plating process and regular purging of the plating bath can significantly mitigate this corrosion phenomenon. Failures stemming from black pad can be distinguished from brittle fracture by the following features: visible discoloration of the pads and a lot-to-lot dependency in failures due to impure plating baths.

62.3.11.1.1 Effect of Lead-Free Conversion. Given these known issues with ENIG, many package suppliers have moved away from it for lead-free applications. However, several package suppliers still use ENIG with standard tin-lead and lead-free solder. There isn’t enough data to show the effect of ENIG on lead-free solder, but preliminary results indicate that the failure modes seen with tin-lead solder would also be seen with lead-free solder. In general, since lead-free solders are stiffer than tin-lead solders, they have higher strain/strain rate strength than tin-lead solders. More detail on tests to evaluate failure strength and failure modes is provided in the next chapter.

62.3.11.2 Solder-On-Pad. This is also known as “pre-applied solder” because it involves pre-applying a small amount of solder on the package substrate pad before the ball-attach process. Care must be taken to ensure that the height of solder applied on the pad does not exceed the thickness of the solder mask (Fig. 62.21).

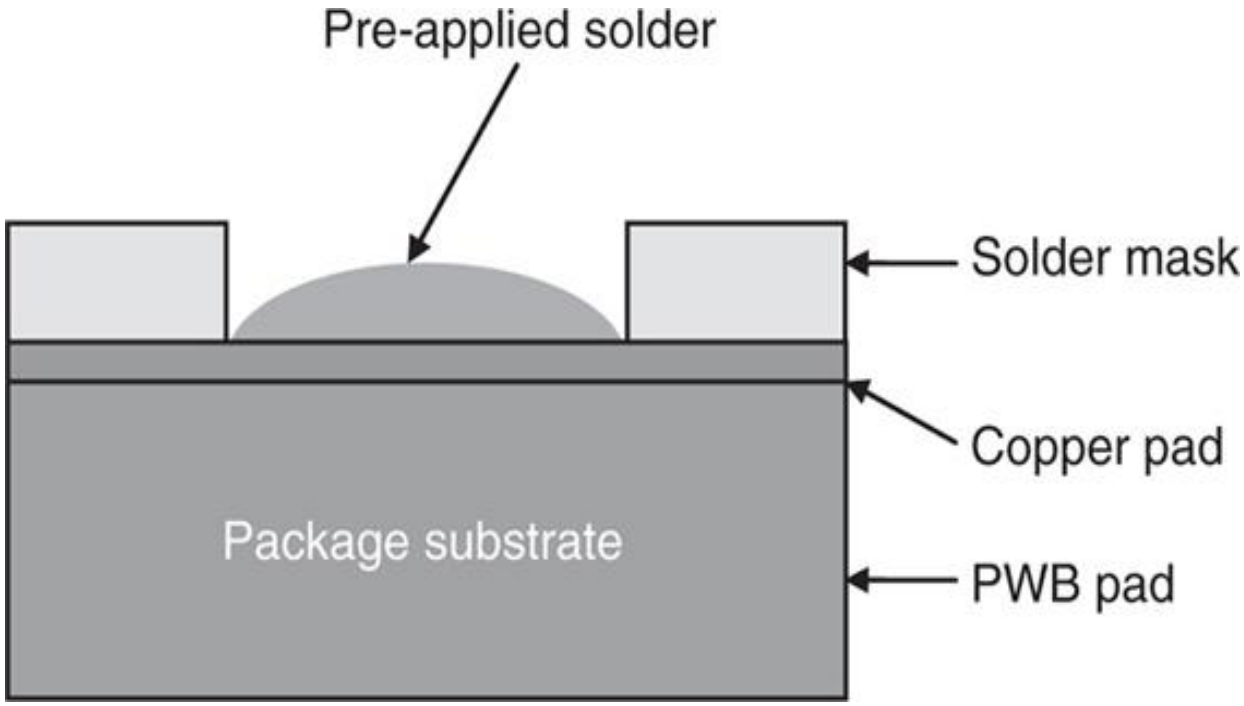


FIGURE 62.21 Solder-on-pad schematic.

Exceeding the height of the solder mask would result in alignment/registration issues during the assembly process. As with ENiG, there are concerns with the mechanical robustness of solder-on-pad (SoP) solder joints. The Ni in ENIG serves as a diffusion barrier for the copper metallization. In the absence of Ni, copper diffusion occurs much faster and two intermetallics are known to form in SOP solder joints: Cu_6Sn_5 and Cu_3Sn. Under high temperature aging conditions, these intermetallics are known to grow in thickness. Thus, if tin-lead or lead-free parts with SOP are aged at high temperature (either in lab testing or in field conditions), they could have a higher propensity for brittle fracture.[22,23] By extension, one concern is that if solder joints can become brittle when aged over time, what would happen if the product has been operating in the field at high nominal operating temperatures, and it is subjected to shock conditions? Would it fail early? For instance, what if the product is a cell phone with an SOP based BGA used in it? If the user drops the cell phone after sustained usage, is there

a propensity for brittle fracture? According to some publications on shock testing of lead-free assemblies (Cheng et al.),[22] aged SOP joints subjected to shock conditions tend to fail relatively early. However, this has not been universally demonstrated. Moreover, the shock conditions to which hand held products are tested (~1500 G max), are much more aggressive than typical shock conditions for server environments (~500 G max). In tests performed on aged tin lead SOP samples subjected to lower shock conditions, the parts were not shown to fail due to brittle fracture, even though the presence of some Kirkendall voiding was observed (Mei et al.).[24] However, the amount of Kirkendall voiding observed was not as pervasive as that reported by Cheng et al.[22] (Fig. 62.22).

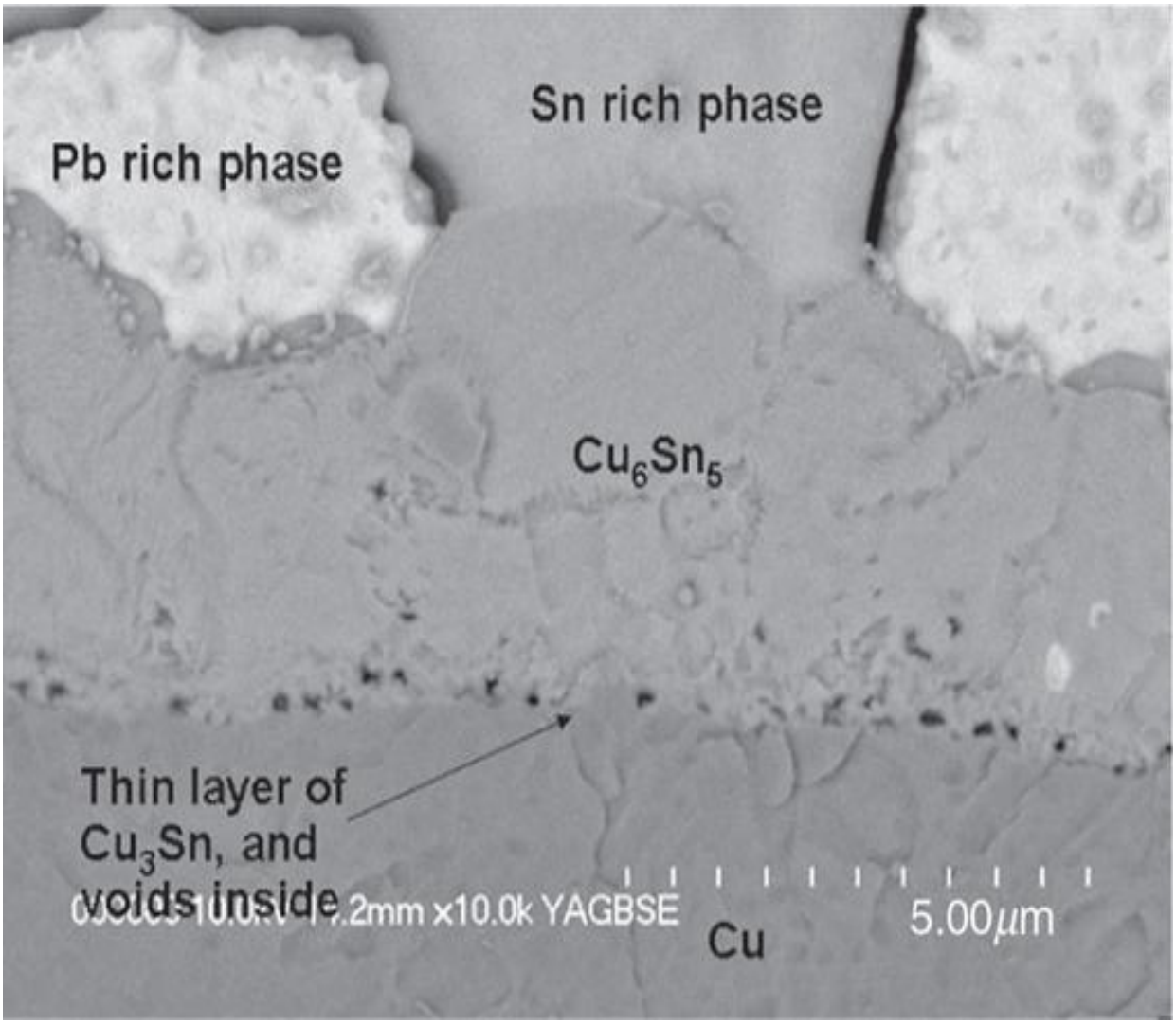


FIGURE 62.22 SEM backscattering electron image of tested sample with solder-on-pad surface finish—package/ball interface. The image shows the intermetallics formed at the joint/package interface. These intermetallics include a thick layer of Cu_6Sn_5 and a thinner layer of Cu_3Sn. Small voids are seen at the Cu_6Sn_5 and Cu_3Sn interface.[24] (*Reprinted with premission from IEEE © [2005].*)

A curve fit of the data by Cheng et al.[22] reported by Mei et al.[24] as a function of void area and aging time for different temperatures is shown in Fig. 62.23.

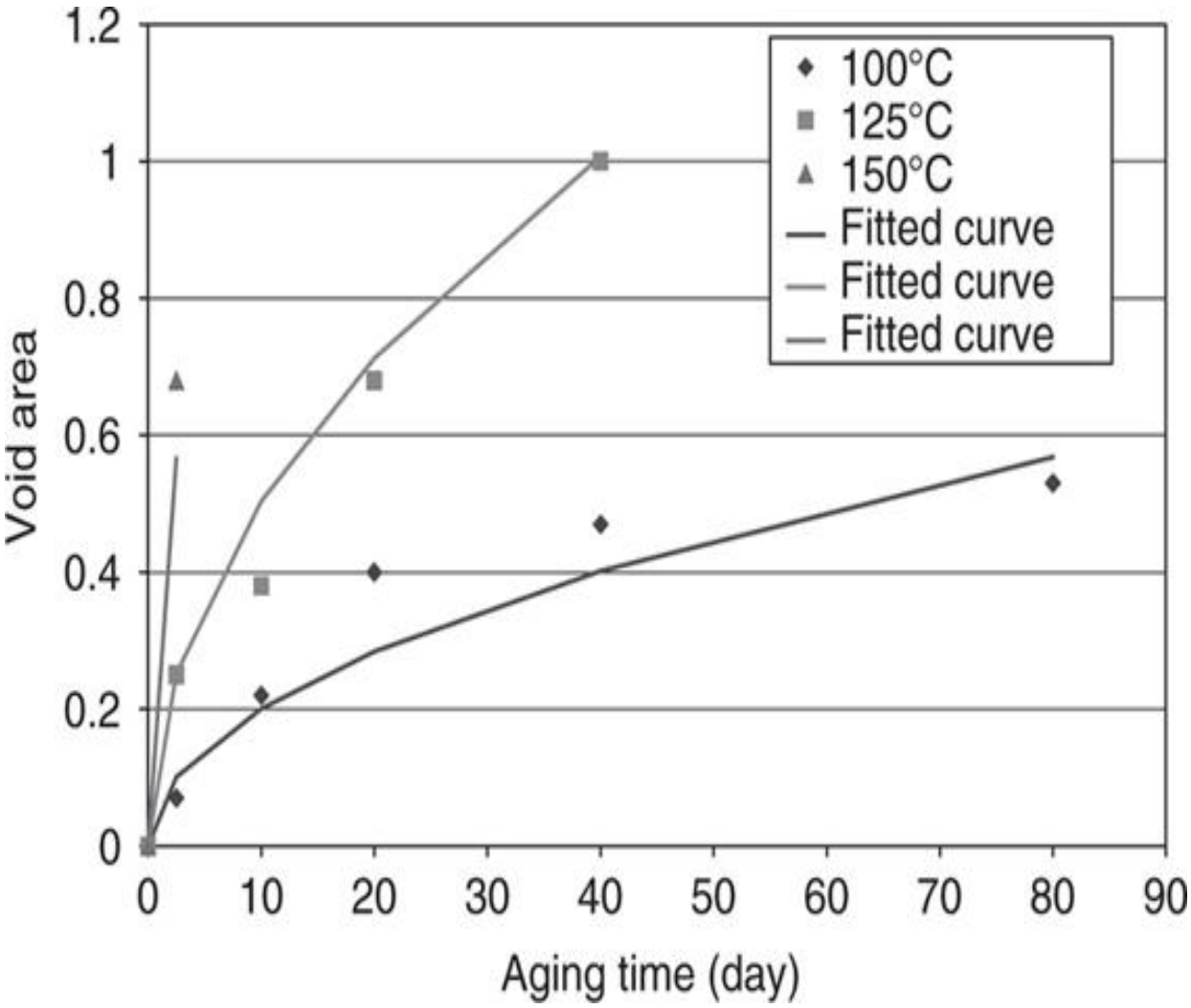


FIGURE 62.23 Curve fit of data at three different temperatures based on the data generated by Cheng et al.[24] The values are based on experimental measurements of void area versus time for different temperatures. (*Reprinted with premission from IEEE © [2005]*.)

The fit equation from the Cheng et al.[22] data is given as[24]:

$$A = Ct^{0.5} \exp\left(\frac{-Q}{RT}\right) \tag{62.1}$$

where A = ratio of voided area to the joint interface area
t = time in days
Q = activation energy
T = absolute temperature in K
R = gas constant.
$C = 145590\ (\text{day}^{-0.5})$
$Q = 45413\ \text{J/mol}\ (0.47\ \text{eV})$

With this approximate curve fit, extrapolating to end-use conditions can give an estimate of the time it would take for the voiding to reach 50 percent of the interface area. For instance, at 50°C nominal operating temperature, it would take 6000 days (16.5 years) to reach 50 percent of the interface area. It is important to note that the mechanisms that control the propensity and pervasiveness of Kirkendall voiding are not clearly known at this time. There isn't enough experimental data in the industry at this time to conclusively validate the aforementioned relations.

The occurrence of Kirkendall voids is not limited to the package/solder joint interface. If OSP is used as the PWB surface finish, the same phenomenon is observed to occur on the PWB side.[24]

In terms of strain/strain rate strength, un-aged, SOP-based joints have been shown to have as much as twice the strength of ENiG joints. More details on comparison tests are outlined in the next chapter.

There are a number of other surface finishes used in the industry, such as Electroless Nickel Electroless Palladium Immersion Gold (NiPdAu), Immersion Silver, Immersion Gold, Immersion Tin, OSP and Electrolytic Nickel Gold. There are reliability and process trade-offs with each surface finish. That is why it is recommended that strain/strain rate characterization and thermal cycling be performed for each

set of surface finish before it is selected for the specific end-use conditions in which it will be used. The industry test methods used to evaluate different surface finishes are outlined in detail in the next chapter.

62.3.12 Final Electrical Test Architecture

During in-circuit testing (ICT), assemblies are subjected to high strains due to the number and distribution of test points applied underneath BGAs. Assemblies are also subjected to high strain rates in ICT because the speed of engagement of test points helps reduce the electrical contact resistance between the test probes and probe pads. Thus, from an electrical test perspective, high strain rates are desirable during ICT. However, there is a strain/strain rate range beyond which the likelihood of solder joint failure increases.

The actual strains induced in a printed circuit board assembly (PCBA) is a function not only of the number and layout of test points, but also the fixture design, package and PWB warpage, the surface finish used on the package and PWB, and the fixture actuation rate. During final test, it is very difficult, if not impossible to reduce the number of test points. Thus, if they are correctly designed-in early in the design process, it would minimize the likelihood of strain-induced failures in final testing.

A schematic showing the forces applied in the immediate vicinity of a BGA package in an ICT fixture is shown in Fig. 62.24. The distribution of test points underneath a BGA should be made as uniform as possible. Several ICT fixtures have push fingers on the top side, which push down on the board, countering the force of the test probes. The use of “push-pins” or “push-fingers” on the top side of the board is not recommended. Push fingers induce localized stress concentrations, resulting in high strain in their immediate

vicinity. If used, push fingers should not be placed close to package corners. For some generic recommendations on ICT test point layout, refer to IPC7351.[15] An alternative to push fingers is the use of a Milled City or zero-flex top plate on the top side.

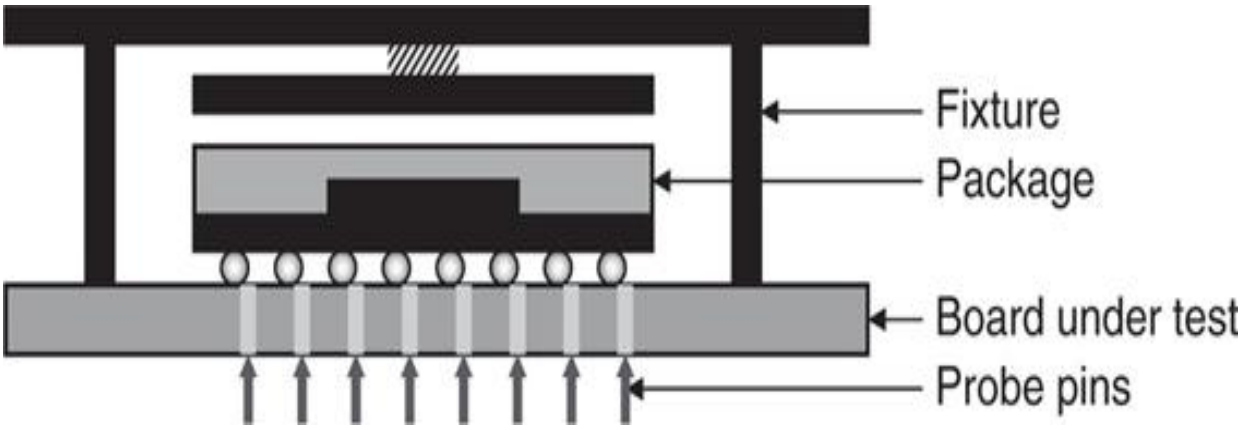


FIGURE 62.24 Schematic of ICT loading conditions.

This is basically a rigid metal plate which has a negative image of the entire board milled out. Thus, as opposed to having several push fingers, the entire board is pressed against the Milled City plate. This significantly reduces local stress concentration, and could potentially be used to enable PCBAs to withstand more test points. Milled City plates are expensive, but considering the cost of line stops and customer-related issues due to strain-induced failures in ICT, the nonrecurring cost of the Milled City is a worthwhile investment.

62.3.12.1 Effect of Lead-Free Conversion. The conversion to lead-free solder has given even more prominence to this issue. With lead-free solders, a higher temperature organic solderability preservative (OSP) could be used. As a result, it could take more force to establish contact with the test pads. This translates to higher force applied to the PCBA. Moreover, the effect of mechanical bending on lead-free solders is yet to be fully characterized.

Thus, there is a greater need to characterize the mechanical force applied on lead-free assemblies.

For the same applied force, the strain on thinner PWBs is higher than that on thick PWBs. Thus, this is more critical on assemblies with relatively thin boards (<93 mils thick). However, depending on the package, warpage, surface finish, and number of test points, it could also be seen on thick boards.

Strain gage characterization should be performed on fixtures with actual boards, in order to verify that excessive strains are not applied on critical components. In an effort to standardize strain characterization, the JEDEC/IPC 9704[25] test method was published in June 2005. This test method outlines the procedures and best practices relating to strain measurement in a manufacturing environment.

62.3.13 Package Design Parameters

A key factor that impacts second-level interconnect reliability is the package itself. Although the primary function of the package is to pass signals, power, and ground from the silicon device to the PWB, the package also provides protection for the silicon and enables a more robust interconnect than a direct chip attach. The critical package design parameters which can have a significant impact on the reliability of the solder joints are discussed in this section.

62.3.13.1 Overall Dimensions and Distance from Neutral Point. Package size continues to grow as the number of I/Os increase to meet the demands of ever increasing IC functionality. As IC complexity increases, memory is embedded in devices, while as silicon feature sizes decrease, I/O counts continue to be driven upward. Package dimensions have surpassed 50 mm. Package layer

counts for both ceramic and plastic material sets continue to increase rapidly.

In addition to the solder joint geometry issues outlined in Sec. 62.3.8, increases in overall size tend to coincide with increases in the distance from the center of the package to the outer ball (see Fig. 62.25). This dimension is referred to as the distance from the neutral point (DNP). As DNP increases, the amount of stress and subsequent damage inflicted on solder joints increases, especially during thermal cycles encountered in field environments. Thus packages with larger DNPs (and with all other material and design parameters equivalent) will have lower interconnect reliability. This is crucial when assessing second-level reliability data.

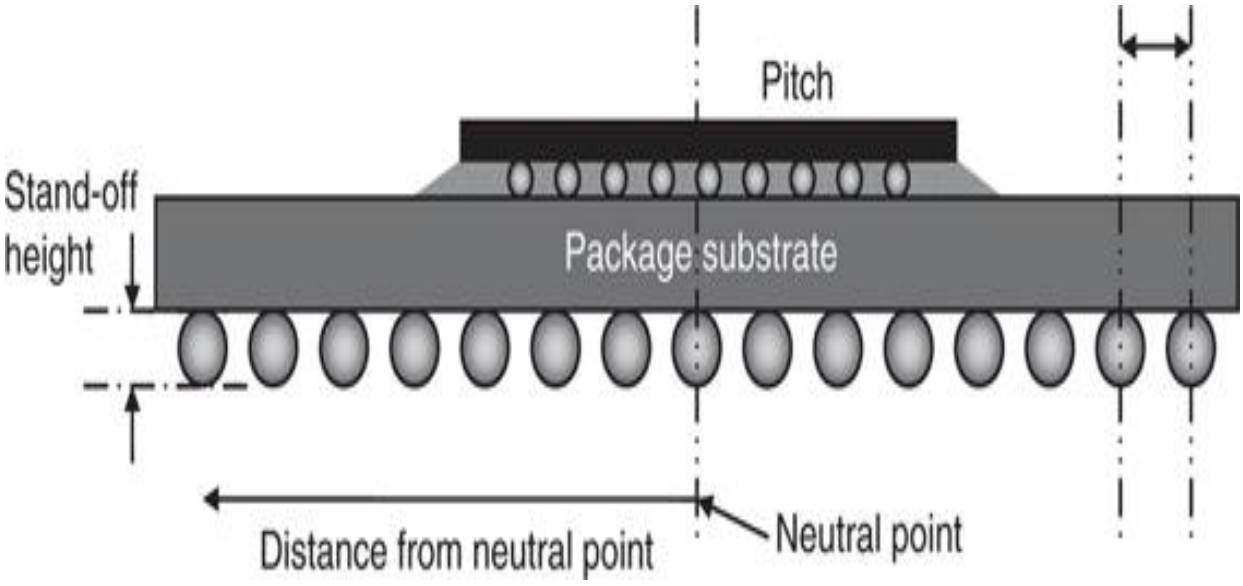
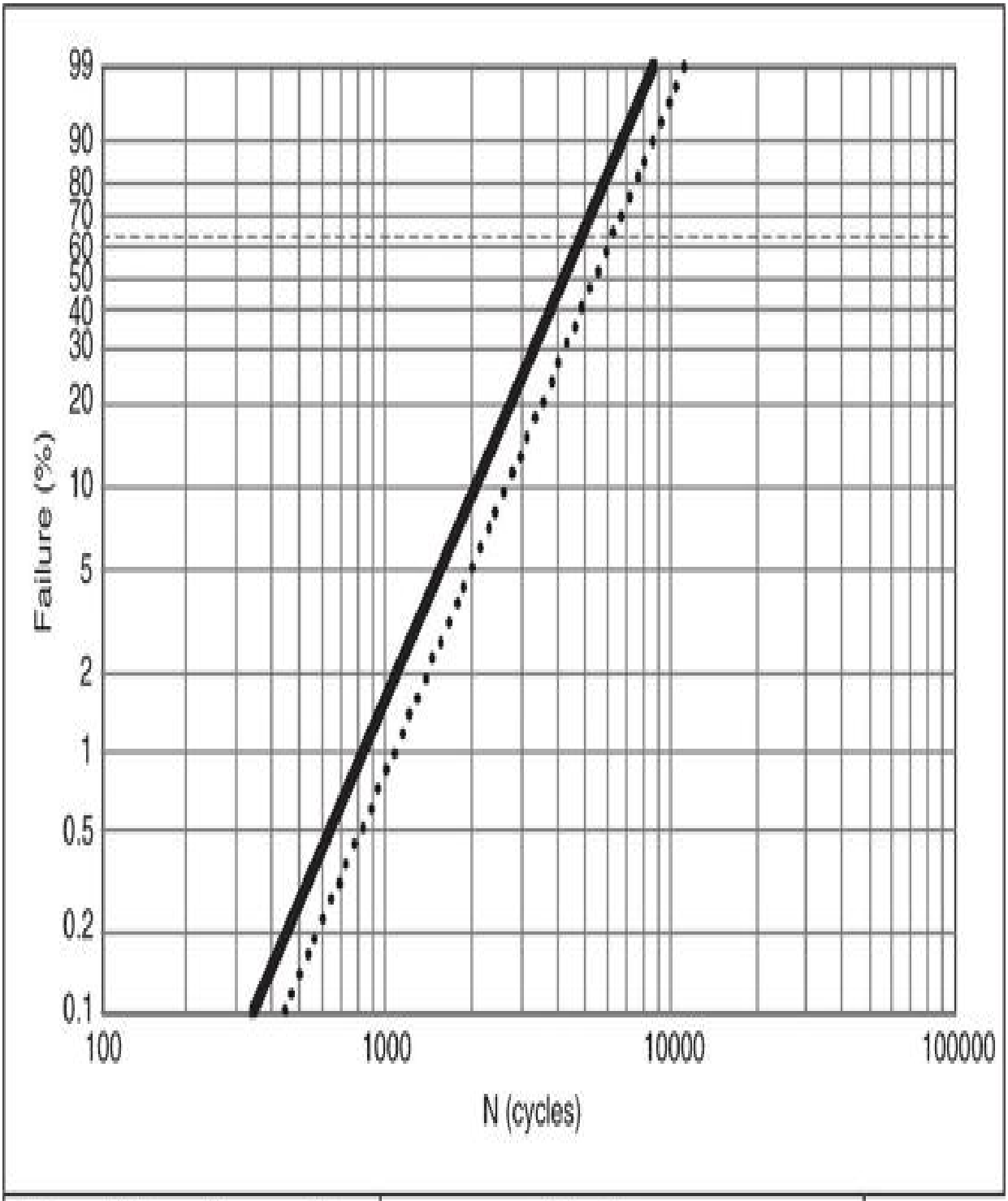


FIGURE 62.25 Distance from neutral point (DNP) for a BGA-type package. The DNP increases when moving away from the center (center line) of the package. Pitch is also indicated in this diagram. Pitch is defined as the center-to-center distance between two adjacent interconnects (in this example, between two adjacent solder balls).

Most packaged IC suppliers qualify their products by thermal cycle experiments. The most common board-level temperature cycling methodology used across the industry is

outlined in IPC 9701.[6] The resistance in each solder joint is typically monitored in real time by incorporating a daisy-chain package and some type of data acquisition system. The end results of these experiments are failure distributions typically presented as Weibull plots (for details on Weibull distributions and failure life analysis, refer to Sec. 64.2.2 in Chap. 64) that show failure percentage as a function of time.[26] Note that if a package with a larger DNP than was qualified is considered, then there could be severe degradation in reliability and a full assessment should be conducted. However, if a package with a smaller DNP (10 to 20 percent smaller) than the package qualified (with all other material and design parameters being equal) is considered, then the proposed package should be at least as reliable as the qualified package.

62.3.13.2 Ball Pitch and Ball Size. Ball pitch is the center-to-center distance between two adjacent solder balls (see Fig. 62.25). In theory one could change the ball pitch and keep the same solder joint size. In practical applications though, decreases in ball pitch also require a reduction in solder ball diameter and pad size for physically accommodating the decrease in distance between adjacent balls. This decrease in ball size, with decreasing pitch, results in the formation of smaller balls with smaller stand-off between the package and the PWB. Smaller solder balls and decreased stand-off have been shown to decrease solder joint reliability (see Fig. 62.26).



Eta	Beta	r^2	n/s
4806	2.6	---	-/-
6231	2.6	---	-/-

	Data set	
▬	1	S3 30 Mil ball 1.5 mm
⋯	2	S3 35 Mil ball 1.5 mm

FIGURE 62.26 Weibull plots for two different ball size/stand-off heights. The solid line indicates the finite element analysis (FEA) predicted failure distribution for an interconnect based on a 30-mil stand-off height. The dashed line indicates the FEA predicted failure distribution for an interconnect based on a 35-mil stand-off height. Note that a reduction in stand-off height correlates with a decrease in fatigue life.

The dashed line in Fig. 62.26 represents the finite element analysis results for a 0.889-mm (35-mil) ball. The solid line represents finite element analysis results for a 0.762-mm (30-mil) ball. Note that the 0.889-mm ball is 1.3 times more reliable than the 0.762-mm ball. Thus reduction in pitch can result in decreases in reliability due to the subsequent decreases in solder ball size necessary to accommodate adjacent balls and the reduced stand-off heights due to smaller solder balls.

The PWB designer is therefore faced with a dilemma when considering a reduction in ball pitch. Not only is there a risk of reduced assembly reliability, but there is also a design challenge. A direct consequence of decreased pitch is added complexity in the ability to route all traces out from the package to the PWB. Designers are also sometimes forced to add additional layers to PWBs in order to accommodate reduced-pitch parts. This layer increase results in increased price and in some instances, drastic reductions in capacity due to the increased complexity associated with fabricating high-layer-count PWBs.

62.3.13.3 Ball Array (Full or Depopulated). Ball array is another variable that has an indirect impact on solder joint reliability. There is a coupled effect between the location of the edge of the packaged die, the solder ball array, and the state of stress in the solder joints. The silicon has a much lower CTE than plastic substrates. Thus the die can create a state of overconstraint, producing excessive stress in the solder joints under and near its edge. This overconstraint tends to be worst in joints near the edge of the die.

Figure 62.27 contains schematics of one configuration where a full array is employed and the edge of the die falls over the solder joints. Figure 62.28 illustrates an alternative design, where a region near the perimeter of the die is depopulated of all solder balls (the depopulated configuration). Many plastic (laminate) package suppliers offer a depopulated option to enhance reliability by not placing solder joints in the worst-case regions under the perimeter of the die. Additionally, many package designers further reduce risk of CTE-induced joint failure by only placing redundant power and ground or nonfunctional thermal balls under the core. If redundant balls or thermal balls do crack, the impact on device performance is negligible. Finally, in large laminate packages, the corner-most balls could also fail early. As a result, many package suppliers depopulate the corner balls of the package to enhance solder fatigue life.

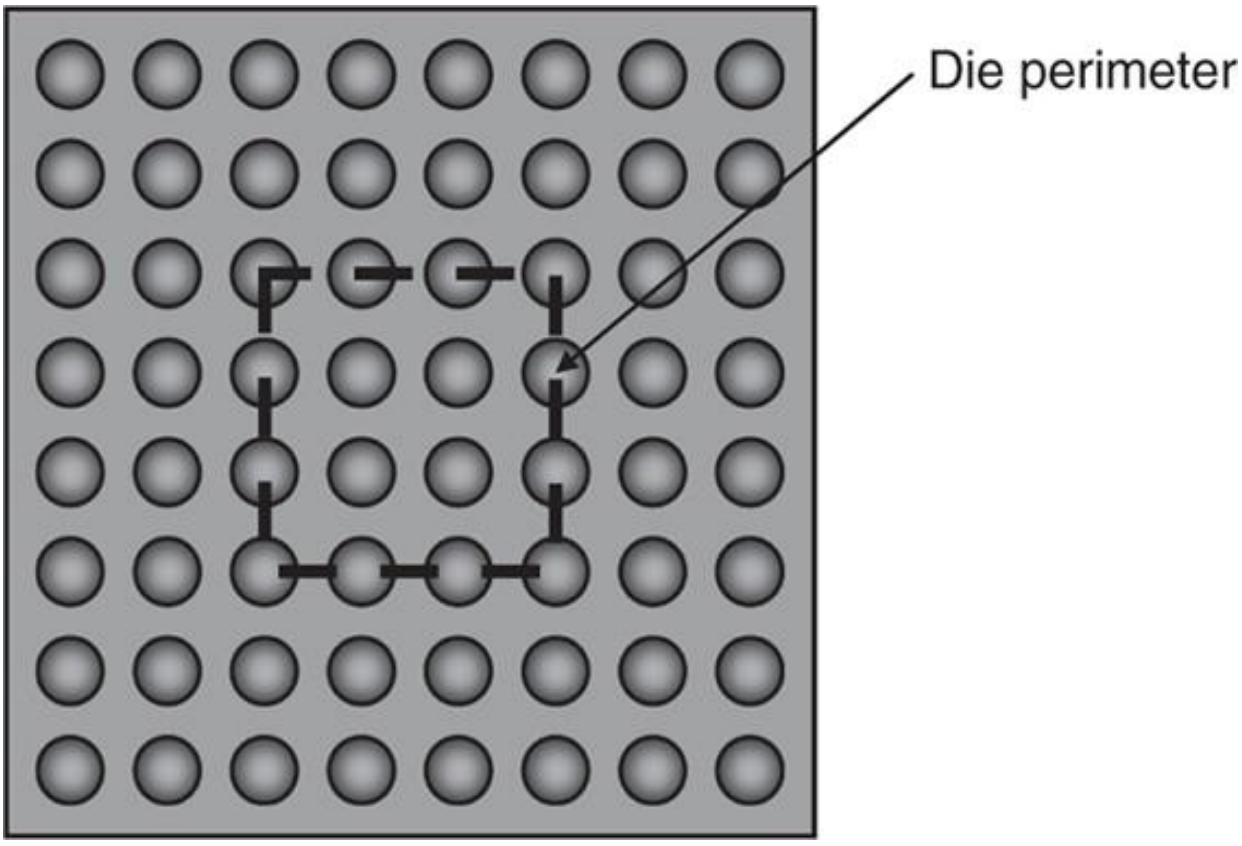


FIGURE 62.27 Full array with solder joints under the die perimeter. Solder ball locations are indicated by the array of circles. The die perimeter is indicated by the black dashed rectangular outline. Note that the die edge falls directly over solder joints.

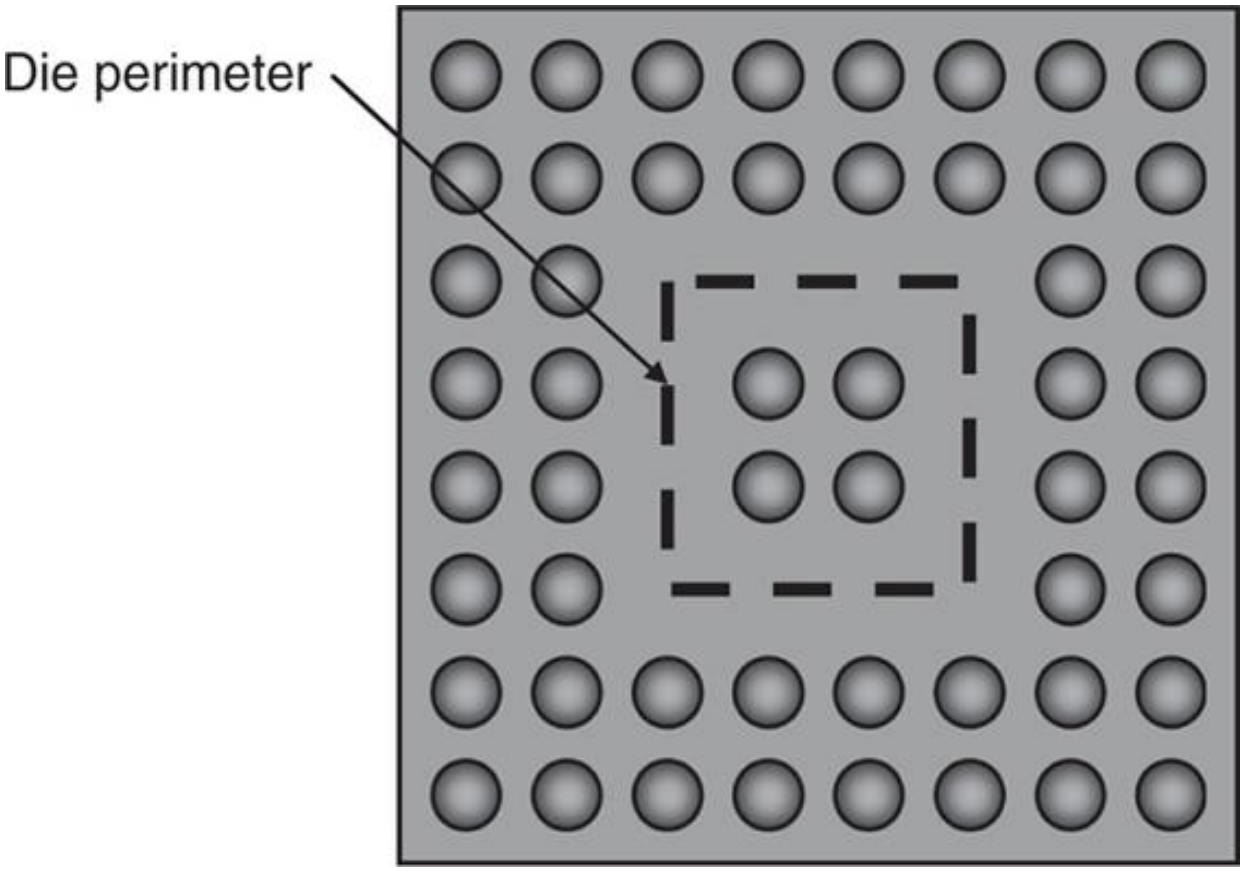


FIGURE 62.28 Depopulated array with no joints under the perimeter of the die. Solder ball locations are indicated by the array of circles. The die perimeter is indicated by the dashed rectangular outline. Note that the die edge falls in an area of depopulated solder balls.

62.3.13.4 Heat Spreader/Stiffener. A cross-sectional schematic of a flip-chip assembly, with a heat slug and stiffener, is shown in Fig. 62.29. The primary reason for employing a heat spreader lid is for thermal management. A secondary benefit is that the stiffener and heat slug reduce the potential for out-of-plane warpage occurring during reflow and thermal cycling. An additional benefit of incorporating a heat slug and stiffener into a laminate

package design is improved ability to handle the package due to increased robustness of the packaged die.

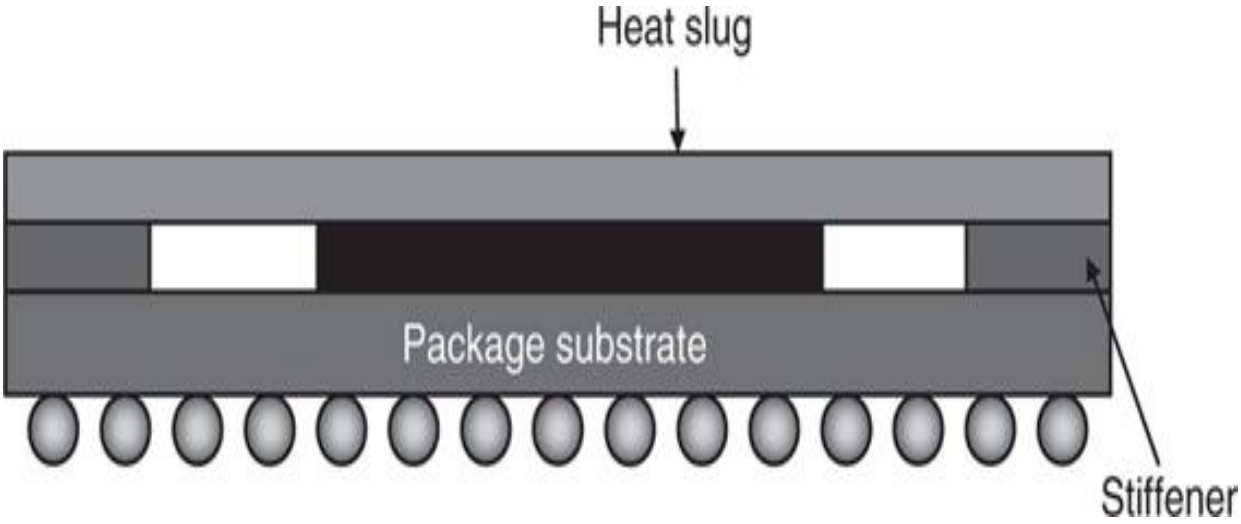


FIGURE 62.29 Flip-chip BGA with stiffener and heat slug. The stiffener provides added rigidity to the package and also provides mechanical support for the heatsink.

A variety of heat spreader materials have been used: copper, aluminum, steel, and aluminum silicon carbide (AlSiC). Copper provides the best thermal conductivity, but it has a high CTE. AlSiC has a slightly higher modulus than copper, but it has a lower CTE. As a result, in several applications, AlSiC is gaining more prevalence. Its thermal conductivity is lower than copper and comparable to aluminum (180 to 200 Wm^{-1} K).

For cost reasons, several package suppliers also use an alternative to the heat spreader/stiffener design, namely, a single piece lid design to act as a rigid support and provide heat transfer at the same time. This design is easier to manufacture and also reduces assembly steps (see Fig. 62.30 for more details).

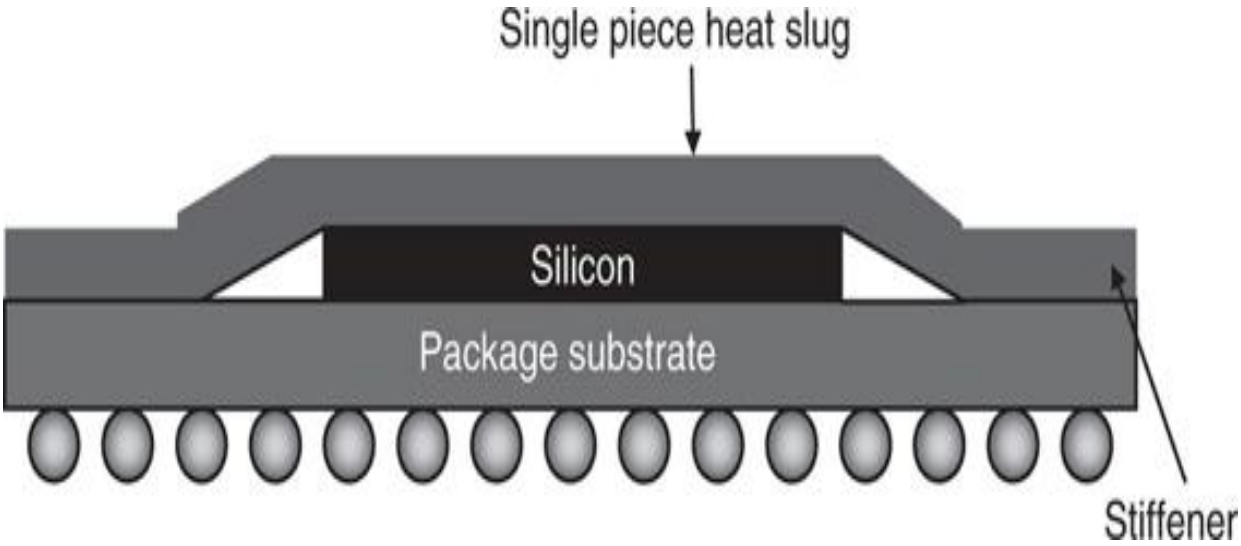


FIGURE 62.30 Single piece lid design.

The thickness of a single piece lid is typically less than that of the heat spreader/stiffener combination. Changing the stiffness of the package could alter its out-of-plane warpage, which in turn could impact the reliability of the solder joints. Therefore the effect on the overall stiffness should be characterized when using a single piece lid. One characterization method is to perform Moiré measurements on the free standing package, as a function of temperature.

Another variation of the standard heat spreader/stiffener design is the use of just a stiffener alone. This is usually for bare die applications where the wattage of the chip is so high that the thermal resistance between the chip and the heat spreader is unacceptable. In such cases, the stiffener is retained for stiffness and robustness, but the heat spreader is removed.

62.3.13.5 Mold Compound Selection. The overmold compound used in plastic ball grid array (PBGA) packages could significantly impact the assembly yield and reliability of solder joints. If the glass transition temperature (T_g) of the mold compound is significantly below the peak reflow temperature and if its modulus and CTE drastically change

above its T_g, the package could warp significantly as it is heated. As a result, when the package reaches liquidus, the effective warpage between the package and PWB could be such that solder joint opens/bridges could occur. In large PBGA packages (>40 mm), it would be more effective to use an integrated heat spreader in the molded package to rigidize it and minimize excessive warpage. Integrated heat spreaders are primarily used to improve thermal performance, but they also help rigidize the package for improved assembly yield.

With the conversion to lead-free materials, the mold compound selected needs to be such that it can withstand the higher reflow temperatures of lead-free assembly. If the mechanical material properties of the mold compound (elastic modulus, CTE, and T_g) are not appropriately selected, the package could warp significantly at reflow temperatures and result in solder joint opens.

62.3.13.6 Underfill Material Selection. The underfill material selected in flip chip BGA (FCBGA) packages could significantly impact the reliability of the board mounted package. If the underfill material is too stiff, it would rigidize the assembly and thus transfer more strain to the silicon die. This could result in delamination at any of the critical interfaces: underfill/ passivation, passivation/die, underfill/substrate, or within low-k layers.

On the other hand, if the underfill material is too soft, it could result in first-level interconnect failure. A less stiff underfill could also help reduce board-level assembly warpage, which in turn helps the second-level interconnects. Thus, the stiffness of the underfill selected should be optimized such that it does not lead to delamination or first-level interconnect failures.[9] In addition to stiffness, CTE, and T_g, there are several other factors that dictate the underfill

material selected, such as thixotropy, viscosity, shrinkage, curing temperature, and curing time.

The choice of underfill material is also influenced by the conversion to lead free. For lead-free packages, even though there is a European exemption on the first-level interconnects,[27] many package suppliers are looking at using lead-free first-level interconnects. As a result, the underfill material selected has to be such that it can withstand the higher reflow temperatures, and has low shrinkage for the increased temperature range.

62.3.13.7 Die/Package Aspect Ratio. The size of the silicon die relative to the package body size could significantly impact the reliability of the package. This is especially applicable to PBGA packages. The larger the die relative to the package, the higher the CTE mismatch-driven strains imparted to the second-level solder joints.[28] The degree of impact varies with package body size and absolute die size.

62.3.13.8 Package Substrate Material. The choice of package substrate material can have a large impact on solder joint reliability. Some substrates require employing solder ball alternatives (such as the ceramic solder column carriers shown in Fig. 62.4) or even the elimination of a soldered solution due to interconnect reliability considerations. A wealth of information regarding ceramic and plastic substrates can be found in the literature.[26,29,30] This section focuses on the impact of those materials on solder joint reliability.

The two key material properties of a substrate that impact interconnect reliability are modulus of elasticity (E) and coefficient of thermal expansion (CTE). Modulus of elasticity is defined as the ratio of stress to strain and can be used to describe a material's ability to resist deformation when subjected to an applied load. CTE relates the change in

length of material when heated or cooled and can be used to describe a material's deformation when subjected to temperature changes. Reference 31 contains detailed discussions of modulus of elasticity and coefficient of thermal expansion. A tremendous amount of material property data can be found in the literature.[26,29,30] Figure 62.31 contains a sketch of a simplified solder joint interconnect. Note that the driving force for solder joint fatigue during field use is the coefficient of thermal expansion mismatch between the assembled package and the PWB. Additionally, the modulus of elasticity of the substrate can impact the fatigue life of solder joints by increasing (or decreasing) the driving force that is imparted to the solder interconnect.

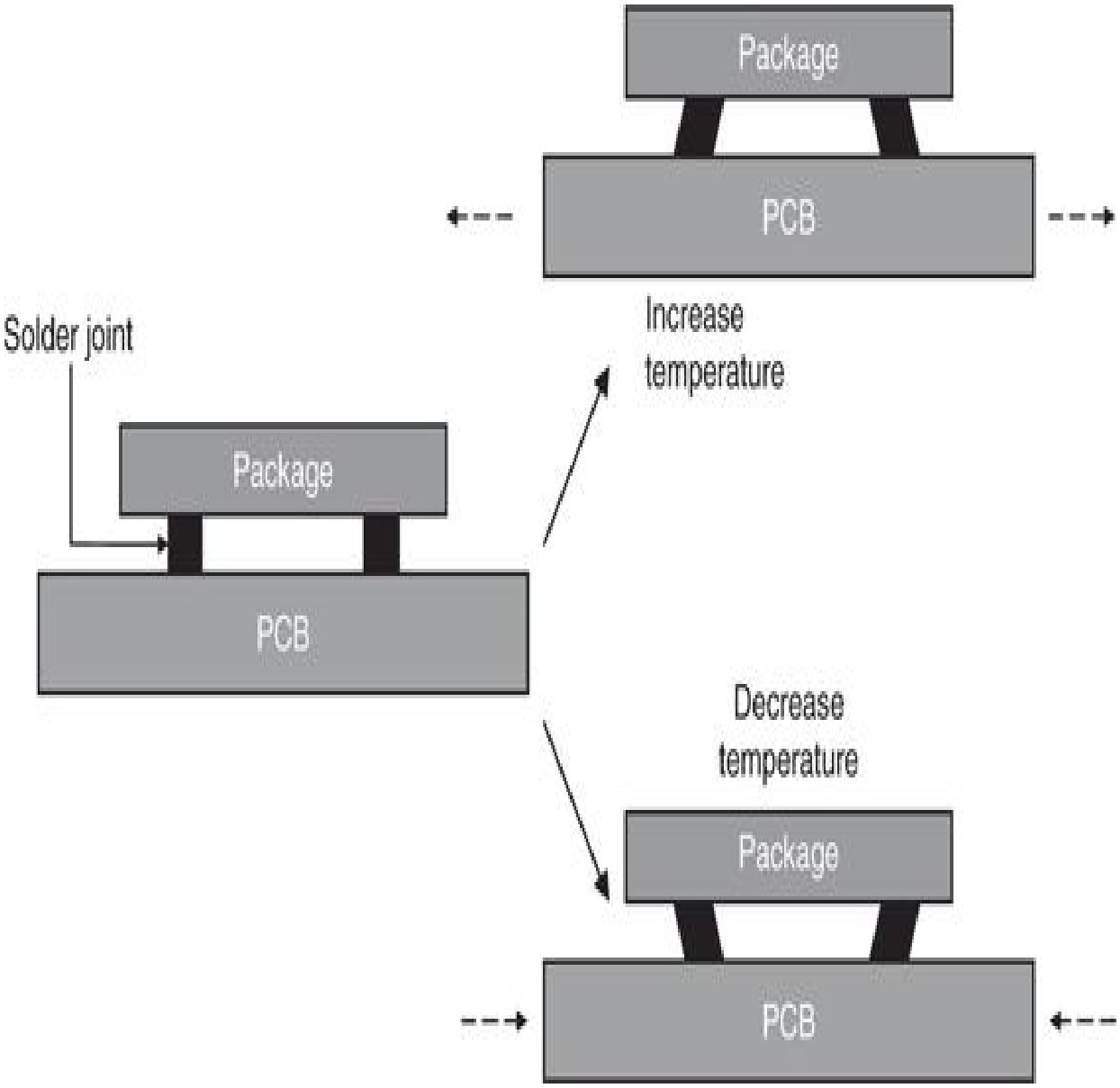


FIGURE 62.31 Simplified CTE mismatch effects. As the temperature increases, the PWB expands at a higher rate than the package due to the package having a lower effective CTE. As the temperature decreases, the opposite effect is observed.

Ceramic materials provide excellent CTE match between the die and package, which then reduces the risk of first-level solder bump failure in flip-chip applications. Unfortunately, this superb CTE match between the ceramic and the silicon die creates a large CTE mismatch between the ceramic package and the PWB. This CTE mismatch

creates severe stress on the second-level interconnects (see Fig. 62.31). This CTE mismatch, combined with DNP issues (previously discussed), limits ceramic BGA body sizes to approximately 32 × 32 mm. Ceramics with larger body sizes typically employ solder columns (Fig. 62.4) or compression-type sockets for second-level interconnect.

The CTEs of plastic packages tend to match the CTEs of PWBs fairly well. This CTE match allows for larger package body sizes to be employed when using a laminate-based BGA than with a ceramic package. It is crucial to note that many other variables independent of second-level reliability must be taken into consideration when selecting a package. Power requirements, signal integrity, first-level reliability (interconnect between the die and package), and cost must all be balanced when selecting the correct package for a specific application.

62.3.13.9 Impact of Low-k Dielectrics. Continued miniaturization and integration has led to the need for a multilevel interconnect layout to minimize the time delay due to parasitic resistance (R) and capacitance (C). The improvement in gate-level device speed is negated by the propagation delay at the metal interconnects because of the increased RC time constant.[32] For instance, the RC delay of long interconnections contributes up to 50 percent of the time delay in devices with a gate length of 250 nm or less.[33] A reduction in the RC time constant requires the use of low resistivity interconnect materials and low capacitance interlayer films. The capacitance is a function of the material dielectric permittivity (ε_i), area (A), and thickness (d). ($C = \varepsilon_i A/d$). Increasing the area would require increased interconnect lengths, which in turn would result in high resistance. The thickness can also not be increased because it also increases resistance and poses manufacturing challenges in consistently filling the interlayer layers. Consequently, the dielectric constant (k) needs to be

reduced. Hence the need for low-*k* materials. In addition to having a low dielectric constant, ideal low-*k* materials need to have low residual stress, high planarization capability, high gap-filling capability, low deposition temperature, and ease of process integration.[32] A list of possible candidates for low-*k* materials is outlined in Table 62.3.[33]

TABLE 62.3 Typical Low-k Materials[33]

Determinant	Materials	Dielectric Constant
Vapor-phase deposition polymers	Fluorosilicate glass (FSG)	3.5–4.0
	Parylene N	2.6
	Parylene F	2.4–2.5
	Black diamond (C-doped oxide)	2.7–3.0
	Fluorinated hydrocarbon	2.0–2.4
	Teflon-AF	1.93
Spin-on polymers	HSQ/MSQ	2.8–3.0
	Polyimide	2.7–2.9
	SiLK (aromatic hydrocarbon polymer)	2.7
	PAE [poly(arylene ethers)]	2.6
	Fluorinated amorphous carbon	2.1
	Xerogels (porous silica)	1.1–2.0

However, several of the new low-*k* materials are porous and structurally weak. This poses several challenges in the back-end assembly process: poor adhesion, residual stresses in the inner layer dielectric (ILD) films, and so on. In addition

to optimizing and better monitoring the wafer-sawing process, the effect of chip-to-package interactions also needs to be characterized. The choice of material set, underfill, substrate, lid material, and so on could impact the reliability of the low-*k* dielectric.

In flip-chip BGA (FCBGA) packages, the choice of underfill material in particular has been the subject of considerable interest.[34–36] In addition to a new material set and design rules, several packaging assembly manufacturers have evaluated the use of low glass transition temperature (T_g) underfills to reduce the stresses imparted to the silicon. However, while using a low T_g underfill may minimize the stresses on the low-*k*, it could in turn transfer the stresses elsewhere, such as in the first-level interconnect.[37] Moreover, the effect of the material set on ILD delamination and solder joint reliability may be different when the free standing package is stressed, as opposed to when it is mounted on a printed circuit board and then stressed.

In wirebond BGA packages, the effect of the wirebonding process on the low-*k* dielectric needs to be characterized.[38] In addition, the choice of mold compound material (modulus and CTE) could also impact the long term reliability of the low-*k* dielectric in the fully assembled package. The package with the selected material set should be subjected to component-level and second-level temperature cycling, followed by scanning acoustic microscopy (SAM) to ensure that there are no delamination-induced failures in the low-*k* dielectric or other critical interfaces.

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CHAPTER 63

LEAD-FREE SOLDER JOINT RELIABILITY: FUNDAMENTALS AND DESIGN-FOR-RELIABILITY RULES

Jean-Paul Clech
EPSI Inc., Montclair, New Jersey

63.1 INTRODUCTION

Solder joints provide mechanical and electrical connections between components and the board or the substrate to which they are attached. Their integrity over the product design life is critical to the electrical performance of the system. Solder joints that crack due to thermal and/or mechanical loads lead to intermittent opens or completely open electrical interconnections. Solder joint failure rates are expected to remain below the components failure rates (often given in FITs, where 1 FIT is defined as 1 failure in 10^9 device hours) throughout the intended design life of the system. In practical terms, this means that components

should fail first and that solder joints should be designed to survive past the functional life of the system.

Over the last 30 years, solder joint performance has been influenced by technology trends:

- The demand for smaller parts and systems has led to finer pitch and smaller size solder joints, which may experience higher stresses than joints of conventional through-hole and first generation surface-mount assemblies.
- Integrated circuit (IC) packages have seen their silicon contents increase, reducing the effective coefficient of thermal expansion of packages and exacerbating the thermal expansion mismatch between board or substrate and components.
- The advent of portable electronics has called for improved drop performance while high-power ICs have raised thermal loads in computationally intensive applications and harsh environments. An example of more demanding use conditions is that of automotive on-engine assemblies that experience temperatures as high as 150 to 175°C.
- The transition from tin-lead to lead-free assemblies, with solder alloys having higher melting points than conventional eutectic tin-lead, has led to the introduction of new package and board materials whose impact on assembly reliability is not well established. Mixed alloys (lead-free paste mixed with lead-free balls of a different composition) have led to an infinity of possible solder alloy compositions, very few of which are characterized as well as tin-lead was.

Safety margins have been greatly reduced since the days of all through-hole assemblies. A proactive approach is thus needed to ensure that soldered assemblies meet product reliability goals. Once reliability goals are agreed upon by interested parties throughout the supply chain,

demonstrating the reliability of a circuit board assembly necessitates that proper resources be allocated to conduct adequate reliability testing and modeling.

Solder joint field failures fall into two grand categories or a combination of both:

- Infant mortality failures—these are often due to poor soldering quality such as insufficient solder, poor wetting or excessive offset of components with respect to mounting pads. Meeting workmanship requirements does not imply that field reliability goals are met. For example, Class III, “high-reliability” products that meet the most demanding workmanship requirements have failed in the field. Workmanship standards set criteria to achieve a certain level of soldering quality. They are not based on reliability test data.
- Wear-out failures that occur prematurely due to excessive stresses that could have been anticipated had design-for-reliability studies been performed. For example, leaded packages with a low expansion lead-frame (e.g., Alloy 42 instead of copper) add local stresses due to the local thermal expansion mismatch between solder and the lead foot. These stresses, combined with shear stresses due to the global in-plane expansion mismatch between the board and the component, can be detrimental to solder joint reliability and need to be considered when assessing product reliability. Another example is that of pure creep failures that occur under constant load, a violation of an old rule-of-thumb—learned from experienced engineers from the through-hole assembly era—which states that solder joints should not be subjected to static mechanical loads.

Soldering quality remains a prerequisite to long-term reliability and is best achieved by following industry standards and best soldering practices. This is addressed in

other chapters of this handbook and IPC standards (e.g., J-STD-001). The present chapter focuses on design-for-reliability rules that help build-in reliability at the design stage. Established rules-of-thumb and simple algebraic equations are given that enable physical designers to make quick decisions and rational choices in the early stages of board design. These rules and guidelines apply to both tin-lead and lead-free assemblies. Lead-free failures that have been brought to the author's attention occurred on similar components and under similar circumstances as for field failures of tin-lead assemblies. Chapters 62 and 64 cover test and modeling techniques that are of use to quantify and prove in the reliability of soldered circuit boards and packages.

63.2 RELIABILITY DEFINITION AND GOALS

The standard definition of reliability, as applied to solder joints, is that of industry associations (e.g., IPC-SM785, IPC/JEDEC 9701):

> "Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels."

The above definition is well accepted in courts of law during litigation proceedings involving solder joint failures in electronic products that have ceased performing properly. Three items are highlighted in the above definition:

- "*Given conditions*" refers to the spectrum of loads—thermal, mechanical and/or electrical—that the product is expected to sustain in use. This includes one-time or

cumulative stresses that the products will experience during shipping and handling and under field use conditions.

- The "*specified period of time*" is the target design life, for example, a 3- to 5-year life for laptop or desktop computers, 100,000 miles or 10 years of life for an automobile.
- "*Acceptable failure levels*" refers to the fraction-failed or percentage of failures that should not be exceeded at the end of life, for example, no failures at 40 years in some aerospace, medical, or solar panel applications, less than 0.01 percent cumulative failures at 15 to 20 years in telecommunication network applications, etc.

Reliability goals are set based on end-user requirements or customers' expectations. Design-for-reliability requires an upfront investment of time and resources, and a commitment to meet reliability goals. How to achieve these goals is the responsibility of the product management team, preferably with buy-in and input from the entire supply chain. Solder joints being the interface between board and components, both board and component characteristics have an impact on solder joint life. Reliability is best achieved through a team effort involving equipment manufacturers, suppliers, and assemblers.

63.3 WHY DO SOLDER JOINTS FAIL?

Both standard SnPb and lead-free solder joints have failed in the field. Unfortunately, field failures are not talked about much in the public domain and the history of SnPb failures is bound to repeat itself with lead-free or mixed assemblies. Most failures can be attributed to poor initial solder joint quality and/or an oversight of use conditions or basic design-

for-reliability practices. A few examples of failures investigated by the author and some of his consulting colleagues are discussed briefly in this section.

Through-hole solder joints have failed under numerous circumstances, especially under harsh conditions such as in automotive under-the-hood or on-engine units. Some of these failures, which are easily observed on the solder side of through-hole assemblies, are illustrated by photographs posted by repair shops on the World Wide Web (e.g., under automotive forums). However, very little to no failure mode analysis is available. This author participated in a field failure investigation, where through-hole solder joint failures occurred within a short period of time (less than 1 year) in a consumer, video system subassembly. Fatigue failures occurred in substandard solder fillets that were subject to thermomechanical cyclic loads.

SnPb solder joints of Leadless Ceramic Chip Carriers (LCCC) have failed in medical implants (Engelmaier, ca. 2000), even though the LCCC parts were small, solder joints met workmanship standards and use conditions were very mild (constant, internal body temperature around 37°C). The failures were attributed to excessive thermal cycling cumulative damage that occurred in the LCCC solder joints when “traveling salesmen” carried and delivered medical implants to health-care facilities up and down the East Coast of the United States, subject to diurnal and seasonal temperature cycles in their vehicles. The lesson learned in this case is the need to account for all thermo-mechanical cycles that circuit boards may experience from the end of the assembly line to the end of the design life.

Both SnPb and lead-free leaded components with Alloy 42 lead-frames have experienced solder joint failures. Alloy 42 small outline transistor (SOT) and small outline diodes (SOD) have failed under harsh automotive conditions. Alloy 42 TSOPs have failed in use in desktop computer applications (Engelmaier, ca. 1992–2000). In addition to the global CTE

mismatch between the component body and the circuit boards, the solder joints of these devices experience large stresses and strains due the local CTE mismatch along the interface between the foot of Alloy 42 leads (CTE around 4 ppm/°C) and the solder joint alloy (CTE around 24 ppm/°C). In several of these cases, failures could have been prevented by exceeding workmanship standards. As demonstrated by Reichelt (1998), even IPC Class III requirements may not be sufficient for components with Alloy 42 leads. Instead, assembly standards may need to be tightened for some harsh environment applications, requiring zero offset and no rotation of component leads with respect to the mounting pads on circuit boards.

SnPb solder joints have also failed in the case of leaded components with copper lead-frames. Here, the local CTE mismatch is much less of a concern since copper has a CTE of about 17 ppm/°C, close enough to the CTE of tin-based solders. SnPb solder joints of low profile Small Outline Integrated Circuit (SOIC) failed in a computer application within 1 year of use. Failure analysis showed coarsening of the SnPb microstructure, a strong indication of thermal cycling creep-fatigue failures. While the lead-frames were made of copper, the low-profile components had rather short leads that may not have been compliant enough to absorb cyclic shear strains driven by the board-to-component global CTE mismatch. Lesson learned: in the case of low-profile leaded components, estimate or measure leads stiffness as well as board and component in-plane CTEs to make sure that the leads are compliant enough to handle solder joint cyclic strains due to global CTE mismatches (Kotlowitz, 1989).

SnPb failures have occurred by pure creep rupture in through-hole assemblies with insufficient solder filling—in spite of meeting workmanship requirements—or due to excessive static loads. The rule-of-thumb (original source unknown) still holds that soft solder joints are not load-

carrying members. Thus, they should not be subjected to constant, static loads, especially by design.

No component is immune to solder joint failures when reliability is not built-in at the design stage or when use conditions are not accounted for properly. Assembly standards may provide an agreed upon level of quality but do not warranty that solder joint reliability requirements are met. The latter are application dependent and are unique to each and every product. Exceeding industry's standard workmanship requirements may be needed in some applications.

63.4 MAIN EFFECTS AND BASIC RULES-OF-THUMB

63.4.1 Under Thermal or Power Cycling Conditions

Under thermal cycling conditions, the in-plane thermal expansion between board and components results in cyclic shear deformations of the joints. Referring to Fig. 63.1, the outermost critical joints are sheared by an angle γ. If the board and component are infinitely stiff, or if stress relaxation in the soft solder joints is complete, the maximum cyclic shear angle (or strain) is approximated as

$$\Delta\gamma_{MAX} = \frac{L \cdot \left|\alpha_B - \alpha_C\right| \cdot \Delta T}{h_S} \qquad (63.1a)$$

where L is the distance to neutral point (DNP) or distance from the component center to the most critical joint, h_S is the component stand-off height or solder joint thickness

between the board and component pads, a_C and a_B are the in-plane coefficients of thermal expansion (CTEs) on the component bottom side and on the top side of the board, respectively. D*T* is the temperature swing between the cold and hot sides of the thermal cycle.

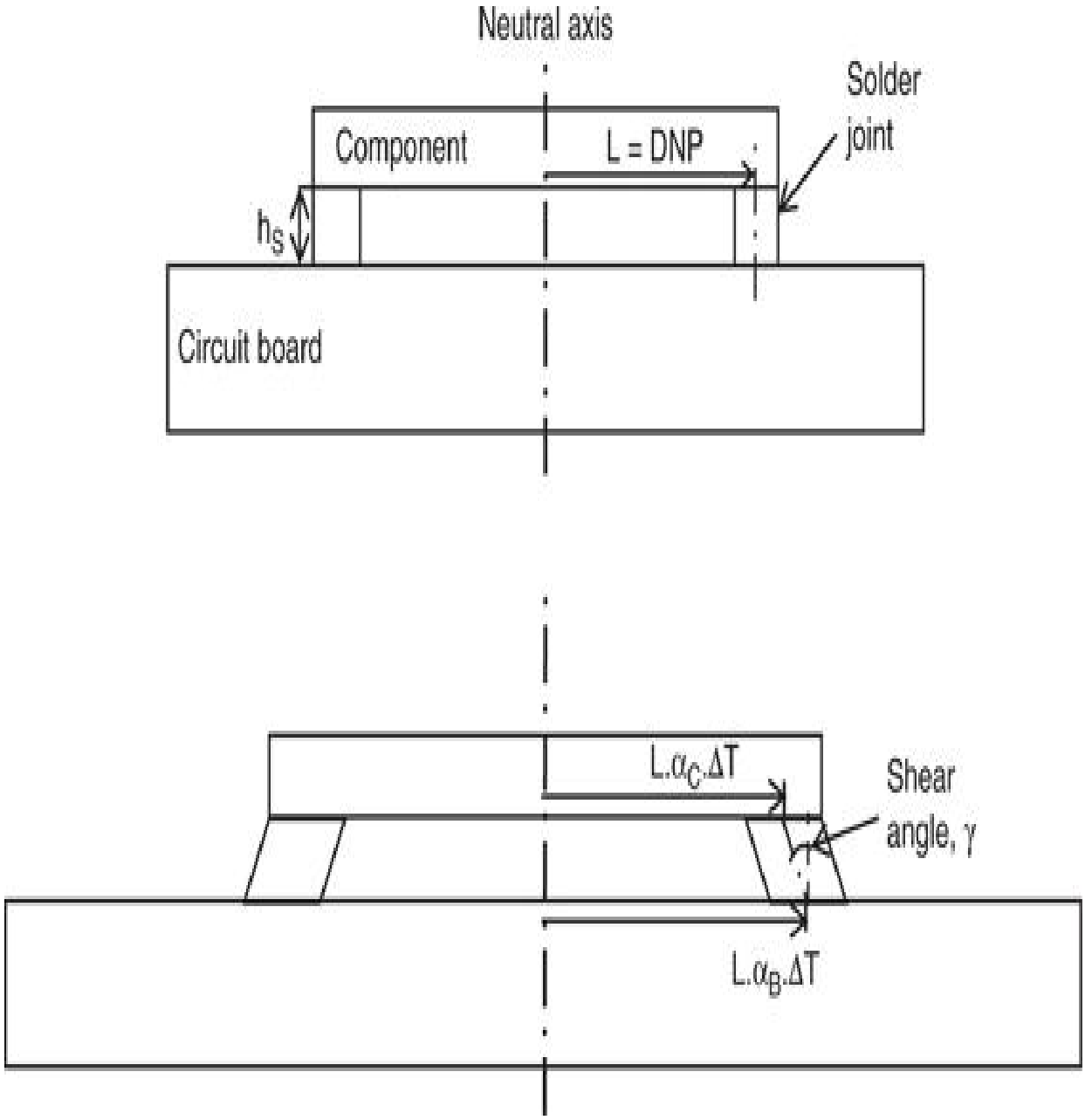


FIGURE 63.1 Solder joints under shear due to the difference in the in-plane thermal expansion of the board and component during thermal or power cycling. The amount of shear is given by the shear angle γ.

Example: Consider a ceramic ball grid array (CBGA) with a CTE of 6 ppm/°C and a 20 × 20 array of solder joints (1 mm pitch) mounted on a circuit board with an in-plane CTE of 18 ppm/°C. The component stand-off height is 20 mils or 0.508 mm.

The maximum DNP at a corner joint is L = 10 * 1 mm * √2 = 14.142 mm. For a temperature swing DT = 30°C, the maximum cyclic shear strain is

$$\Delta\gamma_{MAX} = \frac{14.142 \cdot (18 \cdot 10^{-6} - 6 \cdot 10^{-6}) \cdot 30}{0.508} = 0.01 = 1\% \qquad (63.1b)$$

Shear strains or angles, as given by Eq. (63.1a), are dimensionless or in angular radians. The 1 percent shear strain in the above example corresponds to a shear angle of 180° * 0.01/p = 0.57°. This may seem like a small angle of shear but, under repeated cyclic loading, these small angles of deformation have a cumulative effect due to the permanent set that is induced in the solder joints by plastic flow and creep of the soft solder alloy. The 1 percent shear strain is considered high and would raise a flag about the long-term reliability of these corner joints. The 1 percent level is not an absolute threshold, it simply suggests that the reliability of those solder joints has to be investigated more in depth. For example, if the solder attach or pad area is large enough, then the solder joints have a sufficiently large load bearing area to reduce shear stresses and to provide for extended crack propagation times.

Solder joints that are subjected to thermal cycling fail in low cycle fatigue, that is, they fail in a few hundred to a few thousand cycles. The actual failure mechanism is a combination of creep and cyclic fatigue. As a first order approximation, the number of cycles to failure, N_f, follows a Coffin-Manson relationship with an exponent m in the approximate range 1 to 2:

$$N_f \propto 1/\left(\Delta\gamma_{MAX}\right)^m \qquad (63.2)$$

Equations (63.1a) and (63.2) suggest four different ways to increase the life of solder joint attachments under thermal cycling conditions:

- Keep the component and/or die size as small as can be.
- Minimize the board to component CTE mismatch, $\Delta\alpha = |\alpha_B - \alpha_C|$.
- Increase the component stand-off height, h_S.
- Reduce the maximum allowed temperature swing, ΔT, and do not allow it to increase over time using reliable cooling techniques.

The above rules-of-thumb apply regardless of the solder alloy composition, tin-lead or lead free. The CTE mismatch effect is very strong as can be seen in Fig. 63.2 for two different types of component, a leadless ceramic chip carrier (LCCC) with a CTE of 5.4 ppm/°C (Sherry and Hall, 1986) and a chip scale package (CSP) with a CTE of 8.6 ppm/°C (Choi et al., 1998). LCCCs were mounted on circuit boards with in-plane CTEs in the range 9 to 21 ppm/°C. The CSPs were assembled on circuit boards with in-plane CTEs in the range 13.4 to 17.3 ppm/°C. In the latter case, when the board CTE increases from 13.4 to 17.3 ppm/°C (a change of about 4 ppm/°C), solder joint life decreases from 2000 to 500 cycles, that is, by a multiplicative factor of four times. Clearly, solder joint life is highly impacted by the board-to-component CTE mismatch and it is of utmost importance to control, measure and/or predict board and component CTEs accurately.

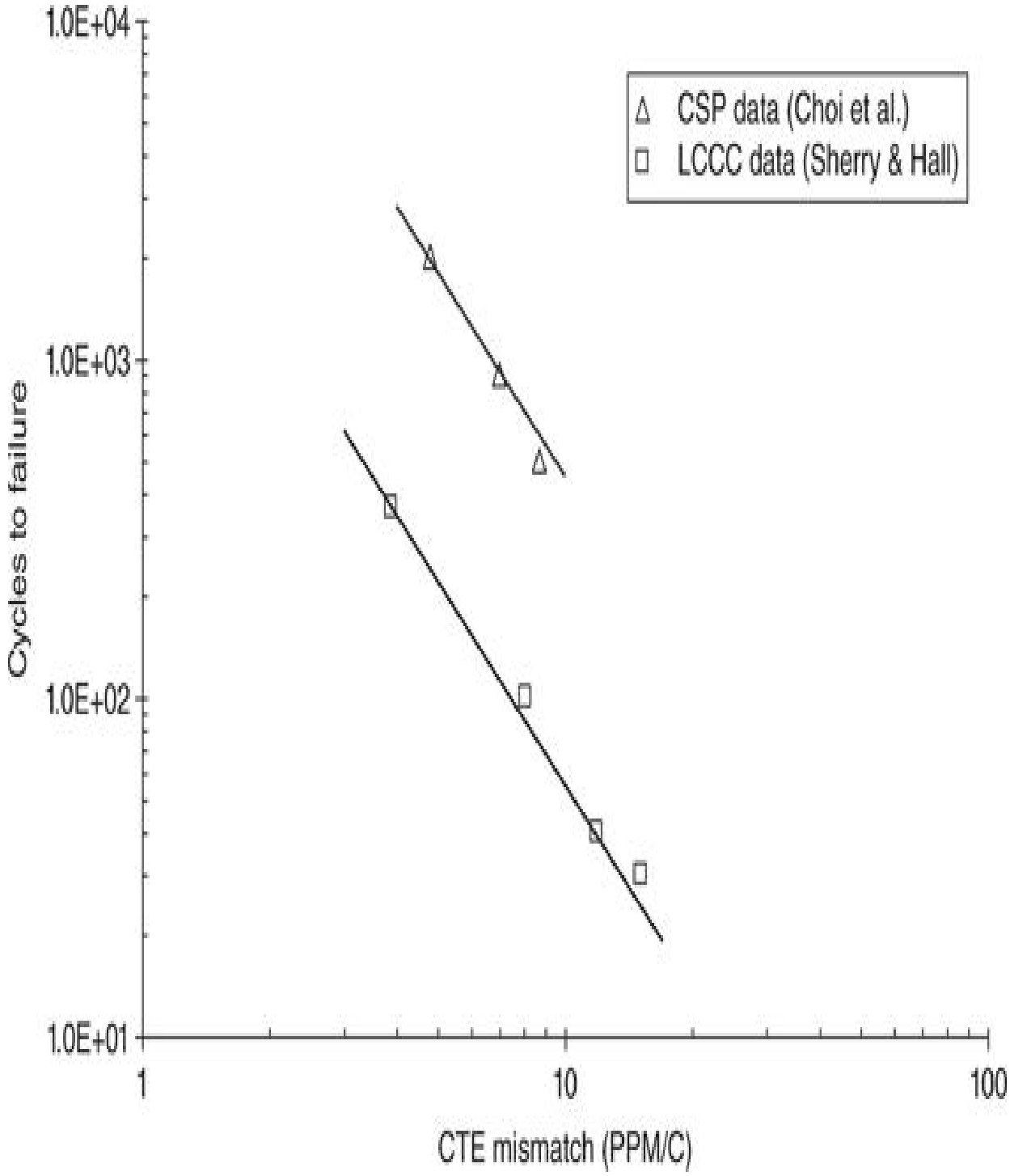


FIGURE 63.2 Log-log plot of cycles-to-failure (median or characteristic life) versus CTE mismatch for two component types mounted on double-sided rigid boards. The slope of the best-fit lines that have been forced through each dataset is exactly −2. The goodness of fit suggests that the Coffin-Manson relationship [Eq. (63.2)] captures the CTE mismatch effect well.

Another significant loading mechanism takes place in single-sided assemblies whereby the assembly bends due to the bimetallic strip effect (Fig. 63.3). The solder joints resist the expansion mismatch between the board and component, creating shear forces and moments at the board and component interfaces with the solder joints. These forces and moments force the assembly to bend as illustrated in Fig. 63.3. Thus, the shear strain in solder joints has two components: ϕ due to simple, in-plane shear, as previously discussed, and θ due to bending of the assembly. These two changes in the corner angle of the idealized solder joint of Figs. 63.1 and 63.3 ($\angle ABC = 90°$) go in opposite directions. Thus, bending of the assembly by bimetallic strip effect relieves stresses and strains in the solder joints. The bending of single-sided assemblies during thermal cycling was first characterized experimentally by Hall (1984). This stress relief mechanism is the main reason why single-sided, thinner board assemblies lead to longer solder joint life than thicker board assemblies. Any other means of reducing the flexural stiffness of boards, such as the use of more compliant laminate materials, will enhance the ability of the board to flex and improve solder joint reliability under thermal cycling conditions. Opposite requirements apply under mechanical loading conditions. Last, the ability of the assembly to flex in the component area is suppressed in mirrored, double-sided assemblies with components mounted back to back or with a slight offset of components on the top and bottom side of the board. The resulting decrease in solder joint life can be by a multiplicative factor of two to three times.

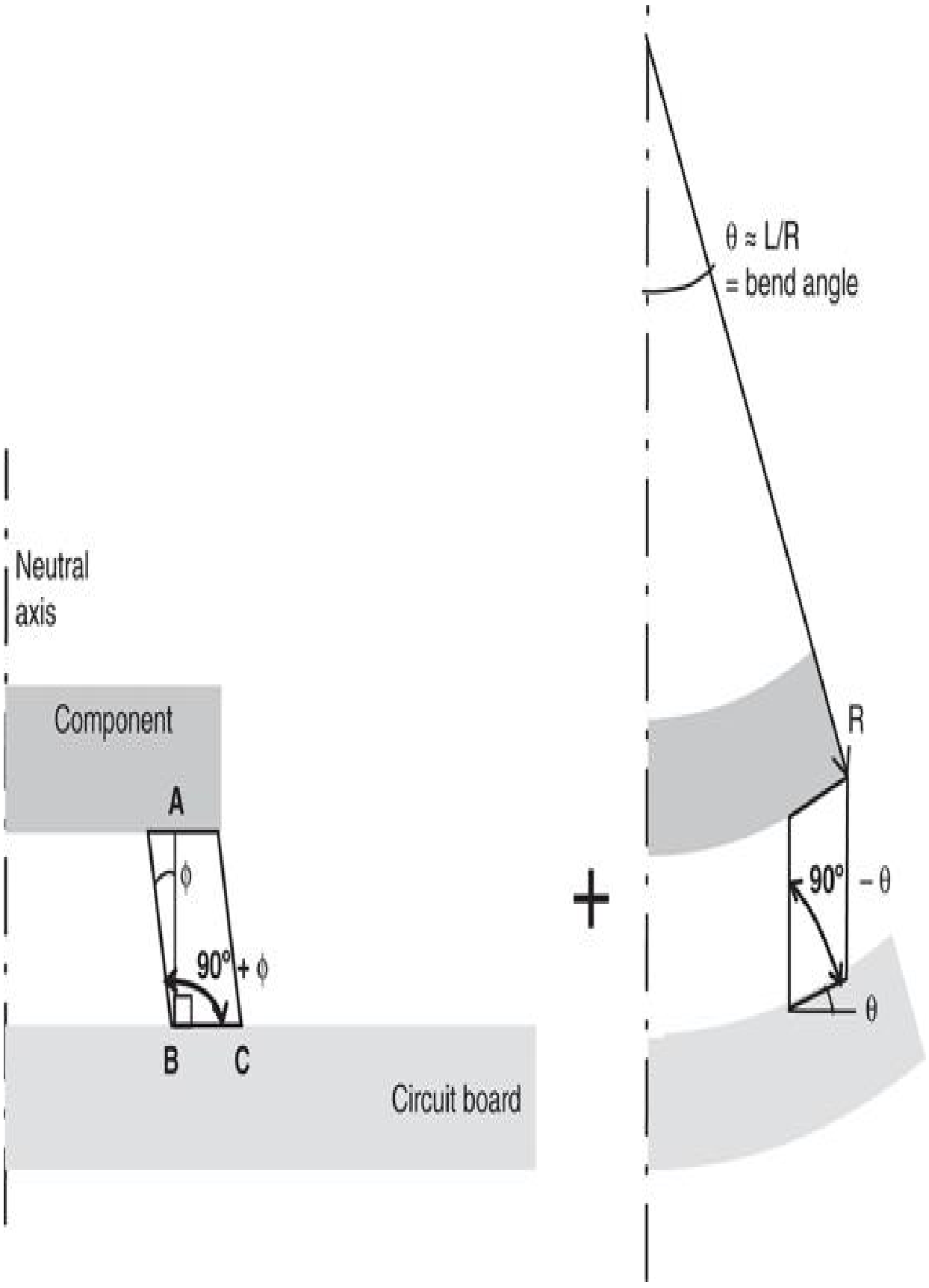

θ ≈ L/R
= bend angle
Neutral
axis
Component
A
ϕ
90° + ϕ
B
C
Circuit board
+
R
90° − θ
θ

FIGURE 63.3 Under thermal cycling conditions, bending relieves shear stresses and strains in solder joints of single-sided assemblies. In addition to in-plane shear (angle ϕ in drawing to the left), the solder joint is sheared due to bending of the assembly (angle θ in drawing to the right) by bimetallic strip effect. The resulting shear strain, or angle, is $\gamma = \phi - \theta$.

Industry standards for reliability assessment of surface-mount assemblies under thermal or power cycling conditions include IPC-SM-785 and IPC-9701.

63.4.2 Under Mechanical Loading Conditions

Under out-of-plane mechanical loading conditions (bend, drop, shock, vibration), solder joints are stretched (or compressed) in the *z* direction, perpendicular to the mid-plane of the board (Fig. 63.4). In a bend test or under vibration, the board flexes up or down at a rapid rate and the solder joints fail in high cycle fatigue (i.e., in tens of thousands to millions of cycles).

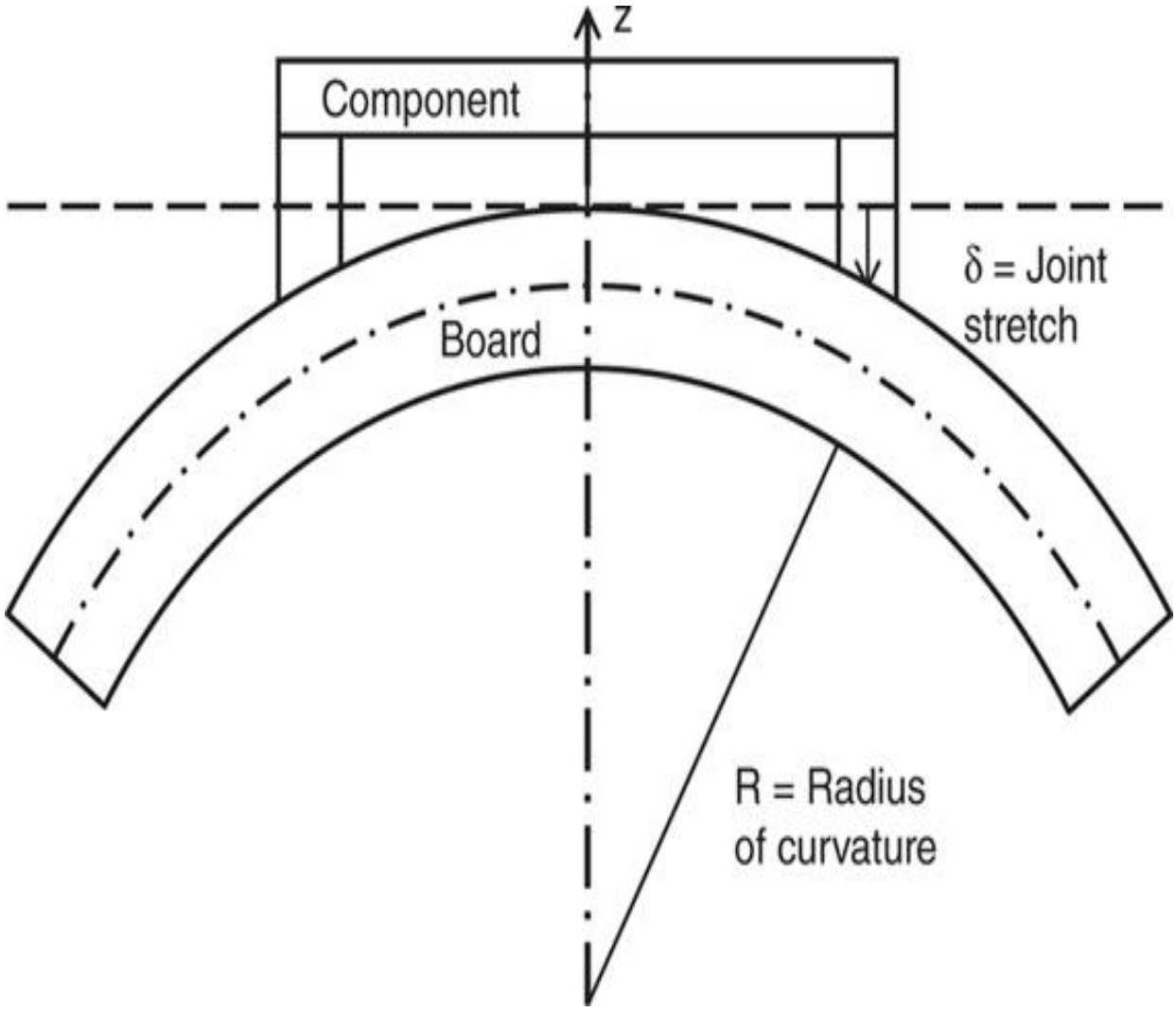
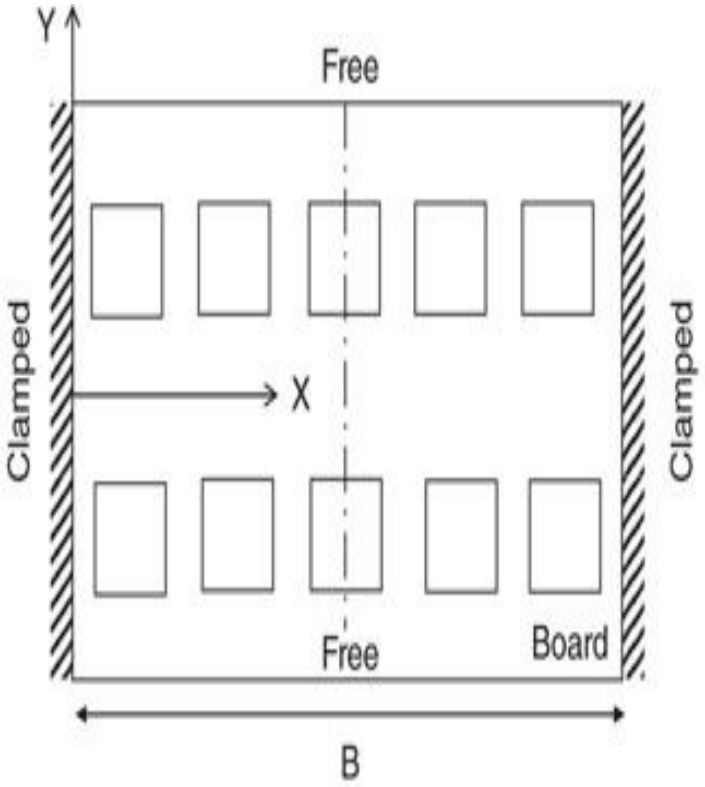


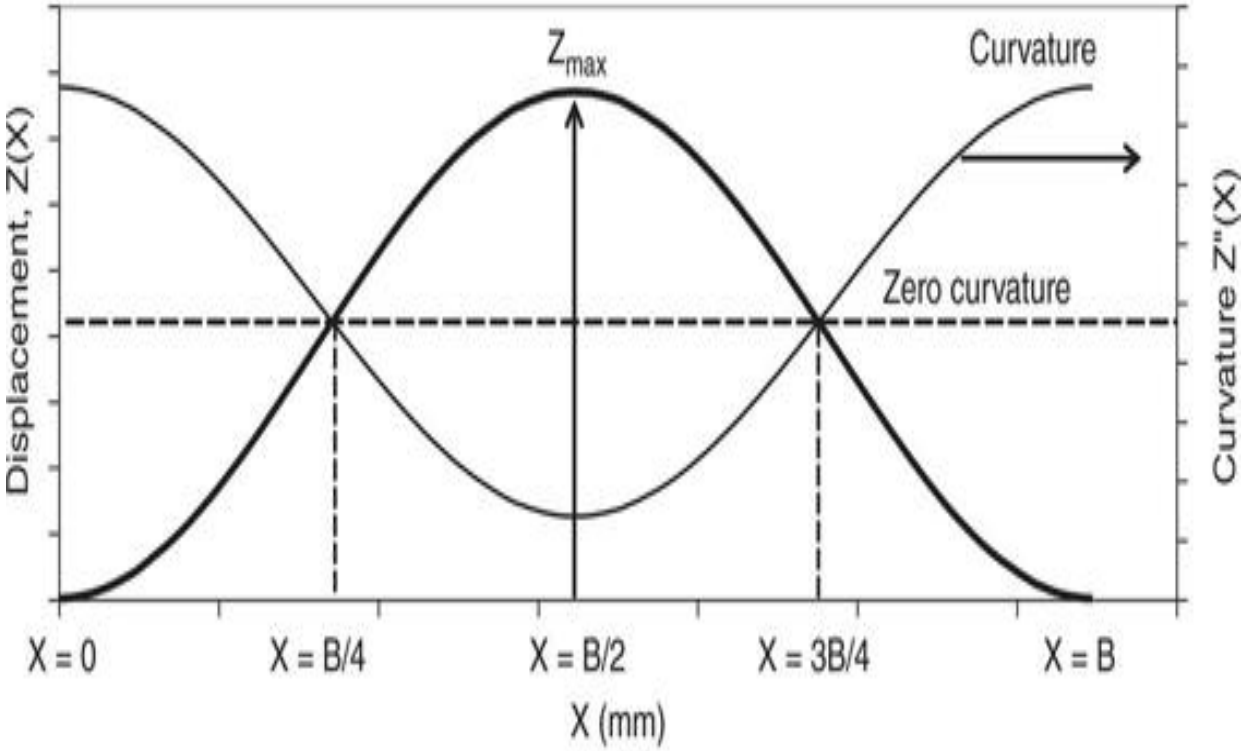
FIGURE 63.4 Under bend, drop, or vibration loading in a direction perpendicular to the board, out-of-plane flexure is the main deformation mode of the board. Outer-row solder joints are stretched (or compressed) due to board curvature. The amount of tensile stretch in the joints is given by the relative deflection of the board, δ.

Out-of-plane flexure can be minimized by “clamping” or stiffening the board. “Clamping” can be achieved by securing the board to the product’s chassis, frame, or housing using wedge-clamps or other fixation means such as screws. Stiffening of the board is by means of rigid, stiffening ribs that are bonded, bolted down or riveted to the board in the direction that is at the intersection of the mid-plane of the board with the plane of maximum bending or curvature

(*x* axis in Fig. 63.5*a*). In the example of Fig. 63.5*a* (board with two free edges and two clamped edges), out-of-plane deformations can be further reduced by using stiffening ribs that go from one clamped edge to the other. Ribs that would be mounted parallel to the *y* direction of the board would be ineffective and make things worse because the added mass of the rib(s) would lower the resonance frequency of the board and amplify out-of-plane deflections.


Y
Free
Clamped
X
Clamped
Free
Board
B

(a)


Z_{max}
Curvature
Zero curvature
Displacement, Z(X)
Curvature Z"(X)
X = 0
X = B/4
X = B/2
X = 3B/4
X = B
X (mm)

(b)

FIGURE 63.5 (*a*) Example of boundary conditions for a circuit board subjected to out-of-plane vibrations. The left and right edges are clamped, the two other edges are free. Components are shown as squares. (*b*) First mode shape (thick solid line) and curvature (thin solid line) of board in Fig. 63.5*a*.

Figure 63.5*b* shows the board deflection profile [first mode shape, $Z(X)$] as well as the curvature plot for the board in Fig. 63.5*a*.

The first mode shape is approximated as

$$Z(X) = Z_{MAX} \cdot \left[1 - \cos\left(2\pi \frac{X}{B}\right)\right] \tag{63.3a}$$

where B is the length of the board in between the two opposite clamps. The corresponding curvature is

$$Z''(X) = Z_{MAX} \cdot \left(\frac{2\pi}{B}\right)^2 \cdot \cos\left(2\pi \frac{X}{B}\right) \tag{63.3b}$$

The maximum out-of-plane deflection is in the center area of the board. As importantly, curvature is the largest, in absolute values, at the center of the board but also near the clamped edges of the board. Since curvature of the board is what stretches (or compresses) solder joints, first solder joint failures are as likely to occur in the center area of the board as near the clamped edges (left- or right-side components in Fig. 63.5*a*). This has been verified experimentally in the NASA-JGPP lead-free solder project (Woodrow, 2005). Thus, large critical components should not be mounted near the center of the board or near clamped edges. As can be seen in Fig. 63.5*b*, the ideal location where to mount critical components is one-fourth of the way along the length of the board (at positions $X = B/4$ or $X = 3B/4$) since, at these locations, the board curvature is nil.

The resonance or natural frequency, f_n, of a flat board goes as

$$f_n \propto \sqrt{\frac{D_B}{\rho_B}} \tag{63.4}$$

where ρ_B is the mass per unit area of the assembled board and D_B is its flexural rigidity:

$$D_B = \frac{E_B \cdot h_B^3}{12(1-\upsilon_B^2)} \tag{63.5}$$

E_B is the effective Young's modulus of the board, n_B is its Poisson's ratio and h_B is the board thickness.

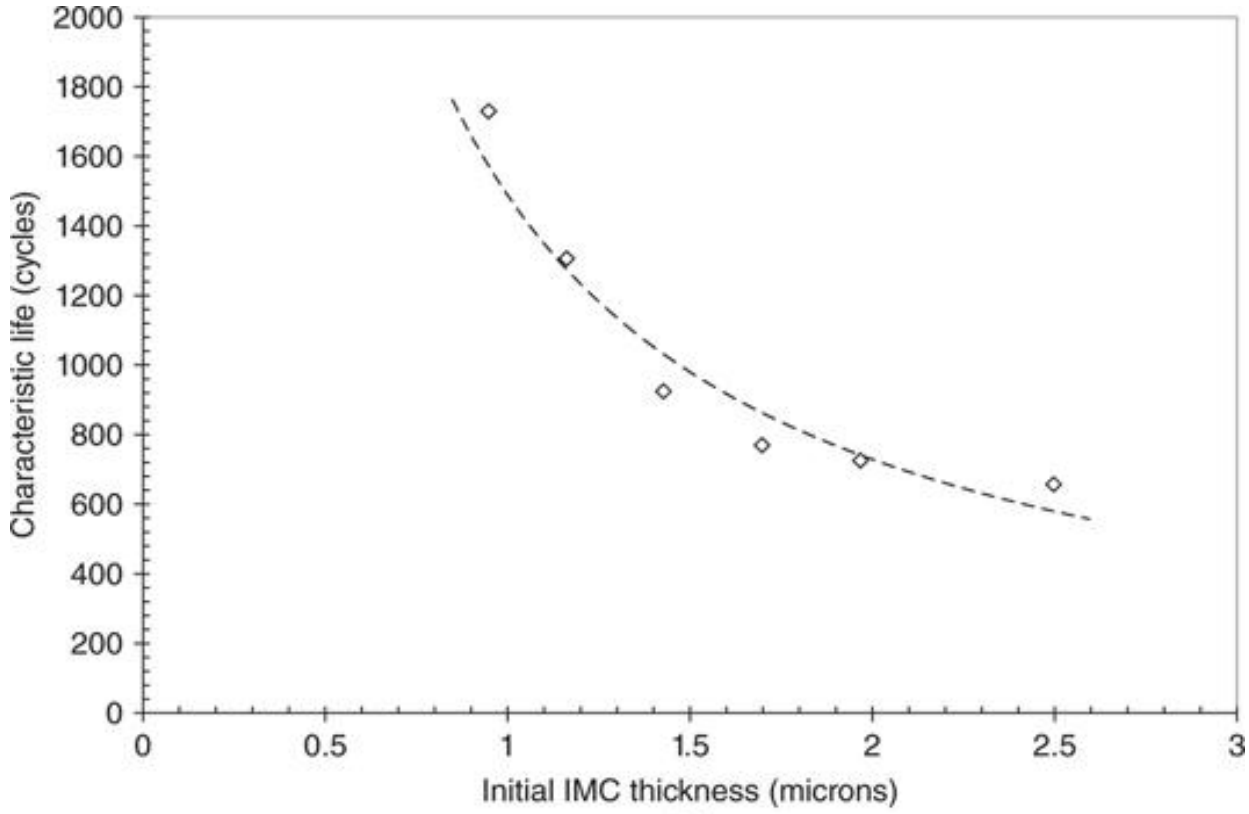
Since dynamic displacements at the center of the board go as G_{out}/f_n^2 (Steinberg, 2000), where G_{out} is the output acceleration ($G_{out} = Q.G_{in}$, where G_{in} is the input acceleration and $Q \sim \sqrt{f_n}$ is the board transmissibility), board and solder joint strains can be reduced by increasing the minimum resonance frequency of the board. Equations (63.4) and (63.5) thus suggest several ways to improve solder joint life under shock and vibration conditions, namely, by increasing the board stiffness—using a thicker board or stiffer laminate materials—or by reducing the board mass per unit area. Steinberg (2000) offers a wider spectrum of design guidelines to improve board assembly reliability under shock, drop, and vibration conditions. The majority of these generic guidelines apply regardless of solder composition, tin-lead or lead free.

Industry standards for reliability testing under mechanical loading conditions include JEDEC/JESD22-B111 (drop test),

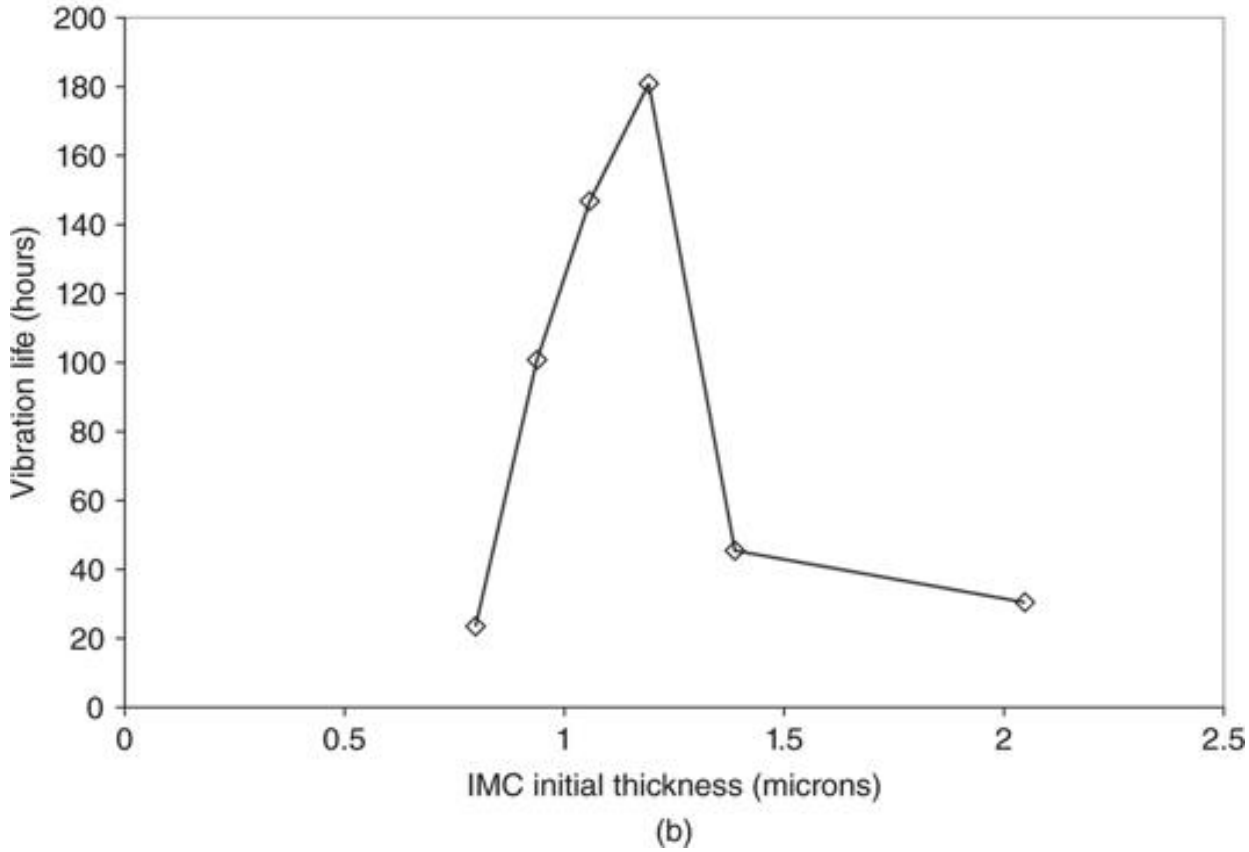
JEDEC/JESD22-B113 (bend test), IPC-JEDEC-9707 (spherical bend test), MIL-STD-810G (environmental/vibration testing).

63.4.3 Process and Intermetallic Thickness Effect

While design parameters and material properties have a significant impact on solder joint reliability, process deviations from standard reflow temperature profiles also affect solder joint life. Figure 63.6*a*, *b* shows solder joint life in terms of characteristic life under thermal cycling conditions and life in hours under vibration testing versus the initial intermetallic compound (IMC) thickness for two different components (1206 resistor in Fig. 63.6*a*, mBGA component in Fig. 63.6*b*). The data has been plotted from tabulated test results by Tu et al., 1997 and 2001. The initial IMC thickness depends on the soldering temperature profile and the time above liquidus. The trends are device specific and should not be applied to other devices without caution. Nevertheless, the test data from Tu et al. clearly indicate that the effect of intermetallic thickness is significant. The life trend in Fig. 63.6*a* is an inverse relationship with the characteristic life decreasing by more than two times when the initial IMC thickness changes from 1 to 2.5 μm. The vibration data in Fig. 63.6*b* does not follow a monotonous trend and suggests a possible, optimal IMC thickness for improved reliability under mechanical loading conditions.


Characteristic life (cycles)
2000
1800
1600
1400
1200
1000
800
600
400
200
0
0
0.5
1
1.5
2
2.5
3
Initial IMC thickness (microns)

(a)


Vibration life (hours)
200
180
160
140
120
100
80
60
40
20
0
0
0.5
1
1.5
2
2.5
IMC initial thickness (microns)

(b)

FIGURE 63.6 (*a*) Effect of initial intermetallic thickness on thermal cycling life of 1206 resistor solder joints on FR-4 board (SnPb assembly). Data points are from Table I in Tu et al., 1997. (*b*) Effect of initial intermetallic thickness on vibration life of BGA solder joints on FR-4 board (SnPb assembly). Data points are from Tables I and II in Tu et al., 2001.

Soldering or reflow profiles are standardized for yield purposes. The data of Fig. 63.6*a*, *b* suggest that the product management team should monitor assembly profiles closely since deviations from standard conditions can have a large impact on IMC thickness and, thus, on solder joint reliability. This should not be an issue when communication channels are established whereby assemblers at a given site or at a different manufacturing location keep interested parties updated on current assembly conditions.

63.5 PARAMETERS THAT AFFECT SOLDER JOINT RELIABILITY UNDER THERMAL CYCLING CONDITIONS

A large number of solder joint failures occur under thermal or power cycling conditions. Figure 63.7 gives a list of 14 parameters that affect solder joint life under such conditions. Not shown in Fig. 63.7, but also significant, are the pitch of the assembly, P, and the board pad and component terminal finishes. Besides in-plane CTEs of boards and components, other properties that matter are Young's moduli in flexure and in tension as well as Poisson's ratios. Important geometric parameters that affect solder joint life, other than the critical DNP of the component and the solder joint thickness, include board and component thickness and the solder joint load bearing or crack area, A. The latter is typically determined by the component solder attach area or the diameter of the solderable pad area on the component side. For multilayer components such as BGA type

components with a substrate, die attach layer and a molding compound cap, the thickness, and basic mechanical properties (CTEs, moduli and Poisson's ratio) of each material layer also affect solder joint reliability. The reasons why all of these parameters matter and affect solder joint life are discussed below.

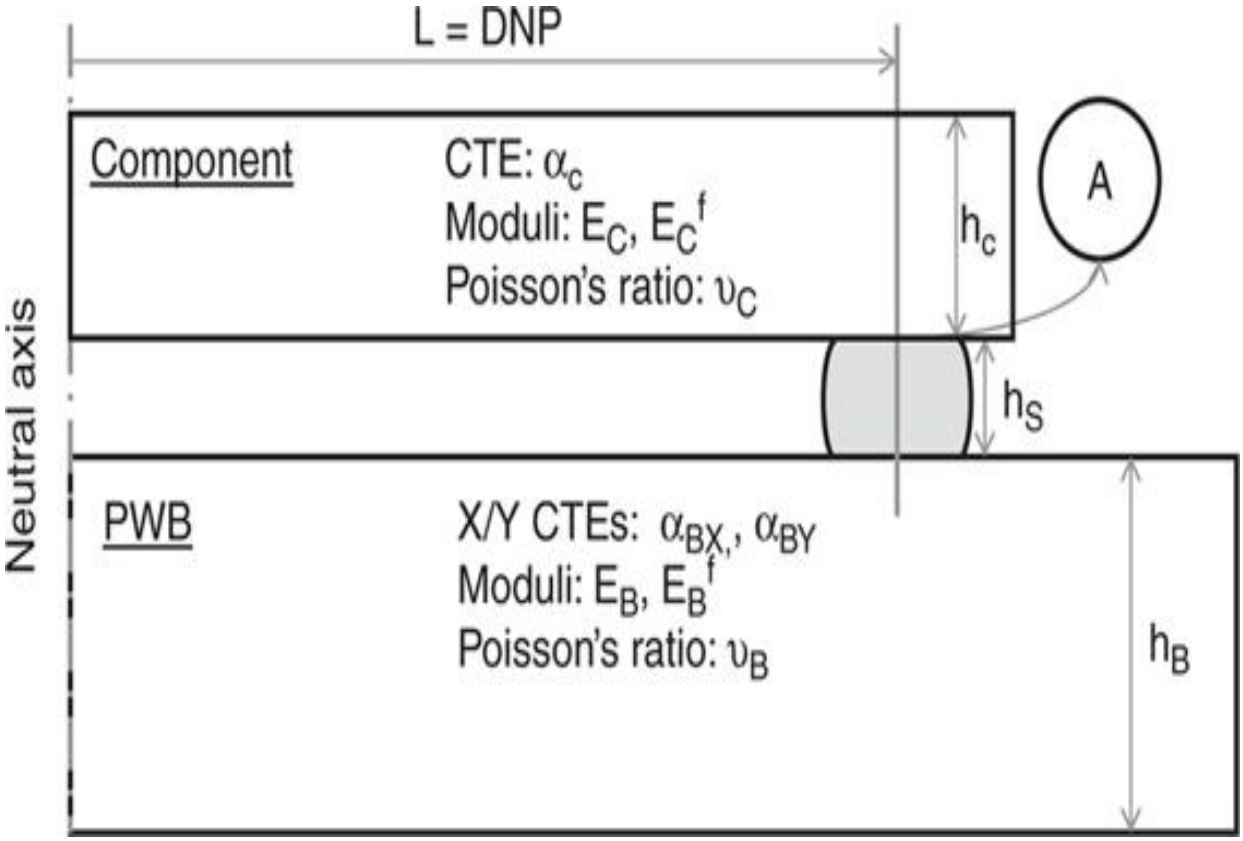


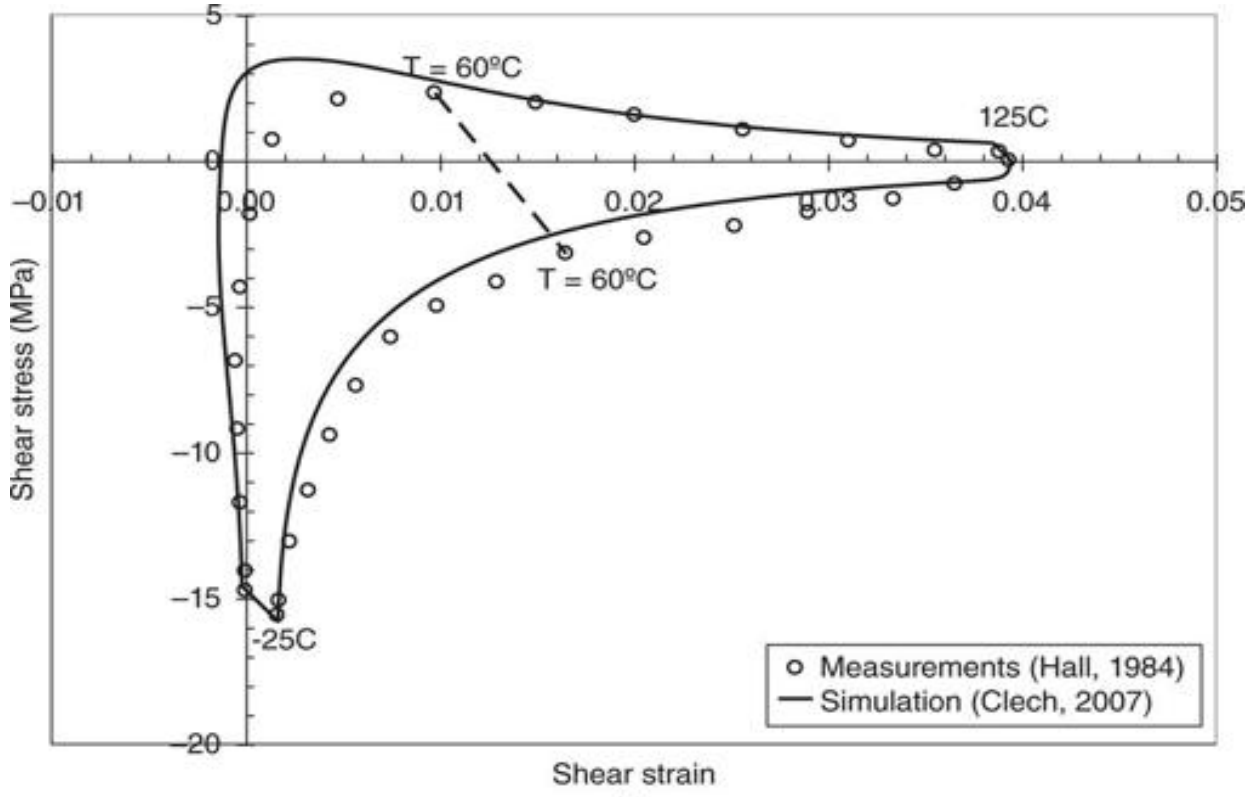
FIGURE 63.7 Schematic of assembly cross-section showing 14 parameters that affect solder joint reliability: nine board and component material properties plus five geometric parameters (assembly pitch, *P*, not included).

The above 15 parameters (pitch included) are required entries in the simulation of solder joint stress/strain hysteresis loops during thermal cycling. Examples of measured hysteresis loop data (symbols) and simulations are shown in Fig 63.8*a* for a SnPb assembly and 63.8*b* for a SnAgCu assembly (Hall, 1984, Shirazi, 2011, Clech, 2007, 2013). The solder joint stress/strain loops lay between

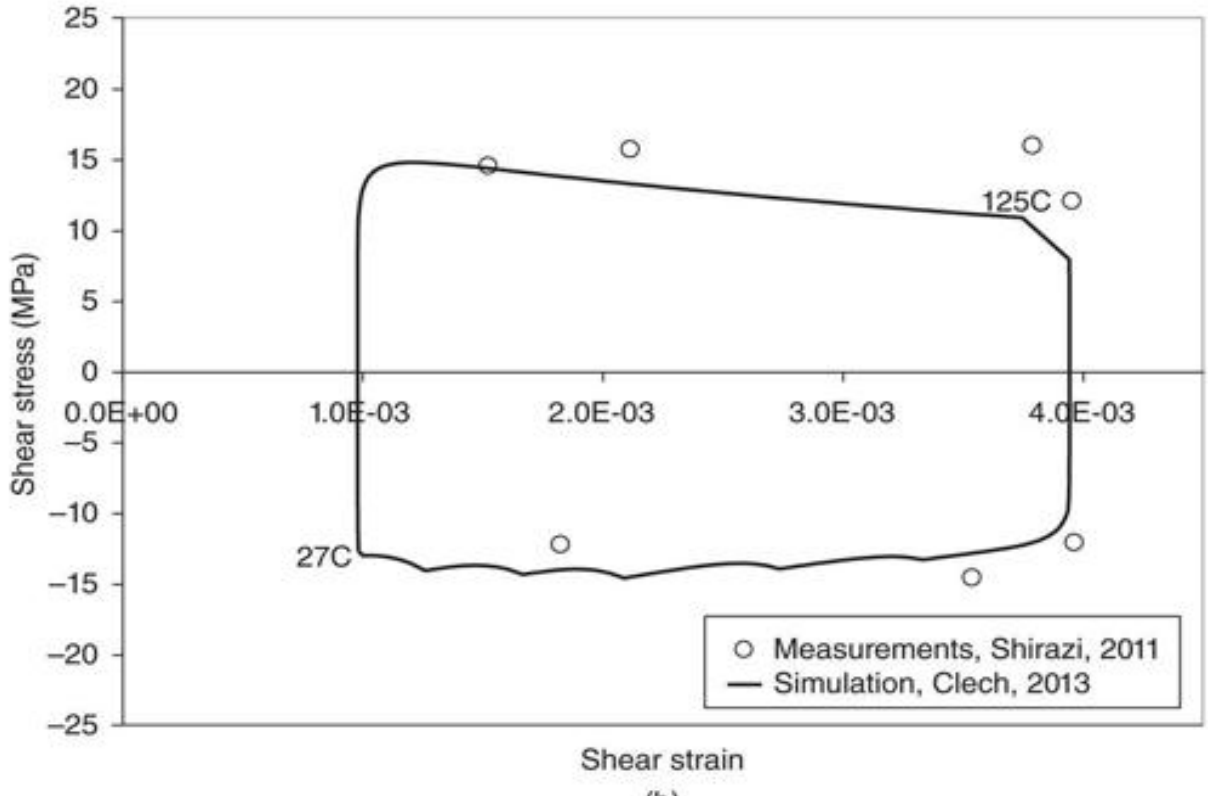
isothermal stress reduction lines of slope k at the temperature extremes T_{min} and T_{max}. The slope or stiffness parameter κ is given as

$$\kappa = Kh_S/A \tag{63.6}$$

where K is the stiffness or spring constant of the assembly. In the case of leaded packages, K is the lead flexural stiffness in the diagonal direction of the package. For leadless assemblies, K is the equivalent spring constant of three springs in series [Eqs. (18) to (23) in Clech, 1996] that account for elastic deformations of the board and component in tension and in bending as in a bimetallic strip (Hall, 1984).


5
0
−5
−10
−15
−20
−0.01
0.00
0.01
0.02
0.03
0.04
0.05
T = 60°C
125C
T = 60°C
-25C
Shear stress (MPa)
Shear strain
Measurements (Hall, 1984)
Simulation (Clech, 2007)

(a)


25
20
15
10
5
0
−5
−10
−15
−20
−25
0.0E+00
1.0E-03
2.0E-03
3.0E-03
4.0E-03
125C
27C
Shear stress (MPa)
Shear strain
Measurements, Shirazi, 2011
Simulation, Clech, 2013

(b)

FIGURE 63.8 (*a*) (after Fig. 1 in Clech, 2013): Example of measured and simulated stress/strain hysteresis loop for corner joints of SnPb LCCC assembly on FR-4. Temperature cycle is between −25 and 125°C, with 0.5°C/min ramp rates and 2 h dwell times at the temperature extremes. (*b*) SAC305 stress/strain hysteresis loops during thermal cycling. Data points (circles) are from Shirazi, 2011, and simulation (solid line) is from Fig. 12 in Clech, 2013.

For example, for single-sided leadless assemblies, the assembly stiffness K is the equivalent stiffness of three springs in series:

$$\frac{1}{K}=\frac{1}{K_1}+\frac{1}{K_2}+\frac{1}{K_3} \tag{63.7a}$$

where the spring constants are K_1 for mechanical stretching of the component, K_2 for mechanical stretching of the substrate, K_3 for bending of the assembly. The spring constants are estimated from strength of materials (Hall, 1984; Clech, 1996):

$$K_1=\frac{\mathrm{E}_C^{\iota}h_C P}{L(1-\nu_C)} \tag{63.7b}$$

$$K_2=\frac{2\mathrm{E}_B^{\iota}h_B P}{L(1-\nu_B^2)} \tag{63.7c}$$

$$K_3=(D_C+D_B)\frac{P}{LH^2} \tag{63.7d}$$

where $H=\frac{h_C}{2}+h_S+\frac{h_B}{2}$, and D_C and D_B are component and board flexural rigidity factors:

$$D_C = \frac{E_C^f h_C^3}{12(1-\nu_C)}, \; D_B = \frac{E_B^f h_B^3}{6(1-\nu_B^2)} \tag{63.7e}$$

In the above, subscripts "*C*" and "*B*" are for component and board, respectively. *P* is the assembly pitch, h_C is the component thickness, h_B is the board thickness, n_i's are Poisson's ratios, E_i^t 's are Young's moduli in tension (superscript "*t*") and E_i^f 's are Young's moduli in flexure (superscript "f"). Equations (63.7c) to (63.7e) show that the board parameters of Fig. 63.5 have a significant effect on the assembly stiffness *K* and, thus, on solder joint reliability. A different formulation of stiffness parameters applies to double-sided, mirrored assemblies (Clech, 1996), where identical components are mounted back to back on the bottom and top side of the board. Because of symmetry with respect to the mid-plane of the board, the ability of the board to bend in the component mounting area is suppressed in mirrored assemblies. This stiffens the assembly considerably and reduces solder joint life during thermal cycling.

The hysteresis loop areas give the strain energy density per cycle and represent the amount of work (per unit volume) exerted by the assembly on the solder joints. Cycles to failure, N_f, scaled for the solder joint crack area, *A*, have been found to be in an inverse relationship with strain energy density for SnPb (Clech, 1996) and SAC387/396 assemblies (Clech, 2005):

$$N_f/A = C/\Delta W \tag{63.8}$$

where *C* is a solder-dependent fatigue constant.

Thus, strain energy density is an engineering measure of solder joint damage during thermal cycling. Life predictive

correlations as were just mentioned are not widely available for newer or exotic lead-free solder compositions. However, a simplified stress/strain loop model (Clech et al., 2009) provides guidelines for designers to minimize strain energy density, that is, to maximize solder joint life based on design parameters alone, regardless of the solder joint composition. For a given assembly and thermal cycle, and assuming that stress relaxation in solder joints is complete, the strain energy density takes on a maximum value [Eq. (3) in Clech et al., 2009]:

$$\Delta W_{\max} = \kappa \cdot g_0^2 \cdot \Delta T^2 \tag{63.9}$$

where $g_0 = \dfrac{L \cdot \left|\alpha_B - \alpha_C\right|}{h_S}$ is the shear strain per degree of temperature rise.

An example application illustrating how to use the above design equations to predict the effect of board thickness—and that of the concurrent change in board CTE and Young's modulus—on solder joint reliability is given in the next section.

63.6 SIGNIFICANCE OF BOARD PARAMETER EFFECTS

63.6.1 Board Properties: T_g, CTEs, Young's Modulus

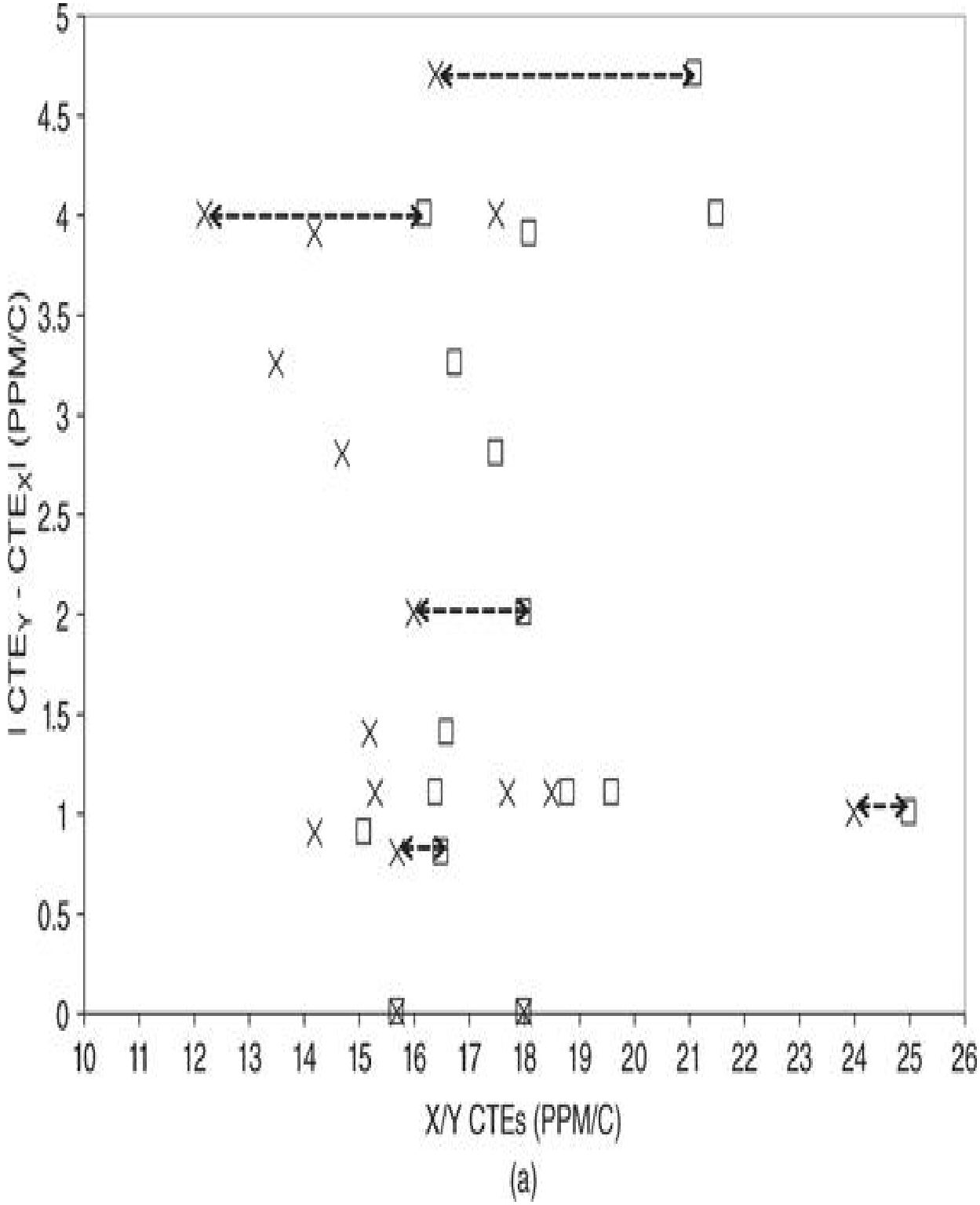
Epoxy-fiberglass boards exhibit a glass transition temperature, T_g, beyond which its moduli of elasticity drop by orders of magnitude. Typical T_g's for commercial grade FR-4 boards are in the range 110 to 150°C. As a rule,

assembled circuit boards should not operate above their glass transition temperature. This rule applies under accelerated thermal cycling conditions as well since reliability test results are more difficult, if not impossible, to interpret when test vehicles go over the glass transition temperature of the board.

Below the T_g of the board, the modulus of elasticity decreases slightly as temperature increases. At a minimum, board properties should be measured at room temperature. As discussed in the previous section, board moduli and CTEs have a strong impact on solder joint reliability. Good estimates of these properties for the product boards of interest are thus critical to solder joint reliability assessment and/or predictions. A common mistake is to use Young's modulus and CTEs provided by suppliers for thin prepregs or laminates. These prepreg or laminate properties are provided for information purposes and are not representative of product board properties. Board properties depend on glass-cloth style, epoxy contents, layer stack-up (core, prepreg, solder mask; power, ground, signals), and other board contents (filled or unfilled vias, pads) that are unique to each product board. It is thus important to measure or model board properties accurately based on the construction of representative test or product boards. For critical components, for example, a large BGAs with a large number of mounting pads and vias under the component, a component-area board coupon is preferred since in-plane CTEs can be 1 to 2 ppm/°C higher in that area compared to an area of the board that does not carry components.

Note also that, for most epoxy-fiberglass boards, CTEs may differ by a couple of ppm/°C (up to almost 5 ppm/°C) in the *x* and *y* (in-plane) directions of the board. Figure 63.9*a* shows measured *x* and *y* CTEs (horizontal axis) for a variety of test boards from the literature and the corresponding difference in *x* and *y* CTEs on the vertical axis. For a given board, *x* and *y* CTEs are represented by a pair of symbols ("×" and "□"),

some of which are connected by a dashed, double-arrowed line for illustration purposes. For example, for the pair of symbols near the top of the chart, the *x* direction CTE is close to 16 ppm/°C, whereas the *y* direction CTE on the same board is near 21 ppm/°C. The difference in *x* and *y* CTEs on the same board coupon is 4.7 ppm/°C. This may have a significant effect on the attachment reliability of rectangular components. To maximize solder joint reliability, these components should be mounted with their long axis in the direction of the board that has the lowest in-plane CTE. This simple rule applies, for example, to chip resistor and capacitors, or resistor network assemblies.


5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
| CTE$_Y$ - CTE$_X$ | (PPM/C)
X/Y CTEs (PPM/C)

(a)

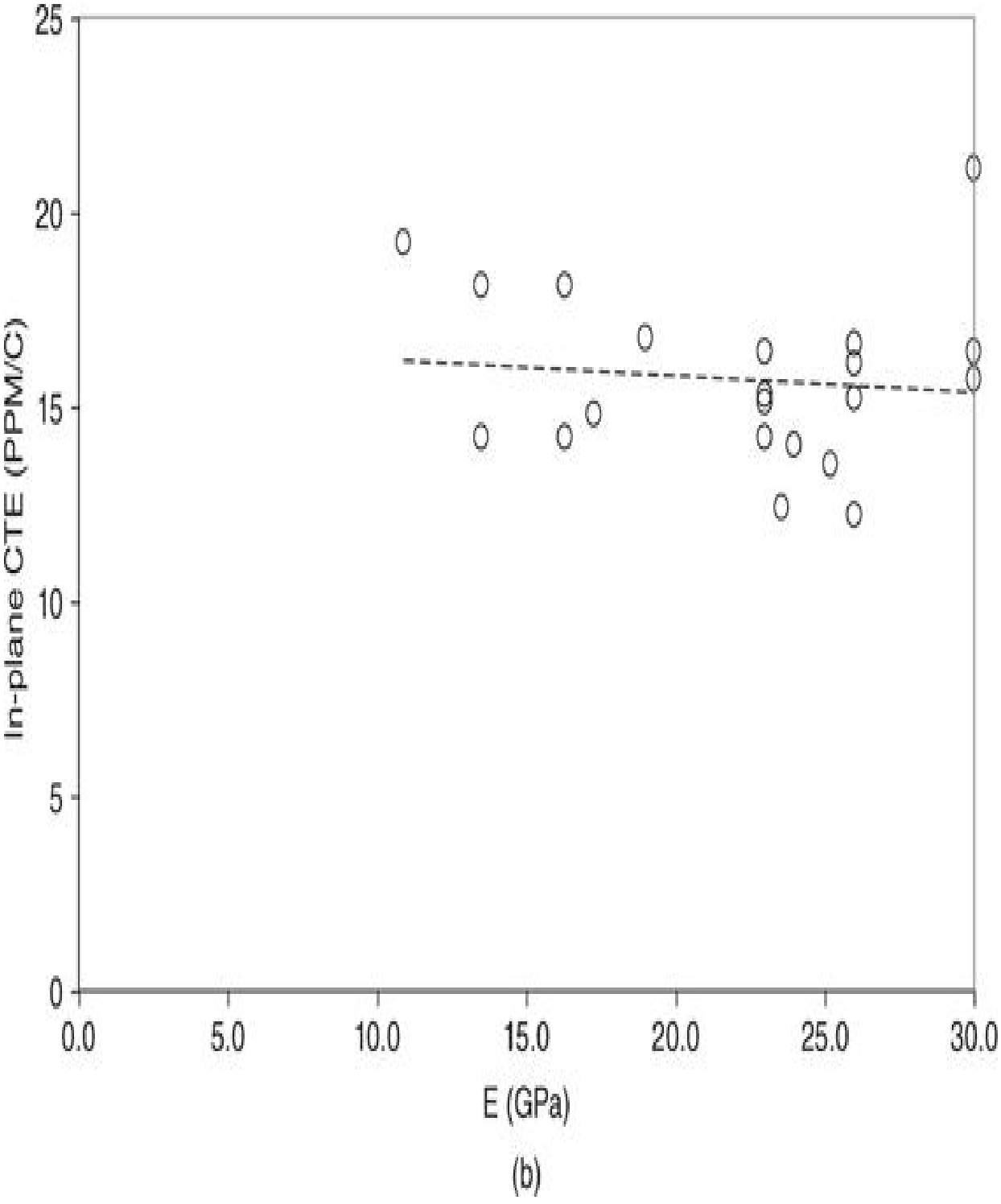


FIGURE 63.9 (*a*) Updated survey of *x* and *y* CTEs of FR-4 type test boards. *X* and *y* CTEs are represented by a pair of symbols ("×" and "□") parallel to the horizontal axis and the corresponding difference, for a given board, is along the vertical axis. (*b*) Updated survey of FR-4 test board properties: in-plane CTEs versus Young's modulus. CTEs cover the range 12 to 21 ppm/°C, Young's modulus varies from about 10 to 30 GPa.

Board CTEs and moduli are not measured in a systematic manner or it is often assumed that they follow “handbook” values. A shown in Fig. 63.9*b*, in-plane CTEs and moduli that were measured on FR-4 type boards cover a wide range of values: 12 to 21 ppm/°C for CTEs and 10 to 30 GPa for Young’s modulus. Figure 63.9*b* is an update of a survey of measured properties from throughout the literature (see Fig. 3 in Clech, 2013). Clearly, there are no “typical” values of epoxy-fiberglass board properties and the use of “handbook” or so-called “standard” values should be avoided. This is consistent with the conclusions of Ratanawilai et al. (2003) who found that in-plane CTEs measured on a variety of memory boards from one company varied from 12 to 22 ppm/ºC. The wide range of modulus and in-plane CTEs in Fig. 63.9*b* also suggests that board constructions can be tailored upfront to give them optimum properties (moduli and CTEs) that will help improve solder joint reliability.

In-plane board CTEs can be measured by means of strain gauges, thermo-mechanical analysis (TMA) or laser moiré interferometry (Han et al., 1996). Board modulus can be measured by dynamic mechanical analysis (DMA), or by use of a tensile or a three or four-point bend test specimen. Relevant industry standards include IPC-TM-650 for T_g and *x*/*y* CTEs, and ASTM-D-3039, ASTM-D-790 and ASTM-D-6272 for board moduli.

63.6.2 Board Thickness Effect

The effect of board thickness on attachment reliability under thermal cycling conditions can be large. Primavera (1999), for example, reports a life reduction of two times for chip scale packages (CSPs) on 1.575-mm-thick boards compared to identical CSPs on 0.4-mm-thin boards. It is important to keep in mind that board properties (moduli and CTEs) change with board thickness because these properties

depend on the board layer count and the relative board contents (epoxy fiberglass and copper) and their respective properties. The impact of “board thickness” on attachment reliability is the result of the synergistic effect of the board thickness itself and that of concurrent changes in board moduli and CTEs.

By combining and expanding Eqs. (63.6) to (63.9), and keeping only the terms where board thickness and properties appear, the dependence of cycles to failure, N_f, on board thickness, in-plane CTE and board moduli, as well as component properties, is given by simple design equations (Clech, 2015):

$$N_f \propto 1/(\kappa \cdot g_0^2) \propto 1/[K \cdot (\alpha_B - \alpha_C)^2] \tag{63.10a}$$

$$N_f = C_1 \cdot \frac{\left[\dfrac{1-\upsilon_C}{E_C h_C} + \dfrac{1-\upsilon_B^2}{2E_B h_B} + \dfrac{\left(\dfrac{h_B}{2} + h + \dfrac{h_C}{2}\right)^2}{\dfrac{E_{C,f} h_C^3}{12(1-\upsilon_C)} + \dfrac{E_{B,f} h_B^3}{6(1-\upsilon_B^2)}}\right]}{(\alpha_B - \alpha_C)^2} \tag{63.10b}$$

where C_1 is a constant that accounts for non-board-related factors in Eqs. (63.6) to (63.9) such as component size, stand-off height, assembly pitch and thermal conditions.

When cycles-to-failure are available for different board thickness, C_1 is obtained by plotting N_f versus the calculated ratio of algebraic terms on the right-hand side of Eq. (63.10b) (large bracket and parenthesis squared) and fitting a linear trendline with zero intercept through the data. Regardless of the constant C_1, Eq. (68.10b) is a simple algebraic equation that gives the shape of design curves for

cyclic lives versus board thickness, given known entries for the board modulus and CTE. No assumption is being made on the shape of these design curves. Instead, the board thickness dependence, and the effect of the board modulus, come straight out of the strength-of-materials formulation of the assembly stiffness, *K*.

Example: Figure 63.10 shows the fit of Eq. (63.10b) to thermal cycling characteristic lives (Shih et al., 2004) for a "hiCTE" ceramic ball grid array (CBGA) package mounted on boards of thickness 62, 93, and 130 mils. The test boards of different thickness had different in-plane CTEs and moduli as measured by Shih et al. (2004) and as indicated in the legend of Fig. 63.10. The three curves of Fig. 63.10 correspond to the graphs of Eq. (63.10b) for the different values or pairs of modulus and CTE of the test boards. For the 62- and 93-mil boards, the in-plane CTEs are very close, 15.9 ppm/°C and 15.85 ppm/°C, respectively. Their moduli are 26 and 23 GPa, respectively. Thus, the vertical shift between the two top curves of Fig. 63.10 is essentially due to the change in the board modulus. The shift between the middle and lower curves is much larger. Part of it is due to the change in modulus from 26 to 30 GPa, but that shift should not much larger than the shift between the two top curves when the board modulus changed from 23 to 26 GPa. Instead, a greater fraction of the shift between the two lower curves is due to the larger change in board CTE, from 15.9 to 18.75 ppm/°C. The board properties and the model [Eq. (63.10b)] explain why the life reduction is much larger when the board thickness goes from 93 to 130 mils compared to going from 62 to 93 mils. In the latter case, the CTEs are about the same and the modulus decreases, thus the life reduction is small. In the former case (93 to 130 mils), the board modulus increases and the CTE mismatch between the board and component increases significantly, leading to a large reduction in solder joint life.

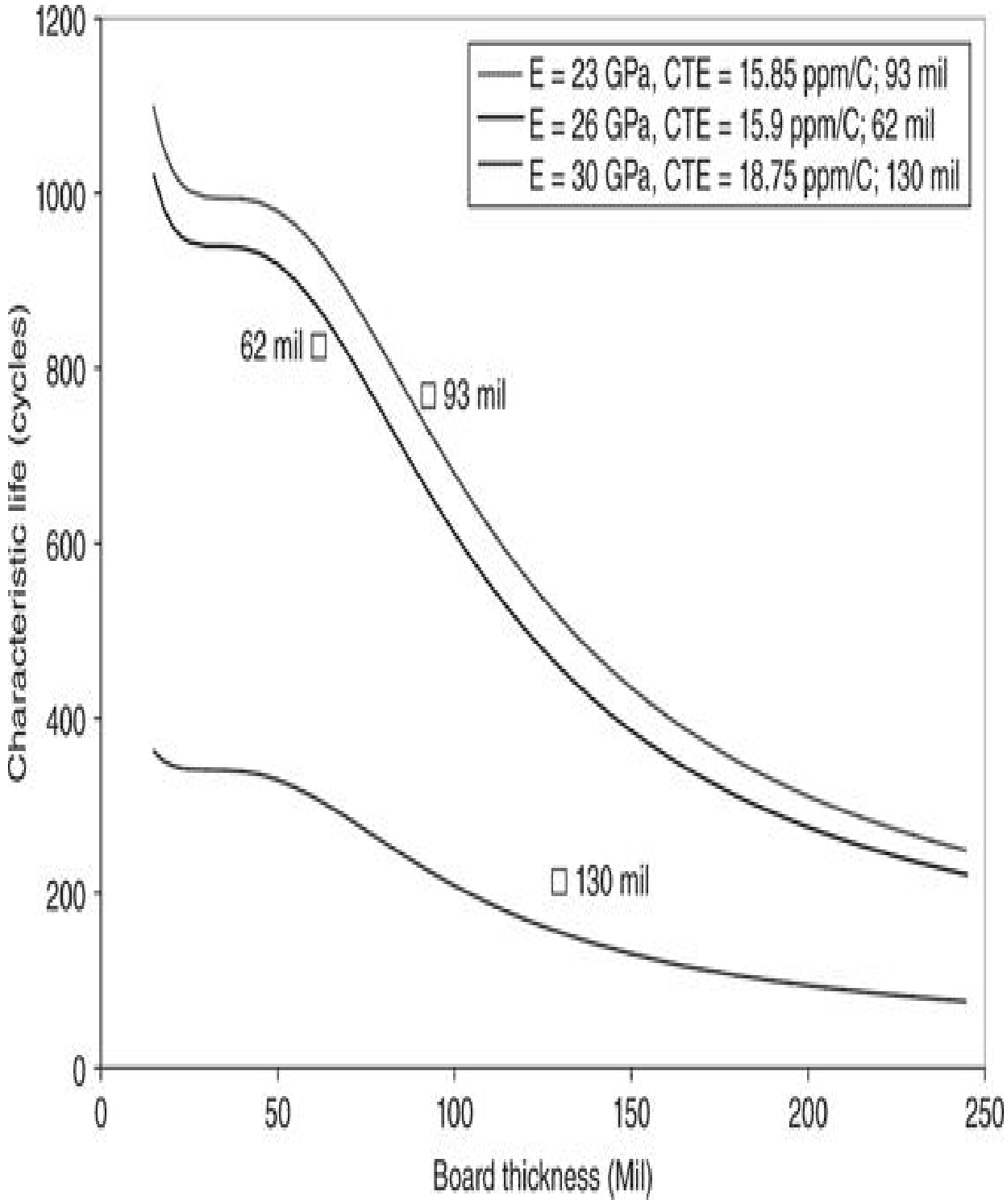


FIGURE 63.10 Solder joint life is plotted versus board thickness. Model lines are after Eq. (63.10) for given values of board's modulus E and in-plane CTE in diagonal direction of package. Data points for the same pairs of E and CTE values are test results for hiCTE CBGAs on 62-, 93-, and 130-mil-thick boards after R. Shih, 2004.

The board thickness model [Eq. (63.10b)] and the test results are in very good agreement. Shih et al. (2004) also reported that their test results were confirmed by finite-element analysis. The usefulness of Eq. (63.10b) is that it allows quantifying how much of the change in life is due to CTE effects and how much is due to the board modulus. Further validation of the use of Eq. (63.10a, b) is given in Clech (2015), including its application to the effect of component thickness effects as in the case of thick CBGA substrates and bare die assemblies.

The above example clearly illustrates that board thickness effects cannot be considered separately from board effective properties. The change in board properties with board thickness also points to the need to measure or model the effective properties of circuit boards, CTEs and moduli, accurately.

63.6.3 Rule-of-Mixtures to Estimate the Effective Properties of Circuit Boards

The rule-of-mixtures is a rough approximation that is of use to get quick estimates of board in-plane CTEs and moduli based on the thickness (h_i), CTE (α_i) and modulus (E_i) of each layer (index "I") in the board stack-up:

$$E_B = \frac{\sum_i E_i h_i}{h_B} \qquad (63.11a)$$

$$CTE_B = \frac{\sum_i E_i \alpha_i h_i}{E_B h_B} \qquad (63.11b)$$

In this author's experience, the rule-of-mixtures applies well to rigid, multilayer, epoxy-fiberglass boards that have a symmetrical stack-up without "compliant" layers that could give in shear. Advanced laminate and blending models are also available for more refined predictions of board properties (Sottos et al., 1999).

63.6.4 Single- versus Double-Sided Mirrored Assemblies

When identical components are mounted back-to-back in a mirrored, double-sided assembly, solder joint life under thermal cycling conditions can be reduced by a large factor, as much as two or three times (Juso et al., 1998; Primavera, 2003; Shih et al., 2004). The amount of life reduction is also component dependent because of board-to-component interaction that is controlled by their relative stiffness.

The driving force behind the reduction in solder joint life is suppression of the stress-relief mechanism associated with board bending. The board is no longer able to flex by bimetallic strip effect in the component mounting area. Solder joints are thus subject to higher shear forces than in a single-sided assembly. This effect is purely mechanical. In a mirrored assembly, the bending term, K_3, of the assembly stiffness K in Eq. (63.7a), becomes infinite and the board axial stiffness, K_2 in Eq. (63.7c), is reduced by a factor of two times because each component of the mirrored assembly acts on one half of the board thickness. The assembly

stiffness of a mirrored assembly is thus obtained from the formula (Clech, 1996):

$$\frac{1}{K_{\text{MIRRORED}}} = \frac{1}{K_1} + \frac{2}{K_2} \qquad (63.12)$$

where K_1 and K_2 are calculated as per Eq. (63.7b, c). This effect is purely mechanical. Since solder joint cyclic life goes as the inverse of the assembly stiffness [Eqs. (63.6), (63.8), and (63.9)], everything else being equal (e.g., no change in the board CTE), the ratio of solder joint lives for single versus mirrored assemblies goes as $K/K_{MIRRORED}$ (Clech, 2015), where the assembly stiffness K for single-sided assemblies is calculated by means of Eq. (63.7a).

63.6.5 SMD versus Non-SMD Pads

Board pad and solder mask design can affect solder joint life. The question is often asked which is better, solder mask design (SMD) pads or non-solder mask defined (NSMD) pads (Fig. 63.11)? Until recently, that is, for SnPb board assemblies, the industry consensus has been in favor of NSMD pads on the board side. SMD pads have been suggested as a way to mitigate pad cratering failures (Gray et al., 2010) that occur with stiff, lead-free solder joints. Some lead-free alloys being stiffer and having less ductility than standard SnPb, especially under high-strain rate conditions as under drop or shock conditions, solder joints can pull corner pads and the underlying epoxy out of the board. In SMD designs, solder mask holds the pads down and provide additional strength between board pads and epoxy-fiberglass boards.

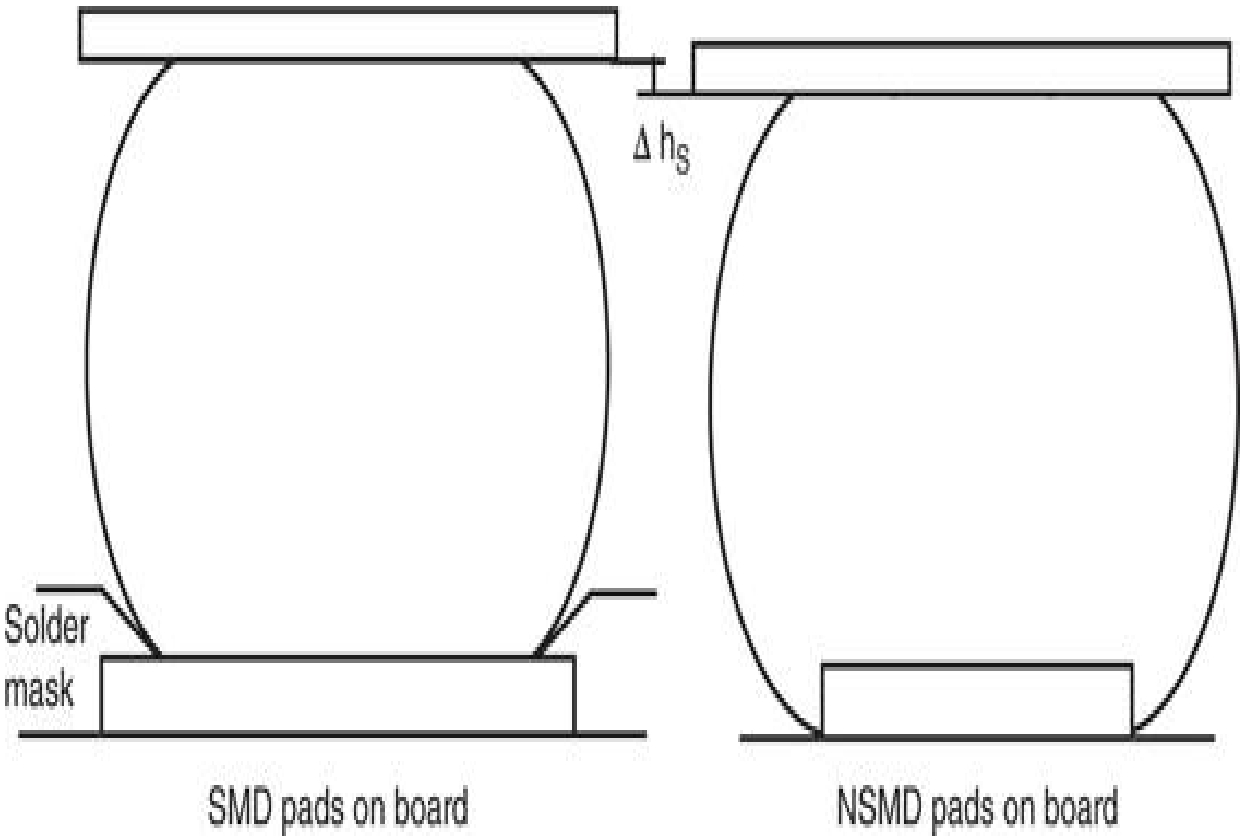


FIGURE 63.11 With solder mask defined (SMD) pads on the board side, the lower solder fillets are shaped by solder mask covering the periphery of the pads. With nonsolder mask defined (NSMD) pads on the board, solder wets the edges of the board pad, resulting in a small reduction in solder joint height, Δh_S.

SMD design pads may be preferable for boards under drop/shock/vibration loads. There is also evidence that SMD designs may enhance thermal cycling lives. Darveaux et al. (1995) reported that SnPb BGA assemblies with SMD pads had a 15 percent longer life than similar assemblies with NSMD pads on the board side. The slight decrease in fatigue life for NSMD assemblies was mostly due to their lower stand-off height, 20.8 mils versus 22.2 mils (Dh_S = 1.4 mils in Fig. 63.11). The industry consensus in favor of NSMD pads, contrary to the life improvement observed in the Darveaux (1995) experiment, is quality driven. Solder mask being susceptible to manufacturing offsets in the *x* and *y* directions of the board may encroach over board pads in an uncontrolled manner. The risk of uncontrolled solder mask

encroachment leads to reduced assembly yields and solder joints of uncontrolled shape with a reduced solder wetting area on the board pads, which, in turn, may result in infant mortality solder joint failures.

63.6.6 Board Pad versus Component Pad Size

Another common question related to board pad design is: given a component with a fixed pad size (diameter of solder-wettable area for BGAs and CSPs), what should be the pad size (diameter of solder-wettable area) on the board side? As a general rule, board pad diameters should not be larger than component pad diameters. Equal pad sizes are acceptable. Board pads that are slightly smaller (e.g., by 10 percent in diameter) than component pads provide for improved reliability under thermal cycling conditions (Ejim et al., 1995, 1996).

For a given solder ball diameter, equal or slightly smaller board pads provide for a slight increase in stand-off height, h_S, which increases solder joint life. A second argument is that, shear forces being equal at the solder joint to package and board interfaces, a slight reduction of the board pad wettable area is beneficial since it raises shear stresses (shear force divided by area) on the board side of the joint while reducing solder joint shear stresses on the component side, which is where most solder joint failures occur. However, much smaller board pad diameters should be avoided since this configuration leads to significantly higher shear stresses on the board side, a shift in failure location from the component to the board side, and failures that occur much earlier than they would on the component side.

When selecting board pad diameters, it is useful to estimate the expected solder joint height since the latter has

a significant impact on solder joint life. For many area array components that are light enough (e.g., plastic BGAs and CSPs), solder joints are barrel-shaped and actually take on the shape of a truncated sphere (Fig. 63.12). The solder joint height can then be estimated by back-solving the truncated sphere volume equation for h_S:

$$V = \frac{\pi h_S}{6}\left[h_S^2 + \frac{3}{4}(b^2 + c^2)\right] \tag{63.13}$$

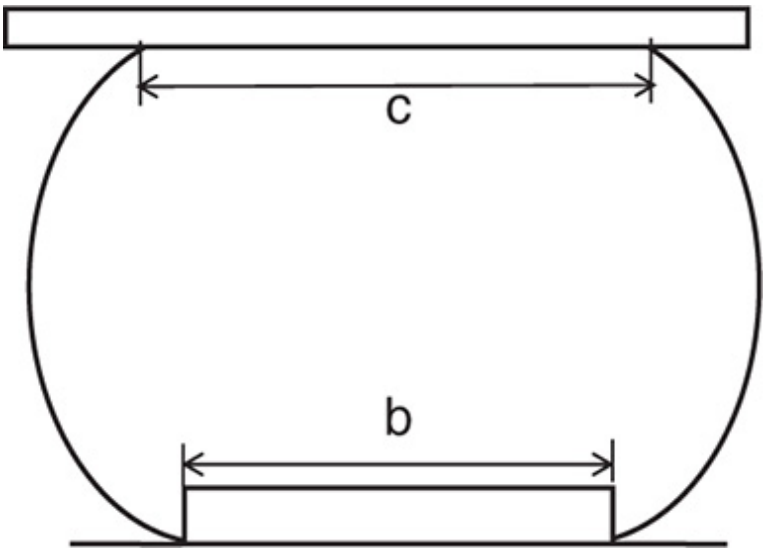


FIGURE 63.12 Component versus board pad size: on the component side, the solder-wettable pad area, with diameter "*c*," is determined by the package solder mask opening. On the board side, a slightly smaller, solder-wettable pad area, with diameter "*b*," provides for improved solder joint reliability under thermal cycling conditions.

where b and c are the board and component pad diameters and V is the total solder volume of the barrel-shaped solder joint (V = solder ball volume + solder volume in solder paste). Equation (63.13) has a closed-form solution for h_S. It can also be solved using a "Goal Seek…" menu in conventional spreadsheets.

63.6.7 Board Finish Effect

A correlation of lead-free thermal cycling data is shown in Fig. 63.13 as characteristic life scaled for the solder joint crack area versus the maximum cyclic shear strain computed as per Eq. (63.1). The data is for a variety of boards and components with SnAgCu solder balls and/or paste in the narrow composition range SAC387 to SAC396 (note: SAC387 has 3.8 percent wt. Ag and 0.7 wt. Cu, the rest being tin). The data points in Fig. 63.13 are highlighted by board finish: immersion Ag, organic solder preservative (OSP) or NiAu (after Fig. 2b in Clech, 2004).

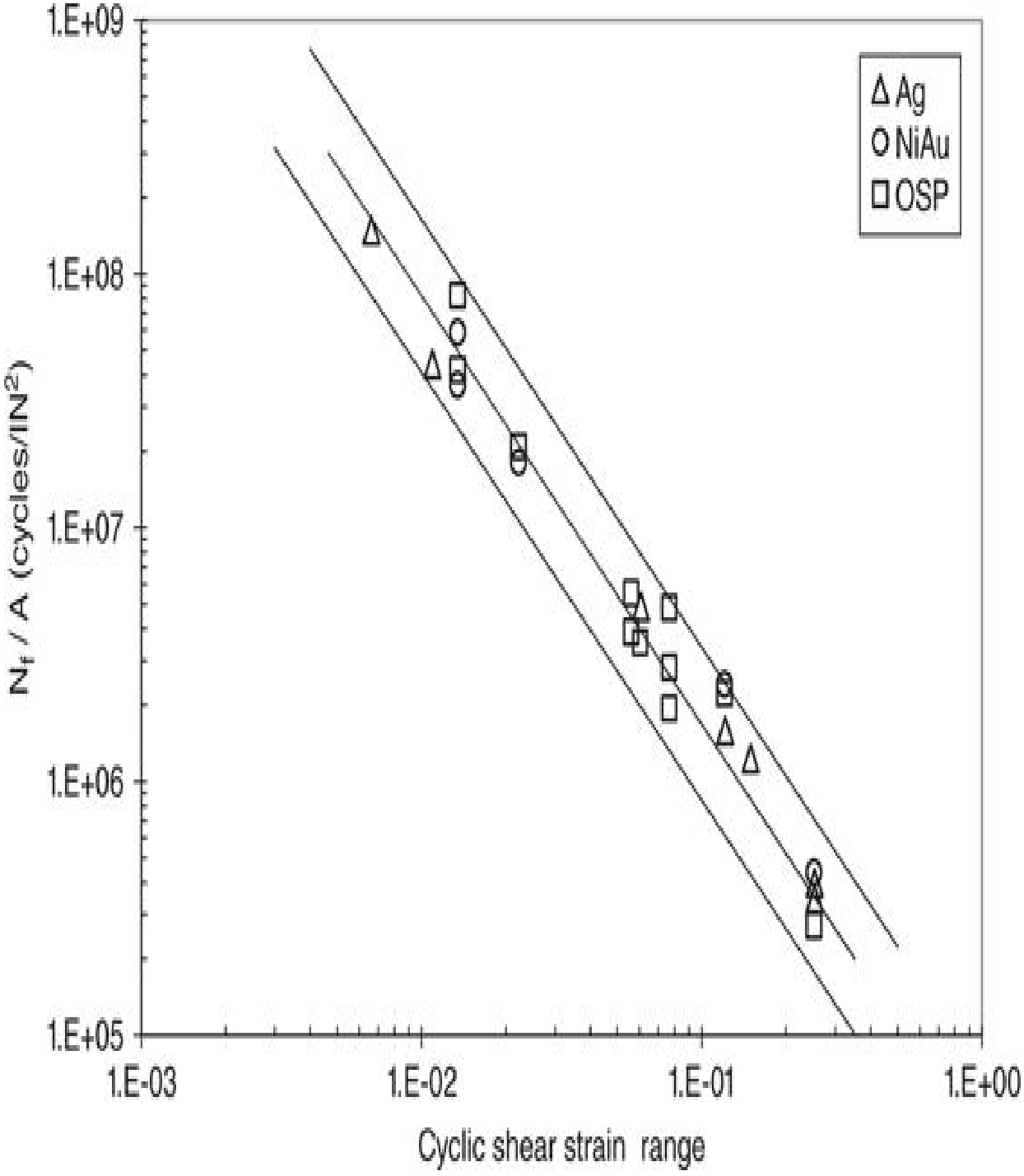


FIGURE 63.13 Correlation of lead-free solder joint life (N_f) scaled for the solder joint crack area (A) versus cyclic strain range during thermal cycling (after Clech, IPC Apex 2004). While the data is for a variety of components, the data points are shown in terms of board finish (Ag, NiAu, or OSP).

A centerline through all the data is shown as a dashed line which has a correlation coefficient of 96 percent, which indicates that the overall correlation is reasonably good. The spread of the data in Fig. 63.13 is typical of solder joint fatigue. The data points for a given board finish are above or below the centerline and no clear trend is visible per board finish type. Over a range of cyclic shear strains of more than one order of magnitude along the horizontal axis, none of the three board finishes appears to stand out and provide overwhelmingly better results than the others. The conclusion is not that board finishes do not matter. They do in terms of solder wetting, intermetallic formation and initial solder joint quality. However, the effect of available board finishes on solder joint fatigue life appears to be within the typical spread of fatigue data.

63.7 LEAD-FREE RELIABILITY TRENDS

63.7.1 Overview

A multitude of lead-free solder alloys have been developed over the years. Besides SnAg, SnBi, AuSn, and a few other eutectic compositions that have been in use for decades in niche applications, grand families of lead-free alloys have emerged such as SnAgBi (SAB), SnAgCu (SAC), SnCu, SnCuNi, SnZn, etc. … possibly with additions of a variety of elements. While Sn is the main constituent, alloy composition varies as well, for example, SAC0307, SAC105, SAC305, SAC387, SAC405 within the SAC family alone. Lead-free balls of one composition are also reflowed with lead-free paste of another composition. This leads to an infinite number of possible average compositions in actual solder joints, depending on ball and paste alloys, pad sizes and ball

and paste solder volume. Because of the proliferation of lead-free solder alloys, much work remains to be done for the field of lead-free reliability to be established as thoroughly as for standard SnPb reliability.

Solder alloy properties that are of use for lead-free reliability assessment include ductility, strength, toughness, ductile-to-brittle transition temperature, creep rates and creep rupture times, elasticity modulus, Poisson's ratio, their temperature dependence and their sensitivity to ageing conditions. For example, creep laws are essential to the simulation of stress/strain loops as shown in Fig. 63.8*b*, and to the development of acceleration factors (Clech, 2013; Darveaux, 2012). The above properties are not readily available for all new alloys, which may hinder the acceptance of some lead-free compositions.

Many lead-free alloys have a higher peak reflow temperature than standard SnPb. This has led to frequent changes in board and package materials that need to be tracked closely by all participants of the supply chain. Changes in circuit board epoxy, package substrate materials (including solder mask in BGAs and CSPs) and molding compounds can all affect assembly yields—for example, due to warpage (Ahsan et al., 2008)—and attachment reliability (Vandevelde et al., 2011).

63.7.2 Effect of Ag Content on Reliability

Among SAC solders, alloys with low Ag contents, for example, SAC105 with 1.0 percent wt. Ag, 0.5 percent wt. Cu, appear to have a better performance under drop test conditions than SAC alloys with higher Ag contents, for example, SAC305. Data from two sources (Syed et al., 2007; Yongping et al., 2013) are plotted in Fig. 63.14 as the number of drop to failures, normalized to SAC305, versus the %Ag

contents. The improvement for SAC105 versus SAC305 is a factor of 1.2 to 1.7 times.

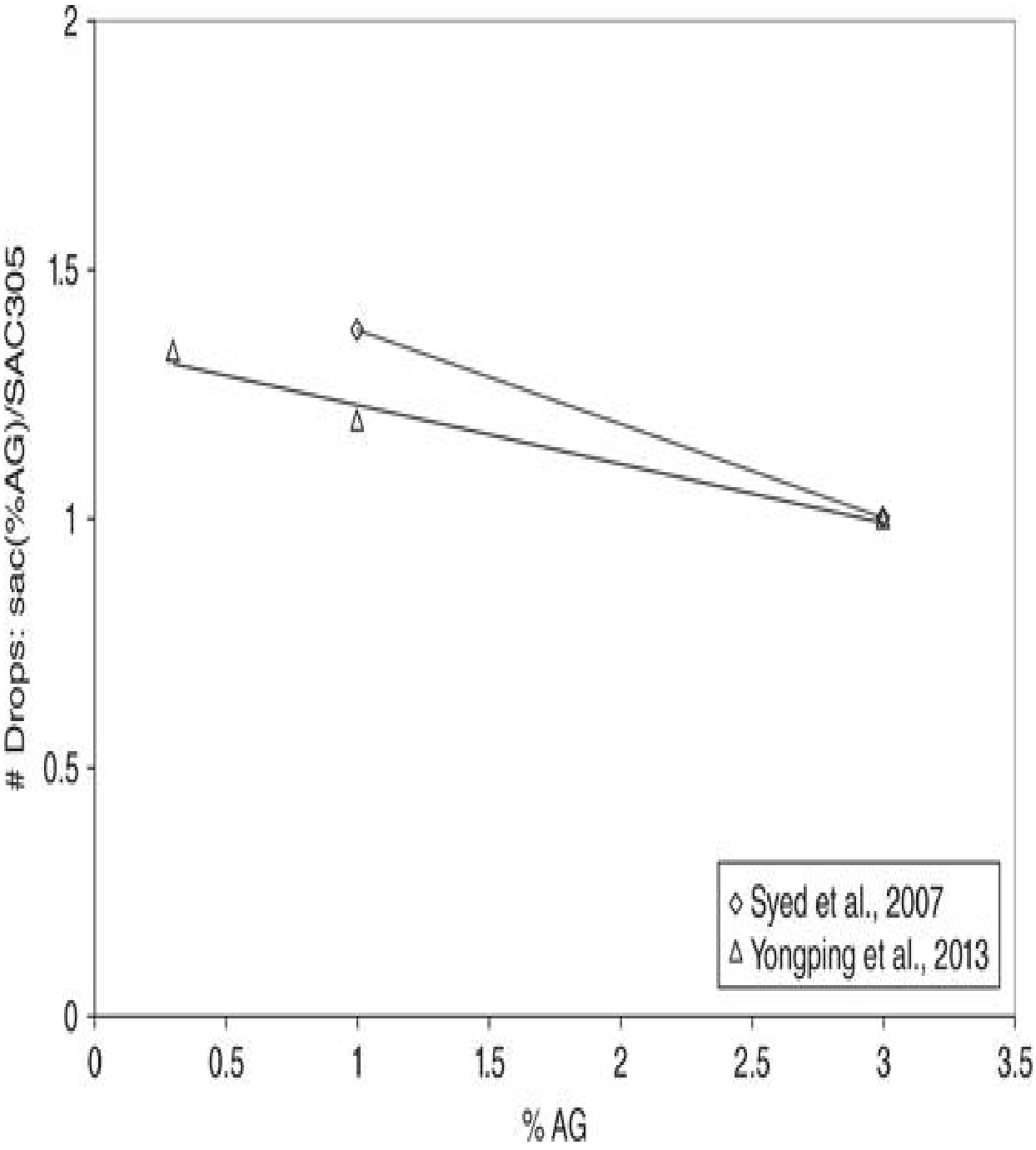
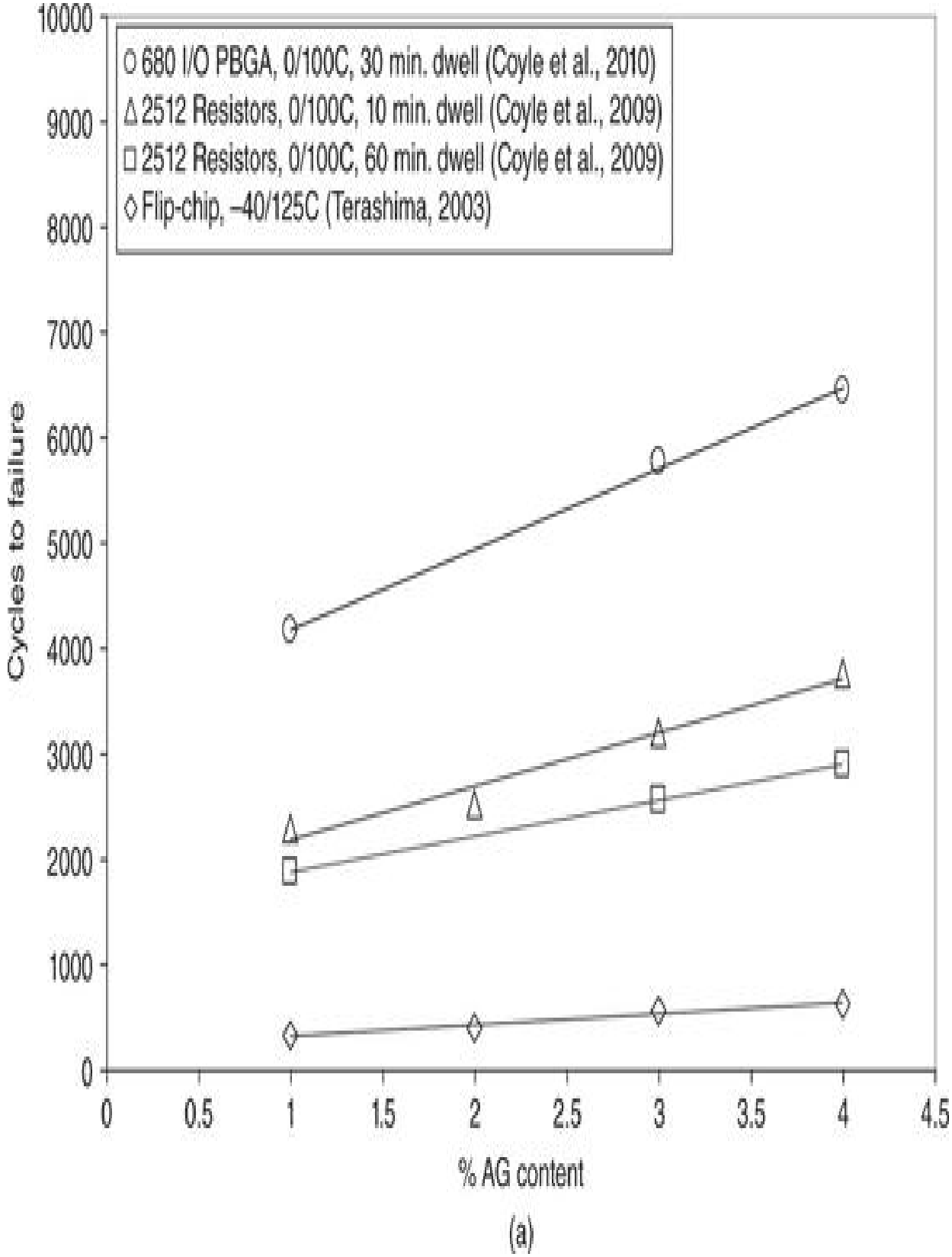
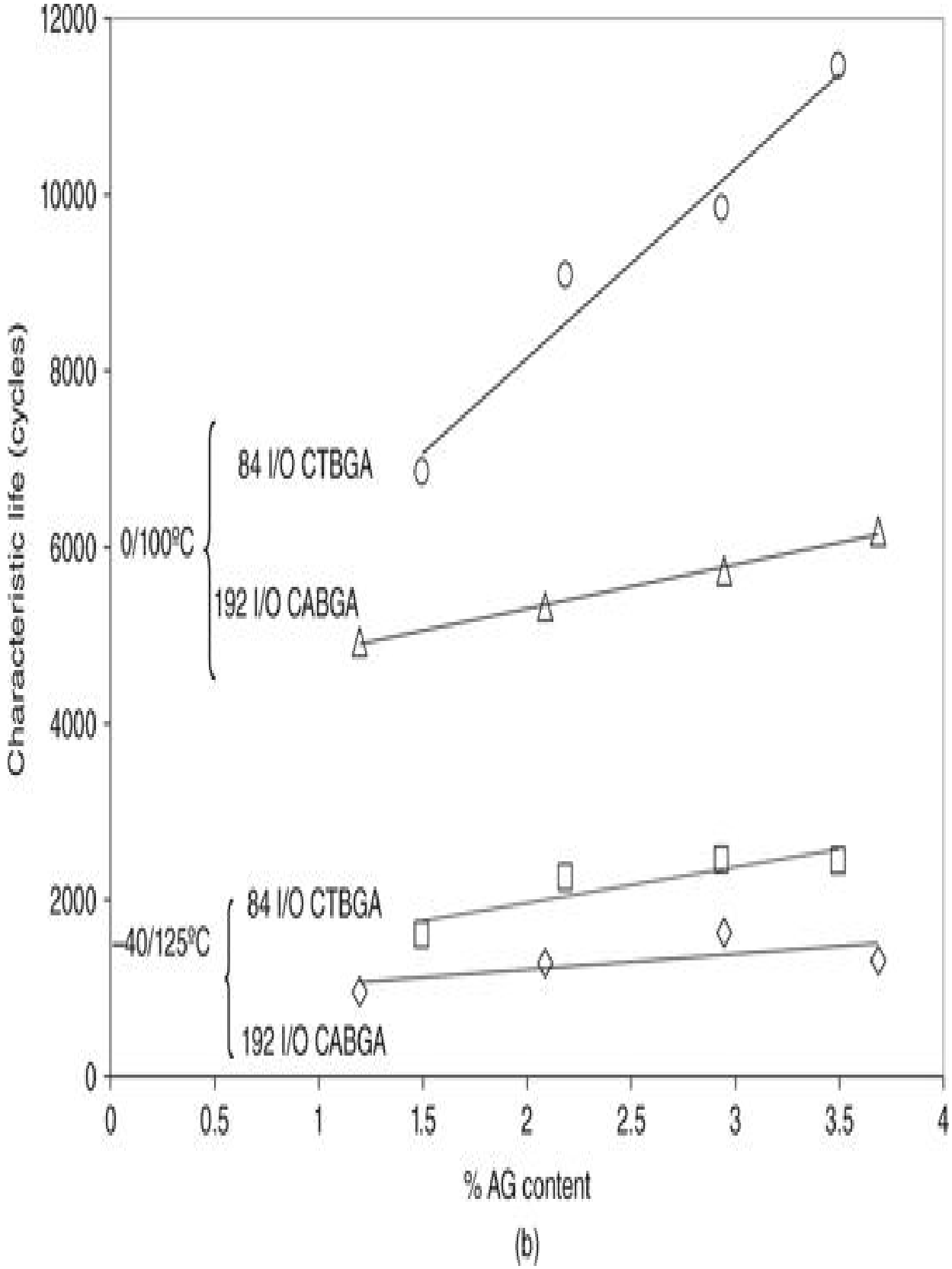


FIGURE 63.14 Effect of %Ag in SAC solder joints on the number of drops to failure. For each dataset, the data has been normalized to the number of drops to failure for SAC305 assemblies.

The trend is reversed under thermal cycling conditions. Figure 63.15*a*, *b* (after Fig. 20a, b in Clech, 2013) shows cycles to failure versus Ag content in SAC assemblies for a variety of components. The source of test data is indicated in the legend (Fig. 63.15*a*) or in the figure caption (Fig. 63.15*b*). The trends through each dataset are linear, at least in the plotted range of 1 to 4 percent Ag contents. The slopes of the linear trendlines vary by one order of magnitude depending on the component type and test conditions. The slopes decrease with an increase in thermal expansion mismatch between board and components, as seen in Fig. 63.15a when going from the PBGAs to the resistors to the bare chips datasets. The slopes also decrease under harsher test conditions, as seen Fig. 63.15b.


680 I/O PBGA, 0/100C, 30 min. dwell (Coyle et al., 2010)
2512 Resistors, 0/100C, 10 min. dwell (Coyle et al., 2009)
2512 Resistors, 0/100C, 60 min. dwell (Coyle et al., 2009)
Flip-chip, –40/125C (Terashima, 2003)
Cycles to failure
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
% AG content

(a)


12000
10000
8000
6000
4000
2000
0
Characteristic life (cycles)
0/100°C
84 I/O CTBGA
192 I/O CABGA
–40/125°C
84 I/O CTBGA
192 I/O CABGA
0
0.5
1
1.5
2
2.5
3
3.5
4
% AG content

(b)

FIGURE 63.15 (*a*) (After Fig. 20a in Clech, 2013): Effect of %Ag contents in SAC solder joints on the number of cycles-to-failure during thermal cycling for PBGA, resistor, and flip-chip assemblies. (*b*) (After Fig. 20b in Clech, 2013): Effect of %Ag contents in SAC solder joints on the number of cycles-to-failure during thermal cycling for CSP assemblies. The test data (symbols) is after Parker et al., 2012.

63.7.3 Impact on Accelerated Testing Conditions

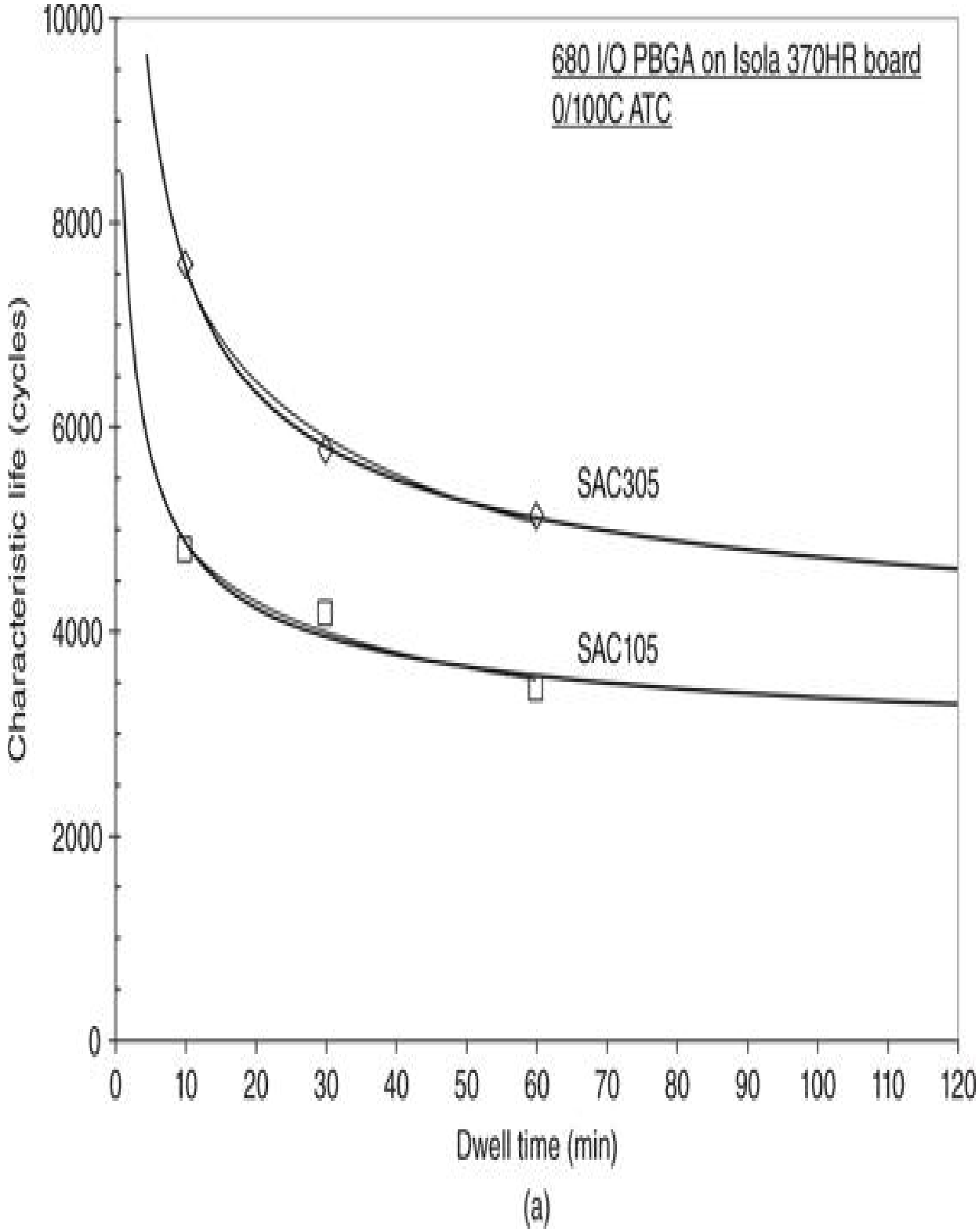
For the most part, accelerated testing conditions to prove in the reliability of lead-free assemblies are similar to test conditions for SnPb assemblies. One noticeable difference is that IPC 9701 provides a longer dwell time option of 30+ min, instead of about 15 min for SnPb, for accelerated thermal cycling. The reasoning behind this is that, since lead-free solders creep at much slower rates than SnPb, more time is needed to provide sufficient stress relaxation at the temperature extremes.

Several studies on SAC assemblies have shown that the failure modes remain the same and failure times for short and long dwell conditions are correlated accurately by strain energy predictive models (Bath et al., 2005; Clech, 2005, 2013). The main impact of long dwell times is to lengthen the test duration to acquire a full failure distribution, as required by IPC 9701, possibly by a factor of 1.5 to 2.5 times or more.

The Industry Working Group (Bath et al., 2005) tested SAC396 assemblies between 0 and 100°C with cold dwells of 10 min and hot dwells of either 10 or 60 min. Stress/strain loop simulation for the critical solder joints of interest showed that the 10-min hot dwell cycle provided for 50 percent stress relaxation at 100°C and that the 60-min hot dwell cycle was not as effective in terms of damage per unit of time (Clech, 2005). This is because, at the start of a dwell period, creep rates in solder joints are at their highest level,

and as time goes on, the creep rates slow down rather quickly, leading to less creep damage per unit of time. The Industry Working Group concluded that accelerated thermal cycling with long dwell times was not necessary.

More recent studies lead to similar conclusions for SAC105 and SAC305 assemblies (Coyle et al., 2010; Clech, 2013). As an example, Fig. 63.16*a* shows cycles to failure, in terms of characteristic life, versus dwell times during thermal cycling of SAC105 and SAC305 Plastic BGA (PBGA) assemblies between 0 and 100°C. The data points (symbols) are from Coyle et al., 2010. The simulations (solid lines) are based on a strain energy model using different creep laws for SAC105 and SAC305 solders (Clech, 2013). The failure modes were similar for the three different dwell times in test (10, 30, and 60 min) and the predictive strain energy model correlates rather well with the test results. The thin lines through the SAC105 and SAC305 data points represent empirical power laws that are fitted to the test data. Their exponents are −0.18 and −0.22 for SAC105 and SAC305, respectively. Figure 63.16*b* shows the same results as Fig. 63.16*a* in terms of test duration (time to 63.2 percent failure in months) versus dwell time. The simulations and the data show a linear trend except for very short dwell times. Going from 10 to 30 or 60 min for the dwell times, the test duration increases by a factor of approximately 1.5 to 2.5 times. Given that a typical thermal cycling test runs from 3 to 6 months or more, the duration and cost of accelerated thermal cycling need be taken into consideration when deciding to extend the dwell times at the temperature extremes.


680 I/O PBGA on Isola 370HR board
0/100C ATC
SAC305
SAC105
Characteristic life (cycles)
Dwell time (min)
0
2000
4000
6000
8000
10000
0
10
20
30
40
50
60
70
80
90
100
110
120

(a)

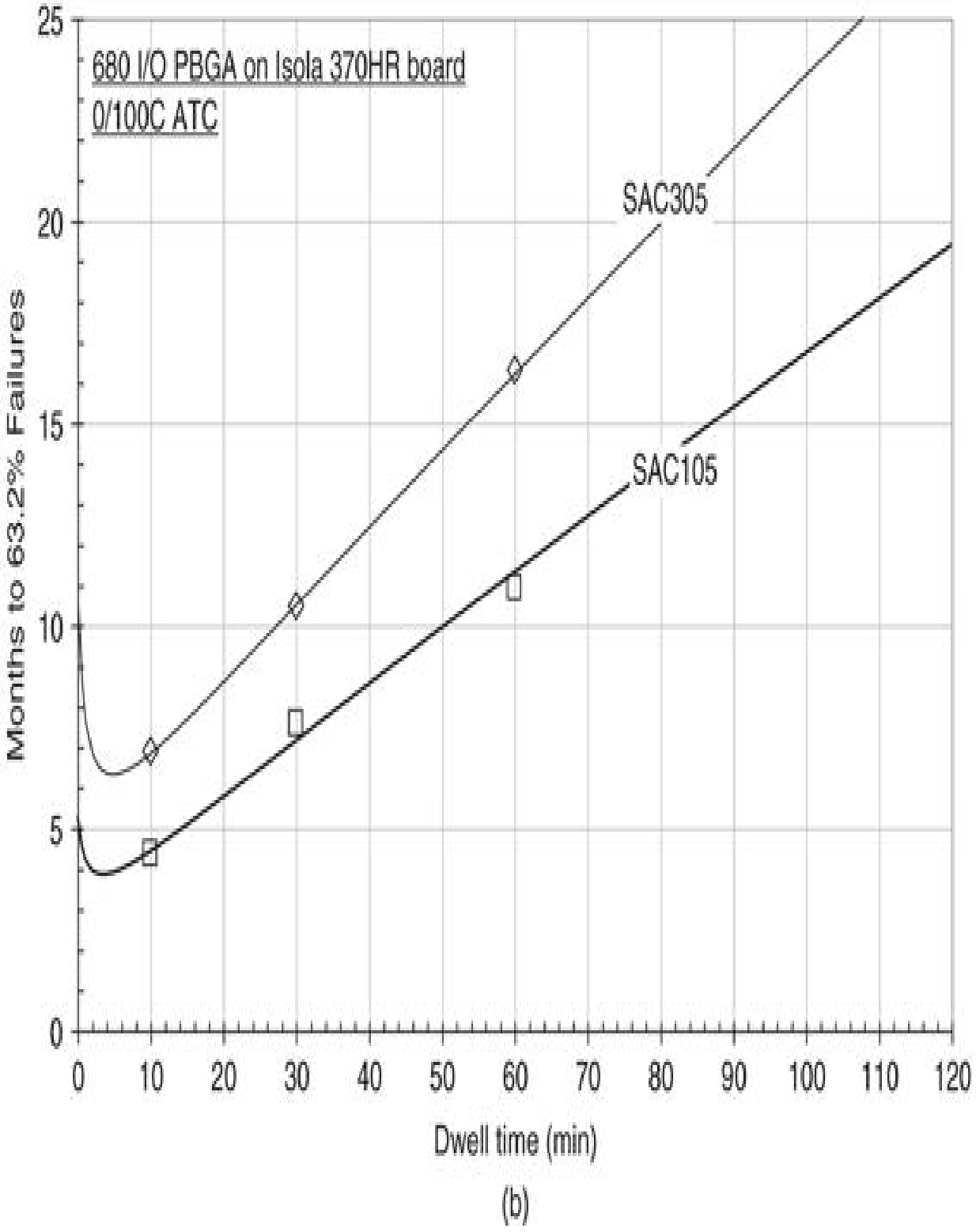


FIGURE 63.16 (*a*) (after Fig. 19a in Clech, 2013): Cycles to 63.2 percent failures versus dwell times (equal dwell times, hot and cold, in 0 to 100°C thermal cycle) for 680 I/O SAC105 and SAC305 PBGA assemblies on Isola 370HR board. Data

points are from Coyle et al., 2010. Simulations (solid lines) are from Clech, 2013. (*b*) (after Fig. 19b in Clech, 2013): Time to 63.2 percent failures (in months) versus dwell times (equal dwell times, hot and cold, in 0 to 100°C thermal cycle) for 680 I/O SAC105 and SAC305 PBGA assemblies on Isola 370HR board. Data points are from Coyle et al., 2010. Simulations (solid lines) are from Clech, 2013.

63.8 CONCLUSIONS

Solder joint reliability is critical to the performance of electronic systems. Numerous factors impact attachment reliability, including package and board geometry and material properties. The impact of board parameters was discussed in details in this chapter. Rules-of-thumb, design guidelines and simple equations are provided that should be of use for physical designers to make rational choices during the early stages of product development. These simple tools and guidelines are intended to minimize solder joint stresses and strains. They apply regardless of solder composition, SnPb or lead free.

Given the strong impact of board and package material properties, the solder attachment reliability assurance process rests heavily on suppliers' buy-in and participation. Reliability is in the details and requires input from the entire supply chain. At the very least, end users should be notified promptly of changes in materials. Reliable material properties, and updates, should also be readily available to physical designers.

Important trends in lead-free solder joint reliability were also discussed, such as the effect of Ag content on the performance of SAC assemblies. Opposite trends are established for SAC alloys with decreasing Ag content under drop conditions and accelerated thermal cycling. The projection of thermal cycling data from test to use conditions becomes critical in the selection of lead-free solder alloys. Some of the test and modeling techniques that may be of

use in the alloy selection process are discussed in Chaps. 62 and 64.

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CHAPTER 64

COMPONENT-TO-PWB RELIABILITY: ESTIMATING SOLDER JOINT RELIABILITY AND THE IMPACT OF LEAD-FREE SOLDERS

Mudasir Ahmad
Cisco Systems, San Jose, California

Mark Brillhart
Palo Alto, California

64.1 INTRODUCTION

In Chap. 63, the critical design variables that could impact the reliability and manufacturability of printed circuit assemblies (PCAs) have been outlined. The use of various assessment tools to quantify the expected life of PCAs is an important aspect of design for reliability. Data collected from standard tests can be used with acceleration transforms and

finite element analysis to assess the expected service life of any interconnect. Experimental data play a crucial role in reliability assessments. Poor data or data obtained under incorrect experimental conditions can lead to grossly inaccurate reliability assessments. “Garbage in equals garbage out” is nowhere more true than in interconnect reliability assessments. The history and experience gained over years of use of tin-lead solders are no longer applicable to lead-free assemblies because lead-free solders behave differently under the same end-use conditions and relatively little data are available on the characteristics of lead-free solders. The formulas for predicting the field life of solder joint interconnects would have to be revisited and validated with extensive experimental data. Moreover, the introduction of lead-free materials is accompanied by new failure mechanisms that are yet to be fully understood and mapped into field-life prediction models.

64.1.1 Experimental Tests

The different levels of solder joint interconnects in a typical PCA are illustrated in Fig. 64.1.

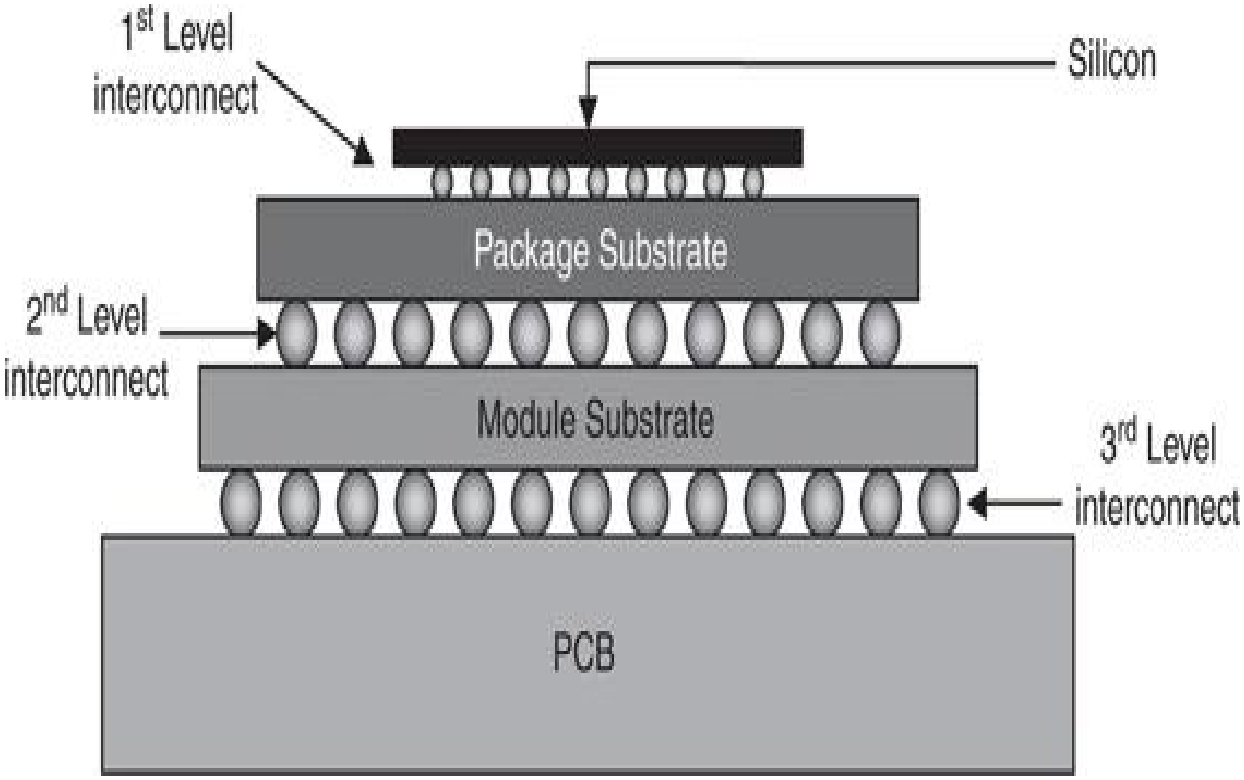


FIGURE 64.1 First-, second-, and third-level interconnects defined, employing a flip-chip assembly as an example. The first-level interconnect is the primary connection between the silicon die and the package substrate. In this example, the connection is created by the solder bumps between the die and the package. The second-level interconnect in this example is the next level of connection between the package substrate and the module substrate. The third-level interconnect in this example is created when the solder balls on the bottom side of the module substrate are attached via surface-mount technology (SMT) to the printed wiring board (PWB).

A myriad of experimental tools have been developed to assess solder joint reliability rapidly. These include

- Thermal cycling
- Thermal shock
- Air-to-air cycling
- Liquid-to-liquid cycling
- Mechanical bending
- Mechanical deflection
- Hyper-Peltier cooled thermal cycling

It is crucial for the PWB designer to understand the techniques employed, the applicability of the results, and the quality of the data when assessing the reliability of any package that will be placed on his or her PWB. Although rapid assessments are desirable, their benefit diminishes if the failure modes are fictitious and not indicative of expected field failures.

64.1.2 Impact of Lead-Free Materials on Reliability

The conversion to lead-free materials requires a reassessment of these experimental tools and field-life assessment techniques. New materials and failure modes need to be adequately captured in numerical and experimental test methods to model correctly the sort of thermal and mechanical conditions that an interconnect would be exposed to in field operating conditions.

The following key aspects of quantitative reliability assessment are discussed at length in this chapter:

- Thermomechanical reliability:
  - Temperature cycling tests used to determine the thermomechanical reliability of tin-lead and lead-free assemblies
  - The role of Weibull plots in estimating the failure distribution and characteristic life of solder joints from temperature cycling data
  - The acceleration transforms that can be used to estimate the field life of tin-lead and lead-free solder joints based on the results of temperature cycling tests
  - The role of power and minicycles in predicting the field life of solder joints

- Examples illustrating the use of acceleration transforms to compare the fatigue life of packages tested in different thermal cycling and end-use conditions
- Mechanical reliability:
  - Bend test methodologies and test methods that could be used to perform a relative comparison between different package types and surface finishes
  - Sample experimental data showing the comparative difference between different surface finishes and solder metallurgies
  - Shock test methodologies that could be used to perform a relative comparison between different packages and end-use conditions
  - Ball adhesion test methodologies: high-speed shear, pull testing, and impact testing

In addition, this chapter outlines the role of numerical analysis techniques in analyzing and improving the reliability of solder joint interconnects. Detailed procedures illustrating the use of finite element analysis (FEA)[1] in estimating the thermomechanical fatigue life of solder joint interconnects and monotonic bend testing are also discussed.

64.2 THERMOMECHANICAL RELIABILITY

In field operating conditions, ball grid array (BGA) solder joints are continuously subjected to strains due to the coefficient of thermal expansion (CTE) mismatch between the package and the PWB. These strains, which are caused by small but frequent fluctuations in temperature, accumulate as the device is powered up or down. As a result, cracks initiate in the solder joint interconnects and can

eventually propagate, leading to solder joint opens. The ability of the solder joint interconnects to withstand these differential strains during field operating conditions for a desired lifetime is generally referred to as *thermomechanical reliability*. The most common method for accelerating this failure in the lab is by thermally cycling the assembled device through extreme temperatures while recording any electrical opens that may occur during the test.

64.2.1 Temperature Cycling

Thermal cycle experiments have been the current industry standard for assessing second-level interconnect reliability. These types of tests tend to produce solder joint and solder joint-pad interfacial fractures that are typically seen in field failures. The fact that thermal cycle tests produce the same physical failures allows for detailed acceleration transformations and finite element-based life assessments to be made employing thermal cycle data as input.

The industry test method that is widely used for this testing is IPC-9701.[2] IPC-9701 provides detailed guidelines for the recommended temperature cycling test methods for evaluating the reliability of surface-mount solder joints. In addition, IPC-9701 also provides guidelines for estimating the performance of solder joints in different field-use conditions from the recommended accelerated thermal cycling tests.

An important benefit of performing industry standardized testing as recommended by IPC-9701 is that device suppliers can perform this test routinely for their devices, irrespective of where the device would be used. The results of the tests can then be used to determine whether the device will survive in a variety of end-use conditions. This saves significant testing cost and design time while providing a baseline for comparison of devices from different suppliers.

Where there are minor differences between the conditions in which the device is to be used, finite element analysis can be performed to bridge the differences between the tested device and the actual environment in which a very similar device would be used. The entire process by which the reliability of a device can be assessed is illustrated in Fig. 64.2.

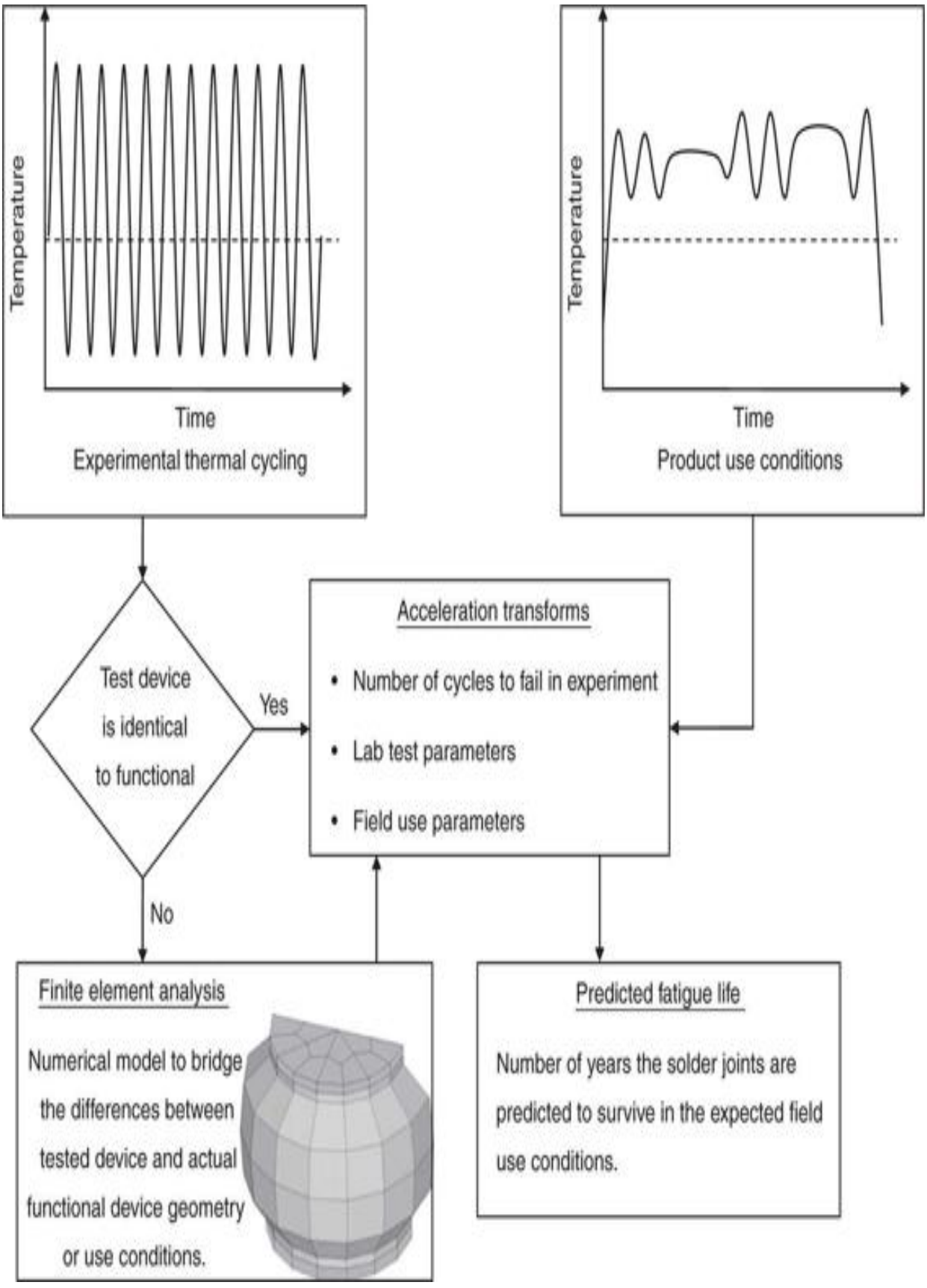

Temperature
Time
Experimental thermal cycling
Temperature
Time
Product use conditions
Test device is identical to functional
Yes
No
Acceleration transforms
• Number of cycles to fail in experiment
• Lab test parameters
• Field use parameters
Finite element analysis
Numerical model to bridge the differences between tested device and actual functional device geometry or use conditions.
Predicted fatigue life
Number of years the solder joints are predicted to survive in the expected field use conditions.

FIGURE 64.2 Flowchart of the solder joint thermomechanical reliability qualification process. Experimental data generated in the lab environment is compared with the expected product end-use conditions. If the package tested is identical to that used in the product, the acceleration transforms are used to map the fatigue life in the lab to the fatigue life in the product end-use conditions. If the package tested is similar but not identical to that used in the product, FEA is performed to account numerically for the differences between the tested and actual package before using the acceleration transforms.

Thermal cycle experiments are typically performed in single-chamber ovens. Dual-chamber systems are sometimes employed, but single-chamber equipment tends to dominate the test space. The main drawback of a dual-chamber oven is the lack of control over the thermal loading profile when transferring from one chamber (or thermal zone) to the other. Regardless of whether a single or dual chamber is used, temperature is cycled from a maximum (T_{max}) to a minimum (T_{min}) value. Temperature is ramped from one temperature extreme to another at a controlled rate, referred to as the *ramp rate*. Temperature is also held at the maximum and minimum values for a predetermined time known as the *dwell time*. Table 64.1 lists typical experimental parameters for second-level reliability qualification. Figure 64.3 contains a plot of temperature versus time along with explanations of the key experimental parameters.

TABLE 64.1 Typical Thermal Cycle Test Parameters for Second-Level Reliability Qualification

Parameter	Value
Maximum temperature (T_{max})	100°C
Minimum temperature (T_{min})	0°C
Ramp rates from T_{min} to T_{max} and T_{max} to T_{min}	10°C/min
Dwell time at T_{max} and T_{min}	10 min

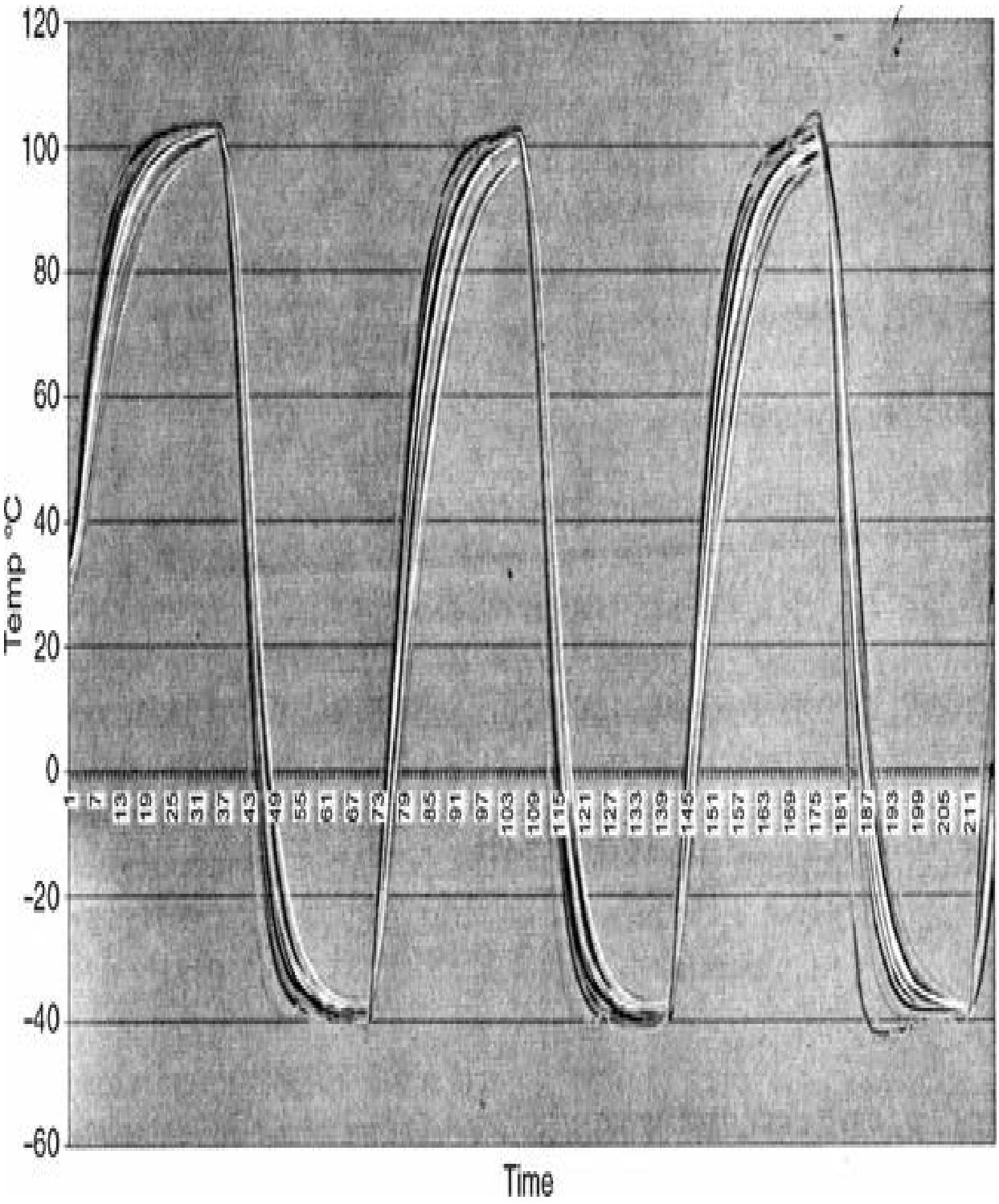


FIGURE 64.3 Typical thermal cycle profile. In this plot, T_{max} = 100°C, T_{min} = –40°C, and the cyclic frequency is 60 min.

Data acquisition systems and/or event detectors (commonly referred to as *glitch detectors*) are employed to

monitor resistance and/or scan for intermittent opens in real time. One of the early techniques for assessing solder joint integrity during thermal cycling was to remove parts periodically from the test chamber and measure resistance manually at room temperature.

The major risk associated with this technique is that opens are observed only at temperature extremes when the deformations due to CTE mismatch are largest. As the package cools to room temperature, most of the CTE-based deformations that pull cracked surfaces of solder joints are gone and there is a potential for cracked surfaces to be in enough physical contact to provide acceptable continuity. In some cases, the cycle number at which opens are observed at temperature extremes is much shorter than the cycle at which the same opens are observable at room temperature.

A schematic of a typical thermal cycling chamber, with the boards installed and connected to a data acquisition system, is shown in Fig. 64.4.

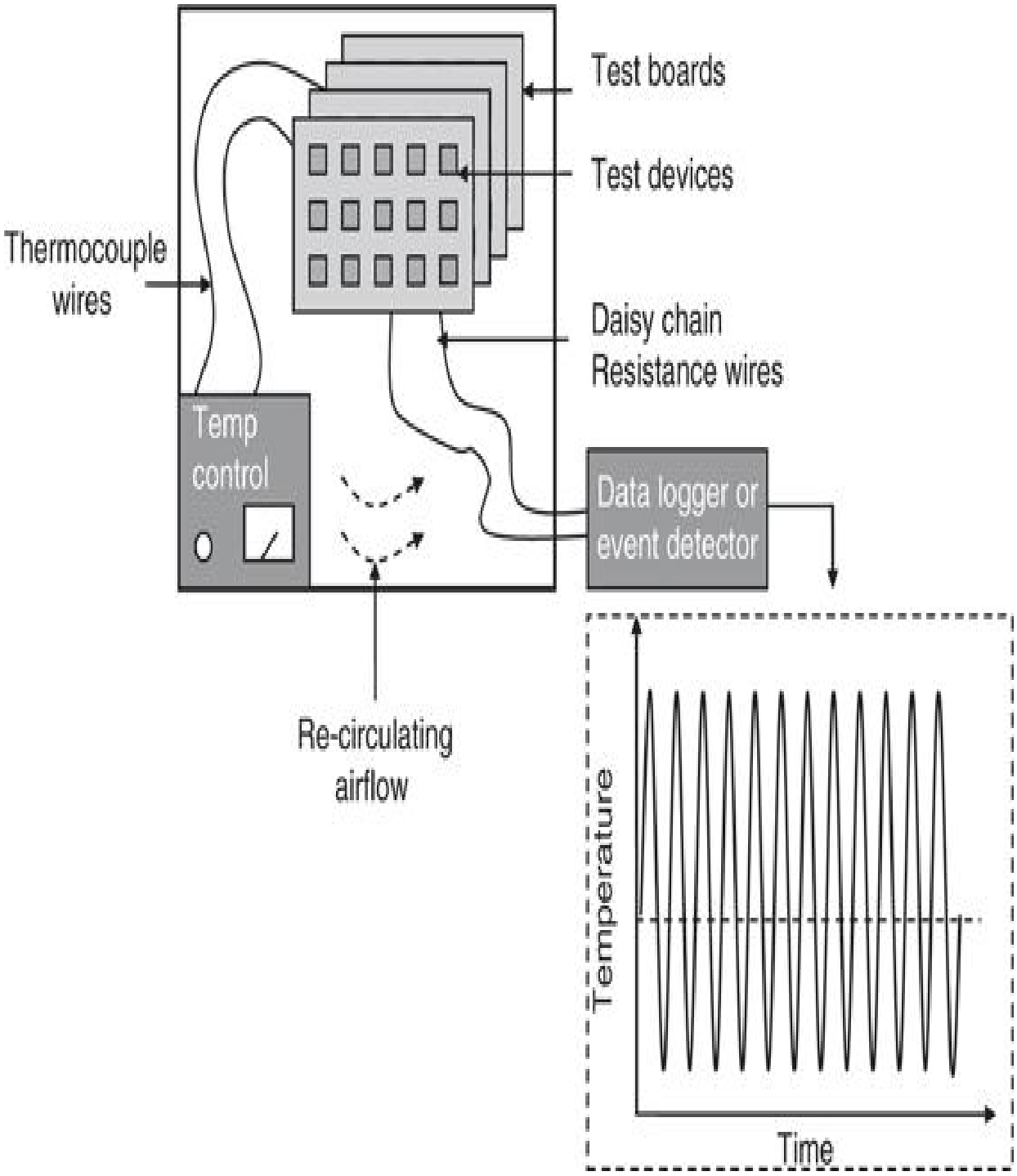


FIGURE 64.4 Schematic of a typical thermal cycling chamber and data acquisition system.

64.2.1.1 Effect of Lead-Free Conversion. The thermal cycling profile listed in Table 64.1 is also applicable to lead-free solders. Most of the damage accumulation occurs during

the high-temperature dwell phase. If the high-temperature dwell cycle is shortened, the damage accumulated per cycle would be reduced. It is desirable to maintain a high-temperature dwell long enough to allow creep saturation. However, practical limitations prevent this; as a result, the recommendations in IPC-9701-A[3] (Appendix B) are that a 10-min dwell time be used, and where possible a 30-min (or higher) dwell time could be used. Finite element analysis could be used to calibrate the experimental data and determine the effect of dwell time on long-term reliability.

64.2.1.2 Thermal Shock. Thermal shock experiments continuously cycle parts from a high to a low temperature very rapidly. These types of experiments are typically used as screening tools or to run parallel experiments on a known good part and a proposed new component to assess the relative performance of each part. Thermal shock experiments are quite rapid, with thermal shock test durations on the order of days rather than the months associated with thermal cycle test times.

The main drawback of thermal shock experiments lies in the fact that these types of tests tend to induce failure modes not observed in the field. Additionally, even if solder joint fatigue can be induced, it is very difficult to map the high ramp rates associated with thermal shock loading conditions to the more gradual thermal loading conditions that occur in the field. Consequently, this test technique is limited to relative comparisons between packages in which the failure modes have been shown to be comparable under the same thermal shock test conditions.

64.2.2 Weibull Distributions

The results of the temperature cycling tests described in Sec. 64.2.1 can be used to estimate the field operating life of the

solder joint interconnects by using the acceleration transforms outlined in detail in Sec. 64.2.3.

However, to determine the field operating life, one needs to know the life of the parts in lab testing. The raw data obtained from the lab test could be fitted with a failure distribution to determine the mean life of the parts. Typical failure distributions include Weibull, Normal, Lognormal, and Exponential. For wear-out type of failures, the Weibull and Lognormal distributions are usually used, with Weibull being the most common. Weibull distributions are lowest value distributions derived from the weakest-link theory.[4,5] Solder joint interconnects can be considered as connected in series. Usually, the failure of one joint at a critical location could cause the entire device to fail. The joints that fail early are usually located at the highest stress locations in the package. Devices with more resilient joints would not fail early. A Weibull distribution captures the minimum solder joint life, and the shape parameter captures the quality of the joints as a function of their construction and the applied stress.[4] There are different types of Weibull distributions: one-parameter, two-parameter, and three-parameter. The three-parameter Weibull Probability Distribution Function (PDF)[6] is as shown in Eq. (64.1).

$$f(t)=\frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \qquad (64.1)$$

where $f(t)$ = Probability Distribution Function

β = shape parameter (which defines the shape of the distribution)

η = scale parameter (which defines the characteristic life of the distribution; this is the time in which 63.2 percent of the tested samples would fail)

γ = location parameter (which defines the location of the distribution in time)

t = time

Two-parameter and three-parameter distributions are commonly used to fit the temperature cycling data. The two-parameter distribution fits a straight line though the data, whereas the three-parameter distribution fits a non-linear curve through the data. In general, the two-parameter distribution is more conservative than the three-parameter distribution. Best practice is to perform regression analysis to determine which distribution best fits the data.

Another important factor in the statistical assessment of test data is the *confidence interval*. Confidence intervals (or *confidence bounds*) take into account the quality of the data based on the number of samples tested.[7] When two separate experimental data sets are being compared, double-sided confidence bounds are useful in normalizing the data based on the number of samples tested in each data set. An example of upper and lower confidence bounds set at 90 percent is illustrated in Fig. 64.5.

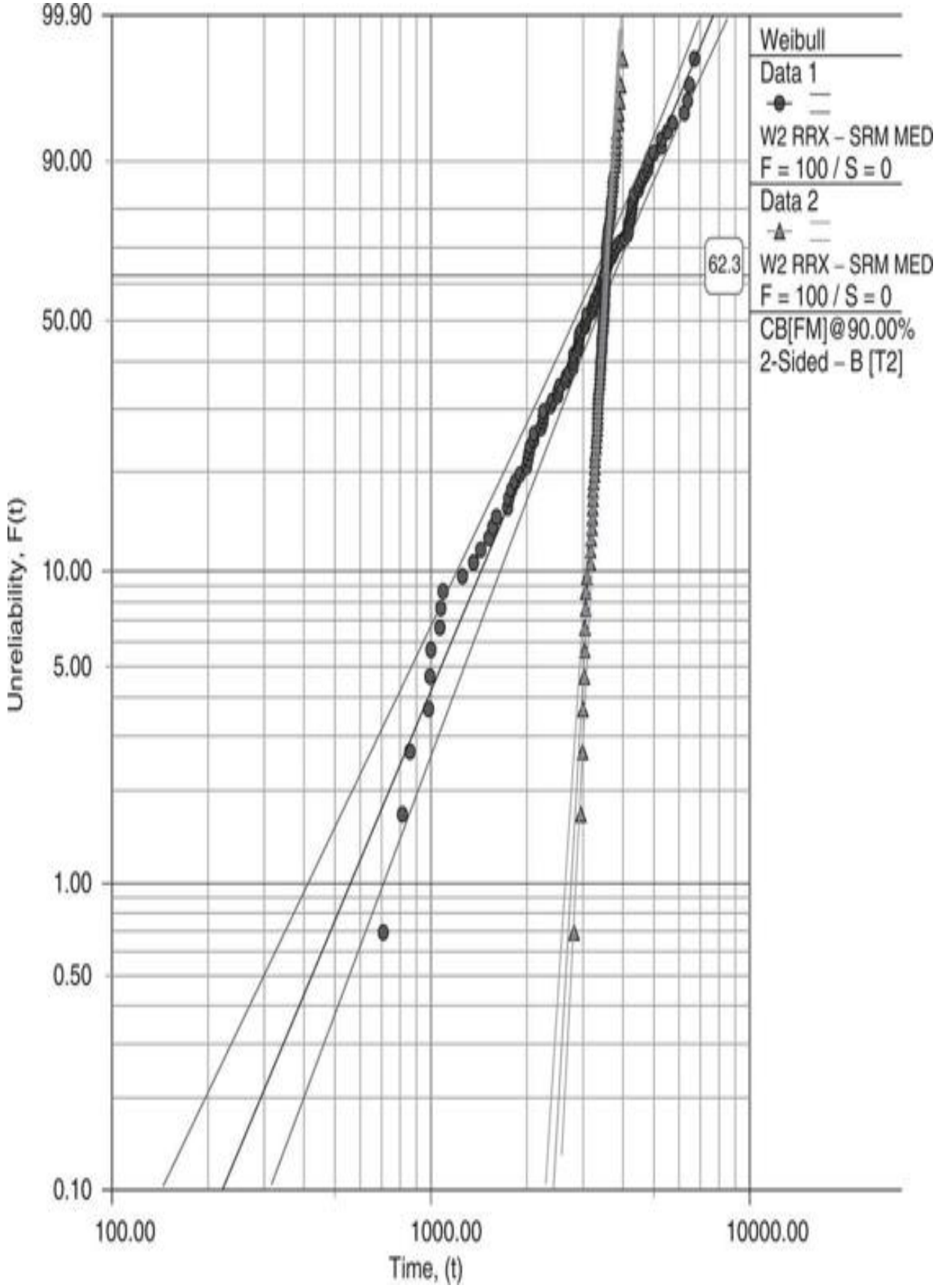

99.90
90.00
50.00
10.00
5.00
1.00
0.50
0.10
Unreliability, F(t)
100.00
1000.00
10000.00
Time, (t)
62.3
Weibull
Data 1
W2 RRX – SRM MED
F = 100 / S = 0
Data 2
W2 RRX – SRM MED
F = 100 / S = 0
CB[FM]@90.00%
2-Sided – B [T2]

FIGURE 64.5 A typical two-parameter Weibull distribution. The plot shows two data sets with different shape parameter (β) values but comparable characteristic life (η). Extrapolating to 1 percent failure free life shows that the 90 percent lower-bound confidential interval for data set 1 is lower than that for data set 2, even though the characteristic lives are comparable.

64.2.3 Material Properties

A tremendous number of researchers have explored the reliability of Pb/Sn solder alloys.[8] A wealth of data, material properties, and proposed constitutive relationships have been captured in the literature.[8,9,10] However, there is relatively little information in the literature on the material properties of lead-free solders. Moreover, the material property information available is on slightly different compositions of lead-free solders, with tests performed in different ways.

One of the challenges with both Pb/Sn and lead-free solders is that they undergo viscoplastic deformation (creep) as a function of time, temperature, strain rate, and applied stress. A variety of creep deformation models have been used to model the viscoplastic behavior of lead-free solders. The Anand model has been successfully used to model the viscoplastic behavior of Pb/Sn solders. The model allows for the simultaneous incorporation of time-independent plastic deformation as well as time-dependent creep deformation.

The functional form of the Anand model is given as shown in Eqs. (64.2) through (64.5).[11,12]

$$\dot{\varepsilon}_p = A\left[\sin h\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \tag{64.2}$$

where $\dot{\varepsilon}_p$ = inelastic strain rate
A = experimentally determined empirical constant
Q = activation energy
R = gas constant
ξ = stress multiplier
σ = equivalent stress
s = internal state variable
m = strain rate sensitivity parameter

$$\dot{s} = \left\{ h_o \left(|B| \right)^a \frac{B}{|B|} \right\} \frac{d\varepsilon_p}{dt} \tag{64.3}$$

$$B = 1 - \frac{s}{s^*} \tag{64.4}$$

$$s^* = \hat{s} \left\{ \frac{\dfrac{d\varepsilon_p}{dt}}{A} \exp\left(\frac{Q}{kT} \right) \right\}^n \tag{64.5}$$

where h_o = hardening/softening constant
a = hardening/softening strain rate sensitivity coefficient
s^* = saturation value of s for a given set of temperature and strain rate data
$\hat{s}$ = saturation coefficient
n = strain rate sensitivity coefficient for the saturation value of deformation resistance

The relevant material property information on the solder composition close to that recommended by iNEMI[13]

(Sn3.9Ag0.6Cu) is listed in Table 64.2.

TABLE 64.2 Material Properties: Anand's Constants for Lead-Free Solder

Reference	Pei & Qu[14]	Rodgers[15]	Reinikainen[16]
Solder material	95.5Sn3.8Ag0.7Cu	95.5Sn3.8Ag0.7Cu	95.5Sn3.8Ag0.7Cu
Strain rate range	25–180°C	20–125°C	—
Specimens used	1 mm dog bone	4 mm dia. dog bone	—
S_0 (MPa)	21.57	24.04	1.3
Q/R (K)	10041	11049	9000
A (sec-1)	9450.6	8.75e+06	500
ξ	1.1452	4.12	7.1
m	0.1158	0.23	0.3
h_o	133.8025	9537	5900
$\check{S}$	13.3372	90.37	39.4
n	0.0402	2.26e–10	0.03
a	0.1082	1.2965	1.4

One disadvantage of the Anand model is that it mainly captures steady-state creep of solder, but it does not capture primary creep (see Fig. 64.6). Since a significant portion of solder joints' field life is spent in the primary creep phase, it is difficult to predict fatigue life driven by end-use conditions. In other words, although the Anand model can be successfully used in predicting the fatigue life of solder joints tested in laboratory conditions, it may not be very accurate in predicting the fatigue life of solder joints in field use conditions. What may be needed is a time-hardening creep

model that can better capture primary, secondary (steady-state), and tertiary creep.

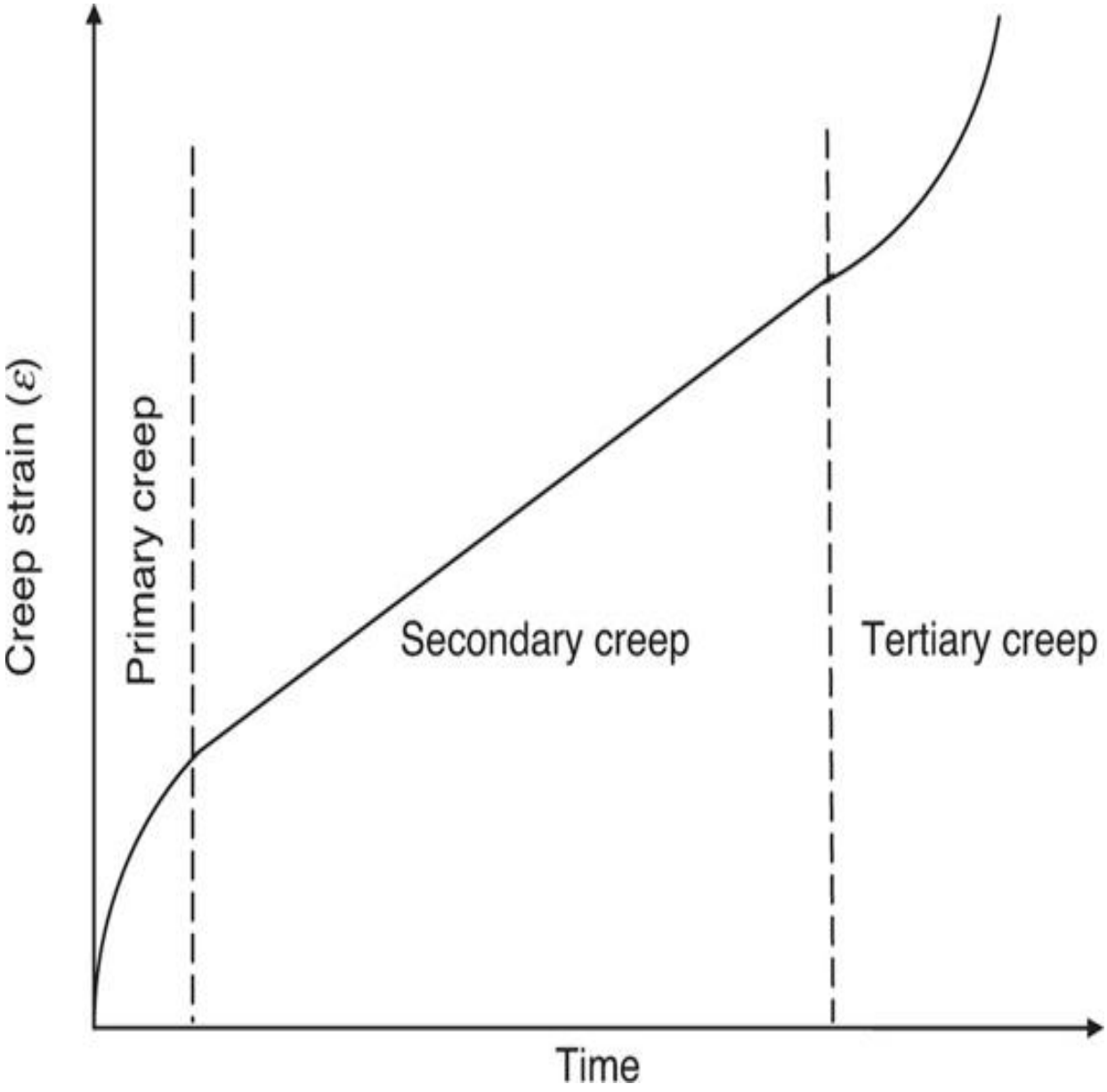


FIGURE 64.6 A typical creep strain versus time curve for viscoplastic materials. The curve shows that creep strain starts out as a non-linear curve, becomes steady for a significant period, and then increases significantly into tertiary creep. Most of the life of a solder joint is spent in the primary and secondary creep strain range of the curve.

Another model that proposes the incorporation of primary and tertiary creep strain rates is the A-Ω model.[17] This model

proposes that the primary creep strain rate be represented as an exponential decay function of increasing creep strain, and the tertiary creep strain rate be represented as an exponential growth function of increasing creep strain. However, this model is relatively new and has not been validated with independent experimental reliability data across the industry.

Other models available in the literature for different lead-free solder metallurgies are listed in Table 64.3.

TABLE 64.3 Material Properties for Lead-Free Solder[18]

Creep Model	Metallurgy	Constant	Value	Ref.
$\dot{\varepsilon} = C_1[(C_3\sigma)]^{-C_2}\exp\left(\frac{-C_4}{T}\right)$ (Norton creep model)	Sn4.0Ag0.5Cu	C_1 (s^{-1})	8×10^{-11}	Weise[19]
		C_2	12	
		C_3 (MPa^{-1})	1	
		C_4 (K)	8,996.57	
$\dot{\varepsilon} = A_1\left(\frac{\sigma}{\sigma_n}\right)^{n_1}\exp\left(-\frac{Q_1}{RT}\right) + A_2\left(\frac{\sigma}{\sigma_n}\right)^{n_2}\exp\left(-\frac{Q_2}{RT}\right)$ (Double power law)	Sn4.0Ag0.5Cu	A_1 (s^{-1})	10^{-6}	Weise[20]
		n_1	3	
		Q_1/R (K)	34.6	
		A_2 (s^{-1})	10^{-12}	
		n_2	12	
		Q_2/R (K)	59.1	
$\frac{d\gamma}{dt} = C_1[\sin h(C_2\sigma)]^{C_3}\exp\left(-\frac{C_4}{T}\right)$ (Garofalo creep)	Sn3.8Ag0.7Cu	C_1 (s^{-1})	32000	Pang[21]
		C_2	37×10^{-9}	
		C_3 (MPa^{-1})	5.1	
		C_4 (K)	6524.7	

A more comprehensive list of mechanical material properties of lead-free solders and other materials used in electronic packages can be found in Reference 22.

64.2.4 Norris-Landzberg Acceleration Transformation

PWB designers typically receive a failure distribution plot (see Fig. 64.5) as part of a second-level package qualification report. This failure distribution plot is typically obtained in a thermal cycle oven under controlled temperature profiles that include the maximum and minimum temperatures (T_{max} and T_{min}, respectively) of the thermal cycle along with the frequency (f) of the experimental thermal cycle. The designer must then relate these experimental data obtained under ideal conditions to a different thermal cycle condition (or conditions) encountered in the product end-use environment. Although relative comparisons of two packages thermally cycled under identical conditions can be made in a ranking sense, this type of analysis yields no information regarding the actual lifetime of the solder joints under field loading conditions. This section focuses on the mapping of a laboratory thermal cycle to different end-use thermal profiles using strain as a damage metric.

64.2.4.1 Fatigue Behavior. The fatigue behavior of many metals (including Pb/Sn and lead-free solder alloys) can be described by the Coffin-Manson relationship [Eq. (64.6)],[9] which relates the fatigue life of a metal to the plastic strain the material experiences during loading. Elastic strain is the reversible or recoverable deformation that occurs during a loading cycle. Plastic strain is the amount of irreversible (or permanent) deformation that occurs during a loading cycle.

$$\varepsilon = \varepsilon_e + \varepsilon_p = AN_f^{-c} + BN_f^{-m} \tag{64.6}$$

where ε = total strain per cycle
ε_p = plastic portion of the cyclic strain
ε_e = elastic portion of the cyclic strain
N_f = number of cycles to failure
A,B,c,m = experimentally determined empirical constants

Most solder joints fail in the low cycle fatigue region (less than 10,000 cycles to failure),[9] where strain is primarily plastic. Thus, neglecting the elastic component of strain, Eq. (64.6) can be simplified and rearranged to yield a relationship between the number of cycles to failure and the plastic strain [see Eq. (64.7)].[9]

$$N_f = (A/\varepsilon_p)^{1/m} \tag{64.7}$$

where ε_p = plastic portion of the cyclic strain
N_f = number of cycles to failure
A,m = experimentally determined constants

This can be further simplified to the most common form of the Coffin-Manson relationship shown in Eq. (64.8).[9]

$$N_f \propto \varepsilon_p^c \tag{64.8}$$

where ε_p = plastic portion of the cyclic strain
N_f = number of cycles to failure
c = an experimentally determined empirical constant

When any metal is cycled at a temperature above 50 percent of its melting temperature (homologous temperature), the strain rates, dwell times, and maximum

temperature influence its fatigue life.[9] This is due to the occurrence of creep, along with plastic and elastic deformation, within these temperature regimes.[9] Norris and Landzberg proposed a modified version of the Coffin-Manson relationship that considers the effects of frequency (f) and maximum temperature (T_{max}) on solder joint fatigue life [Eq. (64.9)].[9,10] This relationship is based on detailed physical and empirical analysis of the relationships between temperature and frequency on the thermal fatigue behavior of Pb/Sn solder alloys employed in interconnects.[10]

$$N_f = (A/\varepsilon_p)^{1.9} f^{1/3} \exp\left(\frac{0.123}{kT_{max}}\right) \tag{64.9}$$

where ε_p = plastic portion of the cyclic strain
N_f = number of cycles to failure
k = Boltzmann's constant (eV)
f = cyclic frequency
T_{max} = maximum temperature of the thermal cycle (K)
A = an experimentally determined empirical constant

64.2.4.2 Acceleration Factors. One of the challenges that must be addressed when attempting to employ Eq. 64.9 directly to assess fatigue life is the determination of the plastic strain and the value of the constant A. It is crucial to remember that the goal of this analysis is to develop an acceleration transform (or acceleration factor) that can be employed to use known fatigue-life data obtained under controlled laboratory conditions to estimate the number of cycles to failure under field conditions. The acceleration factor AF is defined as the ratio of the number of cycles to

fail in the field N_{fF} to the number of cycles to fail in the lab N_{fL} [see Eq. (64.10)].

$$AF = \frac{N_{fF}}{N_{fL}} \tag{64.10}$$

where AF = acceleration factor
N_{fF} = number of cycles to failure in the field
N_{fL} = number of cycles to failure in the lab

Substituting Eq. (64.9) for lab and field conditions into Eq. (64.10), one obtains Eq. (64.11).

$$AF = \frac{N_{fF}}{N_{fL}} = \frac{(A/\varepsilon_{pF})^{1.9} f_F^{1/3} \exp\left(\frac{0.123}{kT_{maxF}}\right)}{(A/\varepsilon_{pL})^{1.9} f_L^{1/3} \exp\left(\frac{0.123}{kT_{maxL}}\right)} \tag{64.11}$$

where AF = acceleration factor
N_{fF} = number of cycles to failure in the field
N_{fL} = number of cycles to failure in the lab
ε_{pF} = plastic portion of the cyclic strain in the field
ε_{pL} = plastic portion of the cyclic strain in the lab
f_F = cyclic frequency
f_L = cyclic frequency
T_{maxF} = maximum temperature of the thermal cycle in the field (K)
T_{maxL} = maximum temperature of the thermal cycle in the lab (K)
k = Boltzmann's constant (eV)
$_L$ = lab conditions
$_F$ = field conditions

Equation (64.11) can be algebraically rearranged to yield Eq. (64.12). Note that the "max" subscripts on the maximum temperatures have been dropped to simplify the notation.

$$AF = \frac{N_{fF}}{N_{fL}} = \left[\frac{\varepsilon_{pL}}{\varepsilon_{pF}}\right]^{1.9} \left[\frac{f_F}{f_L}\right]^{1/3} \exp\left[1414\left(\frac{1}{T_F} - \frac{1}{T_L}\right)\right] \tag{64.12}$$

where AF = acceleration factor
ε_{pF} = plastic portion of the cyclic strain in the field
ε_{pL} = plastic portion of the cyclic strain in the lab
f_F = cyclic frequency in the field
f_L = cyclic frequency in the lab
T_F = maximum temperature of the thermal cycle in the field (K)
T_L = maximum temperature of the thermal cycle in the lab (K)

When considering package interconnects of the same geometry and material set, one can reduce the strain term ε_p in Eq. (64.9) to the change in temperature.[10] This is a key feature that enables the development of an acceleration transform. The goal of this analysis is to develop a transform that allows one to map laboratory thermal cycle loading conditions to field loading conditions for the same package. Thus it is valid to assume that the strain term can be reduced to the change in temperature, as shown in Eq. (64.13).

$$\varepsilon_p \propto \Delta T \tag{64.13}$$

where ε_p = plastic portion of the cyclic strain

ΔT = difference between maximum and minimum temperature of the thermal cycle

Substitution of Eq. (64.12) (including $_L$ and $_F$ subscripts for lab and field, respectively) yields the final form of the acceleration factor relationship, which can be seen in Eq. (64.14).[10]

$$AF = \frac{N_{fF}}{N_{fL}} = \left[\frac{\Delta T_L}{\Delta T_F}\right]^{1.9}\left[\frac{f_F}{f_L}\right]^{1/3} \exp\left[1414\left(\frac{1}{T_F} - \frac{1}{T_L}\right)\right] \tag{64.14}$$

where AF = acceleration factor

f_F = cyclic frequency in the field

f_L = cyclic frequency in the lab

T_F = maximum temperature of the thermal cycle in the field (K)

T_L = maximum temperature of the thermal cycle in the lab (K)

ΔT_F = difference between maximum and minimum temperature of the thermal cycle in the field

ΔT_L = difference between maximum and minimum temperature of the thermal cycle in the lab

Figure 64.7 contains experimental failure data for a ceramic ball grid array (CBGA) cycled under the same two conditions. The predicted acceleration factor was calculated to be 3.2 employing Eq. (64.14). This predicted value correlates quite well with the CBGA data (acceleration factor ranges from 2.9 to 3.6). Note that this approach tends to be overly conservative when mapping large lab ΔT into small field ΔT (in the case of minicycles, to be discussed in a subsequent section).

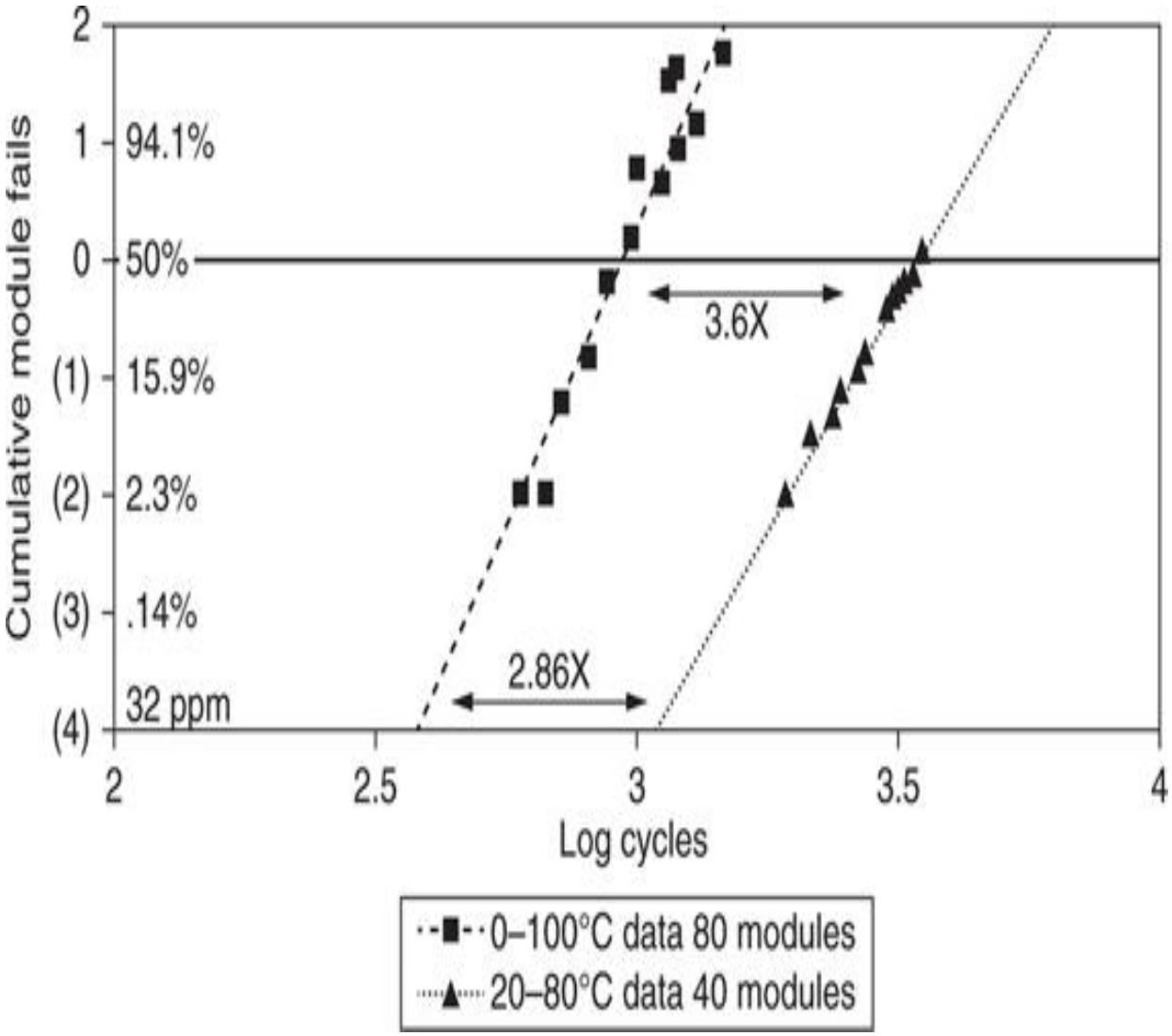


FIGURE 64.7 Weibull plots for a CBGA package cycled under two different loading conditions. Solid triangles and the dotted line are employed to indicate failures and associated failure distribution of a CBGA package cycled from 20 to 80°C (the least severe case presented in this figure). Solid squares and the dashed line indicate the failures and associated distribution for the identical package cycled from 0 to 100°C. Notice that an increase in the severity of the thermal cycle loading conditions (from 20 to 80°C to 0 to 100°C) creates an associated decrease in fatigue life. (*Reprinted with permission from J. Lau*, Ball Grid Array Technology, *McGraw-Hill, 1995, p. 162*.)

64.2.4.3 Effect of Lead-Free Conversion.

The acceleration factor equation [Eq. (64.14)] is specifically derived from experimental data for Pb/Sn solder joints. What remains to be conclusively demonstrated is an equivalent acceleration transform for lead-free solder joints. Several

studies have been performed, but there are no acceleration transforms accepted industrywide for lead-free solders. One of the acceleration transforms proposed is discussed in this section. A more comprehensive list of other field life prediction studies can be found in the appendix of IPC-9701-A.[3]

64.2.4.4 Modified Norris-Landzberg Acceleration Transform for Lead-Free Solder. Based on experimental data generated on a select variety of packages, Pan et al. proposed an updated form of the Norris-Landzberg acceleration transform [see Eq. (64.15)].[23]

$$AF = \frac{N_{fF}}{N_{fL}} = \left[\frac{\Delta T_L}{\Delta T_F}\right]^{2.65} \left[\frac{t_F}{t_L}\right]^{0.136} \exp\left[2185\left(\frac{1}{T_F} - \frac{1}{T_L}\right)\right] \tag{64.15}$$

where AF = acceleration factor
t_F = dwell time at high temperature in the field
t_L = dwell time at high temperature in the lab
T_F = maximum temperature of the thermal cycle in the field (K)
T_L = maximum temperature of the thermal cycle in the lab (K)
ΔT_F = difference between maximum and minimum temperature of the thermal cycle in the field
ΔT_L = difference between maximum and minimum temperature of the thermal cycle in the lab

The primary differences between Eqs. (64.14) and (64.15) are that the frequency term is replaced by the dwell time at high temperature, and the constants have been revised. This equation has been shown by Pan et al. to predict well within the temperature range of 0 to 100°C. However, predictions are less accurate for temperatures outside of this range.[23]

Although the aforementioned proposed acceleration transform is a first-order estimate, much more data would be needed to validate or improve this estimate. Several additional variables must be evaluated to study their impact on the acceleration transform. Some of the variables that impact the acceleration transform include the following:

- *Effect of different package types* The differential strain imparted on solder joints in a ceramic flip-chip ball grid array (FCBGA) is quite different from that imparted on a thin small outline package (TSOP) package, for example. As a result, the acceleration factors from one may not necessarily apply to the other. The construction and effective CTE mismatch of the packages to be qualified must be as close as possible to the packages tested.[23]
- *PWB thickness effect* A thick board is likely to constrain a package more rigidly than a thin board. Similarly, the number of layers in the board could significantly alter its overall stiffness. Tests are frequently done on thinner boards because they are less costly and easier to fabricate. However, if the end-use condition entails the use of a thicker board, IPC-9701 recommends performing the test on at least two different board thicknesses so that the data can be extrapolated to a range of board thicknesses. The effect of board stiffness on lead-free packages appears to be similar to that on Pb/Sn packages, as shown in Sec. 63.3.3 of Chap. 63.
- *Cycling frequency* As evidenced in the study performed by Pan et al. [23] and by Clech,[24] the temperature cycling frequency could have a significant effect on the reliability of the packages being tested. Both the ramp rate and the dwell time affect the results. Most of the damage accumulation during temperature cycling occurs in the hot dwell part of the cycle. A reduction in dwell time reduces the amount of damage accumulated per cycle, which in turn means longer solder fatigue life. A long hot dwell

would result in almost complete creep stress relaxation in the solder joints. Consequently, some studies have indicated that a longer dwell time could result in eventual creep saturation.[25,26,27] Increasing the dwell time has shown some reduction in fatigue life in some studies, but the reduction was not very significant in some of those.[28] In addition to hot dwell time, ramp rate of heating and cooling also impacts the effective fatigue life of lead-free solder joints. The amount of reduction in lead-free solder fatigue life due to ramp rate is a function of the package type. Packages with higher effective CTE mismatched substrates (e.g., CBGAs) are more sensitive to the ramp rate than packages with a less differential strain (e.g., plastic ball grid arrays [PBGAs]).

- *Temp cycling range* Clearly, the higher the temperature cycling range, the lower the fatigue life of the solder joints. Some studies have also indicated that an increased average temperature could also result in a reduction in the fatigue life of lead-free solder joints. In other words, both factors—high maximum temperature and high average temperature—could contribute to a reduction in solder fatigue life.[24]
- *The distance from neutral point (DNP) effect* This is the effective distance along the diagonal of the package, from the center to its outermost corner. Some studies have indicated that the DNP plays a significant role in altering the acceleration transforms of a lead-free package.[24]
- *Size and orientation of tin (Sn) grains*[29] Depending on the cooling rate, Pb free solders containing a high percentage of Sn tend to have very large Sn grains with varied orientation. Sn has very anisotropic material properties, and consequently, the bulk properties of the Pb-free solder joints could change significantly depending on the size and orientation of the Sn grains in any given solder joint. Consequently, the strength of the solder joints within a

single BGA could vary significantly. In other words, the joints at the high stress regions may not be the first to fail. This random orientation of Sn grains within a solder joint poses a significant challenge in determining the fatigue life and acceleration factors of Pb-free solder joints.[29]

It has also been observed that while the ductility of Pb/Sn increases with aging, the ductility of lead-free solders tends to decrease with aging.[30] In other words, the strain/strain rate characteristics of lead-free solders could change with aging. Further studies are also needed to quantify fully the aging effect and incorporate it into long-term field life prediction models.

64.2.4.5 Backward Compatibility. On small PWBs with relatively few components, it is possible to convert all the components to lead-free assemblies at once. However, in the transition to lead-free assemblies, there will be instances where not all the components on a complex PWB can be converted to lead-free solder. This would inevitably create situations where both tin-lead and lead-free parts are attached on the same board.

Consequently, the use of Pb/Sn paste to assemble lead-free components (backward compatibility) would have to be studied. Component suppliers do not recommend the use of mixed solder metallurgies for a variety of reasons:

- The peak reflow temperature of lead-free solders is higher than that of tin-lead solders. Assembling lead-free components with Pb/Sn paste would involve limiting the peak reflow temperature to that of Pb/Sn components (~220°C). Consequently, the lead-free solders may not fully melt during reflow, resulting in unpredictable long-term solder joint reliability.
- The thermal gradients across components and the PWB could vary significantly, and as a result, it is difficult to

ensure that the microstructure formed across the solder joints is consistent.

- There are no known and validated acceleration transforms to predict the field reliability of lead-free components assembled with Pb/Sn paste. Thus, even if the assembled parts pass temperature cycling relative to their Pb/Sn and lead-free counterparts, it is difficult to extrapolate to field conditions and predict how they will perform when subjected to actual end-use conditions.
- There is very little data on the bend/shock resistance of mixed-metallurgy solder joints. The intermetallics formed at the package-joint and PWB-joint interfaces can be quite complex and different. The resistance of these intermetallics to mechanical loading has not been characterized.

There is very little information in the literature on the process consistency of backward-compatible assemblies and their consequent long-term reliability. Some information can be found in References 28, 31, 32, and 34. Some reliability data have been shown to indicate that the reliability of backward-compatible assemblies can be significantly improved if the SnAgCu ball melts fully and good dissolution with the Pb/Sn paste is achieved.[31] However, the factors that influence the degree of dissolution, such as the peak temperature and time above liquidus (TAL), are generally difficult to control consistently. Moreover, the amount of dissolution obtained is a function of the solder ball volume relative to the volume of paste used. Consequently, packages with smaller solder ball pitch could also be more sensitive to assembly process variations in backward-compatible assemblies.

In view of all the unknowns and process dependencies outlined, the assembly of lead-free components with Pb/Sn paste is generally not recommended. If it has to be performed, detailed studies should be conducted to

benchmark the consistency of the assembly process as well as the consequent effect on the long-term reliability (both thermomechanical and mechanical) of the assemblies.

64.2.5 Power and Minicycles

Consider a processor in a server. The server may only be powered down and back up one time per month (a conservative estimate). Power-downs and power-ups are referred to as *power cycles*. A reliability estimate could be made assuming that one thermal cycle occurred per month from the operating temperature within the region of the package to ambient. This would yield a tremendously high lifetime estimate that would unfortunately be misleading. It is important to consider what happens to the packaged device during typical usage of the server. The device temperature will probably increase during usage and decrease when not in use. These smaller temperature rises can occur multiple times throughout a day. These types of thermal conditions are referred to as *minicycles* and can have a dramatic impact on the long-term reliability of an interconnect. Section 64.2.6.3 presents a technique for incorporating minicycles and power cycles in a lifetime assessment.

64.2.5.1 Miner's Rule. Miner's rule[33] is employed when attempting to assess fatigue life under multiple fatigue loading conditions. It is commonly used when addressing the combined power and minicycle thermal loading conditions described in the previous section. Miner's rule is based on the premise that fatigue damage accumulates over each cycle. When a critical quantity of damage has been imparted on a system, the system will fail.

Miner's rule states that the sum of the ratios of the actual number of cycles to fail of a given fatigue loading condition

to the number of cycles to fail if only that fatigue loading condition occurs is equal to 1. Equation (64.16) contains a general expression of Miner's rule.[9]

$$\Sigma \frac{N_{ai}}{N_{oi}} = 1.0 \qquad (64.16)$$

where N_{ai} = actual number of fatigue cycles that occur
N_{oi} = number of cycles to fail if only that specific fatigue cycle occurred

Miner's rule can be expanded and rearranged for power cycle and minicycle considerations. Equation (64.17) contains that expression.

$$N_{poweractual}/N_{poweronly} + N_{miniactual}/N_{minionly} = 1.0 \qquad (64.17)$$

where $N_{poweractual}$ = actual number of power cycles that occur before failure
$N_{poweronly}$ = number of power cycles to fail if only power cycles occur
$N_{miniactual}$ = actual number of power cycles that occur before failure
$N_{minionly}$ = number of minicycles to fail if only minicycles occur

The Norris-Landzberg acceleration transformation can be combined with Miner's rule to estimate the fatigue life of a package. Note that the Norris-Landzberg method tends to be conservative when assessing minicycles whose changes in temperature are much smaller than the experimental temperature change applied when qualifying the part.

64.2.6 Practical Examples

64.2.6.1 Comparing the Reliability of Two Packages Qualified under Different Thermal Loading

Conditions

Given: Thermal cycle qualification data and test conditions for packages A and B (Table 64.4)

TABLE 64.4 Package A and Package B Qualification Data

	Package A	Package B
T_{max}	110°C	100°C
T_{min}	−10°C	0°C
Frequency	1 cycle/h	1 cycle/h
N_{50} (number of cycles to 50% failure)	2291	3575

Solution: It is necessary to decide which thermal profile will be kept as a constant and which one will be mapped. This problem can be solved both ways—each temperature cycling condition could be mapped into the other. Either method requires utilizing Eqs. (64.10) and (64.14) to transform the number of cycles to failure. For clarity, let condition A refer to the thermal conditions that package A was qualified under, and let condition B refer to the qualification test conditions to which package B was exposed.

64.2.6.2 Map Package A Lifetime into Package B Thermal Loading Conditions. Using Eq. (64.10), one would derive Eq. (64.18).

$$AF = \frac{N_{fAA}}{N_{fAB}} \tag{64.18}$$

where AF = acceleration factor

N_{fAA} = number of cycles to failure in package A cycled from –10 to 125°C (condition A)

N_{fAB} = number of cycles to failure in package A cycled from 0 to 100°C (condition B)

Equation (64.14) can be rearranged to yield Eq. (64.19).

$$AF = \left[\frac{\Delta T_B}{\Delta T_A}\right]^{1.9} \left[\frac{f_A}{f_B}\right]^{1/3} \exp\left[1414\left(\frac{1}{T_A} - \frac{1}{T_B}\right)\right] \tag{64.19}$$

where AF = acceleration factor

f_A = cyclic frequency for condition A (1 cycle/h)

f_B = cyclic frequency for condition B (1 cycle/h)

T_A = maximum temperature for condition A (110°C, 383 K)

T_B = maximum temperature for condition B (100°C, 373 K)

ΔT_A = difference between maximum and minimum temperature of condition A (120)

ΔT_B = difference between maximum and minimum temperature of condition B (100)

Substitution of the values in Table 64.4 into Eq. (64.19) yields an acceleration factor of 0.641. Package A would be expected to survive 3574 cycles ($N_{fAB} = N_{fAA}/AF$ = 2,291/0.641) if subjected to condition B thermal loading conditions. The packages appear to be comparable.

64.2.6.3 Assessing Expected Field Life of a New Package Based on Thermal Cycle Data

Given: Thermal cycle qualification data for a new ball grid array package (use package B in Table 64.4) and estimates of field loading conditions (see Table 64.5)

TABLE 64.5 Field Conditions for Example

	Power Cycle	Minicycle
T_{max} (°C)	65	80
T_{min} (°C)	25	65
ΔT (°C)	40	15
Frequency	1 cycle per 30 days, 30 min duration	4 cycles per day, 60 min duration

Solution: The process for solving this problem is as follows. The experimentally obtained qualification data (presented in Table 64.4) must be mapped into number of power cycles to failure and number of minicycles to failure. These estimates assume that only power cycles occur and that only minicycles occur (that is the underlying assumption when mapping the experimental data to the end-use power cycle and minicycle conditions). After mapping the experimental data into field conditions, Miner's rule is employed to assess the number of cycles to fail based on the simultaneous occurrence of both power cycles and minicycles throughout the package lifetime.

When employing Eq. (64.14) to map power cycles and minicycles, it is important to consider the implications of how the *frequency* term is interpreted. The Norris-Landzberg approach assumes that the frequency corresponds to the duration of the cycle, not how often that cycle occurs.

Equation (64.14) can be employed to determine the acceleration factors. Equations (64.20) and (64.21) contain the expressions for power cycles and minicycles, respectively.

$$AF = \left[\frac{\Delta T_L}{\Delta T_P}\right]^{1.9} \left[\frac{f_P}{f_f}\right]^{1/3} \exp\left[1414\left(\frac{1}{T_P} - \frac{1}{T_L}\right)\right] \tag{64.20}$$

where AF = acceleration factor
f_P = cyclic frequency for a power cycle (2 cycles/h)
f_L = cyclic frequency in the lab (1 cycle/h)
T_P = maximum temperature of a power cycle (65°C, 338 K)
T_L = maximum temperature of the thermal cycle in the lab (100°C, 373 K)
ΔT_P = difference between maximum and minimum temperature of a power cycle (40)
ΔT_L = difference between maximum and minimum temperature of the thermal cycle in the lab (100)

$$AF = \left[\frac{\Delta T_L}{\Delta T_M}\right]^{1.9} \left[\frac{f_M}{f_L}\right]^{1/3} \exp\left[1414\left(\frac{1}{T_M} - \frac{1}{T_L}\right)\right] \tag{64.21}$$

where AF = acceleration factor
f_M = cyclic frequency for a minicycle (1 cycle/h)
f_L = cyclic frequency in the lab (1 cycle/h)
T_M = maximum temperature of a minicycle (80°C, 353 K)
T_L = maximum temperature of the thermal cycle in the lab (100°C, 373 K)
ΔT_M = difference between maximum and minimum temperature of a minicycle (15)
ΔT_L = difference between maximum and minimum temperature of the thermal cycle in the lab (100)

Substitution of the data in Tables 64.4 and 64.5 yields a power cycle acceleration factor of 10.6 and a minicycle acceleration factor of 45.6. Equation (64.10) can be rearranged to yield Eq. (64.22).

$$N_{fi} = AF_i \times N_{fL} \tag{64.22}$$

where N_{fi} = number of cycles to fail under minicycle (i) or power cycle (i)
N_{fL} = number of cycles to fail in the lab
AF_i = acceleration factor for minicycle (i) or power cycle (i)

Substitution of the lab number of cycles to fail from Table 64.4 into Eq. (64.22) for minicycle and power cycles yields 37,895 power cycles to fail (assuming only power cycles occur) and 163,020 minicycles to fail (assuming only minicycles occur).

Miner's rule [Eq. (64.17)] can now be applied to determine the actual number of cycles to fail. It is important to note that at this stage the number of minicycles to fail if only minicycles occur and the actual number of power cycles to fail if only power cycles occur is known. The actual number of minicycles and power cycles to fail remains unknown; thus Eq. (64.17) is only one equation, whereas two unknowns still exist: $N_{poweractual}$ and $N_{miniactual}$.

Therefore, it is important to consider the number of minicycles that occur per power cycle. In this case, there is one power cycle per 30 days and 4 minicycles per day. This equates to 120 minicycles per power cycle. Equation (64.17) can now be written as shown in Eq. (64.23).

$$N_{poweractual}/N_{poweronly} + K^* N_{poweractual}/N_{minionly} = 1.0 \tag{64.23}$$

where $N_{poweractual}$ = actual number of power cycles that occur before failure
$N_{poweronly}$ = number of power cycles to fail if only power cycles occur
$N_{miniactual}$ = actual number of minicycles that occur before failure
$N_{minionly}$ = number of minicycles to fail if only minicycles occur
K = number of minicycles that occur per power cycle

Equation (64.23) can be solved for the number of power cycles to fail, which yields a value of 1311 power cycles or 107.8 years. It is important to employ a confidence factor (safety factor). Taking 2 as a standard safety factor, the final fatigue life is estimated at 53.9 years.

64.3 MECHANICAL RELIABILITY

As discussed in Sec. 63.3.11 of Chap. 63 the surface finishes used on packages have been shown to have a significant impact on the mechanical robustness of BGA packages. With increased I/O density, finer pitch, and new substrate technologies (e.g., flex substrates), BGA packages tend to be more fragile and susceptible to mechanically induced failures. These failures are mostly catastrophic in nature, but the loading conditions could vary from bending during production assembly to shock due to shipping or accidental drops. Both monotonic and cyclic conditions could result in catastrophic failure either in manufacturing or field operating conditions. This section focuses on the test methodologies used in quantifying and benchmarking different mechanically induced loading conditions on printed circuit assemblies (PCAs). In general, the mechanical loading conditions that an assembly undergoes could be classified by the strain and strain rate level, as illustrated in Fig. 64.8. As Fig. 64.8 shows, bend and shock tests each cater to different ranges of the strain/strain rate spectrum.

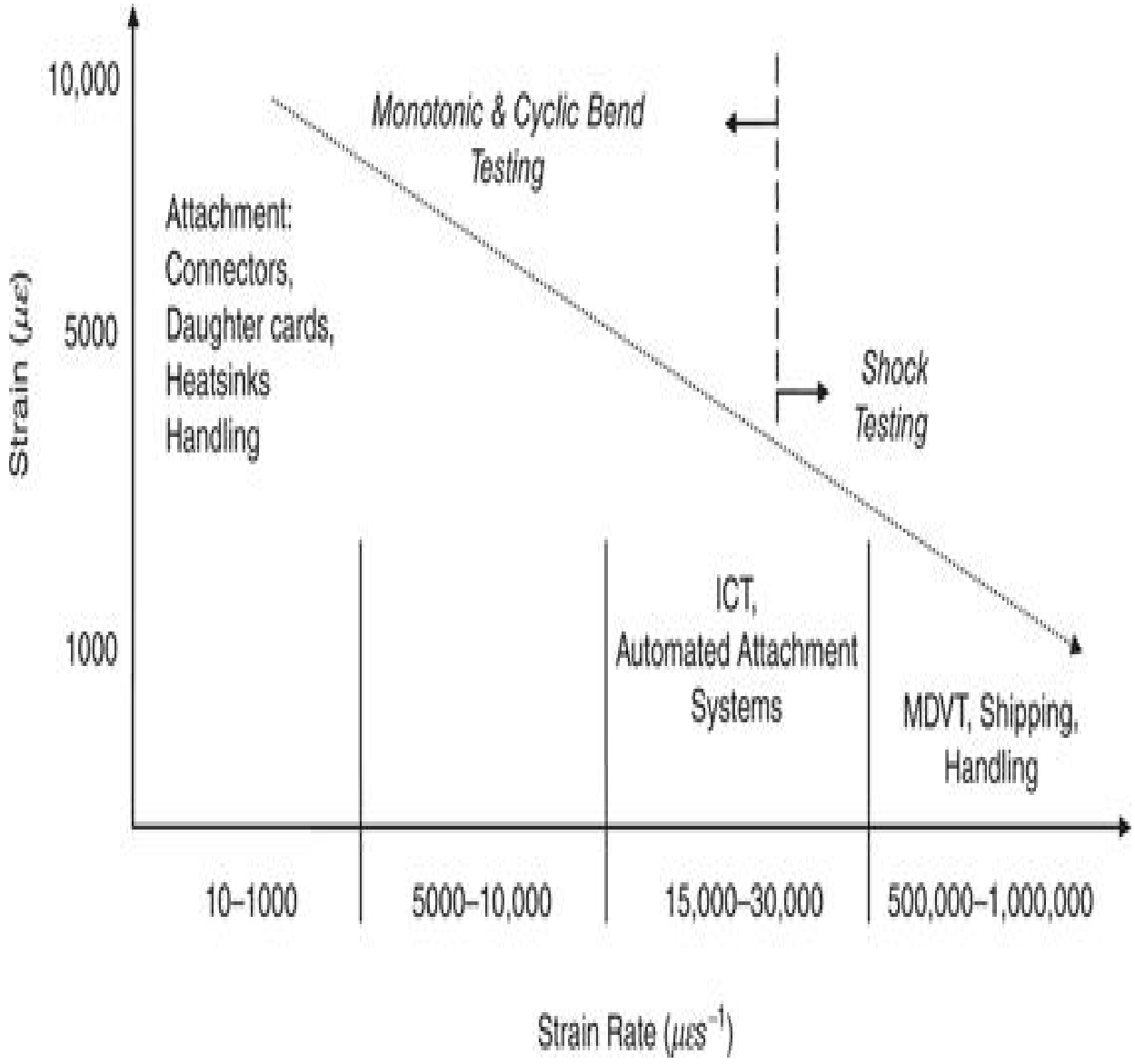


FIGURE 64.8 Spectrum of strain/strain rate in which mechanical testing fits with the assembly process. The monotonic and cyclic bend testing focuses on high-strain, low-strain rates, whereas the shock testing focuses on low-strain, high-strain rates.

64.3.1 Monotonic Bend Testing

Monotonic (bend-to-failure) testing is designed to simulate the assembly conditions to which a PCA is subjected in manufacturing. A variety of assembly steps impart loading conditions that are similar to a monotonic bend test, such as

heatsink attachment, connector attachment, in-circuit test (ICT), handling, and card-cage installation. These assembly steps could mechanically induce several different failure modes. Monotonic bend testing in a controlled condition serves two critical purposes:

- A comparative assessment can be performed between different package types and material sets.
- The failure modes induced at different strain levels can be catalogued. Production operations can then be characterized with strain gauges and compared with the monotonic bend test data to determine whether excessive strain was applied on the PCA during any given assembly step.

To ensure consistency in results and to allow for ease of comparison, an industry standard test method has been developed and published jointly by IPC and JEDEC (IPC/JEDEC-9702).[35] This test method outlines in detail the requirements of the monotonic bend test method. The test setup is illustrated in Fig. 64.9. The typical failure modes observed at the solder joint interconnects are shown in Fig. 64.10.

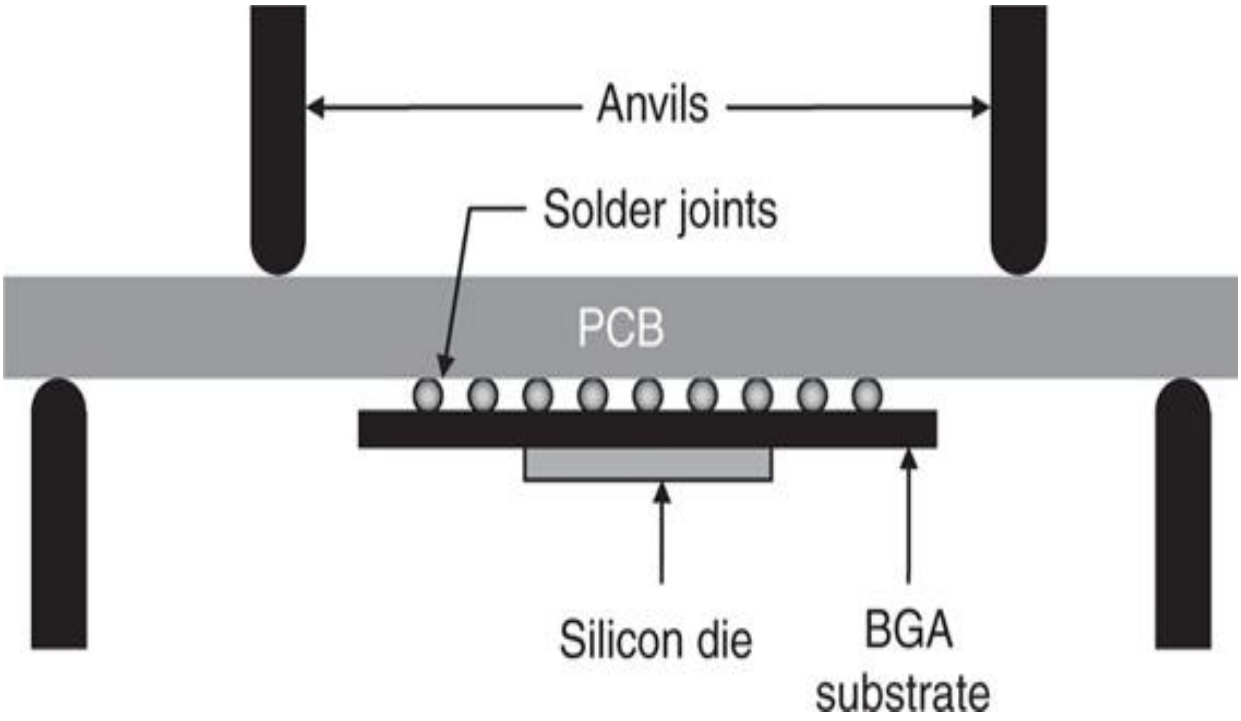


FIGURE 64.9 Schematic of four-point bend test setup. A four-point bend test setup is used to determine the strains-to-failure rate of the BGA solder joints.

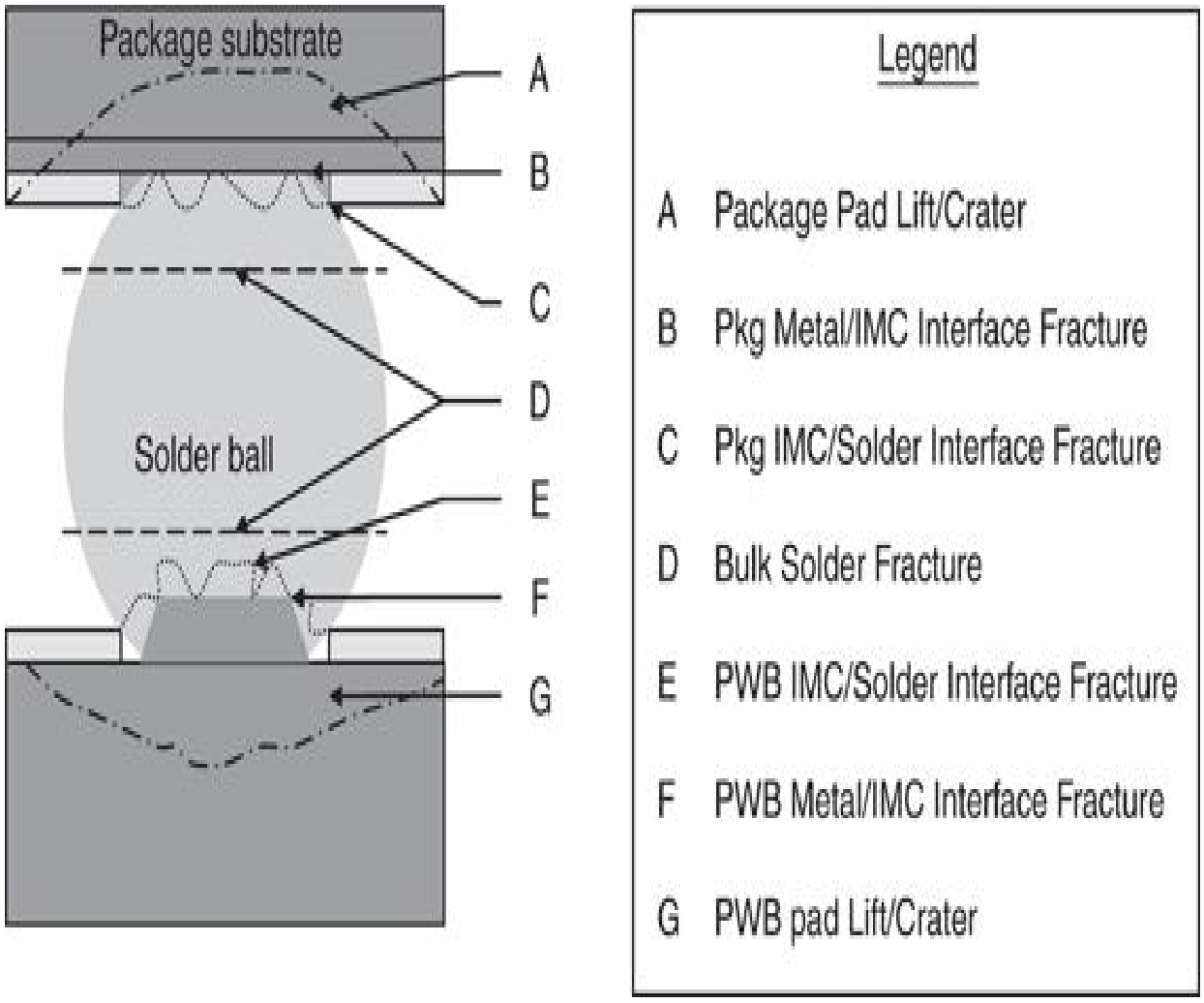


FIGURE 64.10 Different interconnect failure modes.

64.3.1.1 Strain Measurement in Production. A common procedure for performing strain measurements on live PCAs during production is outlined in IPC/JEDEC 9704.[36] This provides a comprehensive guideline on ways to perform strain measurements and reporting the recorded data. It also includes sample guidelines on the amount of strain/strain rate considered acceptable as a function of board thickness. One assembly process that is particularly susceptible to high strain/strain rates is ICT. Once the ICT fixture is engaged, there is a sudden spike in strain (high strain rate), which is again repeated when the fixture is disengaged, as shown in Fig. 64.11.

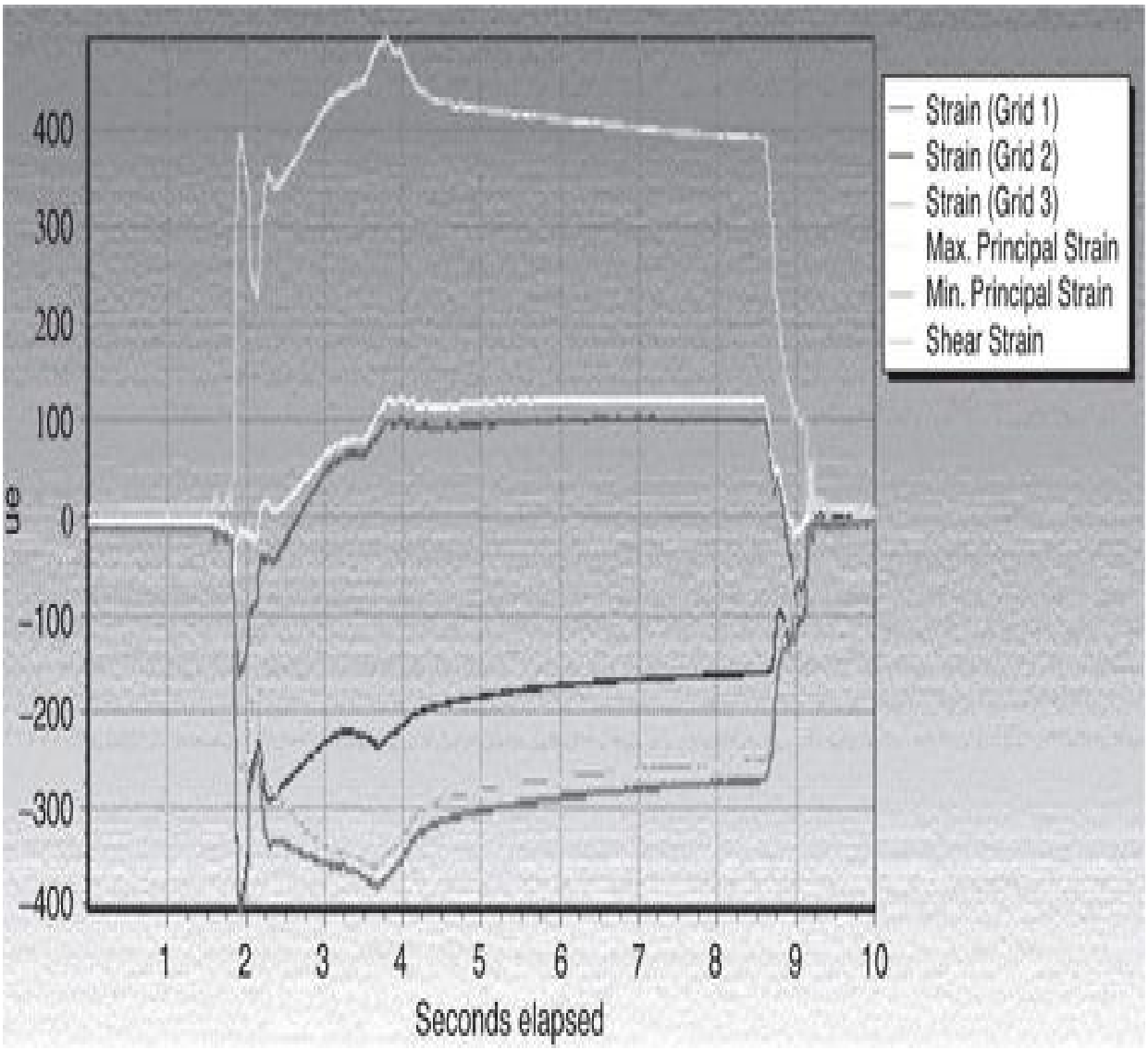
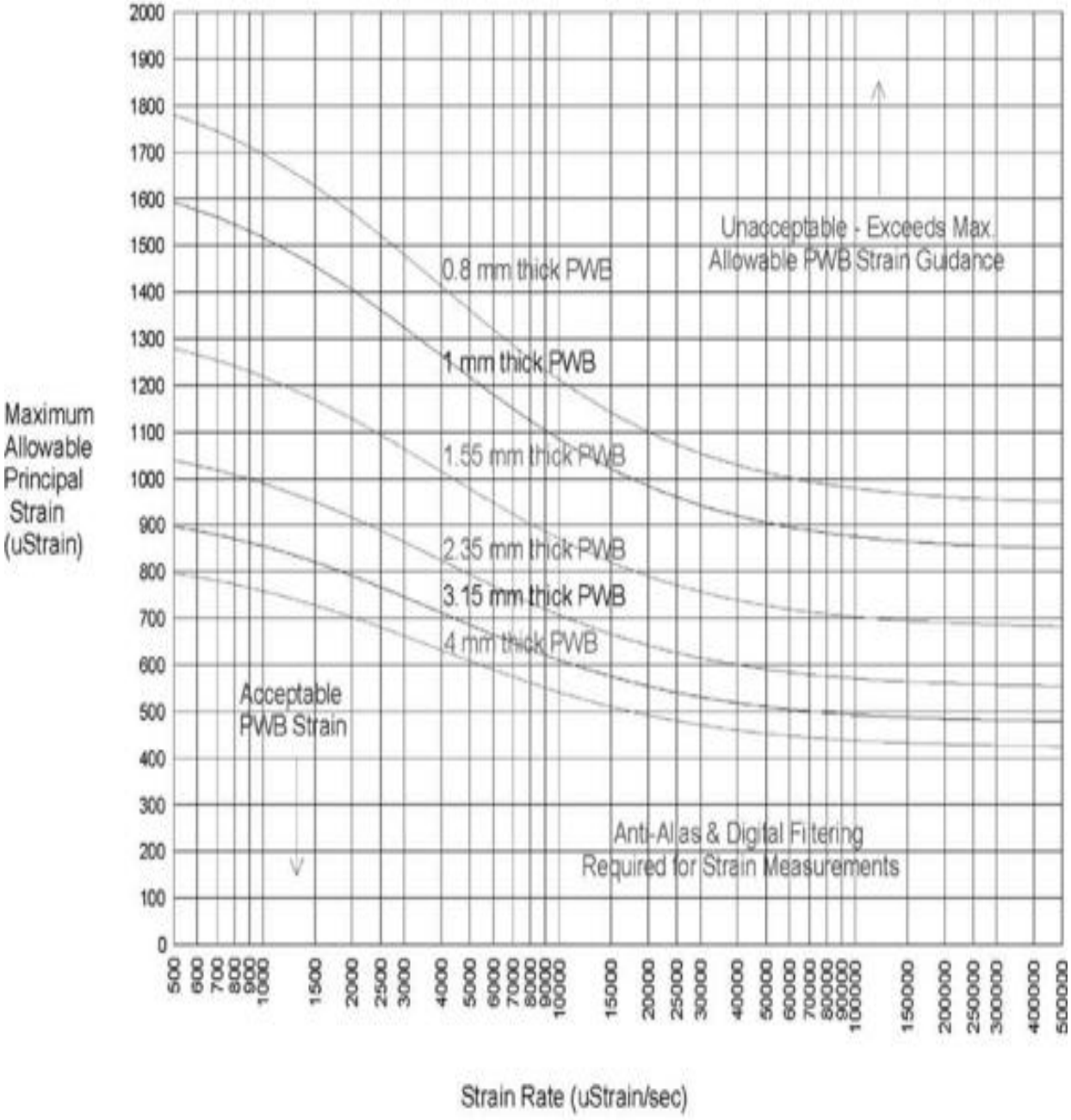


FIGURE 64.11 Strain versus time plot of an actual ICT fixture as it is engaged, the test is performed, and the fixture is subsequently disengaged. The sharp increase in strain during engagement and disengagement is the source of the high strain rate. The fixture is engaged at high speed to improve electrical contact between the probe pins and the PWB test pads.

Based on experimentally generated data on the production floor and in controlled four-point bend tests described earlier, guidelines can be developed on the maximum range of strain for a given strain rate that would be acceptable for a package in different production operations. A typical example of such a guideline is given in Fig. 64.12. It is important to note that this is just a sample guideline.



PWB strain = max. principal strain (absolute value) measured immediately adjacent to cornermost solder joint

Strain rate = change in strain (absolute value) between consecutive readings

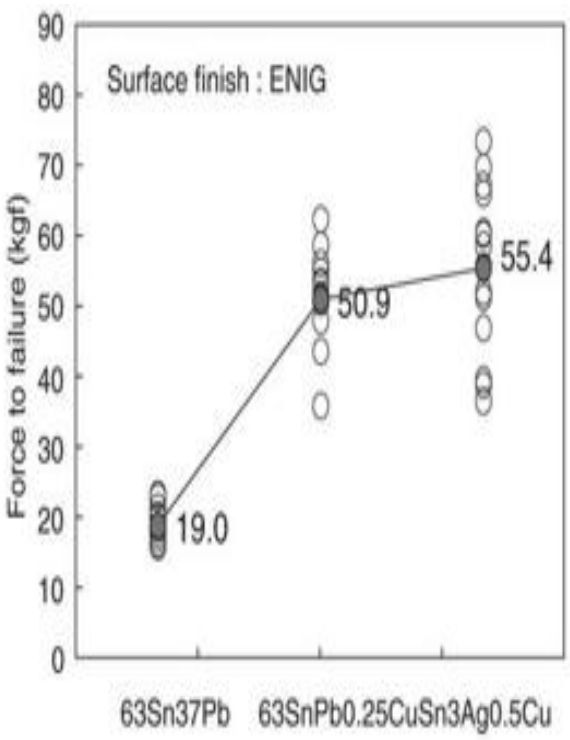
Max. allowable strain = sqrt[2.35/(PWB thickness)]*[550 + 2.2e6/(strain rate + 4000)]

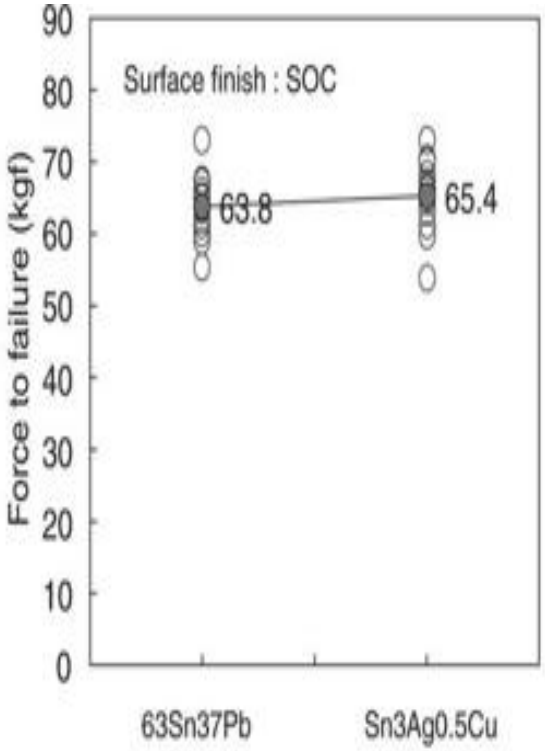
Units:

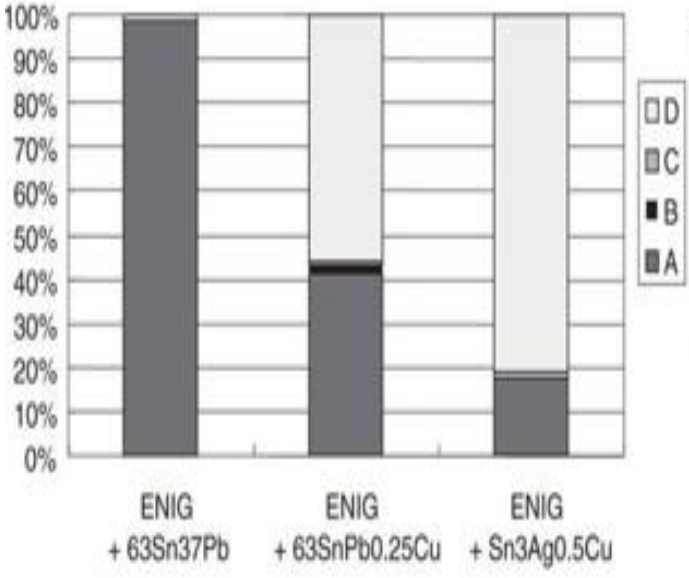
- Strain [uStrain]
- Strain rate [uStrain/sec]
- PWB thickness [mm]

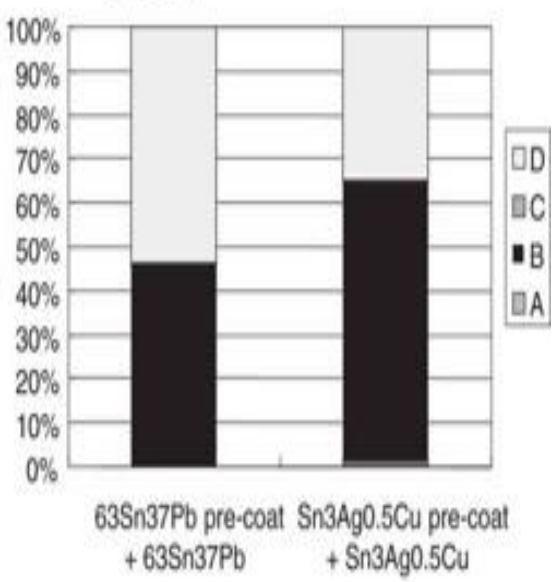
FIGURE 64.12 Typical example of strain/strain rate limits as a function of PWB thickness for BGA solder joint interconnect failure. Note that the acceptable strain limit decreases with increasing strain rate. Note also that for a given strain rate, the maximum acceptable strain limit decreases as the PWB thickness decreases. (*Reprinted with permission from Sun Microsystems, Inc*.)

64.3.1.2 Effect of Lead-Free Conversion. Because of the conversion to lead-free solder, the intermetallics formed at the package-joint and PWB-joint interface would be different from those in Pb/Sn assemblies. Consequently, the response to bending of a lead-free assembly would be significantly different from that of a Pb/Sn assembly. There are relatively little experimental data in the industry comparing the mechanical reliability of lead-free soldered assemblies with Pb/Sn assemblies. One data set showing a relative comparison between Pb/Sn and SnAgCu for two different surface finishes is shown in Fig. 64.13.[37]









Failure Mode Legend:

Mode A: within the solder joint on the substrate side

Mode B: pad lift on the substrate side

Mode C: within the solder joint on the board side

Mode D: pad lift on the board side

FIGURE 64.13 Data set comparing the force-to-failure rate of Pb/Sn, Pb/Sn/Cu and Sn/Ag/Cu assemblies for two different surface finishes (ENIG and SOC). The histograms show a comparison of the different failure modes obtained in the bend tests.[37] All samples were tested within one day of board assembly. (*Reprinted with permission from Kyocera SLC Technologies. /© [2005] IEEE*.)

The results in Fig. 64.13 show the following:

- For ENIG surface finish packages, the average force-to-failure value for the SnAgCu assemblies is almost three times that of the Pb/Sn assemblies. This is because the SnAgCu joints are stiffer than the Pb/Sn joints.
- Failure mode A is significantly more pervasive in the Pb/Sn assemblies but not as much in the SnAgCu assemblies. Thus, the propensity for brittle solder joint fracture is higher in the Pb/Sn assemblies with ENIG.
- The introduction of a small amount of copper in the Pb/Sn assemblies tends to increase the bending strength of the Pb/Sn assemblies by more than two times.
- The average force to failure with a solder-on-copper (SOC or SOP) surface finish is higher than that with ENIG, especially for the Pb/Sn solder joints. For the SnAgCu joints, there is a marginal increase in relative strength.

Thus, mechanical bend strength is a function of the solder metallurgy and the surface finish used. These results indicate that SnAgCu solder joints are stiffer and have a higher average force-to-failure value compared to Pb/Sn joints with the same surface finish. Another important factor in the bend strength of solder joints is the time after reflow, as shown in Fig. 64.14.[37]

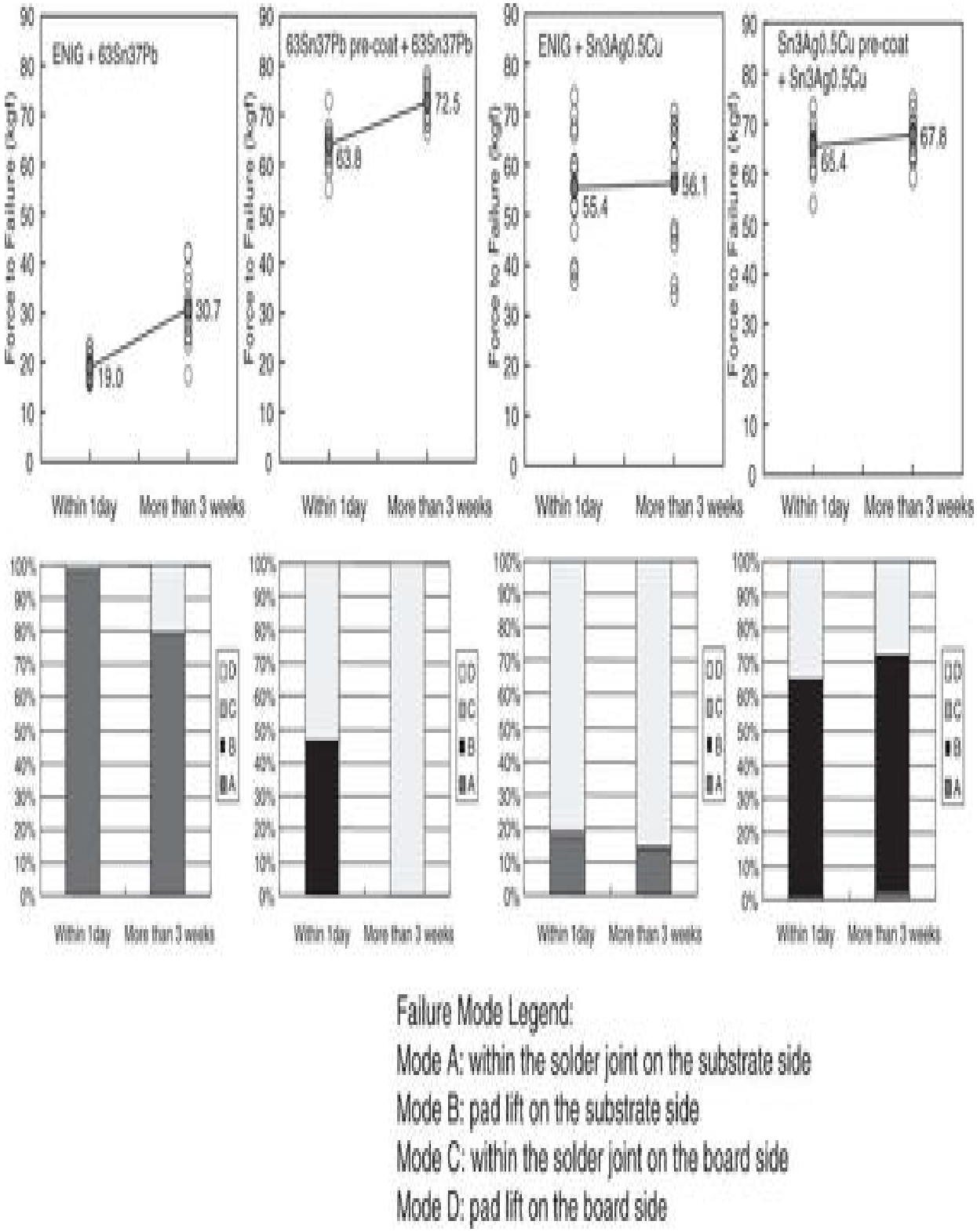


FIGURE 64.14 Data set comparing the force-to-failure value of Pb/Sn and Sn/Ag/Cu assemblies for two different surface finishes (ENIG and SOP) as a function of time after reflow. The histograms show a comparison of the different

failure modes obtained in the bend tests. (*Reprinted with permission from Kyocera SLC Technologies. /© [2005] IEEE*.)

The results in Fig. 64.14 show the following:

- For ENIG surface finish packages, Pb/Sn joints are more sensitive to time after reflow than SnAgCu joints. The average force-to-failure value of Pb/Sn joints with ENIG increased by more than 50 percent, whereas the average force-to-failure value of SnAgCu with ENIG did not change noticeably over time.
- For solder pre-coat (SOP) packages, the strength of Pb/Sn joints increased by slightly more than 10 percent over three weeks, whereas the strength of SnAgCu joints with SOP does not change noticeably over time.

Thus, mechanical bend strength is a function of the time after reflow along with solder metallurgy and surface finish. The underlying failure mechanisms have not been understood clearly enough to explain the dependence on time after reflow.

64.3.2 Cyclic Bend Testing

In addition to monotonic loading conditions, certain repetitive operations could also lead to mechanical failures. A typical example is a PWB used in cell-phone applications. The PWB could be subjected to multiple small deflections each time the cell-phone keypad is pressed. This can cause an incremental deterioration in the mechanical response of the PWB and lead to solder joint interconnect failures in BGAs mounted on the PWB. This sort of failure mechanism is more prevalent in relatively thin PWBs used in cell-phone applications. However, similar failures could also occur if, for example, multiple runs of ICT are performed on PCAs in high-end server/network applications. An industry standard test

method has been developed by JEDEC to characterize the response of a PCA to cyclic loading conditions (JESD22-B113).[38] The layout of the test board as specified in the test method is similar to that for the monotonic four-point bend test. Some data on the cyclic bend response of SnAgCu solder joints can be found in Reference 39.

64.3.3 Shock Testing

As with bend testing, a shock test methodology is needed to simulate the shock conditions that a PCA may undergo during assembly, shipping, and handling conditions. Shock test conditions usually induce strain rates on the order of 100,000 $\mu\varepsilon$/s. (microstrain per second), whereas typical monotonic bend test strains are on the order of 10,000 $\mu\varepsilon$/s. Thus, the strains to failure under typical shock test conditions are lower than the strains to failure under typical bend test conditions. However, the failure modes could be different. Hence the need to characterize both bend and shock conditions. There are different classifications of typical shock conditions. For example, those experienced by handheld products [cell-phones, personal digital assistants (PDAs), etc.] are different from those experienced by typical network/server products. The former requires resistance to more stringent shock levels (~1500 G),[40] whereas the latter requires resistance to shock levels on the order of ~500 G. An example of the typical shock test conditions applicable to these product categories is summarized in Table 64.6.

TABLE 64.6 Examples of Typical Shock Conditions Used for Different End-Use Environments (the Specific Conditions Tested Depend on the End Users)

Test Parameters	Typical Field Conditions	
	Handheld Products	Network/Server Products
Acceleration peak (G)	1500–2900	100–400
Pulse duration (ms)	0.3–0.5	1.2–2

In addition to shock testing, several component suppliers also perform drop testing. For handheld products in particular, some suppliers prefer to perform board-level drop testing instead. Details of the drop test method are outlined in JESD22-B111.[41] Several component suppliers perform vibration testing in addition to shock testing to simulate shipping conditions.

The design of the carrier tray or chassis in which the PWB is installed could significantly impact the reliability of printed circuit board assemblies (PCBAs). If the resonant frequency of the PCBA matches that of the chassis, and the mode shapes corresponding to the resonant frequency are such that they induce a strain above the critical solder joint failure strain, brittle fracture can occur. Accelerometers and strain gages should be used to characterize both mode shapes and strains in the PWB assemblies mounted on carrier trays or in chassis. The chassis design should be optimized to ensure that the strains that might impact the PCBAs are minimized, especially at the critical locations. Ways to do this include adding stiffeners, frames, and struts in the chassis at critical, high-strain locations.

Finally, an additional way to mitigate shipping failures is to use shock indicators in the shipped product. A typical shock indicator changes color if the applied G values exceed a preset threshold. The use of a shock indicator in products can help in root cause analysis of failed parts.

64.3.4 Ball Shear/Pull Testing

Ball shear testers are employed to quantify the strength of the interface between a solder ball and its package prior to second-level attach. Ball shear experiments can also be employed to assess the solder ball-package pad interface qualitatively. This is accomplished by assessing the failure mode observed during a ball shear experiment.

However, certain failure modes are a function of the speed of the test. The failure modes observed at relatively low speeds (0.0001 to 0.0006 m/s) are different from those observed at high speeds (0.01 to 1.0 m/s). In general, solder shear strength tends to increase with shear speed. It is therefore important that failure mode characterization as a function of shear speed be performed before this technique can be used effectively as an inline monitoring tool to control the quality of substrate lots. To address this, JEDEC has published a revised version of the standard ball shear test to include high speed shear testing procedures (JESD22-B117A[42]).

In addition to speed, a number of other factors could impact the fracture strength of solder joints, including surface finish, pad size, ball diameter, ball metallurgy, and pad construction. All these need to be taken into account when comparing ball shear data across different packages. Another important factor that could impact the force-to-failure and the failure modes induced is the time after reflow. It is preferable to perform the test as early as possible after reflow.[43]

In addition to the high-speed shear/pull test, other methodologies are also being explored to characterize the interface strength of solder joints. One is a Charpy impact type of test.[44] This involves impacting the ball with a pendulum. The amount of energy imparted into the ball is estimated and the failure modes as a function of impact

toughness are catalogued. This test is a sort of mini-shock test designed to produce an effect comparable to the high-speed shear test. Another methodology is the use of a hot pin pull test in which a heated pin is inserted into the solder ball, cooled, and then pulled at high speed. Efforts are being made to measure the force to cause failure, so that pull/shear force or impact energy could be used as a metric to assess the strength or weakness of a joint.

64.3.4.1 Effect of Lead-Free Conversion. Depending on the surface finish, the intermetallics formed in SnAgCu solders are different from those formed in Pb/Sn joints. Refer to Sec. 60.3.11 in Chap. 60 for more details. Preliminary results on high-speed pull/shear testing of SnAgCu joints indicate a higher interfacial fracture rate than Pb/Sn joint. However, the SnAgCu joints exhibited moderately higher fracture strength.[43]

64.4 FINITE ELEMENT ANALYSIS

Finite element analysis (FEA) is a numerical technique used to solve complex boundary value problems. It involves discretizing a complex geometry into smaller simpler geometries that can be represented by a set of differential equations. These equations can then be solved numerically to determine the deformation of the overall structure subjected to structural, thermal, or other loading conditions. FEA is a powerful numerical tool that has been used to assess the reliability of solder joints. FEA can be employed to

- Estimate the fatigue life of a new package
- Compare reliabilities of different packaging options
- Assess impact on reliability due to material and design changes to the package

- Assess impact on reliability due to PWB material and design changes
- Determine changes in warpage due to package density and location

FEA has been used effectively in simulating thermomechanical, bending, and shock conditions. This section focuses on the use of FEA to determine the lifetime of packages subjected to thermomechanical strains, and the use of bend test simulations to determine the factors that influence the bend strength of a package.

64.4.1 FEA for Thermomechanical Lifetime Assessment

FEA lifetime assessments are typically broken down into four phases:

- Phase 1: global model
- Phase 2: local model
- Phase 3: single-joint lifetime assessment
- Phase 4: statistics-based package reliability estimate

Figure 64.15 shows the interrelationships between these four phases.

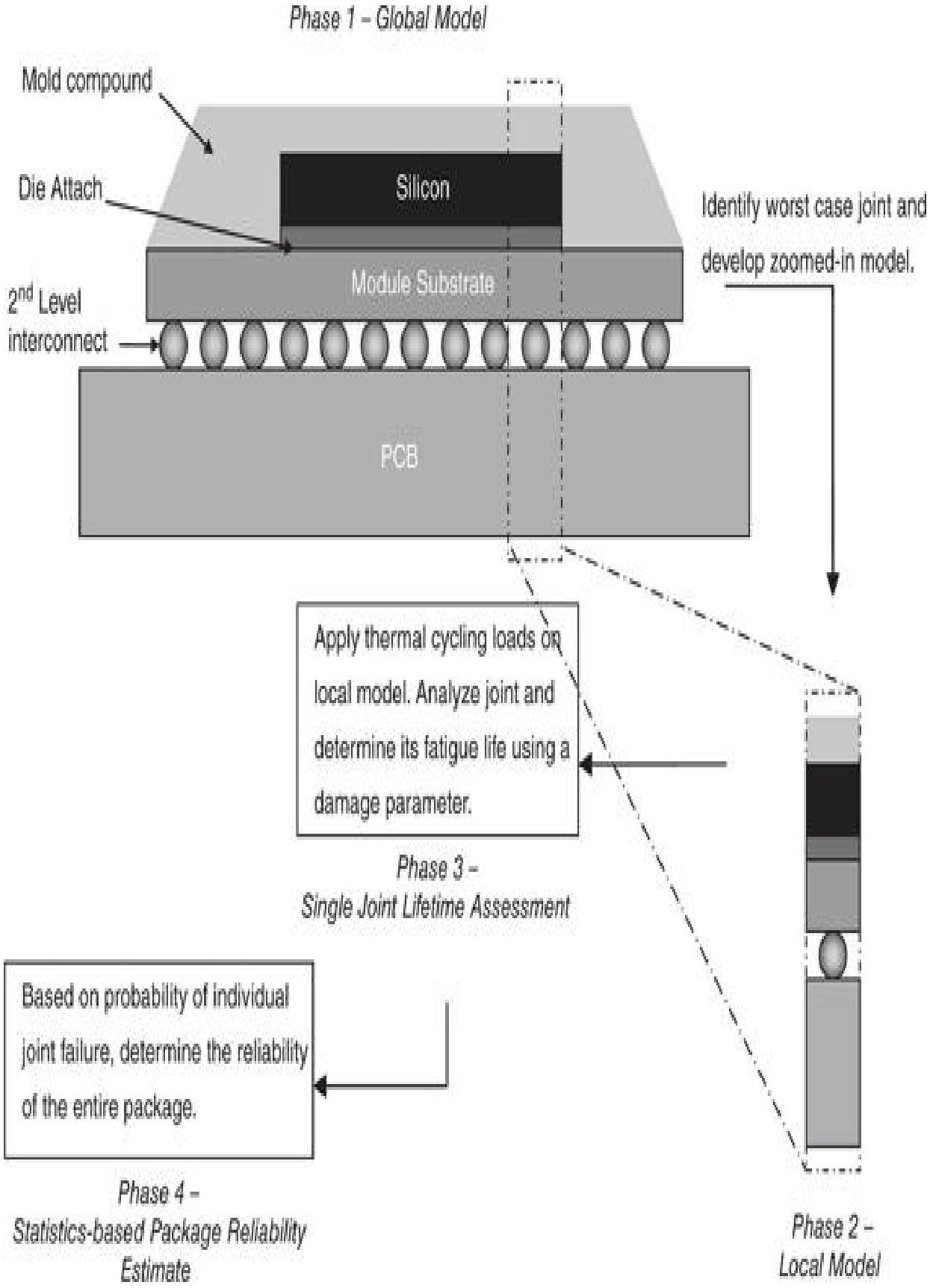

Phase 1 – Global Model
Mold compound
Die Attach
Silicon
Module Substrate
2nd Level interconnect
PCB
Identify worst case joint and develop zoomed-in model.
Apply thermal cycling loads on local model. Analyze joint and determine its fatigue life using a damage parameter.
Phase 3 – Single Joint Lifetime Assessment
Based on probability of individual joint failure, determine the reliability of the entire package.
Phase 4 – Statistics-based Package Reliability Estimate
Phase 2 – Local Model

FIGURE 64.15 FEA flowchart. Phase 1 involves creating the global model to determine global strains and displacements across the entire package. The global model also helps identify the locations of maximum stress. Phase 2 entails zooming into the location with the maximum strain. The boundary conditions applied around the local model are extracted from the global model. Phase 3 involves applying thermal cycling loads on the local model and determining the fatigue life of the worst-case solder joint in the local model. Phase 4 entails the use of statistical assessment tools to determine the reliability of the other solder joints relative to the worst case and thus estimating the solder joint reliability of the entire package.

64.4.1.1 Phase 1: Global Model.

Phase 1 involves building a global geometric model of the package. Models in FEA can be two-dimensional, 2.5-dimensional (strip), or three-dimensional. Two-dimensional models (plane strain or plane stress) are computationally very efficient as only a two-dimensional cross section of the assembled package is modeled. However, they are based on the assumption that the out-of-plane deformation and stresses in the assembly are negligible, which is not the case with discrete solder joints. Thus, although they are useful for providing qualitative deformation and stress comparisons, they are not useful for quantitative fatigue-life estimates. A 2.5-dimensional or strip model has a thickness, but it is very small—just enough to capture the round shape of the solder joints. While it is an improvement over a two-dimensional model, it does not capture the increased stress concentration at package corners. A three-dimensional model is a much closer representation of an assembled package. Although it is computationally challenging, it is the best way to estimate the deformation and stresses induced in an assembled package. A global model of one-eighth of a BGA package can be found in Fig. 64.16.

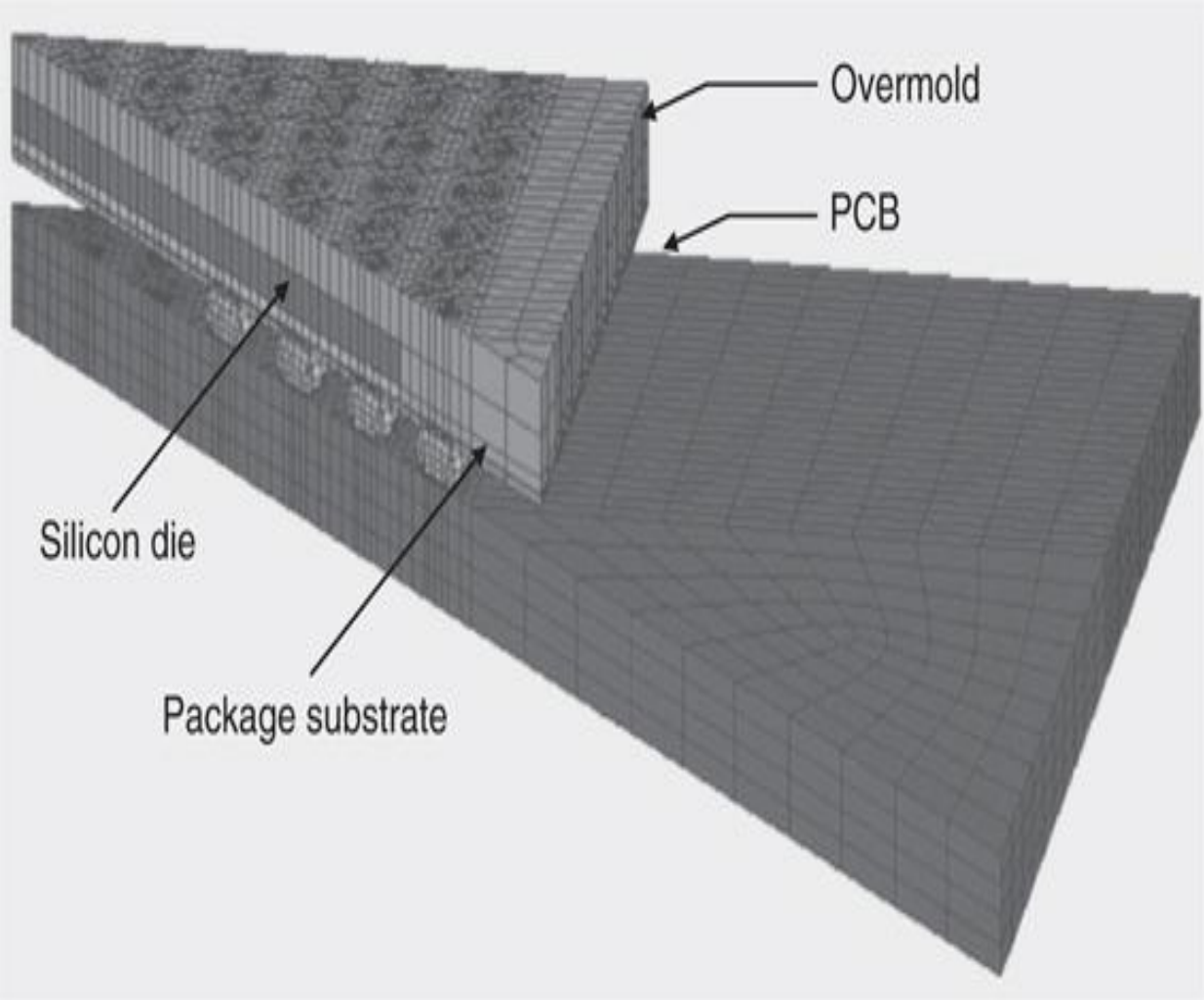


FIGURE 64.16 Global FEA model of one-eighth of a BGA. Note the PWB, package substrate, die, and overmold are all created by a series of elements.

Note that only one-eighth of the package is modeled (Fig. 64.16). This is due to the fact that the package is octant symmetric, and thus symmetry boundary conditions can be employed to reduce the model size, which in turn increases the speed at which a solution can be obtained.[46] Wherever possible, the deformation results of the global FEA model should be verified with experimental warpage measurement (using tools like Shadow Moiré[45]).

A unit temperature rise is applied to the global model, the worst-case joint is determined, and the displacements of the worst-case joints are calculated. Worst-case joint

determination is typically based on a maximum stress or strain in the solder joints. It is essential to obtain the displacements of the worst-case joint because those displacements can now be incorporated in a local model that will simulate multiple thermal cycles on a worst-case joint.

Only a unit temperature rise is applied to the global model to reduce the computational run time. An additional assumption employed in global models to reduce run time is that all materials are linear-elastic and temperature-independent. Because the goal of the global model is to determine the worst-case joint and the corresponding displacement, this approach is typically valid. Reference 46 contains a series of experimental cases and corresponding FEA predictions that validate the global/local approach and the linear elastic, temperature-independent unit temperature rise technique for the packages studied.

64.4.1.2 Phase 2: Local Model. A local model of the worst-case joint is created and subjected to simultaneous temperature cycle and temperature-scaled displacement-loading conditions obtained from the global model. The displacement field of the worst-case joint obtained in the global model when subjected to a unit temperature rise is scaled to match the expected displacement when the local model is subjected to actual thermal cycles. The advantage of this approach is that the local model can incorporate time and temperature material dependence because a reduced number of elements are employed when compared to the global model.

A local model of a solder joint can be found in Fig. 64.17. The local model is subjected to multiple thermal cycles and a final damage parameter is extracted. A typical thermal cycling loading profile to which the model is subjected is similar to that shown in Fig. 64.3. About two to four cycles are run to achieve stability of the hysteresis loop.

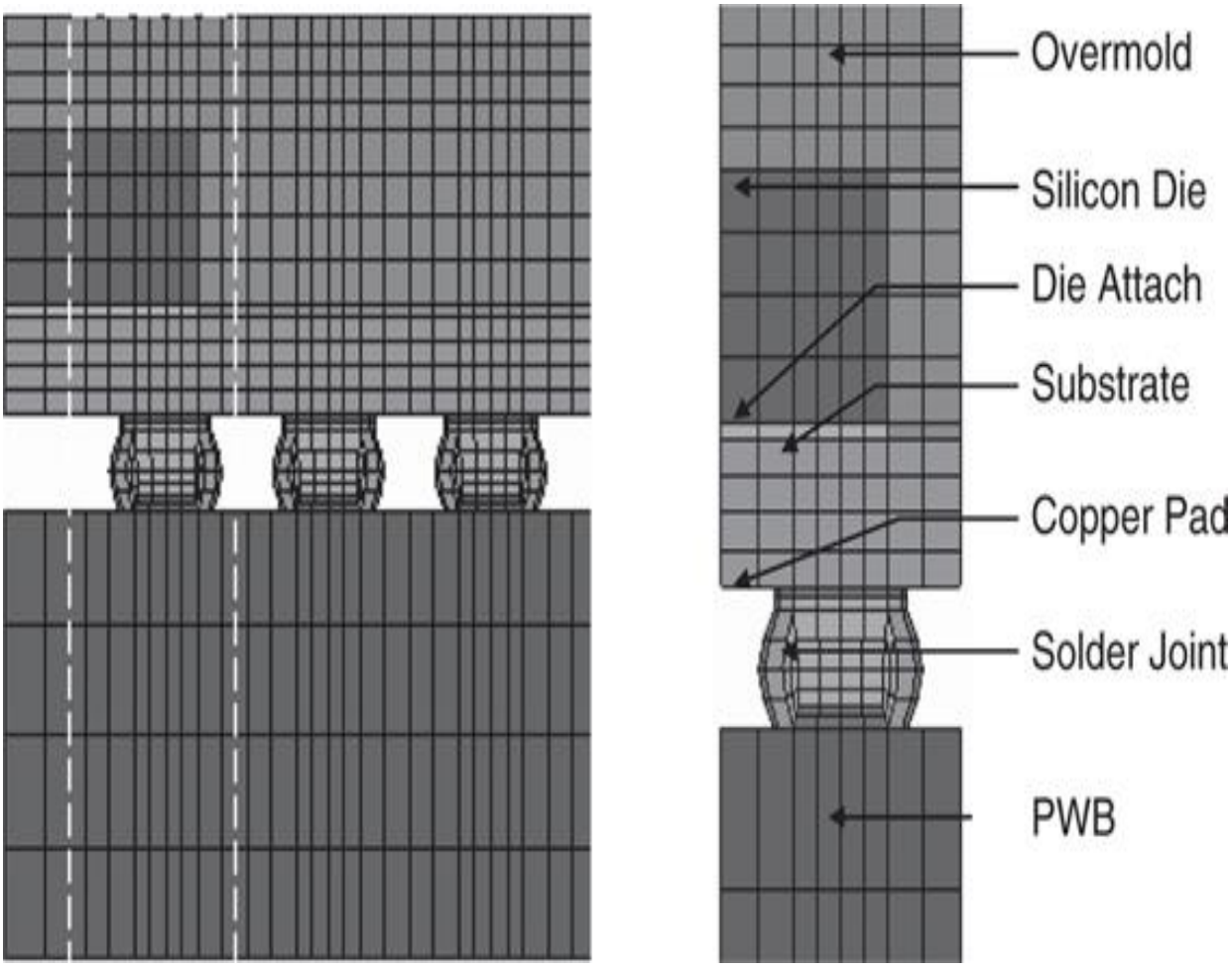


FIGURE 64.17 Close-up of three solder joints. The local model is created from one of the solder joints and its associated PWB, package substrate, die, and overmold. In this figure, the leftmost ball and associated material for the local model are indicated by the area inside the dashed rectangle.

Plastic work and plastic strain are two of the most common local damage parameters employed in solder joint lifetime estimations. The type of damage parameter selected is usually dictated by the experimental data available for a specific joint type (BGA, CCGA) that correlate damage with fatigue life. A methodology that employs plastic work and a correlation between plastic work and crack initiation and propagation can be found in References 10 and 46.

64.4.1.3 Phase 3: Solder Joint Fatigue-Life Assessment. The local model damage parameter is then

employed to determine the fatigue life of a given joint. Techniques for assessing lifetime based on a damage parameter range from employing plastic strain [Coffin-Manson relationship, Eq. (64.8)] to complex considerations of crack initiation and crack growth rates correlated with plastic work.[10,46] Regardless of the technique, the output of this phase is an estimate of the reliability of one joint: the worst-case solder joint.

Some of the fatigue-life prediction models that have been employed for lead-free solder joints are outlined in Table 64.7. In addition, other models for predicting fatigue life from the finite element models and performing relative comparative analysis can be found in References 16 and 47.

TABLE 64.7 Different Fatigue-Life Models for Predicting Fatigue Life from the Finite Element Model Results[18]

Fatigue-Life Model	Constants	Test Conditions	Reference
$N_f = C_1(\varepsilon_{cr})^{C_2}$ N_f = Number of cycles to fail ε_{cr} = Average equivalent creep strain	$C_1 = 4.5$ $C_2 = -1.295$	Flip-chip bumps with and without underfill. Wirebonded PBGA packages mounted on PWB	Schubert[48]
$N_f = C_1(\Delta W_{cr})^{C_2}$ W_{cr} = Average viscoplastic strain energy density/cycle	$C_1 = 345$ $C_2 = -1.02$	Flip-chip bumps with and without underfill. Wirebonded PBGA packages mounted on PWB.	Schubert[48]
$N_f = C_1(\varepsilon_{cr})^{C_2}$	$C_1 = 0.0468$ $C_2 = -1$	Several different BGA packages: CABGA, CBGA, FlexBGA, PBGA, TSCSP, etc. Double power law creep constitutive relations.[20]	Syed[49]
$N_f = C_1(\Delta W_{cr})^{C_2}$	$C_1 = 0.0015$ $C_2 = -1$	Several different BGA packages: CABGA, CBGA, FlexBGA, PBGA, TSCSP, etc. Double power law creep constitutive relations.[20]	Syed[49]
$1/N_f = 1/N_p + 1/N_c$ $N_p = (W_p/W_{p0})^{1/c}$ $N_c = (W_c/W_{c0})^{1/d}$ N_p = Number of cycles to failure due to plastic damage N_c = Number of cycles to failure due to creep damage W_p = Plastic work density calculated per load cycle W_c = Creep work density calculated per load cycle	$W_{p0} = 106.45$ $W_{c0} = 30.025$ $c = -0.51$ $d = -0.44$	Solder joint samples attached to copper coupons, subjected to cyclic loading. One-dimensional analytical model to derive constants.	Zhang[50]

A comparison of the results obtained by Schubert's[48] model with those obtained by Syed's[49] model can be found in Reference 51. It is important to note that these models are a function of the way that the material properties of the solder joints are modeled. In other words, the solder material properties used to derive these models play a significant role in the accuracy of the models. If a particular fatigue-life model is selected, the corresponding solder constitutive model used to derive the model constants should be used in the analysis.

In addition, several other factors could significantly alter the accuracy of a model, such as time step size, mesh density, material properties, reference temperature, element size, element type, and even software. All these need to be taken into account when using a model to predict fatigue life. Best practice recommendation is to run not just one, but a set of fatigue-life models and calibrate with existing experimental data before using the models to make fatigue-life predictions on packages on which no experimental data are available. Finally, it is important to note that these models only provide guidance on trends and relative comparisons. They should not be used as a substitute for experimental thermal cycle data for a given package under consideration.

64.4.1.4 Phase 4: Statistics-Based Package Reliability Assessment.

This final phase considers the reliability of all of the solder joints when determining the reliability of the package. Techniques employed here range from simply assuming that all joints are of equal reliability to performing a series reliability calculation to solve simultaneously an assumed distribution of failures (such as a Weibull distribution; see Sec. 64.2.2) considering each joint. It is also common to weigh the reliability of joints other than the worst-case joint by considering the displacement of all joints with respect to the displacement of the worst-case

joint.[46] This allows for the impact of DNP to be incorporated in the potential distribution of failures among joints at different locations.

64.4.1.5 Temperature-Dependent Material Properties. As mentioned earlier, the aforementioned procedure is based on the assumption that the mechanical properties of the package material set do not change significantly with temperature. There are certain packages, however, for which this technique is not applicable. A typical example is an FCBGA package in which the underfill material has a glass transition temperature (T_g) around 70 to 100°C and undergoes several orders of magnitude change in modulus above the T_g. Clearly, the properties of such a material are strongly dependent on temperature. In such a case, the following procedure can be followed:

1. The global model is cooled from its stress-free temperature (which is usually the adhesive cure temperature) to the lowest temperature to which the package has been thermal cycled (0°C if a 0 to 100°C thermal profile is used).
2. Cut boundary interpolation is performed at small temperature steps (such as 5 or 10°C), recording the deformation of the nodes at each temperature step. This information is stored in a set of data files.
3. A submodel is created of the worst-case solder joint (the one that shows the most stress or deformation in the global model). The files stored in step 2 are applied as load boundary conditions on the nodes forming the submodel boundary at each temperature step. Temperature-dependent material properties should be used in both models.
4. On completing the analysis, one can use the plastic work or strain accumulated to determine the expected fatigue

life of the package based on the worst-case solder joint, as outlined in Phase 3 of the previous section.

If computer resources are available, a complete global model could be used to determine the plastic work or strain per solder joint. However, this could be very time-consuming depending on the complexity of the package under consideration.

64.4.1.6 Impact on First-Level Interconnect. In FCBGA-type packages using temperature-dependent material properties, failure resulting from solder joint fatigue may occur not only at the board-level interconnect but also at the first-level interconnect (between the silicon die and substrate). The flip-chip bumps are encapsulated by the underfill to improve their thermomechanical reliability by evenly distributing the CTE-mismatch-induced strains between the die and substrate. If the underfill material properties are such that the underfill softens drastically above its T_g, then there is a possibility that the flip-chip bumps may fail early during thermal cycling.[52] To simulate this, the global-submodel approach outlined earlier can be used. In this case, the flip-chip bumps would also be incorporated in the submodel as shown in Fig. 64.18.

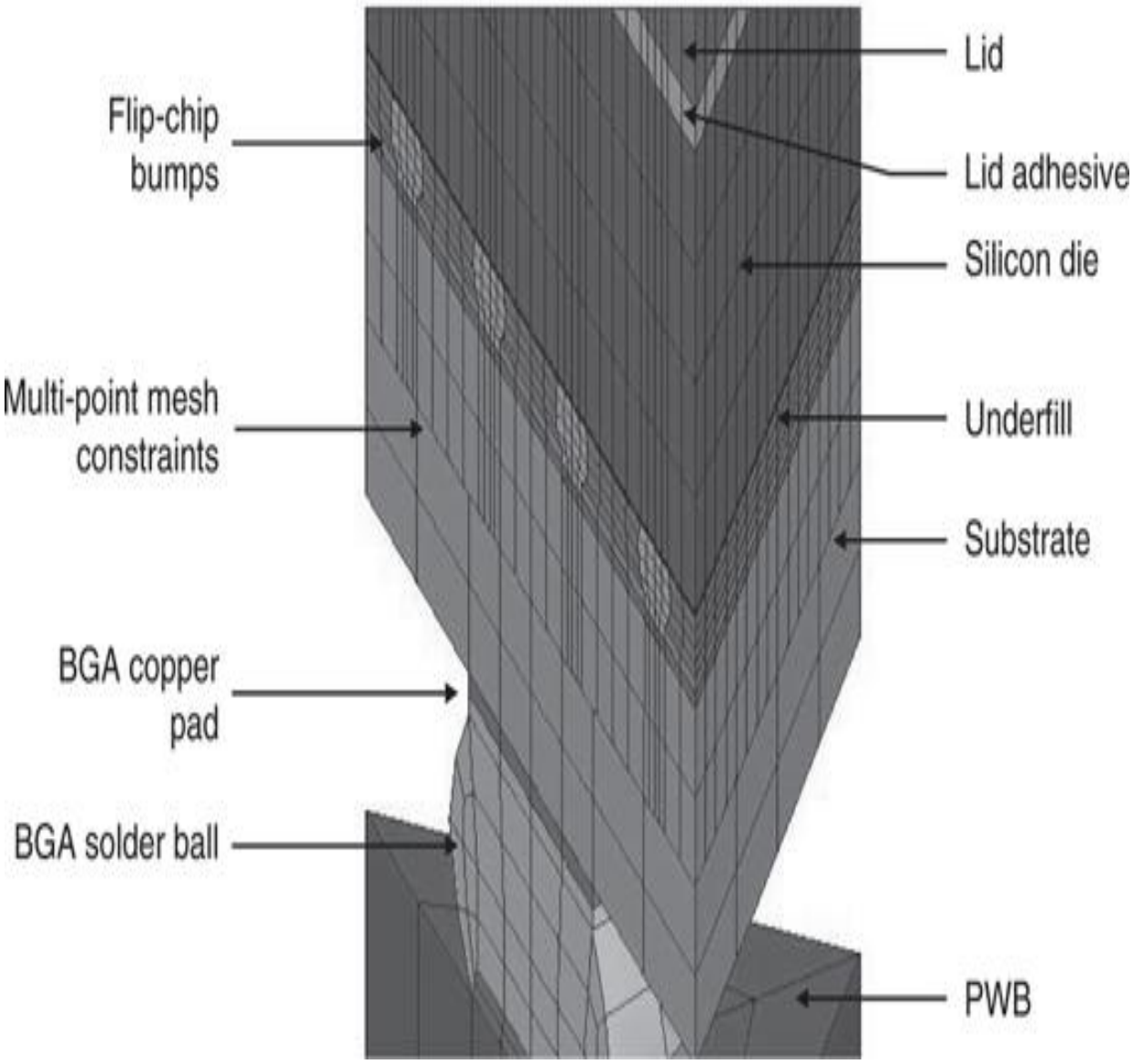


FIGURE 64.18 Three-dimensional submodel detail showing the flip-chip bumps and underfill included in the model. The submodel can be used to determine the fatigue life of the flip-chip bumps and the BGA solder joint underneath at the same time.

64.4.2 FEA for Monotonic Bend Testing

FEA simulations of monotonic bend testing involve a quarter-symmetry model of the assembly placed between anvils and deformed while monitoring the strains induced in the

package, solder joint interconnects, and the PWB. The details of the quarter-symmetry model are shown in Fig. 64.19.

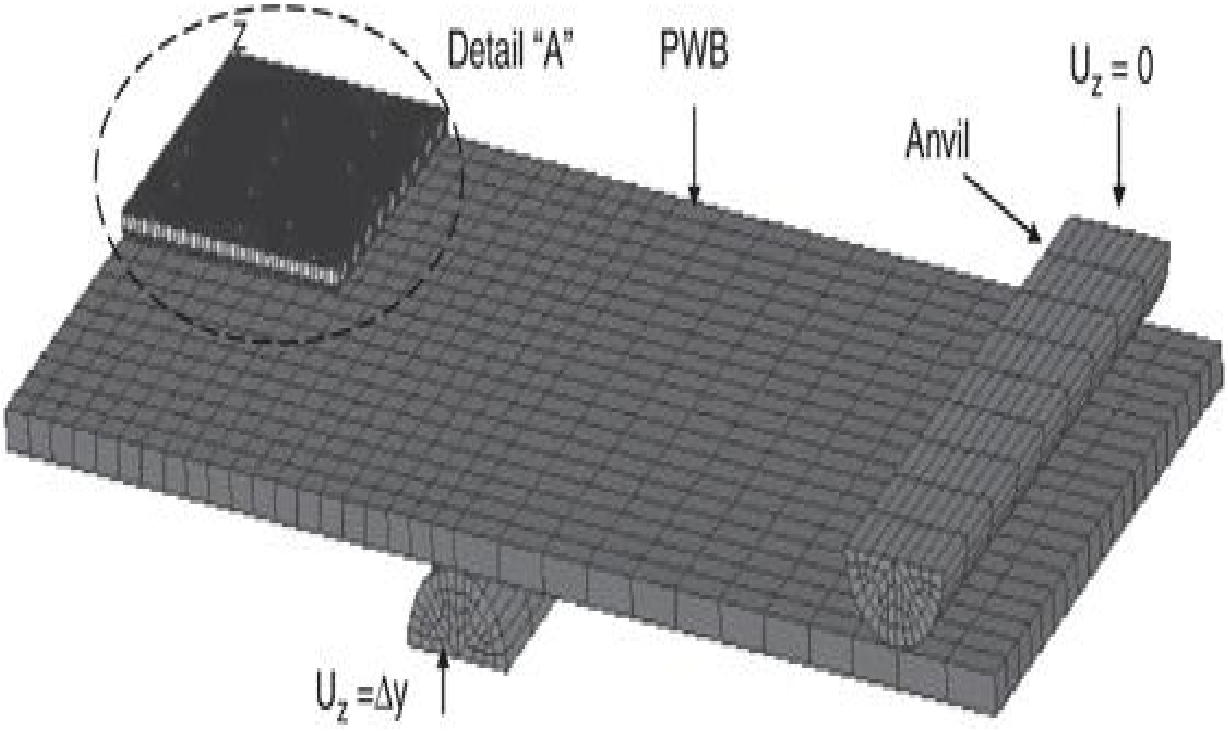


FIGURE 64.19 Three-dimensional quarter-symmetry model showing an FCBGA package mounted on a PWB between support anvils. Contact elements between the anvils and the PWB simulate the flexure of the PWB as one anvil set is moved vertically relative to the other. Detail A of the model is shown in Fig. 64.20.

Bend test FEA simulations achieve two primary objectives:

- To determine the relationship between PWB strain and critical joint strain. This in turn helps bridge differences between the controlled conditions in which the bend testing is performed and the conditions in which bending occurs during assembly.
- To perform a comparative assessment of different packages. FEA can be used to derive solder joint strains from experimental PWB strain data for different test conditions.

The FEA model is shown in Figs. 64.19 and 64.20. Solid structural elements are used to model the PWB, solder joints, and package details. Based on the premise that at high strain rates, the solder material becomes brittle and behaves almost like a linear elastic material, the solder joint elements are modeled as linear elastic. Contact elements are used at the interface between the PWB and anvils to simulate contact between the PWB and the anvils as the assembly is deformed. The solder joint geometry is modeled as closely as possible to the solder joints' actual shape after reflow.

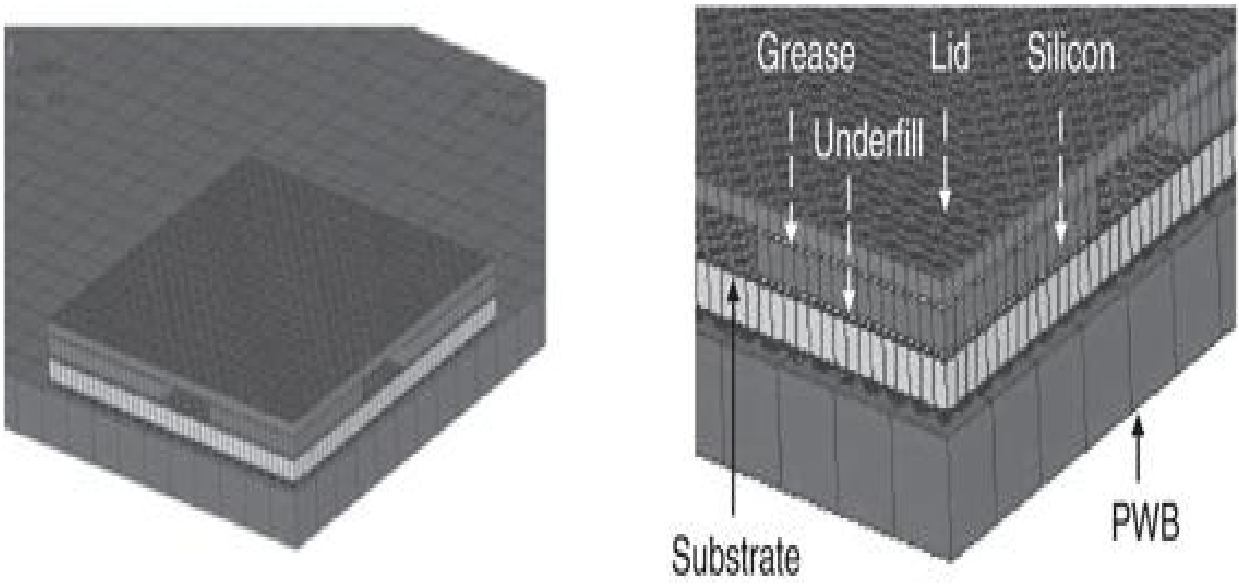


FIGURE 64.20 Detail A of the image model shown in Fig. 64.19. The image on the left shows the package (quarter-symmetry). The zoomed-in image on the right shows all the details of the FCBGA package construction.

A variety of different parametric analyses can be performed to determine the effect of different geometric variables on the critical joint strain. A few examples of such analyses are described in this section.

64.4.2.1 Strain Distribution Around the Package. Per IPC/JEDEC-9702, it is recommended that three strain gauges be placed around a package during four-point bend testing (see Fig. 64.21). These gauges are to be used to characterize

the strain response of the given package mounted on a board of a certain thickness. FEA was used to determine the joint-to-board strain ratio for each case, which in turn can be used to determine which strain gauge location is most or least sensitive to board flexure. The results of the simulation are shown in Fig. 64.22.

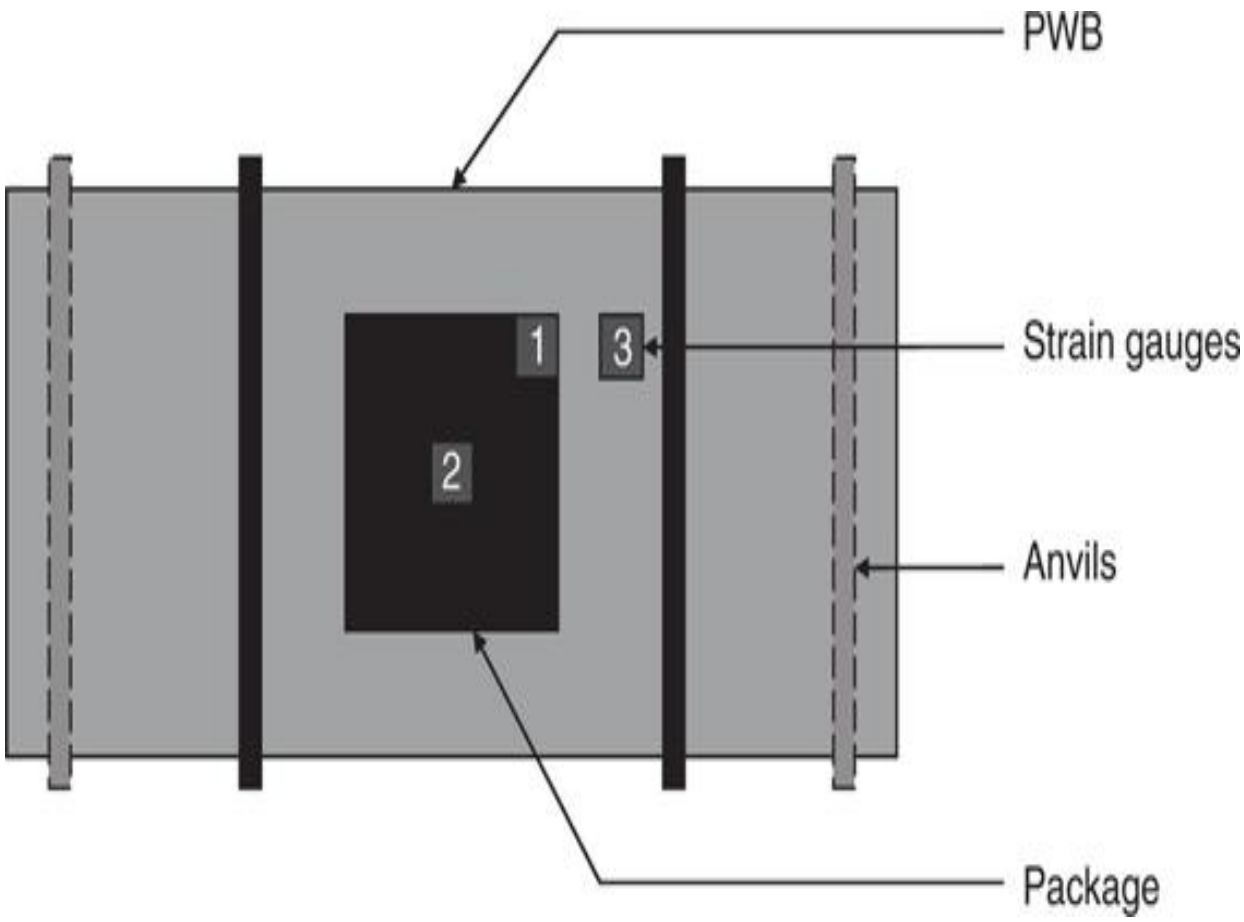


FIGURE 64.21 Nomenclature for the four-point bend test set up as outlined in IPC/JEDEC-9702. Three strain gauges are placed on the board to measure the strain distribution around the package. Gauge 1 is placed under the package, directly below the corner most solder joint. Gauge 2 sits directly below the package center. Gauge 3 is placed next to the package on the PCB topside, midway between the package edge and the anvil.

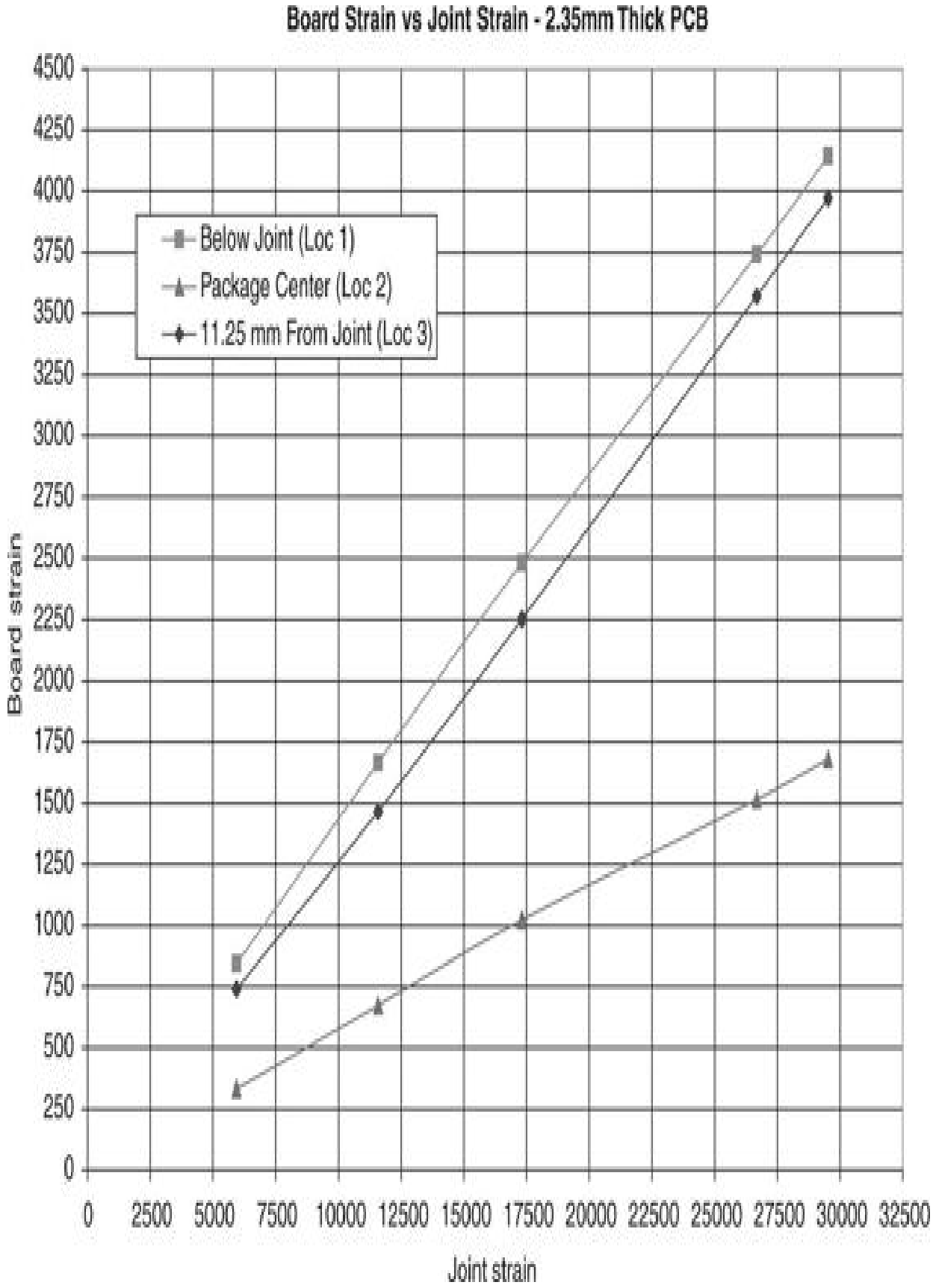

Board Strain vs Joint Strain - 2.35mm Thick PCB
Below Joint (Loc 1)
Package Center (Loc 2)
11.25 mm From Joint (Loc 3)
Board strain
Joint strain
4500
4250
4000
3750
3500
3250
3000
2750
2500
2250
2000
1750
1500
1250
1000
750
500
250
0
0
2500
5000
7500
10000
12500
15000
17500
20000
22500
25000
27500
30000
32500

FIGURE 64.22 Solder joint-to-PWB strain relationship for three gauge locations. The results indicate that the gradient at locations 1 and 3 are relatively close. The gradient at location 2 is quite low. This indicates that the PWB strain at location 2 is least sensitive to variations in critical solder joint strain. The nomenclature for the strain gauge locations is given in Fig. 64.21.

The results indicate that the highest sensitivity to solder joint strain is obtained at locations 1 and 3 (see Fig. 64.21). Location 2 reflects the global bending of the entire assembly. These results are in line with measured experimental data. The absolute strain value and the change in strain at location 2 is least sensitive to the critical solder joint failure strain.

64.4.2.2 Effect of Package Pad Size on Joint-to-Board Strain. FEA can also been used to estimate the effect of changes in solder joint pad size on the joint-to-board strain ratio. Two different package pad sizes were used: 0.53 mm, solder mask defined, (pad design 1) and 0.4 mm, solder mask defined, (pad design 2) while the PCB pad design was kept constant (0.5 mm, non-solder mask defined). The results in terms of the joint-to-board strain at location 3 are shown in Fig. 64.23.

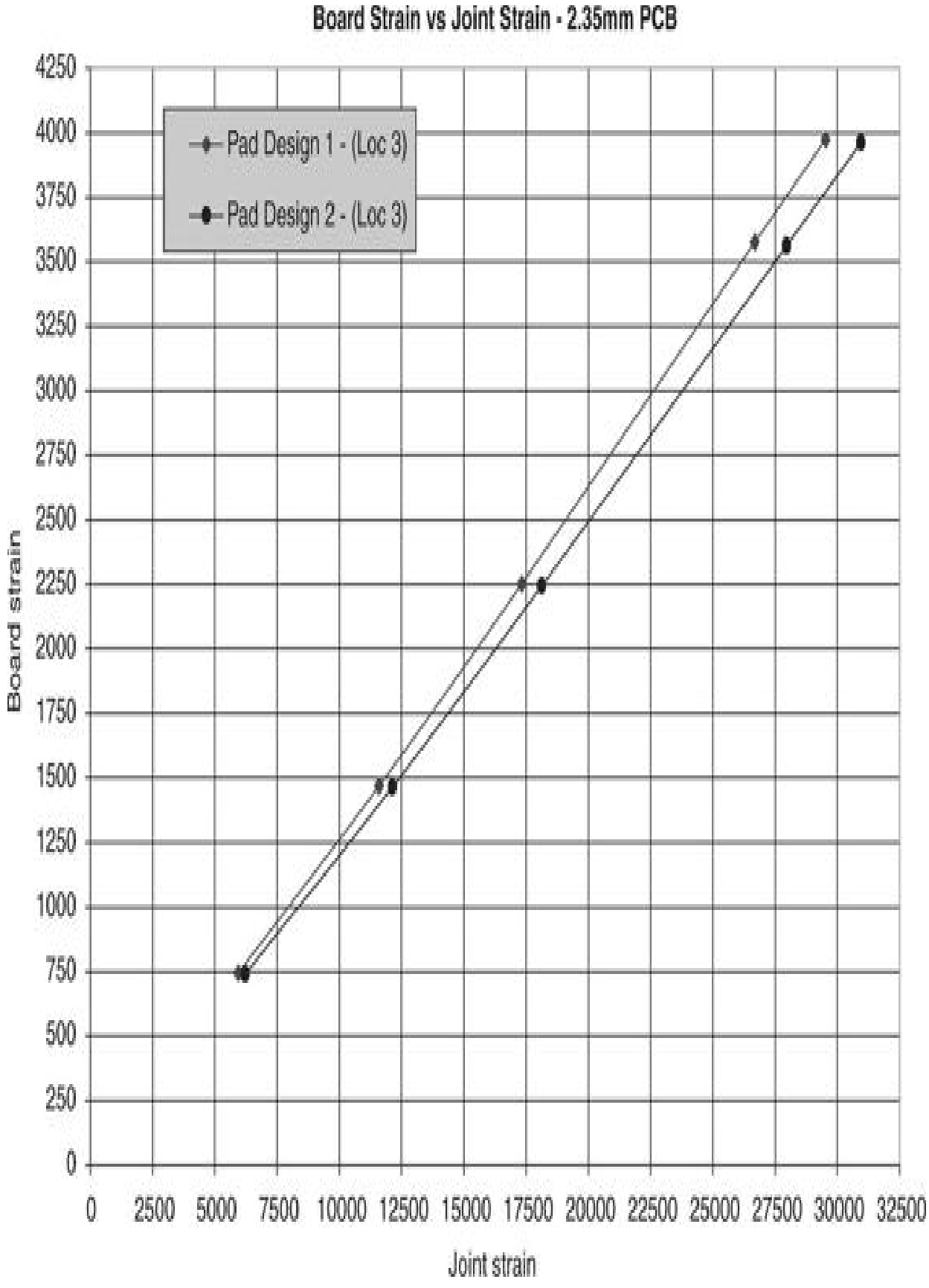

Board Strain vs Joint Strain - 2.35mm PCB
Pad Design 1 - (Loc 3)
Pad Design 2 - (Loc 3)
Board strain
4250
4000
3750
3500
3250
3000
2750
2500
2250
2000
1750
1500
1250
1000
750
500
250
0
0
2500
5000
7500
10000
12500
15000
17500
20000
22500
25000
27500
30000
32500
Joint strain

FIGURE 64.23 Two different solder joint pad sizes analyzed. The results indicate that for the same PWB strain, the solder joint strain is ~18 percent higher for pad design 2 as compared to pad design 1.

The results in Fig. 64.23 indicate that pad size change could have a significant impact on the strain in critical solder joints. As a result, care should be taken in using data generated with one pad size to qualify or accept the bending strength with another pad size, unless the absolute strain-to-failure value is much higher than the required strength.

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PART 12

FLEXIBLE CIRCUITS

CHAPTER 65

FLEXIBLE CIRCUIT APPLICATIONS AND MATERIALS

Happy T. Holden

Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

65.1 INTRODUCTION TO FLEXIBLE CIRCUITS

Flexible circuits are a form of printed wiring interconnect structure built on thin, flexible substrates. They are also bendable to complete three-dimensional (3D) wiring that rigid circuit boards cannot achieve. Because of this flexibility, flexible circuits have many advantages over other wiring methods and have many applications in electronic equipment that require high-density wiring in a small space. As the samples in Fig. 65.1 show, most flexible circuits have cabling functions rather than the mounting functions of electronic components.

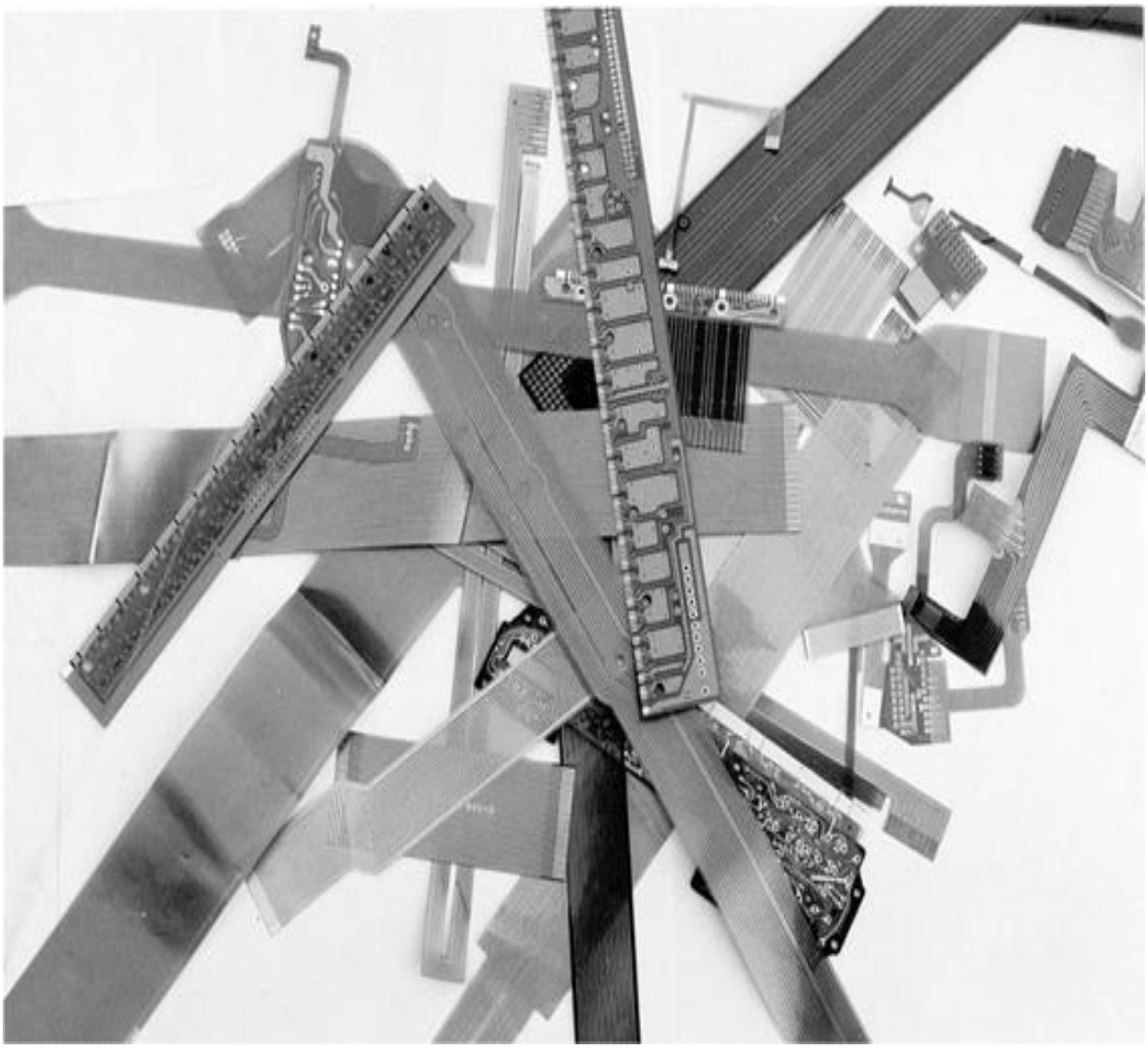

FIGURE 65.1 Various examples of flexible circuits.

Tape-automated bonding (TAB) has not been considered as a type of flexible circuit because of the slightly different manufacturing processes. However, the basic construction and materials of the final products are the same; therefore, TAB is categorized as a type of flexible circuit in this book (see Fig. 65.2).

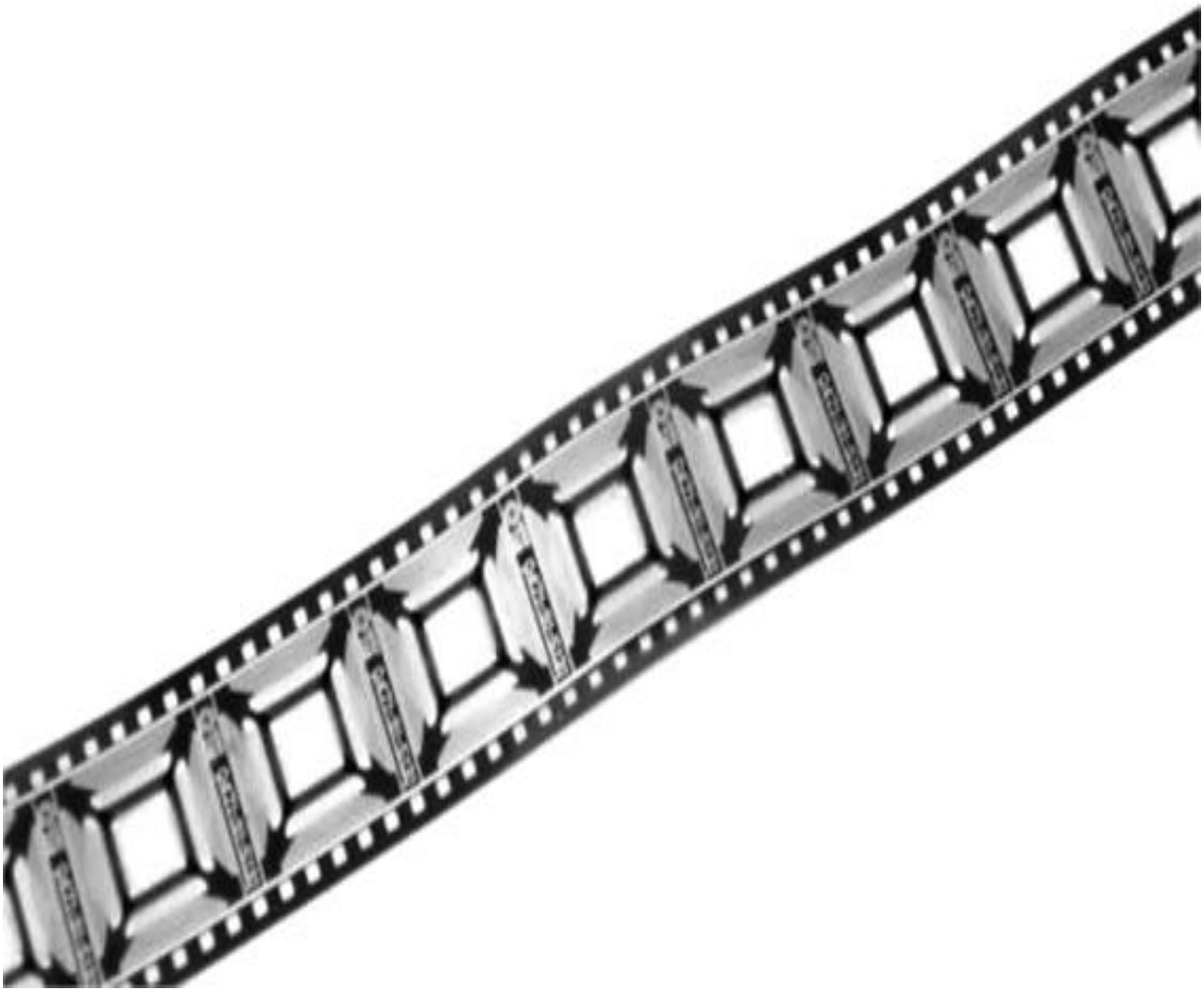

FIGURE 65.2 Example of fine TAB circuits.

65.1.1 Advantages and Disadvantages of Flexible Circuits

The basic advantages of the flexible circuits are its thinness and ability to bend. However, a thin flexible circuit generates many supplemental advantages not available with other wiring methods (see Table 65.1). A 3D wiring with component assembling in a small space and a long-term dynamic flexing with small radius are typical examples of what other wiring materials cannot replace. On the other hand, flexible circuits also have many disadvantages due to unstable thin

constructions. It is necessary to consider how to avoid the disadvantages when using a flexible circuit in a packaging system. Otherwise, overall process yield and productivity will be low and the final cost will be relatively very high.

TABLE 65.1 Advantages and Disadvantages of Flexible Circuits

Advantages	Disadvantages
Thin	Fragile
Light	Unstable dimensionally
Bendable	Low reliability—fatigue
Flexible	Difficult to design
Long flexing endurance	Complicated manufacturing process
3D wiring	Difficult to handle
High-density wiring in a small space	Need special tools for assembling
Avoid connectors and soldering	Low yield in assembling
Avoid missed wiring	Difficult to rework
Low total cost, including all elements	High cost of circuit fabrication

65.1.2 Economics of Flexible Circuits

The largest disadvantage of flexible circuits is that they cost more than rigid circuit boards or flat cables of the same size. Usually, flexible circuits are larger than rigid circuit boards to allow 3D wiring capability; however, the total circuit cost increases, using flexible circuits is still often cheaper than using multiple rigid boards and associated connectors.

That is, the cost of using flexible circuits must be compared to the total cost of rigid circuit boards in terms of the following:

- Connectors
- Wires
- Additional assembly costs

Because the total cost of a flexible circuit is greater than that of an equivalent rigid circuit board alone, designers should not choose flexible circuits over other wiring methods unless three-dimensional advantages are needed, especially for consumer applications that require low-cost wiring. A flexible circuit should be used only when it provides the solution for the application's wiring requirements (e.g., when the application requires bendable wiring in a small space, lightweight, long-flex endurance, and so on). The critical question is whether the value of a flexible circuit's performance is greater than its cost.

Miniaturization of electronic products requires extremely lightweight wiring in a small space, and therefore there have been many opportunities for flexible circuits. Figure 65.3 shows examples of flexible circuits applied to a digital camera in which their advantages make them the best technical solution, and also the least expensive. In this example, the entire circuit was divided into one multilayer rigid board and more than 10 flexible circuits to optimize the advantages and minimize the total wiring costs.

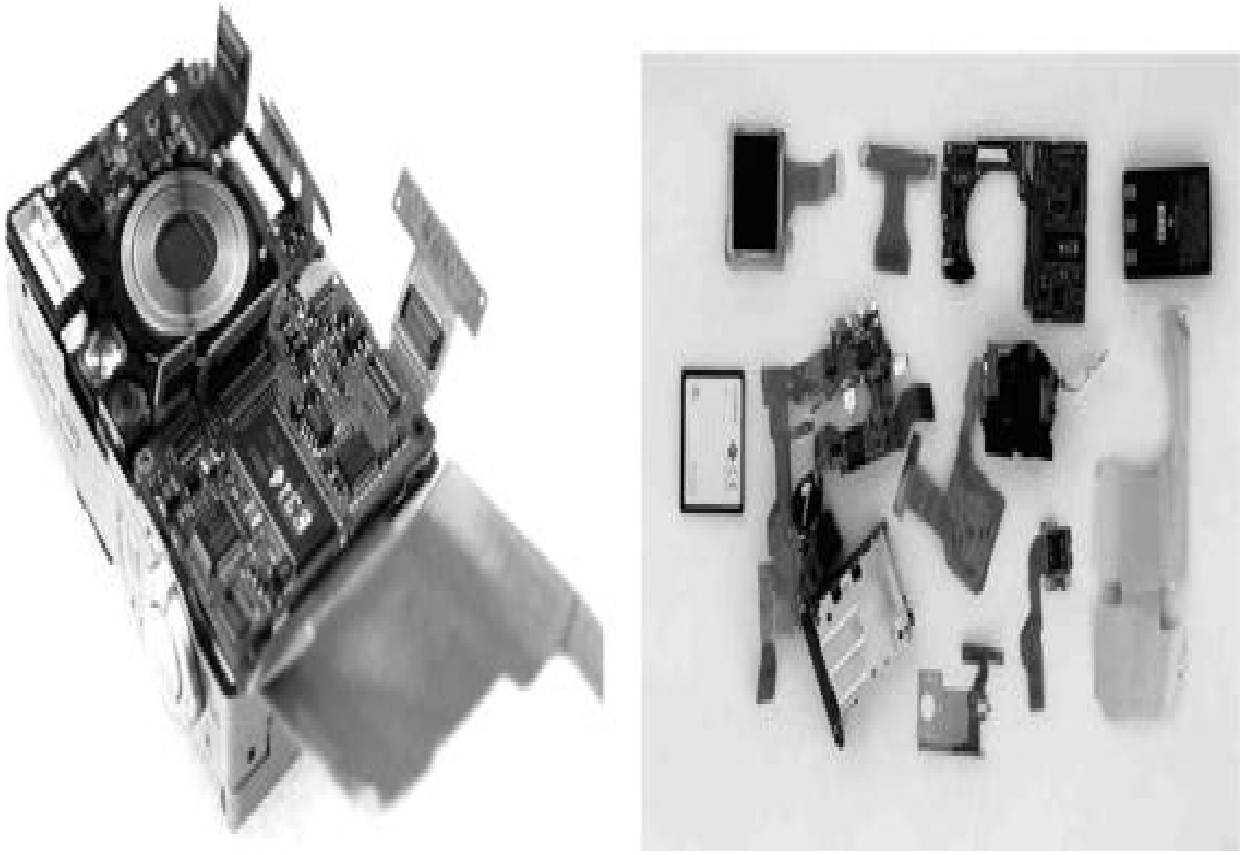

FIGURE 65.3 Flexible circuits applied for digital camera. (*Courtesy of Canon*.)

65.2 APPLICATIONS OF FLEXIBLE CIRCUITS

As described, a flexible circuit should be adopted only when other wiring or packaging methods cannot satisfy the application's requirements. Table 65.2 shows how features of flexible circuits relate to appropriate applications. The table shows typical examples of flexible circuit applications in electronic products. Portable electronic products such as cellular phones, digital cameras, automobile instrument panels, and handheld calculators require reliable 3D wiring in a small space. In some cameras, more than 10 flexible circuits are squeezed into a small space. Flexible circuits are used for the hinge wiring in many electronic products that

have mechanical moving parts, such as notebook computers, palmtop computers, and personal digital assistants (PDAs). Many new electronic products, such as hard disk drives, small printers, and clamshell type cellular phones, require a long-life dynamic flexible endurance. Multilayer rigid/flexible circuits have been effective in reducing wiring space and increasing wiring reliability in aerospace electronic equipment and small portable electronic products such as cellular phones. Only flexible circuits could satisfy all these wiring requirements. Efforts to minimize the cost of flexible circuit wiring for consumer applications are ongoing. Often, the miniaturization of a consumer electronic product assumes a wiring system with multiple flexible circuits, especially if the equipment has mechanical moving portions.

TABLE 65.2 Features and Applications of Flexible Circuits

Features	Applications
High-density wiring in a small space	Digital camera, cellular phone, flat panel display, video camera, facsimile, ultrasound probe
Lightweight	Calculator
3D wiring	Automobile instrument panel, cellular phone, camera, notebook computer
Reliable wiring	Aerospace applications, industrial applications
Long flexing endurance	Printer, hard disk drive, floppy disk drive, CD drive, VCR

65.3 HIGH-DENSITY FLEXIBLE CIRCUITS

Serious progress in the density of flexible circuits was made during the second half of the 1990s, owing to the extreme

miniaturization of electronic products. These products incorporate a new technical concept in the design of the circuits. They have a much higher density than traditional flexible circuits, with dimensions for traces, spaces, and via holes equivalent to those of rigid high-density interconnect (HDI) boards. (Details are described in the chapter on Special Construction of Flexible Circuits, Chap. 70.) They also have supplemental constructions on the circuit to allow higher termination capabilities. This type of construction is called an *HDI flexible circuit* (i.e., a flexible circuit for high-density interconnects).

65.3.1 Specifications

Table 65.3 shows typical requirements for interconnection in the end product, and the preferred specification of circuit parameters for the use of high-density flexible circuits.

TABLE 65.3 Common New Requirements for High-Density Flexible Circuits

Requirements for End Use	Preferred Specification for Flexible Circuits
High-density wiring	Pitches smaller than 150 µm, via holes smaller than 150 µm in diameter thin and light Base 25 µm or thinner, conductor thinner than 12 µm
High-density SMT	Small opening on coverlay, tin or lead-free plating High-density connection High dimensional accuracy (<0.3 mm diameter) bonding High-density flying lead, pitch <100 µm
Chip-on-flex, flip-chip	High-density microbump array, pitch <100 µm High reliability for vibration High bond strength of conductors
For mechanical shock	High bond strength between layers wide-range heat cycle High heat resistance
For salty moistures	High insulation resistance

Portable electronic products are exposed to more severe conditions than ever before. As a result, they need higher reliability for the circuits as listed in Table 65.3. In the case of portable telephones, they are often carried in the owner's pocket, where they may be exposed to a variety of conditions, including continuous vibration, mechanical shock, temperature, humidity, pocket lint, and even perspiration. Other portable electronic products, such as digital cameras, PDAs, and notebook computers, could be exposed to similar conditions.

65.3.2 Applications

Due to usage and assembly technologies, many applications require increased performance for high-density flexible circuits. The manufacturing processes for these circuits must adapt to new requirements imposed by additional process conditions. Table 65.4 lists major applications and the associated advantages of using high-density flexible circuits for a given purpose.

TABLE 65.4 Major Applications of High-Density Flexible Circuits

Applications	Reasons to Use High-Density Flexible Circuits
Wireless suspension of disk drives	High-density wiring in a small space Flexible, thin, light, 3D wiring Direct connection to magnetic heads
Interconnections of disk drive actuators	High-density wiring in a small space Flexible, thin, light, 3D wiring Repeated reparability
Interposer of CSP	High-density wiring in a small space Thin, light, 3D wiring
Flat-panel displays	High-density wiring in a small space Flexible, thin, light, 3D wiring Chip-on-flex capability High-density connection
Ultrasound probes	High-density wiring in a small space Flexible, thin, light, 3D wiring Direct connection to ultrasound device
Cellular phones	High-density wiring in a small space Flexible, thin, light, 3D wiring surface-mount technology (SMT) and COF capability
Inkjet printers	High-density wiring in a small space Flexible, thin, 3D wiring Direct connection to printer head device

Without high-density flexible circuits, these applications could not achieve miniaturization or support valuable new functions. For example, specially developed high-density flexible circuits can provide highly reliable connections at a low cost for new tiny magnetic heads of hard disk drives with

a vertical recording system. Chip-scale package (CSP) technologies can be developed with high-density flexible circuits. Driver integrated circuits (ICs) for flat panel displays in personal computers and large flat panel TVs are assembled with a set of chip-on-flex (COF) substrates. Due to the limited space within the camera bodies, small liquid crystal display (LCD) monitors for video cameras and digital cameras are assembled using long-tailed high-density flexible circuits. The wiring of the “next generation” of portable electronics cannot be completed without high-density flexible circuits.

65.4 MATERIALS FOR FLEXIBLE CIRCUITS

The basic difference between flexible circuits and rigid circuit boards is the thin and flexible materials used in the substrates of flexible circuits. Furthermore, because the flexible circuits have complicated constructions, supplemental materials other than copper-clad materials have been required to build a whole circuit.

65.4.1 Traditional Flexible Circuit Materials

Table 65.5 shows traditional major materials and typical examples of flexible circuits. A broad variety of the materials are employed to build traditional flexible circuits. Film materials, such as polyimide (PI) films and polyester (PET) films are the specially adapted for use in flexible circuits. For greater flexibility, rolled annealed (RA) copper foil is used as the major conductor material.

TABLE 65.5 Traditional Major Materials Used to Build Flexible Circuits

Application	Typical Materials
Base substrates	Polyimide film (PI), polyester film (PET), polyester terephthalate Thin glass-epoxy, fluorinated ethylene propylene (FEP), resin-coated paper
Conductors	Electrodeposited (ED) copper foil, RA copper foil, stainless steel foil, aluminum foil, etc.
Copper-clad laminates	Epoxy-based, acrylic-based, phenol-based (adhesive-based)
Coverlay	PI film, PET film, flexible solder mask
Adhesive layer	Acrylic resin, epoxy resin, phenol resin, pressure-sensitive adhesives (PSAs)
Stiffener	PI film, PET film, glass-epoxy, metal boards, etc.

Coverlays and stiffeners are typical examples of the special components needed to build flexible circuits. Many types of materials have been introduced to accommodate the designs of the end applications.

65.4.2 HDI-Oriented Flexible Circuit Materials

Since 1990, many new materials for flexible circuits have been developed in conjunction with design and manufacturing processes to satisfy new requirements in HDI applications. These include

- High-performance films
- Adhesiveless laminates
- Direct cast processes of liquid polyimide resins
- Photoimageable coverlay

See Table 65.6 for a list of new materials for HDI flexible circuits. There is a significant difference between traditional flexible circuits and HDI flexible circuits. For example, more than 80 percent of traditional flexible circuits were covered by adhesive-based copper-clad laminates that use the traditional polyimide films, Kapton H™ or Apical AV™. Conversely, the majority of high-density flexible circuits used in large-volume applications utilize all new materials.

TABLE 65.6 Materials for High-Density Flexible Circuits

Application Areas	New Materials for High-Density Flexible Circuits
Base dielectrics	Polyimide films (Kapton K, E, EN, KJ; Apical NP, FP; Upilex-S) Liquid polyimide resin, PEN film, LCP films
Conductor materials	Ultrathin copper foils, sputtered copper, copper alloys, stainless steel foil
Copper-clad laminates	Adhesiveless laminates (cast type, sputtered/plated type, laminated type)
Coverlay	Photoimageable coverlay (PIC) (dry film type, liquid ink type)
Adhesive sheets	Hot-melt polyimide film

HDI applications require finer traces and microvia holes in severe manufacturing and application conditions. For manufacturing convenience, flexible circuit producers prefer thinner conductors and substrates. However, physical performances of thinner materials may not be optimal. Thinner materials impact both the performance and manufacturing yield of the final flexible circuit.

Dimensional stability of the materials in high-density flexible circuits during manufacturing is a key to good process yields. To produce reliable high-density flexible circuits, conflicts between materials, constructions, and manufacturing processes must be resolved. Measures to accomplish this objective have been undertaken. For

example, new construction designs and manufacturing technologies now require use of the materials shown in Table 65.7.

TABLE 65.7 Comparison of Selected Properties of Flexible Base Materials

Substrate Material	Dielectric Constant	Dissipation Factor	Dielectric Strength, V/mil	Moisture Absorption, %	Tensile Strength, kpsi	Elongation, %
Polyester	3.2	0.005	7000	< 0.08	25	~120
Polymide	3.5	0.003	7000	1.3–3.0	25	~60
PEN	2.9	0.004	7500	1.0	30–35	~75
LCP	2.9	0.003	6000	0.02–0.1	15–25	~15
FEP	2.0	0.0002	5000	< 0.01	2–3	~300
PTFE	2.5	0.0002	5000	< 0.01	15–25	N/A
PVC	4.7	0.093	500	< 0.5	5	120–500
Aramid paper	2.0	0.007	380	3.0	11	~10

65.5 SUBSTRATE MATERIAL PROPERTIES

Many kinds of materials have been developed as the major dielectric layers of flexible circuits; however, polyimide films and polyester films have been the major core material for both substrate films and coverlay films with adhesive for traditional flexible circuits. The polyimide films have been the major substrate material for the soldering process and other high-temperature terminations processes, such as

wirebonding and flip-chip, because of their high-temperature resistance and good balance of physical properties. Polyester films are not available for standard soldering, but they are a low-cost solution for large circuits such as those used in automobile instrument panels and long cable circuits of printers.

65.5.1 Comparison of Substrate Materials

There have been examples of other materials, such as thin glass-epoxy, that have not been widely used. To satisfy the new concept of HDI flexible circuits, innovative uses of raw materials such as polyethylene naphthalate (PEN) film, liquid crystal polymer (LCP) film, and polyether ether ketone (PEEK) film have been introduced. Comparisons are shown in Table 65.8.

TABLE 65.8 Comparison of Substrate Materials

	Polyimide	Polyester	Thin Glass Epoxy	LCP	PEEK
Maximum operating temperature	>200°C	<70°C	~105°C	~90°C	>200°C
Standard thickness	12.5, 25, 50, 75, 125 µm	25, 50, 75, 100, 125, 188 µm	100, 150, 200 µm	(50 µm)	(50 µm)
Soldering	Applicable	Difficult	Applicable	Possible	Possible
Wire bonding	Possible	No	Difficult	Difficult	Possible
Color	Brown	Transparent	Transparent	Transparent	Milky
Moisture absorption	High	Low	Low	Low	Low
Dimensional stability	Acceptable	High	High	Good	High
Flexibility	High	High	Low	High	High
Cost	High	Low	Medium	Low	High

65.5.2 Polyimide Film

Polyimide film continues to be the major substrate material for flexible circuits because only it can support high-temperature processes such as soldering and wirebonding. Both Kaptons H, HN, VN, and FN films by Du Pont and Apical AV by Kaneka have been used in the flexible circuit industry for a long time. Both of these materials have a good property balance, and they are still the major substrates in traditional flexible circuits.

65.5.2.1 Properties of Polyimide Films. Table 65.9 shows major properties of typical polyimide films, Kaptons H(HN), VN, FN, and Apical AV. These have good mechanical properties and provide excellent performance as base substrate films and coverlay films in dynamic flexing

applications. They have flame-retardant characteristics, and it is not difficult to achieve Underwriters Laboratories (UL) flame class 94-V-0 or 94-VTM-0. The largest disadvantage of polyimide film is its higher cost compared to other common plastic films such as PET.

TABLE 65.9 Properties of Traditional Polyimide Films and New Polyimide Films

		Kapton H(HN)™	Apical AV™	Kapton FN™	Apical NP™	Apical HP™	Upilex S™
		DuPont	Kaneka	DuPont	Kaneka	Kaneka	Ube
Manufacturer thickness (μm)		12.5, 25, 50, 75, 125	12.5, 25, 50, 75, 125	12.5, 25, 50, 75	12.5, 25, 50, 75	12.5, 25, 50, 75	12.5, 25, 50, 75, 125
Tensile strength (kg/mm^2)	MD	25.2	25.0	28.3	30.0	28.6	39.4
	TD	22.3	27.0	25.4	32.0	29.0	40.2
Elongation (%)	MD	85	119	16	82	40	22
	TD	83	114	32	73	38	21
Tensile modulus (kg/mm^2)	MD	336.1	305.9	785.5	407.9	654.0	897.3
	TD	321.4	312.2	622.4	428.3	665.0	912.1
CTE (ppm) (100–200°C)	MD	27	35	3	17	12	14
	TD	31	31	12	13	11	15
CHE (ppm) (50°C, 35–75% RH)	MD	15	16	5	13	8	9
	TD	16	15	8	12	6	10
Heat (%) shrinkage (200°C, 2 h)	MD	0.18	0.08	0.03	0.06	0.06	0.07
	TD	0.20	0.03	0.02	0.02	0.02	0.10
Water absorption (23°C, 24 h)		2.8	2.9	2.2	2.5	1.1	1.9
Alkaline resistance		17.4	25.9	5.5	22.9	4.2	~0
Chemical etching		Possible	Possible	Possible	Possible	Possible	Difficult

There are several barriers to using traditional polyimide films as the major substrate materials in HDI flexible circuits. Dimensional stability is the largest issue. Both Kapton H film and Apical AV by Kaneka have coefficients of thermal efficiency (CTEs) higher than 30 ppm, which is not acceptable for the large-volume production processing of HDI flexible circuits. Relatively high moisture absorption is another major barrier to using these films as the base material of the flexible circuits. High moisture levels in the films cause a lot of supplemental problems, mostly in increased temperature processes. Higher-performance polyimide films are required as the substrate material of HDI flexible circuits.

The primary materials used in industry to optimize cost and performance have been 50-µm-thick polyimide film, used for industrial and avionics applications, and 25-µm-thick films, used for consumer applications. However, since late 1990s, films as thin as 12.5 µm have been specified to reduce thickness and increase flexibility.

65.5.2.2 High-Performance Polyimide Film. Various manufacturers have made several aggressive measures to commercialize high-performance polyimide films. Upilex-S by Ube Industry has excellent chemical stability, and it is a barrier for chemical processes such as adhesion with the other materials or chemical etching. Strong chemicals, such as hydrazine, are required to do the chemical etching. Upilex-S could be the major material as the substrate of TAB, which requires very high dimensional stability at high heat resistance. Newly developed polyimide films such as Kapton VN, E, EN, and Kaneka's Apical NP and FP have higher dimensional stability and lower moisture absorption rates. It is possible to etch these films using mild alkaline chemistry. Basic properties of the materials are summarized in Table 65.8.

Hot-melt-type (thermoplastic) polyimide films have been developed as high-heat-resistant adhesive materials. Mitsui Chemical's TPI, DuPont's Kapton KJ, Ube's Upicel, and Kaneka's Pixeo are typical examples. These are coated on dimensionally stable polyimide films to ensure good physical performance.

65.5.2.3 Liquid Polyimide Resin (Photoimageable). Many new HDI applications require special capabilities and properties on the substrates that are not provided by commercial polyimide films. In these cases, circuit manufacturers initiate production by manufacturing polyimide substrates. Sometimes manufacturers have to start from the synthesis of polyimide resins.

Several liquid polyimide resins have been developed as the base materials of high-density flexible circuits. Some of these liquid polyimide resins can be photoimaged, and have been used in high volume as the dielectric layer and coverlay in the wireless suspension of hard disk drives.

These liquid polyimide resins could be the major dielectric materials of special high-density flexible circuits that demand extremely high density, down to 5-µm pitches with 10-µm via holes. The cost of these materials is higher than that of polyimide film. However, they have broader capability for meeting nonstandard requirements such as ultrathin substrates with microvia holes. The properties are very dependent on the manufacturer.

65.5.2.4 Type H (HN) Kapton Polyimide Film Details. The polyimides are a class of chemical compounds. The word "imide" refers to the cyclic structure characterized by a double-bond linkage between one nitrogen atom (N) and two carbonyl groups. In a polymer the latter are usually attached to a benzene ring. A polyimide which is presently commercially available is obtained by a polycondensation reaction between an aromatic

tetracarboxylic acid anhydride and an aromatic diamine which yields a polyarnic acid intermediate. The acid is then dehydrated to yield a high-molecular-weight polyimide. Many variations and properties are possible by using a variety of amino compounds. In the case of Kapton, * 4,4’-diaminediphenyl ether, R is used as the aromatic amine. The resultant compound, in film form, is transparent, amber-colored, flexible, flame-resistant, and infusible (chars at 1500°F). It possesses excellent chemical resistance (except for strong inorganic acids and bases), and it has a useful operating range from −430 to 780°F. Its dielectric properties, such as dielectric strength and dissipation factor, are excellent and remain constant over a wide range of temperature and frequency.

The development of polyimide film materials has provided the necessary impetus to the design and manufacture of FPW devices. Shortly after and coincidentally with the introduction of this excellent engineering thermoplastic, FPW took a big jump in applications varying from complicated aerospace computers to camera interconnections. The properties of Kapton polyimide film are as indicated below.

- *Physical and thermal properties:* This polyimide film retains their physical properties over a wide temperature range. They have been used in field applications in which the environmental temperatures have been as low as −269°C and as high as 400°C, but most of the data fall in the −195 to 200°C range. Summaries of the physical and thermal properties of Kapton polyimide film are given in Table 65.10.

TABLE 65.10 Typical Thermal Properties of Kapton Polyimide Film

Property	Typical Values	Test Conditions	Test Methods
Melting point	None		
Zero strength temperature	815°C	20-psi load for 5 s.	Hot bar (DuPont test)
Coefficient of linear expansion	2.0×10^{-5} in/(in°C)	(–) 14°C to 38°C	ASTM: D-696-44
Coefficient of thermal conductivity	3.72×10^{-4} cal.cm/(cm^2)(s)(°C)	25°C	Model TC-1000
	$3\,89 \times 10^{-4}$ cal.cm/(cm^2)(s)(°C)	75°C	Twin Heatmaster
	4.26×10^{-4} cal.cm/(cm^2)(s)(°C)	200°C	Comparative Tester
	4.51×10^{-4} cal.cm/(cm^2)(s)(°C)	300°C	
Specific heat	0.261	cal/(g)(°C)	Differential calorimetty
Flammability	Self-extinguishing		
Heat-sealable	No		

[a]Kapton is a registered trademark of E. I du Pont de Nemours & Company.

- *Tensile stress-strain:* A series of tensile stress-strain curves for 0.001 in polyimide film as a function of temperature is shown in Fig. 65.4.

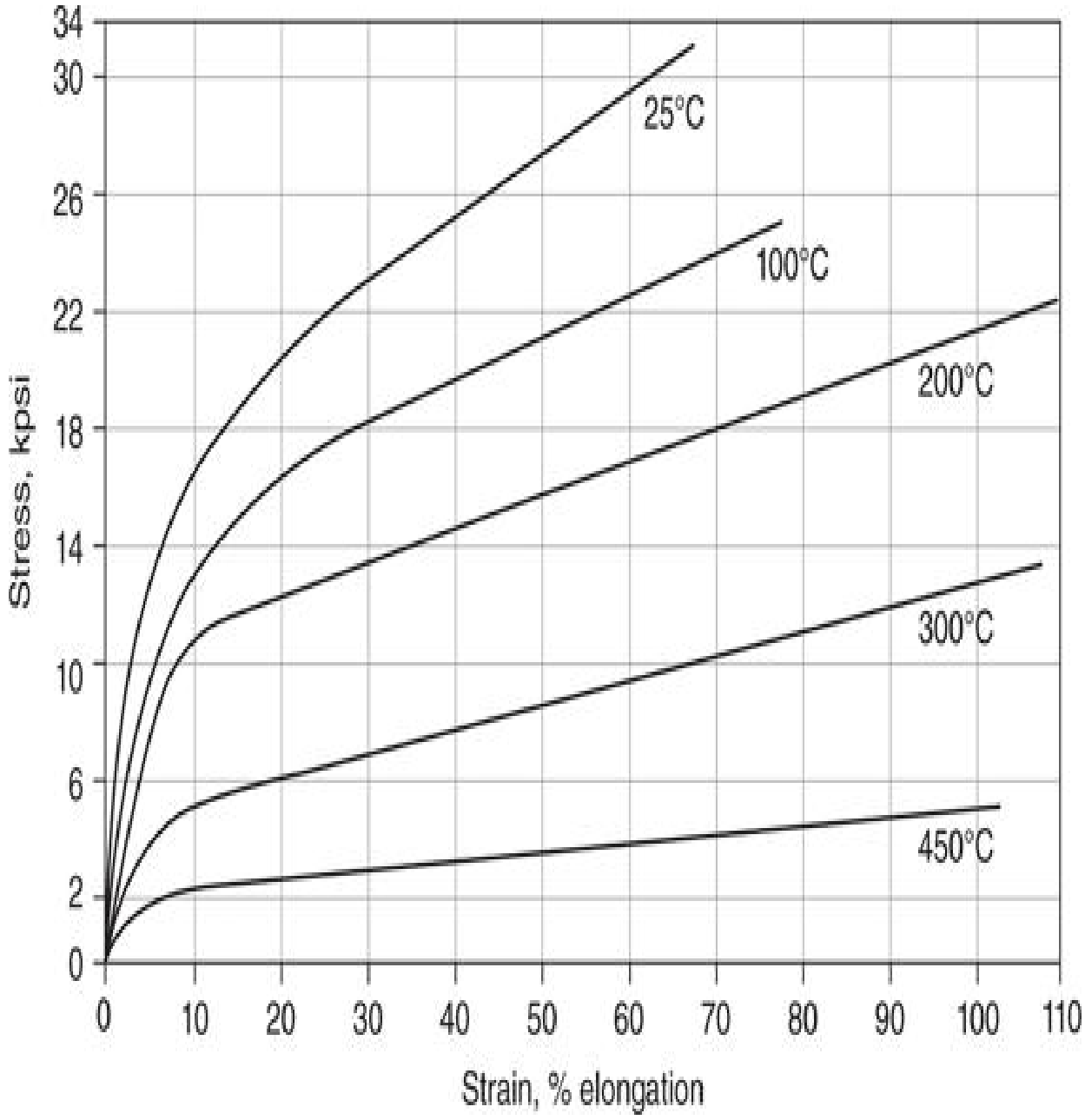

FIGURE 65.4 Tensile stress-strain curves of Kapton polyimide film.

The unusual values of tensile strength, tensile modulus, and ultimate elongation at various temperatures can be obtained from the typical stress-strain curves shown. Such properties as tensile strength and modulus have an inverse relation with temperature, and elongation peaks to a maximum value at 200 to 250°C. Other factors such as humidity, film thickness and Instron elongation rate were

found to have only a negligible effect on the shape of the 25°C curve.

- *Hydrolytic stability:* Kapton polyimide film is made by a condensation reaction therefore, its properties are affected by water. Although long-term exposure to boiling water, as shown in Figs. 65.5 and 65.6, will reduce the level of film properties, sufficient tensile and elongation remain to ensure good mechanical performance. A decrease in the temperature and water concentration will reduce the rate of Kapton property reduction, and higher temperatures and pressures will increase.

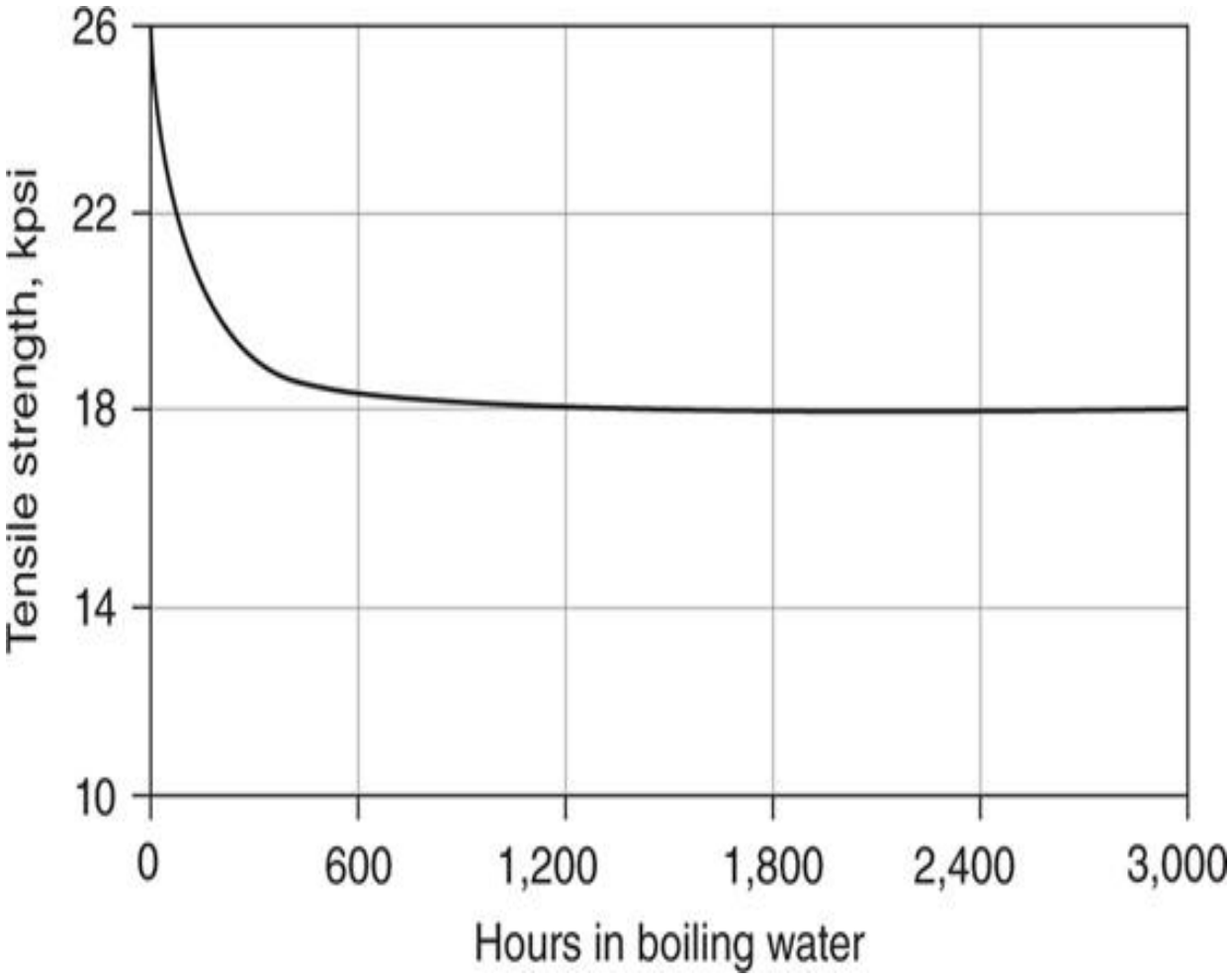

FIGURE 65.5 Tensile strength of Kapton polyimide film after exposure to water at 100°C.

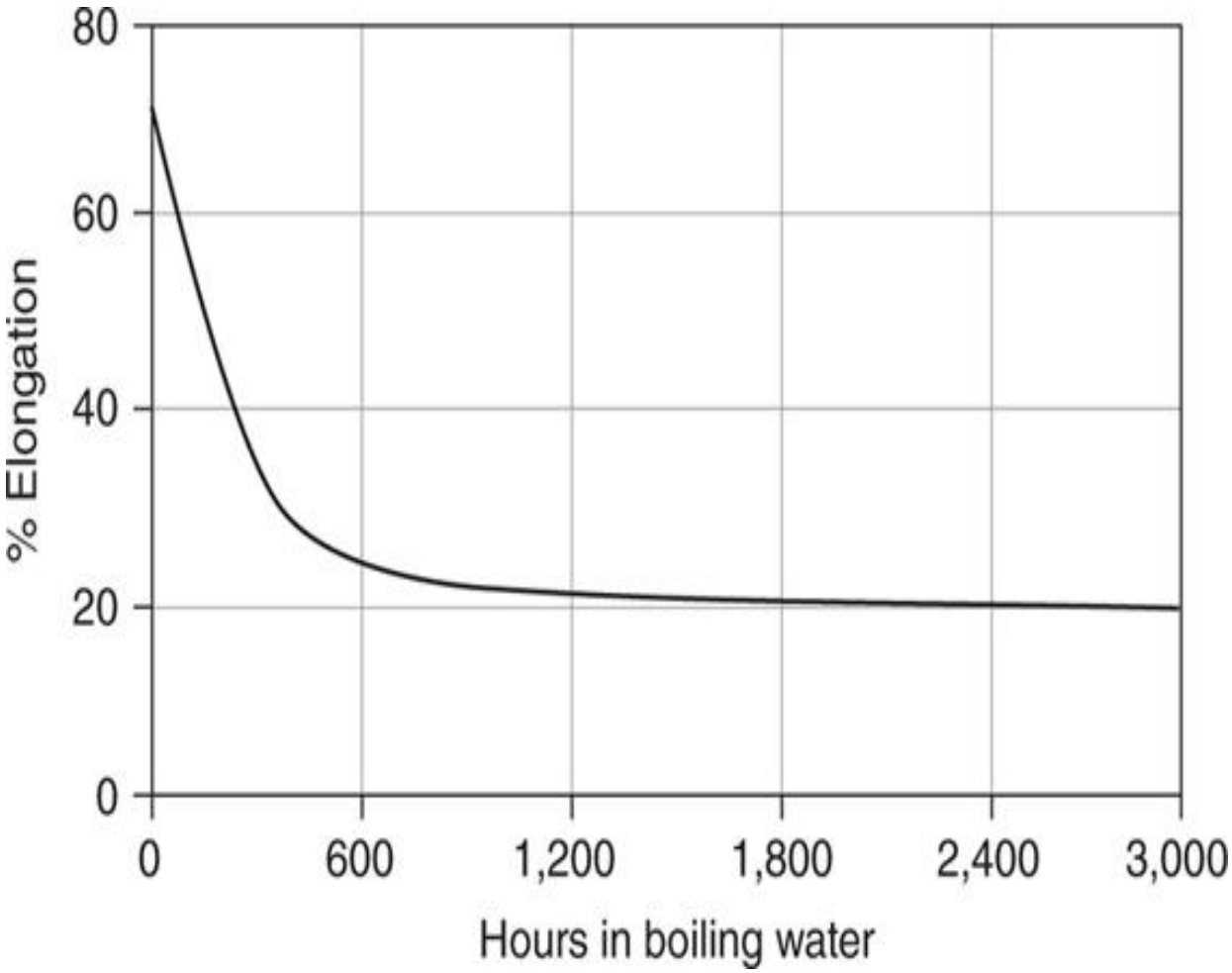

FIGURE 65.6 Ultimate elongation of Kapton polyimide film after exposure to water at 100°C.

- *Dimensional stability:* The dimensional stability of Kapton polyimide film depends on two factors: the normal coefficient of thermal expansion, and the residual stresses placed in the film during manufacture. The latter cause Kapton to shrink on its first exposure to elevated temperatures as indicated in the bar graphs in Fig. 65.7. Once the film has been exposed, the normal values for thermal expansion listed in Table 65.11 can be expected.

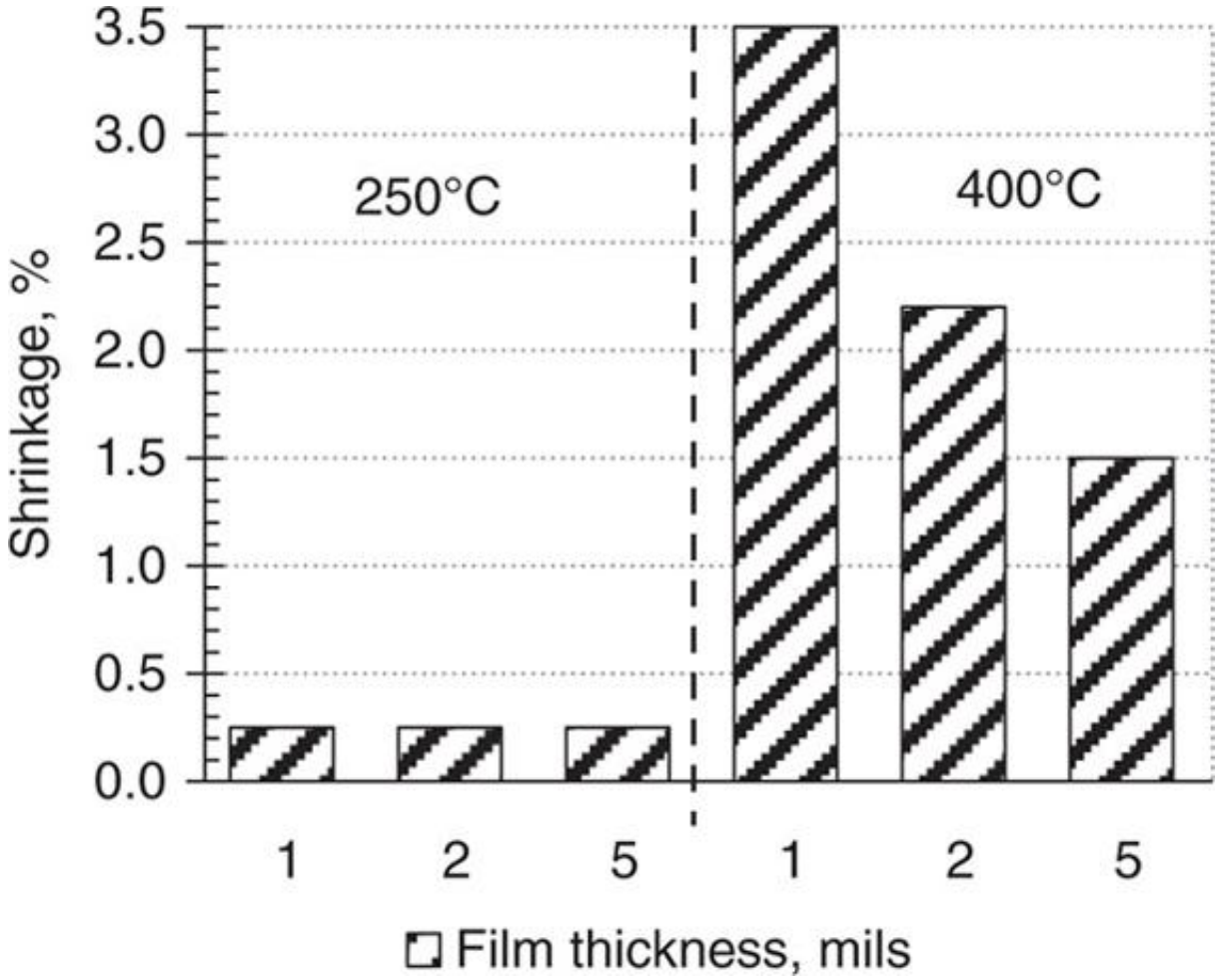

FIGURE 65.7 Residual shrinkage versus exposure temperature and gauge for 0.001 in, type H Kapton polyimide film.

TABLE 65.11 Thermal Coefficient of Expansion of Kapton Polyimide Film Thermally Exposed

Temperature Range, °C	K, in/(in)(°C) $\times 10^5$
23–100	1.80
100–200	3.10
200–300	4.85
300–400	7.75
23–400	4.55

The dimensional changes of the film as a function of temperature and orientation and after etching in ferric chloride are shown in Tables 65.12 and 65.13. The shrinkage rates of Kapton in the machine direction (MD) and cross machine direction (XD) at 150°C and 250°C as shown in Figs. 65.8 and 65.9. The dimensional change of Kapton film is the MD and XD as a function of relative humidity is shown in Fig. 65.10.

TABLE 65.12 Dimensional Change of Kapton Polyimide Film at 150°C and after Etching

	0.001 in Film				0.002 in Film			
	Mean		2 sigma		Mean		2 sigma	
Conditioning	MD	XD	MD	XD	MD	XD	MD	XD
150°C for 30 min	1.01	1.18	0.29	0.48	1.14	1.29	0.32	0.32
150°C for 30 min + recycle 150°C for 30 min	0.10	0.09	0.18	0.16	0.10	0.08	0.12	0.14
Etchant ($FeCl_3$)	0.47	0.56	0.16	0.32	0.48	0.51	0.16	0.26
150°C for 30 min + etchant	0.14	0.12	0.26	0.24	0.18	0.16	0.10	0.24

MD = machine direction
XD = cross machine direction

TABLE 65.13 Dimensional Change of Kapton Polyimide Film at 250°C and after Etching

	0.001 in Film				0.002 in Film			
	Mean		2 sigma		Mean		2 sigma	
Conditioning	MD	XD	MD	XD	MD	XD	MD	XD
250°C for 30 min	2.17	2.30	0.46	1.01	2.26	2.26	0.48	0.80
250°C for 30 min + recycle 250°C for 30 min	−0.04	−0.03	0.12	0.10	0.00	0.02	0.08	0.16
Etchant ($FeCl_3$)	0.47	0.56	0.16	0.32	0.48	0.51	0.16	0.26
250°C for 30 min + etchant	0.06	0.01	0.16	0.24	0.07	0.08	0.16	0.18

MD = machine direction
XD = cross machine direction

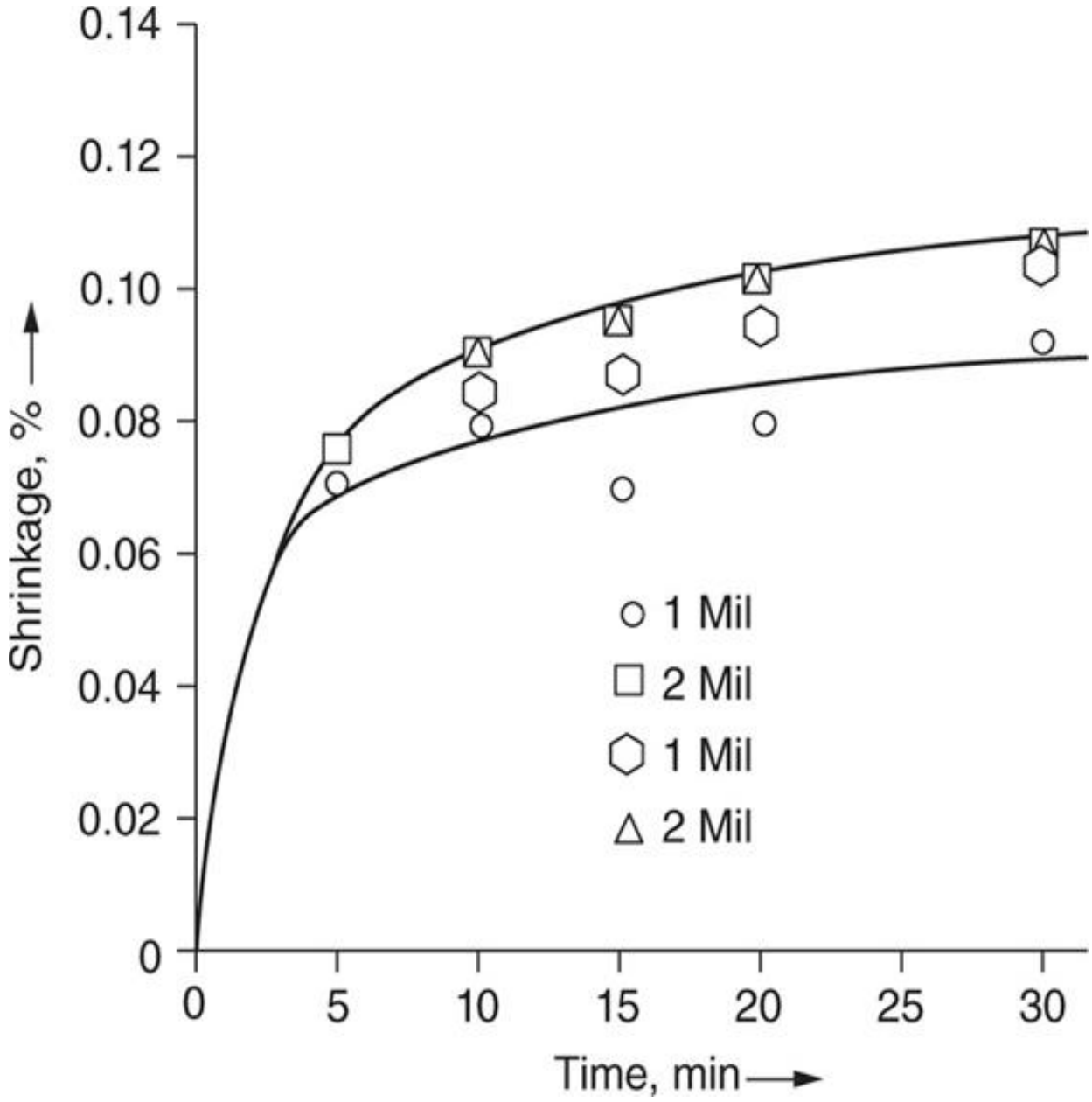

FIGURE 65.8 Shrinkage rate of Kapton polyimide film at 150°C in machine direction (MD).

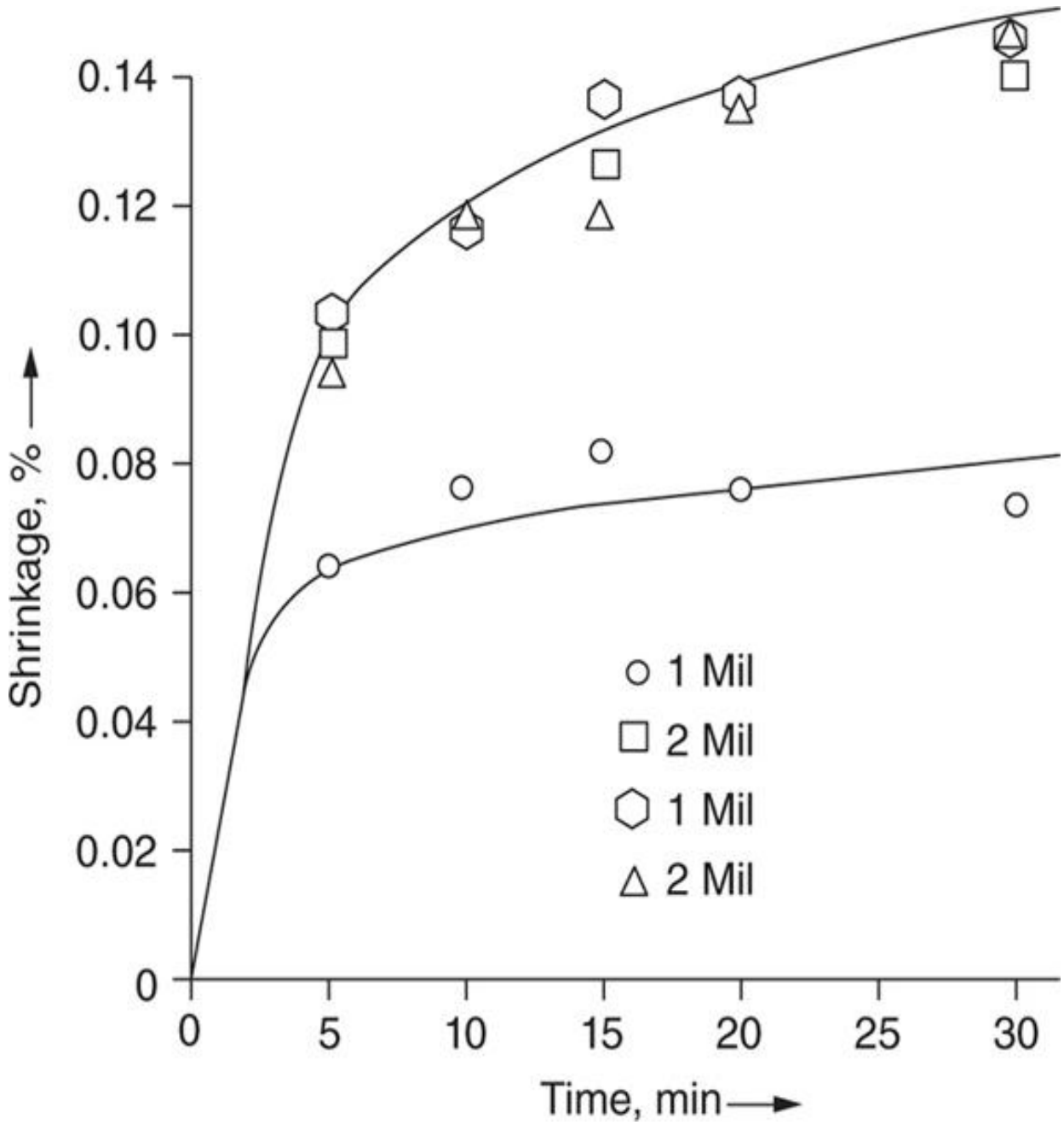

FIGURE 65.9 Shrinkage rate of Kapton film at 150°C on cross-machine direction (XD).

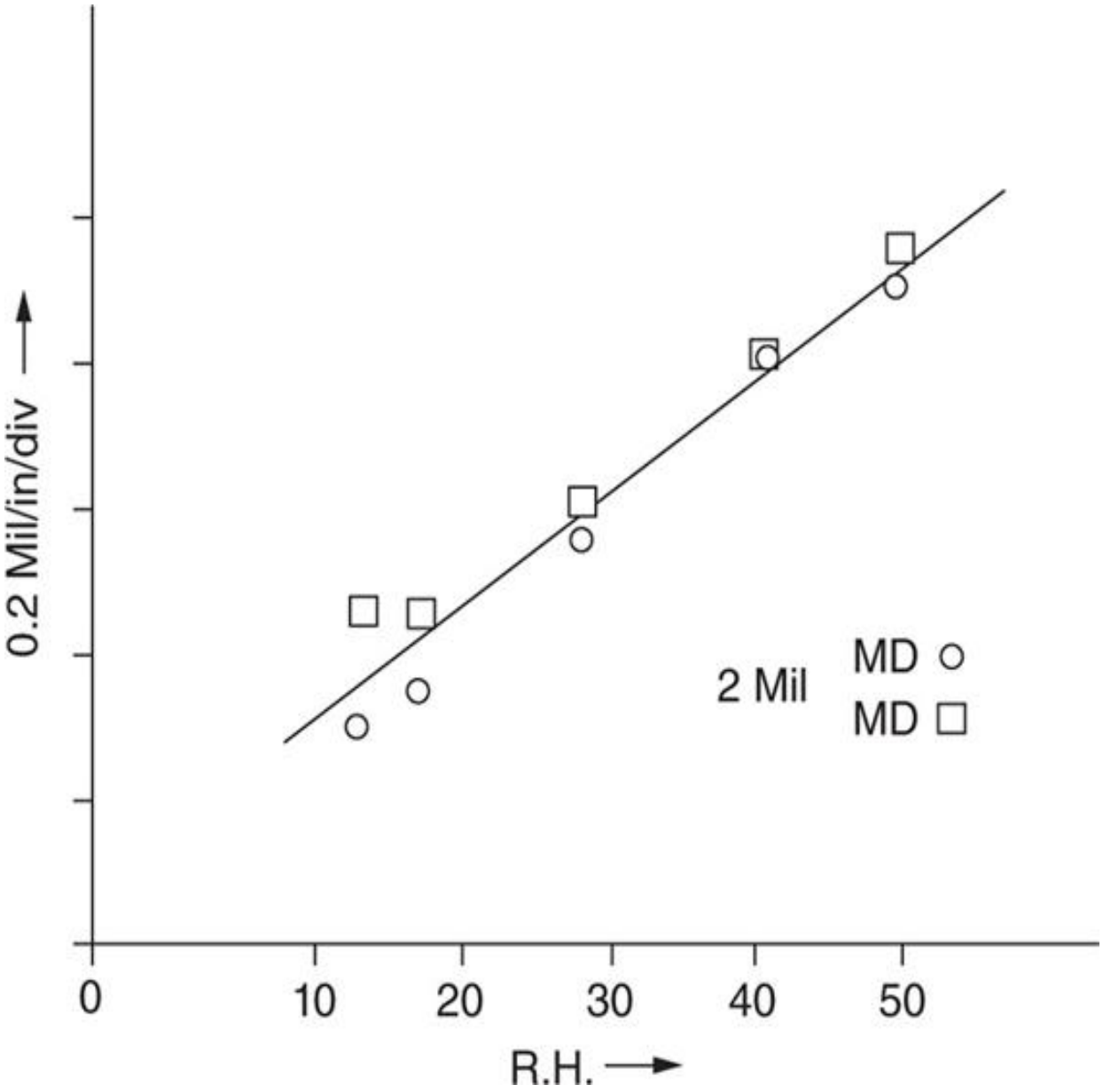

FIGURE 65.10 Dimensional change of Kapton film versus relative humidity.

- *Cut-through and cold-flow film:* Most organic films exhibit a tendency to flow or thin out under high compressive stresses, especially at elevated temperatures. Kapton film possesses an extremely high resistance to such stresses. Test procedures described: ASTM D-876-61 have been adapted to flat films to provide data in Figs. 65.11 and 65.12. Stresses range from an infinitely high point load to 12,000 psi at cut-through for 0.001 in film.

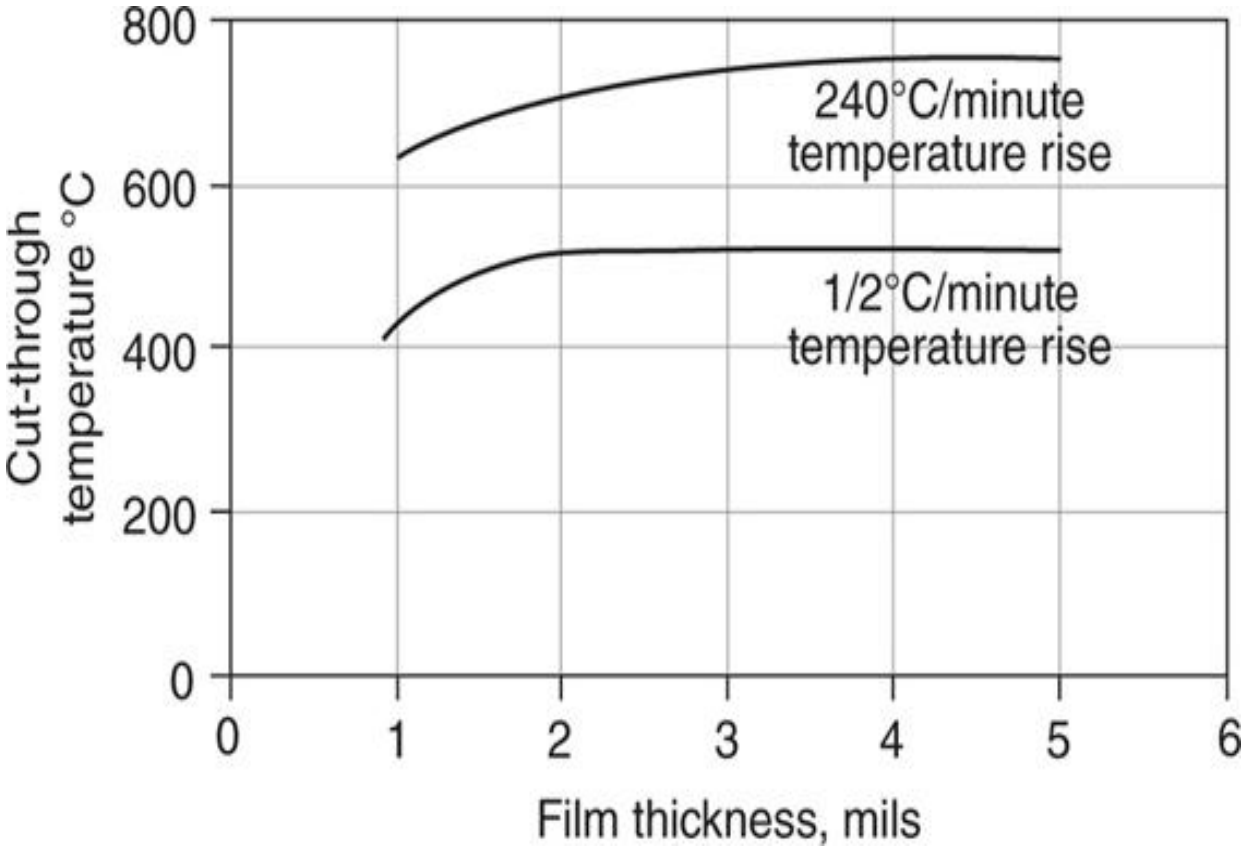

FIGURE 65.11 Cut-through temperature of Kapton film versus rate of temperature rise and gauge.

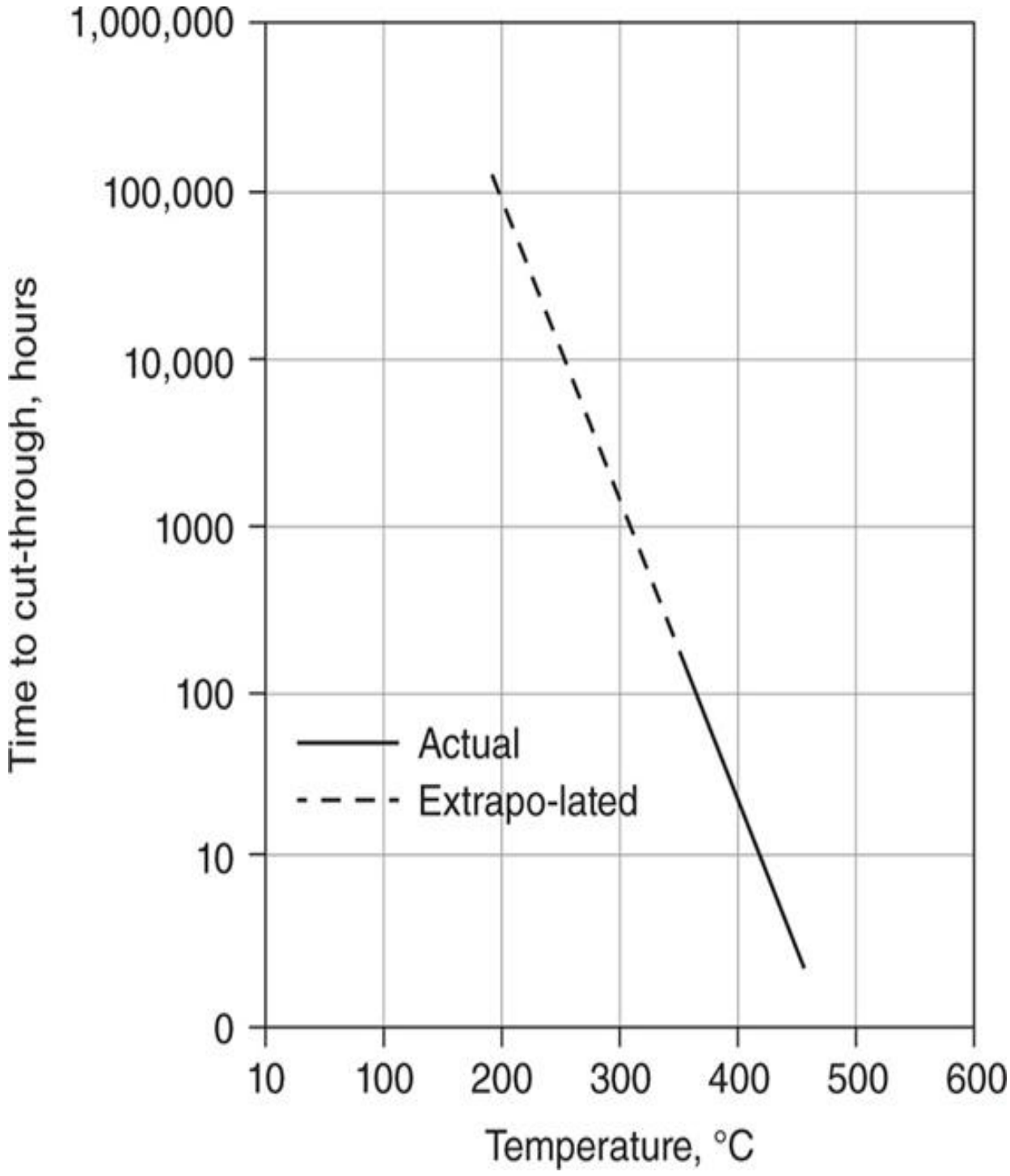

FIGURE 65.12 Resistance to cut-through temperature of Kapton film versus temperature.

Kapton film is subject to oxidative degradation. Therefore, its useful life is a function of both temperature and oxygen concentration in the test environment. The

effect of those factors is shown in Figs. 65.13 to 65.16 and Table 65.14.

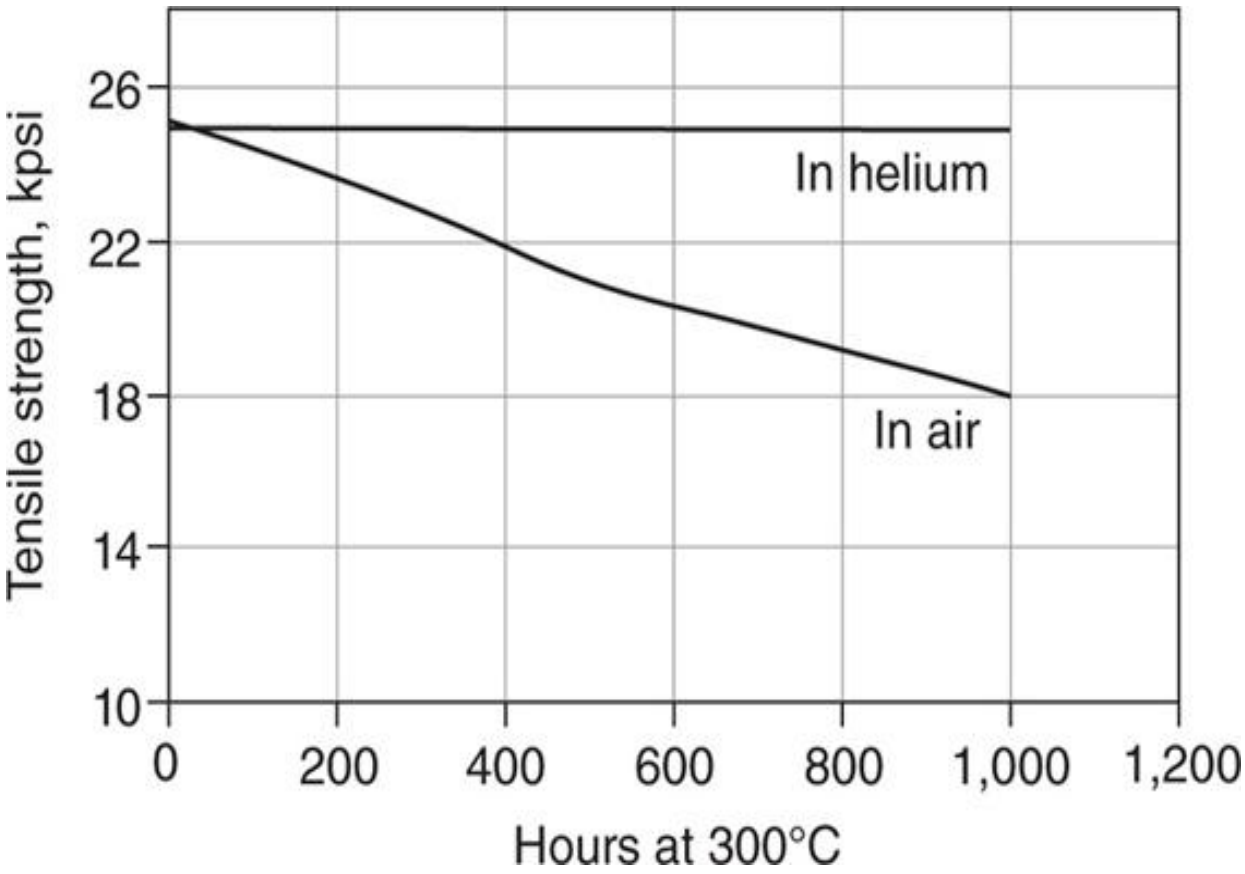

FIGURE 65.13 Tensile strength of 0.001 in Kapton film versus aging at 300°C.

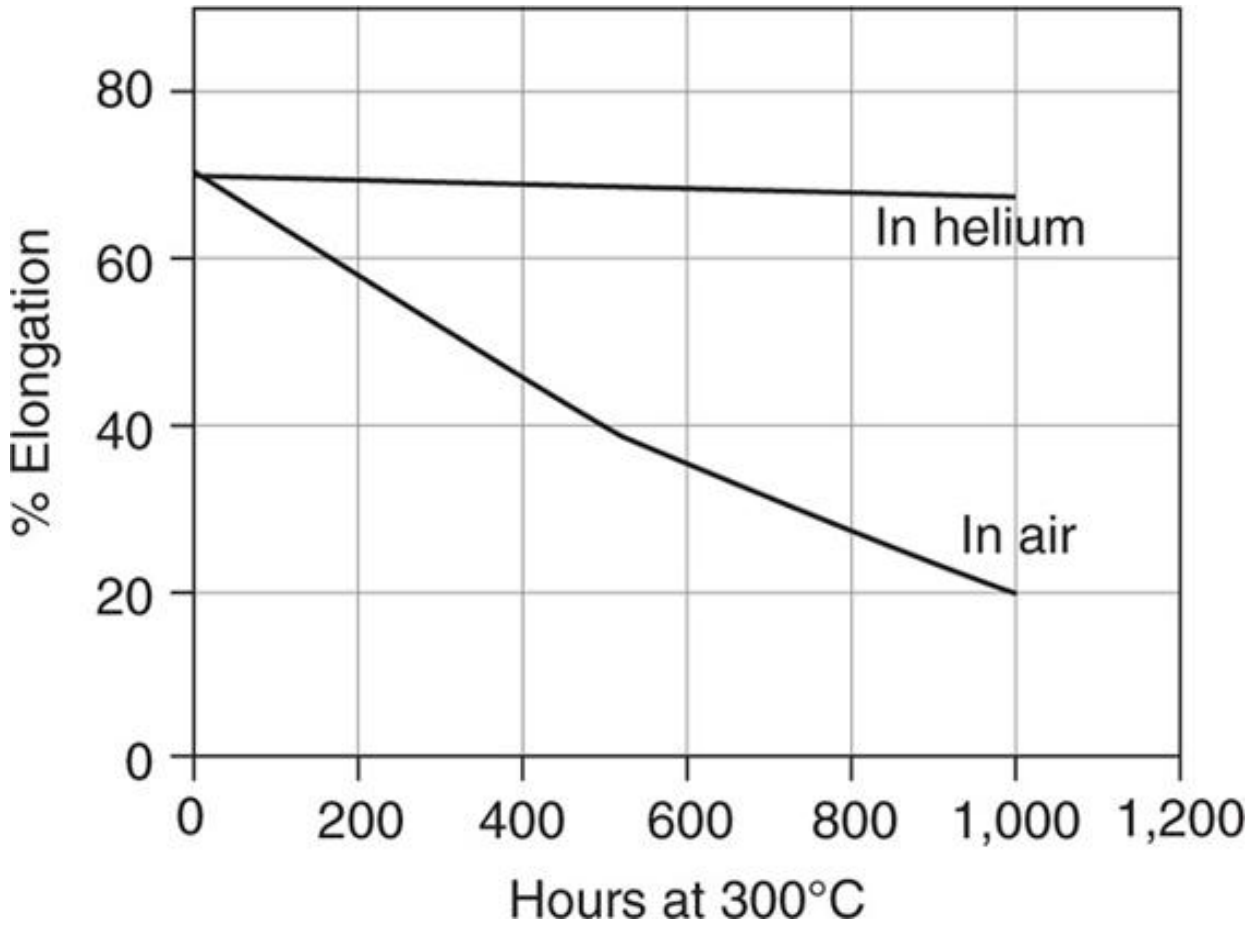

FIGURE 65.14 Ultimate elongation of 0.001 in Kapton film versus aging at 300°C.

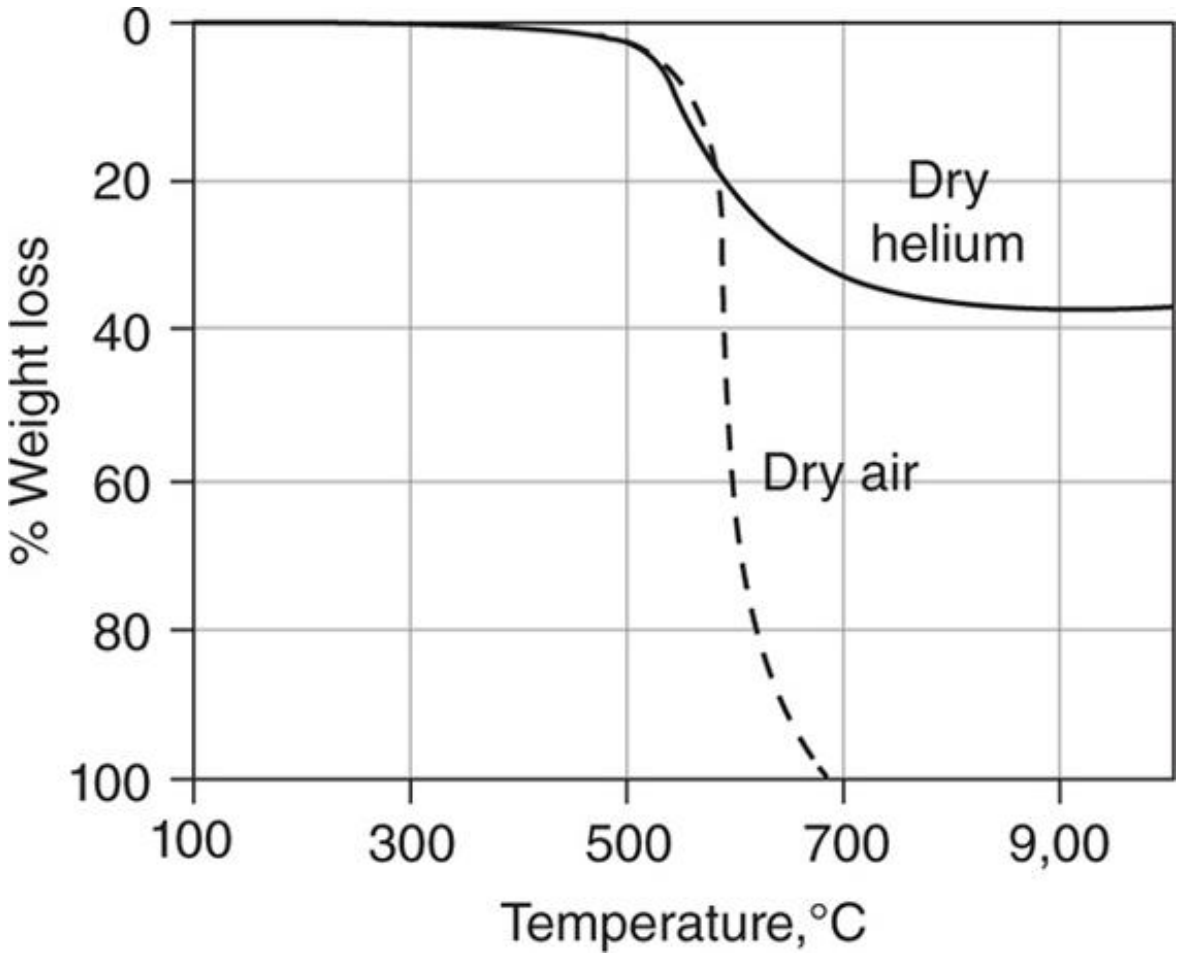

FIGURE 65.15 Weight loss of 0.001 in Kapton film at a temperature rise of 3°C min.

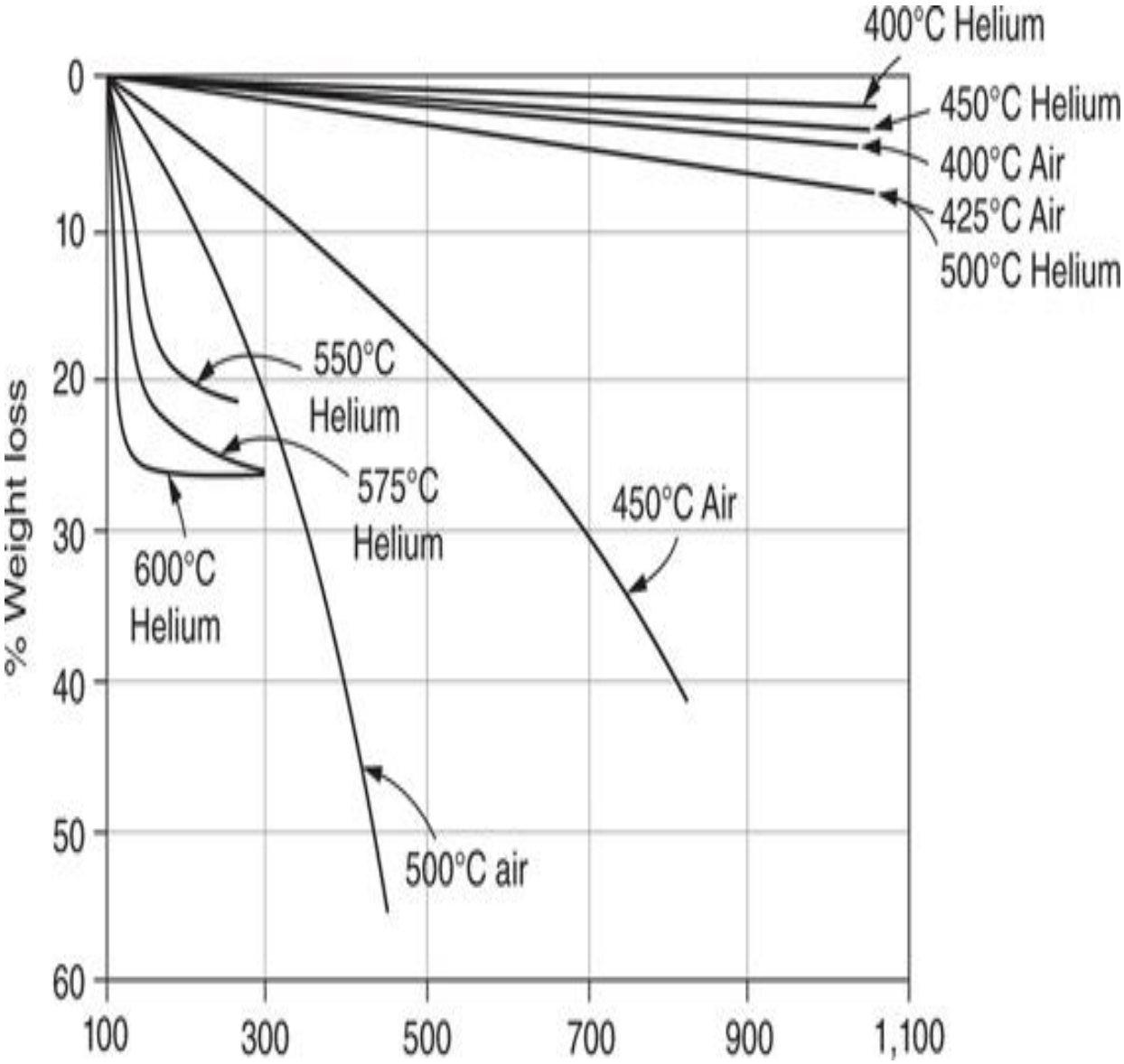

FIGURE 65.16 Isothermal weight loss of 0.001 in Kapton polyimide film.

TABLE 65.14 Time Required for Reduction in Ultimate Elongation from 70 to 1 Percent of 0.001 in Kapton Polyimide Film

Temperature, °C	Environment	
	Air	Helium
450	2h	22 h
425	5h	3½ days
400	12 h	2 weeks
375	2 days	2 months
350	6 days	1 year
300	3 months	
275	1 year	
250	8 years	

- *Electrical properties of Kapton polyimide film* The most common electrical properties of Kapton film in various gauges are given in Table 65.15. They are measured at 25°C and 50 percent relative humidity. The effects of such factors as humidity, temperature, and frequency on these basic values are shown in forthcoming tables.

TABLE 65.15 Typical Electrical Properties of Kapton Polyimide Film

Property	Typical Value	Test Condition	Test Method
Dielectric strength			
0.001 in	7000 V/in × 10^{-3}	60 cycles	ASTM D-149-61
0.002 in	5400 V/in × 10^{-3}	¼ in. electrodes	
0.003 in	4600 V/in × 10^{-3}		
0.005 in	3600 V/in × 10^{-3}		
Dielectric constant			
0.001 in	3.5		
0.002 in	3.6	1 kHz	ASTM D-150-59T
0.003 in	3.7		
0.005 in	3.7		
Dielectric factor			
0.001 in	0.0025		
0.002 in	0.0025	1 kHz	ASTM D-150-59T
0.003 in	0.0025		
0.005 in	0.0027		
Volume resistivity			
0.001 in	1×10^{18} Ω·cm		
0.002 in	8×10^{17} Ω·cm	125 V	ASTM D-257-61
0.003 in	5×10^{17} Ω·cm		
0.005 in	1×10^{17} Ω·cm		
Corona threshold voltage			
0.001 in	465 V		
0.002 in	550 V		
0.003 in	630 V	60 cycles	ASTM 1868-61T
0.005 in	800 V	¼ in electrodes	
0.005 in H, 0.002 in FEP			
0.005 in H, 0.0005 varnish	1600 V		

- *Effect of humidity* Because the water content of Kapton film can affect the film's electrical properties, electrical measurements are presented for 0.001-in film after exposure to environments of various humidities at 25°C. The amount of moisture absorbed in Kapton film depends upon the relative humidity, as shown in Fig. 65.17. Table 65.16 shows the effect of humidity on the electrical properties of Kapton film. The effect of temperature on the value of the dielectric constant and dissipation factor of Kapton film at various isotherms are shown in Figs. 65.18 to 65.21.

TABLE 65.16 Relative Humidity versus Electrical Properties of Kapton Polyimide Film

Relative Humidity, %*	AC Dielectric Strength, V/in × 10^{-3}	Dielectric Constant	Dissipation Factor
0	7800	3.0	0.0018
30	7300	3.3	0.0021
50	7000	3.5	0.0025
80	6500	3.7	0.0037
100	6200	3.9	0.0047

*For calculations involving absolute content, 50% RH in our study is equal to 1.3% water in the film and 100% RH is equal to 2.9% water, the maximum absorption possible regardless of the driving force.

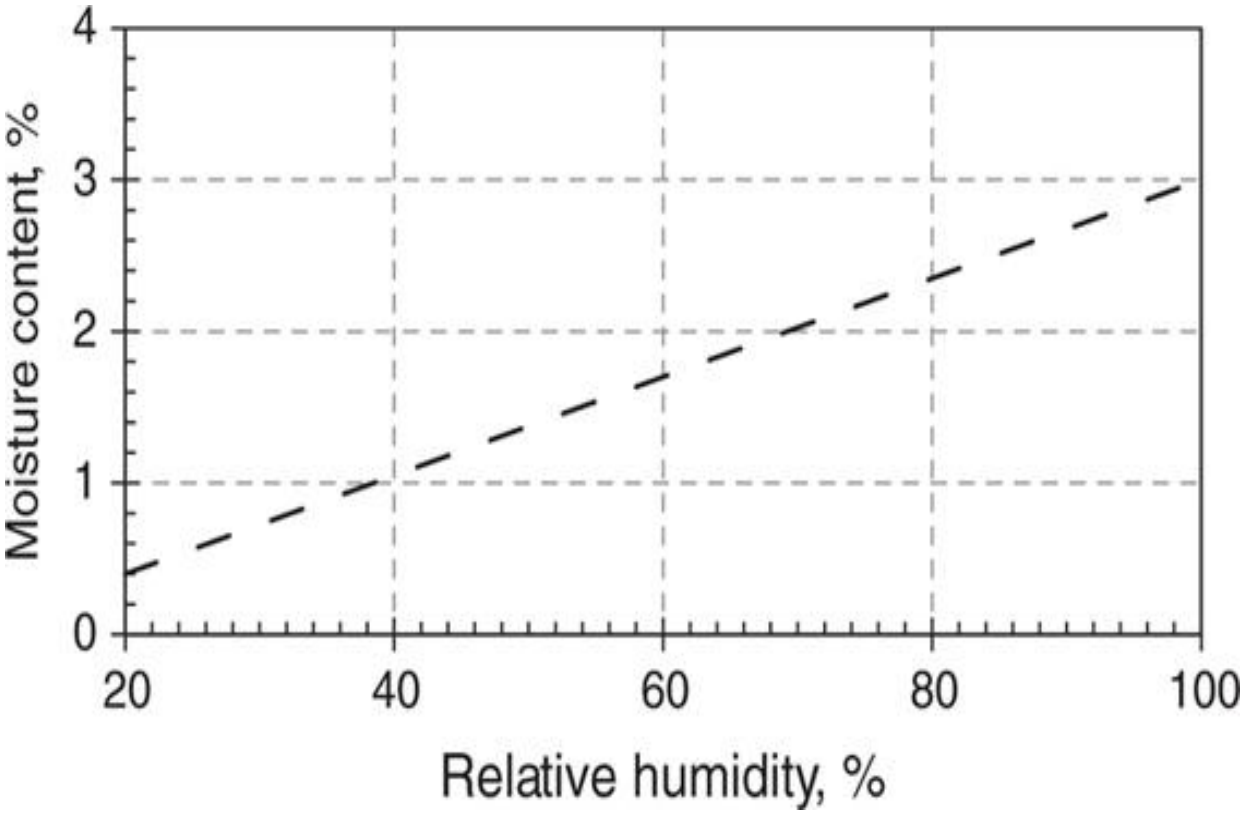

FIGURE 65.17 Moisture content of Kapton polyimide film versus typical relative humidity values at 23°C.

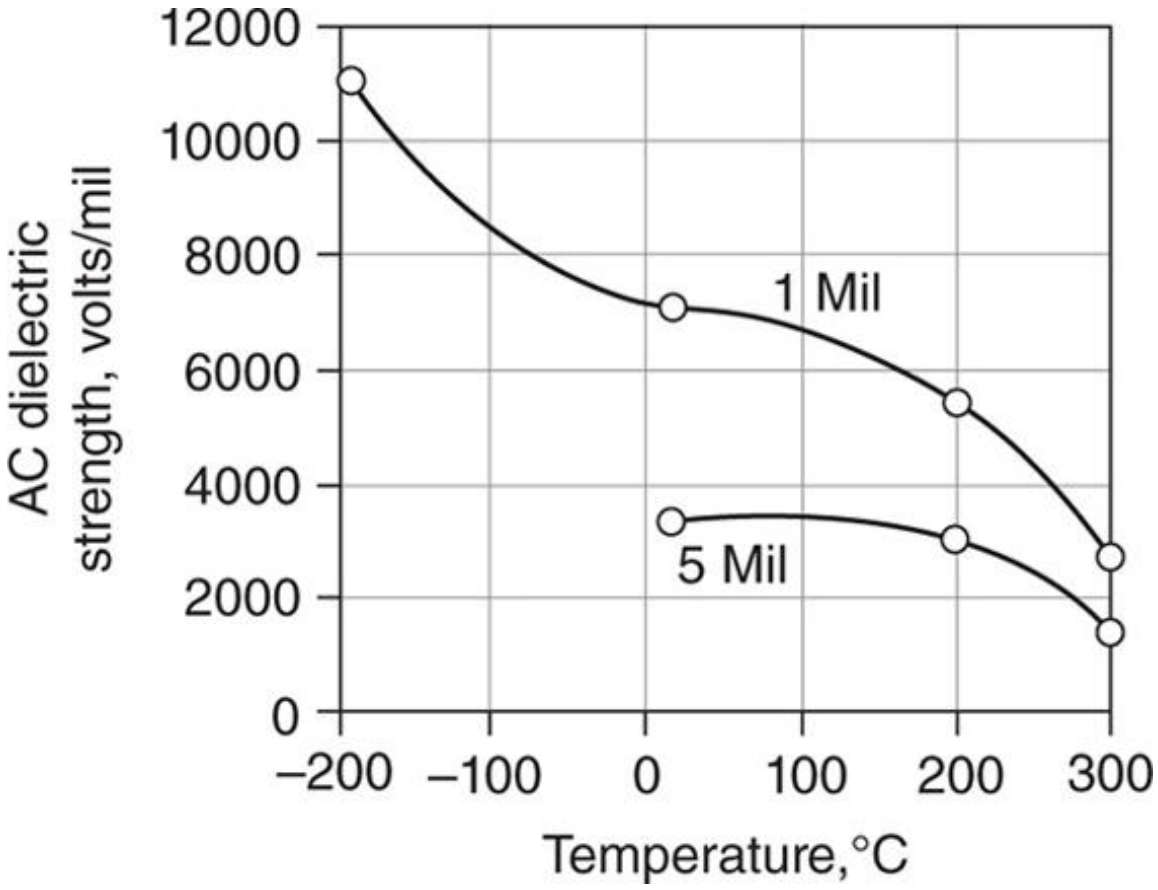

FIGURE 65.18 AC dielectric strength of 0.001-in Kapton film versus temperature.

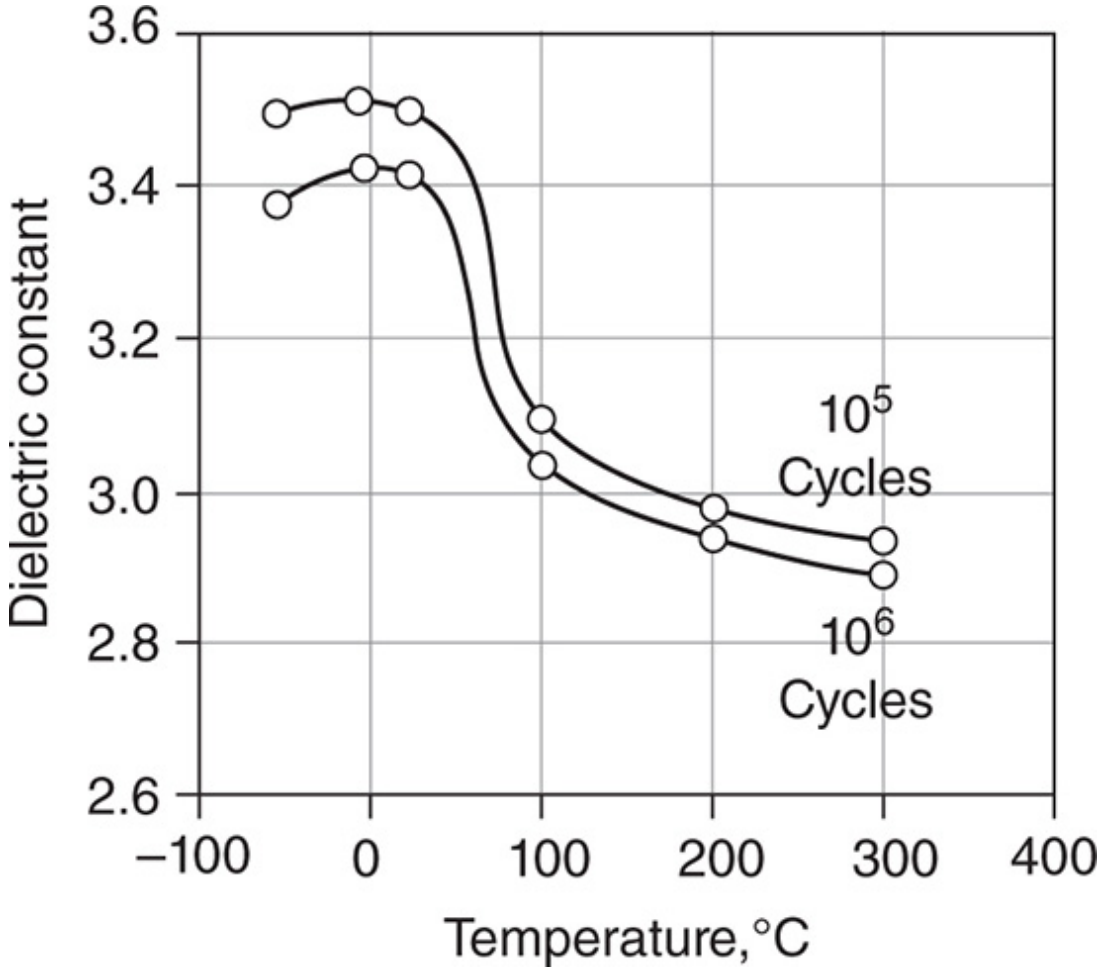

FIGURE 65.19 Dielectric constant of 0.001-in Kapton film versus temperature.

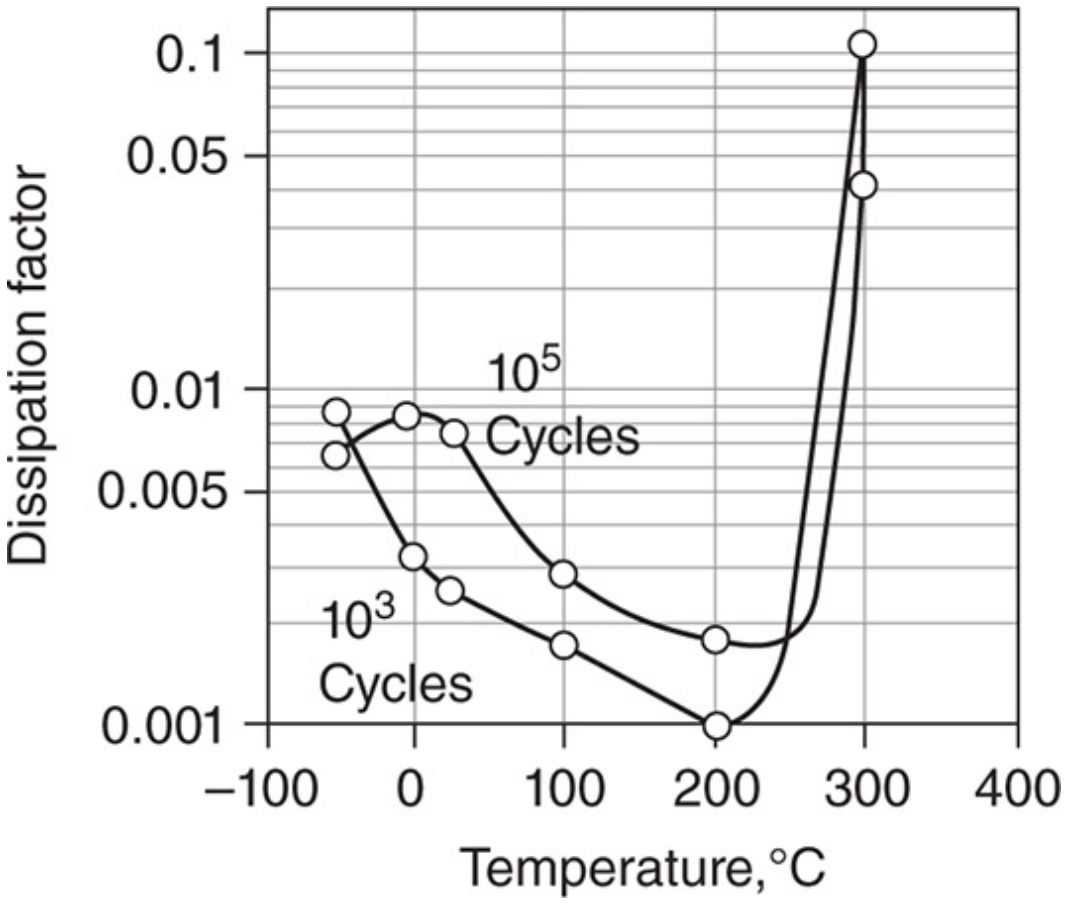

FIGURE 65.20 Dissipation factor of 0.001-in Kapton film versus temperature.

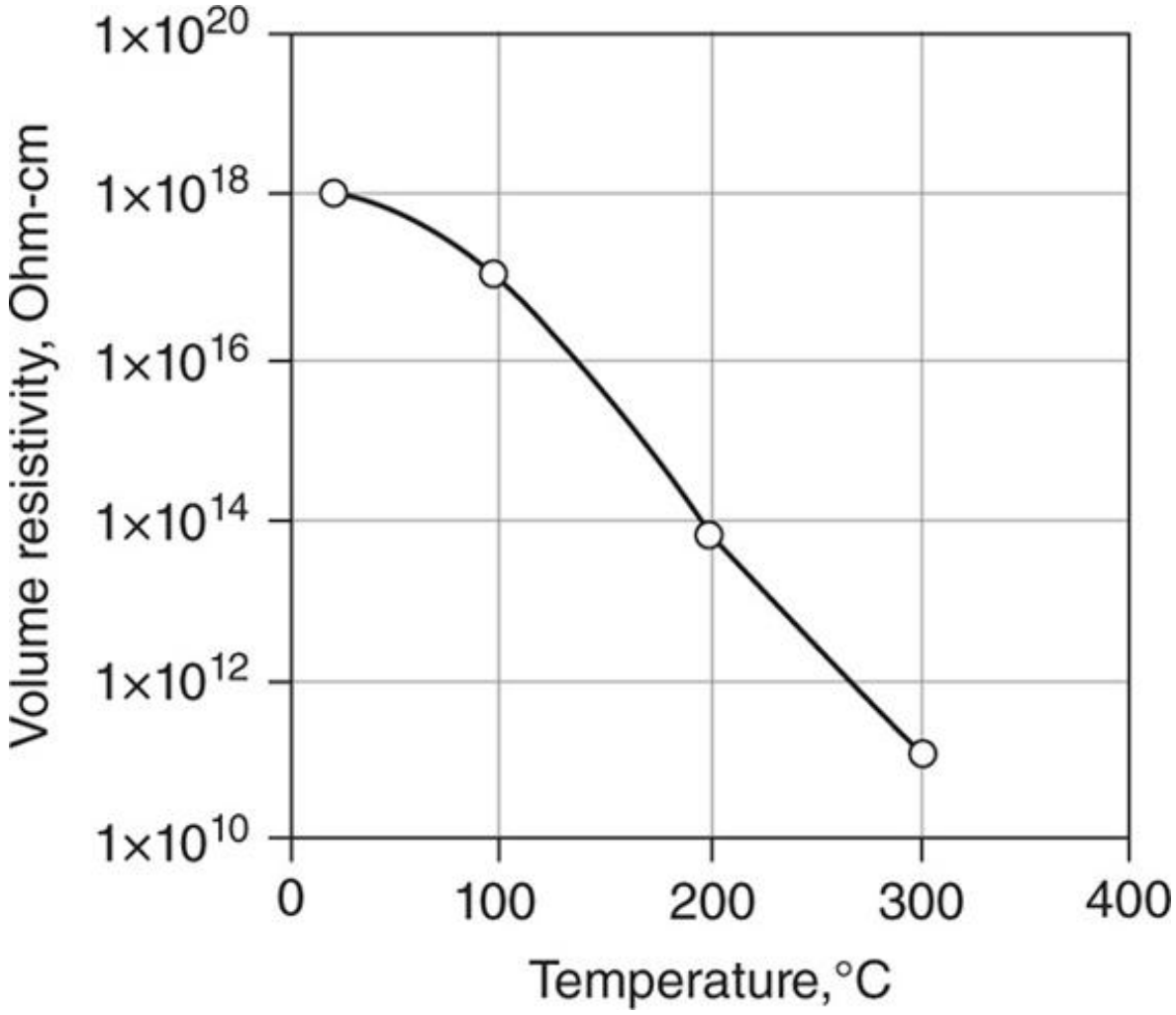

FIGURE 65.21 Volume resistivity of 0.001-in Kapton film versus temperature.

- *Effect of frequency* The effects of frequency on the value of the dielectric constant and dissipation factor of Kapton film at various isotherms are shown in Figs. 65.22 and 65.23.

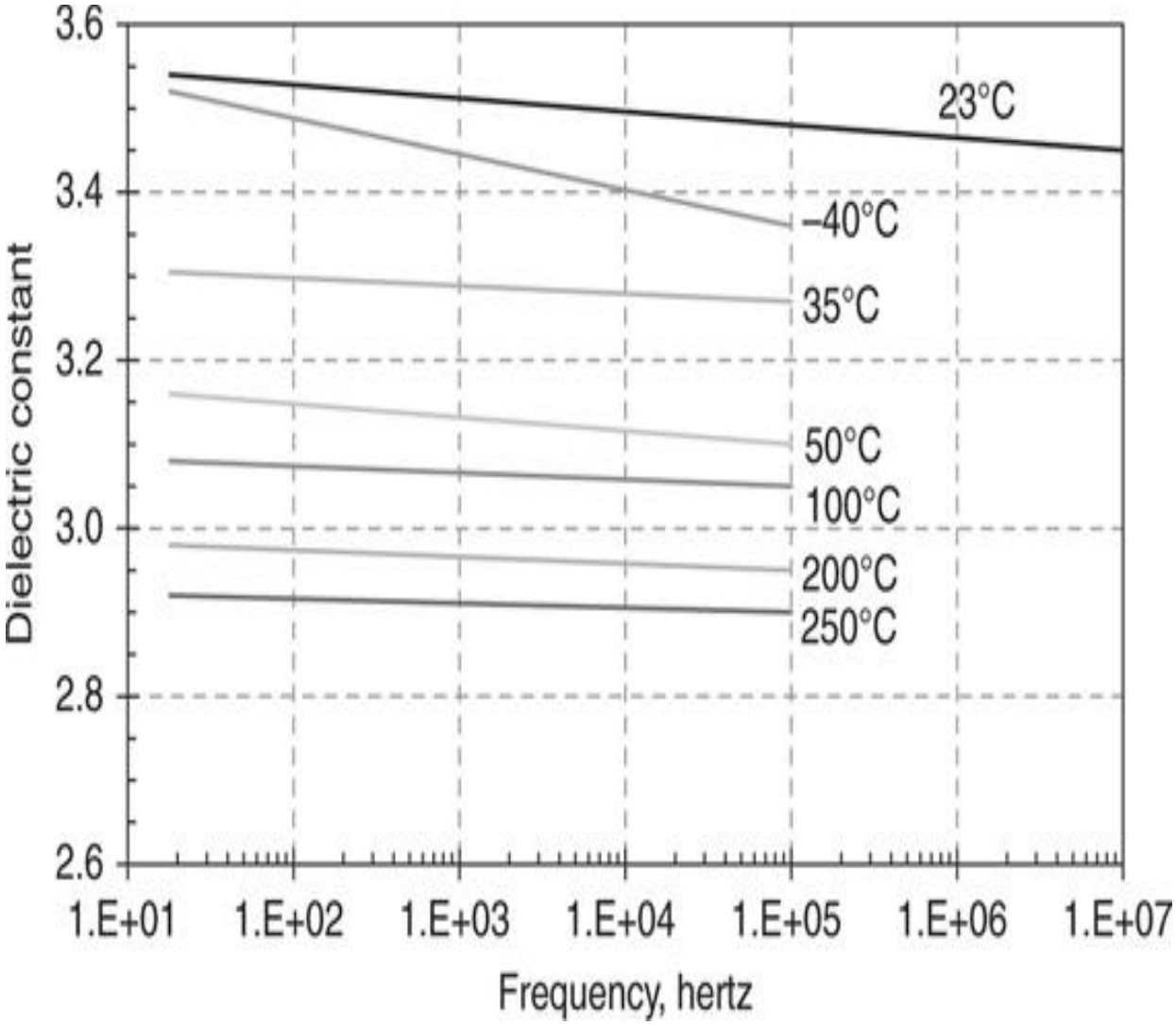

FIGURE 65.22 Volume resistivity of 0.001-in Kapton film versus temperature.

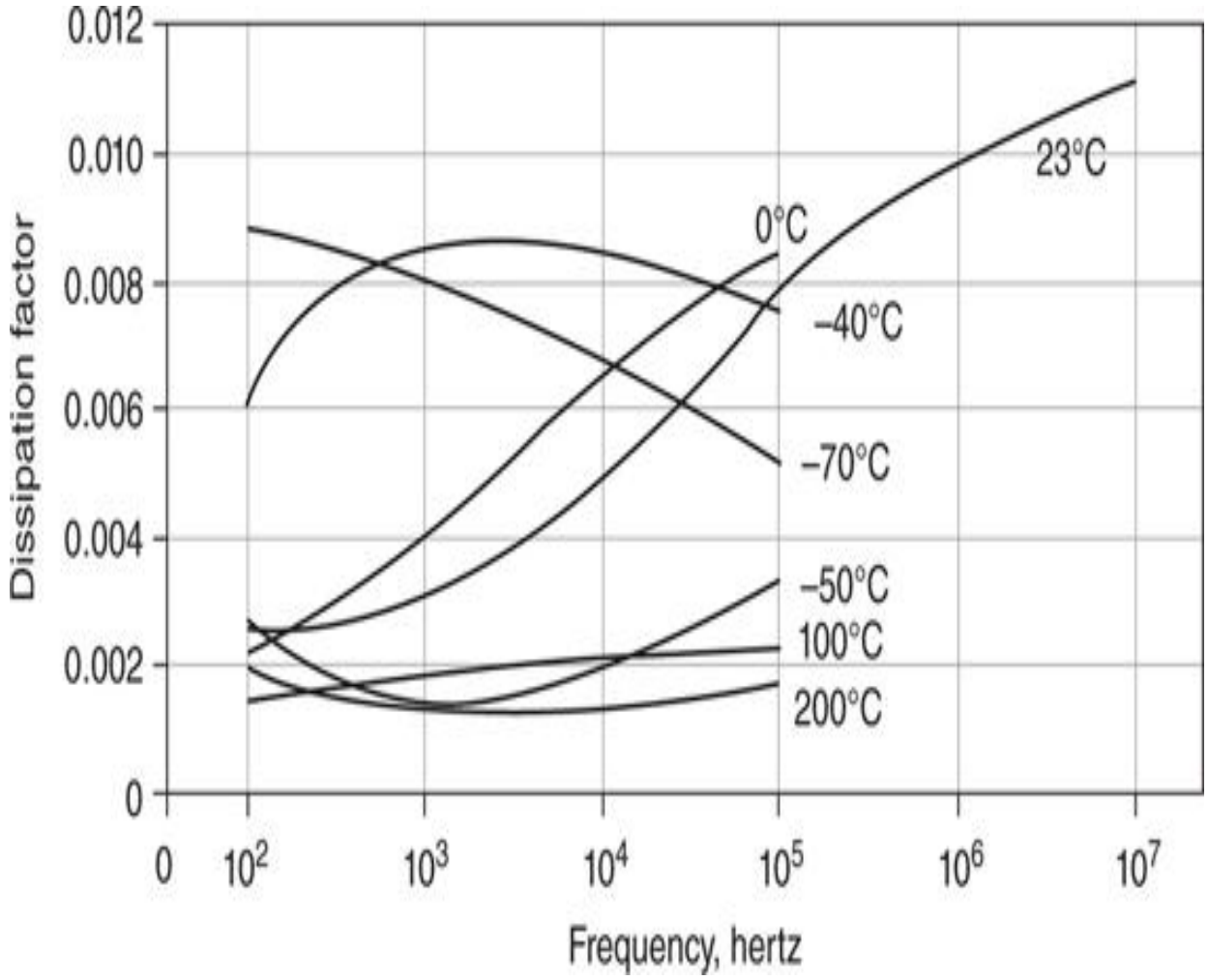

FIGURE 65.23 Volume resistivity of 0.001-in Kapton film versus temperature.

- *Conditioning prior to lamination Kapton polyimide film* In making and processing copper laminates and flexible printed wiring, it must be remembered that, under normal plant conditions, Kapton contains small amounts of moisture absorbed from the atmosphere. The moisture does not have a major effect on film properties, but it must be eliminated during high-temperature manufacturing and processing steps to avoid blisters and delamination in laminates and circuits.

During lamination to copper and any subsequent high-temperature processing steps, moisture must be dried from Kapton to avoid blistering and delamination of the film from

copper. Under severe high-temperature lamination conditions, embrittlement of the Kapton can occur. The rate at which moisture is absorbed or dried from Kapton depends on the temperature, relative humidity, film thickness and adhesive coating. Sheets of uncoated Kapton type H conditioned at 23°C, 100 percent RH and then placed in a 23°C, 0 percent RH dry box lost moisture at the rate shown in Table 65.17.

TABLE 65.17 Rate of drying of Kapton Polyimide Film at 23°C

Film Thickness, in	Time for Half of Moisture to Leave Film, min
0.001	3
0.002	10
0.003	21
0.005	54

65.5.3 Polyester Film

The most significant polyester used in the manufacture of flexible printed wiring is that referred to as Mylar, which chemically is polyethylene terephthalate. It is formed by the condensation reaction of ethylene glycol and terephthalic acid, and it is available only in film form. Its unusual balance of properties makes it especially useful in electrical and electronics fields as a replacement for heavier, conventional insulating materials. Mylar polyester film has a dielectric strength of 700 V/in $\times 10^{-3}$ for 0.001-in film, a tensile strength of 23,000 psi, and excellent resistance to most chemicals and moisture; it can withstand temperature extremes from −60 to 150°C. It remains flexible and does

not become brittle with age. Mylar can be laminated, embossed, metalized, punched, dyed, or coated. Adhesives are available for laminating it to itself and practically any other material. The film can also be coated with heat-sealable, friction, or abrasive materials.

There are eight types of Mylar polyester film. Each is manufactured in roll or sheet form in a range of thicknesses from 0.00025 to 0.0140 in and in widths from ½ to 60 to 72 in depending on gauge and type. It is important to know the correct type in order to specify properly. The individual types are as follows:

1. Type A. General-purpose; has exceptional high-temperature durability properties. It is available up to 0.014 in thick. This type is normally used in motors, wire and cable, lamination, and flexible printed wiring.
2. Type C. Has a higher level of insulation resistance than type A films; it also has more clarity and sparkle than type A film. It is especially designed for capacitors, and it is also normally used for metallization and metallic yarn.
3. Type D. Has high transparency in the heavier gauges. It is used in cartography and drafting and for graphic arts applications where appearance and dimensional stability are important.
4. Type HS. Used for jackets of capacitors. It shrinks 30 percent in both directions when heated to 100°C. The film remains strong and tough after shrinking.
5. Type M. Has a heat-sealable polymer coating and is highly moisture proof. Like all types of Mylar polyester film, it does not get brittle with age and has a long shelf life.
6. Type S. For stationery supplies, book jackets, and sheet protectors. The film is very transparent and has a brilliant surface.

7. Type T. Has an unusually high tensile strength in the longitudinal direction. It has more longitudinal stiffness than equivalent gauges of the other films. It is used for magnetic and pressure-sensitive tapes.
8. Type W. Resistant to the sun's ultraviolet radiation. It was specifically developed for exterior glazing applications. Greenhouses made with it last 4 to 7 years in sun or snow.

The important physical, thermal, and electrical properties of Mylar are given in Table 65.18. The properties of Mylar (polyester) and Kapton (polyimide) are similar except for the higher temperature capability of the polyimides films.

TABLE 65.18 Basic Properties of PET Films (Nonflammable Grade)

Test Items	Properties	
	MD	TD
Tensile strength (kgf/mm^2)	16	16
Elongation	110%	100%
Edge tear resistance (kgf/mm)	51	58
Folding endurance	37,000 times	39,000 times
Heat shrinkage	1.4%	−0.2%
CTE	30 ppm	
CHE	10 ppm	
Water absorption	0.7%	
Volume resistivity	4 × exp 15 Ω-cm	
Dielectric constant	3.0 for 1 MHz	
Dielectric loss	0.03 for 1 MHz	
Breakdown voltage	13.6 kV	
Light transmission	46%	
Chemical resistance	Stable in weak acid and alkaline solution Stable in organic solvent	
Flammability	UL-94-VTM-0	

Data courtesy of Mitsubishi Plastic.

PET film (polyester film or polyethylene terephthalate) has been produced as a common film for general use, for the following reasons:

- It can provide a low-cost solution.
- It has excellent mechanical performance at room temperature.
- It has low moisture absorption and its dimensional stability is excellent.

Unfortunately, PET film cannot keep its high performance at higher temperatures than 70°C, and it is available for only nonsoldering applications. (Several soldering technologies have been developed for PET-based flexible circuits, but they are very specialized.) Also, PET films are flammable and it is difficult to achieve UL flame class certification. Not many available PET films can satisfy the flammability requirements of UL-94. Typical properties are shown in Table 65.18.

65.5.4 Other Materials Used for Flexible Circuits

Thin glass epoxy sheets less than 200 μm thick can be flexible and can be used as a base substrate of low-cost flexible circuits. Their physical properties are basically the same as those of rigid circuit boards, and standard manufacturing processes and assembling processes for rigid circuit boards are available for these materials. Standard soldering processes are applicable. But glass epoxy sheets do not have high flexibility, and they are not available for repeated flexing use. The basic properties of these materials are listed in Table 65.19.

TABLE 65.19 Properties of Thin Glass/Epoxy Substrate

Items	Risho Industrial		Matsushita Electric
	MD	TD	(R-5766 Series)
Tensile strength (kg/mm^2)	24.5	17.0	—
Elongation (%)	3.2	1.6	—
Thickness (μm)	120		50, 70, 100, 130, 150, 180, 200
Dimension change by heat (%)	−0.05		—
Dimension change by humidity (%)	0.03		—
Surface resistance (Ω)	1 × exp 12–13		5.2 × exp 14
Volume resistivity (Ω · cm)	1 × exp 12–13		
Dielectric constant	—		4.7
Dissipation factor (at 1 MHz)	—		0.015
Water absorption (%)	1.0		0.18
Breakdown voltage (kV/0.1 mm)	3.6		—
Bond strength (kg/cm)	—		1.39
Soldering resistance	—		260°C × 120 s
Flammability	—		UL-94-V-0

These materials are supplied as copper-clad laminates.

Fluorized carbon polymer films have been applied as a low-loss substrate material for flexible circuits. However, they do not have good dimensional stability or adhesion characteristics. High cost of the materials is the major reason that they cannot be standard in flexible circuits. In the last 20 years, several heat-resistant films, such as polypalabalic acid film and polysulfon film, have been

developed as alternative substrate materials in flexible circuits instead of polyimide films. Unfortunately, there was no successful material from a business standpoint. LCP films and PEEK have been considered as the new materials of high-speed flexible circuits based on the low dielectric constant and loss tangents.

65.6 CONDUCTOR MATERIALS

As flexible circuits have various mechanical stresses, their conductors also have requirements for more flexibility and toughness than traditional ED copper foils of standard rigid circuit boards. An RA copper foil is the solution for high flexing endurance. It is necessary for dynamic flexing use. RA copper foils are more expensive than ED copper, especially at thicknesses of less than 18 μm. Therefore, high-ductility electrodeposited (HD-ED) copper foils have been developed that have greater flexibility than ED copper foils and a lower cost than RA copper foils. The differences between the copper foils are shown in Table 65.20.

TABLE 65.20 Basic Properties of Copper Conductors

	ED Foil	HD-ED Foil	RA Foil
Manufacturer	Furukawa Electric	Furukawa Electric	Japan Energy
Grade	STD foil	HD foil	RA
Thickness (μm)	9, 12, 18, 35, 70	18, 35	12, 18, 35, 70
Tensile strength (kg/mm^2)	TD 34	TD 32	MD 21.5
			TD 18.9
Elongation (%)	TD 9	TD 23	MD 12.8
			TD 9.5
Surface roughness (μm)	8	10	<3.5
Cost	Low	Middle	High

Data measured for 35-μm thick foils.

Due to the stringent requirements of fine-line etching, thinner copper foils have been developed with small surface profiles. RA copper foil 12 μm thick is a standard product. Low-profile 12-μm-thick ED copper foils have also been commercialized for fine-line etching. A special treatment has been developed to ensure reliable bond strength with each adhesive material. In the next 5 years, these materials will be standard and utilized in large volume. RA copper foils thinner than 10 μm are available; however, processing and high material costs need to be addressed before large-volume production can commence.

Copper foils thinner than 5 μm will be demanded for the semi-additive process to generate 10-μm wide traces or finer since the beginning of 2000s. Two types of technologies have been developed to have ultrathin copper foils. The first one is the “etch-down” process used to reduce the copper

thickness from standard thick RA copper foils. Through this process, foils 3 to 5 μm thick can be obtained from 12-μm RA copper foils. The second is the use of ultrathin foils. ED copper foils 1 to 5 μm thick have been commercialized with the carrier copper foils. Ultrathin copper layers have been built on the smooth surface of other copper foils with standard thickness. The carrier copper foils are removed mechanically after the lamination with the base layers. Ultrathin copper foils have been applied to adhesiveless laminates through casting or lamination processes.

In addition, sputtering and plating technologies have achieved conductors thinner than 5 μm with semi-additive processes. Among others, these processes can generate copper, nickel, and gold conductors. Also, they can produce fine traces at less than 10 μm pitch on flexible substrates. Plating baths and chemicals have been developed for these technologies.

Special metal and alloy foils other than copper ones have been developed for specific applications.

Aluminum conductors have been developed as the low-cost solution. They have been applied for volume production of the keyboards of calculators, antennas of wireless devices, and so on. But they could not be universal conductor materials of standard flexible circuits because of difficulty in soldering and the special chemistries needed for etching. The wireless suspension of disk drives has consumed a large volume of special stainless steel and copper alloy foils because of the special mechanical performance of the circuits. A high-resolution printer head has also utilized thin tungsten foils as the conductor of thermal printer head circuits. Nickel-chromium alloy foils have been developed as the conductor materials of flexible heater circuits.

65.7 COPPER-CLAD LAMINATES

The majority of flexible circuit manufacturers start the process with copper-clad materials. The properties of these materials depend on the capabilities of laminate manufacturers, even though the same base films and copper foils are used. To choose the right materials, manufacturers must carefully consider the basic properties of each laminate material.

65.7.1 Adhesive-Based Laminates

Historically, copper-clad laminates with acrylic or epoxy adhesives have been the major materials for flexible circuits. Each manufacturer has developed a special resin grade or special additives to ensure reliable flexibility and bond strength. Other adhesive materials such as phenol resin or silicon resin have been developed; however, they have not become standard adhesive materials in flexible circuits.

The adhesive-based copper-clad laminates still represent more than 50 percent of the traditional flexible circuit market. The major properties of the materials are shown in Table 65.21. The manufacturing process is illustrated in Fig. 65.24. Mostly, these films are processed and supplied in roll form. The surfaces of polyester films and polyimide films undergo special processes such as sandblasting and plasma treatment to achieve a reliable bond strength. A specially blended adhesive resin is coated on the film and dried. Then a copper foil is laminated continuously under appropriate temperature and pressure. The surfaces of the copper foils receive a specific treatment according to the requirements of each laminate's manufacturer.

TABLE 65.21 Basic Properties of Adhesive-Based Copper-Clad Laminates (Polyimide-Based)

Items	Properties		
Manufacturer	DuPont	Nikkan	Shin-Etsu
Grade	Pyralux LF	Nikaflex	RAR Series
Adhesive layer	Acrylic	Epoxy	Epoxy
Peel strength (kgf/ccm)	1.4	1.3	1.8
Dimensional stability MD	−0.08	−0.09	−0.09
(%) TD	−0.07	+0.03	−0.04
Flexing endurance MD	N/A	3200	2650
(MIT, 2.0R) TD		2950	2850
Insulation resistance (Ω)	1.0 × exp 11	2.5 × exp 13	1.0 × exp 13
Surface resistivity (Ω)	1.0 × exp 13	2.7 × exp 14	1.0 × exp 14
Volume resistivity (cm)	1.0 × exp 14	2.0 × exp 16	1.0 × exp 16
Soldering resistance	288°C × 5 min	280°C × 10 s	280°C × 10 s
Flammability	No	UL-94-VTM-0	UL-94-VTM-0

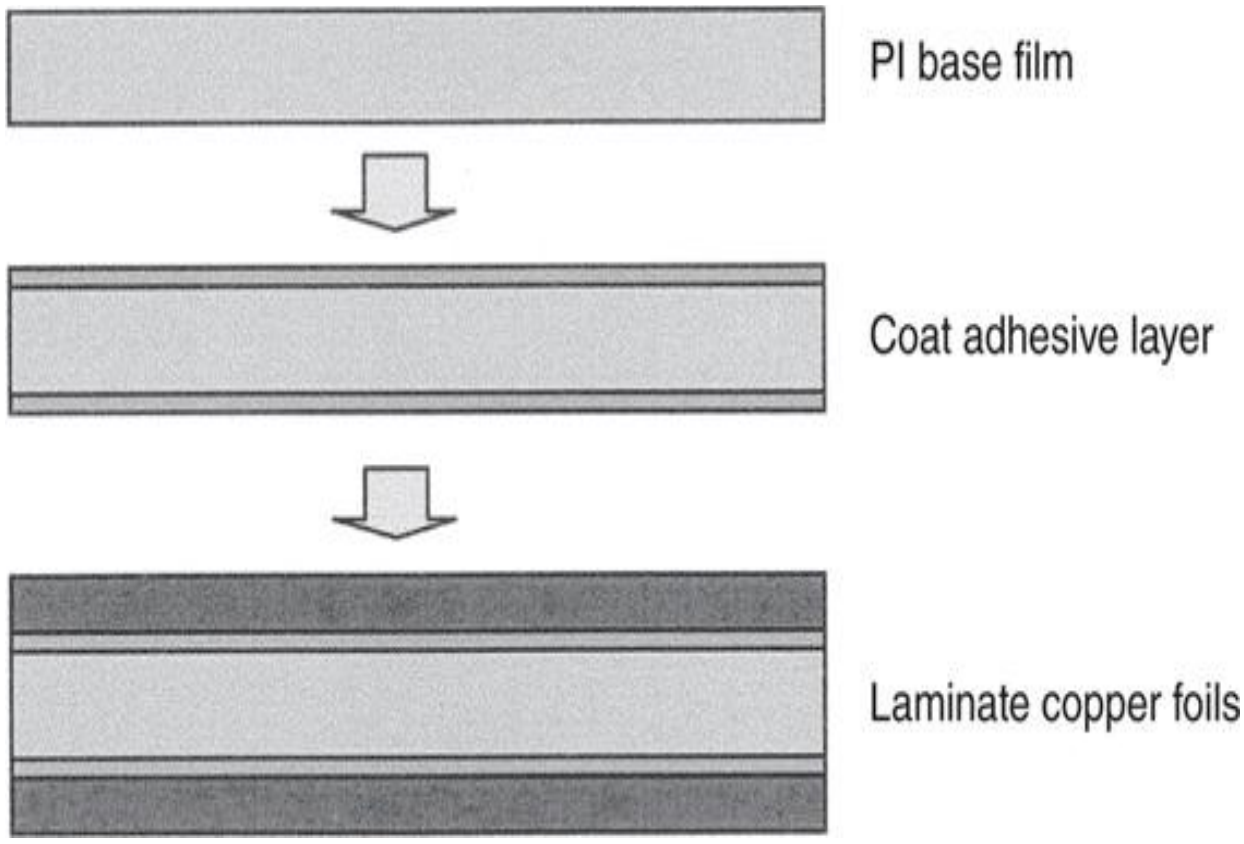

FIGURE 65.24 Manufacturing process for adhesive type laminate, showing a polyimide-based film combined with an adhesive layer coat and laminated to copper foils.

The same process is repeated for double-sided copper-clad laminates. (Some laminate manufacturers, however, have developed simplified manufacturing processes that can make the double-sided laminate in one single process to reduce manufacturing cost.) A well-conditioned aging process is important to achieving reliable bond strength and flexible characteristics of the laminates as the raw material of flexible circuits.

Most of the adhesive resins have lower heat resistances than polyimide films and are the bottleneck for high-temperature processing of flexible circuits (e.g., lead-free soldering and wirebonding).

The flame-retardant properties of the laminates depend on the composition of the adhesive materials used by each

manufacturer. Usually, a normal flame-retardant component in an adhesive resin has a negative effect on bonding. Several adhesive resins contain organic bromine molecules as the flame-retardant components, and will be eliminated for the ecological concerns. (For a discussion of this issue, see Chap. 6.) As soldering temperatures increase, heat-resistant adhesives or adhesiveless laminates systems are required.

65.7.2 Adhesiveless-Based Laminates

Several laminates without adhesive layers have been developed as the advanced materials for the next generation of flexible circuits. Lamination technology using epoxy resin or acrylic resin has been almost eliminated from HDI flexible circuits even though it uses new high-performance polyimide films as the substrates. Three types of adhesiveless copper-clad laminates have been developed (see Fig. 65.25):

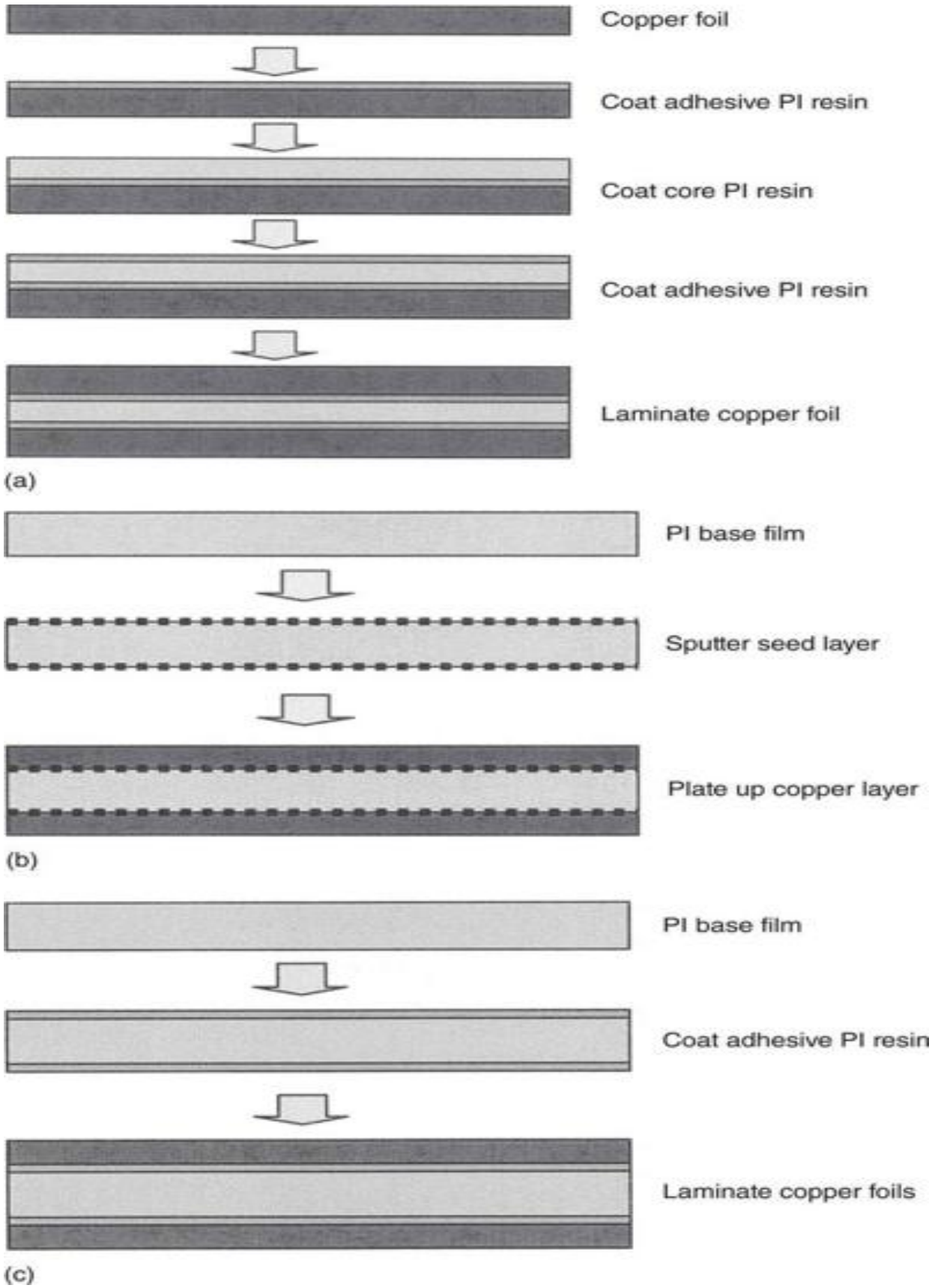
Copper foil
Coat adhesive PI resin
Coat core PI resin
Coat adhesive PI resin
Laminate copper foil
(a)
PI base film
Sputter seed layer
Plate up copper layer
(b)
PI base film
Coat adhesive PI resin
Laminate copper foils
(c)

FIGURE 65.25 (*a*) Manufacturing process of adhesiveless laminate using the cast process, (*b*) manufacturing process of adhesiveless laminate using plating process, (*c*) manufacturing process of adhesiveless laminate using lamination process.

- Cast
- Sputtering/plating
- Lamination

Each has different manufacturing processes and advantages as the major materials of HDI flexible circuits. Table 65.22 shows basic performances of typical adhesiveless laminate materials. Currently, there is no perfect solution that satisfies all requirements including cost. Suitable adhesiveless laminate materials should be chosen according to the specifications of the final flexible circuits and the convenience of manufacturing processes.

TABLE 65.22 Comparison of Adhesiveless Copper-Clad Laminates

Items	Sputtering/Plating Process	Cast Process	Lamination Process
Manufacturer	Gould Electronics	Nippon Steel Chemical	DuPont
Grade	GouldFlex	Espanex	Pyralux AP
Choice of dielectric	Wide	Small	Small
Base etchability	Fair	Difficult	Difficult
Dielectric thickness (μm)	12.5–125	12.5–50	12.5–150
Choice of conductors	Small	Wide	Wide
Conductor thickness (μm)	~35	12–70	12–70
Bond strength	1.2	1.5	1.4
Double-sided	Available	Available	Available
Flexing endurance	N/A	180 (MIT 0.8R)	N/A
Dimensional change after etching	MD: −0.05%	MD: −0.02%	MD: −0.05%
	TD: 0.03%	TD: −0.02%	TD: −0.05%
Insulation resistance (Ω)	>1 × exp 10	>1 × exp 13	>1 × exp 14
Volume resistivity (Ω-cm)	>1 × exp 14	>1 × exp 15	>1 × exp 17
Flammability	UL-94-VTM-0	UL-94-VTM-0	UL-94-VTM-0
Roll clad	Standard	Standard	Not available

65.7.2.1 Cast-Type Adhesiveless Laminates. The cast-type adhesiveless laminates have a good cost/performance balance. They have a high bond strength between substrate layers and conductor foils. They can also use special conductors such as copper alloy, nickel, stainless steel, etc. In addition, they have good flexibility to generate

very thin substrate layers down to 12 µm thick. They can have a wide range of copper thicknesses because of the process. There is no difficulty in making 70- or 105-µm copper laminates. Because it has been around longer, the cast-type laminate has a relatively broader availability than other adhesiveless laminates. The process can produce both single-sided and double-sided laminates.

The liquid polyimide resins are coated on a metal foil, directly controlling mechanical stress on the materials. Air-floating conveyors have been employed to reduce the stress. A thermal treatment process is the key to ensuring good physical performance of the laminates. Generally, two or more polyimide layers are coated on the metal foil to ensure both good dimensional stability and high bond strength. Usually, it is difficult to apply the chemical etching process to adhesive polyimide resins using standard alkaline solutions.

Producing double-side laminates through casting requires a special process because the chemical imidation reaction generates a lot of moisture and results in delamination during the lamination process. One special process is to coat hot-melt-type polyimide on the top of the substrate layer, and another is to laminate another copper foil at high temperature and pressure. Physical performance varies depending on the combination of the polyimide resins and lamination conditions. Usually, higher temperatures than 300°C are required.

65.7.2.2 Sputtering/Plating-Type Adhesiveless Laminates. A two-step process is required to produce sputtering/plating-type adhesiveless laminates. The first step is a kind of sputtering process to produce seed layers on substrate films. The seed layers have two functions: to generate conductive layers on the nonconductive plastic films, and to increase the bonding strength between base films and conductor layers. Generally, the sputtered layers are thinner than 100 nm. Therefore, the second step builds

the thick conductor layers by electrical plating. To produce double-sided laminates, the process is usually repeated twice.

Sputtering/plating-type adhesiveless laminates can generate the thin conductors required for high-density circuits. Theoretically, these laminates provide stable conductor layers thinner than 10 μm at low cost. Technically, it is very possible to have 0.1- to 1.0-μm-thick conductors. Although plating-type laminates provide more substrate material choices, their basic physical properties depend heavily on substrates. The majority of manufacturers introduced the sputtering process to generate a seed layer for good bond strength between the substrate and the conductor. Two or three steps of sputtering processes with nickel, chromium, and their alloys are employed to strike a good balance of chemical, physical, and electrical performance. Sometimes seed layers cannot be etched.

Few choices are available for conductor materials. Thick conductors are not optimal because they require a longer plating process. Micron-size pinholes in the conductor layer are the biggest issue with this material. Several manufacturers have introduced additional chemical processes to eliminate these pinholes. Generally, the bond strength of the laminate is lower than that of other types.

65.7.2.3 Lamination-Type Adhesiveless Laminates.

Thermoplastic-type polyimide resins with high-temperature melting points have been developed to serve as the hot-melt adhesives between copper foils and dimensionally stable polyimide films. The adhesiveless flexible laminates are produced by a heat lamination of the copper foils and base polyimide films that have thin hot-melt polyimide layers coated on the surface of the core polyimide films. The polyimide films, with hot-melt polyimide layers, are supplied by the major polyimide film suppliers. Temperatures higher than 330°C are required to produce

reliable laminates. Materials processed at temperatures lower than 200°C are available for several hot-melt polyimide resins; however, their physical properties are inferior to those of standard laminates.

Producing double-sided laminates is not tremendously difficult. A conventional vacuum heat press with a higher processing temperature than 350°C is available to produce the laminate for small-volume production. A high-temperature roll laminator or belt laminator is used for high volume production.

Lamination-type adhesiveless laminates have advantages in small-volume production. Special polyimide films that have hot-melt polyimide resin on the surface of dimensionally stable polyimide film are available commercially. If a manufacturer has high-temperature heat press equipment, it is not difficult to produce the laminates. A compact roll-type heat laminator was developed to produce the rolled laminates.

Many choices of conductor materials are available for lamination-type adhesiveless laminates. Due to the special combination of conductor materials with stainless steel and copper alloy foils, this material has a variety of uses in multilayer rigid/flexible aerospace applications and in wireless suspension of disk drives. Generally, the adhesive polyimide is difficult to etch using standard alkaline etching solutions, so strong chemistry or a physical process such as plasma etching is required for the process.

Figure 65.26 shows the thickness ranges available for the substrates and conductors for each type material. All of the laminates have expanded their capabilities, and several thicknesses are overlapped. Therefore, circuit manufacturers have more choices for specific thicknesses and can consider other performance variables, including cost.

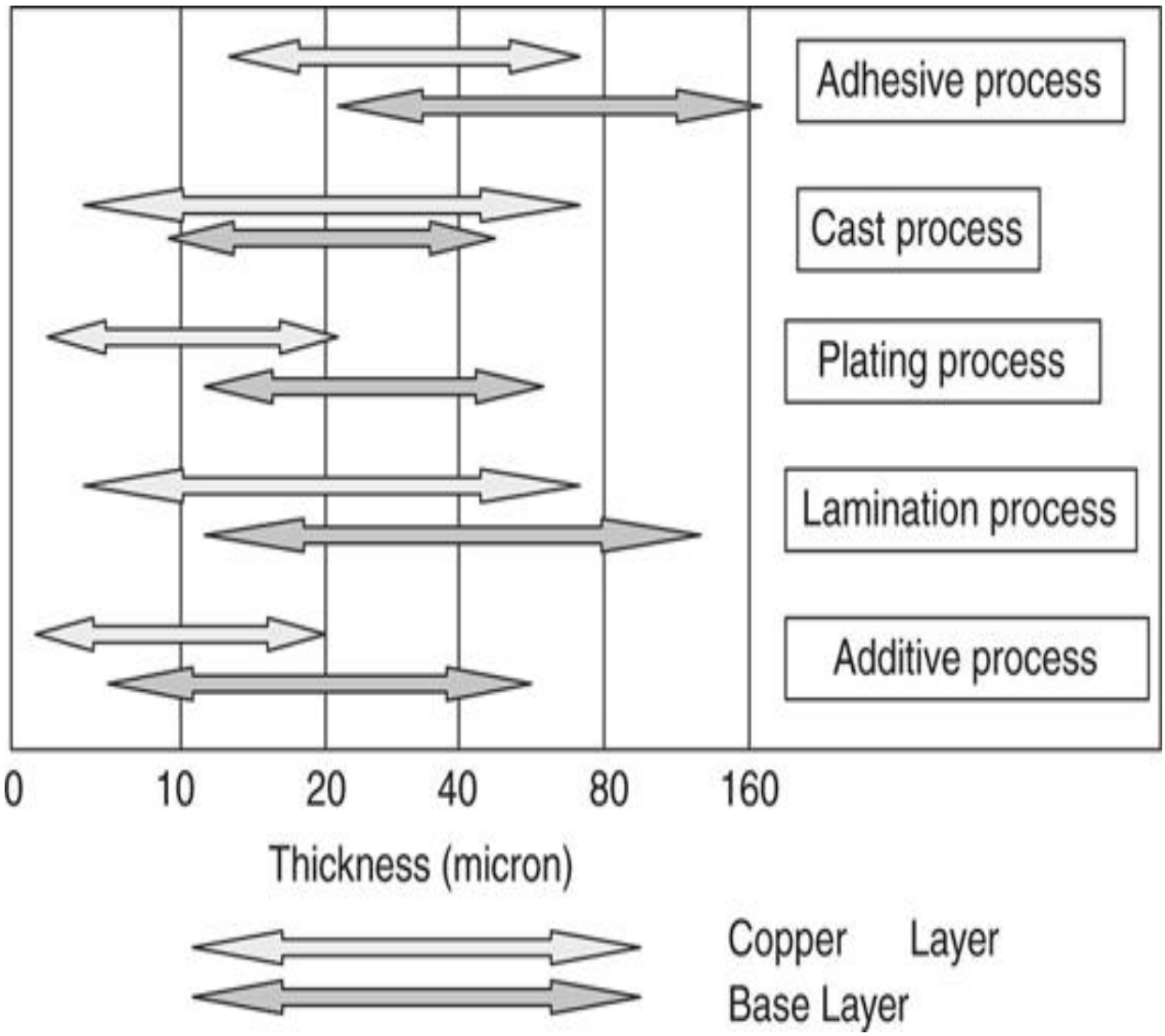

FIGURE 65.26 Thickness range of the copper-clad laminates.

65.8 COVERLAY MATERIALS

One of the major differences between flexible circuits and rigid circuit boards is coverlay. In addition to the solder mask used for assembly, coverlay is the mechanical protector for the fragile conductors on flexible circuits. Film-based coverlay and flexible solder mask have been standard materials for traditional flexible circuits. Several types of photoimageable coverlay materials have been developed to

satisfy the fine-resolution requirements of HDI flexible circuits:

- Film coverlay
- Screen-printable coverlay (flexible soldermask)
- Photoimageable coverlay (dry-film type and liquid type)

Several types of the materials are available for each coverlay type.

65.8.1 Film Coverlay

Usually the same films are chosen for the coverlay films as are used for the substrate layers. The films are coated with semicured acrylic or epoxy resin, which is used as an adhesive layer. The surfaces of the adhesive layers are covered with release films when the materials are delivered to circuit manufacturers. Semicured adhesive resins are unstable at room temperature, so film coverlay must be kept in refrigerators. The adhesive resins of the coverlay usually have only weeks of pot life even when they are kept in low-temperature environments, and exact conditioning is required for processing.

The process of manufacturing with film coverlay is very complicated, which makes process automation difficult and increases the cost. The manual registration process and the use of unstable film material are major issues when considering film coverlay for HDI flexible circuits due to small hole capability and lower dimensional accuracy. Basic properties of the typical materials are shown in Table 65.23.

TABLE 65.23 Basic Properties of Film Coverlay (Polyimide Film Base)

Manufacturer	DuPont	Nikkan Industry
Grade	Pyralux LF	CISV
Adhesive	Acrylic	Epoxy
Lamination temperature	180°C	160°C
Storage condition	Room temperature	Refrigerator
Bond strength (kg/cm)	1.3	1.0
Surface resistivity (Ω)	1.0 × exp 13	3.0 × exp 14
Volume resistivity (Ω-cm)	1.0 × exp 14	1.2 × exp 16
Soldering resistance	288°C × 5 min	280°C × 10 s
Flammability	No	UL-94-V-0

65.8.2 Screen-Printable Coverlay Ink (Flexible Solder Mask)

A screen-printing process similar to that used for rigid circuit boards is available for flexible circuits as the low-cost coverlay process. However, specially conditioned liquid solder mask materials are required to produce appropriate flexibility for the circuits. Standard solder mask materials designed for the rigid boards have small cracks and delaminations when bending. Basic properties of the typical materials are shown in Table 65.24.

TABLE 65.24 Basic Properties of Screen-Printable Coverlay

Manufacturer	Taiyo Ink	Nippon Polytech
Grade	S-222	NPR-5
Base resin	Epoxy	Epoxy
Color	Green	Green
Hardness	5H	H
Peel strength	100/100 (crosshatch)	100/100 (crosshatch)
Flexibility	N/A	0.5 mm diameter
Soldering resistance	260°C × 20 s	260°C × 20 s
Insulation resistance (Ω)	>1 × exp 13	>1 × exp 12
Flammability	UL-94-V-0	UL-94-V-0

Generally, because of poor resolution, a screen-printing process does not satisfy the requirements of high-density SMT assembling on flexible circuits. Also, such as process does not provide good mechanical performance for dynamic flexing. Typical property examples are shown in Table 65.25.

TABLE 65.25 Detailed Characteristics of Various Insulations

	TPE Plastic	TPE Glass Cloth	FEP Plastic	FEP Glass Cloth	Kapton Polyimide Film	CTFE	Epoxy Ducron	Poly Propylene	Mylar Polyester Film	Polyvinyl Chloride	Polyethylene
Spec. gr. flammable	2.15 NO	2.2 NO	2.15 NO	2.2 NO	1.42 Self-test	2.10 NO	1.38 YES	0.905 Slow-burning	1.395 YES	1.25 Self-test	0.93 YES
Appearance	Translucent	Tan	Clear bluish	Tan	Amber	White and opaque	Translucent	Clear	Clear	Translucent	Clear
Bondability with adhesives	Good*	Good*	Good*	Good*	Good	Good*	Good*	Poor	Good	Good	Poor
Bondability to itself	Good	Good	Poor	Good	Poor	Good	Good	Good	Poor	Good	Good
Chemical resistance	Exc.	Exc.	Exc.	Exc.	Exc.	Exc.	Good	Good	Exc.	Good	Good
Sunlight resistance	Exc.	Exc.	Exc.	Exc.	Exc.	Exc.	Fair	Low	Fair	Fair	Low
Water absorption, %	<0.01/24 h	0.10/0.68†	<0.01/24 h	0.18/0.30†	3.0/24 h	0	1.5	0.01	0.8/24 h	0.10	0.01/24 h
Volume resistivity, Ω-cm	$>10^{17}$	$>10^{15}$	$>10^{17}$	$>10^{15}$	$>10^{17}$	$>10^{15}$	$>10^{15}$	$>10^{17}$	$>10^{18}$	$>10^{13}$	$>10^{15}$
Dielectric constant, -10^6 Hz	2.2	2.5/5†	2.1	2.5/5†	3.5	2.5	—	2.0	2.8–3.7	3.6–4.0	2.2
Dissipation factor, -10^6 Hz	2×10^{-4}	7×10^{-4} 10^{-3}†	2×10^{-4}	10^{-4} 10^{-3}†	3×10^{-3} 14×10^{-3}	15×10^{-3}	70×10^{-3}	2×10^{-4} 3×10^{-4}	2×10^{-3} 16×10^{-3}	14×10^{-2}	6×10^{-4}
Service temp.											
Min, °C	−200	−70	−200	−70	−200	−70	−20	−55	−60	−30	−20
Max, °C	250	250	200	200	300	125	100	100	105	85	60
Tensile str.											
psi @25°C	3000	20,000†	3000	20,000†	25,000	4500	3000	5700	20,000	3000	2000
$N/M^2\times10^6$ @25°C	0.2067	1.378	0.2067	1.378	1.697	0.31	0.8825	0.3927	1.378	0.2067	0.1378
Modulus of elasticity											
Psi	58,000	4.01	50,000	4.01	510,000	190,000	12,000	170,000	550,000		50,000
$N/M^2\times10^6$	3.930	0.0003	3.934	0.0003	34.623	12.90	3.930	11.713	37.895		3.445
Thermal expansion	(−30 to 30°C)		(−30 to 30°C)		(−14 to 38°C)	(−195 to 90°C)	(−30 to 30°C)	(−30 to 30°C)	(21 to 50°C)		(−30 to 30°C)
In/(in)(°F) $\times10^{-6}$	55	low†	50	low†	11	48	11	61	15		100
cm/(cm)(°C) $\times10^{-6}$	100		90		20	82	20	110	27		180
Dielectric strength											
V/in $\times10^{-3}$	600	650 1600†	2800	650 1600†	7000	1100	900	650	700	800‡	585
Sample size,in	0.015	0.003	0.005	0.003	0.002	0.0192		0.125	0.001		0.125

*Must be treated.
†Depends on % glass cloth.
‡Depends on formulation (plasticizer).

65.8.3 Dry-Film–Type Photoimageable Coverlay

The basic idea of the photoimageable coverlay is to satisfy both of fine resolutions of the opening and physical flexibility by one single material. Also, its simple manufacturing process should reduce costs.

From a processing standpoint, there are two types of PIC materials: dry film and liquid. The dry-film type is easily processed when manufactured with vacuum laminators, which provide good encapsulation with the fine conductors. A vacuum press is also available for a small-volume production. However, the cost per unit area is higher for the dry-film type than for liquid materials.

Dry-film–type and liquid ink–type photoimageable coverlay materials have been developed with different resin matrixes to satisfy different technical requirements of HDI flexible circuits. A comparison of the materials is given in Table 65.26. Properties of the materials are shown in Tables 65.27 and 65.28.

TABLE 65.26 Comparison of Photoimageable Coverlay Materials

	Dry Film Type		Liquid Ink Type	
	Acrylic-Base/Epoxy-Base	Polyimide-Base	Epoxy-Base	Polyimide-Base
Applicator	Vacuum laminator	Roll laminator	Screen print Spray coat Curtain coat	Screen print Spray coat Roll coat
Thickness range (μm)	25–50	25–50	10–25	10–20
Minimum opening (μm)	70	70	70	50
Flexibility	*	Good	*	Good
Heat resistance	Acceptable	Excellent	Acceptable	Good
Electrical properties	*	Good	*	*
Chemical properties	Acceptable	Good	Good	Excellent
Handling	Easy	Difficult	Fair	Difficult
Technical hurdle	Low	High	High	Very high
Storage condition	Refrigerator	Room temperature	Refrigerator	Freezer
Quick turn	Easy	Easy	Slow	Slow
Material cost	Medium	High	Low	High
Process cost	Medium	High	Low	Low

*Depends on manufacturer.

TABLE 65.27 Properties of Liquid/Epoxy-Type Photoimageable Coverlay

Manufacturer	PolyTech	Coates	Asahi	Peters
Grade	NPR-80	Image Flex	Focus Coat	Elpemer
Pencil hardness	5H	H, HB	4H	6H
Bond strength on copper	100/100	100/100	100/100	100/100
Flexibility	MIT test 0.5 mm R > 500 times	1-mm mandrel: pass	180° bend: pass	3-mm mandrel: pass
Insulation resistance (Ω)	2 × exp 12 (IPC)	5 × exp 11 (IPC)	6 × exp 13 (JIS)	2 × exp 14 (VDE)
Volume resistance (Ω-cm)	–	–	5 × exp 14	1 × exp 15
Dielectric strength	28 kV/mm	91 kV/mm	(2.1 kV/0.16 mm)	88 kV/mm
Soldering resistance	260°C × 10 s	260°C × 10 s	260°C × 1 min	288°C × 20 s
Flammability	UL-94-V-0	UL-94-VTM-0	N/A	UL-94-V-0
Resistance in Ni/Au plating	Pass	Pass	Pass	Pass
Exposure intensity (mJ/cm^2)	150	400	300	150
Developer	Sodium carbonate	Sodium carbonate	Sodium carbonate	Sodium carbonate

TABLE 65.28 Properties of Different Photoimageable Coverlay Materials

	DuPont	NSCC	Nitto Denko	Toray
	Puralux PC	Espanex SFP	JR-3000	Photoneece
Material	Acrylic/dry film	Polyimide/dry film	Polyimide/liquid ink	Polyimide/liquid ink
Pencil hardness	3H	–	–	–
Tensile strength (MPa)	N/A	226	120	148
Elongation	>55%	–	11%	36%
CTE (ppm/K)	130	23	35	16.1
Bond strength on copper	100/100	0.8 kg/cm	100/100	100/100
Flexibility	MIT 0.38R	MIT 0.38R	N/A	N/A
	100 times	1200 times		
Surface resistance (Ω)	>1.0 × exp 12	>1.0 × exp 13	–	>1.0 × exp 16
Volume resistance (Ω-cm)	3.4 × exp 16	1.0 × exp 16	5 × exp 15	>1.0 × exp 16
Dielectric strength (kV/mm)	>80	–	240	>300
Dielectric constant	3.5–3.6	3.5	3.3	3.2
Loss tangent	0.03	0.007	0.6	0.002
Soldering resistance	260°C × 10 s	350°C (JIS)	>300°C	>300°C
Flammability	UL-94	UL-94-VTM-0	Self-distinguishable	Self-distinguishable
Resistance in Ni/Au plating	Pass	Pass	Pass	Pass
Exposure intensity (mJ/cm^2)	200	400	500	150
Developer	Sodium carbonate	Lactic acid solution	Alkaline solution	Special chemical

The materials were developed assuming different applications; therefore, measured data are not exactly equivalent.

65.8.3.1 Acrylic or Epoxy/Dry-Film Type. Acrylic or epoxy/dry-film types were the first materials developed to act as the flexible photoimageable coverlay for HDI flexible circuits. They have the same product concept as the photoimageable solder mask of rigid circuit boards. The same vacuum laminators and imaging equipment are available for these materials.

Managing the conditioning of the process is not difficult. Acrylic or epoxy/dry-film types are good for small-volume production because of the flexible manufacturing process. They may need some more improvements in electrical performance and chemical resistance if they are to be used in the general application of high-density flexible circuits. The present version of the materials, however, yields a good balance of performances for both high-density soldering and flexing endurance.

65.8.3.2 Polyimide/Dry-Film Type. The physical performance of the polyimide/dry-film type is excellent. When applied to polyimide-based adhesiveless laminates, it provides very high heat resistance and good dimensional stability. Also, it has high electrical properties. It has been applied in high-density wiring of interconnection in the head suspension of disk drives. The major issues with this material are the complicated pattern-generation process and high material cost. It requires multiple chemical processes using special chemical solutions. A high-temperature baking of over 250°C is another difficulty. This is required to complete the standard manufacturing process of flexible circuits.

65.8.4 Liquid-Based Photoimageable Coverlay

Eventually, photoimageable coverlay could be the practical solution for HDI flexible circuits in large-volume production. It

is similar to the solder mask of rigid circuit boards; however, the materials for flexible circuits must have high flexibility. None of the materials developed as solder masks for rigid boards are available for flexible circuits, even though dynamic flexing is not required. The liquid PIC requires special coating equipment such as a screen printer or sprayer. It can, however, provide a low-cost coverlay for large-volume production.

65.8.4.1 Epoxy/Liquid Ink. This material combination has been providing the best cost/performance combination for large-volume applications. Many manufacturers have tried to develop a good photoimageable coverlay with this combination, and Table 65.29 shows several successful examples. They provide good performance balances in mechanical, electrical, and chemical properties. A specialty is that these materials yield higher flexibility, without serious curling during the thermal processing, than other materials offer.

TABLE 65.29 Comparison of Stiffener Materials

	Paper/Phenol	Glass Epoxy	Polyimide	Polyester	Metal
Thickness range (μm)	500–2500	100–2000	25–125	25–250	Very wide
Soldering	Possible	Possible	Possible	No	Possible
Adhesion by thermoset resin	No	Possible	Possible	No	Possible
Cost	Low	High	Medium	Low	Medium

These materials are available by screen printing, spray coating, and other coating methods. UL-certified grades are available for commercial use. The flexibility of the materials allows several cycles of bending; however, the materials are

not available for the long-term flexing that applications such as hard disk drives and printers require.

65.8.4.2 Polyimide/Liquid Ink. This material concept was generated as the reliable thin dielectric layer of flexible circuits for both substrates and coverlay. Polyimide/liquid ink is highly reliable for a wide range of thicknesses. A 10-μm-thick layer could have sufficient performance to be a coverlay of a high-density flexible circuit. An appropriate combination with an adhesiveless copper laminate allows long-term dynamic flexing. The major issues are short pot life and high cost. Some of the ink materials must be stored at a temperature lower than 0°C. The materials require severe process conditions, especially for the final curing, where they require a temperature higher than 300°C. The cost of polyimide-based photoimageable materials is 5 to 10 times higher than for epoxy-based materials.

65.9 STIFFENER MATERIALS

All kinds of sheet or board material could be used as stiffener materials for the flexible circuits; however, several materials are commonly used. Typical stiffener materials for the traditional flexible circuits are listed in Table 65.29. Paper phenol boards and glass epoxy boards are employed for relatively thick requirements. Polyimide films and polyester films are employed for relatively thin requirements. Aluminum plates and stainless steel plates are commonly used as the stiffener materials of flexible circuits. A specialty of the metal stiffeners is their forming capabilities after they are bonded on flexible circuits. Paper phenol and polyester are not available for thermo-setting adhesives because of the low heat resistance.

65.10 ADHESIVE MATERIALS

Several different types of adhesive materials can be used in flexible circuits depending on the application, except for the adhesive layer of copper laminates and film coverlays. The major applications are the bonding of stiffeners and multilayer constructions.

Table 65.30 compares the materials. Pressure-sensitive adhesives (PSAs) provide a low-cost solution due to their simple application process. A problem of PSA is creep characteristics under mechanical stress, as PSA cannot maintain the exact positions of the stiffener boards under the stress. Thermosetting adhesives provide a reliable bonding between the layers, but they require a long processing time in a heat press with suitable press pad materials and impose a higher processing cost.

TABLE 65.30 Comparison of Adhesive Materials for Flexible Circuits

	Thermosetting Epoxy and Acrylic Resin	Hot-Melt-Type Polyimide Resin	Pressure-Sensitive Adhesives (PSAs)
Reliability	High	High	Acceptable
Bond strength	High	High	Acceptable
Creep	Small	Small	Large
Soldering	OK	OK	OK
Application process	Complicated	Complicated	Simple
Process temperature	160–180°C	>330°C	Room temperature
Material cost	Low	High	Low
Total cost	High	Very high	Low

Usually, the adhesive materials are supplied on or between separation sheets by rolled form. They should be kept in the refrigerators. The mechanical pretreatments are conducted with the separation sheets.

65.11 RESTRICTION OF HAZARDOUS SUBSTANCE ISSUES

Two issues have arisen regarding restriction of hazardous substance issue (RoHS) requirements for the flexible circuit materials: flame-retardant molecules with bromine in adhesive resins, and heat resistance for high-temperature processing with lead-free soldering. Although the issue of bromine is not actually a part of the RoHS requirement, it has been linked to the general environmental issues of printed circuit materials and processes.

Adhesiveless copper laminates can be the solution for the both of these problems because they do not use adhesive layers and have much higher heat resistance than adhesive-based laminates. However, because some of the applications need adhesive-based copper laminates, manufacturers of flexible laminates have been developing alternative materials without bromine-based flame-retardant reagents.

There have been technical barriers to developing new materials with a good balance of performances for coverlay eliminating bromine compounds. Film coverlay have to have an adhesive layer with some flame-retardant reagent. Few new epoxy resins have good balance for all of the physical performances without bromine compounds.

New materials of photoimageable coverlay have been developed without bromine molecules. Not many choices offer a balanced performance, especially high flexibilities for dynamic flexing. Polyimide-based photoimageable coverlays are the solution to satisfy the all of the physical

requirements, but these polyimide materials are remarkably more expensive.

65.12 ACKNOWLEDGMENTS

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CHAPTER 66
DESIGN OF FLEXIBLE CIRCUITS

Happy T. Holden
Co-Editor-in-Chief, Printed Circuits Handbook, *and PCB Technologist, Zeeland, Michigan*

66.1 INTRODUCTION

Because of the broad wiring capabilities now available, it is possible to cover all 3D wiring of an electronic product by one flex circuit, or by a set of multilayer rigid/flex circuits, without the need for connectors, extra cables, and soldering. However, to achieve this, the shape of the flex circuit may be very complicated and the size may be large. As a result, the final cost could be extremely high. If so, the use of flexible circuits is not an acceptable solution, especially for large-volume consumer applications. It may be better to divide the wiring into two or more parts to make each circuit simpler. A combination of simple circuits can be less expensive than one flex circuit, even though it mandates several connections between different circuits. A circuit designer should also consider the manufacturing convenience of flex circuits. There are serious differences among rigid circuit

boards. A small design modification can sometimes reduce the total cost significantly.

66.1.1 Design Procedure

To achieve the best cost-performance combination for a wiring design with flex circuits, an appropriate design procedure is recommended, as illustrated in Fig. 66.1. The steps in the process are as follows:

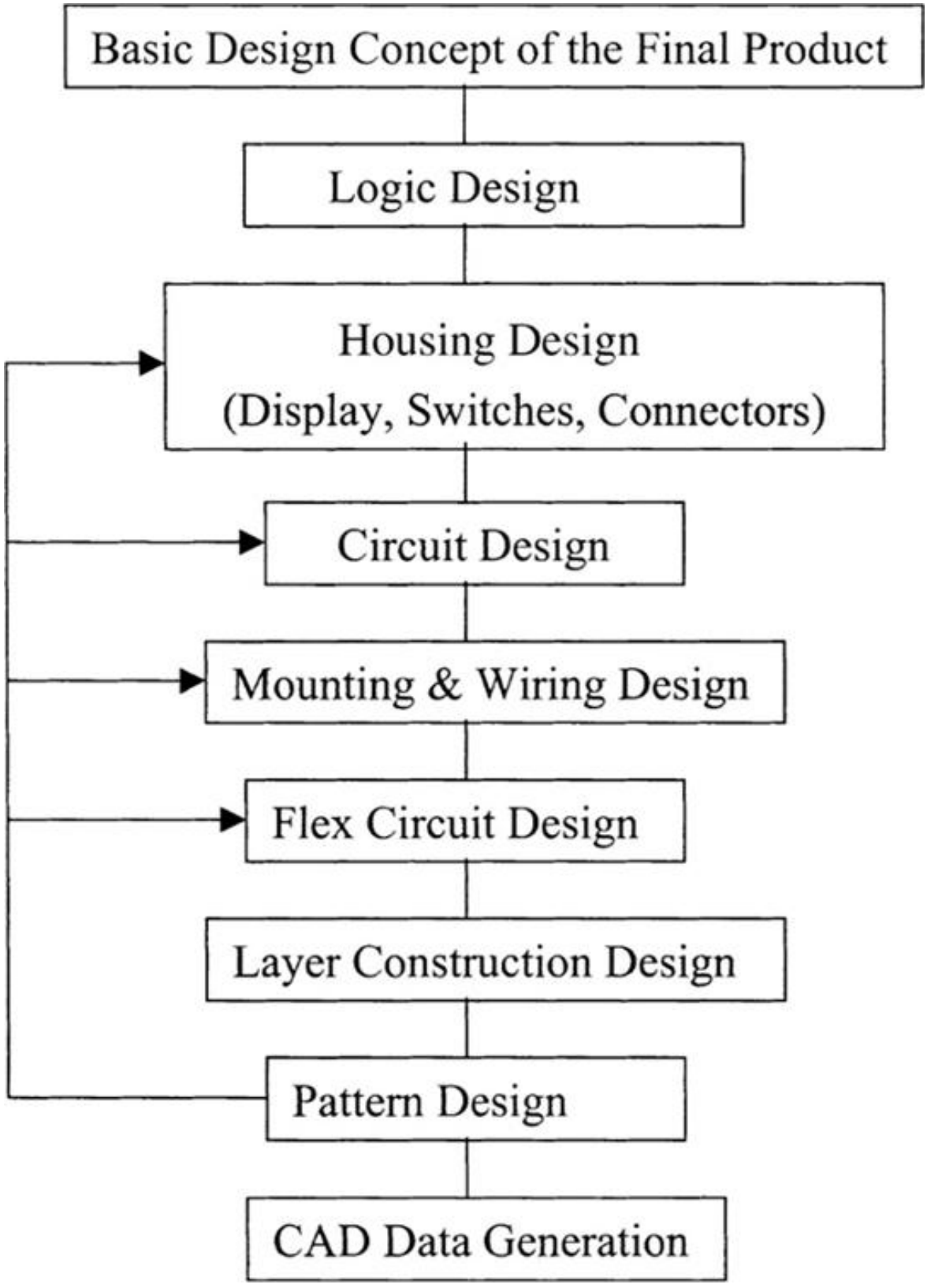


FIGURE 66.1 Design procedure for flexible circuits.

- A design concept for an electronic product is determined according to the basic specifications for the final product.
- A logical circuit design and electronic circuit design are formulated.
- A design for the equipment housing is made according to the final product concept. (This should sometimes be done independently in the case of consumer applications, especially for portable electronic products.)
- The circuit design is formulated. Appropriate circuit selection is conducted depending on total conditions such as allowed space, sizes of components, operating temperature, possible assembling process, required reliability, and so on.

A flex circuit or a combination with a flex circuit is considered to be the solution for a small wiring space.

- If the first circuit design does not satisfy the original specifications, the previous design steps are repeated to solve the conflicts.
- A suitable value analysis is done to minimize the total wiring cost.
- Conductor trace patterns and coverlay opening patterns are designed to minimize the mechanical stress.
- Numerical data for photo plotter, NC drilling, punching dies, and other tooling is generated.

66.2 TYPES OF FLEXIBLE CIRCUITS

Flexible circuits allow for more variety in their basic structures and supplemental structures than do rigid circuit boards, as shown in Table 66.1. Flexible circuits have single- or double-side constructions with through holes similar to rigid boards. However, multilayer construction has significant

differences from rigid boards; this is because the flexibility of the composite board will be very low when the circuit has more than two conductor layers. Therefore, the flexing parts of the circuit have to have special layer constructions to keep flexibility. The construction is called rigid/flex when the rigid part includes rigid board materials such as glass/epoxy. A simple single- or double-side flexible circuit is mechanically fragile, so coverlay and stiffener boards are generally added as the supplemental structures of the flexible circuits. Further special constructions, such as flying leads and dimples, are used for specific applications.

TABLE 66.1 Construction Types of Flex Circuits

Classification	Structure Types
Basic structure includes	• Single-sided flexible circuits
	• Double-sided flexible circuits with or without through holes
	• Multilayer flexible circuits with through holes
	• Multilayer rigid/flexible circuits with through holes
	• Blind via holes, inner via holes
	• Flying-lead structure
Supplemental structure includes	• Coverlay structure
	• Stiffener structure
	• Dimple structure
	• Microbump structure

An appropriate combination of a basic structure and supplemental structures should be chosen according to the requirements of the application. Also, appropriate termination technologies and suitable circuit constructions must be considered together.

66.2.1 HDI Flexible Circuits

There are significant differences in design, materials, and manufacturing technologies between traditional flexible circuits and new high-density flexible circuits developed for high-density interconnect (HDI). Figure 66.2 shows one way of defining the areas of high-density flexible circuits by using the technical hurdles of manufacturing for both trace densities and via hole sizes. Advanced etching technology is needed to give the high-density flexible circuits fine traces. Also needed are new micro via hole generation technologies other than traditional mechanical drilling, such as laser, plasma, and chemical etching.

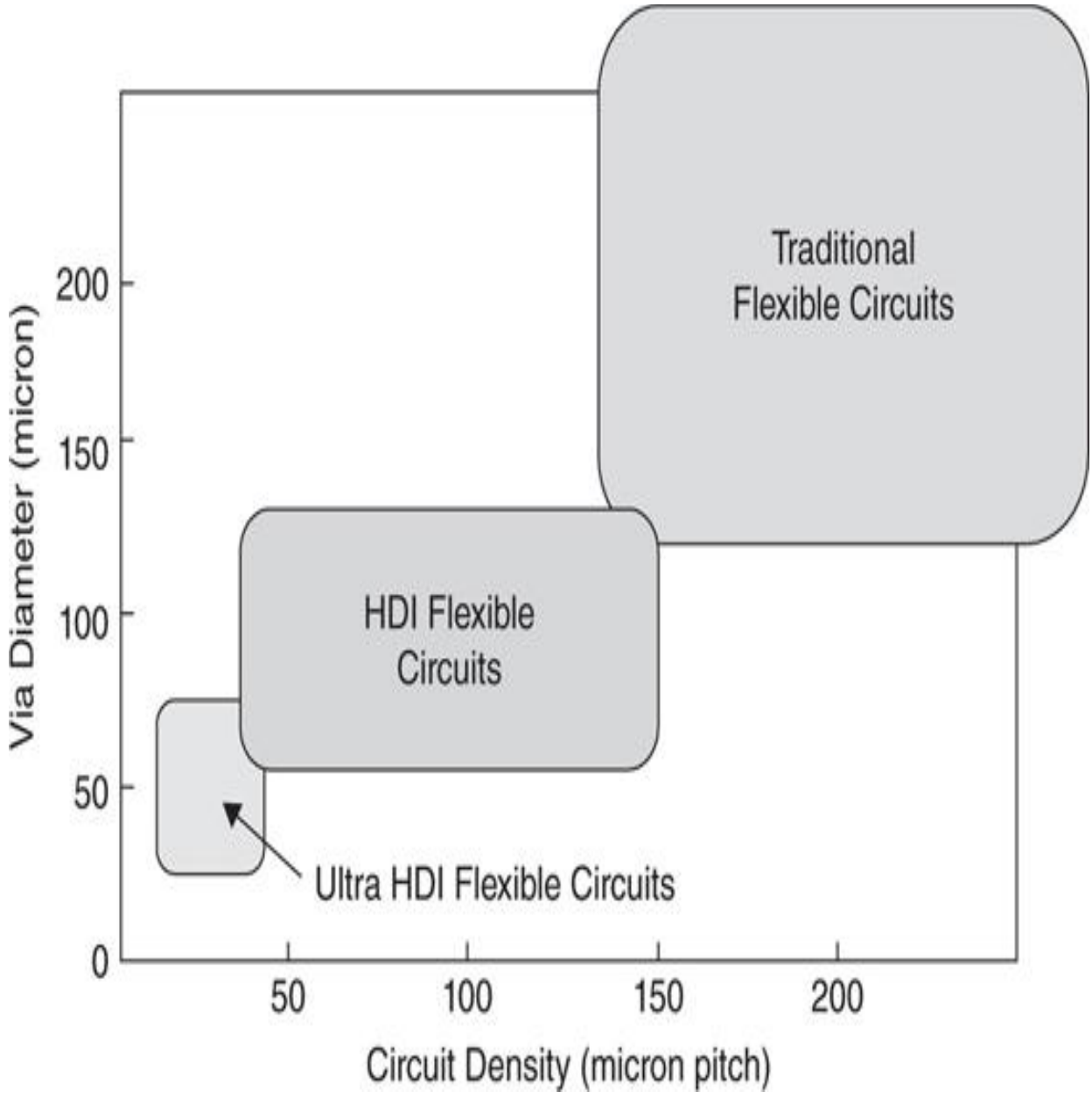


FIGURE 66.2 Definition of HDI flexible circuits.

Ultrahigh-density flexible circuits have been developed for special applications. They have extremely fine circuits that are smaller than 20 μm in pitch, as well as micro via hole connections smaller than 25 μm in diameter. Product concepts for ultrahigh-density flexible circuits are very different from those for traditional flexible circuits in construction and manufacturing technologies. They need

completely new concepts for the manufacturing processes, such as an additive process with new materials and new equipment. (See Chaps. 25 and 26 for detailed discussions of HDI design and fabrication.)

New high-density flexible circuits have supplemental structures such as flying leads and microbump arrays to complete high-density terminations. As volume production is limited, the designers should consider the manufacturers' process capabilities seriously.

66.2.2 Single-Sided Circuits

A bare single-sided flex circuit has a construction very similar to those of the single-sided rigid circuit boards, except for the thickness of the substrate layers. On the other hand, the protection of the conductors of the flexible circuits is very different from the rigid boards. A film coverlay system is introduced for the flexible circuits instead of solder masks (see Fig. 66.3). As introduced in Chap. 61, there are several choices of substrate (see Table 66.2). A 25-μm-thick polyimide film substrate is the most common material for consumer applications, with large volume due to its low cost. For higher reliability thicker film should be chosen, while for lower reliability, a thinner film can be used.

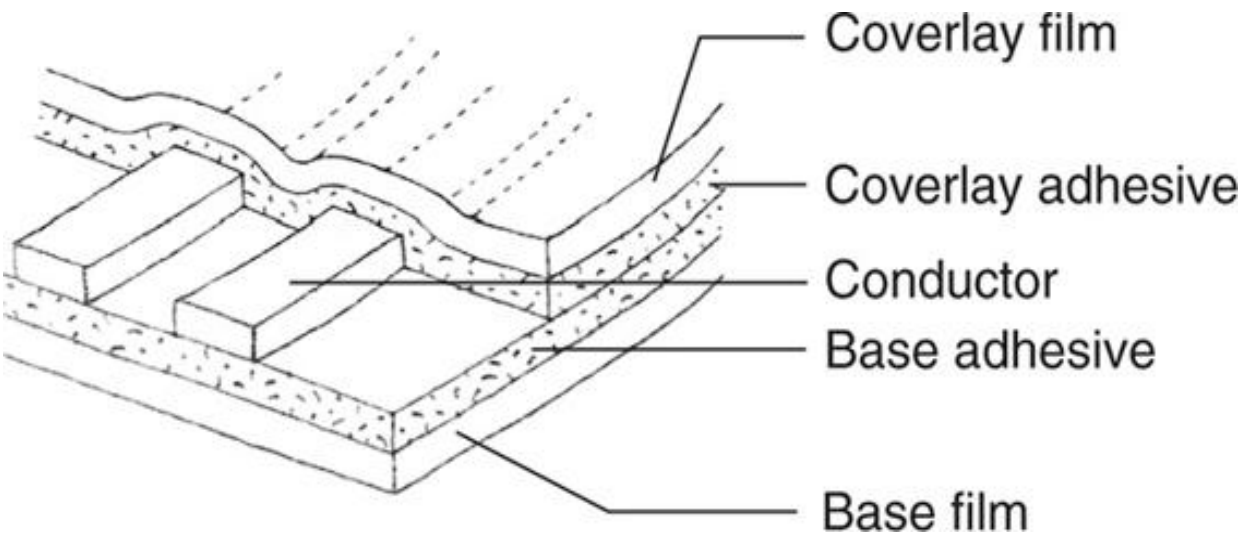


FIGURE 66.3 Basic structure of single-sided flexible circuit.

TABLE 66.2 Thickness of Base Substrates

	Base Film, µm	Adhesive, µm
Polyester base/adhesive type	25, 38, 50, 75, 100, 125, 188	25–50
Polyimide base/adhesive type	12.5, 25, 38, 50, 75, 125	25–50
Polyimide base/adhesiveless type	12.5, 25, 30, 35, 40, 50	No
Glass-epoxy	100, 200	~0

Adhesive layer thickness is doubled for double-sided laminates.

The thickness of the adhesive layers must be counted when total thickness is considered.

Possible fine-line capability is illustrated for each copper thickness in Fig. 66.4. Currently 18- and 35-µm copper foils are standard. Copper foils 12 µm and 9 µm thick are becoming the new standard to enable finer pattern etching. Thinner copper foils are available in sputtered/plated adhesiveless laminate materials. The fine-trace etching

capability depends very much on the manufacturer, especially the exposure process and etching process.

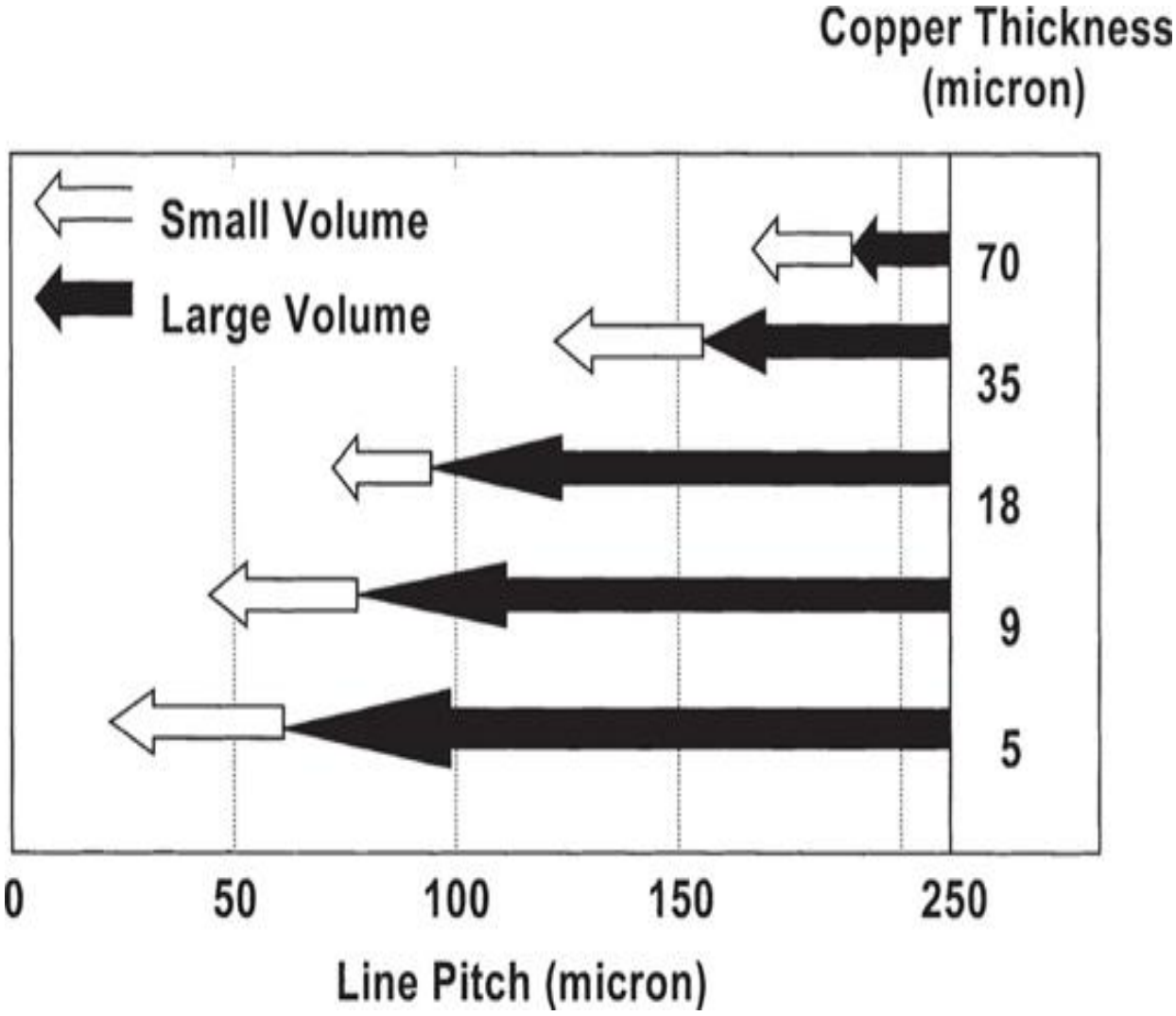


FIGURE 66.4 Fine line capabilities. Potential line pitch is noted for copper thickness alternatives along with whether a given thickness leads itself to high-volume production or requires too a high level of technical interaction.

66.2.3 Coverlay System of Flexible Circuits

The coverlay system of flexible circuits is one of the big differences from rigid printed circuit boards, as shown in Fig.

66.3. A coverlay has to have more functions than the solder mask of rigid boards. It should not only have solder dam capability, but also mechanical protection capability for the fragile conductors of flexible circuits. Also it is required to have high toughness to survive long flex endurance and to optimize the major advantage of flexible circuits.

Appropriate coverlay material and thickness including adhesive layers have to be chosen to have the best balance between the layers. Generally, the same film material laminated with appropriate adhesive as base substrate is selected as the coverlay materials. Polyimide film coverlay should be selected for the high temperature assembling processes such as soldering.

The manufacturing process for the film coverlay is very complicated compared to the solder masks of the rigid boards, so the final cost of the circuits cannot be low. Flexible, screen-printable inks are a low-cost solution; however, most of the ink materials made of epoxy resins do not have good mechanical properties and cannot be applied for dynamic flexing usage. A combination of polyimide-based screen-printable coverlay on adhesiveless copper-clad laminate provides the smallest total thickness with very long flexing endurance life. A comparison of cross sections is shown in Fig. 66.5.

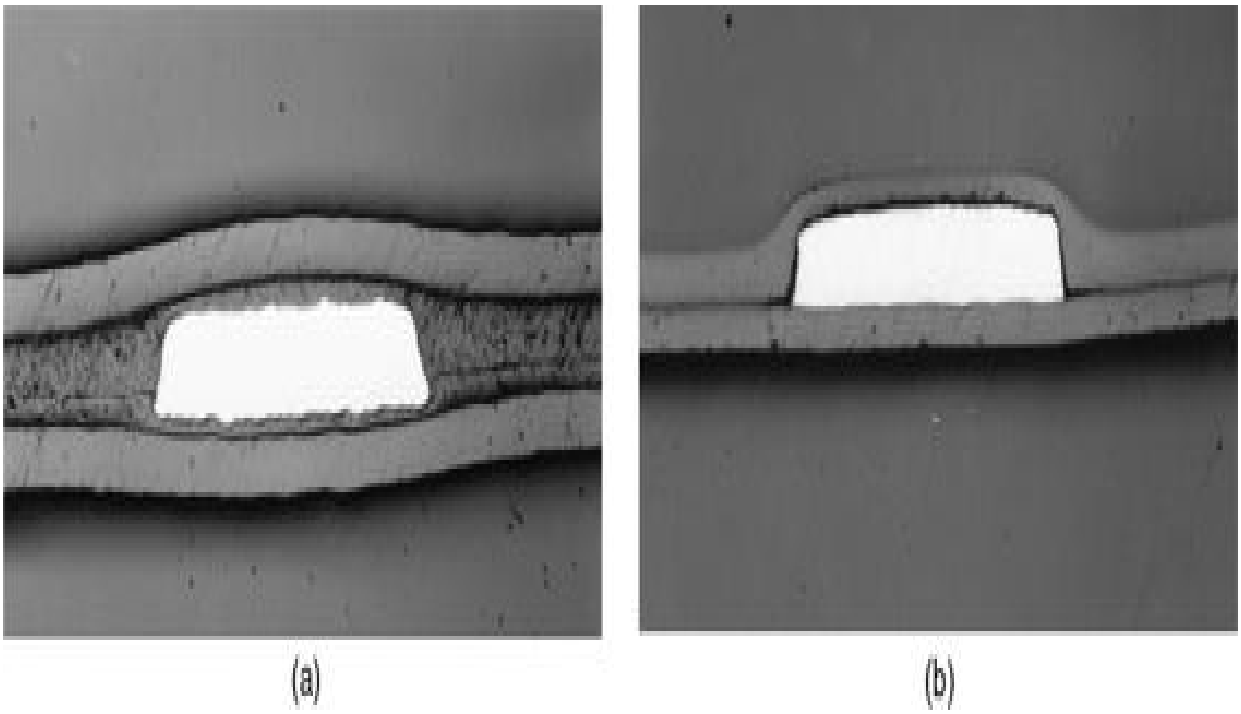


FIGURE 66.5 Cross-section of a single-sided flexible circuit showing (*a*) adhesives-based laminate and film overlay, (*b*) adhesiveless laminate with liquid coverlay.

High-density flexible circuits that have been developed since 1990 need a small pitch opening with high accuracy on the coverlay. Because traditional coverlay technologies have no capabilities to meet these requirements, new technologies were required. Many new technologies and new materials have been developed to satisfy the new requirements of high-density flexible circuits. The capabilities of the major technologies are shown in Table 66.3.

TABLE 66.3 Varieties of Coverlay

	Material Selection	Thickness, µm	Dimensional Accuracy (Minimum Opening)	Reliability (Flexing Endurance)
Traditional film coverlay	PI, PET	30–100	±0.3 mm (800 µm)	High (long)
Film coverlay + laser drilling	PI, PET	30–100	±50 µm (50 µm)	High (long)
Screen print liquid ink	Epoxy, PI	10–20	±0.3 mm (600 µm)	Acceptable (short)
Photoimageable (dry film type)	Epoxy, PI, acrylic	25–50	±50 µm (80 µm)	Acceptable (short)
Photoimageable (liquid ink type)	Epoxy, PI	10–20	±50 µm (80 µm)	Acceptable (short)

For example, laser drilling is capable of generating openings smaller than 100 µm on the traditional film coverlay; therefore, it satisfies the requirements of physical performance and high density surface-mount technology (SMT) assembling. However, the processing costs of the laser abrasion are much higher than other coverlay processes, and it is difficult to apply for the high-volume production of consumer applications. A screen-printing process provides a slightly higher resolution than traditional prepunching process of the film coverlay, but the process can not satisfy the recent requirement for high density SMT assembly. A practical solution is the combination of film coverlay for the flexing areas and solder mask for the SMT areas. It needs supplemental processing to complete the construction, accordingly the total process yield will be lower and the final cost of the circuits could be higher.

The idea of the photoimageable coverlay could be the final solution to solve the all requirements, including the processing cost. The photoimageable solder mask materials developed for rigid boards are too brittle, however, and a lot of cracks can be created easily by small radius bending—requiring flexible materials. Several types of flexible

photoimageable coverlay materials have been developed with different base resin systems. Most of the photoimageable coverlay materials provide finer resolutions than 200-μm pitches, but the physical performances very depend on the base resin systems. Suitable material should be chosen for the applications.

Appropriate surface treatments for the bare conductors after the coverlay construction should be chosen according to termination technologies. Several examples are listed in Table 66.4. Details are explained in Chap. 64.

TABLE 66.4 Surface Treatments and Termination Technologies

Surface Treatment	Termination Technologies
Solder and lead-free solder	Lead-free soldering, FFC connector
Lead-free Hot-air leveling	Lead-free soldering
OSP (preflux)	Lead-free soldering
Hard Ni/Au plating	Connector, pressure contact
Soft Ni/Au plating	Wire bonding, direct bonding
Tin	Lead-free soldering

66.2.4 Surface Treatment Alternatives Stiffener Boards

Thinness and bendability are the major advantages of flexible circuits. However, flexible circuits can lose mechanical strength when it is necessary as part of a composite assembly. The addition of stiffeners on flexible circuits is a practical solution to solve the conflicts, but

appropriate stiffener board materials and adhesive materials have to be chosen based on the applications purposes.

Figure 66.6 illustrates typical examples of the stiffener systems. The first one shows a stiffener construction for an insertion part into a connector. A stiffener adjusts the total thickness of the insertion part. Heat resistant materials, such as polyimide films, are not required for the construction. PET films with pressure-sensitive adhesive (PSA) could provide the low cost combination. A second example shows a case of the assembling of the traditional lead components. A relatively thick stiffener board, such as glass/epoxy, is bonded on the component side to support heavy parts. The soldering for the leads is conducted at the other side. Heat resistant materials including adhesives have to be chosen to survive the high temperature soldering process. Thermo-setting type adhesives should be chosen instead of PSA for the high reliability requirements. The third example indicates the case of SMT assembling. A thin heat resistant stiffener material such as polyimide film is bonded on the other side of SMT assembling.

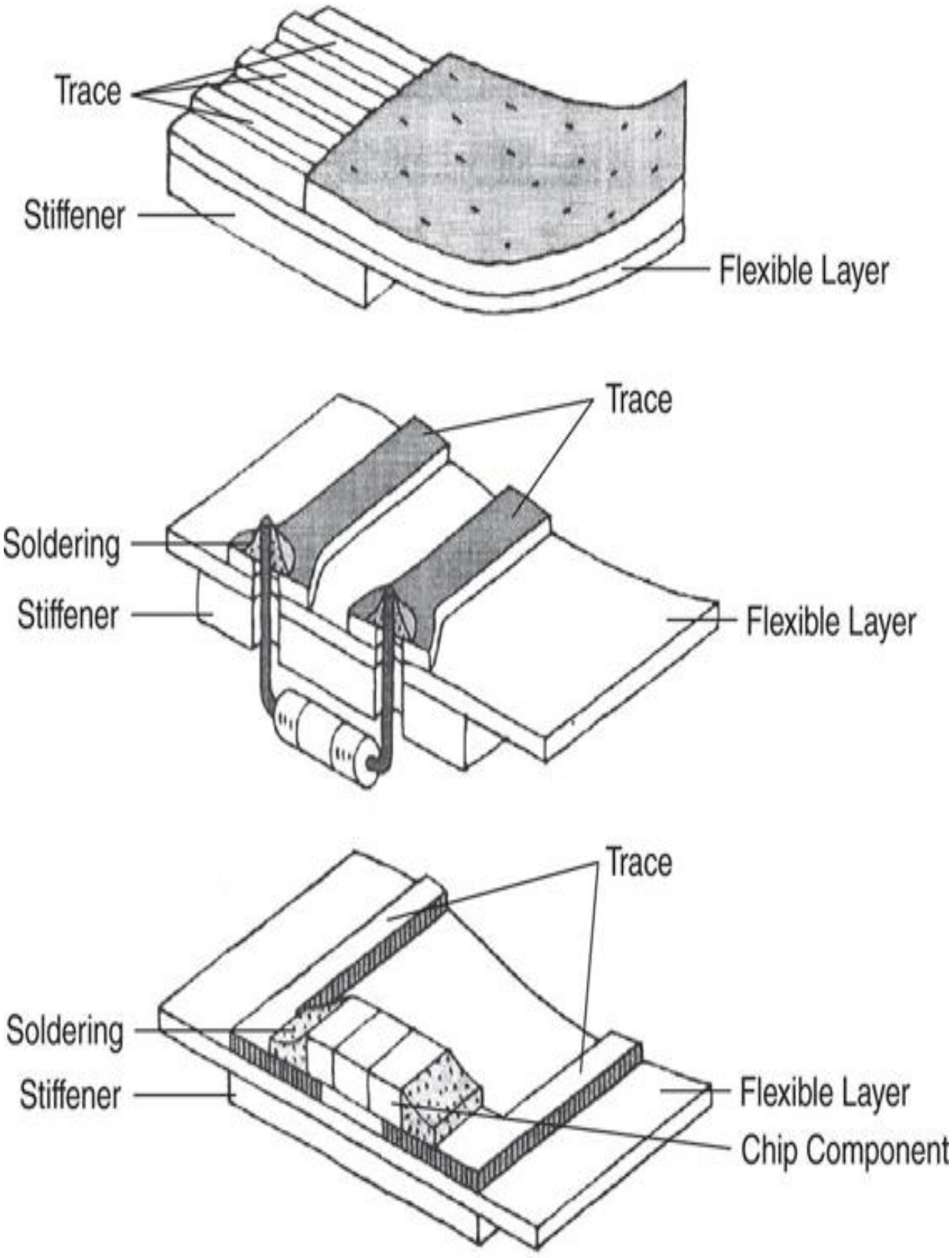


FIGURE 66.6 Stiffener systems for flexible circuits.

66.2.5 Double-Sided Circuits with Via Holes

A double-sided flexible circuit can have the same through-hole structures for the traditional designs as rigid circuit boards. However, there are several critical differences in micro via holes on flexible circuits. Most of the differences come from a thin-film base substrate such as polyimide film. Electrically plated copper conductors are much more brittle than rolled-annealed copper foils; therefore, thin copper plating is preferred to maintain the flexibility of the circuits. Generally, sufficient through-hole reliability is established with 15-μm-thick copper plating. Copper plating should be eliminated from the dynamic flexing area by using a suitable masking method.

Adhesiveless, copper-clad laminates that have simple and uniform substrate layers and smooth copper surfaces have become popular in high-density flex circuits. Because of thin film materials, there are several choices in small hole generation and copper plating processes. Flex circuits can contain both through holes and blind via holes for double-sided circuits as shown in Fig. 66.7. Micro-size blind via holes on double-sided flex circuits confer the ability to make SMT assembly density much higher.

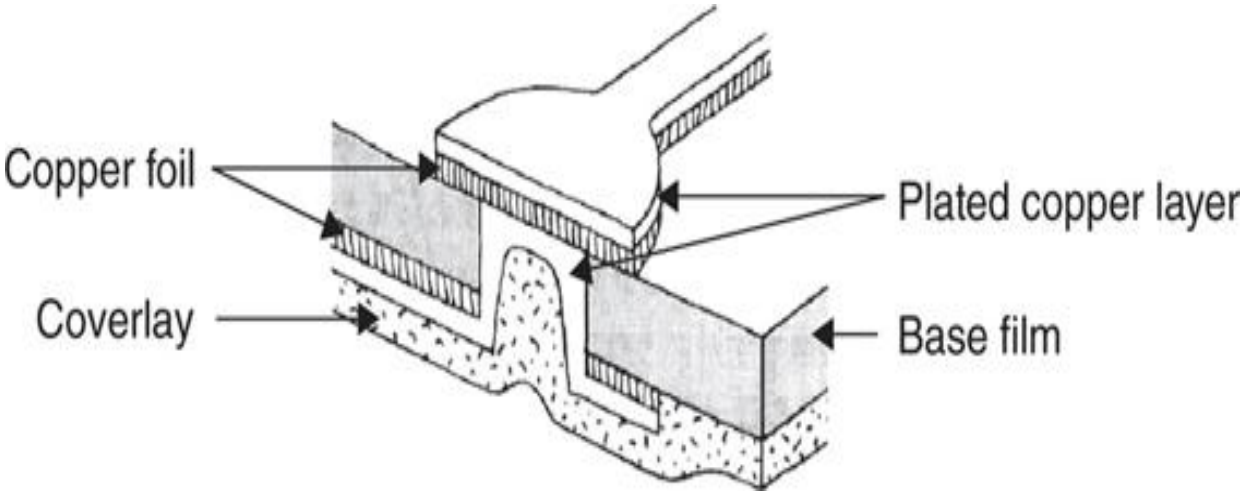


FIGURE 66.7 Blind via structure of double sided flexible circuits.

The micro via hole capability depends on the process used by the manufacturer; however, general ideas are introduced in Chap. 61. Certainly the smaller via holes are available for the thinner substrates. Using the latest technology, such as excimer laser drilling, micro via holes smaller than 40 μm are available for 25-μm-thick adhesiveless polyimide base substrates.

Microvia hole capabilities for polyimide substrates are shown in Fig. 66.8.

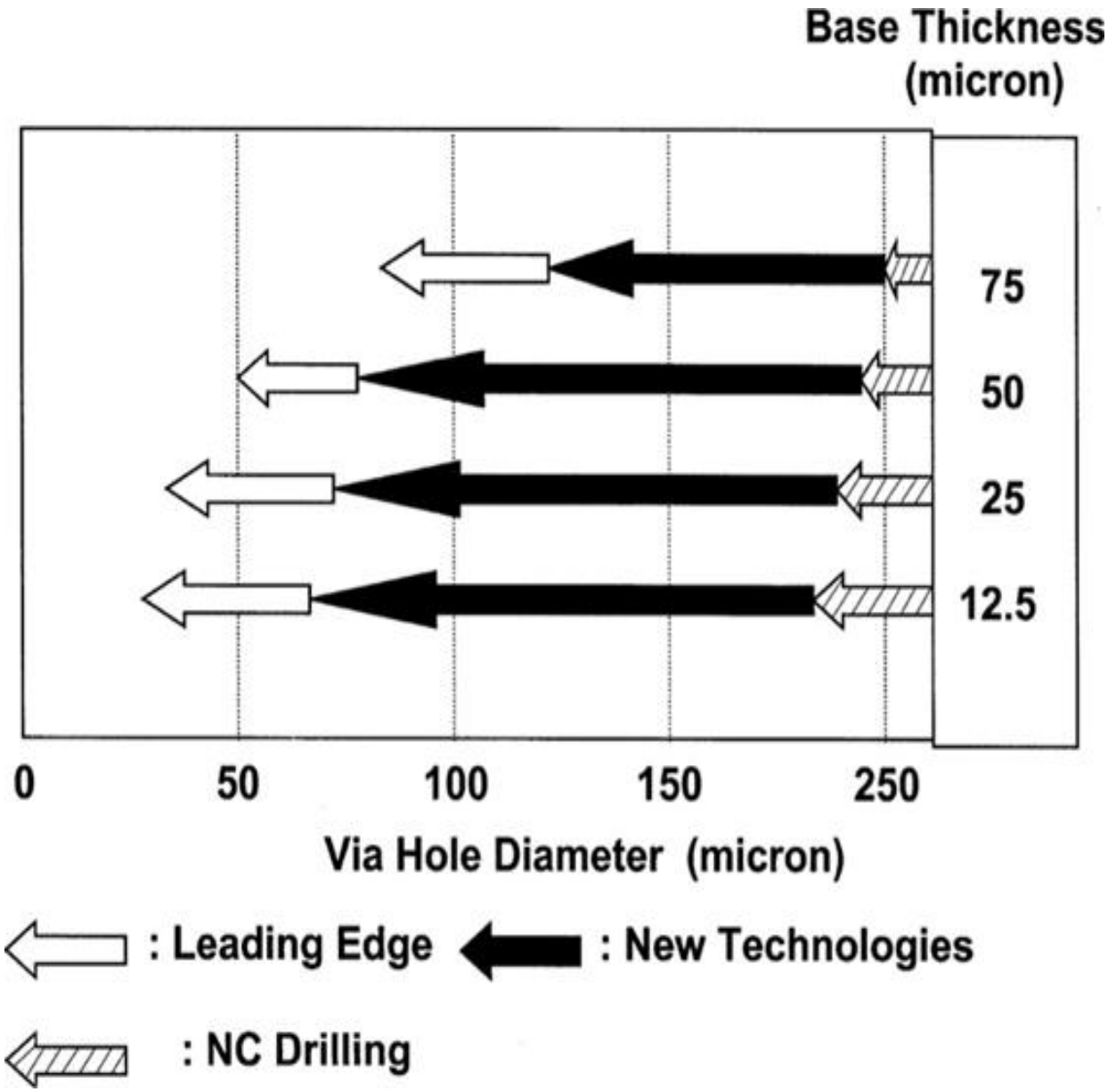


FIGURE 66.8 Microvia capabilities shown by base thickness and hole diameter. Also shown is the range of technologies from HDI to mechanical drilling required to create the vias.

Basically, the same construction systems of coverlay, stiffeners, and surface treatments as single-side flexible circuits could be available for double-side flexible circuits.

66.3 MULTILAYER RIGID FLEX (MULTILAYER FLEX)

A simple, multilayer, flexible circuit does not make sense other than for its small thickness, because these circuits will not have any more flexibility. Therefore, rigid/flexible constructions that contain both rigid parts and flexible parts have been developed. A typical layer construction is illustrated in Fig. 66.9. It is not a simple combination of flexible circuits and rigid circuits. Generally, there are common flexible layers that are separated in the flexible parts. A flexible layer of the flexible parts can have only one or two conductor layers to keep high flexibility. At the rigid parts, the flexible inner layers are sandwiched by cap layers that consist of rigid circuit materials such as glass epoxy or glass polyimide. The constructions of rigid parts are very similar to those of rigid multilayer circuits except for the thin polyimide dielectric layer inside. Thin polyimide films were used as the cap layer at the rigid part to reduce the total thickness required in portable electronics such as cellular phones. The multilayer construction in these cases, the circuits are called multilayer flex.

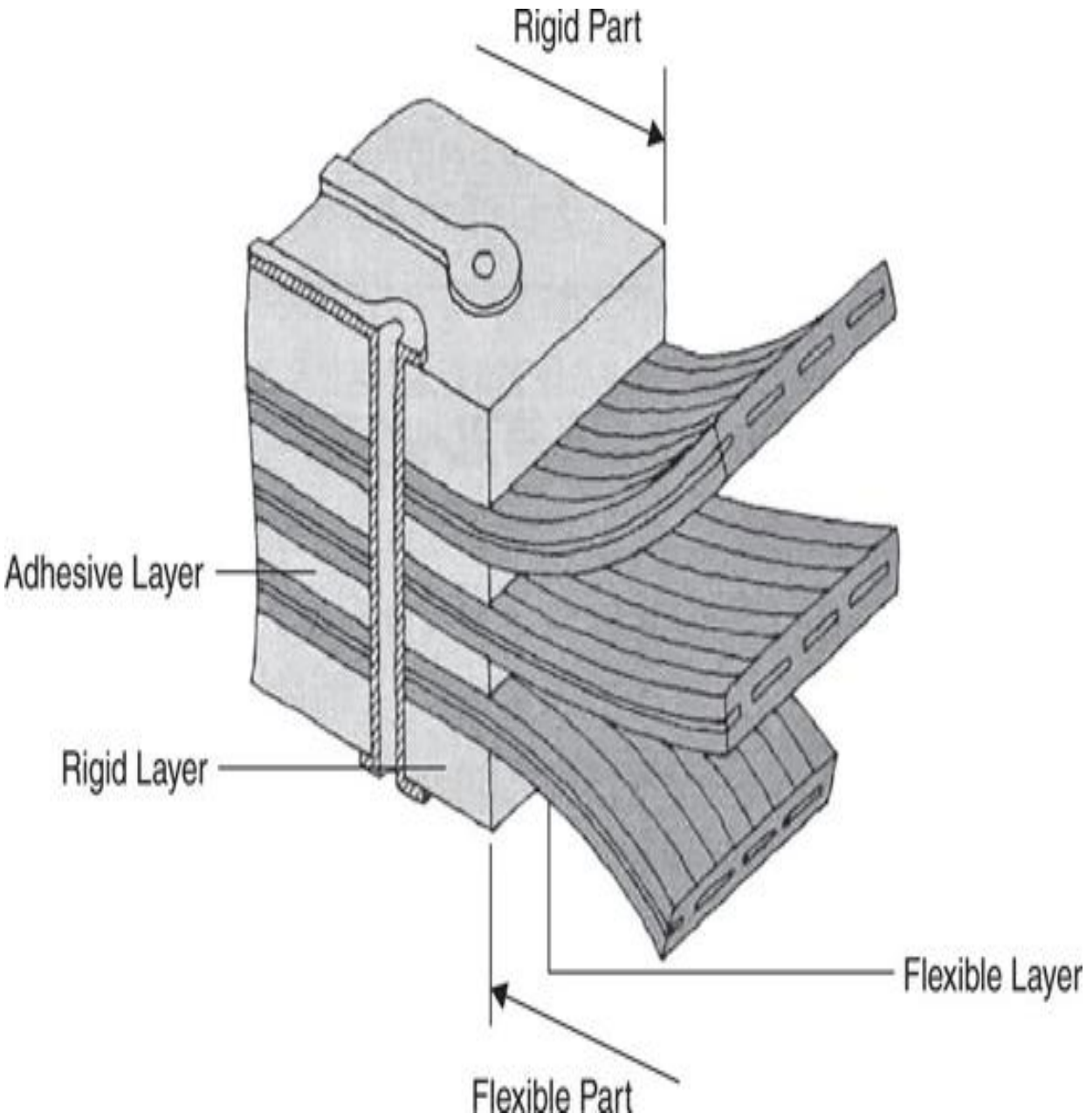


FIGURE 66.9 Multilayer rigid flex construction.

Through-hole and blind via hole constructions similar to those of multilayer rigid circuit boards are available using coated copper foil or photo-via processes for multilayer flexible and rigid/flexible circuits. However, there are more varieties from which to choose in both materials and manufacturing processes. Basically, the same assembly technologies are available on the rigid parts. The latest

portable electronic equipment, such as palmtop computers, requires high-density SMT assembling on the rigid parts.

There are no limits to the number of flex layers. More than 30 layers are built into one rigid/flex circuit for aerospace applications. However, the circuits require very complicated manufacturing processes—more so than the standard rigid multilayer circuits—and therefore their costs are much higher than costs for rigid boards of the same size. Design should be considered seriously prior to manufacturing to reduce the total cost based on the capability of the manufacturer. A higher circuit density can reduce the layer counts and the total manufacturing cost.

66.3.1 Flying-Lead Construction (Double Access Construction)

A specialty construction for flexible circuits is the double-electrical access capability on even single conductor layer circuits, achieved by removing the base insulation layer under the conductors as shown in Fig. 66.10. It can be an alternative construction instead of double-side circuits with through holes for the low cost 3D wiring. When the insulation layers are removed from both sides of the conductors, they can then be partially free from the organic materials. Unsupported conductors, also known as flying leads or flying fingers, are not a new idea in the construction of flexible printed circuitry (Fig. 66.10). The biggest advantage of flying-lead technology is its extremely high heat resistance and thermal conductivity when compared to standard conductors insulated by dielectric substrate materials. Based on the lack of insulation, flying leads can be treated as a bare conductor material similar to bare wire. There are many high-density flexible circuit applications that require flying-lead terminations. Details are discussed in Chap. 64.

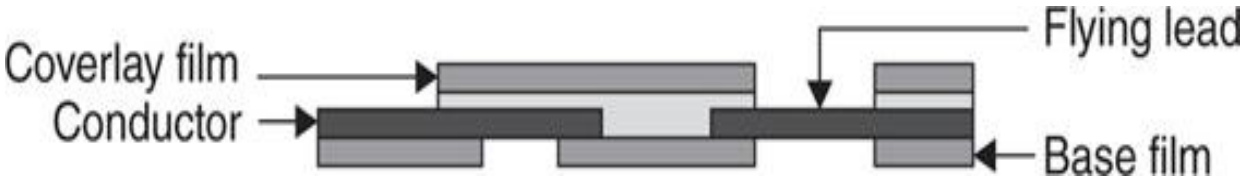


FIGURE 66.10 Flying lead construction (double-sided construction).

Consideration must be given to specific surface treatments required on the flying leads to make each of the various application terminations. Previously, tin/lead plating was the most common treatment for various soldering processes; however, it is expected to be replaced by lead-free technologies, which need higher temperatures for the soldering. Soft gold plating with a nickel underplating is the standard surface treatment for the wire bonding and direct bonding to the other devices. The purity and the thickness of the plated gold, along with the bond strength of the plated layer, are important factors in bond performance.

Copper thickness is a key consideration when developing a new circuit design involving flying leads. Although it is easier to manufacture high-density circuits utilizing thinner copper, the resultant flying lead may be extremely fragile and will not have the mechanical strength of the thicker copper circuits (see Fig. 66.11). Manufacturing yield plays an important role in the overall circuit costs, and thinner copper foils typically result in more damage during processing. It is important to understand this correlation as poor circuit design can affect manufacturing yields.

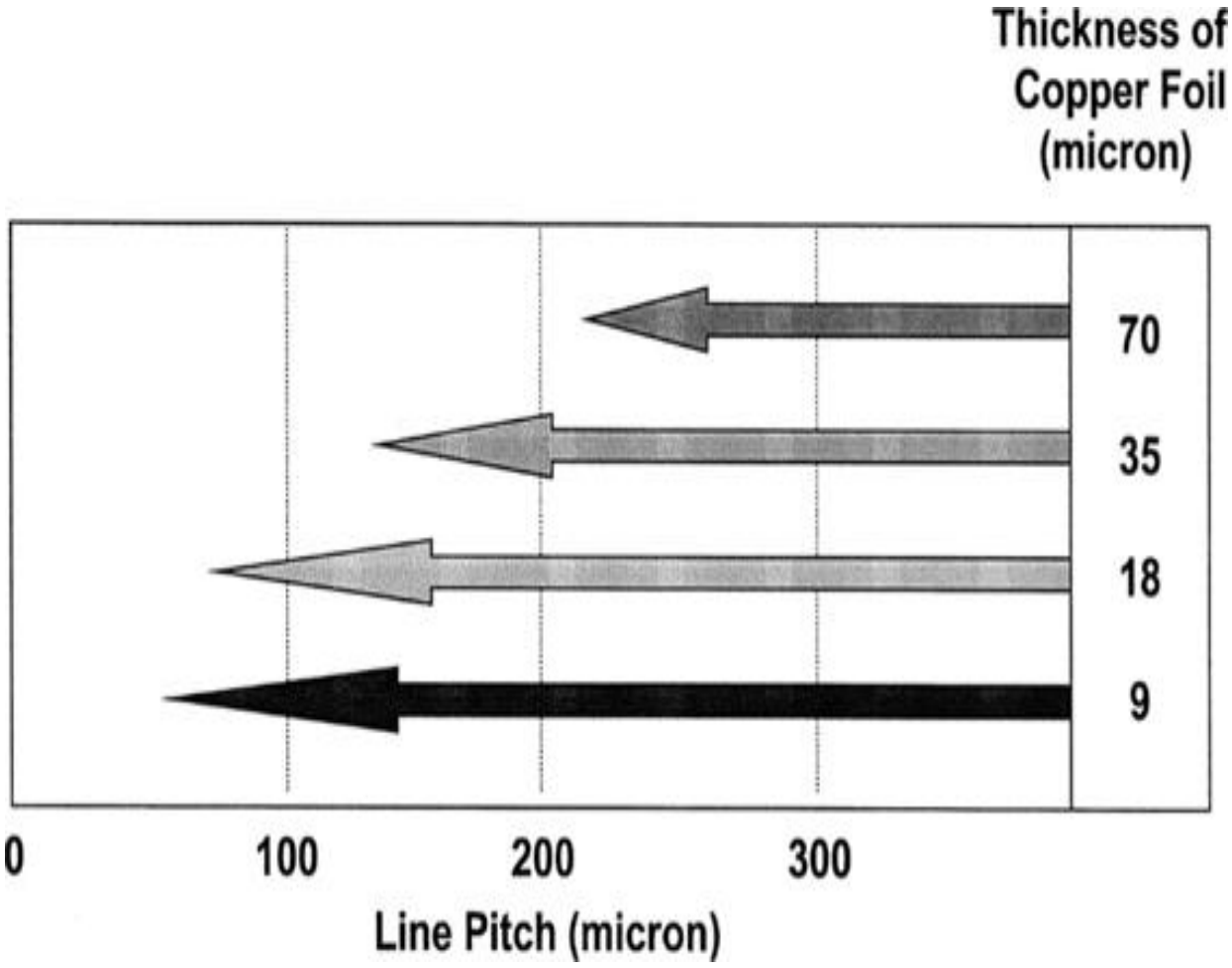


FIGURE 66.11 Flying lead capability of copper foil, showing potential line width versus thickness of the copper foil.

Because the flying leads are basically bare conductors, suitable surface treatments should be conducted according to termination technologies.

66.3.2 Microbumps and Dimples

Many kinds of microbump arrays and dimple arrays have been developed for high-density terminations of flexible circuits other than solder ball grid arrays. Recent technologies allow for a wide variety of shapes, materials, sizes, and pitches; down to 50 μm. The solder ball arrays are built by similar processes of the rigid ball grid array (BGA)

substrates. The combinations of the electrical and electroless-plating process provide a lot of choice for the shapes and sizes of the microbump arrays on flexible circuits. The double-access capabilities of flexible circuits provide more choices for the locations of the microbumps, as shown in Fig. 66.12, other than through coverlay. The microbumps can be built on the bottom side of the conductors through base layers. They can be also built on both sides of the flying leads. An appropriate design should be chosen according to the requirements of the terminations. Whether it's a permanent connection or nonpermanent connection is one of the key points needed for designing the basic constructions of the microbumps. Bump density and reliability are other factors needed to design the microbump structures. Details of the manufacturing processes are described in Chaps. 64 and 67.

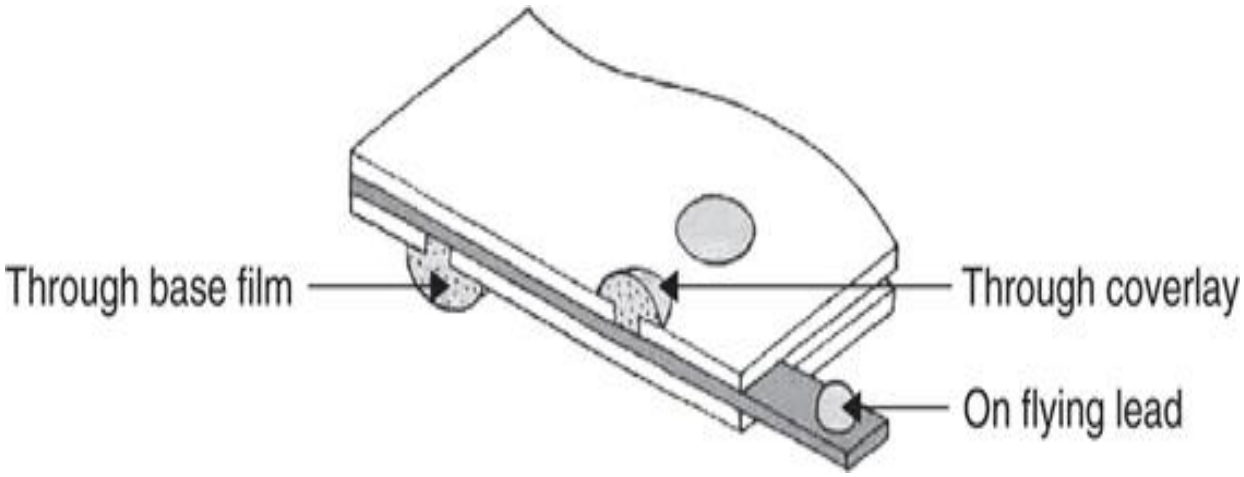


FIGURE 66.12 Locations of microbumps.

Dimple structure of flexible circuits is a low cost solution for the nonpermanent termination. Multiple dimple arrays can be formed on the polyimide base or PET base flexible circuits by simple pressing processes. (Details are shown in Fig. 66.13.) A typical example of the dimple termination is the connection of the disposable cartridges of ink jet printers. Over 60 dimples with hard gold plating are formed

at the end of flexible circuit for the connection with the ink cartridge. The dimple arrays can make reliable connections over one thousand times.

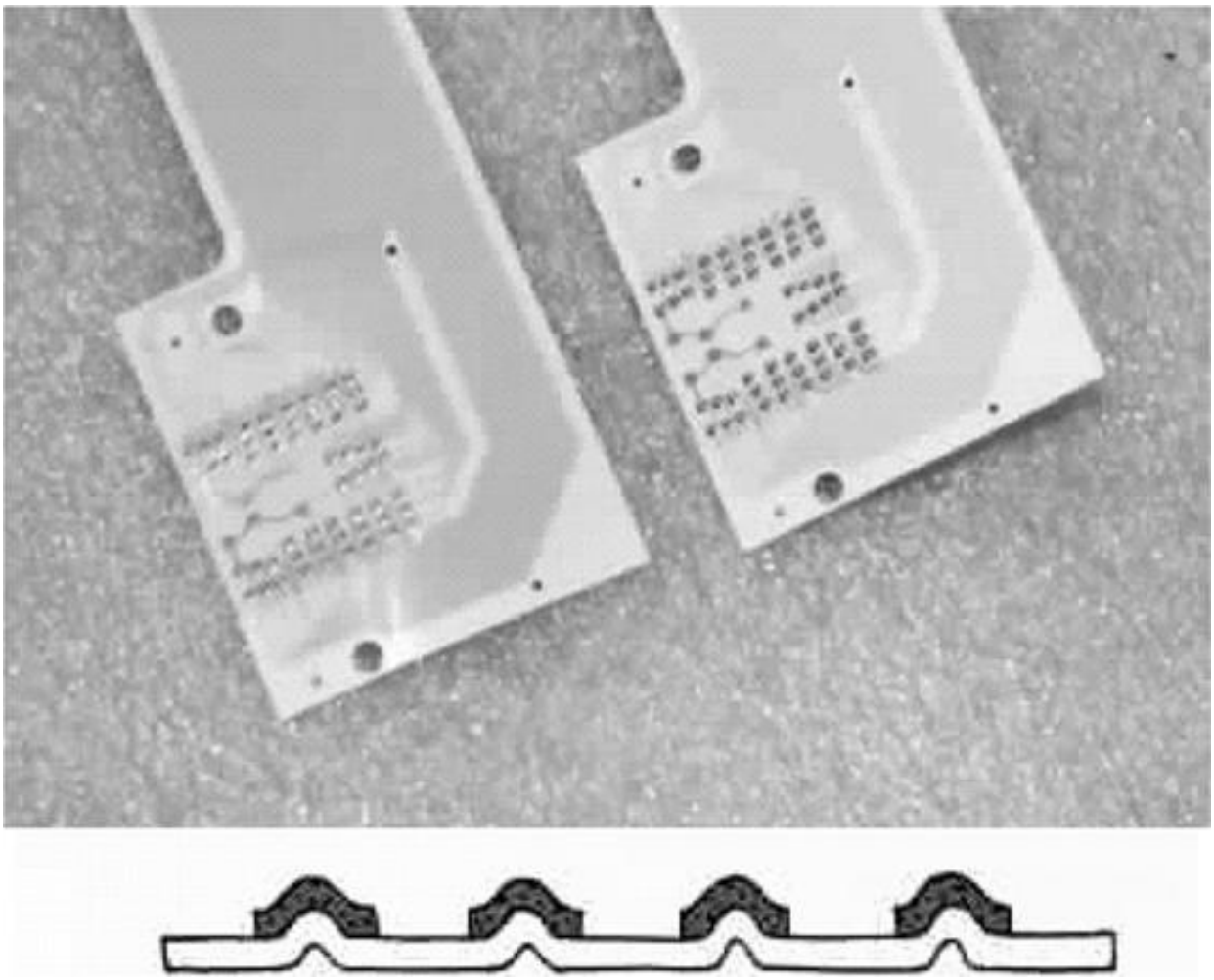


FIGURE 66.13 Dimple structures (ink jet printer).

66.4 CIRCUIT DESIGNS FOR FLEXIBILITY

One of the major features of flexible circuits is their long flexing endurance. A suitable layer construction and

materials survives over billion times of flexing with a small radius (Fig. 66.14).

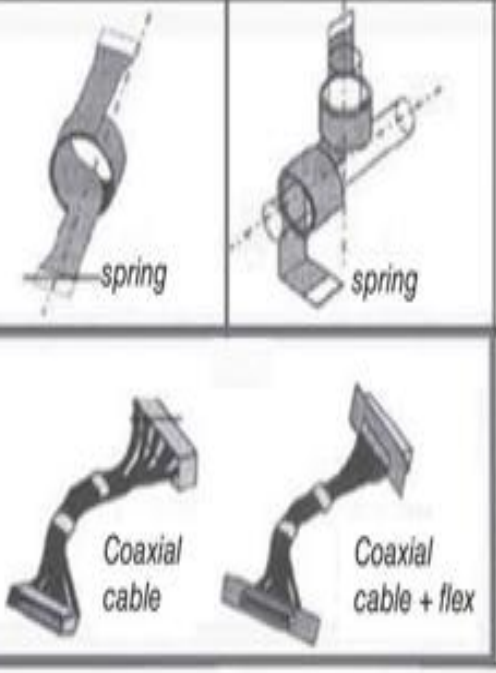
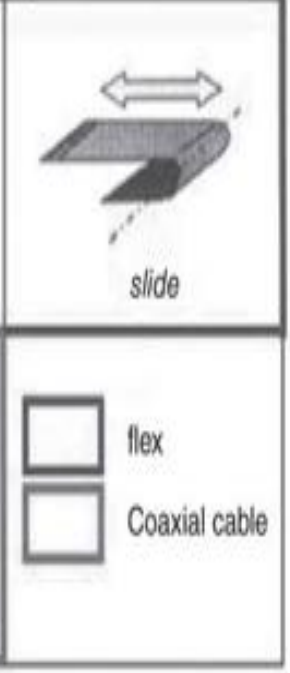
Hinge Type	Shell	Revolve	Universal	Slide
Diagram				
Copper Thickness	RA copper ½ oz	RA copper ½ oz	RA copper ½ oz	HTE copper ⅓ oz
PI	1 or ½ mil	1 or ½ mil	1 or ½ mil	0.7, 0.8, or ½ mil
Structure suggestion	1. Single side flex 2. Double sided flex with one side trace 3. Multi-layer with air gap	1. Single side flex 2. Double sided flex with one side trace	1. Single side flex 2. Double sided flex with one side trace	1. Single side flex is preferred 2. Double sided flex with one side trace 3. Due to very tight space, air gap is not preferred
Application				

FIGURE 66.14 Four types of flexible hinges with copper, bend, structures, and applications.

A basic idea of the mechanical stress during the bending is illustrated in Fig. 66.15*a*. To have the longest flexing life, the conductor layer should be the center of the layer construction. It should have symmetrical layer constructions for both sides of the conductor layer. The flexing life will be remarkably shorter when the conductor layer is outside of the bending center as shown in Fig. 66.15*b*. A rolled annealed copper foil should be used instead of ED copper foil for a longer flexing life. But there is no exact relation between roll direction and flexing endurance; the exact performance should be evaluated for each material. Generally, 35-µm-thick RA copper is more expensive than the same thick ED copper foil. The cost difference between RA copper foil and ED copper foil will be larger at thinner thickness. A high ductility ED copper foil could be alternative choice for middle class dynamic flexing. Its flexing life is shorter than RA copper foil, but it is less expensive and it can survive one million flexing instances with an appropriate layer construction and flexing radius.

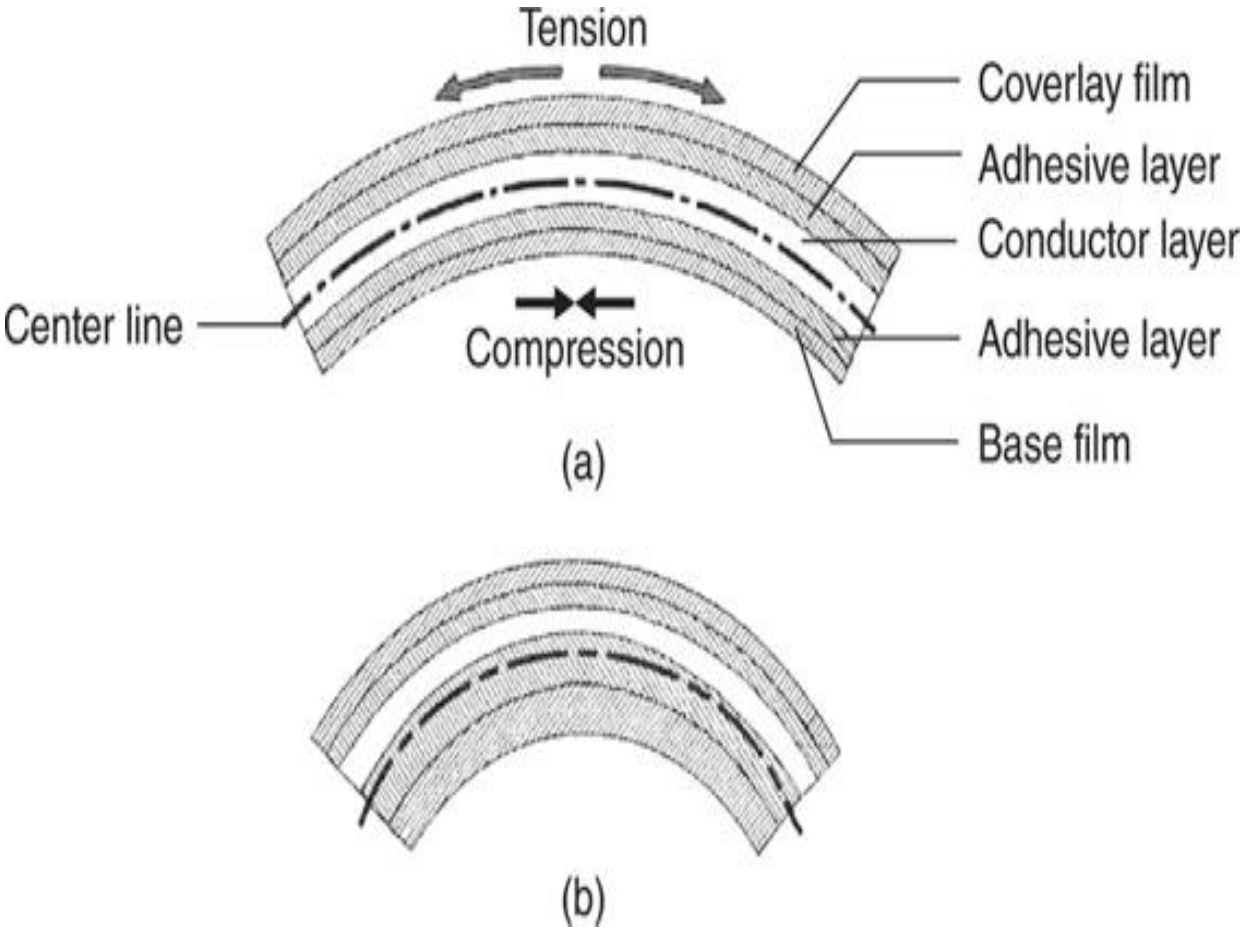


FIGURE 66.15 Mechanical stress at bending: (*a*) symmetrical, (*b*) nonsymmetrical.

Another principle is that for dynamic flexing, the thinner the layer, the better. An 18-µm-thick copper foil has a longer flexing life than a 35-µm-thick copper foil. A 12.5-µm-thick polyimide film provides a longer flexing life than a 25-µm-thick polyimide film (Fig. 66.16). Adhesive layers should be as thin as possible for dynamic flexing. But thin adhesive layers do not have good bond strength and good encapsulation for traces, and therefore a suitable thickness should be determined based on experimental data. Generally, polyimide films have a longer life than polyester films. The combination of a thin, adhesiveless, polyimide base laminate and a thin coverlay of liquid polyimide resin could be the best solution to have the longest flexing life.

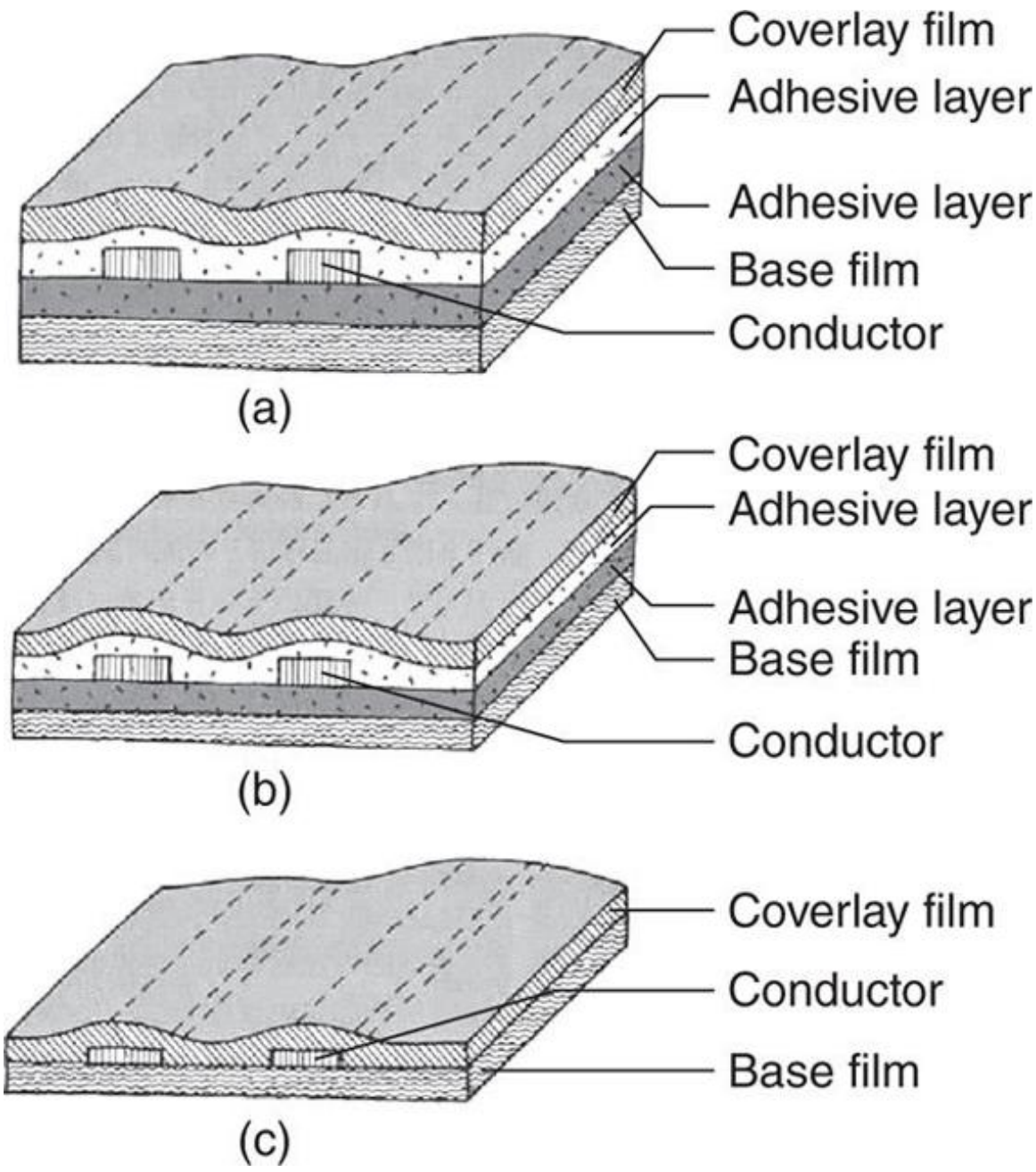


FIGURE 66.16 Layer construction for dynamic flexing: (*a*) standard layer construction, (*b*) dynamic flexing construction with thin adhesive layers, and (*c*) dynamic flexing construction without adhesive layer.

Many kinds of bending modes on flexible circuits could be practical, but in IPC-TM-650 it is recommended to evaluate the flexing life using the movement shown in Fig. 66.17.

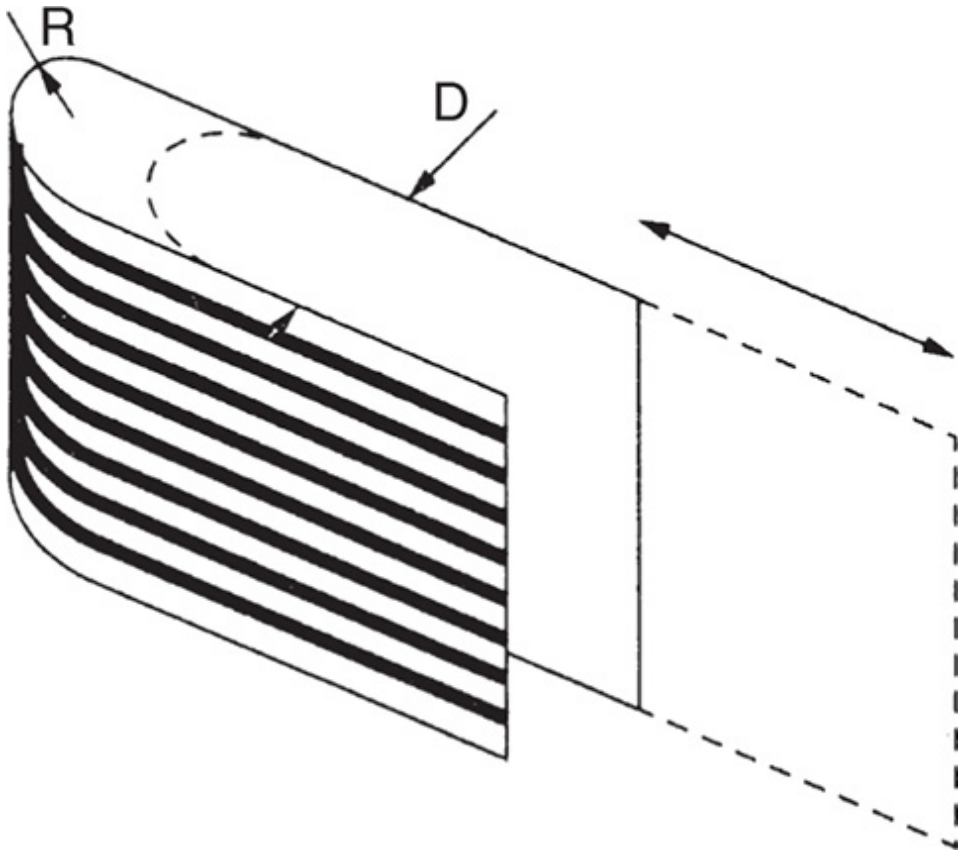


FIGURE 66.17 Typical dynamic flexing mode of flexible circuit specified by IPC-TM-650.

The larger flexing radius provides a longer flexing life, as shown in Fig. 66.18.

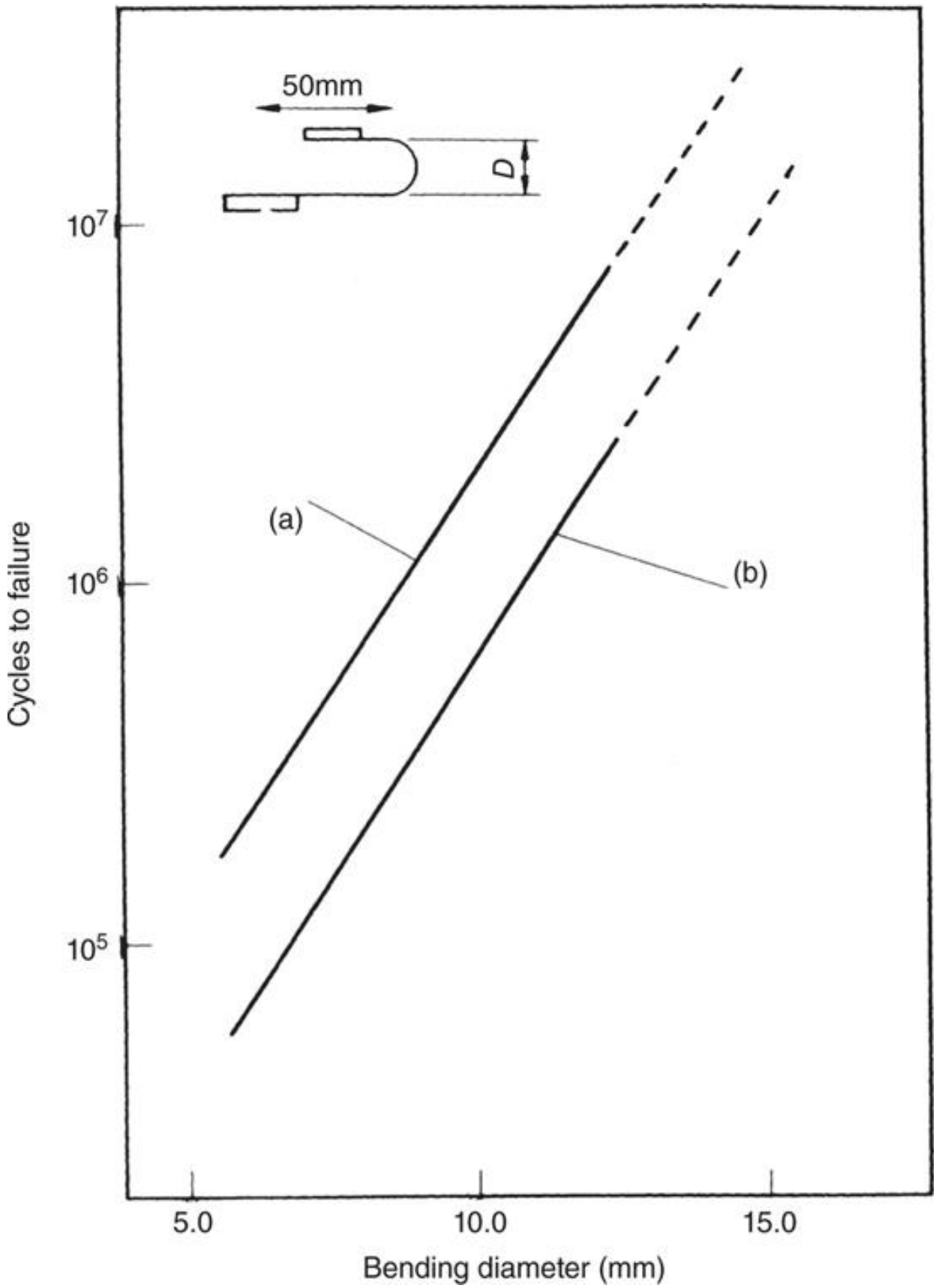

50mm
D
10^7
10^6
10^5
(a)
(b)
Cycles to failure
5.0
10.0
15.0
Bending diameter (mm)

FIGURE 66.18 Flexing radius and life as specified by IPC-TM-650 test method. Bending diameter (mm): (*a*) RA copper foil, (*b*) ED copper foil.

There are several ideas for reducing the risks of flexing failures in actual cases for electronic products; Fig. 66.19 shows some examples.

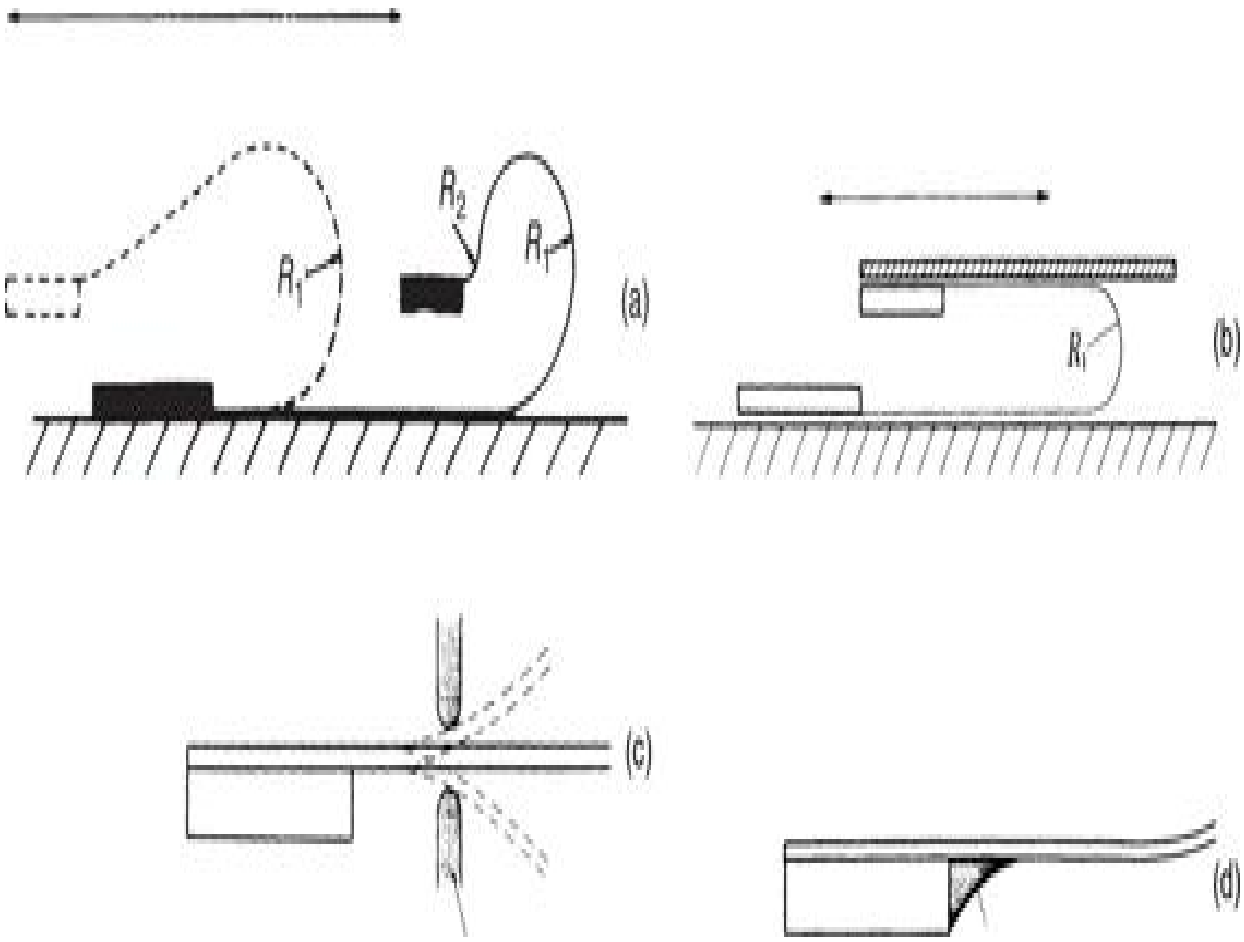
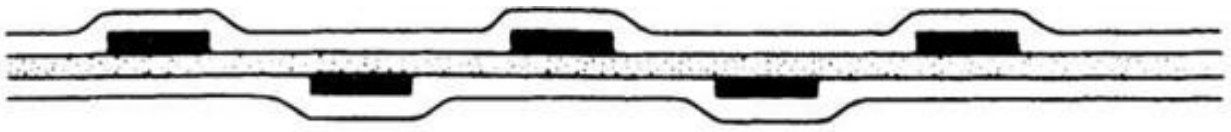


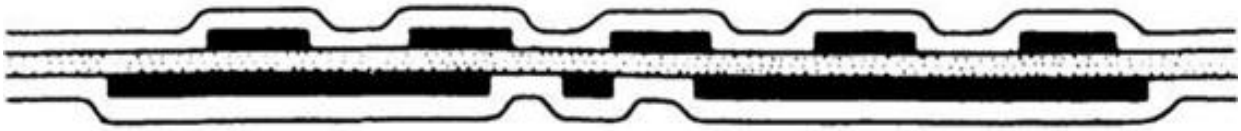
FIGURE 66.19 Design of dynamic flexing part of flexible circuits: (*a*) unacceptable technique, (*b*) guide board, (*c*) loose guide, (*d*) silicone rubber.

Basically, double-sided flexible circuits with through holes are not available for dynamic flexing. The flexibility depends on the configuration of conductors in both sides of the base substrate, as shown in Fig. 66.20 shows examples. Bending the circuit with thin copper circuits on the outside of the flexible circuits may cause them to break, because the mechanical stresses are concentrated on the small traces.



(a)

(b)



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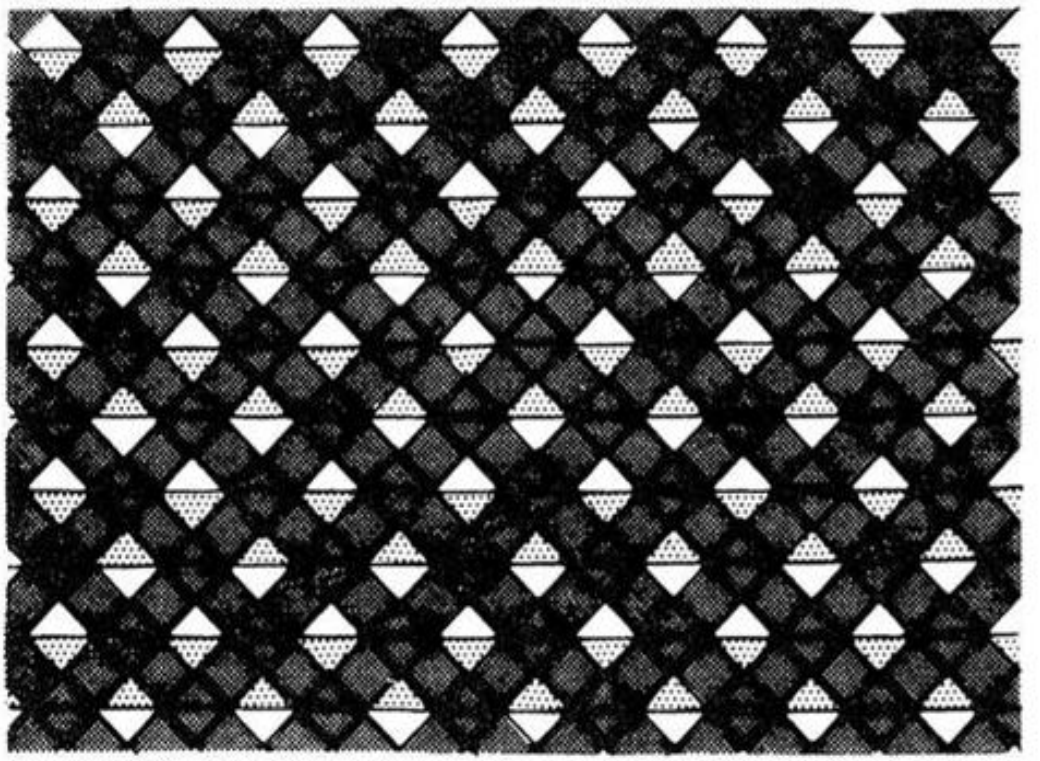

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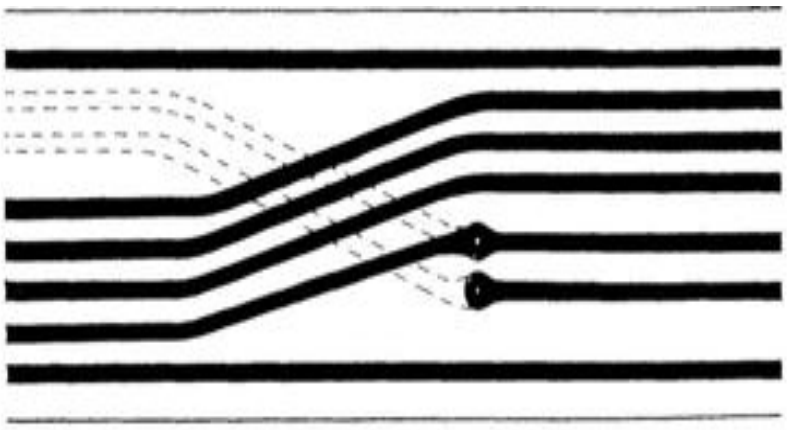

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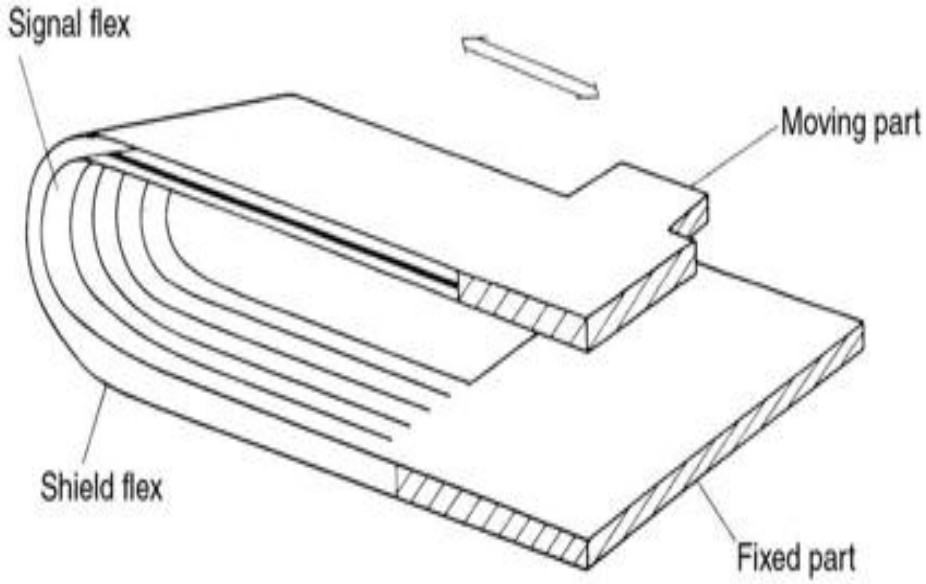

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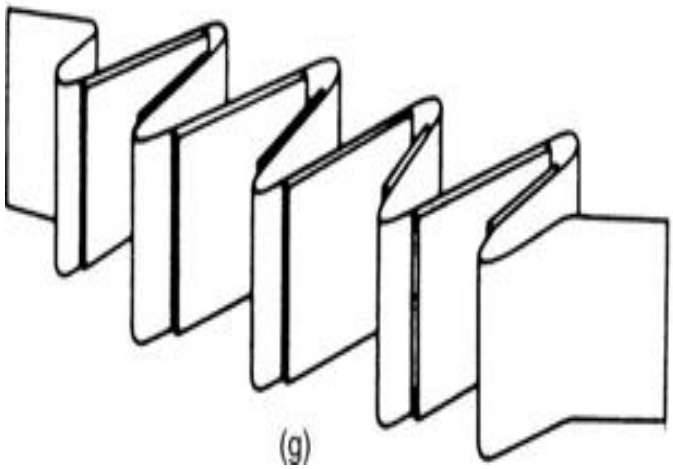
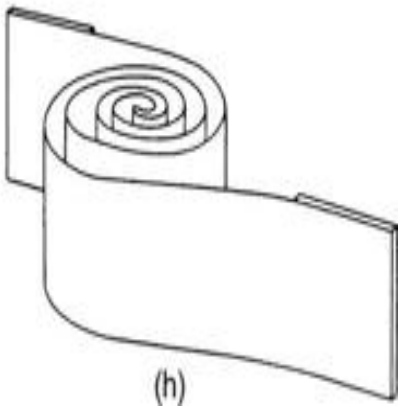


(g)



(h)

FIGURE 66.20 Circuits configuration of double-sided flexible circuits at flexing parts: (*a*) preferred, (*b*) acceptable, (*c*) unacceptable, (*d*) meshed shield layer, (*e*) crossing traces, (*f*) separated shield layer for dynamic flexing, (*g*) fan folded, (*h*) coiled.

A dynamic flexing area of a double-sided flexible circuit should have only one conductor layer. Coverlay on the other side of conductor should also be eliminated to enable symmetrical layer constructions. Copper plating for the through holes of double-sided flexible circuits should be eliminated from dynamic flexing areas using a plating mask.

66.5 ELECTRICAL DESIGN OF THE CIRCUITS

There is no significant difference between the electrical performance of flexible circuits and that of rigid circuit boards. But there are small differences in conductivity and insulation resistance depending on the materials. Also, there are small differences in dielectric constant and tangent delta. Therefore, similar calculations can be applied to determine electrical performances for a flexible circuit. However, flexible circuits have a relatively long parallel circuit for cabling capability, and impedance should be managed carefully, especially for high-speed circuits with high frequencies.

66.5.1 Insulation Resistance

Insulation resistance (IR) is one of the most critical parameters from both a design and materials standpoint. IR tests are utilized in determining the raw materials properties, as well as controlling quality of the end product, since they are indicators of moisture and other contamination

commonly found in the manufacture and handling of flexible printed wiring. The test is conducted by performing IR measurements between conductors on a layer and/or between the layers in a double-sided or multilayer board after a specified time in a humidity and temperature cycle. A voltage of 100 V AC is applied during the test, and measurements are made immediately thereafter.

Cover-coated flexible wiring retain their high-IR values even under severe humidity conditions. Wiring that is not cover coated usually retains high-IR values provided the surfaces are clean and free from flux, fingerprints, etc. The insulation resistance of a 30-ll, polyimide, FPW device of microstrip design and cover coated with a 0.001-in polyimide film-phenolic modified polyvinyl butyral adhesive is shown in Table 66.5.

TABLE 66.5 Insulation Resistance of 30 Ω Microstrip Flexible Printed Circuit (Average Readings)

FPW Device No.	Initial, $\Omega \times 10^{11}$	After Humidity, $\Omega \times 10^{9}$
Line to line		
1	5	7.1
2	5	3.9
3	5	3.6
4	5	4.8
Line to shield		
1	5	11.6
2	5	3.2
3	5	9.0
4	5	8.2

1. All after-humidity readings were taken within 0 to 2 h after removal from humidity.
2. Above readings are average for 45 measurements per FPW.

66.5.2 Dielectric Withstanding Voltage

This property of the wiring is dependent upon the *air* density and conductor spacing. The important factor for the designer to consider is the potential at which flashover occurs in the air above the conductors. The results in Fig. 66.21 will serve as a design guide. The de breakdown voltage variation, as a function of conductor spacing for cover-coated flexible

printed wiring, is shown in Fig. 66.22. *As* indicated, increasing altitude lowers the insulating properties of air, owing to ionization, and thus greater conductor spacing is required.

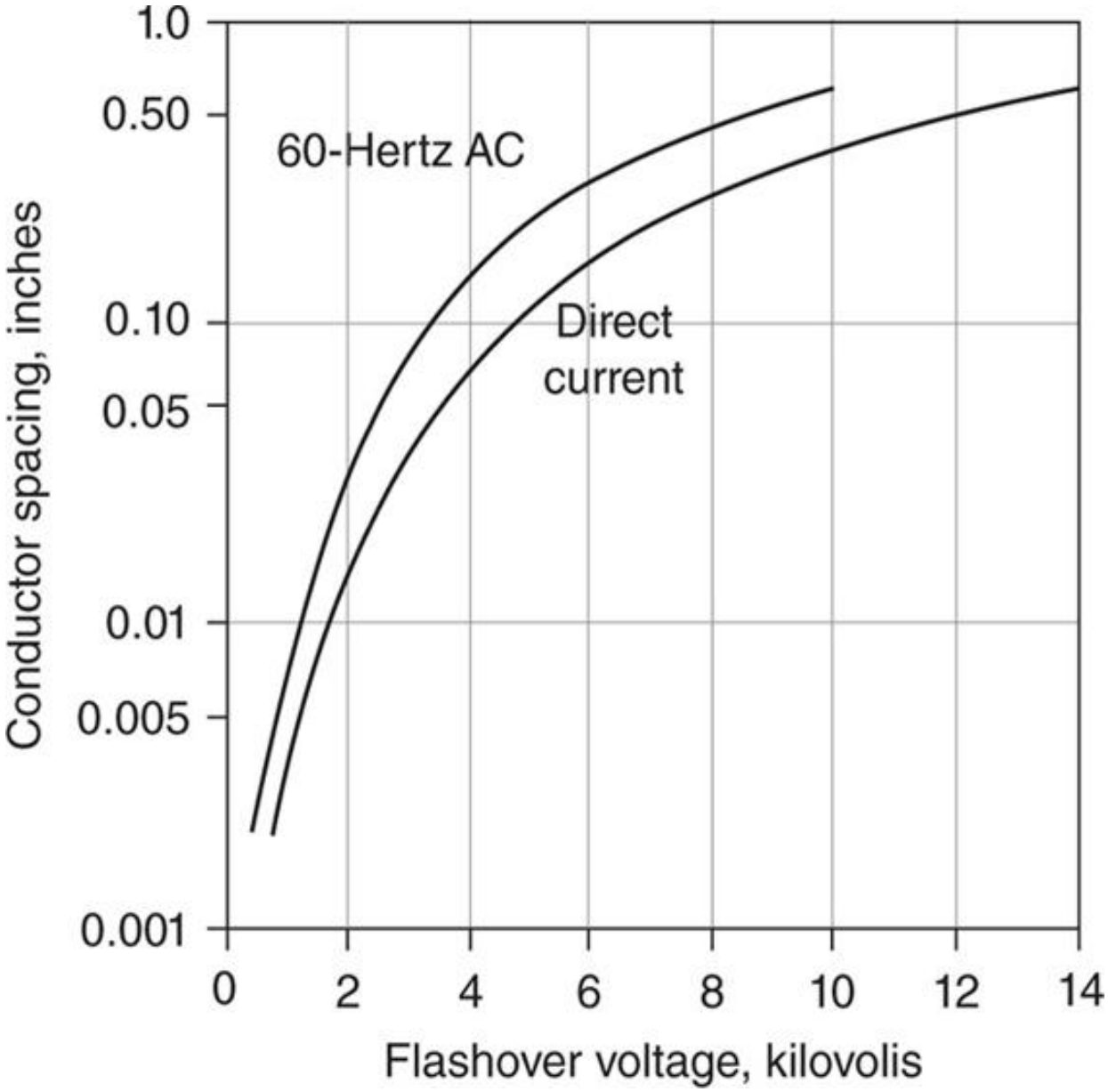


FIGURE 66.21 Flashover voltage in air. (*Sanders Associates*.)

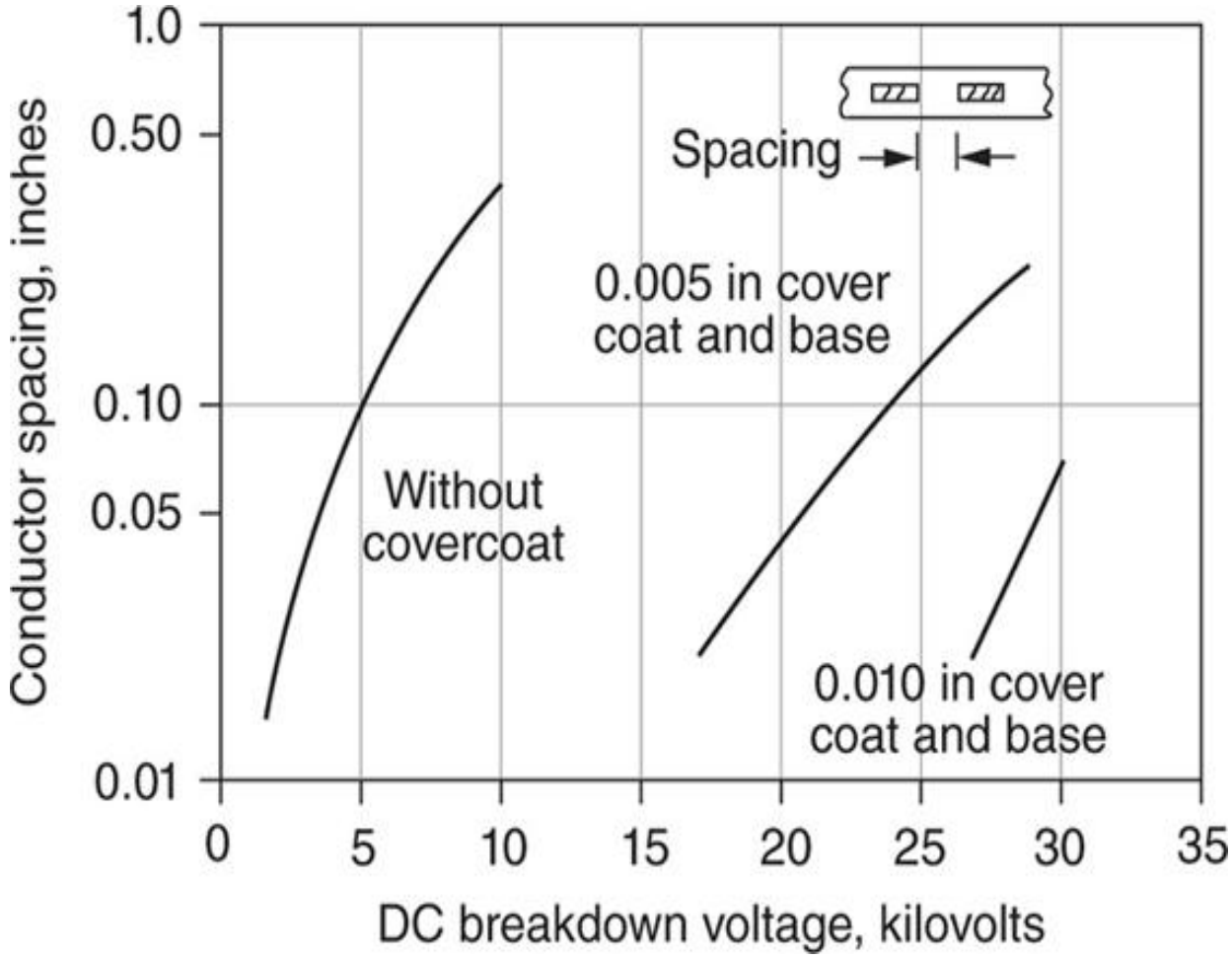


FIGURE 66.22 Breakdown voltage between insulated conductors. (*Sanders Associates*.)

66.5.3 Determination of Conductor Size

The size of a conductor for a given printed wiring application is based upon the following parameters:

- Current-carrying capacity
- Conductor resistance
- Maximum allowable temperature rise in conductor
- Derating effect of multiple conductors in same wiring
- Effects of mounting on current-carrying capacity

- Fusing current
- Capacitance

66.5.4 Capacitance

Capacitance between adjacent conductors consists of both parallelplate capacitance C_P and fringing capacitance C_r, as shown in Fig. 66.23. Parallel-plate capacitance is generally negligible, since the conductors are very thin and thus have small areas opposing each other. Fringing capacitance is therefore the principal form of distributed capacitance between adjacent conductors in flexible printed wiring. Since some portion of the fringing field (usually about half) extends into the air outside the thin insulation, calculation of exact capacitance depends on thickness and dielectric constant of the insulation, dielectric constant of the surrounding medium, widths and thicknesses of the conductors, spacing of the conductors, presence of nearby grounds, and frequency (dielectric constants change with frequency).

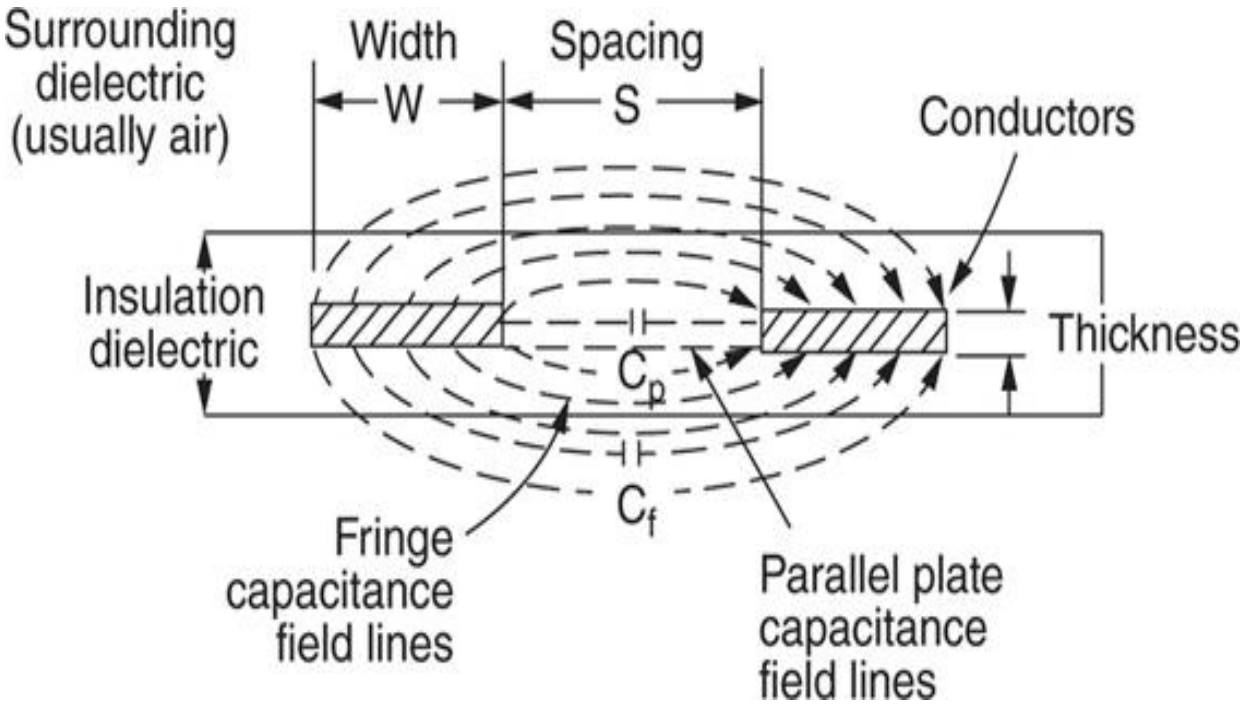


FIGURE 66.23 Distributed capacitance between conductors is and that of air. The capacitance fringing C_f capacitance.

Actual measurements are required to obtain accurate capacitance values. However, distributed capacitance can be roughly examined by establishing a dielectric constant of "median value," which falls between that of the insulating material values calculated by using that approximation serve as guidelines to the distributed capacitance which will actually exist in a given circuit configuration. The results of such a calculation are shown in Fig. 66.24. The capacitance per foot at l kHz between two conductors in flexible printed wiring insulated with 0.005 in of polyester is shown. To determine capacitance values for similar flexible wiring with other insulation materials, multiply the values found from Fig. 66.24 by the proper dielectric constant ratio found from Table 66.6. The values shown in Fig. 66.24 assume a conductor pair free from the influence of other surrounding conductors or ground planes.

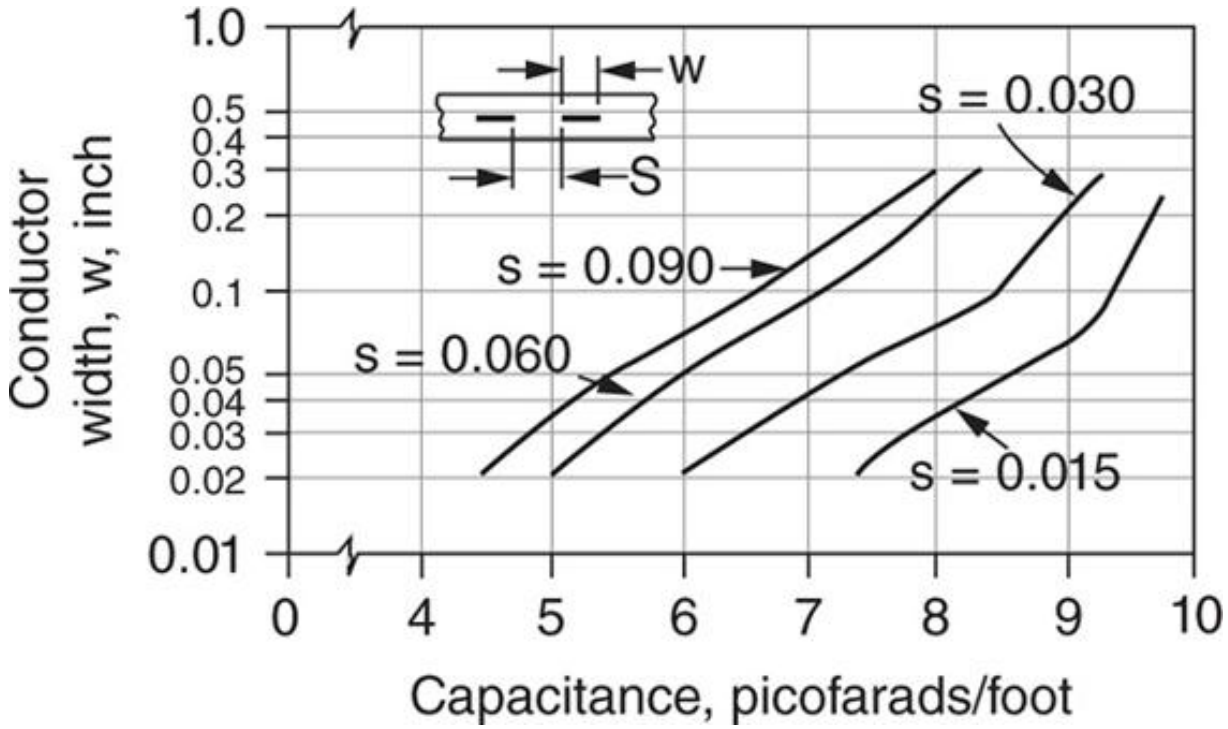


FIGURE 66.24 Calculated capacitance between two adjacent parallel conductors insulated with 0.005 in of Kel-F or polyester (heat sealable); calculated for 2-oz conductor at 1 kHz.

TABLE 66.6 Ratio of Dielectric Constants

Polyester	1.0
FEP Teflon	0.90
Polyethylene	0.93
Vinyl (PVC)	1.4
Polymide (Kapton)	1.21

In practice, the isolation shown in Fig. 66.25*a* is seldom encountered, and measurements made between two conductors "guarded" by two other grounded conductors, in *b*, show capacitance values reduced by approximately 20 percent from those found by using

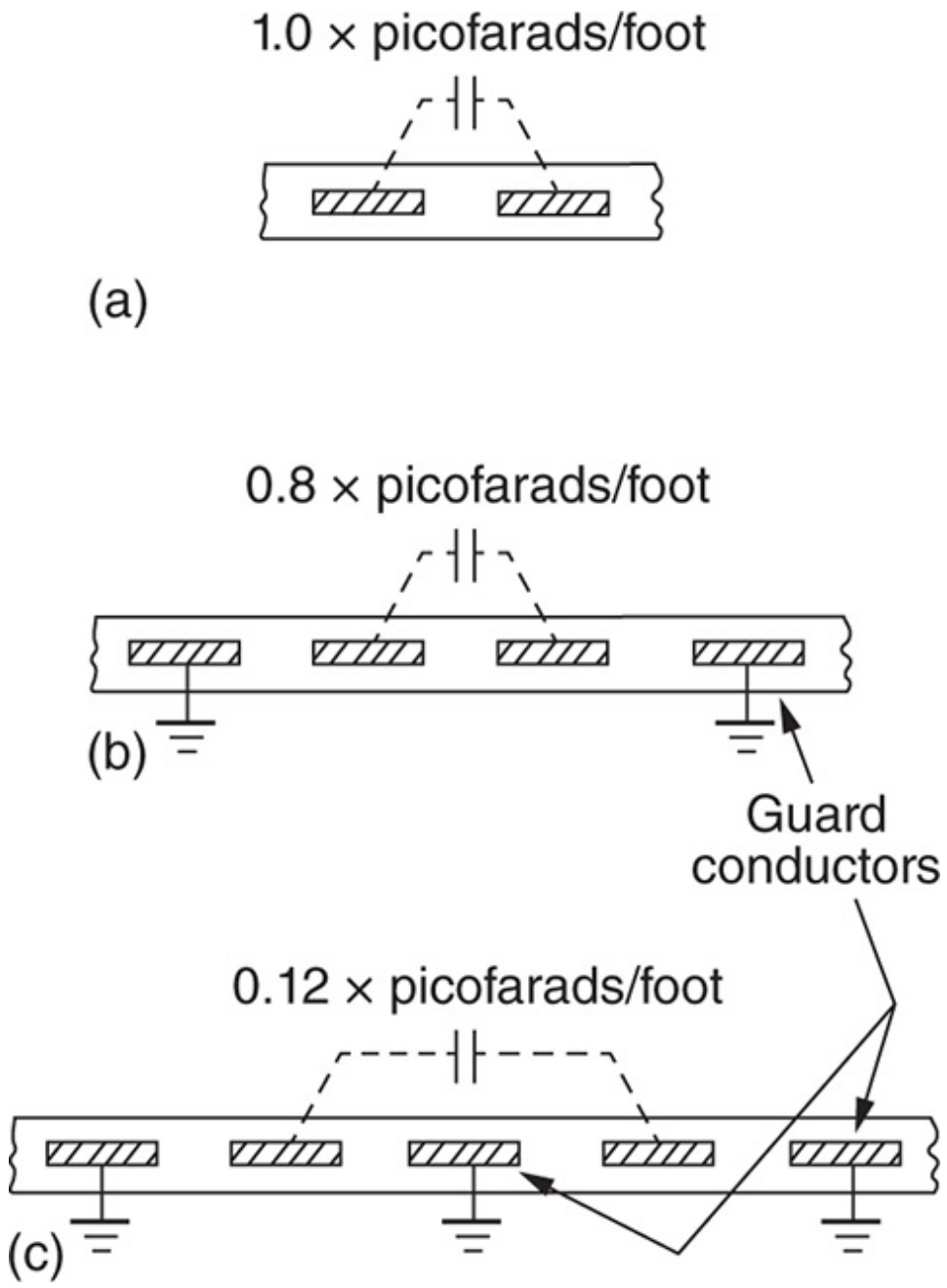


FIGURE 66.25 Typical conductor shielding effect resulting from “guarding” by adjacent grounded conductors: (*a*) no guard conductors, (*b*) peripheral guard conductors, (*c*) interspersed and peripheral guard conductors.

The reduction occurs because some of the fringing flux lines normally joining the measured conductors now terminate on the surrounding grounded conductors and therefore do not contribute to the measured value. Capacitance between two conductors was even more

drastically reduced (about 85 percent) when a grounded conductor was placed between the conductors and grounded conductors also were placed on either side (Fig. 66.25*c*). If the guard conductors of *b* and *c* are floating rather than grounded, capacitance between the measured pair will increase slightly. That situation is seldom encountered in practice, since conductors other than spares usually are not floating.

For some applications it is desirable to find the capacitance between two flat conductors which are completely enclosed by the insulation and have and have their wide surfaces facing each other. Figure 66.26 illustrates the geometry of the problem. Capacitance in that case can be found using one of the two following relations:

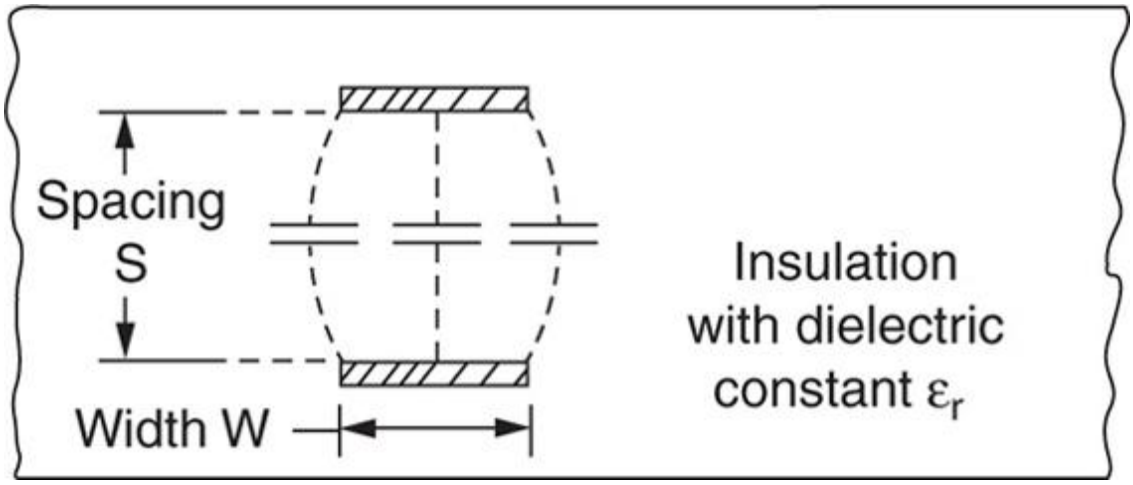


FIGURE 66.26 Capacitance between two conductors with large surface opposing is largely parallel-plate capacitance.

For $\frac{w}{s} < 1$

$$C_{\text{total}} = \frac{3.68\varepsilon_r}{10_{10}\left[\frac{45}{w}\right]} \quad \text{pF/ft}$$

where w = width, ft
s = dielectric separation between conductors, ft
C = capacitance, pF/ft
ε_r = effective dielectric constant

In this case, the result will be approximately 2 percent higher for w/s <1/2 and approximately 10 percent high for w/s = 1

For w/s > 1

$$C_{\text{total}} = 2.7\frac{w}{s}\varepsilon_r x\left[1+\frac{s}{\pi\omega}\left(1+2.303\log_{10}\frac{2\pi\omega}{s}\right)\right] \text{pF/ft}$$

In this case, the result will be approximately 4 percent low for w/s = 2 and approximately 10 percent low for w/s = 1.

For w/s > 1

$$C_{\text{total}} = 2.7\frac{w}{s}\varepsilon_r x\left[1+\frac{s}{\pi\omega}\left(1+2.303\log_{10}\frac{2\pi\omega}{s}\right)\right] \text{pF/ft}$$

In this case, the result will be approximately 4 percent low for w/s = 2 and approximately 10 percent low for w/s = 1.

Figure 66.27 is an approximate guideline to the capacitance between two flat conductors which are exposed to air on either side of a dielectric layer. Capacitance of flat conductors to surrounding metallic shields and/or ground

planes is shown in Fig. 66.28 for standard flexible printed wiring using FEP Teflon insulation.

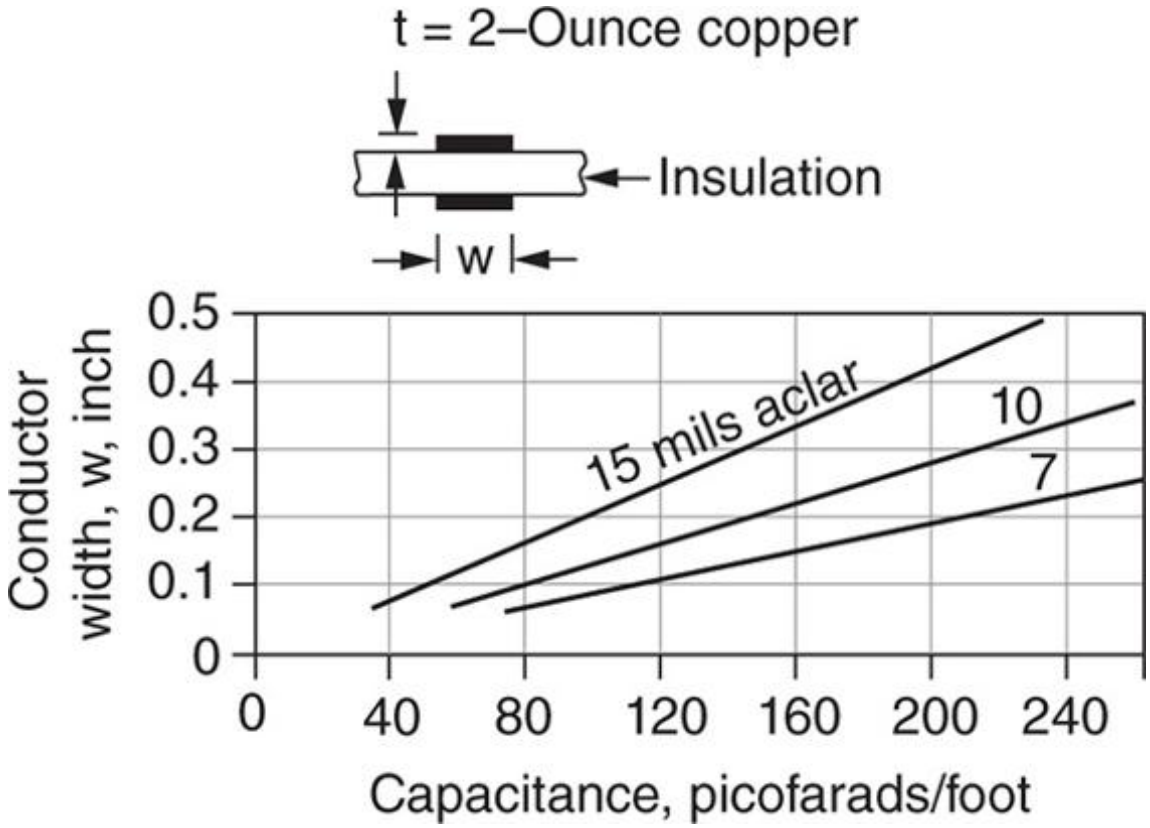


FIGURE 66.27 Typical capacitance at 1 MHz between two flat conductors exposed to air on either side of a dielectric layer.

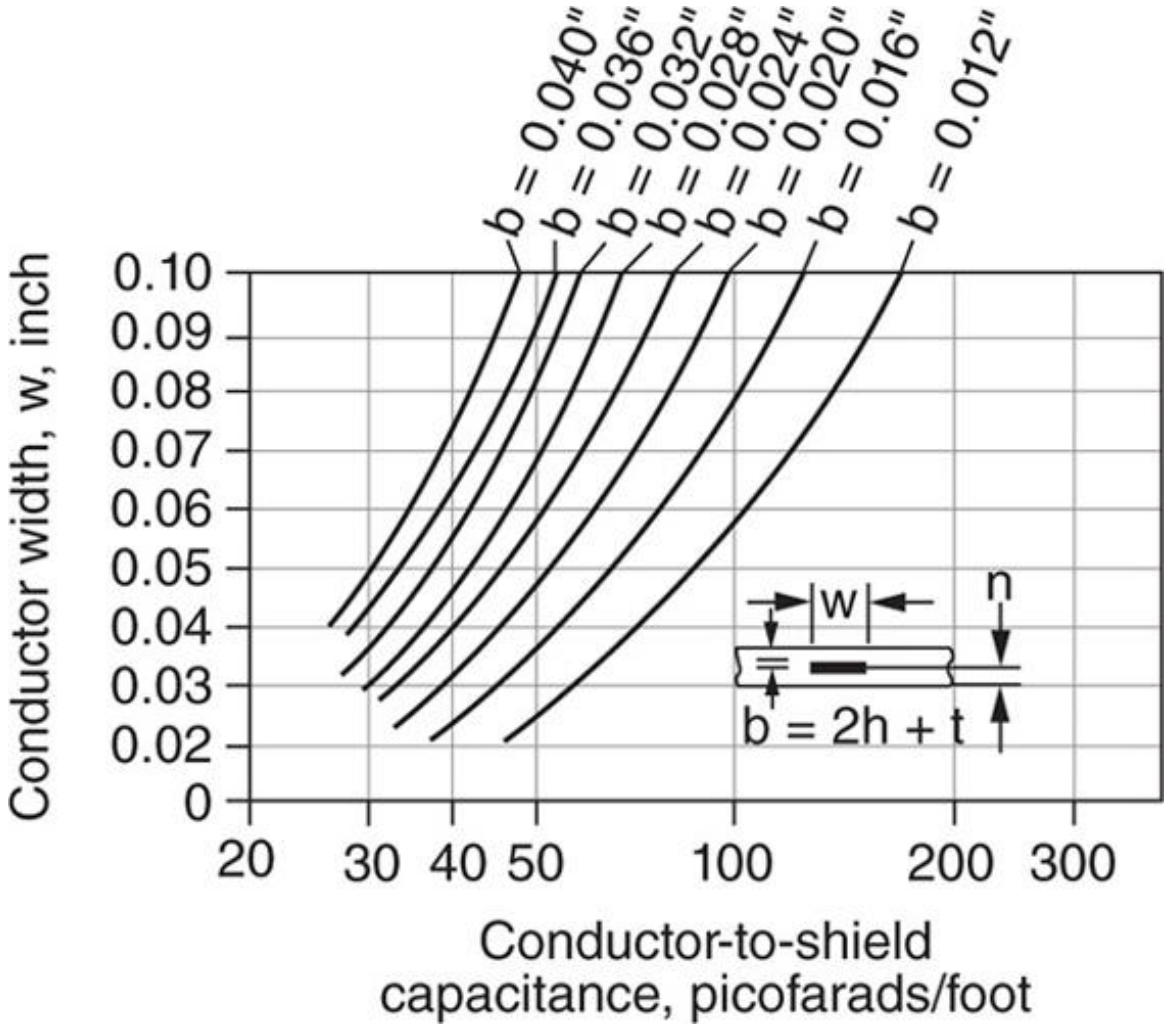


FIGURE 66.28 Typical conductor-to-shield capacitance for 2-oz copper conductor insulated with FEP Teflon.

66.6 DESIGN OF FLEXIBLE PRINTED WIRING WITH TRANSMISSION LINE PROPERTIES

Flexible printed wiring has found widespread use in transmission line applications either as a replacement for coaxial wires or in initial designs of high-speed circuits. With the advent of LSI devices the use of printed wiring with transmission line properties has increased manyfold. This

section will provide the designer with sufficient data to effectively design flexible printed wiring with transmission line properties.

The Institute of Printed Circuits defines and explains the term “transmission line” as follows: “‘Transmission line’ is one signal-carrying circuit composed of conductors and dielectric material with controlled electrical characteristics used for the transmission of high-frequency or narrowpulse type signals.”

Transmission lines are a group of electrical interconnections on an organic base which are used in highfrequency applications, usually above 50 MHz. In such circuitry the interconnecting metallic conductor is acquiring additional electrical characteristics and acts as the transmission line waveguide.

Two types of such transmission line configurations are utilized: “microstrip,” in which the conductor is located above a single ground plane (Fig. 66.29*a*) and “strip-line” in which the conductor is located centrally between two ground planes (Fig. 66.29*b*). Important parameters of such conductors are line width, dielectric separation to ground plane, and dielectric constant of the insulating materials, all of which determine the impedance, signal propagation, and cross-talk characteristics of the lines. The following parameters govern the design of flexible printed wiring transmission line devices.

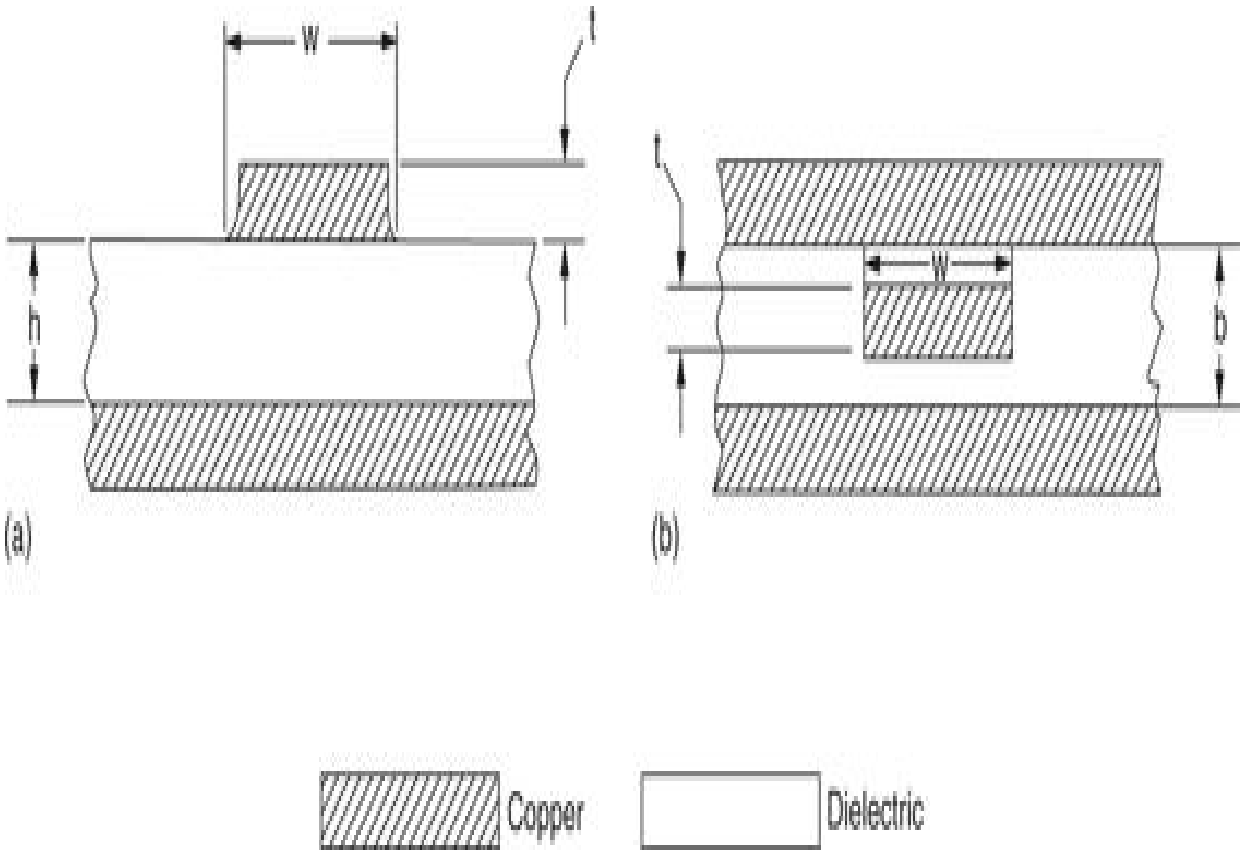


FIGURE 66.29 Printed wiring transmission line configurations.

Characteristic impedance The single and most important electrical parameter in determining the performance of high-speed circuits is the characteristic impedance of the conductors. If Z_0 is controlled, signal reflections which result from the passage of fast pulses through an impedance discontinuity or mismatch at the load end of the line will be avoided. The characteristic impedance is dependent upon the conductor line width *w*, dielectric thickness *h* or *b*, conductor thickness, dielectric constant of the insulating medium, and the configuration (microstrip or strip-line) of the device. The general equation for characteristic impedance of any high frequency transmission line is as follows:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

where Z_0 = impedance, Ω
R = resistance per unit length of line
L = inductance per unit length of line
G = conductance per unit length of line

$$\omega = 2\pi f$$

C = capacitance per unit length of line

If the line is lossless, the equation is simplified:

$$Z_0 = \sqrt{\frac{L}{C}}$$

66.6.1 Microstrip Configuration

A specific formula for microstrip is the following:

$$Z_0 = \frac{h}{w}\frac{377}{\varepsilon_r}$$

where *h* and *w* are given in the diagram and *is* the effective dielectric constant of the material (considering the effect of air). This analytical method disregards fringing effects and leakage flux and gives validity to the notion that more reliable values may be obtained by measurement. To account for the fringing effects of microstrip transmission

line, and if the analytical method must be used, the following formula is recommended:

$$Z_0 = \frac{h}{w} \frac{377}{\sqrt{\varepsilon_r}\ [1+(2h/\pi\omega)(1+\ln \pi\omega/h)]}$$

If the microstrip line is embedded or covercoated as shown in Fig. 66.30, the Z_0 values will be reduced by approximately 22 percent. Typical values of Z_0 for microstrip fabricated of an epoxy glass base material having a dielectric constant varying from 6 at 1 kHz to 5 at 25 MHz when conductors are exposed to air, are given in Fig. 66.31.

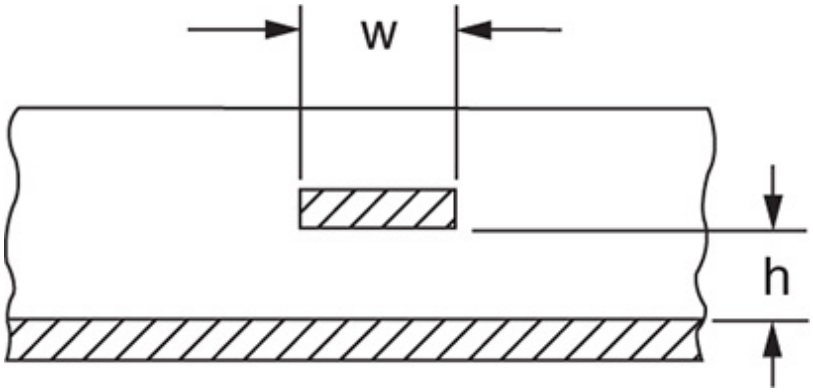


FIGURE 66.30 Schematic representation of embedded or cover-coated microstrip FPW.

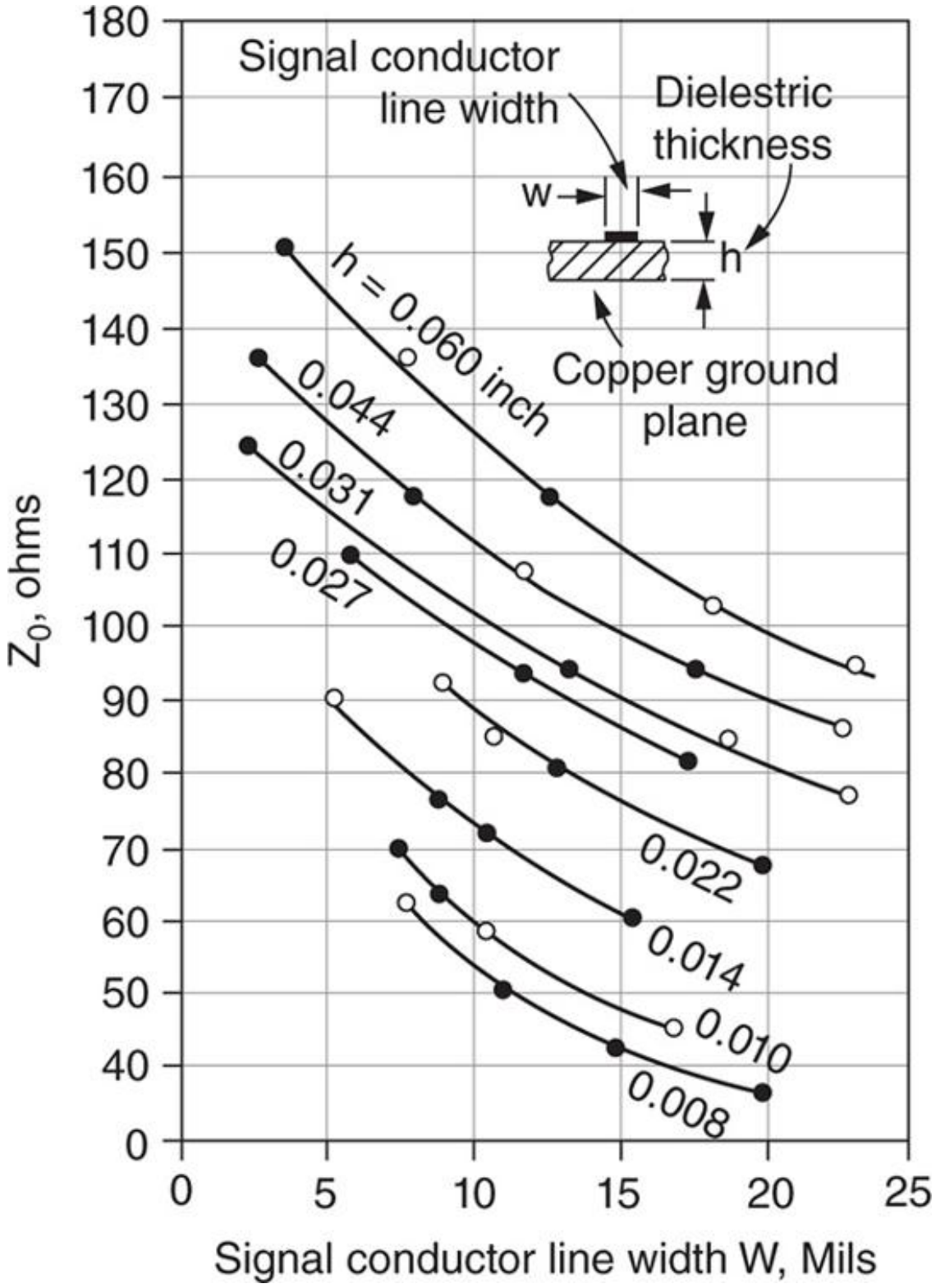


FIGURE 66.31 Characteristic impedance (Z_0 of microstrip wiring as a function of line width *w* and dielectric thickness *h*. Conditions: (1) 2-oz copper conductors; (2) measurement made at 26°C (room temperature) and room humidity; (3)

board material dielectric constant relatively stable with frequency varying from about 6 at 1 kHz to about 5 at 25 MHz.

66.6.2 Strip-Lines

The characteristic impedance Z_0 of strip transmission line when $w/b >> 0.35$ can be determined by the following relation:

$$Z_0 = (60/\sqrt{\varepsilon_r})[\ln(4b/d_0)]$$

where d_0, the effective *wire* diameter for square configuration, is $0.567w + 0.67t$.

Representative values of Z_0 for microstrip and strip-line transmission line wiring are presented in Fig. 66.32. The use of curves to determine strip-line parameters is preferred over the more cumbersome methods of calculation. A family of curves that has proved to be very useful for that purpose is shown in Fig. 66.33. It is applicable to a wide range of copper thicknesses.

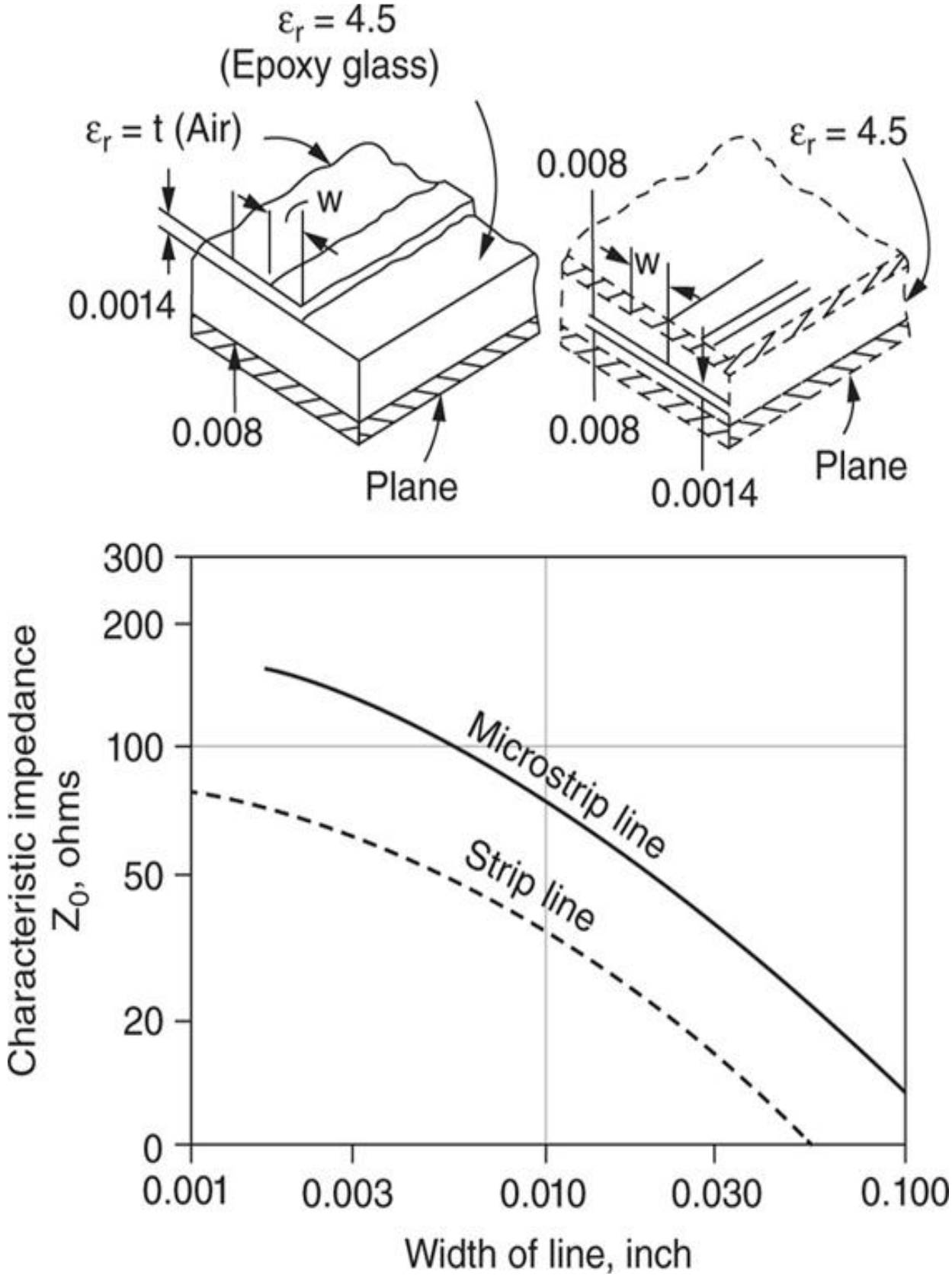

ε_r = 4.5
(Epoxy glass)
ε_r = t (Air)
w
0.0014
0.008
Plane
0.008
ε_r = 4.5
w
0.008
0.0014
Plane
300
200
100
50
20
0
Characteristic impedance
Z_0, ohms
Microstrip line
Strip line
0.001
0.003
0.010
0.030
0.100
Width of line, inch

FIGURE 66.32 Characteristic impedance Z_0 comparison of microstrip and stripline transmission line wiring devices.

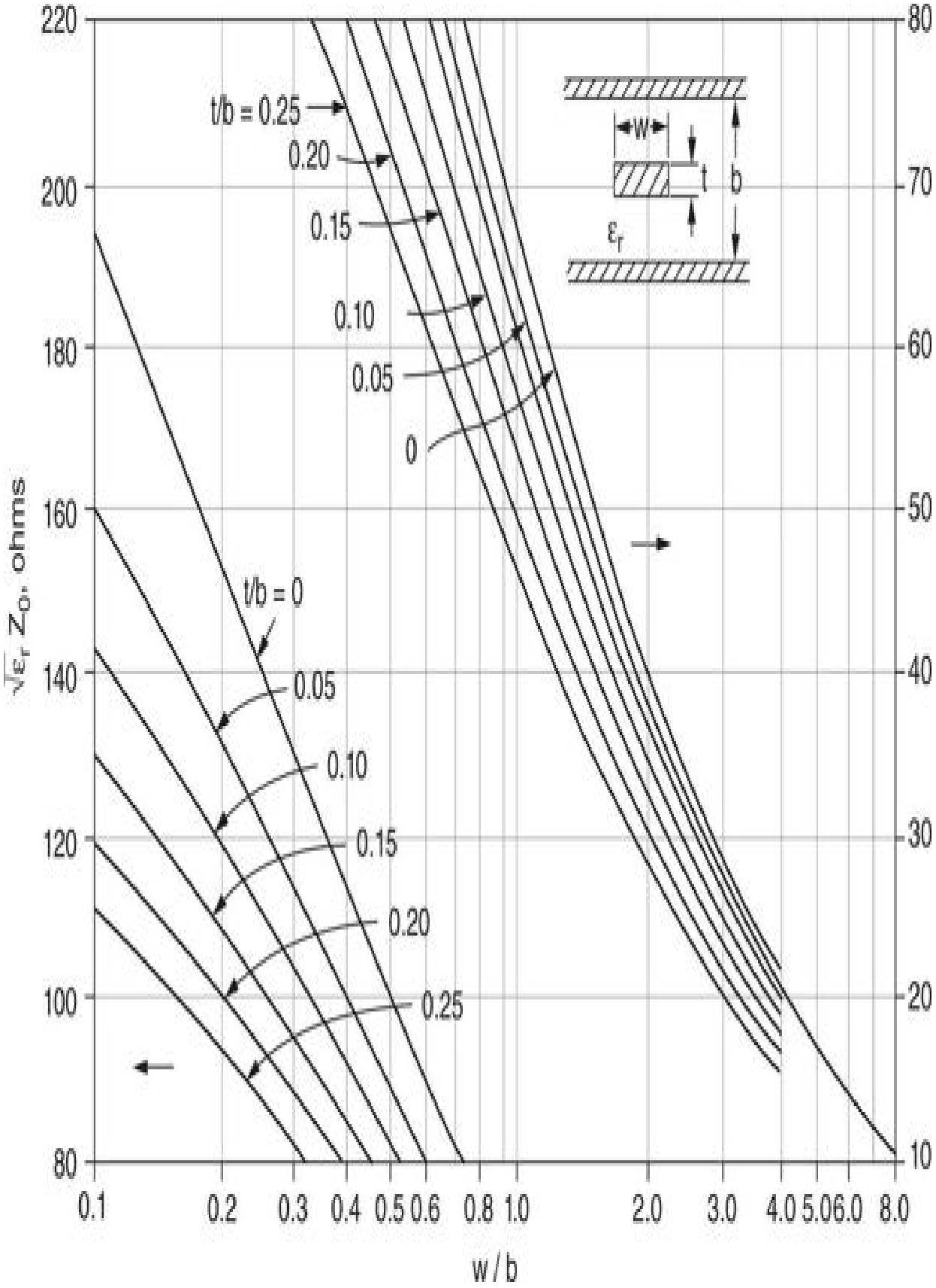

220
200
180
160
140
120
100
80
80
70
60
50
40
30
20
10
t/b = 0.25
0.20
0.15
0.10
0.05
0
t/b = 0
0.05
0.10
0.15
0.20
0.25
w
t
b
ε_r
$\sqrt{\varepsilon_r}\ Z_0$, ohms
0.1
0.2
0.3
0.4
0.5
0.6
0.8
1.0
2.0
3.0
4.0
5.0
6.0
8.0
w / b

FIGURE 66.33 Graph of Z_0 versus w/b for various values of t/b.

If one were to fix the parameter t at 0.0028 in (2-oz copper), the family of curves could be redrawn to show the relations of w and b for various values of normalized characteristic impedance $\varepsilon_r Z_0$. That family of curves is shown in Fig. 66.34, and it is usable for any insulating material whose dielectric constant is known or measurable.

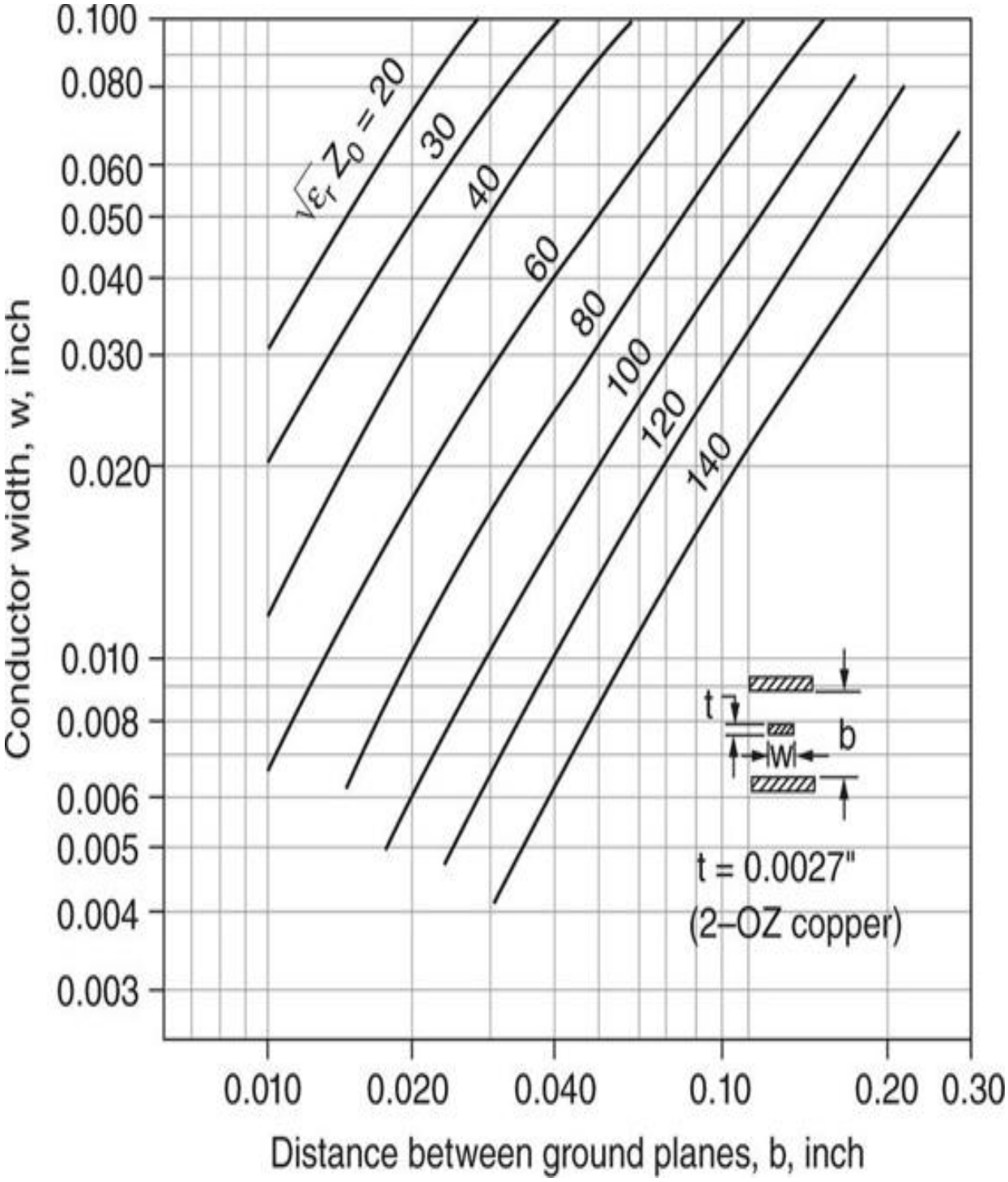


FIGURE 66.34 Normalized impedance $\varepsilon_r Z_0$ as a function of conductor width *w* and dielectric separation *b* in strip-line configuration.

Specific Example: The following exercise is presented to familiarize the designer with the use of the curves in the

solution of a typical design problem given these conditions:

Flexible printed wiring, cover coated
$Z_0 = 75\ \Omega$
Overall thickness = 0.062 in
Material = Teflon, $\varepsilon_r = 2.1$

Determine the proper curve in the family. Since the material has been designated as Teflon with an ε_r of 2.1, the suggested curve would be $\varepsilon_r Z_0 = 110$.

Determine dielectric separation b. Knowing that the overall thickness should not exceed 0.062 in, the value of b should be set at 0.050 in. The number is based upon the difference between the overall thickness and the expected thickness of the two ground shields and two cover-coated layers.

Determine conductor width w. The value of w as read from the graph is 0.017 in.

The construction of the strip-line in this hypothetical case is shown in Fig. 66.35. The spacing between conductors is determined by FPW width, electrical parameters, and processing limitations.

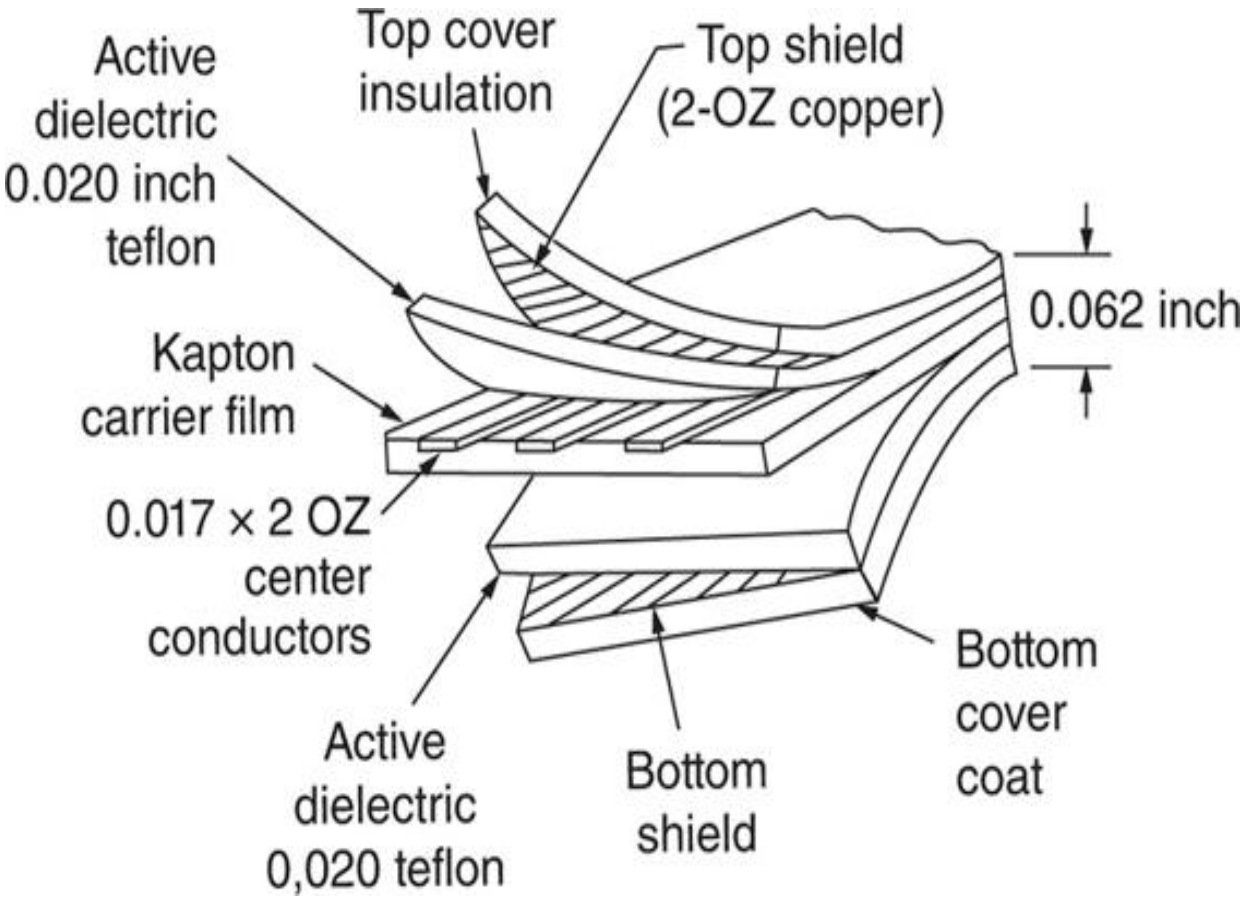


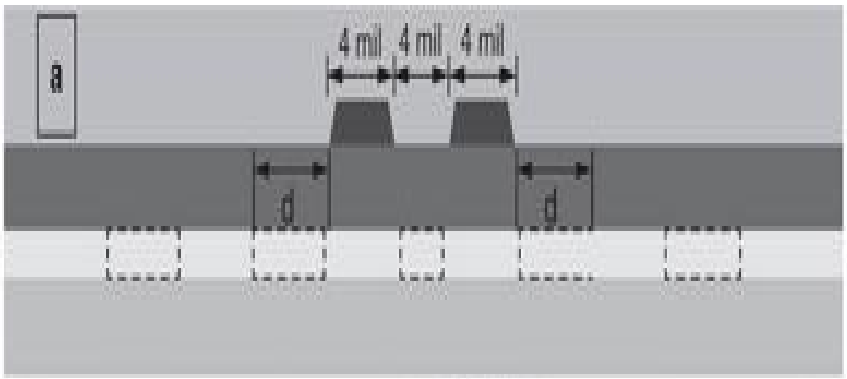
FIGURE 66.35 Seventy-five ohm strip-line flexible printed circuit device.

66.6.3 Special Transmission Lines for Flexing

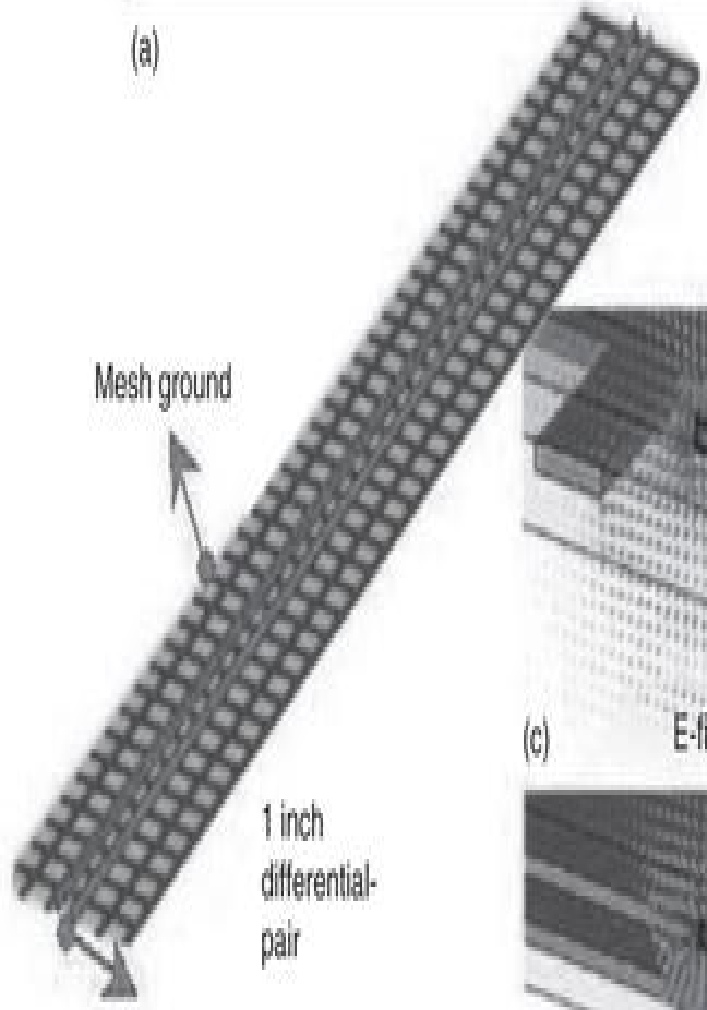
Three high-speed differential transmission line configurations are available:

1. Edge-coupled differential microstrip with mesh GND
2. Coplanar differential microstrip w/o opposing GND
3. Broadside coupled differential microstrip w/offset GND

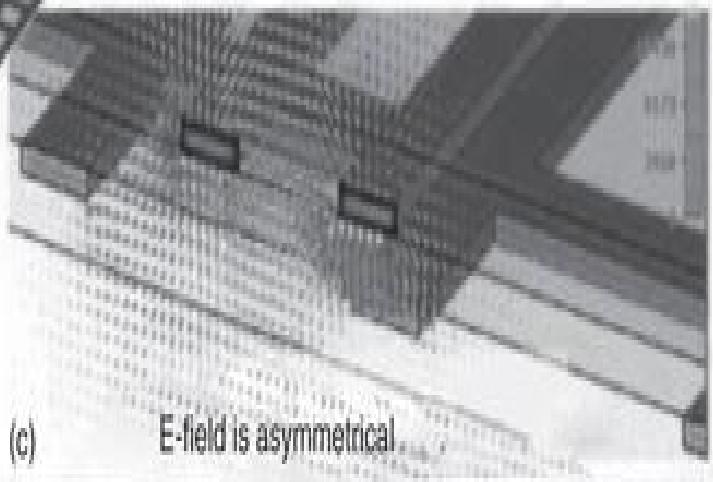
1. Edge-coupled differential microstrip with mesh GND is very common. Figure 66.36 shows a closer view of the mesh GRN and the E-fields.



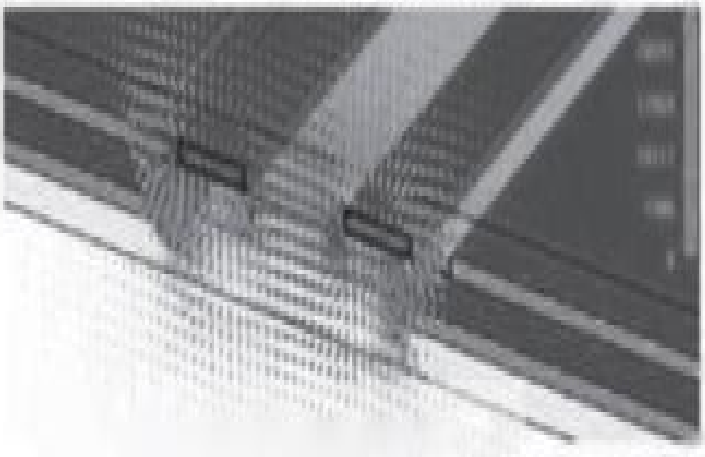
(a)



(b)



(c) E-field is asymmetrical



(d) E-field is symmetrical

FIGURE 66.36 (*a*) Mesh GND differential microstrip; (*b*) a 1.0-in simulated transmission line; (*c*) unbalanced E-field from asymmetrical spacing to Mesh; (*d*) symmetrical E-field from balanced Mesh.

2. Coplanar differential microstrip w/o opposing GND is also popular but has its reference plane enlarged under the active differential lines (as seen in Fig. 66.37).

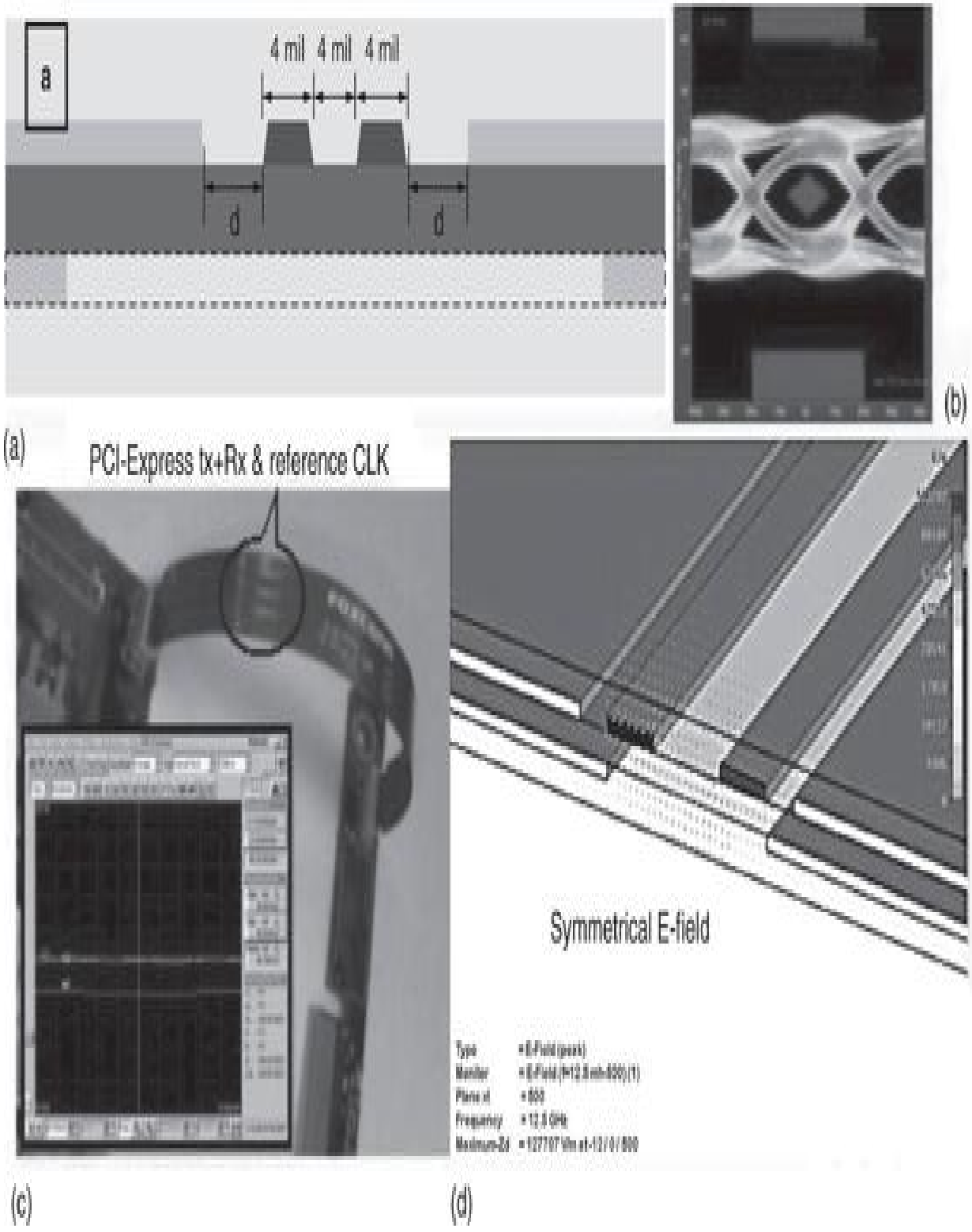
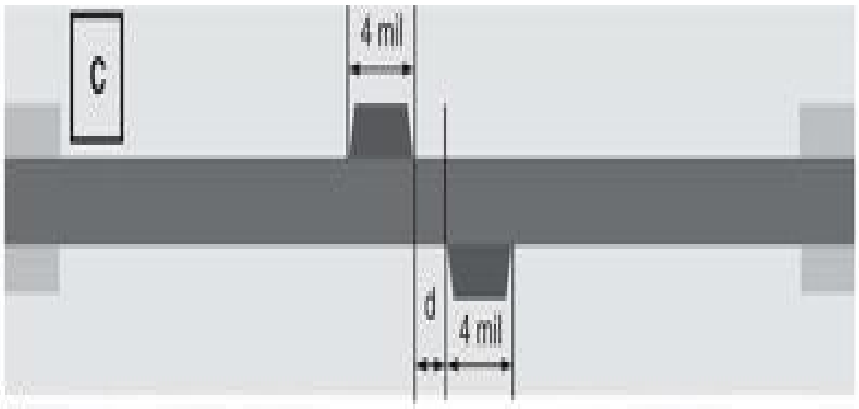
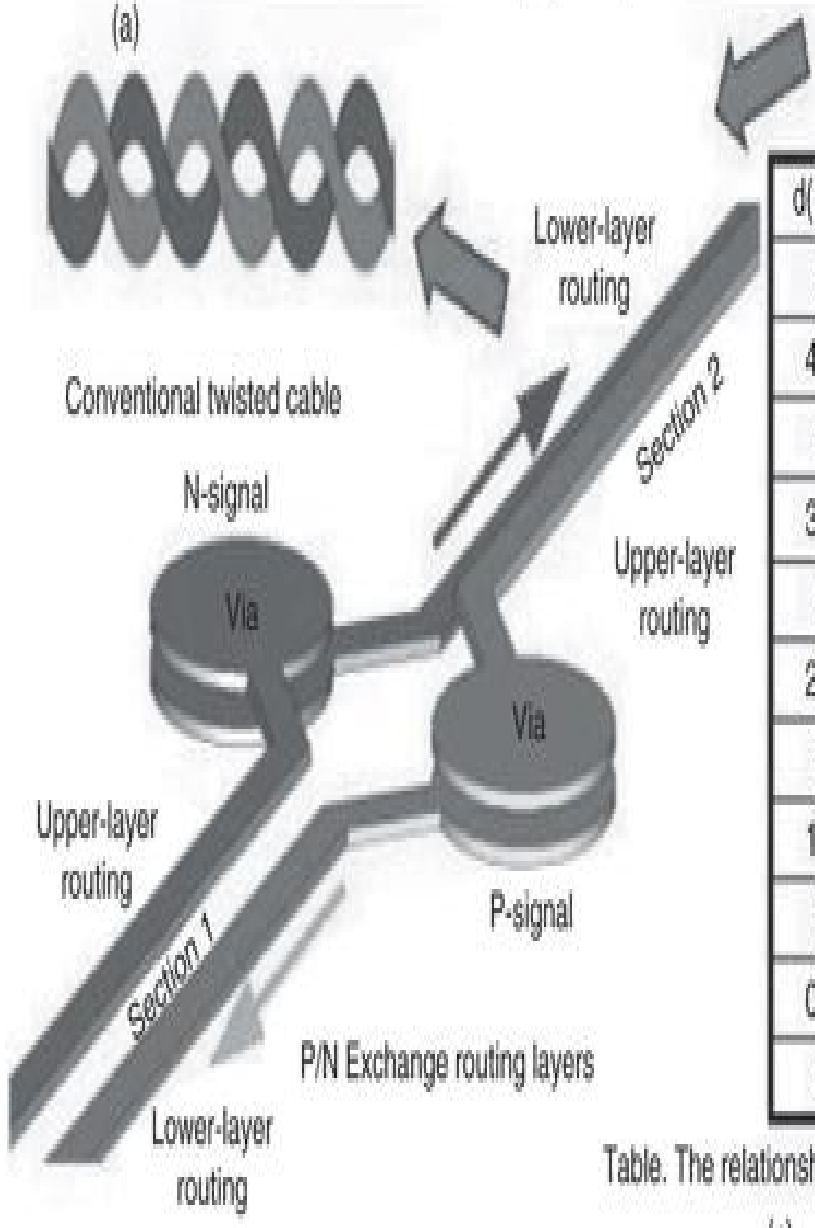


FIGURE 66.37 (*a*) Structure of a coplanar transmission line without bottom GND; (*b*) eye-diagram for PCI-Express transmission line in *c*; (*d*) simulation of the symmetrical E-field for this “relieved” coplanar diff. microstrip.

3. Broadside coupled differential microstrip w/offset GND has its copper plane moved back from the flexing section but “flips” its signal traces from side-to-side like a twisted pair (Fig. 66.38).



(a)



(b)

d(mil)	Zdiff (Ohm)
5	120.847
4.5	116.744
4	112.339
3.5	107.789
3	103.115
2.5	98.337
2	93.298
1.5	88.198
1	82.83
0.5	77.564
0	72.096

Signal interfaces

- 1394(110 Ohm)
- PCI-Express genl (100 Ohm)
- USB 2.0 (90 Ohm)
- PCI-Express Gen2 (85 Ohm)

Table. The relationship of offset distance d and Zdiff.

(c)

FIGURE 66.38 New design with offset broadside-coupled differential transmission line: (*a*) structure, (*b*) relationship of the offset distance (d) and resulting impedance (Z diff.), (*c*) new design scheme: change the offset distance (d) of the P/N signal lines on different layers to match the requirement of the target impedance.

66.6.4 Electrical Parameters

Capacitance *C* for double-sided wiring is determined by the formula:

$$C = \frac{0.2249}{d}\varepsilon_r A$$

where C = capacitance, pF/in
ε_r = dielectric constant relative to air = 1
A = area of smallest electrode, in^2
d = thickness of dielectric, in

Under normal conditions, lines that are parallel and are separated by 0.062 in on 0.062-inthick epoxy glass ($\varepsilon_r = 5$) will have a capacitance of 0.5 pF/in. Corresponding wiring fabricated from Teflon will have a *C* of 0.3 pF/in.

In multilayer boards, capacitance is calculated by a different formula, although the conductors are still capacitively coupled when they physically approach each other in the horizontal or vertical direction. An approximate value for the amount of capacitive coupling may be calculated by the equation:

$$C = \frac{w\varepsilon_r}{h4.45}$$

where ε_r = effective dielectric constant
h = height, in $\times 10^{-3}$
w = width, in $\times 10^{-3}$

for the configuration shown in Fig. 66.39.

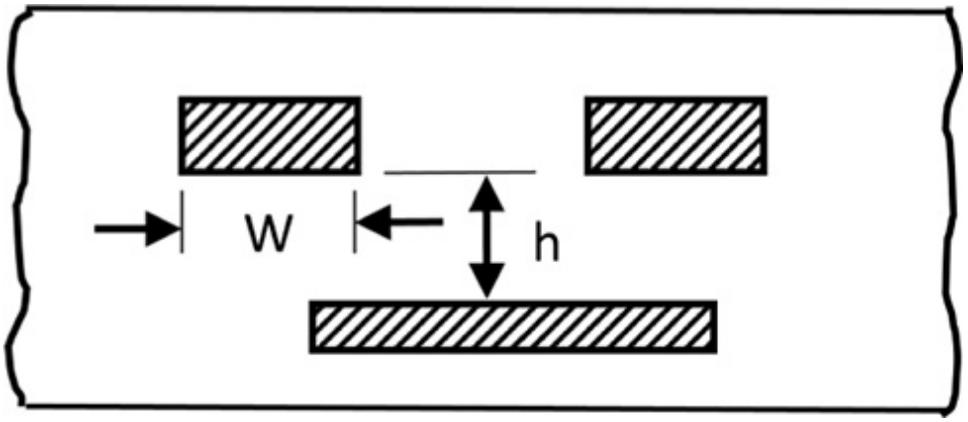


FIGURE 66.39 Schematic of multilayer printed circuit.

Microstrip may be used as a single wiring layer or the outside layer of a multilayer board. Strip transmission line may be used either as one or a multitude of wiring layers. Capacitance of strip transmission line can be approximated by the equation:

$$C = 0.9 \frac{w/b}{1-(t/b)} \varepsilon_r$$

66.6.4.1 Time Delay. The delay in the signal propagation velocity in microstrip line can be calculated using the formula:

$$T_d = 1.015\sqrt{\varepsilon_r} \text{ ns/ft}$$

where T_d is time delay per unit length of conductor and ε_r is effective dielectric constant of the transmission line or the dielectric constant of the board's dielectric if the conductor is embedded.

The equation is valid only when the conductor's capacitance is greater than the load capacitance that results when switching circuits are added to the line. Embedding microstrip lines, as in multilayer printed wiring, makes the circuit appear "electrically larger." That is, a signal takes longer to travel a given distance in the embedded line than in the unembedded or pure microstrip line. Therefore, embedding the lines means that critical wiring lengths must be reduced 22 percent to maintain the same time delay (length embedded = 0.78 × length unembedded). It is apparent that line delays may approach circuit delays. Figure 66.40 shows graphically the relation between circuit and line delays. The solid lines represent circuit delays and the broken lines represent percents of logic delays: 10, 20, 30, 40, and 50 percent. For a required maximum total delay and a given logic delay, the maximum line length can be determined.

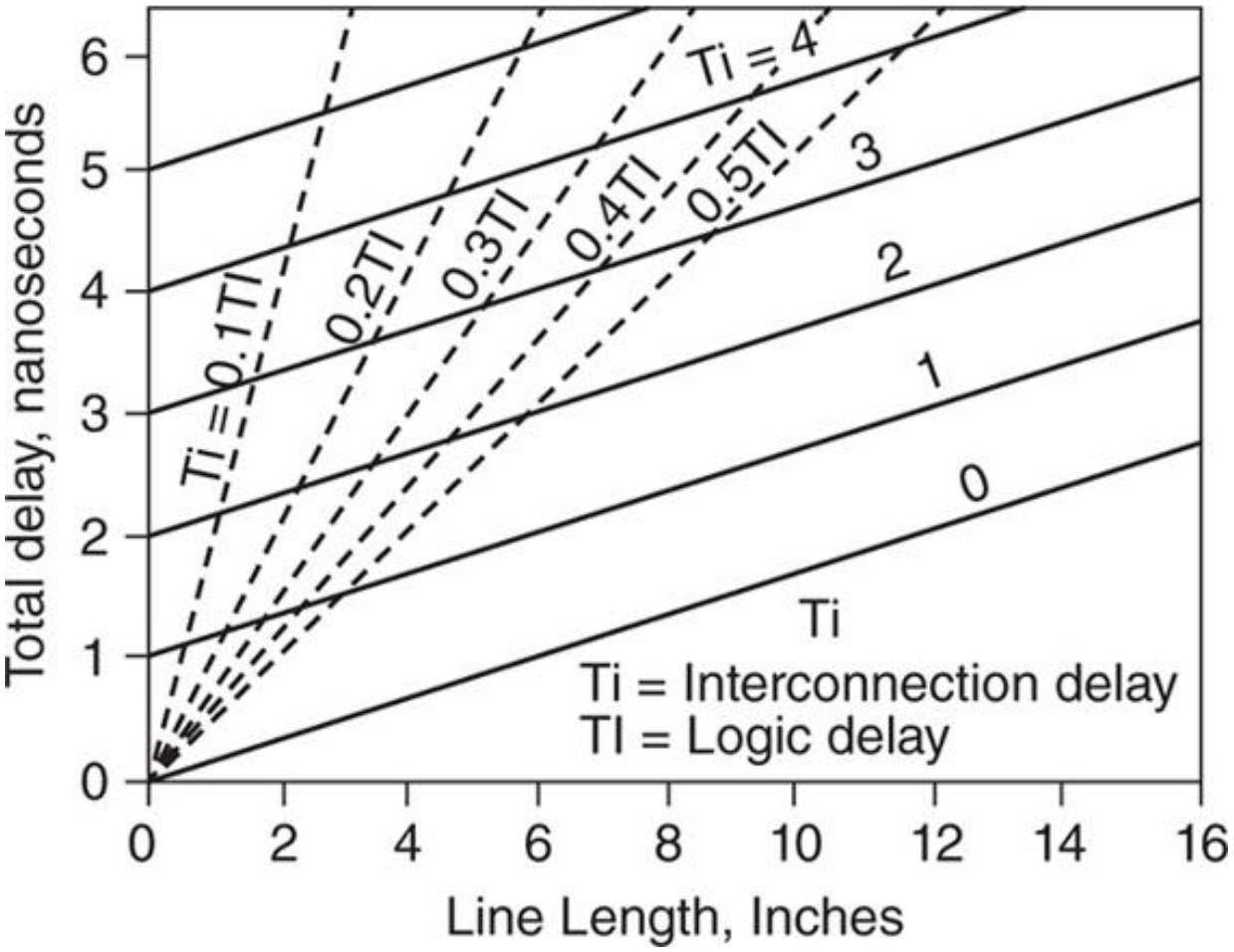


FIGURE 66.40 Interconnection delay and logic delay versus length for a dielectric of 4.5.

66.6.4.2 Cross Talk. Cross talk is the undesirable coupling of energy between signal paths. The unwanted transfer of energy between lines results from the capacitive and inductive coupling of the lines and is a function of length of the lines, space between the lines, and the dielectric constant. The phenomenon is often a limiting factor in high-speed digital systems in which coupling between lengths of parallel lines may be the only alternative to the high wiring density which is required. Cross talk between an active line, that is, the line carrying the voltage pulse, and a passive line in the vicinity places a spurious pulse on the passive line. If the latter pulse is of sufficient amplitude, it could falsely switch circuits on the passive line. Traditionally, before cross

talk could be calculated it was necessary to calculate or measure mutual inductance, mutual capacitance, propagation velocity, and impedance of the lines. Analytical methods are unwieldy because of the effect of air on the dielectric constant and the uncertainty of fringe field effect. A method that is now available depends only on the geometric cross section of the lines and is independent of time, length, and voltage.

For the case of microstrip, then, induced voltage values due to cross talk may be calculated by use of the formulas:

$$V_B(t) = K_S\left[V_i(t) - V_i(t - 2l\sqrt{LC})\right]$$

$$V_F(t) = K_F l \frac{dV_i}{dt}(t - l\sqrt{LC})$$

where l = length of coupled region

V_B = induced backward voltage as seen at the ends of the coupled region

V_F = induced forward voltage as seen at the ends of the coupled region

V_i = input voltage

K_S = backward cross-talk constant

K_F = forward cross-talk constant

t = time, ns

K_B is always positive with respect to the driving signal; K_F is negative for microstrip and will be zero for homogeneous dielectric media. To determine cross-talk constants for any system, use line lengths in which $2T_d$ is significantly greater than the rise time and use the following formulas:

$$K_B = \frac{V_B}{V_t} \quad \text{and} \quad K_F = \frac{V_{F\max}}{dV_t/dt_{\max}} \frac{1}{l}$$

where l = length of coupled region
V_B = induced backward voltage
V_F = induced forward voltage
V_t = input voltage

Pulse cross talk is represented by

$$V_B(t) = K_B\left[V_i(t) - V_i(t-1)\sqrt{LC}\right]$$

$$K_B = V_i \qquad K_i = V_i \qquad V_t \rightarrow V_i$$

Empirical values for K_B and K_F are given in Figs. 66.41 and 66.42.

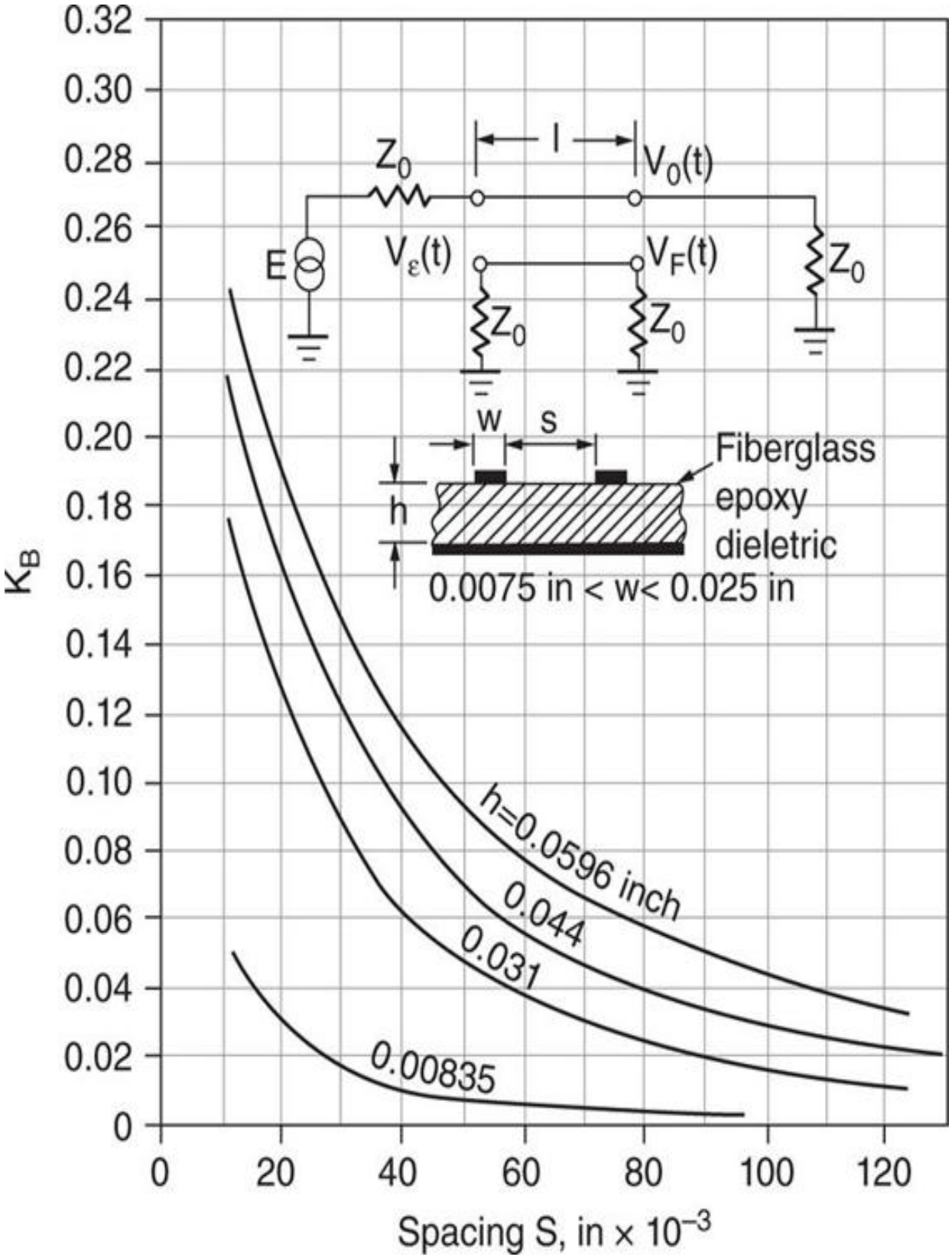

0.32
0.30
0.28
0.26
0.24
0.22
0.20
0.18
0.16
0.14
0.12
0.10
0.08
0.06
0.04
0.02
0
K_B
0
20
40
60
80
100
120
Spacing S, in × 10^{-3}
Z_0
l
$V_0(t)$
E
$V_\varepsilon(t)$
$V_F(t)$
Z_0
Z_0
Z_0
w
s
h
Fiberglass
epoxy
dieletric
0.0075 in < w< 0.025 in
h=0.0596 inch
0.044
0.031
0.00835

FIGURE 66.41 Back cross-talk constant as a function of spacing. Notes: (1) Lines terminated in Z_0, the characteristic impedance of each line. (2) Curves valid for 0.0075 in < W < 0.025 in. (3) Copper weight is 2 oz (0.0028 in). (4) Time delay of line = T_d = 1.8 ns/ft. (5) $V_B(t) = K_B V_0(t + \text{l}t_d - K_B V(t - \text{l}T_d)$.

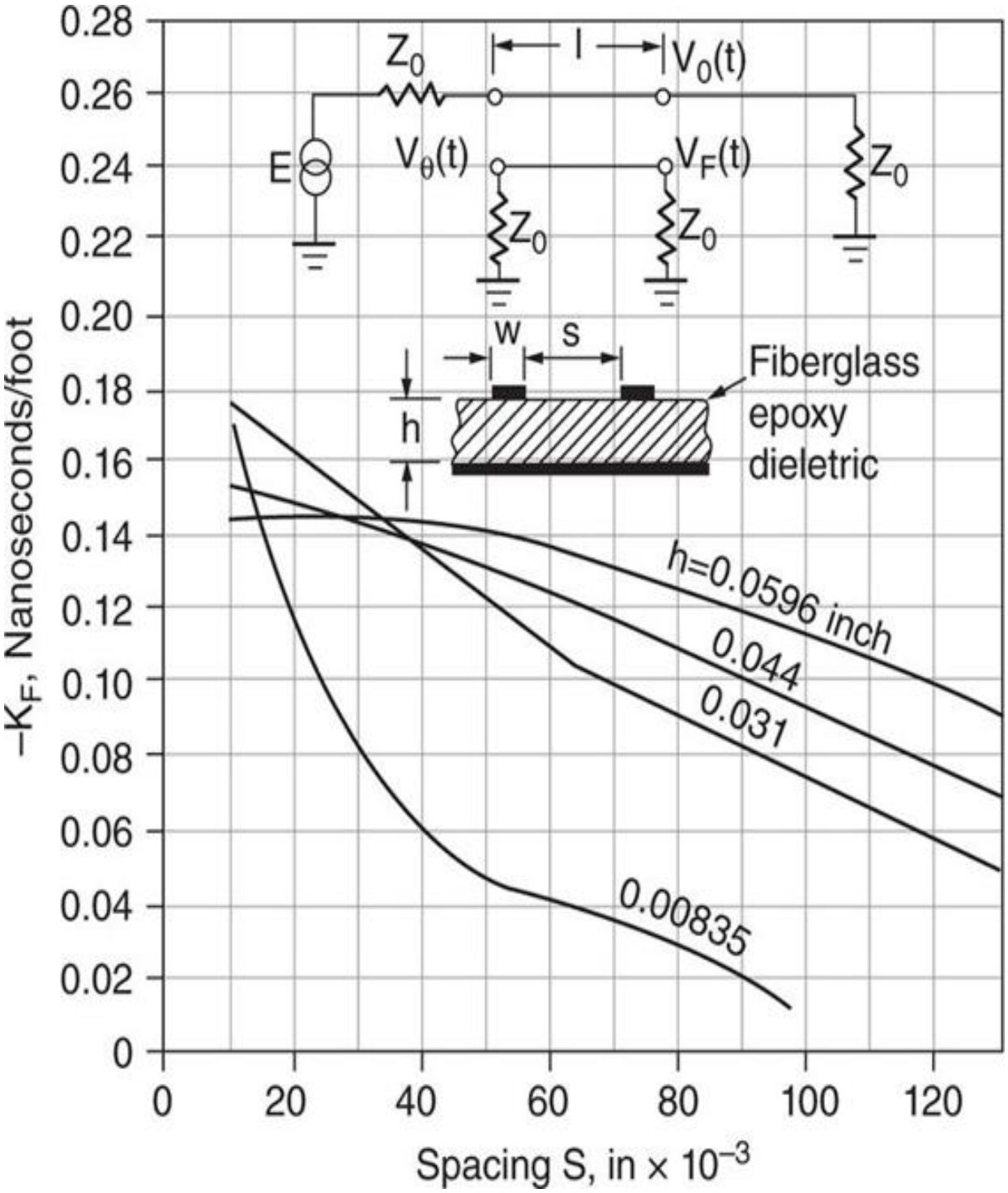


FIGURE 66.42 Forward cross-talk constant as a function of spacing. Notes: (1) Lines terminated in characteristic impedance. (2) Curves valid for 0.0075 in < W < 0.025 in. (3) Copper weight is 2 oz (0.0028 in). (4) Time delay of line = T_d = 1.8 ns/ft. (5) $V_F(t) = K_F\, \mathrm{l}d[V_0(t)]/dt$.

66.6.4.3 Attenuation. Power may be lost in transmission lines by radiation, heating of the conductors, and heating of the dielectric. Heat losses in both the conductor and the dielectric increase with frequency. Conductor losses are greater the lower the characteristic impedance of the cable. The converse is true of dielectric losses. Because of its low impedance, the specified printed wiring has an attenuation higher than that of the most common coaxial cables. Typical data for a frequency range of 1 to 3000 MHz are shown in Fig. 66.43.

Shields	Disturbing Conductors	Grounded Conductors	Sensitive Conductors	Cross Talk: Inductive, μV/A/ft (10 Ω)	Cross Talk: Capacitive, μV/V/ft (5000 Ω)
No shield	1 + 2	—	3 + 4	23	6.9
	1 + 2	3	3 + 4	23	3.4
	1 + 2	4	3 + 4	23	16.8
	1 + 2	—	4 + 5	9	3.0
	1 + 2	3	4 + 5	9	0.4
Shield on one side, 1/16-in Al strip grounded	1 + 2	—	3 + 4	23	2.3
	1 + 2	3	3 + 4	23	0.5
	1 + 2	4	3 + 4	23	5.2
	1 + 2	—	4 + 5	9	0.2
	1 + 2	3	4 + 5	9	0.1
Shields both sides, 1/16-in Al strip Al foil grounded	1 + 2	—	3 + 4	23	0.4
	1 + 2	3	3 + 4	23	0.0
	1 + 2	4	3 + 4	23	0.8

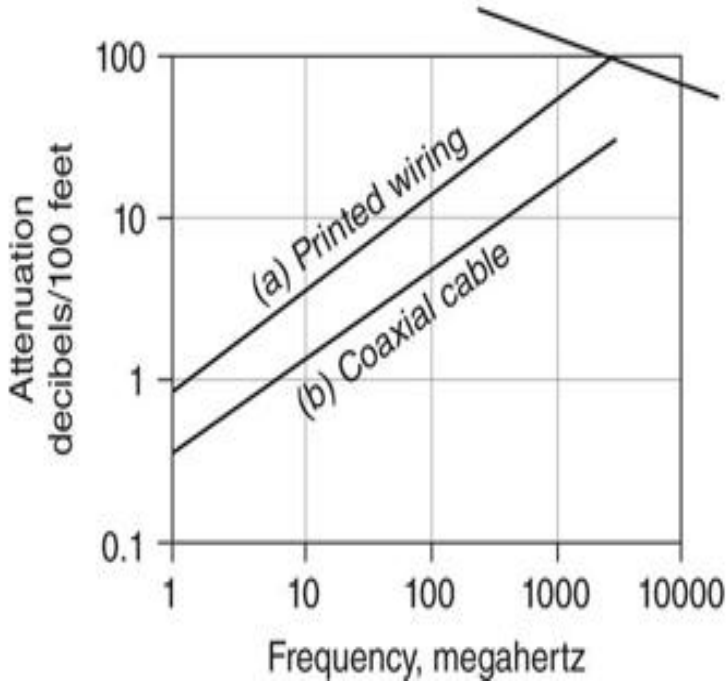


FIGURE 66.43 Attenuation of wiring devices. (*a*) Flexible printed circuits with 0.025 × 0.0027 in copper conductors, spacing between conductors 0.020 in, polyester dielectric 0.003 in thick on top and bottom of conductors, aluminum shield on one side or both sides of the cable. (*b*) Coaxial cable type RG-55/V. (*NASA-MSFC, Huntsville, AL*.)

66.7 CIRCUIT DESIGNS FOR HIGHER RELIABILITY

Because of the thin and fragile materials used, flexible circuits have lower mechanical reliability than rigid circuit boards. They have a low conductor bond strength and low base substrate tear strength. Nevertheless, most of the flexible circuits are subject to more mechanical stresses due to movement. This means that special care is required in the circuit design to gain higher circuit reliability.

There are several ways to make the reliability higher. Figures 66.44 and 66.45 show several common ideas for increasing the reliability of flexible circuits by modifying conductor patterns.

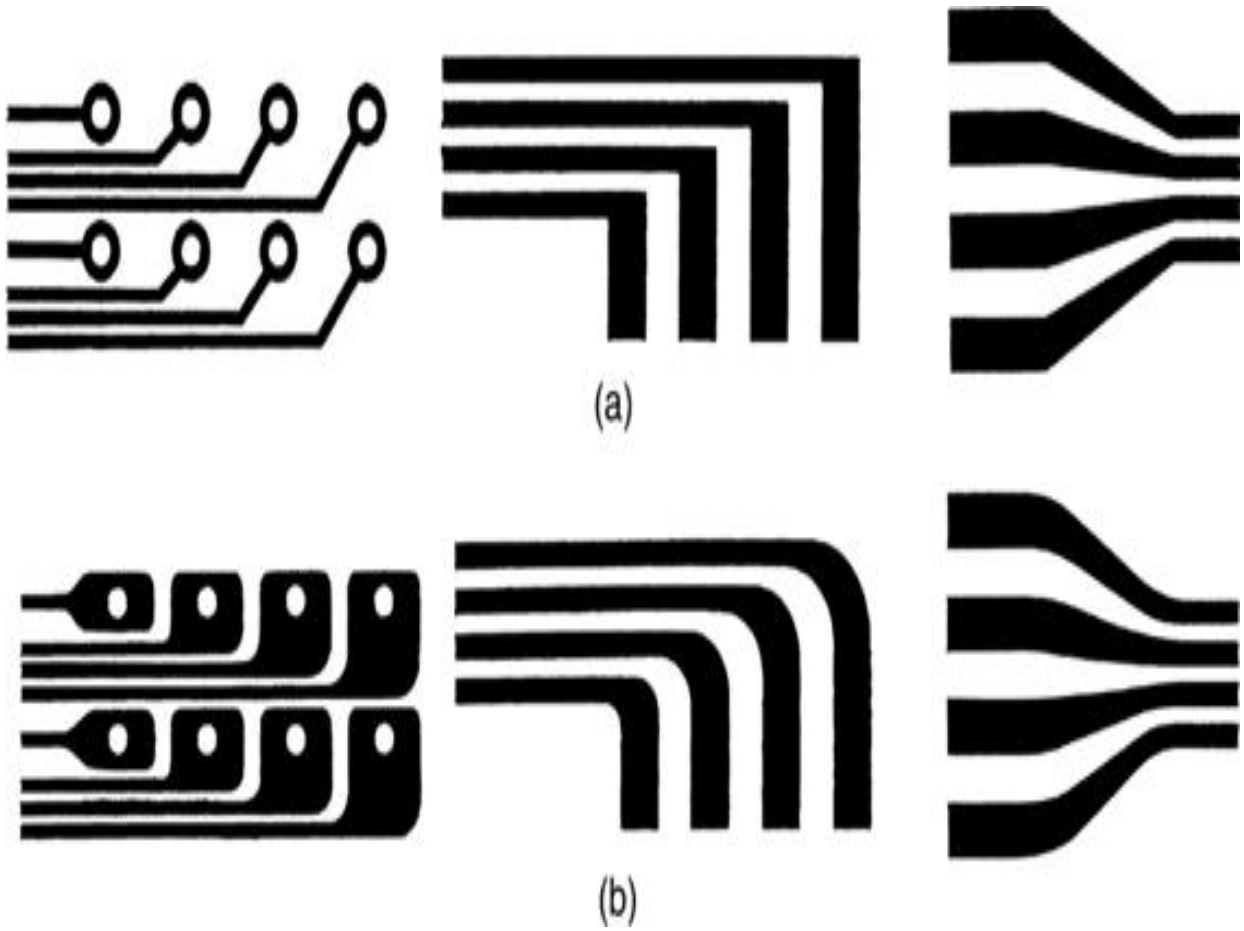


FIGURE 66.44 Reliability design for flexible circuits: (*a*) unacceptable, (*b*) preferred.

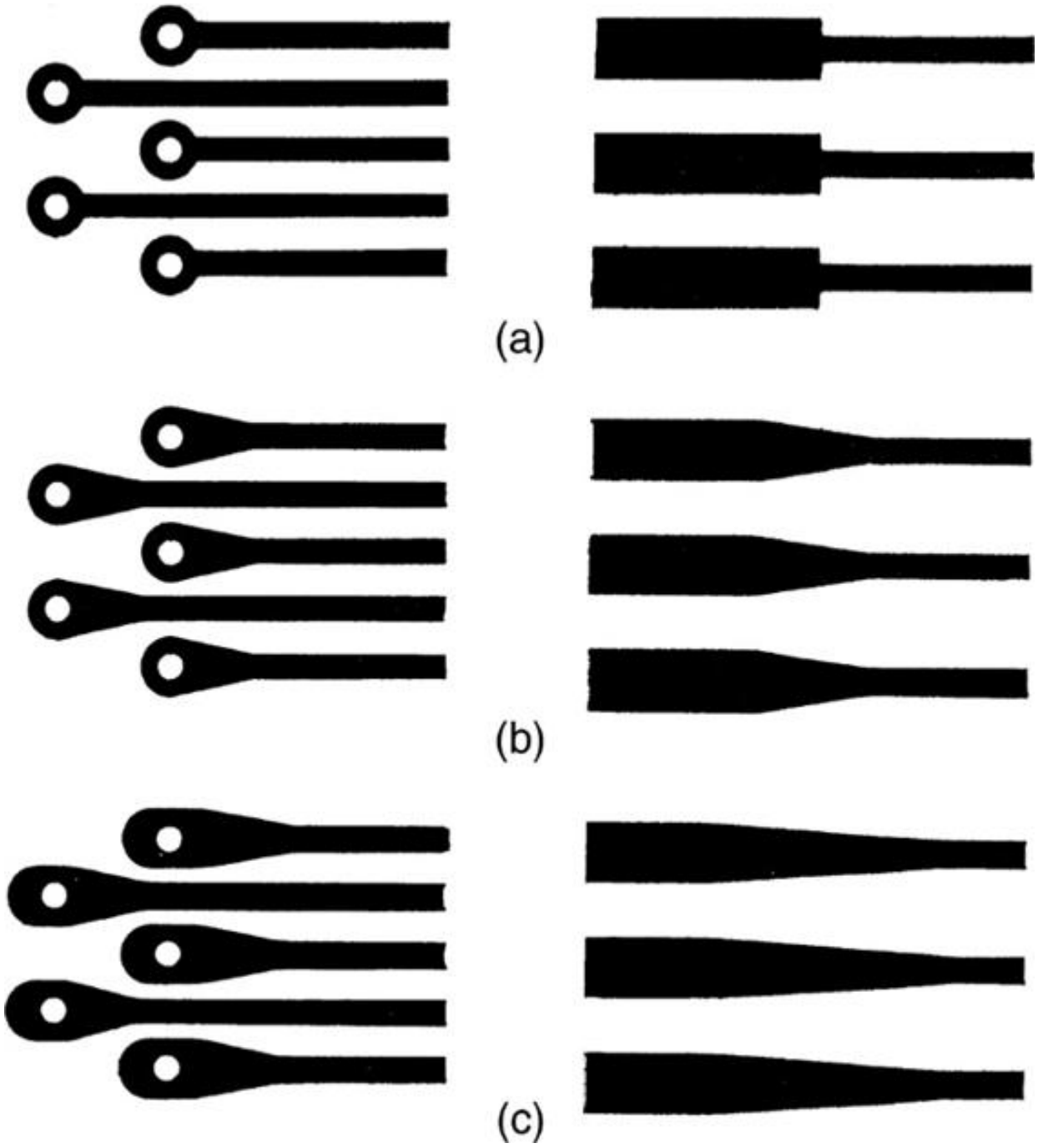


FIGURE 66.45 Reliable pattern design for flexible circuits: (*a*) unacceptable, (*b*) acceptable, (*c*) preferred.

The trace patterns should be smooth slopes between different widths. The pad size should be as large as possible. Figure 66.46 shows an example applied for automobile instrument panels. The conductors are designed to be as

wide as possible, and the spaces between conductors are kept in the safety range. A suitable coverlay opening could increase the reliability, as shown in Fig. 66.47. The amount of squeeze-out of coverlay adhesives should be minimized, however. The edge areas of stiffener boards are dangerous places in which mechanical stresses are concentrated. Figure 66.48 shows ways of reducing these risks.

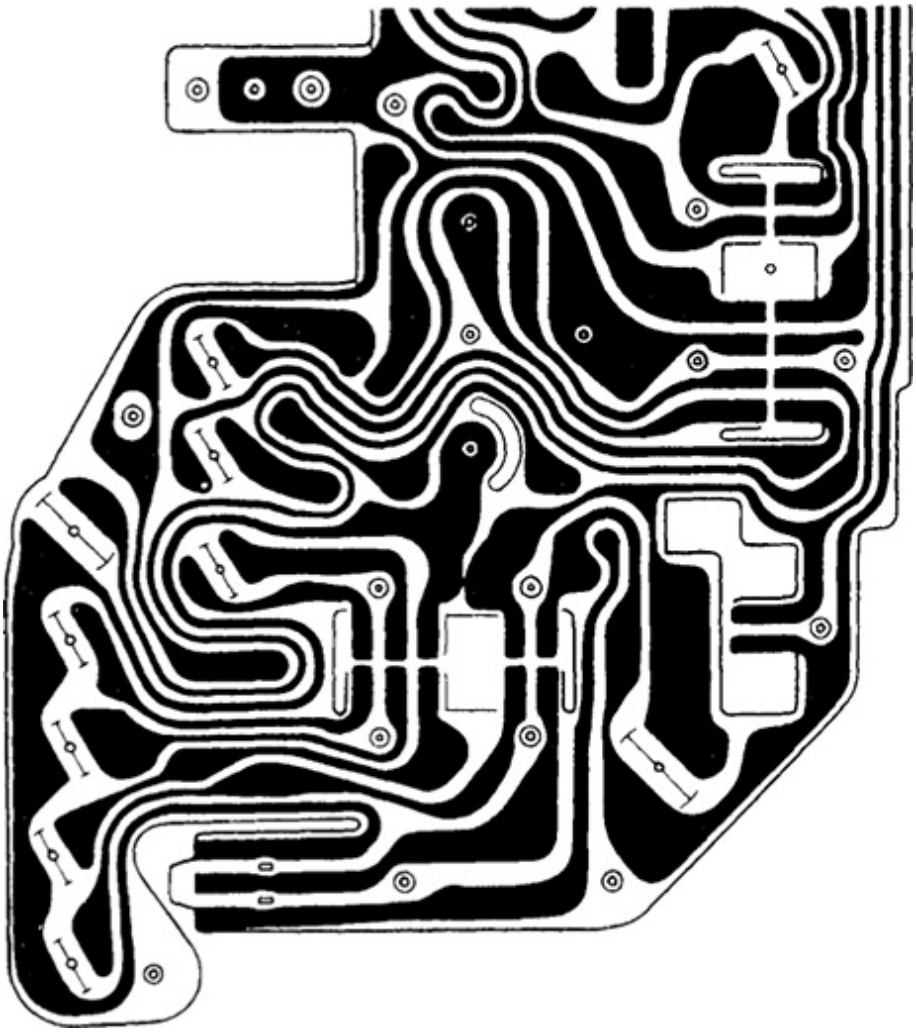


FIGURE 66.46 Conductor pattern designed for the instrument panel of an automobile.

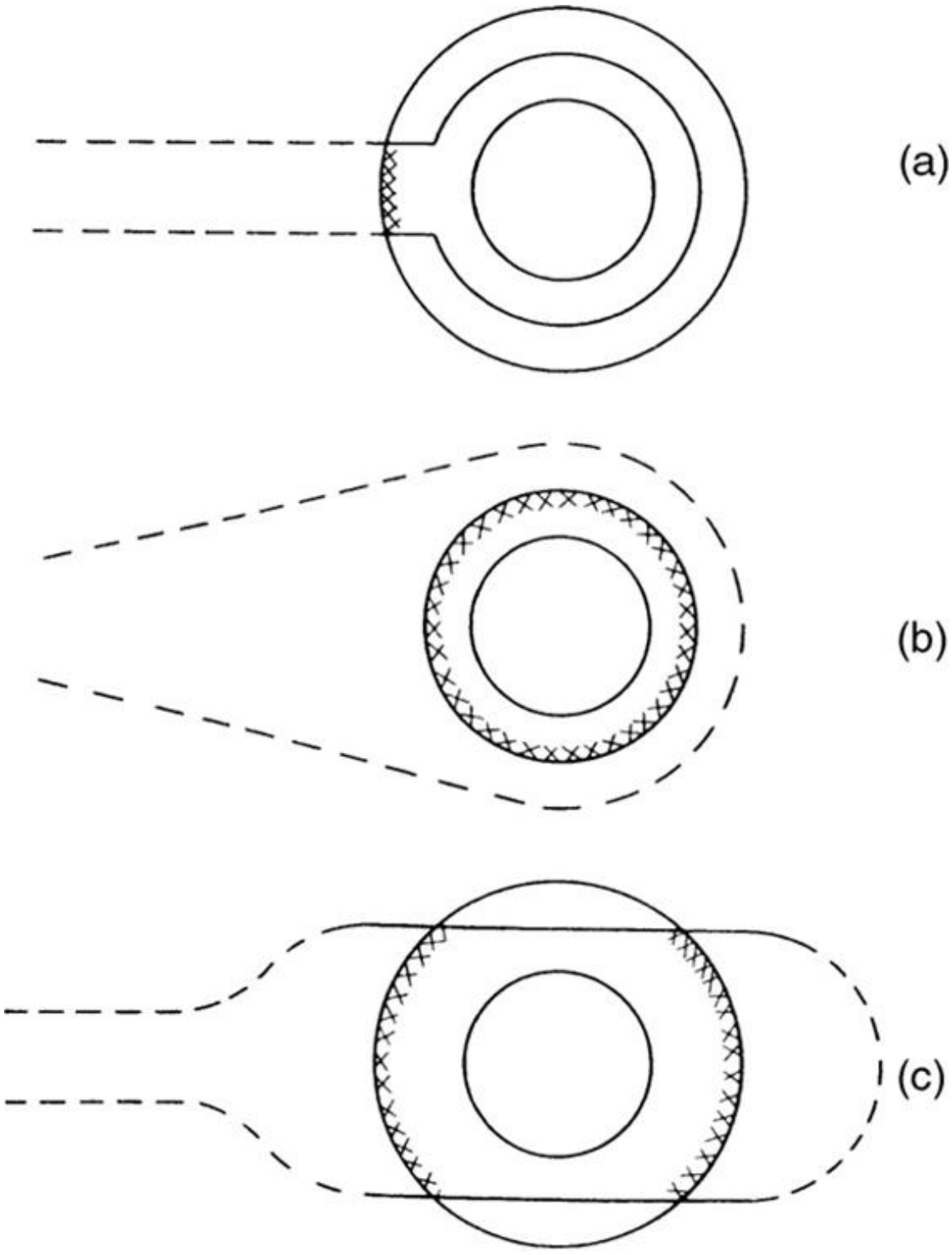


FIGURE 66.47 Coverlay opening for reliable solder pads: (*a*) unacceptable, (*b*) acceptable, (*c*) preferred.

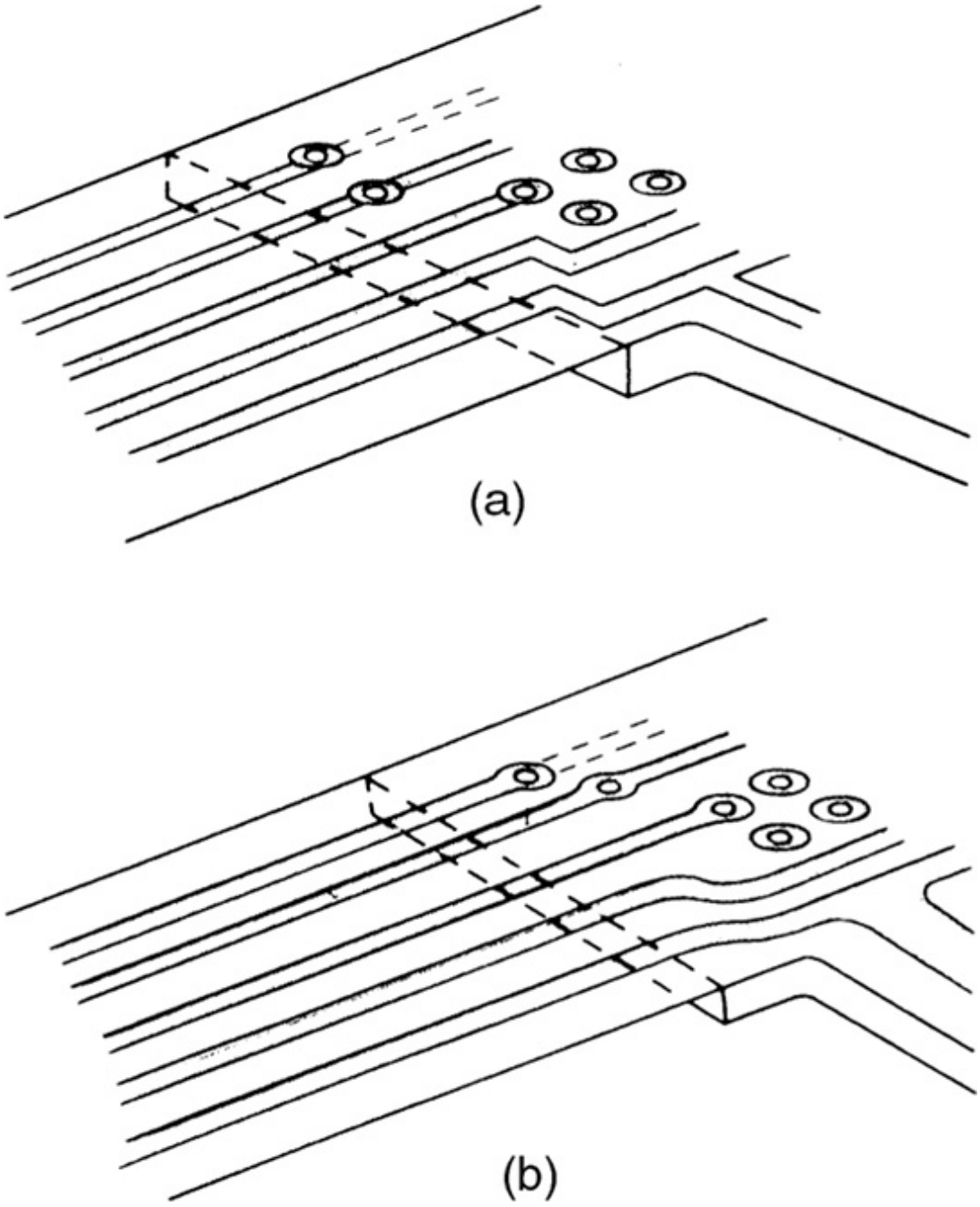


FIGURE 66.48 Circuit design at stiffener edge: (*a*) unacceptable, (*b*) preferred.

66.8 ACKNOWLEDGMENTs

The author extends his appreciation to the industry and the many who contributed to the progress of flexible circuit

activities, specifically J. R. Cannizzaro, who authored this chapter in prior *Printed Circuits Handbooks*. Sincere thanks also goes to Dominique K. Numakura, at DKN Research, for his authorship of this chapter in the previous (6th) edition of *Printed Circuits Handbook*.

CHAPTER 67

MANUFACTURING FLEXIBLE CIRCUITS

Joseph Fjelstad
Verdant Electronics, Seattle, Washington

67.1 INTRODUCTION

The manufacturing of flexible circuits is fundamentally the same as the manufacturing of rigid PCBs. Any facility capable of manufacturing rigid single, double-sided or multilayer circuits has all the basic tools required to make single-, double-sided, multilayer and rigid/flexible circuits; however, there are some significant differences in terms of the ancillary tooling and materials required to be successful. Compared with rigid boards achieving high productivity at high yield is much more challenging when manufacturing flexible circuits. The thin materials used for flexible circuits are much more delicate and prone to damage thus learning how to handle and process flexible materials are critical elements of their successful production. Manufacturing facilities for achieving high-volume production of flexible circuits must be engineered from the ground up and

specialized equipment is often called for, one of the most obvious of which is equipment designed for roll to roll processing. This chapter discusses some of the various methods and approaches to manufacturing flexible circuits and include discussions on some of the limitations of the processes used beginning with Table 67.1 which highlights some of the unique and significant differences between processing flexible circuits and rigid ones

TABLE 67.1 Unique Flexible Circuits Processing Features and Steps

Area of Concern	Issues for Processing Flexible Materials
Materials	Thin, low stiffness materials Low dimensional stability
Fragility, mechanical distortion	Less amenable to panel processing automation
Automation	Roll to roll processing
Flex specific features	Coverlayers and stiffeners

Most of the issues related to flexible circuit manufacture are a function of the delicate nature of the base which can be easily damaged. Coverlayers or cover-coating materials and the use of stiffeners in constructions are typically specific to flexible circuits and they require supplemental manufacturing processes. Because every additional process can impact manufacturing they can also impact process yield. The limitless variety of circuit outlines and shapes used in flexible circuit designs can often impact material yield and productivity which can increase cost. In addition being thin and delicate flexible base materials can easily incur serious, often fatal damage if they are handled improperly.

Flex materials can also undergo significant dimensional change in the manufacturing process resulting in a pattern

shift relative to mechanical features such as drill holes and the circuit pattern which can negatively impact yield. While some inroads are being made toward automation much flex circuit manufacturing requires skilled “touch labor” and labor intensity, of course, impacts product cost. Successful manufacturing of flexible circuits requires a partnership between design and manufacturing. Decisions made in design can have a significant impact on manufacturing yield, thus it is highly recommended the design and manufacturing have a continuing dialogue on an ongoing basis to ensure mutual success.

As a final note of introduction roll-to-roll (RTR) manufacturing systems are available where there is need for high-volume and high productivity manufacture of flexible circuits. However, it should be noted that RTR manufacturing is not flexible and not well suited to nonstandard flexible circuit constructions. For the most part they are dedicated manufacturing lines best suited to the production of single sided circuits and, to a slightly lesser extent, double-sided ones due to intrinsic limitations of the process.

67.2 FUNDAMENTAL FLEX CIRCUIT PROCESSING STEPS

Figure 67.1 provides a flow diagram of the fundamental steps required and manufacturing of the double-sided flexible circuit having both plated-through holes and stiffeners attached. The fundamental steps for producing a single-sided flexible circuit are incorporated within this process flow as well. The first half of the manufacturing process of flex through and including imaging and etching steps is relatively fundamental and is amenable to automation using roll to roll processing. However, processing subsequent to the steps through the etching process is

typically more labor-intensive and is thus a source and cause of increase cost in manufacturing. The designer who understands and appreciates the manufacturing process well can help control the total cost of his design and production. It is highly recommended that designers familiarize themselves with the manufacturing process to the greatest extent possible as the decisions they make in design will inevitably have an impact on both productivity and yield. The design coupled with a good process can reduce the total cost significantly, especially for complicated constructions.

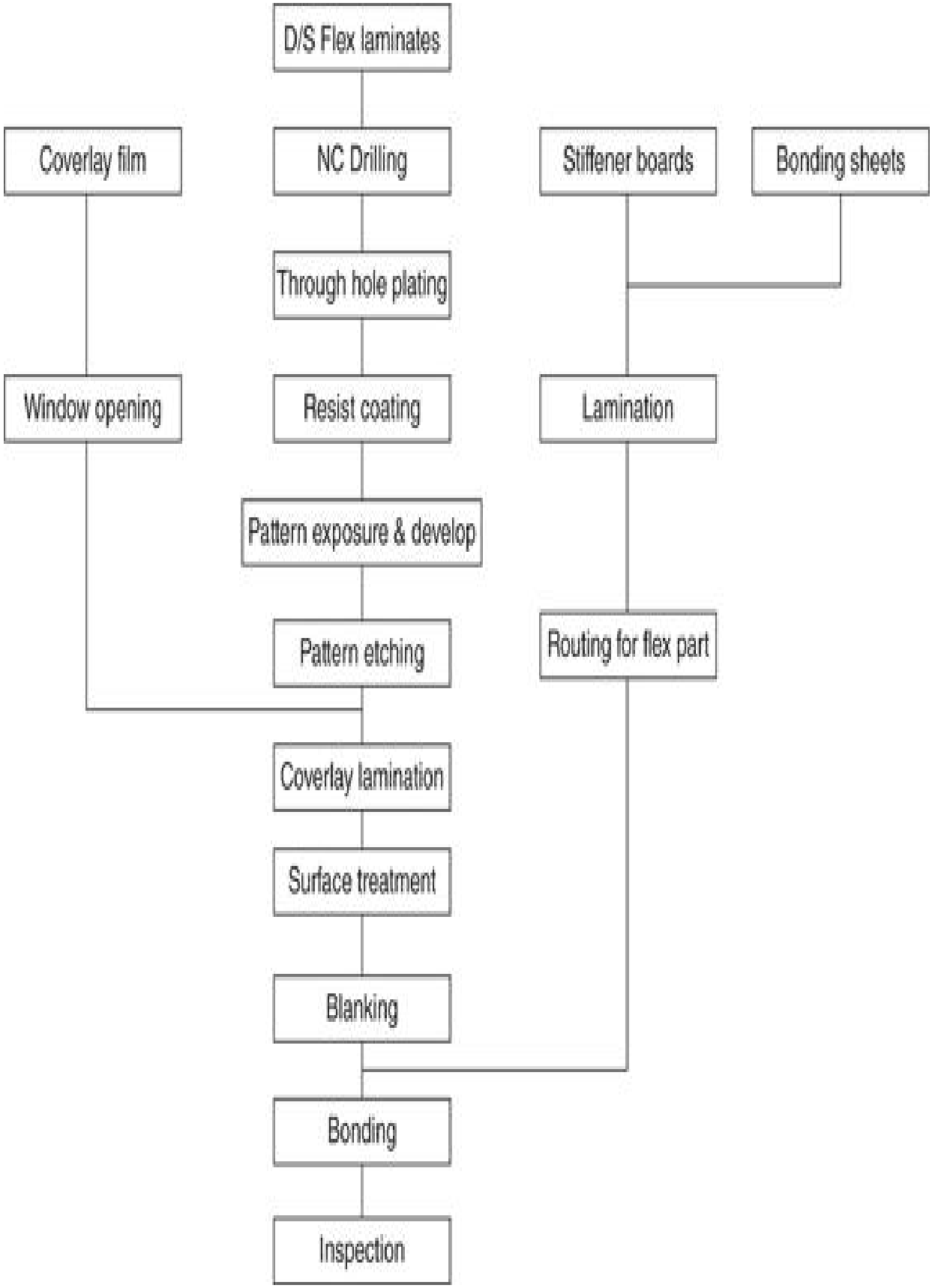

D/S Flex laminates
Coverlay film
NC Drilling
Stiffener boards
Bonding sheets
Through hole plating
Window opening
Resist coating
Lamination
Pattern exposure & develop
Pattern etching
Routing for flex part
Coverlay lamination
Surface treatment
Blanking
Bonding
Inspection

FIGURE 67.1 Standard manufacturing flow for double-sided flexible circuits.

67.2.1 Preparation of Flex Materials

It is common for materials used in flexible circuit manufacturing to be supplied in roll form; however, materials are often supplied in sheet form. Copper clad flexible laminates are, for example, often made available in boxes as flat sheets. In contrast coverlay films are most often supplied in rolled form. In manufacturing the first step in processing is to slit and cut the rolled materials into workable panel sizes. It is possible to cut with a manual shearing tool; however, it is advisable to use an automated feeding and cutting tool to get a consistent size and minimize handling damage. The surface preparation for copper foils on clad laminates, especially for single-sided laminates, is arguably best done before cutting and while still in roll form provided such RTR processing equipment is available. Chemistry used should be capable of removing any machine processing oils remnant from the processes used in its manufacturing. It may be accompanied by a light etch and/or a soft brushing step to ready the material for imaging and etching. Any such equipment when used should not produce any scratches nor induce any mechanical stresses in the copper clad laminate. Any scratching or deformation of the material in the process is capable of reducing manufacturing yield significantly so care is advised.

67.2.2 Direct Casting of Polymer to Copper Foil Processing

For special substrate constructions, especially ultrathin substrates or ultrahigh-density flexible circuits, a unique process involving the direct casting of polyimide resin onto

copper foils has been developed as an alternative to copper foil laminated to polyimide films. In some cases, photosensitive polyimide varnish is coated on to a carrier stainless foil. Electroless and electrolytic coppers are thereon plated to provide a thin conductor layer which can be circuitized. The photosensitive polyamide varnish materials used in the casting process can also be used to produce a reliable coverlay alternative for HDI flexible circuits. The technology of the direct casting is also useful in the building of multilayer constructions using semi-additive processing techniques. Special proprietary surface treatments of the polyimide film is required to assure suitable bond strength. The thin copper layers built in sequence can be imaged and etched to generate fine traces. When completed, the finished circuit can be removed from its stable stainless steel foil base to provide the desired flexibility. In some cases, the carrier foil is patterned and etched for use as an integral stiffener.

67.2.3 Mechanical Generation of Through-Holes

There are several different methods available for producing through-holes in flexible circuits. Method is predicated on a number of criteria including the materials being processed, the circuit construction and features size. Additional considerations include matters related to manufacturing volume, circuit density, and desired reliability.

Figure 67.2 in cross sectional view the major process steps in series used in the manufacture of a double-sided flexible circuit. Drilling can be performed using numerically controlled drill machines of the type used in the manufacture of typical rigid boards. One advantage in the manufacture of flex circuits is that, owing to the thinness of the material, more circuits can be drilled in a stack at one time when

compared to the rigid counterparts. However, appropriate backing boards and drilling conditions should be determined to ensure hole quality. A suitable combination of the NC drilling machine conditions and proper drill bit selection will allow the producers to generate smaller holes than 100 mm in diameter.

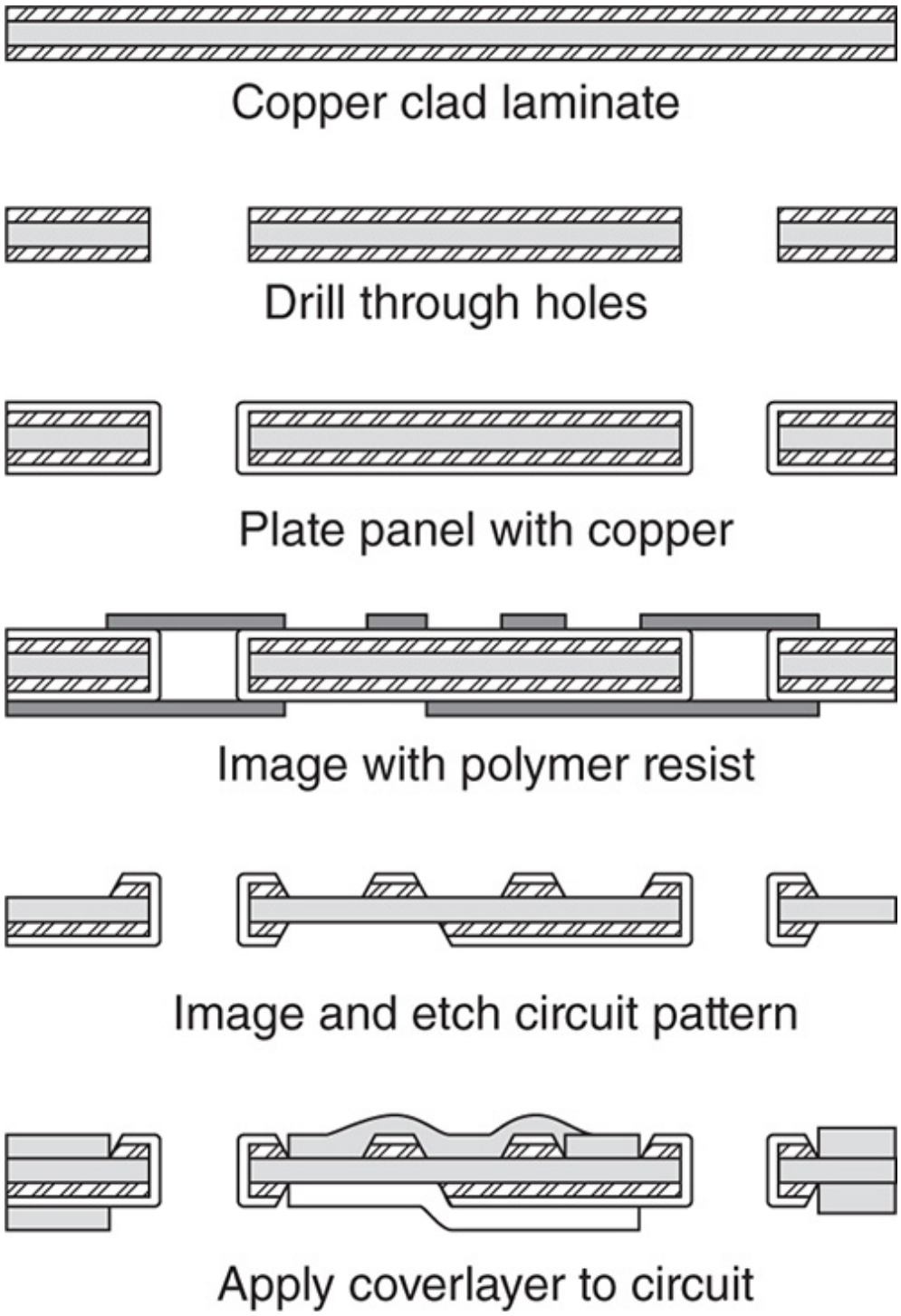


FIGURE 67.2 Typical manufacturing process steps for a double-sided flexible circuit.

Numerically controlled punching tools employing a suitable die set and punch conditions can also produce very small holes and thin copper clad laminates. Punching can be a low-

cost solution; however, it often requires a high volume production to offset the high-cost punch and die tooling. Such tools can generate holes smaller than 100 µm in diameter at very high rates, especially where repeating patterns with many holes in grid form are required. An example would be an IC packaging, such as a BGA. Another advantage of the punching process is that it easily adaptable to RTR processing. One drawback of punching is that it is not capable of producing blind via constructions.

67.2.4 Through-Hole Metallization Processes

Through-hole plating processes, similar to those used in rigid board fabrication, are available for, flexible circuits. More detail on the actual processes can be found in other chapters of this book.

To begin a mild cleaning process is applied prior to the chemical plating process because of thin base layers and relatively small smear amounts. Standard electroless (chemical plating) and electroplating processes are used. In addition direct copper-plating processes which employ a conductive carbon coating have been used successfully for the seed layer in the holes. Once a seed layer is established a suitable thickness copper is electrolytic deposited over the entire surface of the panel in addition to the through-holes. In general, thinner copper (i.e., nominally 20 µm) is recommended to ensure greatest flexibility of the circuits. Thicker copper plating in the through-holes (i.e., greater than 25 µm) is generally recommended higher reliability applications.

Selective copper plating of the through holes (sometimes referred to as button plating) requires an additional imaging step. Such structures are often required for dynamic flexing circuits. Precise thickness control of the through-hole copper

is highly desirable, unfortunately electroplated copper does not naturally deposit uniformly on the surface of the base copper foil. This had spillover effects in that nonuniform plated copper will cause a lower etching yield and reduce through hole reliability, especially for small pitch traces.

To mitigate the problem electromagnetic flux fields within the plating solution must be managed to improve distribution. Specialized plating fixtures and good contact at multiple points on the plated panel within the plating fixture is a requirement to obtain the desired results. In addition, proper design of plating fixtures and electrode configuration in the plating process is critical for achieving uniform copper thickness. Finally, well-designed fixturing is required because thin, flexible sheets made wave and flop about due to agitation in the plating bath. In short, while it is not easy to achieve very uniform copper thickness over panels, and especially large panels, with care it can be managed.

Figure 67.3 shows a comparison of a hole plated with an adhesive-based laminate and a hole plated with adhesiveless laminate. The adhesiveless laminate provides a sharp through-hole shape compared to the traditional laminate with adhesives.

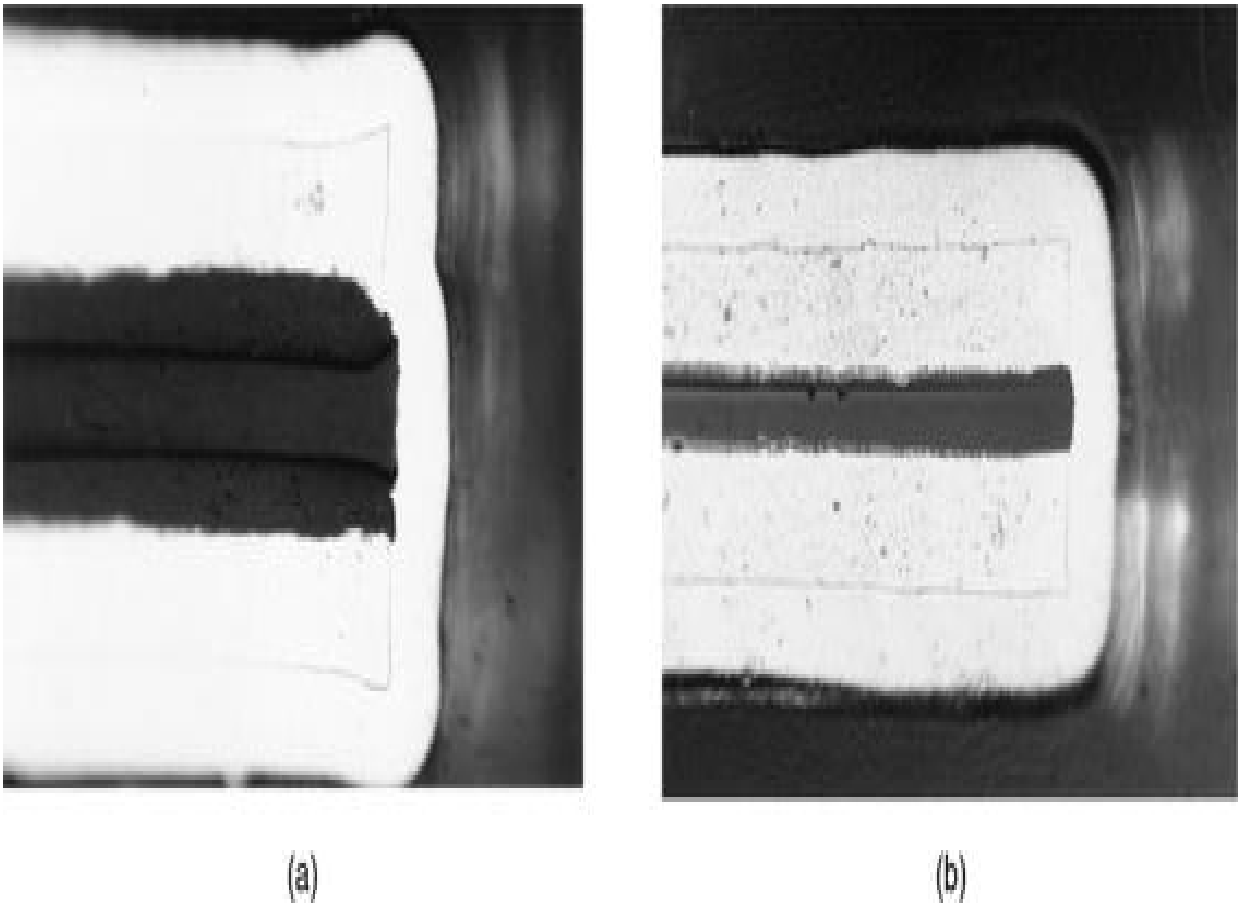


FIGURE 67.3 Adhesiveless copper-clad laminates (those without an epoxy or acrylic resin used to bond copper foil to the base film) provides excellent through-hole definition without desmearing processes a as illustrated above. Cross-section (*a*) is of through-hole of a double-sided circuit with adhesive-based laminate. Cross-section (*b*) is of through-hole of a double-sided circuit with adhesiveless base laminate.

67.3 EQUIPMENT FOR WET PROCESSING OF FLEXIBLE MATERIALS

As with rigid printed circuit boards, many of the processes used in the manufacture of flexible circuits involved the use of liquids. However, the conveyer systems for wet processes designed originally for rigid circuit boards do not work properly for thin flexible materials. They are generally incapable of providing a high process yield because they are

capable of generating wrinkles or scratches in the delicate flex material. This is true even when the flexible sheet is fixed on a leader board or carrier frame. Thus any conveyer system should be engineered to handle thin flexible circuits.

Conveyor systems designed to handle thin flexible materials in the wet manufacturing processes and which have proven successful in production have some distinct modifications over those used for rigid boards. One example is the use of larger diameter conveyer rings with smooth surfaces. Such systems have successfully reduced the scratches on the soft thin copper foil surface. Another attribute is the incorporation of reduced pitch on the transport rings, both line direction and transverse direction. The resulting redundantly overlapped conveyer system, mitigates the problem of the flex material diving down between the rings and/or winding of the thin materials on rolls. While the use of polymer strings and/or thin bars between the conveyer rings can mitigate the diving problem some manufacturers avoid such a solution suggesting that such devices are capable of creating small scratches on the soft copper surface of the flexible material. An example of a system suitable for flexible circuits is illustrated in Fig. 67.4.

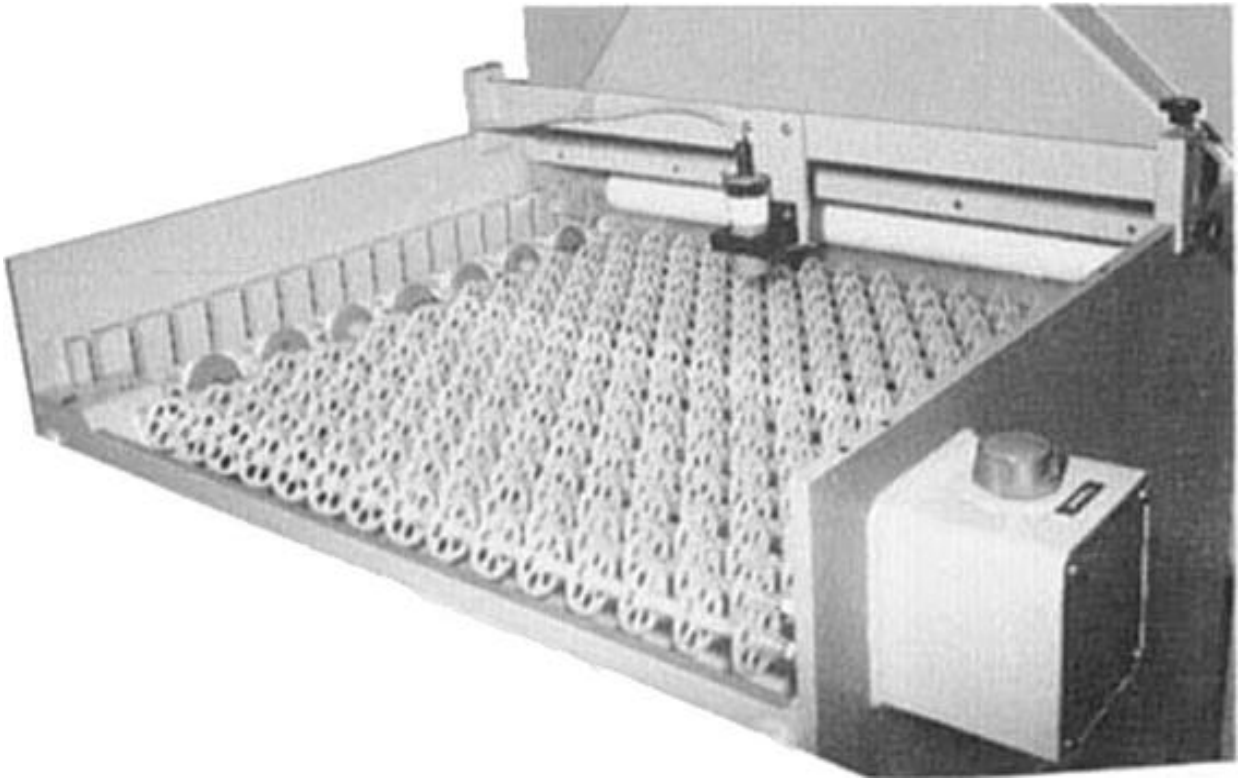


FIGURE 67.4 Special wheel conveyor system for thin, flexible materials showing high-density and smooth wheels. (*Source: Camellia*.)

In combination with a good transport system is a need for an effective sprayer system for delivering process chemistry to the panels passing under and above the conveyer. To ensure good coverage many sprayers oscillate, though fixed spray systems are not uncommon. Spray pressure is of importance. If the spray pressure is too high and or/unequal some fluttering of the panel is likely. This can introduce unwanted distortion for the thin materials especially after etching. Soft rubber rollers are often employed between process and rinse chambers to both minimize dilution of process chemistry and drag out which can result in excessive contamination of rinse waters.

67.3.1 Surface Cleaning of Flexible Materials

A precleaning process is required to remove the stains and oxidation from the surface of the copper foils prior to the coating of screen printed circuit pattern or photo resist material used to define the circuit pattern photolithographically. In addition, adhesiveless laminates typically have an extremely smooth and shiny copper surface; therefore, the chemical cleaning has an important function in making for better adhesion to the etching resist used. This is especially important for fine trace patterning.

A mild chemical cleaning process is preferred. There are a number of proprietary solutions available which employ a diluted organic acid. The treatment should be applied without inducing mechanical damage to the circuit which could negatively impact imaging process yield. Soft scrubbing or soft brushing may be used if a mechanical process is necessary to remove tough stains or oxidation on the copper surface. However, an overly aggressive mechanical brushing can produce mechanical stresses on the thin materials causing loss of dimensional uniformity. As an alternative to conveyer honest chemical processing, a soft brushing processing equipment incorporating a belt conveyor has been developed is available and 10 clean surfaces with minimal mechanical damage to flexible materials; however, process works only for one side of the laminates. Thus, for double-sided laminates the process must be repeated on the second side.

67.3.2 Etch/Plating Resist Coating of Flexible Materials

The photoimageable and screen printed etching resist inks commonly used for rigid circuit boards are suitable for flexible circuit imaging as well. In the case of screen printing, the process inks are generally suitable for relatively coarse pattern etching, especially with large volume production. Dry

film photo resists and resist laminators of the type used for rigid production can be adapted to flexible circuit production.

In the case of RTR processing, the resist material can be paired with unload and take up rollers for step imaging in a suitable imaging system. Because many photoresists can become brittle following exposure it is necessary to make sure that the film is suitably flexible to ensure it does not inadvertently break up during processing. In addition, because tenting of plated-through holes is often performed with double-sided flex circuit panels, it is necessary to make certain that the thickness chosen will withstand the etching process without breaking down and allowing at solution to enter and etch away copper within the plated-through hole.

A thinner dry film can be used for the single-side circuits. Then are photoimageable films are generally capable of resolving much finer features than thicker films. Dry films which are 15 to 20 µm thick are capable of producing 30- to 40-µm lines and spaces at high yield when using 12-µm-thick copper foils. As an alternative a liquid photo resist can be used as thin films can be coated and provide very fine feature definition for high-density circuit traces having pitches of less than 40 µm.

67.3.3 Circuit Pattern Generation on Photoresists

The same type of exposure systems used for rigid printed circuit production can be used for flexible circuits as well. Such systems should have a highly collimated light source as it is generally required for defining high-density circuit traces having pitches smaller than 50 mm at high yield.

The tooling system chosen and employed should be capable of providing good alignment between the circuit pattern and the hole pattern on the copper clad laminate. Moreover, it should be able to achieve good pattern

alignment with high productivity. Auto alignment systems employing CCD cameras have been introduced to help minimize the pattern shift from the via holes generated and plated through in the panel.

Because some dimensional change may occur in the earlier mechanical and wet process manufacturing steps, some dimensional correction to the photomask compensate may be required.

In general a glass photomask tool is recommended for tracers finer than 50 µm pitches over more commonly used polyester base film masks. The setup should ensure that the heavy glass masks are accurately positioned in the machines. Precise alignment between top mask and bottom mask is required for the production of high-density double-side flexible circuits. On occasion, partial dimensional corrections may be required to adjust for random distortions of the thin flexible materials due to processing. Alignment accuracy of better than ±10 µm is required for lines and space pitches' finer than 50 µm.

It is possible to make a corrected photo mask for the imaging process in order to minimize the misalignment. Unfortunately, the distortion of the flexible laminate is generally random and thus not predictable, as a result it may be necessary to generate an image corrected mask for each job lot. In such cases, it is necessary to segregate the materials being processed and hold them until the corrected mask is available for use.

As a practical matter, one of the easiest ways of managing tight dimensions is to reduce panel size; however, the reduction of panel size will also reduce productivity. That said high productivity at low yield is not a desirable situation. Moreover, while it is arguably possible to employ a "step and repeat" approach to imaging similar to that used in the semiconductor industry it is not common. The method involves multiple exposures of the same circuit over a panel.

A recently introduced technology trade named Rainbow, is a self-contained clean environment imaging system, where double-sided copper panels are automatically processed on both sides simultaneously through the stages of etch resist coating, imaging, developing, and rinsing, resulting very high levels of throughout with very fine detail achievement (line and space). Key to the process is a proprietary solvent-free liquid etch resist which is coated at 5 mm thickness and cured instantly using a bank of integrated UV LED lights. In the processing, immediately after coating, phototools are brought into direct contact with the wet resist on the panels before the UV LEDs are used to cure the exposed areas. The phototools are mounted offline into a cart-mounted registration system, which can be swapped out at the process line very quickly resulting in minimal downtime during part changeover. Except for phototooling setup, handling is fully automated thus no human interaction is required during the processing, minimizing risk of contamination and offering the potential of high yields. Designed for innerlayer processing, it is uncertain how the process will work for flex but it appears promising.

Perhaps the most promising solution is the use of laser direct imaging equipment (LDI). Laser direct imaging is capable of making image corrections for any distortions induced in flexible materials in real time. While LDI has been a process of choice since its introduction for prototype and low to middle volume production, recent improvements in the technology and imaging rate as well as the ability to expose both sides of the panel simultaneously make it very attractive for future high-volume production as well. It has been suggested that LDI is not as well suited to the production of circuit traces finer than 25-µm lines and spaces but this seems a minor limitation compared to the benefits and the fact that many circuits do not require features smaller than 25 µm.

67.3.4 Chemical Etching of Copper Clad Flexible Materials

A number of different chemistries are available for use in the etching of copper circuits. Ferric chloride is perhaps the most utilitarian of available etching solutions being capable of etching a wide range of metals and metal alloys including copper. One of its drawbacks is that anything the solution touches is often left with an unsightly brown stain characteristic of ferric chloride processing. In more common choice is a cupric chloride solution which is capable of etching copper effectively and rinses cleanly. Cupric chloride etching solutions are often used in the production of interlayer is for rigid multilayer circuits. A third choice for etching copper is an ammonical alkaline solution. Alkaline etchants offer higher processing speeds; however, this can be a disadvantage when trying to etch very fine line circuits in addition alkaline solutions may chemically attack some types of polyamide films which could undercut very fine circuits that should be used with caution in such applications.

Process engineers should characterize the etching process with the chosen chemistry for the feature sizes being sought at a given copper thickness. The objective is to provide a correction factor to the traces that will be employed in the imaging process. In short, etching is an isotropic process meaning that as the copper is etched down into it is also etched laterally reducing trace width. One relatively simple way to characterize the process is to image patterns of lines and spaces of the target size and shape and etch them followed by accurate measurement of the results. This data can then be fed back to the photo tool maker to adjust line and space to appropriate values. There can be a significant difference in etching factors between middle conductors and edge conductors. The use of nonfunctional conductor

patterns adjacent to circuit features can help ameliorate the effect.

Finally, provided circuit performance is not dependent nor adversely affected by trace width modification, the tapering of traces can be employed to maximize dimensional stability by assuring maximum copper area in the circuit design.

67.4 COVERLAYER/COVER-COATING METHODS

Coverlayers or cover coats are direct analogues of solder mask on rigid circuit boards; however, in the case of flexible circuits the coverlayer or cover coat must remain flexible and not crack in use. The distinction between a coverlayer and a cover coat is that a coverlayer is generally an engineered material which must be preprocessed (i.e., drilled) and then laminated to the flexible circuit with holes aligned to circuit features where some type of interconnection or component lead must be terminated. In contrast a cover coat is often screen printed onto the flexible circuit began leaving open the features of interest. There is a third type of coating for flexible circuits, which is fundamentally a photoimageable polymer film bonded to the flexible circuit exposed and developed. Table 67.2 summarizes the comparison of traditional coverlay technologies and new technologies.

TABLE 67.2 Coverlay Process Options

	Accuracy (Minimum Opening)	Reliability (Flexing Endurance)	Material Selection	Equipment/ Tooling	Technical Hurdles	Cost
Traditional film coverlay	Low (800 µm)	High (long)	PI, PET	NC drill, heat press	Need long experience	High
Film coverlay + laser drilling	High (50 µm)	High (long)	PI, PET	Heat press, laser	Low	High
Screen print liquid ink	Low (600 µm)	Acceptable (short)	Epoxy, PI	Screen printer	Medium	Low
Photoimageable, dry film type	High (80 µm)	Acceptable (short)	Epoxy, PI, acrylic	Laminator, exposure, developer	Medium	Medium
Photoimageable, liquid type	High (80 µm)	Acceptable (short)	Epoxy, PI	Coater, exposure, developer	Relatively high	Low

Among these types, traditional film coverlay generally has the best balance of physical properties and provides the highest reliability especially in dynamic flexible circuit applications where high flexible endurance is required. Unfortunately, traditional coverlayer films are the most difficult to process and not easily automated and thus tend to be more touch labor intensive than the other two methods. While it tooling system can be used to provide gross alignment and operator is normally employed to visually check, adjust fine alignment and tack in place using a hot iron. Moreover, the method is not very amenable to the production of circuits requiring small openings due to squeeze out of the adhesive used in lamination onto the circuit features which need to be free and clear of any foreign material.

Given the increasing demand for ever finer features (i.e., openings in terminations smaller than 200 µm in diameter requiring better than ±100 µm positioning) such as is required for fine pitch BGA, CSP, and other chip type passive components more exacting methods are required. While screen printing of flexible ink cover coats can provide a low-cost solution for volume production, it cannot provide such small openings as are required with high dimensional accuracy. Thus photoimageable coverlayer technologies are often being selected in applications having very small openings with tight dimensional accuracy. The technology has been generally available for many years and improvements in the materials and processes have been ongoing.

67.4.1 Coverlayer Preparation and Lamination

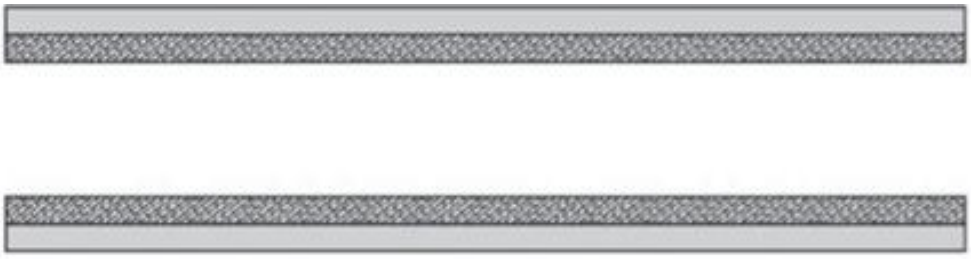
As mentioned earlier adhesive backed polymer films are referred to as coverlayers. The adhesive is generally a partially cured, flexibilized epoxy or acrylic. These are preprocessed with holes or apertures in desired locations and then laminated to the flexible circuit using heat and pressure for specified dwell-time to cure the adhesive, which can vary from a few minutes to up to an hour. In general coverlayer is made up of the same materials set that is used for the creation of a copper clad laminate.

Epoxy-based coverlay films have a relatively short shelf life and room temperature and thus must be kept refrigerated when not actively being processed. Openings for access windows to circuit features of interest are most often made by NC drilling or punching. The surfaces of the flex circuits must be must be thoroughly cleaned before coverlay lamination takes place. Specialty roller tools have been developed for this purpose. In addition the processing area

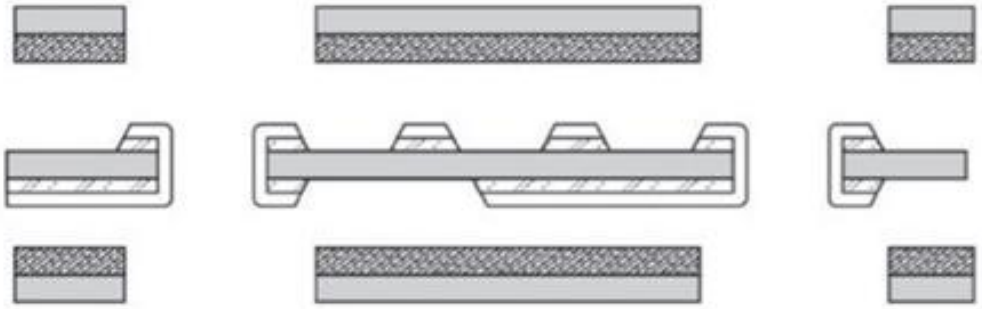
should be kept clean and environmentally controlled to minimize static charge buildup which can attract dust and debris to the circuit surfaces. While keeping relative humidity and the work area can mitigate static charge buildup, moisture is also deleterious as excess moisture in the laminate can cause blistering of the coverlayer.

Automation of the coverlayer lamination process is challenging because the coverlayer material is generally less stable after holes and window openings are formed. For the most part, manual alignment of coverlayer to laminate is used. A talented and attentive technician can achieve very good results aligning and tacking the coverlayer to the circuit for subsequent lamination. For this process unless the circuit needs an accurate registration in the range of 50 to 75 mm. After the coverlay film is temporarily fixed on the circuit, the adhesive layer is cured in a heat press or autoclave similar as multilayer rigid boards. A suitable curing condition should be chosen carefully based on the circuit design and material conditions. Epoxy resins change flow properties significantly by thermal aging, even though they are kept at a low temperature; therefore, a detailed conditioning should be performed based on the flow properties of the adhesives. A high flow of the adhesive resin makes good encapsulation of the conductors, but it also causes a squeeze out of the resin in the openings and resulting potentially deleterious deposits and staining on the copper traces. On the other hand, a low resin flow causes a poor encapsulation and results low bond strength and exposed air voids beside the traces. The selection of the press pad materials and separation films is another key factor to have good encapsulation and minimum squeeze out of the glue from the edges. A vacuum press or a vacuum autoclave helps to make good encapsulation of the conductors, eliminating voids or air traps beside the traces, especially for a thick copper foil.

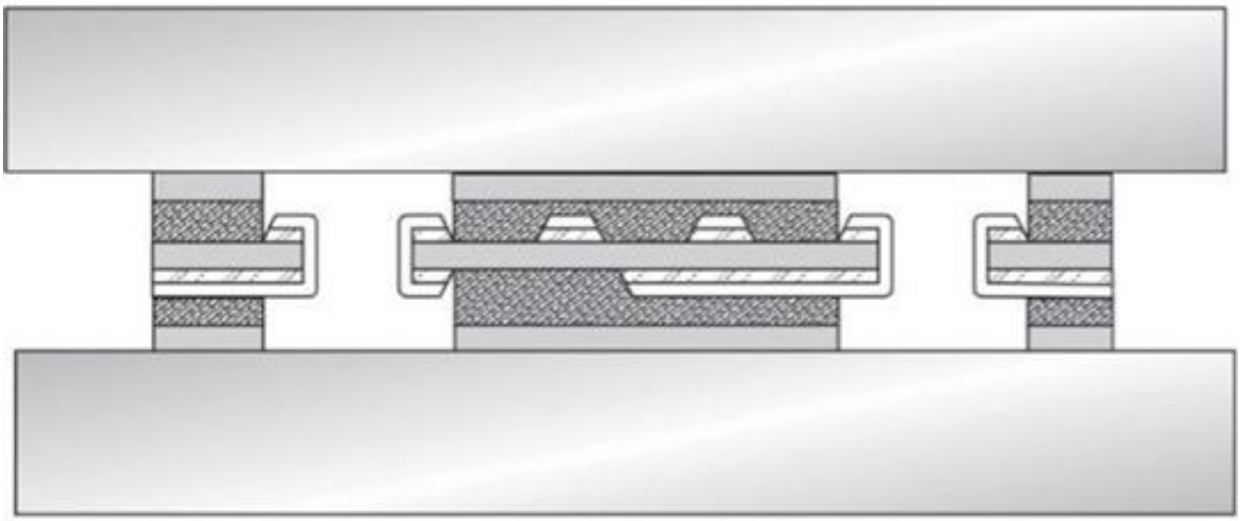
It takes more than one and a half hours for a nominal heated heat press lamination cycle to complete the chemical curing reaction of the adhesive resins, therefore the batch size and the lamination equipment have been becoming larger to make the productivity higher. But it makes the process flexibility lower. A quick press system has been developed to have a better flexibility. One set of coverlay films and an etched flexible circuit panel is hold in a small vacuum press for less than 2 min as the preliminary lamination. After that, several numbers of panels are baked in a thermal oven to complete the chemical curing of the adhesive resin. This process needs a special epoxy resin for the adhesives, but it provides a high flexibility for the small volume and prototype productions. A typical coverlay manufacturing process is shown in Fig. 67.5.



Prepare upper and lower coverlayer film



Align coverlayer to top and bottom of circuit



Laminate using heat and pressure

FIGURE 67.5 Basic coverlayer processing steps are shown above. Coverlayer material is selected and apertures provided to access features of interest and oriented and laminated to surface of the flex using heat and pressure. Special materials are used to ensure good conformance to and sealing of circuits on the surface.

67.4.2 Screen-Printing Coverlay

The screen printing process has been a part of printed circuit manufacturing since the earliest days of the industry. Originally for printing the actual circuits, then as an etch and plating resist and most recently for application of solder mask and legend to the surfaces of the printed circuit board. The same processing methods are suitable for the application of flexible screen printable polymer inks to the surfaces of finished flexible circuits. The major differences in processing are related to fixturing for alignment and the use of the vacuum system in concert with a perforated base to hold the flexible circuit flat and in place during the screen printing process. Care should be exercised relative to the vacuum intensity as it is possible to create a dimpling effect on the surface of the flex circuit which can be seen in the screen printed polymer ink. Postimage curing should be performed a suitable carrier, that is one which will hold the coded flex circuit flat without inducing potential defects. The selection of the ink, carrier and curing conditions should be such that any potential shrinkage of the materials is uniform resulting in a uniformly flat circuit. The basic process is illustrated in Fig. 67.6.

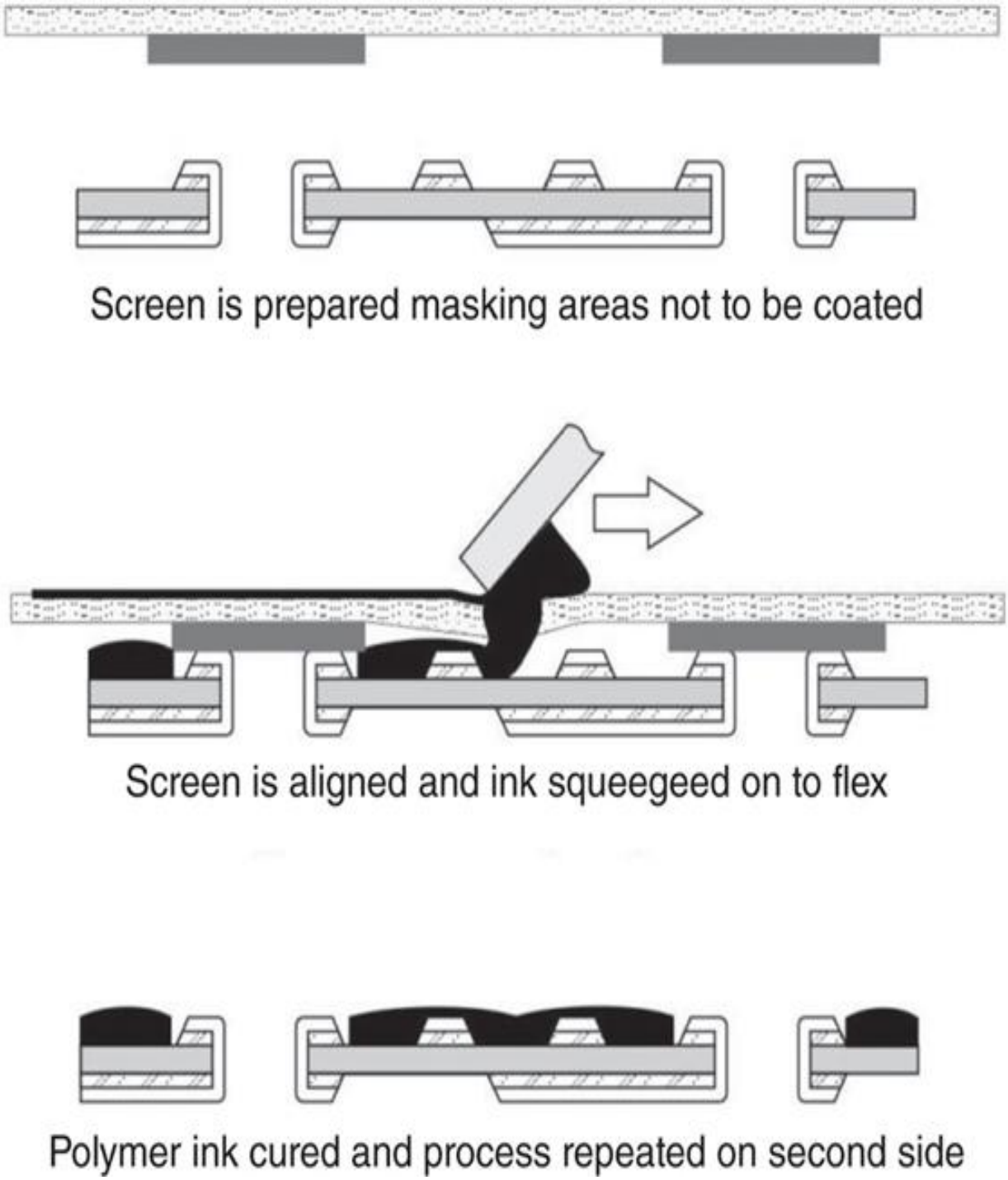


FIGURE 67.6 Screen print process for polymer ink coverlayer deposition.

67.4.3 Photoimageable Coverlay

As photoimageable solder mask systems for rigid circuit boards were developed in the 1980s, similar ideas were tried for flexible circuits. Fine openings and high-dimensional accuracy were expected. Unfortunately, the materials for rigid circuit boards were too brittle for flexible circuits, and therefore new materials were required. As a result, chemical specialty companies developed photoimageable polymer materials in both liquid and dry film forms specifically for use as coverlayers for flexible circuits. The materials found volume opportunities in a number of different markets including automotive, computer, and consumer products. While there were some problems with earlier versions present day materials are much improved. There are differences in terms of the performance of liquid and dry film coverlayers and thus the designer should familiarize themselves with the limitations of each.

The processing steps for the two different types of photoimageable material are quite similar in terms of fundamental steps except for the method of application of the material to the flexible circuit and the need for a baking step in the case of photoresist applied in liquid form as illustrated in Fig. 67.7.

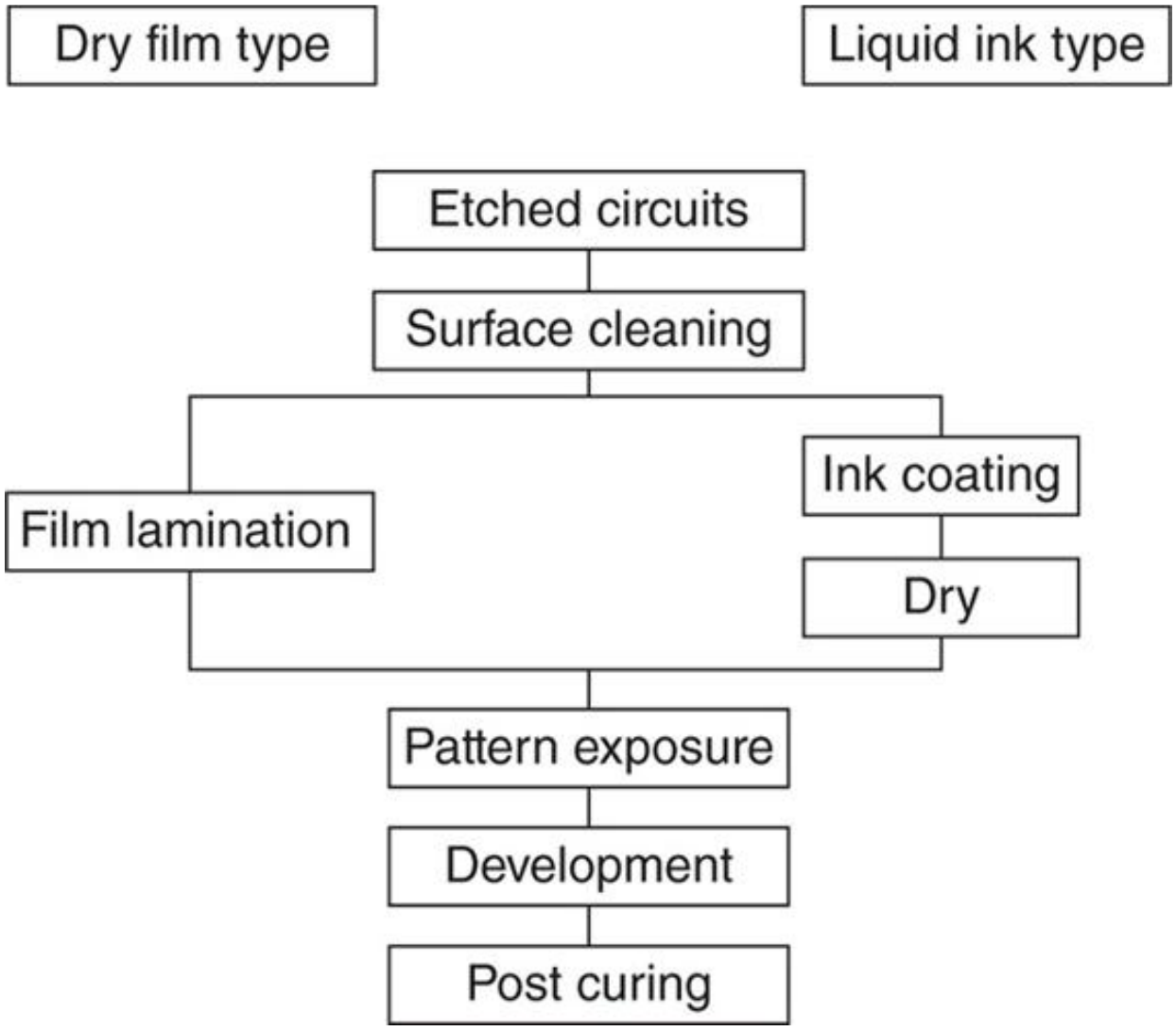


FIGURE 67.7 Comparison of process flow for dry film and liquid polymer photoimageable coverlayers.

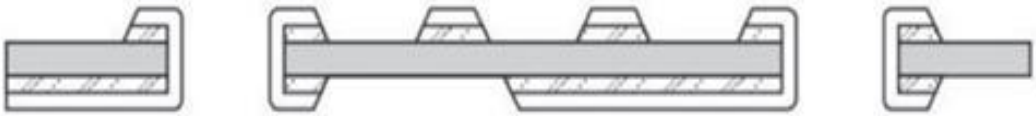
In the case of dry film photoimageable coverlayers, they are commonly applied using a heated roll coating process to coat one or both sides of the flexible circuit with the dry polymer film. This is often done in combination with a vacuum lamination system to assure the removal of air and complete encapsulation of the circuits. However, roll coating laminators used for rigid boards can be quite suitable for roll coating of dry film coverlayer material. That said when thick copper circuit traces are tightly spaced elimination of air entrapped between the traces can be very difficult without

vacuum. It is normally recommended that there be a hold time of between 15 and 30 min to allow the photoimageable polymer to stabilize before exposure.

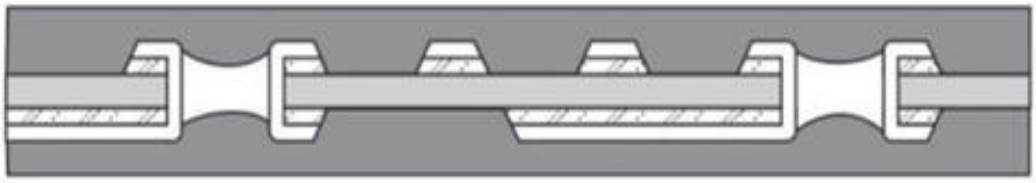
With respect to the application of polymer ink photoimageable coverlay material there are a few options. The simplest of these is to use a screen printing process to fully coat the surface of the flexible circuit. Another option is to use a spray process and the third is to employ a curtain coating process where the circuits are passed underneath a continuously flowing curtain of liquid photoresist to apply a uniform coating over the entire surface of the circuit as it passes under and through the flow of material. The latter to processes require special capital equipment the cost of which is much greater than a simple screening chase; however, the productivity can be quite high offsetting the cost. For all of the aforementioned processes the steps must be repeated for two-sided circuits and thus a drying step is required between coatings. There exist automatic coating machines capable of processing double-sided circuits; however, they are best suited to very high-volume production application.

Following drying the same ultraviolet exposure equipment used for manufacturing traditional printed circuits can be used to expose coverlayers of both dry film and liquid form. Likewise development process can be carried out using the same equipment and chemistry as is commonly used for the development of rigid printed circuit board solder masks (i.e., 1 percent aqueous solution of sodium carbonate). Following development a baking step is normally employed to ensure the coating material’s long-term performance. This is carried out at a nominal temperature of 150°C usually for about one half hour for full cure. Conventional air convection ovens can be used. In addition conveyorized infrared ovens have been used for post baking by some manufacturers successfully. Good process controls in such applications are of great importance.

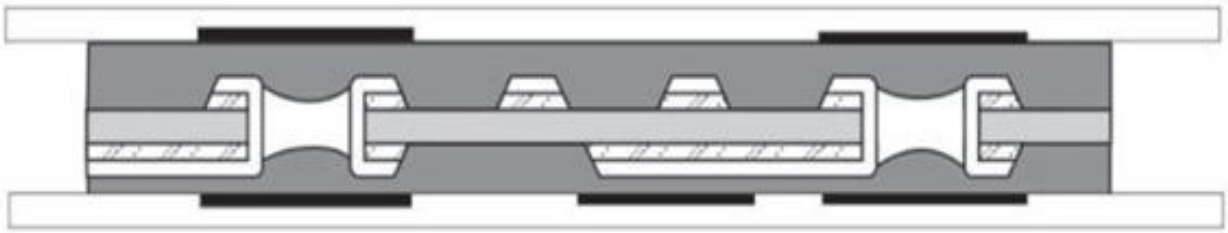
Figure 67.8 provides a graphic representation of the basic processing steps for application of a photoimageable coverlayer and Fig. 67.9 shows a photo micro-graphic example of an opening formed in a photo imaged and developed coverlayer material.



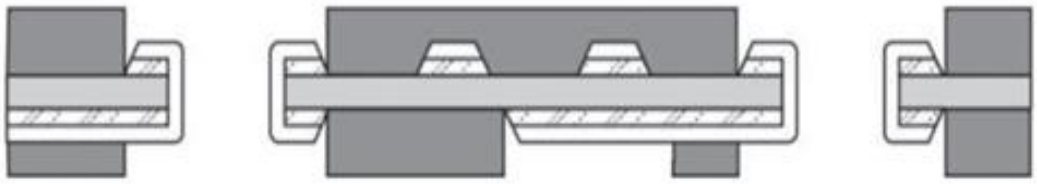
Functional flex circuit with pre-cleaned before coating



Flex circuit coated with photoimagable polymer



Photomask tools are aligned and polymer us exoised



Unexposed polymer is developed leaving access to selected circuit features

FIGURE 67.8 Basic processing steps for the application of a dry film or liquid polymer coverlayer.

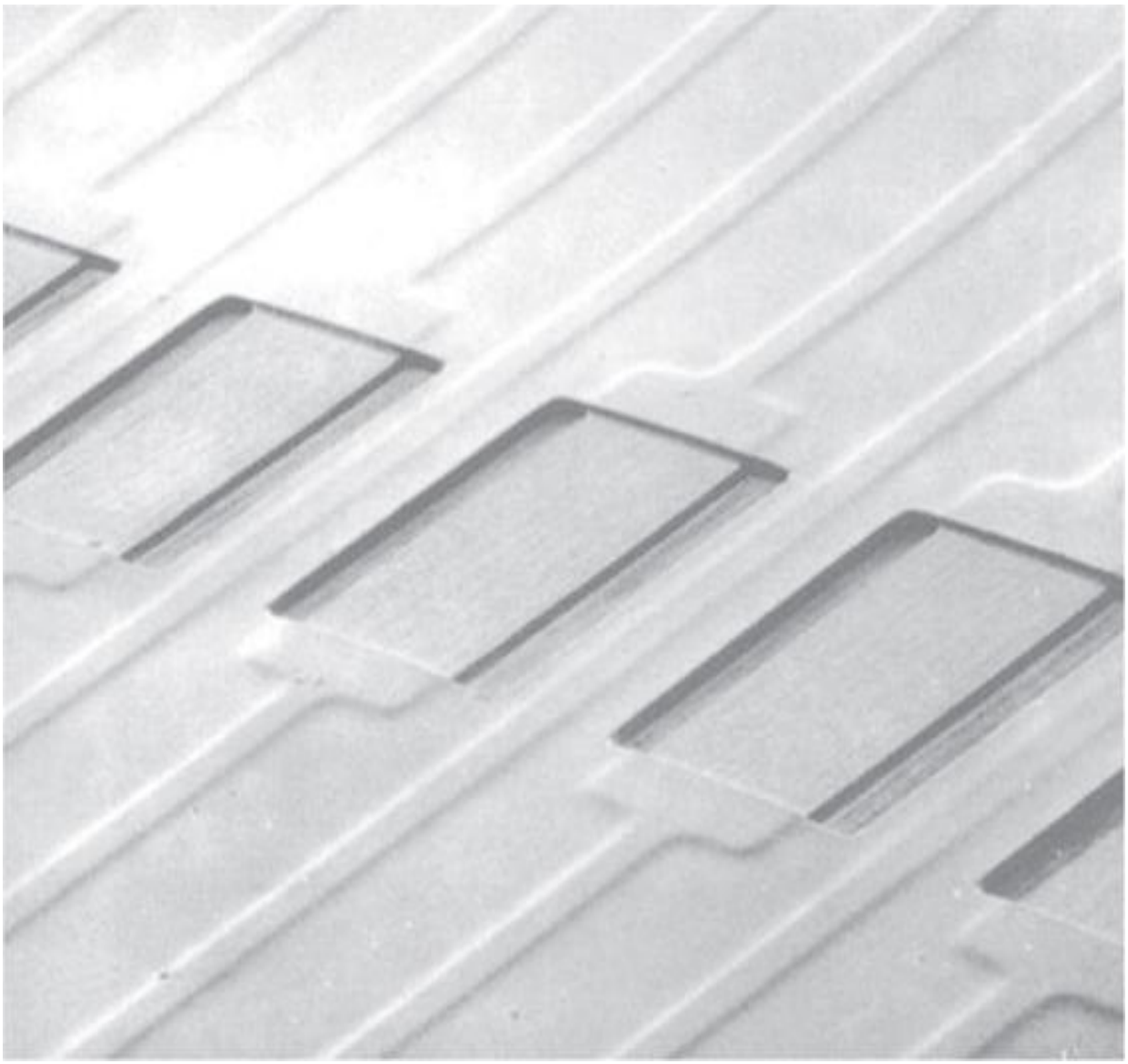


FIGURE 67.9 Photoimaged coverlayer defining terminations on flex. Lead pitch is 500 µm.

67.4.4 Laser Drilling on Film Coverlay

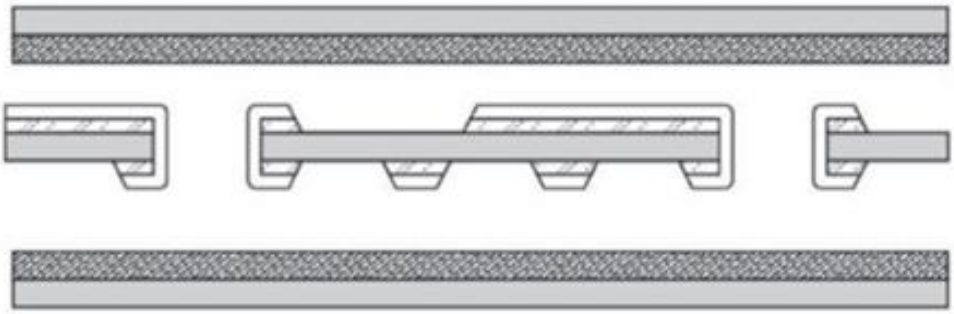
Lasers have seen a significantly increased in use in the processing of rigid printed circuits. The primary use of lasers has been to make small holes in circuit material. Depending on the thickness of the material small through holes can be

made with significant success; however, the major interest for the use of lasers in printed circuit manufacture is to make blind vias. Thus it should come without surprise that lasers have been adapted to the manufacture of flexible circuits especially in the ablation of polymer materials and most especially in the ablation of polymer materials over features of interest such as is common in the use of coverlayers.

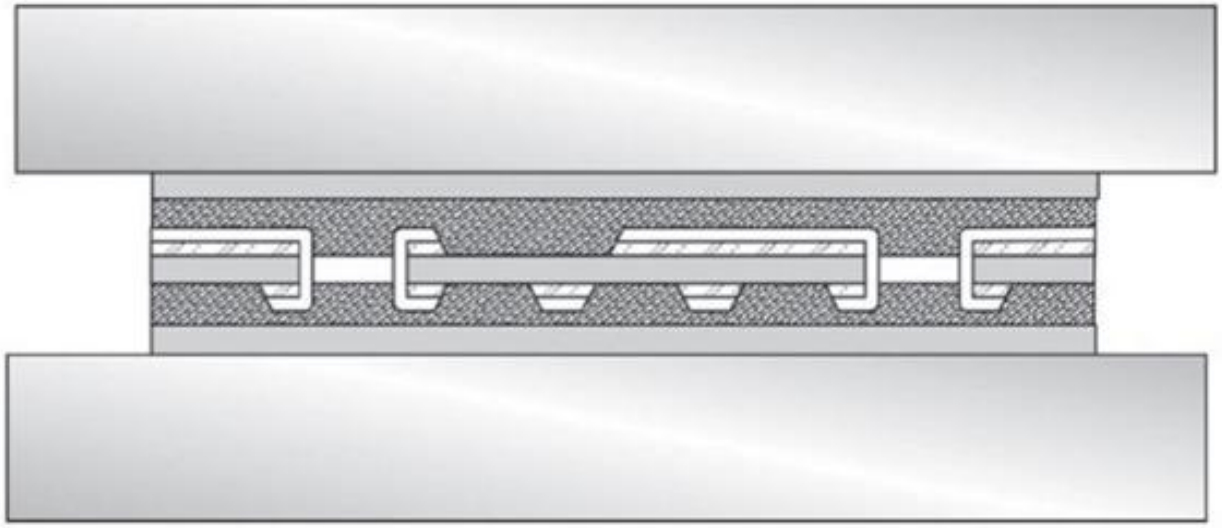
One of the advantages of using lasers to ablate polymer is that it obviates the need for a number of process steps required by the photoimaging process. In this regard they are well suited to the manufacture of prototype circuits or small volume production runs.

Another advantage of lasers is that they have the ability to ablate very fine features as might be required by some designs that the traditional photoimageable polymer approach cannot accomplish. For example, excimer lasers can provide extreme detail openings with feature sizes down to 50 μm and less leaving a clean surface behind. Other lasers including CO_2 and YAG lasers are equally capable of ablating polymer materials and/or an order of magnitude more effective in terms of rate of material removal but often require additional steps to remove char and other residue from the underlying copper surface.

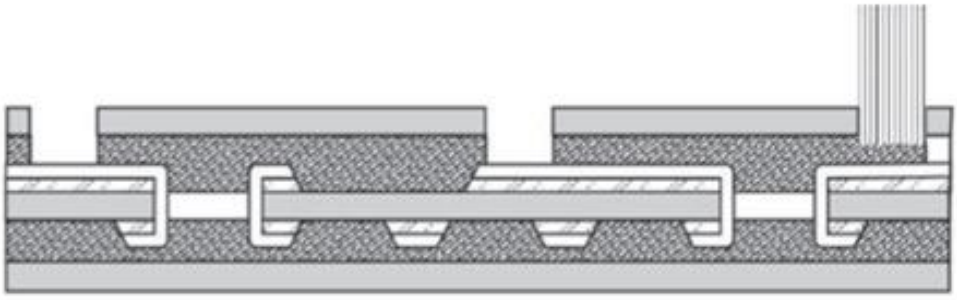
Again while excimer lasers provides excellent results in many applications the ablation rate, depending on the thickness of the material, can be appreciably slower than alternative lasers and are thus best suited to unique applications. The basic process as illustrated in Fig. 67.10 and a photomicrographs of an excimer laser ablated hole and a CO_2 laser ablated hole can be seen in Fig. 67.11. Finally it is worth remembering that lasers can perform other tasks and can, for example, also be used to cut the circuit from the flexible panel.



Sheet coverlayer to top and bottom of circuit



Laminate using heat and pressure



Laser ablate coverlayer material
from features of interest

FIGURE 67.10 Flowchart of process for laser drilling of film coverlay.

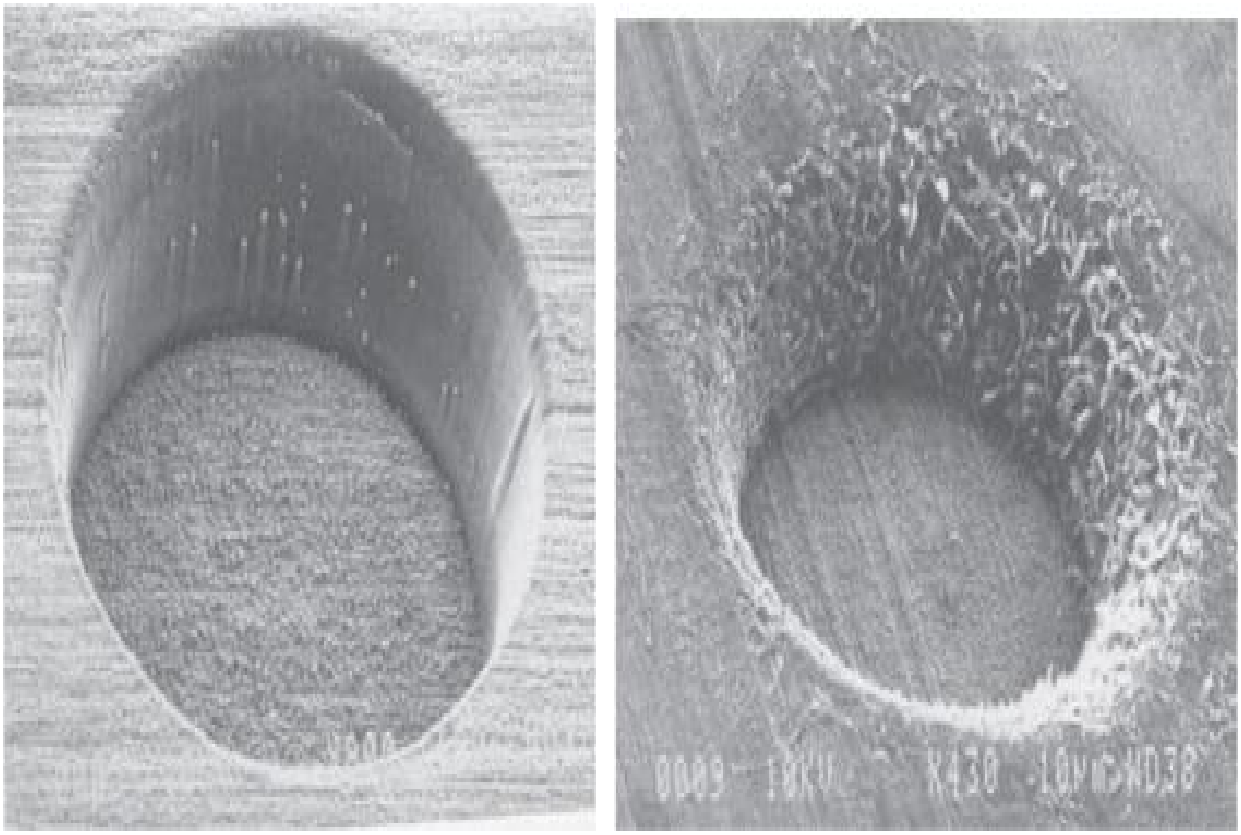


FIGURE 67.11 Small coverlay openings drilled in a polymer material using different types of lasers using different types of lasers. On the left above is a hole drilled by an excimer laser and on the right. Hole drilled using a CO_2 laser. Hole diameters are 100 µm and 200 µm, respectively. (*Source: Shinozaki*.)

67.5 INTERCONNECTION SURFACE TREATMENTS

Regardless of the method used for creating holes in the coverlayer the exposed copper surfaces normally require some additional treatment either to preserve the solderability of the feature as in the case of land pattern is for electronic components, or to assure a reliable contact surface on terminations designed for interconnection by electromechanical connectors or to provide a surface for wire

bonding integrated circuit chips directly to circuit terminations. Both electroless and electrolytic processes are used to plate metals for these differing purposes.

Metals commonly used to protect solderability include tin, solder, and nickel-gold. Molten solder can also be applied to the surface by a roll tinning process. Hot air leveling processes can also be used. In such a process the circuit is first fluxed and then dipped into a molten solder bath using special fixturing. The finished circuit will emerge with all copper terminations coated with a solder alloy. The process is challenging because it is difficult to get a uniform finish over all of the exposed contacts.

OSP (organic solderability protectant) coatings are also common for flexible circuits because they are easily applied and provide good results. There are limitations in terms of the shelf life of such finishes, however. Moreover, given that many electronic assemblies have components attached on two surfaces, there is need for them to withstand more than one reflow cycle while maintaining their solderability.

Nickel and gold as mentioned above can serve multiple purposes. The gold plating used should match the purpose. In the case of a wire bonding application, the goal should be a soft gold and in the case of a contact surface for connector the hard gold is preferred. An electroless nickel-gold plating process is often used for plating exposed contacts through coverlayer openings. There are a number of purveyors of proprietary chemistries for this purpose. One should be mindful of the fact that certain chemistries, especially strong alkaline chemistries having a high pH, can attack both the polymer film and the adhesive used to bonded to the flex circuit. The chemistry formulator should be capable of providing proven recommendations relative to the processing. That said it is important to remove any stains or residues before plating with an electroless chemistry elsewise it is likely that skips in the plating will occur. In some cases the mechanical brushing step may be required

but if such is performed it should be done with care so as not to distort the circuit.

A summary of surface treatments for flexible circuits can be found in Table 67.3.

TABLE 67.3 Treatments for Exposed Connecting Metal Surfaces on Flexible Circuits

	Materials	Process Conditions
Electroplating	Ni, Au, Sn, solder, etc.	Wet process
Electroless plating	Ni, Au, Sn, solder, etc.	Wet process
Hot-air leveling	Solder	>260°C
Solder roll coating	Solder	>260°C
OSP	Organic molecules	Wet process

67.6 DEPANELIZATION OF FLEXIBLE CIRCUITS

As a final step in the process the flexible circuits must be removed from the panel on which they were fabricated. The final step is commonly referred to within the circuit manufacturing industry as depanelization. Flexible circuits are often designed with fanciful contoured shapes with many curves, thus removal of the circuit from the panel can be challenging if the method chosen is not well-suited to the task. That said, owing to their thickness flexible circuits can be depanelized in a number of different ways. For example, the prototype circuit could be cut from the panel by simply using household scissors (with great care, of course). In addition they can be cut out using and numerically controlled

table cutter such as is used in the sign industry. As mentioned earlier, a laser can be employed to cut the flexible circuit from its panel. It is even possible, though not common, to depanelized flexible circuits using a chemical milling process such as is used in the fabrication of tape automated bonding (TAB) circuits. Flexible circuits can also be depanelized en masse using an NC router, a method used daily in the manufacture of rigid printed circuits. However, the method most frequently used in too depanelize flexible circuits is punching or blanking as it is also known. A punching press similar to those used in the processing of rigid boards can be used for the blanking of flex circuits; however, again owing to their thinness flexible circuits have the added advantage that they can be punched using steel rule die technology in addition to the much more robust Class A punch and die set tooling used for rigid printed circuits. In addition due to their thinness press tonnage can be significantly less.

Steel rule dies are especially well-suited to flexible circuits and the tooling can be turned around rapidly. The only drawback of steel rule die tooling is that there is mention of accuracy is not as good as Class A tooling. Moreover, steel rule die cutters have a shorter operational life than Class A tools and the blades must be replaced with greater frequency. The comparison between steel rule die and Class A tooling is offered in Table 67.4. Figure 67.12 shows an example of steel rule die in Fig. 67.13 illustrates the operation of a steel rule die.

TABLE 67.4 Comparison of Punching Technologies

Items	Steel Rule Dies	Hard Tool Dies
Accuracy	~0.2 mm whole tool	~0.01 mm whole tool
Minimum hole size	3 mm diameter	0.4 mm diameter
Minimum slit width	Zero	0.5 mm
Minimum corner radius	0.5 mm	0.1 mm
Delivery time	Days	Weeks
Weight	Light weight	Heavy, lift required
Tooling cost	Low	High
Processing cost	Moderate (low rate)	Low (high rate)

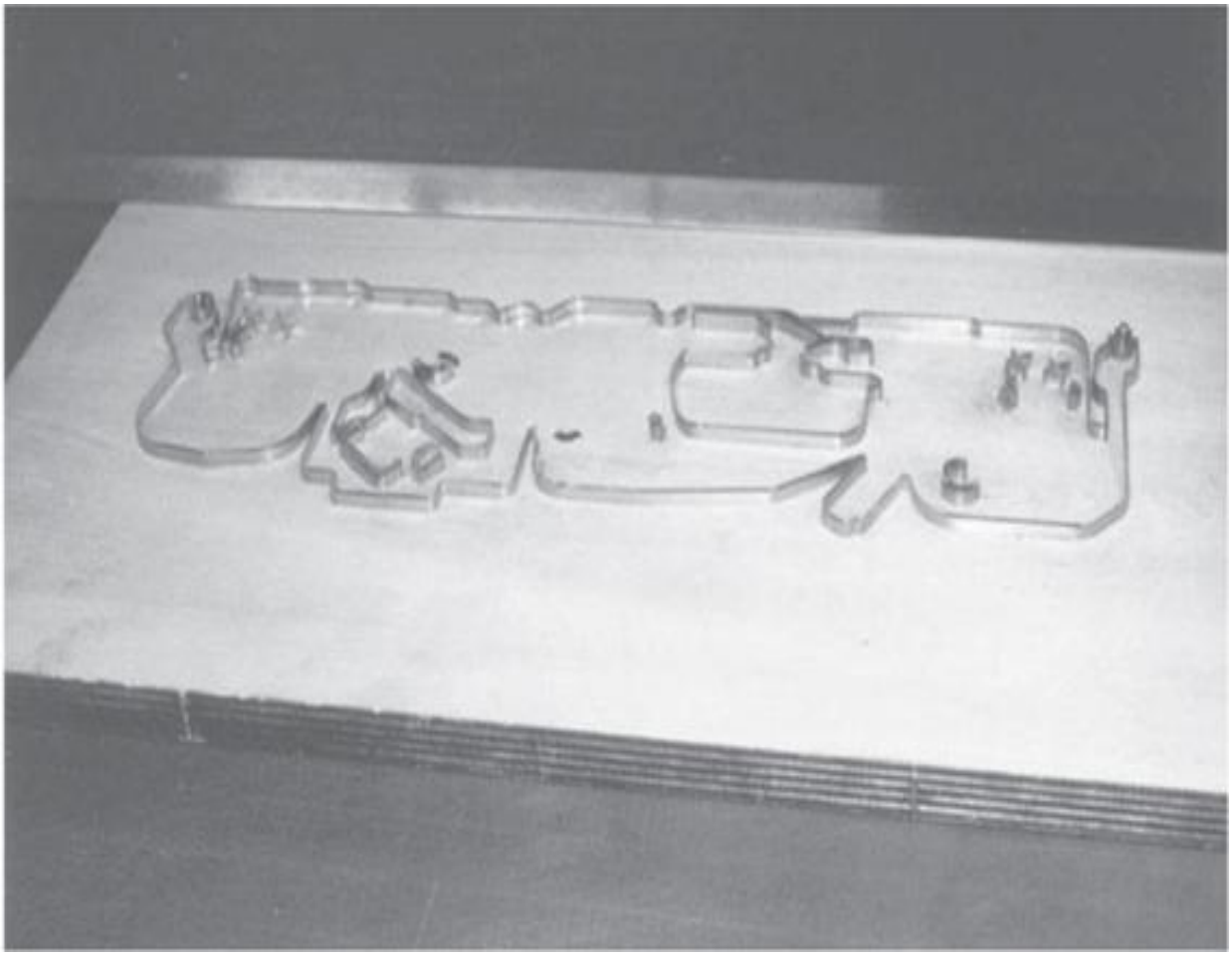
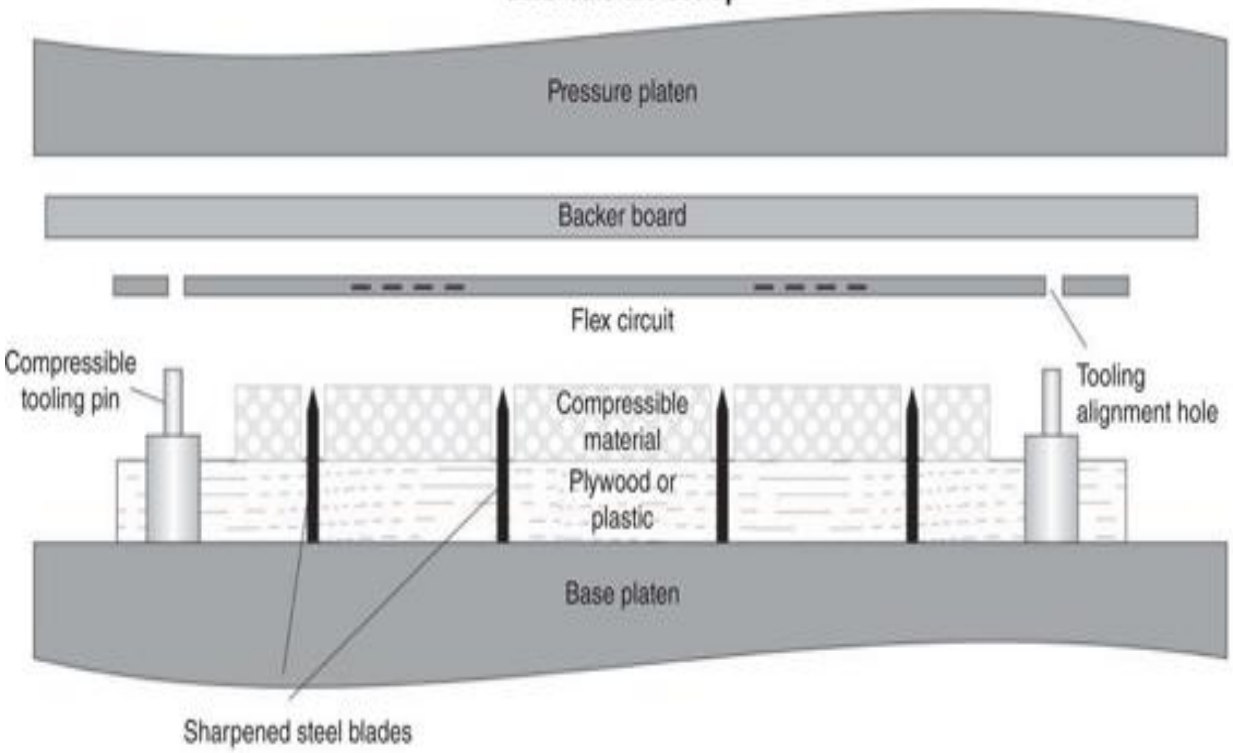
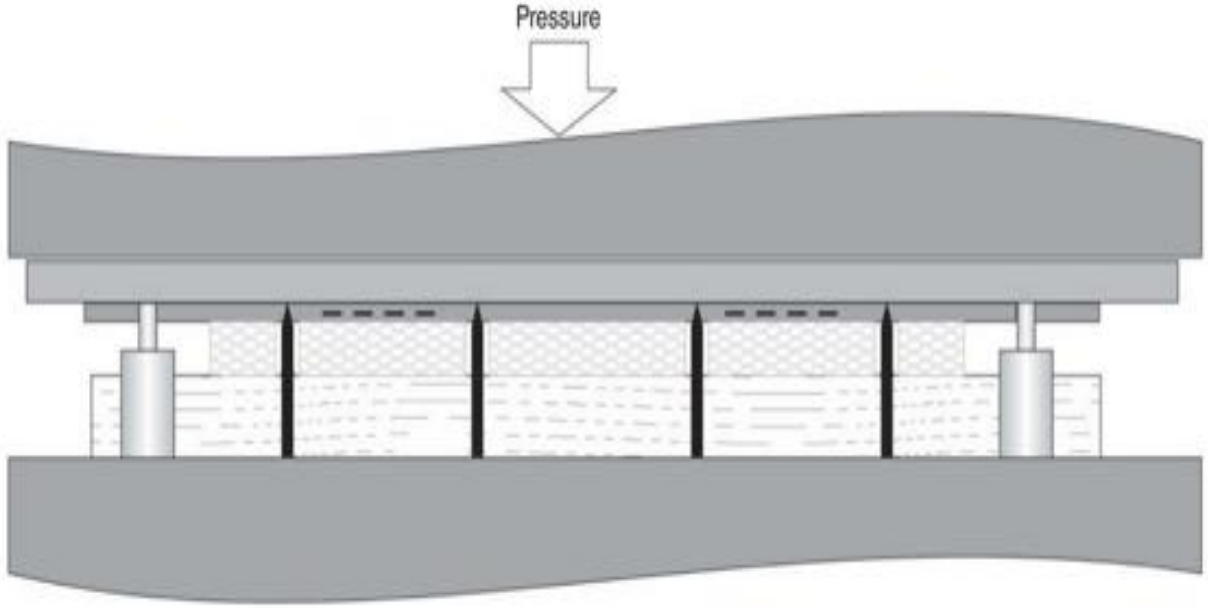


FIGURE 67.12 Steel rule die for blanking flexible circuits.

Steel rule die set-up



Steel rule die operation



De-panelized parts

FIGURE 67.13 Steel rule die set up and operation.

Tooling hole location accuracy is vital in ensuring that the circuit pattern and finished circuit outline are properly matched. Because, as has been pointed out many times earlier, flexible circuit materials are unstable dimensionally care is required both in design and in process. Some manufacturers have found it useful to provide several sets of tooling holes in the panel both outside and inside the circuit area. Such tooling holes are used only once in each process requiring their use. Some equipment suppliers also provide machines which have ability to identify and accurately punched through specially designed features on the panel through the use of CCD cameras. Such tooling methods facilitate punching of tooling holes with great accuracy (±50 μm) and as needed during processing and can as well even be punched after coverlayer lamination. Tooling holes punched after coverlayer lamination are well-suited to serving as alignment holes for depanelization of the circuits from the panel on which they were built. Figure 67.14 and Table 67.4 show the limitations of steel rule dies.

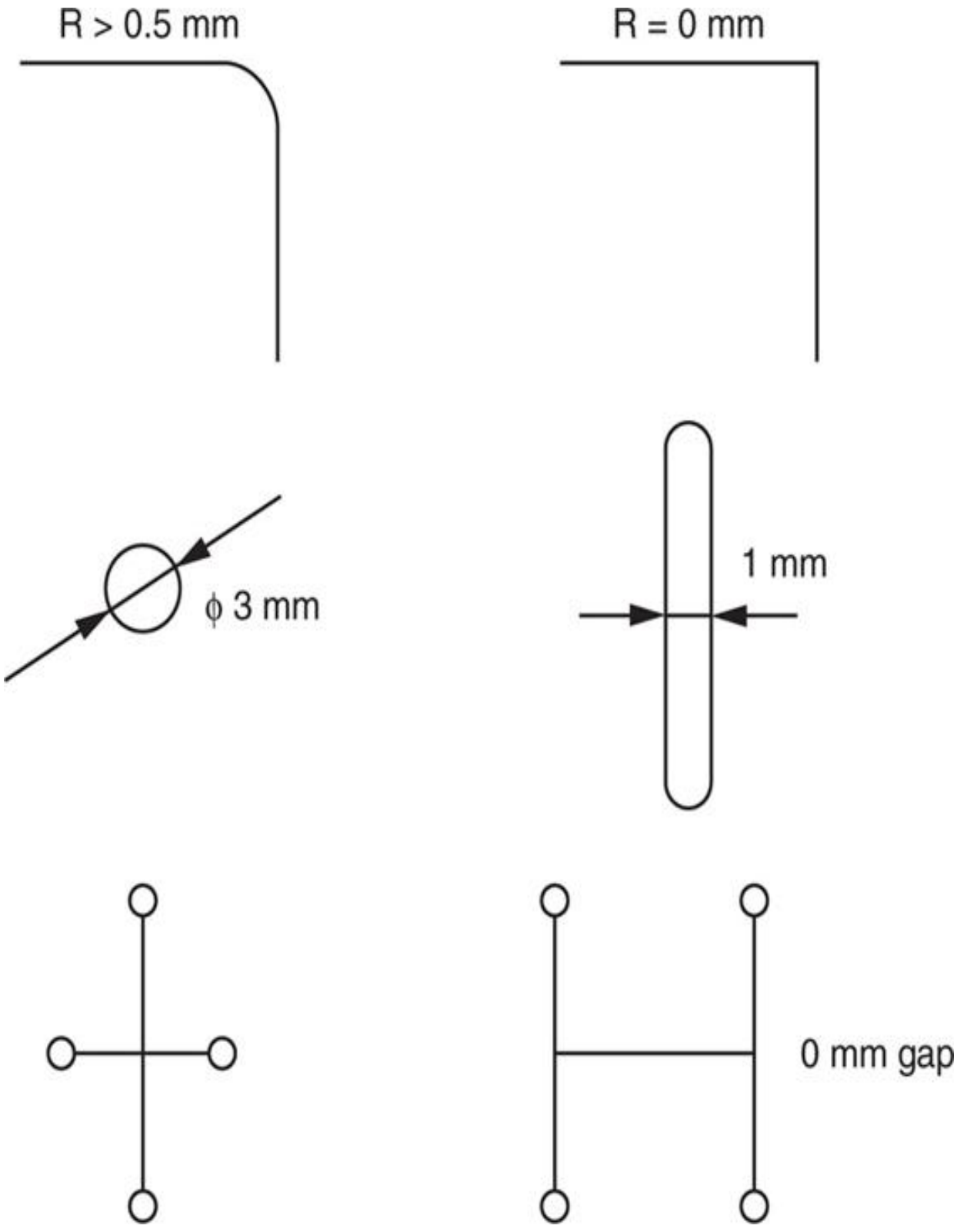


FIGURE 67.14 Limitations of steel rule die features.

67.7 STIFFENER PROCESSES

Stiffeners are a common feature on many flexible circuits. Their purpose is to support the weight of electrical components and connectors mounted on their surface or with component leads passing through the plated-through holes on the flexible circuit. Many different materials can be used as stiffeners including glass epoxy laminates, sheet metal, refractory materials, and even additional layers of the materials used in flexible circuit construction. Stiffeners are generally attached using an adhesive. Often the adhesive is pressure sensitive type, though thermally cured adhesives and flex circuit bonply materials may be used. Processing conditions and parameters should be in accordance with the manufacturer's recommendations.

Stiffener attachment typically involves touch labor and thus can add to cost. However, with judicious use of design it may be possible to offset cost by having the stiffener serve a dual function as a support carrier through subsequent assembly processes such as soldering. This is illustrated in Fig. 67.15.

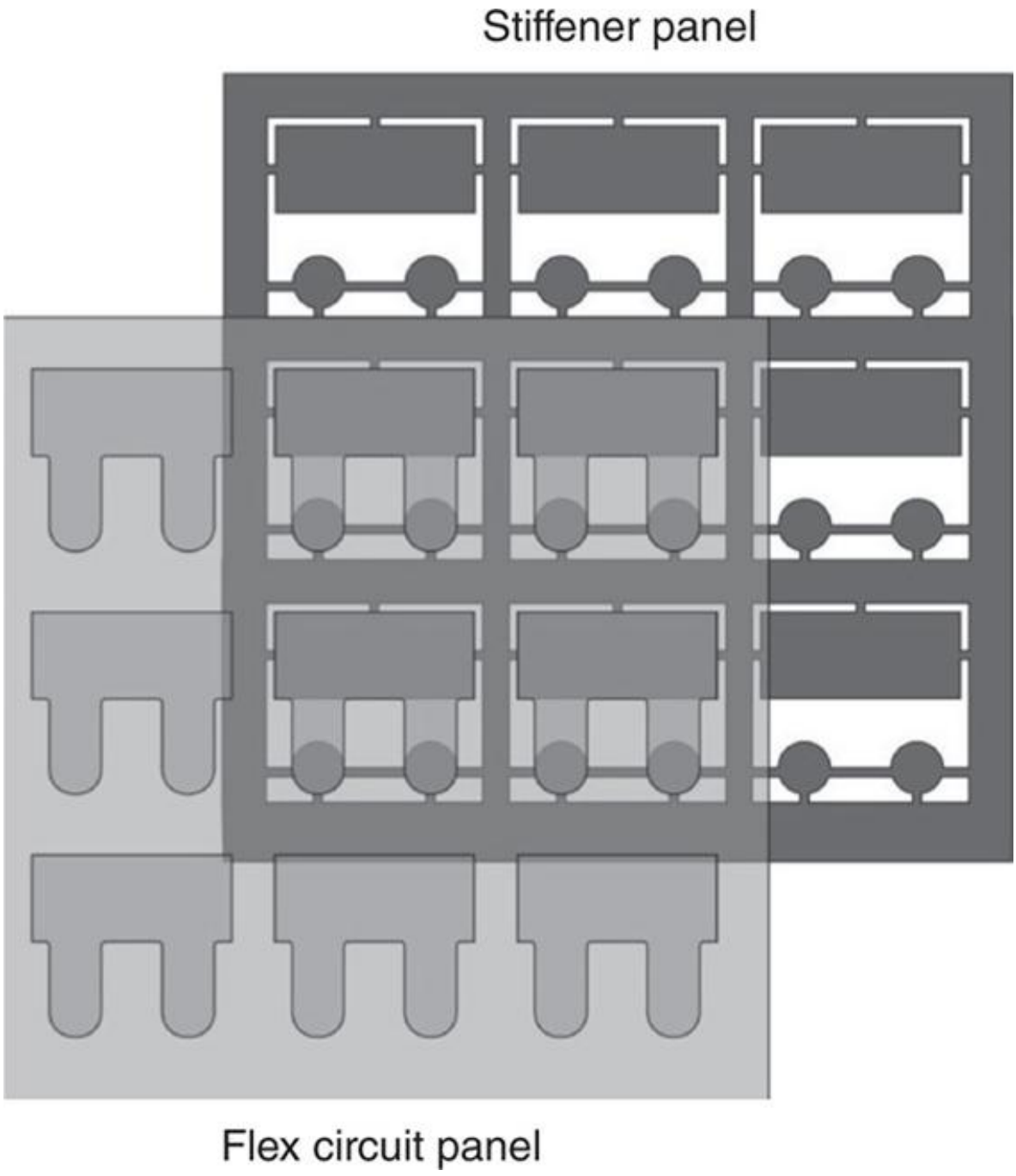


FIGURE 67.15 Flexible circuit panels and stiffener panels can be joined to facilitate mass assembly and separated afterward by cutting away tabs.

In high-reliability applications it is recommended that some matter of strain relief be employed at the transition from rigid to flex to avoid damage to the circuit. As illustrated in Fig. 67.16.

FIGURE 67.16 Methods for relieving strain from flex to rigid transition areas.

67.8 PACKAGING FOR FLEX

Over the years numerous approaches have been employed in the packaging of flexible circuits. There are a few important attributes which all suitable methods share. First they prevent the circuit from being deformed in transit or storage. This is not a function of simply making a flex circuit stay flat, in some cases the flex circuit is actually pretty formed into a shape by the flex circuit manufacture. Special fixtures are developed expressly for this purpose. Often he is employed at temperatures which are close to the glass transition temperature of the resin used and it is allowed to cool in place so that the shape is held. In such cases special packaging of a three-dimensional construct is required. More commonly, however, the flex circuits are shipped in a flat condition with or without stiffeners. Because many flexible circuit materials are hygroscopic and absorb moisture is important to make certain to the extent possible that they are well sealed with moisture impervious materials and perhaps as well with a desiccant to absorb any moisture within the packaging. This will serve well the needs of those in the assembly process as it will not only protect solderability but also help to prevent damage to the circuit during the soldering operation due to explosive outgassing of entrapped moisture. Where there is a good relationship between the manufacturer and the assembler it may be of

advantage to create or have made special containers for the flexible circuit which can be reused.

67.9 HIGH-DENSITY FLEXIBLE CIRCUIT MANUFACTURING

High-density flexible circuits are as the name implies a subset of traditional flexible circuits. High-density circuits are most often employed in high-end applications such as chip packaging, read-write disk drive heads and especially now for smartphones. The point of departure between the two is predicated on the circuit feature sizes. While there is no standardized threshold where circuit design crosses over from standard definition features to high-density features, most observers consider feature sizes under 100 µm to be within the domain of high density. This includes both circuits and through-holes. Because they are a subset there are some differences in materials and processing chemicals and equipment required to make these higher-density flexible circuits. Table 67.5 provides a listing of some of those process and equipment needs for making high-density flex circuits.

TABLE 67.5 New Manufacturing Technologies for High-Density Flexible Circuits

Processes	New Technologies
Raw materials	Stable polyimide film (~20 ppm CTE) Thin copper foil (9, 12 μm) Adhesiveless copper-clad laminates
Microvia hole drilling	Laser (excimer, UV:YAG, carbon dioxide) Microhole punching High-accuracy *x-y* table Plasma etching, chemical etching
Copper plating	Direct plating Seed layer sputtering
Surface cleaning	New cleaning reagent
Etching resist	Thin dry film (~15 μm) Liquid resist
Exposure	Collimated light source, auto aligner Laser direct imaging
Etching	High-resolution etchant
Coverlay	Laser drilling Photoimageable coverlay (dry film type and liquid type)
Surface finishing	Electroless plating for Ni, Au, solder High-speed plating
Flying leads	Laser/chemical etching Chemical etching
Guide holes	Automatic high-accuracy punching machine
Inspection	Universal AOI Noncontact electrical tests
Roll-to-roll system	Low-tension EPC system Automatic aligner with CCD camera

Leading-edge of high-density flexible circuit applications have features sizes with holes, lines, and spaces on the order of 20 µm and less. Some of the technologies that are used in the manufacture of high-density flexible circuits are relatively new while others are derivative of technologies which have been used for more than 30 years. In fact the general process flow for high-density circuits varies little from the process used for the manufacture of standard flexible circuits as is illustrated in Fig. 67.1. And most of the processes and process requirements described in the first portion of this chapter are not entirely different from those required for high-density flexible circuits. This includes material preparation cleaning handling system and the like. The major differences are in the basic materials used, the nature of the drilling process employed and some nuanced elements of process which allow for high-density circuits to be manufactured. This will become clear as a different processing methods are described and illustrated.

67.9.1 Imaging Processes for Making High-Density Flex

Making high-density flexible circuits requires both proper material selection and suitable processing methods. Thus one of the key elements required when it comes to making high-density flexible circuits is the base material, and more specifically the thickness of the copper which is bonded to the polymer. The etching process is an isotropic one thus during etching the copper is etched both down and laterally beneath the resist which defines the circuit features. Thus the thinner the copper, the easier it is to define a fine line feature this is illustrated in Fig. 67.17.

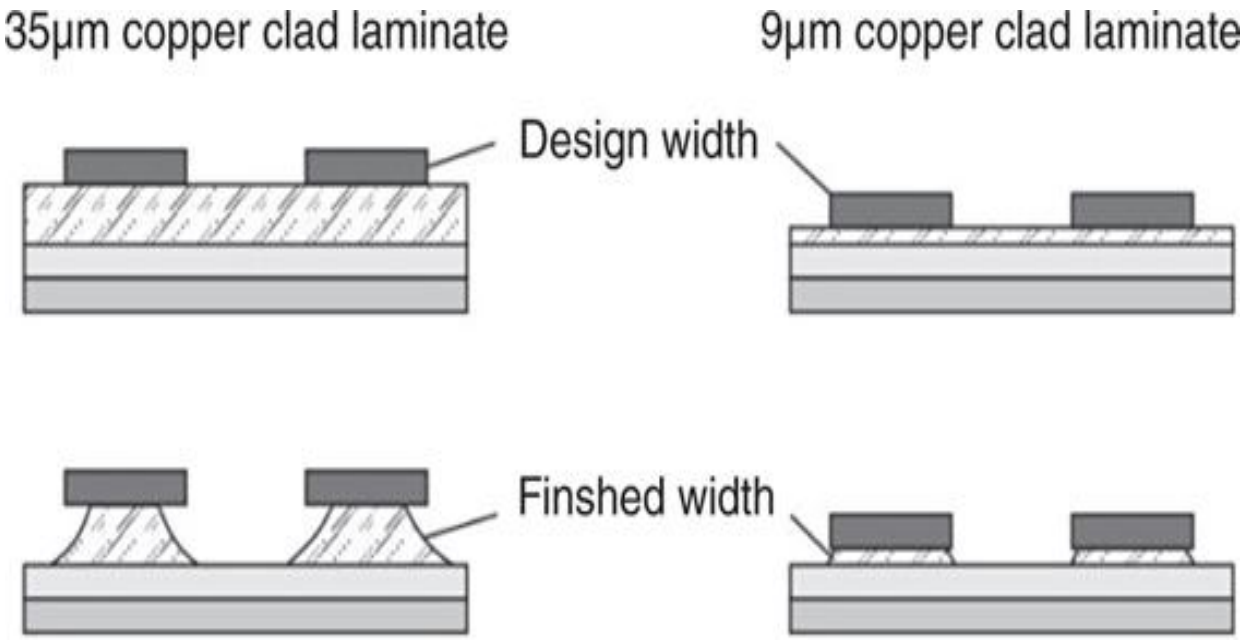


FIGURE 67.17 When the key requirements to making finer line circuits is to use their copper foil to begin with. The fact that etching is an isotropic process and that circuits are etched both laterally and down means in circuit features will take on a nominally trapezoidal shape with thicker copper. Within or copper the finished etched circuit is much more representative of the design.

However, no feature can be resolved at any yield without suitable processes and equipment. In that regard Table 67.6 is provided to alert the reader to the direct and ancillary processes and processing equipment that may be required to reliably produce the high-density circuits being pursued at high yield.

TABLE 67.6 New Technologies Needed to Generate Fine-Line Traces on Flexible Substrates

Processes	New Technologies
Surface treatment	New soft etching chemicals (organic)
	Sputtering of seed layer
Resist coating	High-resolution liquid etching resist and plating resist (spray coater, dipping coater, etc.)
	Thin dry film (~15 µm)
	High-sensitivity dry film with high resolution (10 mJ/cm^2)
	Wet laminator
Exposure	Collimated light source with glass mask (~15-µm line/space)
	Autoalignment system for double-sided circuits (with accurate dimension compensation system, ~5 µm)
	Roll-to-roll conveyor system with low tension
	Laser direct imaging system (30–40 µm line/space)
Etching	High-resolution etchant (cupric chloride, ferric chloride)

With the basic understanding of the fundamentals of making fine line circuits, as illustrated in Fig. 67.17, there are occasions when simple subtractive circuits will not work. Thus when current carrying capacity requirements are higher it is still possible to produce fine line circuit features. This is accomplished by patterning a thin client flexible laminate with a negative image of the circuit pattern and plating up copper within the channels. When plating is complete the resist is stripped from the panel and panel is etched. In the process some of the plated copper is removed at the same time as the background copper. While the features may be nominally diminished in size the process can characterized and modified to meet the needs of almost any circuit

requirement. The general process as illustrated in Fig. 67.18 and a circuit pattern representative of the potential features possible is shown in Fig. 67.19.

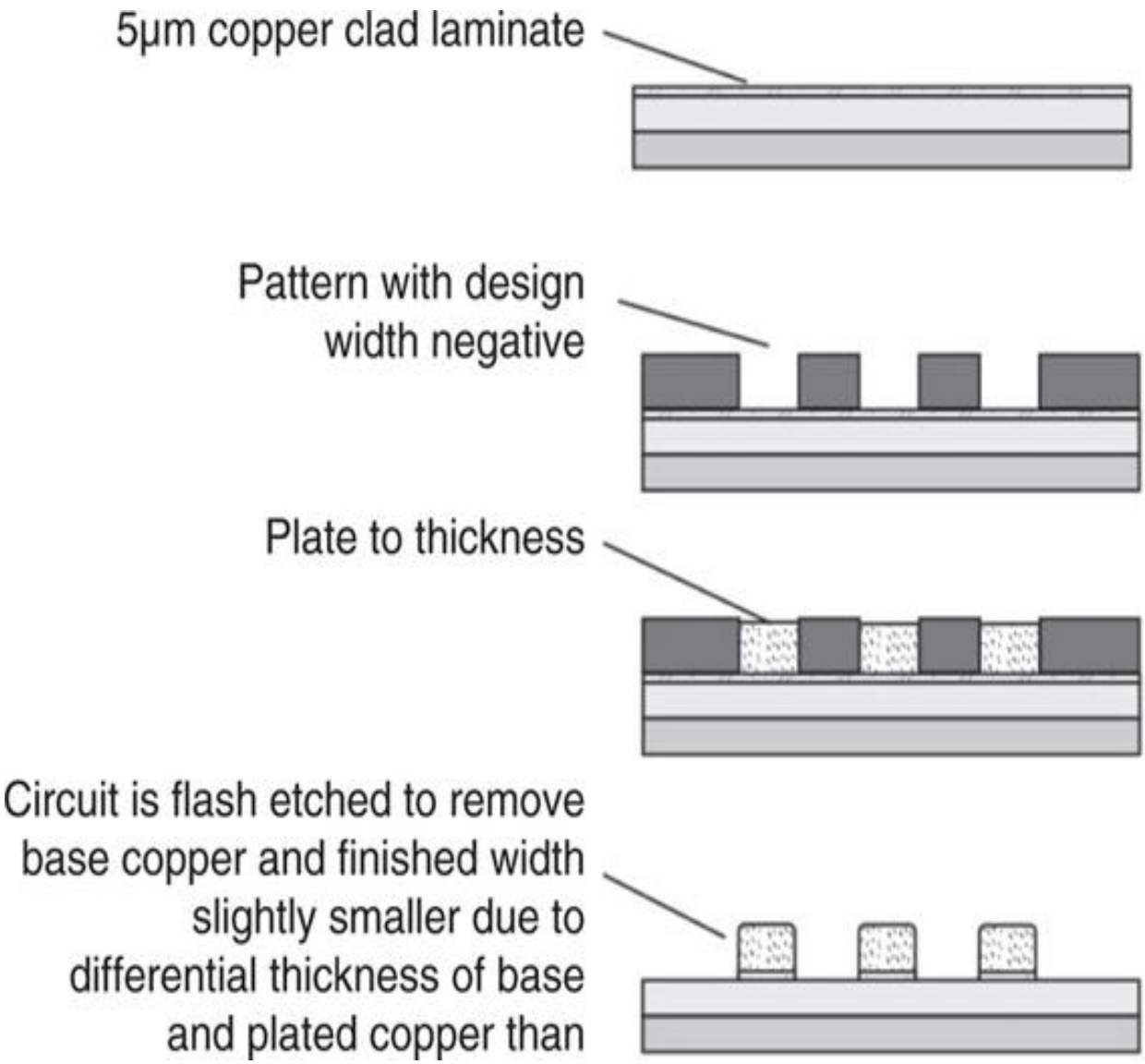


FIGURE 67.18 Illustrated above are the process steps for making a semi-additive or semi-subtractive circuit.

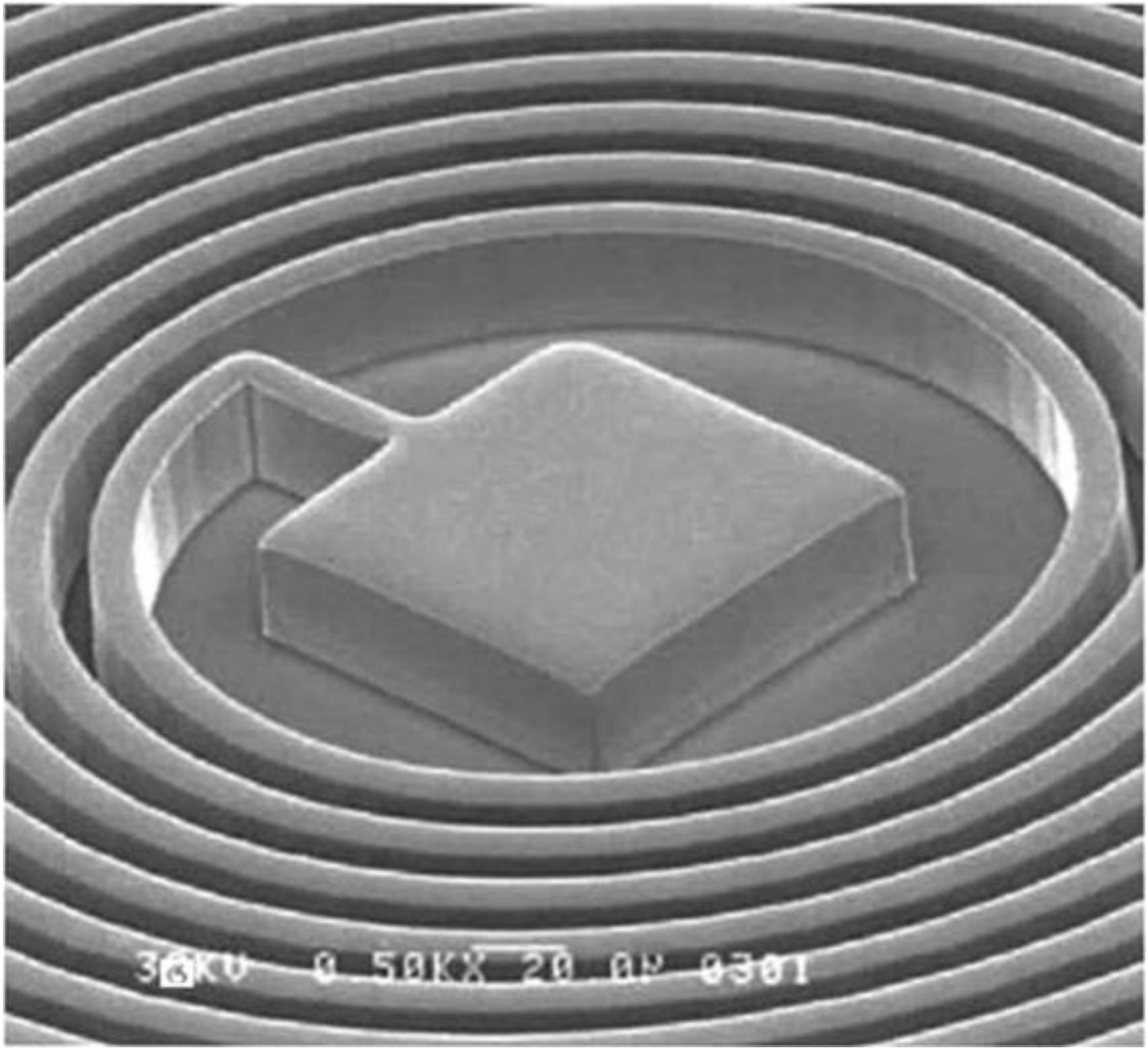


FIGURE 67.19 Shown above is a photomicrograph microscopic inductor. The nominal trace with of the conductor is 10 µm while the nominal thickness is 25 µm.

While there are more exotic ways of creating fine line features for flexible circuits these two methods, subtractive, and semi-additive, generally dominate. While rigid circuits have been produced using a full build electroless copper on a catalytic substrate the approach never found much favor in the flexible circuit world due to the fact that the mechanical properties of the electroless deposits were not well suited to flexible circuit applications. There is, however, an additive

method which has seen some commercialization in flexible circuits. Method is one which employs inkjet technology to deposit a catalytic material onto the surface of bare polymer. The patterned polymer is then immersed in an electroless copper solution wherein copper metal is reduced on the catalyzed surfaces only providing a copper circuit. The process as illustrated in Fig. 67.20.

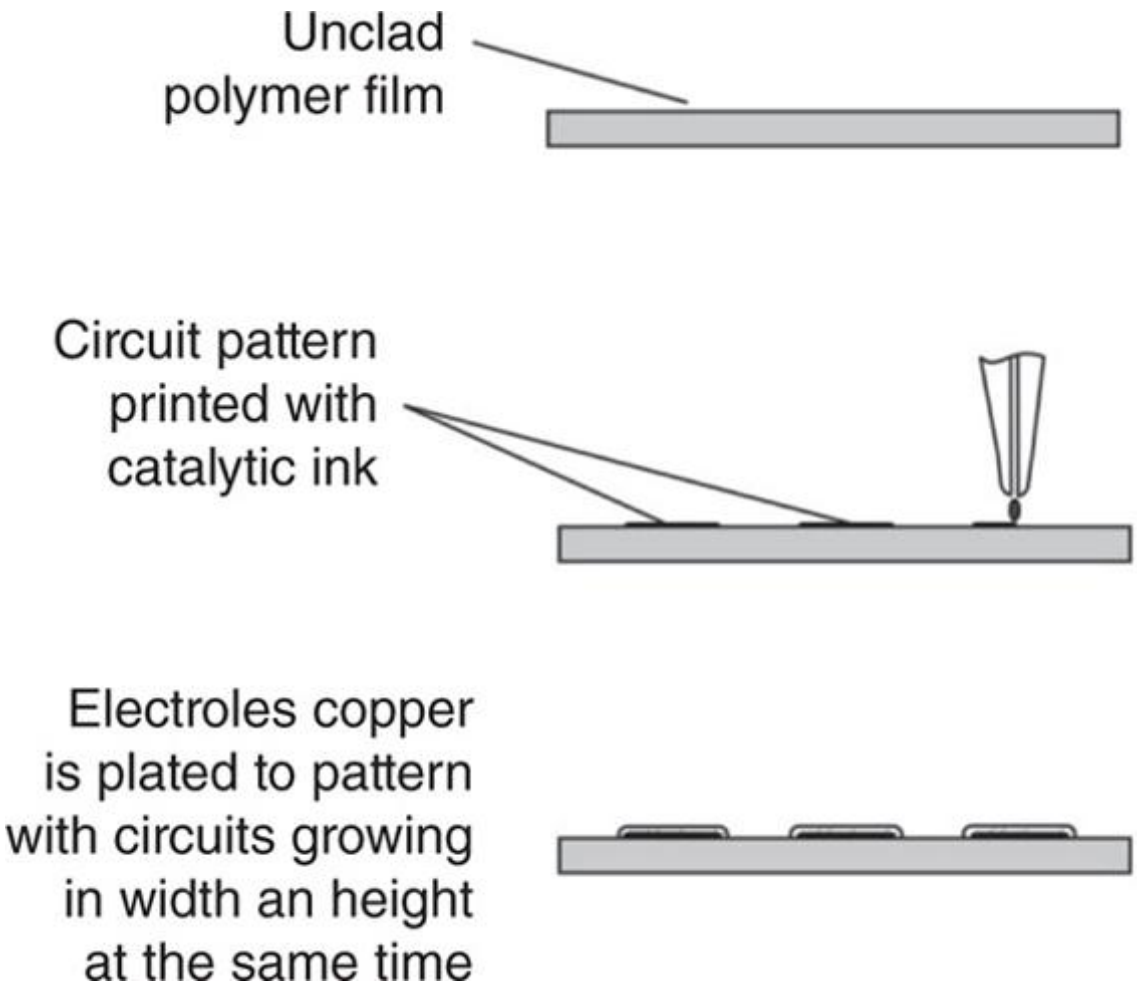


FIGURE 67.20 Above are illustrated the process steps for inkjet printing and electroless plating of catalytic ink circuit patterns.

The last method for making fine line features and circuits is one which has been employed by the semiconductor industry. It is referred to as a resist liftoff process. The method involves coating and patterning a substrate, in the

present case polyamide film, with a resist. The material is then sputtered with copper metal, which is normally preceded by deposition of an angstroms thick layer of nickel and chromium to improve adhesion of the copper to the polymer film. Because sputtering is a nominally “line of sight” process little copper is deposited on the sidewalls of the resist. Thus when the resist is removed the copper deposited on it surfaces is removed at the same time, leaving a thin copper circuit pattern on the polymer film. The processes generally referred to as a “liftoff process.” Again this is not a common method but if one has the equipment that represents an alternative approach. Moreover it is not well-suited to producing circuits with large unmetallized areas. In such cases it may be necessary to abrade the copper surface deposited on the resist to provide the stripping solution better access to the resist.

In concert with all the other methods just described there is one other worthy of inclusion that is particularly well-suited to flexible circuit applications this technique is often called “button plating” or “holes only plating” is a process wherein holes are drilled and plated through in advance and a second imaging step is used to etch the circuit pattern. This helps to keep the copper thin everywhere except in the through-holes and the vicinity of them. The process as illustrated in Fig. 67.21.

Copper clad laminate

Drill through holes and see with copper

Pattern circuit through holes

Plate through holes to thickness required

Strip resist from panel

Image circuit pattern covering holes

Etch circuit pattern

Strip resist to expose thin base copper

FIGURE 67.21 Above is illustrated the processing steps for making a button plate circuit and method which allows the base copper to be at its nominal thickness while providing robust plated-through holes.

67.9.2 Microvia Hole Processing for High-Density Flex Circuits

The other critical features relative to the manufacture of high-density flexible circuits are the micro via holes that are required to interconnect circuit features on different layers. The general discussion on hole formation provided earlier in this chapter provides important background which will be useful in understanding what follows. For purposes of this discussion microvias are defined as through-hole or blind features which are less than 100 µm in diameter. The methods used to create such features fall into three different categories. Holes which are produced mechanically, holes which are produced using photonics, and holes which are produced chemically either by means of a gas or liquid. Thus included in this discussion are all of the methods discussed earlier: mechanical drilling, punching, and laser drilling, and as well this section also includes discussion of liquid and gaseous methods capable of removing exposed polymer, especially polyimide, which is a dominant material used in high-density flexible circuit manufacturing. Table 67.7 provides a general overview of the different methods which will be discussed in the balance of this section.

TABLE 67.7 Comparison of Technologies for Hole Generation on Dielectric Layer

	Drilling	Punching	Laser Drilling	Plasma Etching	Chemical Etching	Photo Polymer Process
Hole diameter	~50	~70	~10	~70	~70	~70
TH for D/S	Yes	Yes	Yes	Yes	Yes	Yes
TH for multilayer	Yes	No	Possible	No	No	No
Blind via hole	No	No	Yes	Yes	Yes	Yes
Material choice	Wide	Wide	Wide	Fair	Small	Small
Technical flexibility	Small	Small	High	Fair	Small	Small
Chemical waste	No	No	Small	Small	Serious	Fair
RTR availability	No	Possible	Possible	Difficult	Possible	Possible

67.9.3 Mechanical Microvia Hole Creation

Drilling and punching of the two dominant methods of hole formation covered under the term “mechanical.” Punching is limited to through hole formation while numerically controlled drilling can be employed for making both through holes and in certain cases blind vias. Present generation numerically controlled drilling machines are capable of producing micro via holes smaller than 100 µm using specially developed drill bits. Some of the latest generation drills have demonstrated ability to drill 50-µm holes in 50-µm-thick copper clad flexible laminate. However, there are limits in drill stack height and thus productivity drops off wherein such small drill bits are used. Numerically controlled micropunching systems are also capable of producing small holes on the order of 70- and 25-µm polymer films at very

high rates. Multipin punch tool sets for predetermined patterns can greatly boost productivity when they can be used. Such tools have found utility in the manufacture of high volume real to reel circuit patterns such as are required for IC circuit packaging.

67.9.4 Laser Microvia Hole Creation

There are three predominant laser technologies used in drilling flexible circuits. They are excimer lasers CO_2 lasers and UV:YAG lasers. All technologies are capable of producing very fine holes on the order of 50 µm and less, though each has its own technical sweet spot. UV:YAG lasers, for example, have the ability to drill through both copper and polymer while excimers are best suited to drilling exposed polymer. Excimer lasers can, however, produce very fine features at high rates. Carbon dioxide lasers have the highest productivity when via holes greater than 60 µm in diameter are required. One of the challenges for CO_2 lasers was their inability to drill copper effectively; however, it was learned through experimentation that if the surface of the copper is given an oxide treatment before drilling both the copper and the base polymer can be drilled at once. This is especially useful in the formation of blind vias. In advantage of laser technology in general is that it is readily adapted to roll to roll processing. Examples of laser drilled features are shown in Fig. 67.22.

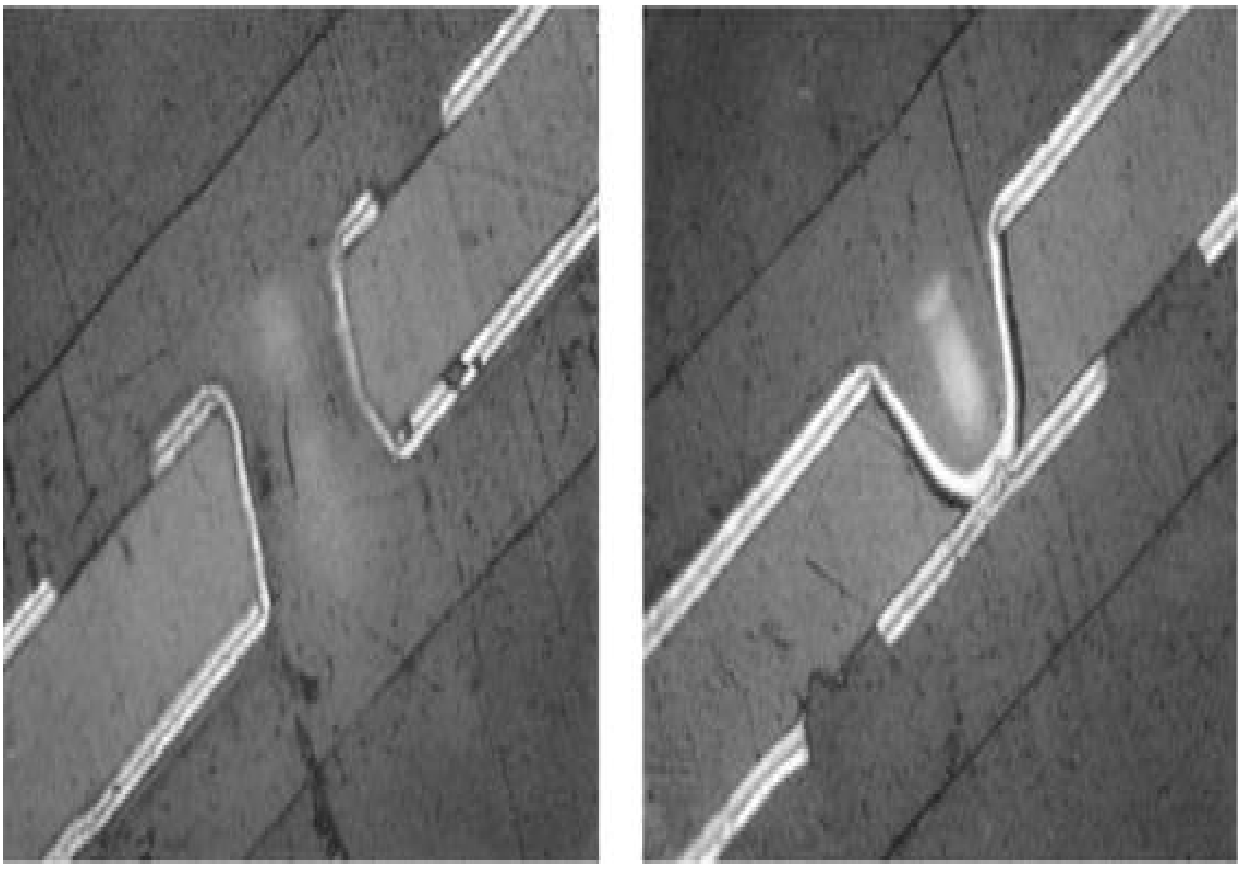


FIGURE 67.22 Examples of laser drilled through and blind vias in polymer film. Note that the features are over coated with a polymer to protect the circuit features.

67.9.5 Chemical Microvia Hole Creation

There are to primary chemical methods employed to produce microvias in flexible base materials. The two processes vary significantly in terms of their capital cost and processing methodology. The older of the two methods is chemical. Chemical etching of polymer is been used by the TAB industry for many years when it was learned that certain polyimide chemistries would etch readily in hot caustic solutions. Processing must be carefully monitored; however, as it is possible to leave residue in the holes which could obviate the making of an electrical interconnection to

exposed copper. In this regard, one of limitations of these types of processes is hole feature sizes in general either process is capable of producing features down to 100 µm in material 50 µm thick.

The other method for making microvias which is also arguably chemical in nature is plasma etching of microvias. The process is performed in a vacuum and a gas mixture comprise typically of CF4, oxygen, and nitrogen is excited by microwave generation to form a plasma which breaks down exposed polymers into fundamental hydrocarbons. While these two methods differ significantly in terms of their fundamental operation, both have distinct advantage over other methods in that a virtually unlimited number of holes can be made at one time. That is whether one etches just one hole or millions in copper clad flexible polyimide substrate, the processing cost is the same.

In this regard, both of the just described processes are best suited to the use of a conformal mask, which is fundamentally, where the copper cladding of the laminate is etched to expose the polymer where holes in the polymer are desired. The basic process steps are illustrated in Fig. 67.23.

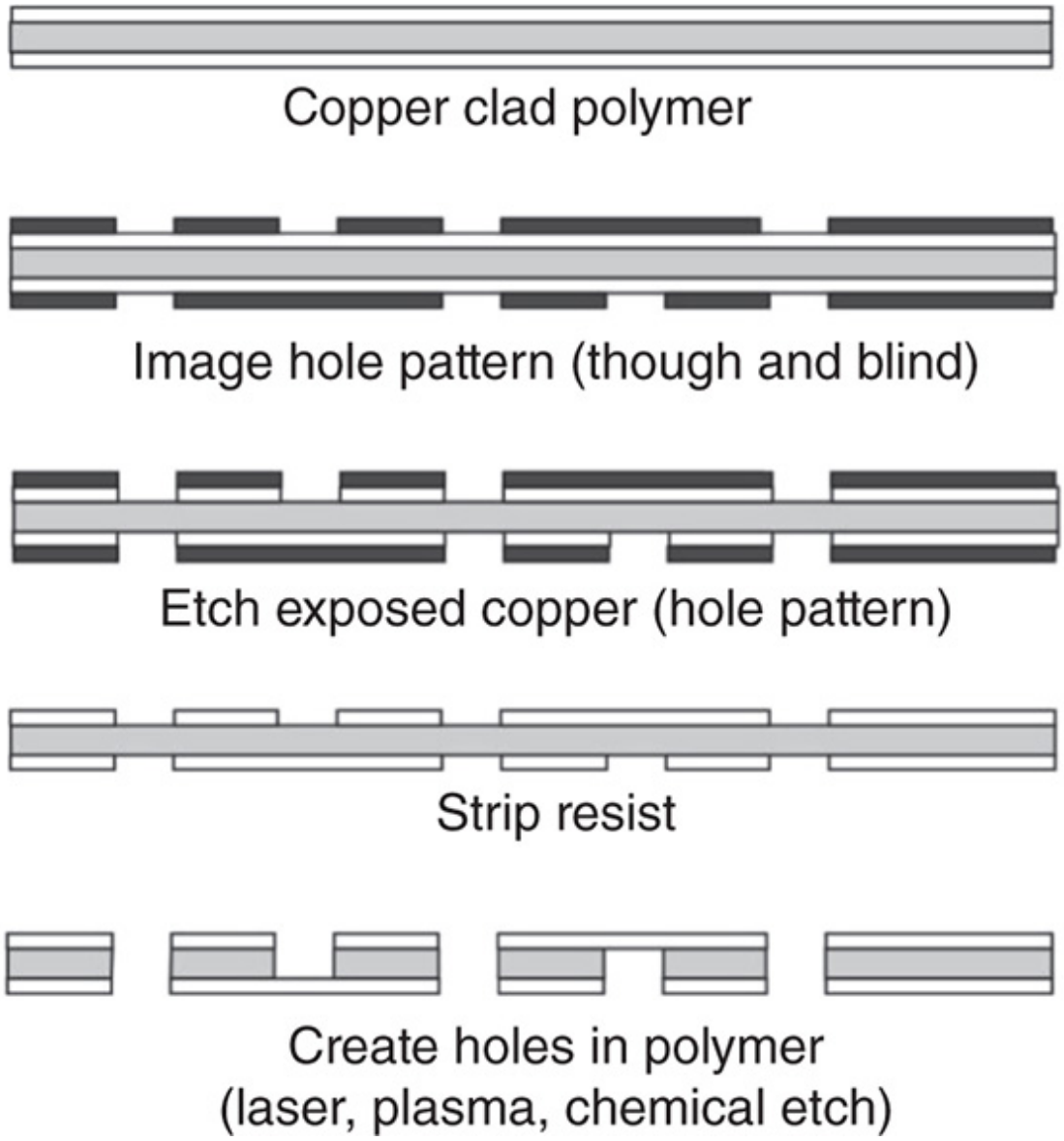


FIGURE 67.23 The conformal mask process is perhaps best suited to plasma and chemical etching of polyimide but can be used with lasers as well.

The difference between the two processes is that chemical processing must be tailored to the polymer and the most well suited to the process is polyimide. In contrast, plasma processing can breakdown almost any polymer so it has wider applicability where and when it may be required in certain special circuit structures. Finally one process attribute that is common with both is undercutting of the surface copper which can make subsequent processing more

challenging with regard to chemical solution exchange, where the metal lip is present. This effect can be seen in Fig. 67.24.

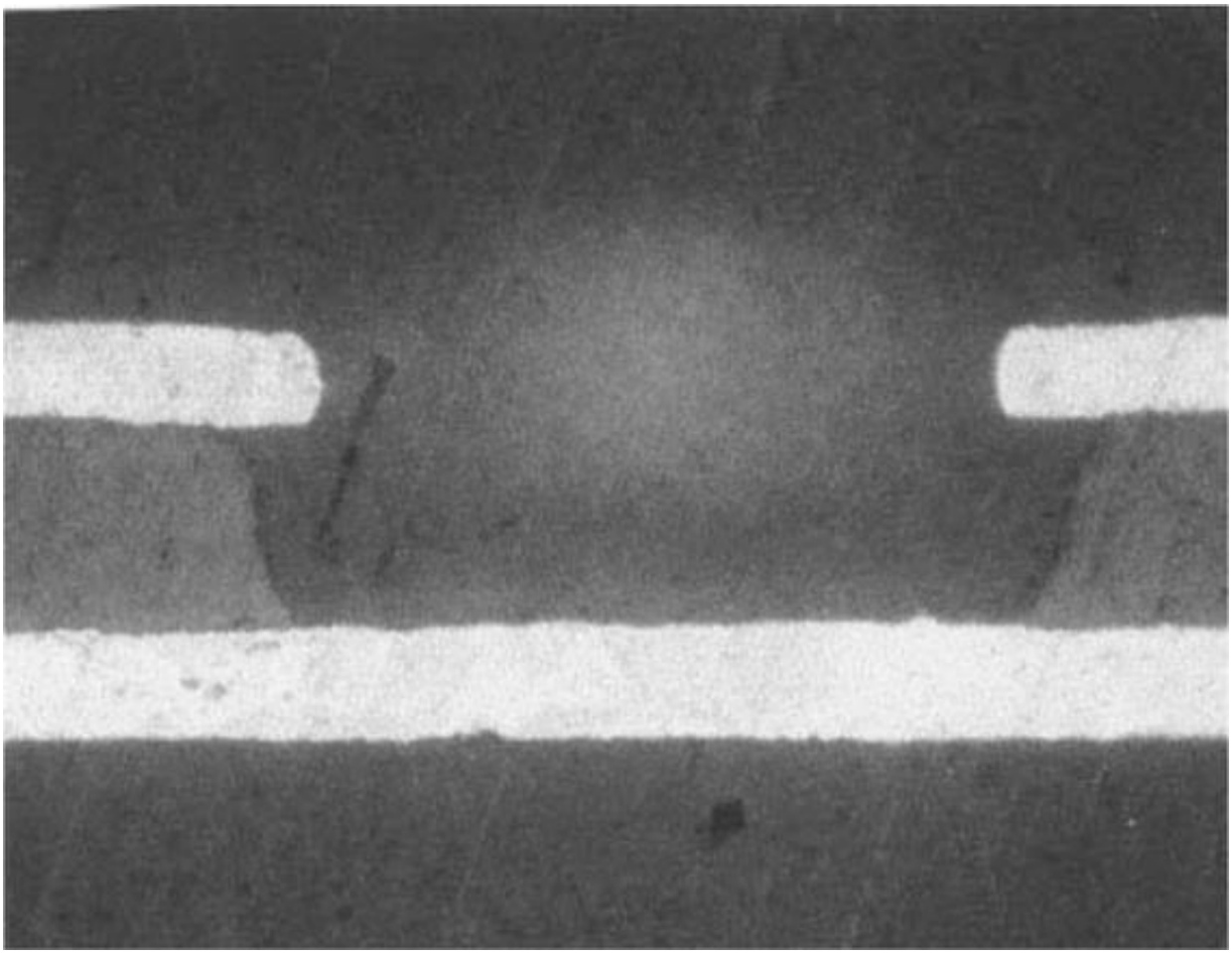


FIGURE 67.24 Microvia generated by plasma etching. The hole diameter is 200 µm. Note the undercutting of the upper copper foil.

With all three general approaches to hole formation in high-density flexible circuits, there are limitations in terms of their technical capabilities these are compared and contrasted in Table 67.8 and a graphic representation of the general capabilities in areas of overlap between the different processing methods is provided in Fig. 67.25. Finally a cost analysis of the various methods discussed for drilling holes using a common 50-µm base material is provided in Fig. 67.26.

TABLE 67.8 Technical Capabilities of Microvia Hole Technologies for Double-Sided Flex Circuits

	Excimer	UV:YAG	Carbon Dioxide	Plasma Etch	Chemical Etch
Hole size (μm)					
For small volume	~10	~15	~50	~70	~50
For large volume	25–150	25–75	75–250	~100	~75
Hole quality	Excellent	Good	Fair	Fair	Fair
Additional cleaning	Necessary	Necessary	Necessary	No	No
Technical hurdles	Low	Low	Fair	High	High
Cost	High	High	Fair	Low	Low

For only specific polyimide resins.

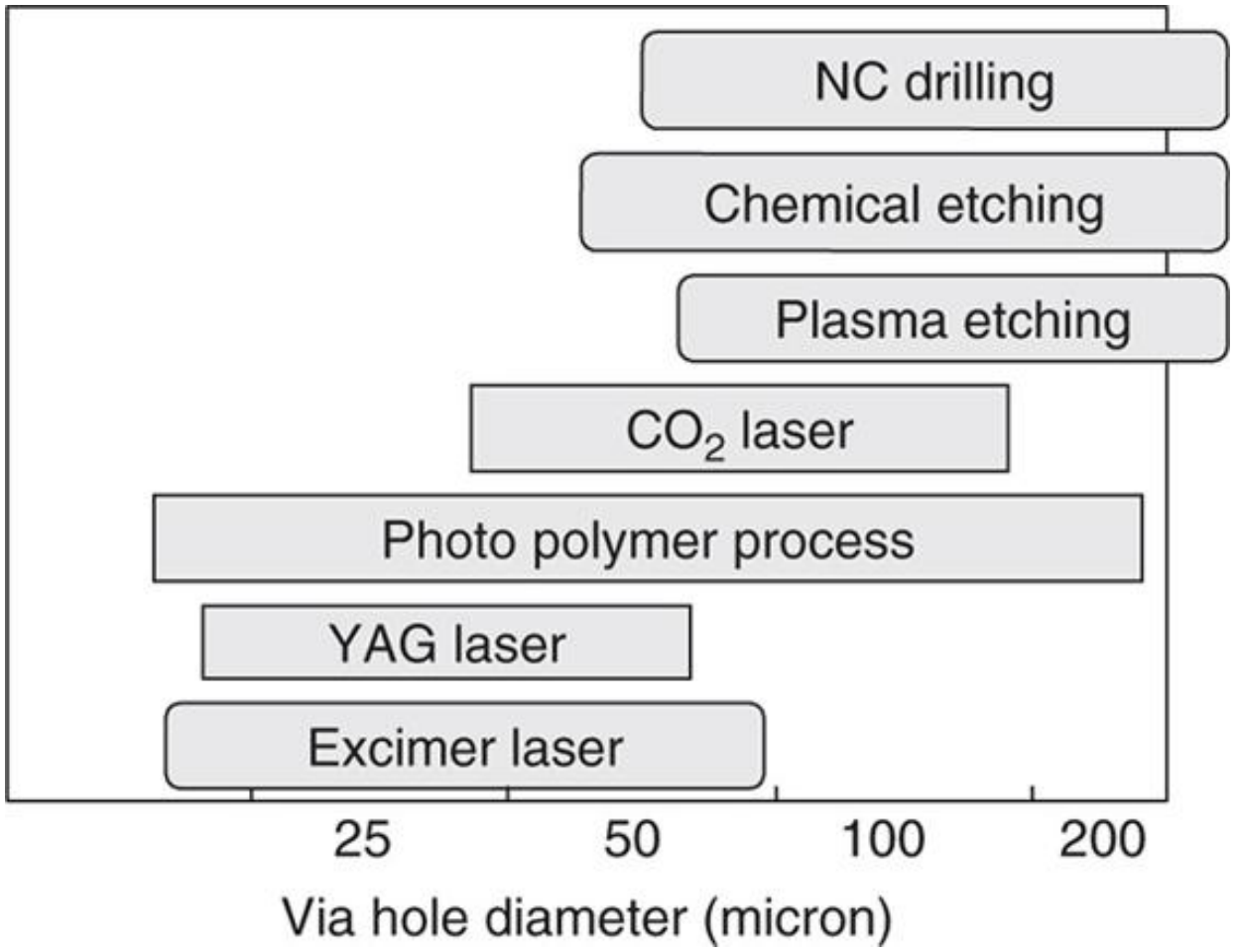
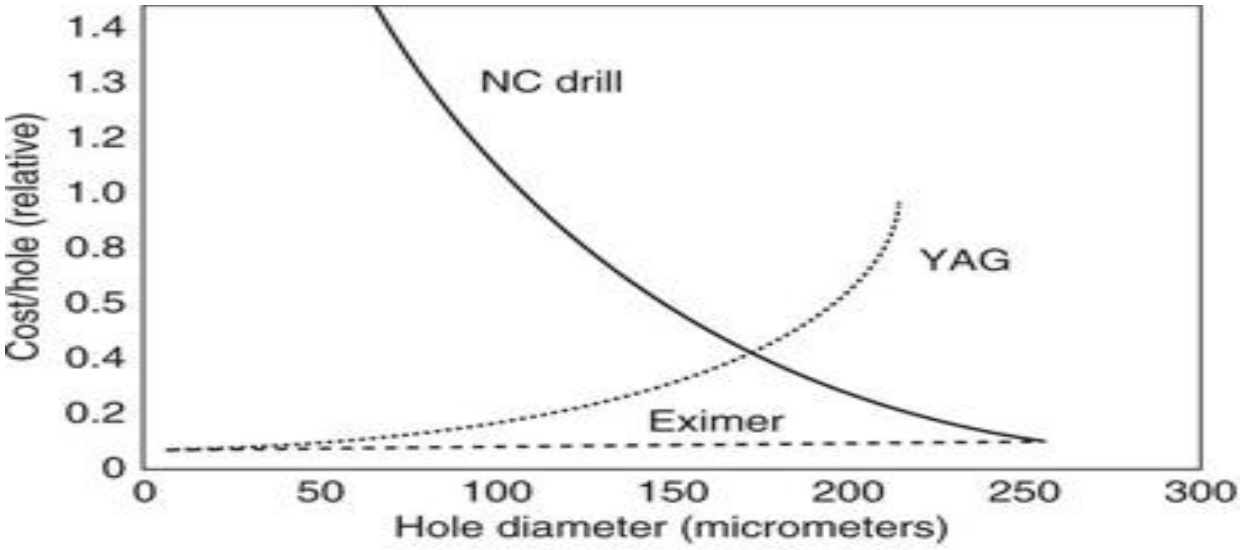
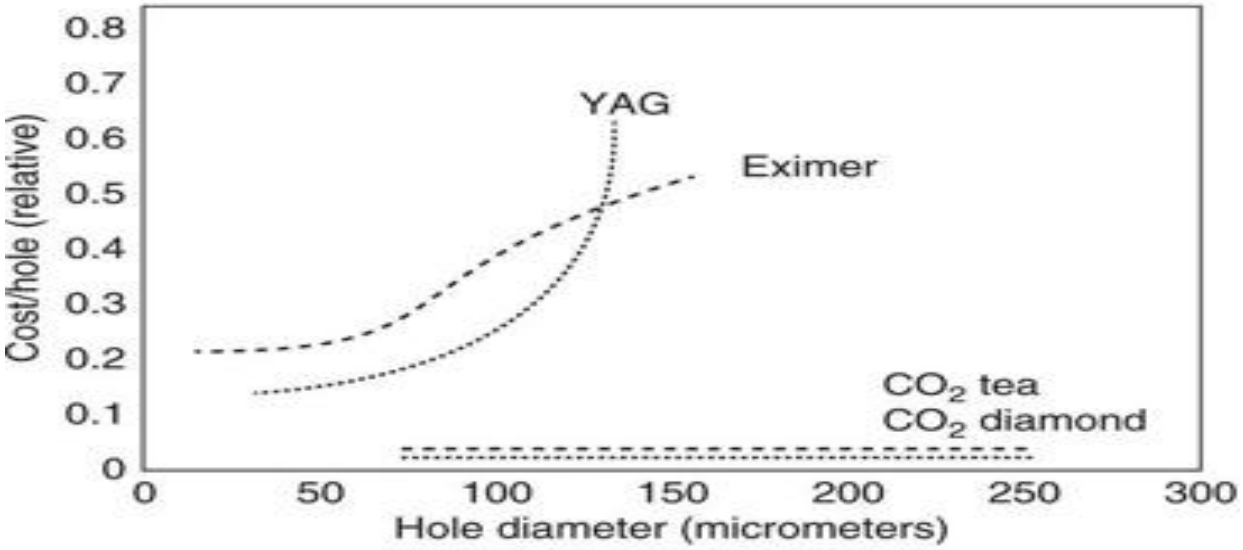


FIGURE 67.25 Microvia hole capabilities of the technologies.


Cost/hole (relative)
1.4
1.3
1.2
1.0
0.8
0.5
0.4
0.2
0
NC drill
YAG
Eximer
0
50
100
150
200
250
300
Hole diameter (micrometers)


Cost/hole (relative)
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
YAG
Eximer
CO_2 tea
CO_2 diamond
0
50
100
150
200
250
300
Hole diameter (micrometers)

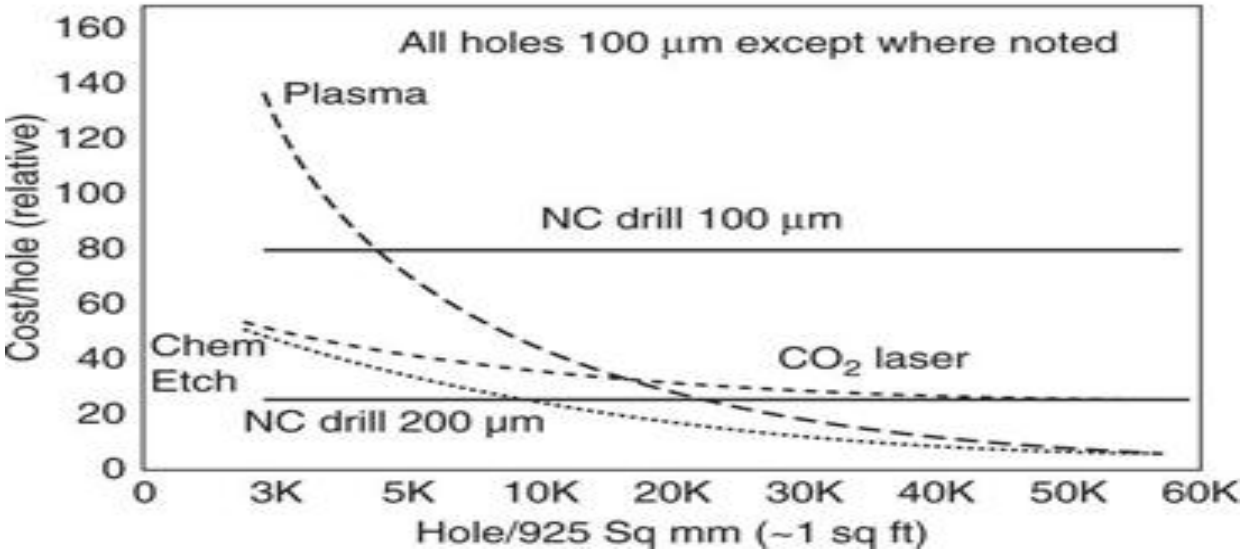

Cost/hole (relative)
160
140
120
100
80
60
40
20
0
All holes 100 μm except where noted
Plasma
NC drill 100 μm
Chem
Etch
CO_2 laser
NC drill 200 μm
0
3K
5K
10K
20K
30K
40K
50K
60K
Hole/925 Sq mm (~1 sq ft)

FIGURE 67.26 Provided is a general cost analysis comparing the various processing methods used for making holes and 50-µm-thick materials. (*After Numakura*.)

Having provided a reasonable overview of the processes used for making microvias in materials used for high-density flex, the adage "use the tool best suited to the task" is found to be no less true in the manufacture of high-density flexible circuits than it is in any other manufacturing discipline. With that in mind Table 67.9 is provided to give the reader an appreciation of which technology is best suited to the type of material being processed

TABLE 67.9 Material Processing Suitability

	Punching and Drilling	Excimer Laser	UV:YAG Laser	Carbon Dioxide Laser	Plasma Etching	Chemical Etching
Copper	Yes	Slow	Slow	No	No	Yes
Epoxy	Yes	Yes	Yes	Yes	Yes	Difficult
FR-4	Yes	Slow	Slow	Yes	No	No
Kapton/Apical	Yes	Yes	Yes	Yes	Yes	Yes
Upilex	Yes	Yes	Yes	Yes	Yes	Difficult
Espanex	Yes	Yes	Yes	Yes	Yes	Difficult
NeoFlex	Yes	Yes	Yes	Yes	Yes	Difficult

In summary the manufacture of flexible circuits, both traditional revenue center of gravity and leading-edge high-density structures is vital to the creation of new and useful products of every sort. While there similarities in processing and some areas of crossover between the two technologies

there are also definitely significant differences between the two. As a result, flexible circuit manufacturing is today split along technological lines. Both types of circuits will be required now and in the future and understanding the nature of the processes required to build both is important to the success of both the manufacturer and the customer. The final figure in this chapter (Fig. 67.27) is provided so that the reader can assess where their products present and future fit in the overall picture of flexible circuit manufacturing in the present day.

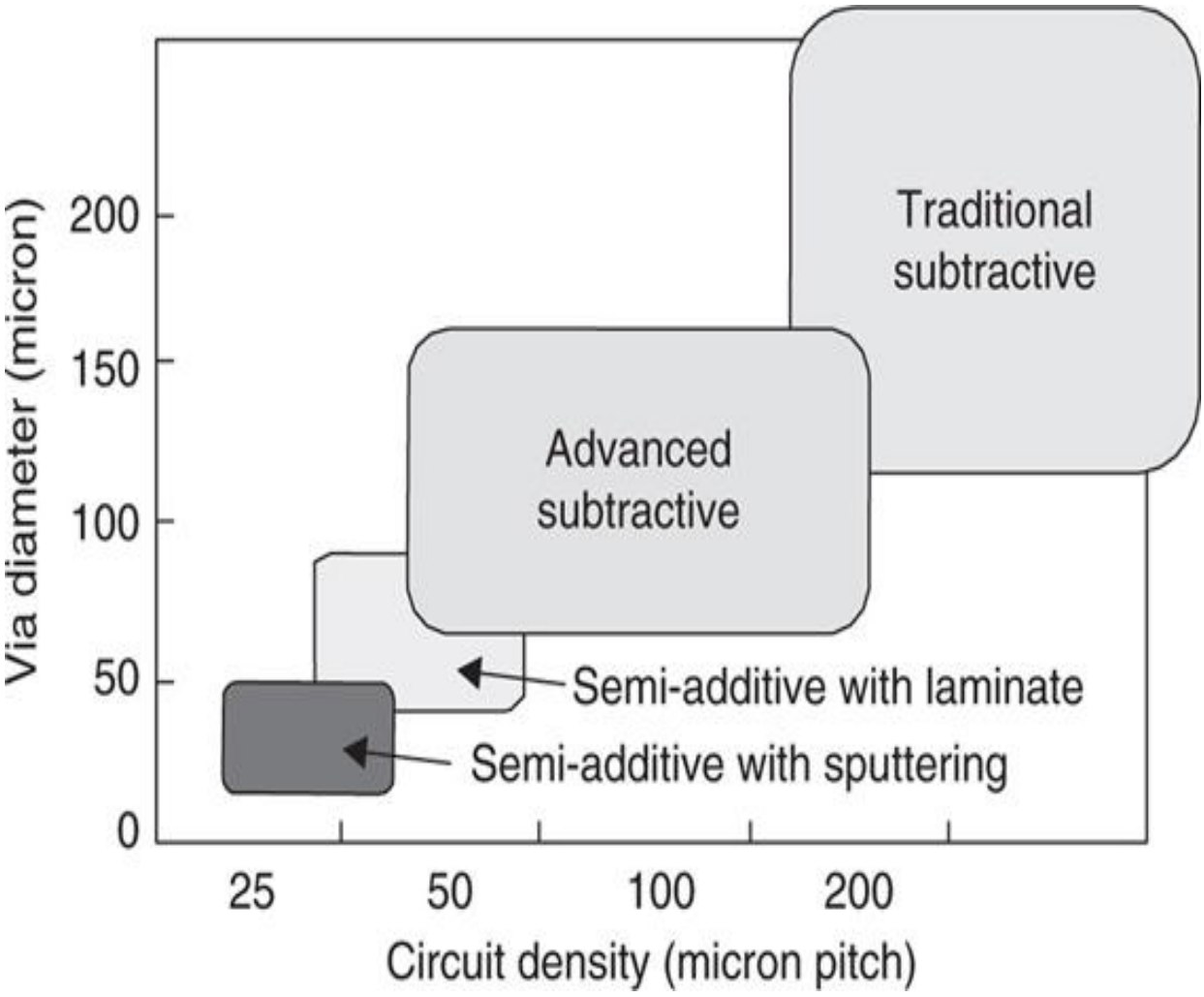


FIGURE 67.27 Total high-density capability.

67.10 ACKNOWLEDGMENTs

The author extends his appreciation to the industry and the many who contributed to the progress of flexible circuit activities. Sincere thanks also goes to Dominique K. Numakura, at DKN Research, for his authorship of this chapter in the previous (6th) edition of *Printed Circuits Handbook*.

CHAPTER 68

TERMINATION OPTIONS FOR FLEXIBLE CIRCUITS

Joseph Fjelstad
Verdant Electronics, Seattle, Washington

68.1 INTRODUCTION

Flexible circuits are highly useful substrates used for interconnecting both electrical and electronic assemblies. To make those vitally important interconnections, termination features are required. These features are typically apertures in one or more of the insulating layers, which cover the metal circuit patterns exposing up to those areas where interconnection is required. The types of materials and processes which can be employed used to make these interconnections can vary widely. For example, some features may be disposed to be interconnected by wire bonding technology, others by a pressure contact of some sort, are still others by solder or some type of conductive or even nonconductive adhesive. Typically the termination areas are provided with a corrosion resistant conductive finish. A common finish for separable contacts is nickle/gold,

though other metal combinations are possible as described in other chapters of this handbook. That said, expensive noble metals are not required for every application and even a carbon ink may be suitable in some cases.

The choice of termination method will influence certain flex circuit design features, such as termination length and width and the type of surface finish that is applied. In many cases the flex circuit may be outfitted with a support material such as a stiffener either to bear the weight of the component or provide a stiffener backer to the flex to allow it to be inserted into an edge card connector, for example. While it is not possible to name and discuss every one of the myriad types of connections that might be used in detail, the major approaches to terminating flexible circuits in a manner that allows them to be interconnected to one or more modules, additional circuit assemblies or connectors it is possible to explore in broad brush strokes the major categories of termination types that are used. By employing a classification process familiar in science we will begin at the highest levels and work our way down to the finest level of interconnect bearing in mind that the approach to interconnection can vary widely even within a particular group this will be illustrated by example. The determination of what solution to employ at each level must be drawn out to the consideration of matters specific to the individual design and its operational environment along with reliability expectations of the customer.

68.1.1 First-Level Consideration—Permanent, Separable, or Intermittent?

The first decision that one must make relative to the type of termination needed is predicated on the nature of the

interconnection. This can be broken down into two fundamental options with a common but less recognized third option, the intermittent contact which is an option generally limited to contact switches. The interconnection may be desirably permanent or the interconnection may be desirably separable, that is allowing the interconnection to be made and broken some specified number of times over the life of a product. In the case of electrical and electronic components (i.e., through hole or surface mount components and connectors), a permanent connection is the default choice and with such devices solder is the typical interconnection medium of choice; however, there are other options as will be shown. For separable interconnections with flexible circuits there are a wide range of commercially available connector solutions to meet the growing demand for diverse solutions. Table 68.1 provides an overview of the basics of permanent and separable connections.

TABLE 68.1 General Capabilities of Separable and Permanent Connection

Mating Objective	Mating Method	Connection Density
Permanent connection	Array soldering	0.35-mm contact pitch
Permanent connection	Linear soldering	150-µm contact pitch
Permanent connection	Anisotropic conductive adhesive	30-µm contact pitch
Permanent connection	Wirebonding	100-µm contact pitch
Permanent connection	Direct bonding (e.g., TAB bonding)	70-µm contact pitch
Separable connection	bumped contact interconnect	20 contacts per square centimeter
Separable connection	SMT mated pair	0.5-mm contact pitch
Separable connection	ZIF connectors	0.25-mm contact pitch
Separable connection	Film connector	100-µm contact pitch
Intermittent	Elastomer buttons, dome switches	0.25- to 10-mm contact pitch

68.1.2 Permanent Interconnection Options

As mentioned above solder is the dominant technology for making permanent connections between electrical and electronic components and circuit boards whether flexible or rigid. Solder makes electromechanical interconnection between circuits and components by forming intermetallic bonds between component leads and circuit termination surfaces. Lap soldering of flex circuits to a circuit substrate has proven a useful method. Hot bar soldering tools have been developed to facilitate such connections. When connected (as illustrated in Fig. 68.1), the flex should be strain relieved in some to protect the interconnection. The subject of soldering is covered in great detail elsewhere in

this book so the reader is referred to that material. That aside the discussion will turn to other options for making permanent connections with flexible circuits.

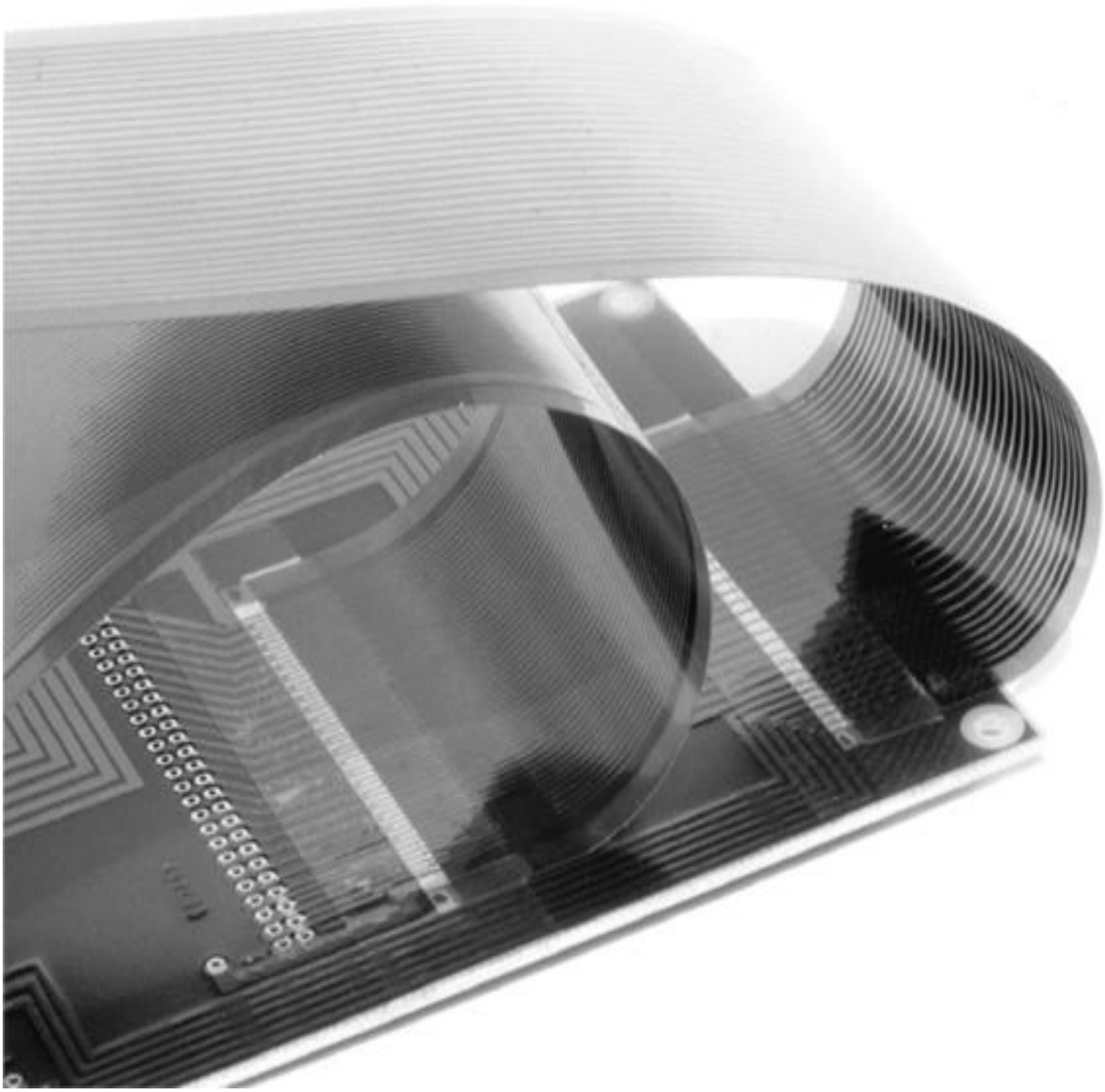


FIGURE 68.1 Flexible circuits connected to a rigid board by solder fusing.

68.2 WIREBONDING TECHNOLOGY

Wirebond technology is used primarily for making interconnection directly from an IC chip to a lead frame, a packaging substrate, or a rigid or flexible substrate. The latter has been historically referred to as chip on board or COB technology. There are three basic types of wirebond technology, thermocompression bonding, thermosonic bonding, and ultrasonic wedge bonding. Wedge bonding is arguably the most versatile because it is a room temperature process and employs relatively inexpensive aluminum wire for making interconnection. While most commonly used for making interconnection between chip and substrate, the technology can also be used for making jumpers in certain applications. Circuit terminations must necessarily have a nickel gold finish. Wedge bonding terminations require a very thin gold flash because Kirkendall voiding can occur with thicker gold deposits. On the other hand thermosonic gold wirebonding requires a thicker gold to make a reliable gold to gold connection (Fig. 68.2).

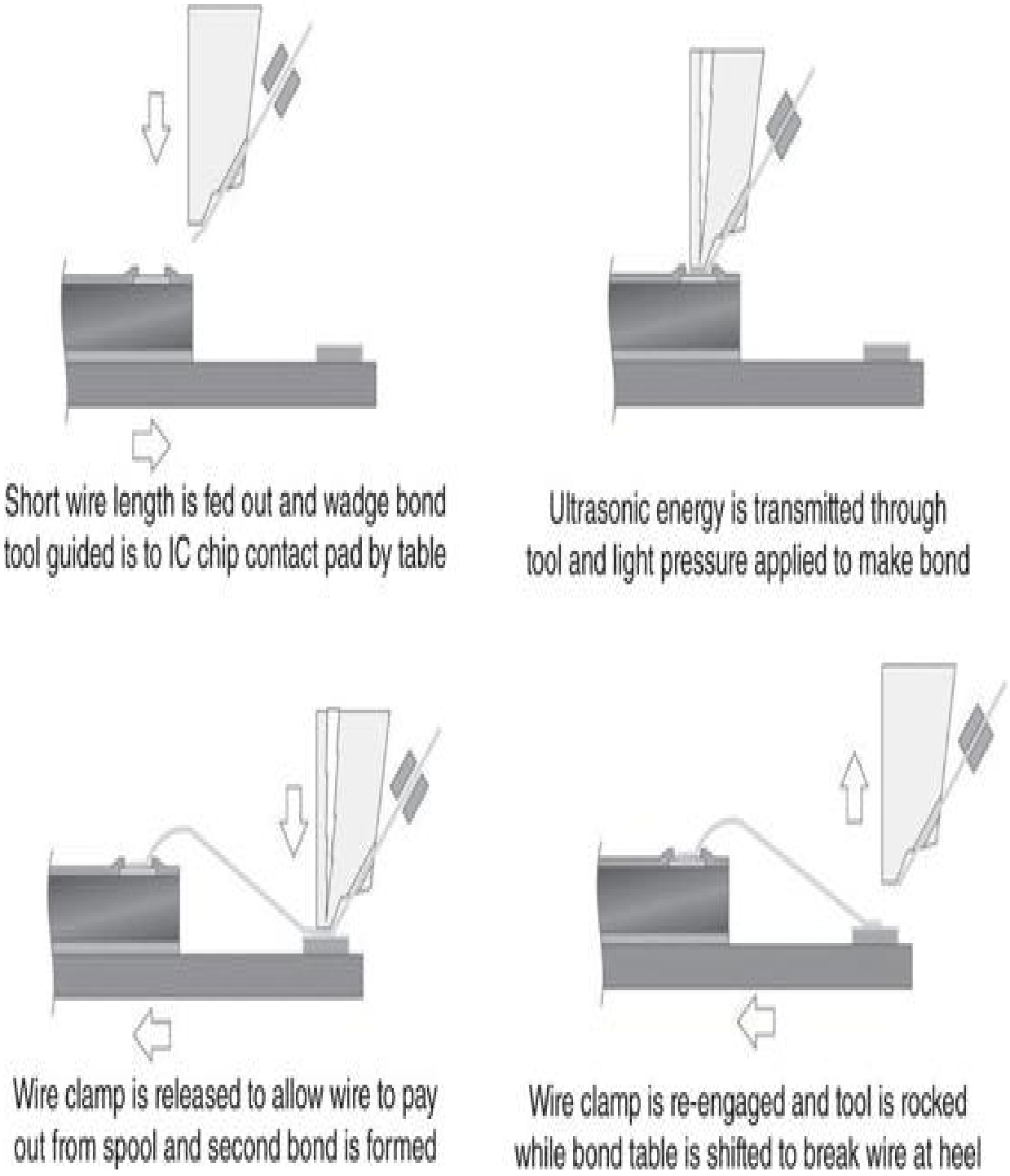


FIGURE 68.2 The basic wedge bonding process.

68.2.1 Conductive Adhesives

There are two general types of conductive adhesives used for electronic interconnections: isotropic conductive adhesives and anisotropic conductive adhesives. However, in some special applications nonconductive adhesives may be used such as where capacitive coupling is employed for the transference of signals, thus discussion here will be limited to the more common types of materials used. Descriptions of the two major types follow and Fig. 68.2 graphically illustrates the difference.

68.2.2 Isotropic Conductive Adhesives

Conductive adhesives are normally mixtures of powdered metal (typically powdered silver) and an adhesive such as epoxy. While the conductivity of conductive adhesives is not quite as good as solder they are quite suitable for many applications. They can deposited en masse onto a substrate in a manner similar to that used with solder paste such as by a stencil or as dots using a dispensing technology. During the cure of the resin adhesive there is typically some shrinkage which draw the conductive particles closer together to improve bulk conductivity.

68.2.3 Anisotropic Conductive Adhesives

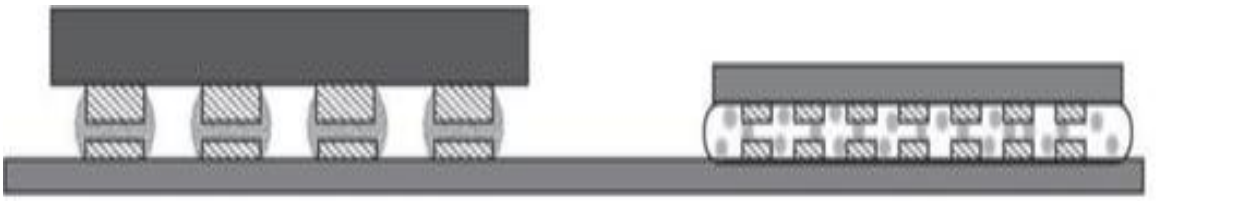
Anisotropic conductive adhesives differ from isotropic conductive adhesives in that they only conduct electricity in the *Z* or vertical axis this is because conductive particles are widely dispersed within the adhesive (Table 68.2). Anisotropic conductive adhesives can be provided in both liquid and film forms. An application and use multiple redundant contacts are made between mating surfaces. The

technology is capable of making very fine pitch interconnections and is widely used for interconnecting driver circuits to displays of every sort (Fig. 68.3).

TABLE 68.2 Capabilities of Certain Anisotropic Conductive Adhesives

Proprietary Formula	A	B	C
Applications	FOG, TCP	FOG, COF	FOB, TCP
Min. pitch	70 µm	50 µm	200 µm
Thickness	25 µm	20 µm	45 µm
Matrix	Epoxy	Epoxy	Epoxy
Particle size	5 µm	5 µm	6 µm
Surface treatment	Gold plating	Gold plating	Gold plating
Process temp.	170°C	190°C	170°C
Process time	15 s	10 s	20 s
Repair	Possible	Good	Possible

FOG: film on glass, FOB: film on board, TCP: tape career package, COF: chip on film.



Isotropic conductive adhesive
– Dense conductive particles
– Conducts in all directions

Anisotropic conductive adhesive
– Dispersed conductive particles
– Conducts in Z (vertical) axis only

FIGURE 68.3 A visual comparison of isotropic and anisotropic conductive adhesives is provided above. In applications isotropic conductive adhesives are

generally better suited to coarser pitch applications while anisotropic conductive adhesives well-suited to fine pitch applications.

68.2.4 Permanent Direct Metal to Metal Interconnection

Beyond the use of an intermediate material to make interconnection between different metallic contacts it is also possible to make direct metallic interconnection between contacts by other means. Three often seen approaches to making such connections include gas-tight interference fit connections, resistance-welded connections, and ultrasonically welded connections. A brief discussion of these follows.

68.2.4.1 Metal to Metal Interference Interconnection. Direct metal to metal interference interconnection is widely used in the backplane industry, where connectors are press fit into slightly undersized plated-through holes resulting in a gas-tight seal between the pins of the connector and the through holes into which they are inserted. The method is not commonly used in flexible circuits but an analog version is reasonably common. This version comes in the form of insulation piercing connectors, which as the name implies have pointed contacts designed to punch through the insulation of a flexible material having copper conductors. The punching process brings the contacts of the connector and the conductor traces of the flexible element in intimate contact to make direct electrical interconnection without an intermediate material. The contacts are often wrapped around the conductor and crimped into place to secure them in position. The same general technology is widely used in the electrical industry, where insulation-coated round wires are commonly used.

68.2.4.2 Resistance-Welded Interconnection.

Resistance welding is a technique used more often in circuit repair than in circuit production. A resistance welded is accomplished by pressing one metal tightly against the other to ensure a good electrical interconnection and then pulsing the joint with a short duration of high current energy causing the interface between the metal surfaces to instantaneously melt and weld together. Most of the equipment that has been developed is suited better to coarser pitch interconnections rather than the fine pitch more commonly found in use today

68.2.4.3 Ultrasonically Welded Interconnection.

The same general type of technology which is used for wirebonding can be used with flexible circuits by design when and where it suits the purpose of the design. Tape automated bonding (TAB) technology has employed this method for making interconnection directly to chips for decades. The delicate leads on the flexible circuit are desirably secured in place until the moment of bonding. One way to do this is to keep them attached on both sides of the aperture that exposes the leads. When the bonding process is ready the leads can be broken and attached and a single bonding step. To ensure that the leads break in the appropriate location a notch may be provided either by etching or embossing the lead at the point where the break is to occur. The technique was first used in volume for chip scale packaging in the mid-1990s. Figure 68.4 shows an example of such an interconnection.

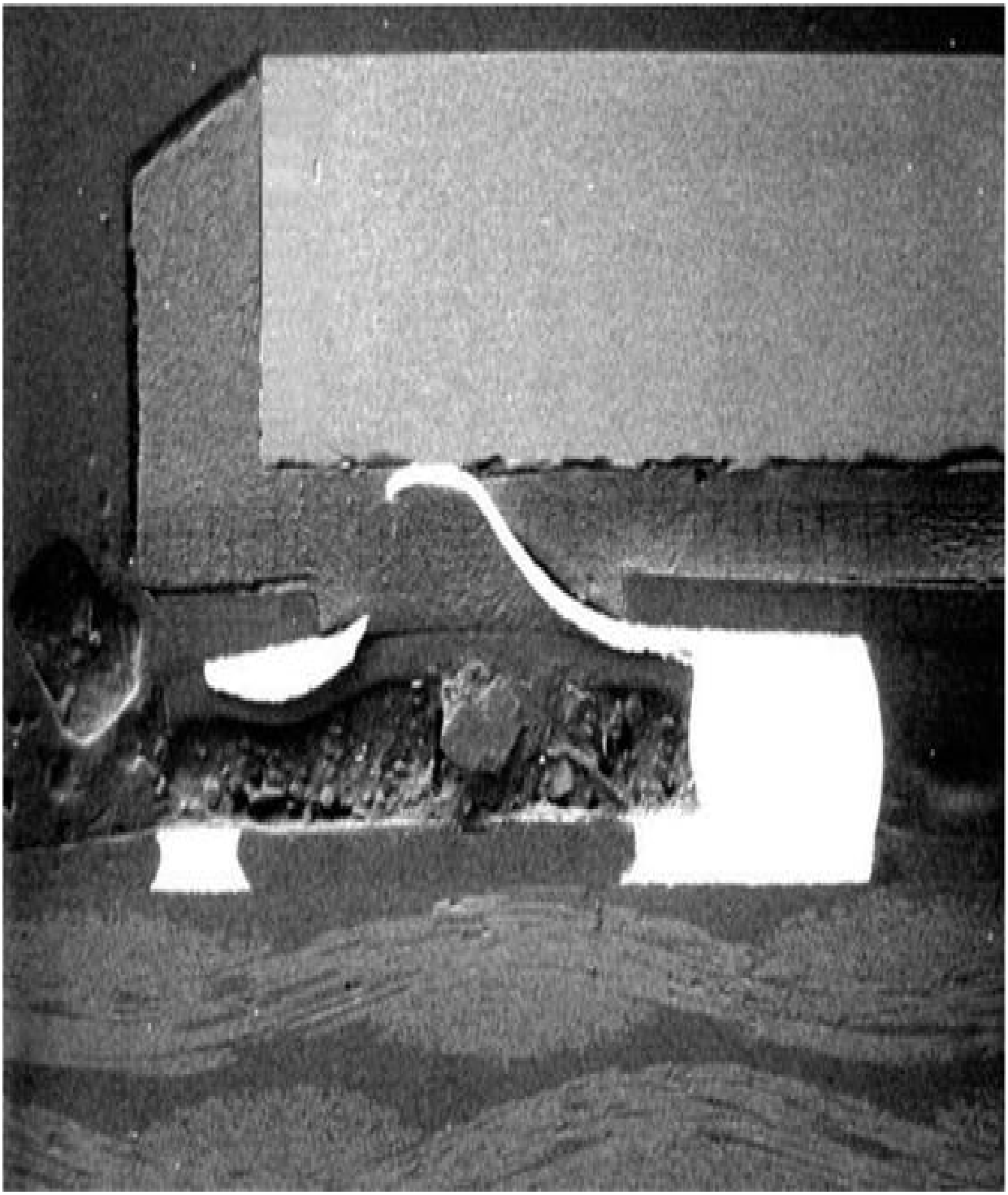


FIGURE 68.4 In cross-section is shown interconnection of the lead of a flexible circuit to an IC chip in a CSP.

68.2.5 Separable Interconnection Options

Separable interconnections are for the most part interconnections made from one specific set of conductors to another. This is typically accomplished through a connector. In the realm of flexible circuits separable interconnection surfaces can reside on the surface of the flex circuit itself or the flex circuit may be permanently joined to a connector of some sort, which is historically, and especially for the military and aerospace sectors which prefer mated pair connector systems and especially bulkhead type connectors wherein half of the connector is passed through the wall of the electronics box in which it resides. Because of the diversity of connector concepts available, the range of connectors which have been used to date is extremely wide. For the purposes of this discussion, the focus will be more limited to general approaches rather than specific solutions, though some specific solutions may be required to carry the message.

68.3 SOLUTIONS WHERE THE FLEX CIRCUIT IS HALF OF THE MATED PAIR

Rigid printed circuits have served as a half of a mated pair interconnection through an edge card contact system almost since the beginning of the electronics industry. One reason is that it reduces by half the number of the connectors required where system elements are joined. It should come without surprise then that the same objective would hold for flexible circuits as well. One of the challenges of making direct connection to a flex circuit, however, is that they are very thin, and the material somewhat more plastic and thus prone to deformation through material creep under pressure and

over time. This is not a major concern when there is sufficient resilience in the spring contact which makes to the flex to ensure continuous contact even as material creeps. Treatment of the flex circuit half of the contacts set ranges from simply providing a surface which is resistant to corrosion (e.g., nickel gold) to providing a topographical element on the contacts (e.g., providing bumps at the point of connection). Metallic bumps can be formed or plated. Formed bumps can be created by embossing the circuit from the backside often in concert with a mating die having cavities into which the copper can distend to form the bumps. This method was used with considerable success with the flex circuits used to interconnect inkjet printheads. Bumps are often provided in an area array configuration to help improve density in terms of contacts per unit area. When pressure forming bumps the lands need to be sufficiently large to allow the formation of the bump. If the lands or pitch are too small there is a potential for the fracture of the copper. That said variation potential is to remove the material from around the periphery of the contacts in the area where they are to be used and provide some sort of resilient material in a bump pattern beneath the areas where contact is to be made. Figure 68.5 shows examples of different contact structures possible on flexible circuits.

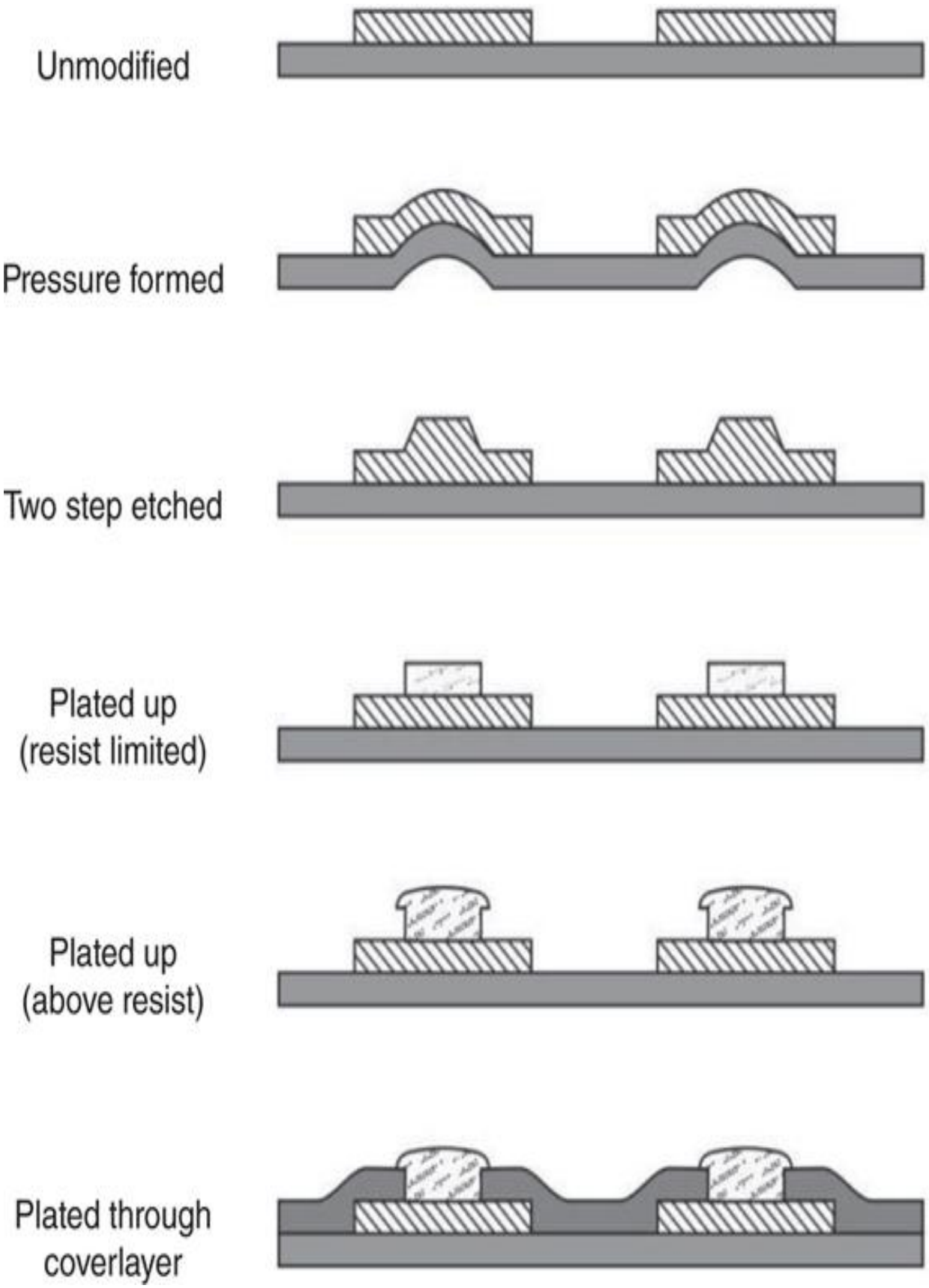

Unmodified
Pressure formed
Two step etched
Plated up
(resist limited)
Plated up
(above resist)
Plated through
coverlayer

FIGURE 68.5 The termination areas of flexible circuits can be modified in a number of ways provide raised contacts.

68.3.1 Connectors for Mating to Flex Circuits

There are a wide variety of commercial connectors available from different suppliers for making connection to flexible circuits. Where the flexible circuit is provided with a stiffener the number of legacy connector possibilities expands appreciably because edge card connectors have been used for rigid boards for decades. Rigid boards typically have beveled edges to facilitate insertion into the connector with flexible circuits on stiffeners it is useful to provide for a similar type interface if possible. For a single-sided connection the flexible circuit can be wrapped around the rigid stiffener and bonded in place to achieve the effect if two flexible circuits are to be connected on the opposite sides of a single stiffener then those two should be bonded to each other to form a small nib at the end of the step and area. The two approaches are illustrated in Fig. 68.6.

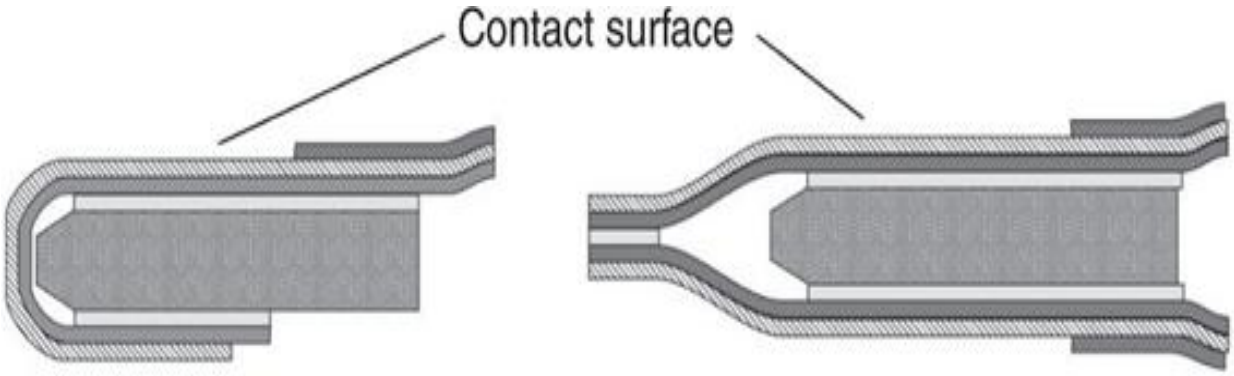


FIGURE 68.6 To allow for easier mating and insertion into standard edge card connectors, the flex circuit is bonded to a stiffener to meet with mating connector requirements for thickness. Beveling is used on standard rigid cards and flex circuits need a similar treatment as illustrated. Flex circuits may be bonded to one or both sides.

68.3.2 ZIF (Zero Insertion Force) Connectors for Flex

In many cases it is desirable to use the thin flexible circuit's edge connections to mate with other electronic elements. Zero insertion force connectors are well-designed to meet such needs because it is otherwise normally too difficult to try and insert with force flexible circuit into mating connectors. ZIF connectors typically have a latch which is listed to allow for easy insertion of the flexible circuit, once the circuit is in place the latches closed locking down the contacts and providing connection from connector to flex. Figure 68.7 shows an example of a ZIF connector.

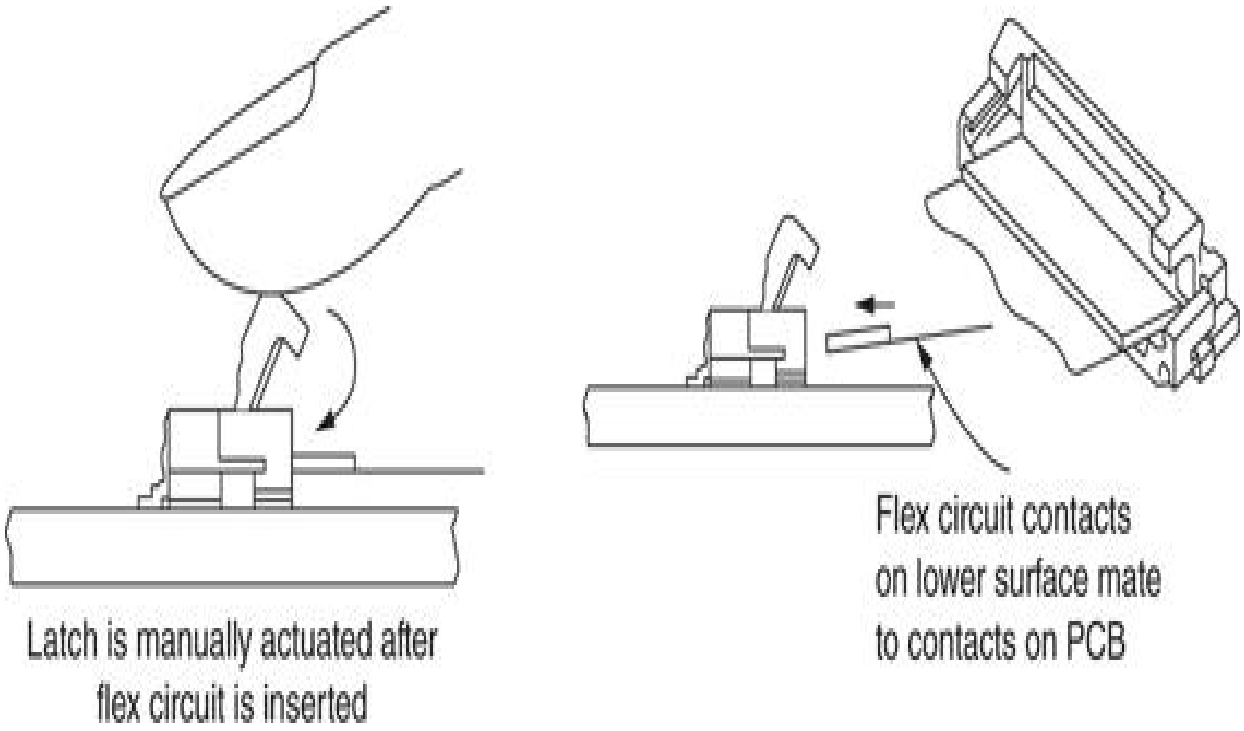
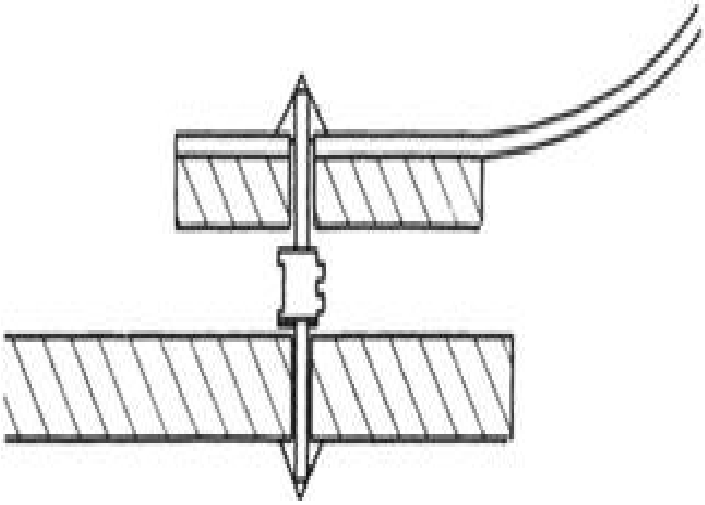
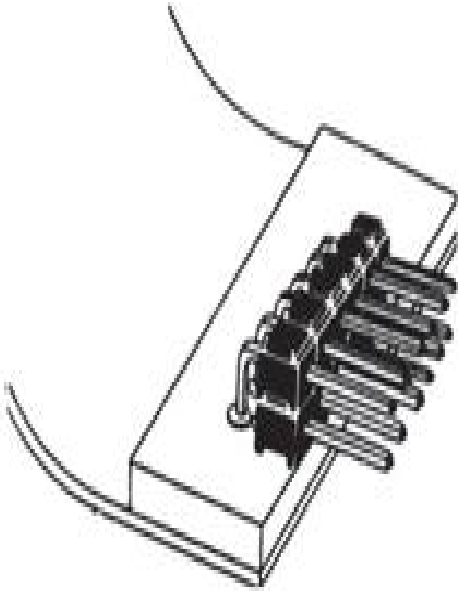


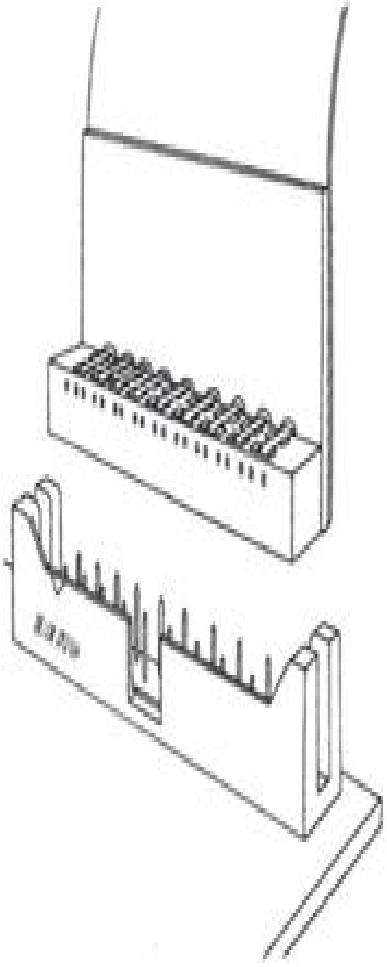
FIGURE 68.7 ZIF connectors are well suited to flexible circuit applications.

68.3.3 Header (Pin in Socket) Through-Hole Connectors for Flex

A popular format in printed circuit design is a so-called pin and socket approach. One half of the mating pair involves a header with pins projected through a plastic body, which holds them in accurate alignment and the other half is a socket that accepts the pins in the mating process. There are a number of different approaches to the design of such structures, a few of which are illustrated in Fig. 68.8.







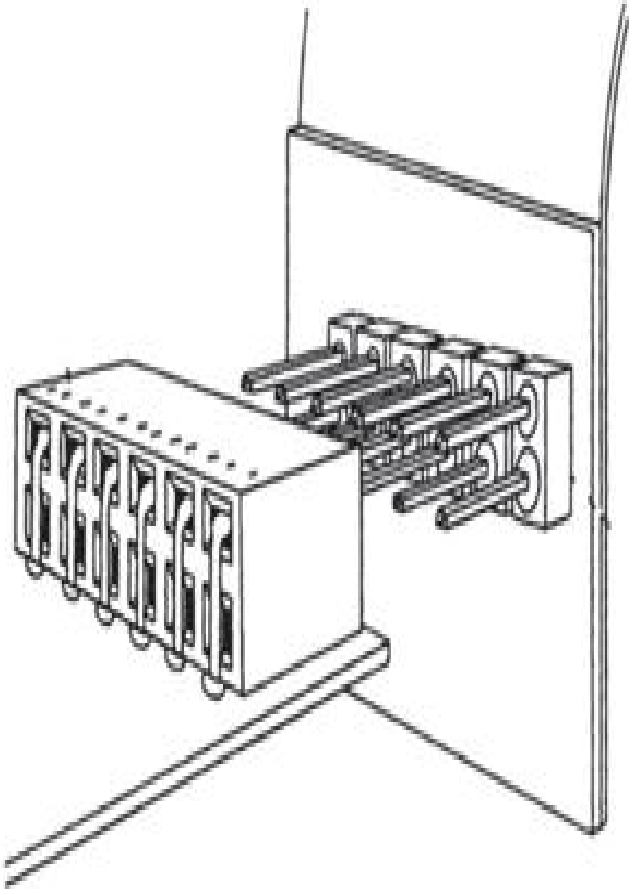


FIGURE 68.8 Examples mated pair through-hole connector concepts involving pin and socket interconnection between flex circuit and rigid board.

68.3.4 Mated Pair Surface Mount Connectors for Flex Circuits

Mated pair surface mount connector technology has been readily adapted to use with flexible circuit technology with great success. And it has served well the design objective of interconnecting many tens of circuits at low profile in a wide range of products including cell phones, digital cameras, and the like. Contact pitch can range down to 0.5 mm and less (down to 0.2 mm in some present advanced generation designs) which offers significant space savings in *x, y*, and *z* dimensions. Figure 68.9 provides an example.

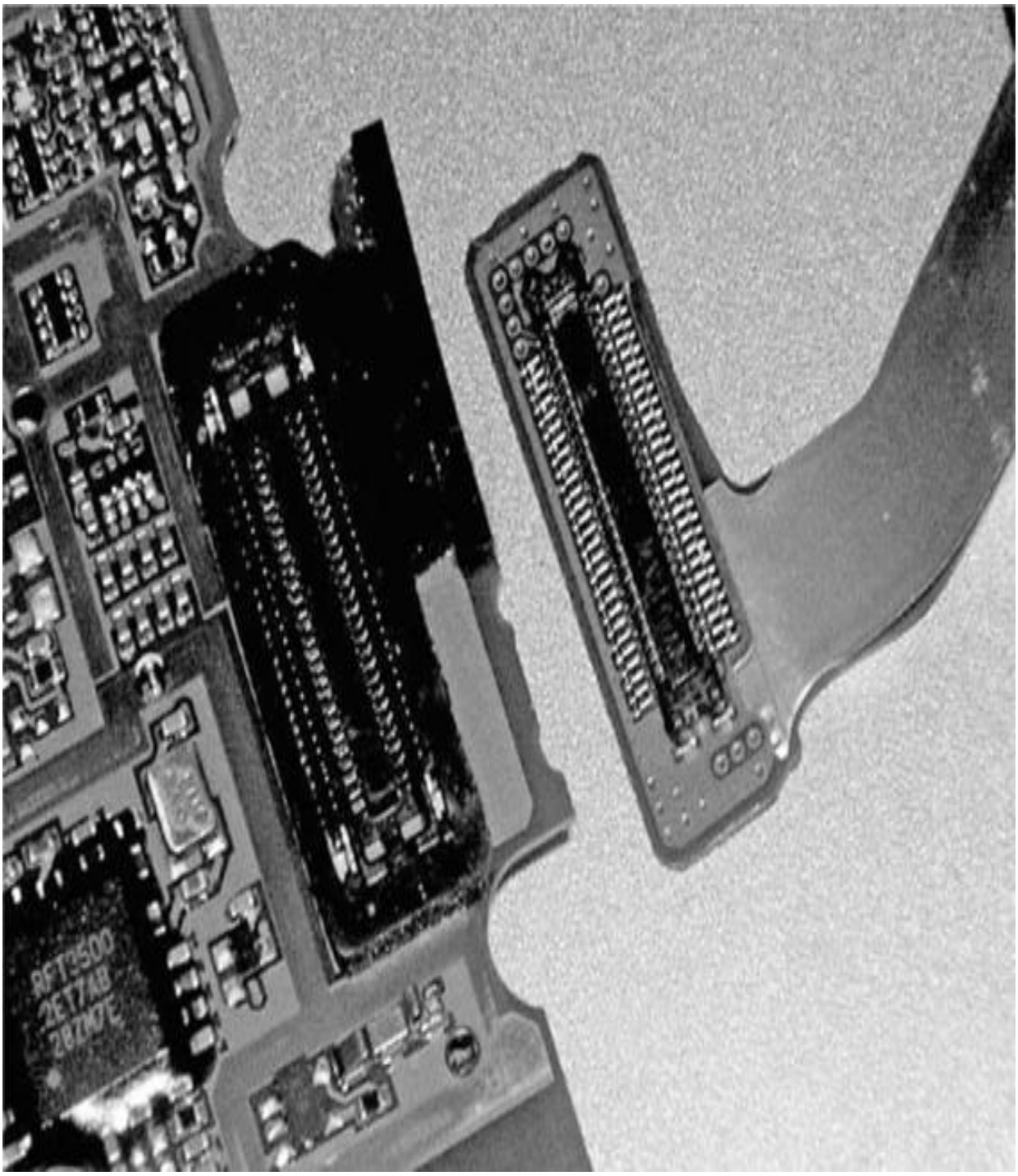


FIGURE 68.9 SMT mated pair connectors for flexible circuits. Example shown is for connection in cellular phone.

68.3.5 Zebra Strip Elastomeric Connectors for Flex

Zebra strip is a term applied to a unique elastomeric method of making connection between flex and rigid boards. The material is comprised of multiple layers of conductive and insulating elastomeric materials and allows for redundant connection between the mated pairs. The latest generations of the material have a 200-µm linear pitch resolution. The disadvantage of the material is that the contact resistance is relatively high making it not suitable for all applications, especially high current applications. Figure 68.10 shows an example of a zebra strip connector in an application.

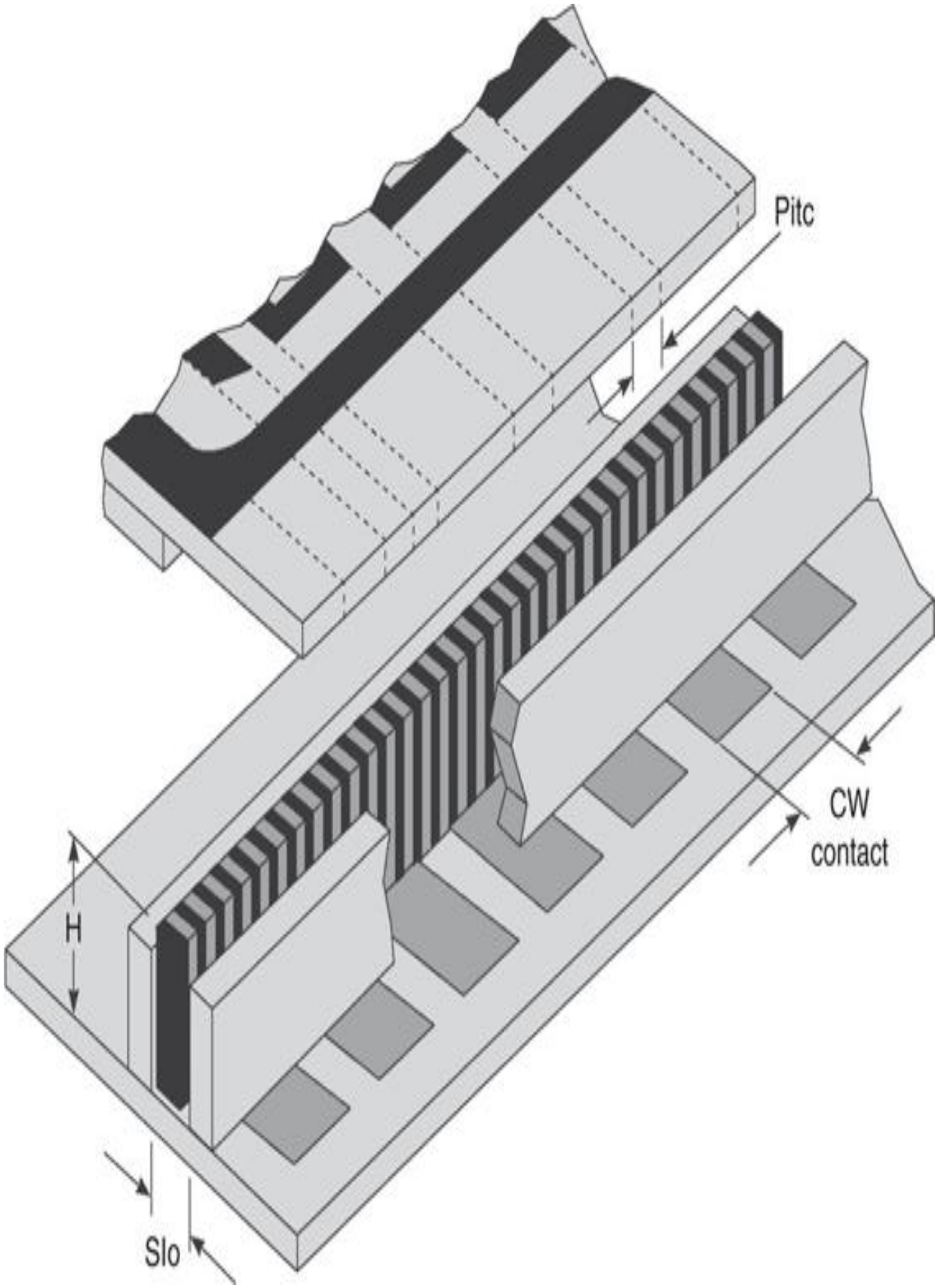

Pitc
CW
contact
H
Slo

FIGURE 68.10 Pressure contact with anisotropic conductive rubber.

68.3.6 Military Style and Bulkhead Connectors for Flex

Military style and bulkhead connectors are used for so-called black box electronics the connectors are designed to port electronic signals to the outside of a box through a weatherproof seal. The devices are typically round body and use pin in socket type interconnection with the mating cable being tightened and sealed by a screw ring cap that joins the mating halves of the connector (Fig. 68.11).

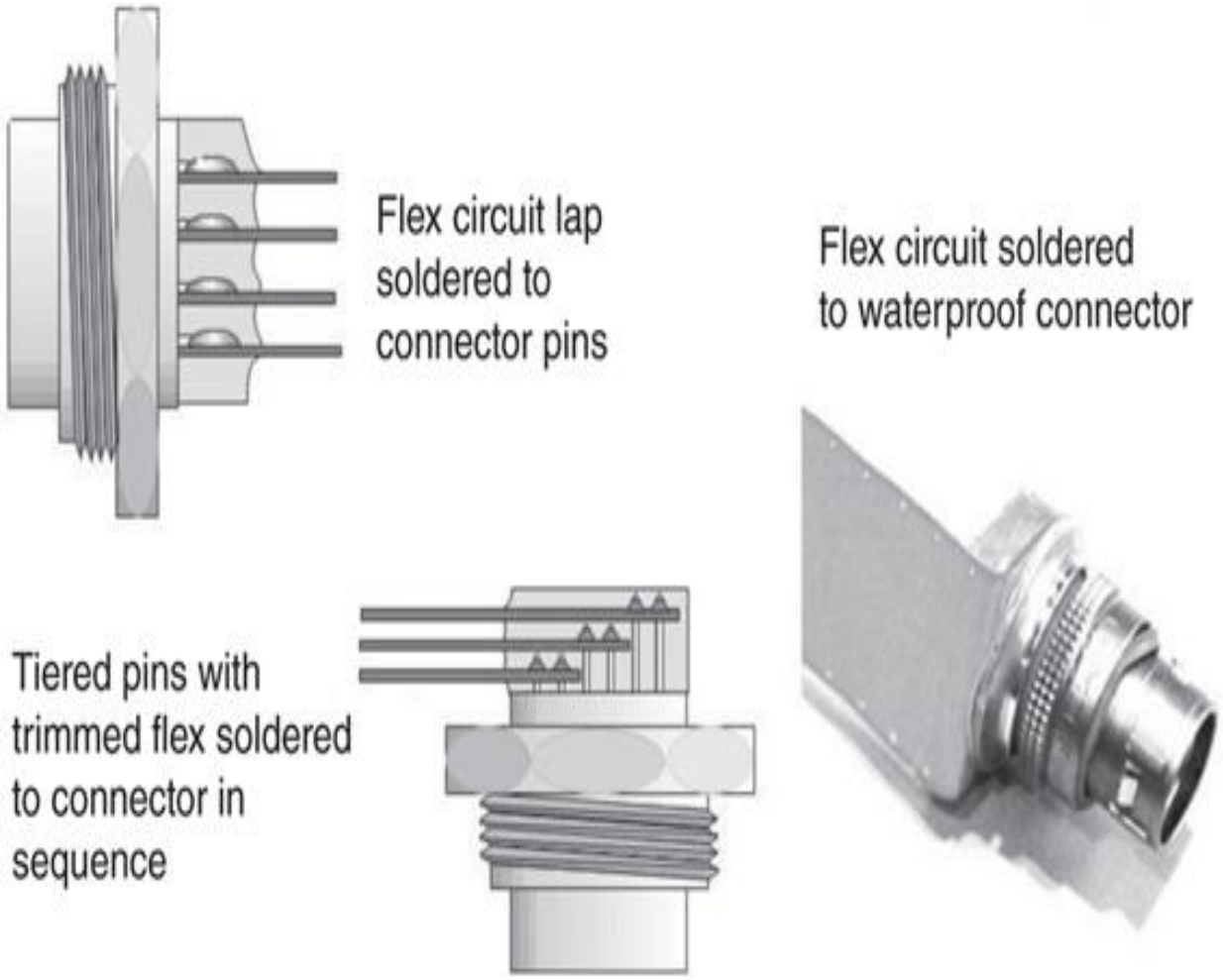


FIGURE 68.11 Examples of flexible circuits integrated into bulkhead and military type connectors.

68.3.7 Intermittent Connectors for Flex

The last type of connection in this overview of termination options for flexible circuits is the intermittent contact. With flexible circuits this means a low profile contact. It is often associated with membrane switch technology which is used in keyboards of every imaginable sort. Here the objective is to make contact and release. There are a number of different ways to execute this objective. Often because they circuits run at relatively high voltages and low current they can be produced using polymer thick film technology (i.e., silver ink). Figure 68.12 shows an example of structural elements of such a circuit and Fig. 68.13 show a perspective view of how contact is made.

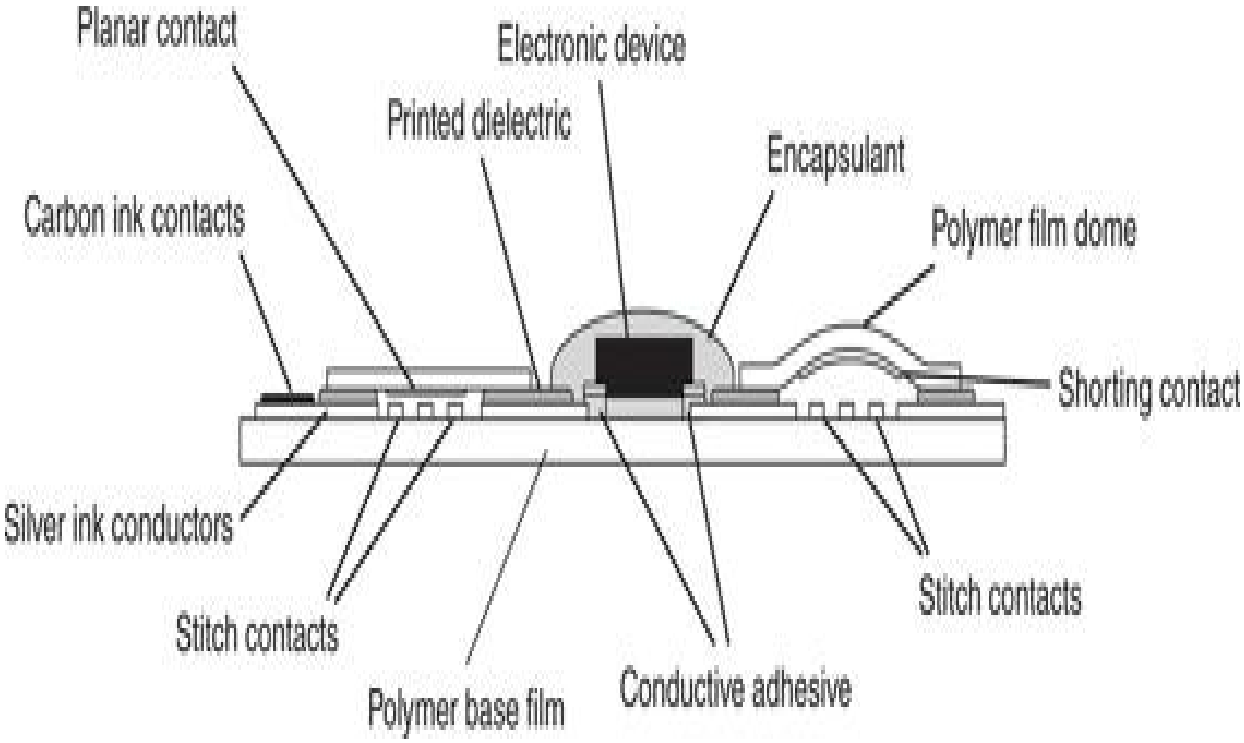


FIGURE 68.12 Representative elements of a membrane switch polymer thick film circuit are illustrated in the above graphic.

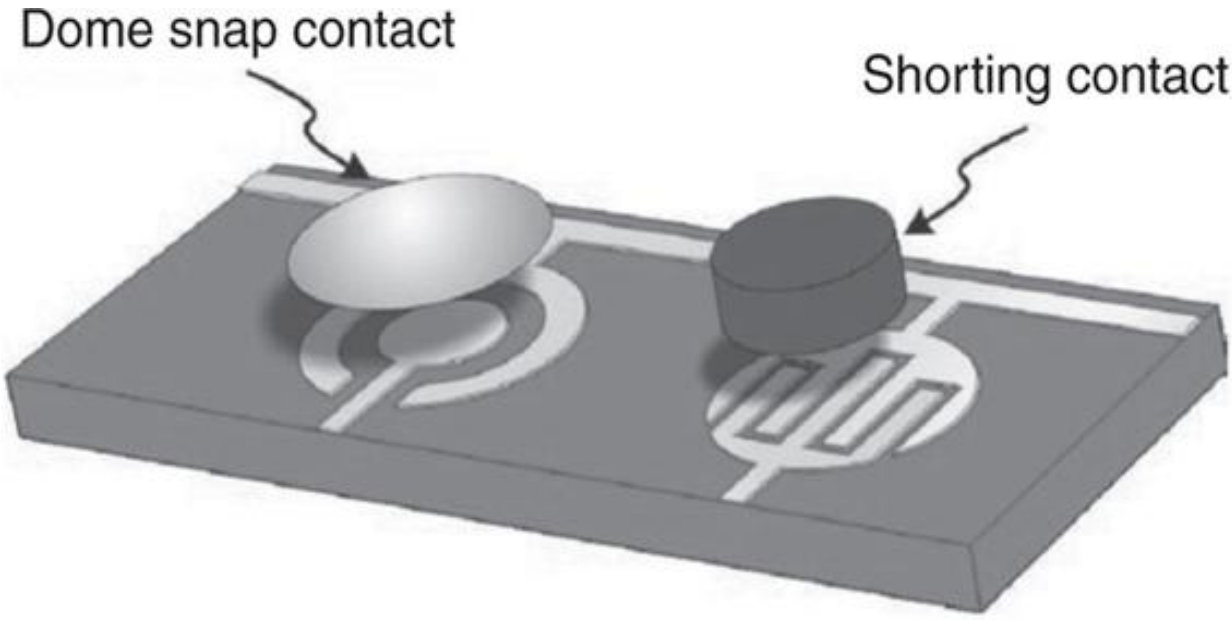


FIGURE 68.13 Shown above are different approaches to making intermittent contact to a flexible circuit the upper interconnecting and insulating elements are absent from the graphic.

68.4 SUMMARY

The methods for terminating flexible circuits permanently, separately, and even intermittently are varied. The correct solution among options available and the examples shown is the one that best suits the objectives of the design. This brief discussion is not meant to be exhaustive but to serve as a guide for the designer so they can have a better grasp of what options are available to them before they set out to create a new design. It is recommended that the designer reach out to connector suppliers for their input on which solutions might be best suited to the application in hand.

68.5 ACKNOWLEDGMENTS

The author extends his appreciation to the industry and the many who contributed to the progress of flexible circuit activities. Sincere thanks also goes to Dominique K. Numakura, at DKN Research, for his authorship of this chapter in the previous (6th) edition of *Printed Circuits Handbook*.

CHAPTER 69

MULTILAYER FLEX AND RIGID FLEX

Joseph Fjelstad
Verdant Electronics, Seattle, Washington

69.1 INTRODUCTION

Multilayer flexible circuits and multilayer rigid flex (a.k.a. flex rigid) circuits represent the technological peak of flexible circuit technology. Presently multilayer flexible and rigid flex circuits have become increasingly important in many high-end consumer products especially applications requiring high-density multilayer flex, where space product is at a premium, while, rigid flex circuits have tended to be employed in lower volumes and serving unique applications often found in military and aerospace product designs.

These interconnection types also tend to be much more engineering intensive requiring a great deal of care both in the aerospace design and the manufacturing process. Interestingly the original idea of stacking together thin layers of flexible material supporting conductors goes back more than 100 years to a patent credited to a German inventor

Albert Hansen. However, the first patent for what we would today call a rigid flex circuit was issued in the mid-1960s to Sanders Associates a pioneer in the technology (see Fig. 69.1). First applications for the technology wherein the aerospace industry where they were used to replace complex wire harnesses in an effort to both improve reliability and reduce weight, while minimizing total volume, all key objectives in virtually every aerospace application. Still rigid flex circuits have been employed in some volume applications in the past, perhaps the most memorable being found in a laptop computer. More recently they have been used in some cell phone designs and high density display driver applications so opportunities for future use and application appear to be on the rise.

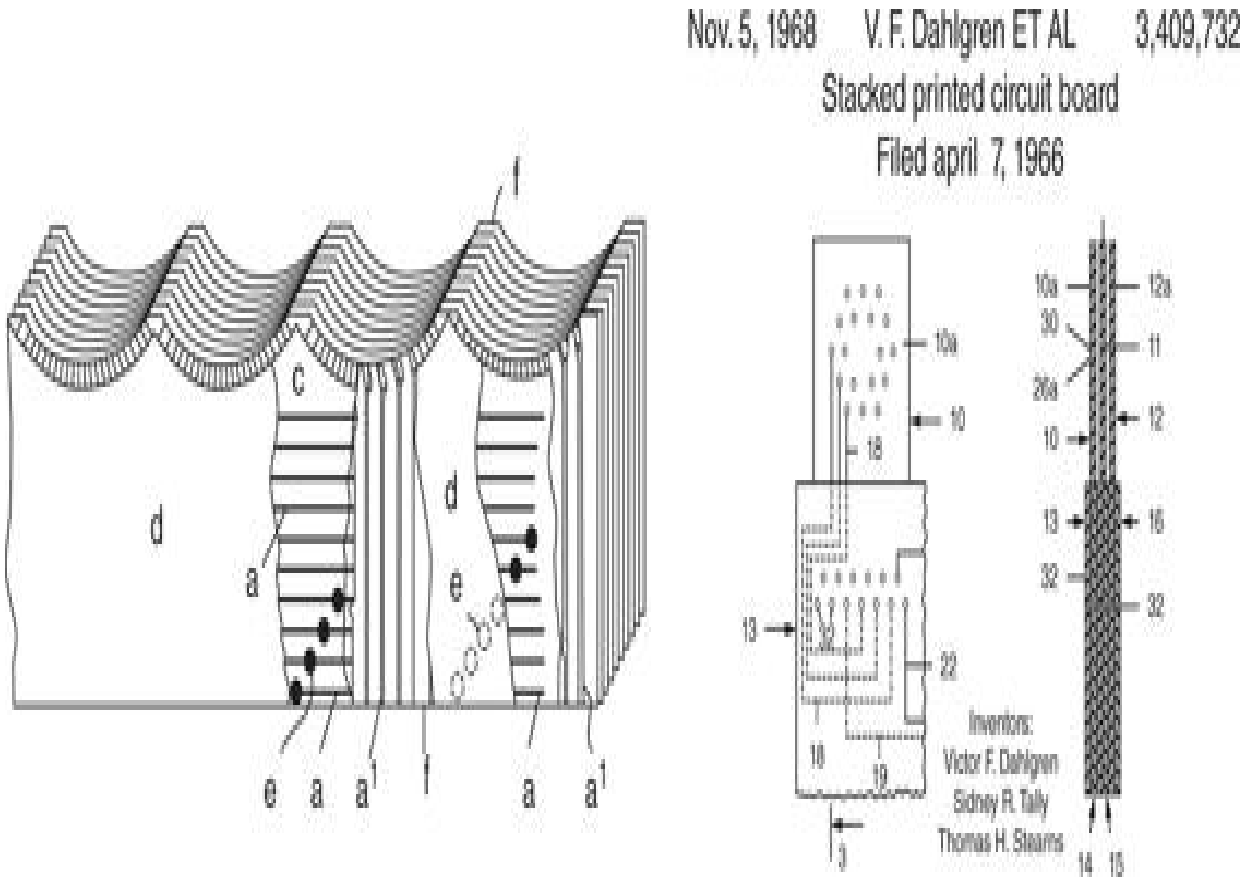


FIGURE 69.1 Drawings from two patents issued more than 60 years apart. On the left a drawing clearly showing multiple layers of interconnecting elements

issued to Albert Hansen and on the right a patent for a rigid flex circuit issued to Victor Dahlgren, Sidney Tally and Thomas Stearns.

Because rigid flex circuits subsume and entail most of the same concerns as are extent for multilayer flexible circuits, this chapter will focus on rigid flex constructions and will examine some of the varied structures and approaches to manufacturing rigid flex circuits, past, present, and prospective.

69.2 MULTILAYER FLEX VERSUS RIGID FLEX

A multilayer flex circuit is as the name implies a circuit structure comprised of multiple layers of flexible materials bonded together and interconnected by plated-through holes. In this overarching definition they are fundamentally the same as multilayer rigid printed circuits. However, they are distinct and the materials and processes associated with their manufacture do have points of departure from more traditional multilayer circuits. Like their rigid flex counterparts multilayer flex can have multiple areas where flexible circuit tentacles ingress from the main body of the circuit. Multilayer flexible circuits may also have stiffeners attached to them to support the weight of components or connectors within the main body or at the distal lands of flexible tentacles. This can make multilayer flexible circuits appear similar to a rigid flex circuit; however, they are different.

Multilayer rigid flex is at the core a combination of rigid multilayer and flexible circuit processes. The finished structures have islands of rigid printed circuit material interconnected by flexible circuits and having plated-through holes, which pass through both the outer rigid printed circuits and the flexible circuits which passed between the

rigid layers which contain them providing electrical interconnection. However, the successful accomplishment of this combination requires a high level of skill in both areas, and it is important to have a clear understanding of the abilities and limitations of the chosen fabricator before designing this type of circuit for a product.

69.2.1 Fundamental Rigid Flex Constructions

There are many different concepts in the construction design of multilayer rigid flexible circuits. Figure 69.2 shows examples of just a few of the arguably endless construction. Layer counts can vary from as few as two to as many as 30 layers or more. For the uninitiated or neophyte who encounters a flexible circuit with a stiffener attached they may be deluded into thinking they are looking at a rigid flex circuit. That said it is important to keep that option in mind when setting out on the design the manufacture of a single double-sided are multilayer flex to which a stiffeners attached post manufacturing is typically going to be a much more cost-effective solution. That said, early rigid flex circuits were originally used mostly with through-hole connectors, which were soldered into the rigid sections and employed in aerospace applications. Today the technology is used with most of the types of components and assembly methods used with rigid PCBs except perhaps for direct chip attach solutions such as wire bonding and flip chip and rigid flex technology serves a much broader array of markets.

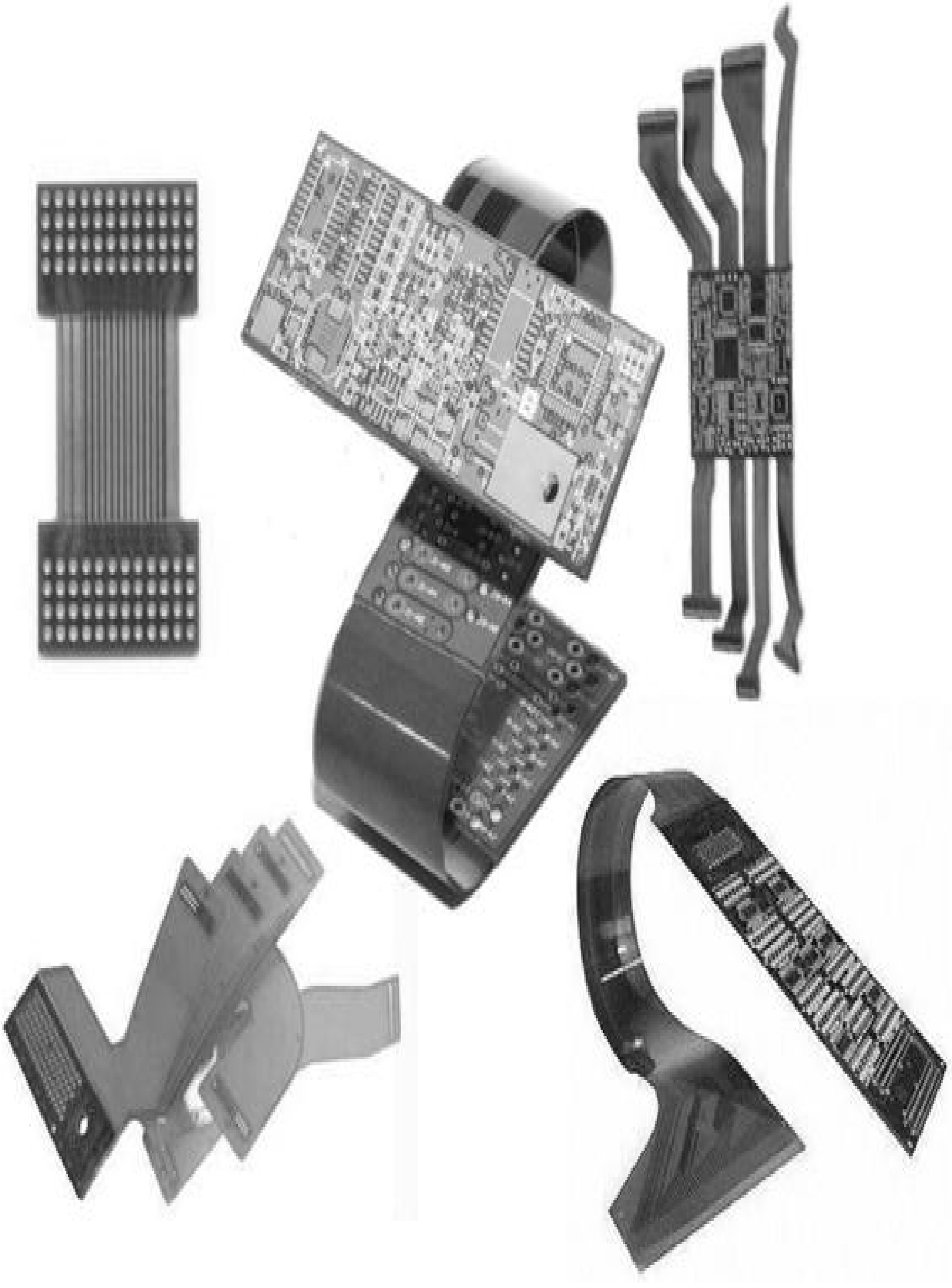


FIGURE 69.2 Rigid flex circuit technology enables a wide range of structures and solutions from simple jumpers (upper left) to highly complex (upper right). The structure in the lower left corner is perhaps the most complex because it has terminations both in rigid and in flexible area of its structure. Each inner circuit layer must be preprocessed before they are laminated to integrate them into the whole where they are interconnected by plated- through holes in the small rigid section on the left.

Over the years there have been a number of innovations incorporated into the rigid flex circuit design and manufacture process to improve both manufacturing and assembly yield as well as field life.

Figure 69.3 shows in cross-section examples of common early approaches to the structure of rigid flex circuits along with an improved design which is much more robust. The improvement came when it was observed that plated-through-hole reliability was suffering and thermal excursions due to the high expansion rate of the body of the circuit, which was caused by the use of unreinforced materials such as flexible circuit bond ply cause sufficient stress fracture plated-through holes either in the barrel or at the corners. In the improved approach flexible bond ply material was replaced with glass reinforced prepregs material such as is commonly used in the manufacture of rigid printed circuits.

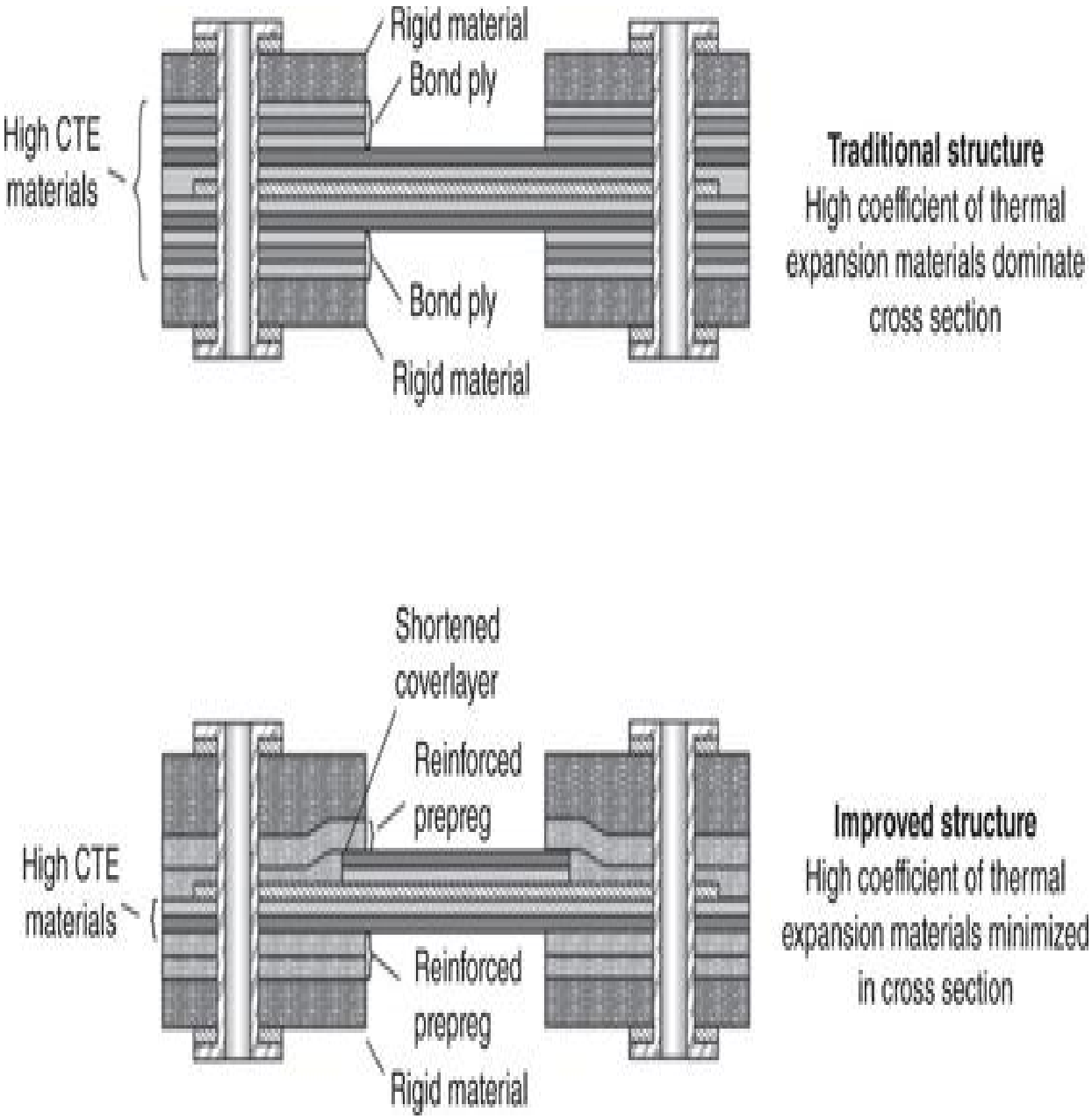


FIGURE 69.3 High coefficient of thermal expansion materials dominated cross-sections in early approaches to rigid flex design and manufacture improves structures refined design, processing and materials to minimize the amount of high CTE material.

Because a material's stiffness increases as a cube of its thickness, the incorporation of air gaps between flexible layers and flexing or bending zones is commonly designed and engineered into the rigid flex manufacturing process. Figure 69.4 illustrates one prospective approach to

manufacturing which achieves the objective of an air gap between layers.

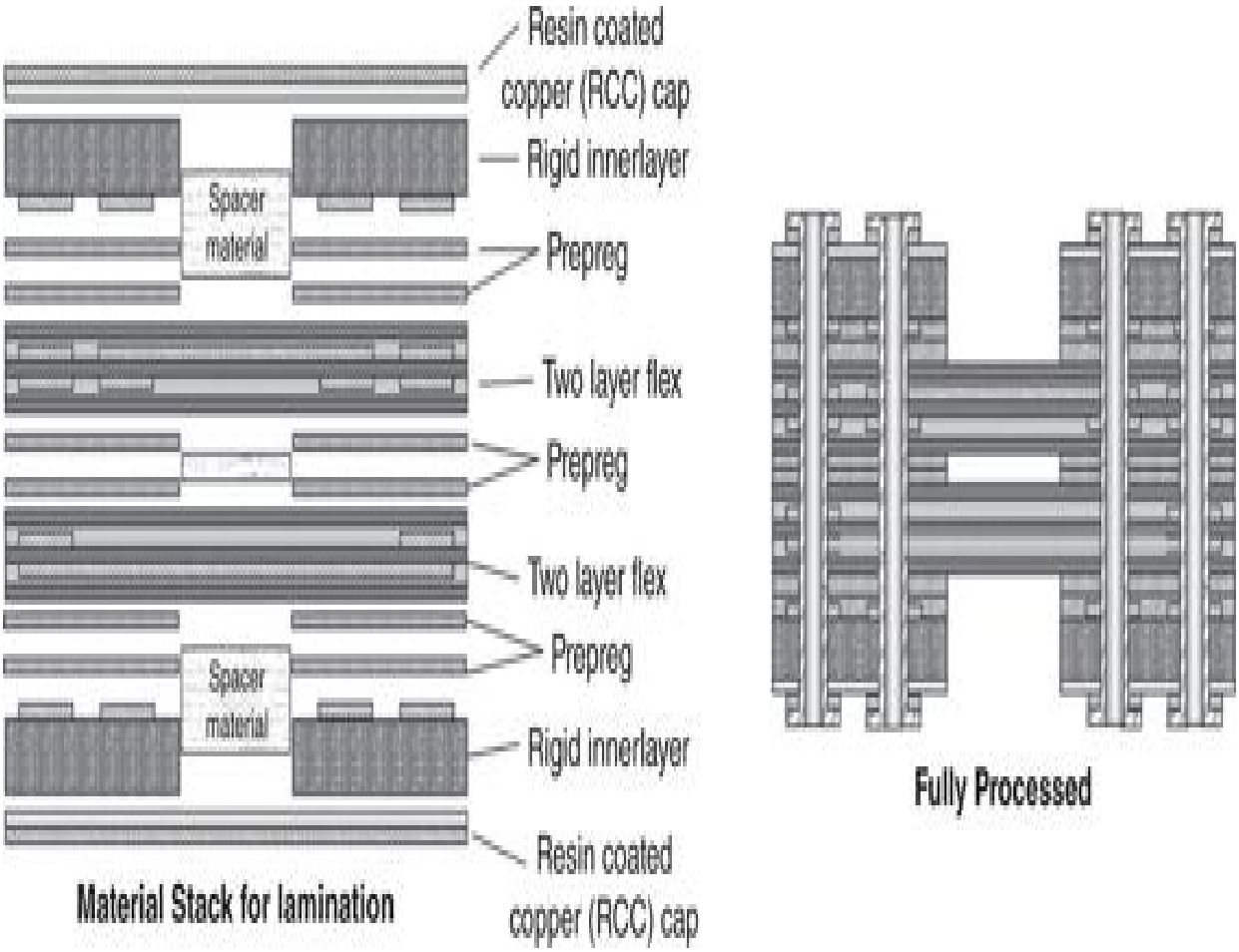


FIGURE 69.4 Shown in cross-section above is a prospective material stack for the manufacture of an eight-layer rigid flex circuit with two double-sided flex circuits incorporated into the center of the circuit.

In another example illustrated in Fig. 69.5, there is shown a multilayer flex circuit comprised of a multilayer distal head for a connector which terminates at two other distal ends through two other multilayer flex circuits each comprised of one single- and one double-sided flex circuit bonded drilled and plated through before the final lamination and plating through. It is a complex and highly engineering intensive structure both from design and manufacture’s perspectives.

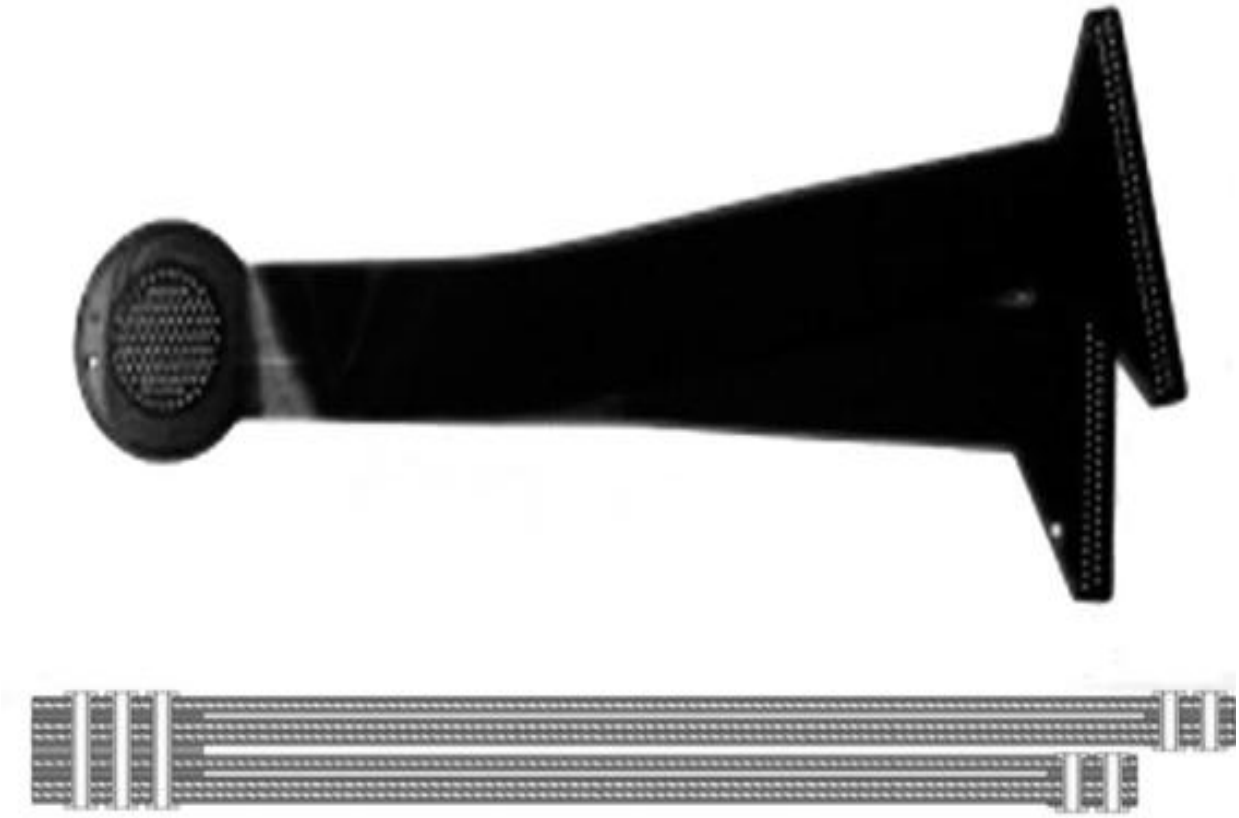


FIGURE 69.5 Multilayer flex circuit can be visually simple, but structurally quite complex as the construction below the circuit image illustrates.

These applications are still common and the designs and constructions are normally fairly straight, except that they often require the use of a technique described earlier called *bookbinder construction*, where each successive layer is lengthened in bend areas in anticipation of and to mitigate the strain-related damage to the outer conductor layers or buckling of circuits that will occur if the technique is not used. The term comes from recognition that such measures are required to keep pages flush on a closed book. Figure 69.6 illustrates the concept in exaggerated cross-section and Fig. 69.7 shows an example of such an implementation.

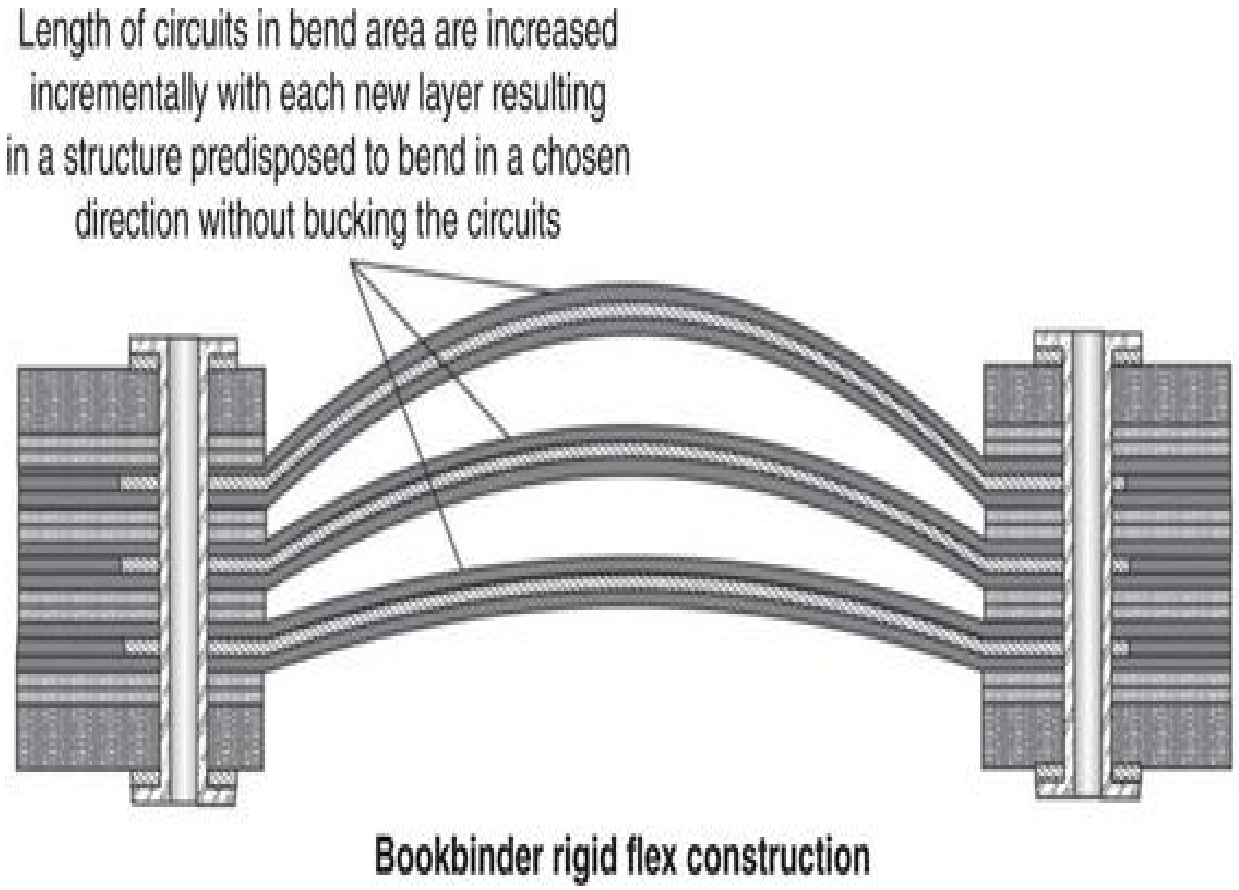


FIGURE 69.6 The bookbinder structure (exaggerated in graphic) is achieved by building circuits having slightly different lengths through the bend area (nominally 250 θm added to circuit length in bend area per layer) so that circuits do not bind or buckle when bent. Tooling is required around the area to hold the circuits in bowed shape during lamination and an aperture in the lamination plates is often required to prevent the area from being flattened.

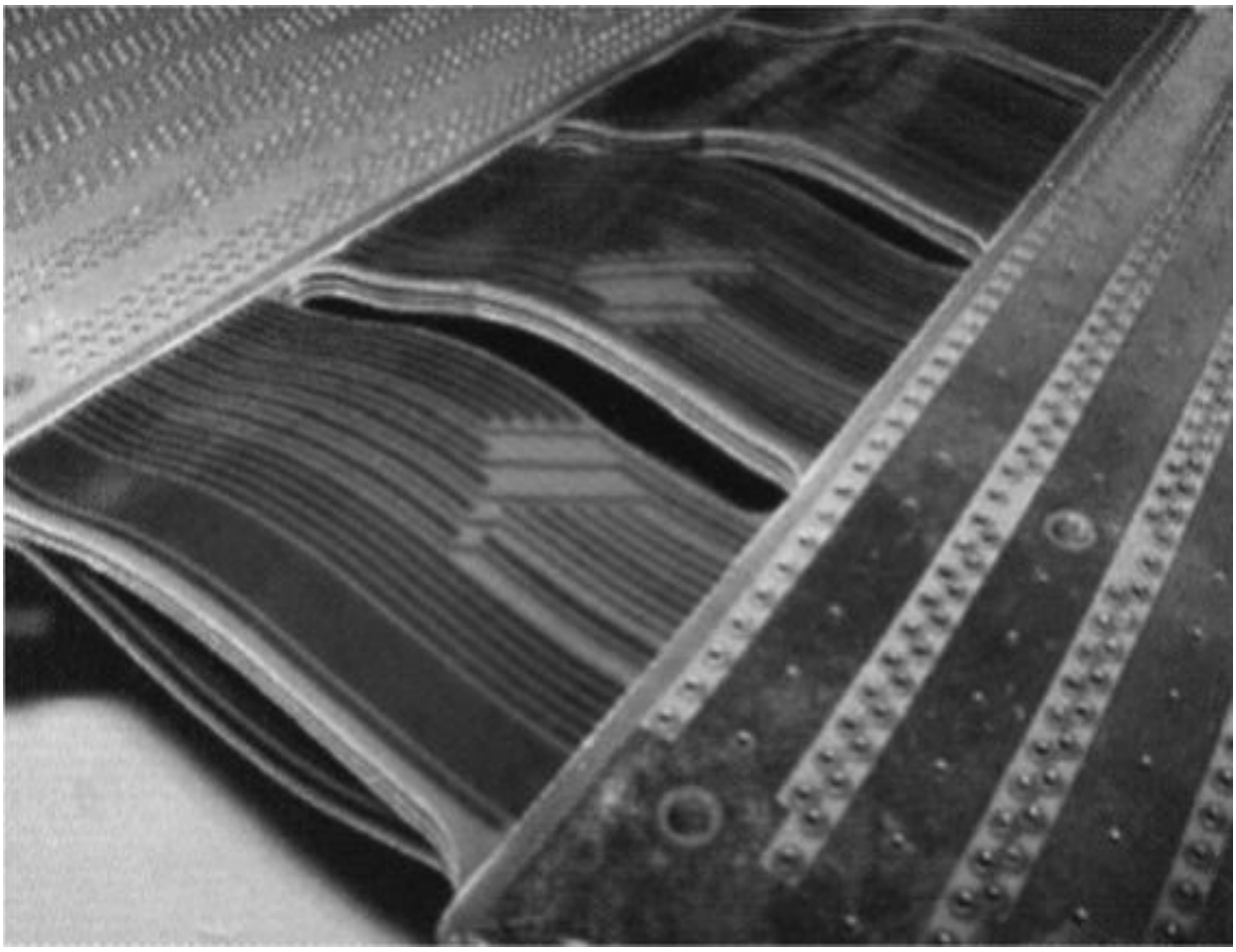


FIGURE 69.7 The bookbinder shown in an application.

69.2.2 Materials for Rigid Flex Manufacturing

As one might expect the material set required for the manufacture of rigid flex circuits is a composite of the materials used for the manufacture of both rigid printed circuits and flexible circuits. Thus flexible base materials, coverlayers, bond plies, and rigid laminates as well as glass reinforced prepregs are part of the material set. In addition, there are specialty materials used in processing including materials for providing conforming pressure to the laminate. In this regard while traditional. Heated hydraulic press

lamination is not uncommon, in the manufacture of rigid flex it is much more common to use vacuum assist lamination or lamination in an autoclave system.

Owing to their applications and the need to solder connectors and other components to them rigid flex materials must be able to withstand high temperatures. This is especially true as we endure the many problems associated with lead-free soldering.

All materials employed in any design should ideally be highly dimensionally stable to minimize movement of features in the lamination process which can make drilling and plating through-holes more challenging if the material is substandard in terms of its dimensional stability. Since rigid flex circuits are only rarely used in dynamic flex applications some leeway can be found in material selection. To improve reliability the use of adhesiveless base materials is a good option. This is because adhesives have a much higher coefficient of thermal expansion than do the base polymers of flexible films. There are a range of adhesives available for bonding coverlayers to flexible circuits again because the rigid flex circuits are rarely dynamically flexed there is some latitude in the choice of material properties for the adhesive. Acrylic adhesives have been a mainstay for coverlayers; however, flexibilized epoxies are suitable in many applications. The use of epoxy glass prepregs and polyamide prepregs help to control *z*-axis expansion in the rigid areas of the circuit assembly.

In general for inner layers on rigid flex 50 µm is suggested as a minimum thickness for the polyamide. The materials must have high heat resistance and high dimensional stability to survive during several high-temperature processes. Thicker polyimide films (greater than 50 µm) are generally recommended because the thicker dielectric materials provided better dimensional stability in the manufacturing processes. Acrylic adhesive systems are frequently used for flexible copper-clad laminates, as well as

and coverlay film and bonding sheets. However polyimide adhesives which have a higher heat resistance than either acrylic or epoxy systems, are also good choices and well suited to the manufacture of a highly reliable product.

Adhesiveless, copper-clad laminates are also well suited for use in the flexible elements of a rigid flex board. Adhesive is laminates made by casting polymer to foil or lamination of foil director polymer normally usually perform better in high-temperature conditions both in process and in use. Adhesive is laminates also provide value owing to the fact that they can reduce the total thickness of the finished board. Finally hot, melt-type, polyimide adhesive systems, including coverlay films and bonding sheets, have been developed to have very high reliability and smaller thicknesses. They can reduce smear level in drilled holes significantly. But they must be processed at temperatures higher than 300°C, and therefore require special facilities and conditioning. Table 69.1 provides a list of material options which may be employed in the manufacture of rigid flex circuits.

TABLE 69.1 Materials for Multilayer Rigid Flexible Circuits

Materials Used	Standard	High Performance
Flexible substrates	Traditional polyimide films (Kapton H, Apical AV)	Improved polyimide films (Kapton E, Apical HP, Upilex S)
Copper-clad laminates (double-sided)	Rolled copper bonded with acrylic or epoxy adhesive	Rolled copper with cast or laminate polyimide film
Coverlayer	Traditional polyimide films coated with acrylic or epoxy adhesives	Newer polyimide films coated with hot-melt polyimide adhesives (one side)
Bonding sheets	Polyimide coated with acrylic glue (two sides) Epoxy glass resin perpreg	Newer polyimide films coated with hot-melt polyimide resin (two sides) Polyimide glass prepregs
Rigid substrates	Copper clad glass/epoxy laminate	Copper clad glass–BT resin boards and glass-polyimide boards
Solder mask	Liquid or dry film, photoimageable	Liquid or dry film, photoimageable
Conductor finish	OSP, NiAu, solder	OSP, NiAu, solder

69.2.3 Manufacturing Process Flow for Rigid Flex

Because of the great diversity of designs and potential layouts and structures of rigid flex circuits, they are much less amenable to a fixed approach when it comes to describing a manufacturing flow. That said Fig. 69.8 is provided to give a general idea of a prospective flow for the manufacture of a rigid flex circuit. It is recommended that anyone looking to embark on a rigid flex design engage the

services of an experienced rigid flex manufacturing engineer who can guide them around potential pitfalls (Fig. 69.8).

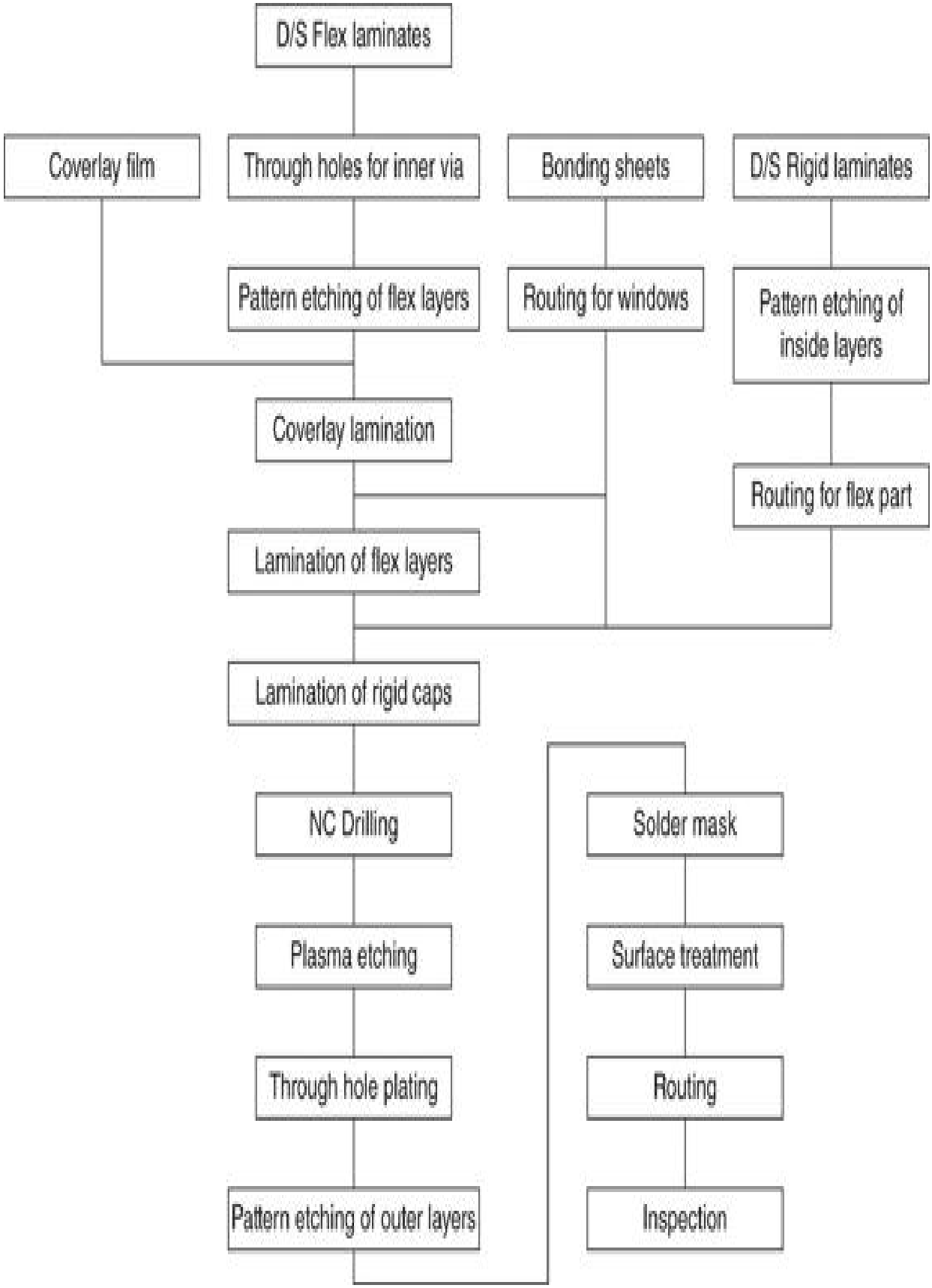

D/S Flex laminates
Coverlay film
Through holes for inner via
Bonding sheets
D/S Rigid laminates
Pattern etching of flex layers
Routing for windows
Pattern etching of inside layers
Coverlay lamination
Routing for flex part
Lamination of flex layers
Lamination of rigid caps
NC Drilling
Solder mask
Plasma etching
Surface treatment
Through hole plating
Routing
Pattern etching of outer layers
Inspection

FIGURE 69.8 Material construction for multilayer rigid flexible circuits.

The process illustrated presumes the use of flexible, double-sided copper-clad laminates; however, single-sided flex may be employed as well of course. The flexible laminates are imaged and etched and any plated vias between first and second metal layers must necessarily be incorporated before the coverlay films are bonded. No openings in the coverlay are generally required as interconnections to terminations in the flexible circuit areas will be accomplished after subsequent laminations with rigid materials. In some cases the flexible layers may be machined by numerically controlled routing; however, it is common practice to machine the bond material which will be used to join rigid and flex elements of the circuit. Machining process prevents the flexible circuits from being bonded to the rigid caps. There are several choices for bond material and the choice can have impact on subsequent processing. While acrylic coated polyamide bond plies are commonly used epoxy glass or polyamide glass bond plies are options. And all polyamide construction should be considered when possible as it minimizes the potential for drills smear.

A spacer material of the dimensions and thickness of the cavity formed are produced and placed in the openings before lamination to help maintain surface planarity. The spacers are removed when the rigid flex circuit is routed from the background. The rigid cap layers commonly have circuitry imaged and etched on the surface that will be joined to the flex in the lamination process.

All of the materials except for the spacers share a common tooling system to ensure that all the features align properly during lamination. The vacuum autoclave lamination system is best suited to the manufacture of rigid flex boards because it ensures highly uniform bonding across the entire surface of the material stacked. Because of the employment of the vacuum any air entrapped in the body of the laminate will

create internal pressure which could lead to delamination, therefore venting holes may be required. These venting holes will require sealing in some manner before wet processing. One common practice of tradition is to place a small dot of epoxy over the vent hole.

Following lamination the panel can generally be processed in the same manner as traditional rigid multilayer circuits; however, drilling and processing conditions can vary. A drill study is recommended when the material set is unusual or the layer count unusually high, this is performed to maximize hole quality while minimizing drill smear. Also because of the materials that and the frequent use of acrylic adhesive which is prone to smearing on hole walls and over internal conductor surfaces, the use of plasma etching is recommended. Keep in mind that because the plasma process takes place in a near vacuum that vent holes may again be needed to prevent delamination. Bear in mind that these vent holes will need to be sealed in some manner before any wet processing can proceed. While plasma is commonly recommended for rigid flex construction, wet processing is also employed to remove drill smear. The common chemistry is a heated solution of potassium permanganate. Care must be used in such processing as excessive dwells can cause swelling of some of the resins and hole wall. This can have deleterious effects on further processing and the ultimate reliability of the plated-through hole.

Because of the diverse material set found in a rigid flex through hole, the choice of processing chemistry is very important. The hole wall may consist of polyamide, epoxy glass and acrylic adhesive for example. The first step in through-hole processing is arguably the most important because it involves the wetting of the surfaces of the hole wall making the surfaces receptive to the catalyst, carbon or graphite material which will provide a conductive path through the hole for electrolytic copper.

Following electroless copper or sensitization of the through holes, the process is largely indistinguishable from that used for standard multilayer board. The major difference comes in the routing process at which time special handling and processing may be required especially at the areas where rigid and flex circuit elements join. Depending on how one has preengineered the transition a great deal of caution may be required. There is often a good deal of touch labor involved at this point. Since there is no one way this problem has been addressed over time it is highly advisable that the transition be discussed in advance with the manufacturing engineer who will be responsible for ensuring any rigid materials including spacers are removed from the flexible areas and the final product.

69.3 ALUMINUM RIGID FLEX CIRCUIT —PROSPECTIVE STRUCTURE FOR THE FUTURE

Aluminum is a ubiquitous metal and the third most abundant element on the planet representing 8.3 percent of the earth’s crust. Given its ubiquity and unique properties is deemed a potentially suitable candidate for the manufacture of rigid flex circuits. However, it is not a drop-in replacement as the use of aluminum requires both the designer and the manufacture to reconsider what they have learned over the years relative to the manufacturing of rigid flex circuits, or for that matter any type of circuit. What follows is a description of a prospective process for manufacturing a rigid flex circuit which is manufactured in accordance with the precepts consistent with what has come to be called the Occam process, where electrically tested and burned- in components are embedded in insulating materials which proximately matched to the coefficient of thermal expansion

of the components used in the assembly. In broader terms, the concepts that will be described in this rest of this chapter fall under the umbrella term of SAFE an acronym which stands for either “solderless assembly for electronics” or “solder alloy free electronics.” Regardless of term, the design and manufacturing processes associated with SAFE manufacturing are relatively simple compared to traditional circuits and the cost should prove significantly lower. These topics will be discussed more fully after a brief description of the process.

69.3.1 Aluminum Rigid Flex Process Steps

First, a sheet of aluminum (other metals are also possible if desired) is prepared with cavities that can be either machined (chemically, mechanically, or laser), embossed into the metal sheet or cast. One or both sides of the metal can be provided with components. The cavities that receive the components are ideally formed such that the depths will match the components’ height so that when components are placed into their assigned cavities with leads facing up, the lead terminations will be flush with the surface. While the use of bare die is possible, the IC components to be used are ideally packaged (CSPs are very well suited). Packaged devices are preferred because packaged IC devices are much more easily tested and burned-in and because they have standardized lead patterns and physical outlines making the design process simpler, especially if a single lead pitch is used for all components (e.g., 0.5 mm). Additionally, nearly all packaged components use copper as the base metal for interconnections which is advantageous for more than just that one reason alone, as will be shown.

While untreated aluminum can be used effectively for many applications, there are some advantages in other

applications to either treating or coating the surfaces. Anodizing of aluminum is a very common industrial process, which results in the surface of the aluminum being converted to alumina (Al_2O_3), an insulator. Another alternative is to coat the aluminum with an organic coating such as an epoxy, which can be done by powder coating or painting by electrophoretic or electrostatic methods resulting in a very uniform coating over the entire substrate. When either anodizing or coating is used, it is important remember that all such processes will reduce all the dimensions of the cavity, with X and Y dimensions potentially being more profoundly impacted, so characterization of any process chosen will likely prove important. Finally, the aluminum could also and alternatively be plated with a metal such as copper for electrical reasons that will again be discussed in more detail later.

After the components are placed and affixed permanently on one or both sides, layers of flexible insulation are applied to one or both surfaces of the metal sheet covering the components. A flexible clad laminate may also be used if desired. At this point, the assembly can be processed almost as if it were a standard rigid printed circuit with high density build-up layers on one or both sides, using lasers to drill holes down to access component terminations and commonly practiced plating and imaging processes to create the circuits. A key difference is that a fill step with an insulating material may be required if through-holes have expose metal. However, if coated with epoxy, this may not be necessary. One caveat for those circuit manufacturers considering exploring processing circuits of this type is that if the aluminum is untreated, the edges need to be sealed to prevent contamination of subsequent processing chemistries that will be used in manufacture.

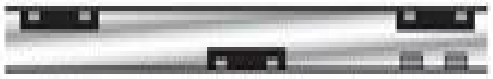
Once all of the circuit layers are complete, a final flexible film (i.e., cover film or coverlayer on one or both sides) is applied, leaving open any features required for

interconnection at the next level. The coverlayer and/or flexible base film will ultimately need to be absent from the areas that are going to require flexing, as well as those that will define the outline of the completed circuit. This can be accomplished by mechanical, chemical or laser methods either alone or in combination with one another. Once the metal is exposed, it can be etched using a suitable chemistry either completely or to some predetermined depth if the designer desires to leave a conductive path between rigid component bearing areas.

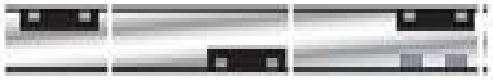
When all of the required interconnections and circuits are added, the assembly can be partially machined to thin the metal carrier enough to allow the residual metal to easily bend and, if the metal is thick enough, hold its shape after bending. Again, the residual metal can serve as a common ground layer for the assembly. If ground isolation is required between rigid areas or desired for purposes of creating a more flexible connecting bridge between rigid areas, the residual metal can be etched using chemistry appropriate for the metal used as component carrier. For the subject aluminum rigid flex constructions, alkaline chemistries such as solutions of sodium hydroxide and sodium gluconate are suitable for aluminum. However, other chemistries such as ferric chloride are also suitable. In fact, ferric chloride is nearly universal in terms of its range of applicability as a metal etchant. The process steps just described are illustrated in Fig. 69.9. Note that the process as illustrated shows complete removal of the metal between rigid areas which is an option where greatest flexibility is desired.

Machine metal base (e.g. Al) with cavities for electronic devices

Place and bond electronic devices into machine cavities



Coat assembly with flexible polymer, liquid or film

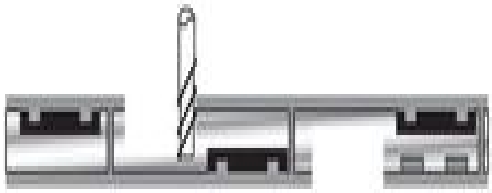


Drill holes where connections to second side is required

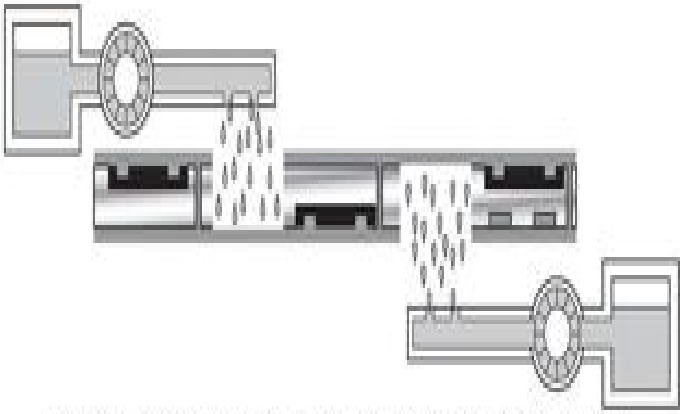
Fill holes with insulation polymer such as filled epoxy

Second drill holes filled with insulating fill polymer

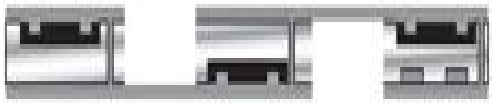
Use build up and thru hole processing for circuits & apply top flex layer



Control depth machine carrier metal part way through in flex areas



Etch remaining metal using chemistry appropriate for metal (optional)



Complete processing (e.g. route circuits for panel (not shown))

Form metal rigid flex circuit to desired shape

FIGURE 69.9 A novel approach to design and manufacture of a rigid flex circuit having metal areas with components placed in routed (as shown) etched, embossed or cast cavities with terminations facing away from the surfaces and a flexible polymer or polymer film bonded to them with interconnections between devices made by using commonly practiced build-up processing methods. Routing and/or etching processes can be used to complete the separation of the metal areas leaving them interconnected by flexible circuits. Other embodiments will be the subject of future articles (patents pending).

Finally, while not a topic of discussion here, the assemblies described can be stacked and interconnected creating 3D assemblies that offer substantial potential to solve a wide range of electronic interconnection problems.

69.3.2 Advantages of Aluminum Rigid Flex Assemblies

There are a striking number of advantages to the design and manufacture of electronic assemblies that do not use solder to make interconnections. The advantages of products manufactured using SAFE techniques also circumscribe the full range of benefits normally considered desirable for any electrical or electronic product, including: economic, electrical, thermal and mechanical performance, security, reliability, regulatory compliance, and environmental friendliness. Following are brief discussions of each of these areas of benefit:

69.3.2.1 Economic Benefits. In a highly cost competitive global economy, the cost of manufacturing is always a high order concern. Looking fist at material, note that the primary material is aluminum. Aluminum is a simple an abundant material sold by weight regardless of thickness and it is less expensive per unit volume than composite materials. Though aluminum is admittedly denser than FR-4 laminate, (2.8 g/cm^3 aluminum versus 1.8 g/cm^3 for FR-4) the amount of aluminum required can be less for reasons,

which will be discussed later making it the finished assemblies very cost competitive from a materials use and cost standpoint. Moreover, with the price of polymers tied to the volatility of the price of oil, there are advantages to being able to use a material such as aluminum the price of which is reasonably predictable because of its global abundance (Fig. 69.9).

Next, as is inferred in the process shown in Fig. 69.9, the number of manufacturing steps is reduced significantly, which obviously reduces manufacturing cost. What should be highly evident is that the entire soldering process with its many steps and requirements is omitted. No stenciling of solder, no reflow, no post-assembly cleaning, etc. There is also no need to be concerned with moisture sensitivity of components. Thus the energy and time wasting baking steps that are commonly called for in conventional processing are obviated. Depending on the complexity of the design, as it has been estimated independently by a number of manufacturing experts, the final cost of such assemblies could be 25 to 35 percent lower than traditional methods (exclusive of the cost of the actual components). Obviously the final number will depend heavily on the specifics of the design and actual savings may be less; however, any savings in today's highly competitive global markets is both welcome and highly prized especially if the final product is not subject to intense environmental scrutiny in search of metals and materials which are proscribed by EU regulations.

Another economic benefit is that the components used do not require special finishes to maintain solderability, nor do they need special treatment to keep out moisture because they will not experience the high temperatures required for lead-free solders. The lack of a need for a finish can and should reduce the cost of the components at some point in time, but it is still possible that electronic component suppliers may in the near term actually charge a premium to the user for *not* adding solder balls or nickel-gold finishes

processes that, paradoxically, in fact, *add* cost to the package.

Finally, reliability, which will be discussed in more detail, also has an impact on economics as warranty payouts for failed products can quickly cut into profits and perhaps even more importantly, undercut a company's reputation with its customers.

69.3.2.2 Electrical Benefits. Such constructions as have been described offer several electrical/electronic benefits. For example, where connections are made to terminations on component lands, the point of interconnection can be made without benefit of a large pad, which can reduce parasitic capacitance. This also frees routing space, allowing for a potential reduction in total layer count (further reducing cost). If proper planning is used in choosing components of a common grid pitch, the integrated power mesh system (IPMS) design layout approaches may be employed, reducing layer counts while improving signal integrity. The metal core is can serve as power or ground with a copper-over-plating as mentioned earlier, to allow for such. This makes it possible to provide both power and ground immediately adjacent to every component (this will be the subject of a future paper). Finally, the completed assembly can also be relatively easily provided with a metal plating after the assembly is complete (or in the latter stages of construction), making the entire assembly metal jacketed and thus EMI and ESD immune, as well as nearly hermetic, exclusive of those areas left open for external I/O connections.

69.3.2.3 Thermal Benefits. Aluminum is a common choice for heat spreaders for high-operating-temperature electronic devices, and in the present case, the heat spreader is an integral part of the assembly. This approach allows the designer to solve any potential thermal problems

on the front rather than the back end of the manufacturing process. The inverse relationship between long-term reliability and the number, temperature extremes and durations of the thermal excursions that must be endured by electronics components having a built-in thermal management solution is a value-added element and thus a potential economic benefit as well.

69.3.2.4 Mechanical Performance Improvements. Since the components are encapsulated in the assembly and thus part of an integrated whole, they are fundamentally immune to the effects of shock and vibration. The CTE (coefficient of thermal expansion) of aluminum and copper are relatively close (22 ppm/°C versus 18 ppm/°C), which reduces the potential stress on interconnections; moreover, the materials expand predictably in all directions, whereas reinforced laminates have CTEs that may vary in X, Y, and Z dimensions, sometimes quite appreciably (e.g., X ~20 ppm/°C, Y ~23 ppm/°C and Z ~80 ppm/°C) and in the case of flexible circuit materials much worse.

The microvias which are used to make connections to components and to any additional build-up layers have been proven superior to solder joints, which have continually proven a weak electromechanical link in traditional electronic assemblies (though there was recent report of microvias also being damaged by the lead-free soldering process). Moreover, there is possibility in some cases to use relatively thin aluminum base material, which could allow the developer to bypass the final etching process and permanently form the final assembly into the desired shape, opening up new possibilities to the clever product designer.

69.3.2.5 Design Security. The methods suggested for the manufacture of a rigid flex circuit as described offer a design security benefit that may not be immediately obvious to many product developers. The methods used obscure the

components used in fabrication, making tear-down and reverse engineering of a product much more daunting and difficult for those wishing to understand what might differentiate the product in hand with previous competitive products. This benefit extends to all kinds of products, from consumer to military. Furthermore, the assembly makes it much more difficult for unscrupulous individuals to extract and reuse components, injecting them into the supply chain as counterfeit devices.

69.3.2.6 Reliability Improvement. Improvement in reliability is largely a by-product of various elements of the electrical, thermal and mechanical performance benefits just discussed, combined with the benefits that can be obtained by simple bypassing of a high-temperature lead-free soldering process. To this point, it is worth repeating that the soldering process is typically the largest cause of defects in assembly and that solder joints are the most common sites for failure of electronic interconnection systems. Moreover, in a solderless assembly, concern over tin whiskers, a topic that has returned to prominence in recent years, is relieved. Finally, conductive anodic filaments (CAF), which is the growth of conductive fibers between adjacent vias in reinforced materials and tin whiskers are obviated by the ability to use homogeneous, unreinforced materials and elimination of solder, respectively.

69.3.2.7 Regulatory Compliance. The EU's RoHS legislative mandate to eliminate lead from electronics solder has proven very costly, however, this stricture is automatically accommodated if one eliminates solder completely. The finished structure described is basically an all-copper interconnection system. On the finished product, only the surface sites required for making electrical connection to the other system elements, such as switches, connectors and the like, need to have a contact finish. The

key point is that since neither copper nor aluminum is considered a problem, both the RoHS and REACH concerns should be obviated provided the other materials selected and used in the assembly (e.g., the flexible polymers) are compliant. Additionally, the material declaration process is greatly simplified. These same benefits hold true relative to the use of conflict materials which is of growing concern among increasing numbers of both governmental and nongovernmental organizations (NGOs) as the structures completed as described are completely devoid of any proscribed or sanctioned materials. In short, the assemblies described allow a product to much more easily pass regulatory scrutiny.

69.3.2.8 Environmental Friendliness. During the last few decades, concern over the environment has moved steadily into the consciousness of government officials, business leaders and the consuming public around the world. The term *social responsibility* is also often used to describe the concern; however, the fact that the industry makes products that impact the environment at the lowest possible level has become increasingly important. With that in mind, consider an electronic structure constructed principally of a material which is desirably and easily recycled, such as aluminum. Moreover, there is the significant amount of energy that is used in traditional manufacturing in component and assembly preparation and in the soldering process, which can be saved when solder is not used. Moreover as suggested earlier in this paper additional energy savings can be found by obviating need for all of the process steps leading up to and following the soldering process.

69.3.3 Discussion

As has been shown there are many reasons to embrace SAFE manufacturing methods for the fabrication of rigid flex circuits. Still, even with all of the cited benefits, there is one recurring concern that is often raised and/or registered relative to products which might be fabricated using SAFE methods: “How does one test and rework such assemblies?” The question is perhaps best addressed with a separate question: “If the process is executed properly and the components are not subjected to thermal extremes, why is there a need to test and rework?” The simple fact is that most electronic assembly problems are related to the inherent weakness of the soldering process and solder joint failure remain a common cause especially when there is shock or vibration. Moreover, below 0.5 mm lead pitch, which is where the component roadmap trends are headed, assembly yields drop off appreciably, even with multiple preassembly inspection steps implemented and/or applied. The EMS industry has come to accept the weakness of its assembly and cleaning processes even as it strives to constantly improve them, making marginal improvements through new materials and equipment and as a result has come to also expect that rework and repair are a natural part of the manufacturing process. This acceptance carries with it what can be best described as a self-defeating ingrained attitude and results in the manufacturing having to continually carry out a process that might otherwise be made unnecessary. In short, if the components are fully tested and burned-in and the processes used are properly controlled, the final product should be high yielding, provided the design is inherently valid and robust. The limits of reliability of future electronic products could well be better defined by IC reliability than the reliability of the circuits and plated vias that are used to interconnect them.

Such structures as have been described in the last section of this chapter are simple to design and eminently possible to manufacture. They can be easily produced using well-

established manufacturing infrastructure tools, equipment, and processing techniques which are simply reordered to make highly useful electronic products in a rigid flex format suitable for use in everything from consumer to high-reliability automotive, military and aerospace products. The limits are likely to be defined more by the imagination of the designer than the limits of the fundamental technology which has been described. Test vehicles are being prepared at this time and will soon be available for evaluation.

69.4 SUMMARY

Mulilayer flex and rigid flex circuits are seasoned and venerable technologies capable of solving many interconnection challenges as they have demonstrated over the last nearly 50 years. They are also typically highly complex structures requiring a great deal of engineering in order to realize a successful design. There was not sufficient space allotted to examine all of the variations possible when it comes to the design and manufacture of rigid flex circuits. With that in mind, it is again recommended that the reader seek the counsel of an experienced manufacturing engineer, one who understands the nuances of rigid flex manufacture before embarking on a rigid flex circuit design.

69.5 ACKNOWLEDGMENTS

The author extends his appreciation to the industry and the many who contributed to the progress of flexible circuit activities. Sincere thanks also goes to Dominique K. Numakura, at DKN Research, for his authorship of this chapter in the previous (6th) edition of *Printed Circuits Handbook*.

CHAPTER 70

SPECIAL CONSTRUCTIONS OF FLEXIBLE CIRCUITS

Dominique K. Numakura
DKN Research, Haverhill, Massachusetts

70.1 INTRODUCTION

Because of thin base layers, the flexible circuits can have many special constructions that are impossible to build by traditional manufacturing processes of the rigid circuit boards. These special constructions generate further functional values for the flexible circuits. This chapter introduces the major constructions in use, along with their manufacturing processes.

70.2 FLYING-LEAD CONSTRUCTION

Flying-lead construction is a special case of the double access flexible circuit. The base layer under the traces are removed and the conductors are completely free from the

organic materials. New HDI flexible circuit applications have arisen involving flying-lead constructions. Applications such as wireless suspension of hard disk drives, interposers for chip-scale packaging, and ultrasound probes depend on the reliability of this high-density interconnect. In competitive markets such as these, it is imperative that flying-lead applications offer low cost and high volume. The TAB (tape automated bonding) is one of the major application of the flying lead costructions.

Traditional manufacturing processes used to create flying leads, such as prepunching or predrilling, are not conducive to the quality levels and manufacturing yields required to achieve low cost, and alternative processes are needed, as described later.

70.2.1 Basic Design

A flying-lead structure is composed of a single layer of high-density-pitch copper conductors accessed from both sides of the substrate. Generally, the substrate side of a conductor on a circuit board is not electrically accessible because the conductive foil is typically laminated to the substrate board in sheet form. In the case of a flex circuit, however, the substrate can be removed by various methods. Dual access is created by removing the coverlayer in the same area on both sides.

Figure 70.1 indicates two basic structures of dual-access conductors, in both the single sided and double-sided types of flexible circuits. Figure 70.2 shows actual examples of the fine flying leads built on the single side circuits and double side circuits. Basically, a coverlayer is applied to the side of the conductive layer opposite the substrate. The coverlayer can be processed easily to create the top-side exposure. The flying lead is created when the base substrate is also removed in the same area.

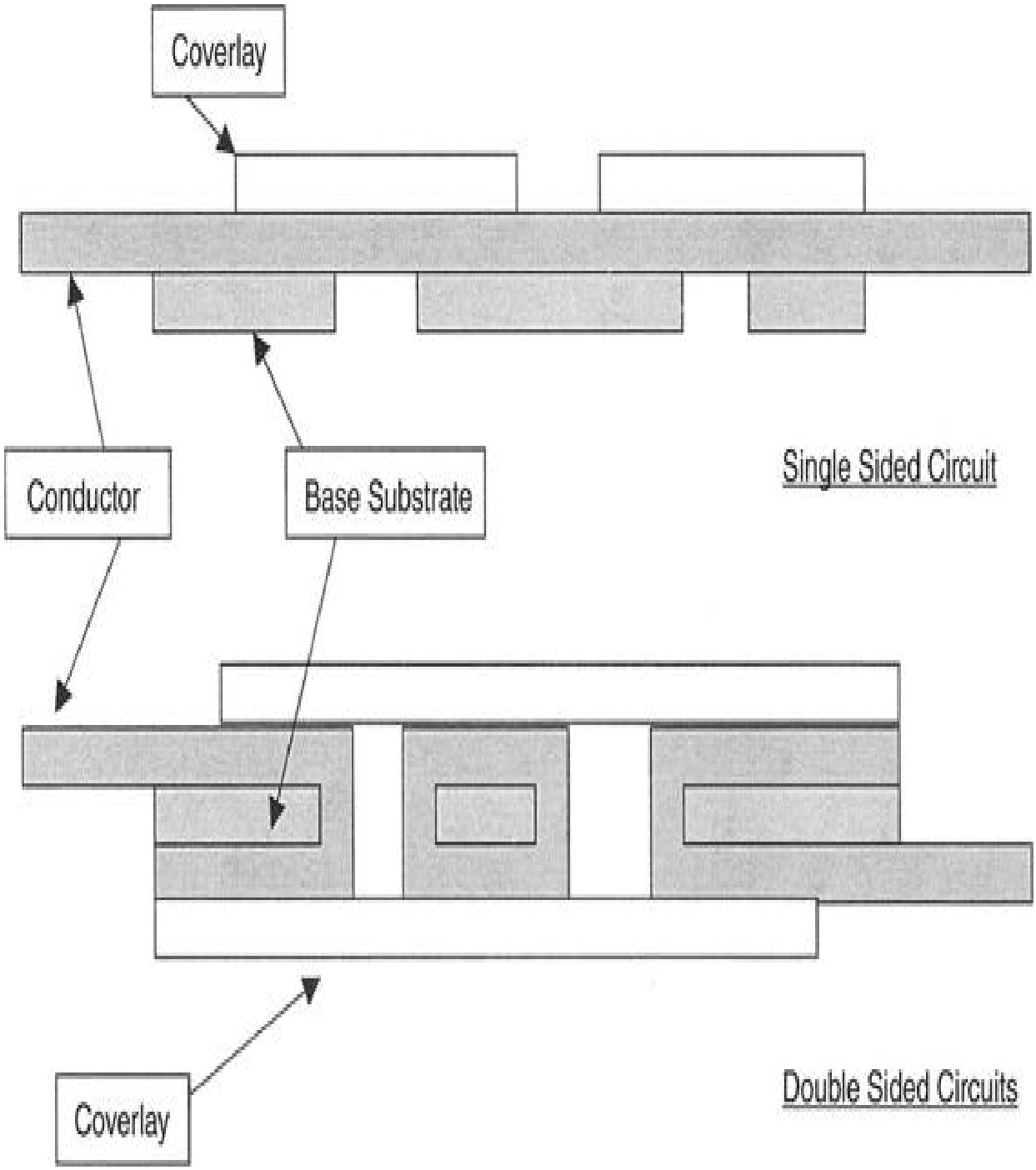


FIGURE 70.1 Basic constructions for flying-leads for flexible circuits.

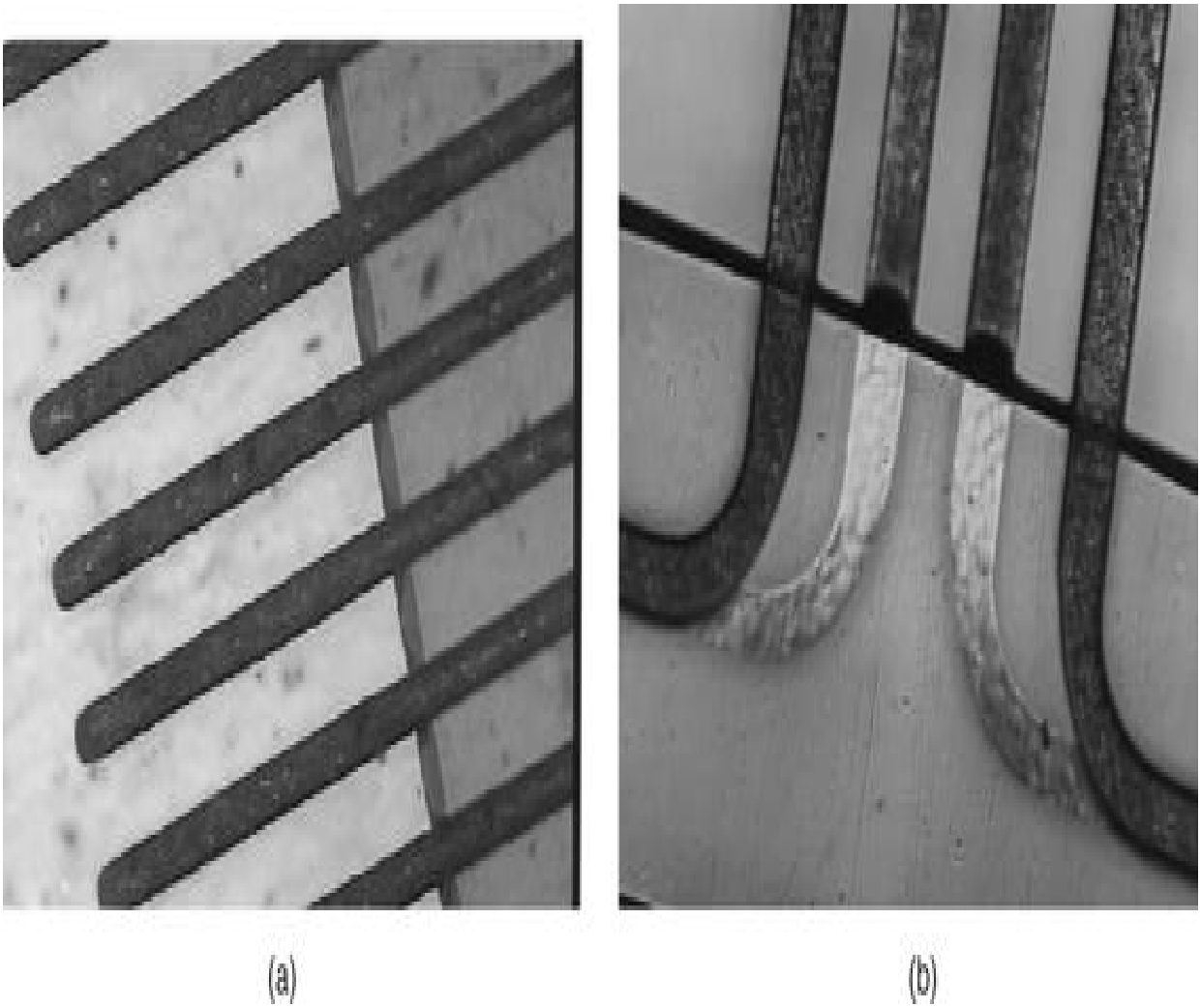


FIGURE 70.2 Typical fine flying leads construction (*a*) single side, (*b*) double side.

70.2.2 Manufacturing Processes for Flying Leads

The fragility of flying leads, caused by the lack of dielectric support, is probably the largest disadvantage in the manufacturing process. Proper circuit design and layout is the key to the manufacturing process yield and subsequent cost and physical performance of the circuit. The most conventional manufacturing process for generating a flying-lead construction involves a prepunching process similar to

the device hole process of tape automated bonding (TAB). Figure 70.3 shows this process schematically. There is no proprietary technology or special tooling required for manufacturing the prepunched window in the base substrate. This process, however, offers the manufacturer very little flexibility and is fairly labor intensive, which makes it difficult to maintain high productivity rates.

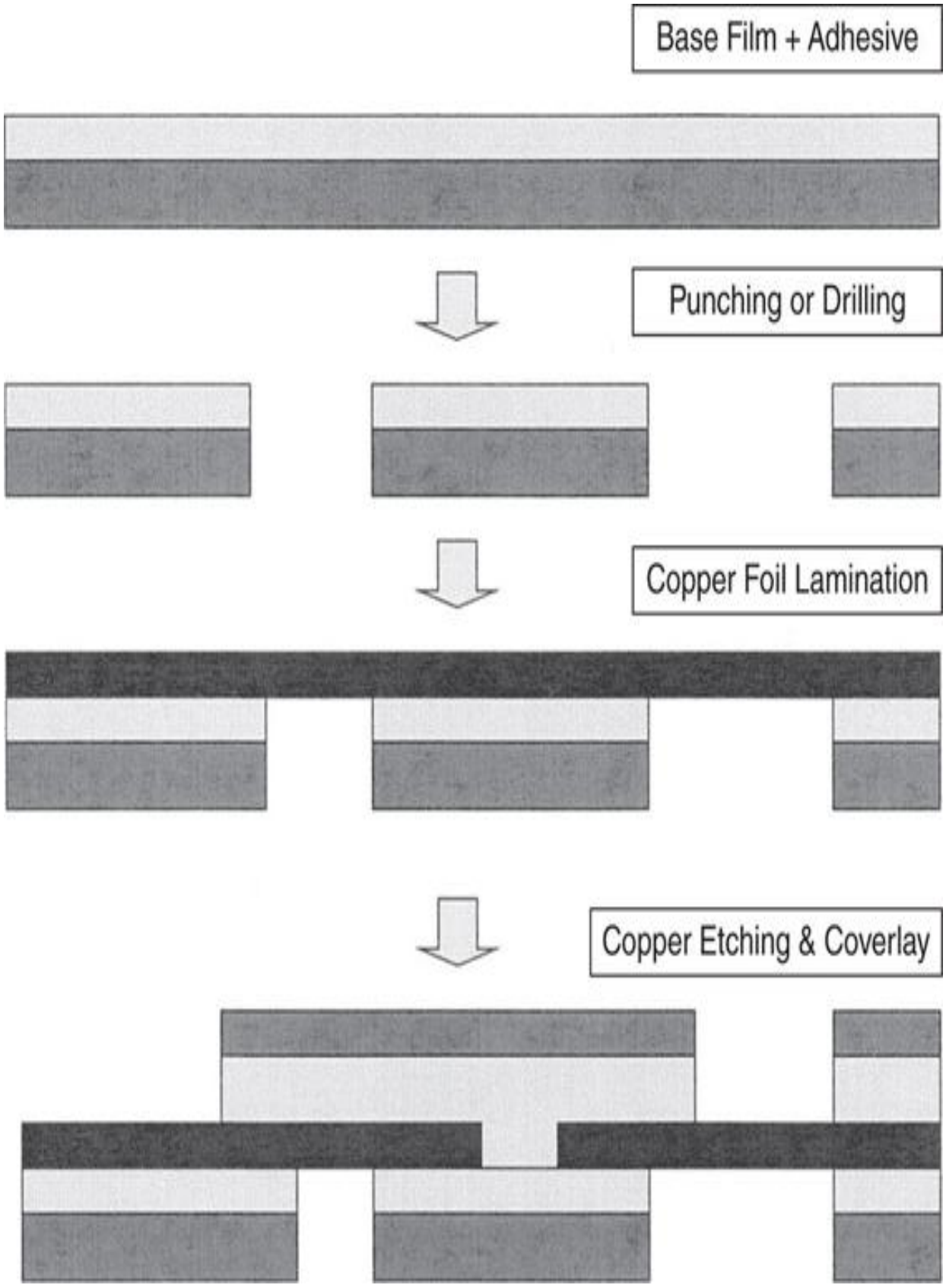
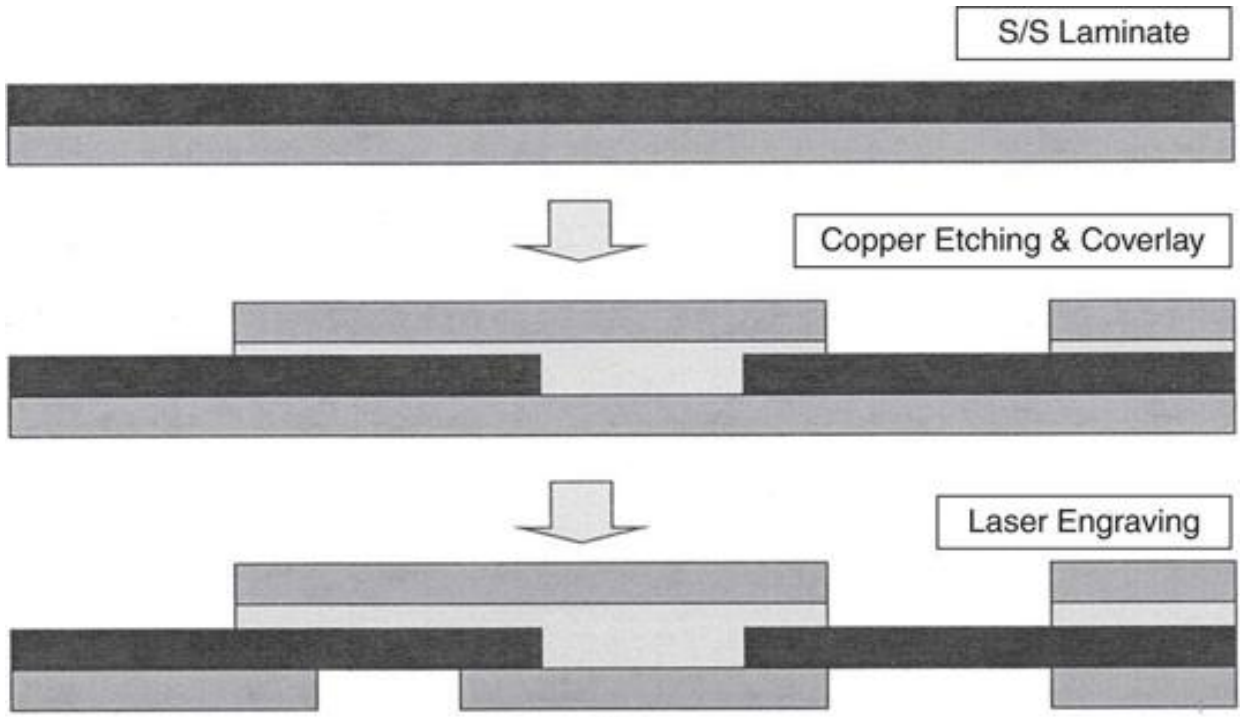

Base Film + Adhesive
Punching or Drilling
Copper Foil Lamination
Copper Etching & Coverlay

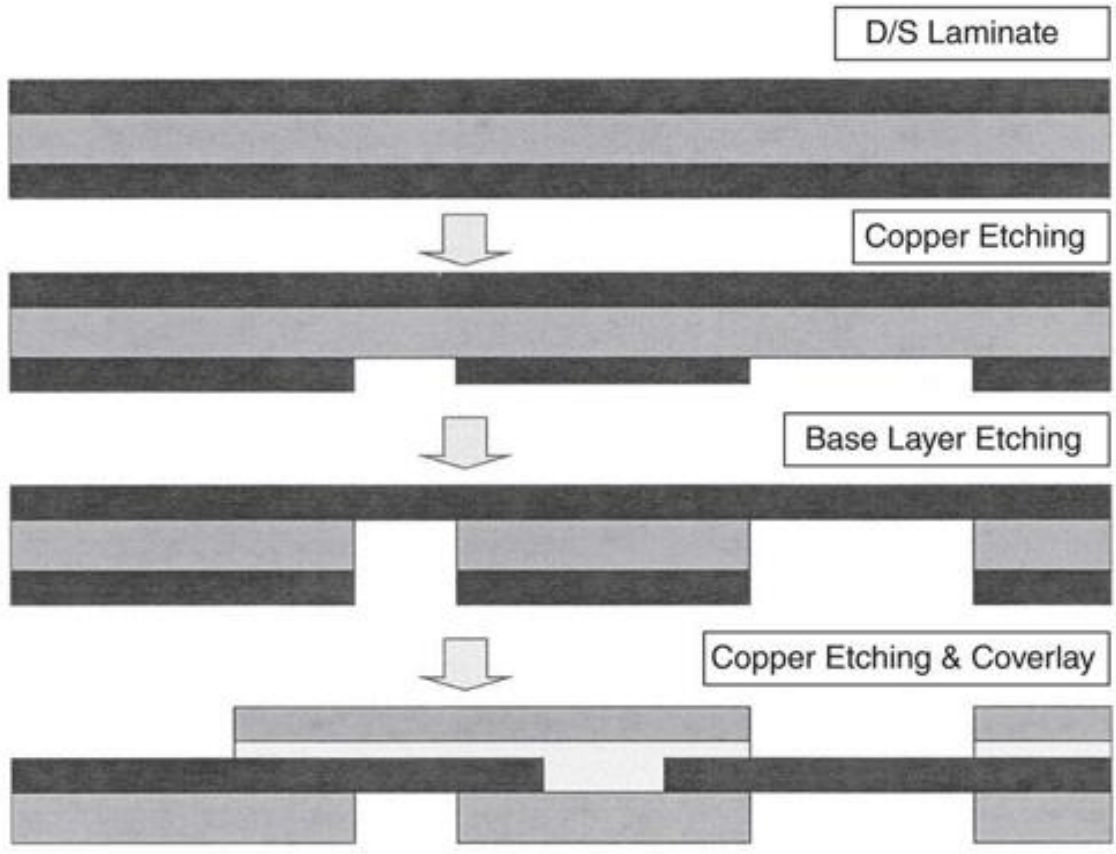
FIGURE 70.3 Manufactuirng process for flying-lead flexiblse circuit construction using prepunching method.

The handling of unstable punched films, along with thin, fragile copper foils, makes it difficult to achieve the high manufacturing yields required to support the cost model associated with high-density flexible circuits. These unstable film substrates also make it difficult to maintain dimensional accuracy between the fingers and the window, a key element for HDI flexible circuits. Adhesive flow or squeeze-out from the edge of the punched film along the conductor can also be an issue when dealing with small window exposures. Openings of less than 1.0 mm are difficult to create with high dimensional accuracy and yield.

Alternative technologies have been developed to generate high-density flying-lead designs with higher accuracy. Laser ablation, plasma etching, and chemical etching are just a few of the possibilities and are illustrated schematically in Fig. 70.4. A comparison of small opening capabilities of each of the processes is illustrated in Fig. 70.5, while a comparison of the technical capabilities of the processes is shown in Table 70.1. With these manufacturing technologies, many kinds of flying-lead constructions became possible.


S/S Laminate
Copper Etching & Coverlay
Laser Engraving

(a)


D/S Laminate
Copper Etching
Base Layer Etching
Copper Etching & Coverlay

(b)

FIGURE 70.4 Manufacturing process for flying lead flexible circuit construction using (*a*) laser ablartion and (*b*) plasma etching or chemical etching.

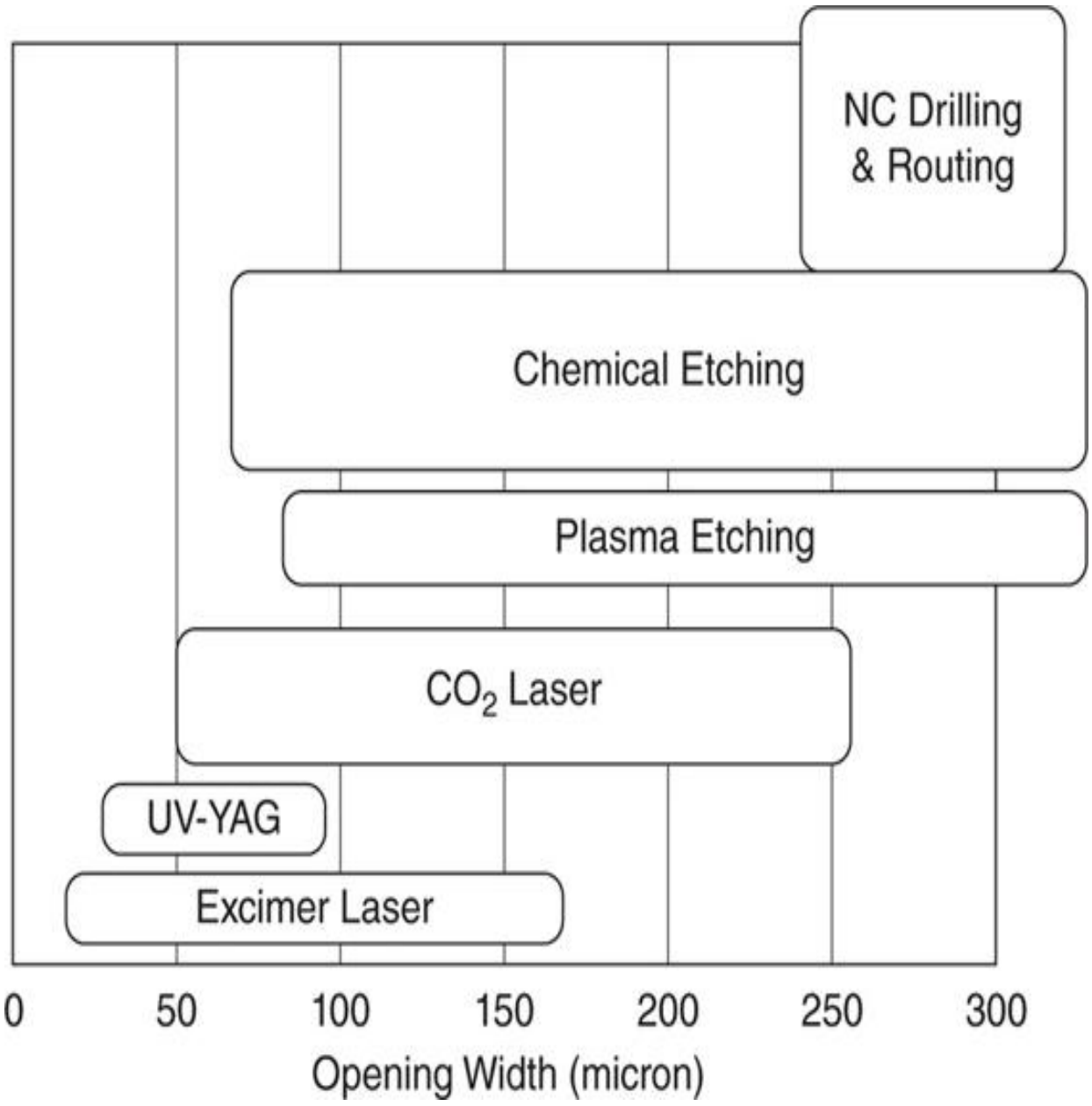


FIGURE 70.5 Comparison of opening sizes of flying-lead flexible circuit manufacturing processes.

TABLE 70.1 Comparison of Flying-Lead Manufacturing Technologies

	Prepunching (NC routing)	Laser Abrasion	Plasma Etching	Chemical Etching
Minimum slit width (μm)	800	50	100	70
Material availability	Fair	Wide	Wide	Limited
Design flexibility	Limited	Wide	Limited	Limited
Capability for high-density flying leads	Limited	Wide	Fair	Fair
Technical hurdles	Low	Fair	High	High
Registration	Difficult	Fair	Fair	Fair
Damage on flying leads	Serious	Small	Fair	Fair
Process cost	High	High	Low	Low
Investment for large volume	Small	High	High	Medium

70.2.3 Laser Abrasion

The excimer laser process has the capability to generate small openings with clearly defined edges on high-density flexible circuits. The narrow slit openings can be made smaller than 50 mm wide. The excimer process is available for all types of flexible circuit materials with high accuracy and fine openings. A carbon residue, typically removed by a suitable wet cleaning process, is found around the edges of the openings. One of the biggest disadvantages of excimer laser system is its slow speed, which accounts for the high processing cost when dealing with larger openings.

The UV:YAG laser process offers a higher productivity rate than the excimer laser for very small openings. It has the ability to cut both copper foil and organic substrate materials with good quality, which makes it suitable for cutting small openings on a wide range of high-density flexible circuits. Unfortunately, the productivity rate becomes extremely slow

when cutting larger openings. Actually, it becomes impractical from a cost standpoint to utilize a UV:YAG laser system for openings larger than 10,000 mm^2.

Carbon dioxide TEA lasers, as well as diamond carbon dioxide lasers, have a much higher productivity rate when producing openings wider than 70 mm. The definition of the opening and quality of the edges, however, is somewhat less desirable than for other laser systems. In order to facilitate surface plating, a suitable cleaning process such as plasma is required to remove the thin residue remaining on the copper surface. A copper mask process helps to improve both quality and speed of the carbon dioxide laser process.

The excimer laser process, like the UV:YAG laser system, minimizes the potential for thermal damage on very thin flying leads. The carbon dioxide laser generates a remarkable amount of heat. The beam power density of the laser must be controlled carefully in order to process 18-mm copper with high-density flying leads narrower than 100 mm wide.

70.2.4 Plasma Etching and Chemical Etching

Plasma and chemical etching processes are other suitable choices for generating high-density flying-lead structures. Although their capabilities are somewhat less than those of laser processing, these processes can provide a lower-cost model of high-volume processing. A copper foil mask is required in order to define the exposure area, and specific process conditions are required to remove organic substrates effectively. These processes are quite effective for single-sided substrates. Double-sided substrates can be processed in this manner given very specific materials and construction.

A big advantage of these processes is the unlimited number of holes or openings that can be processed simultaneously. Performance value is high, while manufacturing costs remain fixed when larger sizes or higher numbers of holes are processed. The plasma process is capable of etching all kinds of organic materials; however, it must be performed in a vacuum chamber.

Capital investment is relatively large for high-volume production. Another issue involves uniform quality over a large working area/panel size in a vacuum chamber of limited size.

Depending on the process conditions, plasma etching creates a wall slope of 30° to 60° at the edge of the openings, and it is difficult to make holes smaller than 100 mm in diameter on a 50-mm-thick polyimide layer.

Chemical etching also offers a low-cost process for creating access openings in high volume on polyimide-based high-density flexible circuits. This process offers the capability of generating openings smaller than 100 mm in diameter or slit width on 25-mm substrates, while providing a very small slope on the wall definition of the opening. The issue in this process is finding the appropriate chemicals and creating the suitable conditions to etch the various flexible substrates.

Sodium hydroxide and potassium hydroxide are popular chemicals for etching Kapton type polyimide materials. Dangerous chemistries and tightly controlled process conditions are required to etch dimensionally stable polyimide substrates such as Upilex. Serious consideration must be given to choosing the appropriate circuit design, materials, and manufacturing processes. On the other hand, chemical processing such as this requires no specialized capital equipment, and it is extremely suitable for high-volume roll-to-roll manufacturing systems.

Typical high-density flying leads produced by new processes are shown in Fig. 70.6.

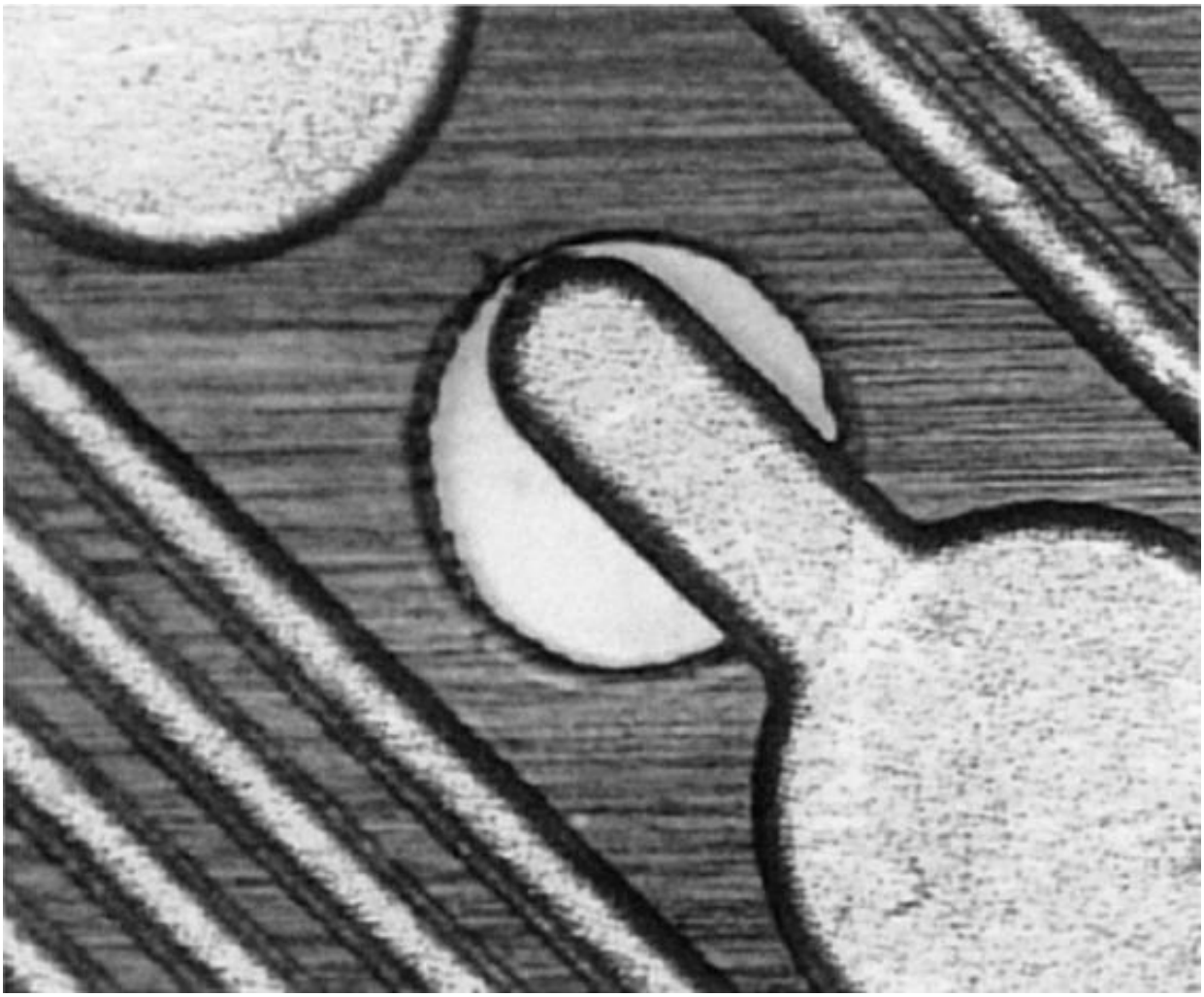


FIGURE 70.6 An example of a tab-shaped flying lead flexible circuit construction. (*Source: Asahi Fine Technology*.)

70.2.5 Economical Comparison

Each technology has its own cost structure, which is dependent on the conditions. Figure 70.7 shows a comparison from an economic study of the various technologies. This study was conducted on 25-mm-thick polyimide substrate with a 300-mm^2 working size. The opening size is assumed to be 0.1 × 3 mm, with flying leads at a 150-mm pitch processed on 18-mm-thick copper.

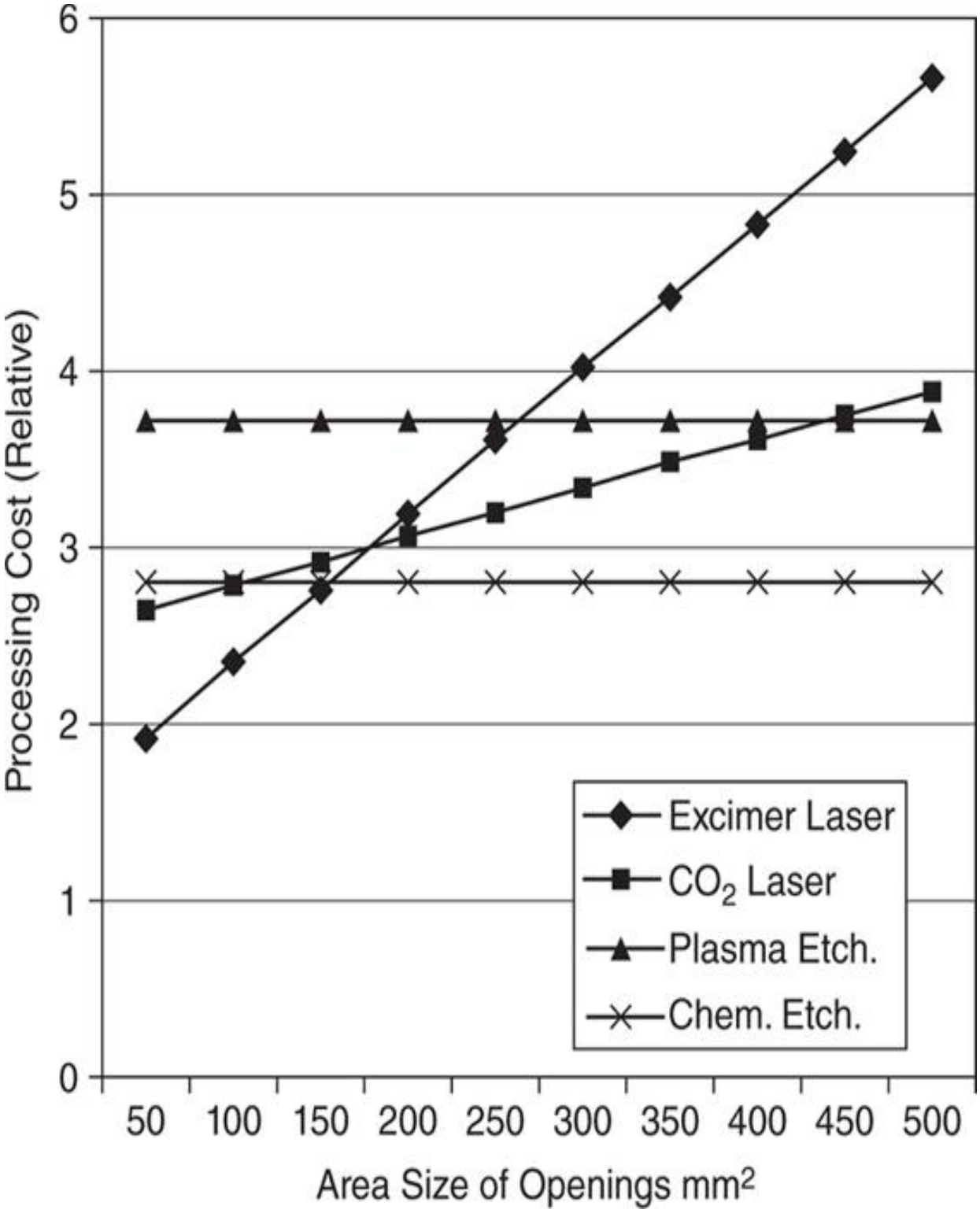


FIGURE 70.7 Cost comparison of flying-lead flexible circuit manufacturing processes.

Plasma and chemical etching processes have little dependency on the size or numbers of openings because they are based on batch processing of the materials in sheets. In contrast, the relative costs of the excimer and carbon dioxide laser process are proportional to the size of the area being processed as well as the opening sizes. This is primarily based on the small size of the laser beam as compared to the size of the opening, and on the need to overlap with each pass of the laser in order to remove the substrate in larger areas. The carbon dioxide laser, however, has higher manufacturing costs than the excimer laser process because of the additional chemical processes required to remove the organic residue left on the copper surface, but it has a lower associated manufacturing cost for larger opening sizes due to faster abrasion speeds.

70.3 TAPE AUTOMATED BONDING

TAB has been developed as the special wiring material for IC chips and liquid crystal displays (LCDs). Although it was developed separately from standard flexible circuits, they have similar constructions and they use similar materials, and can be categorized as one kind of flexible circuits.

70.3.1 Basic Concepts

Basic construction of TAB is the same as that of the flying-lead structure of flex circuits except for the web size used in manufacturing and the sprocket holes made for reel-to-reel conveyor systems which give TAB an appearance similar to that of cinema film. A 35-mm-wide web is the most common standard width for TAB. Webs 70 and 155 mm wide are available for larger circuits, nowadays. Because of the small working areas, TAB is good at producing fine traces with

flying leads. The reeled circuits are convenient for automation of circuit manufacturing and termination. A short strip circuit made by standard manufacturing processes for flex circuits is also called a TAB circuit because it has the same functions. (Examples of TAB are shown in Fig. 70.8.)

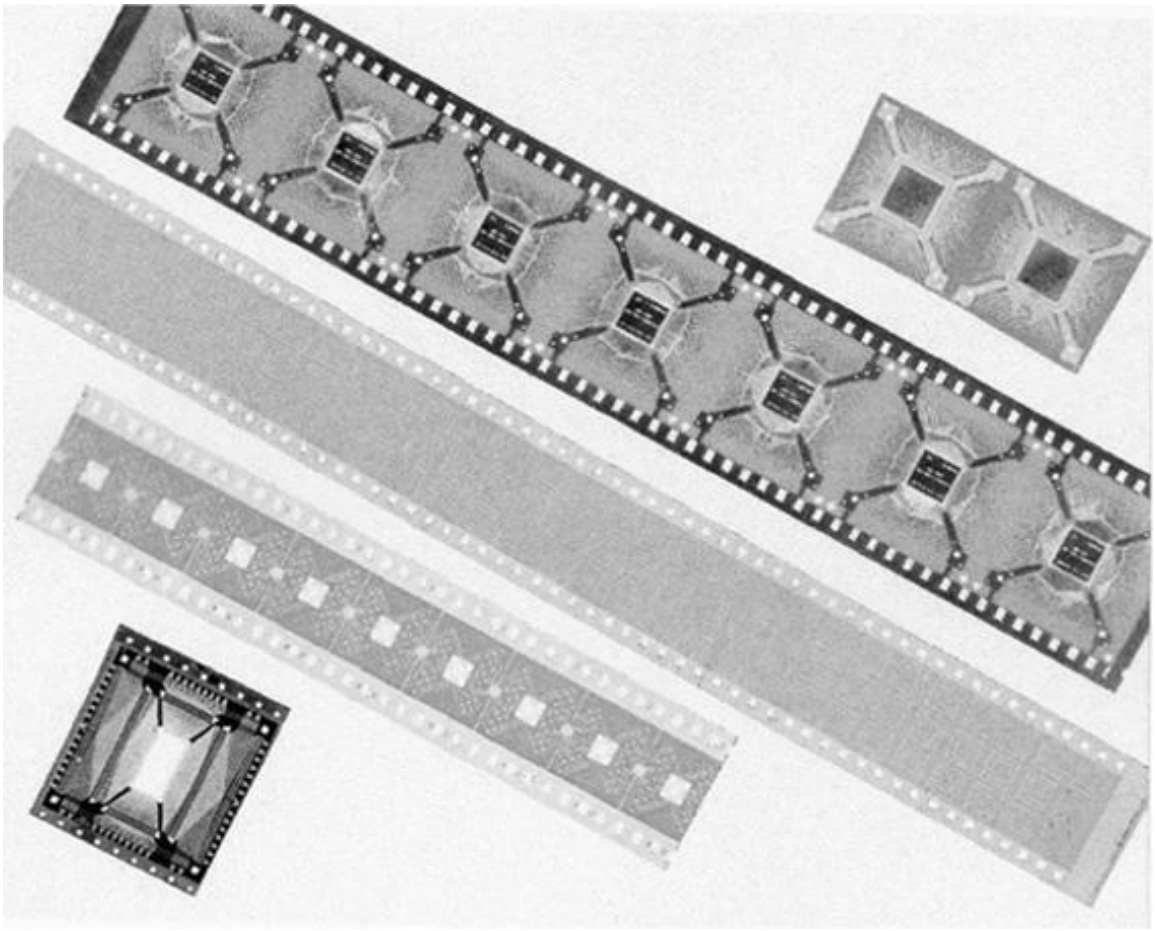


FIGURE 70.8 Examples of TAB high-density flexible circuits.

70.3.2 Manufacturing Processes

The basic manufacturing flow of single-sided TAB is the same as that of the traditional prepunch manufacturing process of flying-lead construction. Basically, all manufacturing processes of TAB are designed for automatic reel-to-reel equipment. Actual processing steps are slightly different as

shown in Fig. 70.9. The process starts from a plain film, mostly polyimide film. The first parts of the manufacturing are glue coating and punching of the hole generation. Secondary, a copper foil is laminated and the fine traces are generated by photolithography and chemical etching. Thirdly, final finishing such as cover coating and surface finishing is conducted. All of the processing equipment has to have loader and unloader by reels. The machines should be free from manual handling to eliminate the mechanical damages on the fragile fine flying leads. The whole process has to be kept in clean rooms to avoid the contamination for the fine lithography processes.

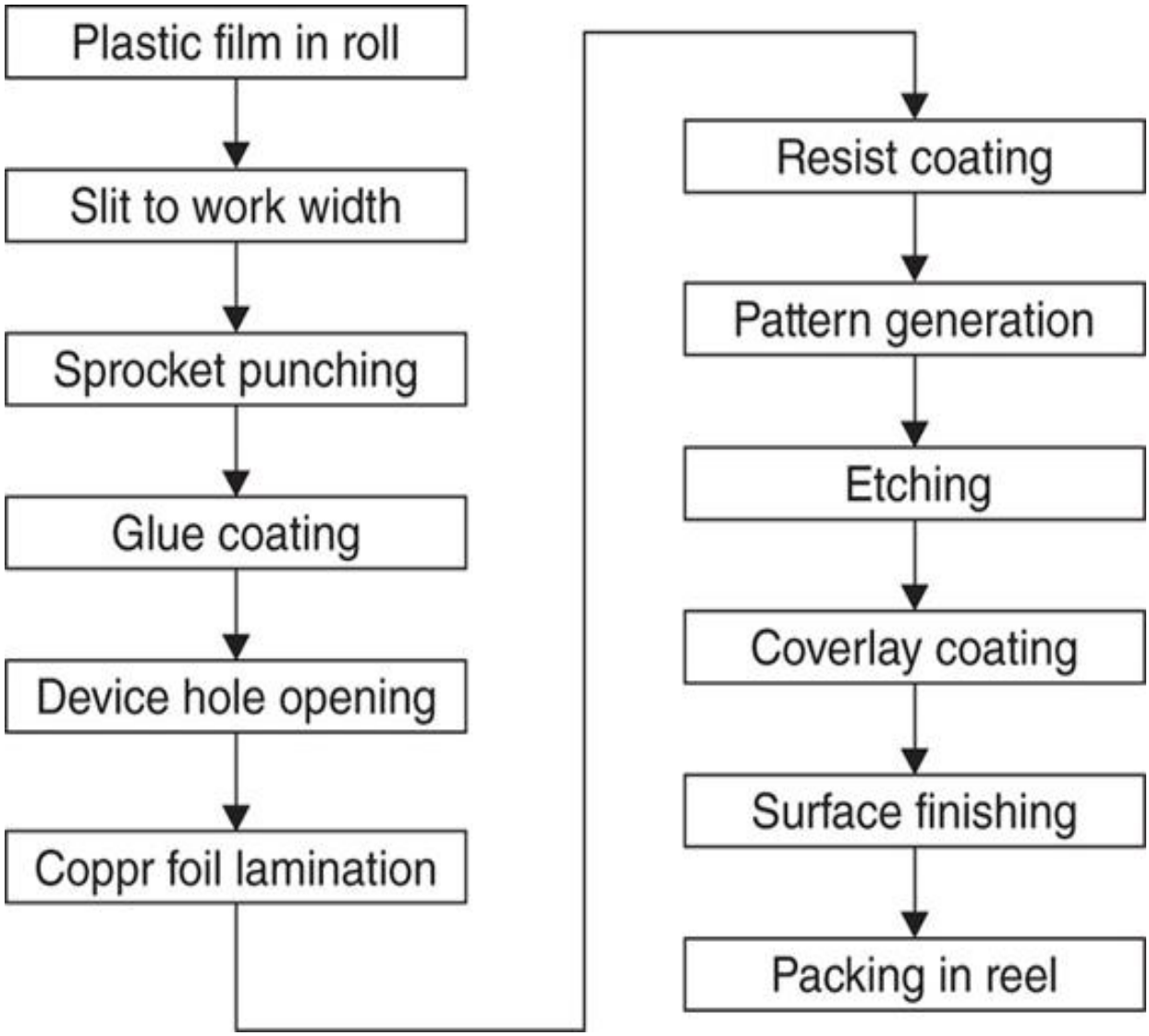


FIGURE 70.9 Manufacturing process flow of TAB.

Because of the narrower material width, TAB constructions have high capability for fine-line generation with good dimensional accuracy. The chemical etching process is also available to generate device holes. The technology can generate 40-mm-pitch traces as the flying leads.

The manufacturing process for the double side TAB with fine flying leads and micro via holes is much more complicated. Very few manufacturers are capable to produce the products with high yield.

70.3.3 Technology Movement of TAB

The TAB manufacturing technology has been experiencing a great progress since 1980s. However, it has been facing a turning point to change the basic process drastically for the finer circuitries.

TAB's manufacturing capabilities are very different from traditional flexible circuits and they cover different application area as shown in Fig. 70.10. TAB has been focusing single side fine traces with flying lead constructions. It has advantages for the volume productions of the small size circuitries because of special reel-to-reel manufacturing.

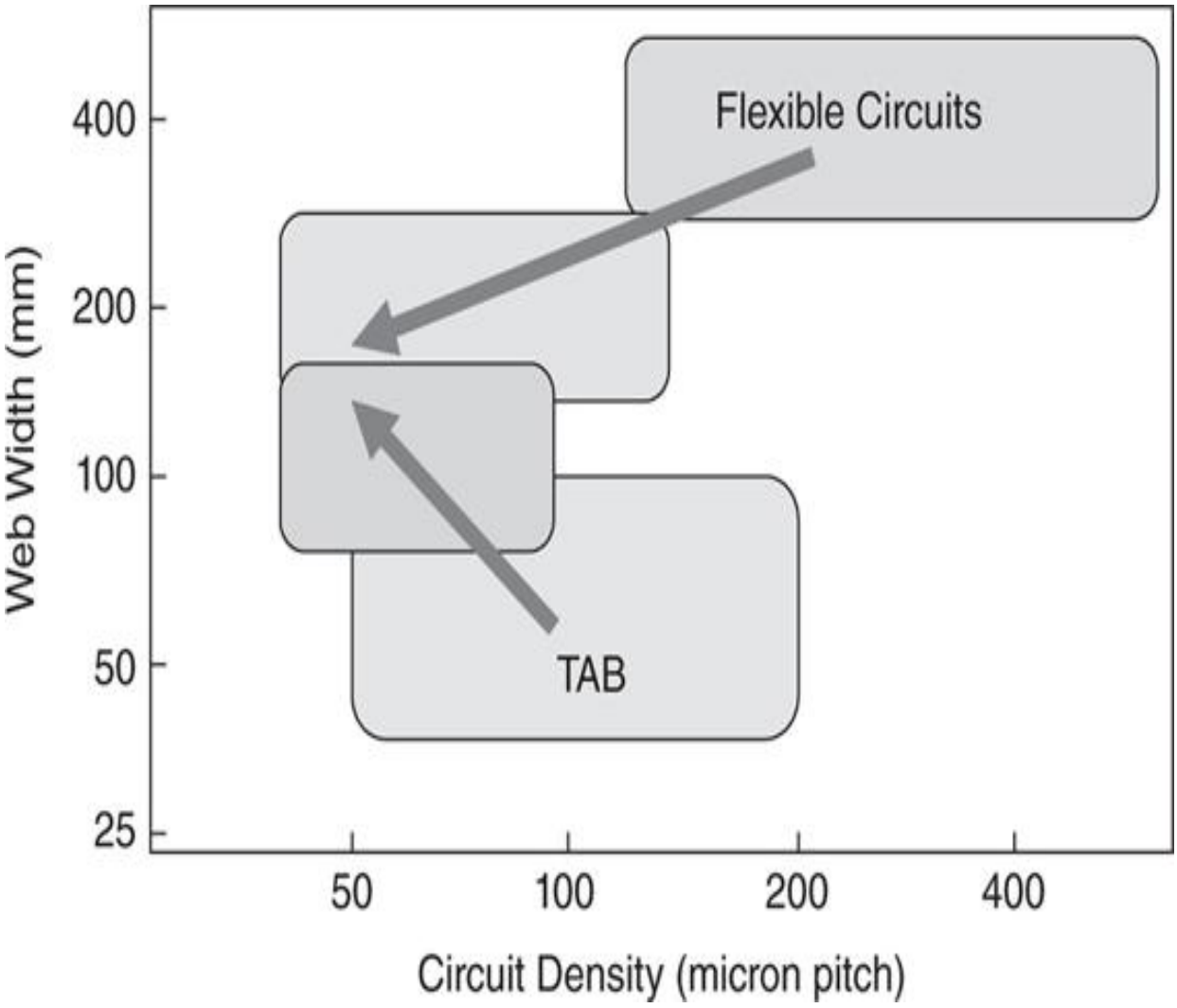


FIGURE 70.10 Recent movement of TAB and high density flexible circuits.

In early usage, only 35 mm wide web was available to have high dimensional stabilities. But the latest RTR manufacturing equipment can manage 155 mm wide materials to generate 40 µm pitch flying leads. Several new processes such as laser drilling and through hole plating have been introduced to produce double side TAB with fine flying leads.

Forty micro meters pitch of traces is almost the technical limit to manage the fragile fine flying leads for both of manufacturing and termination. Therefore, the technology is moving to COF (Chip on Film), that does not have device holes and flying leads, to have finer traces than 40 µm pitches. The manufacturing process and materials do not have significant differences from the roll-to-roll manufacturing process of the fine flexible circuits. On the other hand, the fine line capabilities of the flexible circuits have been getting better reducing their RTR web size.

TAB and flexible circuits had different capabilities in the past. But they have been moving to the same fine circuit area, and there have not bee remarkable differences in their manufacturing processes as shown in Fig. 70.10.

70.4 MICROBUMP ARRAYS

A variety of shapes and materials for micro bump arrays on flexible circuits have been developed to accommodate specific applications.

70.4.1 Varieties of the Bump Shapes and Applications

There are several choices of places to build micro bumps on flexible circuits, as described in Chap. 64 (see Sec. 64.3.8). The same processes used to build ball grid arrays on rigid circuit boards are appropriate for flexible circuits with flexible photo imageable solder mask. It is possible to build micro bumps on bare conductors using plating masks. Many micro bumps are built on fine flying leads without solder masks. A valuable construction of a flexible circuit is micro bumps built on the other side of the circuit through the dielectric layer. This can provide a reliable micro bump array because of the stable construction.

Many different shapes have been developed for micro bump arrays. The fusing solder process can make a spherical bump shape easily. Electrical plating of copper, nickel, gold, and combinations of these elements can provide many varieties of bump shapes. Changing the combination ratios and other factors can generate flat disks, flat domes, straight columns, etc. (Fig. 70.11). The best combination can provide 100- to 150-mm-pitch micro bump arrays on 50-mm-thick dielectric layers.

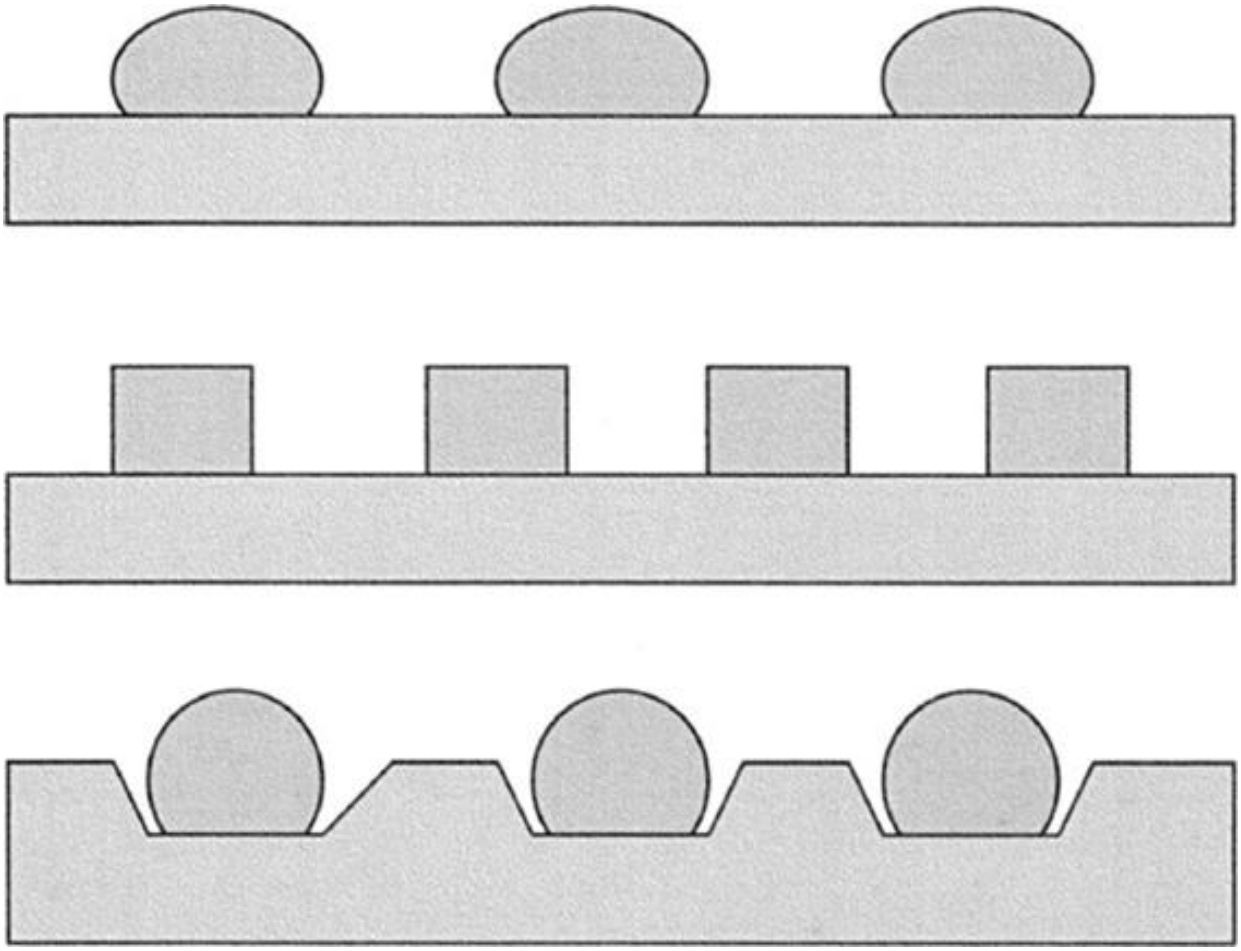
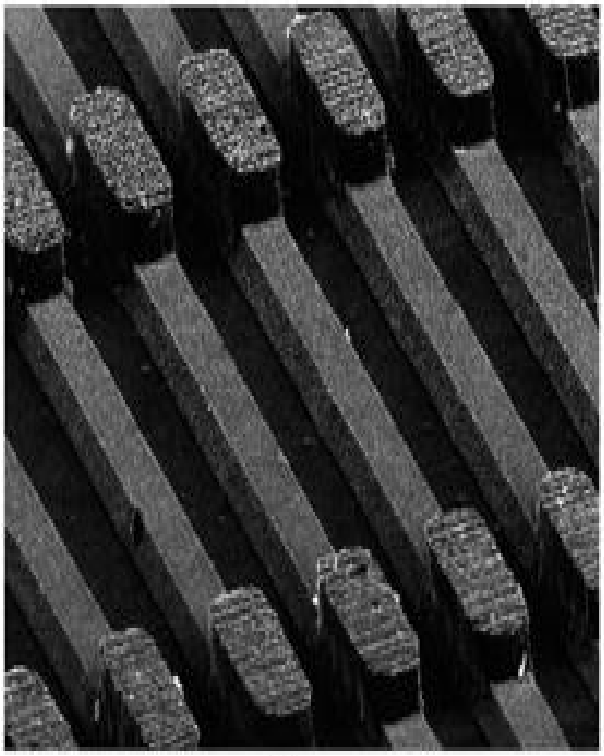
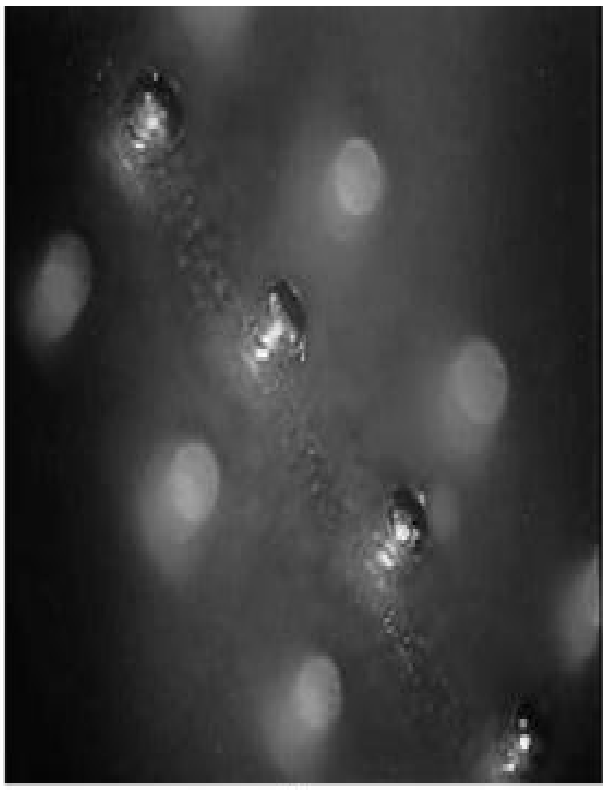


FIGURE 70.11 Microbump arrays on flexible circuits: examples of bump shapes.

Most of the micro bump array constructions of flexible circuits have been developed for high-density termination (e.g., flip-chip, CSP, test probes, etc.). A suitable design shape and materials should be chosen according to the requirements of the termination. Several examples are shown in Fig. 70.12.



(a)



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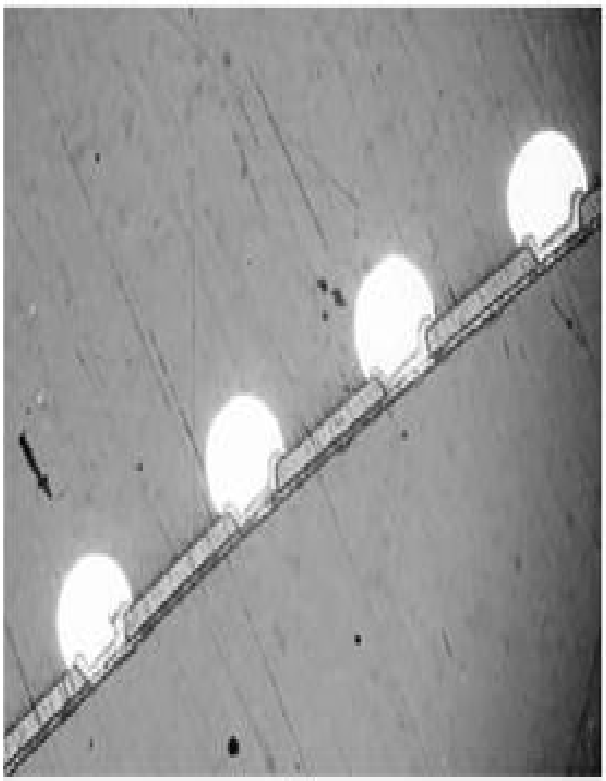

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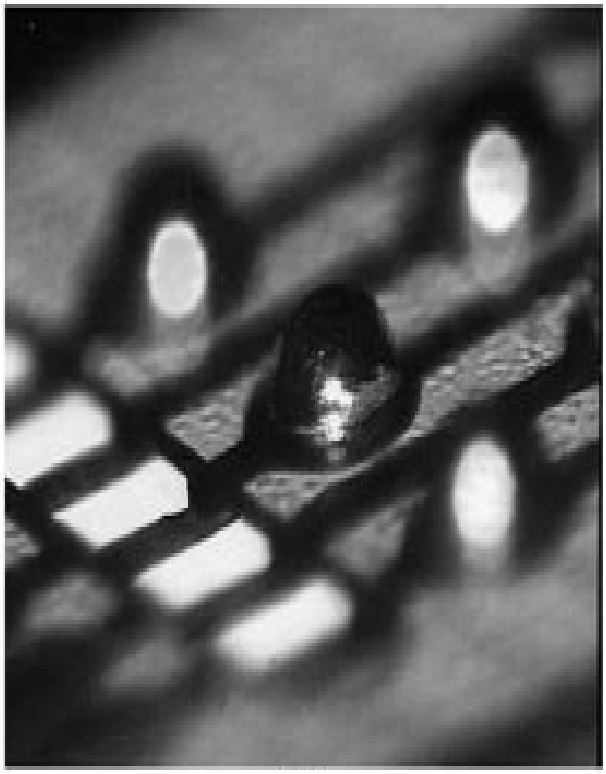


(d)

FIGURE 70.12 Various micro bump arrays on flexible circuits: (*a*) column shape copper bump array on the bare traces, (*b*) column shape Ni/Au bump array built through covelay, (*c*) solder ball array built though base substrate, (*d*) combination of flying leads and solder ball array.

70.4.2 Manufacturing

There are two kinds of manufacturing processes for the micro bump array on flex circuits:

1. The same technology as for ball grid arrays may be used. Solder paste is dispensed on the pads of the circuits with a liquid dispenser or screen printer. The solder paste will form spherical shapes for a refusing process. The process is available for relatively large solder balls.
2. Electroplating processes are used for small solder balls and nonspherical micro bumps.

Suitable combinations of different metal plating can provide wide varieties of micro bumps.

There are several factors that determine the shape and size of the bumps. The thickness of the dielectric layer and the size of the opening are the major factors in determining the bump shapes. The bump shapes will be more spherical when the aspect ratio of the opening is large.

The bump shapes will be like flat discs when the aspect ratio is small. An appropriate plating mask will help to build straight, high bumps.

When the micro bumps need to be built through the insulation layers, it requires a suitable hole generation process. Several laser drilling processes are recommended for small sizes but exact dimensions. Plasma etching and chemical etching are recommended for low cost processing with large numbers of the holes.

70.5 THICK-FILM CONDUCTOR FLEX CIRCUITS

A thick-film circuit is a type of additive manufacturing process. If an organic resin matrix is used, the conductor can be flexible, and this process has been applied in flexible circuits.

70.5.1 Materials

A silver paste conductor with an acrylic resin matrix is the most popular conductor material as the major thick-film conductor material for flexible circuits. It can provide very flexible conductor layers via a simple screen-printing process. Copper-based and carbon-based paste materials have been developed as the low-cost materials, but their conductivity is very low and unstable, and therefore their applicable areas are limited.

The screen printing process with conductive paste provide low cost solutions for the large size flexible circuit employing economical plastic films such as PET films.

70.5.2 Applications

A silver paste thick-film flexible circuit built on polyester film can provide the lowest-cost solution for large circuits. Unfortunately, the conductivity of the traces is much lower than for copper foil conductors, and this material is not available for power circuits or signal layers of high-speed circuits. Standard soldering is not available because of the acrylic-based matrix.

The largest application of thick-film-based flexible circuits is in membrane switches, which need large circuit spaces but

do not carry large currents. The majority of membrane switches are covered by silver paste thick-film flexible circuits. Major switching circuits of keyboard switches are also covered by the same constructions. Most of the key board circuits are covered by the silver paste base membrane switches. Most of the touch panel switches designed for micro waves, office appliances and medical equipment also use PET based membrane switches. Several examples are shown in Fig. 70.13.

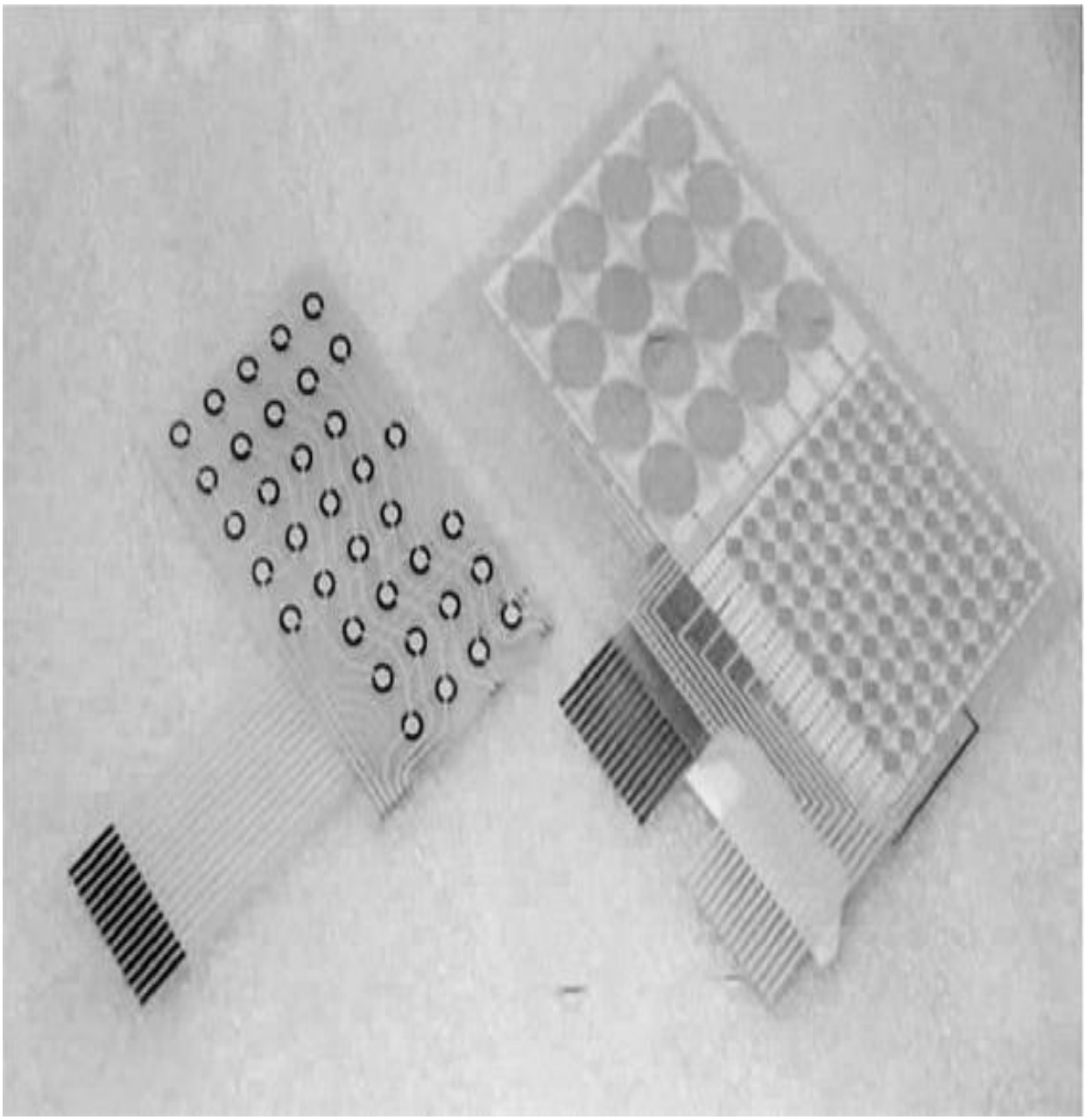


FIGURE 70.13 Membrane switch made by thick film process.

PET based thick film flexible circuits have been consumed for the touch panel switches of the electronic terminals such as PDA because of their transparency.

70.5.3 Manufacturing Process

It is a very simple process to build a thick-film flexible circuit. There are two steps:

1. Screen printing on a flexible film followed by baking
2. Blanking

This still requires that the process conditions be controlled carefully. The basic properties of these circuits change significantly depending on these conditions. A prebaking step is recommended for polyester film substrate to eliminate thermal shrinkage during baking for printed conductor paste. It is not difficult to apply the roll-to-roll manufacturing system for large volume because of the simplicity of the processes.

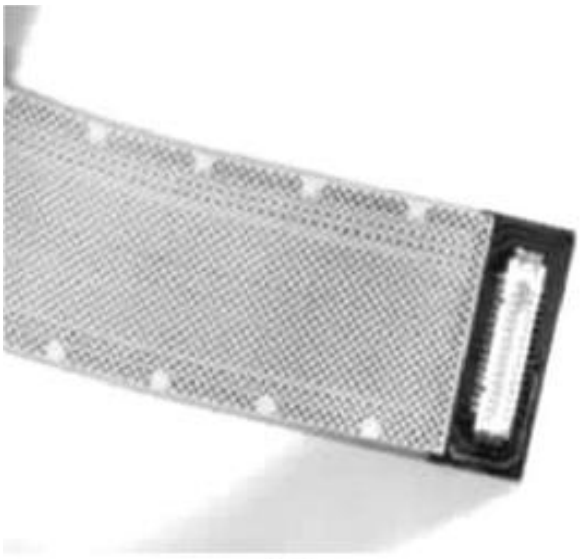
The latest technologies of the printers and screens are able to produce 10- to 15-mm line space with low cost. The electrical properties and trace densities are very depend on the conductor paste. A combination with screen printable nano conductive paste will provide fine conductive traces by a simple manufacturing process.

70.6 SHIELDING OF THE FLEXIBLE CABLES

When the flexible circuits are used as the cables for the high-speed telecommunications, appropriate shielding systems are required. Generally, the cable will be bent frequently, therefore the shielding layers should also have high flexibilities.

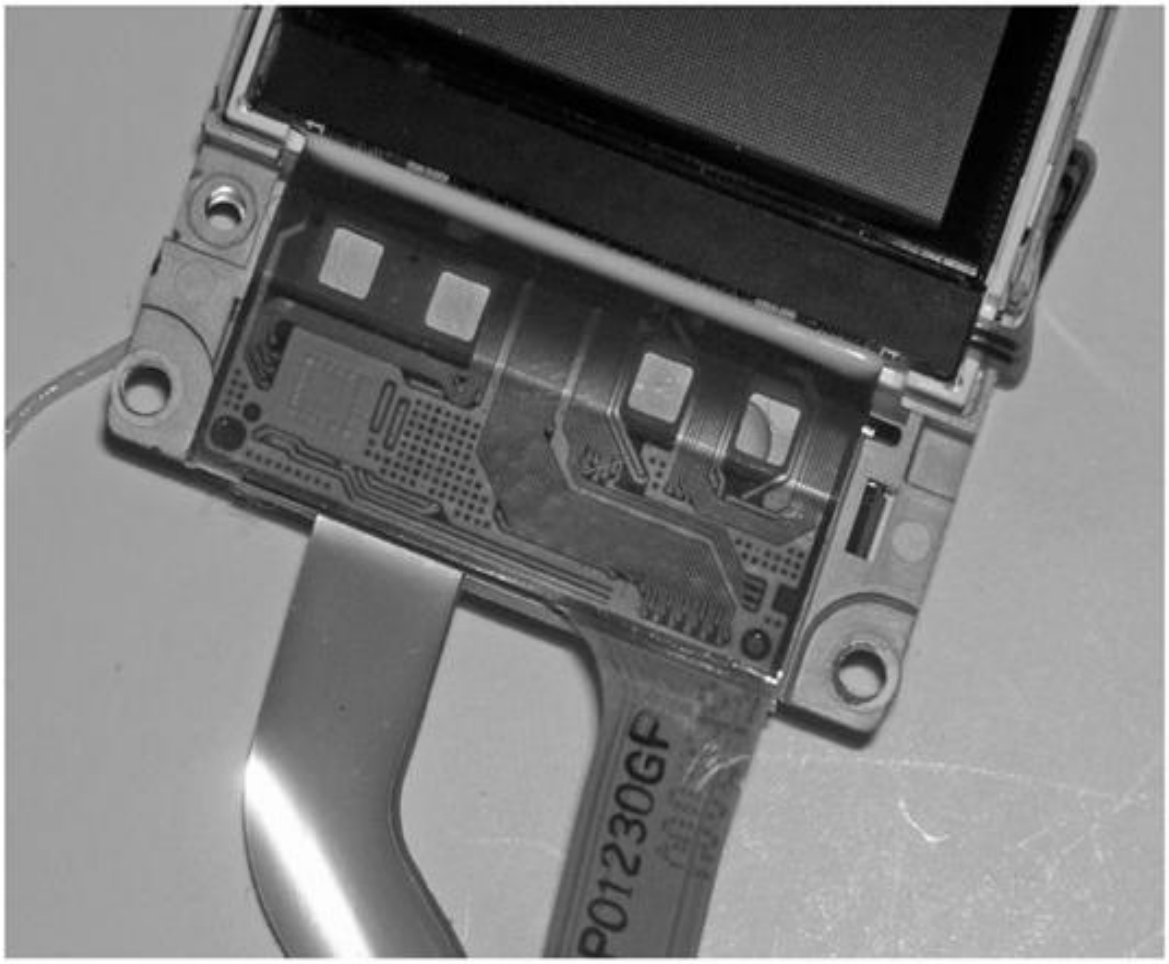
Several materials and constructions are available for the shielding of the flexible cables as shown in Fig. 70.14. Screen-printing of silver paste provides both high shielding effect and high flexibility. Screen-printing of carbon paste provides low cost solution. But its shielding effects are

limited. Thermal lamination of a thin aluminum foil with thin flexible adhesive provides a reliable solution for both shielding efficiencies and flexibilities.



(a)

(b)



(c)

FIGURE 70.14 Shielding of the flexible cables: (*a*) screen-printing of silver paste, (*b*) screen-printing of carbon paste, (*c*) lamination of thin aluminum foil.

70.7 FUNCTIONAL FLEXIBLE CIRCUITS

Various new processes have been developed to build functional elements and devices on the flexible substrates. They have been generating more functions than wiring or assembling board of the discrete components. They are the similar ideas as embedded passive technologies of multilayer boards, but they generate more values with flexible substrates. Table 70.2 shows several material examples and applications. Printed electronics (PE) is the 'next step' in this evolution of flexible interconnects.

TABLE 70.2 Functional Materials for Flexible Circuits

Materials	Functions
NiCr, W	Embedded resistors Heater Mechanical sensors
BaTiO	Embedded capacitance
Tin oxide	Transparent electrode
Poly silicone	Embedded active devices Transistors and diodes Sensor devices
Organic EL	Flexible displays

Figure 70.15 shows examples of sputtered nickel/chromium alloy. The first one is embedded resistors and the second one is a small strain gage built on the flexible substates.

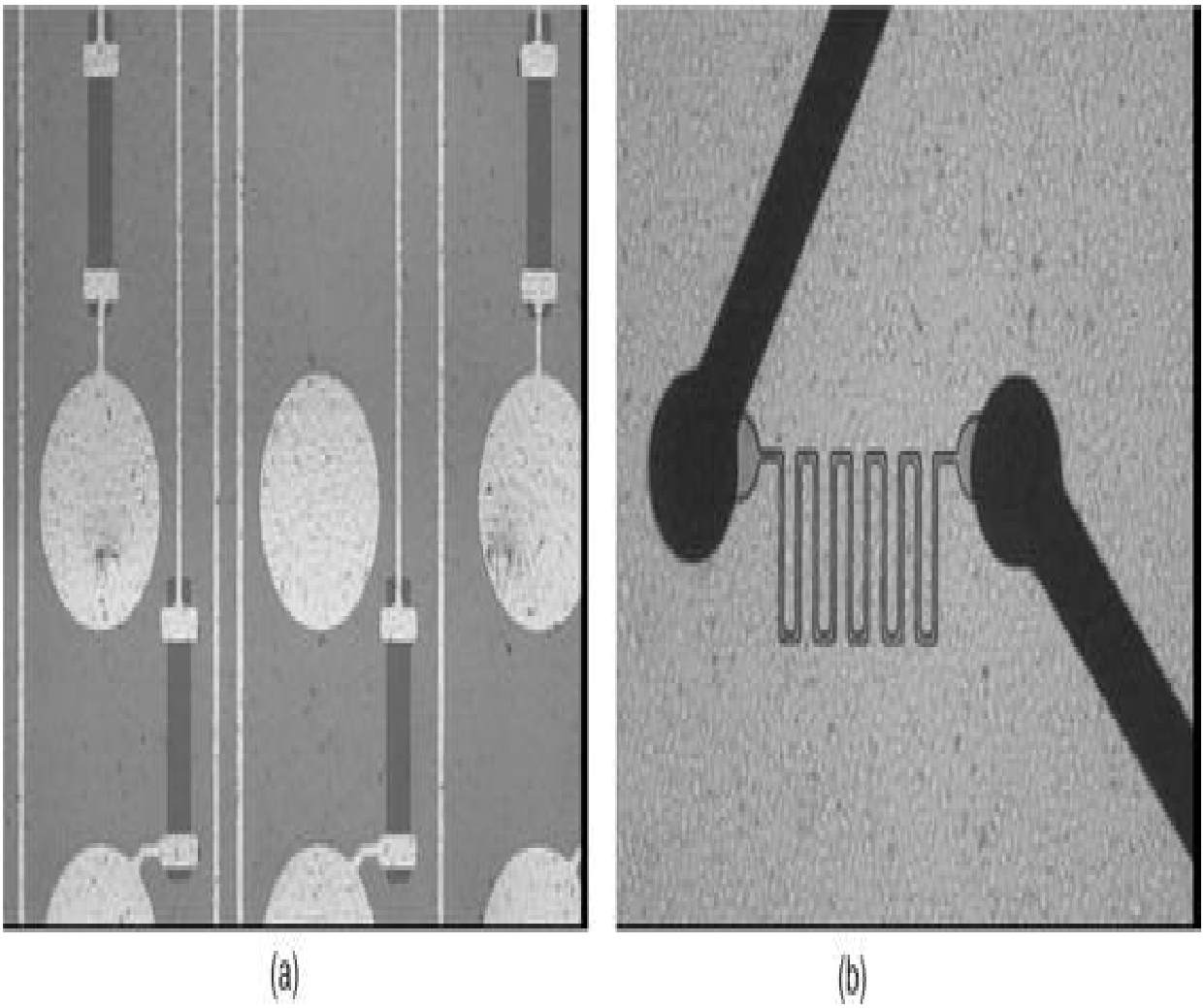


FIGURE 70.15 Examples of functional flexible circuits: (*a*) embedded resistance, (*b*) small strain gage built on flexible substrate. (*Source: MicroConnex*)

CHAPTER 71

FLEXIBLE CIRCUIT QUALITY ASSURANCE: PRINCIPLES AND PRACTICES

Joseph Fjelstad
Verdant Electronics, Seattle, Washington

71.1 INTRODUCTION

There is an old adage which goes: “Individuals tend to do what is inspected rather than what is expected” is a bit cynical but it is also not entirely without merit. It is not than individuals seek to create manufacturing errors but rather that without knowledge of what is being inspected for they have no way of knowing what is expected as a result of their efforts. As a result testing and inspection are among the most important elements of any manufacturing operation. This is because these important operations at once:

- Provide valuable feedback on the health of the manufacturing operation

- Can prevent the escape of defective parts into the assembly process
- Can prevent failure in assembly
- Can prevent failure in the end-use environment

Quality and reliability managers often have a conflicted relationship with manufacturing. As the source of in house “reality checks,” quality and reliability managers are tasked with finding and either repairing or scrapping discrepant circuits. Quality and reliability managers serve as customer advocates in that they seek to prevent discrepant material from shipping to the customer. To many manufacturing people, inspection and testing does not seem to add value to the product. But inspection and testing do add value by helping to ensure customer satisfaction and secure repeat business. On-time delivery helps to meet short-term goals and immediate customer needs, while quality and reliability help to achieve longer-term goals, such as preventing returns and assuring the return of loyal customers.

Today’s methods of just-in-time procurement and assembly make the issue of discrepant material being delivered to the customer particularly damaging. Circuits that do not meet contractual agreements or functional requirements add cost by requiring that circuits and assembled components be remade or replaced. Discrepant product increases cost, monetarily and in terms of capacity reduction that results in a ripple effect upstream that can reach the original equipment manufacturer (OEM). Liability of the fabricator is often extended to include replacement of discrepant circuits as well as assembled parts that cannot be salvaged by the assembler.

Moreover with the mandated implementation of lead-free assembly there has been a significant impact on quality and reliability requirements of flex circuits, raising the bar from former times. What was once an acceptable quality level in a tin-lead assembly may fail catastrophically in a lead-free

assembly and/or rework situation. Whereas tin-lead assembly could be performed at a process temperature of 230°C, lead-free assembly requires temperatures as high as 260°C. As a result new failure modes have been identified (e.g., microvia pullout) and attributed to the high temperatures associated with lead free assembly. Aerospace satellites that fail prematurely in orbit, equipment that fails in the pitch or battle and failure of life support systems are obvious examples of why inspection and test are so important to the electronics industry. Contrary to popular belief, quality and reliability requirements for consumer electronics are increasing and becoming tighter. The requirement for consistent, repeatable quality with appropriate reliability is being mandated, but of course the goal is to achieve this level of quality without incurring additional costs. Pricing was once the major consideration for procurement, but cost is becoming the more dominant factor. Quality and reliability are more important than ever to prevent significant costs to the fabricator, contract manufacturer, OEM, and customer. Quality and reliability, while often referred to interchangeably, actually have different purposes. Quality is mostly about adhering to specified requirements to meet contractual obligations or industry-established minimums. Quality is concerned with the correct part number, revision, amount, dimension requirements, physical and electrical attributes, and requirements including opens, shorts, copper weights and thicknesses, impedance and other variables. Reliability is a measurement of the sum total of the quality requirements and other unspecified attributes of the circuit. Quality confirms that a circuit meets requirements, while reliability demonstrates that the effects of those requirements produce a product that will survive assembly and be functional in the end-use environment.

71.2 BASIC CONCEPTS IN FLEXIBLE CIRCUIT QUALITY ASSURANCE

Because of the different design concepts and materials, there are several significant differences in managing quality assurance for flex circuits versus that for typical rigid circuit boards. In addition, special test methods are required to guarantee the finished quality of high-density flex circuits, and new inspection technologies have been developed for this purpose.

The basic concept of quality assurance for flexible circuits is the same as that for rigid boards, in the sense that any critical defect must be identified and prevented from shipping. The list of identified types of failures is long and varied as will be shown in this chapter. There are concerns not only with circuit continuity but with the viability of the terminations that will be made on the circuits during the assembly process. In concise terms it is a goal of quality assurance to confirm or refute that the circuit meets or exceeds quality requirements and reliability expectations contractually expressed by the customer. In general it is on the manufacturing floor where quality assurance plays its two most important roles, manufacturing floor health monitoring and final evaluation using its two most important tools, inspection, and test. In short, quality control performs test and inspection with the goal of assuring that the process is working properly and furthermore to make sure that the products built meet the requirements and reliability expectations of the customer. This is not an easy task but it is an important one.

The list of variables that must be monitored in process and adjusted as required to ensure consistent outcomes during circuit fabrication is daunting. Variables in the process are monitored and adjusted to ensure consistent outcomes during circuit fabrication. For example there is need to

monitor, test and track such process variables as temperature, pressure, chemical concentrations, pH, and the like. The results are commonly analyzed using statistical methods and tightly controlled to ensure that the process is continuing to produce an acceptable product. Moreover, the materials used in manufacture are necessarily tested with some frequency to ensure that they have not fallen out of conformance with requirements. Quality assurance provides a feedback loop of measurement and adjustment helps to achieve consistency of process and product. Sample circuits, or representative coupons, are submitted to a testing program. It is important that the sample has the same construction and conformation as the circuit being tested. Samples of circuits from a given fabrication lot, taken off the production panel, should be nearly identical and testing of the sample should reflect the attributes of all the associated circuits.

Testing should not be confused with inspection, although they do have complimentary roles. Inspection finds variation that results in the need to sort to separate acceptable from discrepant circuits. Weeding out and rejecting discrepant production circuits reduces production yield, but knowing the production yield is one of the most useful tools for obtaining objective feedback about the general health of the fabrication line and the product being built. Inspection must also be used to assess the quality of the product and ensure that it conforms to established requirements. With increasingly fine line circuits challenging human capabilities the use of automated optical inspection (AOI) is becoming increasingly important. Used properly it can both provide a feedback to manufacturing relative to potential discrepancies in phototools used in the imaging process and can as well provide early feedback to manufacturing whether there will be need to restart a production run to meet manufacturing deadlines.

100 percent testing of any product, including flexible circuits, though possible, is not normally practical therefore testing is commonly done on a sample basis to maintain some manufacturing economy. Moreover, some types of testing actually degrade the quality of the circuit in the process of testing. Still under some circumstances, 100 percent testing may be required.

As alluded to earlier there are fundamentally two levels of interest for inspection and test: the raw material level and the finished circuit level. Raw materials are inspected and tested to ensure that they will meet the requirements established by industry. Raw material testing provides a level of assurance that only acceptable material will be committed to manufacturing, reducing the potential for circuit discrepancies. The final product is also tested to make certain that it meets or exceeds the specified requirements, which are typically related to form, fit, function, and performance in the endues environment. The balance of this chapter will identify and briefly discuss the types of inspection and test that are required for both material and final product.

71.3 RAW MATERIAL TESTING

Raw materials (e.g., base materials, adhesives, foil-clad laminates) are tested to ensure that they are of a high enough quality to produce end-products that are compliant with requirements and will not limit the circuit’s performance as it moves through assembly and to the end-use environment. Material performance is evaluated in several categories (physical, chemical, electrical, and environmental) that reasonably represent the spectrum of potential areas of concern for a product. The following is a review of some of the tests that may be required for flexible raw materials.

71.3.1 Material Physical Performance Testing

The physical performance of the raw material is measured to ascertain that certain minimum physical properties are present in the material and to ensure that it is compliant with the specified requirements. The following common mechanical tests are performed to determine the values of two key physical properties of the flexible base material: the ultimate strength of the base film and the degree to which the material can be stretched before failure. These are important mechanical considerations and are useful in predicting the suitability of a material for a given application. They are also important data input values used in finite element modeling (FEM) and/or finite element analysis (FEA).

- *Initiation tear strength:* A test used to determine how much force is required to initiate tearing in a material. It is a measure of the toughness of the base material, an important factor for flex circuits given the somewhat delicate nature of thin materials.
- *Propagation tear strength:* Evaluated to determine the toughness of the material. This test is designed to measure the force required to propagate a tear in a material after a tear has been initiated. Propagation tear strength can be a vital determinant of the ultimate reliability of a product. The lower this value is, the more important it is that tear-stop features be added to the flex circuit design.
- *Low-temperature flexibility:* Performed to evaluate material resistance to embrittlement and possible fracture at low-temperature conditions, as might be encountered by flex circuit end-products in some applications.
- *Dimensional stability:* Measuring and characterizing a base material’s dimensional stability is important to both the designer and the manufacturer. Any variability in the

materials dimensional response to the manufacturing process is vital to product yield. One of the concerns is the propensity of a material to shrink during the etching process as the elimination of copper removes the truly dimensionally stable element of the laminate. In general, the more dimensionally stable the material, the easier it is to predict the locations of design features after manufacture.

- *Peel strength:* Measured to ensure minimum bond strength. It is normally applied to the measure of copper foil, but it can be applied to other combinations as well. Tests are run under the following conditions to ensure that adequate peel strength is retained after exposure to different conditions.
  - As received to check for minimum bond strength of copper to the flexible dielectric base
  - After floating the sample on 289°C solder for 10 s to check for degradation after simulated assembly and rework.
  - After exposure to five cycles of −50°C, +150°C with 30-min dwells at each extreme, with a 15-min intermediate dwell at room temperature between exposures at extremes to simulate accelerated aging effect on bond strength.
- *Volatile content:* A potential source of outgassing and delamination. The test is employed to determine that the weight percentage of volatile elements in flexible laminate is at a desirably low value.

71.4 ELECTRICAL PERFORMANCE TESTS

The electrical performance of a flex circuit is often critical to the performance of the final product and the electrical performance is often a function of the material itself and its electrical properties. This is increasingly the case as higher performance circuits find their way into ever increasing numbers of applications. The electrical properties are verified by checking material samples and determining values for all of the following attributes.

- *Dielectric constant:* A unitless value, the dielectric constant (D_k) of a material is an important factor and determinant in many predictive calculations of electronic performance. A low D_k is especially important in high-speed applications. It is fundamentally the ratio of the capacitance of the material to the capacitance of air.
- *Dissipation factor:* Fundamentally defined by the relationship between the material's permittivity (capacitance) and its conductivity, when measured at a given frequency. This is an important material property which assist the circuit designer in making calculations of the electronic performance of the end-product. Moisture uptake is a common contributor to increases in dissipation factor and signal loss and will become increasingly important as signal speeds and operating frequencies continue to rise.
- *Dielectric strength:* Is determined to establish the minimum breakdown voltage of the material. It is of particular interest and importance in the fabrication of high-voltage circuits as well as circuits that are to operate at high altitudes and are prone to electrical arcing.
- *Surface and volume resistivity:* Values are measured and established to ensure the material conforms to minimum values for volume and surface electrical resistance under damp heat conditions (such as those that might be encountered during exposure to highly humid

environments), if the resistivity is too low it can negatively alter electronic circuit performance. The test provides a measure of a material's propensity for current leakage under such conditions.

71.4.1 Environmental Performance Testing

Environmental performance testing is undertaken to evaluate certain physical and electrical attributes of the material that may change as a result of exposure to the environment over product life.

- *Moisture absorption:* A determination of how much moisture the base material will absorb under humid conditions. Moisture absorption is relevant to electrical considerations since moisture absorption will alter the dielectric constant of the material. However, it is also a potential concern in assembly since excessive moisture absorption can cause explosive outgassing of absorbed moisture and delamination of cover layers. This is an increasingly important concern with lead-free solder since there is a doubling of vapor pressure between traditional soldering temperatures and nominal temperatures required for lead-free soldering.
- *Moisture and insulation resistance:* Evaluated to determine the effects of extended exposure to moisture on the insulation resistance of the raw material. The purpose is to verify that electrical properties do not degrade beyond established limits for the material under test conditions.
- *Fungus resistance evaluation:* Performed to determine if the material is a nutrient for fungi or other biological material that might be capable of degrading the electrical properties of the flex circuit.

71.5 GENERAL TESTING REQUIREMENTS FOR FLEXIBLE CIRCUIT MATERIALS

There are a range of material tests that are desirably performed on flexible circuit base materials to ensure conformance to requirements. Following are the two primary areas of concern:

- *Chemical performance testing:* Such requirements for flexible circuits are very limited. Processing and application are two major areas of concern relative to chemical performance of raw materials used in flex circuit manufacture. Flexible circuits can be exposed to a variety of chemicals both in process and in use does it is important to determine resistance of the material to any such chemistries that may encounter to assure there are no deleterious or lingering negative effects
- *Flammability testing:* Performed to determine the minimum level of oxygen required to sustain combustion of the laminate. For printed circuitry, a commonly required rating is Underwriters Laboratories' UL 94 V-0, which indicates that the material is nonflammable. While, in the past, UL 94 V-0 ratings for flex laminates were uncommon, advances in flex circuit materials have resulted in a number of materials that meet the requirements of a 94 V-0 rating.

71.6 FLEXIBLE CIRCUIT VISUAL EVALUATION

The final test and inspection of flexible circuits is performed to ensure the products conformance to requirements. The reader will note that the testing of finished flex circuits duplicates many of the tests performed on the raw material. This is to ensure that the manufacturing process has not degraded the material beyond acceptable limits with respect to certain key properties. As with the raw materials, testing requirements have been established in several key areas to ascertain that the product is acceptable for its intended purpose.

Major categories for testing the finished flex circuit include: visual inspection, metal finish solderability, physical dimensions, physical properties, circuit construction integrity, plated-through-hole quality (both before and after thermal stress), electrical properties, environmental properties and cleanliness. Testing requirements for each of the above-mentioned categories are reviewed here in brief fashion. IPC documents describing the precise test methods are available and should be read if more detail is sought or if one wishes to perform the actual testing.

- *Visual inspection requirements:* Visual inspections are commonly performed as part of quality assurance process to ensure conformance to requirements not readily captured by other test techniques. The following are key attributes that are determined visually.
- *Delamination:* Fundamentally any separation of the material from itself (e.g., conductors from laminate, cover films from conductors) constitutes evidence of delamination. It is generally seen as an indicator of improper processing, lack of cleanliness or thermal stress excesses. In nearly all cases, delamination is considered a rejectable condition.
- *Circuit edge condition:* The edges of flex circuits are commonly seen as a site of potential failure thus edge condition is inspected to check for nicks or tears that could

be sites for tear propagation and failure of the circuit. This is of great importance in dynamic flex circuit applications where nicks along the edges of a flex circuit can become sites for tear initiation. Edge condition testing is important for static applications as well, since circuits could be inadvertently stressed and torn during assembly.

- *Stiffener attachment Quality:* Stiffeners normally perform vital mechanical component support functions. As a result, the attachment is checked to ensure integrity of the bond on the flex circuit to the chosen stiffener substrate. If filleting of stiffener edges or an edge break is specified, this inspection step will also verify its presence.
- *Solder wicking under coverlayer:* Evidence of solder wicking along the surfaces of traces away from openings in the coverlayer may be an indication of improper lamination of the coverlayer or excessive exposure to molten solder. The condition is desirable but is generally considered to be acceptable if it is within specified or agreed upon limits.
- *Marking of the circuit:* Marking is checked to verify compliance to the master drawing and to prevent mislocation or misorientation of components during assembly or later, when field repair of the circuit would be required. If serialization of the circuit is used, it can also be checked at this time.
- *Plated-through-hole quality:* As with all printed circuits the quality of plated-through holes is vitally important with flexible circuits as well. Voids of unacceptable size or quantity are inspected in order to avoid soldering or reliability problems with the copper-plated-through hole. Ring voids are a major concern and a definite cause for rejection. If not discovered in inspection during assembly, the problem of voiding in plated-through holes is frequently manifested as an outgassing condition or blow hole in the solder joint.

- *Workmanship:* A catch-all inspection category covers miscellaneous items such as the presence or absence of dirt, oils, fingerprints, wrinkles, bends or creases, and other nonspecific indicators of the workmanship of the circuit's manufacturer. Workmanship inspection may be subjective, but it can provide an indication of the quality of the circuit manufacturer's process.

71.7 FLEXIBLE CIRCUIT DIMENSIONAL REQUIREMENTS

Dimensional measurements of the finished flex circuit are taken to ensure the form and fit of the accuracy is often important to the actual function and ultimate reliability of the circuit. The following are some key points of inspection and measurement:

- *Minimum annular ring determination:* The lack of sufficient annular ring can affect both the solderability and the reliability of an interconnect. Requirements differ greatly for plated and nonplated-through holes. Nonplated-through holes in single-sided flex normally requiring a much greater solderable area to ensure a reliable joint. Thus, annular ring is checked to ensure that minimum requirements are met.
- *Hole pattern accuracy:* Checked to ensure that through holes are in their proper locations. This is an important issue for circuit assembly, especially when automated plated-through-hole assembly procedures are employed. It is also important when the holes are to be used as tooling holes for surface mount assembly.
- *Coverlayer registration:* Has a net effect similar to that of the annular ring because coverlayer misregistration can encroach on the solderable area, resulting in a less reliable

connection. The coverlayer should register on the pad to meet the minimum specified requirements. Registration requirements can vary with pad design features, with some approaches being more forgiving. With single-sided flex circuit designs, where the coverlayer serves to prevent pad lift, registration can be a very important concern. A minimum of 270 percent of land capture is normally recommended.

- *Adhesive squeezeout onto pads:* A fairly common by-product of manufacturing during coverlayer lamination due to adhesive flow under heat and pressure. There are standard allowances for squeeze-out onto lands, but the amount of squeeze-out may need to be negotiated. Good process technique and materials can minimize the effects by damming off the adhesive with conforming press-pad materials. With newer photoimageable coverlayers, this factor is generally not a concern.
- *Air entrapment along the edges of flex circuit traces:* Phenomenon commonly referred to as soda-strawing, it can occur in dense, closely packed circuit designs or when very thick copper is called out by design. While it is not harmful in all applications, acceptability is often based on application of the end product. Capillary wicking of moisture is possible if the effect runs to the edge of the circuit or land. Limits should be agreed upon between the user and manufacturer.
- *Foreign entrapments:* Foreign materials are sometimes present in the raw material and/or under the coverlayer of flex circuits. They are considered acceptable in various applications, provided that they do not bridge conductors or reduce spacing between conductors to less than acceptable limits. They may also be a concern if located in a critical bend area.
- *Hole sizes in flex circuit:* All such features are checked to verify conformance to print requirements and to preempt

assembly problems. If made too small, circuit holes may make insertion of component leads difficult. If the hole is too large, it may be difficult to form solder joints of preferred quality in the assembly process. For tooling holes, hole size inaccuracy is a concern because loss of positional accuracy is a possibility.

- *Circuit conductor pattern:* Obviously the finished conductor pattern on the flex circuit should accurately represent the master drawing. While allowances exist for localized reductions of up to 20 percent in conductor trace width due to nicks or mouse bites, an excessively large number of occurrences is likely to be indicative of problems in the manufacturing process.
- *Conductor width and spacing:* Evaluated because it is increasingly critical especially as line and space on circuits diminish in size. Proper sizing may be critical to ensure proper electrical and/or electronic performance. Evaluation requirements should be defined on and controlled by the master drawing.

71.8 PHYSICAL TESTING REQUIREMENTS FOR FLEXIBLE CIRCUITS

Physical testing is another key part of flex circuit testing. It helps to verify the physical appropriateness of the product for the application. The following tests are performed to ensure product quality and reliability. The flex testing sections are especially important in dynamic flex circuit applications.

- *Plating adhesion:* Tests performed to ensure a good metallurgical bond of plated metals to the base laminate copper foil. One method that has been employed for many

years is the use of home and office tape which has been bonded to the circuits and then rapidly foldaway. The test is commonly referred to in the industry as the tape test. Low bond strength could result in latent failure of the circuit due to conductor lift or shorting.

- *Unsupported hole bond strength:* Evaluated to ensure that the circuit can endure assembly and repair without excessive damage. The land must endure five cycles of soldering and desoldering in accordance with common specifications.
- *Conductor pattern bond strength:* This test which is similar to the plating adhesion test is performed to ensure that the circuit manufacturing process has not reduced foil bond strength to unacceptable levels. Test conditions are essentially identical to those described for raw materials.

71.8.1 Flexibility Testing Requirements for Flexible Circuits

Flexibility is a hallmark feature of flexible circuits and thus evaluating the flexibility of the circuit as a finished product is of significant importance. There are two general types of tests performed one is a folding flexibility test and the other is a flexibility and endurance test.

- *Folding flexibility tests:* Performed to ensure that the circuit can be successfully formed to meet the requirements of the master drawing without delaminating or breaking conductors. Information required for proper testing of folding flexibility includes: location of bend, radius of bend, angle of bend, direction of bend, and number of cycles.
- *Flexibility endurance testing:* Most important for dynamic flex applications it provides important information about

both the circuit and the process. Testing apparatus can vary with customer requirements. Standard test methods using equipment such as the fatigue ductility (a.k.a. Engelmaier) flex tester may require anywhere from a few minutes to several hours to perform. Many disk drive manufacturers opt to test circuits under simulated operating conditions. Flexibility endurance testing can take weeks or even months to complete, but can provide manufacturers with the comfort of hard statistical reliability data. Examples of some of the most commonly used flexibility endurance test concepts are provided in Fig. 71.1.

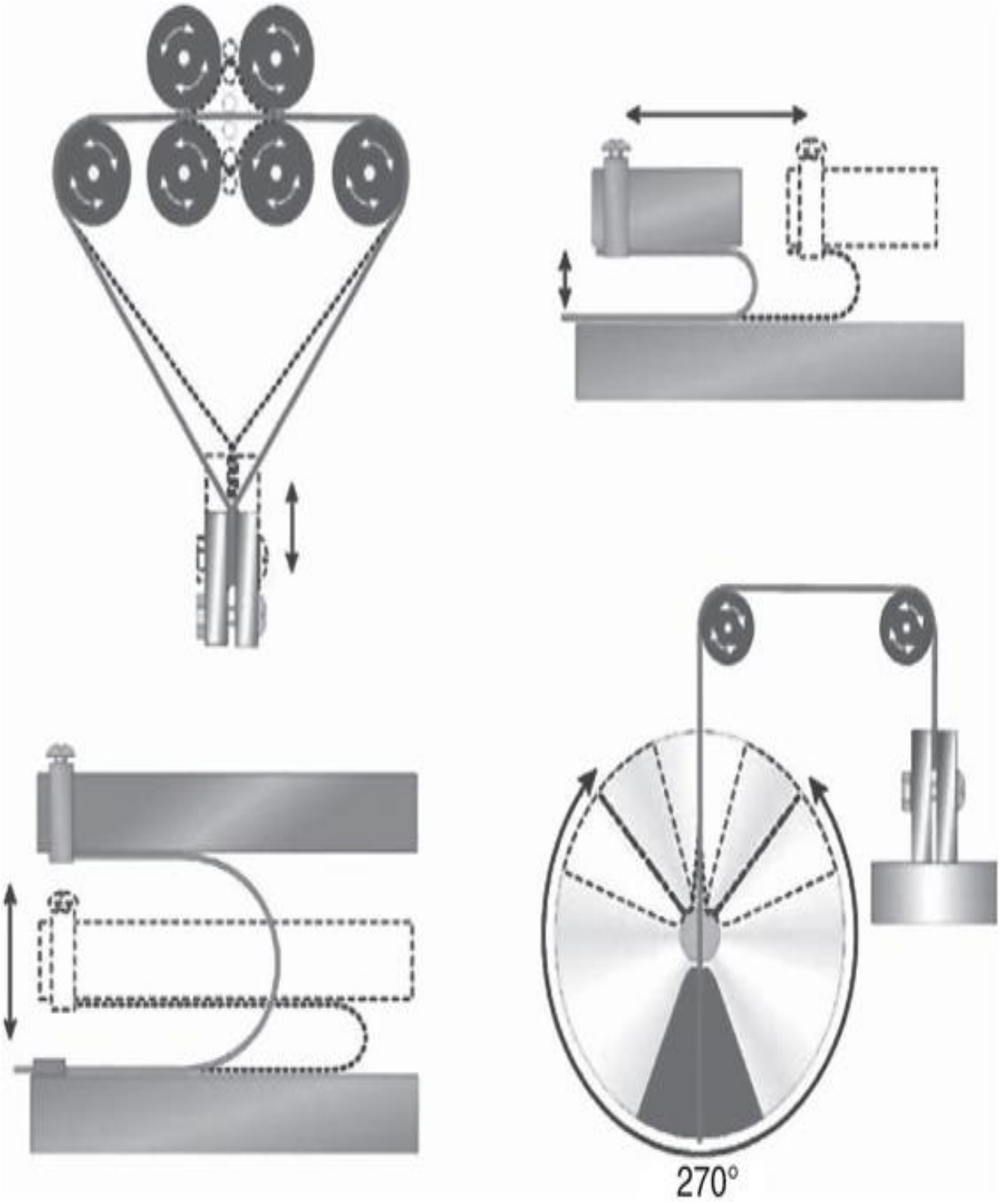


FIGURE 71.1 Examples of testing methods used to elvauate flexual endurance of flexible circuits. Clockwise from upper left: the Engelmaier fatigue ductility flex tester, rolling flex test (Rogers), MIT flex test, and collapsing radius (IBM/Xytratex).

71.8.2 Flexible Circuit Construction Integrity Requirements

The construction integrity of a flex circuit is best evaluated by performing a microscopic evaluation of a cross-section of the product before and after thermal stress testing. This type of inspection is used to reveal the presence of microscopic defects that may impact the reliability of the finished flex circuit. Inspections are performed both as received (prestressed) and after various thermal stress tests have been performed (postthermal stress). The tests are performed to ensure that product quality and reliability are not degraded by the thermal exposure endured during solder assembly and solder rework operations.

71.8.3 Prestress Evaluation Requirements for Flexible Circuits

The following points are evaluated before exposure to solder stress, to screen the product for the presence of defects in the product as received. Major faults detected here may preempt the need for further testing:

- *Lands or pads:* Checked to ensure that they have good adhesion to the substrate before stress testing. Land lifting is usually the result of thermal stress, where expansion of the heated laminate can cause lands to lose adhesion and lift from the surface of the circuit.
- *Plating integrity evaluation:* Checked to ensure that plating quality, uniformity, and thickness all meet specification requirements and that no cracks are present in the through-hole in order to ensure through-hole plating reliability.

- *Layer to layer registration evaluation:* Checked to ensure that minimum requirements for the given class of product are met. This is primarily a concern for multilayer and rigid flex constructions, but it can be a concern with double-sided flex as well.

71.8.4 Poststress Evaluation Requirements for Flexible Circuits

The following checks are performed after required thermal tests. Microscopic evaluation of plated-through-hole cross-sections after thermal stress testing is the approved method for determining ultimate plated-through-hole quality.

- *Thermal stress testing:* A particularly aggressive test developed to assess the effects of assembly simulation, thermal stress testing is a benchmark test within the industry when determining plated-through-hole quality. Historically the test involves placing a flux coated circuit coupon on a bath of molten solder held at a temperature of 289°C (550°F). It is a much more punishing test than typical assembly that is used to weed out marginal quality product. Other tests may be used including ones which simulate the actual manufacturing process such as passing the assembly through a conveyorized oven to simulate assembly conditions or the so-called interconnect stress test (IST), which involves passing a current through a daisy chain of plated-through holes, the current being sufficiently high to achieve temperatures proximate to those seen in a solder flow test.
- *Rework simulation testing:* Another challenging test of plated-through-hole reliability involves the soldering and desoldering of a component lead five times in the plated through-hole. The test was designed and is performed to simulate field repair and evaluate its effects on the flex

circuit’s plated-through-hole integrity. The test must be performed by a skilled operator because an uncontrolled soldering iron could cause significant damage.

- *Lifted lands:* The presence of lifted lands after eight thermal stress test is evaluated to try and determine the circuit construction’s capability in the field. The phenomenon is more common where outer layer circuits are built on materials having a high coefficient of thermal expansion which caused the pads to lift and rotate. Excessive incidents of lifted lands may require a redesign with new materials.

71.9 ELECTRICAL REQUIREMENTS FOR FLEXIBLE CIRCUITS

Finished flexible circuits are required to meet certain electrical requirements to ensure their performance in the field. The specific electrical requirements for the flex circuit are identified and specified to ensure proper electrical performance of the finished product. While the tests outlined below are ones most often called out for circuit acceptance, other tests such as time domain reflectometry (TDR) testing of controlled-impedance circuits may also be required under contract provisions.

- *Circuit continuity and shorting:* Flexible circuits should be electrically tested to make certain that no opens or shorts are present in the board. This testing will ensure conformance to design, and proper circuit performance in the field. Test conditions such as test voltage and minimum resistance between conductors should be called out on the master drawing. There are a range of different tools available for performing this type of testing which include both fixtured tooling systems as well as flying

probe heads. The choice of method is typically a function of volume and complexity.

- *Insulation resistance testing of flexible circuits:* A test which duplicates the raw material test and verifies that circuit manufacture processing has not degraded the insulation resistance of the material beyond customer-specified requirements.
- *Conductive anodic filament evaluation:* Conductive anodic filaments (CAF) are seen as fine conductive paths that form between two adjacent interconnects (e.g., PTH to ground plane). These filaments tend to develop over time in the end-use environment. The filaments have some common attributes. The growth is found between two conductive features that exhibit an electrical bias. It requires a source of moisture and a source of ionic contamination. The fiber grows down a path between the glass fiber and the epoxy matrix. This is obviously of greater concern with rigid flex where glass-reinforced epoxy laminates are made into hybrid structures with homogeneous flex circuit materials which are immune. The concern is that occasionally a conductive pathway is formed down cracks caused by delamination or cohesive failure. The filament growth is from the anodic circuit to the adjacent cathode. Frequently, the fiber shorts to the adjacent structure (e.g., through-hole) and, in the process of shorting, are destroyed by the electric potential, only to then grow again. This may produce an intermittent electrical short that is vexingly difficult to find. CAF testing has been limited to testing a specific coupon in an isotherm with constant humidity. No thermal cycling is employed during the test. The circuits are tested in a humidity chamber typically set to 65°C with 85°C relative humidity.

71.10 ENVIRONMENTAL RESISTANCE REQUIREMENTS

Flexible circuits are used in an ever broadening array of applications so understanding their performance under different environmental conditions is important. Thus certain environmental tests are performed to simulate, in a practical fashion, the effects of various environmental conditions on flex circuit quality, performance and reliability.

- *Moisture an insulation resistance testing:* In the performance of this test, circuits are cyclically exposed to hot, moist air (from 80 percent relative humidity at 25°C to 98 percent relative humidity at 65°C). This is to ensure that no damaging effects occur in the laminate and that undesirable degradation of the insulation resistance of the flex circuit has not occurred. Some variations to the test exist.
- *Thermal shock and thermal cycling:* A number of different types of tests and test conditions have been developed over the years all of which have some measure of acceptance under the broader heading of thermal shock and thermal cycle testing. Most tests consist of exposing the device to temperature extremes to induce thermal-cycle strain-related failures. Thermal cycling is meant to be representative of the temperature extremes a circuit might be exposed to during its lifetime. Cycling conditions range from −65°C to +150°C, with prescribed dwells at anywhere from 10 min to 1 h. Shock testing normally employs short dwell times. The most common temperature conditions for bare-board testing range from −55°C to +125°C. However, with the introduction of product-specific reliability testing by some manufacturers, several new thermal-cycling tests are becoming more common.

- *Cleanliness testing of flexible circuits:* Finished flex circuits must be tested to ensure that the circuits do not carry an excessive amount of ionic or organic contaminants with them. Surface contaminants both ionic and organic have been shown to have a negative effect on long-term reliability.
- *Ionic contamination testing:* It is commonly performed to determine the level of ionic material left on the board. Method most commonly employed is one called solvent extract resistivity testing. It is performed by washing the board using a pure alcohol/water solvent, collecting the solvent and measuring its change in resistance. Ionic contaminants, if left on the board, are capable of causing latent failures due to corrosion and current leakage or shorting.
- *Organic contaminant testing:* Organic contaminants are another potential source of problems that should not remain on the circuit. The contamination can be detected by flushing the surface of a small sample of the circuit with chemically pure acetonitrile onto a clean glass surface and allowing the solvent to evaporate. Residue on the slide may indicate the presence of organic contaminants.

71.11 SOLDERABILITY REQUIREMENTS

A subject unto itself measure of solderability of all circuit substrates is considered vital. Tests for solderability of the finished circuit are performed to ascertain that the flexible circuit will not experience or create problems in assembly operations due to a nonwetting condition. This is normally accomplished by checking that proper wetting of solderable surfaces is present after testing in accordance with an approved test method. EIA/IPC-J-Standard-001 is the

reference standard for all electronic applications across the industry and around the globe. A more detailed discussion of this topic can be found elsewhere in this book.

71.12 STANDARDS AND SPECIFICATIONS FOR FLEXIBLE CIRCUITS

There are a wide array of different standards from different parts of the world which have been promulgated to serve the needs of flexible circuits. Most of the major standards associations have generated new standards or upgraded existing ones for flexible circuits. Following is a listing of some of the most prominent flexible circuit standards developers and custodians.

ANSI (American National Standards Institute)

ANSI-Y-145: Dimensioning and Tolerancing

IEC (**International Electrotechnical Commission)**

IEC 249-2-15: Flexible copper-clad polyimide film of defined flammability grade

IEC 326-7: Specification for single- and double-sided flexible printed boards without through-hole connections

IEC 326-8: Specification for single- and double-sided flexible printed boards with through-hole connections

IEC 326-9: Specification for multilayer flexible printed boards with through-hole connections

IEC 326-10: Specification for flex/rigid double-sided printed boards with through-hole connections

IEC 326-11: Specification for flex/rigid multilayer printed boards with through-hole connections

IPC (Association Connecting Electronics Industries)

2221B: Generic Standard on Printed Board Design

2223C: Sectional Design Standard for Flexible Printed Boards (Formerly IPC-D-249)

2611: Generic Requirements for Electronic Product Documentation

2614: Sectional Requirements for Board Fabrication Documentation

4202A: Flexible Base Dielectrics for Use in Flexible Printed Circuitry (Formerly IPC-FC-231)

4203A: Cover and Bonding Material for Flexible Printed Circuitry (Formerly IPC-FC-232)

4204A: Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry (Formerly IPC-FC-241

4412B: Specification for Finished Fabric Woven from “E” Glass for Printed Boards

4562A: Metal Foil for Printed Board Applications (Formerly IPC-MF-150)

6011: Generic Performance Specification for Printed Boards

6013C: Qualification and Performance Specification for Flexible Printed Boards

9252A: Requirements for Electrical Testing of Unpopulated Printed Boards

A-600H: Acceptability of Printed Boards

DR-572A: Drilling Guidelines for Printed Boards

FC-234A: Pressure Sensitive Adhesive (PSA) Assembly Guidelines for Flexible, Rigid or Rigid-Flex Printed Boards

J-STD-001 Requirements for Soldered Electrical and Electronics Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

J-STD-004 Requirements for Soldering Fluxes

J-STD-005 General Requirements and Test Methods for Electronic Grade Solder Paste

J-STD-006 General Requirements and Test Methods for Soft Solder Alloys and Fluxed and Non-Fluxed Solid Solder for Electronic Soldering Applications.

JIS (Japanese Industrial Standards)

JIS-C 5016: Test methods for flexible printed wiring boards

JIS-C 5017: Flexible printed wiring boards, single-sided and double-sided

JIS-C 6471: Test methods for copper-clad laminates of flexible printed wiring boards

JIS-C 6472: Copper-clad laminates for flexible printed wiring boards (polyester film, polyimide film)

JPCA (Japanese Printed Circuit Association)

JPCA-BM 01: Copper-clad laminates of flexible printed circuits, polyester films, and polyimide films

JPCA-FC 01: Single-sided flexible printed circuits

JPCA-FC 02: Double-sided flexible printed circuits

JPCA-FC 03: Visual defect criteria for flexible printed circuits

MIL (US Military Standard)

MIL-STD-2118: Flexible and rigid-flex printed-wiring for electronic equipment

MIL-C-28809: Circuit card assemblies, rigid, flexible and rigid-flex

MIL-P-50884C: Printed wiring, flexible, and rigid-flex

MIL-STD-105 Sampling Procedures and Inspection Tables

MIL-STD-129 Marking for Shipment and Storage

MIL-STD-130 Identification for Marking

MIL-STD-202 Test Methods for Electronic Equipment

MIL-STD-2000 Soldering and Assembly

MIL-STD-45662 Calibration System Requirements

DOD-D-1000 Engineering Drawings

DOD-STD-100 Engineering Drawing Practices

MIL-S-13949 Plastic Sheet, Laminate, Metal Clad (for PWBs)

MIL-C-14550 Copper Plating (Electrodeposited)

MIL-I-43553 Ink Marking, Epoxy Base

MIL-G-45204 Gold Plating (Electrodeposited)

MIL-I-45208 Inspection System Requirements

MIL-Q-9858 Quality Program Requirements

MIL-P-81728 Plating Tin Lead (Electrodeposited)

MIL-P-55110 Printed Wiring Boards

QQ-N-290 Nickel Plating (Electrodeposited)

UL (Underwriters Laboratories)

UL796F: Flexible materials interconnect constructions

71.13 SUMMARY

There are many tests and inspection steps employed to ensure the reliability of flexible and rigid flex circuits. It is important to note that not all tests are required for every lot. Testing is typically split into two levels: tests required for qualification and tests required for acceptance. Of these two, acceptance testing is more limited in scope, which helps to reduce some of the testing requirements. An effectively run

manufacturing operation is one that rigorously employs statistical process control (SPC) methods. The use of statistical process control, by a quality assurance department, can significantly reduce the need for formal inspection operations by keeping the processes under constant control. Using SPC, it is possible to achieve desired levels of performance and reliability at no extra cost, or even at a reduced cost. Employment of SPC methods is becoming a customer requirement for an increasing number of flex circuit users and is a key conceptual foundation for the ISO-9000 certification program, which is becoming a de facto standard for the world market.

71.14 ACKNOWLEDGMENTS

The author extends his appreciation to the industry and the many who contributed to the progress of flexible circuit activities. Sincere thanks also goes to Dominique K. Numakura, at DKN Research, for his authorship of this chapter in the previous (6th) edition of *Printed Circuits Handbook*.

APPENDIX

SUMMARY OF KEY COMPONENT, MATERIAL, PROCESS, AND DESIGN STANDARDS

Marc Carter

IPC—Association Connecting Electronics Industries, Bannockburn, Illinois

Appropriately selected, properly applied standards are the one of the keys to a globally successful electronics community. They serve as a common “language” between the various participants in the supply chain from early concept, through final delivery, and commercial and technical conflict resolution. By using mutually accepted preexisting standards, two parties to a contract need not recreate every technical definition or requirement for every transaction, greatly facilitating commerce.

The following documents emphasize surface-mount technology. These documents have been developed by standards organizations around the world. The letters in

each document designation indicate the organization that has responsibility for the document. Current details (abstracts, publication revisions, additional supporting documents, etc.) should be obtained at the organization's website/online store. As this is a "living" body of documents and organizations that support them, some documents may become unavailable after this list was compiled.

The reader may also note some apparent overlap where two organizations provide standards for the what appears to be the same entity or process. In some cases, that may reflect historical separation, or a simple failure to coordinate activities. In other cases, the two standards legitimately exist to address different needs, or different markets. It is important for the parties in a supply chain to reach agreement on what standards are most appropriate for their marketplace. In recent years, there has been some increase in communication and coordination between Standards Development Organizations (SDOs) to reduce wasteful overlap, though improvements are still needed.

DoD: Documents prepared by the Department of Defense.

ECA: Documents prepared by the Electronic Components, Assemblies, Equipment and Supplies Association (ECA) of the Electronic Industries Alliance (EIA). EIA ceased operations in 2011 but standard activities under the EIA Standards Council (ESC) continue under the auspices of the Electronic Components Industry Association (ECIA).

IEC: Documents prepared by the IEC—International Electrotechnical Commission.

IECQ: Documents prepared for Quality Assessment System for Electronic Components supported through the IEC.

IPC: Documents prepared by the IPC—Association Connecting Electronics Industries.

JEDEC: Documents of the Solid State Technology Association of the Electronic Industries Alliance (EIA).

JESD: Standards prepared by JEDEC.

JPCA: Standards prepared by JPCA.

J-STD: Joint industry standards (standards followed by more than one association).

MIL: Documents prepared by the military.

COMPONENTS—GENERAL

EIA-186-E: Standard Test Methods for Passive Electronic Component Parts—General Instructions and Index

EIA-481-2-A: Embossed Carrier Taping of Surface Mount Components for Automatic Handling (16, 24, 32, 44, and 56 mm)

EIA-944: Surface Mount Ferrite Chip Bead Qualification Specification

EIA-945: Surface Mount Inductor Qualification Specification

EIA/IS-47: Contact Termination Finish Standard for Surface Mount Devices

EIA/IS-760: Surface Mount Wirewound Inductor Qualification Specification

EIA-JEP-95: JEDEC Registered and Standard Outlines for Solid State and Related Products

EIA-JESD30B: Descriptive Designation System for Semiconductor Device Packages

EIA-PDP-100: Registered and Standard Mechanical Outlines for Electronic Parts

JESD-625A: Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

PASSIVE COMPONENTS

Capacitors

ECA SP 4984: Surface Mount Aluminum Electrolytic Chip Capacitor with Polymer Cathode

EIA-198-E: Ceramic Dielectric Capacitors Classes I, II, III, and IV

EIA-469-C: Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors

EIA-479A: Film-Paper, Film Dielectric Capacitors for 50/60 Hz Voltage Doubler Power Supplies

EIA-535: Series of Detail Specifications on Fixed Tantalum Capacitors

EIA-595: Visual and Mechanical Inspection Multilayer Ceramic Chip Capacitors

EIA/IS-35: Two-Pin Dual In-Line Capacitors

EIA/IS-36: Chip Capacitors, Multilayer (Ceramic Dielectric)

EIA/IS-37: Multiple Layer High Voltage Capacitors (Radial Lead Chip Capacitors)

EIA/IS-717: Surface Mount Tantalum Capacitor Qualification Specification

IEC-384-3: Sectional Specification, Tantalum Chip Capacitors

IEC-384-10: Sectional Specification, Fixed Multilayer Ceramic Chip Capacitors

IECQ Draft: Blank Detail Specification, Fixed Multilayer Ceramic Chip Capacitors

IECQ-PQC-31: Sectional Specification, Fixed Tantalum Chip Capacitors with Solid Electrolyte

IECQ-PQC-32: Blank Detail Specification, Fixed Tantalum Chip Capacitor

Resistors

ECA SP 5052: Resistors, Rectangular, Surface Mount, General Purpose

ECA SP 5053: Resistors, Rectangular, Surface Mount, Precision

EIA/ECA-575: Thick Film Resistor Specification

EIA/ECA-576: Resistors, Rectangular, Surface Mount Precision

EIA/IS-30: Resistors, Rectangular Surface Mount Thick Film

EIA/IS-34: Leaded Surface Mount Resistor Networks, Fixed Film

EIA/RS-344: Low Power, Insulated Fixed Wirewound Resistors

EIA/RS-345: Resistors, Variable, Wirewound (Lead-Screw Actuated)

EIA/RS-360: Resistors, Variable (Lead-Screw Actuated) Nonwirewound

EIA/RS-396: Resistors, Fixed Film Microelement

EIA/RS-451: Resistor Networks—Fixed Film

EIA/RS-452: Fixed Film Resistors—High Resistance/High Voltage

EIA/RS-460: Fixed Film Resistors—General Purpose

ACTIVE COMPONENTS

EIA-JEP-95: JEDEC Registered and Standard Outlines for Solid State and Related Products

EIA-JESD11: Chip Carrier Pinouts Standardized for CMOS 4000, HC, and HCT Series of Logic Circuits

EIA-JESD21-C: Configurations for Solid State Memories

EIA-JESD22-B: Test Methods and Procedures for Solid State Devices Used in Transportation/Automotive Applications (series format—consists of over 16 different test procedure documents)

EIA-JESD-26A: General Specification for Plastic Encapsulated Microcircuits for Use in Rugged Applications

EIA-JESD-30: Descriptive Designation System for Semiconductor Device Packages

EIA SP 4251 Detail Specification for Production Ball Grid Array (BGA), High Pin Count (1089 Pins and Greater) Socket for Use in Electronic Equipment

ELECTROMECHANICAL COMPONENTS

Connectors

EIA-364-C: Electrical Connector/Socket Test Procedures Including Environmental Classifications

EIA/IS-47: Contact Termination Finish Standard for Surface Mount Devices

IPC-CI-408: Design and Application Guidelines for the Use of Solderless Surface Mount Connectors

Sockets

EIA-5400000: Generic Specification for Sockets for Use in Electronic Equipment

EIA-540H000: Sectional Specification for Burn-In Sockets Used with Ball Grid Array Devices for Use in Electronic Equipment

Switches

EIA-448-23: Surface Mountable Switches, Qualification Test

EIA-520AAAD: Detail Specification for Single Pole, Single Throw, Surface Mount Pushbutton Switches

EIA-520DAAD: Detail Specification for Single Pole, Double Throw, Surface Mount Subminiature Size Toggle Switches

EIA-5200000-C: Generic Specification for Special-Use Electromechanical Switches of Certified Quality

EIA-SP-2186: Detail Specification for Single Pole, Double Throw, Surface Mount Subminiature Size Toggle Switches

EIA-SP-3162: Detail Specification for Single Pole, Single Throw, Surface Mount Pushbutton Switches

IECQ-PQC-41: Detail Specification, Dual-in-Line Switch, Surface Mountable, Slide Actuated US0003

Printed Boards

IPC-6011: General Performance Requirements for Printed Boards

IPC-6012: Performance Specification for Rigid Printed Boards

IPC-6013: Performance Specification for Flexible Printed Boards

IPC-6015: Performance Specification for Organic Multichip Module Structures (MCM-L)

IPC-6016: Qualification and Performance Specification for High-Density Interconnect (HDI) Layers or Boards

IPC-6017: Qualification and Performance Specification for Printed Boards Containing Embedded Passive Devices

IPC-6018: Microwave End Product Board Inspection and Test

JPCA DG-04: Flexible Printed Wiring Boards and Material for Flexible Printed Wiring Boards Integrated Standard

MIL-P-50884: Military Specification for Printed Wiring, Flexible, and Rigid Flex

MIL-P-55110: Printed Wiring Boards, Rigid General Specification for Performance

MIL-PRF-31032: Printed Circuit Board/Printed Wiring Board Manufacturing, General Specification

Materials

IPC-3406: Guidelines for Electrically Conductive Surface Mount Adhesive

IPC-3407: General Requirements for Isotropically Conductive Adhesives

IPC-3408: General Requirements for Anisotropically Conductive Adhesive Films

IPC-4101: Specification for Base Materials for Rigid and Multilayer Boards

IPC-4103: Specification for Plastic Substrates, Clad or Unclad, for High-Speed/High-Frequency Interconnection

IPC-4110: Specification and Characterization Methods for Nonwoven Cellulose Based Paper for Printed Boards

IPC-4121: Guidelines for Selecting Core Constructions for Multilayer Printed Wiring Board Applications

IPC-4130: Specification and Characterization Methods for Nonwoven “E” Glass Mat

IPC-4202: Flexible Base Dielectrics for Use in Flexible Printed Wiring

IPC-4203: Adhesive Coated Dielectric Films for Use as Cover Sheets

IPC-4204: Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry

IPC-4411: Specification and Characterization Methods for Nonwoven Para-Aramid Reinforcement

IPC-4412: Specification for Finished Fabric Woven form “E” Glass for Printed Boards

IPC-4552: Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

IPC-4553: Specification for Immersion Silver Plating for Printed Circuit Boards

IPC-4562: Metal Foil for Printed Wiring Applications

IPC-CC-830A: Qualification and Performance of Electrical Insulation Compounds for Printed Board Assemblies

IPC-CF-148: Resin Coated Metal for Multilayer Printed Boards

IPC-CF-152A: Metallic Foil Specification for Copper/Invar/Copper (CIC) for Printed Wiring and Other Related Applications

IPC/JPCA-4104: Specification for High-Density Interconnect (HDI) and Microvia Materials

IPC-SM-840C: Qualification and Performance of Permanent Solder Mask for Printed Boards

J-STD-004: Requirements for Soldering Fluxes

J-STD-005: General Requirements and Test Methods for Electronic Grade Solder Paste

J-STD-006: General Requirements and Test Methods for Soft Solder Alloys and Fluxed and Non Fluxed Solid Solders for Electronic Soldering Applications

DESIGN ACTIVITIES

IPC-1902: Grid Systems for Printed Circuits (equivalent to IEC 60097)

IPC-2141: Controlled Impedance Circuit Boards and High-Speed Logic Design

IPC-2221: Generic Standard on Printed Board Design

IPC-2222: Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223: Sectional Design Standard for Flexible Printed Boards

IPC-2224: Sectional Standard for Design of PWBs for PC Cards

IPC-2225: Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

IPC-2226: Design Standard for High-Density Array or Peripheral Leaded Component Mounting Structures

IPC-2251: Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

IPC-2252: Design and Manufacturing Guide for RF/Microwave Circuit Boards

IPC-2615: Printed Board Dimensions and Tolerances

IPC-7351: Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525: Guidelines for Stencil Design

IPC-7530: Guidelines for Temperature Profiling for Mass Soldering (Wave and Reflow) Processes

IPC-C-406: Design and Application Guidelines for Surface Mount Connectors

IPC-D-279: Reliability Design Guidelines for Surface Mount Technology Printed Board Assemblies

IPC/JPCA-2315: Design Guide for High-Density Interconnects (HDI) and Microvia

JPCA DG-01: Multilayer Printed Wiring Board Design Guide

JPCA DG-02: Double-Sided and Single-Sided Design Guide Manual, Flexible Printed Wiring Board

JPCA DG-04: Flexible Printed Wiring Boards and Material for Flexible Printed Wiring Boards Integrated Standard

J-STD-026: Semiconductor Design Standard for Flip Chip Applications

J-STD-027: Mechanical Outline Standard for Flip Chip or Chip Scale Configurations

COMPONENT MOUNTING

EIA-CB-11: Guidelines for the Surface Mounting of Multilayer Ceramic Chip Capacitors

IPC-4104: Specification for High-Density Interconnect (HDI) and Microvia Materials

IPC-6016: Qualification and Performance Specification for High-Density Interconnect (HDI) Layers or Boards

IPC-7093: Design and Assembly Process Implementation for Bottom Termination Components

IPC-7094: Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7095: Design and Assembly Process Implementation for BGAs

IPC-CM-770D: Guidelines for Printed Board Component Mounting

IPC/JPCA-2315: Design Guide for High-Density Interconnects (HDI) and Microvias

IPC-MC-790: Guidelines for Multichip Module Technology Utilization

IPC-SM-780: Electronic Component Packaging and Interconnection with Emphasis on Surface Mounting

IPC-SM-784: Guidelines for Direct Chip Attachment

J-STD-032: Performance Standard for Ball Grid Array Bumps and Columns

SOLDERING AND SOLDERABILITY

EIA-448-19: Method 19: Test Standard for Electromechanical Components, Environmental Effects of Machine Soldering Using a Vapor Phase System

EIA-534: Applications Guide, Soldering and Solderability Maintenance of Leaded Electronic Components

EIA-638: Surface Mount Solderability Test

EIA/IS-46: Test Procedure for Resistance to Soldering (Vapor Phase Technique) for Surface Mount Devices

EIA/IS-86: Surface Mount Solderability Test

EIA SP 3408: Surface Mount Solderability Test

IPC-AJ-820: Assembly and Joining Handbook

IPC-HDBK-001: Handbook and Guide to the Requirements for Soldered Electrical and Electronic Assemblies

IPC-S-816: Troubleshooting for Surface Mount Soldering

IPC-TR-460A: Troubleshooting Checklist for Wave Soldering Printed Wiring Boards

IPC-TR-462: Solderability Evaluation of Printed Boards with Protective Coatings over Long-Term Storage

IPC-TR-464: Accelerated Aging for Solderability Evaluations

JESD22: B102C Solderability Test Methods

J-STD-001: Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002: Solderability Tests for Component Leads, Terminations, Lugs, Terminals, and Wires

J-STD-003: Solderability Tests of Printed Boards

QUALITY ASSESSMENT

IPC-7912: Calculation of DPMO and Manufacturing Indices for Printed Wiring Assemblies

IPC-9191: General Guideline for Implementation of Statistical Process Control (SPC)

IPC-9194: Implementation of Statistical Process Control (SPC) Applied to Printed Board Assembly Manufacture Guideline

IPC-9199: SPC Quality Rating

IPC-9201: Surface Insulation Resistance Handbook

IPC-9251: Test Vehicles for Evaluating Fine Line Capability

IPC-9252: Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9261: In-Process DPMO and Estimated Yield for PWAs

IPC-A-20/21: Stencil Pattern for Solder Paste Slump Test

IPC-A-24: Flux/Board Interaction Board

IPC-A-36: CFC Cleaning Alternatives Artwork

IPC-A-38: Fine Line Round Robin Test Pattern

IPC-A-48: Surface Mount Airforce Mantech Artwork

IPC-A-600: Acceptability of Printed Boards

IPC-A-610: Acceptability of Printed Board Assemblies

IPC/JEDEC-033: Standard for Handling, Packing, Shipping and Use of Moisture Reflow Sensitive Surface Mount Devices

IPC/JEDEC J-STD-020: Moisture/Reflow Sensitivity Classification for Plastic Integrated Circuits Surface Mount Devices

IPC/JEDEC J-STD-035: Acoustic Microscopy for Nonhermetic Encapsulated Electronic Components

JEDEC JEP-150: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface Mount Components

JEDEC JEP-179: Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface Mount Components

JEDEC JESD-51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JEDEC JESD-51-5: Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

JEDEC JESD-51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

JEDEC JESD-51-9: Test Boards for Area Array Surface Mount Package Thermal Measurements

JEDEC JESD-51-10: Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements

JEDEC JESD 51-11 Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements

J-STD-028: Performance Standard for Flip Chip/Chip Scale Bumps

MIL-STD-883: Methods and Procedures for Microelectronics

SURFACE MOUNT PROCESS

IPC-5701: Users Guide for Cleanliness of Unpopulated Printed Boards

IPC-AC-62: Post Solder Aqueous Cleaning Handbook

IPC-CH-65: Guidelines for Cleaning of Printed Boards and Assemblies

IPC-SA-61: Post Solder Semi Aqueous Cleaning Handbook

IPC-SC-60: Post Solder Solvent Cleaning Handbook

RELIABILITY

IPC-9151: Printed Board Capability, Quality and Relative Reliability ($PCQR^2$) Benchmark Test Standard and Database

IPC-D-279: Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-SM-785: Guidelines for Accelerated Surface Mount Attachment Reliability Testing

JEDEC JESD 22-A113: Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing

JEDEC JESD 22-B113: Board Level Cyclic Bend Test Method for Interconnect Reliability Characterization of Components for Handheld Electronic Products

DATA TRANSFER STANDARDS

EIA-267-C: Axis and Motion Nomenclature for Numerically Controlled Machines

EIA-274-D: Interchangeable Variable Block Data Contouring, Format for Positioning and Contouring/Positioning Numerically Controlled Machines

EIA-358-C: ANSI X3.4 American National Standard Code for Information Interchange for Numerical Machine Control Perforated Tape

EIA-408: Interface between Numerical Control Equipment on Data Terminal Equipment Employing Parallel Binary Data Interchange

EIA-431: Electrical Interface between Numerical Control and Machine Tools

EIA-441: Operator Interface Function of Numerical Controls

EIA-484-A: Electrical and Mechanical Interface Characteristics and Line Control Protocol Using Communication Control Characters for Serial Data Link between a Direct Numerical Control System and Numerical Control Equipment Employing Asynchronous Full Duplex Transmission

EIA-494-B: 32 Bit Binary CL (BCL) and 7 Bit ASCII CL (ACL) Exchange Input Format for Numerically Controlled Machines

IPC-2511: Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology

IPC-2512: Sectional Requirements for Implementation of Administrative Methods for Manufacturing Data Description

IPC-2513: Sectional Requirements for Implementation of Drawing Methods for Manufacturing Data Description

IPC-2514: Sectional Requirements for Implementation of Printed Board Manufacturing Data Description

IPC-2515: Sectional Requirements for Implementation of Bare Board Product Electrical Testing Data Description

IPC-2516: Sectional Requirements for Implementation of Assembled Board Product Manufacturing Data Description

IPC-2517: Sectional Requirements for Implementation of Assembly Circuit Testing Data Description

IPC-2518: Sectional Requirements for Implementation of Bill of Material Product Data Description

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

TEST METHODS

EIA-469-C: Standard Test Method for Destructive Physical Analysis of High Reliability Ceramic Monolithic Capacitors

EIA-638: Surface Mount Solderability Test

EIA/IS-722: Fixed Capacitors for Use in Electronic Equipment; Part 1: Generic specification

EIA IS 46: Test Procedure for Resistance to Soldering (Vapor Phase Technique) for Surface Mount Devices

IPC-9501: PWB Assembly Process Simulation for Evaluation of Electronic Components

IPC-9502: PWB Assembly Soldering Process Guidelines for Non-IC Electronic Components

IPC-9503: Moisture Sensitivity Classification for Non-IC Components

IPC-9504: Assembly Process Simulation for Evaluation of Non-IC Components

IPC-9701: Qualification and Performance Test Methods for Surface Mount Solder Attachments

IPC-9850: Surface Mount Equipment Performance Characterization

IPC/JEDEC-9702: Monotonic Bend Characterization of Board-Level Interconnects

IPC/JPCA-6801: Terms & Definitions, Test Methods, and Design Examples for Build-Up/High-Density Interconnection

IPC-TM-650: Test Methods Manual

JEDEC JESD 22-A111: Evaluation Procedure for Determining Capability to Bottom Side Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices

JEDEC JESD 22-A112: Test Method A112, Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices

JEDEC JESD 22-B105-B: Test Method Lead Integrity

JEDEC JESD 22-B106: Test Method B106c, Resistance to Soldering Temperature for Through-Hole Mounted Devices

JEDEC JESD 22-B108: Coplanarity Test for Surface Mount Semiconductor Devices

JEDEC JESD 22-B117: BGA Ball Shear

JEDEC JESD 51-8: Integrated Circuit Thermal Test Method Environmental Conditions Junction-to-Board

JEDEC Standard 22 Series: Test Methods

REPAIR

IPC-7711A/7721A: Rework, Repair and Modification of Electronic Assemblies

TERMS AND DEFINITIONS

IPC-T-50F: Terms and Definitions for Interconnecting and Packaging Electronic Circuits

JEDEC JEP 99: Glossary of Microelectronic Terms, Definitions, Symbology

JEDEC JESD 12-1: Terms and Definitions for Gate Arrays and Cell-Based Integrated Circuits

JEDEC JESD 77: Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices

JEDEC JESD 99: Terms, Definitions, and Letter Symbols for Microelectronic Devices

JEDEC JESD 100: Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits

HOW TO OBTAIN THESE DOCUMENTS

Following are the addresses of the IPC and ECIA, as well as other sources for documents shown in this SMT listing:

IPC—Association Connecting Electronics Industries

3000 Lakeside Drive #309S

Bannockburn, IL 60015

Phone: (847) 615-7100

Electronic Components Industry Association (ECIA)

1111 Alderman Drive, Suite 400

Alpharetta, GA 30005
Phone: (678) 393-9998

JEDEC
3103 North 10th Street, Suite 240-S
Arlington, VA 22201-2017
Phone: (703) 624-9230

Global Engineering Documents
15 Inverness Way
East Englewood, CO 80112
Phone: (800) 854-7179

Military documents are available from the following address:

Standardization Documents Order Desk
Building 4D, 700 Robbins Avenue
Philadelphia, PA 19111-5094

Central office address of the IEC is as follows:

International Electrotechnical Commission (IEC)
3 Rue de Varembe
1211 Geneva 20, Switzerland

IEC documents are available from the following address:

American National Standards Institute (ANSI)
11 West 42nd Street
New York, NY 10036

GLOSSARY[a]

ACCELERATOR: A chemical that is used to speed up a reaction or cure, as cobalt naphthenate is used to accelerate the reaction of certain polyester resins. It is often used along with a catalyst, hardener, or curing agent. The term “accelerator” is often used interchangeably with the term “promoter.”

ACCURACY: The ability to place the hole at the targeted location.

ADDITIVE PROCESS: A process for obtaining conductive patterns by the selective deposition of conductive material on an unclad base material.

ADHESIVE: Broadly, any substance used in promoting and maintaining a bond between two materials.

AGING: The change in properties of a material with time under specific conditions.

ANNULAR RING: The circular strip of conductive material that completely surrounds a hole.

ARC RESISTANCE: The time required for an arc to establish a conductive path in a material.

ARTWORK MASTER: An accurately scaled configuration used to produce the production master.

BACKUP MATERIAL: A material placed on the bottom of a laminate stack in which the drill terminates its drilling stroke.

BASE MATERIAL: The insulating material upon which the printed wiring pattern may be formed.

BASE MATERIAL THICKNESS: The thickness of the base material excluding metal foil cladding or material deposited on the surface.

BLIND VIA: Conductive surface hole that connects an outerlayer with an innerlayer of a multilayer PWB without penetrating the entire board.

BLISTERING: Localized swelling and separation between any of the layers of the base laminate or between the laminate and the metal cladding.

BONDING LAYER: An adhesive layer used in bonding other discrete layers during lamination.

BOND STRENGTH: The force per unit area required to separate two adjacent layers by a force perpendicular to the board surface; usually refers to the interface between copper and base material.

BOW: A laminate defect in which deviation from planarity results in a smooth arc.

B-STAGE: An intermediate stage in the curing of a thermosetting resin. In it a resin can be heated and caused to flow, thereby allowing final curing in the desired shape.

B-STAGE LOT: The product from a single mix of B-stage ingredients.

B-STAGE RESIN: A resin in an intermediate stage of a thermosetting reaction. The material softens when heated and swells when in contact with certain liquids, but it may not entirely fuse or dissolve.

BURIED VIA: Conductive surface hole that connects one innerlayer to another innerlayer of a multilayer PWB without having a direct connection to either the top or bottom surface layer.

BURR: A ridge left on the outside copper surfaces after drilling.

CAPACITANCE: The property of a system of conductors and dielectrics which permits the storage of electricity when

potential difference exists between the conductors.

CAPACITIVE COUPLING: The electrical interaction between two conductors caused by the capacitance between the conductors.

CARBIDE: Tungsten carbide, formula WC. The hard, refractory material forming the drill bits used in PWB drillings.

CATALYST: A chemical that causes or speeds up the cure of a resin but does not become a chemical part of the final product.

CERAMIC LEADED CHIP CARRIER (CLCC): A chip carrier made from ceramic (usually a 90 to 96 percent alumina or beryllia base) and with compliant leads for terminations.

CHIP CARRIER (CC): An integrated circuit package, usually square, with a chip cavity in the center; its connections are usually on all four sides. (See *leaded chip carrier* and *leadless chip carrier*.)

CHIP LOAD (CL): The movement of the drill downward per revolution; usually given in mils (thousandths of an inch) per revolution.

CHLORINATED HYDROCARBON: An organic compound having chlorine atoms in its chemical structure. Trichloroethylene, methyl chloroform, and methylene chloride are chlorinated hydrocarbons.

CIRCUIT: The interconnection of a number of electrical devices in one or more closed paths to perform a desired electrical or electronic function.

CLAD: A condition of the base material, to which a relatively thin layer or sheet of metal foil (cladding) has been bonded on one or both of its sides. The result is called a metal-clad base material.

CNC: Computer numerically controlled. Refers to a machine with a computer which stores the numerical information about location, drill size, and machine parameters, regulating the machine to carry out that information.

COAT: To cover with a finishing, protecting, or enclosing layer of any compound.

COLD FLOW: The continuing dimensional change that follows initial instantaneous deformation in a nonrigid material under static load. Also called creep.

COLLIMATION: The degree of parallelism of light rays from a given source. A light source with good collimation produces parallel light rays, whereas a poor light source produces divergent, nonparallel light rays.

COMPONENT HOLE: A hole used for the attachment and electrical connection of a component termination, including pin or wire, to the printed board.

COMPONENT SIDE: The side of the printed board on which most of the components will be mounted.

COMPOUND: A combination of elements in a stable molecular arrangement.

CONDUCTIVE FOIL: The conductive material that covers one side or both sides of the base material and is intended for forming the conductive pattern.

CONDUCTIVE PATTERN: The configuration or design of the electrically conductive material on the base material.

CONDUCTOR LAYER 1: The first layer having a conductive pattern, of a multilayer board, on or adjacent to the component side of the board.

CONDUCTOR SPACING: The distance between adjacent edges (not centerline to centerline) of conductors on a single layer of a printed board.

CONDUCTOR THICKNESS: The thickness of the copper conductor exclusive of coatings or other metals.

CONDUCTOR WIDTH: The width of the conductor viewed from vertically above, that is, perpendicularly to the printed board.

CONFORMAL COATING: An insulating protective coating which conforms to the configuration of the object coated and is applied on the completed printed board assembly.

CONNECTOR AREA: The portion of the printed board that is used for providing external (input–output) electrical connections.

CONTACT BONDING ADHESIVE: An adhesive (particularly of the nonvulcanizing natural rubber type) that bonds to itself on contact, although solvent evaporation has left it dry to the touch.

CONTROLLED IMPEDANCE: The matching of substrate material properties with trace dimensions and locations to create a specific electric impedance as seen by a signal on the trace.

COPOLYMER: See *polymer*.

CORE MATERIAL: The fully cured inner-layer segments, with circuiting on one or both sides, that form the multilayer circuit.

CORNER MARKS: The marks at the corners of printed board artwork, the inside edges of which usually locate the borders and establish the contour of the board.

COUPON: One of the patterns of the quality conformance test circuitry area. (See *test coupon*.)

CRAZING: A base material condition in which connected white spots or crosses appear on or below the surface of the base material. They are due to the separation of fibers in the glass cloth and connecting weave intersections.

CROSS-LINKING: The forming of chemical links between reactive atoms in the molecular chain of a plastic. It is cross-linking in the thermosetting resins that makes the resins infusible.

CROSS TALK: Undesirable electrical interference caused by the coupling of energy between signal paths.

CRYSTALLINE MELTING POINT: The temperature at which the crystalline structure in a material is broken down.

CTE: Coefficient of thermal expansion. The measure of the amount a material changes in any axis per degree of temperature change.

CURE: To change the physical properties of a material (usually from a liquid to a solid) by chemical reaction or by the action of heat and catalysts, alone or in combination, with or without pressure.

CURING AGENT: See *hardener*.

CURING TEMPERATURE: The temperature at which a material is subjected to curing.

CURING TIME: In the molding of thermosetting plastics, the time in which the material is properly cured.

CURRENT-CARRYING CAPACITY: Maximum current which can be carried continuously without causing objectionable degradation of electrical or mechanical properties of the printed board.

DATUM REFERENCE: A defined point, line, or plane used to locate the pattern or layer of a printed board for manufacturing and/or inspection purposes.

DEBRIS: A mechanically bonded deposit of copper to substrate hole surfaces.

DEBRIS PACK: Debris deposited in cavities or voids in the resin.

DEFINITION: The fidelity of reproduction of the printed board conductive pattern relative to the production master.

DELAMINATION: A separation between any of the layers of the base laminate or between the laminate and the metal cladding originating from or extending to the edges of a hole or edge of the board.

DIELECTRIC CONSTANT: The property of a dielectric which determines the electrostatic energy stored per unit volume for a unit potential gradient.

DIELECTRIC LOSS: Electric energy transformed into heat in a dielectric subjected to a changing electric field.

DIELECTRIC LOSS ANGLE: The difference between 90° and the dielectric phase angle. Also called the dielectric phase difference.

DIELECTRIC LOSS FACTOR: The product of dielectric constant and the tangent of dielectric loss angle for a material.

DIELECTRIC PHASE ANGLE: The angular difference in phase between the sinusoidal alternating potential difference applied to a dielectric and the component of the resulting alternating current having the same period as the potential difference.

DIELECTRIC POWER FACTOR: The cosine of the dielectric phase angle (or sine of the dielectric loss angle).

DIELECTRIC STRENGTH: The voltage that an insulating material can withstand before breakdown occurs, usually expressed as a voltage gradient (such as volts per mil).

DIMENSIONAL STABILITY: Freedom from distortion by such factors as temperature changes, humidity changes, age, handling, and stress.

DIRECT IMAGING: The exposure of photo resist material with a laser without the use of positive or negative photo tool.

DISSIPATION FACTOR: The tangent of the loss angle of the insulating material. Also called loss tangent or approximate power factor.

DRILL FACET: The surface formed by the primary and secondary relief angles of a drill tip.

DRILL WANDER: The sum of accuracy and precision deviations from the targeted location of the hole.

DUMMY: A cathode with a large area used in a low-current-density pulsating operation for the removal of metallic impurities from solution. The process is called “dummying.”

DWELL POINT: The bottom of the drilling stroke before the drill bit ascends.

EDGE-BOARD CONTACTS: A series of contacts printed on or near an edge of a printed board and intended for mating with a one-part edge connector.

EDX: Energy dispersive x-ray fluorescent spectrometer

ELASTOMER: A material which at room temperature stretches under low stress to at least twice its length but snaps back to its original length upon release of the stress. Rubber is a natural elastomer.

ELECTRIC STRENGTH: The maximum potential gradient that a material can withstand without rupture. It is a function of the thickness of the material and the method and conditions of test. Also called dielectric strength or disruptive gradient.

ELECTROLESS PLATING: The controlled autocatalytic reduction of a metal ion on certain catalytic surfaces.

EMULSION SIDE: The side of the film or glass on which the photographic image is present.

ENTRY MATERIAL: A material placed on top of a laminate stack.

EPOXY SMEAR: Epoxy resin which has been deposited on edges of copper in holes during drilling either as a uniform coating or as scattered patches. It is undesirable because it can electrically isolate the conductive layers from the plated-through-hole interconnections.

ETCHBACK: The controlled removal of all the components of the base material by a chemical process acting on the sidewalls of plated-through holes to expose additional internal conductor areas.

ETCH FACTOR: The ratio of the depth of etch to lateral etch.

EXOTHERM: A characteristic curve which shows heat of reaction of a resin during cure (temperature) versus time. The peak exotherm is the maximum temperature on the curve.

EXOTHERMIC REACTION: A chemical reaction in which heat is given off.

FIBER EXPOSURE: A condition in which glass cloth fibers are exposed on machined or abraded areas.

FILLER: A material, usually inert, added to a plastic to reduce cost or modify physical properties.

FILM ADHESIVE: A thin layer of dried adhesive. Also, a class of adhesives provided in dry-film form with or without reinforcing fabric and cured by heat and pressure.

FLEXURAL MODULUS: The ratio, within the elastic limit, of stress to corresponding strain. It is calculated by drawing a tangent to the steepest initial straight-line portion of the load deformation curve and using the equation $EB = L3m/4bd3$, where EB is the modulus, L is the span (in inches), m is the slope of the tangent, b is the width of beam tested, and d is the depth of the beam.

FLEXURAL STRENGTH: The strength of a material subjected to bending. It is expressed as the tensile stress of the outermost fibers of a bent test sample at the instant of failure.

FLUOROCARBON: An organic compound having fluorine atoms in its chemical structure, an inclusion that usually lends stability to plastics. Teflon[b] is a fluorocarbon.

GEL: The soft, rubbery mass that is formed as a thermosetting resin goes from a fluid to an infusible solid. It is an intermediate state in a curing reaction, and a stage in which the resin is mechanically very weak.

GEL POINT: The point at which gelation begins.

GLASS TRANSITION POINT: The temperature at which a material loses properties and becomes a semiliquid.

GLASS TRANSITION TEMPERATURE: The temperature at which epoxy, for example, softens and begins to expand independently of the glass fabric expansion rate, usually symbolized as T_g.

GLUE-LINE THICKNESS: Thickness of the fully dried adhesive layer.

GRID: An orthogonal network of two sets of parallel lines for positioning features on a printed board.

GROUND PLANE: A conducting surface used as a common reference point for circuit returns, shielding, or heat

sinking.

GULL WING LEAD: A surface mounted device lead which flares outward from the device body.

HALOING: A light area around holes or other machined areas on or below the surface of the base laminate.

HARDENER: A chemical added to a thermosetting resin for the purpose of causing curing or hardening. A hardener, such as an amine or acid anhydride for an epoxy resin, is a part of the chemical reaction and a part of the chemical composition of the cured resin. The terms “hardener” and “curing agent” are used interchangeably.

HEAT-DISTORTION POINT: The temperature at which a standard test bar (ASTM D 648) deflects 0.010 in under a stated load of either 66 or 264 psi.

HIGH-DENSITY INTERCONNECT (HDI): Ultrafine-geometry multilayer PWB constructed with conductive surface microvia connections between layers. (Microvia is usually defined as a hole with a diameter less than 0.006 in.) These boards also usually include buried and/or blind vias and are made by sequential build-up lamination.

HOLE PULL STRENGTH: The force, in pounds, necessary to rupture a plated-through hole or its surface terminal pads when loaded or pulled in the direction of the axis of the hole. The pull is usually applied to a wire soldered in the hole, and the rate of pull is given in inches per minute.

HOOK: A geometric drill bit defect of the cutting edges.

HOT-MELT ADHESIVE: A thermoplastic adhesive compound, usually solid at room temperature, which is heated to fluid state for application.

HYDROCARBON: An organic compound containing only carbon and hydrogen atoms in its chemical structure.

HYDROLYSIS: The chemical decomposition of a substance involving the addition of water.

HYGROSCOPIC: Tending to absorb moisture.

I-LEAD: A surface mounted device lead which is formed such that the end of the lead contacts the board land pattern at a 90° angle. Also called a butt joint.

IMPREGNATE: To force resin into every interstice of a part, as of a cloth for laminating.

INHIBITOR: A chemical that is added to a resin to slow down the curing reaction and is normally added to prolong the storage life of a thermosetting resin.

INORGANIC CHEMICALS: Chemicals whose molecular structures are based on other than carbon atoms.

INSULATION RESISTANCE: The electrical resistance of the insulating material between any pair of contacts, conductors, or grounding devices in various combinations.

INTERNAL LAYER: A conductive pattern contained entirely within a multilayer board. IPC: Institute for Interconnecting and Packaging Electronic Circuits. A leading printed wiring industry association that develops and distributes standards as well as other information of value to printed wiring designers, users, suppliers, and fabricators. IR: Infrared heating for solder-reflow operation.

J-LEAD: A surface mounted device lead which is formed into a “J” pattern folding under the device body.

JUMPER: An electrical connection between two points on a printed board added after the printed wiring is fabricated.

KIRKENDALL VOIDS: In Cu-Au or Cu-Au-Sn systems, pores in the older joint, or at copper interfaces occur through solid-state diffusion. Copper which has a relatively high solubility and solid-state mobility in gold diffuses into the gold. Transported by grain boundry diffusion at temperatures below 150°C, and by bulk diffusion above that temperature. Au-Sn regions result along with atomic vacancies. Then lattice vacancies are in profusion. Pours (voids) can be observed and this material depletion weakens the solder joint.

LAMINATE: The plastic material, usually reinforced by glass or paper, that supports the copper cladding from which circuit traces are created.

LAMINATE VOID: Absence of epoxy resin in any cross-sectional area which should normally contain epoxy resin.

LAND: See *terminal area*.

LANDLESS HOLE: A plated-through hole without a terminal area.

LASER PHOTOPLOTTER (LASER PHOTO GENERATOR, OR LPG): A device that exposes photosensitive material, usually a silver halide or diazo material, subsequently used as the master for creating the circuit image in production.

LAYBACK: A geometric drill bit defect of the cutting edges.

LAYER-TO-LAYER SPACING: The thickness of dielectric material between adjacent layers of conductive circuitry.

LAY-UP: The process of registering and stacking layers of a multilayer board in preparation for the laminating cycle.

LCCC: Leadless ceramic chip carrier.

LEADED CHIP CARRIER: A chip carrier (either plastic or ceramic) with compliant leads from terminations.

LEAD-FREE: Referring to solder alloys made without lead, to conform with the requirements of the European Union directive on the Restriction of Hazardous Substances (RoHS), the most important of which, to the printed circuit industry, is lead. Often used to refer to any process that is designed to be compatible with “lead-free” alloys.

LEADLESS CHIP CARRIER: A chip carrier (usually ceramic) with integral metallized terminations and no compliant external leads.

LEGEND: A format of lettering or symbols on the printed board, for example, part number, component locations, or patterns.

LOOSE FIBERS: Supporting fibers in the substrate of the laminate which are not held in place by surrounding resin.

MAJOR WEAVE DIRECTION: The continuous-length direction of a roll of woven glass fabric.

MARGIN RELIEF: The area of a drill bit next to the cutting edge is removed so that it does not rub against the hole as the drill revolves.

MASTER DRAWING: A document that shows the dimensional limits or grid locations applicable to any or all parts of a printed wiring or printed circuit base. It includes the arrangement of conductive or nonconductive patterns or elements; size, type, and location of holes; and any other information necessary to characterize the complete fabricated product.

MEASLING: Discrete white spots or crosses below the surface of the base laminate that reflect a separation of fibers in the glass cloth at the weave intersection.

MICROSTRIP: A type of transmission line configuration which consists of a conductor over a parallel ground plane separated by a dielectric.

MICROVIA: Usually defined as a conductive hole with a diameter of 0.006 in or less that connects layers of a multilayer PWB. Often used to refer to any small-geometry connecting hole the creation of which is beyond the practical capabilities of traditional mechanical drilling processes.

MINOR WEAVE DIRECTION: The width direction of a roll of woven glass fabric.

MIXED ASSEMBLY: A printed wiring assembly that combines through-hole components and surface mounted components on the same board.

MODULUS OF ELASTICITY: The ratio of stress to strain in a material that is elastically deformed.

MOISTURE RESISTANCE: The ability of a material not to absorb moisture either from air or when immersed in water.

MOUNTING HOLE: A hole used for the mechanical mounting of a printed board or for the mechanical attachment of

components to a printed board.

MULTILAYER BOARD: A product consisting of layers of electrical conductors separated from each other by insulating supports and fabricated into a solid mass. Interlayer connections are used to establish continuity between various conductor patterns.

MULTIPLE-IMAGE PRODUCTION MASTER: A production master used to produce two or more products simultaneously.

NAILHEADING: A flared condition of internal conductors.

NC: Numerically controlled. Usually refers to a machine tool, in this case a drilling machine. The most basic type is one in which a mechanical guide locates the positions of the holes. NC machines are usually controlled by punched tape.

NEMA STANDARDS: Property values adopted as standard by the National Electrical Manufacturers Association.

NOBLE ELEMENTS: Elements that either do not oxidize or oxidize with difficulty; examples are gold and platinum.

OILCANNING: The movement of entry material in the *z* direction during drilling in concert with the movement of the pressure foot.

ORGANIC: Composed of matter originating in plant or animal life or composed of chemicals of hydrocarbon origin, either natural or synthetic.

PAD: See *terminal area*.

PADS ONLY: A multilayer construction with all circuit traces on inner layers and the component terminal area only on the surface of the board. This construction adds two layers but may avoid the need for a subsequent solder resist, and since inner layers usually are easier to form, this construction may lead to higher overall yields. PH: A measure of the acid or alkaline condition of a solution. A pH of 7 is neutral (distilled water); pH values below 7 represent increasing acidity as they go toward 0; and pH

values above 7 represent increasing alkalinity as they go toward the maximum value of 14.

PHOTOMASTER: An accurately scaled copy of the artwork master used in the photo fabrication cycle to facilitate photo processing steps.

PHOTOPOLYMER: A polymer that changes characteristics when exposed to light of a given frequency.

PINHOLES: Small imperfections which penetrate entirely through the conductor.

PINK RING: The appearance of a halo of copper around the hole of a multilayer.

PLASTICIZER: Material added to resins to make them softer and more flexible when cured.

PLASTIC LEADED CHIP CARRIER (PLCC): A chip carrier packaged in plastic, usually terminating in compliant leads (originally "J" style) on all four sides.

PLATED-THROUGH HOLE: A hole in which electrical connection is made between printed wiring board layers with conductive patterns by the deposition of metal on the wall of the hole. (See *PTH*.)

PLATING VOID: The area of absence of a specific metal from a specific cross-sectional area: (1) When the plated-through hole is viewed as cross-sectioned through the vertical plane, it is a product of the average thickness of the plated metal times the thickness of the board itself as measured from the outermost surfaces of the base copper on external layers. (2) When the plated-through hole is viewed as cross-sectioned through the horizontal plane (annular method), it is the difference between the area of the hole and the area of the outside diameter of the through-hole plating.

PLOWING: Furrows in the hole wall due to drilling.

POLYMER: A high-molecular-weight compound made up of repeated small chemical units. For practical purposes, a polymer is a plastic. The small chemical unit is called a

mer, and when the polymer or mer is cross-linked between different chemical units (e.g., styrene-polyester), the polymer is called a copolymer. A monomer is any single chemical from which the mer or polymer or copolymer is formed.

POLYMERIZE: To unite chemically two or more monomers or polymers of the same kind to form a molecule with higher molecular weight.

POTLIFE: The time during which a liquid resin remains workable as a liquid after catalysts, curing agents, promoter, etc. are added. It is roughly equivalent to gel time.

POWER FACTOR: The cosine of the angle between the applied voltage and the resulting current.

PRECISION: The ability to repeatedly place the hole at any location.

PREPRODUCTION TEST BOARD: A test board (as detailed in IPC-ML-950) the purpose of which is to determine whether, prior to the production of finished boards, the contractor has the capability of producing a multilayer board satisfactorily.

PRESS PLATEN: The flat heated surface of the lamination press used to transmit heat and pressure to lamination fixtures and into the lay-up.

PRESSURE FOOT: The tube like device on the drilling machine that descends to the top surface of the stack, holding it firmly down, before the drill descends through the center of the pressure foot. The vacuum system of the drilling machine separates through the pressure foot to remove chips and dust formed in drilling.

PRINTED WIRING ASSEMBLY DRAWING: A document that shows the printed wiring base, the separately manufactured components which are to be added to the base, and any other information necessary to describe the joining of the parts to perform a specific function.

PRINTED WIRING LAYOUT: A sketch that depicts the printed wiring substrate, the physical size and location of electronic and mechanical components, and the routing of conductors that interconnect the electronic parts in sufficient detail to allow for the preparation of documentation and artwork.

PRODUCTION MASTER: A 1:1 scale pattern used to produce one or more printed wiring or printed circuit products within the accuracy specified on the master drawing.

PROMOTER: A chemical, itself a feeble catalyst, that greatly increases the activity of a given catalyst.

PTH: Plated-through holes. Also refers to the technology that uses the plated-through hole as its foundation.

QUADPACK: Generic term for surface mount technology packages with leads on all four sides. Commonly used to describe chip carrier-like devices with gull wing leads.

QUALITY CONFORMANCE CIRCUITRY AREA: A test board made as an integral part of the multilayer printed board panel on which electrical and environmental tests may be made for evaluation without destroying the basic board.

RAW MATERIAL PANEL SIZE: A standard panel size related to machine capacities, raw material sheet sizes, final product size, and other factors.

REGISTER MARK: A mark used to establish the relative position of one or more printed wiring patterns, or portions thereof, with respect to desired locations on the opposite side of the board.

REGISTRATION: The relative position of one or more printed wiring patterns, or portions thereof, with respect to desired locations on a printed wiring base or to another pattern on the opposite side of the base.

REPAIR: The correction of a printed wiring defect after the completion of board fabrication to render the board as functionally good as a perfect board.

RESIN: High-molecular-weight organic material with no sharp melting point. For current purposes, the term “resin,” “polymer,” and “plastic” can be used interchangeably.

RESIST: A protective coating (ink, paint, metallic plating, etc.) used to shield desired portions of the printed conductive pattern from the action of etchant, solder, or plating.

RESISTIVITY: The ability of a material to resist passage of electric current through its bulk or on a surface.

RIFLING: Spiral groove or ridge in the substrate due to drilling.

RIGID/FLEX: A PWB construction combining flexible circuits and rigid multilayer PWBs, usually either to provide a built-in connection or to make a three-dimensional form that includes components.

ROCKWELL HARDNESS NUMBER: A number derived from the net increase in depth of an impression as the load on a perpetrator is increased from a fixed minimum load to as higher load and then returned to minimum load.

RoHS: Acronym for “Restriction of Hazardous Substances.” The name given to a directive of the European Union meant to reduce certain materials considered detrimental to the environment.

ROUGHNESS: Irregular, coarse, uneven hole wall on copper or substrate due to drilling.

SCHEMATIC DIAGRAM: A drawing which shows, by means of graphic symbols, the electrical interconnections and functions of a specific circuit arrangement.

SEM: Scanning electron microscope.

SEQUENTIAL BUILD-UP: A process for making multilayer PWBs in which already finished multilayers are laminated together to form a higher-layer-count final board, or in which additional outerlayers are added to finished multilayer PWBs.

SHADOWING: Etchback to maximum limit without removal of dielectric material from conductors.

SINGLE-IN-LINE PACKAGE (SIP): Component package system with one line of connectors, usually spaced 0.100 in apart.

SMC: Surface mounted component. Component with terminations designed for mounting flush to printed wiring board.

SMD: Surface mounted device. Any component or hardware element designed to be mounted to a printed wiring board without penetrating the board.

SMEAR: Fused deposit left on copper or substrate from excessive drilling heat.

SMOBC: Solder mask over bare copper. A method of fabricating a printed wiring board which results in the final metallization being copper with no other protective metal; but the nonsoldered areas are coated by a solder resist, exposing only the component terminal areas. This eliminates tin-lead under the solder mask.

SMT: Surface mount technology. Defines the entire body of processes and components which create printed wiring assemblies without components with leads that pierce the board. Sn-Au-Cu: An alloy used as a replacement for eutectic tin-lead (Sn-Pb) in “lead-free” solders (often referred to, and pronounced as “snack”).

SOI: SOIC package with J-leads rather than gull wing leads.

SOIC: Small-outline integrated circuit. A plastic package resembling a small dual-in-line package (DIP) with gull wing leads on two sides for surface mounting.

SOT: Small outline transistor. A package for surface-mounting transistors.

SPINDLE RUNOUT: The measure of the wobble present as the drilling machine spindle rotates 360°.

STORAGE LIFE: The period of time during which a liquid resin or adhesive can be stored and remain suitable for use. Also called shelf life.

STRAIN: The deformation resulting from a stress. It is measured by the ratio of the change to the total value of

the dimension in which the change occurred.

STRESS: The force producing or tending to produce deformation in a body. It is measured by the force applied per unit area.

SUBSTRATE: A material on whose surface an adhesive substance is spread for bonding or coating. Also, any material which provides a supporting surface for other materials used to support printed wiring patterns.

SURFACE RESISTIVITY: The resistance of a material between two opposite sides of a unit square of its surface. It may vary widely with the conditions of measurement.

SURFACE SPEED: The linear velocity of a point on the circumference of a drill. Given in units of surface feet per minute—sfm.

TERMINAL AREA: A portion of a conductive pattern usually, but not exclusively, used for the connection and/or attachment of components.

TEST COUPON: A sample or test pattern usually made as an integral part of the printed board, on which electrical, environmental, and micro sectioning tests may be made to evaluate board design or process control without destroying the basic board.

TETRA-ETCH[c]: A nonpyrophoric (will not ignite when exposed to moisture) proprietary etchant.

TETROFUNCTIONAL: Describes an epoxy system for laminates that has four cross-linked bonds rather than two and results in a higher glass transition temperature, or T_g.

T_g: Glass transition temperature. The temperature at which laminate mechanical properties change significantly.

THERMAL CONDUCTIVITY: The ability of a material to conduct heat; the physical constant for the quantity of heat that passes through a unit cube of a material in a unit of time when the difference in temperatures of two faces is 1°C.

THERMOPLASTIC: A classification of resin that can be readily softened and resoftened by repeated heating.

THERMOSETTING: A classification of resin which cures by chemical reaction when tested and, when cured, cannot be resoftened by heating.

THIEF: An auxiliary cathode so placed as to divert to itself some current from portions of the work which would otherwise receive too high a current density.

THIXOTROPIC: Said of materials that are gel-like at rest but fluid when agitated.

THROUGH-HOLE TECHNOLOGY: Traditional printed wiring fabrication where components are mounted in holes that pierce the board.

THROWING POWER: A measure of the degree of uniformity with which metal is deposited on an irregularly shaped cathode. Often refers to the ratio of amount of plated metal on the surface of a copper-clad board to the amount plated on a side of a hole through the same board.

TWIST: A laminate defect in which deviation from planarity results in a twisted arc.

UNDERCUT: The reduction of the cross-section of a metal foil conductor caused by the etchant removing metal from under the edge of the resist.

VAPOR PHASE: The solder-reflow process that uses a vaporized solvent as the source for heating the solder beyond its melting point, creating the component-to-board solder joint.

VIA: A metallized connecting hole that provides a conductive path from one layer in a printed wiring board to another. (1) *Buried via*—connects one inner layer to another inner layer without penetrating the surface. (2) *Blind via*—connects the surface layer of a printed wiring board to an internal layer without going all the way through the other surface layer.

VOID: A cavity left in the substrate.

VOLUME RESISTIVITY: The electrical resistance between opposite faces of a 1-cm cube of insulating materials, commonly expressed in ohm-centimeters. The recommended test is ASTMD 256 51T. Also called the specific insulation.

VULCANIZATION: A chemical reaction in which the physical properties of an elastomer are changed by causing the elastomer to react with sulfur or some other cross-linking agent.

WATER ABSORPTION: The ratio of the weight of water absorbed by a material to the weight of the dry material.

WEAVE EXPOSURE: A condition in which the unbroken woven glass cloth is not uniformly covered by resin.

WEAVE TEXTURE: A surface condition in which the unbroken fibers are completely covered with resin but exhibit the definite weave pattern of the glass cloth.

WETTING: Ability to adhere to a surface immediately upon contact.

WICKING: Migration of copper salts into the glass fibers of the insulating material.

WORKING LIFE: The period of time during which a liquid resin or adhesive, after mixing with catalyst, solvent, or other compounding ingredients, remains usable. (See *potlife*.)

[a] Some terms may not be included in the glossary as they are treated in detail in the text. Please also see the index and subject chapters.

[b] Trademark of E. I. du Pont de Nemours & Company.

[c] Trademark of W. L. Gore and Associates, Inc.

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